

The examination is being carried out on the **following application documents**

Description, Pages

1-35 as originally filed

Claims, Numbers

1-12 as originally filed

Drawings, Sheets

1/15-15/15 as originally filed

- 1 Claims 1, 6 and 7 contravene Art. 76 EPC as they introduce subject matter that extends beyond the application as original filed.

A feature in claim 1 recites "*at least one configurable data input buffer (₄₁₂) configurable to an n -bit width (D_n) where n is a non-zero integer, and further configurable to one of single data rate configuration and double data rate configuration*".

The description is however silent about such a buffer. It discloses a memory device comprising a data input buffer configurable in a high speed mode or parallel clock mode (paragraphs [0027] and [0031]) and a low speed mode or serial clock mode (paragraphs [0027] and [0035]). Furthermore, in both modes, "*each memory device operates at the double data rate, received data is buffered into an internal single data rate even data stream D_E and an internal single data rate odd data stream D_O* " (paragraphs [0033], [0036] and . fig. 3B, 3D). The original description thus even contradicts the above feature of claim 1.

Claim 1 therefore does not meet the requirements of Art. 76 EPC.

Dependent claim 6 recites "*a configuration register configured to store a configuration information indicating whether the configurable clock input buffer is configured as the single ended clock signaling configuration or the differential clock signaling configuration*." However the original description only refers to "a latch" (502 in fig. 6 and paragraphs [0049]-[0052]) storing the state of a MODE signal that is used for configuring the clock input buffer.

Claim 6 thus does not meet the requirements of Art. 76 EPC either.

Dependent claim 7 recites "*a configuration register configured to store the plurality of output buffer drive strengths to be utilized by the one or more configurable output buffers.*" However according to paragraph [0062], "*the output buffer drive strength can also be configured based on the MODE setting*", whose state is stored in latch 502, as explained above. The description is silent about storing drive strengths, and it is not understood how this would be possible with only latch 502.

Claim 7 thus does not meet the requirements of Art. 76 EPC either.

The scope of the search was therefore limited and the above aspects were not taken into consideration.

- 2 Reference is made to the following documents; the numbering will be adhered to in the rest of the procedure.

- D1 US 2004/148482 A1 (GRUNDY KEVIN P [US] ET AL) 29 July 2004 (2004-07-29)
- D2 US 2006/067123 A1 (JIGOUR ROBIN J [US] ET AL) 30 March 2006 (2006-03-30)
- D3 US 6 337 832 B1 (OOISHI TSUKASA [JP] ET AL) 8 January 2002 (2002-01-08)
- D4 US 2003/043684 A1 (JOHNSON CHRISTOPHER S [US] ET AL) 6 March 2003 (2003-03-06)
- D5 EP 0 818 734 A2 (FUJITSU LTD [JP]) 14 January 1998 (1998-01-14)

- 3 Furthermore, notwithstanding the above-mentioned lack of clarity, the subject-matter of claim 1 does not involve an inventive step within the meaning of Article 56 EPC, and the requirements of Article 52(1) EPC are therefore not met.

A set of technical features is regarded as a combination of features if the functional interaction between the features achieves a combined technical effect which is different from, e.g. greater than, the sum of the technical effects of the individual features. In other words, the interactions of the individual features must produce a synergistic effect. If no such synergistic effect exists, there is no more than a mere aggregation of features (see T 389/86, and T 204/06).

This is the case with the features of claim 1. They are not related and do not work together to produce any synergistic effect. For example, receiving a chip enable signal has not much to do with output buffers having a configurable drive strength.

Furthermore, all the features are known separately in the prior art.

Document D1 discloses a configurable non-volatile memory device (paragraph [0035]) comprising:

a plurality of non-volatile memory blocks (307 in fig. 17 and paragraph [0084]) ;
a first clock input port configured to receive a first clock input signal (a first input of differential receivers 310 in fig. 17 and paragraph [0088]) ;
a second clock input port configured to receive a second clock input signal (a second input of differential receivers 310 in fig. 17), the second clock input signal being complementary to the first clock input signal;
a clock output port configured to transfer a clock output signal (Clock out in fig. 17), wherein the clock output signal is referenced to the first clock input signal;
at least one configurable data input buffer configurable to an n-bit width (paragraph [0105]) where n is a non-zero integer, the configurable data interface configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of non-volatile memory blocks.

Document D1 is silent about the remaining features of claim 1.

(a) a chip enable port configured to receive a chip enable signal (CE#) for enabling the configurable non-volatile memory device;

(b) a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and the second clock input signal as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal and the second clock input signal as a single ended signal; and

(c) one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks.

Feature (a) is known from document D2 which discloses a configurable non-volatile memory device (fig. 6) having input buffers with a configurable width and receiving clock and chip enable signals (CLK and CS in fig. 9).

Feature (b) is known from document D3 which discloses a clock buffer (150 in fig. 9) working either with complementary clock signals (/ext. CLK and ext. CLK in fig. 9) or with a single ended clock signal (ext. CLK in fig. 9) and a reference voltage (Vref in fig. 9).

Feature (c) is known from document D4 which discloses a memory device with output buffers having a configurable drive strength (paragraph [0026]), the memory being also configurable to work with a single ended clock signal or differential clock signals (fig. 5).

The solution of claim 1 is therefore considered to lack inventive step.

- 4 Dependent claims 2-5 and 8-12 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the EPC in respect of inventive step.

Document D3 discloses, in fig. 9 and 10, positive and negative clock input signals. Dependent claim 2 is not considered inventive.

Data input buffers using a reference signal are also well known in the art. See for example D5, fig. 6A, 6B. Dependent claims 3-5 are not considered inventive.

Document D1 discloses receiving a reset signal (paragraph [0098]) and loading a configuration at power up (paragraph [0105]). Which configuration is stored upon reset is merely an arbitrary choice. Dependent claims 8-9 are not considered inventive.

Finally, document D1 also discloses that the memory device is a flash memory device (paragraph [0035]). Dependent claims 10-12 are not considered inventive.

- 5 The applicant is invited to file a new set of claims which takes account of the above comments.

The opportunity should then also be taken to attend the following outstanding matter:

- the new independent claim to be filed should be divided in the two part form in accordance with Rule 43(1) EPC with respect to the most relevant prior art document D1;
- the applicant should also indicate in the letter of reply the difference of the subject-matter vis-à-vis the state of the art and **significance thereof**;

- the features of the claims should be provided with reference signs placed in parentheses to increase the intelligibility of the claims (Rule 43(7) EPC); this applies to both the preamble and characterising portion;
- to meet the requirements of Rule 42(1)(b) EPC, the most relevant cited prior art document D1 should be identified in the description and the relevant background art disclosed therein should briefly discussed;
- the description should be brought into conformity with the newly filed independent claim (Rule 42(1)(c) EPC);
- embodiments present in the description that are not covered by the claims should be removed or described as examples;
- care should be taken during revision not to add subject-matter which extends beyond the content of the application as originally filed, Article 123(2) EPC; the applicant is also requested to clearly identify the amendments carried out, irrespective of whether they concern amendments by addition, replacement or deletion, and to indicate the passages of the application as filed on which these amendments are based (see Rule 137(4) EPC and Guidelines H III, 2.1);
- any information the applicant may wish to submit concerning the subject-matter of the invention, for example further details of its advantages or of the problem it solves, and for which there is no basis in the application as filed, should be confined to the letter of reply and not be incorporated into the application (Article 123(2) EPC)



Letter accompanying subsequently filed items

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The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number

19202183.0

Applicant's or representative's reference

B119524WOEPT2

	Description of document	Original file name	Assigned file name
1	Amended claims with annotations	CLMS-HWA-1.PDF	CLMS-HWA-1.PDF
2	Amended claims (clean copy)	CLMS.PDF	CLMS.PDF
3	Amended description (clean copy)	DESC1.pdf	DESC-1.pdf
4	Amended description with annotations	DESC-HWA1.pdf	DESC-HWA-1.pdf
5	Letter relating to the search and examination procedure	EPLETT.pdf	EPLETT.pdf

	Payment	
1	Method of payment	Not specified

Signatures

Place: **Munich**
 Date: **10 August 2020**
 Signed by: **/Johannes Lang/**
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Our ref: B119524WOEPT2 JLA/Wrd/stv

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**In response to the Communication pursuant to Rule 70(2) EPC and
the invitation pursuant to Rule 70a(2) EPC dated April 6, 2020 and
the Extended European Search Report (EESR) dated February 27,
2020**

The applicant desires to proceed further with the above identified European Patent Application.

I. Amendments and Clarity

1. The applicant submits, without prejudice, an amended set of claims 1 to 20 as well as amended page 3 and new page 3a of the description to replace the respective claims and the respective pages of the description presently on file. Furthermore, pages 32 to 35 of the application as filed are withdrawn without re-placement. However, this does not mean waiving the right to reintroduce any deleted subject matter during further proceedings. Further examination shall be based on the amended documents.

The amended documents are enclosed as clean and marked-up copies.

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2. The amended set of claims corresponds to the claims on file with the following amendments:

Generally, while the claims have been amended with respect to several of their features, they are still directed to the same inventive concept as before:

Claim 1 was amended by replacing the feature regarding a chip enable signal/port with the feature “*mode setter (400) for configuring the configurable non-volatile memory device to one of a first operating mode and a second operating mode*”, as the claimed embodiment is mainly directed to a memory device that operates in two modes corresponding to single ended signaling and differential signaling, respectively. This amendment is supported e.g. by paragraphs [0031], [0035], [0055] and [0058] of the application. The removal of the prior feature regarding the chip enable port is based on the assessment of the Examiner stated in the EESR that there is no relevance of this element to the rest of the claim.

In order to address the objection raised in section 1 of the EESR, **claim 1** was further amended by removing the feature regarding the data input buffer that is configurable to one of a single data rate and a double data rate configuration. Instead, the claim now includes a first and a second mode of operation, which can be set by the introduced mode setter (see above for the support in the application), and which includes a first and a second data output clock, which is supported by Figure 8A of the application, as well as paragraphs [0054] to [0064] which describe this Figure. The dependent claims have been amended accordingly, thereby replacing the single/double data rate configuration-related features with feature related to a first/second mode of operation (see e.g. dependent claims 6 and 9), in order to unify the claimed terminology throughout the claims.

Finally, **claim 1** was amended by splitting the “*one or more output buffers*” previously claimed in combination into a first feature regarding “*a configurable clock output buffer (410)*” being enabled in the first operating

mode and being disabled in the second operating mode, on the basis of Figure 8B as well as paragraph [0046] of the application, and a “*configurable buffer (416)*”. It has further been specified in the claim that “*the output data (Qn) is referenced to the first clock input signal (CKI)*” in the second operating mode, and that it is “*synchronized with the first clock output signal (CKO)*” in the first operating mode. Support for these aspects can be found in Figure 3D disclosing CKI & Qn, as well as Figure 3B disclosing CKO & Qn.

Dependent **claim 6** was further amended by removal of the recitation of “*a configuration register*”, in order to address the objection raised in section 1 of the EESR. Instead, dependent claim 6 now recites a latch (502), which was acknowledged to be supported by the specification in section 1 of the EESR.

Dependent **claim 7** has also been amended to remove the recitation of “*a configuration register*”. Consequently, the rejection of section 1 of the EESR is now moot.

The dependent claims have further been amended, wherein the amendments are based on the following support in the application:

Claim 2 is based on Fig. 8A, reference sign 412; **claim 3** is based on Fig. 8A, reference sign 406; **claim 4** is based on Fig. 8A, reference sign 412; **claim 5** is based on the above-cited support re. Enabling/disabling based on the first/second modes and paragraph [0055], as well as claim 8 of the parent application; **claim 6** is based on the support stated with respect to the exchange of the single/double data rate with the first/second mode for claim 1 above; **claim 7** is equivalent to amended claim 5 with respect to the second comparator circuit and is based on claim 3 of the parent application, as well as paragraphs [0055] and [0059] of the application; **claim 8** is based on Fig. 6 and 11 as well as paragraph [0072] of the application; **claim 9** is based on the support stated with respect to the exchange of the single/double data rate with the first/second mode for claim 1 above, as well as on paragraphs [0029] and [0051] of the application; **claims 10 to**

12 are based on paragraph [0039] of the application; **claim 13** is based on paragraphs [0033] and [0037] of the application; **claim 14** is based on paragraph [0043] of the application; **claim 15** is based on paragraph [0046] of the application; **claims 16 to 18** are based on paragraph [0056] of the application; **claims 19 and 20** are based on paragraph [0025] of the application.

3. As requested in section 6.1 of the EESR, reference signs have been introduced throughout the claims to increase the intelligibility of the claims.
4. The description was amended to recite the prior art documents identified in the EESR (section 5 of the EESR) and the “further embodiments” of the description deleted by withdrawal of pages 32 to 35 of the description as filed, thereby deleting the “further embodiments”, as had also been requested by the Examiner in section 5 of the EESR.

II. Novelty

1. The subject-matter of claim 1 is novel over the prior art cited in the EESR.
2. For one, the Examiner had not raised any novelty objections in the EESR. However, the presently amended claim 1 is also novel over each one of prior art documents D1 to D5, at least because they do not disclose the following features of the claim:

(i) “a configurable clock output buffer (410) coupled to the first clock output port and the second clock output port, the configurable clock output buffer (410) configured to be enabled when the configurable non-volatile memory device is configured to the first operating mode, and to be disabled when the configurable non-volatile memory device is configured to the second operating mode;”

and

(ii) “a configurable output buffer (416) configured to have one of a plurality of output buffer drive strengths and to transfer output

data (Qn) retrieved from the one of the plurality of non-volatile memory blocks, wherein the output data (Qn) is referenced to the first clock input signal (CKI) when the configurable non-volatile memory device is configured to the second operating mode, and synchronized with the first clock output signal (CKO) when the configurable non-volatile memory device is configured to the first operating mode”.

3. With respect to the feature of the previous version of the claim corresponding to feature **(ii)**, the Examiner had cited paragraph [0026] of document D4 as allegedly disclosing a memory device with output buffers having configurable drive strength, the memory being configurable to work with a single ended clock signal or differential clock signals (Fig. 5 of D4). However, after thorough analysis of document D4, it appears that this document does not disclose or hint at any aspects with respect to a synchronization of any output data with a “*clock output signal*”, or any aspects with respect to the referencing of output data with a clock input signal. Paragraph [0026], at most, suggests that the drive strength may be one of a normal or reduced level depending on the value of bit “A1” and that a bit “AO” can be used to “*enable or disable state of a delay lock loop used to synchronize initial memory operations*”. With respect to synchronization, the subsequent paragraph [0027] additionally states that:

“As discussed above, the SDRAM 10 synchronizes the output of read data with the rising edges 74 and falling edges 76 of a single clock input system” (emphasis added).

Therefore, document D4 at most suggests that a rising or falling edge of a clock input is used for synchronization of the output of read data. However, this is not the same as synchronization with a “*first clock output signal*”. Furthermore, document D4 appears to be entirely silent with respect to how the “*output of read data*” could be referenced with a “*first clock input signal*”. Accordingly, document D4 does not directly and unambiguously disclose feature **(ii)** as presently claimed.

4. In addition, none of the other cited prior art documents discloses feature **(ii)** (which also appears to be in line with the opinion expressed in the

EESR, because the Examiner had only referred to prior art document D4 with respect to prior feature (c)).

5. With respect to feature **(i)** it appears that neither document D4 nor any of the other cited documents disclose this feature. Particularly, document D4 appears to be silent with respect to enabling and disabling any buffer, let alone enabling or disabling the presently claimed “*clock output buffer*” which is coupled to the first and second clock output port based on the first and second operating mode.
6. Therefore, features **(i)** and **(ii)** can be seen as distinguishing features with respect to each of the cited prior art documents.

III. Inventive Step

1. The subject-matter of new claim 1 is also based on an inventive step.
2. Considering document D1 as the closest prior art for the purpose of the problem-and-solution approach, the subject-matter of claim 1 differs from the disclosure of document D1 at least in the features **(i)** and **(ii)** recited above. It should be noted that even the feature that corresponded to distinguishing feature **(ii)** as recited above had been acknowledged as not being disclosed by document D1.
3. The **technical effect** achieved by the difference between the independent claim and the disclosure of the document D1 is that a higher level of performance can be achieved while also providing a more compatible and thus more cost-effective solution. This effect results from the fact that the proposed solution may be used in both high-speed and low-speed memory systems (see e.g. paragraphs [0026] to [0027] of the application).
4. The **objective technical problem** can be regarded as how to provide a memory device that can be used in both a parallel clocked memory system

and a serially clocked memory system (see e.g. paragraph [0027] of the application).

5. The person skilled in the art when faced with this problem and starting from document D1, would not have arrived at the claimed solution.

For one, none of the cited prior art documents provide a hint or suggestion in the direction of the claimed invention.

In addition, features **(i)** and **(ii)** cannot be construed as a mere aggregation of features as had been assumed for features (a) through (c) in the EESR. One reason for this is that both of these features are related to the first and second operating modes, thereby resulting in a synergistic effect for each of the claimed components based on these operating modes.

The same is true for the present claim feature corresponding to previous feature (b), which had been identified as another one of the distinguishing features in the EESR. Particularly, the feature now corresponding to feature (b) also includes the first and second operating modes, which are selected by the mode setter (400) of amended claim 1. Hence, the features corresponding to features (b) and (c) (i.e. feature **(ii)**) can also no longer be construed as a mere aggregation of features.

With respect to the two preceding paragraphs it should also be noted that the presently introduced “*mode setter*” leads to the claimed features effectively working together to produce a synergistic effect, because the mode setter sets one of the modes with direct consequences for each of the claimed features (and components of the memory device) that relate to these modes. It is thus clear that a combination of any two of the cited prior art documents cannot lead to a combination of the features currently claimed (e.g. the features corresponding to prior features (b) and (c)) in view of the assessment presented in the EESR.

Finally, there is no indication that the distinguishing features of claim 1 formed part of the common general knowledge of the person skilled in the art at the priority date of the present application.

IV. Requests

It is requested to grant a patent on the basis of the amended documents.

Should refusal of the present application be contemplated, **oral proceedings pursuant to Art. 116 EPC** are hereby requested.

The undersigned representative of the applicant would also be pleased to discuss the present case with the Primary Examiner in a telephone conversation or a personal interview.

Johannes Lang
European Patent Attorney

Enclosures:

Amended set of claims **1 to 20** (clean and marked-up copies)

Amended page **3** and new page **3a** of the description (clean and marked-up copies)

[0008] Therefore, it is desirable to provide a memory system device architecture capable of high speed operation while overcoming issues associated with the prior art memory system having memory devices connected in parallel to each other.

Attention is drawn to US 2004/148482 A1 describing a memory system having a plurality of memory devices and a memory controller. The memory devices are coupled to one another in a chain. The memory controller is coupled to the chain and configured to output a memory access command that is received by each of the memory devices in the chain and that selects a set of two or more of the memory devices to be accessed. Attention is further drawn to US 2006/067123 A1 describing a serial flash memory that is provided with multiple configurable pins, at least one of which is selectively configurable for use in either single-bit serial data transfers or multiple-bit serial data transfers. In single-bit serial mode, data transfer is bit-by-bit through a pin. In multiple-bit serial mode, a number of sequential bits are transferred at a time through respective pins. The serial flash memory may have 16 or fewer pins, and even 8 or fewer pins, so that low pin count packaging such as the 8-pin or 16-pin SOIC package and the 8-contact MLP/QFN/SON package may be used. The availability of the single-bit serial type protocol enables compatibility with a number of existing systems, while the availability of the multiple-bit serial type protocol enables the serial flash memory to provide data transfer rates, in systems that can support them, that are significantly faster than available with standard serial flash memories.

Attention is further drawn to US 6 337 832 B1 describing a synchronous semiconductor memory device that operates an input/output buffer circuit in synchronization with an external clock signal in a single data rate SDRAM operation mode. In a double data rate SDRAM operation mode, an internal clock signal of a frequency two times that of the external clock signal is generated. The input/output buffer circuit is operated in synchronization with the internal clock signal.

Attention is further drawn to US 2003/043684 A1 describing a memory device having a mode register with a selectable bit which sets the memory device to operate with a selected one of a plurality of possible clock input signals, for example, a single clock input or differential clock input.

Attention is further drawn to EP 0 818 734 A2 describing a system for signal transmission that has at least one bus for the signal transmission and a reflection-

prevention resistance provided on a stub connected to the bus for preventing reflection of signals at an intersection between the bus and the stub. The system includes termination resistances, and a switch unit for coupling the bus to termination voltage via the termination resistances in a first mode and for disconnecting the bus from the termination voltage in a second mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Embodiments of the clock mode circuits will now be described, by way of example only, with reference to the attached Figures, wherein:

Fig. 1 is a block diagram of a prior art Flash memory system;

Fig. 2A is a general block diagram of a serial memory system receiving a clock signal in parallel;

Fig. 2B is a general block diagram of a serial memory system receiving a clock signal serially;

Fig. 3A is a block diagram of a serial memory system receiving clock signals serially, according to one embodiment;

Fig. 3B is a timing diagram showing the operation of the memory system of Figure 3A;

Fig. 3C is a block diagram of a serial memory system receiving clock signals in parallel, according to another embodiment;

Fig. 3D is a timing diagram showing the operation of the memory system of Figure 3C;

Fig. 4 is a block diagram of a memory device having a native core and a serial input/output interface suitable for use in the serial memory systems of Figures 3A and B;

Fig. 5 is a block diagram illustrating a configurable input circuit embodiment usable in the serial memory systems of Figures 3A and 3C;

Fig. 6 is a circuit schematic embodiment of the mode setter of Figure 5;

Fig. 7 is a sequence diagram illustrating the operation of the mode setter of Figure 6;

Fig. 8A is a schematic embodiment of the configurable input circuit shown in Figure 5;

Fig. 8B is a timing diagram showing the operation of the circuits of Figure 8A;

[0008] Therefore, it is desirable to provide a memory system device architecture capable of high speed operation while overcoming issues associated with the prior art memory system having memory devices connected in parallel to each other. Attention is drawn to US 2004/148482 A1 describing a memory system having a plurality of memory devices and a memory controller. The memory devices are coupled to one another in a chain. The memory controller is coupled to the chain and configured to output a memory access command that is received by each of the memory devices in the chain and that selects a set of two or more of the memory devices to be accessed. Attention is further drawn to US 2006/067123 A1 describing a serial flash memory that is provided with multiple configurable pins, at least one of which is selectively configurable for use in either single-bit serial data transfers or multiple-bit serial data transfers. In single-bit serial mode, data transfer is bit-by-bit through a pin. In multiple-bit serial mode, a number of sequential bits are transferred at a time through respective pins. The serial flash memory may have 16 or fewer pins, and even 8 or fewer pins, so that low pin count packaging such as the 8-pin or 16-pin SOIC package and the 8-contact MLP/QFN/SON package may be used. The availability of the single-bit serial type protocol enables compatibility with a number of existing systems, while the availability of the multiple-bit serial type protocol enables the serial flash memory to provide data transfer rates, in systems that can support them, that are significantly faster than available with standard serial flash memories. Attention is further drawn to US 6 337 832 B1 describing a synchronous semiconductor memory device that operates an input/output buffer circuit in synchronization with an external clock signal in a single data rate SDRAM operation mode. In a double data rate SDRAM operation mode, an internal clock signal of a frequency two times that of the external clock signal is generated. The input/output buffer circuit is operated in synchronization with the internal clock signal. Attention is further drawn to US 2003/043684 A1 describing a memory device having a mode register with a selectable bit which sets the memory device to operate with a selected one of a plurality of possible clock input signals, for example, a single clock input or differential clock input. Attention is further drawn to EP 0 818 734 A2 describing a system for signal transmission that has at least one bus for the signal transmission and a reflection-

prevention resistance provided on a stub connected to the bus for preventing reflection of signals at an intersection between the bus and the stub. The system includes termination resistances, and a switch unit for coupling the bus to termination voltage via the termination resistances in a first mode and for disconnecting the bus from the termination voltage in a second mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Embodiments of the clock mode circuits will now be described, by way of example only, with reference to the attached Figures, wherein:

Fig. 1 is a block diagram of a prior art Flash memory system;

Fig. 2A is a general block diagram of a serial memory system receiving a clock signal in parallel;

Fig. 2B is a general block diagram of a serial memory system receiving a clock signal serially;

Fig. 3A is a block diagram of a serial memory system receiving clock signals serially, according to one embodiment;

Fig. 3B is a timing diagram showing the operation of the memory system of Figure 3A;

Fig. 3C is a block diagram of a serial memory system receiving clock signals in parallel, according to another embodiment;

Fig. 3D is a timing diagram showing the operation of the memory system of Figure 3C;

Fig. 4 is a block diagram of a memory device having a native core and a serial input/output interface suitable for use in the serial memory systems of Figures 3A and B;

Fig. 5 is a block diagram illustrating a configurable input circuit embodiment usable in the serial memory systems of Figures 3A and 3C;

Fig. 6 is a circuit schematic embodiment of the mode setter of Figure 5;

Fig. 7 is a sequence diagram illustrating the operation of the mode setter of Figure 6;

Fig. 8A is a schematic embodiment of the configurable input circuit shown in Figure 5;

Fig. 8B is a timing diagram showing the operation of the circuits of Figure 8A;

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Amended Claims (marked-up)

1. A configurable non-volatile memory device (300) comprising:
 - a plurality of non-volatile memory blocks (302, 304);
 - 5 a mode setter (400) for configuring the configurable non-volatile memory device to one of a first operating mode and a second operating mode;
 - ~~a chip enable port configured to receive a chip enable signal (CE#) for enabling the configurable non-volatile memory device (300);~~
 - a first clock input port configured to receive a first clock input signal (CKI);
 - 10 a second clock input port configured to receive a second clock input signal (CKI#), the second clock input signal being complementary to the first clock input signal;
 - a first clock output port configured to transfer a first clock output signal (CKO), wherein the first clock output signal is referenced to the first clock input signal (CKI);
 - 15 a second clock output port configured to transfer a second clock output signal (CKO#), the second clock output signal being complementary to the first clock output signal (CKO);
 - ~~at least one configurable data input buffer (412) configurable to an n-bit width (Dn) where n is a non-zero integer, and further configurable to one of single data rate configuration and double data rate configuration, the configurable data interface configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of~~
 - 20 ~~non-volatile memory blocks;~~
 - a configurable clock input buffer (406) coupled to the first clock input port and the second clock input port, the configurable clock input buffer (406) being
 - configurable to ~~one of~~ a single ended signaling configuration (702, 704) when the
 - configurable non-volatile memory device is configured to the second operating mode,
 - 30 and configurable to a differential signaling configuration (700) when the configurable non-volatile memory device is configured to the first operating mode, the differential signaling configuration for utilizing the first clock input signal (CKI) and the second

clock input signal (CKI#) as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal (CKI) and the second clock input signal (CKI#) as a single ended signal; and

_____ a configurable clock output buffer (410) coupled to the first clock output port and the second clock output port, the configurable clock output buffer (410) configured to be enabled when the configurable non-volatile memory device is configured to the first operating mode, and to be disabled when the configurable non-volatile memory device is configured to the second operating mode; and

~~one or more a configurable output buffers buffer (410, 416) configurable~~ configured to have one of a plurality of output buffer drive strengths and to transfer the output data (Qn) retrieved from the one of the plurality of non-volatile memory blocks, wherein the output data (Qn) is referenced to the first clock input signal (CKI) when the configurable non-volatile memory device is configured to the second operating mode, and synchronized with the first clock output signal (CKO) when the configurable non-volatile memory device is configured to the first operating mode.

2. The configurable non-volatile memory device as claimed in claim 1, ~~wherein the first clock input signal is a positive clock input signal, and the second clock input signal is a negative clock input signal respectively~~ further comprising:

_____ a voltage input port (VREF) for receiving a reference voltage; and
_____ a configurable data input buffer (412) being configurable to utilize the reference voltage to determine logic levels of input data (Dn) when the configurable non-volatile memory device is configured to the first operating mode, and to disable the utilization of the reference voltage when the configurable non-volatile memory device is configured to the second operating mode.

3. The configurable non-volatile memory device as claimed in claim 1 ~~or 2~~, wherein the at least one configurable data input buffer is further configured to utilize a reference voltage (VREF) for determining logic levels of the common data signals configurable clock input buffer (406) comprises:

_____ a first comparator circuit (700) configured to compare the first clock input signal (CKI) to the second clock input signal (CKI#) when the configurable non-volatile memory device is configured to the first operating mode; and

a first buffer circuit (702, 704) configured to receive either the first clock input signal (CKI) or the second clock input signal as the single ended signal when the configurable non-volatile memory device is configured to the second operating mode.

- 5 4. The configurable non-volatile memory device as claimed in any one of claims 2 to 3, wherein the reference voltage is set to a predetermined voltage level configurable data input buffer (412) comprises:

a second comparator circuit (720) configured to compare the input data (Dn) to the reference voltage (VREF) when the configurable non-volatile memory device is
10 configured to the first operating mode; and

a second buffer circuit (722) configured to receive the input data (Dn) and provide a buffered input data signal without the utilization of the reference voltage (VREF) when the configurable non-volatile memory device is configured to the second operating mode.

- 15 5. The configurable non-volatile memory device as claimed in claim 3, wherein ~~the~~ reference voltage is set to half of the common data signal's high logic level the first comparator circuit (700) is disabled when the configurable non-volatile memory device is configured to the second operating mode, and first buffer circuit (702, 704) is
20 disabled when the configurable non-volatile memory device is configured to the first operating mode.

- 25 6. The configurable non-volatile memory device as claimed in claim 1, further comprising a ~~configuration register latch (502)~~ configured to store a configuration information indicating whether the configurable non-volatile memory device is configured to the first operating mode or to the second operating mode ~~clock input buffer is configured as the single ended clock signaling configuration or the differential clock signaling configuration.~~

- 30 7. The configurable non-volatile memory device as claimed in claim ~~14~~, further comprising a ~~configuration register configured to store the plurality of output buffer drive strengths to be utilized by the one or more configurable output buffers~~ wherein the second comparator circuit (720) is disabled when the configurable non-volatile memory device is configured to the second operating mode, and the second buffer

circuit (722) is disabled when the configurable non-volatile memory device is configured to the first operating mode.

8. The configurable non-volatile memory device as claimed in any one of claims 1 to 7, further comprising a reset port configured to receive a reset signal (RST#) for resetting the configurable non-volatile memory device to a default configuration wherein the mode setter (400) comprises a voltage sense circuit (500) configured to detect a predetermined level of the reference voltage when the configurable non-volatile memory device is powered-up or reset.

9. The configurable non-volatile memory device as claimed in any one of claims 1 to 8, wherein the default configuration comprises the single ended clock signaling configuration mode setter (400) configures the configurable non-volatile memory device to the second operating mode by default when the configurable non-volatile memory device is powered-up or reset.

10. The configurable non-volatile memory device as claimed in any one of claims 1 to 9, wherein the configurable non-volatile memory device is a flash memory device.

11. The configurable non-volatile memory device as claimed in any one of claims 1 to 10, wherein the configurable non-volatile memory device is a NOR flash memory device.

12. The configurable non-volatile memory device as claimed in any one of claim 1 to 10, wherein the configurable non-volatile memory device is a NAND flash memory device.

13. The configurable non-volatile memory device as claimed in any one of claims 1 to 12, wherein the first operating mode is a high speed operating mode, and the second operating mode is a low speed operating mode.

14. The configurable non-volatile memory device as claimed in claim 8, wherein the predetermined level of the reference voltage (VREF) is a half level of a main supply voltage (VDD).

15. The configurable non-volatile memory device as claimed in any one of claims 1 to 14 further comprising a clock generator (408) coupled to the configurable clock input buffer (406) and the configurable clock output buffer (410), the clock generator (408) is configured to provide internal clock signals (CK, CK#), wherein the internal clock signals (CK, CK#) are utilized for generating the output data (Qn).

16. The configurable non-volatile memory device as claimed in any one of claims 1 to 15 further comprising a clock synthesizer unit (706) configured to be utilized for the synchronization of the output data (Qn) and the first clock output signal (CKO) when the configurable non-volatile memory device is configured to the first operating mode.

17. The configurable non-volatile memory device as claimed in claim 16, wherein the clock synthesizer unit (706) is a phase locked loop (PLL).

18. The configurable non-volatile memory device as claimed in claim 16, wherein the clock synthesizer unit (706) is a delay locked loop (DLL).

19. The configurable non-volatile memory device as claimed in any one of claims 1 to 18, wherein the first clock input signal (CKI), the second clock input signal (CKI#), the first clock output signal (CKO) and the second clock output signal (CKO#) are configured as SSTL signals when the configurable non-volatile memory device is configured to the first operating mode.

20. The configurable non-volatile memory device as claimed in any one of claims 1 to 18, wherein the first clock input signal (CKI), the second clock input signal (CKI#), the first clock output signal (CKO) and the second clock output signal (CKO#) are HSTL signals when the configurable non-volatile memory device is configured to the first operating mode.

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Amended Claims (clean)

1. A configurable non-volatile memory device (300) comprising:
 - a plurality of non-volatile memory blocks (302, 304);
 - 5 a mode setter (400) for configuring the configurable non-volatile memory device to one of a first operating mode and a second operating mode;
 - a first clock input port configured to receive a first clock input signal (CKI);
 - a second clock input port configured to receive a second clock input signal (CKI#), the second clock input signal being complementary to the first clock input
 - 10 signal;
 - a first clock output port configured to transfer a first clock output signal (CKO), wherein the first clock output signal is referenced to the first clock input signal (CKI);
 - a second clock output port configured to transfer a second clock output signal (CKO#), the second clock output signal being complementary to the first clock output
 - 15 signal (CKO);
 - a configurable clock input buffer (406) coupled to the first clock input port and the second clock input port, the configurable clock input buffer (406) being configurable to a single ended signaling configuration (702, 704) when the configurable non-volatile memory device is configured to the second operating mode, and
 - 20 configurable to a differential signaling configuration (700) when the configurable non-volatile memory device is configured to the first operating mode, the differential signaling configuration for utilizing the first clock input signal (CKI) and the second clock input signal (CKI#) as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal (CKI) and the second clock
 - 25 input signal (CKI#) as a single ended signal; and
 - a configurable clock output buffer (410) coupled to the first clock output port and the second clock output port, the configurable clock output buffer (410) configured to be enabled when the configurable non-volatile memory device is configured to the first operating mode, and to be disabled when the configurable non-volatile memory
 - 30 device is configured to the second operating mode; and
 - a configurable output buffer (416) configured to have one of a plurality of output buffer drive strengths and to transfer output data (Qn) retrieved from the one of the

plurality of non-volatile memory blocks, wherein the output data (Qn) is referenced to the first clock input signal (CKI) when the configurable non-volatile memory device is configured to the second operating mode, and synchronized with the first clock output signal (CKO) when the configurable non-volatile memory device is configured to the first operating mode.

2. The configurable non-volatile memory device as claimed in claim 1, further comprising:
 - a voltage input port (VREF) for receiving a reference voltage; and
 - a configurable data input buffer (412) being configurable to utilize the reference voltage to determine logic levels of input data (Dn) when the configurable non-volatile memory device is configured to the first operating mode, and to disable the utilization of the reference voltage when the configurable non-volatile memory device is configured to the second operating mode.
3. The configurable non-volatile memory device as claimed in claim 1 or 2, wherein the configurable clock input buffer (406) comprises:
 - a first comparator circuit (700) configured to compare the first clock input signal (CKI) to the second clock input signal (CKI#) when the configurable non-volatile memory device is configured to the first operating mode; and
 - a first buffer circuit (702, 704) configured to receive either the first clock input signal (CKI) or the second clock input signal as the single ended signal when the configurable non-volatile memory device is configured to the second operating mode.
4. The configurable non-volatile memory device as claimed in any one of claims 2 to 3, wherein the configurable data input buffer (412) comprises:
 - a second comparator circuit (720) configured to compare the input data (Dn) to the reference voltage (VREF) when the configurable non-volatile memory device is configured to the first operating mode; and
 - a second buffer circuit (722) configured to receive the input data (Dn) and provide a buffered input data signal without the utilization of the reference voltage (VREF) when the configurable non-volatile memory device is configured to the second operating mode.

5. The configurable non-volatile memory device as claimed in claim 3, wherein the first comparator circuit (700) is disabled when the configurable non-volatile memory device is configured to the second operating mode, and first buffer circuit (702, 704) is disabled when the configurable non-volatile memory device is configured to the first operating mode.

6. The configurable non-volatile memory device as claimed in claim 1, further comprising a latch (502) configured to store a configuration information indicating whether the configurable non-volatile memory device is configured to the first operating mode or to the second operating mode.

7. The configurable non-volatile memory device as claimed in claim 4, wherein the second comparator circuit (720) is disabled when the configurable non-volatile memory device is configured to the second operating mode, and the second buffer circuit (722) is disabled when the configurable non-volatile memory device is configured to the first operating mode.

8. The configurable non-volatile memory device as claimed in any one of claims 2 to 7, wherein the mode setter (400) comprises a voltage sense circuit (500) configured to detect a predetermined level of the reference voltage when the configurable non-volatile memory device is powered-up or reset.

9. The configurable non-volatile memory device as claimed in any one of claims 1 to 8, wherein the mode setter (400) configures the configurable non-volatile memory device to the second operating mode by default when the configurable non-volatile memory device is powered-up or reset.

10. The configurable non-volatile memory device as claimed in any one of claims 1 to 9, wherein the configurable non-volatile memory device is a flash memory device.

11. The configurable non-volatile memory device as claimed in any one of claims 1 to 10, wherein the configurable non-volatile memory device is a NOR flash memory device.

12. The configurable non-volatile memory device as claimed in any one of claim 1 to 10, wherein the configurable non-volatile memory device is a NAND flash memory device.
- 5 13. The configurable non-volatile memory device as claimed in any one of claims 1 to 12, wherein the first operating mode is a high speed operating mode, and the second operating mode is a low speed operating mode.
- 10 14. The configurable non-volatile memory device as claimed in claim 8, wherein the predetermined level of the reference voltage (VREF) is a half level of a main supply voltage (VDD).
- 15 15. The configurable non-volatile memory device as claimed in any one of claims 1 to 14 further comprising a clock generator (408) coupled to the configurable clock input buffer (406) and the configurable clock output buffer (410), the clock generator (408) is configured to provide internal clock signals (CK, CK#), wherein the internal clock signals (CK, CK#) are utilized for generating the output data (Qn).
- 20 16. The configurable non-volatile memory device as claimed in any one of claims 1 to 15 further comprising a clock synthesizer unit (706) configured to be utilized for the synchronization of the output data (Qn) and the first clock output signal (CKO) when the configurable non-volatile memory device is configured to the first operating mode.
- 25 17. The configurable non-volatile memory device as claimed in claim 16, wherein the clock synthesizer unit (706) is a phase locked loop (PLL).
18. The configurable non-volatile memory device as claimed in claim 16, wherein the clock synthesizer unit (706) is a delay locked loop (DLL).
- 30 19. The configurable non-volatile memory device as claimed in any one of claims 1 to 18, wherein the first clock input signal (CKI), the second clock input signal (CKI#), the first clock output signal (CKO) and the second clock output signal (CKO#) are configured as SSTL signals when the configurable non-volatile memory device is configured to the first operating mode.

20. The configurable non-volatile memory device as claimed in any one of claims 1 to 18, wherein the first clock input signal (CKI), the second clock input signal (CKI#), the first clock output signal (CKO) and the second clock output signal (CKO#) are
- 5 HSTL signals when the configurable non-volatile memory device is configured to the first operating mode.

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