

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INFINEON TECHNOLOGIES AMERICAS CORP.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

Case IPR2025-01456
Patent 10,140,028

PATENT OWNER'S PRELIMINARY RESPONSE

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37 C.F.R. § 42.104(b)(3).....4

PATENT OWNER'S EXHIBIT LIST

Exhibit	Description
2001	Lowenstein Declaration In Support of Notice of Intent
2002	Woo Declaration In Support of Notice of Intent
2003	Courtney Declaration In Support of Notice of Intent
2004	Complaint for Patent Infringement in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.), Dkt. 1 (Mar. 25, 2025) [Complaint]
2005	November 3, 2017 Notice Letter to Cypress Semiconductor Corporation [11/03/17 Letter] (CONFIDENTIAL)
2006	First Amended Scheduling Order in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.), Dkt. 43 (Oct. 17, 2025) [Amended-Scheduling-Order]
2007	Defendant's Opening Claim Construction Brief in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.), Dkt. 44 (Oct. 27, 2025) [Opening-Claim-Construction-Brief]
2008	Defendants' Election of Asserted Prior Art Grounds in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.) (served Nov. 3, 2025) [Election-of-Grounds]
2009	<i>Reserved</i>
2010	<i>Reserved</i>
2011	<i>Reserved</i>
2012	Declaration of Boris Teksler [Teksler-Decl.] (CONFIDENTIAL – ATTORNEY'S EYES ONLY)

Exhibit	Description
2013	Press Release, Infineon Technologies AG completes acquisition of Cypress Semiconductor Corporation (Apr. 16, 2020) [Press-Release-Cypress]
2014	<i>Reserved</i>
2015	February 21, 2020 Email from Conversant (Feb. 21, 2020) [02/21/20 Email] (CONFIDENTIAL)
2016	Conversant Presentation (Feb. 21, 2020) [02/21/20 Conversant Presentation] (CONFIDENTIAL)
2017	Cypress Response Presentation (May 20, 2020) [05/20/20 Cypress Response Presentation] (CONFIDENTIAL)
2018	Conversant Response Presentation (July 14, 2020) [07/14/20 Conversant Response Presentation] (CONFIDENTIAL)
2019	Cypress Response Letter (Sep. 9, 2020) [09/09/20 Cypress Response Letter] (CONFIDENTIAL)
2020	<i>Reserved</i>
2021	MOSAID Response Presentation (Feb. 9, 2024) [02/09/24 MOSAID Response Presentation] (CONFIDENTIAL)
2022	MOSAID – Infineon/Cypress Presentation (February 28, 2023) [02/28/23 MOSAID-Infineon/Cypress Presentation] (CONFIDENTIAL)
2023	Email chain (April 14, 2023) (Apr. 12, 2023) [04/12/23 Email] (CONFIDENTIAL)
2024	<i>Reserved</i>
2025	Infineon's Preliminary Invalidity Contentions in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.) (served Aug. 15, 2025) [Invalidity-Contentions]

Exhibit	Description
2026	Declaration of Sunil P. Khatri, Ph.D. [Khatri-Decl.]

All emphases in quotations are added unless otherwise stated.

I. INTRODUCTION

The Board should deny institution because the Petition fails to show a reasonable likelihood of prevailing on any challenged claim for numerous, independently sufficient reasons.

As an initial matter, the Petition should be rejected because it fails to reconcile its claim construction positions with those it takes in the co-pending district court action between the parties. In the district court, Petitioner maintains that the terms “positive clock input signal” and “negative clock input signal” are indefinite and that the term “clock output signal” must be construed to mean “a periodic signal used to synchronize system operations” or a “synchronous periodic signal.” *See* Ex. 2007 [Opening-Claim-Construction-Brief] 3, 7. Here, Petitioner does not disclose these positions and instead maintains that “Petitioner submits that no claim terms presently require a formal construction for purposes of addressing the grounds in this Petition.” Pet., 7. Under the Director’s recent decisions, Petitioner’s unexplained inconsistency is sufficient reason to deny institution. *See* Section II.A *infra*.

Even if that could be overlooked, Petitioner does not show that any of its grounds, all based upon a combination of Ryu and Cole, disclose or render obvious multiple claim elements. For example, each claim requires “a chip enable port configured to receive a chip enable signal *for enabling the configurable non-volatile memory device*.” Ex. 1001 [’028] cl. 1. Petitioner equates Ryu’s “CEB”

with a device-level “chip enable signal,” but Ryu makes clear that the CEB merely gates an output buffer; it does not enable or disable the non-volatile memory device. Directly to the contrary, Ryu’s non-volatile memory device operates without regard to the CEB signal. *See* Section II.B.1 *infra*. Likewise, Petitioner provides no mapping for the claimed “output buffers.” The claims require the *same* one or more configurable output buffers to satisfy *two* functions. But Petitioner relies on an alleged “output buffer” in *Ryu* to satisfy one function (“output data synchronized with the clock output signal”), but on a different alleged “output buffer” in the different reference *Arcoleo* to satisfy the other (“configurable to one of a plurality of output buffer drive strengths”). Critically, Petitioner never explains how its hypothetical combined system would have the combined dual functionality or how any output of *Arcoleo*’s alleged output buffer is synchronized with any alleged “clock output signal.” *See* Section II.B.2.

Finally, Petitioner never adequately states its Ryu/Cole combination. Consequently, Petitioner does not establish a motivation to combine Ryu and Cole with its other references, let alone a reasonable expectation of success. While Petitioner offers several rationales, in light of its unexplained combination, those rationales are conclusory at best. *See* Section II.C *infra*.

For each of these reasons, institution should be denied.

II. THE PETITION FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD OF SUCCESS.

A. The Petition Is Deficient Because It Does Not Disclose, Reconcile, Or Apply Its District Court Claim Constructions.

In the Petition, Petitioner contends that “no claim terms presently require a formal construction.” Pet., 7. In the District Court Action, however, Petitioner takes the opposite approach, insisting that multiple claim terms of the ’028 patent are indefinite or must be construed in a way that materially narrows their scope.

The ’028 patent is currently asserted in *MOSAID Technologies Inc. v. Infineon Technologies AG, et al.*, No. 1:25-cv-00436 (W.D. Tex.) (the “District Court Action”). There, Petitioner argues that: (i) the terms “positive clock input signal” and “negative clock input signal” are indefinite; and (ii) the term “clock output signal” must be construed to mean “a periodic signal used to synchronize system operations” or a “synchronous periodic signal.” See Ex. 2007 [Opening-Claim-Construction-Brief] 3, 7. Petitioner does not disclose these positions to the Board, does not attempt to reconcile them with its “no construction necessary” position here, and does not show that its grounds satisfy the claims even under its own proposed constructions.

Under recent Director decisions, that combination of nondisclosure, inconsistency, and substantive failure warrants denial of institution. In *Revvo*, the Director explained that while “the Board’s trial rules do not necessarily prohibit

petitioners from taking inconsistent claim construction positions before the Board and a district court,” a petitioner that advances different positions “should, at a minimum, explain why alternative positions are warranted.” *Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20, 3-5 (Nov. 3, 2025) (precedential) (quoting *Cambridge Mobile Telematics, Inc. v. Sfara, Inc.*, IPR2024-00952, Paper 12, 8-9 (Dec. 13, 2024) (informative)); 37 C.F.R. § 42.104(b)(3) (IPR challenge must “[p]rovide a statement of the precise relief requested for each claim challenged” which “must identify . . . [h]ow the challenged claim is to be construed”); *see also Sun Pharm. Indus. Ltd. v. Nivagen Pharm., Inc.*, IPR2025-00893, Paper 18, 2-3 (Sept. 19, 2025) (denying institution where petitioner advanced narrow construction in district court and a broader “plain and ordinary meaning” in petition without sufficient explanation, noting that unexplained differences undermine Office’s goal of “uniformity and predictability” in claim construction). In *Tesla*, the Director denied institution where the petitioner—as here— argued a term was indefinite in district court while telling the Board that “no claim term requires express construction.” *Tesla, Inc. v. Intellectual Ventures II LLC*, IPR2025-00340, Paper 18, 2-5 (Nov. 5, 2025) (informative). The Board held that the mere fact that indefiniteness cannot be raised in an IPR “is not a sufficient explanation” for the divergent positions and that, at a minimum, the petitioner had to either justify the difference or show that, even assuming definiteness, the prior art still met the

limitation. *Id.*

1. Petitioner’s Indefiniteness Arguments For The
“Positive”/“Negative Clock Input Signal[s]” Terms Are Not
Disclosed or Reconciled.

In the District Court Action, Petitioner urges the court to hold the “positive clock input signal” and “negative clock input signal” terms of claim 2 indefinite.

Petitioner contends in the District Court Action:

This Court should find the terms “positive” and “negative clock input signals” indefinite because POSITAs lack reasonable certainty about what dependent claim 2’s “positive” and “negative clock input signal[s]” are. Those terms are nowhere defined—the specification never uses them, nor do the other claims—which suggests they are indefinite. ...

Beyond the lack of definition, the words “positive” and “negative” make little sense in the context of a clock signal. A clock signal does not carry a “positive” or “negative” designation; it toggles between high (voltage present) and low (no voltage present). At most, one might attempt to infer from the specification a “positive” clock signal (high) and a “zero” clock signal (low). But Claim 2 explicitly refers to a “negative clock input signal,” and the patent never explains what that means. Even if “negative” were read to mean “low,” claim 2 still cannot be reconciled with the nature of a clock signal. A clock does not remain at high or low indefinitely—it oscillates. Claim 2, therefore, is internally incoherent: it assigns static labels (“positive” and “negative”) to a signal whose essence is dynamic.

Because the claim language is ambiguous and the specification fails to clarify, a POSITA could not determine with reasonable certainty the scope of Claim 2. The Court should hold dependent claim 2 indefinite.

Ex. 2007 [Opening-Claim-Construction-Brief] 7-8. In sum, Petitioner’s district court position is that these terms are so unclear that they cannot be applied at all.

Here, by contrast, Petitioner tells the Board that “no claim terms presently require a formal construction,” never discloses any indefiniteness challenge, and proceeds as if all terms—including the “positive” and “negative clock input signal[s]”—can be applied under an “ordinary and customary meaning.” Pet., 7-8. Petitioner offers no explanation of how a term it contends is indefinite in district court can be applied here at all—much less without construction—and does not separately show that its Ryu-Cole-Arcoleo combinations satisfy the relevant limitations under any construction that it regards as definite.

Under *Tesla*, it is not enough for Petitioner to respond that indefiniteness is not an IPR ground. The Director has already held that this “is not a sufficient explanation” for taking inconsistent positions, and that a petitioner must either justify the difference or show that, even assuming definiteness, a POSITA would still understand the asserted art to meet the limitation. *Tesla*, IPR2025-00340, Paper 18, 3-5. Petitioner does neither here. Under *Revvo*, *Tesla*, and *Sun*, that omission alone

weighs against institution.

2. Petitioner Does Not Apply Its District Court Construction Of “clock output signal.”

Petitioner’s inconsistency is even more pronounced for the “clock output signal” limitation. In the District Court Action, Petitioner has asked the court to construe “clock output signal” as “a synchronous periodic signal used to synchronize system operations” or alternatively as “a periodic signal that synchronizes system operations,” or alternatively as a “synchronous periodic signal.” Ex. 2007 [Opening-Claim-Construction-Brief] 3, 7. Petitioner’s district court constructions, however, are not applied in this proceeding, where again Petitioner maintains that “no claim terms presently require a formal construction.” Pet., 7.

To be sure, Petitioner does attempt to map the prior art “based on two interpretations of ‘clock’ signal.” *Id.*, 7, 18. But, for both “interpretations,” Petitioner does not identify or apply its district court constructions. In its first interpretation, Ground 1A, which purports to adopt Patent Owner’s position, Petitioner makes clear that it does not agree that Ryu’s strobe can be a “clock signal,” much less a “clock output signal.” *See id.*, 8 (“the term ‘clock’ signal is distinguished from a ‘strobe’ signal ...”); *id.*, 28, n.3 (“Petitioner’s mapping of data strobe inputs to clock input signals in this ground is based on Patent Owner’s interpretation of clock signals as encompassing data strobes, which Petitioner does not concede.”).

While Ground 1B does not rely upon a strobe, there too, Petitioner does not apply its own constructions. *See id.*, 67-70. Under those constructions, the “clock output signal” must be “a synchronous periodic signal used to synchronize system operations,” a “periodic signal that synchronizes system operations,” or a “synchronous periodic signal.” Ex. 2007 [Opening-Claim-Construction-Brief] 3, 7. In Ground 1B, Petitioner suggests that in view of Grundy, a POSITA “would have implemented the non-volatile memory device of the Ryu-Cole-Arcoleo combination to include a clock line that passes through the device” and that the device “includes a clock output port configured to transfer a clock output signal that is referenced to a first clock input signal.” Pet., 50-52. But Petitioner never applies its district court constructions to its Ryu-Grundy-Cole-Arcoleo device.

In short, for “clock output signal,” Petitioner (i) advocates for narrowing, periodic, synchronous “clock output signal” constructions in district court; (ii) refuses to disclose or apply those constructions in this IPR, instead relying on its own interpretation of Patent Owner’s infringement contentions in its Ground 1A, and a vague Grundy-based alternative for Ground 1B; and (iii) never explains how any signal satisfies the “clock output signal” limitation under Petitioner’s proposed construction. Again, under *Revvo*, *Tesla*, and *Sun*, this combination of nondisclosure, inconsistency, and substantive failure supports denying institution.

B. Petitioner Fails To Show Multiple Claim Limitations (All Grounds, All Challenged Claims).

Both of Petitioner’s grounds fail because the cited art does not teach multiple limitations present in all challenged claims.

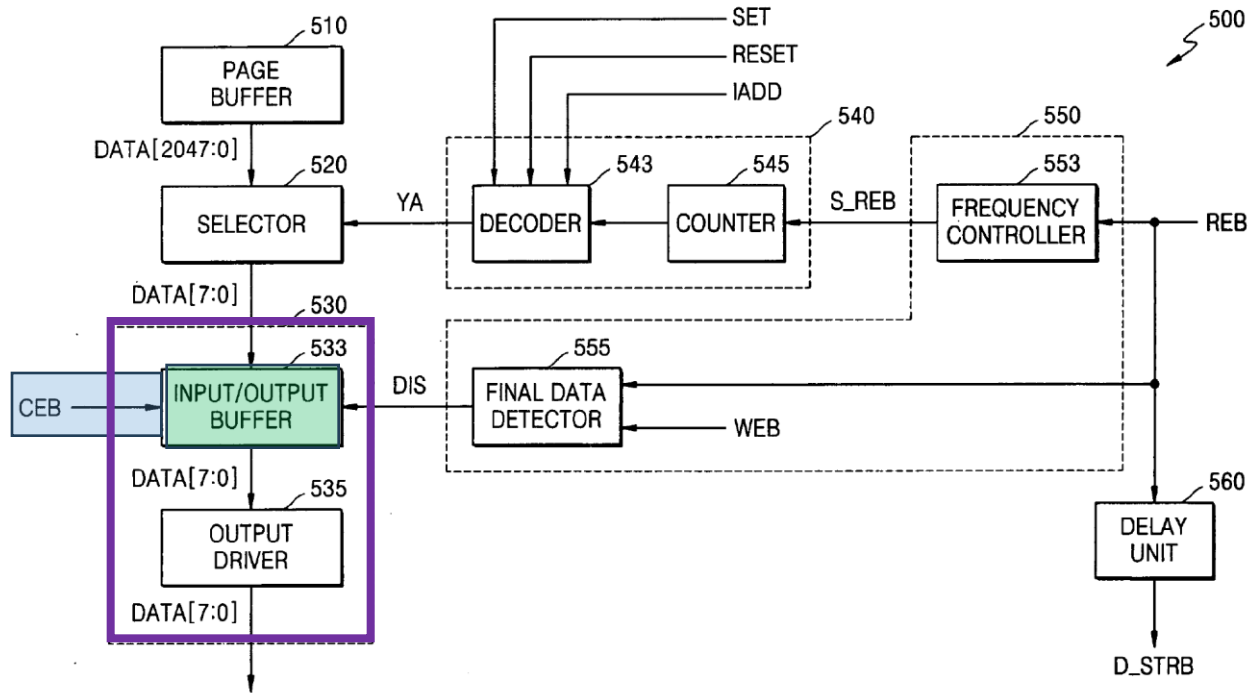
1. Petitioner Fails To Show “a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device.”

Each of the claims requires “a chip enable port configured to receive a chip enable signal for *enabling* the configurable non-volatile memory device.” Ex. 1001 [’028] cl. 1.¹ Petitioner fails to prove that its alleged “chip enable signal” *enables* its alleged “configurable non-volatile memory device.” Petitioner relies upon a Ryu’s “CEB” signal as the “chip enable signal.” But Ryu is explicit—the CEB only activates an input/output buffer, not the non-volatile memory device itself. Indeed, as explained in more detail below, Ryu’s non-volatile memory device can remain enabled even in the absence of the CEB signal.

Petitioner identifies Ryu’s Figure 5 as the alleged “**configurable non-volatile memory device**”:

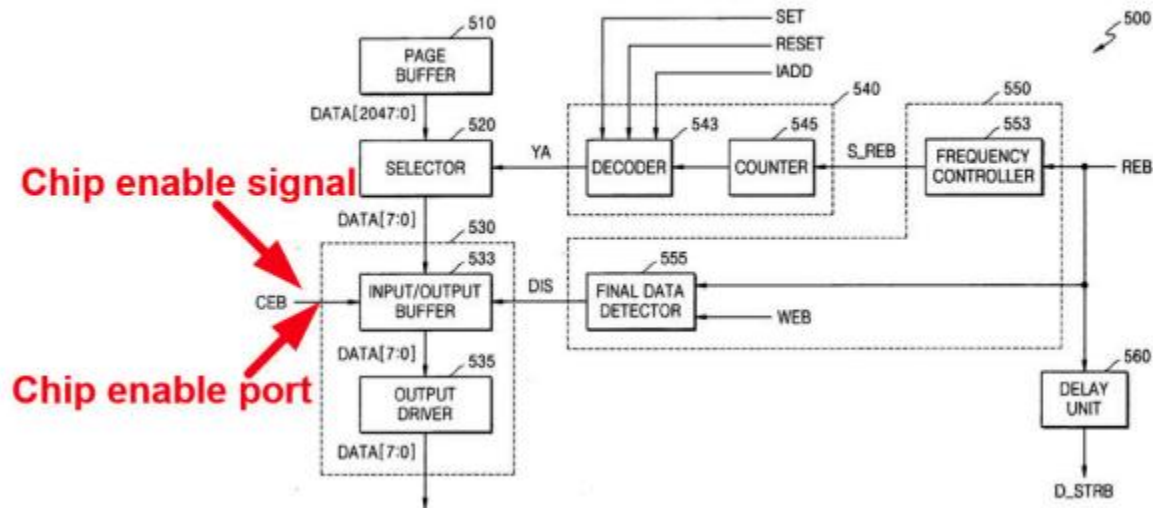
¹ Claim 1 is the only independent claim in the ’028 patent. Petitioner’s Ground 1B refers back to Petitioner’s Ground 1A for this limitation. *See, e.g.*, Pet., 66 (referring to this limitation as “Element [1b]”).

FIG. 5



Pet., 25. Petitioner further identifies the CEB input in Figure 5 as the claimed “chip enable signal,” and argues that a POSITA would have understood or found obvious that CEB was received at a “chip enable port”:

FIG. 5



Pet., 26 (Ryu’s Figure 5, as labeled by Petitioner).

Petitioner provides a conclusory statement that “Ryu’s enable signal CEB represents a chip enable signal for enabling the configurable non-volatile memory device, a memory chip.” Pet., 26 (citing Ex. 1003 [Sechen-Decl.] ¶ 89). While this bare conclusion is accompanied by a string of pin citations to five exhibits as supposed “corroboration,” the Petition lacks any explanation or discussion of why or how the CEB meets the claim element.

In fact, the opposite conclusion is provable based on Ryu itself. Ryu’s CEB signal does not enable the Figure 5 device. It only enables use of the input/output buffer inside output unit 530. But neither the input/output buffer nor the output unit 530 that contains the input/output buffer are Petitioner’s “configurable non-volatile memory device”; they are merely components within what Petitioner has identified

as the claimed “device.” See Pet., 23 (“Ryu discloses that an output unit of the memory device can be ‘activated in response to an enable signal (CEB)’”). Indeed, Ryu is express that the CEB signal only “activate[s]” the “output unit 530,” and is not a device-level chip enable signal for Ryu’s Figure 5. See, e.g., Ex. 1004 [Ryu] [0043] (“***The output unit 530 is activated*** in response to an enable signal CEB ...”), [0059] (similar); see also *id.*, [0060] (“The input/output buffer 533 outputs or blocks the data DATA[7:0] in response to the enable signal CEB or the disable signal DIS”), [0061] (“***The enable signal CEB, which is a signal for activating the input/output buffer 533,*** allows the input/ output buffer 533 to output the data DATA[7:0]”). See also Ex. 2026 [Khatri-Decl.] ¶ 36.

These disclosures confirm that CEB does not enable Ryu’s Figure 5 system (*i.e.*, the alleged “non-volatile memory device”). As Dr. Khatri explains:

The CEB input to Ryu’s Figure 5 controls only when data is output from the output unit 530. It does not turn Figure 5 on or off. Even when the CEB is de-asserted and the output unit is disabled, Figure 5’s nonvolatile memory remains enabled and active. A POSITA would inspect Ryu’s Figure 5 and conclude that the Figure 5 system is clearly “enabled” in this circumstance regardless of whether CEB is asserted, because CEB only drives the “input/output buffer” 533, and does not drive other components of the Figure 5 system, such as the page buffer 510, the selector 520, the decoder 543, the counter 545, the frequency controller 553, the delay unit 560, and the final data detector 555. A

POSITA would readily understand that since CEB does not drive these components, their operation continues, independent of the value of CEB. Petitioner agrees with this, stating that “Ryu discloses that *an output unit* of the memory device can be ‘activated in response to an enable signal (CEB).’” Pet., 23.

Ex. 2026 [Khatri-Decl.] ¶ 37.

Thus, Ryu makes clear that its CEB does not enable the nonvolatile memory device, it merely activates an output unit. The ’028 patent, moreover, makes a clear distinction between signals that enable or disable memory devices at the device level (labeled “CE#” in various examples) from output-level signals that only disable or enable ports to read or write data (labeled “DSI,” “EN_E” and “EN_O” in various examples). *Compare* Ex. 1001 [’028] 1:67-2:2 (“Each memory device is enabled/disabled with respective chip select signals CE#1, CE#2, CE#3 and CE#4, provided by memory controller 14”) *with* 10:6-9 (“DSI is used for enabling the output port Qn buffer to output read data”), 12:8-10 (“data from RD_E and RD_O will be provided on Q_E and Q_O in response to enable signals EN_E and EN_O at the high logic level”).

The supposed “corroboration” for Petitioner’s view that Ryu’s CEB is “a chip enable signal for enabling” Ryu’s Figure 5 does not support Petitioner’s point. Pointing to the use of the label “CEB” in other contexts, Petitioner’s expert argues the abstract proposition that “multiple references that use the acronym ‘CEB’ to refer

to an active low chip enable signal, and specifically, an active low chip enable signal where ‘B’ (for “bar” or complement) indicates active low.” Ex. 1003 [Sechen-Decl.]

¶ 89. None of the examples cited by Petitioner’s declarant, however, refer to the CEB signal *in Ryu’s Figure 5*. Nor do these signals labeled “CEB” in other references and different devices “enabl[e] the [alleged] configurable non-volatile memory device” that Petitioner identifies as Ryu’s Figure 5. Allusions to acronyms in other references cannot permit contradicting the operation of Ryu itself. The fact that some of Petitioner’s expert’s examples from other contexts may be device-enabling signals, *see, e.g.*, Ex. 1026 [Min] [0036] (referring to a “chip enable signal CEB ... [that] enables the semiconductor memory device or chip”), Ex. 1032 [Park] 11:35-36 (referring to a “chip enable signal CEB [being] kept to logic low while the flash memory device 100 executes the data input operation”), for example, does not show that the output-enabling signal CEB in Ryu’s Figure 5 operates to enable the device of Ryu’s Figure 5—and claim 1, of course, recites not simply “a chip enable port configured to receive a chip enable signal,” but “a chip enable port configured to receive a chip enable signal *for enabling the configurable non-volatile memory device*.” Whether a POSITA might recognize abstract “chip enable signals” in other contexts in other references has no bearing upon whether Ryu’s CEB signal functions in Ryu’s disclosed device so as to satisfy this claim limitation, particularly when it in fact does not. Ex. 2026 [Khatri-Decl.] ¶ 39.

Thus, Petitioner has not demonstrated that Ryu discloses or renders obvious “a chip enable port configured to receive a chip enable signal for *enabling* the configurable non-volatile memory device.” Instead, Ryu itself confirms that the CEB signal Petitioner relies upon does *not* enable the alleged configurable non-volatile memory device. Ex. 2026 [Khatri-Decl.] ¶ 40.

2. Petitioner Fails To Show “one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data ... the output data synchronized with the clock output signal in a double data rate configuration.”

Claim 1, the only independent claim in the '028 patent, requires that the same “one or more configurable output buffers” within the claimed “memory device” perform two distinct roles. They must be “configurable to one of a plurality of output buffer drive strengths” and they must also “transfer the output data ... the output data synchronized with the clock output signal in a double data rate configuration.” Ex. 1001 ['028] cl. 1.

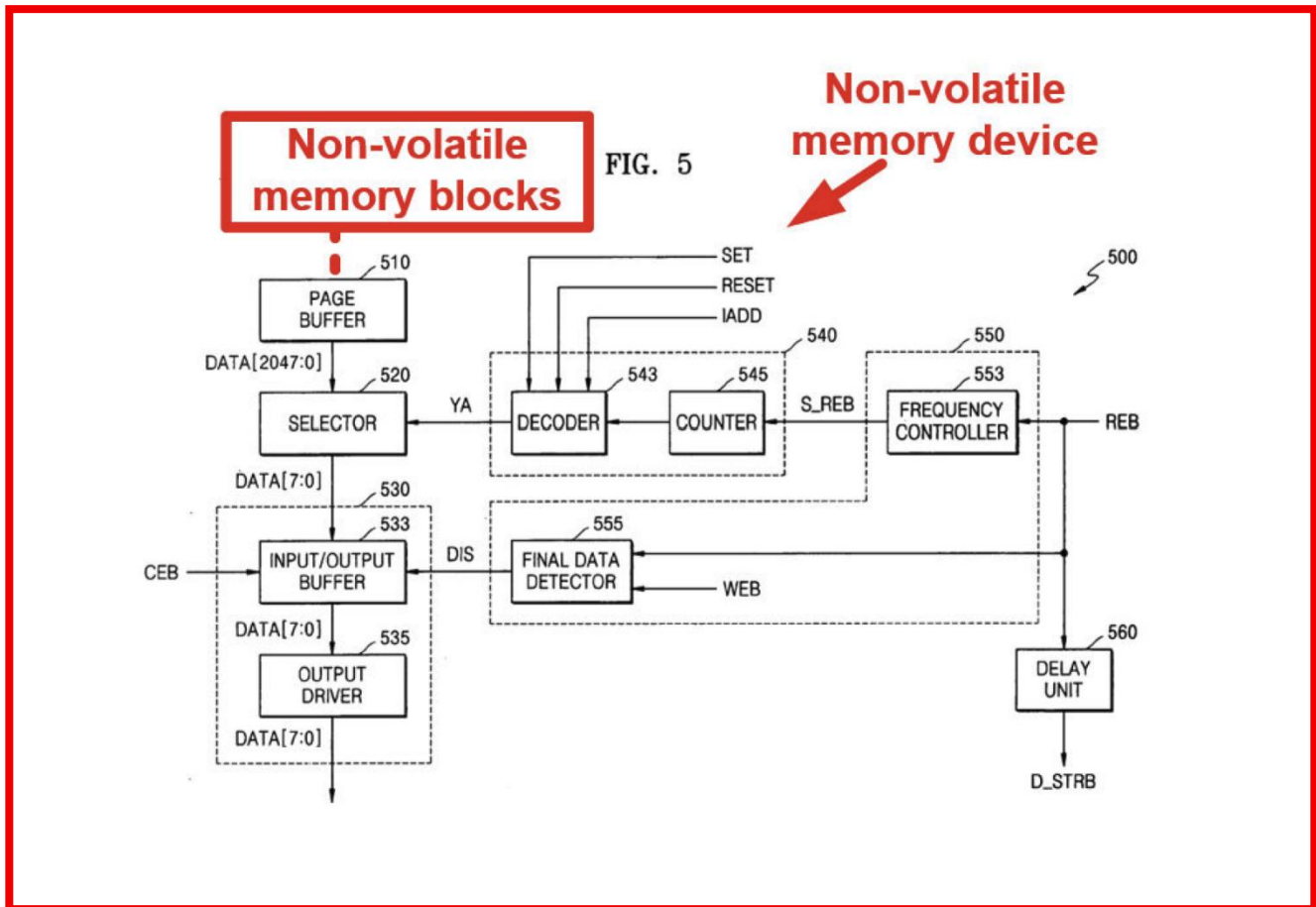
Petitioner contends that this limitation is satisfied by its Ryu-Cole-Arcoleo combination but fails to prove it. Critically, Petitioner fails to identify “one or more configurable output buffers” that perform *both* roles that claim 1 requires. Instead, Petitioner hot swaps between different components, in different references, for the two roles. Initially, Petitioner relies upon Ryu’s output unit 530 to satisfy the “output data synchronized with the clock output signal” language, mapping the “clock output

signal” to Ryu’s D_STRB. Pet., 47. Later, however, when arguing that the claimed “output buffer” is “configurable to one of a plurality of output buffer drive strengths,” Petitioner changes its claim mapping to argue that *Arcoleo*—not Ryu—provides the claimed “output buffer.” Petitioner never argues that the output data transferred by *Arcoleo*’s “output buffer” is synchronized with any alleged “clock output signal,” as the claim requires. And Petitioner never shows that Ryu’s “output buffers” are configurable, again, as the claim requires.

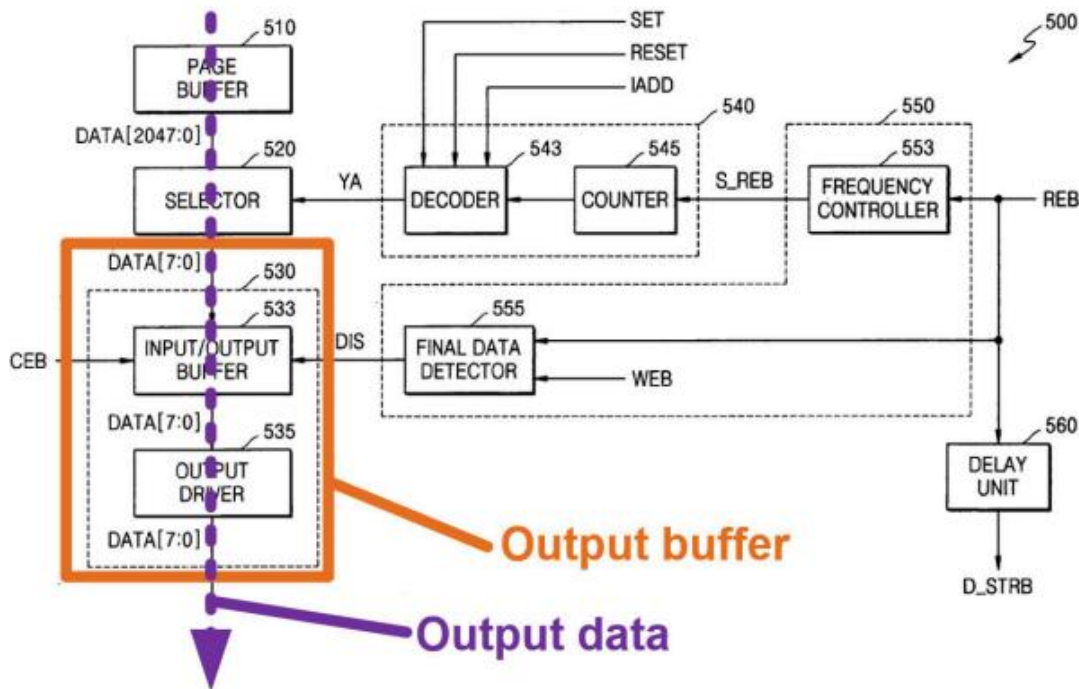
To belabor the crucial point, claim 1 does not recite one or more output buffers, *some* of which might have configurable output buffer drive strengths, and *others* of which might output data synchronized with a clock output signal. Every one of the claimed “output buffers” must be “configurable to one of a plurality of output buffer drive strengths to transfer the output data ... the output data synchronized with the clock output signal in a double data rate configuration.” In switching between the disclosures of Ryu and *Arcoleo* for different parts of this limitation, Petitioner thus fails to show how this limitation is present in its combined system.

- a. *Petitioner Only Contends That “output data” From Ryu’s “output buffer” Is “synchronized with the clock output signal.”*

As already noted, Petitioner identifies the claimed “**memory device**” with the system depicted in Ryu’s Figure 5:



Pet., 25 (Ex. 1004 [Ryu] Fig. 5 (as annotated by Petitioner)). Petitioner maps the claimed “output buffer,” “output data,” and “clock output signal” to Ryu’s output unit (labeled 530 above), Ryu’s DATA[7:0], and Ryu’s D_STRB within Ryu’s Figure 5, respectively:



Pet., 47 (Ryu’s Figure 5, as annotated by Petitioner with Petitioner’s claim mappings).

Petitioner then argues this alleged “output data” is “synchronized with the clock output signal” because Ryu discloses that its D_STRB signal “may be ... output at the same time with the DATA[7:0] to the external source.” *See* Pet., 47 (quoting Ex. 1004 [Ryu] [0064]). Petitioner also argues, citing Ryu, why a POSITA would supposedly have recognized that this alleged synchronization is “in a double data rate configuration.” *See* Pet., 47-48.

This synchronization theory relies exclusively upon Ryu. Petitioner does not identify any “clock output signal” in its combination other than Ryu’s D_STRB, and Petitioner does not argue that anything other than the output of Ryu’s output unit is

“synchronized with” that alleged “clock output signal,” whether in a double data rate configuration or in any other configuration. Pet., 46-50.

b. Petitioner Relies Only On Arcoleo For “configurable” Output Buffer Drive Strengths.

The same limitation of claim 1 also requires “output buffers configurable to one of a plurality of output buffer drive strengths ...” Ex. 1001 [’028] cl. 1. For this aspect of the limitation, Petitioner exclusively relies upon *Arcoleo*. It identifies Arcoleo’s “output buffer drive strength selector” 405 in Figure 4 as providing the claimed configurability of output buffer drive strengths. See, e.g., Pet., 48-50. In doing so, Petitioner now maps the claimed “output buffer” not to Ryu’s output unit but to portions of Arcoleo’s Figure 4:

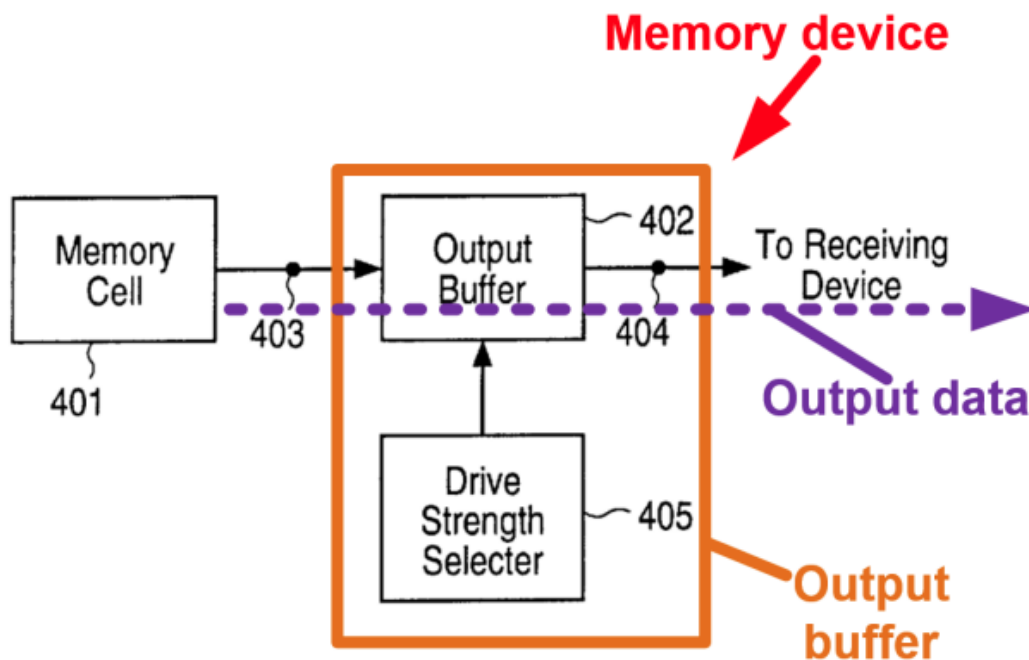


FIG. 4

Pet., 49 (Arcoleo’s Figure 4, annotated by Petitioner, identifying Arcoleo’s output buffer 402 and drive strength selector 405 as an “output buffer”).

While Petitioner phrases these arguments about this limitation as arguments “[t]o the extent [that] Ryu does not expressly disclose that the output buffer is configurable to one of a plurality of output buffer drive strengths,” Pet., 48, Petitioner never argues that Ryu alone expressly discloses an output buffer “configurable to one of a plurality of output buffer drive strengths,” or that Cole does, or that Ryu in combination with Cole does. *See generally* Pet., 46-48. Again, Petitioner *exclusively* relies on Arcoleo for “output buffers configurable to one of a plurality of output buffer drive strengths.” Petitioner thus maps different output buffers, with different inputs, outputs, and circuitry, to the same limitation of claim 1. Yet Petitioner does not describe how these differences would be reconciled or even recognize that there are differences to begin with.

c. Petitioner Does Not Show That Arcoleo’s Alleged “output buffer” Transfers “output data synchronized with the clock output signal.”

While Petitioner’s arguments rely upon its contention that “Arcoleo describes a configurable output buffer that is configurable to one of a plurality of output buffer drive strengths,” Pet., 49-50, Petitioner never even argues—let alone establishes—that any “output data” transferred by Arcoleo’s output buffer is “synchronized with [any] clock output signal in a double data rate configuration,” as required by the

claim. *See generally* Pet., 46-50. Here, again, Petitioner exclusively identifies D_STRB in Ryu with the claimed “clock output signal,” but never makes any argument connecting D_STRB to any timing of any output of Arcoleo’s output buffer. See Section II.B.2.a *supra*.

Accordingly, Petitioner does not show how its Ryu-Cole-Arcoleo combination teaches “one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data ... the output data synchronized with the clock output signal in a double data rate configuration.” At best, Petitioner attempts to argue that an unspecified combination of Ryu and Cole teaches an “output buffer” that transfers output data “synchronized with the clock output signal in a double data rate configuration,” and Petitioner separately attempts to argue that Arcoleo teaches an “output buffer[] configurable to one of a plurality of output buffer drive strengths.” This piecemeal analysis does not show how the limitation is present in Petitioner’s combined system.

C. Petitioner Fails To Show A Motivation To Combine With a Reasonable Expectation Of Success.

Regardless of Petitioner’s need to resort to tertiary references like Arcoleo, Petitioner’s grounds are all founded upon a base combination of Ryu and Cole. Petitioner, however, never adequately explains how these references would be combined. As the Federal Circuit has made clear, however, an obviousness finding

cannot stand without a “clear[] explan[ation]” of “*how* the combination of the two references was supposed to work.” *PersonalWeb Techs. LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017) (emphasis in original). Indeed, “a clear, evidence-supported account of the contemplated workings of the combination *is a prerequisite* to adequately explaining and supporting a conclusion that a relevant skilled artisan would have been motivated to make the combination and reasonably expect success in doing so.” *Id.* Because Petitioner never specifies its combination, Petitioner’s enumerated “motivations” are conclusory and should be rejected.

1. The Ryu-Cole Combination Is Never Reduced To A Coherent Working Architecture.

Petitioner repeatedly characterizes its combination in the same high-level terms—namely, that “a POSITA would have implemented Ryu’s non-volatile memory device to include a configurable input section as suggested by Cole.” *See, e.g., Pet.*, 15; *see also id.*, 14, 16-17 (similar). In other words, Petitioner says a POSITA would make Ryu’s memory device “include” Cole’s configurable input section. But Petitioner never goes on to describe, even at a functional level, how that combined device is supposed to operate.

Petitioner’s element-by-element mapping does not cure this. Petitioner expressly identifies Ryu’s Figure 5 embodiment as the claimed “non-volatile memory device.” *See Pet.*, 25 (annotating Ryu’s Fig. 5). Petitioner then states that

this device is “modified in the combination based on Cole to include ‘an input section’...” and maps the entirety of limitation [1c]—requiring first and second clock input ports and corresponding first and second clock input signals—and the entirety of limitation [1f]—requiring a configurable clock input buffer that utilizes those signals—to that “input section” attributed to Cole. *See, e.g.,* Pet., 27-31, 41-46.

To support those mappings, Petitioner cites passages from Cole describing how Cole’s configurable input section receives strobe inputs, controls latch banks, and routes data through input data paths. *See, e.g.,* Pet. 27-31 (citing Ex. 1005 [Cole]). But Petitioner never explains which functional blocks in the combined Ryu-Cole device are performing which claimed roles, or how Ryu’s existing control and data signals would interact with Cole’s strobe inputs and latch banks. To be clear, although Petitioner’s burden may not include fully drafting schematics of all circuitry that a “Ryu-Cole” might employ, Petitioner must, at a minimum, indicate which parts of Ryu and which parts of Cole are implicated in the “Ryu-Cole” system that it claims a POSITA would supposedly be motivated to create, and how those parts connect together, at least functionally, in a single design. That description is missing.

The omission is most evident in Petitioner’s treatment of Ryu’s D_STRB signal and Cole’s xxStbP signal. Petitioner asserts that “Ryu’s D_STRB signal

provides a ***clock output signal*** as claimed.” Pet., 32 (emphasis in original). As Petitioner itself recognizes, Ryu expressly discloses that D_STRB is generated by delaying either (1) Ryu’s read control signal or (2) Ryu’s flash clock signal. *See* Pet., 35-36; *see also id.*, 32; Ex. 2026 [Khatri-Decl.] ¶ 54. In other words, absent modifications to be explained by Petitioner, Ryu’s existing D_STRB is referenced to timing signals that are present in Ryu and provided to the Figure 5 embodiment of Ryu. *Cf.* Pet., 35 (citing Ex. 1004 [Ryu] [0094]) (“Ryu expressly discloses that D_STRB is generated by ‘delaying the flash clock signal F_CLK by a predetermined time,’ meaning that Ryu specifically contemplates D_STRB being referenced to a flash clock signal”); *see also* Pet., 35 (citing Ex. 1004 [Ryu] [0064]) (“D_STRB may [be] created by delaying the read control signal REB”). Ex. 2026 [Khatri-Decl.] ¶ 54.

In the combination, however, Petitioner, maps the claimed “first clock signal” to Cole’s “xxStbP” signal. To satisfy limitation [1d]—which recites “the clock output signal [being] referenced to the first clock input signal”—Petitioner contends that a POSITA would have found it obvious to reference Ryu’s D_STRB signal (clock output signal) to one of Cole’s complementary strobe input signals, such as xxStbP, so that the D_STRB signal can be used by external device(s) as an indication of the exact timing of values in the output data presented at the input-output pin (IOP).” Pet., 36. Petitioner never explains how a POSITA would actually modify

Ryu's design to achieve that—*i.e.*, what becomes of the existing REB/F_CLK-based generation of D_STRB, or how D_STRB is now a function of xxStbP rather than REB or F_CLK in the combined system. Petitioner does not, for example, explain any modifications to Ryu's memory controller, or other components of Ryu, that would allow them to operate off of a new clock "xxStbP" in Ryu's Figure 5, in addition to (or instead of) their existing clocking in Ryu's Figure 5. Ex. 2026 [Khatri-Decl.] ¶ 55.

Nor does Petitioner reconcile the very different roles these signals play in the two references. As Petitioner acknowledges, "Cole explains that the 'strobe inputs 12 [xxStbP and xxStbN] are provided by the source of the data being transferred.'" Pet., 28 (citing Ex. 1005 [Cole] [0020]). In Cole, that is, Cole's strobe inputs accompany incoming data from an external source—a source that is not specified, but is configured to interact with Cole's system and provide xxStbP and xxStbN inputs to that system in the course of transferring data into Cole. Ex. 2026 [Khatri-Decl.] ¶ 56.

By contrast, in the portions of Ryu relied upon by Petitioner, "read control signal REB" and F_CLK are signals used for controlling a read of data that is already stored on Ryu's memory device (and thus are not provided along with external data from an external source into the Ryu's Figure 5). *See generally* Ex. 1004 [Ryu] [0042], [0045], [0047]-[0048], [0066]; *see also* Ex. 2026 [Khatri-Decl.] ¶ 57.

Similarly, Ryu's F_CLK signal is an input to Ryu's system "and generates a sub flash clock signal S_REB." Ex. 1004 [Ryu] [0080]. Ryu's REB and F_CLK are used to control the output of data from Ryu's memory device to Ryu's memory controller (not to Cole's external source); they are issued by Ryu's controller to request reads and time data output *from* Ryu's Figure 5 device, not to accompany a transmission of data *into* Ryu's Figure 5 device. Ex. 2026 [Khatri-Decl.] ¶ 57; *see also, e.g.*, Ex. 1004 [Ryu] [0048], [0072]; *see also* Pet., 59 (quoting Ex. 1004 [Ryu] [0005]) ("[a] controller...applies a read control signal REB to the non-volatile memory device to receive data during a read operation").

Functionally, then, Petitioner's [1d] theory requires D_STRB in the combined device to be referenced to a *different kind of signal* (Cole's data strobe inputs which accompany incoming data) than in Ryu (the controller's read control signal REB, or the Ryu system's flash clock F_CLK, which are for *outgoing* data). But Petitioner does not explain how Ryu's memory controller (or other components) would be modified as to produce Cole's signals. Ex. 2026 [Khatri-Decl.] ¶ 58.

Similarly, for limitation [1g], Petitioner asserts that "Ryu's output data is both edge aligned and synchronized with the clock output signal ('D_STRB') in a double data rate configuration." Pet., 47. This would again result in a fundamental incompatibility, since portions of the design (corresponding to [1g]) operate using the D_STRB, while other portions of the design (corresponding to 1[d]) operate

using Cole's clocking. Given that the sources of these two clocks are different, and their relative phase and timing are not disclosed by Petitioner, the combined design is doomed to fail.

In other words, to meet [1d], Petitioner assumes a modified Ryu in which D_STRB is referenced to a "xxStbP" signal from Cole that replaces Ryu's REB or F_CLK signals, while to meet [1g], Petitioner returns to an unmodified Ryu in which D_STRB is generated by delaying REB and the data is timed off REB edges. Petitioner never articulates any single, consistent way a POSITA would resolve that electrical conflict, or discuss what the various timing relationships between the disparate clocks would be in "Ryu-Cole." Ex. 2026 [Khatri-Decl.] ¶¶ 61-62.

Petitioner has therefore failed to do what *PersonalWeb* requires: provide a clear, evidence-supported account of how the teachings of Ryu and Cole would be implemented together so that a POSITA could reasonably expect the combined design to work. Instead, Petitioner stitches together favorable pieces of Ryu and Cole in a way that cannot all be true at once. Under *PersonalWeb*, that failure to articulate a coherent combined architecture is fatal to any finding that a POSITA would have been motivated to make the combination with a reasonable expectation of success.

2. Petitioner's Asserted Motivations Are Conclusory.

Petitioner offers a list of five “reasons [that] would have prompted a POSITA to integrate a configurable input section that can be selectively configured to a single ended signal mode or a differential signaling mode as suggested by Cole in the non-volatile memory device of Ryu.” Pet., 14-15. As explained above, however, *PersonalWeb* requires a clear, evidence-supported account of how the contemplated Ryu-Cole aspects of its combinations are supposed to work before any motivation or reasonable expectation of success can be found. *See* Section II.C.1 *supra*. Petitioner never articulates such a working architecture, so its “predictable results” theory is already unsupported. In any event, each of Petitioner’s five asserted “reasons” independently fails.

First, Petitioner contends that “a POSITA would have pursued the combination to achieve interoperability between Ryu’s device and other devices regardless of the type of signaling employed.” Pet., 15. According to Petitioner, this “would have been beneficial to allow Ryu’s nonvolatile memory device to toggle between the single ended signaling mode and the differential signaling mode so that these modes ‘co-exist and co-operate with each other in the same system.’” *Id.*, 15 (citing Ex. 1005 [Cole] [0002]).

But Petitioner’s explanation that this “interoperability” would be beneficial is unexplained. Cole explains that its input section would be useful when “integrated

circuits of the different types...must co-exist and co-operate with each other in the same system.” Petitioner doesn’t explain why this scenario, for use in the context such as the input section of an IC “such as a CPU and/or chipset,” *see* Ex. 1005 [Cole] [0013], presents itself in the context of Ryu’s device, or would otherwise provide any benefit to Ryu’s memory device. Petitioner never identifies any such any “integrated circuits of . . . different types” in Ryu’s memory device, never identifies what “other devices” in Ryu’s system would require different signaling modes, and never explains why a POSITA would redesign Ryu’s interface. The asserted “interoperability” benefit is therefore an abstract statement about Cole, not tethered to how Petitioner is proposing to modify Ryu. Ex. 2026 [Khatri-Decl.] ¶ 65.

Second, Petitioner contends that a “POSITA would have implemented Ryu’s non-volatile memory device to include a configurable input section as suggested by Cole to allow the memory device to receive data signals according to either a single-ended or differential mode signaling configuration.” Pet., 15. Here, Petitioner simply restates the desired result of Petitioner’s combination—the claimed functionality. Ex. 2026 [Khatri-Decl.] ¶ 66. Petitioner effectively says that a POSITA would be motivated to combine Ryu and Cole so that the combined system would satisfy the claim—a prototypical example of hindsight-based analysis, not evidence of any motivation to combine. *Apple, Inc. v. Voip-pal.com, Inc.*, IPR2016-01198, Paper 53 (Final Written Decision) at 23 (Nov. 20, 2017) (“Petitioner’s

position ... is not grounded in what a skilled artisan would have gleaned from the teachings of the prior art, and is instead an impermissible exercise of hindsight with the claims ... serving as a guide”).

Third, Petitioner argues that a POSITA “would have implemented Ryu’s memory device with a configurable input section as suggested by Cole to allow the memory device to efficiently latch received data regardless of whether the received data is signaled using either a single-ended or differential signaling scheme.” Pet., 16. This rationale presupposes two things that Petitioner never supports: (i) that Ryu’s memory device would, in practice, be required to receive data using single-ended and differential signaling (or would advantageously be used in such a context), and (ii) that adding Cole’s configurable input section to Ryu’s device would be an “efficient” way to meet that hypothetical requirement. Petitioner cites no evidence of any latching “inefficiency” in Ryu or any need to handle both signaling modes at the memory-device pins. *See* Ex. 2026 [Khatri-Decl.] ¶ 67. Without presenting any arguments that support this, Petitioner’s “efficiency” label is pure *ipse dixit*. Even if that could be overlooked, a generalized desire to improve a device is not a motivation to combine. *See, e.g., ActiveVideo Networks, Inc. v. Verizon Commc’ns, Inc.*, 694 F.3d 1312, 1327-28 (Fed. Cir. 2012) (finding a generic motivation to “build something better” or “more efficient, cheaper,” etc. to be “insufficient”); *Samsung Elecs. Co., Ltd. v. Red Rock Analytics, LLC*, IPR2018-00556, Paper 18, 21 (Aug. 20,

2018) (“statements of increased utility and minimal modifications are generic, and fail to provide necessary factual support—they are akin to stating in a conclusory fashion that the combination ‘would have been obvious.’”); *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-00582, Paper 34, 21-22 (Aug. 5, 2019) (informative) (“Petitioner’s reliance on a generic desire for ‘improved access times’ in the Reply strikes us as merely a bald statement about what could have been achieved at the time of the invention.”).

Fourth, Petitioner argues that “a POSITA would have been motivated to implement the memory device of Ryu with a configurable input section that receives two complementary strobe input signals as taught by Cole (e.g., xxStbP, xxStbN) to enable generation of internal strobe signals according to either of a single-ended or differential signaling mode.” Pet., 17. Here, Petitioner recites an aspect of Cole—using complementary strobes to generate internal strobes—but never explains why a POSITA working with Ryu’s architecture would choose to restructure Ryu’s interface in that manner. Ryu already discloses its own scheme for generating and using D_STRB based on REB or F_CLK. Ex. 1004 [Ryu] [0064], [0066], [0094]. Petitioner does not identify any shortcomings in Ryu’s design, or any incentive to replace its design with Cole’s design. Ex. 2026 [Khatri-Decl.] ¶ 68.

Finally, Petitioner invokes *KSR* and *Intel* to contend that “a POSITA would have found it obvious to combine the teachings of Ryu with Cole because the

combination merely involves the application of a known technique to a known system to achieve predictable results... ‘It’s enough... to show that there was a known problem... in the art, that [another known teaching] ... helped address that issue, and that combining the teachings of ... wasn’t beyond the skill of an ordinary artisan. Nothing more is required to show a motivation to combine under *KSR*.’” Pet., 18 (citing *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81, (Fed. Cir. 2023)). Even crediting Petitioner’s characterization of Cole, *arguendo*, Petitioner never shows that this alleged “problem” is present in Ryu’s system, or that a POSITA would otherwise perceive Ryu’s memory device as a candidate for Cole’s supposed solution. Ex. 2026 [Khatri-Decl.] ¶ 69. Consequently, Petitioner does not substantiate its premise that Cole’s configurable logic addresses any problem in Ryu.

Therefore, even if Petitioner had adequately stated its combination, Petitioner’s alleged motivations for a POSITA to arrive at that combination are conclusory. But obviousness cannot be shown by conclusory statements. *See In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”). Thus, Petitioner fails to prove obviousness.

III. CONCLUSION

For the foregoing reasons, the Board should not institute trial.

Respectfully submitted,

Dated: December 10, 2025

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CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITS

This Patent Owner Preliminary Response (the “POPR”) consists of 6,743 words, excluding table of contents, table of authorities, certificate of service, this certificate, or table of exhibits. The POPR complies with the type-volume limitation of 14,000 words as mandated in 37 C.F.R. § 42.24. In preparing this certificate, counsel has relied on the word count of the word-processing system used to prepare the paper (Microsoft Word).

Respectfully submitted,

Dated: December 10, 2025

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the following documents were served by electronic service, by agreement between the parties, on the date below:

PATENT OWNER'S PRELIMINARY RESPONSE

EXHIBIT 2026

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