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Tony Zhou

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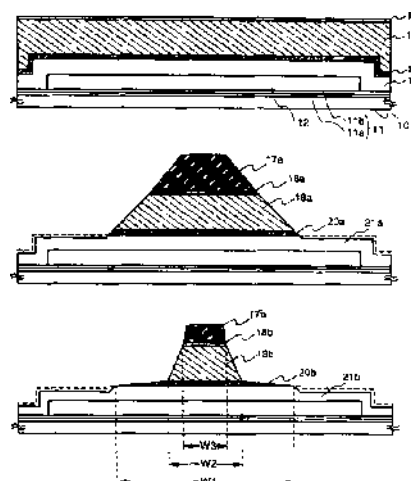
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[57] Abstract

The wiring of the present invention has a stacked structure, which includes a first conductive layer (first layer) having a first width, made of one or more elements selected from W and Mo, or alloys or compounds primarily consisting of these elements; a low-resistance second conductive layer (second layer) with a second width smaller than the first width, made of an alloy or compound primarily consisting of Al; and a third conductive layer (third layer) with a third width smaller than the second width, made of an alloy or compound primarily consisting of Ti. Adopting this structure provides ample room for the expansion of the pixel segment in the present invention. At least the edge of the second conductive layer is characterized by a tapered cross-section. Due to this shape, satisfactory coverage can be achieved.



1. A wiring having a stacked structure, the wiring comprising a first conductive layer having a first width as the first layer, a second conductive layer having a second width as the second layer, with the second width being smaller than the first width, and a third conductive layer having a third width as the third layer, with the third width being smaller than the second width.
- Wherein the cross section of the edge of the first, second, or third conductive layer is tapered.
2. The wiring according to claim 1, wherein the first conductive layer comprises at least one selected from W and Mo.
3. The wiring according to claim 1, wherein the second conductive layer comprises Al.
4. The wiring according to claim 1, wherein the third conductive layer comprises Ti.
5. The wiring according to claim 1, wherein the second conductive layer is covered with the first conductive layer, the third conductive layer, and the insulating film, and the region contacting the insulating film is oxidized.
6. The wiring according to claim 1, wherein the wiring is used for at least one selected from a liquid crystal display device and a light-emitting device.
7. A method for manufacturing wiring, comprising the steps of:
- forming a first-shaped conductive layer comprising a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;
- Etching the first conductive layer, the second conductive layer, and the third conductive layer to form a second-shaped conductive layer, which includes a stack composed of the first conductive layer of a first width, the second conductive layer of a second width, and the third conductive layer of a third width; and
- Etching the second conductive layer of a second width and the third conductive layer of a third width to form a third-shaped conductive layer, which includes a stack composed of the first conductive layer of a fourth width, the second conductive layer of a fifth width, and the third conductive layer of a sixth width.
- Wherein the edge cross-section of the first conductive layer, the second conductive layer, or the third conductive layer is trapezoidal.
8. A method for manufacturing wiring, comprising the steps of:
- forming a first-shaped conductive layer comprising a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;
- Etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer, which includes a stack of the first conductive layer, the second conductive layer of the first width, and the third conductive layer of the second width;
- Etching the first conductive layer to form a third-shaped conductive layer, which includes a stack of a first conductive layer of the third width, a second conductive layer of the first width, and a third conductive layer of the second width; and

Etching the second conductive layer of the first width and the third conductive layer of the second width to form a fourth-shaped conductive layer, which includes a stack of the first conductive layer of the fourth width, the second conductive layer of the fifth width, and the third conductive layer of the sixth width,

The edge cross-section of the first conductive layer, the second conductive layer, or the third conductive layer is of a tapered shape.

9. A method for manufacturing wiring, comprising the steps of:

forming a first-shaped conductive layer comprising a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

Etching the first conductive layer, the second conductive layer, and the third conductive layer to form a second-shaped conductive layer, which includes a stack of a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width;

Etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer, which includes a stack of the first conductive layer with the fourth width, the second conductive layer with the fifth width, and the third conductive layer with the sixth width; and

Performing plasma treatment on the third-shaped conductive layer,

The edge cross-section of the first conductive layer, the second conductive layer, or the third conductive layer is of a tapered shape.

10. A method for manufacturing wiring, comprising the steps of:

forming a first-shaped conductive layer comprising a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

Etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer, which includes a stack of the first conductive layer, the second conductive layer of the first width, and the third conductive layer of the second width;

Etching the first conductive layer to form a third-shaped conductive layer, which includes a stack of a first conductive layer with a third width, a second conductive layer with a first width, and a third conductive layer with a second width;

Etching the second conductive layer of the first width and the third conductive layer of the second width to form a fourth-shaped conductive layer, which includes a stack of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width; and

Performing plasma treatment on the fourth-shaped conductive layer,

The edge cross-section of the first conductive layer, the second conductive layer, or the third conductive layer is of a tapered shape.

11. The method for manufacturing wiring according to any one of claims 7 to 10, wherein the first conductive layer comprises at least one selected from W and Mo.

12. The method for manufacturing wiring according to any one of claims 7 to 10, wherein the second conductive layer comprises Al.
13. The method for manufacturing wiring according to any one of claims 7 to 10, wherein the third conductive layer comprises Ti.
- 5 14. The method for manufacturing wiring according to any one of claims 7 to 10, wherein oxygen or a gas, or H₂O, mainly containing oxygen is used, or plasma treatment is performed.
15. A wiring board comprising an insulating substrate and wiring,
wherein the wiring has a stacked structure comprising a first conductive layer having a first width as the first layer, a second conductive layer having a second width as the second layer, with the second width being smaller
10 than the first width, and a third conductive layer having a third width as the third layer, with the third width being smaller than the second width.
- Wherein the cross section of the edge of the first, second, or third conductive layer is tapered.
16. The wiring board according to claim 15, wherein the first conductive layer comprises at least one of W and Mo.
- 15 17. The wiring board according to claim 15, wherein the second conductive layer comprises Al.
18. The wiring board according to claim 15, wherein the third conductive layer comprises Ti.
19. The wiring board according to claim 15, wherein the second conductive layer is covered by the first conductive layer, the third conductive layer, and the insulating film, and the region in contact with the insulating film is oxidized.
- 20 20. The wiring board according to claim 15, wherein a liquid crystal display device or a light-emitting device is manufactured using the wiring board.
21. A method for manufacturing a wiring board, comprising the steps of:
forming a first-shaped conductive layer comprising a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;
25 etching the first conductive layer, the second conductive layer, and the third conductive layer to form a second-shaped conductive layer, which includes a stack composed of a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width;
and etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer, which includes a stack composed of a first conductive layer with a
30 fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width,
wherein the cross-section of the edges of the first conductive layer with the fourth width, the second conductive layer with the fifth width, or the third conductive layer with the sixth width is tapered in shape.
22. A method for manufacturing a wiring board, the method comprising the steps of:

forming a first-shaped conductive layer, which comprises a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

Etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer, which includes a stack of the first conductive layer, the second conductive layer of the first width, and the third conductive layer of the second width;

etching the first conductive layer to form a third-shaped conductive layer, which comprises a stack composed of a first conductive layer having a third width, a second conductive layer having a first width, and a third conductive layer having a second width; and

Etching the second conductive layer of the first width and the third conductive layer of the second width to form a fourth-shaped conductive layer, which includes a stack of the first conductive layer of the fourth width, the second conductive layer of the fifth width, and the third conductive layer of the sixth width,

wherein the cross-section of the edges of the first conductive layer with the fourth width, the second conductive layer with the fifth width, or the third conductive layer with the sixth width is tapered in shape.

23. A method for manufacturing a wiring board, the method comprising the steps of:

forming a first conductive layer on an insulating surface;

forming a second conductive layer on the first conductive layer;

forming a third conductive layer on the second conductive layer;

etching the first to third conductive layers to form a conductive layer having tapered sections;

and performing plasma treatment on the conductive layer having tapered sections.

24. A method for manufacturing a wiring board, the method comprising the steps of:

forming a first-shaped conductive layer, which includes a stack composed of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

Etching the first conductive layer, the second conductive layer, and the third conductive layer to form a second-shaped conductive layer, which includes a stack of a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width;

Etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer, which includes a stack of the first conductive layer with the fourth width, the second conductive layer with the fifth width, and the third conductive layer with the sixth width; and

Performing plasma treatment on the third-shaped conductive layer,

wherein the cross-section of the edges of the first conductive layer with the fourth width, the second conductive layer with the fifth width, or the third conductive layer with the sixth width is tapered in shape.

25. A method for manufacturing a wiring board, the method comprising the steps of:

forming a first-shaped conductive layer, which comprises a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

Etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer, which includes a stack of the first conductive layer, the second conductive layer of the first width, and the third conductive layer of the second width;

Etching the first conductive layer to form a third-shaped conductive layer, which includes a stack of a first conductive layer with a third width, a second conductive layer with a first width, and a third conductive layer with a second width;

Etching the second conductive layer of the first width and the third conductive layer of the second width to form a fourth-shaped conductive layer, which includes a stack of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width; and

Performing plasma treatment on the fourth-shaped conductive layer,

wherein the cross-section of the edges of the first conductive layer with the fourth width, the second conductive layer with the fifth width, or the third conductive layer with the sixth width is tapered in shape.

26. The method for manufacturing a wiring board according to any one of claims 21 to 25, wherein the first conductive layer includes at least one selected from W and Mo.

27. The method for manufacturing a wiring board according to any one of claims 21 to 25, wherein the second conductive layer comprises Al.

28. The method for manufacturing a wiring board according to any one of claims 21 to 25, wherein the third conductive layer comprises Ti.

29. A method for manufacturing a wiring board according to any one of claims 21 to 25, wherein plasma treatment is performed using oxygen, a gas mainly containing oxygen, or H₂O.

30. A semiconductor device, comprising:

a semiconductor layer on a substrate;

a gate insulating film on the semiconductor layer;

The wiring on the gate insulating film has a stacked structure, including a first conductive layer with a first width as the first layer, a second conductive layer with a second width as the second layer, where the second width is smaller than the first width, and a third conductive layer with a third width as the third layer, where the third width is smaller than the second width.

Wherein the cross section of the edge of the first, second, or third conductive layer is tapered.

31. A semiconductor device according to claim 30, wherein the first conductive layer comprises at least one selected from W and Mo.

32. The semiconductor device according to claim 30, wherein the second conductive layer comprises Al.

33. A semiconductor device according to claim 30, wherein the third conductive layer comprises Ti.

34. A semiconductor device according to claim 30, wherein the second conductive layer is covered by the first conductive layer, the third conductive layer, and an insulating film, and the region contacting the insulating film is oxidized.

35. A semiconductor device according to claim 30, wherein the semiconductor device is at least one selected from either a liquid crystal display device or a light-emitting device.

36. A semiconductor device according to claim 30, wherein the semiconductor device is at least one selected from a personal computer, a player using a recording medium, and a display.

37. A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a semiconductor layer on a substrate;

forming a gate insulating film on the semiconductor layer;

forming a first-shaped conductive layer consisting of a stack of a first conductive layer, a second conductive layer, and a third conductive layer on the gate insulating film;

etching the first conductive layer, the second conductive layer, and the third conductive layer to form a second-shaped conductive layer consisting of a stack of a first conductive layer of a first width, a second conductive layer of a second width, and a third conductive layer of a third width; and

and etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer, which includes a stack composed of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width,

Wherein the cross section of the edge of the first, second, or third conductive layer is tapered.

38. A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a semiconductor layer over a substrate;

forming a gate insulating film on the semiconductor layer;

forming a first-shaped conductive layer consisting of a stack of a first conductive layer, a second conductive layer, and a third conductive layer on the gate insulating film;

Etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer, which includes a stack of the first conductive layer, the second conductive layer of the first width, and the third conductive layer of the second width;

etching the first conductive layer to form a third-shaped conductive layer, which comprises a stack composed of a first conductive layer having a third width, a second conductive layer having a first width, and a third conductive layer having a second width; and

Etching the second conductive layer of the first width and the third conductive layer of the second width to form a fourth-shaped conductive layer, which includes a stack of the first conductive layer of the fourth width, the second conductive layer of the fifth width, and the third conductive layer of the sixth width,

Wherein the cross section of the edge of the first, second, or third conductive layer is tapered.

39. A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a semiconductor layer over a substrate;

forming a gate insulating film on the semiconductor layer;

5 forming a first-shaped conductive layer consisting of a stack of a first conductive layer, a second conductive layer, and a third conductive layer on the gate insulating film;

Etching the first conductive layer, the second conductive layer, and the third conductive layer to form a second-shaped conductive layer, which includes a stack of a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width;

10 etching a second conductive layer of a second width and a third conductive layer of a third width to form a third-shaped conductive layer, which comprises a stack consisting of a first conductive layer of a fourth width, a second conductive layer of a fifth width, and a third conductive layer of a sixth width; and

Performing plasma treatment on the third-shaped conductive layer,

Wherein the cross section of the edge of the first, second, or third conductive layer is tapered.

15 40. A method for manufacturing a semiconductor device, the method comprising the steps of:

forming a semiconductor layer over a substrate;

forming a gate insulating film on the semiconductor layer;

forming a first-shaped conductive layer consisting of a stack of a first conductive layer, a second conductive layer, and a third conductive layer on the gate insulating film;

20 Etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer, which includes a stack of the first conductive layer, the second conductive layer of the first width, and the third conductive layer of the second width;

25 Etching the first conductive layer to form a third-shaped conductive layer, which includes a stack of a first conductive layer with a third width, a second conductive layer with a first width, and a third conductive layer with a second width;

Etching the second conductive layer of the first width and the third conductive layer of the second width to form a fourth-shaped conductive layer, which includes a stack of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width; and

Performing plasma treatment on the fourth-shaped conductive layer,

30 Wherein the cross section of the edge of the first, second, or third conductive layer is tapered.

41. The method for manufacturing a semiconductor device according to any one of claims 37 to 40, wherein the first conductive layer includes at least one selected from W and Mo.

42. The method for manufacturing a semiconductor device according to any one of claims 37 to 40, wherein the second conductive layer comprises Al.

43. A method for manufacturing a semiconductor device according to any one of claims 37 to 40, wherein the third conductive layer comprises Ti.

5 44. A method for manufacturing a semiconductor device according to any one of claims 37 to 40, wherein plasma treatment is performed using oxygen, a predominantly oxygen-containing gas, or H₂O.

45. A method for manufacturing a semiconductor device according to any one of claims 37 to 40, wherein the semiconductor device is at least one selected from a liquid crystal display device and a light-emitting device.

10 46. A method for manufacturing a semiconductor device according to any one of claims 37 to 40, wherein the semiconductor device is at least one selected from a personal computer, a media playback device using a recording medium, and a display.

Wiring and methods for manufacturing wiring, as well as wiring boards and methods for manufacturing wiring boards

Technical Field

5 This invention relates to wiring formed using thin-film technology and methods for manufacturing such wiring. The present invention also relates to wiring boards and methods for manufacturing such wiring boards. In this specification, a wiring board refers to an insulating substrate made of materials such as special-purpose glass or various substrates having wiring formed using thin-film technology.

Background Technology

10 In recent years, technology for forming thin-film transistors (TFTs) using semiconductor thin films (with a thickness of approximately several to several hundred nanometers) on substrates with insulating surfaces has attracted attention. TFTs are widely used in electronic devices such as integrated circuits (ICs) and electro-optical instruments. In particular, TFTs are being rapidly developed as switching elements for image display devices.

15 Typically, liquid crystal display devices are known as image display devices. Compared to passive-type liquid crystal display devices, active matrix-type liquid crystal display devices are increasingly being used because they provide higher-resolution images. In active matrix-type liquid crystal display devices, pixel electrodes arranged in a matrix are driven to form display patterns on the screen. More specifically, a voltage is applied between a selected pixel electrode and a counter electrode corresponding to the pixel electrode, thereby optically modulating the liquid crystal layer disposed between the pixel electrode and the counter electrode. This optical modulation is perceived
20 by an observer as a displayed pattern.

 Such active matrix-type liquid crystal display devices have been widely used, and there is an increasing demand for high precision, high aperture ratio, high stability, and larger screen sizes. There is also a demand for improving productivity and reducing costs.

25 When aluminum (Al) is used as the wiring material to manufacture the said TFTs, heat treatment may lead to the formation of protrusions such as bumps and whiskers. Al atoms can diffuse into the insulating film and the active region (particularly the channel formation region), which may result in TFT operational failures or degradation of its electrical characteristics.

30 In such cases, heat-resistant metal materials have been considered (typically, metal elements with high melting points, such as tungsten (W) and molybdenum (Mo)). However, the resistance of these elements is significantly higher compared to that of Al (see Table 1).

Table 1

Wiring Materials	Resistivity ($\mu\Omega\text{cm}$)
Al	2
W	10-20
Mo	15-25

Therefore, as screen size increases, line delay becomes an issue. In view of this, methods of reducing resistance by increasing the thickness of the wiring have been considered. However, as the wiring width increases, the design freedom and the aperture ratio of the pixel segment decrease. Furthermore, increasing the film thickness of the wiring is likely to cause short circuits at sections where the wirings three-dimensionally intersect, and the coverage at wiring step sections may also decrease.

Summary of the Invention

Therefore, in view of the above circumstances, an object of the present invention is to provide wiring that facilitates screen enlargement and a method for manufacturing such wiring, as well as to provide a wiring board and a method for manufacturing the wiring board.

According to the present invention, the wiring is a stacked structure, which includes: As the first layer, a conductive film primarily containing one or more elements selected from W and Mo; as the second layer, a low-resistance conductive film primarily containing Al; and as the third layer, a conductive film primarily containing Ti, thereby aiming to reduce wiring resistance. According to the present invention, the low-resistance conductive film primarily containing Al is sandwiched between other conductive films, thereby preventing the formation of protrusions such as bumps and whiskers caused by heat treatment. Furthermore, since the first and second layers are made of high melting point conductive films, they function as Al barriers, which prevent Al atoms from diffusing into the insulating film and active region (Table 2). Additionally, when an insulating film is formed on the wiring of the present invention and contact is formed with the wiring, the third layer acts as a stopper against the etching of the insulating film, thereby facilitating contact formation. When Al comes into contact with an ITO film (a typical transparent conductive film), Al causes electrochemic Al corrosion, leading to an increase in contact resistance. However, the third layer is made of a conductive film primarily containing Ti, resulting in satisfactory contact resistance.

Table 2

Wiring Materials	Melting Point [$^{\circ}\text{C}$]
Al	660.4
W	3387
Mo	2610
Ti	1675

Additionally, according to the present invention, the edges of the second layer, which is at least composed of a low-resistance conductive film mainly containing Al, are tapered. Due to this tapered shape, the coverage over step sections is improved. In this specification, the taper angle refers to the angle formed between the horizontal surface and the side surface of a material layer. Moreover, in this specification, for convenience, the side surface with a taper angle is referred to as a beveled shape, and the tapered section is referred to as a tapered segment.

The structure disclosed in this specification concerning the present invention relates to a stacked structure wiring, which includes a first conductive layer having a first width as the first layer, a second conductive layer with a second width smaller than the first width as the second layer, and a third conductive layer with a third width smaller than the second width as the third layer. It is characterized by the tapered cross-sectional shape of the edge of the first, second, or third conductive layers.

In the aforementioned structure, the wiring is characterized by a stacked structure, comprising a conductive layer (first layer) made of an alloy or compound primarily containing W, a conductive layer (second layer) made of an alloy or compound primarily containing Al, and a conductive layer (third layer) made of an alloy or compound primarily containing Ti. In another scenario, the wiring is characterized by a stacked structure, which includes a conductive layer (first layer) made of an alloy or compound primarily containing Mo, a conductive layer (second layer) made of an alloy or compound primarily containing Al, and a conductive layer (third layer) made of an alloy or compound primarily containing Ti. For example, materials such as W, WN, Mo, or other similar materials may be used as the first layer. As the second layer, materials such as Al, Al-Si (2 wt%), Al-Ti (1 wt%), Al-Nd (1 wt%), Al-Sc (0.18 wt%), or other similar materials may be used. As the third layer, materials such as Ti, TiN, or other similar materials may be used. These layers can be formed by methods such as sputtering, plasma CVD, or similar techniques. Moreover, when forming Al-Si or similar materials in the second layer, there is a limitation on the ratio at which elements such as Si can dissolve into Al (solid solubility limit). This is because higher solubility leads to an increase in electrical resistance and changes in thermal resistance. Therefore, those skilled in the art can appropriately determine the ratio of Si or similar materials to Al based on the electrical resistance and thermal resistance suitable for wiring, as well as the solid solubility limit of an element such as Si.

Table 3 shows examples of resistance in each conductive layer constituting the wiring. From Table 3, it is understood that the conductive layers made from alloys or compounds primarily containing Al exhibit significantly lower resistance compared to other conductive layers.

Table 3

Wiring Materials		Resistivity ($\mu\Omega\text{cm}$)
Materials primarily containing W	W	10-20
	WN	150-220
Materials primarily containing Al	Al	2
	Al-Si (2wt%)	3.5 - 4.5
	Al-Ti (1wt%)	8-10
	Al-Nd (1wt%)	7-10
	Al-Sc (0.18wt%)	3.5 - 4.0
Materials primarily containing Ti	Ti	50 - 60
	TiN	130 - 200

Any etching method may be used, provided that the first, second, and third conductive films with thermal resistance and electrical conductivity can be etched at a high speed and with good accuracy, and the edge sections of the films can be tapered. Among these, dry etching methods utilizing high-density plasma are preferred. Etching devices using microwave, helicon wave plasma (HWP), or inductively coupled plasma (ICP) are suitable for obtaining high-density plasma. For example, an electron cyclotron resonance (ECR) etcher, a surface wave plasma (SWP) etcher, an ICP etcher, a dual-frequency parallel plate excitation etcher, or other similar instruments can be used. In particular, ICP etchers are easy to control for plasma and facilitate the expansion of substrates to be processed.

For example, to perform high-precision plasma processing, a method is used in which plasma is formed by applying high-frequency electric power to multiple helical coils, where several helical coil segments are connected in parallel through impedance matching circuits. In addition, high-frequency electric power is also applied to the lower electrode holding the substrate to be processed, thereby supplying a bias voltage thereto.

When an ICP etcher employing such multiple helical coils is used, the taper angle can vary significantly depending on the bias electric power applied to the substrate side. Therefore, by further increasing the bias electric power and adjusting the pressure, the taper angle can be modified within the range of 50°-85°.

Chlorine gas is preferred as the etching gas for the second and third layers. For example, SiCl_4 , HCl , CCl_4 , BCl_3 , Cl_2 , or other similar gases may be used.

As the etching gas for the first layer, fluorine gas is preferably used. For example, NF_3 , CF_4 , C_2F_6 , SF_6 , or other similar gases may be used. When chlorine gas and fluorine gas are used simultaneously, the etching rate in the first layer is increased, which is desirable.

Furthermore, by forming the wiring with a stacked structure including the aforementioned conductive layers, ICP etching or other similar methods can be used to taper the wiring edges. By tapering the wiring edges, the coverage of the thin film to be formed in subsequent processes can be satisfactory.

In the above structure, the edge of the first conductive layer is preferably tapered. The tapered section (i.e., the taper segment) is a region that does not overlap with the second conductive layer, and its width corresponds to the width obtained by subtracting the second width from the first width. Furthermore, it is preferable that the second conductive layer is tapered, and its taper angle is greater than that of the tapered segment of the first conductive layer. Furthermore, it is preferable that the third conductive layer is tapered, and its taper angle is approximately the same as that of the tapered section of the second conductive layer.

The structure for implementing this solution involves a method for manufacturing wiring, which includes the following steps: Form the first-shaped conductive layer, which includes a stack composed of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface. Etch the first conductive layer, the second conductive layer, and the third conductive layer to form the second-shaped conductive layer, which includes a stack consisting of a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width. Then, etch the second conductive layer with a second width and the third conductive layer with a third width to form the third-shaped conductive layer, which includes a stack composed of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width, wherein the edge cross-section of the first conductive layer, the second conductive layer, or the third conductive layer is tapered.

In the aforementioned structure, the wiring is characterized by a stacked structure, which includes a conductive layer (first layer) primarily composed of an alloy or compound containing W, a conductive layer (second layer) primarily composed of an alloy or compound containing Al, and a conductive layer (third layer) primarily composed of an alloy or compound containing Ti. In another case, the wiring is characterized by a stacked structure, which includes a conductive layer (first layer) primarily composed of an alloy or compound containing Mo, a conductive layer (second layer) primarily composed of an alloy or compound containing Al, and a conductive layer (third layer) primarily composed of an alloy or compound containing Ti.

In addition, by enabling the wiring to have a stacked structure that includes the aforementioned conductive layer, the wiring edges can be made to form tapered shapes using the ICP etching method or other similar methods. By tapering the edges of the wiring, the coverage of the thin film to be formed in subsequent processes can be made satisfactory.

In the above structure, the edge of the first conductive layer is preferably tapered. The tapered section (i.e., the taper segment) is a region that does not overlap with the second conductive layer, and its width corresponds to the width obtained by subtracting the second width from the first width. It is also preferable that the second conductive layer is tapered, and its taper angle is greater than the taper angle of the tapered section of the first conductive layer. Furthermore, it is preferable that the third conductive layer is tapered, and its taper angle is approximately the same as that of the tapered section of the second conductive layer.

5 The structure of the present invention relates to a wiring board including an insulating substrate and wiring, characterized in that the wiring has a stacked structure, which includes: a first conductive layer with a first width as the first layer; a second conductive layer with a second width smaller than the first width as the second layer; and a third conductive layer with a third width smaller than the second width as the third layer, and is further characterized in that the edge cross-section of the first conductive layer, the second conductive layer, or the third conductive layer is tapered.

10 In the aforementioned structure, the wiring forming method is characterized in that a conductive film primarily containing W, a conductive film primarily containing Al, and a conductive film primarily containing Ti are stacked on top of each other and then etched with a mask. Furthermore, in the aforementioned structure, the wiring formation process is characterized in that a conductive film primarily containing Mo, a conductive film primarily containing Al, and a conductive film primarily containing Ti are stacked on top of each other and then etched using a mask.

15 In the above structure, the edge of the first conductive layer is preferably tapered. The tapered section (i.e., the taper segment) is a region that does not overlap with the second conductive layer, and its width corresponds to the width obtained by subtracting the second width from the first width. It is also preferable that the second conductive layer is tapered, and its taper angle is greater than the taper angle of the tapered section of the first conductive layer. Furthermore, it is preferable that the third conductive layer is tapered, and its taper angle is approximately the same as that of the tapered section of the second conductive layer.

20 In addition, the structure for implementing the present invention pertains to a method for manufacturing a wiring board, characterized by including the following steps: forming a first conductive layer on an insulating surface; forming a second conductive layer on the first conductive layer; forming a third conductive layer on the second conductive layer; and etching the first to third conductive layers to form conductive layers with tapered sections.

25 In the aforementioned structure, the wiring formation process is characterized in that a conductive film primarily containing W, a conductive film primarily containing Al, and a conductive film primarily containing Ti are stacked on top of each other and then etched with a mask. Additionally, in the aforementioned structure, the wiring formation process is characterized by conductive films primarily containing Mo, primarily containing Al, and primarily containing Ti stacked on top of each other, followed by etching with a mask.

30 Furthermore, by enabling the wiring to have a stacked structure that includes the aforementioned conductive layers, the wiring edge is tapered using the ICP etching method or other similar techniques. By tapering the edges of the wiring, the coverage of the thin film to be formed in subsequent processes can be made satisfactory.

35 In the above structure, the edge of the first conductive layer is preferably tapered. The tapered section (i.e., the taper segment) is a region that does not overlap with the second conductive layer, and its width corresponds to the width obtained by subtracting the second width from the first width. It is also preferable that the second conductive layer is tapered, and its taper angle is greater than the taper angle of the tapered section of the first conductive layer. Furthermore, it is preferable that the third conductive layer is tapered, and its taper angle is approximately the same as that of the tapered section of the second conductive layer.

According to the present invention, low resistivity in wiring can be achieved through a simple method suitable for conventional wiring or wiring board manufacturing processes. Therefore, the degree of design freedom and pixel aperture ratio can be enhanced. Due to the wiring comprising conductive layers with a tapered shape, satisfactory coverage is achieved. Due to these advantages, in semiconductor devices represented by active matrix-type liquid crystal display devices, the present invention provides sufficient room for screen expansion caused by the increase in pixel segment area, thereby enhancing the operating characteristics and reliability of the semiconductor device.

These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying drawings.

Description of Drawings

In the drawings:

Figures 1A - 1C illustrate the typical principles of the present invention.

Figures 2A and 2B illustrate the typical shapes of wiring produced according to the present invention.

Figures 3A and 3B schematically illustrate the morphology of wiring produced according to the present invention.

Figures 4A - 4C illustrate the typical shapes of wiring produced according to the present invention.

Figures 5A - 5C illustrate the typical shapes of wiring produced according to the present invention.

Figures 6A - 6C illustrate the typical shapes of wiring produced according to the present invention.

Figures 7A - 7C illustrate the typical principles of the present invention.

Figures 8A - 8C are cross-sectional views illustrating the manufacturing process of pixel TFTs and TFT driver circuits.

Figures 9A - 9C are cross-sectional views illustrating the manufacturing process of pixel TFTs and TFT driving circuits.

Figure 10 is a cross-sectional view illustrating the manufacturing process of pixel TFTs and TFT driving circuits.

Figure 11 is a top view showing the arrangement of pixel TFTs.

Figure 12 is a cross-sectional view illustrating the manufacturing process of active matrix liquid crystal display devices;

Figure 13 is a cross-sectional view illustrating the manufacturing process of active matrix liquid crystal display devices;

Figure 14 is a cross-sectional structural view of the driving circuit and pixel segment of the light-emitting device.

Figure 15A is a top view of a light-emitting device, and Figure 15B is a cross-sectional structural view of the driving circuit and pixel segment of the light-emitting device.

Figure 16 is a cross-sectional structural view of the driving circuit and pixel segment of the light-emitting device.

Figures 17A and 17B illustrate the typical principles of the present invention.

Figures 18A and 18B are cross-sectional views illustrating the manufacturing process of active matrix-type liquid crystal display devices.

Figure 19 is a cross-sectional structural view of the pixel segment of the light-emitting device.

5 Figures 20A to 20C show examples of semiconductor devices.

Figure 21 is a cross-sectional view illustrating the manufacturing process of pixel TFTs and TFT driver circuits; and

Figure 22 schematically illustrates the shape of wiring produced under the first etching conditions.

10 Detailed Implementation Plan

Hereinafter, the present invention will be described by way of exemplary embodiments with reference to Figures 1A to 1C. In this embodiment, a wiring board equipped with TFT and gate electrodes according to the present invention will be described.

15 First, the base insulating film 11 is formed on substrate 10. Substrate 10 may be a glass substrate, quartz substrate, silicon substrate, plastic substrate, metal substrate, flexible substrate, or other similar substrates. Examples of glass substrates include substrates made of glass such as barium borosilicate glass or aluminoborosilicate glass. In addition, the flexible substrate refers to a film-shaped substrate made of materials such as PET, PES, PEN, acrylic resin, or similar materials. If semiconductor devices are manufactured using flexible substrates, it can be expected that their weight will be light. It is preferable to form single-layer or multi-layer barrier layers such as Al films
20 (AlON, AlN, AlO, etc.), carbon films (diamond-like carbon (DLC), etc.), or SiN films on the front surface or both the front and back surfaces of flexible substrates to improve their lifespan.

25 Additionally, as the base insulating film 11, a base film 11 is formed from insulating films such as silicon oxide films, silicon nitride films, or silicon oxynitride films. Among these, the base film 11 with a double-layer structure (11a, 11b) is provided as an example; however, the base film 11 can be a single-layer insulating film or may have a multi-layer structure with two or more layers. Note that the base insulating film may not be formed.

30 Then, a semiconductor layer 12 is formed on the base insulating film 11. An amorphous semiconductor film is created using known methods (sputtering, LPCVD, plasma CVD, etc.), crystallized via known crystallization methods (laser crystallization method, thermal crystallization method, thermal crystallization method using a catalyst such as nickel, etc.), and patterned into the desired shape using the first photomask to obtain the semiconductor layer 12. The thickness of the formed semiconductor layer 12 ranges from 25 to 80 nm (preferably 30 to 60 nm). There is no particular restriction on the material of the crystalline semiconductor film; however, it is preferably formed of silicon, silicon-germanium (SiGe) alloy, or other similar materials.

Then, an insulating film 13 is formed to cover the semiconductor 12. The thickness of the insulating film 13 ranges from 40 to 150 nm, such that the silicon-containing insulating film has either a single-layer or multi-layer structure achieved by plasma CVD or sputtering. The insulating film 13 will serve as the gate insulating film.

Subsequently, a first conductive film 14 (thickness: 20 to 100 nm), a second conductive film 15 (thickness: 100 to 800 nm), and a third conductive film 16 (thickness: 20 to 100 nm) are stacked on the insulating film 13. Here, these conductive films can be formed using sputtering, plasma CVD, or other similar methods. Since the first conductive film 14 is in contact with the insulating film 13, a conductive film primarily containing W or Mo (e.g., W, WMo, Mo) can be used to prevent impurities from diffusing from the substrate 10 into the channel formation region. Additionally, for the second conductive film 15, a low-resistance conductive film primarily containing Al (e.g., Al, Al-Ti, Al-Sc, Al-Si, etc.) can be used. For the third conductive film 16, a conductive film primarily containing Ti (e.g., Ti, TiN, etc.) with low contact resistance can be used.

Then, a resist mask 17a is formed using the second photomask, and the first etching process is performed using an inductively coupled plasma (ICP) etching apparatus or similar equipment. Due to the first etching process, the first to third conductive films 14–16 are etched, resulting in conductive layers 18a–20a with tapered edges, as shown in Figure 1B.

The second etching process is performed using an ICP etching apparatus or similar equipment, employing the resist mask 17a originally formed during the second photolithography process. As a result of the second etching process, the second conductive layer 19a and the third conductive layer 18a are selectively etched to form the second conductive layer 19b and the third conductive layer 18b, as shown in Figure 1C. During the second etching process, the resist mask 17a, the first conductive layer 20a, and the insulating film 13 are lightly etched to form the resist mask 17b, the first conductive layer 20b, and the insulating film 21b. The first conductive layer 20b has a first width (W1), the second conductive layer 19b has a second width (W2), and the third conductive layer 18b has a third width (W3). The first width is greater than the second width, and the second width is greater than the third width.

Here, to suppress the reduction of the insulating film 13, etching is performed twice (the first and the second etching processes). However, there is no particular limitation as long as the electrode structure shown in Figure 1C (a stacked structure of the third conductive layer 18b, the second conductive layer 19b, and the first conductive layer 20b) can be formed. Etching may be performed once.

As described above, according to the present invention, the gate line is formed from a low-resistance conductive layer. Therefore, even if the pixel segment area is enlarged, it can still be sufficiently driven. It goes without saying that the present invention is applicable to various wirings as well as gate lines, and enables the production of wiring boards having such wirings formed thereon. Furthermore, according to the present invention, the operating characteristics and reliability of semiconductor devices with such wiring formed thereon can also be improved.

The present invention, with the above-mentioned structure, will be detailed through the following embodiments.

The present invention will be described by way of embodiments; however, it should be noted that the invention is not limited thereto.

5

[Embodiment 1]

Next, a typical structure of a wiring board equipped with gate electrodes in accordance with the present invention will be described.

10 First, the base insulating film 11 is formed on substrate 10. As the substrate 10, a glass substrate, a quartz substrate, a silicon substrate, or a metal substrate, or a flexible substrate with an insulating film formed thereon can be used. Furthermore, a plastic substrate having thermal resistance that can withstand processing temperatures can be used. In this embodiment, a glass substrate (Corning 1737) is employed.

15 As the base insulating film 11, a base film 11 made of insulating films such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed. Here, the base film 11 with a double-layer structure (11a, 11b) is given as an example, but the base film 11 may be a single-layer insulating film or a multilayer structure with two or more layers. Note that the base insulating film may not be formed. In this embodiment, a silicon oxychloride film 11a with a thickness of 50 nm is formed (composition ratio: Si=32%, O=27%, N=24 %, H=17%). Next, a silicon oxynitride film 11b with a thickness of 100 nm is formed (composition ratio: Si=32%, O=59%, N=7%, H=2%).

20 Then, a semiconductor layer 12 is formed on the base insulating film 11. An amorphous semiconductor film is formed using known methods (such as sputtering, LPCVD, plasma CVD, etc.), crystallized using known crystallization techniques (e.g., laser crystallization, thermal crystallization, thermal crystallization using catalysts such as nickel, etc.), and patterned into the desired shape using a first photomask, thus obtaining the semiconductor layer 12. The thickness of the formed semiconductor layer 12 is between 25–80 nm (preferably 30–60 nm). There is no particular restriction on the material of the crystalline semiconductor film; however, it is preferably formed using silicon, silicon germanium (SiGe) alloys, or other similar materials. In this embodiment, an amorphous silicon film with a thickness of 55 nm is formed by plasma CVD, and a nickel-containing solution is applied to the amorphous silicon film. The amorphous silicon film is dehydrogenated at 500°C for 1 hour. Then, it undergoes thermal crystallization at 550°C for 4 hours. Laser annealing is performed to improve crystallization, forming a crystalline silicon film. The crystalline silicon film is patterned by photolithography to form the semiconductor layer 12.

25 Then, an insulating film 13 is formed to cover the semiconductor layer 12. The insulating film 13, formed by plasma CVD or sputtering, has a thickness of 40 to 150 nm to ensure that the silicon-containing insulating film adopts a single-layer or multilayer structure. The insulating film 13 will serve as the gate insulating film. In this embodiment, a silicon oxynitride film formed by plasma CVD (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2% (thickness: 110 nm)).

35

Subsequently, a first conductive film 14 (thickness: 20 to 100 nm), a second conductive film 15 (thickness: 100 to 800 nm), and a third conductive film 16 (thickness: 20 to 100 nm) are stacked on the insulating film 13. Here, these conductive films 3 are formed by sputtering or similar methods. Since the first conductive film 14 is in contact with the insulating film 13, a conductive film mainly containing W or Mo (e.g., W, WMo, Mo, etc.) can be used to prevent impurities from diffusing from the substrate 10 into the channel formation region. In addition, for the second conductive film 15, a low-resistance conductive film mainly containing Al (e.g., Al, Al-Ti, Al-Sc, Al-Si) can be used. For the third conductive film 16, a conductive film mainly containing Ti (e.g., Ti, TiN, etc.) with low contact resistance can be used. In this embodiment, the first conductive film 14, made of a W film (thickness: 30 nm), the second conductive film 15, made of an Al-Ti film (thickness: 500 nm), and the third conductive film 15, made of a Ti film (thickness: 50 nm), are stacked through sputtering. The Ti content of the second conductive film 15 is 1%, and Al-Ti is used as the target material to form the second conductive film 15.

Then, the first etching process is performed. The first etching process is carried out under the first and second etching conditions. In this embodiment, the ICP etching method is employed under the first etching condition. More specifically, BCl_2 , Cl_2 , and O_2 are used as etching gases, with a gas flow rate ratio of 65:10:5 (sccm). The RF power of 450 W (13.56 MHz) is supplied to the coil-shaped electrode under a pressure of 1.2 Pa. Etching is performed for 147 seconds by generating plasma. Here, a dry etching apparatus (model E645-ICP) manufactured by Matsushita Electric Industrial Co., Ltd. is used, employing an ICP system. An RF power of 300 W (13.56 MHz) is also supplied to the substrate side (sample stage), thereby predominantly applying a negative self-bias. Under the first etching conditions, the etching rate for the resist mask is 235.5 nm/min, for Al-Ti is 233.4 nm/min, and for W is 133.8 nm/min. The etching rate of Ti is almost the same as that of Al-Ti. As shown in Figure 22, the Al-Ti film and the Ti film are etched under the first etching conditions to obtain the second conductive film 29 and the third conductive film 28. Under the first etching conditions, the etching of the Al-Ti film and Ti film results in tapered edges for the second and third conductive layers. Additionally, under the first etching conditions, the taper angle of the Al-Ti film and the Ti film becomes approximately 45° . Since the etching rate of W is significantly lower than that of the resist mask, Ti, and Al-Ti, the surface of the first conductive film 14 is primarily etched to form the shape indicated by reference numeral 30.

Thereafter, the etching conditions are changed to the second etching conditions without removing the resist mask 17a. Under the second etching conditions, CF_4 , Cl_2 , and O_2 are used as etching gases, with a gas flow rate ratio of 25:25:10 (sccm), 500 W RF (13.56 MHz) power is supplied to the coil-shaped electrode at a pressure of 1 Pa, generating plasma to perform etching for 30 seconds. 20 W RF (13.56 MHz) power is also supplied to the substrate side (sample stage), thereby applying a primarily negative self-bias. Under the second etching condition, CF_4 , Cl_2 , and O_2 are mixed, exclusively etching the W film. The etching rate of W under the second etching condition is 124.6 nm/min. To perform etching without leaving residues on the gate insulating film, the etching time can be increased by approximately 10-20%.

During the first etching process, by appropriately shaping the resist mask, the edges of the first and second conductive layers are tapered due to the bias applied to the substrate. The taper angle can be set between 15° and 45°. Thus, a first-shaped conductive layer including the first conductive layer 20a, the second conductive layer 19a, and the third conductive layer 18a is formed through the first etching process. The width of the first conductive layer 20a in the channel length direction corresponds to W1 as shown in the above-mentioned embodiment pattern. Reference numeral 21a denotes the gate insulating film, and the region of the gate insulating film 21a not covered by the first-shaped conductive layer is lightly etched by approximately 20-50 nm. The first etching process here corresponds to the first etching process described in the above embodiment mode (Figure 1B). Figure 2A shows a scanning electron microscope photograph of the first-shaped conductive layer formed at that time.

Then, a second etching process is performed without removing the resist mask. Here, BCl₃ and Cl₂ are used as etching gases. The gas flow rate ratio is 20:60 (sccm), and 600 W of RF (13.56 MHz) power is supplied to the coil-shaped electrode at a pressure of 1.2 Pa, with plasma generated for etching. 100 W of RF (13.56 MHz) power is also supplied to the substrate side (sample stage), thereby applying a substantially negative self-bias voltage thereto. In the second etching process, the Al-Ti film and the Ti film are selectively etched. As a result of the second etching process, the taper angle of the Al-Ti film and the Ti film changes to 80°. During the second etching process, the second conductive layer 19b and the third conductive layer 18b are formed. On the other hand, the first conductive layer 20a is hardly etched compared to the second conductive layer 19b and the third conductive layer 18b, forming the first conductive layer 20b. The second etching process here is equivalent to the second etching process (Figure 1C) described in the above embodiment mode. Therefore, a second-shaped conductive layer is formed, consisting of a first conductive layer with a width of W1 in the channel length direction, a second conductive layer with a width of W2 in the channel length direction, and a third conductive layer with a width of W3 in the channel length direction. Figure 2B shows a scanning electron microscope photograph of the second-shaped conductive layer.

Table 4 shows the results obtained by calculating the thickness (nm) of the base film to be etched, taking into account the in-plane variation of the etching rate of the Al-Ti film when the etching rate for films formed beneath the Al-Ti film is 2-10. At that time, the thickness was calculated assuming an Al-Ti film thickness of 500 nm with ±5% in-plane variations.

Changes in the etching rate for Al-Ti film ($\pm\%$)	Selectivity for the base film								
	2	3	4	5	6	7	8	9	10
1	300.0	200.0	150.0	120.0	100.0	85.7	75.0	66.7	60.0
2	350.1	233.4	175.1	140.1	116.7	100.0	87.5	77.8	70.0
3	400.4	266.9	200.2	160.1	133.5	114.4	100.1	89.0	80.1
4	450.7	300.5	225.4	180.3	150.2	128.8	112.7	100.2	90.1
5	501.3	334.2	250.6	200.5	167.1	143.2	125.3	111.4	100.3
6	552.0	368.0	276.0	220.8	184.0	157.7	138.0	122.7	110.4
7	603.0	402.0	301.5	241.2	201.0	172.3	150.7	134.0	120.6
8	654.2	436.1	327.1	261.7	218.1	186.9	163.5	145.4	130.8
9	705.7	470.5	352.9	282.3	235.2	201.6	176.4	156.8	141.1
10	757.6	505.1	378.8	303.0	252.5	216.5	189.4	168.4	151.5
11	809.8	539.9	404.9	323.9	269.9	231.4	202.4	180.0	162.0
12	862.4	574.9	431.2	345.0	287.5	246.4	215.6	191.6	172.5
13	915.5	610.3	457.7	366.2	305.2	261.6	228.9	203.4	183.1
14	969.0	646.0	484.5	387.6	323.0	276.9	242.2	215.3	193.8
15	1023.0	682.0	511.5	409.2	341.0	292.3	255.8	227.3	204.6

As shown in Table 4, as the variation in the etching rate for the Al-Ti film increases, the thickness to be etched becomes larger. Furthermore, as the selectivity for the base film increases, the thickness to be etched becomes thinner. If these characteristics are utilized, wiring of the desired shape can be formed.

As described above, according to the present invention, since the gate line is formed by a low-resistance conductive layer, the pixel segment can be sufficiently driven even if the area of the pixel segment is expanded. Furthermore, the operational characteristics and reliability of semiconductor devices having such wiring formed thereon can be improved.

[Embodiment 2]

In this embodiment, the changes in the first etching conditions of the first etching process in Embodiment 1 will be described with reference to FIGS. 3A-3B to FIGS. 6A-6C. Here, the first etching condition is changed, and only two layers (the first and third conductive layers) constitute the gate line in Embodiment 1. However, the present invention is also applicable to the case where the gate line is composed of three layers, using the first conductive layer in Embodiment 1 as the bottom layer.

First, a silicon oxynitride film 33 with a thickness of 200 nm is formed on the 1737 glass substrate 10 by sputtering. Then, a first conductive film 34 made of an Al-Ti film (thickness: 500 nm) and a second conductive film 35 made of a Ti film (thickness: 100 nm) are stacked through sputtering (Figure 3A).

Then, the etching process is performed after forming a resist film on the second conductive layer 35. The etching process is conducted under the first etching conditions in the first embodiment. In this embodiment, the ICP etching method is used, with BCl_3 and Cl_2 as the etching gases, and the pressure is set to 1.2 Pa. Etching is performed by varying the gas flow rate as shown in Table 5 and adjusting the electric power supplied to the coil-shaped electrode and the substrate side (sample stage) (Figure 3B). As a result of this etching process, the resist film, the second conductive film 35, and the first conductive film are etched, forming the second conductive layer 37, the first conductive layer 38, and the oxynitride film 40. Reference numeral 36 denotes the resist film after the etching process.

Table 5

	ICP	Bias Voltage	Gas	Flow Rate Ratio	Etching Time
Working Conditions	(W)	(W)		(sccm)	(sec.)
1	100	300	$\text{BCl}_3:\text{Cl}_2$	60:20	268
2	300	300	$\text{BCl}_3:\text{Cl}_2$	60:20	168
3	700	300	$\text{BCl}_3:\text{Cl}_2$	60:20	159
4	500	100	$\text{BCl}_3:\text{Cl}_2$	60:20	175
5	500	200	$\text{BCl}_3:\text{Cl}_2$	60:20	147
6	500	400	$\text{BCl}_3:\text{Cl}_2$	60:20	147
7	500	300	$\text{BCl}_3:\text{Cl}_2$	20:60	60
8	500	300	$\text{BCl}_3:\text{Cl}_2$	40:40	81
9	500	300	$\text{BCl}_3:\text{Cl}_2$	70:10	350

Figures 4A-4C to 6A-6C illustrate the conductive layer patterns observed using a scanning electron microscope at a magnification of 15,000 times under the working conditions shown in Table 5. Figure 4A shows the conductive layer formed under Working Condition 1. Figure 4B shows the conductive layer formed under Working Condition 2. Figure 4C shows the conductive layer formed under Working Condition 3. Figure 5A shows the conductive layer formed under Working Condition 4. Figure 5B shows the conductive layer formed under Working Condition 5. Figure 5C shows the conductive layer formed under Working Condition 6. Figure 6A shows the conductive layer formed under working condition 7. Figure 6B shows the conductive layer formed under working condition 8. Figure 6C shows the conductive layer formed under working condition 9. From FIGS. 4A-4C, it is understood that the conical angle increases as the electric power supplied to the coiled electrode increases. From FIGS. 5A-5C, it is understood that the conical angle increases as the electric power supplied to the substrate side increases. From FIGS. 6A-6C, it is understood that the *conical* angle increases as the BCl_3 gas flow rate ratio increases. Therefore, the change in the conical angle depends on the working conditions. In addition, Table 6 shows the etching rates obtained under the conditions shown in Table 5. Table 7 shows the selectivity ratios for various films. Under conditions where the selectivity between Al-Ti and W is high, anisotropic etching can be performed, thereby forming a conductive layer having a desired shape.

Table 6

Working Conditions	ICP	Bias Voltage	Flow Rate Ratio	Al-Si (nm/min)		Resist film (nm/min)		W (nm/min)		SiON (nm/min)	
	(W)	(W)	(sccm)	(Ave)	(3 σ)	(Ave)	(3 σ)	(Ave)	(3 σ)	(Ave)	(3 σ)
1	100	300	60 : 20	168.8	39.3	122.4	33.1	37.1	6.4	38.4	8.1
2	300	300	60 : 20	236.9	51.4	197.9	36.7	59.4	16.2	66.4	8.9
3	700	300	60 : 20	262.1	63.2	263.1	33.2	110.7	23.1	107.6	12.0
4	500	100	60 : 20	236.7	40.6	133.7	26.3	41.4	17.0	56.0	8.2
5	500	200	60 : 20	246.8	46.1	199.6	23.7	69.1	22.3	81.8	8.8
6	500	400	60 : 20	251.0	55.2	255.3	24.4	102.6	21.3	104.0	13.4
7	500	300	20 : 60	750.7	111.0	395.2	70.7	127.8	49.9	104.0	17.6
8	500	300	40 : 40	495.6	116.5	351.1	62.2	112.4	39.4	101.0	16.8
9	500	300	70 : 10	142.3	24.2	148.6	17.7	61.0	10.8	99.3	9.7

Table 7

Working Conditions	Selectivity to Al-Si			Selectivity to resist film			Selectivity to W			Selectivity for SiON		
	Resist film	W	SiON	Al-Si	W	SiON	Al-Si	Resist film	SiON	Al-Si	Resist film	W
1	1.38	4.55	4.40	0.73	3.30	3.19	0.22	0.30	0.97	0.23	0.31	1.03
2	1.20	3.99	3.57	0.84	3.33	2.98	0.25	0.30	0.89	0.28	0.34	1.12
3	1.00	2.37	2.44	1.00	2.38	2.45	0.42	0.42	1.03	0.41	0.41	0.97
4	1.77	5.72	4.23	0.56	3.23	2.39	0.17	0.31	0.74	0.24	0.42	1.35
5	1.24	3.57	3.02	0.81	2.89	2.44	0.28	0.35	0.85	0.33	0.41	1.18
6	0.98	2.45	2.41	1.02	2.49	2.46	0.41	0.40	0.99	0.41	0.41	1.01
7	1.90	5.88	7.22	0.53	3.09	3.80	0.17	0.32	1.23	0.14	0.26	0.81
8	1.41	4.41	4.91	0.71	3.12	3.47	0.23	0.32	1.11	0.20	0.29	0.90
9	0.96	2.33	1.43	1.04	2.44	1.50	0.43	0.41	0.61	0.70	0.67	1.63

5 As described above, by changing the working conditions, a conductive layer of the desired shape can be obtained. Furthermore, even if the pixel segment area is enlarged, the pixel can still be sufficiently driven. The operating characteristics and reliability of a semiconductor device having such wiring formed thereon can also be improved.

10 [Embodiment 3]

In this embodiment, the case where the wiring formed in Embodiment 1 is subjected to plasma treatment will be explained with reference to FIGS. 17A and 17B. In this specification, plasma treatment refers to exposing the sample to a plasma treatment gas environment.

15 First, according to Embodiment 1, the state shown in Figure 1C is obtained. Figures 17A and 17C show the same state, and the corresponding sections are denoted by identical reference numerals.

The wiring thus formed is subjected to plasma treatment using oxygen, a gas primarily containing oxygen, or H₂O (Figure 17B). The plasma treatment is performed using a plasma generator (such as a plasma CVD apparatus, dry etching apparatus, sputtering apparatus, etc.) for 30 seconds to 20 minutes (preferably 3 to 15 minutes). Additionally, it is preferable to process the wiring under conditions of a gas flow rate of 50-300 sccm, a substrate temperature ranging from room temperature to 200°C, and RF power of 100-2000 W. Due to the plasma treatment, the second conductive layer 19b, composed of Al or an alloy or compound mainly containing Al within the three-layer conductive structure, may be oxidized. Therefore, section 22 of the conductive layer 19b that is not in contact with other conductive layers becomes oxidized. This further reduces the formation of protrusions, such as bumps and whiskers.

Needless to say, if oxygen or an oxygen-rich gas, or H₂O is used, or ashing is performed to remove the resist film 17b, then the exposed section of the second conductive layer 19b will be oxidized. However, it is more likely that a sufficient oxide film will be formed when plasma treatment is performed after removing the resist film 17b.

As described above, according to the present invention, the gate line is formed from a low-resistance conductive layer. Therefore, even if the pixel segment area is enlarged, the pixel can still be effectively driven. Furthermore, semiconductor devices with such wiring formed thereon can have improved operating characteristics and reliability.

[Embodiment 4]

Examples of wiring boards manufactured by applying the present invention to wiring structures different from those in Embodiments 1 to 3 will be described with reference to Figure 7.

First, as the substrate 10, a glass substrate, a quartz substrate, a silicon substrate, a metal substrate, or a flexible pillar substrate with an insulating film formed thereon can be used. Furthermore, a plastic substrate having thermal resistance that can withstand processing temperatures can be used. In this embodiment, a glass substrate (Corning 1737) is employed.

Then, a first conductive film 44 (thickness: 20-100 nm), a second conductive film 45 (thickness: 100-800 nm), and a third conductive film 46 (thickness: 20-100 nm) are stacked on the substrate 10. Here, these conductive films can be formed by sputtering, and since the first conductive film 44 is in contact with the insulating film, a conductive film mainly containing W or Mo can be used to prevent impurities from diffusing from the substrate 10 into the channel formation region. In addition, as the second conductive film 45, a low-resistance conductive film primarily containing Al or Cu can be used. As the third conductive film 46, a conductive film primarily containing Ti and having low contact resistance can be used. In this embodiment, these conductive films can be formed by sputtering, and the first conductive film 44, made of a Mo film (thickness: 30 nm), the second conductive film 45, made of an Al-Ti film (thickness: 500 nm), and the third conductive film 46, made of a Ti film (thickness: 50 nm), are stacked together.

Then, the etching process is carried out. The etching process is performed under the first etching condition and the second etching condition. In this embodiment, the ICP etching method is employed under the first etching condition. More specifically, BCl_2 , Cl_2 , and O_2 are used as etching gases, with a gas flow ratio of 65:10:5 (sccm). An RF power of 450 W (13.56 MHz) is supplied to the coil-shaped electrode at a pressure of 1.2 Pa to generate plasma for etching. Here, an ICP dry etcher (model E645-□ICP) manufactured by Matsushita Electric Industrial Co., Ltd. is used. A 300 W RF power (13.56 MHz) is also supplied to the substrate side (sample stage), thereby causing a substantially negative self-bias voltage to be applied thereto. Under the first etching condition, the Al-Ti film and Ti film are etched to form the edge of the first conductive layer into a tapered shape. Furthermore, under the first etching condition, although the taper angle of the Al-Ti film and Ti film becomes approximately 45° , the Mo remains unetched.

Subsequently, the etching condition is changed to the second etching condition without removing the resist mask 47. Under the second etching condition using CF_4 , Cl_2 , and O_2 as etching gases, the gas flow ratio is 25:25:10 (sccm). A 500 W RF power (13.56 MHz) is supplied to the coil-shaped electrode at a pressure of 1.2 Pa, generating plasma for the etching process. A 20 W RF power (13.56 MHz) is also supplied to the substrate side (sample stage), thereby applying a substantially negative self-bias voltage. In the second etching condition, a mixture of CF_4 , Cl_2 , and O_2 is used to etch only the Mo film. To ensure etching without leaving residues on the gate insulating film, the etching time can be increased approximately by 10-20%.

During the etching process, by appropriately shaping the resist mask, and due to the bias applied to the substrate side, the edges of the first and second conductive layers are formed into a tapered shape. The taper angle can be set between 15° and 45° . Hence, the etching process forms a conductive layer composed of the first conductive layer 50, the second conductive layer 49, and the third conductive layer 48.

Subsequently, an insulating film 51 is formed to cover the conductive layer. The insulating film 51 is formed by plasma CVD or sputtering with a thickness of 40-150 nm, to obtain a silicon-containing insulating film in a single-layer or multi-layer structure. In this embodiment, a silicon oxynitride film (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%) is formed by plasma CVD with a thickness of 110 nm.

Next, a semiconductor layer 52 is formed on the insulating film 51. An amorphous semiconductor film is formed using known methods (sputtering, LPCVD, plasma CVD, etc.). This film is crystallized using known crystallization methods such as laser crystallization, thermal crystallization, or thermal crystallization using a catalyst like nickel. The crystallized semiconductor film is patterned into the desired shape using a photomask, thereby forming the semiconductor layer 52. The thickness of the formed semiconductor layer 52 is between 25 and 300 nm (preferably between 30 and 150 nm). There is no particular restriction on the material of the crystalline semiconductor film; however, it is preferably formed of silicon, silicon-germanium (SiGe) alloy, or other similar materials. In this embodiment, the amorphous silicon film formed by plasma-enhanced CVD has a thickness of 55 nm, and this amorphous silicon film undergoes a laser annealing process to form a crystalline silicon film. The crystalline silicon film is patterned through photolithography to form the semiconductor layer 52.

As described above, according to the present invention, the gate lines are formed from a low-resistance conductive layer. Therefore, when using TFTs with an inverted staggered structure, the pixels can still be sufficiently actuated even if the pixel segment area is enlarged. Moreover, the operating characteristics and reliability of semiconductor devices having such wiring formed thereon can be improved.

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[Embodiment 5]

10 In this embodiment, as a typical wiring board utilizing the present invention, the manufacturing method for the active matrix substrate will be described with reference to Figures 8A-11. In this specification, a substrate on which a driving circuit with CMOS circuits, a pixel segment having pixel TFTs, and storage capacitors are simultaneously formed will be referred to as an active matrix substrate for convenience.

In this embodiment, a substrate 400 made of glass, such as barium borosilicate glass (e.g., #7059 glass and #1737 glass produced by Corning Inc.) or aluminoborosilicate glass, is used. As the substrate 400, quartz substrate, silicon substrate, metal substrate with insulating films formed thereon, or flexible substrate can be used. On the other hand, a heat-resistant plastic substrate capable of withstanding high temperatures can be used.

15 Then, a base film 401 composed of an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed on substrate 400. In this embodiment, the base film 401 has a double-layer structure; however, it may have a single-layer structure or a multilayer structure composed of two or more insulating films. As the lower layer of base film 401, a silicon oxynitride film 401a is formed using SiH₄, NH₃, and N₂O as reaction gases by plasma CVD, with a thickness of 10–200 nm (preferably 50–100 nm). In this embodiment, a silicon oxynitride film 401a is formed to a thickness of 50 nm (composition ratio: Si=32%, O=27%, N=24%, H=17%). Subsequently, as the upper layer of base film 401, a silicon oxide film 401b is formed using SiH₄ and N₂O as reaction gases by plasma CVD, with a thickness of 50–200 nm (preferably 100–150 nm). In this embodiment, a silicon oxide film 401b is formed to a thickness of 100 nm (composition ratio: Si=32%, O=59%, H=2%).

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Then, semiconductor layers 402–406 are formed on base film 401. A semiconductor film with a thickness of 25–300 nm (preferably 30–200 nm) is formed using well-known methods (such as sputtering, LPCVD, plasma CVD, etc.), crystallized by well-known crystallization methods (e.g., laser crystallization, thermal crystallization methods such as furnace annealing and rapid thermal annealing (RTA), or thermal crystallization using metal elements to accelerate crystallization, etc.), and crystalline semiconductor films are patterned into the shapes required. Examples of semiconductor films include amorphous semiconductor films, microcrystalline semiconductor films, and crystalline semiconductor films, as well as composite semiconductor films with amorphous structures, such as amorphous silicon oxide films. In this embodiment, an amorphous silicon film with a thickness of 55 nm is formed by plasma CVD, while a lanthanum-containing solution remains on the amorphous silicon film. The amorphous film undergoes dehydrogenation at 500 °C for 1 hour and is subjected to thermal crystallization at 550 °C for 4 hours. The crystalline silicon film is patterned by photolithography to form semiconductor layers 402–406.

In the case of manufacturing crystalline semiconductor films using the laser crystallization method, a continuous oscillation or pulsed oscillation solid-state laser, gas laser, or metal laser can be used. Examples of solid-state lasers include continuous oscillation type or pulsed oscillation type YAG lasers, YVO₄ lasers, YLF lasers, YAlO₃ lasers, glass lasers, ruby lasers, alexandrite lasers, Ti: sapphire lasers, and the like. Examples of gas lasers include continuous oscillation type or pulsed oscillation type excitation lasers, Ar lasers, Kr lasers, CO₂ lasers, and the like. Examples of metal lasers include ammonia cadmium lasers, copper vapor lasers, and gold vapor lasers. When using these lasers, the laser beam emitted by the laser oscillator can be condensed into a linear shape by an optical system and then irradiated onto the semiconductor film. The crystallization conditions should be appropriately selected by those skilled in the art. When using a pulsed oscillation excitation laser, the pulse frequency is set at 300 Hz, and the laser energy density is set at 100–1200 mJ/cm² (typically 200–800 mJ/cm²). Furthermore, when using a pulsed oscillation YAG laser with a second harmonic, the pulse frequency is set at 1–300 Hz, and the laser energy density is set at 300–1200 mJ/cm² (typically 350–1000 mJ/cm²). It is also possible to condense the laser beam into a straight line with a width of 100–1000 μm (e.g., 400 μm) and irradiate the entire surface of the substrate, with the overlap ratio of the linear beam set at 50–98%. In addition, when using a continuous oscillation laser, the energy density requirement is approximately 0.01–100 MW/cm² (preferably 0.1–10 MW/cm²). Irradiation is performed by moving the sample stage at a relative speed of approximately 0.5–2000 cm/s with respect to the laser beam.

However, in this embodiment, the amorphous film is crystallized using a metal-element-assisted crystallization method, so the metal element remains in the crystalline silicon film. Thus, an amorphous silicon film with a thickness of 50–100 nm is formed on the crystalline silicon film, and heat treatment (e.g., thermal annealing using an annealing furnace, RTA, etc.) is conducted to diffuse the metal element into the amorphous film. After the heat treatment, the amorphous film is removed by etching. As a result, the content of metal elements in the crystalline silicon film can be reduced or removed.

Needless to say, crystalline semiconductor films obtained solely by laser crystallization can also be used to fabricate TFTs. However, if the thermal crystallization method using metal elements is combined with the laser crystallization method, the crystallinity of the crystalline semiconductor film is improved. Consequently, the electrical characteristics of the TFT are also improved. And this is desirable. For example, when the TFT is fabricated using a crystalline semiconductor film obtained solely by laser crystallization, the mobility is approximately 300 cm²/Vs. On the other hand, when the TFT is manufactured using a crystalline semiconductor film obtained through thermal crystallization employing metal elements combined with a laser crystallization method, the mobility is significantly improved (i.e., approximately 500-600 cm²/Vs).

After the formation of semiconductor layers 402-406, trace amounts of impurity elements (boron or phosphorus) can be doped to control the threshold voltage of the TFT.

Subsequently, a gate insulating film 407 is formed to cover the semiconductor layers 402-406. The gate insulating film 407 is formed from a silicon-containing insulating film via plasma-enhanced CVD or sputtering, achieving a thickness of 40-150 nm. In this embodiment, a silicon oxynitride film (composition ratio: Si = 32%, O = 59%, N = 7%, H = 2%) is formed by plasma CVD with a thickness of 110 nm. It should be understood that gate insulating film 407 is not limited to silicon oxynitride film; it may also be another silicon-containing insulating film with either a single-layer or multi-layer structure.

In the case of using a silicon oxide film, the silicon oxide film can be formed by plasma CVD. More specifically, a silicon oxide film can be formed by mixing tetraethyl orthosilicate (TEOS) with O₂, setting the reaction pressure and substrate temperature at 40 Pa and 300°C-400°C, and performing discharge at a high frequency (13.56 MHz) with a power density of 0.5-0.8 W/cm², a silicon oxide film can be formed. The silicon oxide film thus manufactured, after thermal annealing at 400°C to 500°C, exhibits satisfactory electrical characteristics as a gate insulating film.

Then, the first conductive film 408a (thickness: 20-100 nm), the second conductive film 408b (thickness: 100-800 nm), and the third conductive film 408c (thickness: 20-100 nm) are stacked over the gate insulating film 407. In this embodiment, the first conductive film 408a made of a WN film (thickness: 30 nm), the second conductive film 408b made of an Al-Sc film (thickness: 370 nm), and the third conductive film 408c made of a TiN film (thickness: 30 nm) are stacked.

In this embodiment, although the first conductive film 408a is made of WN, there is no particular limitation thereto. The first conductive film 408a may be formed as a conductive layer made of an element selected from W and Mo, or an alloy or a compound mainly containing these elements. In addition, although the second conductive film 408b is made of Al-Si, there is no particular limitation thereto. The second conductive film 408b may be formed as a conductive layer made of Al, or an alloy or a compound mainly containing Al. In addition, although the third conductive film 408c is made of TiN, there is no particular limitation thereto. The third conductive layer 408c may be formed as a conductive layer made of Ti, or an alloy or a compound mainly containing Ti.

Next, etch-resistant masks 410-415 are formed by photolithography, thereby performing a first etching process to form electrodes and wiring. The first etching process is performed under the first etching condition and the second etching condition (Figure 8B). In this embodiment, the ICP etching method is employed under the first etching condition. More specifically, BCl_2 , Cl_2 , and O_2 are used as etching gases, with a gas flow ratio of 65:10:5 (sccm). These gases are supplied to a coil-shaped electrode at 450 W RF (13.56 MHz) power under a pressure of 1.2 Pa, where plasma is generated for etching. An RF (13.56 MHz) power of 300 W is also supplied to the substrate side (sample stage), thereby applying a substantially negative self-bias voltage thereto. Under the first etching condition, the Al-Sc film and the TiN film are etched to form tapered edges of the second and third conductive layers. Furthermore, under the first etching condition, the taper angles of the Al-Sc film and the TiN film are approximately 45° , while the WN film is hardly etched.

Subsequently, the etching condition is switched to the second etching condition without removing the resist masks 410-415. Under the second etching condition, CF_4 , Cl_2 , and O_2 are used as etching gases, with a gas flow ratio of 25:25:30 (sccm). RF power of 500W (13.56 MHz) is supplied to the coil-shaped electrode under a pressure of 1.2Pa to generate plasma for etching. A 20 W RF power (13.56 MHz) is also supplied to the substrate side (sample stage), thereby applying a substantially negative self-bias voltage. To ensure etching without leaving residues on the gate insulating film, the etching time can be increased approximately by 10-20%.

During the first etching process, by appropriately shaping the resist mask, the edges of the first to third conductive layers are tapered due to the effect of the bias applied to the substrate side. The taper angle can be set between 15° and 45° . Thus, through the first etching process, the first-shaped conductive layers 417-422, composed of the first, second, and third conductive layers (the first conductive layers 417a-422a, the second conductive layers 417b-422b, and the third conductive layers 417c-422c), are formed.

Reference numeral 416 denotes the gate insulating film. The regions of the gate insulating film 416 not covered by the first-shaped conductive layers 417 to 422 are etched by approximately 20 to 50 nm and become thinner.

Then, a second etching process is performed without removing the resist mask (Figure 8C). Here, BCl_2 and Cl_2 are used as etching gases, with a gas flow ratio of 20:60 (sccm). An RF power of 600 W (13.56 MHz) is supplied to the coil-shaped electrode under a pressure of 1.2 Pa to generate plasma for etching. An RF power of 100 W (13.56 MHz) is also supplied to the substrate side (sample stage), thereby applying a substantially negative self-bias voltage thereto. During the second etching process, the Al-Sc film and the TiN film are selectively etched. Due to the second etching process, the second conductive layers 428b-433b and the third conductive layers 428c-433c are formed. On the other hand, the first conductive layers 417a to 422a are hardly etched, and thus the second-shaped conductive layers 428 to 433 are formed.

As described above, due to the first etching process and the second etching process, and using the structure of the present invention, the gate electrodes 428 to 431, one electrode of the storage capacitor 432, and the source line 433 are formed.

Next, the first doping process is performed without removing the resist mask, whereby an impurity element capable of introducing n-type conductivity is added to the semiconductor layer with a low concentration. The doping process can be carried out using ion doping or ion implantation. Ion doping is carried out at a dose of 1×10^{13} - $5 \times 10^{14}/\text{cm}^2$ and under an acceleration voltage of 40-80 keV. In this embodiment, ion doping is carried out under the conditions of a dose of $1.5 \times 10^{13}/\text{cm}^2$ and an acceleration voltage of 60 keV. As the impurity element introducing n-type conductivity, an element belonging to Group 15 (typically phosphorus (P) or arsenic (As)) is used. Here, phosphorus (P) is used. In this case, conductive layers 428-433 act as masks for introducing n-type impurity elements, and impurity regions 423-427 are formed in a self-aligned manner. Impurity elements introducing n-type properties are added to impurity regions 423-427 to achieve a concentration range of 1×10^{18} to $1 \times 10^{20}/\text{cm}^3$.

After removing the photoresist mask, new resist masks 434a-434c are formed, and the second doping process is conducted at an acceleration voltage higher than that of the first doping process. At this time, ion doping is carried out at a dose of 1×10^{13} to $5 \times 10^{15}/\text{cm}^3$ and an acceleration voltage of 60-120 keV. The doping process is performed using the second conductive layers 428b-432b as masks for the impurity elements, so that the impurity elements are added to the semiconductor layer below the tapered section of the first conductive layer. Then, the third doping process is performed at an acceleration voltage lower than that of the second doping process, thereby resulting in the state shown in Figure 9A. At this time, ion doping is performed under conditions where the dose is 1×10^{15} - $q \times 10^{17}/\text{cm}^2$ and the acceleration voltage is 50-100 keV. Due to the second and third doping processes, n-type impurity elements are added to low-concentration impurity regions 436, 442, and 448, which overlap with the first conductive layer, at a concentration ranging from 1×10^{18} to $5 \times 10^{19}/\text{cm}^3$. On the other hand, n-type impurity elements are added to high-concentration impurity regions 435, 438, 441, 444, and 447, at a concentration ranging from 1×10^{19} to $5 \times 10^{20}/\text{cm}^3$.

Needless to say, by setting an appropriate acceleration voltage, low-concentration impurity regions and high-concentration impurity regions can be formed through a single doping process without requiring the second and third doping processes.

Then, after removing the resist masks 434a-434c, new resist masks 450a-450c are formed, thereby performing a fourth doping process. Due to the fourth doping process, impurity regions 453, 454, 459, and 460 formed in the semiconductor layer serve as the active layers of the p-channel TFT, to which impurity elements providing conductivity opposite to the aforementioned conductivity type are added. The second conductive layers 428a-432a are used as masks for the impurity elements, and n-type impurity elements are added, thereby forming the impurity regions in a self-aligned manner. In this embodiment, impurity regions 453, 454, 459, and 460 are formed by ion doping using diborane (B_2H_6). In the fourth doping process, the semiconductor layer constituting the n-channel TFT is covered by the resist masks 450a-450c. Due to the first to third doping processes, phosphorus is added to the impurity regions 438 and 439 at different concentrations. However, since doping is performed in both regions, the concentration of p-type impurity elements becomes 1×10^{19} - 5×10^{21} atoms/ cm^3 , and thus these regions serve as the source region and drain region of the p-channel TFT. Therefore, there is no problem.

As a result of the above-described process, impurity regions are formed in each semiconductor layer.

5 Then, the resist masks 450a-450c are removed, and the first interlayer insulating film 461 is formed. The first interlayer insulating film 461 is formed of a silicon-containing insulating film with a thickness of 100 to 200 nm by plasma CVD or sputtering. In this embodiment, a silicon oxynitride film with a thickness of 150 nm is formed by plasma CVD. Needless to say, the first interlayer insulating film 461 is not limited to silicon oxynitride film but may be another silicon-containing insulating film having a single-layer or multi-layer structure.

10 Then, as shown in Figure 9C, the crystallinity of the semiconductor layers is restored, while impurity elements added to the respective semiconductor layers are activated by irradiation with a laser beam. It is preferable to use a continuous oscillation type or pulsed oscillation type solid-state laser, a gas laser, or a metal laser. In particular, it is preferable to perform a laser annealing process using a YAG laser. If a continuous wave laser is used, the energy density of the laser beam is required to be approximately 0.01-100 MW/cm² (preferably 0.01-10 MW/cm²), and the substrate is required to move relative to the laser beam at a speed of 0.5-2000 cm/s. If a pulsed oscillation laser is used, it is preferable to set the frequency to 300 Hz and the laser energy density to 50-900 mJ/cm² (typically 50-500 mJ/cm²). At this time, the laser beams can overlap by 50-98%. In cases where the region where the second
15 conductive layer contacts the first interlayer insulating film 461 is sufficiently oxidized, even under heat treatment, protrusions such as bulges or whiskers will not be formed. Thermal annealing using an annealing furnace or RTA can be applied.

20 Heat treatment may be performed before the formation of the first interlayer insulating film. In cases where the wiring to be used is not heat-resistant, it is preferable to perform an activation process after the formation of the interlayer insulating film (mainly a silicon-containing insulating film, such as a silicon nitride film) to protect the wiring, as demonstrated in this embodiment.

25 Then, hydrogenation can be performed through thermal treatment (300°C to 450°C, 1 to 12 hours), during which the unsaturated bonds in the semiconductor layer are terminated due to the action of the hydrogen contained in the first interlayer insulating film 461. Despite the presence of the first interlayer insulating film, the semiconductor layer can still be hydrogenated. As another method of hydrogenation, plasma oxidation (using hydrogen activated by plasma) or heat treatment at 300°C to 450°C for 1 to 12 hours in an atmosphere containing 3 to 100% hydrogen may be performed.

Next, a second interlayer insulating film 462a made of inorganic insulating film material or organic insulating material is formed on the first interlayer insulating film 461. In this embodiment, an acrylic resin film is formed with a viscosity of 10 to 1000 cp (preferably 40 to 200 cp), with a thickness of 1.6 μm , and uneven thickness is formed on its surface. Without using an organic resin film, the second interlayer insulating film 462b is formed in the shape shown in Figure 21.

In this embodiment, in order to prevent specular reflection, a second interlayer insulating film is formed with uneven thickness, thereby creating uneven thickness on the surface of the pixel electrode. Furthermore, in order to achieve light scattering by forming uneven thickness on the surface of the pixel electrode, an arc-shaped protrusion can be formed in the lower region of the pixel electrode. In this case, the arc-shaped protrusions can be formed using the same photomask as that used for forming the TFTs. Therefore, the number of processes does not need to increase. In the pixel area, rather than the wiring and TFT areas, an arc-shaped protrusion can be appropriately formed on the substrate. In view of this, the uneven thickness region formed along the surface of the insulating film covering the arc-shaped protrusion causes uneven thickness on the surface of the pixel electrode.

As the second interlayer insulating film 462a, a film whose surface requires leveling can be used. In this case, it is preferable, after forming the pixel electrode, to create uneven thickness on the surface using known methods such as sandblasting or etching to prevent mirror reflection and allow reflected light to scatter, thereby improving whiteness.

In the driving circuit 506, wirings 463 to 467 are formed to electrically connect with the respective impurity regions. By making the Ti film (thickness: 50 nm) and alloy (Al and Ti) films (thickness: 500 nm) stacked film is formed to create these wires. It should be understood that these wires may have a single-layer structure or a multi-layer structure consisting of three or more layers, instead of a double-layer structure. Furthermore, the material of the wiring is not limited to Al and Ti. For example, a stacked film obtained by forming Al or Cu on a TaN film and then forming a Ti film thereon can be shaped to form wiring (Figure 10).

In pixel section 507, a pixel electrode 470, gate line 469, and connection electrode 468 are formed, allowing the source lines (433a-433c) to be electrically connected to the pixel TFT. Additionally, gate line 469 is electrically connected to the gate electrode of the pixel TFT. In addition, the pixel electrode 470 is electrically connected to the drain region 422 of the pixel TFT and to the semiconductor layer 458 serving as one electrode plate of the storage capacitor. For the pixel electrode 470, it is preferable to use a material with excellent reflectivity, such as a thin film mainly containing Al or Ag, or a stacked film of these thin films.

As mentioned above, a driver circuit having a CMOS circuit including n-channel TFT 501, p-channel TFT 502, and n-channel TFT 503, and a pixel segment 507 having a pixel TFT 504 and a storage capacitor 505, which includes capacitor wiring 523, can be formed on the same substrate. In this way, the active matrix substrate is completed.

5 The n-channel TFT 501 of driver circuit 506 has a channel formation region 437, a low-concentration impurity region 436 (GOLD region) that overlaps with the first conductive layer 428a, which forms part of the gate electrode, and a high-concentration impurity region 452 serving as the source or drain region. By connecting electrode 466 to the n-channel TFT 501, the p-channel TFT 502 forming part of the CMOS circuit features a channel formation region 440, a high-concentration impurity region 454 serving as the source or drain region, and an impurity region 10 453 doped with both n-type and p-type impurity elements. Furthermore, the n-channel TFT 503 has a channel formation region 443, a low-concentration impurity region 442 (GOLD region), which overlaps with the first conductive layer 430 constituting part of the gate electrode, and a high-concentration impurity region 456 functioning as a source region or a drain region.

15 The pixel TFT 504 of the pixel segment 507 includes a channel formation region 446, a low-concentration impurity region 445 (Lightly Doped Drain (LDD) region) formed outside the gate electrode, and a high-concentration impurity region 458 acting as a source region or a drain region. Additionally, n-type and p-type impurity elements are added to the semiconductor layer acting as one electrode plate of the storage capacitor 505. The storage capacitor 505 is composed of electrodes (stacked structures 432a-432c) and a semiconductor layer using the insulating film 416 as a dielectric.

20 In the pixel configuration of this embodiment, the edges of the pixel electrodes are arranged to overlap with the source lines, thereby achieving light shielding between the gaps of the pixel electrodes without using a black matrix.

25 Additionally, Figure 11 shows a top view of the pixel section of the active matrix substrate manufactured in this embodiment. The corresponding sections in Figures 8A-8C-11 are indicated by the same reference numerals. The dot-dash line A-A' in Figure 10 corresponds to the cross-section along the dot-dash line A-A' in Figure 11. The dot-dash line B-B' in Figure 10 corresponds to the cross-section along the dot-dash line B-B' in Figure 11.

In the wiring thus produced, low resistance is achieved, and the wiring board having such wiring can also be fully used for an enlarged pixel segment.

This embodiment can be arbitrarily combined with any of Embodiments 1 to 4.

[Embodiment 6]

In this embodiment, the process of manufacturing a reflective liquid crystal display device using the active matrix substrate manufactured in Embodiment 5 will be described with reference to Figure 12.

First, according to Embodiment 5, an active matrix substrate as shown in Figure 10 is obtained. Thereafter, an alignment film 567 is formed on at least the pixel electrode 470 of the active matrix substrate in Figure 10, and a rubbing process is performed. In this embodiment, before the formation of alignment film 567, an organic resin film, such as an acrylic resin film, is shaped to form columnar spacers 572 that maintain the substrate gap at the required positions. Additionally, spherical spacers may be distributed across the entire surface of the substrate instead of columnar spacers.

Then, the counter substrate 569 is manufactured. Color layers 570 and 571, and the leveling film 573 are formed on the counter substrate 569. The red layer 570 overlaps with the blue layer 571 to form a light shielding section. It is also possible to partially overlap the red layer with the green layer to form a light shielding section.

In this embodiment, the substrate described in Embodiment 5 is used. Therefore, as shown in Figure 11, which illustrates the top view of the pixel section of Embodiment 5, it is required that light shielding should be provided at least in the gaps between the gate line 469 and the pixel electrode 470, the gate line 469 and the connecting electrode 468, and the connecting electrode 468 and the pixel electrode 470. In this embodiment, the arrangement of each color layer should ensure that the light-shielding section composed of stacked color layers overlaps with the positions requiring light shielding, and under this condition, the sub-base plate is fixed.

As described above, the gaps between the individual pixels are light-shielded by the segments composed of laminated color layers, thereby reducing the number of processes without forming a separate light-shielding layer, such as a black mask.

Then, a counter electrode 576 composed of a transparent conductive film is formed at least on the leveling film 573 in the pixel section, and an alignment film 574 is formed over the entire surface of the counter substrate, thereby enabling a rubbing process.

Afterward, the active matrix substrate and the counter substrate, on which the pixel section and driving circuits are formed, are bonded together using a sealant layer 568. After the filler is mixed into the sealant 568, the two substrates are bonded together at the same intervals using the filler and columnar spacers. Thereafter, a liquid crystal material 575 is injected between the substrates, and the substrates are completely sealed with a sealant (not shown). For the liquid crystal material 575, known liquid crystal materials can be used. Thus, the reflective liquid crystal display device shown in Figure 12 is completed. If necessary, the active matrix substrate or counter substrate can be separated into the required shape. Additionally, the polarizing plate (not shown) is only attached to the counter substrate. Then, the flexible printed circuit (FPC) is bonded using known techniques.

The liquid crystal display panel manufactured as described above can be used as the display part of various electronic devices. The liquid crystal display panel can be fully utilized for large areas without reducing the aperture ratio of the pixel segments.

This embodiment can be freely combined with any of Embodiments 1-5.

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[Embodiment 7]

In this embodiment, the manufacturing process of an active matrix type liquid crystal display device will be described with reference to Figure 13, and this liquid crystal display device is distinct from the liquid crystal display device in embodiment 6, which uses the active matrix substrate manufactured in embodiment 5.

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First, according to Embodiment 5, an active matrix substrate as shown in Figure 8A to Figure 8C is obtained. Thereafter, an alignment film 1067 is formed on the active matrix substrate shown in FIGs. 8A to 8C, and a rubbing treatment is performed. In this embodiment, before forming the alignment film 1067, an organic resin film, such as an acrylic resin film, is shaped to create columnar spacers 572 at required positions to maintain substrate gaps. Furthermore, spherical spacers can be distributed across the entire surface of the substrate instead of columnar spacers.

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Then, an auxiliary substrate 1068 is prepared. The auxiliary substrate is provided with a color filter, in which a color layer 1074 and a light shielding layer 1075 are arranged to correspond to each pixel. Light shielding layers 1077 are evenly formed in the driver circuit section. A leveling film 1076 covering the color filter and the light shielding layer 1077 is provided. Then, a counter electrode 1069 made of a transparent conductive film on the leveling film 1076 is formed in the pixel section, and an adjustment film 1070 is formed over the entire surface of the auxiliary substrate 1068, followed by a rubbing treatment.

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Then, the active matrix substrate and the auxiliary substrate, on which pixel segments and driving circuits are formed, are bonded together using a sealant layer 1071. Fillers are mixed into the sealant layer 1071, and the two substrates are bonded to each other at the same intervals using the fillers and columnar spacers. Thereafter, liquid crystal material 1073 is injected between the substrates, and the substrates are completely sealed with a sealant (not shown). For liquid crystal material 1073, a known liquid crystal material can be used. Thus, the active matrix type liquid crystal display device shown in Figure 11 is completed. If necessary, the active matrix substrate or auxiliary substrate can be separated into the required shape. In addition, polarization plates and the like can be appropriately provided using known techniques. The FPC is then bonded using known techniques.

25

The liquid crystal display panel manufactured as described above can be used as the display portion of various electronic devices. The liquid crystal display panel can be fully utilized for large areas without reducing the aperture ratio of the pixel section.

30

This embodiment can be freely combined with any of Embodiments 1 to 5.

[Embodiment 8]

In this embodiment, as an application of the wiring board of the present invention, the typical production situation of light-emitting devices will be described using the TFT manufacturing method, which is employed for producing the active matrix substrate in Embodiment 5. In this specification, the light-emitting device is referred to as a display panel, in which the light-emitting element formed on the substrate is sealed between the substrate, the cover member, and the display module, wherein the IC is mounted on the display panel within the display module. The light-emitting element includes a light-emitting layer containing organic compounds, enabling electroluminescence from an electric field, along with an anode layer and a cathode layer. Furthermore, luminescence in an organic compound includes fluorescence generated when a singlet excited state returns to a normal state and phosphorescence produced when a triplet excited state returns to a normal state. Either one or both types of luminescence are included.

In this specification, all layers formed between the anode and the cathode in a light-emitting element are defined as organic light-emitting layers. Specifically, the organic light-emitting layers include a light-emitting layer, a hole injection layer, an electron injection layer, a hole transport layer, an electron transport layer, and so on. The basic structure of a light-emitting element consists of the sequential stacking of an anode layer, a light-emitting layer, and a cathode layer. In addition to the above structure, the light-emitting element may have the following structures: A structure in which an anode layer, a hole injection layer, a light-emitting layer, and a cathode layer are stacked in sequence; or a structure in which an anode layer, a hole injection layer, a light-emitting layer, an electron transport layer, and a cathode layer are stacked in sequence, etc.

Figure 14 is a cross-sectional view of the light-emitting device of this embodiment. In Figure 14, a switching TFT603 provided on substrate 700 is formed using the n-channel TFT503 shown in Figure 10. Regarding the configuration of the switching TFT603. Refer to the description of the n-channel TFT503.

Although the present embodiment illustrates a double-gate structure with two channel formation regions, a single-gate structure with one channel formation region or a triple-gate structure with three channel formation regions may also be used.

The driving circuit provided on substrate 700 is formed using the CMOS circuit shown in Figure 10. Therefore, for the description of the driving circuit configuration, refer to the description of the n-channel TFT 501 and the p-channel TFT 502. Although the present embodiment illustrates a single-gate structure, a double-gate structure or a triple-gate structure may also be used.

Furthermore, wires 701 and 703 function as source lines for the CMOS circuit, while wire 702 functions as a drain line. Wiring 704 functions to electrically connect the source line 708 to the source region of the switching TFT, while wiring 705 functions to electrically connect the drain line 709 to the drain region of the switching TFT.

The current control TFT 604 is formed using the p-channel TFT 502 in Figure 10. Therefore, the description of the current control TFT 604 can refer to the description of the p-channel TFT 502. Although the present embodiment represents a single-gate structure, a double-gate structure or a triple-gate structure may also be used.

Wiring 706 serves as the source line (equivalent to the current supply line) for the current control TFT 604, and reference numeral 707 denotes an electrode that is electrically connected to the pixel electrode 711 by overlapping with it.

The pixel electrode 711 is the anode of the light-emitting element and is made of a transparent conductive film. As the transparent conductive film, a mixture of indium oxide and tin oxide, a mixture of indium oxide and zinc oxide, zinc oxide, tin oxide, or indium oxide can be used. A transparent conductive film containing gallium may be used. Before forming the aforementioned wiring, the pixel electrode 711 is formed on the flat interlayer insulating film 710. In this embodiment, it is extremely important to use the resin-based leveling film 710 to level the step difference caused by the TFT. The light-emitting layer to be formed later is very thin, so light emission defects may occur due to the presence of step differences. Therefore, it is preferable to smooth the surface before forming the pixel electrode so that the light-emitting layer can be formed on a flat surface.

After the conductive lines 701-707 are formed, a wiring pad 712 is formed, as shown in Figure 14. The wiring pad 712 can be formed by patterning an insulating film or an organic resin film containing silicon (thickness 100-400 nm).

Since wiring pad 712 is made of an insulating film, electrostatic breakdown of elements should be considered during the film formation process. In this embodiment, static electricity is suppressed by adding carbon particles or metal particles to the insulating film material used for wiring pad 712 to increase resistance. At this point, the amount of carbon particles or metal particles added can be adjusted to make the resistance $1 * 10^6 - 1 * 10^{12} \Omega \cdot m$ (preferably $1 * 10^8 - 1 * 10^{10} \Omega \cdot m$).

A light-emitting layer 713 is formed on the pixel electrode 711. Although one pixel is shown in Figure 14, the formed light-emitting layers should correspond to R (red), G (green), and B (blue) in this embodiment. Furthermore, in this embodiment, the low-molecular-weight organic light-emitting material is formed via vapor deposition. More specifically, a stacked structure is used, in which a copper phthalocyanine (CuPc) film (thickness: 20 nm) is provided as a hole injection layer, and a tris (8-hydroxyquinoline) aluminum complex (Alq₃) film (thickness: 70 nm) is provided as a light-emitting layer on the hole injection layer. By adding fluorescent substances such as dihydroxyquinoline acridine, terrylene, or DCM1 to Alq₃, the color of the emitted light can be controlled.

It should be noted that typical organic light-emitting materials that can be used as the light-emitting layer have been described above, but the present embodiment is not limited thereto. The light-emitting layer (for emitting light and transporting carriers of the emitted light) can be formed by any combination of a light-emitting layer, a charge transport layer, or a charge injection layer. In this embodiment, a low-molecular-weight organic light-emitting material is used as the light-emitting layer; however, medium-molecular-weight or high-molecular-weight organic light-emitting materials may also be used. In this specification, medium molecular weight organic light-emitting materials refer to those without sublimation properties, containing 20 or fewer molecules, or having a linked molecule length of 10 μm or shorter. In addition, as an example of using high-molecular-weight organic luminescent materials, a stacked structure can be employed in which a poly (thiophene) (PEDOT) film (thickness: 20 nm) is spin-coated as a hole injection layer, and a poly (p-phenylene vinylene) (PPV) film (thickness: approximately 100 nm) is formed as the light-emitting layer on the hole injection layer. When using π -conjugated polymers such as PPV, emission wavelengths ranging from red to blue can be selected. Furthermore, it is possible to use inorganic materials such as silicon carbide as the charge transport layer or charge injection layer. Known materials can be used as the organic light-emitting materials and inorganic materials.

Next, a cathode 714 made of a conductive film is formed on the light-emitting layer 713. In this embodiment, alloy films of aluminum and lithium are used as conductive films. Needless to say, a known MgAg film (an alloy film of magnesium and silver) may be used. As the cathode material, a conductive film made of an element belonging to Group 1 or Group 2 of the periodic table, or a conductive film containing these elements, may be used.

5 When the cathode 714 is formed, the light-emitting element 715 is completed. The light-emitting element 715 here refers to a diode formed by a pixel electrode (anode) 711, a light-emitting layer 713, and a cathode 714.

It is useful to form a passivation film 716 to completely cover the light-emitting element 715. As the passivation film 716, an insulating film with a single-layer or multi-layer structure, such as a carbon film, a silicon nitride film, or a silicon oxynitride film, may be used.

10 In such cases, it is preferable to use a film with satisfactory coverage as the passivation film. The use of carbon films (particularly DLC films) is effective. Since the DLC film can be formed in a temperature range from room temperature to 100° C, the DLC film can be easily formed even on the light emitting layer 713 with low heat resistance. In addition, due to its high oxygen shielding effect, the DLC film can suppress formation over the light-emitting layer 713 and can be easily formed. Furthermore, due to its high barrier effect against oxygen, the DLC
15 film can suppress oxidation of the light-emitting layer 713. Therefore, the light-emitting layer 713 can be protected from oxidation during subsequent sealing processes.

Furthermore, a sealant layer 717 is formed on the passivation film 716, and a cover member 718 is bonded to the sealant layer 717. As the sealant layer 717, a UV-curable resin can be used, and it is effective to add hygroscopic materials or materials with antioxidant properties to the sealant layer 717. Furthermore, in this embodiment, as the
20 cover member 718, a glass substrate, quartz substrate, or a plastic substrate (including a plastic film) with carbon film (preferably DLC film) formed on both sides is used.

Therefore, the light-emitting device with the configuration shown in Figure 14 is completed. After the terminal block 712 is formed, it is effective to continuously perform the process of forming the passivation film 716 without exposing it to the environment in a multi-chamber type (or tandem type) thin film forming apparatus. It is possible to continuously carry out the process until adhesive cover part 718 without exposing it to the aforementioned environment.

Thus, n-channel TFTs 601 and 602, a switching TFT (n-channel TFT) 603, and a current control TFT (n-channel TFT) 604 are formed on the substrate 700.

Furthermore, as shown in Figure 14, by forming the impurity layer to overlap with the gate electrode via the insulating film, an n-channel TFT that is less likely to degrade due to the hot carrier effect can be formed. Therefore, a highly reliable light-emitting device can be obtained.

In this embodiment, only the configuration of the pixel segments and the driving circuit is shown. However, according to the manufacturing process of this embodiment, logic circuits such as signal separation circuits, D/A converters, operational amplifiers, and γ -correction circuits can be formed on the same insulator. Furthermore, even memory and microprocessors can be formed.

Following the sealing (or encapsulation) process conducted to protect the light-emitting element, the light-emitting device of this embodiment will be described with reference to Figure 15A and Figure 15B. If necessary, reference numerals used in Figure 14 will be cited.

Figure 15A is a top view showing the state when the light-emitting element is completely sealed. Figure 15B is a cross-sectional view taken along the line C-C' in Figure 15A. The sections enclosed by dashed lines and denoted by reference numerals 801, 806, and 807 are respectively the source side driving circuit, the pixel section, and the gate side driving circuit. Reference numeral 901 denotes a cover member, 902 denotes a first sealing layer, 903 denotes a second sealing layer, and a sealing material 907 is formed in the inner section enclosed by the sealing layer 902.

Reference numeral 904 denotes wiring, which transmits signal input to the source side driving circuit 801 and the gate side driving circuit 807 and receives video signals and clock signals from the flexible printed circuit (FPC) to be the external input terminal. Here, although only the FPC is shown, a printed wiring board (PWB) can also be connected to the FPC. The light-emitting device in this specification includes not only the light-emitting device itself but also a light-emitting device equipped with an FPC or a PWB.

Next, the cross-sectional configuration diagram will be explained with reference to Figure 15B. The pixel segment 806 and the gate side driving circuit 807 are formed over substrate 700. The pixel segment 806 is composed of the current control TFT 604 and a plurality of pixels including a pixel electrode 710, and the pixel electrode 710 is electrically connected to the drain line of the current control TFT 604. Furthermore, the gate side driving circuit 807 is composed of a CMOS circuit (see Figure 14), which is obtained by combining an n-channel TFT 601 and a p-channel TFT 602.

Pixel electrode 711 serves as the anode of the light-emitting element. Wiring terminals 712 are formed at both ends of pixel electrode 711, and the light-emitting layer 713 and cathode 714 of the light-emitting element are formed on pixel electrode 711.

The cathode 714 serves as a common wiring for all pixels and is electrically connected to the FPC 905 through a connecting line 904. In addition, all components contained within the pixel segment and the gate-side driving circuit 807 are covered by the cathode terminal 14 and the passivation film 716.

5 The cover 901 is bonded to the first sealing layer 902. A spacer made of resin film may be formed to ensure the gap between the cover 901 and the light-emitting element. The inner section of the first sealing layer 902 is filled with sealing material 907. Epoxy resin is preferably used for the first sealant layer 902 and the sealing material 907. Preferably, the first sealant layer 902 is less likely to transmit moisture and oxygen. In addition, the sealing material 907 may contain materials with hygroscopic and antioxidative properties.

10 The sealing material 907, formed to cover the light-emitting element, also serves as an adhesive for bonding the cover 901. In this embodiment, materials for the plastic substrate 901a constituting the cover member 901 may include fiberglass reinforced plastic (FRP), polyvinyl fluoride (PVF), polyester resin, polyester, or acrylic resin.

Furthermore, after bonding the cover member 901 to the sealing material 907, a second sealant layer 903 is formed to cover the side surface (exposed surface) of the sealing material 907. The second sealant layer 903 may be made using the same material as that used for the first sealant layer 902.

15 In the above configuration, by encapsulating the light-emitting element with the sealing material 907, the light-emitting element can be completely isolated from the external environment. This prevents accelerated erosion of the light-emitting layer material due to oxidation, such as moisture and oxygen, from external intrusion. Thus, a highly reliable light-emitting device is obtained. Furthermore, the light-emitting device is fully suited for large-area applications without reducing the aperture ratio of the pixel section.

20 This embodiment can be arbitrarily combined with any one of Embodiments 1 to 5.

[Embodiment 9]

In this embodiment, a light-emitting device with a different pixel configuration from that of previous embodiments will be described with reference to Figure 16.

25 In Figure 16, as the current control TFT 4501, a TFT with the same configuration as the p-channel TFT 502 in Figure 10 is used, while as the switch TFT 4402, a TFT with the same configuration as the pixel TFT 504 in Figure 10 is used. Needless to say, the gate electrode of the current control TFT 4501 is electrically connected to the drain line of the switch TFT 4402. In addition, the drain line of the current control TFT 4501 is electrically connected to the pixel electrode 4504 formed on the insulating film 4409.

30 In this embodiment, the pixel electrode 4504 made of a conductive film functions as the cathode of the light-emitting element. More specifically, an alloy film of aluminum and lithium is used. A conductive film made of an element belonging to Group 1 or Group 2 of the periodic table or a conductive film doped with the element can be used.

5 A light-emitting layer 4505 is formed on the pixel electrode 4504. In Figure 16, only one pixel is shown. In this embodiment, a light-emitting layer corresponding to G (green) is formed by vapor deposition and coating (preferably spin coating). More specifically, the light-emitting layer has a multilayer structure, with a lithium fluoride (LiF) film (thickness: 20 nm) formed as the electron injection layer. On the lithium fluoride film, a polyphenylene vinylene (PPV) layer (thickness: 70 nm) is further formed as the light-emitting layer.

An anode 4506, made of a transparent conductive film, is formed on the light-emitting layer 4504. In this embodiment, the transparent conductive film is made from a mixture of indium oxide and zinc oxide or their oxide mixture.

10 Once the anode 4506 is formed, the light-emitting element 4507 is completed. Here, the light-emitting element 4507 refers to a diode formed by the pixel electrode (anode) 4504, the light-emitting layer 4505, and the anode 4506.

It is beneficial to form a passivation film 4508 to completely cover the light-emitting element 4507. As the passivation film 4508, an insulating film with either a single-layer structure or a multi-layer structure is used, including carbon films, silicon nitride films, or silicon oxynitride films.

15 Additionally, a sealing material 4509 is formed on the passivation film 4508, and a cover 4510 is bonded to the sealing material 4509. As the sealing material 4509, a UV-curable resin can be used, and it is effective to add materials with hygroscopic or anti-oxidation properties to the sealing material 4509. In this embodiment, as the cover member 4510, a glass substrate, a quartz substrate, or a plastic substrate (including a plastic film) with carbon films (preferably DLC films) formed on both sides thereof is used.

20 In the wiring of light-emitting devices manufactured in this manner, low resistance is achieved, making such light-emitting devices fully suitable for large areas without lowering the aperture ratio of pixel segments.

This embodiment can be freely combined with any of Embodiments 1-5.

[Embodiment 10]

25 In this embodiment, a typical liquid crystal display device according to the present invention will be described. The configuration of TFTs in the device differs from that of the active matrix substrate manufactured in Embodiment 5.

On the active matrix substrate shown in Figure 18A, a driving circuit 506 having an n-channel TFT 503 and a p-channel TFT 502, and a pixel segment 507 having a pixel TFT 504 and a storage capacitor 505, are formed.

30

These TFTs are obtained by forming gate lines 512-517 on substrate 501, forming insulating films 511 (511a and 511b) on the gate lines 512-517 (512a-517a, 512b-517b, and 512c-517c), and forming channel formation regions, source regions, drain regions, LDD regions, etc., in the semiconductor layer over the insulating films. The semiconductor layer is formed in the same manner as in Embodiments 1 to 5 according to the present invention.

5 The total thickness of the gate lines 512-517 should be 200-400 nm (preferably 250 nm), allowing the gate lines 512-517 to be tapered to improve the step coverage of the coating film formed on the upper layers. The gate lines 512-517 are formed so that the tapered angle becomes 5°-30° (preferably 15°-30°). The tapered section is formed through dry etching, and its angle is controlled by the etching gas and the bias applied to the substrate side.

10 Additionally, impurity regions are formed during the first to second doping processes. First, the first doping process is carried out to form the LDD region of the n-channel TFT. Doping can be carried out by means of ion doping or ion implantation. Phosphorus (P) is added as an impurity element introducing n-type (donor) characteristics, and the first impurity region is formed with a mask. Then, a mask is reformed to cover the LDD region of the n-channel TFT, thereby forming the source region and the drain region of the n-channel TFT during the second doping process.

15 During the third doping process, the source region and the drain region of the p-channel TFT are formed. Doping is performed using ion doping or ion implantation, with only impurity elements introducing P-type (acceptor) properties being added. At this time, the semiconductor layer in which the n-channel TFT is to be formed is covered with a mask, so the p-type impurity elements will not be added to the semiconductor layer. In this embodiment, although LDD regions are not formed in the p-channel TFT, they may be formed.

20 Thus, in the n-channel TFT 503, the LDD region 530 and the source or drain region 531 are formed outside the channel formation region 529. The p-channel TFT 502 also has the same configuration and is composed of a channel formation region 527 and a source or drain region 528. In the present embodiment, a single-gate structure is used; however, a dual-gate structure or a triple-gate structure may be utilized.

25 In the pixel segment 507, the pixel TFT 504, formed by an n-channel TFT, adopts a multi-gate structure to reduce OFF current, and the LDD region 533 as well as the source or drain regions 534-536 are formed outside the channel formation region 532.

30 The interlayer insulating film is composed of a first interlayer insulating film 540 (thickness: made of inorganic materials such as silicon oxide, silicon nitride, or silicon oxynitride. 50-500nm) and a second interlayer insulating film 541 made of organic insulating materials such as polyimide, acrylic resin, polyimide amide, and benzocyclobutene (BCB). Thus, the surface of the interlayer insulating film can be satisfactorily flattened through the second interlayer insulating film formed from organic insulating materials. Organic resin materials typically have a low dielectric constant, enabling them to reduce parasitic capacitance. However, organic resin materials are not suitable for use as protective films due to their hygroscopicity and are preferably combined with the first interlayer insulator 540.

Thereafter, a resist mask with a predetermined pattern is formed, and contact holes are created which extend to the source region or the drain region formed in the semiconductor layer. The contact holes are formed through dry etching. In this case, a mixed gas of CF₄, O₂, and He is used as the etching gas to first etch the second interlayer insulating film 541 made of an organic resin material, followed by using CF₄ and O₂ as the etching gas to etch the first interlayer insulating film 540.

Then, a conductive metal film is formed through sputtering or vacuum vapor deposition. Thus, a resist mask pattern is formed, and the wirings 543 to 549 are formed through etching. In this way, an active matrix substrate can be formed.

The process of manufacturing an active matrix-type liquid crystal display device using the active matrix substrate shown in Figure 18A will be described. Figure 18B shows a state where the active matrix substrate is bonded to the sub-substrate 554 using the sealant 558. First, columnar spacers 551 and 552 are formed on the active matrix substrate shown in Figure 18A. The spacer 551 provided in the pixel segment is formed so as to overlap with the contact segment on the pixel electrode. Although it will vary depending on the liquid crystal material to be used, the height of the spacers is set at 3-10 μm. In the contact section, a recessed section is formed corresponding to the contact hole. Thus, by aligning the formed spacers with the recessed sections, the orientation of the liquid crystal can be protected from interference. Subsequently, an alignment film 553 is formed and undergoes rubbing treatment. A transparent conductive film 555 and an alignment film 556 are formed on the auxiliary substrate 554. Then, the active matrix substrate and the auxiliary substrate are connected to each other, and liquid crystal 557 is injected into the gap between them.

The active matrix-type liquid crystal display device manufactured as described above can be used as a display instrument for various electronic devices. The aforementioned liquid crystal display panel is fully applicable to large areas without lowering the aperture ratio in the pixel segment.

This embodiment can be freely combined with any of Embodiments 1-5.

[Embodiment 11]

The case of manufacturing a light-emitting device using the active matrix substrate described in Embodiment 10 will be described.

In Figure 19, as the current control TFT4501, a TFT having the same configuration as the n-channel TFT503 shown in Figure 16 is used. Needless to say, the gate electrode of the current control TFT4501 is electrically connected to the drain line of the switching TFT4402. The drain line of the current control TFT 4501 is electrically connected to the pixel electrode 4504 formed on the insulating film 4409.

In this embodiment, the pixel electrode 4505 made of a conductive film serves as the cathode of the light-emitting element. More specifically, an alloy film of aluminum and lithium is used. A conductive film made of an element belonging to Group 1 or Group 2 of the periodic table or a conductive film doped with the element can be used.

5 A light-emitting layer 4505 is formed on the pixel electrode 4504. In Figure 19, only one pixel is illustrated. In this embodiment, the light-emitting layer corresponding to G (green) is formed via vapor deposition and coating (preferably spin coating). More specifically, a stacked structure is used, wherein a LiF film (thickness: 20 nm) is formed as an electron injection layer, and a PPV film (thickness: 70 nm) is further formed as the light-emitting layer.

10 Next, an anode 4506 made of a transparent conductive film is formed on the light-emitting layer 4505. In this embodiment, a conductive film made of a mixture of indium oxide and tin oxide or a mixture of indium oxide and zinc oxide is used.

When the anode 4506 is formed, the light-emitting element 4507 is completed. The light-emitting element 4507 refers to a diode composed of a pixel electrode (cathode) 4504, a light-emitting layer 4505, and an anode 4506.

15 It is beneficial to form a passivation film 4508 to completely cover the light-emitting element 4507. As the passivation film 4508, an insulating film with either a single-layer structure or a multi-layer structure is used, including carbon films, silicon nitride films, or silicon oxynitride films.

20 Furthermore, a sealing material 4509 is formed on the passivation film 4508, and a cover 4510 is bonded to the sealing material 4509. As the sealing material 4509, a UV-curable resin can be used, and it is useful to form a hygroscopic material or a material with anti-oxidation properties within the sealing material 4509. In this embodiment, as the cover 4510, a glass substrate, a quartz substrate, or a plastic substrate with a carbon film (preferably a DLC film) formed on both sides thereof (including plastic film) is used.

The light-emitting device manufactured in this way can be fully utilized for large-area applications without reducing the aperture ratio in the pixel segments.

25 This embodiment can be freely combined with any of Embodiments 1-5.

[Embodiment 12]

30 The wiring board formed according to the present invention can be used for various electro-optical devices (active matrix liquid crystal display devices, active matrix EC display devices, and active matrix light-emitting devices). Specifically, the present invention can be implemented in all electronic devices in which these electro-optical devices are incorporated into a display portion.

Examples of such electronic devices include personal computers and monitors. Figures 20A to 20C illustrate examples thereof.

Figure 20A shows a personal computer, which includes a main body 3001, an image input section 3002, a display section 3003, a keyboard 3004, and the like. The present invention is applied to the display portion 3003 and can be readily utilized for expanding the display portion 3003.

Figure 20B illustrates a playback device using a storage-program recording medium (hereinafter simply referred to as a recording medium), which includes a main body 3401, a display portion 3402, a speaker portion 3403, a recording medium 3404, operation switches 3405, and the like. This playback device utilizes digital versatile discs (DVDs), compact discs (CDs), and other media as recording media, and can be used for listening to music, watching movies, playing games, and browsing the Internet. The present invention can be applied to the display portion 3402. The present invention can be utilized to expand the display portion 3402 at any time.

Figure 20C illustrates a display device, which includes a main body 4101, a base 4102, a display portion 4103, and the like. The present invention can be applied to the display portion 4103. The display of the present invention is fully prepared for screen expansion. Specifically, the present invention is advantageous for displays with a diagonal size of 10 inches or greater (especially 30 inches or greater).

As described above, the application range of the present invention is extremely wide, and it can be applied to electronic devices across various fields. Furthermore, the electronic device of this embodiment can be obtained by utilizing a structure formed from any arbitrary combination of Embodiments 1 to 11.

By adopting the structure of the present invention, the following basic important facts can be obtained.

- (a) A simple method suitable for conventional wiring and the process of manufacturing wiring boards.
- (b) Achieving low resistance in wiring. Therefore, the degree of design freedom and pixel aperture ratio are increased.
- (c) Satisfactory coverage is achieved.
- (d) In semiconductor devices, such as active matrix liquid crystal display devices, while the above advantages are satisfactory, the area of the pixel segment is also increased. The present invention is fully prepared for the expansion of the screen, which will improve the operating characteristics and reliability of semiconductor devices.

Various other modifications will become apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of the invention. Therefore, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that such claims be broadly interpreted.

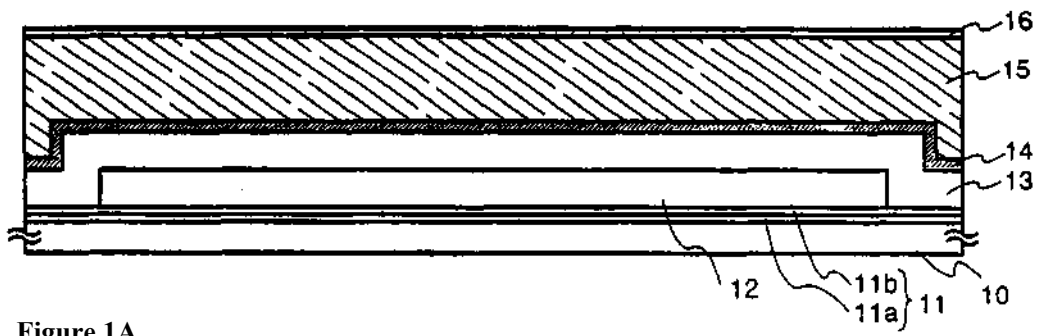


Figure 1A

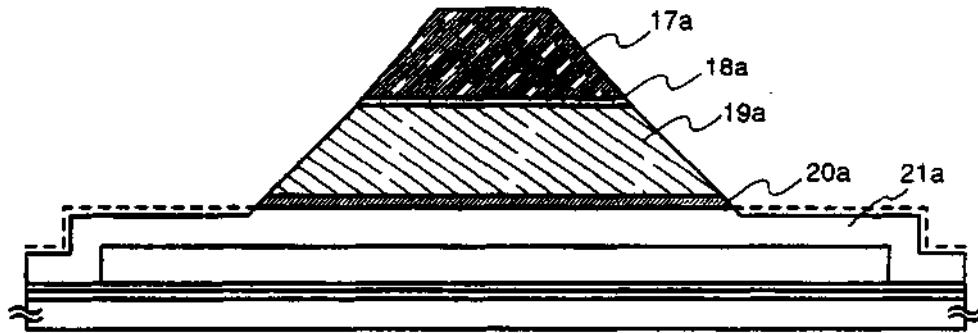


Figure 1B

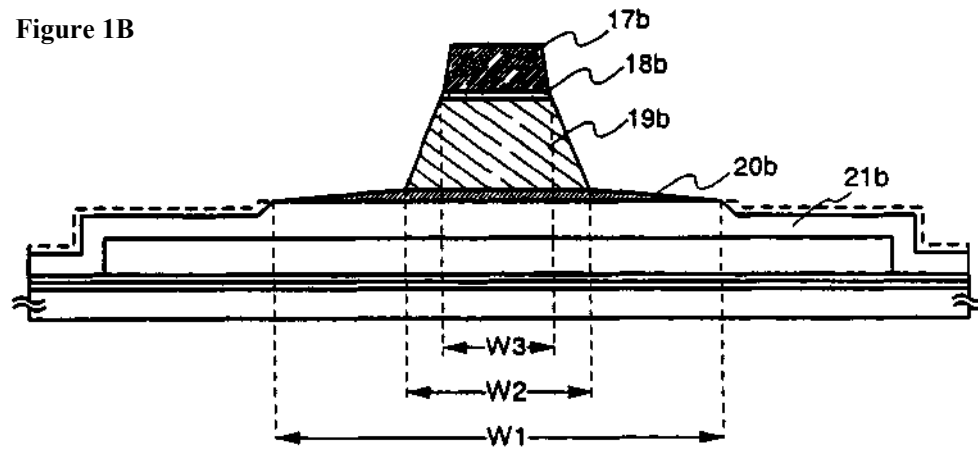


Figure 1C

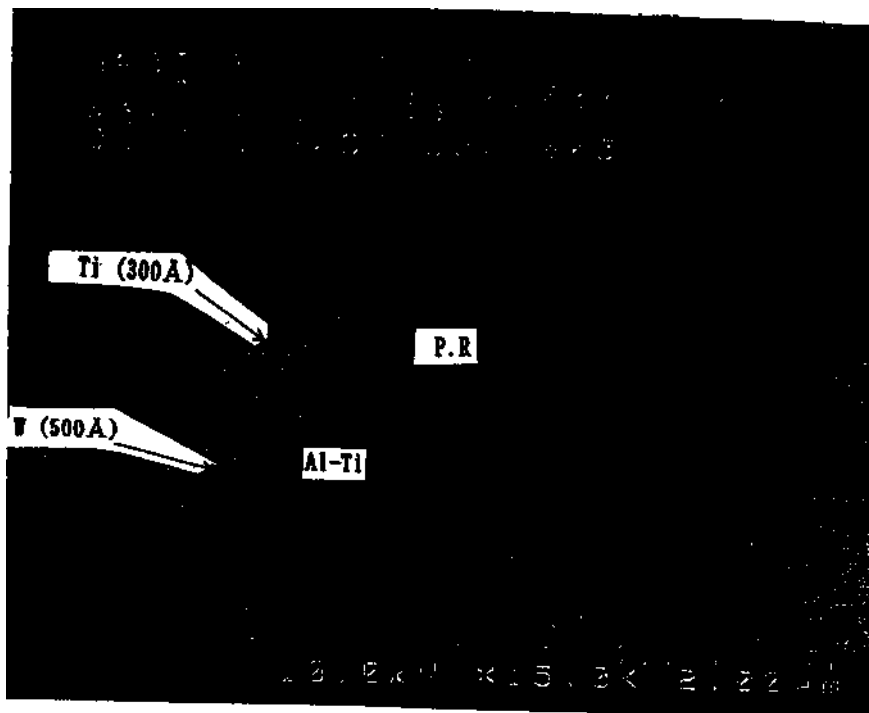


Figure 2A

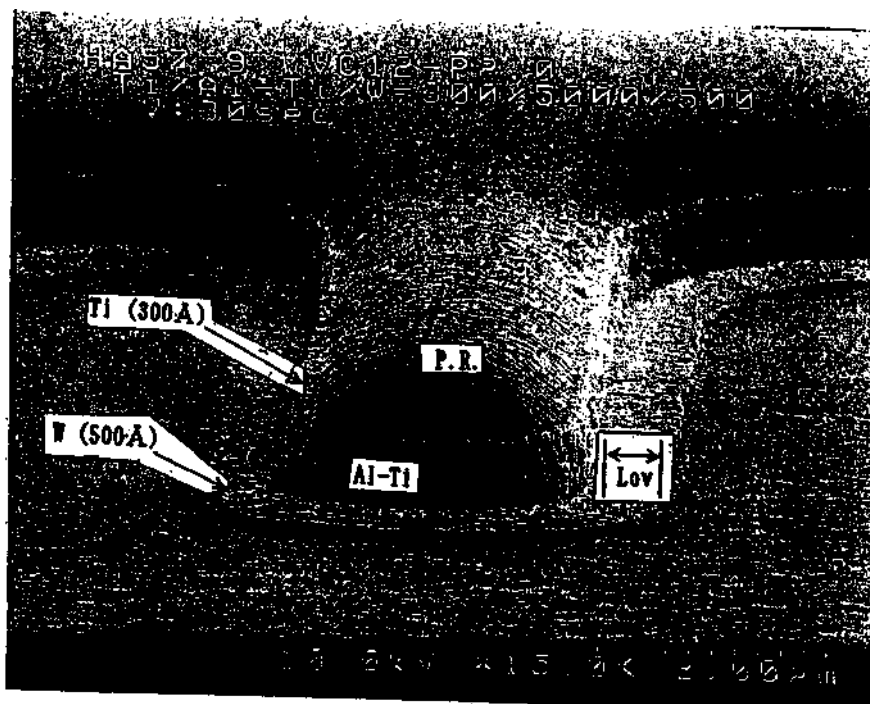


Figure 2B

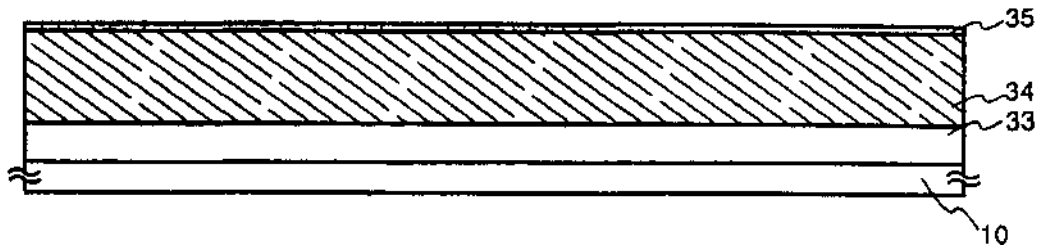


Figure 3A

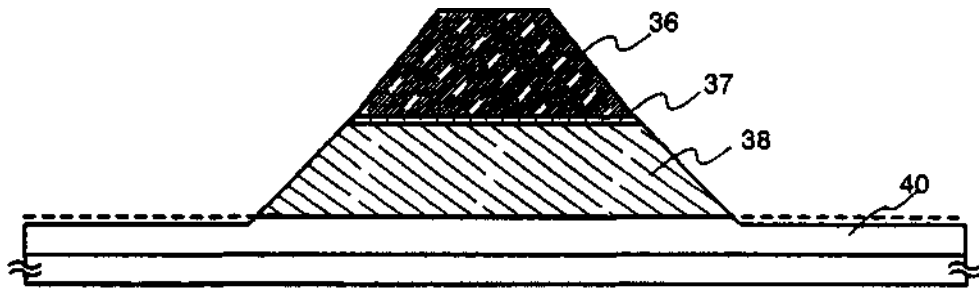


Figure 3B

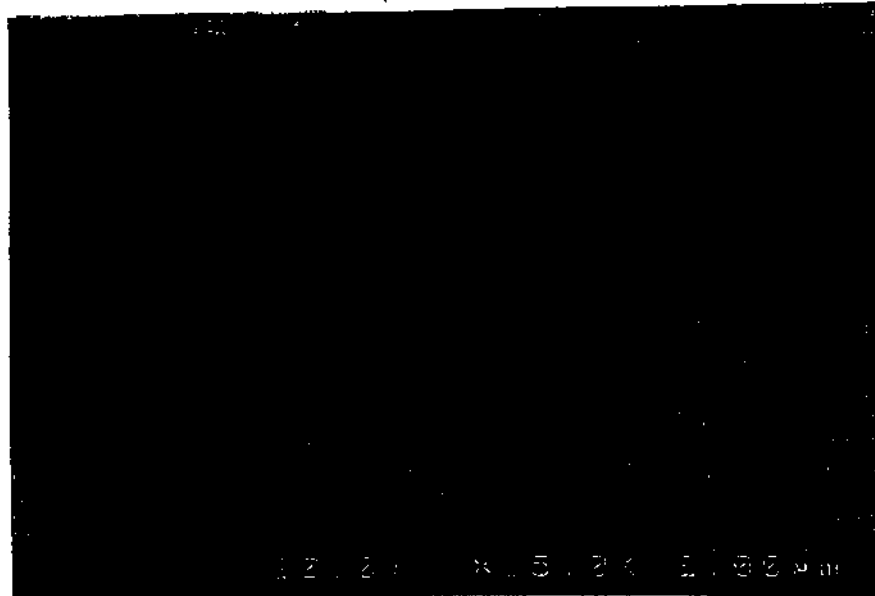


Figure 4A

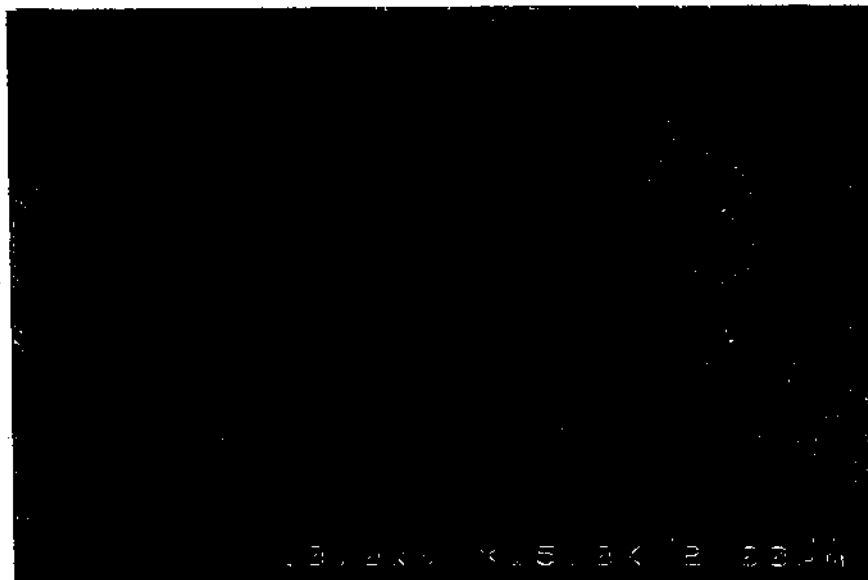


Figure 4B

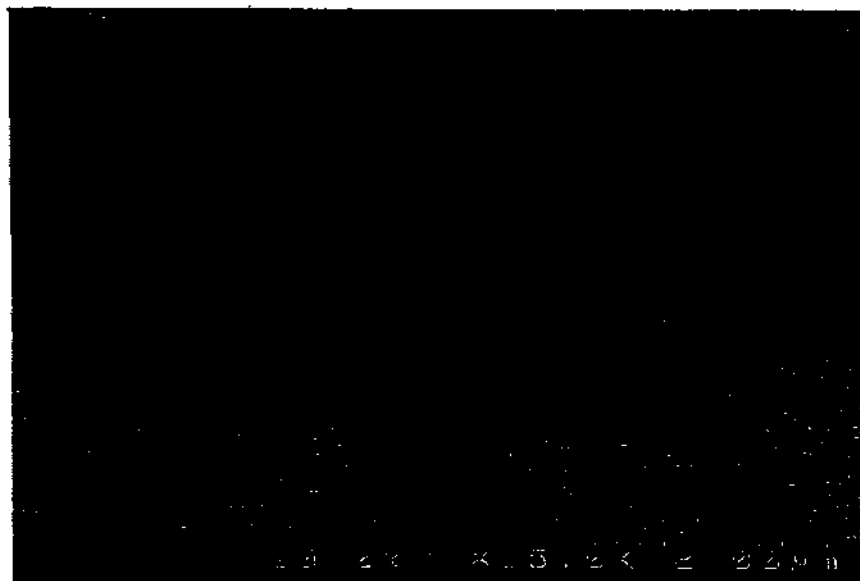


Figure 4C

Figure 5A

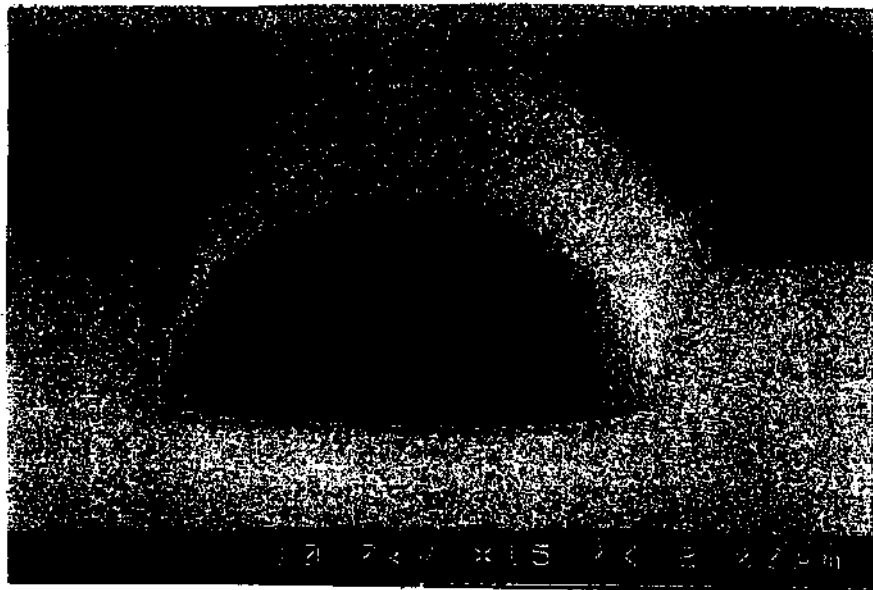
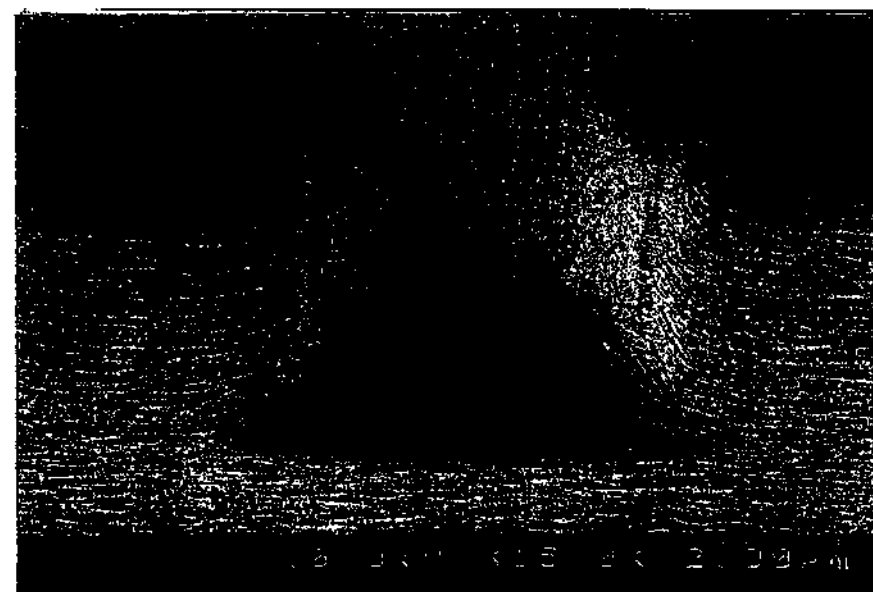


Figure 5B



Figure 5C



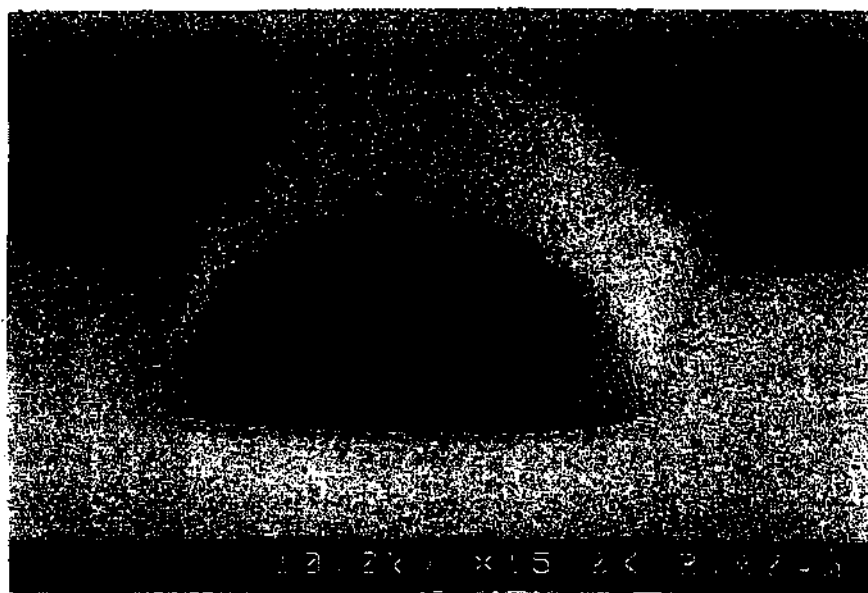


Figure 6A



Figure 6B

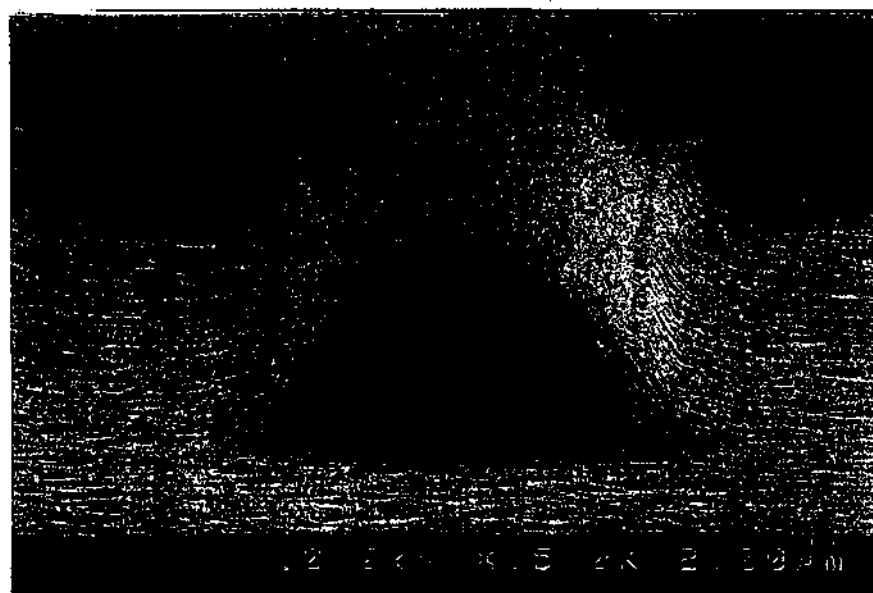


Figure 6C

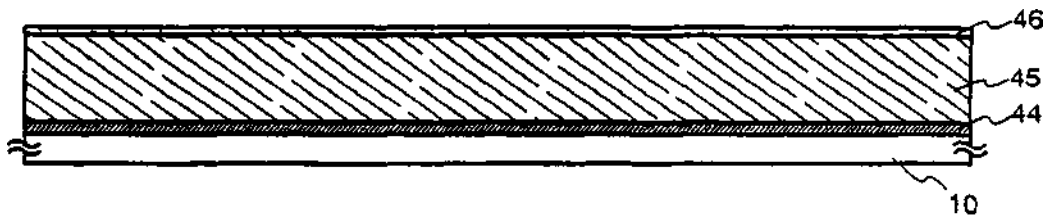


Figure 7A

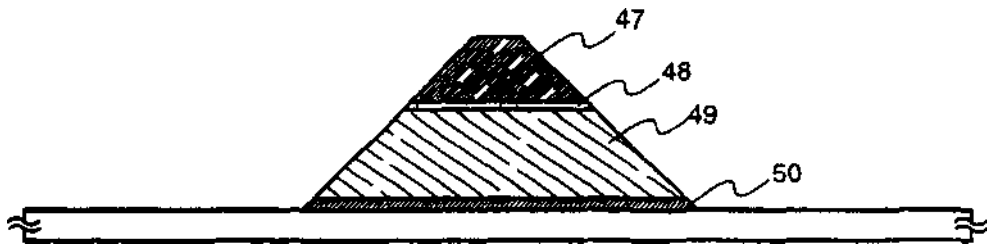


Figure 7B

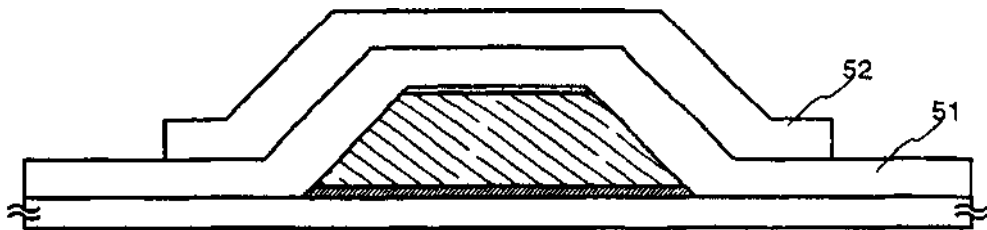


Figure 7C

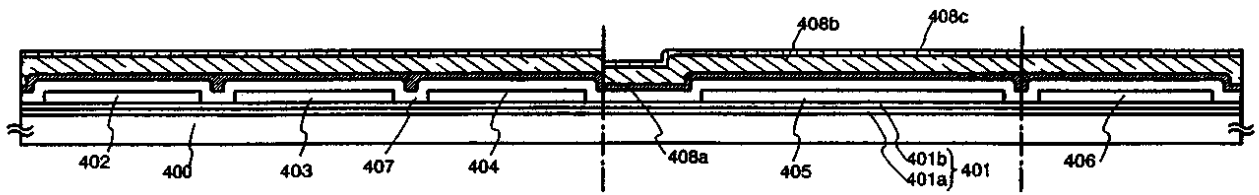


Figure 8A

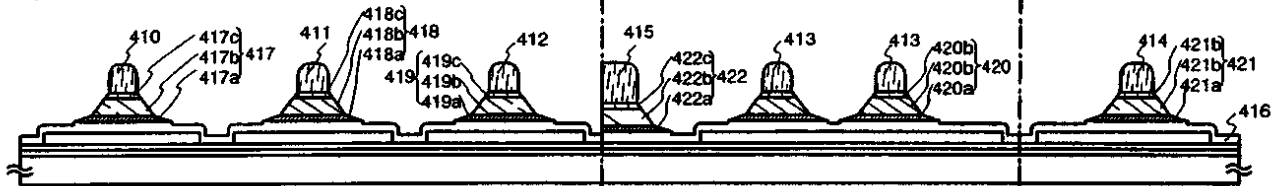


Figure 8B

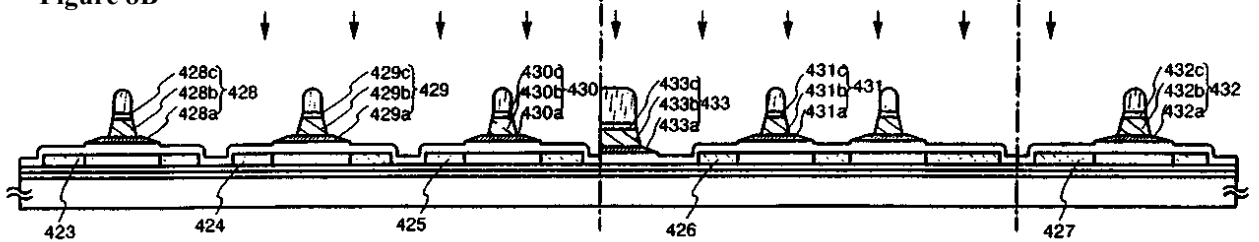


Figure 8C

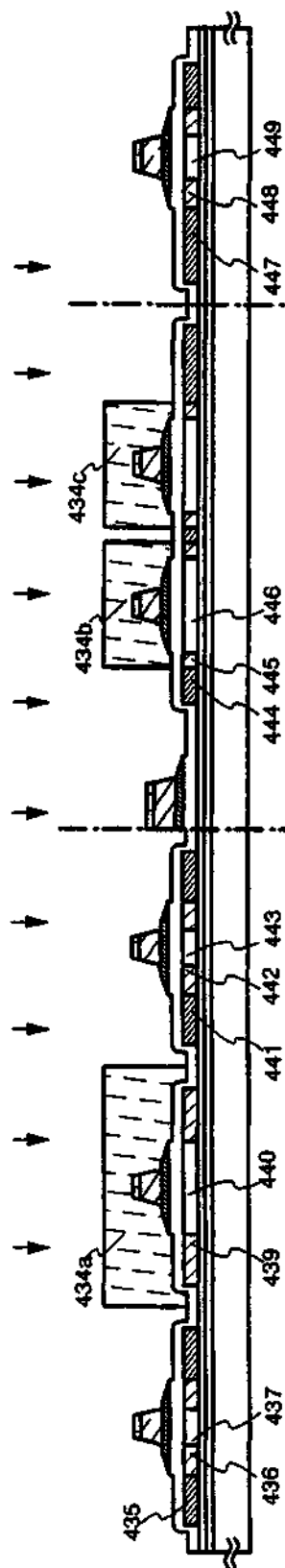


Figure 9A

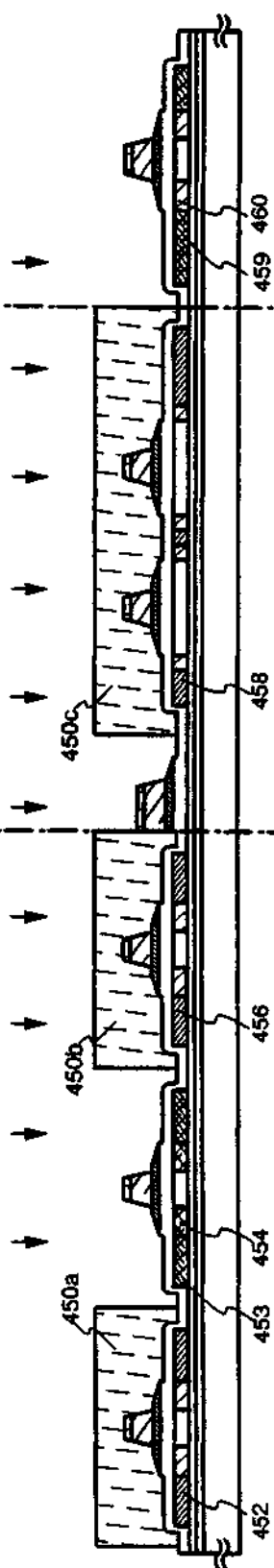


Figure 9B

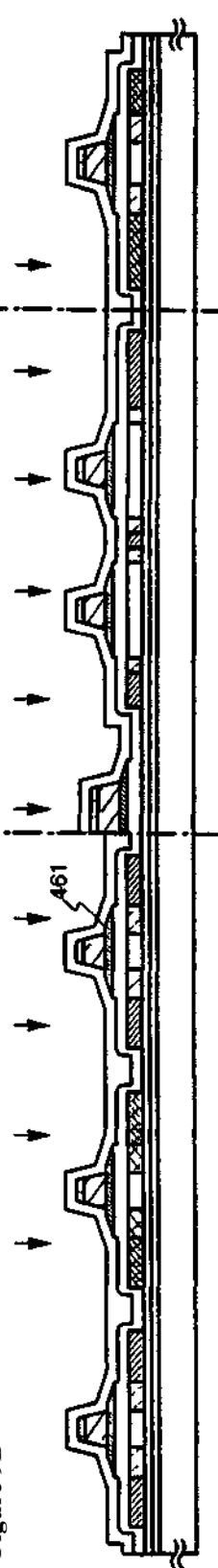


Figure 9C

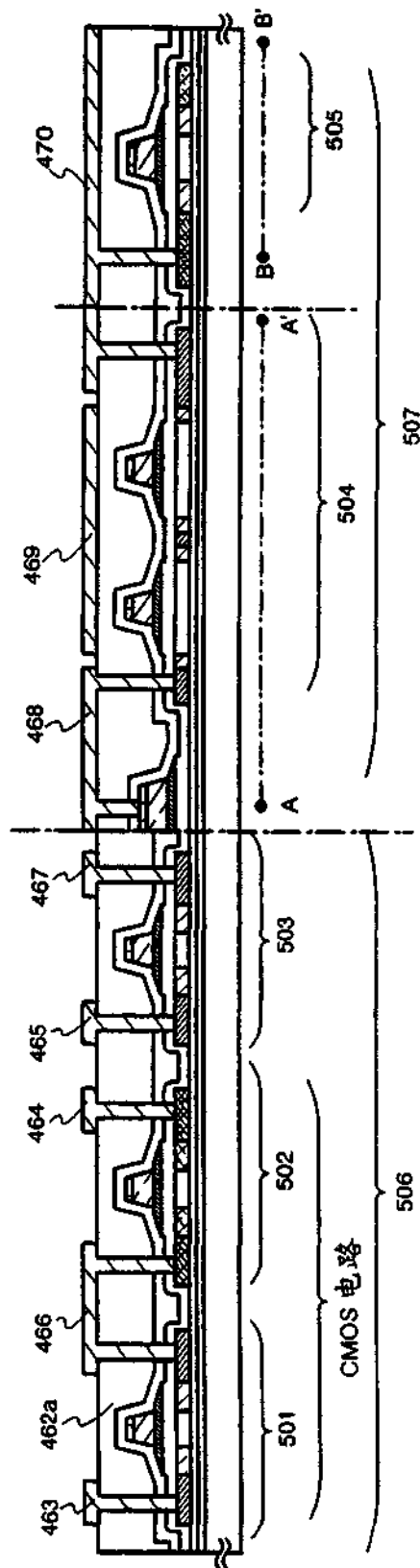


Figure 10

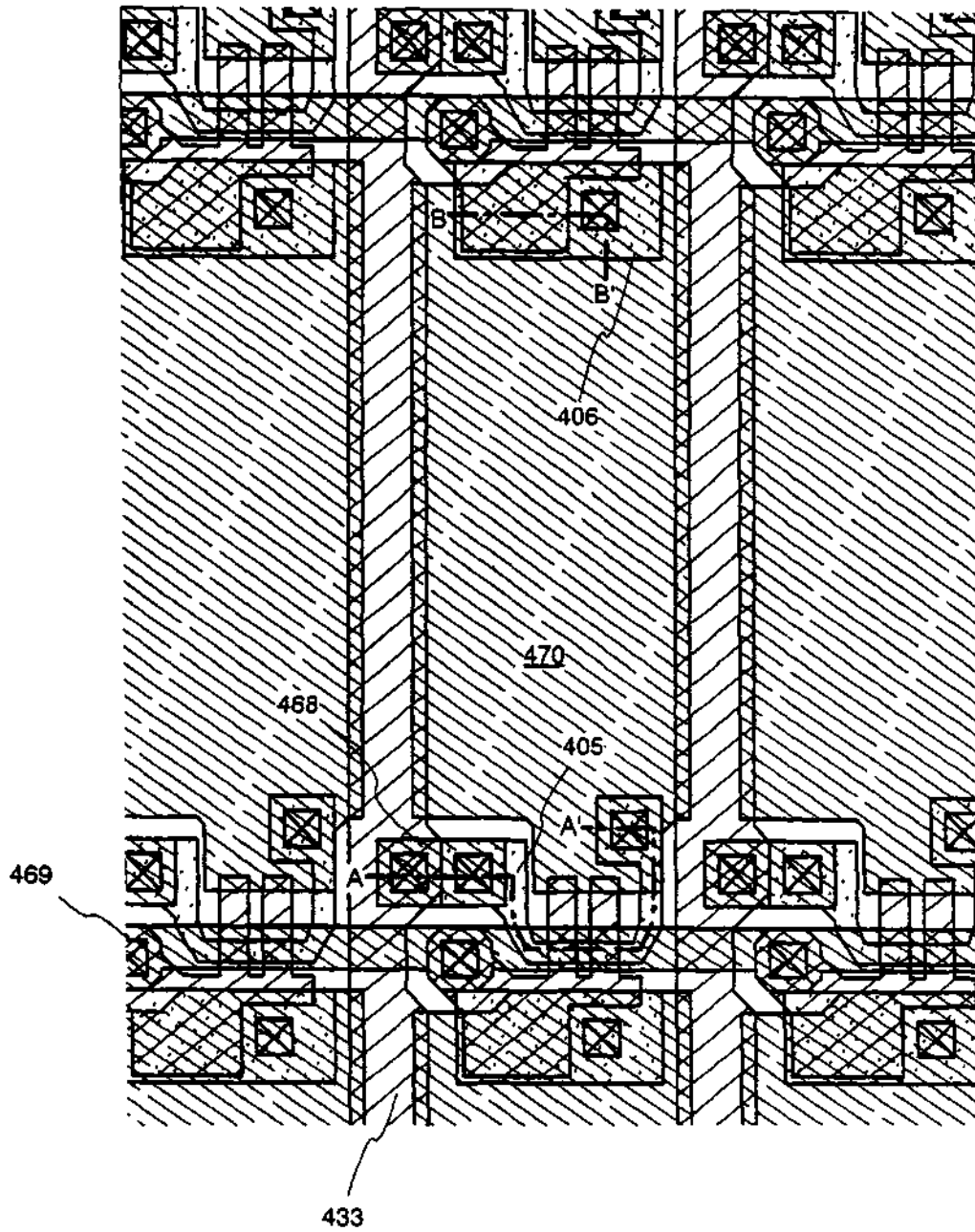


Figure 11

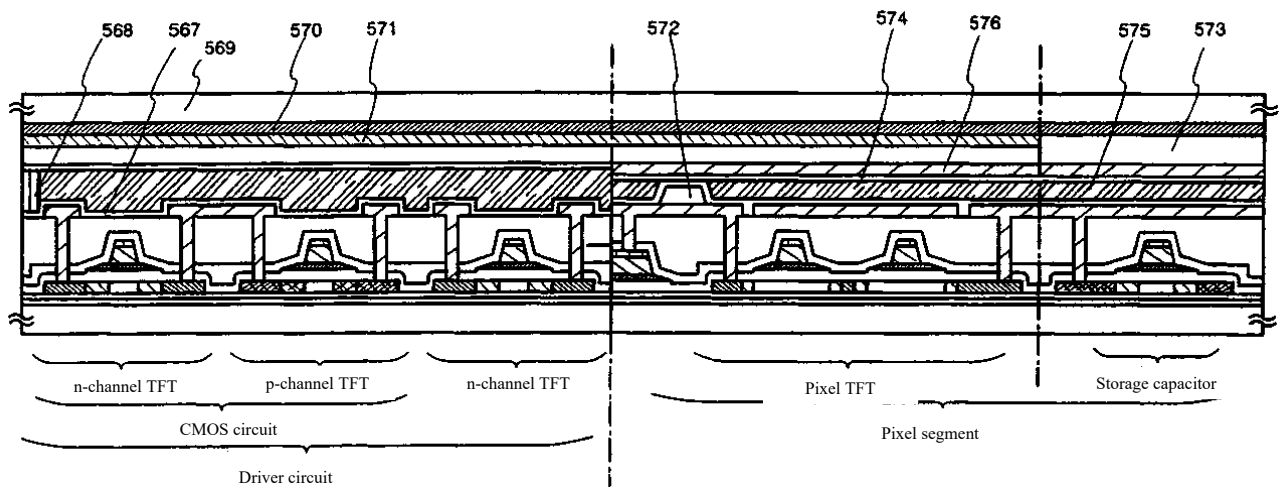


Figure 12

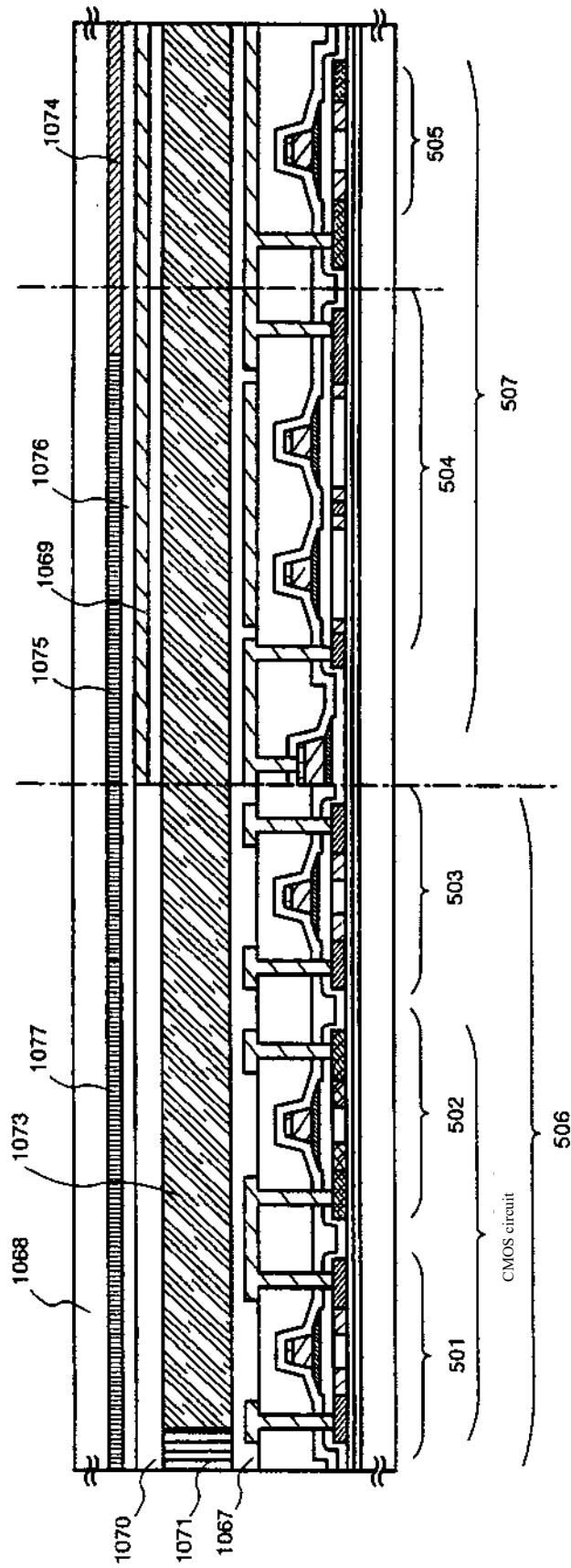


Figure 13

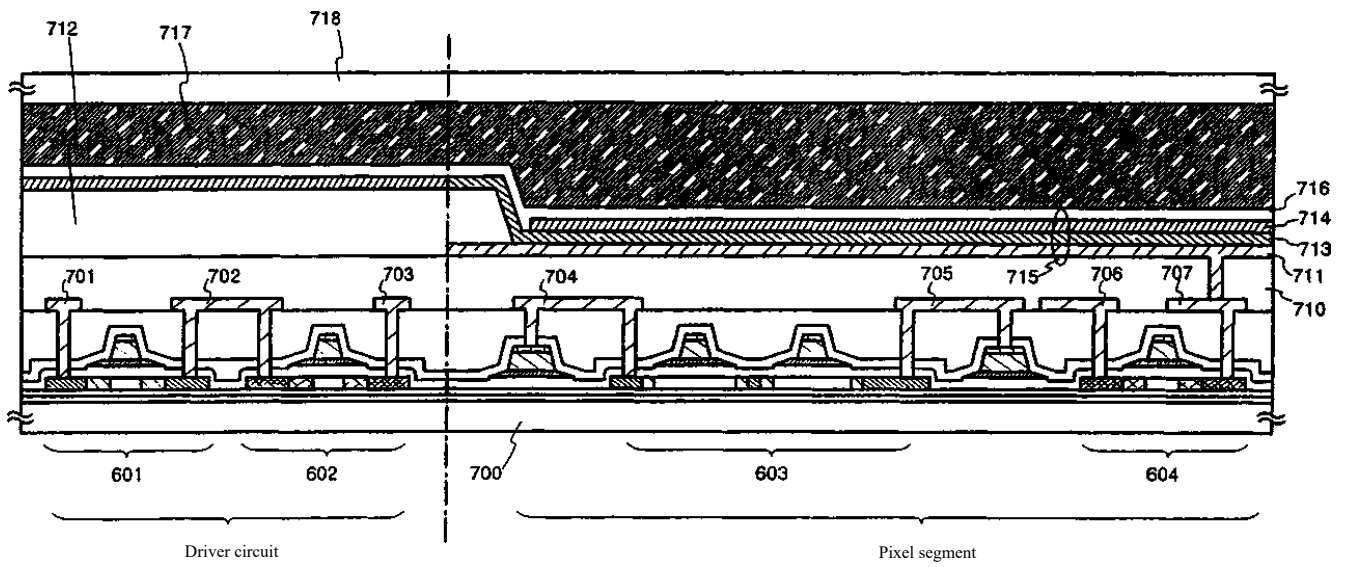


Figure 14

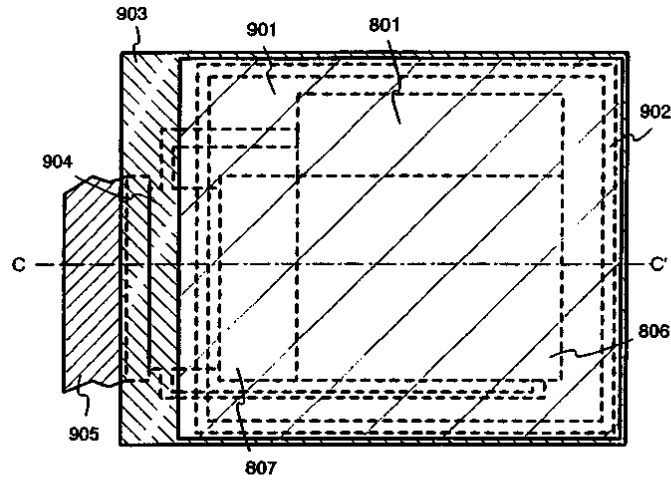


Figure 15A

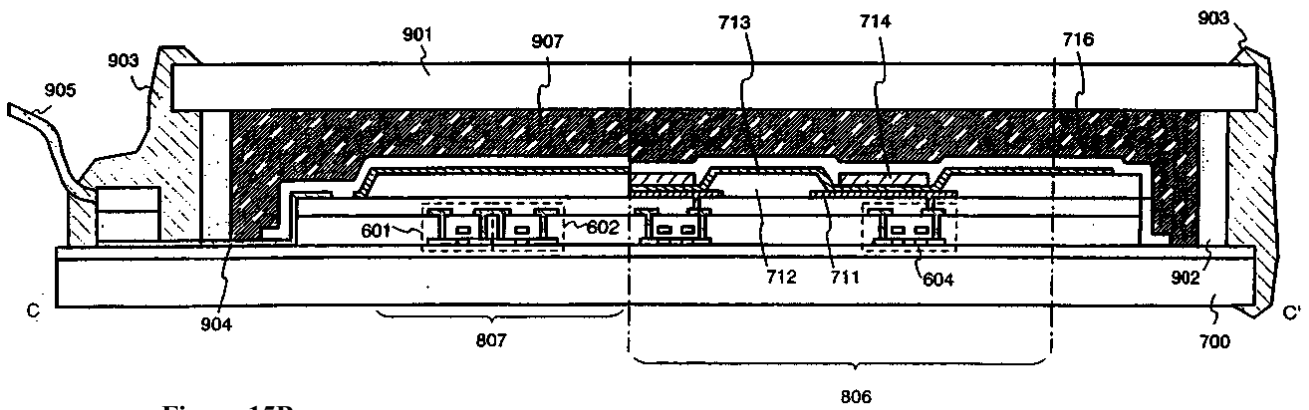


Figure 15B

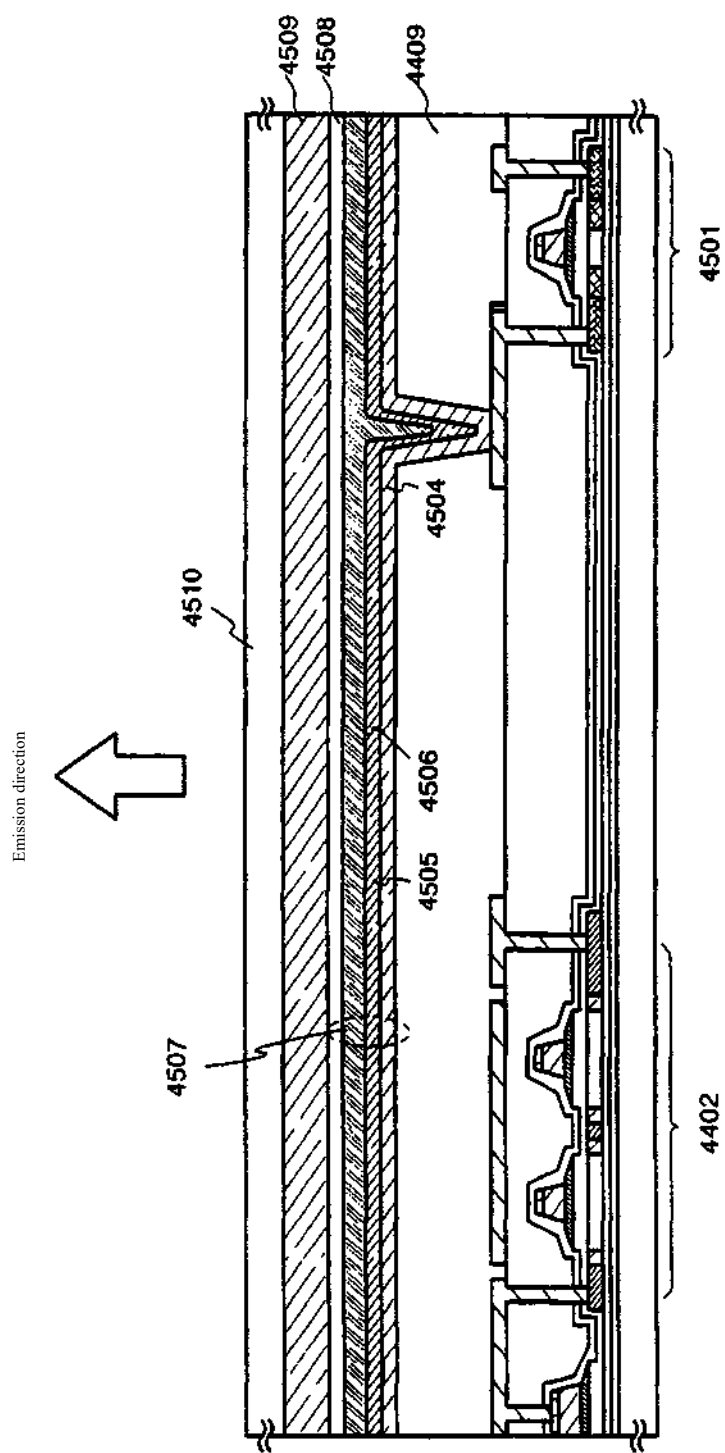


Figure 16

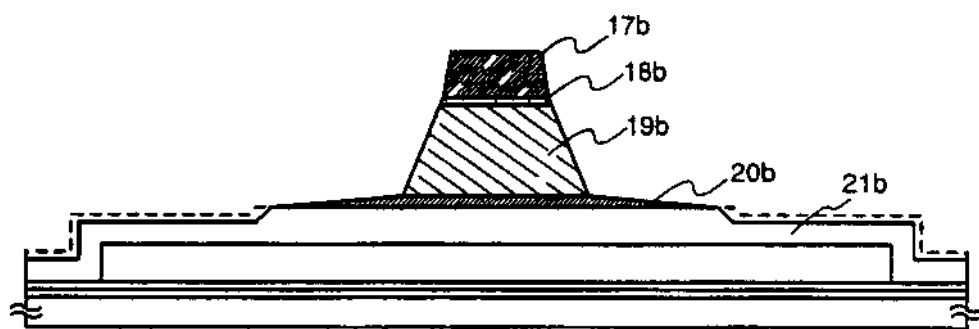


Figure 17A

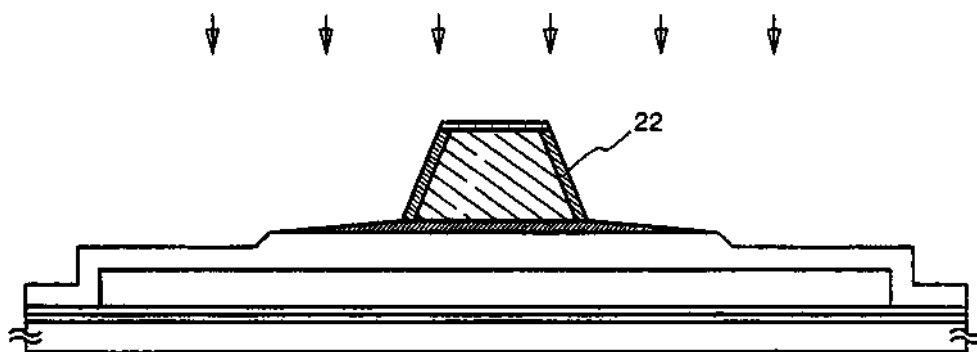


Figure 17B

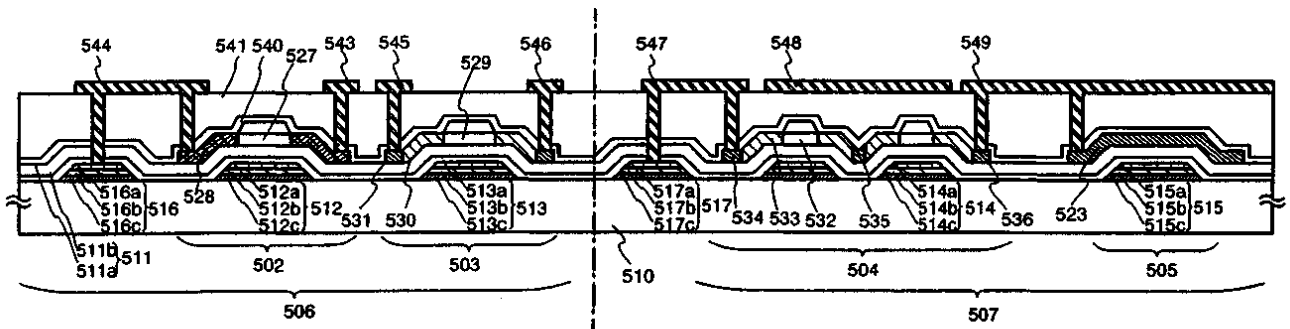


Figure 18A

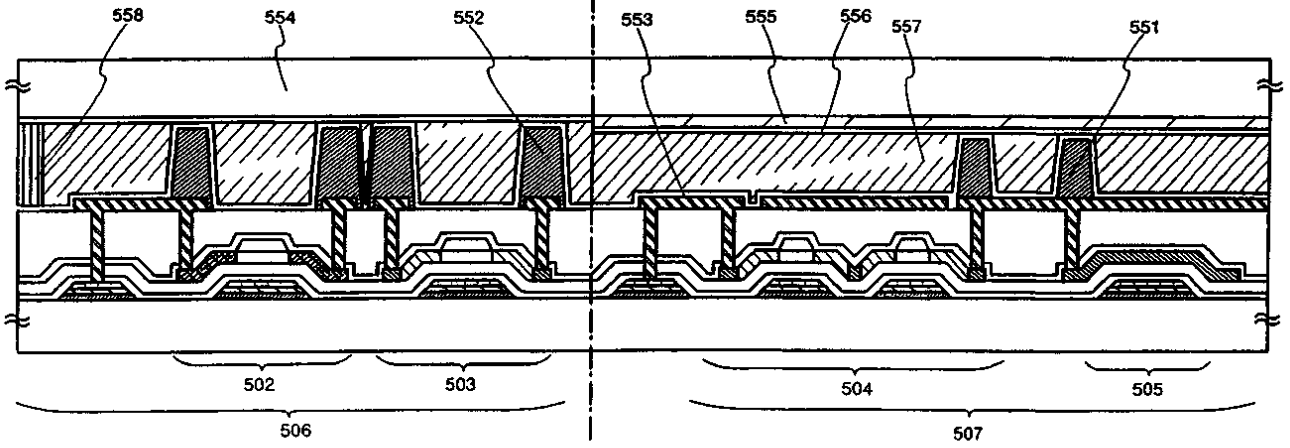


Figure 18B

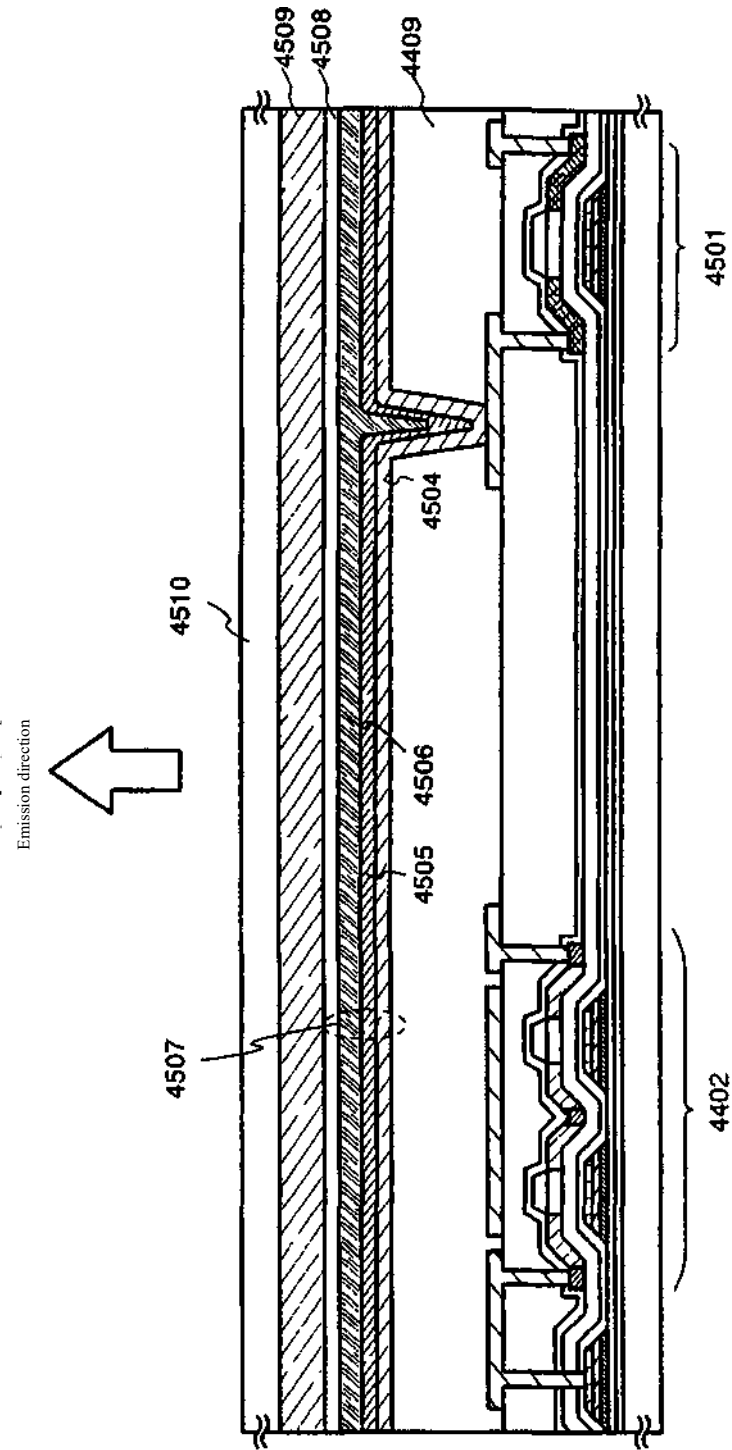


Figure 19

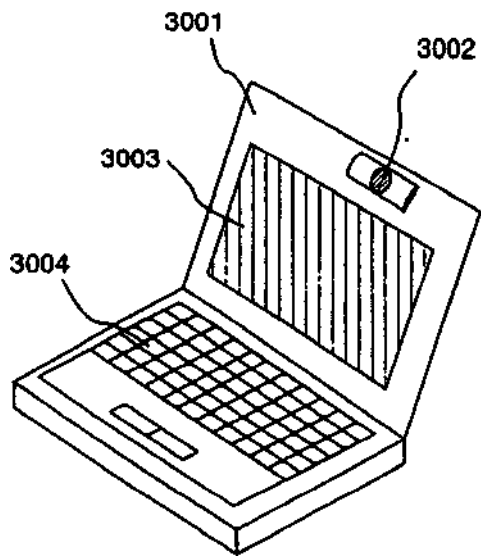


Figure 20A

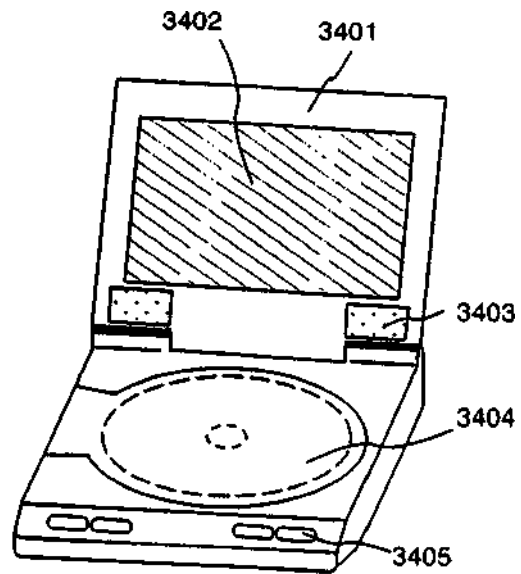


Figure 20B

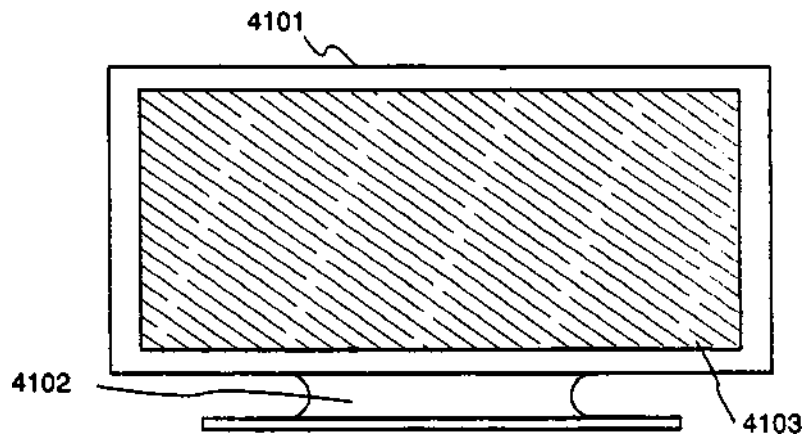


Figure 20C

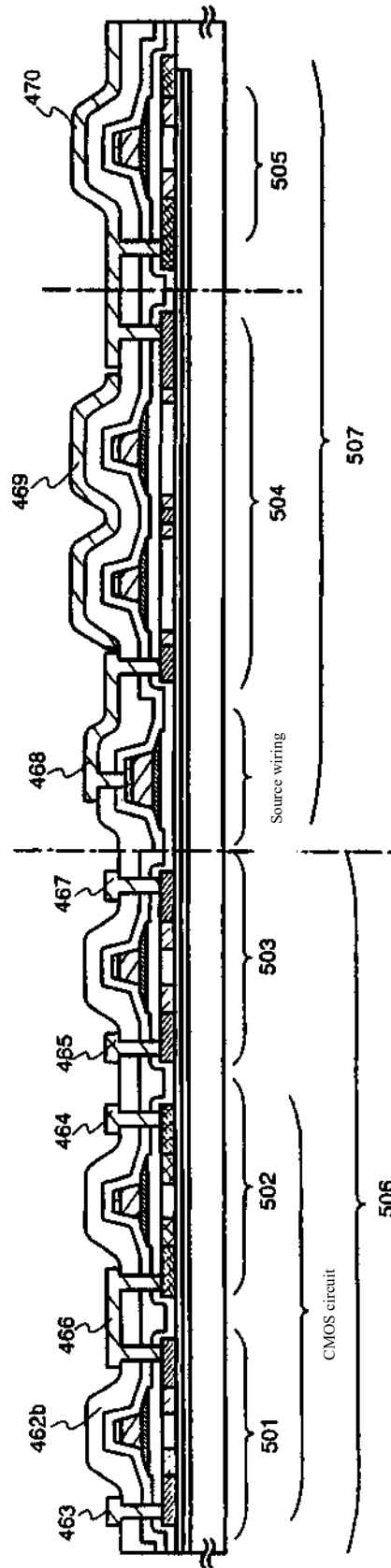


Figure 21

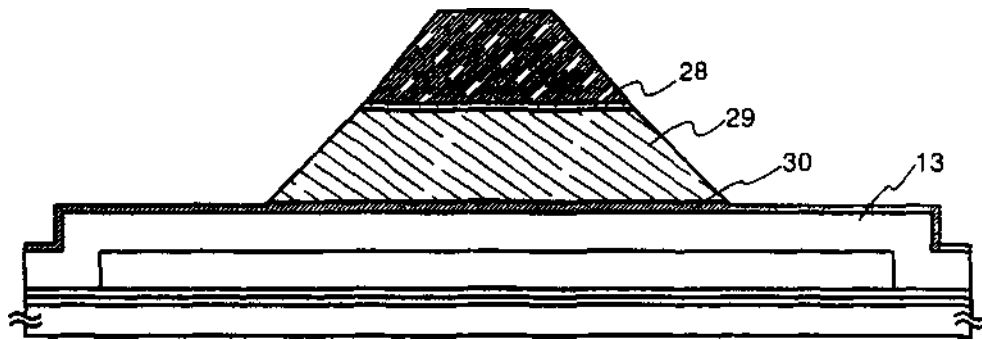


Figure 22

[19]中华人民共和国国家知识产权局

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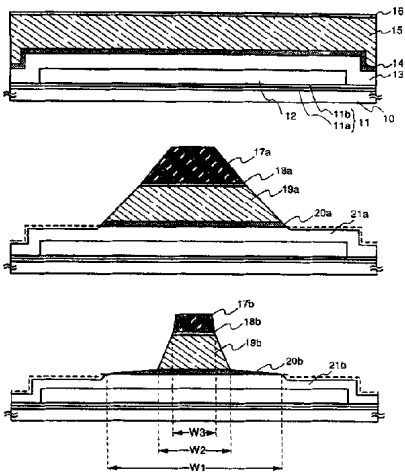
代理人 吴立明 梁 永

权利要求书 8 页 说明书 37 页 附图 22 页

[54] 发明名称 布线和制造布线的方法以及布线板和制造布线板的方法

[57] 摘要

本发明的布线具有层叠结构,它包括具有第一宽度的第一导电层(第一层),由选自 W 和 Mo,或主要含该元素的合金或化合物的一种或多种元素制成;低阻的第二导电层(第二层),其具有小于第一宽度的第二宽度,由主要含 Al 的合金或化合物制成;及第三导电层(第三层),其具有小于第二宽度的第三宽度,由主要含 Ti 的合金或化合物制成。采用这种结构,使本发明为像素段的扩大留有充分的余地。至少第二导电层的边缘具有锥形的截面。由于这种形状,使得能够获得令人满意的覆盖范围。



I S S N 1 0 0 8 - 4 2 7 4

1. 一种具有层叠结构的布线，该布线包括第一宽度第一导电层作为第一层，第二宽度第二导电层作为第二层，而第二宽度小于第一宽度，及第三宽度第三导电层作为第三层，第三宽度又小于第二宽度。

5 其中，第一导电层，第二导电层，或第三导电层的边缘的截面为锥形形状。

2. 根据权利要求1的布线，其中第一导电层至少包括选自W和Mo中的一个。

3. 根据权利要求1的布线，其中第二导电层包括Al。

10 4. 根据权利要求1的布线，其中第三导电层包括Ti。

5. 根据权利要求1的布线，其中第二导电层为第一导电层，第三导电层，及绝缘膜所覆盖，接触绝缘膜的区域被氧化。

6. 根据权利要求1的布线，其中布线被用于至少选自液晶显示器件和发光器件中的一个。

15 7. 一种制造布线的方法，该方法包括步骤：

形成第一形状导电层，其包括绝缘表面上第一导电层，第二导电层，及第三导电层组成的叠层；

蚀刻第一导电层，第二导电层，及第三导电层以形成第二形状导电层，其包括第一宽度第一导电层，第二宽度第二导电层，及第三宽度第三导电层组成的叠层；及

20 蚀刻第二宽度第二导电层和第三宽度第三导电层以形成第三形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层，

25 其中第一导电层，第二导电层，或第三导电层的边缘截面为锥形形状。

8. 一种制造布线的方法，该方法包括步骤：

形成第一形状导电层，其包括绝缘表面上第一导电层，第二导电层，及第三导电层组成的叠层；

30 蚀刻第二导电层和第三导电层以形成第二形状导电层，其包括第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；

蚀刻第一导电层以形成第三形状导电层，其包括第三宽度第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；及

蚀刻第一宽度第二导电层和第二宽度第三导电层以形成第四形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层，

5 其中第一导电层，第二导电层，或第三导电层的边缘截面为锥形形状。

9. 一种制造布线的方法，该方法包括步骤：

形成第一形状导电层，其包括绝缘表面上第一导电层，第二导电层，及第三导电层组成的叠层；

10 蚀刻第一导电层，第二导电层和第三导电层以形成第二形状导电层，其包括第一宽度第一导电层，第二宽度第二导电层，及第三宽度第三导电层组成的叠层；

蚀刻第二宽度第二导电层和第三宽度第三导电层以形成第三形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层；以及

15 对第三形状导电层进行等离子体处理，

其中第一导电层，第二导电层，或第三导电层的边缘截面为锥形形状。

10. 一种制造布线的方法，该方法包括步骤：

20 形成第一形状导电层，其包括绝缘表面上第一导电层，第二导电层，及第三导电层组成的叠层；

蚀刻第二导电层和第三导电层以形成第二形状导电层，其包括第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；

蚀刻第一导电层以形成第三形状导电层，其包括第三宽度第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；

25 蚀刻第一宽度第二导电层和第二宽度第三导电层以形成第四形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层；以及

对第四形状导电层进行等离子体处理，

30 其中第一导电层，第二导电层，或第三导电层的边缘截面为锥形形状。

11. 根据权利要求 7 至 10 中任何一项权利要求的制造布线的方法，其中第一导电层至少包括选自 W 和 Mo 中的一个。

12. 根据权利要求 7 至 10 中任何一项权利要求的制造布线的方法，其中第二导电层包括 Al。

13. 根据权利要求 7 至 10 中任何一项权利要求的制造布线的方法，其中第三导电层包括 Ti。

5 14. 根据权利要求 7 至 10 中任何一项权利要求的制造布线的方法，其中使用氧或主要含氧的气体，或 H₂O 进行等离子体处理。

15. 一种布线板，该布线板包括绝缘基板和布线，
其中布线具有层叠结构，其包括第一宽度第一导电层作为第一层，第二宽度第二导电层作为第二层，向第二宽度小于第一宽度，及
10 第三宽度第三导电层作为第三层，第三宽度又小于第二宽度，

其中第一导电层，第二导电层，或第三导电层的边缘的截面为锥形形状。

16. 根据权利要求 15 的布线板，其中第一导电层至少包括选自 W 和 Mo 中的一个。

15 17. 根据权利要求 15 的布线板，其中第二导电层包括 Al。

18. 根据权利要求 15 的布线板，其中第三导电层包括 Ti。

19. 根据权利要求 15 的布线板，其中第二导电层被第一导电层，第三导电层，及绝缘层所覆盖，接触绝缘膜的区域被氧化。

20. 根据权利要求 15 的布线板，其中液晶显示器件或发光器件采用
20 该布线板制造。

21. 一种制造布线板的方法，该方法包括步骤：

形成第一形状导电层，其包括绝缘表面上第一导电层，第二导电层，及第三导电层组成的叠层；

蚀刻第一导电层，第二导电层，及第三导电层以形成第二形状导电层，其包括第一宽度第一导电层，第二宽度第二导电层，及第三宽度第三导电层组成的叠层；以及
25

蚀刻第二宽度第二导电层和第三宽度第三导电层以形成第三形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层，

30 其中第四宽度第一导电层，第五宽度第二导电层，或第六宽度第三导电层的边缘的截面为锥形形状。

22. 一种制造布线板的方法，该方法包括步骤：

形成第一形状导电层，其包括绝缘表面上堆迭的第一导电层，第二导电层及第三导电层；

蚀刻第二导电层和第三导电层以形成第二形状导电层，其包括第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；

5 蚀刻第一导电层以形成第三形状导电层，其包括第三宽度第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；以及

蚀刻第一宽度第二导电层和第二宽度第三导电层以形成第四形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层，

10 其中第四宽度第一导电层，第五宽度第二导电层，或第六宽度第三导电层的边缘的截面为锥形形状。

23. 一种制造布线板的方法，该方法包括步骤：

在绝缘表面上形成第一导电层；
15 在第一导电层上形成第二导电层；
在第二导电层上形成第三导电层；
蚀刻第一至第三导电层以形成具有锥形段的导电层；以及对具有锥形段的导电层进行等离子体处理。

24. 一种制造布线板的方法，该方法包括步骤：

20 形成第一形状导电层，其包括绝缘表面上第一导电层，第二导电层，及第三导电层组成的叠层；

蚀刻第一导电层，第二导电层和第三导电层以形成第二形状导电层，其包括第一宽度第一导电层，第二宽度第二导电层，及第三宽度第三导电层组成的叠层；

25 蚀刻第二宽度第二导电层和第三宽度第三导电层以形成第三形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层；以及

对第三形状导电层进行等离子体处理，

30 其中第四宽度第一导电层，第五宽度第二导电层，或第六宽度第三导电层的边缘的截面为锥形形状。

25. 一种制造布线板的方法，该方法包括步骤：

形成第一形状导电层其包括绝缘表面上堆迭的第一导电层，第二

导电层, 及第三导电层;

蚀刻第二导电层和第三导电层以形成第二形状导电层, 其包括第一导电层, 第一宽度第二导电层, 及第二宽度第三导电层组成的叠层;

蚀刻第一导电层以形成第三形状导电层, 其包括第三宽度第一导电层, 第一宽度第二导电层, 及第二宽度第三导电层组成的叠层;

蚀刻第一宽度第二导电层和第二宽度第三导电层以形成第四形状导电层, 其包括第四宽度第一导电层, 第五宽度第二导电层, 及第六宽度第三导电层组成的叠层; 以及

对第四形状导电层进行等离子体处理,
其中第四宽度第一导电层, 第五宽度第二导电层, 或第六宽度第三导电层的边缘的截面为锥形形状。

26. 根据权利要求 21 至 25 中任何一项权利要求的制造布线板的方法, 其中第一导电层至少包括选自 W 和 Mo 中的一个。

27. 根据权利要求 21 至 25 中任何一项权利要求的制造布线板的方法, 其中第二导电层包括 Al。

28. 根据权利要求 21 至 25 中任何一项权利要求的制造布线板的方法, 其中第三导电层包括 Ti。

29. 根据权利要求 21 至 25 中任何一项权利要求的制造布线板的方法, 其中使用氧或主要含氧的气体, 或 H₂O 进行等离子体处理。

30. 一种半导体器件, 该半导体器件包括:

基板上的半导体层;

半导体层上的栅绝缘膜;

栅绝缘层上的布线, 该布线具有层叠结构, 其包括第一宽度第一导电层作为第一层, 第二宽度第二导电层作为第二层, 第二宽度小于第一宽度, 及第三宽度第三导电层作为第三层, 第三宽度又小于第二宽度,

其中第一导电层, 第二导电层, 或第三导电层的边缘的截面为锥形形状。

31. 根据权利要求 30 的半导体器件, 其中第一导电层至少包括选自 W 和 Mo 中的一个。

32. 根据权利要求 30 的半导体器件, 其中第二导电层包括 Al。

33. 根据权利要求 30 的半导体器件, 其中第三导电层包括 Ti。

34. 根据权利要求 30 的半导体器件，其中第二导电层被第一导电层，第三导电层，及绝缘膜所覆盖，接触绝缘膜的区域被氧化。

35. 根据权利要求 30 的半导体器件，其中半导体器件至少选自液晶显示器件和发光器件中的一个。

5 36. 根据权利要求 30 的半导体器件，其中半导体器件至少选自个人计算机，使用记录介质的播放机，和显示器中的一个。

37. 一种制造半导体器件的方法，该方法包括步骤：

在基板上形成半导体层；

在半导体层上形成栅绝缘膜；

10 形成第一形状导电层，其包括栅绝缘膜上第一导电层，第二导电层，及第三导电层组成的叠层；

蚀刻第一导电层，第二导电层和第三导电层以形成第二形状导电层，其包括第一宽度第一导电层，第二宽度第二导电层，及第三宽度第三导电层组成的叠层；以及

15 蚀刻第二宽度第二导电层和第三宽度第三导电层以形成第三形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层，

其中第一导电层，第二导电层，或第三导电层的边缘的截面为锥形形状。

20 38. 一种制造半导体器件的方法，该方法包括步骤：

在基板上方形成半导体层；

在半导体层上形成栅绝缘膜；

形成第一形状导电层，其包括栅绝缘膜上第一导电层，第二导电层，及第三导电层组成的叠层；

25 蚀刻第二导电层和第三导电层以形成第二形状导电层，其包括第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；

蚀刻第一导电层以形成第三形状导电层，其包括第三宽度第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；以及

30 蚀刻第一宽度第二导电层和第二宽度第三导电层以形成第四形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层，

其中第一导电层，第二导电层，或第三导电层的边缘的截面为锥形形状。

39. 一种制造半导体器件的方法，该方法包括步骤：

在基板上方形形成半导体层；

5 在半导体层上形成栅绝缘膜；

形成第一形状导电层，其包括栅绝缘膜上第一导电层，第二导电层，及第三导电层组成的叠层；

10 蚀刻第一导电层，第二导电层和第三导电层以形成第二形状导电层，其包括第一宽度第一导电层，第二宽度第二导电层，及第三宽度第三导电层组成的叠层；

蚀刻第二宽度第二导电层和第三宽度第三导电层以形成第三形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层；及

对第三形状导电层进行等离子体处理，

15 其中第一导电层，第二导电层，或第三导电层的边缘的截面为锥形形状。

40. 一种制造半导体器件的方法，该方法包括步骤：

在基板上方形形成半导体层；

在半导体层上形成栅绝缘膜；

20 形成第一形状导电层，其包括栅绝缘膜上第一导电层，第二导电层，及第三导电层组成的叠层；

蚀刻第二导电层和第三导电层以形成第二形状导电层，其包括第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；

25 蚀刻第一导电层以形成第三形状导电层，其包括第三宽度第一导电层，第一宽度第二导电层，及第二宽度第三导电层组成的叠层；

蚀刻第一宽度第二导电层和第二宽度第三导电层以形成第四形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层，以及

对第四形状导电层进行等离子体处理，

30 其中第一导电层，第二导电层，或第三导电层的边缘的截面为锥形形状。

41. 根据权利要求 37 至 40 中任何一项权利要求的制造半导体器

件的方法，其中第一导电层至少包括选自 W 和 Mo 中的一个。

42. 根据权利要求 37 至 40 中任何一项权利要求的制造半导体器件的方法，其中第二导电层包括 Al。

43. 根据权利要求 37 至 40 中任何一项权利要求的制造半导体器件的方法，其中第三导电层包括 Ti。

44. 根据权利要求 37 至 40 中任何一项权利要求的制造半导体器件的方法，其中使用氧或主要含氧的气体，或 H₂O 进行等离子体处理。

45. 根据权利要求 37 至 40 中任何一项权利要求的制造半导体器件的方法，其中半导体器件至少选自液晶显示器件和发光器件中的一个。

46. 根据权利要求 37 至 40 中任何一项权利要求的制造半导体器件的方法，其中半导体器件至少选自个人计算机，使用记录介质的播放机，及显示器中的一个。

布线和制造布线的方法以及布线板和制造布线板的方法

技术领域

- 5 本发明涉及使用薄膜技术形成的布线及制造布线的方法。本发明还涉及布线板及制造布线板的方法。在本说明书中，布线板是指用玻璃等制造的绝缘基板或具有使用薄膜技术形成的布线的各种基板。

背景技术

- 10 近年来，使用在有绝缘表面的基板上形成的半导体薄膜（厚度约几至几百 nm）来形成薄膜晶体管（TFT）的技术已受到人们的注意。TFT 广泛地应用于电子器件如集成电路（IC）和电光仪器。特别是 TFT 作为图象显示仪的开关元件正在得到迅速地发展。

- 通常，液晶显示器件是作为图象显示仪器为人们所知的。与无源型液晶显示器件相比，由于能得到精度更高的图象，有源矩阵型液晶显示器件正在更多地使用。在有源矩阵型液晶显示器件中，排列在矩阵中的象素电极受到驱动，从而在屏幕上形成显示图形。更具体地说，电压加在选出的象素电极和与此象素电极相对应的反电极之间，由此配置在象素电极和反电极之间的液晶层就受到光学调制，而这种光学调制是由观测者以显示图形而认知的。

- 20 这种有源矩阵型液晶显示器件得到了比较广泛的应用，而且对高精度、高孔径比，高稳定性，以及屏幕尺寸的扩大存在日益增长的需要。对提高生产力和降低成本也有要求。

- 在使用铝（Al）作为上述 TFT 的布线来制造 TFT 的情况下，由于热处理而形成凸出物如凸起和须状物，Al 原子会扩散到绝缘膜和有源区（特别是沟道形成区），这就会造成 TFT 工作故障或 TFT 电气特性下降。

在这种情况下，考虑使用耐热处理的金属材料（有代表性的是，具有高熔点的金属元素，诸如钨（W）和钼（Mo））。然而这些元素的电阻与 Al 的电阻相比却非常高（见表 1）。

表 1

布线材料	电阻率 ($\mu\Omega\text{cm}$)
Al	2
W	10 - 20
Mo	15 - 25

因此，在屏幕尺寸扩大时，线路延迟就成了问题。有鉴于此，考虑通过使布线变得较厚来降低电阻的方法。但是，在布线宽度增大时，设计自由度和像素段的孔径比都会降低。此外，在布线的薄膜厚度做得更大时，很可能在布线相互三维交叉区段造成短路，并且在布线阶差段其覆盖范围也会下降。

发明内容

因此，考虑到上述情况，本发明的目的是提供便于屏幕扩大的布线和制造此布线的方法，以及提供布线板和布线板的制造方法。

根据本发明，布线为层叠结构，它包括：作为第一层是主要含有选自 W 和 Mo 的一种或多种元素的导电膜，或选自 W 和 Mo 的一种或多种元素；作为第二层，主要含 Al 的低阻导电膜；及作为第三层，主要含 Ti 的导电膜，由此试图降低布线电阻。根据本发明，主要含 Al 的低阻导电膜用其他导电膜夹在当中，由此能够避免因热处理而形成凸出物如凸起和须状物。此外，由于第一和第二层用高熔点的导电膜制成，它们起阻挡金属的作用，这就能防止 Al 原子扩散到绝缘膜和有源区（表 2）。还有，在本发明的布线上形成绝缘膜且与此布线形成接触时，第三层对绝缘膜的蚀刻起挡板的作用，所以接触能够易于形成。当 Al 与 ITO 膜（典型的透明导电膜）接触时，Al 引起电腐蚀使接触电阻增加。但是，第三层由主要含 Ti 的导电膜制成，所以接触电阻变得令人满意。

表 2

布线材料	熔点 [$^{\circ}\text{C}$]
Al	660.4
W	3387
Mo	2610
Ti	1675

此外,根据本发明,至少由主要含 Al 的低阻导电膜制成的第二层的边缘呈锥形。由于这种锥形形状,在阶差段的覆盖范围提高了。在本说明书中,锥形角是指由材料层的水平表面和侧表面所形成的角度。还有,在本说明书中,为方便起见,有锥形角的侧表面称为锥形形状,呈锥形的区段称为锥形段。

在本说明书中公开的本发明的结构涉及到呈层叠结构的布线,它包括具有第一宽度的第一导电层作为第一层,具有小于第一宽度的第二宽度第二导电层作为第二层,以及具有小于第二宽度的第三宽度第三导电层作为第三层,其特征在于第一导电层,第二导电层,或第三导电层的边缘的截面呈锥形形状。

在上述结构中,布线的特点是具有层叠结构,它包括由主要含 W 的合金或化合物制成的导电层(第一层),由主要含 Al 的合金或化合物制成的导电层(第二层),以及由主要含 Ti 的合金或化合物制成的导电层(第三层)。另一种情况是,布线的特点是呈层叠结构,它包括由主要含 Mo 的合金或化合物制成的导电层(第一层),由主要含 Al 的合金或化合物制成的导电层(第二层),以及由主要含 Ti 的合金或化合物制成的导电层(第三层)。例如,作为第一层,能够使用 W, WN, Mo, 或其他类似材料等。作为第二层,能使用 Al, Al-Si (2 wt %), Al-Ti (1 wt %), Al-Nd (1 wt %), Al-Sc (0.18 wt %), 或其他类似材料等。作为第三层能使用 Ti, TiN, 或其他类似材料等。这些层可以通过溅射,等离子体 CVD, 或诸如此类的方法来形成。此外,当在第二层中形成 Al-Si 或类似材料时,对元素如 Si 能溶入 Al 的比率有限制(固溶度限制)。因为溶解度较高时,电阻增加,热阻也发生变化。因此,本领域的技术人员可根据适合于布线的电阻和热阻以及元素例如 Si 的固溶度限制,适当地确定 Si 或类似材料对 Al 的比率。

表 3 示出构成布线的各导电层中电阻的实例。从表 3 了解到由主要含 Al 的合金或化合物制成的导电层与其他导电层相比,具有非常低的电阻。

表 3

布线材料		电阻率 [$\mu\Omega\text{cm}$]
主要含 W 的材料	W	10-20
	WN	150-220
主要含 Al 的材料	Al	2
	Al-Si (2wt%)	3.5-4.5
	Al-Ti (1wt%)	8-10
	Al-Nd (1wt%)	7-10
	Al-Sc (0.18wt%)	3.5-4.0
主要含 Ti 的材料	Ti	50-60
	TiN	130-200

任何蚀刻方法都可以采用，只要具有热阻和电导的第一，第二，及第三导电膜能够以高速度和良好的精度蚀刻，并且薄膜的边缘段能做成锥形就行。这其中，最好使用利用高密度等离子体的干法蚀刻法。

5 使用微波，螺旋波等离子体（HWP），或感应耦合等离子体（ICP）的蚀刻仪适合于获得高密度等离子体。例如，电子回旋共振（ECR）蚀刻仪，表面波等离子体（SWP）蚀刻仪，ICP 蚀刻仪，双频平行板激发型蚀刻仪，或其他类似仪器等都可以使用。尤其是 ICP 蚀刻仪易于控制等离子体，而且便于待处理基板的扩大。

10 例如，为了进行高精度等离子体处理，使用的方法是通过多重螺旋线圈（其中多个螺旋线圈段通过阻抗匹配电路并联连接）施加高频电功率来形成等离子体。此外，高频电功率也加在持有待处理基板的低电极上，从而供给其偏压。

当使用采用这种多重螺旋线圈的 ICP 蚀刻仪时，锥形角可有显著地改变，要视加在基板侧的偏压电功率而定。因此，通过进一步增加偏压电功率并改变压力，能在 $50^\circ - 85^\circ$ 范围改变锥形角。

作为用于蚀刻第二和第三层的气体，最好是氟气。例如，可以使用 SiCl_4 ， HCl ， CCl_4 ， BCl_3 ， Cl_2 ，或其他类似气体等。

20 作为用于蚀刻第一层的气体，最好是氟气。例如可以使用 NF_3 ， CF_4 ， C_2F_6 ， SF_6 ，或其他类似气体等。在氟气与氟气同时采用时，第一层中的蚀刻率提高，这是所希望的。

此外，通过使布线具有包括上述导电层的层叠结构，使用 ICP 蚀

刻法或其他类似方法使布线边缘形成锥形。通过使布线边缘形成锥形，在后面过程中将要形成的薄膜其覆盖范围能够令人满意。

在上述结构中，第一导电层的边缘最好做成锥形。呈锥形形状的区域（即锥形段）是一个与第二导电层不相重叠的区域，该区的宽度与从第一宽度中减掉第二宽度所得到的宽度相当。还有，最好是第二导电层做成锥形，且使其锥形角大于第一导电层锥形段的锥形角。此外，最好第三导电层做成锥形，且使其锥形角基本上与第二导电层锥形段的锥形角相同。

实现本方案的结构涉及到制造布线的方法，其包括的步骤为：形成第一形状导电层，其包括绝缘表面上第一导电层，第二导电层，以及第三导电层组成的叠层；蚀刻第一导电层，第二导电层，以及第三导电层以形成第二形状导电层，其包括第一宽度第一导电层，第二宽度第二导电层，以及第三宽度第三导电层组成的叠层；及蚀刻第二宽度第二导电层和第三宽度第三导电层以形成第三形状导电层，其包括第四宽度第一导电层，第五宽度第二导电层，及第六宽度第三导电层组成的叠层，其中第一导电层，第二导电层，或第三导电层的边缘截面呈锥形。

在上述结构中，布线的特点是具有层叠结构，其包括由主要含 W 的合金或化合物制成的导电层（第一层），由主要含 Al 的合金或化合物制成的导电层（第二层），以及由主要含 Ti 的合金或化合物制成的导电层（第三层）。另一种情况是，布线特点是呈层叠结构，其包括由主要含 Mo 的合金或化合物制成的导电层（第一层），由主要含 Al 的合金或化合物制成的导电层（第二层），以及由主要含 Ti 的合金或化合物制成的导电层（第三层）。

此外，通过使布线能具有包括上述导电层的层叠结构，使用 ICP 蚀刻法或其他类似的方法等使布线边缘形成锥形。通过使布线边缘形成锥形，在后面的过程中将要形成的薄膜其覆盖范围能够令人满意。

在上述结构中，第一导电层的边缘最好做成锥形。呈锥形形状的区域（即锥形段）是一个与第二导电层不相重叠的区域，该区的宽度与从第一宽度中减掉第二宽度所得到的宽度相当。还有最好第二导电层也做成锥形，且使其锥形角大于第一导电层锥形段的锥形角。此外，最好第三导电层做成锥形，且使其锥形角基本上与第二导电层锥形段

的锥形角相同。

本发明的结构涉及到包括绝缘基板和布线的布线板，其特征在于布线为层叠结构，其包括；具有第一宽度的第一导电层作为第一层；具有小于第一宽度的第二宽度第二导电层作为第二层；以及具有小于第二宽度的第三宽度第三导电层作为第三层，并且其特征还在于第一导电层，第二导电层或第三导电层的边缘截面呈锥形形状。

在上述结构中，布线形成方法的特征在于主要含 W 的导电膜，主要含 Al 的导电膜，以及主要含 Ti 的导电膜都叠放在彼此的顶上，再带掩模进行蚀刻。此外，在上述结构中，布线形成过程的特征在于主要含 Mo 的导电膜，主要含 Al 的导电膜，以及主要含 Ti 的导电膜都叠放在彼此的顶上，再用掩膜进行蚀刻。

在上述结构中，第一导电层的边缘最好做成锥形。呈锥形形状的区域（即锥形段）是一个与第二导电层不相重叠的区域，该区的宽度与从第一宽度中减掉第二宽度所得到的宽度相当。还有最好第二导电层也做成锥形，且使其锥形角大于第一导电层锥形段的锥形角。此外，最好第三导电层做成锥形，且使其锥形角基本上与第二导电层锥形段的锥形角相同。

此外，实现本发明的结构涉及到布线板的制造方法，其特点包括上述步骤：在绝缘表面上形成第一导电层；在第一导电层上形成第二导电层；在第二导电层上形成第三导电层，并对第一至第三导电层进行蚀刻以形成有锥形段的导电层。

在上述结构中，布线形成过程的特征在于主要含 W 的导电膜，主要含 Al 的导电膜，以及主要含 Ti 的导电膜都叠放在彼此的顶上，再带掩模进行蚀刻。此外，在上述结构中，布线形成过程的特征在于主要含 Mo 的导电膜，主要含 Al 的导电膜，以及主要含 Ti 的导电膜都叠放在彼此的顶上，再带掩模进行蚀刻。

此外，通过使布线能具有包括上述导电层的层叠结构，使用 ICP 蚀刻法或其他类似方法等使布线边缘形成锥形。通过使布线边缘形成锥形，在后面的过程中将要形成的薄膜，其覆盖范围能够令人满意。

在上述结构中，第一导电层的边缘最好做成锥形。呈锥形形状的区域（即锥形段）是一个与第二导电层不相重叠的区域，该区的宽度与从第一宽度中减掉第二宽度所得到的宽度相当。还有最好第二导电

层也做成锥形，且使其锥形角大于第一导电层锥形段的锥形角。此外，最好第三导电层做成锥形，且使其锥形角基本上与第二导电层锥形段的锥形角相同。

5 根据本发明，凭借适合于常规布线或制造布线板的过程的简单方法，布线中能够实现低电阻。因此，设计自由和象素段孔径比的程度可以提高。由于布线包括具有锥形形状的导电层，故得到了满意的覆盖范围。因为有这些优点，在以有源矩阵型液晶显示器件为代表的半导体器件中，本发明对因象素段面积增加所致的屏幕扩大留充分的余地，这就使半导体器件的工作特性和可靠性得以提高。

10 本发明的这些优点和其他优点对本领域技术人员在参照附图阅读和理解下面的详细说明时会变得明显起来。

附图说明

在附图中：

图 1A - 1C 示出本发明的典型原理；

15 图 2A 和 2B 示出根据本发明生产的布线的典型形状；

图 3A 和 3B 示意性地示出根据本发明生产的布线的形态；

图 4A - 4C 示出根据本发明生产的布线的典型形状；

图 5A - 5C 示出根据本发明生产的布线的典型形状；

图 6A - 6C 示出根据本发明生产的布线的典型形状；

20 图 7A - 7C 示出根据本发明的典型原理；

图 8A - 8C 为截面视图，其说明象素 TFT 和 TFT 驱动电路的制造过程；

图 9A - 9C 为截面视图，其说明象素 TFT 和 TFT 驱动电路的制造过程；

25 图 10 为截面视图，其示出象素 TFT 和 TFT 驱动电路的制造过程；

图 11 为顶视图，其示出象素 TFT 的配置；

图 12 为截面视图，其说明有源矩阵型液晶显示器件的制造过程；

图 13 为截面视图，其说明有源矩阵型液晶显示器件的制造过程；

图 14 为发光器件的驱动电路和象素段的截面结构视图；

30 图 15A 为发光器件的顶视图，图 15B 为该发光器件驱动电路和象素段的截面结构视图；

图 16 为发光器件驱动电路和象素段的截面结构视图；

图 17A 和 17B 示出本发明的典型原理;

图 18A 和 18B 为截面视图, 其说明有源矩阵型液晶显示器件的制造过程;

图 19 为发光器件像素段的截面结构视图;

5 图 20A 至 20C 示出半导体器件实例;

图 21 为截面视图, 其说明像素 TFT 和 TFT 驱动电路的制造过程;
及

图 22 示意性地示出根据第一蚀刻工况生产的布线的形状。

具体实施方案

10 下面, 将通过例证性实施方案参照图 1A - 1C 对本发明予以说明。
在本实施方案中, 将对采用本发明的装有 TFT, 栅极的布线板予以说明。

首先, 在基板 10 上形成底绝缘膜 11。作为基板 10, 可以使用玻璃基板, 石英基板, 硅基板, 塑料基板, 金属基板, 挠性基板, 或其他类似基板等。玻璃基板的实例包括用玻璃如钡硼硅玻璃或铝硼硅玻璃制成的玻璃基板。此外, 挠性基板是指用 PET, PES, PEN, 丙烯酸树脂, 或诸如此类材料所制成的薄膜形状基板。如果半导体器件使用
15 挠性基板制造, 可以料到其重量会轻。在挠性基板的正面或其正面和背面最好形成单层或多层的屏障层如 Al 膜 (AlON, AlN, AlO, 等等),
20 碳膜 (类金刚石碳 (DLC), 等等), 或 SiN 膜以提高寿命。

此外, 作为底绝缘膜 11, 形成了由绝缘膜如氧化硅膜, 氮化硅膜, 或氮氧化硅膜制成的底膜 11。其中, 双层结构 (11a, 11b) 的底膜 11 是作为例子; 但是, 底膜 11 可以是单层膜的绝缘膜或可具有两层或更多层的多层结构。注意也可以不形成底绝缘膜。

25 然后, 在底绝缘膜 11 上形成半导体层 12。通过用已知的方法 (溅射, LPCVD, 等离子体 CVD, 等等) 形成非晶结构半导体膜, 用已知的结晶法 (激光结晶法, 热结晶法, 使用催化剂如镍的热结晶法, 等等) 使该半导体膜结晶, 并使用第一光掩膜使结晶的半导体膜形成图形具有所要求的形状, 就得到了半导体层 12。形成的半导体层 12 厚度在
30 25 - 80 nm (最好是 30 - 60 nm)。对结晶半导体膜的材料没有特别的限制; 但是, 结晶半导体膜最好用硅, 硅锗 (SiGe) 合金, 或其他类似材料等形成。

然后，形成绝缘膜 13 以覆盖半导体 12。形成的绝缘膜 13 厚度在 40-150 nm 以便通过等离子体 CVD 或溅射使含硅绝缘膜具有单层结构或多层结构。绝缘膜 13 将成为栅绝缘膜。

其次，第一导电膜 14（厚度：20-100 nm），第二导电膜 15（厚度：100-800 nm），及第三导电膜 16（厚度：20-100 nm）被层叠在绝缘膜 13 上。这里，这些导电膜可以利用溅射，等离子体 CVD 或其他类似方法形成，而由于第一导电膜 14 与绝缘膜 13 接触，可以使用主要含 W 或 Mo 的导电膜（W，WMo，Mo 等）以防止杂质从基板 10 扩散到沟道形成区。此外，作为第二导电膜 15，可以使用主要含 Al 的低阻导电膜（Al，Al-Ti，Al-Sc，Al-Si，等）。作为第三导电膜 16，可以使用主要含 Ti（Ti，TiN，等）接触电阻低的导电膜。

然后，使用第二光掩模形成抗蚀掩模 17a，而第一蚀刻过程在感应耦合等离子体（ICP）蚀刻仪或其他类似仪器中进行。由于第一蚀刻过程，第一至第三导电膜 14-16 被蚀刻，得到如图 1B 所示的边缘处有锥形段的导电层 18a-20a。

第二蚀刻过程在 ICP 蚀刻仪或其他类似仪器中进行，使用如原来在第二光刻法中形成的抗蚀掩模 17a。由于第二蚀刻过程，第二导电层 19a 和第三导电层 18a 被选择性地蚀刻得到如图 1C 所示的第二导电层 19b 和第三导电层 18b。在第二蚀刻过程中，抗蚀掩膜 17a，第一导电层 20a，及绝缘膜 13 进行轻微蚀刻以形成抗蚀掩膜 17b，第一导电层 20b，及绝缘膜 21b。第一导电层 20b 具有第一宽度（W1），第二导电层 19b 具有第二宽度（W2），及第三导电层 18b 具有第三宽度（W3）。第一宽度大于第二宽度，而第二宽度大于第三宽度。

这里，为了抑制绝缘膜 13 的膜还原，蚀刻进行两次（第一和第二蚀刻过程）。然而，只要能够形成如图 1C 所示的电极结构（第三导电层 18b，第二导电层 19b，及第一导电层 20b 的层叠结构），就不存在特别的限制。蚀刻可以进行一次。

如上所述，根据本发明，由低阻导电层形成栅线。因此，即使像素段面积扩大，其也足以被驱动。不用说，本发明适用于各种布线以及栅线，并且能够制造其上形成有此类布线的布线板。此外，根据本发明，其上形成有此类布线的半导体器件，其工作特性和可靠性也能够提高。

具有上述结构的本发明将通过下述实施方案予以详细说明。

本发明将通过实施方案进行说明，但是，应当指出本发明并不局限于此。

5 [实施方案 1]

下面将说明使用本发明装有栅电极的布线板的典型结构。

首先，在基板 10 上形成底绝缘膜 11。作为基板 10，可以使用玻璃基板，石英基板，硅基板，或金属基板，或其上形成有绝缘膜的挠性基板。此外，可以使用具有耐受处理温度热阻的塑料基板。在本实施方案中，使用玻璃基板（Corning 公司生产的 1737）。

作为底绝缘膜 11，形成了由绝缘膜如氧化硅膜，氮化硅膜，或氮氧化硅膜制成的底膜 11。这里，双层结构（11a，11b）的底膜 11 是作为例子，但是，底膜 11 可以是单层膜的绝缘膜或可以有两层或更多层的多层结构。注意也可以不形成底绝缘膜。在本实施方案中，形成的是厚度为 50 nm 的氮氧化硅膜 11a（组成比：Si=32%，O=27%，N=24%，H=17%）。其次，形成的是厚度为 100 nm 的氮氧化硅膜 11b（组成比：Si=32%，O=59%，N=7%，H=2%）。

然后，在底绝缘膜 11 上形成半导体层 12。通过用已知的方法（溅射，LPCVD，等离子体 CVD，等）形成非晶结构的半导体膜，用已知的结晶法（激光结晶法，热结晶法，使用催化剂如镍的热结晶法，等）使该半导体膜结晶，并使用第一光掩模使结晶的半导体膜形成图形具有所要求的形状，就得到了半导体层 12。形成的半导体 12 厚度在 25 - 80 nm（最好是 30 - 60 nm）。对结晶半导体膜的材料没有特别的限制；但是，结晶半导体膜最好用硅，硅锗（SiGe）合金，或其他类似材料等形成。在本实施方案中，通过等离子体 CVD 形成的非晶硅膜其厚度为 55 nm，而含镍的溶液则放在非晶硅薄膜上。非晶硅膜在 500℃下脱氢 1 小时。并在 550℃下热结晶 4 小时。为改善结晶情况而实施激光退火法来形成结晶硅膜。结晶硅膜用光刻法成形来形成半导体层 12。

然后，形成绝缘膜 13 以覆盖半导体层 12。通过等离子体 CVD 或溅射形成的绝缘膜 13 厚度在 40 - 150 nm 以便使含硅绝缘膜具有单层或多层结构。绝缘膜 13 将成为栅绝缘膜。在本实施方案中，通过等离子

体 CVD 形成的氮氧化硅膜（组成比：Si=32%，O=59%，N=7%，H=2%）厚度为 110 nm。

其次，第一导电膜 14（厚度：20 到 100 nm），第二导电膜 15（厚度：100 到 800 nm），及第三导电膜 16（厚度：20 到 100 nm）被层叠在绝缘膜 13 上。这里，这些导电膜 3 用溅射等方法形成，而由于第一导电膜 14 与绝缘膜 13 接触，可以使用主要含 W 或 Mo 的导电膜（W，WMo，Mo，等）以防止杂质从基板 10 扩散到沟道形成区。此外，作为第二导电膜 15，可以使用主要含 Al 的低阻导电膜（Al，Al-Ti，Al-Sc，Al-Si 等）作为第三导电膜 16，可以使用主要含 Ti（Ti，TiN，等）接触电阻低的导电膜。在本实施方案中，由 W 膜（厚度：30 nm）制的第一导电膜 14，由 Al-Ti 膜（厚度：500 nm）制的第二导电膜 15，及由 Ti 膜（厚度：50 nm）制的第三导电膜 16 通过溅射进行叠层。第二导电膜 15 的 Ti 比为 1%，并且使用 Al-Ti 作为靶子来形成第二导电膜 15。

然后，进行第一蚀刻过程。第一蚀刻过程在第一蚀刻工况和第二蚀刻工况下进行。在本实施方案中，在第一蚀刻工况下使用 ICP 蚀刻法。更具体地说，是使用 BCl_3 ， Cl_2 ，和 O_2 作为蚀刻气体，气体流量比率为 65:10:5（sccm），而 450W 的 RF（13.56 MHz）功率在 1.2Pa 的压力下，供给到线圈形电极上。通过产生等离子体进行 147 秒钟的蚀刻。这里，使用干法蚀刻仪（型号为 E645-ICP），其使用 Matsubshita 电气工业有限公司生产的 ICP。300W 的 RF（13.56 MHz）功率也供给到基板侧（样品台），因此对其施加的基本上是负的自偏压。在第一蚀刻工况下，对抗蚀掩模的蚀刻速度是 235.5 nm/min，对 Al-Ti 的蚀放慢速度是 233.4 nm/min，对 W 的蚀刻速度是 133.8 nm/min。对 Ti 的蚀刻速度几乎与对 Al-Ti 的蚀刻速度相同。如图 22 所示，Al-Ti 膜和 Ti 膜按第一蚀刻工况进行蚀刻以得到第二导电膜 29 和第三导电膜 28。在第一蚀刻工况下，对 Al-Ti 膜和 Ti 膜蚀刻使第二和第三导电层的边缘成锥形。此外，在第一蚀刻工况下，Al-Ti 膜和 Ti 膜的锥形角约变成 45° 。因为对 W 的蚀刻速度对抗蚀掩模，Ti，及 Al-Ti 的蚀刻速度要小得多，故主要对第一导电膜 14 的表面进行蚀刻以形成用参考数字 30 所指示的形状。

其后，蚀刻工况改变成第二蚀刻工况而不去掉抗蚀掩模 17a。在第

二蚀刻工况下,使用 CF_4 , Cl_2 , 和 O_2 作为蚀刻气体,气体流量比率为 25: 25: 10 (sccm), 500W 的 RF (13.56 MHz) 功率在 1Pa 的压力下供给到线圈形电极上,通过产生等离子体进行 30 秒钟的蚀刻。20W 的 RF (13.56 MHz) 功率也供给到基板侧(样品台),由此对其施加的基本上是负的自偏压。在第二蚀刻工况下, CF_4 , Cl_2 , 和 O_2 混合,只对 W 膜蚀刻。在第二蚀刻工况下对 W 的蚀刻速度是 124.6 nm/min。为了进行蚀刻而不在栅绝缘膜上留下残留物,蚀刻时间可以增加约 10-20%。

在第一蚀刻过程中,通过把抗蚀掩模形状做得适当,由于加在基板侧偏压的作用,第一和第二导电层的边缘就形成锥状。锥形角可以设定在 15° - 45° 。从而,通过第一蚀刻过程就形成了包括第一导电层 20a, 第二导电层 19a, 及第三导电层 18a 的第一形状导电层。第一导电层 20a 在沟道长度方向的宽度与在上述实施方案模式中示出的 W1 相当。参考数字 21a 代表栅绝缘膜,而栅绝缘膜 21a 未被第一形状导电层覆盖的区域要轻微蚀刻约 20-50 nm。此处的第一蚀刻过程与上述实施方案模式中说明的第一蚀刻过程(图 1B)相当。图 2A 示出当时形成的第一形状导电层的扫描电子显微镜照片。

然后,进行第二蚀刻过程而不去掉抗蚀掩模。这里,使用 BCl_3 和 Cl_2 作为蚀刻气体。气体流量比率为 20: 60(sccm), 600W 的 RF(13.56 MHz) 功率在 1.2Pa 的压力下供给到线圈形电极上,通过产生等离子体进行蚀刻。100W 的 RF (13.56 MHz) 功率也供给到基板侧(样品台),由此对其施加的基本上是负自偏压。在第二蚀刻过程中,对 Al-Ti 膜和 Ti 膜进行选择性的蚀刻。由于第二蚀刻过程,Al-Ti 膜和 Ti 膜的锥形角变成为 80° 。在第二蚀刻过程中,形成了第二导电层 19b 和第三导电层 18b。另一方面,第一导电层 20a 与第二导电层 19b 和第三导电层 18b 相比几乎不能蚀刻来形成第一导电层 20b。这里的第二蚀刻过程与上述实施方案模式中说明的第二蚀刻过程(图 1C)相当。因此,形成了第二形状导电层,它由在沟道长度方向上宽度为 W1 的第一导电层,在沟道长度方向上宽度为 W2 的第二导电层,以及在沟道长度方向上宽度为 W3 的第三导电层组成。图 2B 示出第二形状导电层的扫描电子显微镜照片。

表 4 示出,在 Al-Ti 膜下形成的膜对 Al-Ti 膜的蚀刻率为 2-10 的情况下,考虑到 Al-Ti 膜蚀刻率的面内变化,通过计算待蚀刻底层膜

的厚度 (nm) 而得到的结果。当时是假定 Al-Ti 膜厚度为 500 nm, 面内存在 $\pm 5\%$ 的变化而计算的厚度。

表 4

对Al-Ti膜蚀刻率的变化 ($\pm\%$)	对底层膜的选择比								
	2	3	4	5	6	7	8	9	10
1	300.0	200.0	150.0	120.0	100.0	85.7	75.0	66.7	60.0
2	350.1	233.4	175.1	140.1	116.7	100.0	87.5	77.8	70.0
3	400.4	266.9	200.2	160.1	133.5	114.4	100.1	89.0	80.1
4	450.7	300.5	225.4	180.3	150.2	128.8	112.7	100.2	90.1
5	501.3	334.2	250.6	200.5	167.1	143.2	125.3	111.4	100.3
6	552.0	368.0	276.0	220.8	184.0	157.7	138.0	122.7	110.4
7	603.0	402.0	301.5	241.2	201.0	172.3	150.7	134.0	120.6
8	654.2	436.1	327.1	261.7	218.1	186.9	163.5	145.4	130.8
9	705.7	470.5	352.9	282.3	235.2	201.6	176.4	156.8	141.1
10	757.6	505.1	378.8	303.0	252.5	216.5	189.4	168.4	151.5
11	809.8	539.9	404.9	323.9	269.9	231.4	202.4	180.0	162.0
12	862.4	574.9	431.2	345.0	287.5	246.4	215.6	191.6	172.5
13	915.5	610.3	457.7	366.2	305.2	261.6	228.9	203.4	183.1
14	969.0	646.0	484.5	387.6	323.0	276.9	242.2	215.3	193.8
15	1023.0	682.0	511.5	409.2	341.0	292.3	255.8	227.3	204.6

如表 4 所示, 随着对 Al-Ti 膜蚀刻率变化的增加, 要蚀刻的厚度变大。此外, 随着对底层膜选择比的增加, 待蚀刻厚度变薄。如果这些特性得到利用, 就能形成所需形状的布线。

如上所述, 根据本发明, 由于栅线由低阻导电层形成, 所以即使象素段的面积扩大, 象素段也足以能被驱动。此外, 其上形成有此种布线的半导体器件之工作特性和可靠性也能提高。

[实施方案 2]

在本实施方案中, 将参照图 3A-3B 到图 6A-6C 对实施方案 1 中第一蚀刻过程第一蚀刻工况改变的情况予以说明。这里, 第一蚀刻工况改变了, 实施方案 1 中只有两层 (第一和第三导电层) 构成了栅线。但是, 本发明也适用于栅线由三层组成的情况, 其使用实施方案 1 中的第一导电层作为底层。

首先, 通过溅射在 1737 玻璃基板 10 上形成氮氧化膜 33 使其厚度为 200 nm。然后, 由 Al-Ti 膜 (厚度: 500 nm) 制的第一导电膜 34

和由 Ti 膜 (厚度: 100 nm) 制的第二导电膜 35 通过溅射进行层叠 (图 3A)。

然后, 蚀刻过程在第二导电层 35 上形成抗蚀膜后进行。该蚀刻过程在第一实施方案中的第一蚀刻工况下进行。在本实施方案中, 使用 ICP 蚀刻法, 用 BCl_3 和 Cl_2 作蚀刻气体, 压力在 1.2 Pa。通过改变如表 5 所示的气体流量率和供给到线圈形电极和基板侧 (样品台) 的电功率进行蚀刻 (图 3B)。由于这一蚀刻过程, 抗蚀膜, 第二导电膜 35, 及第一导电膜被蚀刻, 形成了第二导电层 37, 第一导电层 38, 还有氮氧化物膜 40。参考数字 36 代表蚀刻过程后的抗蚀膜。

表 5

工况	ICP (W)	偏压 (W)	气体	流量率 (sccm)	蚀刻时间 (sec.)
1	100	300	$\text{BCl}_3 : \text{Cl}_2$	60 : 20	268
2	300	300	$\text{BCl}_3 : \text{Cl}_2$	60 : 20	168
3	700	300	$\text{BCl}_3 : \text{Cl}_2$	60 : 20	159
4	500	100	$\text{BCl}_3 : \text{Cl}_2$	60 : 20	175
5	500	200	$\text{BCl}_3 : \text{Cl}_2$	60 : 20	147
6	500	400	$\text{BCl}_3 : \text{Cl}_2$	60 : 20	147
7	500	300	$\text{BCl}_3 : \text{Cl}_2$	20 : 60	60
8	500	300	$\text{BCl}_3 : \text{Cl}_2$	40 : 40	81
9	500	300	$\text{BCl}_3 : \text{Cl}_2$	70 : 10	350

图 4A-4C 至 6A-6C 示出用扫描电子显微镜, 放大倍数为 15000 倍时观测到的表 5 所示工况下得到的导电层图形。图 4A 示出在工况 1 下形成的导电层。图 4B 示出工况 2 下形成的导电层。图 4C 示出工况 3 下形成的导电层。图 5A 示出工况 4 下形成的导电层。图 5B 示出工况 5 下形成的导电层。图 5C 示出工况 6 下形成的导电层。图 6A 示出工况 7 下形成的导电层。图 6B 示出工况 8 下形成的导电层。图 6C 示出工况 9 下形成的导电层。从图 4A-4C 了解到随着加在线圈形电极上电功率的增加, 锥形角变大。从图 5A-5C 了解到随着加在基板侧上电功率的增加, 锥形角变大。从图 6A-6C 了解到随着 BCl_3 气体流量率的增加, 锥形角变大。因而, 锥形角的改变视工况而定。此外, 表 6 示出了在表 5 所示工况下得到的蚀刻率。表 7 示出了对各种膜的选择比。在 Al-Ti 与 W 间选择比大的工况下, 能进行各向异性蚀刻, 因而可以形成具有

所需形状的导电层。

表 6

工况	ICP	偏压	流量率	Al-Si (nm/min)		抗蚀膜 (nm/min)		W (nm/min)		SiON (nm/min)	
	(W)	(W)	(sccm)	(Ave)	(3 σ)	(Ave)	(3 σ)	(Ave)	(3 σ)	(Ave)	(3 σ)
1	100	300	60 : 20	168.8	39.3	122.4	33.1	37.1	6.4	38.4	8.1
2	300	300	60 : 20	236.9	51.4	197.9	36.7	59.4	16.2	66.4	8.9
3	700	300	60 : 20	262.1	63.2	263.1	33.2	110.7	23.1	107.6	12.0
4	500	100	60 : 20	236.7	40.6	133.7	26.3	41.4	17.0	56.0	8.2
5	500	200	60 : 20	246.8	46.1	199.6	23.7	69.1	22.3	81.8	8.8
6	500	400	60 : 20	251.0	55.2	255.3	24.4	102.6	21.3	104.0	13.4
7	500	300	20 : 60	750.7	111.0	395.2	70.7	127.8	49.9	104.0	17.6
8	500	300	40 : 40	495.6	116.5	351.1	62.2	112.4	39.4	101.0	16.8
9	500	300	70 : 10	142.3	24.2	148.6	17.7	61.0	10.8	99.3	9.7

5 表 7

工况	对 Al-Si 的选择比			对抗蚀膜的选择比			对 W 的选择比			对 SiON 的选择比		
	抗蚀膜	W	SiON	Al-Si	W	SiON	Al-Si	抗蚀膜	SiON	Al-Si	抗蚀膜	W
1	1.38	4.55	4.40	0.73	3.30	3.19	0.22	0.30	0.97	0.23	0.31	1.03
2	1.20	3.99	3.57	0.84	3.33	2.98	0.25	0.30	0.89	0.28	0.34	1.12
3	1.00	2.37	2.44	1.00	2.38	2.45	0.42	0.42	1.03	0.41	0.41	0.97
4	1.77	5.72	4.23	0.56	3.23	2.39	0.17	0.31	0.74	0.24	0.42	1.35
5	1.24	3.57	3.02	0.81	2.89	2.44	0.28	0.35	0.85	0.33	0.41	1.18
6	0.98	2.45	2.41	1.02	2.49	2.46	0.41	0.40	0.99	0.41	0.41	1.01
7	1.90	5.88	7.22	0.53	3.09	3.80	0.17	0.32	1.23	0.14	0.26	0.81
8	1.41	4.41	4.91	0.71	3.12	3.47	0.23	0.32	1.11	0.20	0.29	0.90
9	0.96	2.33	1.43	1.04	2.44	1.50	0.43	0.41	0.61	0.70	0.67	1.63

10 如上所述，通过改变工况，能够得到所需形状的导电层。此外，即使像素段面积扩大，像素也足以能被驱动。其上形成有这种布线的半导体器件之工作特性和可靠性也能够提高。

[实施方案 3]

15 在本实施方案中，对实施方案 1 中形成的布线进行等离子体处理的情况将参照图 17A 和 17B 予以说明。在本说明书中，等离子体处理是指将样品暴露在等离子体处理气体环境中。

首先，根据实施方案 1，得到图 1C 所示的状态。图 17A 和图 17C 示出同一状态，而且相应的区段用同样的参考数字表示。

如此形成的布线要经受使用氧，主要含氧的气体，或 H_2O 的等离子体处理（图 17B）。使用等离子体发生仪（等离子体 CVD 仪，干法蚀刻仪，溅射仪，等）进行 30 秒-20 分钟的等离子体处理（最好 3-15 分钟）。此外，最好是布线在气流量在 50-300 sccm，基板温度在室温至 200℃，RF 功率在 100-2000W 的工况下处理。由于等离子体处理，在构成三层结构的导电层当中由 Al，或主要含 Al 的合金或化合物制成的导电层所组成的第二导电层 19b 可能被氧化。因此，与其他导电层不接触的导电层 19b 的区段 22 被氧化。这就使凸出物的形成如凸起和须状物能进一步减小。

不用说，如果使用氧气或主要含氧的气体，或 H_2O 进行灰化以去除抗蚀膜 17b，那么第二导电层 19b 的暴露段就被氧化了。但是，在去除抗蚀膜 17b 后进行等离子体处理时将更可能形成足够的氧化膜。

如上所述，根据本发明，栅线是由低阻电导层形成的。因此，即使像素段面积扩大，像素也足以能被驱动。此外，其上形成有这种布线的半导体器件，其工作特性和可靠性能够提高。

[实施方案 4]

对本发明应用在与实施方案 1 至 3 中布线结构不同的布线结构上而制造的布线板实例，将参照图 7 予以说明。

首先，作为基板 10，可以使用玻璃基板，石英基板，硅基板，金属基板，或其上形成有绝缘膜的挠性基板。此外，可以使用具有耐受处理温度热阻的塑料基板。在本实施方案中，使用玻璃基板（Corning 公司生产的 1737）。

然后，第一导电膜 44（厚度：20-100 nm），第二导电膜 45（厚度：100-800 nm），及第三导电膜 46（厚度：20-100 nm）被层叠基板 10 上。这里，这些导电膜可通过溅射来形成，而由于第一导电膜 44 与绝缘膜接触，故可以使用主要含 W 或 Mo 的导电膜以使防止杂质从基板 10 扩散到沟道形成区。此外，作为第二导电膜 45，可以使用主要含 Al 或 Cu 的低阻导电膜。作为第三导电膜 46，可以使用主要含 Ti 接触电阻低的导电膜。在本实施方案中，这些导电膜可以通过溅射形成，由 Mo 膜（厚度：30 nm）制的第一导电膜 44，由 Al-Ti 膜（厚度：500 nm）制的第二导电膜 45，及由 Ti 膜（厚度：50 nm）制的第三导电膜

46 进行层叠。

然后，进行蚀刻过程。蚀刻过程在第一蚀刻工况和第二蚀刻工况下进行。在本实施方案中，在第一蚀刻工况下，使用 ICP 蚀刻法。更具体地说，使用 BCl_3 ， Cl_2 和 O_2 作为蚀刻气体，气体流量比率为 65: 10: 5 (sccm)，450W 的 RF (13.56 MHz) 功率在 1.2Pa 的压力下供给到线圈形电极上，通过产生等离子体进行蚀刻。这里，使用利用 Matsubshita 电气工业有限公司生产的 ICP 的干法蚀刻仪(型号 E645-□ICP)。300W 的 RF (13.56 MHz) 功率也供给到基板侧(样品台)，因此加在其上的基本上是负自偏压。在第一蚀刻工况下，对 Al-Ti 膜和 Ti 膜进行蚀刻使第一导电层的边缘成锥形。此外，在第一蚀刻工况下，尽管 Al-Ti 膜和 Ti 膜的锥形角成为约 45° ，但 Mo 未被蚀刻。

其后，蚀刻工况改变成第二蚀刻工况而不去掉抗蚀掩模 47。在第二蚀刻工况下，使用 CF_4 ， Cl_2 ，及 O_2 作为蚀刻气体/气体流量比率为 25: 25: 10 (sccm)，500W 的 RF (13.56 MHz) 功率在 1.2Pa 的压力下供给到线圈形电极上，通过产生等离子体进行蚀刻。20W 的 RF (13.56 MHz) 功率也供给到基板侧(样品台)，因而，对其施加的基本上是负自偏压。在第二蚀刻工况下 CF_4 ， Cl_2 ，和 O_2 混合，只对 Mo 膜蚀刻。为了进行蚀刻而又不在于栅绝缘膜上留下残留物，蚀刻时间可以增加约 10-20%。

在上述蚀刻过程中，通过把抗蚀掩模形状做得适当，由于加在基板侧偏压的作用，第一和第二导电层的边缘就形成锥形。锥形角可以定在 15° - 45° 。从而，通过蚀刻过程就形成了由第一导电层 50，第二导电层 49，和第三导电层 48 组成的导电层。

然后，形成绝缘膜 51 以覆盖该导电层。通过等离子体 CVD 或溅射形成绝缘膜 51，其厚度为 40-150 nm 以便得到单层结构或多层结构的含硅绝缘膜。在本实施方案中，利用等离子体 CVD 形成氮氧化硅膜(组成比: Si=32%，O=59%，N=7%，H=2%)，厚度为 110 nm。

然后，在绝缘膜 51 上形成半导体层 52。通过用已知的方法(溅射，LPCVD，等离子体 CVD，等)形成非晶结构的半导体膜，用已知的结晶法(激光结晶法，热结晶法，使用催化剂如镍的热结晶法，等)使该半导体膜结晶，并使用光掩模使结晶的半导体膜形成图形具有所要求的形状，就得到了半导体层 52。形成的半导体层 52 厚度在 25-300 nm

(最好在 30-150 nm)。对结晶半导体膜的材料没有特别的限制；但是，结晶半导体膜最好用硅，硅锗 (SiGe) 合金，或其他类似材料等形成。在本实施方案中，通过等离子体 CVD 形成的非晶硅膜其厚度为 55 nm，且此非晶硅膜要经过激光退火过程以形成结晶硅膜。结晶硅膜通过光刻法成形以形成半导体层 52。

如上所述，根据本发明，栅线由低阻导电层形成。因此，在使用反向交错结构的 TFT 时，即使像素段面积扩大，像素也足以能被驱动。此外，其上形成有这种布线的半导体器件之工作特性和可靠性也能提高。

[实施方案 5]

在本实施方案中，作为利用本发明的典型布线板，对有源矩阵基板的制造方法将参照图 8A-11 予以说明。在本说明书中，对其上同时形成有 CMOS 电路的驱动电路，有像素 TFT 的像素段和存储电容器的基板，为方便起见将称这为有源矩阵基板。

在本实施方案中，使用由玻璃如钡硼硅玻璃（例如 Corning 公司生产的 #7059 玻璃，#1737 玻璃）或铝硼硅玻璃制的基板 400。作为基板 400，可以使用石英基板，硅基板，或其上形成有绝缘膜的金属基板或挠性基板。另一方面，可以使用本实施方案的有耐受处理温度热阻的塑料基板。

然后，由绝缘膜如氧化硅膜，氮化硅膜，或氮氧化硅膜组成的底膜 401 在基板 400 上形成。在本实施方案中，底膜 401 为双层结构；但是，底膜 401 可以为单层结构或者有两层或更多层绝缘膜的多层结构。作为底膜 401 的下层，氮氧化硅膜 401a，使用 SiH_4 ， NH_3 和 N_2O 作为反应气体通过等离子体 CVD 形成，其厚度为 10-200 nm（最好 50-100 nm）。在本实施方案中，形成了厚度为 50 nm（组成比：Si=32%，O=27%，N=24%，H=17%）的氮氧化硅膜 401a。然后，作为底膜 401 的上层，氮氧化硅膜 401b，使用 SiH_4 和 N_2O 作为反应气体通过等离子体 CVD 形成，其厚度为 50-200 nm（最好 100-150 nm）。在本实施方案中，形成了厚度为 100 nm（组成比：Si=32%，O=59%，H=2%）的氮氧化硅膜 401b。

然后，在底膜 401 上形成半导体层 402-406。通过用已知的方法

(溅射, LPCVD, 等离子体 CVD, 等)形成厚度为 25-300 nm(最好 30-200 nm)的半导体膜, 用已知的结晶法(激光结晶法, 热结晶法如使用退火炉的热退火和快速热退火(RTA), 使用金属元素加速结晶的热结晶法, 等等)使半导体膜结晶, 并使结晶半导体膜形成图形为所要求的形状。半导体膜的实例包括非晶半导体膜, 微晶体半导体膜, 及晶体半导体膜, 并且可以使用具有非晶结构的复合半导体膜如非晶硅锗膜。在本实施方案中, 通过等离子体 CVD 形成非晶硅膜, 厚度为 55 nm, 而含镍溶液则留在非晶硅膜上。非晶膜在 500℃下脱氢 1 小时, 并在 550℃经受热结晶 4 小时。晶体硅膜通过光刻法成形以形成半导体层 402-406。

在利用激光结晶法制造晶体半导体膜的情况下, 可以使用持续振荡型或脉冲振荡型固态激光器, 气体激光器, 或金属激光器。固态激光器的实例包括持续振荡型或脉冲振荡型 YAG 激光器, YVO₄ 激光器, YLF 激光器, YA10₃ 激光器, 玻璃激光器, 红宝石激光器, 翠绿宝石激光器, Ti: 蓝宝石激光器, 等等。气体激光器的实例包括持续振荡型或脉冲振荡型激发物激光器, Ar 激光器, Kr 激光器, CO₂ 激光器, 等等。金属激光器的实例包括氦镭激光器, 铜蒸汽激光器, 及金蒸汽激光器。在使用这些激光器的情况下, 激光振荡器发射出的激光束可以通过光学系统浓聚成直线形再辐射到半导体膜上。结晶工况要由本领域的技术人员进行适当地选择。在使用脉冲振荡型激发物激光器的情况下, 脉冲振荡频率设定在 300 Hz, 激光能量密度设在 100-1200 mJ/cm²(典型情况是 200-800 mJ/cm²)。此外, 在使用脉冲振荡型 YAG 激光器的情况下, 使用二次谐波, 脉冲振荡频率设定在 1-300 Hz, 而激光能量密度设定在 300-1200 mJ/cm²(典型情况是 350-1000 mJ/cm²)。被浓聚成宽度为 100-1000 μm(例如, 400 μm)直线形的激光光线辐射到基板整个表面上也是可能的, 直线束的重叠比设定在 50-98%。此外, 在使用持续振荡型激光器情况下的能量密度要求在约 0.01-100 MW/cm²(最好是 0.1-10 MW/cm²)。以约 0.5-2000 cm/s 的速度相对于激光束移动样品台来进行辐照。

但是, 在本实施方案中, 非晶膜是使用金属元素加速结晶法结晶的, 所以金属元素仍留在晶体硅膜中。因此, 在晶体硅膜上形成了厚度为 50-100 nm 的非晶硅膜, 进行热处理(使用退火炉的热退火, RTA

等)将金属元素扩散入非晶膜,热处理后通过蚀刻将非晶膜去除。由此,晶体硅膜中金属元素的含量可以减少或去除。

不用说,使用只进行激光结晶而得到的晶体半导体膜也能够制造 TFT。但是,如果把使用金属元素的热结晶法与激光结晶法结合起来,那么晶体半导体膜的结晶度就提高了。因而 TFT 的电气特性也提高了。而这是所希望的。例如,当 TFT 使用只进行激光结晶而得到的晶体半导体膜制造时,迁移率约为 $300 \text{ cm}^2/\text{Vs}$ 。而另一方面,当 TFT 使用通过采用金属元素的热结晶法和激光结晶法而得到的晶体半导体膜制造时,迁移显著提高(即,约 $500\text{--}600 \text{ cm}^2/\text{Vs}$)。

10 半导体层 402-406 形成后,可以进行微量杂质元素(硼或磷)的掺杂以控制 TFT 的阈值。

然后,形成栅绝缘膜 407 以覆盖半导体层 402-406。栅绝缘膜 407 用含硅的绝缘膜形成以便通过等离子体 CVD 或溅射使厚度为 $40\text{--}150 \text{ nm}$ 。在本实施方案中,通过等离子体 CVD 形成的氮氧化硅膜(组成比: Si=32%, O=59%, N=7%, H=2%)厚度为 110 nm 。应当理解到,栅绝缘膜 407 并不限于氮氧化硅膜,它可以是具有单层结构或多层结构的另外一种含硅绝缘膜。

在使用氧化硅膜的情况下,氧化硅膜可以通过等离子体 CVD 形成。更具体地说,通过将基原硅酸四乙脂(TEOS)与 O_2 混合,将反应压力和基板温度设定在 40Pa 和 $300^\circ\text{C}\text{--}400^\circ\text{C}$,并使放电在高频(13.56 MHz)电密度为 $0.5\text{--}0.8 \text{ W/cm}^2$ 情况下进行,就能形成氧化硅膜。这样制造的氧化硅膜经 $400^\circ\text{C}\text{--}500^\circ\text{C}$ 下的热退火后显示出作为栅绝缘膜的令人满意的电气特性。

然后,第一导电膜 408a(厚度: $20\text{--}100 \text{ nm}$),第二导电膜 408b(厚度: $100\text{--}800 \text{ nm}$),及第三导电膜 408c(厚度: $20\text{--}100 \text{ nm}$)被层叠在栅绝缘膜 407 上。在本实施方案中,对由 WN 膜(厚度: 30 nm)制的第一导电膜 408a,由 Al-Sc 膜(厚度: 370 nm)制的第二导电膜 408b,及由 TiN 膜(厚度: 30 nm)制的第三导电膜 408c 进行层叠。

在本实施方案中,尽管第一导电膜 408a 用 MN 制成,但对其没有特别的限制。作为第一导电膜 408a,可以形成由选自 W 和 Mo 的元素,或主要含该元素的合金或化合物制成的导电层。此外,尽管第二导电膜 408b 用 Al-Si 制成,但对其没有特别的限制。作为第二导电膜

408b, 可以形成由 Al, 或主要含 Al 的合金或化合物制成的导电层。此外, 尽管第三导电膜 408c 用 TiN 制成, 但对其没有特殊的限制。作为第三导电层 408c, 可以形成由 Ti, 或主要含 Ti 的合金或化合物制成的导电层。

5 其次, 抗蚀掩膜 410-415 通过光刻法形成, 从而进行形成电极和布线的的第一蚀刻过程。在第一蚀刻工况和第二蚀刻工况下进行第一蚀刻过程 (图 8B)。在本实施方案中, 在第一蚀刻工况下, 使用 ICP 蚀刻法。更具体地说, 使用 BCl_3 , Cl_2 和 O_2 作为蚀刻气体, 气体流量比率为 65: 10: 5 (sccm) 向 450W 的 RF (13.56 MHz) 功率在 1.2Pa 的压力下供给到线圈形电极上, 通过产生等离子体进行蚀刻。300W 的 RF (13.56 MHz) 功率也供给到基板侧 (样品台), 因而对其施加的基本上是负自偏压。在第一蚀刻工况下, 对 Al-Sc 膜和 TiN 膜进行蚀刻使第二和第三导电层的边缘形成锥形。此外, 在第一蚀刻工况下, Al-Sc 膜和 TiN 膜的锥形角约成为 45° , 而 WN 膜则几乎未被蚀刻。

15 其后, 蚀刻工况改变到第二蚀刻工况而不去掉抗蚀掩模 410-415。在第二蚀刻工况下, 使用 CF_4 , Cl_2 和 O_2 作为蚀刻气体, 气体流量比率为 25: 25: 30 (sccm), 500W 的 RF (13.56 MHz) 功率在 1.2Pa 压力下供给到线圈形电极上, 通过产生等离子体进行蚀刻。20W 的 RF (13.56 MHz) 功率也供给到基板侧 (样品台), 因而, 对其施加的基本上是负自偏压。为了进行蚀刻而又不在于栅绝缘膜上留下残留物, 蚀刻时间可以增加约 10-20%。

在第一蚀刻过程中, 通过把抗蚀掩模形状做得适当, 由于加在基板侧偏压的作用, 第一至第三导电层的边缘就形成锥形。锥形角可以设定在 15° - 45° 。因此, 通过第一蚀刻过程就形成了由第一、第二、及第三导电层 (第一导电层 417a-422a, 第二导电层 417b-422b, 及第三导电层 417c-422c) 组成的第一形状导电层 417-422。

参考数字 416 代表栅绝缘膜。栅绝缘膜 416 未被第一形状导电层 417-422 覆盖的区域被蚀刻掉约 20-50 nm 而变薄。

然后, 进行第二蚀刻过程而不去掉抗蚀掩模 (图 8C)。这里, 使用 BCl_3 和 Cl_2 作为蚀刻气体, 气体流量比率为 20: 60 (sccm), 600W 的 RF (13.56 MHz) 功率在 1.2Pa 压力下供给到线圈形电极上, 通过产生等离子体进行蚀刻。100W 的 RF (13.56 MHz) 功率也供给到基板

侧(样品台),因而对其施加的基本上是负自偏压。在第二蚀刻过程中,对Al-Sc膜和TiN膜进行选择性地蚀刻。由于第二蚀刻过程。形成了第二导电层428b-433b和第三导电层428c-433c。另一方面,第一导电层417a-422a几乎未被蚀刻,因而形成了第二形状导电层
5 428-433。

如上所述,由于第一蚀刻过程和第二蚀刻过程,使用本发明的结构,形成了栅电极428-431,存储电容器的一个电极432,及源线433。

然后,进行第一掺杂过程而不去掉抗蚀掩模,因而能传递n型的杂质元素就加在浓度低的半导体层上。利用离子掺杂或离子注入可以
10 进行该掺杂过程。离子掺杂在剂量为 1×10^{13} - $5\times 10^{14}/\text{cm}^2$,加速电压为40-80keV的工况下进行。在本实施方案中,离子掺杂在剂量为 $1.5\times 10^{13}/\text{cm}^2$ 、加速电压为60keV的工况下进行。作为传递n型的杂质元素,使用属于第15族(典型的是磷(p)或砷(As))的元素。这里,使用的是磷(p)。在这种情况下,导电层428-433对传递n型的
15 杂质元素起掩模的作用,而杂质区423-427则以自调整方式形成。传递n型的杂质元素加在杂质区423-427以便浓度范围在 1×10^{18} - $1\times 10^{20}/\text{cm}^3$ 。

在去掉抗蚀掩模后,又新形成抗蚀掩模434a-434c,第二掺杂过程在比第一掺杂过程加速电压高的加速电压下进行。这时的离子掺杂
20 在剂量为 1×10^{13} - $1\times 10^{15}/\text{cm}^2$,加速电压为60-120keV的工况下进行。使用第二导电层428b-432b作为对杂质元素的掩模进行该掺杂过程,使杂质元素加在第一导电层锥形段下边的半导体层上。然后,在比第二掺杂过程加速电压低的加速电压下进行第三掺杂过程,因而得到图9A所示的状态。这时,离子掺杂在剂量为 1×10^{15} - $1\times 10^{17}/\text{cm}^2$,加速电
25 压为50-100keV的工况下进行。由于第二和第三掺杂过程,传递n型的杂质元素加在与第一导电层重叠,浓度范围为 1×10^{18} - $5\times 10^{19}/\text{cm}^3$ 的低浓度杂质区436,442和448。另一方面,传递n型的杂质元素加到浓度范围在 1×10^{19} - $5\times 10^{20}/\text{cm}^3$ 的高浓度杂质区435,438,441,444和447。

不用说,通过设定适当的加速电压,低浓度杂质区和高浓度杂质区通过一个掺杂过程而不用第二和第三个掺杂过程就能形成。

然后,在去掉抗蚀掩模434a-434c后,又新形成抗蚀掩模450a-

450c, 因而要进行第四掺杂过程。由于第四掺杂过程, 在半导体层中形成的杂质区 453, 454, 459 和 460 为 p-沟道 TFT 的有源层, 在这些杂质区中加入了提供与上述电导率类型相反电导率的杂质元素。第二导电层 428a-432a 用作对杂质元素的掩膜, 并加入了传递 n 型的杂质元素, 因而杂质区以自调整方式形成。在本实施方案中, 通过使用乙硼烷 (B_2H_6) 的离子掺杂来形成杂质区 453, 454, 459 和 460。在第四掺杂过程中, 构成 n-沟道 TFT 的半导体层由抗蚀掩模 450a-450c 所覆盖。由于第一至第三掺杂过程, 磷被加到不同浓度的杂质区 438 和 439。但是, 掺杂在两个区进行, 所以传递 p 型的杂质元素浓度成为 $1 \times 10^{19} - 5 \times 10^{21}$ 原子/ cm^3 , 因而这些区域起 P-沟道 TFT 的源区和漏区的作用。因此, 不存在问题。

由于上述过程而在各半导体层形成了杂质区。

然后, 去掉抗蚀掩模 450a-450c, 就形成了第一层间绝缘膜 461。第一层间绝缘膜 461 用厚度为 100-200nm 的含硅绝缘膜通过等离子体 CVD 或溅射而制成。在本实施方案中, 通过等离子体 CVD 形成厚度为 150nm 的氮氧化硅膜。不用说, 第一层间绝缘膜 461 并不限于氮氧化硅膜, 而可以是具有单层结构或多层结构的另一种含硅绝缘膜。

然后, 如图 9C 所示, 半导体层的结晶度恢复了, 而加到各相应半导体层的杂质元素则用激光束辐照进行活化。最好使用持续振荡型或脉冲振荡型固态激光器, 气体激光器, 或金属激光器。特别是, 最好进行使用 YAG 激光器的激光退火过程。如果使用持续振荡型激光器, 要求激光光线的能量密度在约 $0.01-100MW/cm^2$ (最好是 $0.01-10MW/cm^2$), 而基板要以 $0.5-2000cm/s$ 的速度相对于激光光线移动。如果使用脉冲振荡型激光器, 最好将频率设定在 300Hz, 激光能量密度设定在 $50-900mJ/cm^2$ (典型情况是 $50-500mJ/cm^2$)。这时, 激光光线可以重叠 50-98%。在第二导电层与第一层间绝缘膜 461 接触的区域被充分氧化的情况下, 即使受热处理也不会形成如凸起和须状物凸出物, 可以应用使用退火炉的热退火或 RTA。

在形成第一层间绝缘膜之前, 可以进行热处理。在待用的布线不耐热的情况下, 最好在层间绝缘膜 (主要含硅的绝缘膜, 如氮化硅膜) 形成以后进行活化过程以使像在本实施方案中一样来保护布线等。

然后, 通过热处理 ($300^\circ C-450^\circ C$, 1-12 小时) 能进行氢化作用。

在此过程中由于第一层间绝缘膜 461 中所含氢的作用，半导体层不饱和键被端接起来。尽管存在第一层间绝缘膜，但半导体层还是能够被氢化。作为另一种氢化作用的方法，可以进行等离子体氢化作用（使用由等离子体激发的氢）或在含 3-100% 氢的环境中在 300℃-450℃ 进行 1-12 小时的热处理。

其次，在第一层间绝缘膜 461 上形成用无机绝缘膜材料或有机绝缘材料制的第二层间绝缘膜 462a。在本实施方案中，形成的是丙烯酸树脂膜，其厚度为 1.6 μm，粘度为 10-1000cp（最好在 40-200cp），在其表面上还形成厚度不均。在不使用有机树脂膜的情况下，形成了如图 21 所示形状的第二层间绝缘膜 462b。

在本实施方案中，为了防止镜面反射，形成了第二层间绝缘膜，其上厚度不均，从而在象素电极表面上形成厚度不均。此外，为了通过在象素电极表面形成厚度不均而获得光散射，可以在象素电极的下区形成弧形凸起段。在这种情况下，使用与形成 TFT 时同样的光掩模可以形成这些弧形凸起段。因此，过程的数目无需增加。在象素段而不是布线和 TFT 段的基板上可以适当地形成弧形凸起段。有鉴于此，沿着覆盖弧形凸起段的绝缘膜表面上所形成的厚度不均区在象素电极表面上形成厚度不均。

作为第二层间绝缘膜 462a，可以使用表面有待弄平的膜。在这种情况下，最好在形成象素电极后，通过进行已知的喷砂，蚀刻，等使表面形成厚度不均来防止镜面反射并允许被反射的光线散射，由此提高了白度。

在驱动电路 506 中，形成与各个杂质区电连接的导线 463-467。通过使 Ti 膜（厚度：50nm）和合金（Al 和 Ti）膜（厚度：500nm）的层叠膜成形来形成这些导线。应当了解到这些导线可以有单层结构或由三层或更多层组成的多层结构来代替双层结构。此外，布线的材料也不限于 Al 和 Ti。例如，通过在 TaN 膜上形成 Al 或 Cu，及其上形成 Ti 膜所得到的层叠膜可以成形以形成布线（图 10）。

在象素段 507，形成了象素电极 470，栅线 469，以及连接电极 468。连接电极 468 使源线（433a-433c）能电连接至象素 TFT 上。此外，栅线 469 还电连接至象素 TFT 的栅电极上。另外，象素电极 470 电连接至象素 TFT 的漏区 422，并且电连接到起构成存储电容器一个电极板作

用的半导体层 458 上。作为像素电极 470, 最好使用反射性极好的材料如主要含 Al 或 Ag 的薄膜, 或此薄膜的层叠膜。

如上所述, 具有包括 n-沟道 TFT501, P-沟道 TFT502 及 n-沟道 TFT503 的 CMOS 电路的驱动电路, 及具有像素 TFT504 和包括电容器布线 523 的存储电容器 505 的像素段 507 可以在同一基板上形成。这样, 有源矩阵基板就完成了。

驱动电路 506 的 n-沟道 TFT501 具有沟道形成区 437, 低浓度杂质区 436 (GOLD 区), 其与构成部分栅电极的第一导电层 428a 重叠, 以及起源区或漏区作用的高浓度杂质区 452。通过把电极 466 接到 n-沟道 TFT501 而构成 CMOS 电路的 p-沟道 TFT502 具有沟道形成区 440, 起源区或漏区作用的高浓度杂质区 454, 以及杂质区 453, 此区中掺入了传递 n 型的杂质元素和传递 p 型的杂质元素。此外, n-沟道 TFT503 具有沟道形成区 443, 低浓度杂质区 442 (GOLD 区), 其与构成部分栅电极的第一导电层 430 重叠, 以及起源区或漏区作用的高浓度杂质区 456。

像素段 507 的像素 TFT504 具有沟道形成区 446, 栅电极外形成的低浓度杂质区 445 (轻微掺杂漏 (LDD) 区), 以及起源区或漏区作用的高浓度杂质区 458。此外, 传递 n-型的杂质元素和传递 p-型的杂质元素加到起存储电容器 505 一个电极板作用的半导体层上。存储电容器 505 由电极 (层叠结构 432a-432c) 和使用绝缘膜 416 作电介质的半导体层组成。

在本实施方案的像素配置中, 像素电极边缘要安排成与源线相重叠, 这样像素电极间的间隙就实现光屏蔽而不用黑色矩阵。

此外, 图 11 示出本实施方案中制造的有源矩阵基板像素段的顶视图。图 8A-8C-11 中相对应的区段用同样的参考数字表示。图 10 中点划线 A-A' 与图 11 中沿点划线 A-A' 所剖的截面相对应。图 10 中点划线 B-B' 与图 11 中沿点划线 B-B' 所剖的截面相对应。

在如此生产出的布线中, 实现了低阻, 而具有此布线的布线板也完全可以用于扩大的像素段。

本实施方案可以随意地与实施方案 1-4 的任何一个结合起来。

[实施方案 6]

在本实施方案中，使用实施方案 5 中制造的有源矩阵基板来制造反射型液晶显示器件的过程将参照图 12 予以说明。

首先，根据实施方案 5，得到如图 10 所示的有源矩阵基板。其后，至少在图 10 中有源矩阵基板上的像素电极 470 上形成调整膜 567，并进行磨擦处理。在本实施方案中，调整膜 567 形成之前，先使有机树脂膜如丙烯酸树脂膜成形，从而在所要求的位置形成保持基板间隙的柱形分隔件 572。此外，球形分隔件可以分布在基板的整个表面上而取代柱形分隔件。

然后，制造副基板 569(counter substrate)。在副基板 569 上形成彩色层 570 和 571，及校平膜 573(leveling film)。红色层 570 与蓝色层 571 相重叠以形成光屏蔽段。将红色层与绿色层部分地重叠来形成光屏蔽段也是可能的。

在本实施方案中，使用实施方案 5 中说明的基板。因此，在示出实施方案 5 像素段顶视图的图 11 中，要求至少栅线 469 和像素电极 470 之间的间隙，栅线 469 和连接电极 468 之间的间隙，以及连接电极 468 和像素电极 470 之间的间隙应当进行光屏蔽。在本实施方案中，各彩色层的设置应使由叠层彩色层组成的光屏蔽段与待进行光屏蔽的位置相重叠，在此条件下固定副基板。

如上所述，各个像素之间的间隙用由叠层彩色层组成的光屏蔽段进行光屏蔽，因而过程的数目能够减少而不用形成光屏蔽层如黑色掩模。

然后，至少在像素段中的校平膜 573 上形成由透明导电膜组成的反电极 576，在副基板的整个表面上形成调整膜 574，从而进行磨擦处理。

然后，其上形成有像素段和驱动电路的有源矩阵基板及副基板用密封剂层 568 相互粘在一起。填料混入密封剂后 568 中，两个基板在相同的间隔用填料和柱形分隔件相互粘在一起。其后，在基板之间注入液晶材料 575，并用密封剂对基板进行完全密封（未示出）。对于液晶材料 575，可以使用已知的液晶材料。这样，图 12 所示的反射型液晶显示器件就完成了。如果需要的话，有源矩阵基板或副基板可分离成所需的形状。此外，极化板（未示出）只粘在副基板上。然后，挠性印刷电路（FPC）用已知的技术粘结。

按如上所述制造的液晶显示板可以用来作为各种各样电子设备的显示部分。液晶显示板完全可以用于大面积而无须降低像素段的孔径比。

本实施方案能随意与实施方案 1-5 中的任何一个相结合。

5

[实施方案 7]

在本实施方案中，有源矩阵型液晶显示器件的制造过程将参照图 13 予以说明，而该液晶显示器件与使用实施方案 5 中制造的有源矩阵基板的实施方案 6 之液晶显示器件不同。

10 首先，根据实施方案 5，得到如图 8A-8C 所示的有源矩阵基板。其后，在图 8A-8C 中的有源矩阵基板上形成调整膜 1067，并进行摩擦处理。在本实施方案中，形成调整膜 1067 之前，使有机树脂膜如丙烯酸树脂膜成形，从而在所要求的位置形成保持基板间隙的柱形分隔件 572。此外，球形分隔件可以分布在基板的整个表面来代替柱形分隔件。

15

然后，制备副基板 1068。副基板装有色彩滤波器，滤波器中设置彩色层 1074 和光屏蔽层 1075 以使与各像素相对应。在驱动电路段均等地形成光屏蔽层 1077。设置了覆盖色彩滤波器和光屏蔽层 1077 的校平膜 1076。然后，由校平膜 1076 上透明导电膜制的反电极 1069 在像素段形成，调整膜 1070 在副基板 1068 的整个表面上方形成，其后进行摩擦处理。

20

然后，其上形成有像素段和驱动电路的有源矩阵基板和副基板用密封剂层 1071 相互粘结。填料混入密封剂层 1071 中，两个基板在相同的间隔用填料和柱形分隔件相互粘结在一起。其后，在基板之间注入液晶材料 1073，并用密封剂对基板进行完全密封（未示出）。对于液晶材料 1073，可以使用已知的液晶材料。这样，图 11 所示的有源矩阵型液晶显示器件就完成了。如果需要的话，有源矩阵基板或副基板可以分离成所需的形状。此外，使用已知技术适当地设置极化板等。然后，FPC 用已知技术粘接。

25

30 如上所述制造的液晶显示板可以用作各种各样电子设备的显示部分。液晶显示板完全可以用于大面积而无需降低像素段的孔径比。

本实施方案能随意与实施方案 1-5 中的任何一个结合起来。

[实施方案 8]

在本实施方案中，作为利用本发明布线板的实施方案，对发光器件的典型生产情况将利用制造 TFT 的方法予以说明，而该法是用来制造实施方案 5 中有源矩阵基板的。在本说明书中，发光器件该称为显示板，其中在基板上形成的发光元件被封在基板和覆盖件及显示组件之间，在显示组件中 IC 安装在显示板上。发光元件包括含有有机化合物的发光层，它使得利用电场发出的电致发光能被得到，阳极层，以及阴极层。此外，有机化合物内的发光包括在单一态激发态返回到常态时得到的荧光和三重态激发态返回到常态时得到的磷光。两种发光之一或两种发光都包括在内。

在本说明书中，在发光元件中阳极和阴极之间形成的所有层都定义为有机发光层。具体地说，有机发光层包括发光层，空穴注入层，电子注入层，空穴迁移层，电子迁移层，等等。发光元件的基本结构是在结构中依次堆叠了阳极层，发光层及阴极层。除上述结构外，发光元件可能具有的结构为：阳极层，空穴注入层，发光层，及阴极层依次堆叠的结构；阳极层，空穴注入层，发光层，电子迁移层，及阴极层依次堆叠的结构，等。

图 14 为本实施方案发光器件的截面视图。在图 14 中，设置在基板 700 上的开关 TFT603 使用图 10 中的 n-沟道 TFT503 形成。有关开关 TFT603 的配置，可参照 n-沟道 TFT503 的说明。

虽然本实施方案表示的是结构中形成有两个沟道形成区的双栅结构，但可以使用结构中形成有一个沟道形成区的单栅结构或结构中形成三个沟道形成区的三栅结构。

设置在基板 700 上的驱动电路使用图 10 所示的 CMOS 电路形成。因此，关于驱动电路配置的说明，可参照 n-沟道 TFT501 和 p-沟道 TFT502 的说明。虽然本实施方案表示的是单栅结构，但也可以使用双栅结构或三栅结构。

此外，导线 701 和 703 起 CMOS 电路源线的作用，而导线 702 起漏线的作用。导线 704 起将源线 708 电连接到开关 TFT 源区的导线的作用，导线 705 起将漏线 709 电连接到开关 TFT 漏区的导线的作用。

电流控制 TFT604 用图 10 中 p-沟道 TFT502 形成。因此，关于电

流控制 TFT604 的说明, 可以参照 p-沟道 TFT502 的说明。虽然本实施方案表示的是单栅结构, 但可以使用双栅结构或三栅结构。

5 导线 706 为电流控制 TFT604 的源线 (相当于电流供应线), 参考数字 707 表示通过与电流控制 TFT 的像素电极 711 相重叠而电连接到像素电极 711 的上的电极。

像素电极 711 为发光元件的阳极, 用透明导电膜制成。作为透明导电膜, 可以使用氧化铟和氧化锡的混合物, 氧化铟和氧化锌的混合物, 氧化锌, 氧化锡, 或氧化铟。可以使用加有镓的透明导电膜。在形成上述布线以前, 像素电极 711 在平坦的层间绝缘膜 710 上形成。
10 在本实施方案中, 使用树脂制的校平膜 710 整平 TFT 造成的台阶差极其重要。稍后将形成的发光层非常薄, 所以由于台阶差的存在可能会造成光发射缺陷。因此, 最好在形成像素电极之前将表面整平从而发光层能在平整的表面上形成。

在导线 701-707 形成之后, 形成接线排 712, 如图 14 所示。通过
15 使绝缘膜或含硅的有机树脂膜 (厚度 100-400nm) 成形可以形成接线排 712。

由于接线排 712 用绝缘膜制成, 故在膜形成过程中应当考虑元素的静电击穿。在本实施方案中, 通过向将作为接线排 712 材料的绝缘膜加入碳粒子或金属粒子来增加电阻, 从而使静电受到抑制。这时,
20 可以调节碳粒子或金属粒子的加入量使电阻成为 $1 \times 10^6 - 1 \times 10^{12} \Omega \text{m}$ (最好在 $1 \times 10^8 - 1 \times 10^{10} \Omega \text{m}$)。

在像素电极 711 上形成发光层 713。虽然在图 14 中示出一个像素, 但形成的发光层要能与本实施方案中的 R (红色), G (绿色), 和 B (蓝色) 相对应。此外, 在本实施方案中, 低分子量的有机发光材料
25 通过气相沉积形成。更具体地说, 是使用层叠结构, 在该结构中设置铜酞菁 (CuPc) 膜 (厚度: 20nm) 作为空穴注入层, 设置三-8-羟基基喹啉并铝络合物 (Alq₃) 膜 (厚度 70nm) 作为空穴注入层上的发光层。通过向 Alq₃ 加入荧光物如二羟基喹啉并吡啶、三苯胺苯, 或 DCM1, 能够控制发射光的颜色。

30 应当注意可以用作发光层的典型有机发光材料在上面已进行了说明, 但是本实施方案并不限制于此。发光层 (用于发射光和移动光发射的载体) 可以通过任意组合发光层, 电荷迁移层, 或电荷注入层而

形成。在本实施方案中，作用低分子量的有机发光材料作为发光层；但是，也可以使用中等分子量的有机发光材料或高分子量的有机发光材料。在本说明书中，中等分子量有机发光材料是指没有升华特性，含 20 或更少的分子或链接分子长度为 $10\mu\text{m}$ 或更短的有机发光材料。

5 此外，作为使用高分子量有机发光材料的实例，可以使用层叠结构，在此结构中，通过旋转涂敷聚噻吩（PEDOT）膜（厚度：20nm）作为空穴注入层，在空穴注入层上形成对亚苯基次乙烯基（PPV）膜（厚度：约 100nm）作为发光层。在使用 PPV 的 π -共轭型聚合物时，从红至蓝的发光波长能进行选择。此外，使用无机材料如碳化硅作为电荷迁移层或电荷注入层也是可能的。作为有机发光材料和无机材料，可以使用已知的材料。

其次，由导电膜制的阴极 714 在发光层 713 上形成。在本实施方案中，使用铝和锂的合金膜作为导电膜。不用说，可以使用已知的 MgAg 膜（镁和银的合金膜）。作为用于阴极的材料，可以使用由属于周期表第一族或第二族的元素制的导电膜或加有这些元素的导电膜。

15 在阴极 714 形成时，发光元件 715 就完成了。这里的发光元件 715 是指由像素电极（阳极）711，发光层 713，及阴极 714 形成的二极管。

形成钝化膜 716 是有用的，以便完全覆盖发光元件 715。作为钝化膜 716，使用单层结构或多层结构的绝缘膜，包括碳膜，氮化硅膜，或氮氧化硅膜。

20 在这种情况下，最好使用有令人满意覆盖范围的薄膜作为钝化膜。使用碳膜（特别是 DLC 膜）是有效的。由于 DLC 膜能在从室温到 100°C 的温度范围内形成，故 DLC 膜甚至在低热阻的发光层 713 之上也能容易地形成。此外，由于对氧的屏蔽作用高，DLC 膜能够抑制发光层 713 之上也能容易地形成。此外，由于对氧的屏蔽作用高，DLC 膜能够抑制发光层 713 的氧化。因此，在进行随后的密封过程时发光层 713 能够免于被氧化。

此外，在钝化膜 716 上形成密封剂层 717，覆盖件 718 粘合密封剂层 717 上。作为密封剂层 717，可以使用 UV-可固化树脂，而在密封剂层 717 中加入有吸湿性的材料或有抗氧化作用的材料是有效的。此外，在本实施方案中，作为覆盖件 718，使用玻璃基板，石英基板，或其两侧都形成有碳膜（最好是 DLC 膜）的塑料基板（包括塑料薄膜）。

因此,具有图 14 所示配置的发光器件就完成了。接线排 712 形成后,连续地进行纯化膜 716 的形成过程而不暴露给多室型(或串联型)薄膜形成仪中的环境是有效的。连续地进行该过程直到粘结覆盖件 718 而不暴露给上述环境也是可能的。

- 5 因此,在基板 700 上形成了 n-沟道 TFT601 和 602,开关 TFT (n-沟道 TFT) 603,以及电流控制 TFT (n-沟道 TFT) 604。

此外,如图 14 所述,通过形成借助于绝缘膜与栅电极相重叠的杂质后,可以形成不大可能因热载体效应而变坏的 n-沟道 TFT。因此,就能获得了高度可靠的发光器件。

- 10 在本实施方案中,只示出了像素段和驱动电路的配置。但是,按照本实施方案的制造过程,能够在同一绝缘体上形成逻辑电路诸如信号分隔电路,D/A 转换器,运算放大器,及 γ -校正电路。此外,甚至能够形成存储器和微信息处理机。

- 15 为保护发光元件而进行的密封(或封装)过程之后,本实施方案的发光器件将参照图 15A 和 15B 予以说明。如果需要的话,将引用图 14 中使用的参考数字。

- 20 图 15A 为顶视图其示出发光元件完成密封时的状态。图 15B 为沿图 15A 中直线 C-C'取的截面视图。用虚线围起来并用参考数字 801,806,及 807 表示的区段分别为源侧驱动电路,像素段,及栅侧驱动电路。参考数字 901 表示覆盖件,902 表示第一密封剂层,903 表示第二密封剂层,在用密封剂层 902 围起来的内区段形成密封材料 907。

- 25 参考数字 904 表示布线,它把信号输入传输给源侧驱动电路 801 和栅侧驱动电路 807 并且从将成为外部输入端的挠性印刷电路(FPC)接收视频信号和时钟信号。这里,虽然仅示出 FPC,但印刷布线板(PWB)也可以连接到 FPC 上。本说明书中的发光器件不仅包括发光器件本身而且包括带有 FPC 或 PWB 的发光器件。

- 30 其次,将参照图 15B 说明截面配置图。像素段 806 和栅侧驱动电路 807 在基板 700 之上形成。像素段 806 由电流控制 TFT604 和包括像素电极 710 的多个像素所组成,像素电极 710 与电流控制 TFT604 的漏线电连接。此外,栅侧驱动电路 807 由 CMOS 电路(见图 14)组成,后者通过把 n-沟道 TFT601 与 P-沟道 TFT602 相结合而得到。

像素电极 711 起发光元件阳极的作用。接线排 712 在像素电极 711

的两端形成，发光元件的发光层 713 和阴极 714 在像素电极 711 上形成。

5 阴极 714 起所有像素公用布线的作用，并且通过连接线 904 电连接至 FPC905。此外，像素段和栅侧驱动电路 807 所含的所有元件都被阴极端 14 和纯化膜 716 所覆盖。

10 覆盖件 901 与第一密封剂层 902 粘接。可以形成树脂膜制的分隔件以保证覆盖件 901 与发光元件之间的间隙。第一密封剂层 902 的内区段灌满了密封材料 907。最好将环氧树脂用于第一密封剂层 902 和密封材料 907。最好第一密封剂层 902 不太可能传输水分和氧气。此外，密封材料 907 可以含具有吸湿性和抗氧化作用的材料。

为覆盖发光元件而形成的密封材料 907 还起着连接覆盖件 901 的粘接剂作用。在本实施方案中，作为构成覆盖件 901 的塑料基板 901a 的材料，可以使用玻璃钢（FRP），聚氧乙烯（PVF），聚脂树脂，聚脂，或丙烯酸树脂。

15 此外，在覆盖件 901 与密封材料 907 粘接后，形成第二密封剂层 903 以覆盖密封材料 907 的侧表面（暴露的表面）。第二密封剂层 903 可以用与第一密封剂层 902 所用的同样材料制成。

20 在上述配置中通过用密封材料 907 封装发光元件，发光元件能与外界完全隔绝，因而由于氧化作用如水分和氧气而引起的发光层材料加速剥蚀能够防止从外界侵入。这样，就得了高度可靠的发光器件。此外，发光器件完全适用于大面积而不必降低像素段的孔径比。

本实施方案能够随意与实施方案 1-5 的任何一个结合。

[实施方案 9]

25 在本实施方案中，具有与实施方案中不同像素配置的发光器件将参照图 16 予以说明。

30 在图 16 中，作为电流控制 TFT4501，使用具有与图 10 中 P-沟道 TFT502 同样配置的 TFT，而作为开关 TFT4402 则使用具有与图 10 中像素 TFT504 同样配置的 TFT。不用说，电流控制 TFT4501 的栅电极电连接至开关 TFT4402 的漏线上。此外，电流控制 TFT4501 的漏线电连接至在绝缘膜 4409 上形成的像素电极 4504 上。

在本实施方案中，用导电膜制成的像素电极 4504 起发光元件阴极

的作用。更具体地说，使用铝和锂的合金膜。可以使用由属于周期表中第一族或第二族元素制成的导电膜或加有该元素的导电膜。

在象素电极 4504 上形成发光层 4505。在图 16 中只示出一个象素，在本实施方案中，相应于 G（绿色）的发光层通过气相沉积和涂敷（最好是旋转涂敷）形成。更具体地说，发光层为多层结构，其中形成氟化锂（LiF）膜（厚度：20nm）作为电子注入层。在氟化锂膜上再形成多聚合苝苯基乙烯基（PPV）膜（厚度：70nm）作为发光层。

在发光层 4504 上形成由透明导电膜制成的阳极 4506。在本实施方案中，作为透明导电膜，使用由氧化铟和氧化锡的混合物或氧化铟和氧化锌的混合物制成的导电膜。

阳极 4506 形成时，发光元件 4507 就完成了。这里发光元件 4507 是指由象素电极（阳极）4504，发光层 4505，及阳极 4506 形成的二极管。

形成纯化膜 4508 是有用的以便完全覆盖发光元件 4507。作为纯化膜 4508，使用单层结构或多层结构的绝缘膜，包括碳膜，氮化硅膜，或氮氧化硅膜。

此外，在纯化膜 4508 上形成密封材料 4509，覆盖件 4510 粘结在密封材料 4509 上。作为密封材料 4509，可以使用 UV-可固化树脂，而在密封材料 4509 中加入有吸湿性或抗氧化作用的材料是有效的。在本实施方案中，作为覆盖件 4510，使用玻璃基板，石英基板，或其两侧都形成有碳膜（最好是 DLC 膜）的塑料基板（包括塑料薄膜）。

在这样制造的发光器件布线中，实现了低阻，而这样的发光器件完全适用于大面积而不用降低象素段的孔径比。

本实施方案能够随意与实施方案 1-5 中的任何一个相结合。

[实施方案 10]

在本实施方案中，将对根据本发明的典型液晶显示器件予以说明。器件中 TFT 的配置与实施方案 5 中制造的有源矩阵基板的 TFT 配置不同。

在图 18A 所示的有源矩阵基板上，形成了具有 n-沟道 TFT503，和 P-沟道 TFT502 的驱动电路 506，及具有象素 TFT504 和存储电容器 505 的象素段 507。

5 这些 TFT 是通过在基板 501 上形成栅线 512-517, 在栅线 512-517 (512a-517a, 512b-517b, 及 512c-517c) 上形成绝缘膜 511 (511a 和 511b), 及在绝缘膜上的半导体层中形成沟道形成区, 源区, 漏区, LDD 区等而得到的。半导体层是根据本发明, 以与实施方案 1-5 中同样的方式形成的。

10 形成栅线 512-517 其厚度应为 200-400nm (最好 250nm), 这样栅线 512-517 可做成锥形以提高将在其上层形成的涂敷膜之台阶覆盖范围。形成栅线 512-517 要使锥形角成为 5° - 30° (最好 15° - 30°)。锥形段通过干法蚀刻形成, 而其角度由蚀刻气体和加在基板侧的偏压来控制。

此外, 在第一至第二掺杂过程中形成杂质区。首先, 进行第一掺杂过程, 从而形成 n-沟道 TFT 的 LDD 区。掺杂可以利用离子掺杂或离子注入进行。加入磷 (P) 作为传递 n-型 (施主) 的杂质元素, 第一杂质区带掩模形成。然后, 重新形成掩模以覆盖 n-沟道 TFT 的 LDD 区, 15 从而在第二掺杂过程中形成了 n-沟道 TFT 的源区和漏区。

在第三掺杂过程中, 形成 P-沟道 TFT 的源区和漏区。利用离子掺杂或离子注入进行掺杂, 只加入传递 P-型 (受主) 的杂质元素。这时, 其中将形成 n-沟道 TFT 的半导体层用掩模覆盖, 所以传递 P-型的杂质元素将不会被加到半导体层上。在本实施方案中, 虽然在 P-沟道 TFT 20 中没制造 LDD 区, 但可以形成 LDD 区。

这样, 在 n-沟道 TFT503 中, LDD 区 530 和源区或漏区 531 是在沟道形成区 529 之外形成的。P-沟道 TFT502 也有同样的配置, 并且由沟道形成区 527 及源区或漏区 528 组成。在本实施方案中, 使用单栅结构; 但是, 可以使用双栅结构或三栅结构。

25 在像素段 507 中, 由 n-沟道 TFT 形成的像素 TFT504 为了减少 OFF 电流而具有多栅结构, 而 LDD 区 533, 及源区或漏区 534-536 则在沟道形成区 532 之外形成。

30 层间绝缘膜由用无机材料如氧化硅、氮化硅, 或氮氧化硅制的第一层间绝缘膜 540 (厚度: 50-500nm) 及用有机绝缘材料如聚酰亚胺, 丙烯酸树脂, 聚酰亚胺氮化物, 及苯并环丁烯 (BCB) 制的第二层间绝缘膜 541 所组成。这样, 通过由有机绝缘材料形成的第二层间绝缘膜, 层间绝缘膜的表面能够令人满意地整平。有机树脂材料通常其介电常

数低，所以能够减少寄生电容。但是，有机树脂材料由于其吸湿性而不适于作保护膜，所以最好与第一层间绝缘体 540 结合起来。

其后，形成具有预先定图形的抗蚀掩模，并形成接触孔，其伸到半导体层中形成的源区或漏区。接触孔通过干法蚀刻形成。在这种情况下，使用 CF_4 、 O_2 和 He 的混合气体作为蚀刻气体首先对由有机树脂材料制的第二层间绝缘膜 541 进行蚀刻，其后，使用 CF_4 和 O_2 作为蚀刻气体对第一层间绝缘膜 540 蚀刻。

然后，通过溅射或真空蒸汽汽化来形成导电金属膜。这样就形成了抗蚀掩模图形，并通过蚀刻形成导线 543-549。这样，就能够形成有源矩阵基板。

使用图 18A 中有源矩阵基板制造有源矩阵型液晶显示器件的过程将予以说明。图 18B 示出有源矩阵基板用密封剂 558 粘结在副基板 554 上的状态。首先，在图 18A 所示的有源矩阵基板上形成柱形分隔件 551 和 552。在像素段中设置的分隔件 551 要形成得与像素电极上的接触段相重叠。虽然会随着将要使用的液晶材料而有所改变，但分隔件的高度将设定在 $3\text{-}10\mu\text{m}$ 。在接触段，对应接触孔形成凹入段。因此，通过使形成的分隔件与凹入段相对准，液晶的定向就能够免受干扰。其后，形成调整膜 553，并进行摩擦处理。在副基板 554 上形成透明导电膜 555 和调整膜 556。然后，有源矩阵基板和副基板相互连接，并在其中间注入液晶 557。

按上述制造的有源矩阵型液晶显示器件能够用作为用于各种电子器件的显示仪器。上述的液晶显示板完全适用于大面积而不必降低像素段中的孔径比。

本实施方案能够随意与实施方案 1-5 中的任何一个相结合。

[实施方案 11]

对使用实施方案 10 中说明的有源矩阵基板制造发光器件的情况将予以说明。

在图 19 中，作为电流控制 TFT4501 使用具有与图 16 中 n-沟道 TFT503 同样配置的 TFT。不用说，电流控制 TFT4501 的栅电极电连接到开关 TFT4402 的漏线上。电流控制 TFT4501 的漏线电连接至绝缘膜 4409 上形成的像素电极 4504。

在本实施方案中，由导电膜制成的象素电极 4505 起发光元件阴极的作用。更具体地说，使用铝和锂的合金膜。可以使用由属于周期表中第一族或第二族元素制成的导电膜或加有该元素的导电膜。

- 在象素电极 4504 上形成发光层 4505。在图 19 中只示出一个象素。
- 5 在本实施方案中与 G（绿色）相应的发光层通过气相沉积和涂敷（最好是旋转涂敷）形成。更具体地说，使用层叠结构，在此结构中形成 LiF 膜（厚度：20nm）作为电子注入层，其上再形成 PPV 膜（厚度：70nm）作为发光层。

- 其次，在发光层 4505 上形成由透明导电膜制的阳极 4506。在本
- 10 实施方案中，使用由氧化铟和氧化锡的混合物或氧化铟和氧化锌的混合物制成的导电膜。

在阳极 4506 形成时，发光元件 4507 就完成了。发光元件 4507 是指由象素电极（阴极）4504，发光层 4505，及阳极 4506 组成的二极管。

- 15 形成纯化膜 4508 是有用的以便完全覆盖发光元件 4507。作为纯化膜 4508，使用单层结构或多层结构的绝缘膜，包括碳膜，氮化硅膜，或氮氧化硅膜。

- 此外，在纯化膜 4508 上形成密封材料 4509，覆盖件 4510 粘接到密封材料 4509 上。作为密封材料 4509，可以使用 UV-可固化树脂，并
- 20 且在密封材料 4509 中形成有吸湿性的材料或有抗氧化作用的材料是有用的。此外，在本实施方案中，作为覆盖件 4510，使用玻璃基板，石英基板，或其两侧形成有碳膜（最好是 DLD 膜）的塑料基板，石英基板，或其两侧形成有碳膜（最好是 DLC 膜）的塑料基板（包括塑料薄膜）。

- 25 这样制造的发光器件完全可以用于大面积用而不必降低象素段中的孔径比。

本实施方案能够随意与实施方案 1-5 中的任何一个相结合。

[实施方案 12]

- 30 根据本发明形成的布线板能够用于各种各样的电光仪器（有源矩阵型液晶显示器件，有源矩阵型 EC 显示仪器，及有源矩阵型发光器件）。具体地说，在这些电光仪器被纳入到显示部分的所有电子设备

中都能够实施本发明。

这类电子设备的实例包括个人计算机和显示器。图 20A-20C 示出其实例。

图 20A 示出个人计算机，它包括本体 3001，图象输入部分 3002，
5 显示部分 3003，键盘 3004，等。本发明应用于显示部分 3003。本发明随时可用于扩大显示部分 3003。

图 20B 示出使用存储程序记录介质（以下只称为记录介质）的播放机，它包括本体 3401，显示部分 3402，扬声器部分 3403，记录介质 3404，操作开关 3405 等。这种播放机使用数字通用光盘（DVD），
10 光盘（CD），等作为记录介质，能够用来听音乐，看电影，玩游戏，及上互联网。本发明可应用于显示部分 3402。本发明随时可用于扩大显示部分 3402。

图 20C 示出显示器，它包括本体 4101，底座 4102，显示部分 4103，等。本发明可应用于显示部分 4103。本发明的显示器对屏幕的扩大做好充分准备。特别是，本发明有利于对角线尺寸为 10 英寸或更大（特别是 30 英寸或更大）的显示器。
15

如上所述，本发明的应用范围极大，而且本发明可应用于各个领域的电子设备。此外，采用利用实施方案 1-11 任意组合而得到的结构能够获得本实施方案的电子设备。

20 采用本发明的结构，可以得到下面的基本重要事实。

（a）适合于常规布线和制造布线板的过程的简单方法。

（b）布线中实现低电阻。因此，设计自由和象素段孔径比的程度提高了。

（c）得到了满意的覆盖范围。

25 （d）在半导体器件如有源矩阵型液晶显示器件中，在上述优点使人满意的同时，象素段的面积也增大了，本发明对屏幕的扩大做好了充分准备，这将提高半导体器件的工作特性和可靠性。

各项其他改进对本领域的技术人员将会变得明显起来并且能够易于被他们实现而又不偏离本发明的领域与构思。因此，不打算把此处
30 所附的权利要求范围限制在如这里所提出的说明，而是对这些权利要求予以广泛的解释。

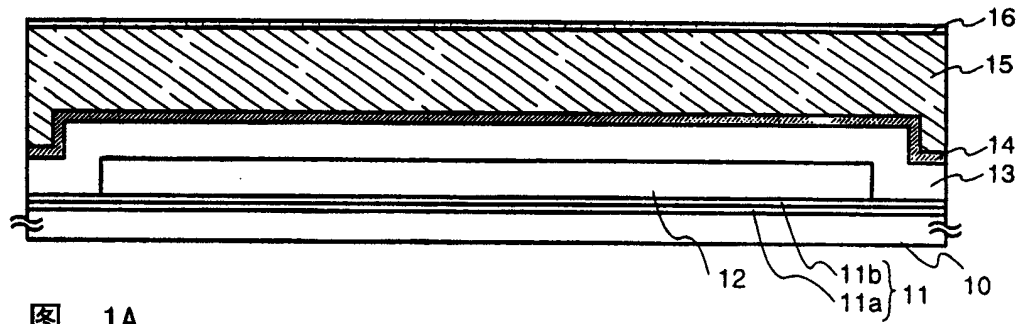


图 1A

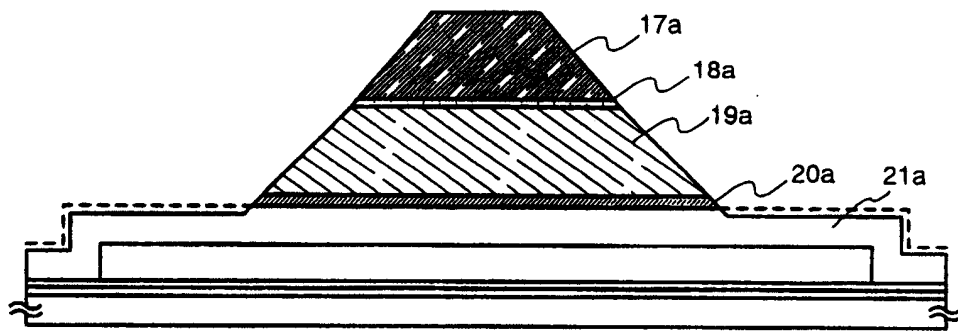


图 1B

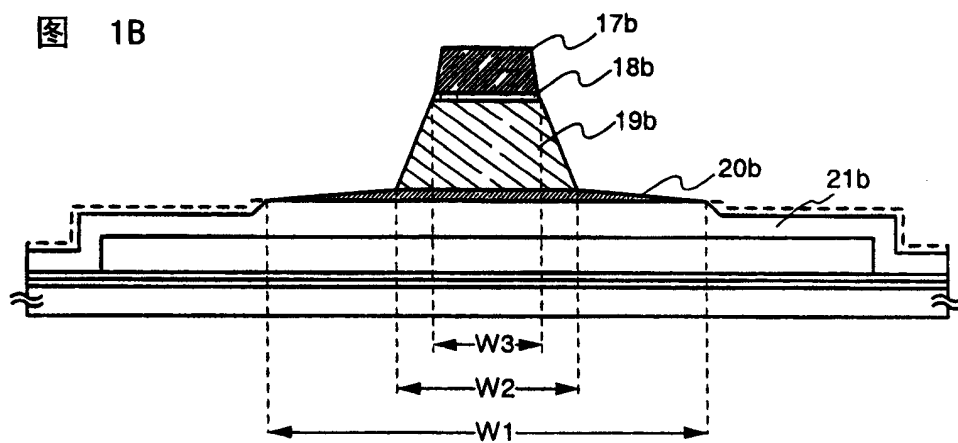


图 1C

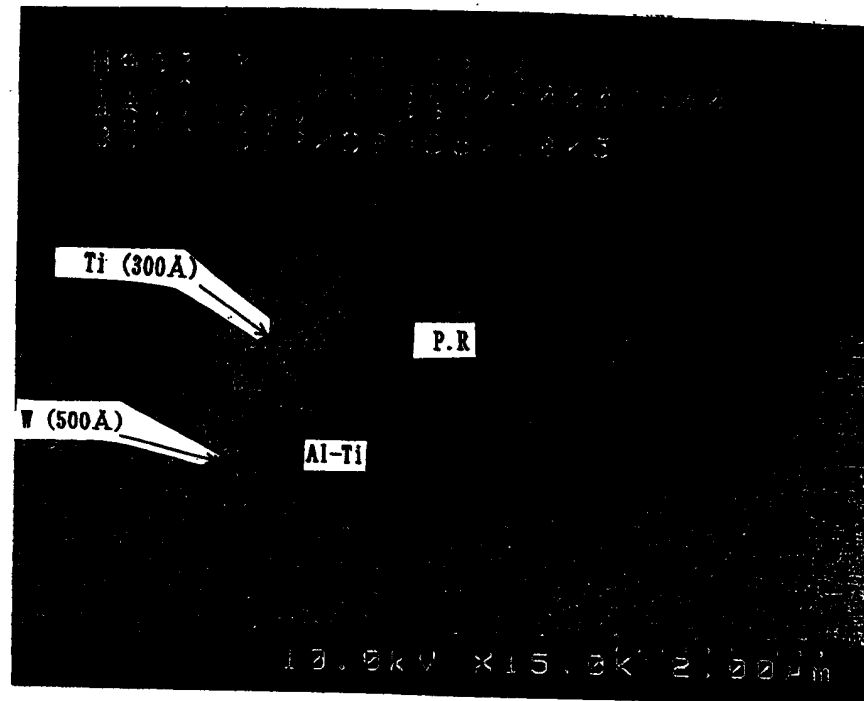


图 2A

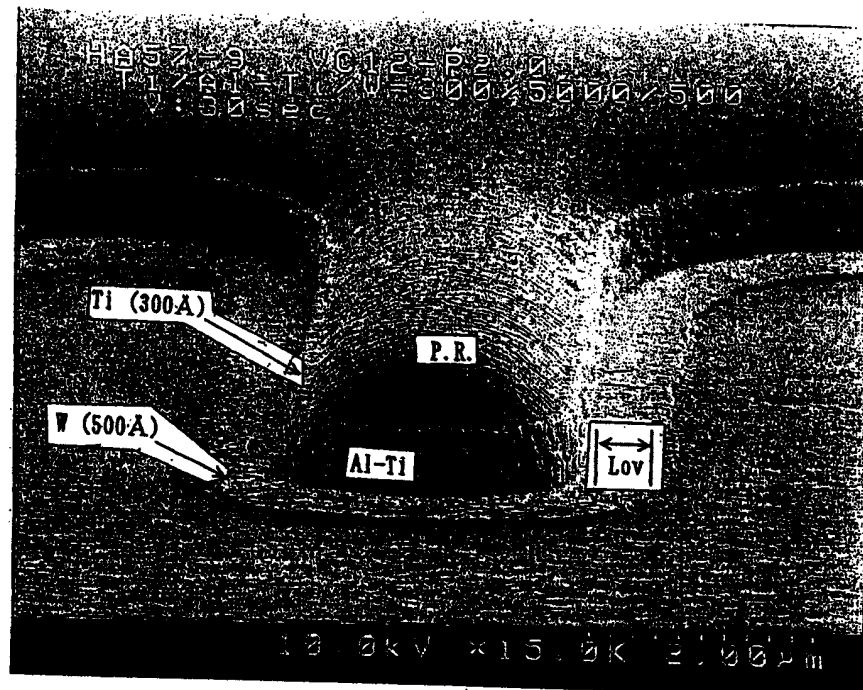


图 2B

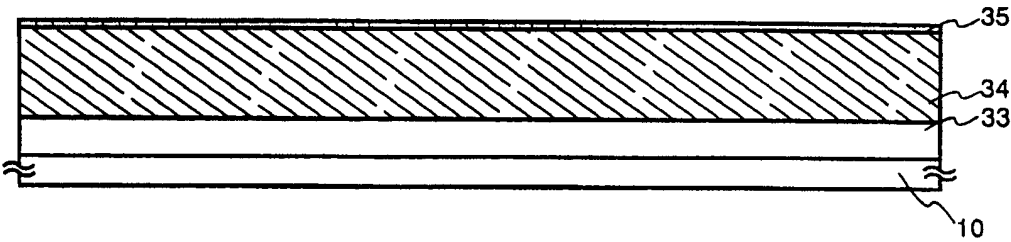


图 3A

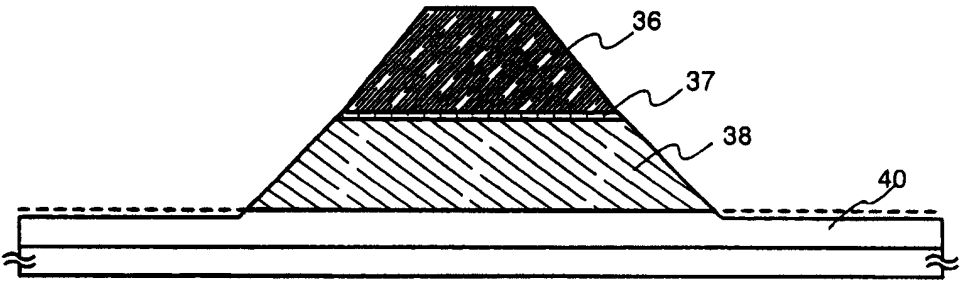


图 3B

图 4A

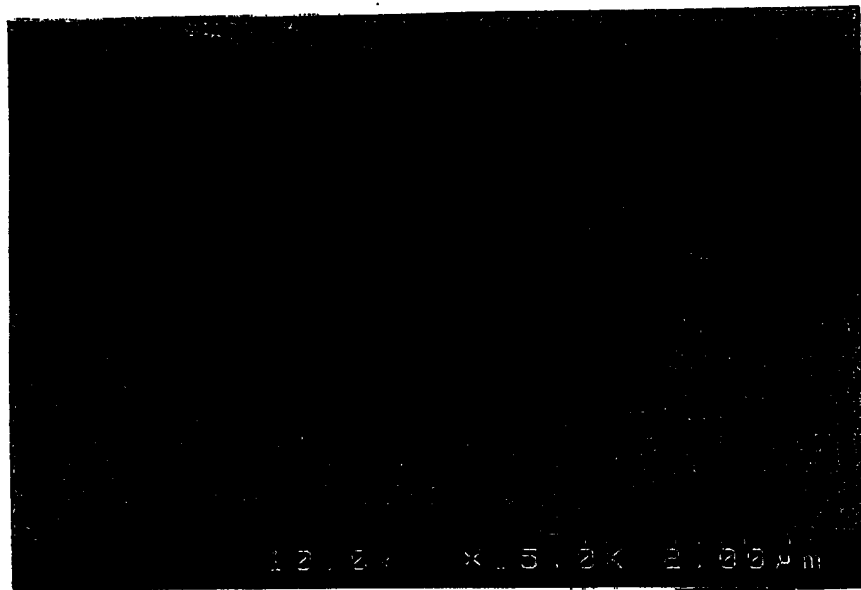


图 4B



图 4C

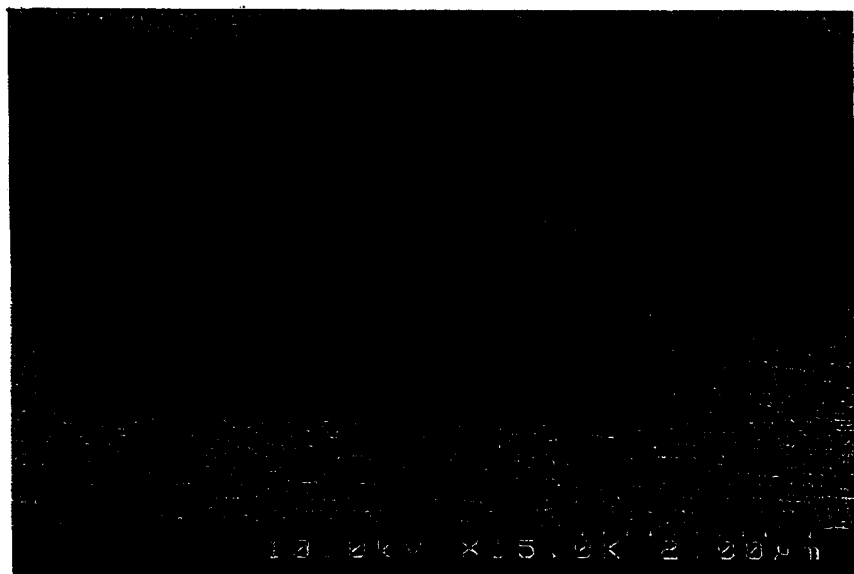


图 5A

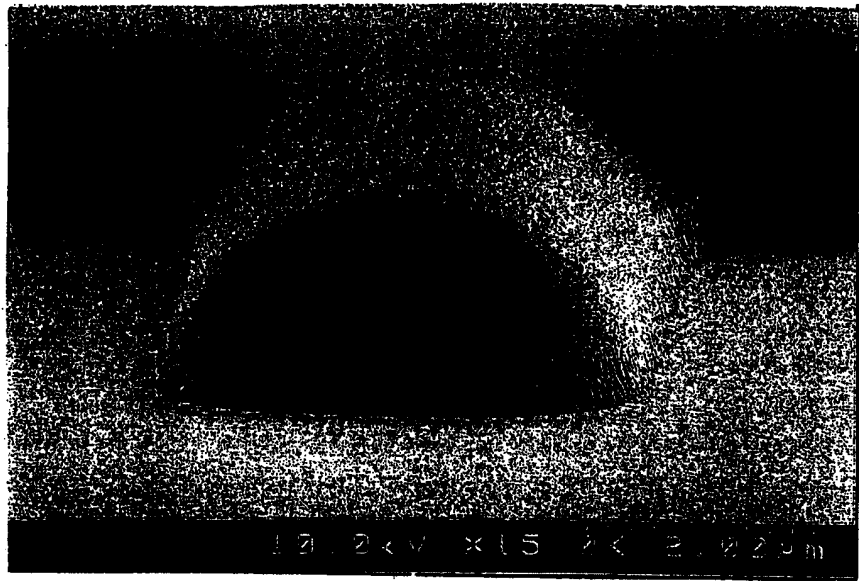


图 5B

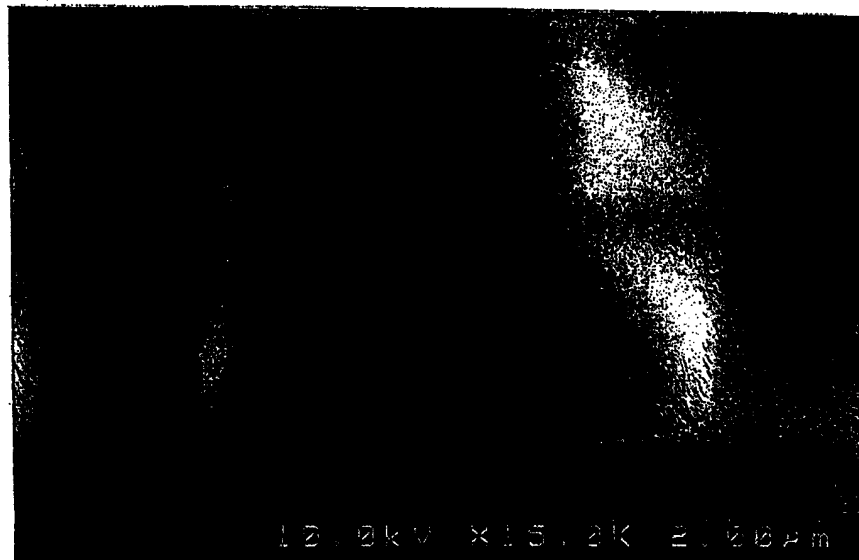
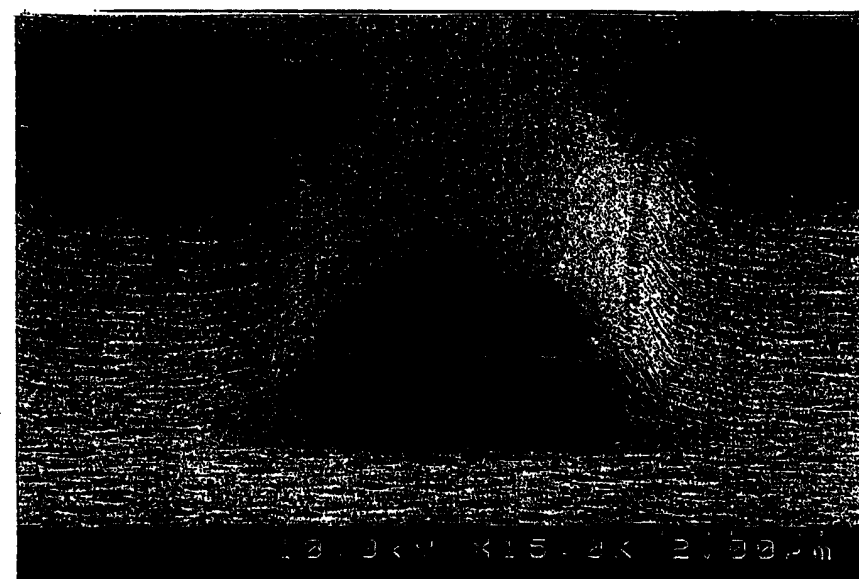


图 5C



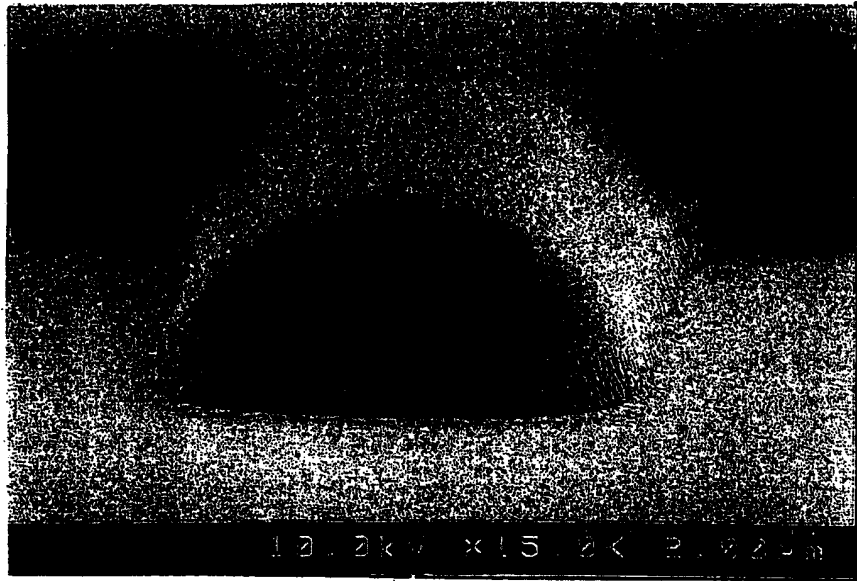


图 6A

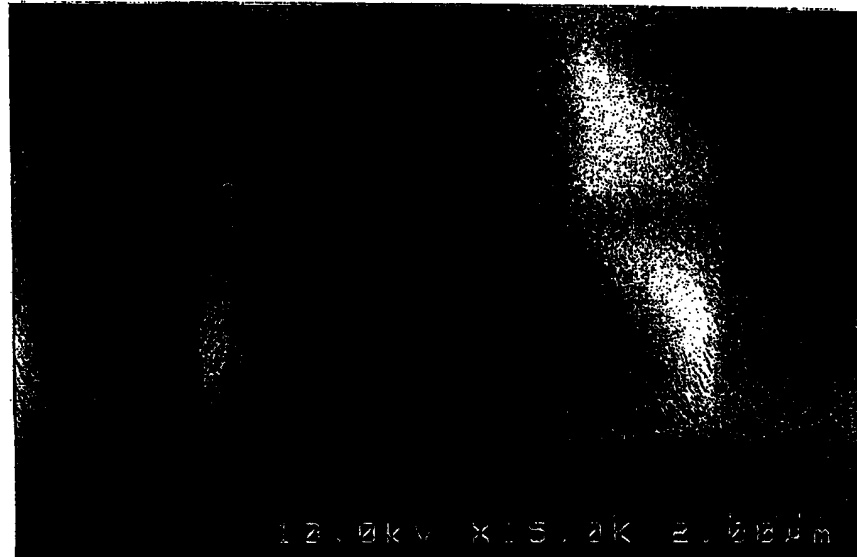


图 6B

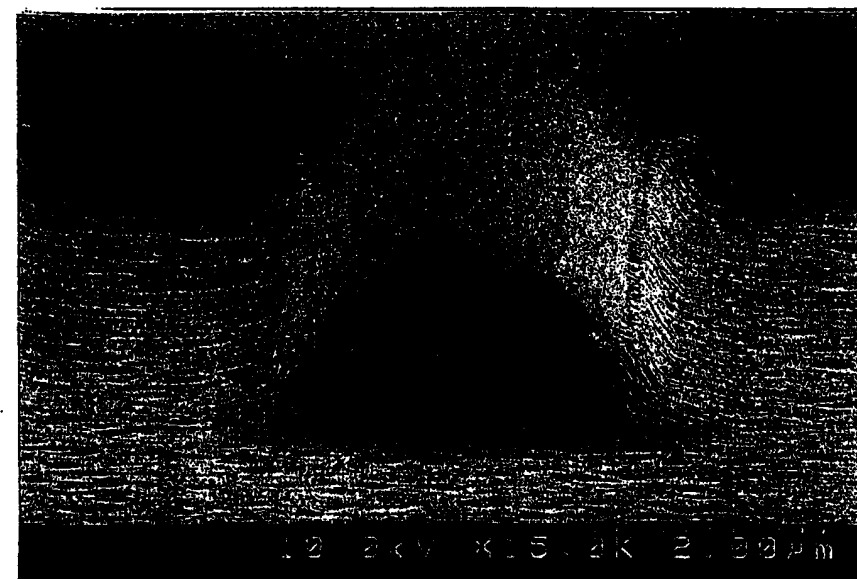


图 6C

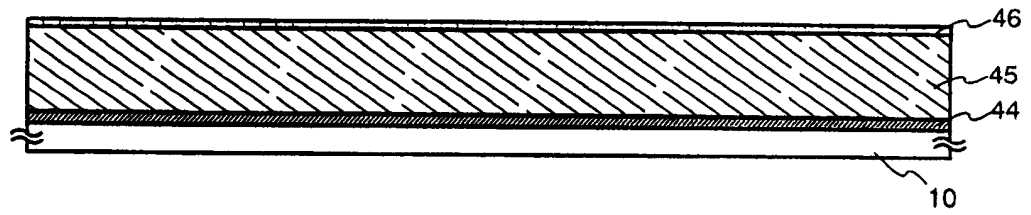


图 7A

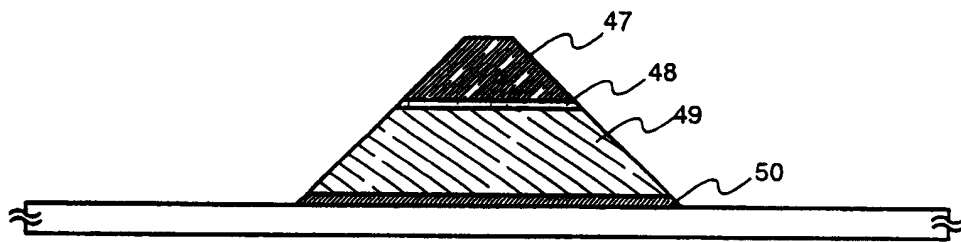


图 7B

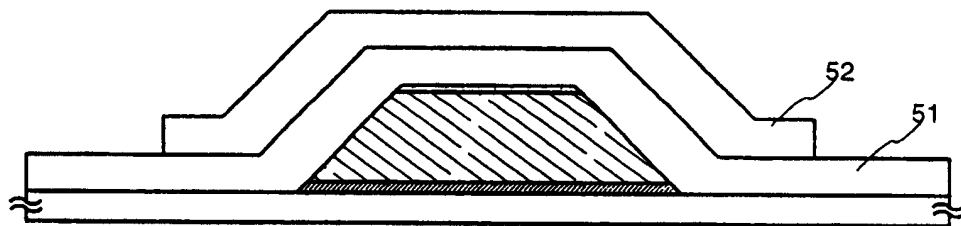
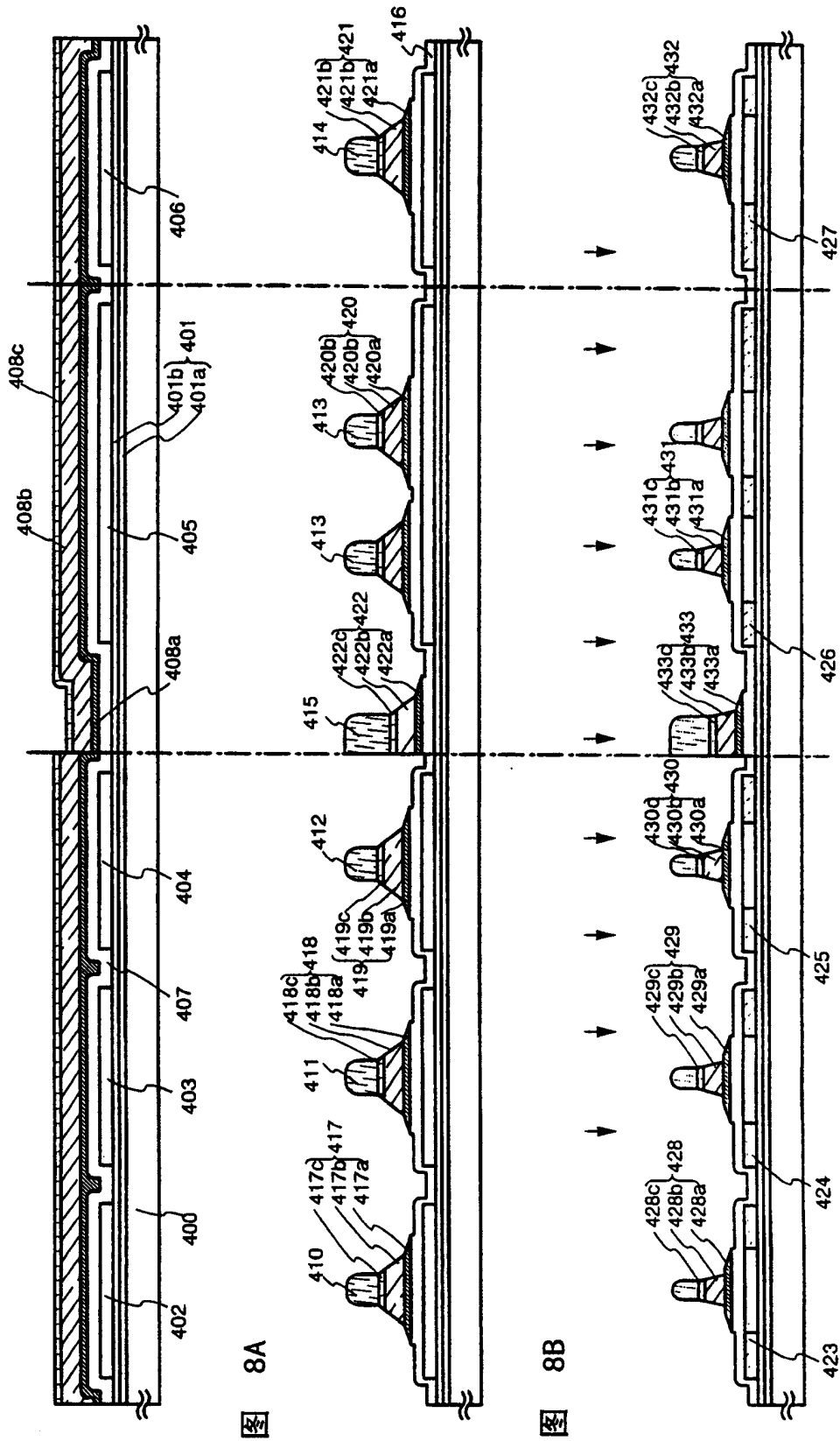


图 7C



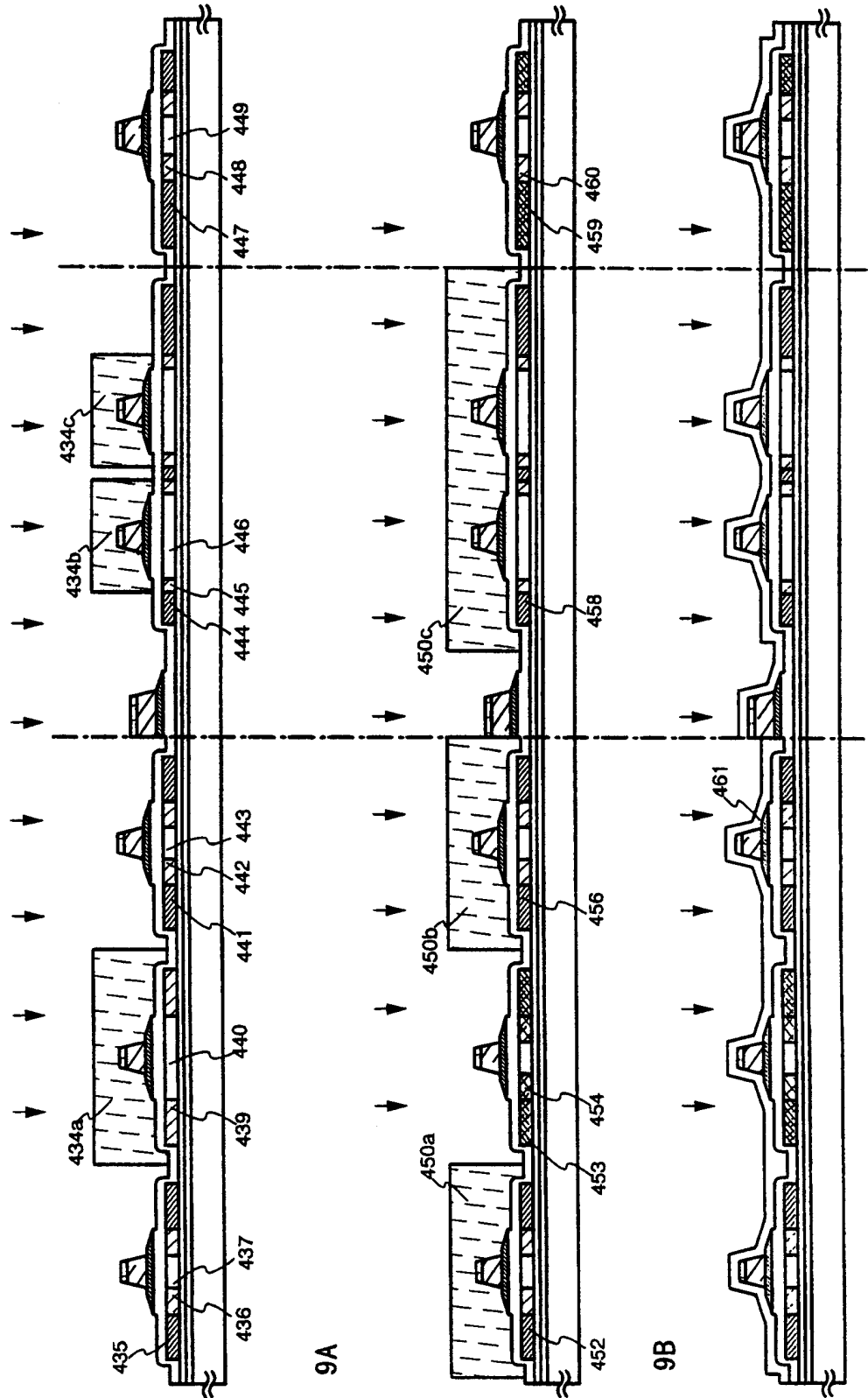


图 9A

图 9B

图 9C

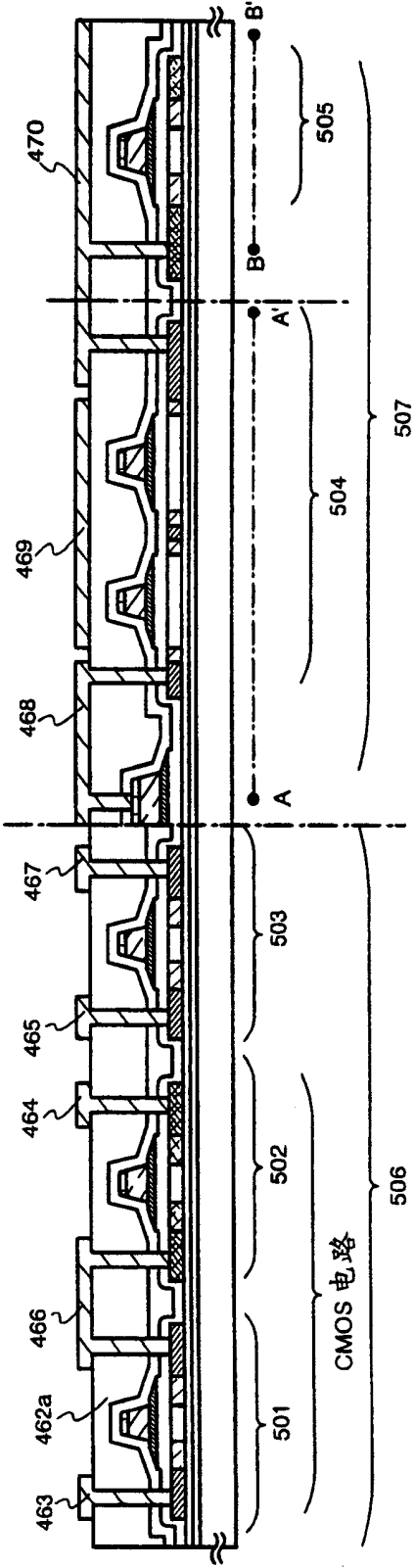


图 10

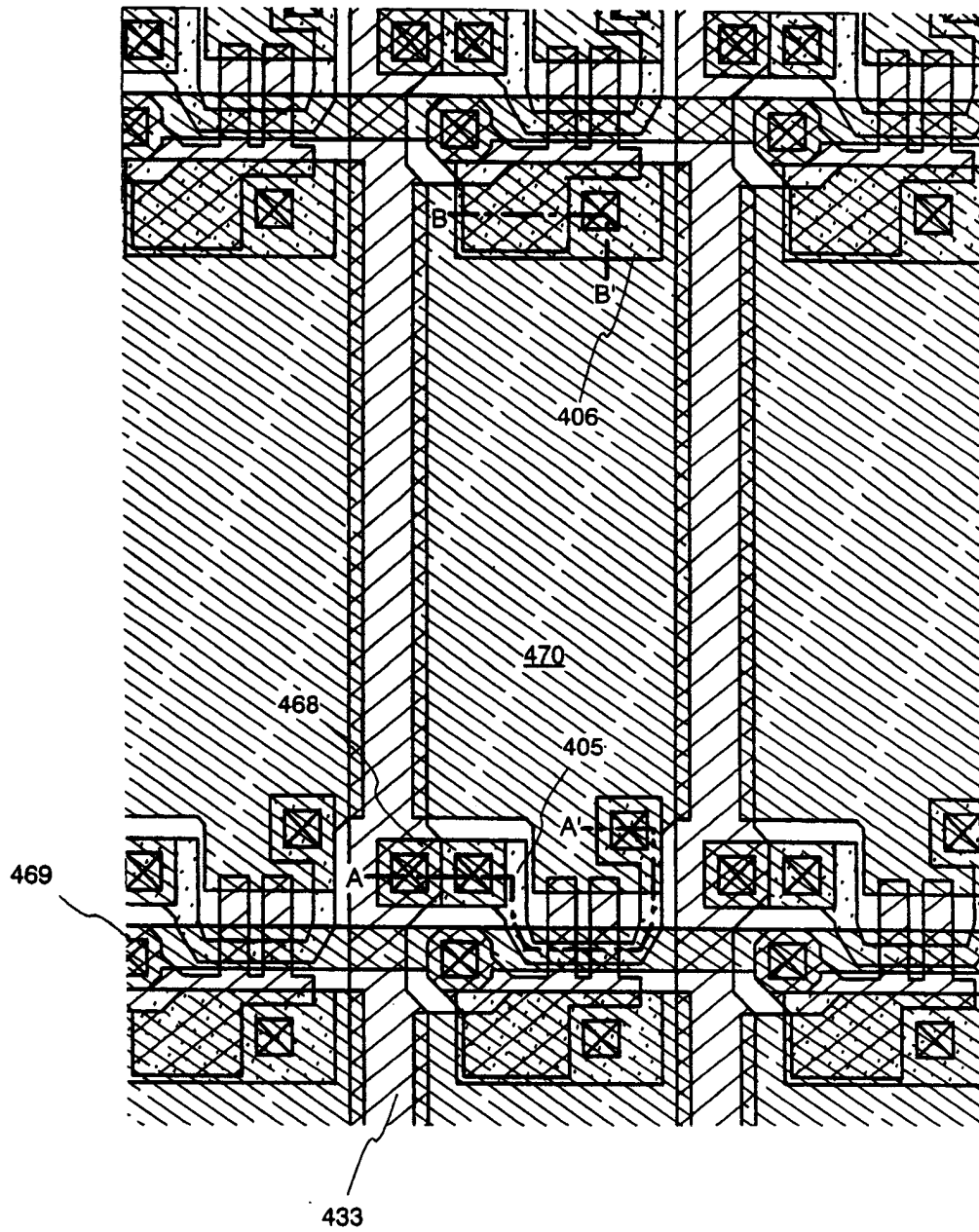


图 11

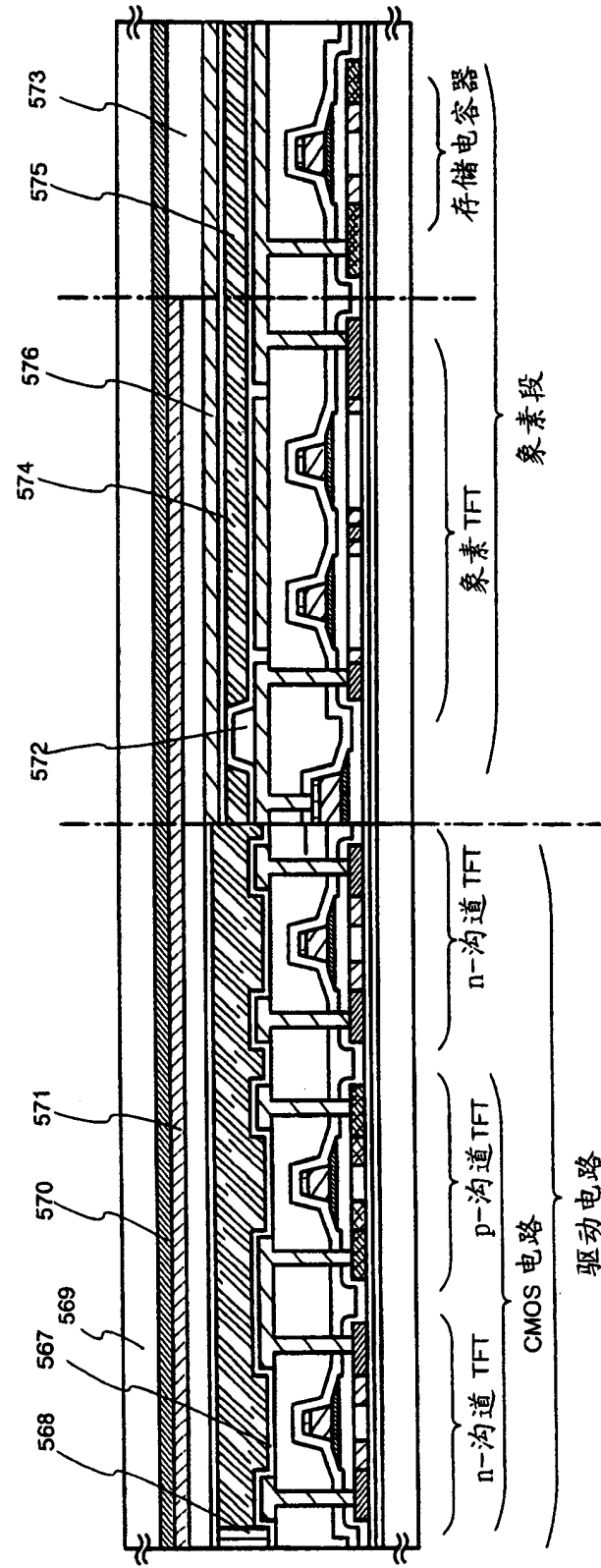


图 12

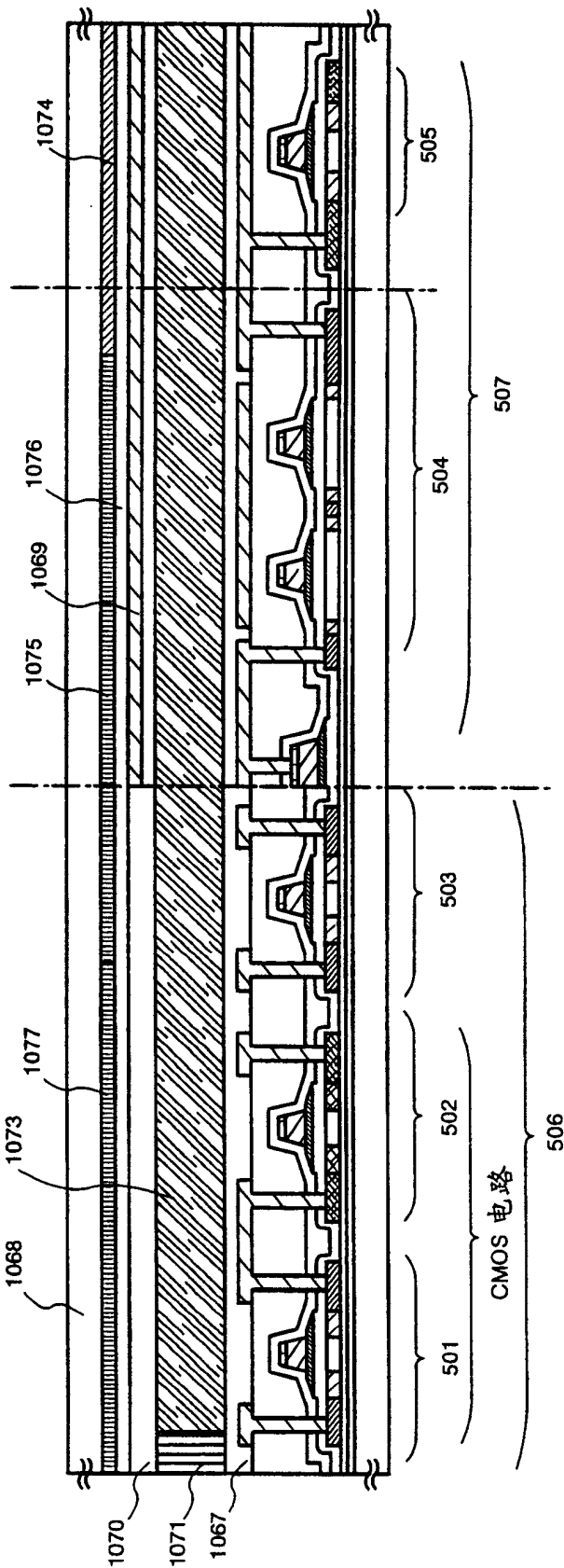


图 13

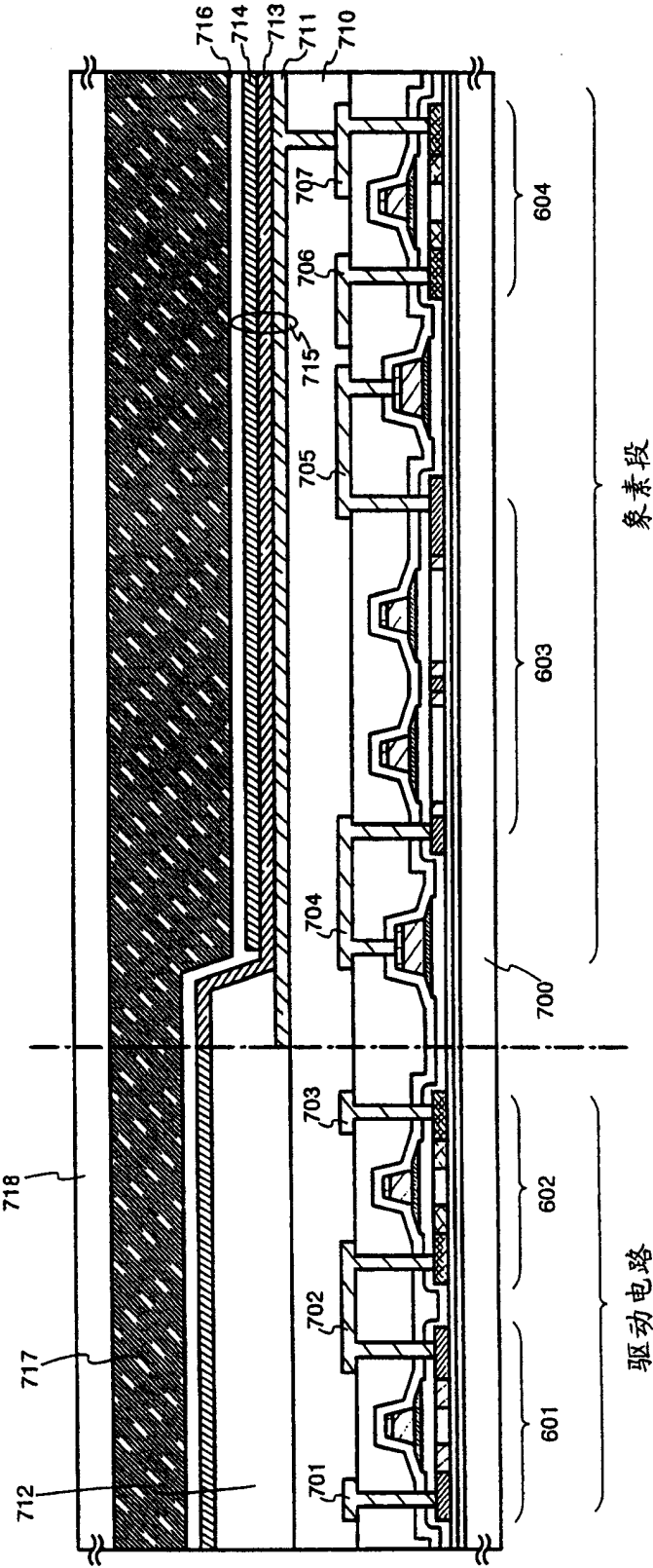


图 14

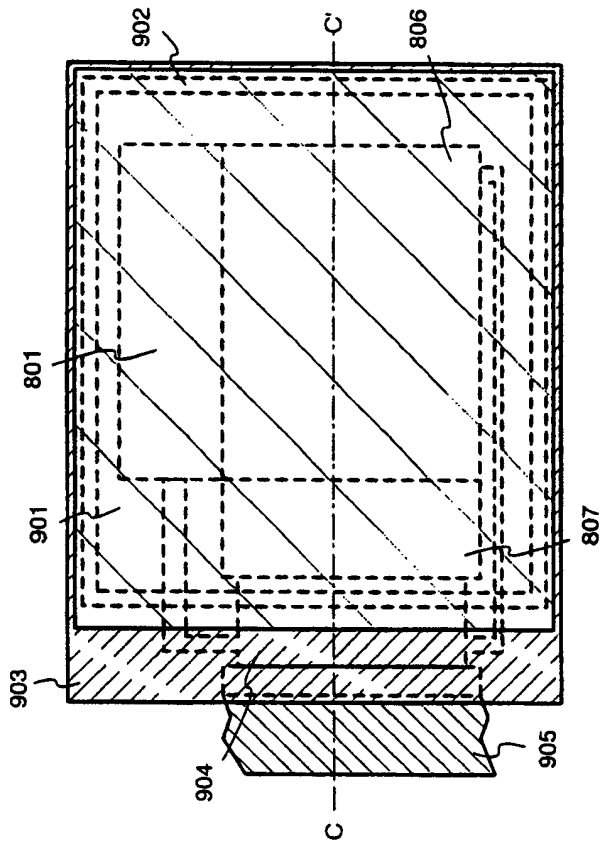


图 15A

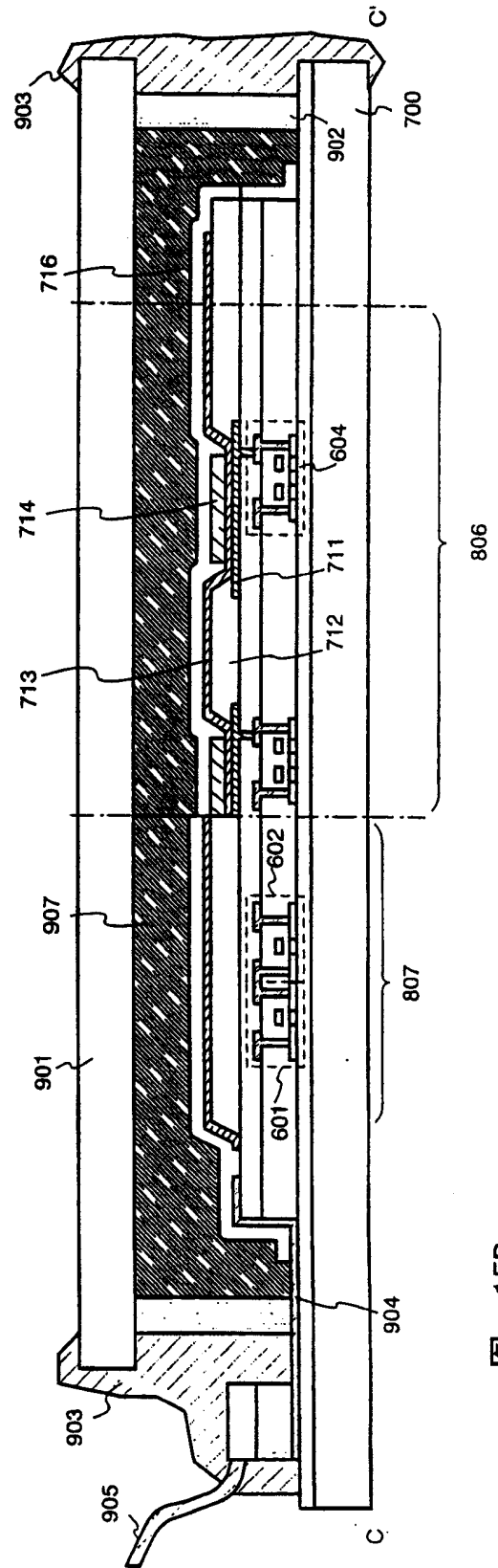


图 15B

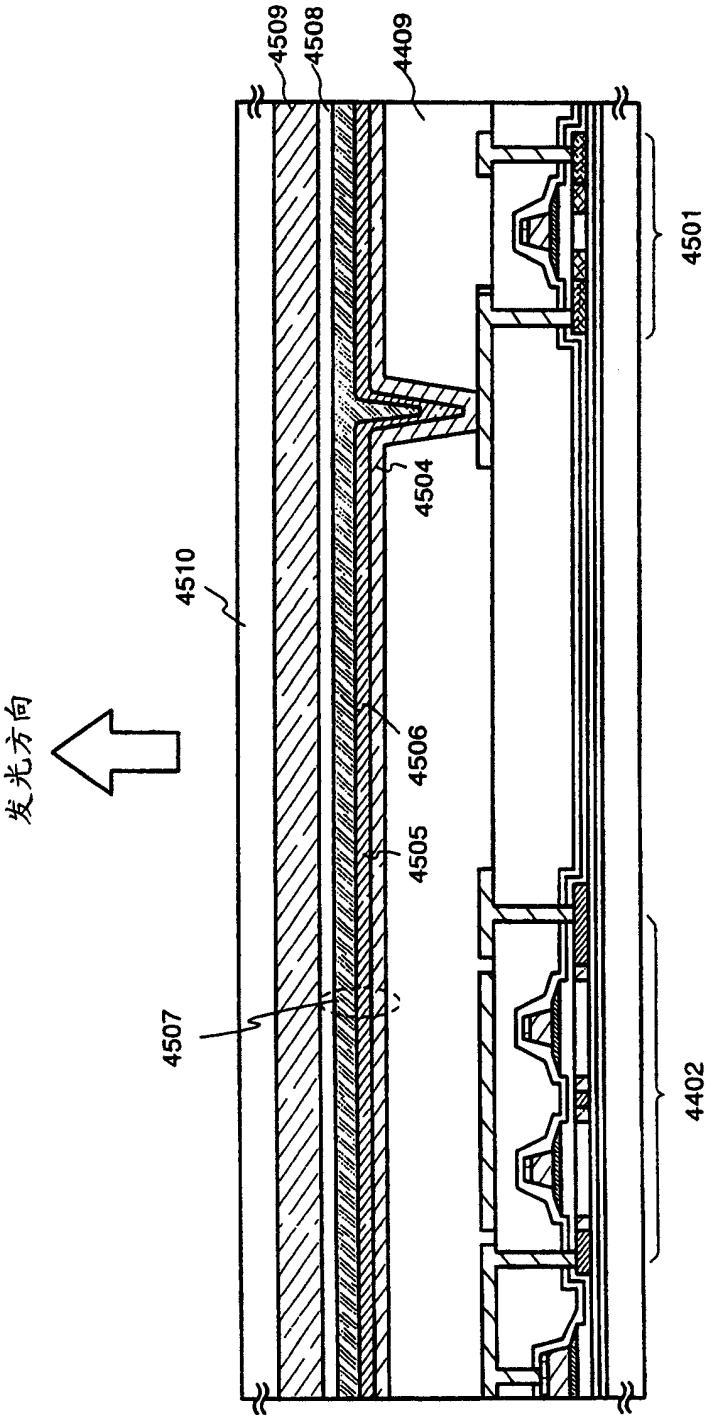


图 16

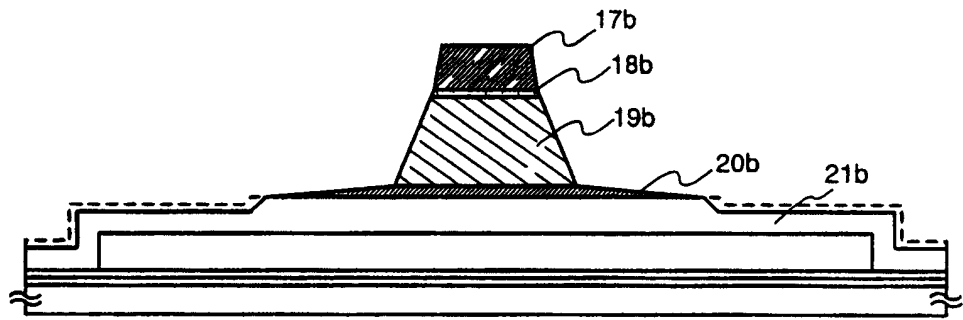


图 17A

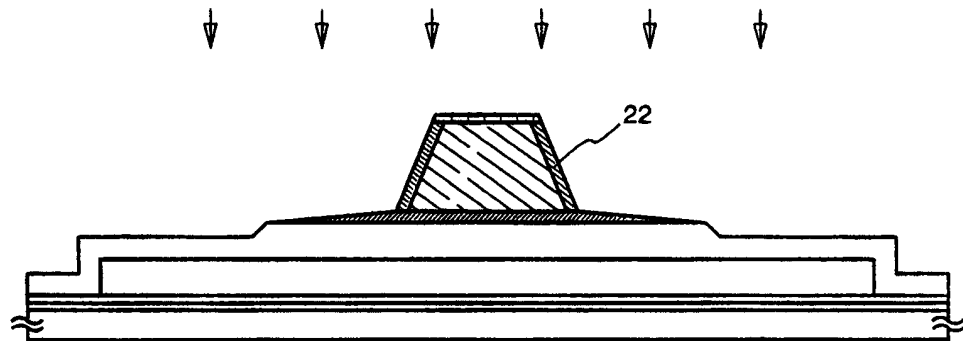


图 17B

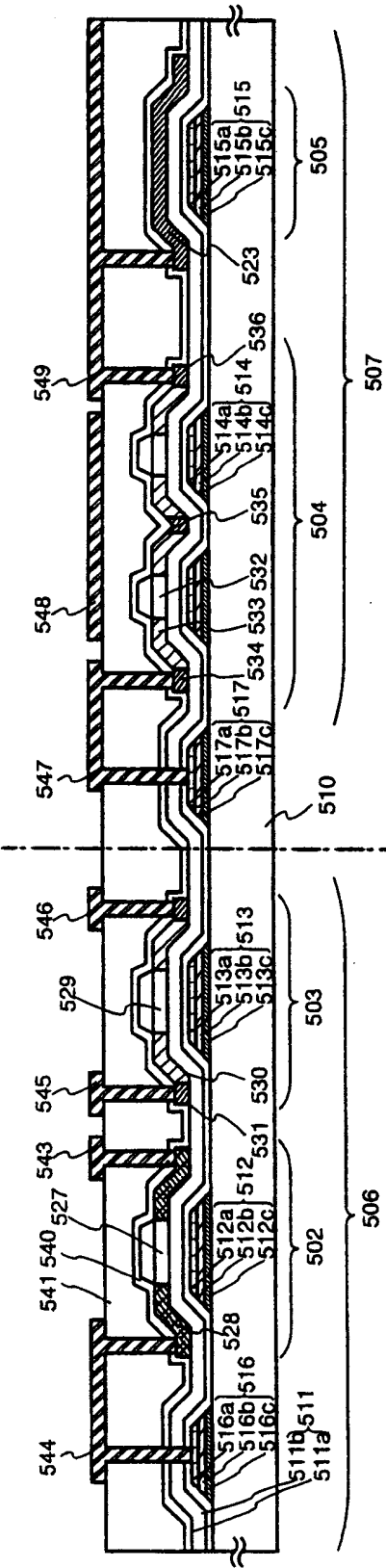


图 18A

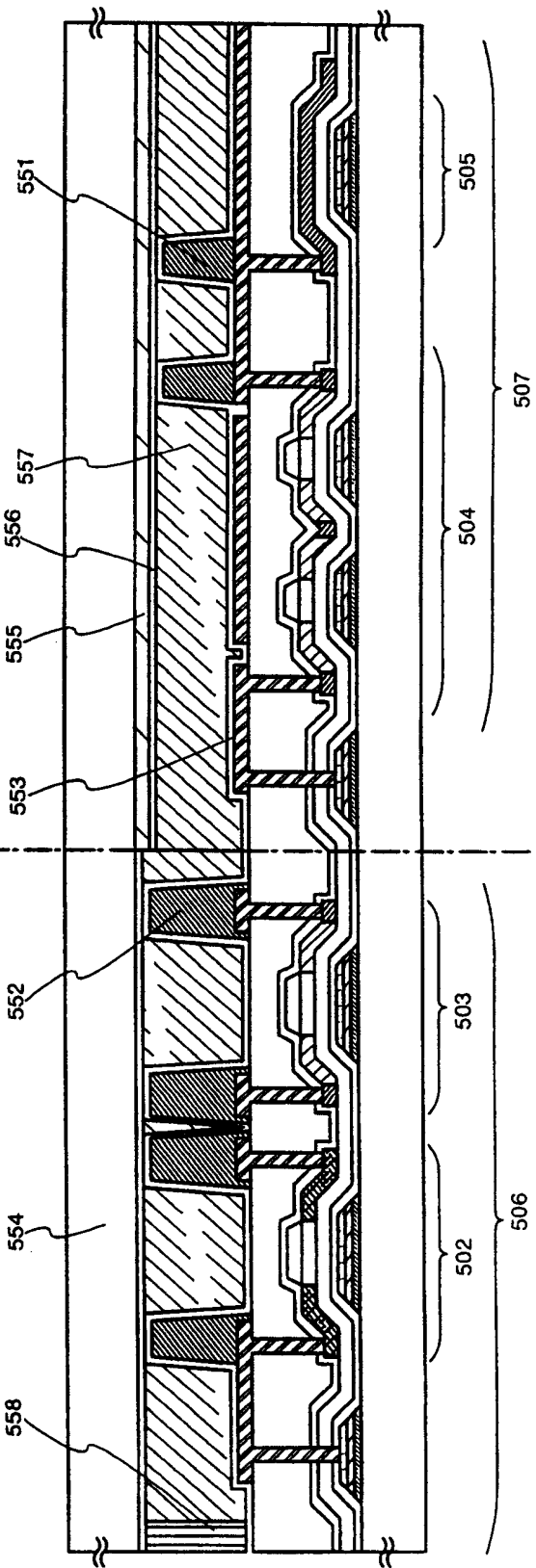


图 18B

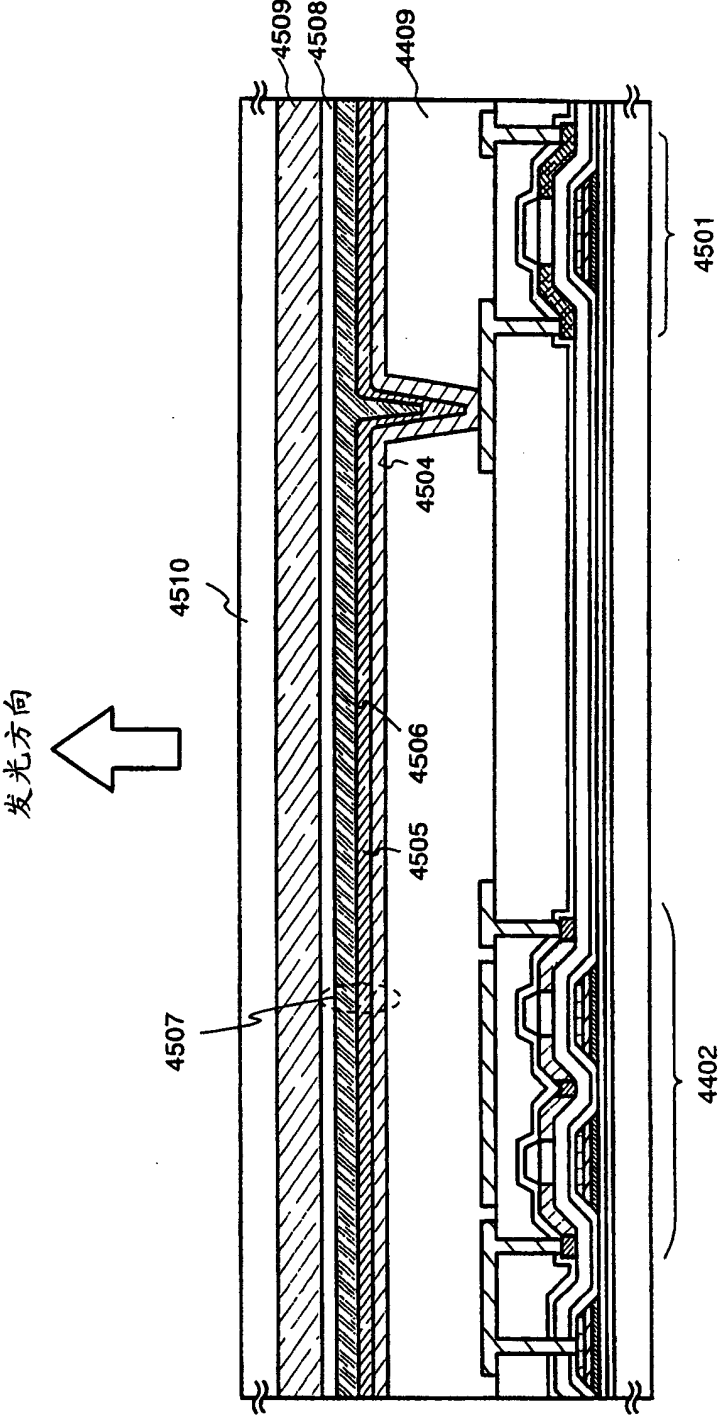


图 19

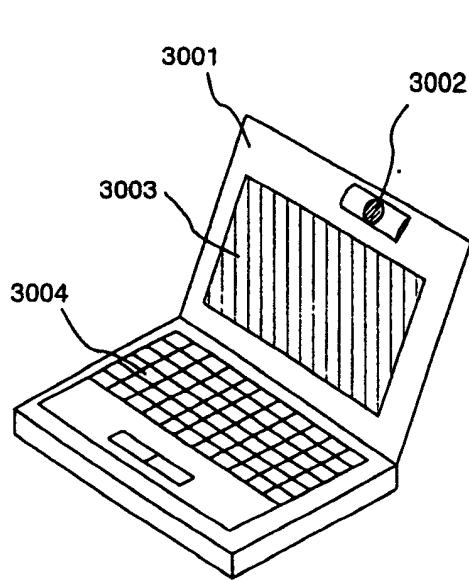


图 20A

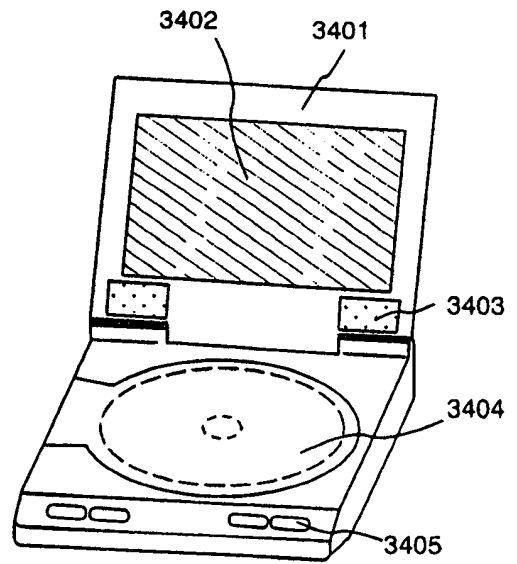


图 20B

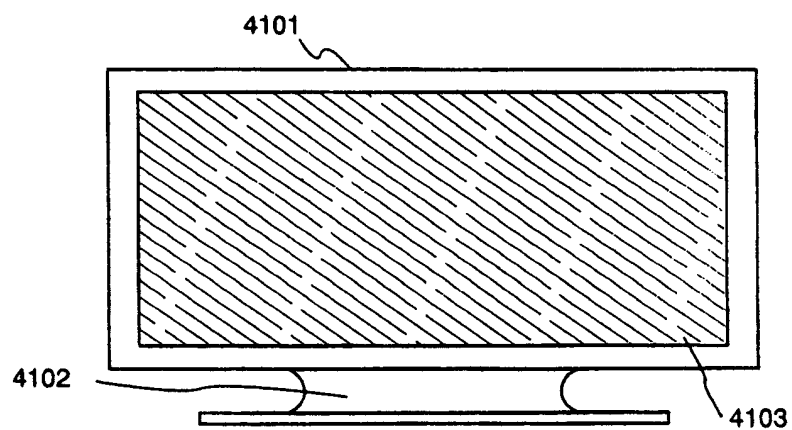


图 20C

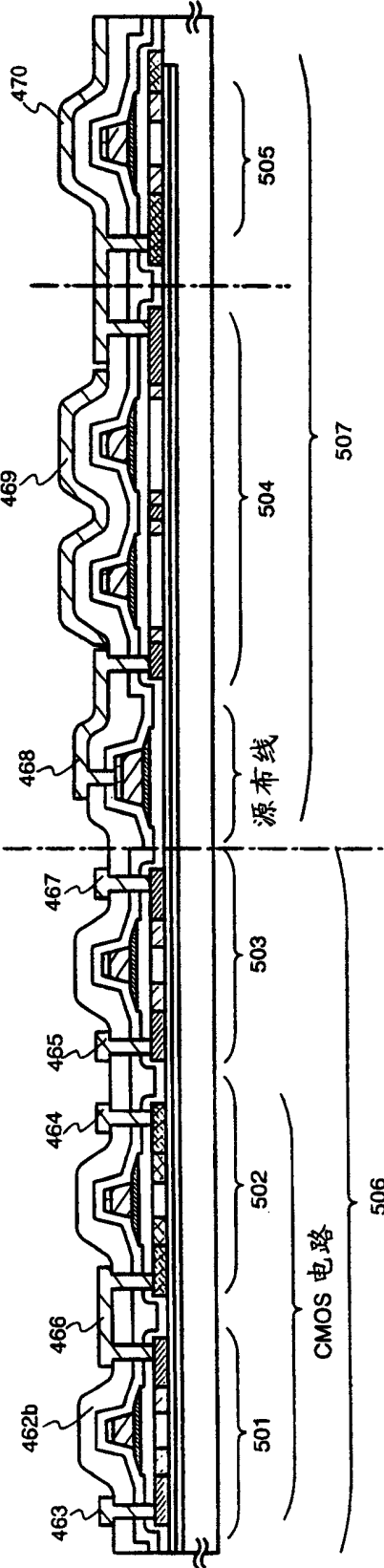


图 21

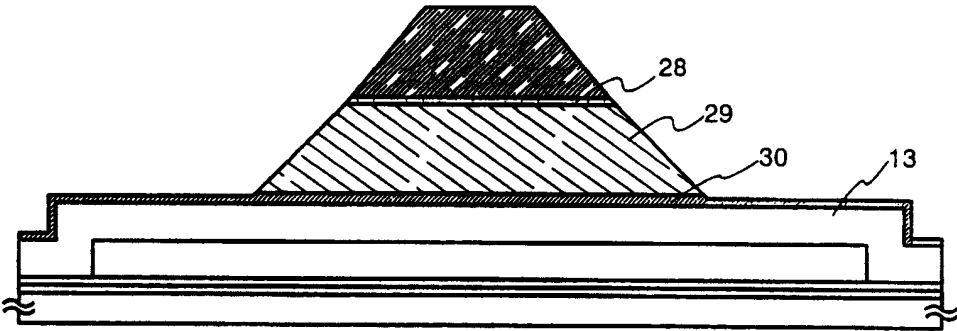


图 22