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I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willfully false statements and the like are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code.

In signing this declaration, I understand that the translation and this declaration may be filed as evidence in a contested case. I acknowledge that I may be subject to cross-examination within the United States.



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(54) Multilayer Wiring Structure for
Semiconductor Device

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unit wiring conductor layer is wider than the width
of the upper layer unit wiring conductor layer.

(5) A multilayer wiring structure for a
semiconductor device as described in any one of
claims 1 to 4, characterized in that at least a portion
of the thickness direction of the lower layer's unit
wiring conductor layer is embedded within the
lower layer's total thickness. 3. Detailed Description
of the Invention

This invention relates to a multilayer
wiring structure for semiconductor integrated
circuit devices (ICs), etc.

Multi-layer wiring is generally used to
increase the integration density of ICs and the like.
Figure 1 is a simplified plan view showing a two-
layer wiring example. Solid lines indicate first-layer
wiring, and dashed lines indicate second-layer
wiring. The first-layer wiring is used as lead-out
lines for individual transistors, diodes, resistors,
capacitors, etc., as well as for signal lines, power
lines, ground lines, etc. In the figure, (1) is the first-
layer power line, (2) is the first-layer signal line, and
(3) is the second-layer signal line. The terminals of
the first-layer signal line (2) are connected to the
second-layer signal line (3) by passing through the
interlayer insulating film (not shown) via through-
holes, as depicted in the figure.

Specification

1. Title of the Invention

Multi-Layer Wiring Structure for a Semi-
Floating Device

2. Scope of the Patent Claims

(1) A multilayer wiring structure for a
semiconductor device, characterized in that:

the lower layer wiring and the upper layer wiring
are superimposed via an interlayer insulating film;

the lower layer wiring is formed by multiple layers
of unit wiring conductive layers;

the side end faces of said unit wiring conductive
layers form a stepped configuration with steps
corresponding to the thickness of said unit wiring
conductive layers.

(2) A multilayer wiring structure for a
semiconductor device according to Claim 1,
characterized in that the width of the lower unit
wiring conductor layer is narrower than the width of
the upper unit wiring conductor layer.

(3) A multilayer wiring structure for a
semiconductor device according to Claim 1,
characterized in that the lower and upper unit wiring
conductor layers, having substantially the same
width, are stacked with a lateral offset relative to
each other.

(4) A multilayer wiring structure for a
semiconductor device as described in Claim 1,
characterized in that the width of the lower layer

By alternately connecting the first and second layer wiring, each element within the device is interconnected with power lines, electrode lead pads, etc., to form the desired circuit.

Figure 2 is a partial perspective view showing the structure of the two-layer wiring, depicting the first-layer power line (1) and second-layer signal line (3) provided on an insulating film (5), represented by an oxide layer covering the semiconductor substrate (4). The first-layer wiring (1) and second-layer wiring (3) are mutually separated by an interlayer insulating film (4) that blocks direct current between them. Generally, both types of wiring utilize metals such as Al, Al-81, Al-Si-Cu, primarily composed of aluminum, or even Au, which has lower wiring resistance. The width and thickness of the first-layer wiring (1) vary depending on the type of metal used. Particularly in devices like Bip LSI, which shorten propagation delay time by carrying high currents, minimizing voltage drop from the power supply—by considering the thickness, width, and distance from the power pad of the power line—is essential for proper device operation. For example, in gate arrays, a power line for approximately 2000 gates is about 9mm wide. To ensure smooth routing over the second layer without breaking the trace, a thickness of approximately 7000Å for the first layer trace (1) is most desirable. To reduce the electrical resistance of the first

layer trace (1), a trace width of about 600μm is required in the example above. Increasing this trace width introduces two significant drawbacks. One is the large capacitance between the trace and the substrate (4), and the capacitance between the first layer wiring (1) and the second layer wiring (3) increases. Particularly when the second layer wiring (3) is a signal line, the cross-sectional area between the first layer wiring (1) and the second layer wiring (3) becomes larger, causing signal delay due to increased wiring capacitance. For high-speed devices, this hinders performance improvements achieved through miniaturization of constituent elements. The second drawback is the increased chip area. Even as device integration advances and active regions, signal lines, etc., are miniaturized, higher integration density leads to greater power consumption and necessitates wider wiring widths. To illustrate with a concrete example, in the case of the aforementioned 2000-gate bipolar LSI, the main power supply lines feeding the internal gates are configured with two thick lines running in the X-direction through the center of the chip: one for the power supply and one for ground. Branching off from these are approximately 20 rows of branch power supply lines, each containing two lines running in the Y-direction, sufficient to supply power to about 100 gates.

Furthermore, buffer power lines are arranged around the periphery, encircling the internal gate. Therefore, the width required for other lines in the X direction is 3600 μm: 600 μm × 2 lines for the main power lines and 600 μm × 2 lines × 2 rows for the buffer power lines. Meanwhile, the Y-direction requires 40 branch power lines at 40 μm each and buffer power lines at 600 μm × 2 lines × 2 rows, totaling 1600 + 2400 = 4000 μm of power line width. Comparing this value to the chip area clearly reveals how extensive the wasted space is. Under a 2.54mm design rule, the configured LSI requires approximately 9.6mm² of area, with 38% in the X-direction and 42% in the Y-direction occupied solely by power supply wiring strips. As described above, in the conventional structure, the proportion of the chip area occupied by power supply wiring reaches 58%.

To address this issue, doubling the thickness of the first layer wiring while halving the wiring width is expected to yield significant improvement. Figure 3 shows a partial perspective view of the two-layer wiring structure in this case, and Figure 4 shows a partial cross-sectional view along line IVIN. As shown in Figure 4,

the interlayer film (6) handling the first layer wiring (1) with a large step height, and the second layer wiring (3) at the step edge, form a so-called negative slope. This results in poor step coverage, causing the interlayer film (6) and second-layer wiring (3) develop constrictions. This not only reduces film thickness and lowers insulation resistance but also increases wiring resistance. Consequently, it not only has the disadvantage of increasing device wiring delay (RXO) time but also, as shown in Figure 3, as the film thickness of the first-layer wiring (1) increases, the resist cannot adequately follow the step edge of the second layer wiring (3). This causes side etching on the second layer wiring (3), resulting in extremely poor device reliability.

This invention was made to solve the aforementioned problems. It achieves the desired objective by forming the step into a multi-step staircase configuration and reducing the width of the first layer wiring compared to conventional methods while maintaining the same wiring resistance. The invention is described below with reference to the drawings.

Figure 5 is a cross-sectional view showing a first embodiment of the present invention. By applying two-stage wiring to the first layer wiring (1) of a semiconductor device, as shown by (1a) and (1b), the step height is achieved by dividing the step height of the conventional wide-width wiring into two stages, thereby achieving the same low step height as conventionally. The second-layer wiring (3), which is provided transversely across this first-layer wiring (1), must cross over the two-step step height. However, the conventional method shown in Figure 3, which simply thickens the general wiring (1), results in a high step height as described above, causing a break in the second-layer wiring (3) would break. In contrast, this embodiment requires crossing a step of only about 7000Å, as indicated by the aforementioned data, ensuring sufficient resist coverage. One might consider thickening the resist to prevent breaks in the second-layer wiring (3). However, besides forming the second-layer source lines, narrow signal lines (line width ~2 μm, spacing ~2 μm) are required for the wiring pitch. Increasing the resist thickness would make the fine photolithography of these signal lines impossible. Therefore, a thin resist film (film thickness 7000~9000 Å) is required. In this example, compared to

conventional wide power lines, the first layer wiring (1) is formed by sequentially stacking a first power line (1a) that is slightly narrower than about half the width and a second power line (1b) that is slightly wider than the first. This achieves wiring resistance and step height nearly identical to conventional methods while halving the wiring width. Specifically, where the conventional method in Figure 2 required a first layer wiring (1) with a width of 600 μm, this implementation method finishes the first conductor (1a) with a width of 294 μm and places the second conductor (1b) on top of it with a width of 306 μm. (1b) to 306 μm, and the second conductor (1b) extends approximately 5 μm on each side of the first conductor (1a). Although not directly related to the present invention and therefore not illustrated, when simultaneously forming fine wiring connected via contact holes provided in the insulating film (5) to diffusion regions on the semiconductor substrate (4), it is preferable to form this fine wiring simultaneously with the second conductor (1b) rather than with the first conductor (1a). This is because if formed simultaneously with the first conductor (1a), it would be excessively affected by the etching during the patterning of the second conductor (1b).

Figures 6A to 6D are cross-sectional views showing the configuration of the first layer wiring (1) in the first to fourth embodiments of the present invention, respectively. Figure 6A is for the first embodiment described with reference to Figure 5, wherein the second conductor (1b) extends on both sides of the first conductor (1a). (1a) on both sides. Figure 6B shows the second embodiment where the first conductor (1a) extends beyond the second conductor (1b) on one side, while the second conductor extends beyond the first on the other side. Figure 6C shows the third embodiment where the first conductor (18) extends beyond the second conductor (16) on both sides. Figure 6D shows the first conductor (1a) embedded in the insulating film (5) and the second conductor (16) extending widely on both sides over it. In all cases, a small step difference can be maintained. Applying these embodiments enables the aforementioned gate array example to reduce its chip size from 9.6 mm × 9.6 mm to 7.8 mm × 7.5 mm, shrinking the chip area to 63.4%. It is well known that LSI yield improves as chip area decreases, making the ability to reduce the width of the power lines described above extremely beneficial. Figure 7 is a cross-sectional view showing the configuration of the first layer wiring (1) in the fifth embodiment of the present

invention. The first layer wiring (1) is formed by stacking a first conductor (1a), a second conductor (10), and a third conductor (1c). This allows the wiring width to be reduced to approximately one-third while maintaining a small step height. Figure 8 is an isometric view showing the configuration of the sixth embodiment of the present invention. This embodiment employs a three-layer wiring structure, wherein (7) is an interlayer insulating film formed on the second layer wiring (3), and (8) is the third layer wiring formed thereon. Both the first-layer wiring (1) and the second-layer wiring (3) are formed with the aforementioned two-step low step height, and the wiring width is approximately half that of conventional methods. Therefore, the second-layer wiring (3) and third-layer wiring (8) can be smoothly formed by traversing only the low step height without crossing a large step height. Since they are sufficiently covered by a thin resist film during photolithography, the formation of fine patterns is also possible simultaneously. The inter-line capacitance between the first layer wiring (1) and the second layer wiring (3) is reduced not only because the wiring width is narrower (approximately $1/2 \times 1/2 = 1/4$), but also because the interlayer insulation film at the step region does not become thinner, further decreasing the inter-wiring capacitance.

Although the third-layer wiring (8) was formed as a single-layer configuration, adopting a two-step structure here would also minimize the wiring clearance with the second-layer wiring (3).

Furthermore, this invention can naturally be applied to multilayer wiring structures with four or more layers. Additionally, each layer's wiring can be formed using a three-step structure equivalent to that shown in Figure 7.

Moreover, the multi-step structure's intermediate layers used in this invention can be applied to pads such as input/output pads and power pads. Generally, pad wiring with greater film thickness reduces shock to the underlying insulating film during bonding. Therefore, using the conductors of the above multi-step structure eliminates the need to unnecessarily thicken the underlying insulating film to prevent leakage due to damage, allowing the underlying insulating film thickness to be reduced.

As detailed above, in a configuration with multiple wiring layers separated by interlayer insulation films, the wiring thickness is increased and the pitch width is reduced as a multi-layer structure while maintaining a small pitch and without reducing the effective cross-sectional area of the bottom layer wiring. This reduces the chip area occupied by the wiring. Furthermore, not only is the coverage of the interlayer insulation film ensured, but the top layer wiring also allows for easy microfabrication without creating

narrow sections or breakage points. and broken filaments in the upper layer wiring, enabling easy microfabrication. This results in a semiconductor device with a small chip size, low cost, and high reliability.

4. Brief Description of the Drawings

Figure 1 is a simplified plan view showing a two-layer wiring structure. Figure 2 is an isometric view showing an example of a conventional two-layer wiring structure. Figure 3 is an isometric view showing another example of a conventional two-layer wiring structure. Figure 4 is a partial cross-sectional view along line N-N. Figure 5 is a cross-sectional view showing the first embodiment of the present invention. Figures 6a, b, c, and d are cross-sectional views showing the first, second, and fourth embodiments of the present invention, Fig. 7 is a cross-sectional view showing the configuration of the first layer wiring in the fifth embodiment of the present invention, and Fig. 8 is an isometric view showing the sixth embodiment of the present invention.

In the figures: (1) is the first layer wiring, (1a), (1b), (1c) is a unit wiring idle layer, (3) is the second layer wiring, (4) is the semiconductor substrate, (5) is the dielectric layer, (6) and (7) are interlayer insulating films, and (8) is the third layer wiring.

Note that the same reference numerals indicate the same or corresponding parts.

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Figure 1

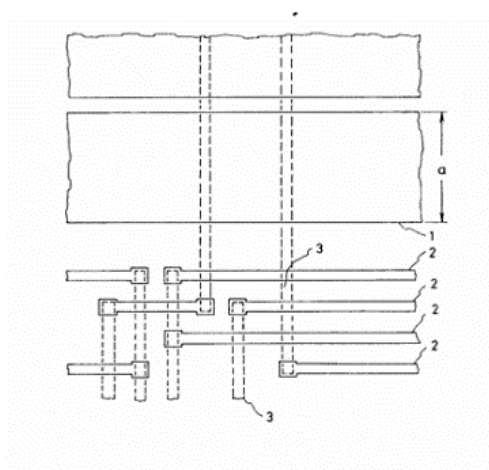


Figure 4

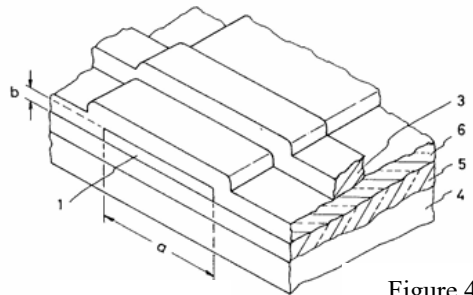


Figure 2

Figure 5

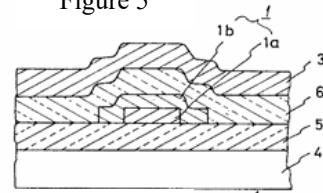


Figure 6

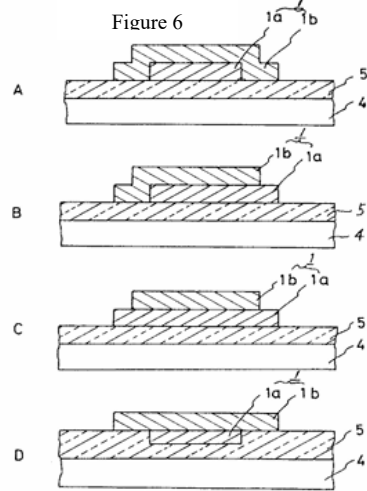


Figure 3

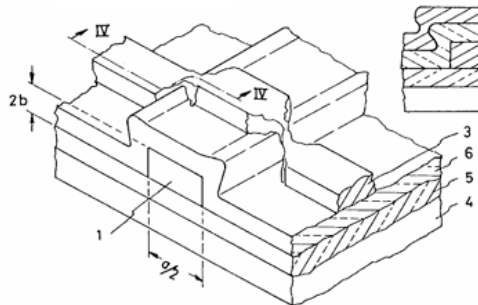


Figure 4

Figure 7

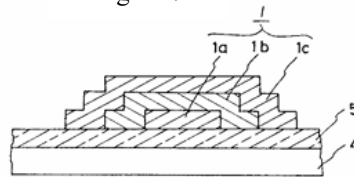
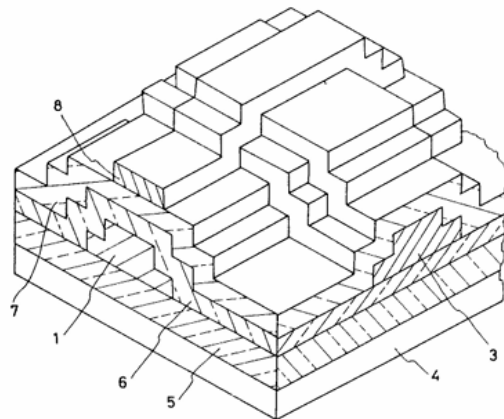


Figure 8



⑫ 公開特許公報 (A)

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⑤④半導体装置の多層配線構造

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明 細 書

1. 発明の名称

半導体装置の多層配線構造

2. 特許請求の範囲

(1) 下層配線と上層配線とが層間絶縁膜を介して重畳してなる半導体装置の多層配線において、上記下層配線を複数段の単位配線導体層で形成し、その側端面が上記単位配線導体層の厚さをステップとする階段状となるようにしたことを特徴とする半導体装置の多層配線構造。

(2) 下段の単位配線導体層の幅を上段の単位配線導体層の幅より狭くしたことを特徴とする特許請求の範囲第1項記載の半導体装置の多層配線構造。

(3) ほぼ同一幅の下段および上段の単位配線導体層を互いに幅方向にずらして重ねたことを特徴とする特許請求の範囲第1項記載の半導体装置の多層配線構造。

(4) 下段の単位配線導体層の幅を上段の単位配線導体層の幅より広くしたことを特徴とする特許

請求の範囲第1項記載の半導体装置の多層配線構造。

(6) 下層の単位配線導体層の厚さ方向の少なくとも一部をその下層の絶縁層内に埋め込んだことを特徴とする特許請求の範囲第1項ないし第4項のいずれかに記載の半導体装置の多層配線構造。

3. 発明の詳細な説明

この発明は半導体集積回路装置(IC)などにおける多層配線構造に関するものである。

IC等の集積度の向上には一般に多層配線が用いられる。第1図はその一例として2層配線を示す簡略平面図で、実線は一層目配線、破線は二層目の配線を示し、一層目の配線は個々のトランジスタ、ダイオード、抵抗、キャパシタ等の引出し線として利用される他、信号ライン、電源ライン、接地ライン等として用いられる。図において、(1)は一層目電源ライン、(2)は一層目信号ライン、(3)は二層目信号ラインで、一層目信号ライン(2)の各終端は同図に示す様に層間絶縁膜(図示せず)に開孔(スルーホール)し、二層目信号ライン(3)

に接続される。一、二層目配線を交互に継ぎ合わせることでデバイス中の各素子と電源ライン、電極引出し用パッド等とを相互に接続させ所望の回路を構成する。

第2図は2層配線の構造を示す部分斜視図で、半導体基板(4)を覆う酸化膜等で代表される絶縁膜(5)の上に設けられた一層目電源ライン(1)および二層目信号ライン(3)を示す。一層目配線(1)、二層目配線(3)間はこれらが直流的に遮断される層間絶縁膜(4)で相互に分離されている。一般に両配線はAlを主とするAl、Al-Si、Al-Si-Cuやさらに配線抵抗の低いAu等が利用される。一層目配線(1)の幅aおよび厚さbは使用する金属の種類で異なる。特に電流を多く流すことで伝播遅延時間を短くしているバイポーラ(Bip)LSI等では、電源ラインの厚さ、幅、給電用パッドからの距離を考慮して電源からの電圧ドロップを極力少なくすることがデバイスを正常に働かせる上で不可欠である。例えばゲートアレイ等の場合2000ゲート程度では電源ラインが9mm程度となる。二層目の配線を断

線させることなく、スムーズに乗り越えさせるために一層目配線(1)の厚さは7000Å程度が最も望ましい。一層目配線(1)の電気抵抗を下げるため、例えば上述の例では600μm程度の配線幅が要求される。この配線幅が広くなることは二つの大きな欠点を生じる。一つは配線と基板(4)、一層目配線(1)と二層目配線(3)との間の容量が大きい点である。特に二層目配線(3)が信号ラインの時一層目配線(1)、二層目配線(3)間の交叉面積が広くなり、配線容量の増加による信号の遅延を引き起す。このことは高速デバイスにとつて、構成エレメントの微細化による高性能化を阻む原因となる。第二の欠点はチップ面積が大きくなつてしまい事であり、デバイスの集積化が進み活性領域、信号ライン等が微細化されたとしても、集積度が上がることで消費電力も大きくなり、さらに太い配線幅を必要とすることになる。具体例で示せば前記2000ゲートバイポーラLSIの場合内部ゲートに供給する主電源ラインはチップの中央をX方向に電源ラインとグラウンドラインとの2本の太い配線を有し、

これに約100ゲート分の枝電源ラインを2本づつY方向に20列並べて構成される。さらに、周辺にはバッファ電源ラインが内部ゲートを取り囲む様に並ぶ。従つてX方向の電源ラインに要する幅は主電源ラインとして(600μm×2本)、バッファ電源ラインとして(600μm×2本×2列)となり合計3600μmもの幅が必要となる。一方、Y方向は40μmの枝電源ラインが40本とバッファ電源ラインが600μm×2本×2列合計1600+2400=4000μmもの電源ライン幅が必要となる。この値をチップ面積と比較すると無駄なスペースがいかに広いものかが明らかとなる。2.5μmのデザインルールで、構成したLSIは約9.6mm²の面積が必要であり、X方向の38%、Y方向の42%は電源配線帯のみに占有されている。以上の様に従来の構造では、電源配線のチップ全体に占める面積の割合は58%に達する。

この問題を解決する手法として一層目配線厚さを2倍にして配線幅を半分にするれば著しい改善効果が期待される。第3図はこの場合の2層配線の

構造を示す部分斜視図、第4図はそのⅣ-Ⅳ線での部分断面図で、第4図に示すように段差の大きい一層目配線(1)を覆う層間膜(6)や、二層目配線(3)が段差エッジでいわゆるネガティブ・スロープとなり、ステップカバレッジが悪くなり層間膜(6)および二層目配線(3)にくびれが生じ膜厚が薄くなり、絶縁抵抗が低くなるばかりでなく、配線抵抗が高くなると云う問題が生じデバイスの配線による遅延(R×C)時間をより大きくすると云う欠点があるのみでなく、第3図に示すように一層目配線(1)の膜厚増加に伴いレジストが二層目配線(3)を段差部で充分覆いきれないので、二層目配線(3)にサイドエッチングを生じると云う問題が発生し、デバイスとして信頼性の極めて悪いものとなる欠点があつた。

この発明は上述の問題を解決するために成されたもので段差を複数段の階段状とし、かつ配線抵抗を同一にして一層目の配線幅を従来より縮減して所期の目的を達成せんとするものである。以下図面に示つてこの発明を説明する。

第5図はこの発明の第1の実施例を示す断面図で、半導体装置の一層目配線(1)を(1a)および(1b)で示す二段階の配線を施すことにより段差は従来の広い幅の配線の段差を2段階に設けることにより従来と同一の低段差を図るものである。この一層目配線(1)を横断するように設けられた二層目配線(3)によつて2段の段差を越えることになるが、単に一層目配線(1)を厚くする従来の第3図の方式では前述のように高段差となり二層目配線(3)に断線を生じていたのに対して、この実施例では、前述のデータでいえば、約7000Å程度の段差を越えればよいことになり、レジストのカバレッジは十分保証される。二層目配線(3)の断線を防ぐにはレジストを厚くすれば良いとの考えが浮かぶであろうが、二層目の電源ライン形成の他に配線ピッチの狭い信号ライン(線幅2μm, 間隔2μm程度)が要求されるので、レジスト厚さを厚くするとこの信号ラインの微細な写真製版が不可能となる。従つて、薄いレジスト膜(膜厚7000~9000Å)が要求される。この実施例では従来の広い電源

ラインと比較して、約1/2よりやや狭い第1の導体(1a)とこれよりやや広い第2の導体(1b)とを順次重ねて一層目の配線(1)を形成することにより従来と配線抵抗、段差をほぼ同一にしかつ配線幅を1/2にすることができる。すなわち、第2図の従来の方式で600μm幅の一層目配線(1)を要した場合には、この実施例の方式では第1の導体(1a)を294μm幅に仕上げ、その上に第2の導体(1b)を306μmとし、第1の導体(1a)の両側に約5μmづつ第2の導体(1b)が広がるようにする。なお、この発明とは直接関係ないので、図示しないが、半導体基板(4)の拡散領域などへ絶縁膜(5)に設けたコンタクトホールを介して接続する細い配線を同時に形成するときには、この細い配線は第1の導体(1a)と同時にではなく、第2の導体(1b)と同時に形成した方がよい。これは、第1の導体(1a)と同時に形成しておく、第2の導体(1b)のパターニング時のエッチングで余分な影響を受けるからである。

第6図A~Dはそれぞれこの発明の第1~第4

の実施例における一層目配線(1)の形態を示す断面図で、第6図Aは第5図について説明した第1の実施例のもので、第2の導体(1b)が第1の導体(1a)の両側に延びている場合、第6図Bの第2の実施例は第1の導体(1a)と第2の導体(1b)とが片側では前者が後者より延び、他の側では後者が前者より延びている場合、第6図Cの第3の実施例は第1の導体(1a)が第2の導体(1b)より幅広く両側に延びている場合、第6図Dは第1の導体(1a)が絶縁膜(5)に埋め込まれ、第2の導体(1b)かその上に幅広く両側に延びている場合を示し、いずれも一段の段差を小さく保持できる。

これらの実施例を適用した場合、前述のゲートアレイの例では9.6mm×9.6mmのチップサイズを7.8×7.5mmに縮小することが可能で、チップ面積は63.4%に縮小される。LSIの歩留りはチップ面積が小さくなる程有利であることはよく知られており、上述の電源ラインの幅の縮小ができることは極めて有益である。

第7図はこの発明の第5の実施例における一層

目配線(1)の形態を示す断面図で、一層目配線(1)を第1の導体(1a)、第2の導体(1b)および第3の導体(1c)を重ねて形成したもので、1段の段差を小さく保持しつつ配線幅を約1/3にできる。

第8図はこの発明の第6の実施例の構成を示す斜視図で、この実施例は三層配線構造のもので、(7)は二層目配線(3)の上に形成された層間絶縁膜、(8)はその上に形成された三層目配線である。一層目配線(1)および二層目配線(3)がともに前述の2ステップの低段差で形成されており配線幅は従来のほぼ1/2になっている。従つて、二層目配線(3)および三層目配線(8)は大きな段差を横切ることなく、低段差を横切のみでスムーズに行うことができ、写真製版時に薄いレジスト膜で十分カバレッジされるので、同時に微細パターンの形成も可能となる。一層目配線(1)と二層目配線(3)との線間容量は配線幅が狭くなつた分だけ小さく(約1/2×1/2=1/4に)なるのみでなく、段差部の層間絶縁膜が薄くなることもないので配線間容量は一層小さくなる。三層目配線(8)を単板形状としたが、これも2ステ

ツブ構造にすれば二層目配線(3)との配線間容量も小さくできる。

更に、四層以上の多層配線構造にも、当然この発明は適用できる。また、各層配線を第7図に示したと同等な3ステップ構造にすることもできる。

なお、この発明に用いた複数ステップ構造の導体層は入出力パット、電源パットなどのパットに応用できる。一般にパット配線は膜厚が大きい程ボンディング時の下地絶縁膜へのショックが小さいので、上記複数ステップ構造の導体層を用いれば、下地絶縁膜を必要以上に厚くして破損によるリークの発生に備える要はなく、下地絶縁膜厚を薄くできる。

以上詳述したように層間絶縁膜を介して複数層の配線を有する構成において、下層の配線を有効断面積を減えることなく、一段の段差を小さく保持したまま複数段構造として配線厚さを大きく配線幅を小さくしたので、配線の占めるチップ面積を小さくでき、しかも層間絶縁膜のカバレッジは

勿論、上層の配線にも狭窄部、断線部を生じることなく微細加工が容易にできるのでチップサイズの小さく安価なしかも信頼性の高い半導体装置が得られる。

4. 図面の簡単な説明

第1図は2層配線を示す簡略平面図、第2図は従来の2層配線の一例を示す斜視図、第3図は従来の2層配線の他の例を示す斜視図、第4図はそのⅣ-Ⅳ線での部分断面図、第5図はこの発明の第1の実施例を示す断面図、第6図A、B、C、Dはそれぞれこの発明の第1、第2、第3、第4の実施例における一層目配線の構成を示す断面図、第7図はこの発明の第5の実施例における一層目配線の構成を示す断面図、第8図はこの発明の第6の実施例を示す斜視図である。

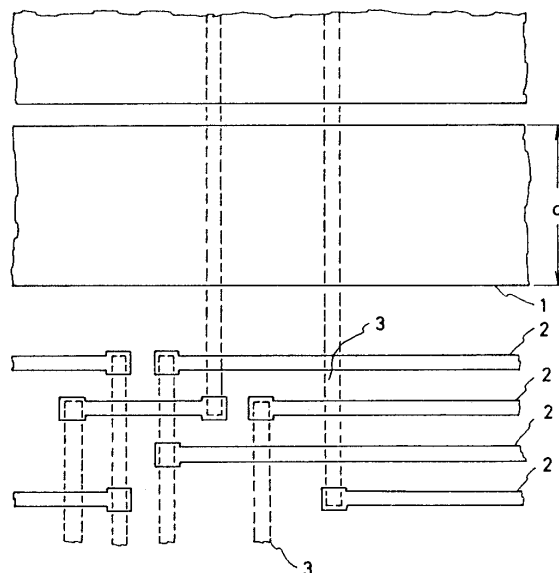
図において、(1)は一層目配線、(1a)、(1b)、(1c)は単位配線導体層、(3)は二層目配線、(4)は半導体基板、(5)は絶縁層、(6)、(7)は層間絶縁膜、(8)は三層目配線である。

なお、図中同一符号は同一または相当部分を示

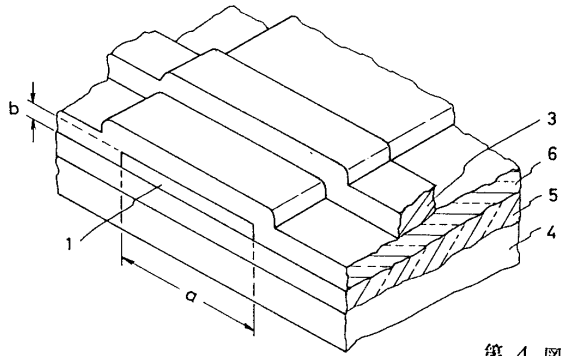
す。

代理人 葛 野 信 一(外1名)

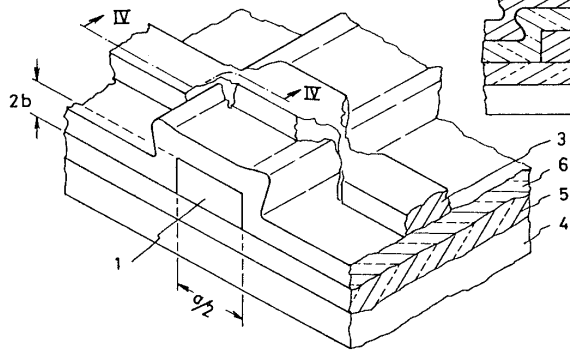
第1図



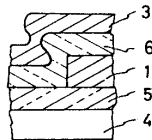
第 2 図



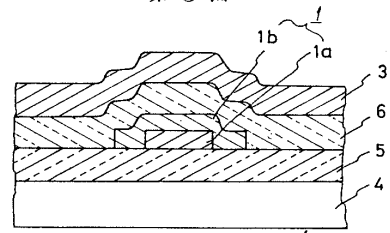
第 3 図



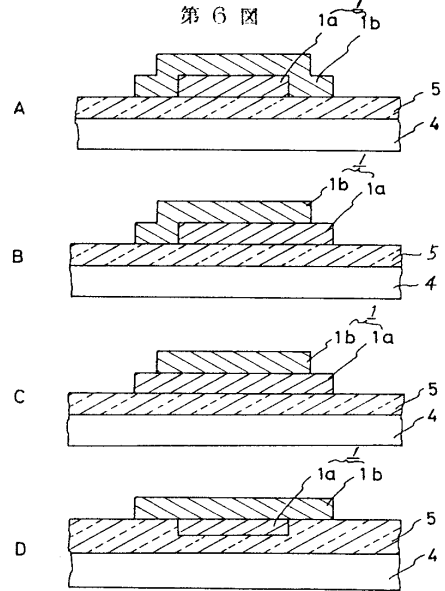
第 4 図



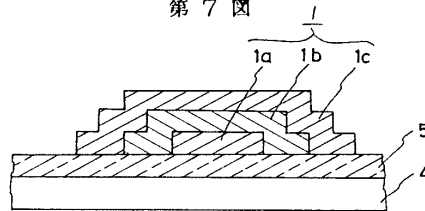
第 5 図



第 6 図



第 7 図



第 8 図

