

Flexible Electronics: Materials and Applications

Electronic Materials: Science and Technology

Series Editor: Harry L. Tuller
Professor of Materials Science and Engineering
Massachusetts Institute of Technology
Cambridge, Massachusetts
tuller@mit.edu

Flexible Electronics: Materials and Applications

William S. Wong and Alberto Salleo, eds.

ISBN 978-0-387-74362-2, 2009

Nanocomposites: Ionic Conducting Materials and Structural Spectroscopies

Philippe Knauth and Joop Schoonman, eds.

ISBN 978-0-387-33202-4, 2008

Electroceramic-Based MEMS: Fabrication-Technology and Applications

N. Setter

ISBN 978-0-387-23310-9, 2005

Nanostructured Materials: Selected Synthesis Methods, Properties and Applications

Philippe Knauth and Joop Schoonman, eds.

ISBN 978-1-4020-7241-3, 2002

Nanocrystalline Metals and Oxides: Selected Properties and Applications

Philippe Knauth and Joop Schoonman, eds.

ISBN 978-0-7923-7627-9, 2002

High-Temperature Superconductors: Materials, Properties, and Applications

Rainer Wesche

ISBN 978-0-7923-8386-4, 1999

Amorphous and Microcrystalline Silicon Solar Cells: Modeling, Materials and Device Technology

Ruud E.I. Schropp and Miro Zeman, eds.

ISBN 978-0-7923-8317-8, 1998

Microactuators: Electrical, Magnetic, Thermal, Optical, Mechanical, Chemical and Smart Structures

Massood Tabib-Azar,

ISBN 978-0-7923-8089-4, 1998

Thin Film Ferroelectric Materials and Devices

R. Ramesh, ed.

ISBN 978-0-7923-9993-3, 1997

Wide-Gap Luminescent Materials: Theory and Applications

Stanley R. Rotman, ed.

ISBN 978-0-7923-9837-0, 1997

Piezoelectric Actuators and Ultrasonic Motors

Kenji Uchino

ISBN 978-0-7923-9811-0, 1996

William S. Wong · Alberto Salleo
Editors

Flexible Electronics: Materials and Applications

 Springer

Editors

William S. Wong
Palo Alto Research Center
3333 Coyote Hill Road
Palo Alto, CA 94304
ws@parc.com

Alberto Salleo
Stanford University
Department of Materials Science &
Engineering
Stanford, CA 94305-2205
asalleo@stanford.edu

ISBN 978-0-387-74362-2 e-ISBN 978-0-387-74363-9
DOI 10.1007/978-0-387-74363-9

Library of Congress Control Number: PCN applied for

© Springer Science+Business Media, LLC 2009

All rights reserved. This work may not be translated or copied in whole or in part without the written permission of the publisher (Springer Science+Business Media, LLC, 233 Spring Street, New York, NY 10013, USA), except for brief excerpts in connection with reviews or scholarly analysis. Use in connection with any form of information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed is forbidden.

The use in this publication of trade names, trademarks, service marks and similar terms, even if they are not identified as such, is not to be taken as an expression of opinion as to whether or not they are subject to proprietary rights.

Printed on acid-free paper.

springer.com

Contents

1	Overview of Flexible Electronics Technology	1
	I-Chun Cheng and Sigurd Wagner	
1.1	History of Flexible Electronics	1
1.2	Materials for Flexible Electronics	3
1.2.1	Degrees of Flexibility	3
1.2.2	Substrates	5
1.2.3	Backplane Electronics	8
1.2.4	Frontplane Technologies	12
1.2.5	Encapsulation	16
1.3	Fabrication Technology for Flexible Electronics	18
1.3.1	Fabrication on Sheets by Batch Processing	18
1.3.2	Fabrication on Web by Roll-to-Roll Processing	19
1.3.3	Additive Printing	20
1.4	Outlook	20
	References	20
2	Mechanical Theory of the Film-on-Substrate-Foil Structure: Curvature and Overlay Alignment in Amorphous Silicon Thin-Film Devices Fabricated on Free-Standing Foil Substrates	29
	Helena Gleskova, I-Chun Cheng, Sigurd Wagner, and Zhigang Suo	
2.1	Introduction	29
2.2	Theory	32
2.2.1	The Built-in Strain ϵ_{bi}	35
2.3	Applications	36
2.3.1	Strain in the Substrate, $\epsilon_s(T_d)$, and the Film, $\epsilon_f(T_d)$, at the Deposition Temperature T_d	36
2.3.2	Strain in the Substrate, $\epsilon_s(T_r)$, and the Film, $\epsilon_f(T_r)$, at Room Temperature T_r	38
2.3.3	Radius of Curvature R of the Workpiece	42
2.3.4	Strain of the Substrate and the Curvature of the Workpiece for a Three-Layer Structure	46
2.3.5	Experimental Results for a-Si:H TFTs Fabricated on Kapton	47

2.4	Conclusions	50
	References	50
3	Low-temperature Amorphous and Nanocrystalline Silicon	
	Materials and Thin-film Transistors	53
	Andrei Sazonov, Denis Striakhilev, and Arokia Nathan	
3.1	Introduction	53
3.2	Low-temperature Amorphous and Nanocrystalline Silicon Materials	55
3.2.1	Fundamental Issues for Low-temperature Processing	55
3.2.2	Low-temperature Amorphous Silicon	56
3.2.3	Low-temperature Nanocrystalline Silicon	56
3.3	Low-temperature Dielectrics	57
3.3.1	Characteristics of Low-temperature Dielectric Thin-film Deposition	57
3.3.2	Low-temperature Silicon Nitride Characteristics	57
3.3.3	Low-temperature Silicon Oxide Characteristics	58
3.4	Low-temperature Thin-film Transistor Devices	59
3.4.1	Device Structures and Materials Processing	60
3.4.2	Low-temperature a-Si:H Thin-Film Transistor Device Performance	61
3.4.3	Contacts to a-Si:H Thin-film Transistors	62
3.4.4	Low-temperature Doped nc-Si Contacts	64
3.4.5	Low-temperature nc-Si TFTs	66
3.5	Device Stability	67
3.6	Conclusions and Future Prospective	70
	References	70
4	Amorphous Silicon: Flexible Backplane and Display Application	75
	Kalluri R. Sarma	
4.1	Introduction	75
4.2	Enabling Technologies for Flexible Backplanes and Displays	76
4.2.1	Flexible Substrate Technologies	76
4.2.2	TFT Technologies for Flexible Backplanes	82
4.2.3	Display Media for Flexible Displays (LCD, Reflective-EP, OLED)	89
4.2.4	Barrier Layers	90
4.3	Flexible Active Matrix Backplane Requirements for OLED Displays	91
4.3.1	Active Matrix Addressing	92
4.4	Flexible AMOLED Displays Using a-Si TFT Backplanes	95
4.4.1	Backplane Fabrication Using PEN Plastic Substrates	95
4.4.2	Flexible OLED Display Fabrication	98
4.4.3	Flexible AMOLED Display Fabrication with Thin-film Encapsulation	100

4.5	Flexible Electrophoretic Displays Fabricated using a-Si TFT Backplanes	102
4.6	Outlook for Low-Temperature a-Si TFT for Flexible Electronics Manufacturing	102
	References	105
5	Flexible Transition Metal Oxide Electronics and Imprint Lithography	107
	Warren B. Jackson	
5.1	Introduction	107
5.2	Previous Work	108
5.3	Properties of Transistor Materials	113
	5.3.1 Semiconductors	113
	5.3.2 Dielectrics	115
	5.3.3 Contact Materials	116
5.4	Device Structures	117
5.5	Fabrication on Flexible Substrates	119
	5.5.1 Imprint Lithography	120
	5.5.2 Self-Aligned Imprint Lithography	122
	5.5.3 SAIL Transistor Results	126
	5.5.4 Summary of Imprint Lithography	127
5.6	Flexible TMO Device Results	128
5.7	Future Problems and Areas of Research	133
	5.7.1 Carrier Density Control	134
	5.7.2 Low-Temperature Dielectrics	135
	5.7.3 Etching of TMO Materials	135
	5.7.4 P-type TMO	136
	5.7.5 Stability	136
	5.7.6 Flexure and Adhesion of TMO	137
	5.7.7 Flexible Fabrication Method Yields	137
5.8	Summary	138
	References	139
6	Materials and Novel Patterning Methods for Flexible Electronics	143
	William S. Wong, Michael L. Chabinyc, Tse-Nga Ng, and Alberto Salleo	
6.1	Introduction	143
6.2	Materials Considerations for Flexible Electronics	145
	6.2.1 Overview	145
	6.2.2 Inorganic Semiconductors and Dielectrics	145
	6.2.3 Organic Semiconductors and Dielectrics	146
	6.2.4 Conductors	149
6.3	Print-Processing Options for Device Fabrication	150
	6.3.1 Overview	150

6.3.2	Control of Feature Sizes of Jet-Printed Liquids	151
6.3.3	Jet-Printing for Etch-Mask Patterning	153
6.3.4	Methods for Minimizing Feature Size	154
6.3.5	Printing Active Materials	156
6.4	Performance and Characterization of Electronic Devices	157
6.4.1	Overview	157
6.4.2	Bias Stress in Organic Thin-Film Transistors	158
6.4.3	Nonideal Scaling of Short-Channel Organic TFTs	163
6.4.4	Low-Temperature a-Si:H TFT Device Stability	165
6.4.5	Low-temperature a-Si:H p-i-n Devices	167
6.5	Printed Flexible Electronics	170
6.5.1	Overview	170
6.5.2	Digital Lithography for Flexible Image Sensor Arrays	170
6.5.3	Printed Organic Backplanes	172
6.6	Conclusions and Future Prospects	176
	References	176
7	Sheet-Type Sensors and Actuators	183
	Takao Someya	
7.1	Introduction	183
7.2	Sheet-type Image Scanners	184
7.2.1	Imaging Methods	185
7.2.2	Device Structure and Manufacturing Process	186
7.2.3	Electronic Performance of Organic Photodiodes	190
7.2.4	Organic Transistors	191
7.2.5	Photosensor Cells	193
7.2.6	Issues Related to Device Processes: Pixel Stability and Resolution	195
7.2.7	A Hierarchal Approach for Slow Organic Circuits	196
7.2.8	The Double-Wordline and Double-Bitline Structure	196
7.2.9	A New Dynamic Second-Wordline Decoder	199
7.2.10	Higher Speed Operation with Lower Power Consumption	199
7.2.11	New Applications and Future Prospects	200
7.3	Sheet-Type Braille Displays	201
7.3.1	Manufacturing Process	201
7.3.2	Electronic Performance of Braille Cells	204
7.3.3	Organic Transistor-based SRAM	210
7.3.4	Reading Tests	211
7.3.5	Future Prospects	212
7.4	Summary	212
	References	213

8 Organic and Polymeric TFTs for Flexible Displays and Circuits	215
Michael G. Kane	
8.1 Introduction	215
8.2 Important Organic TFT Parameters for Electronic Systems	216
8.2.1 Field-Effect Mobility	216
8.2.2 Threshold Voltage	219
8.2.3 Subthreshold Swing	220
8.2.4 Leakage Currents	222
8.2.5 Contact Resistance	222
8.2.6 Capacitances and Frequency Response	223
8.2.7 TFT Nonuniformity	225
8.2.8 Bias-Stress Instability and Hysteresis	225
8.3 Active Matrix Displays	227
8.3.1 Introduction	227
8.3.2 Liquid Crystal and Electrophoretic Displays	228
8.4 Active Matrix OLED Displays	236
8.4.1 Introduction	236
8.5 Using Organic TFTs for Electronic Circuits	242
8.5.1 Thin-Film Transistor Circuits	242
8.5.2 Frequency Limitations of OTFTs	246
8.5.3 Integrated Display Drivers	247
8.5.4 Radio Frequency Identification Tags	248
8.6 Conclusion	256
References	256
 9 Semiconducting Polythiophenes for Field-Effect Transistor Devices in Flexible Electronics: Synthesis and Structure Property Relationships	 261
Martin Heeney and Iain McCulloch	
9.1 Introduction	261
9.2 Polymerization of Thiophene Monomers	264
9.2.1 General Considerations	264
9.2.2 Synthetic Routes for the Preparation of Thiophene Polymers	264
9.3 Poly(3-Alkylthiophenes)	273
9.3.1 Electrical Properties	275
9.3.2 Thin-film Device Processing and Morphology	276
9.3.3 Doping and Oxidative Stability	277
9.4 Polythiophene Structural Analogues	279
9.5 Thienothiophene Polymers	286
9.5.1 Poly(Thieno(2,3-b)Thiophenes)	286
9.5.2 Poly(Thieno(3,2-b)Thiophenes)	288
9.6 Summary	292
References	293

10	Solution Cast Films of Carbon Nanotubes for Transparent Conductors and Thin Film Transistors	297
	David Hecht and George Grüner	
10.1	Introduction: Nanoscale Carbon for Electronics, the Value Proposition	297
10.2	Carbon NT Film Properties	298
10.2.1	Carbon Nanotubes: The Building Blocks	298
10.2.2	Carbon Nanotube Network as an Electronic Material	298
10.2.3	Electrical and Optical Properties of NT Films	300
10.2.4	Doping and Chemical Functionalization	304
10.3	Fabrication Technologies	305
10.3.1	Solubilization	306
10.3.2	Deposition	306
10.4	Carbon NT Films as Conducting and Optically Transparent Material	309
10.4.1	Network Properties: Sheet Conductance and Optical Transparency	309
10.4.2	Applications: ITO Replacement	312
10.4.3	Challenges and the Path Forward	312
10.5	TFTs with Carbon Nanotube Conducting Channels	313
10.5.1	Device Characteristics	314
10.5.2	Device Parameters	316
10.5.3	Challenges and the Path Forward	323
10.6	Conclusions	324
	References	325
11	Physics and Materials Issues of Organic Photovoltaics	329
	Shawn R. Scully and Michael D. McGehee	
11.1	Introduction	329
11.2	Basic Operation	329
11.2.1	Photocurrent	331
11.2.2	Dark Current	331
11.3	Organic and Hybrid Solar Cell Architectures	332
11.4	Materials	334
11.5	Light Absorption	334
11.6	Exciton Harvesting	338
11.6.1	Effects of Disorder	340
11.6.2	Extrinsic Defects	344
11.6.3	Measuring Exciton Harvesting	344
11.6.4	Approaches to Overcome Small Diffusion Lengths	347
11.7	Exciton Dissociation	349
11.8	Dissociating Geminate Pairs	351
11.9	Heterojunction Energy Offsets	355
11.10	Charge Transport and Recombination	357
11.10.1	Diffusion-Limited Recombination	359

11.10.2 Interface-Limited (Back Transfer Limited)	
Recombination	360
11.10.3 Measurements Relevant for Extracting Charge	363
11.11 Nanostructures	364
11.12 Efficiency Limits and Outlook	367
References	368
12 Bulk Heterojunction Solar Cells for Large-Area PV Fabrication on Flexible Substrates	373
C. Waldauf, G. Dennler, P. Schilinsky, and C. J. Brabec	
12.1 Introduction and Motivation	373
12.1.1 Photovoltaics	373
12.1.2 Technology Overview	374
12.1.3 Motivation for Large-Area, Solution-Processable Photovoltaics	375
12.2 The Concept of Bulk Heterojunction Solar Cells	377
12.2.1 Basics of Organic Solar Cell Materials	377
12.2.2 Fundamentals of Photovoltaics	378
12.2.3 Understanding and Optimization of BHJ Composites	385
12.3 Challenges for Large-Area Processing	401
12.3.1 Production Scheme	401
12.3.2 Encapsulation of Flexible Solar Cells	404
12.4 Conclusions	408
References	409
13 Substrates and Thin-Film Barrier Technology for Flexible Electronics	413
Ahmet Gün Erhat, Min Yan, and Anil R. Duggal	
13.1 Introduction	413
13.2 Barrier Requirements	414
13.2.1 Generic Requirements	416
13.2.2 Substrate-Specific Requirements	417
13.3 Thin-Film Barrier Technology	419
13.3.1 Historical Background	419
13.3.2 Permeation Measurement Techniques	420
13.3.3 Permeation Through Thin-Film Barriers	426
13.4 Barrier-Device Integration	437
13.4.1 Substrate and Barrier Compatibility with OLEDs	437
13.4.2 Thin-Film Encapsulation	440
13.5 Concluding Remarks	442
References	442
Index	451

Contributors

C. J. Brabec Konarka Technologies GmbH, Altenbergerstrasse 69, A-4040 Linz, Austria, cbrabec@konarka.com

Michael L. Chabinyc Materials Department, University of California, Santa Barbara, USA, mchabinyc@engineering.ucsb.edu

I-Chun Cheng Department of Electrical Engineering and Graduate Institute of Photonics and Optoelectronics, National Taiwan University, Taipei, 10617 Taiwan, ichuncheng@cc.ee.ntu.edu.tw

G. Dennler Konarka Technologies GmbH, Altenbergerstrasse 69, A-4040 Linz, Austria

Anil R. Duggal General Electric Global Research Center, 1 Research Circle, KWD 272, Niskayuna, NY 12309, USA, duggal@research.ge.com

Ahmet Gün Erlat General Electric Global Research Center, 1 Research Circle, KWC 331, Niskayuna, NY 12309, USA, erlat@research.ge.com

Helena Gleskova Department of Electronic and Electrical Engineering, University of Strathclyde, Royal College Building, Glasgow, G1 1XW, UK, helen.gleskova@eee.strath.ac.uk

George Gruner Department of Physics and Astronomy, University of California, Los Angeles, CA 90095-01547, USA, ggruner@ucla.edu

David Hecht Department of Physics and Astronomy, University of California, Los Angeles, CA 90095-01547, USA, Dhecht99@ucla.edu

Martin Heeney Department of Materials, Queen Mary, University of London, London, E1 4NS, UK, m.heeney@qmul.ac.uk

Warren B. Jackson Hewlett-Packard Laboratories, Mail Stop 1198, Palo Alto, CA 94304, USA, warren.jackson@hp.com

Michael G. Kane Sarnoff Corporation, CN5300, Princeton, NJ 08543, USA, mkane@sarnoff.com

Iain McCulloch Department of Chemistry, Imperial College London, London SW7 2AZ, UK, i.mcculloch@imperial.ac.uk

Michael D. McGehee Department of Materials Science and Engineering, Stanford University, Stanford, CA, USA, mmcgehee@stanford.edu

Arokia Nathan London Centre for Nanotechnology, London, UK

Tse-Nga Ng Palo Palo Alto Research Center, Palo Alto, CA 94304, USA

Alberto Salleo Stanford University, Stanford, CA 94305, USA, asalleo@stanford.edu

Kalluri R. Sarma Honeywell International, Phoenix, AZ 85036, USA, kalluri.r.sarma@honeywell.com

Andrei Sazonov The Department of Electrical and Computer Engineering, University of Waterloo, Ontario, Canada, asazonov@venus.uwaterloo.ca

P. Schilinsky Konarka Technologies GmbH, Landgrabenstrasse 94, D-90443 Nürnberg, Germany

Shawn R. Scully Department of Materials Science and Engineering, Stanford University, Stanford, CA, USA

Takao Someya School of Engineering, Quantum-Phase Electronics Center, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656 Japan, someya@ap.t.u-tokyo.ac.jp

Denis Striakhilev The Department of Electrical and Computer Engineering, University of Waterloo, Canada

Zhigang Suo Division of Engineering and Applied Science, Harvard University, Cambridge, MA 02139, USA

Sigurd Wagner Department of Electrical Engineering, Princeton Institute for the Science and Technology of Materials, Princeton University, Princeton, NJ 08544, USA, wagner@princeton.edu

C. Waldauf Konarka Technologies GmbH, Altenbergerstrasse 69, A-4040 Linz, Austria

William S. Wong Palo Alto Research Center, Palo Alto, CA 94304, USA, wsw@parc.com

Min Yan General Electric Global Research Center, 1 Research Circle, KWC 335, Niskayuna, NY 12309, USA, yanm@research.ge.com

Chapter 1

Overview of Flexible Electronics Technology

I-Chun Cheng and Sigurd Wagner

Abstract This chapter provides an overview of the history, concepts, and possible applications of flexible electronics from the perspectives of materials and fabrication technology. The focus is on large-area capable electronic surfaces. These are made of backplane and frontplane optoelectronics that are fabricated as fully integrated circuits on flexible substrates. The discussion covers flexible electronics, and reaches back to rigid-substrate precursor technology where appropriate. Flexible electronics is a wide-open and rapidly developing field of research, development, pilot production, and field trials. The chapter puts a perspective on the technology by systematizing it and by describing representative examples.

1.1 History of Flexible Electronics

Flexible electronics has a long history. Anything thin is flexible. Forty years ago single-crystalline silicon solar cells were thinned to raise their power/weight ratio for use in extraterrestrial satellites. Because these cells were thin, they were flexible and warped like corn flakes. Today, silicon-integrated circuits are thinned to become compliant so that the owner of a smart card does not break it when he sits on it. Flexible can mean many qualities: bendable, conformally shaped, elastic, lightweight, nonbreakable, roll-to-roll manufacturable, or large-area. The field has open boundaries that move with its development and application. In this chapter we cover a newly emerging segment of flexible electronics that is largely connected with active thin-film transistor (TFT) circuits. Therefore, this survey is representative but incomplete. To the industrial community today, flexible electronics means flexible displays and X-ray sensor arrays. To researchers flexible means conformally shaped displays and sensors, electronic textiles, and electronic skin.

I-Chun Cheng (✉)

Department of Electrical Engineering, and Graduate Institute of Photonics and Optoelectronics,
National Taiwan University, Taipei, 10617 Taiwan
e-mail: ichuncheng@cc.ee.ntu.edu.tw

The development of flexible electronics dates back to the 1960s. The first flexible solar cell arrays were made by thinning single crystal silicon wafer cells to $\sim 100\text{ }\mu\text{m}$ and then assembling them on a plastic substrate to provide flexibility [1, 2]. The energy crisis in 1973 stimulated work on thin-film solar cells as a path to reducing the cost of photovoltaic electricity. Because of their relatively low deposition temperature, hydrogenated amorphous silicon (a-Si:H) cells lend themselves to fabrication on flexible metal or polymer substrates. In 1976, Wronski, Carlson, and Daniel at RCA Laboratories reported a Pt/a-Si:H Schottky barrier solar cell made on a stainless steel substrate, which also served as the back contact [3]. In the early 1980s, n^+-i a-Si:H/Pt Schottky barrier and p^+-i-n^+ a-Si:H/ITO solar cells were made on organic polymer ("plastic") film substrates by Plattner et al. [4] and by Okaniwa et al. [5–7], respectively. Okaniwa and coworkers also studied the flexibility of their solar cells. Around the same time, the CdS that had been developed for CdS/Cu₂S solar cells on glass substrates was made by continuous deposition on a moving flexible substrate in a reel-to-reel vacuum coater [8]. Beginning in the early 1980s, the roll-to-roll fabrication of a-Si:H solar cells on flexible steel [9] and organic polymer substrates [10] was introduced. Today, a-Si:H solar cells routinely are made by roll-to-roll processes.

The first flexible TFT dates back to 1968, when Brody and colleagues made a TFT of tellurium on a strip of paper and proposed using TFT matrices for display addressing. In the following years, Brody's group made TFTs on a wide range of flexible substrates, including Mylar, polyethylene, and anodized aluminum wrapping foil. The TFTs could be bent to a $1/16''$ radius and continued to function. They could be cut in half along the channel direction, and both halves remained operational [11, 12].

In the mid-1980s, the active-matrix liquid-crystal display (AMLCD) industry started in Japan by adopting the large-area plasma enhanced chemical vapor deposition (PECVD) machines that had been developed for a-Si:H solar cell fabrication. The success of the a-Si:H TFT backplane-based AMLCD industry and the demonstration of a-Si:H solar cells on flexible substrates stimulated research on silicon-based thin-film circuits on novel substrates. In 1994, Constant et al. at Iowa State University demonstrated a-Si:H TFT circuits on flexible polyimide substrates [13]. Their demonstration included two approaches to achieving overlay registration in photolithography: (1) the edge of the polyimide substrate was affixed to a rigid silicon wafer by using vacuum compatible epoxy resin and (2) a conformal coating of polyimide was applied to a silicon wafer to form a polyimide film; after the TFT circuitry had been fabricated on top of the polyimide film, it was detached from the wafer. In 1996, a-Si:H TFTs were made on flexible stainless steel foil [14]. In 1997, polycrystalline silicon (poly-Si) TFTs made on plastic substrates using laser-annealing were reported [15, 16]. Since then, research on flexible electronics has expanded rapidly, and many research groups and companies have demonstrated flexible displays on either steel or plastic foil substrates. For example, in 2005 Philips demonstrated a prototype rollable electrophoretic display [17] and Samsung announced a $7''$ flexible liquid crystal panel [18]. In 2006, Universal Display Corporation and the Palo Alto Research Center presented a prototype flexible organic light-emitting diode (OLED) display with full-color and full-motion with a poly-Si TFT backplane made on steel foil [19].

1.2 Materials for Flexible Electronics

A generic large-area electronic structure is composed of (1) a substrate, (2) backplane electronics, (3) a frontplane, and (4) encapsulation. To make the structure flexible, all components must comply with bending to some degree without losing their function. Two basic approaches have been employed to make flexible electronics: (1) transfer and bonding of completed circuits to a flexible substrate and (2) fabrication of the circuits directly on the flexible substrate.

In the transfer-and-bond approach, the whole structure is fabricated by standard methods on a carrier substrate like a Si wafer or a glass plate. Then it is transferred to [20–23] or fluidic self-assembled on [24] a flexible substrate. The transfer-and-bond approach has been extended to the bonding of ribbons of Si and GaAs devices to a stretched elastomer, which upon relaxation forms a “wavy” semiconductor that can be stretched and relaxed reversibly [25, 26]. The transfer approaches have the advantage of providing high-performance devices on flexible substrates. These processes are sophisticated advances over the original flexible wafer-based solar cell arrays [1, 2]. Their drawbacks are small surface area coverage and high cost. Bonded circuits will likely be added to large-area electronic surfaces at low density for high-speed communication and computation, lasing, and similarly demanding functions.

In many applications, the majority of the surface will be covered with electronics fabricated directly on the substrate. There are many approaches to integrating disparate materials and oftentimes flexible substrates are not fully compatible with existing planar silicon microfabrication processes. Direct fabrication may require (1) relying on polycrystalline or amorphous semiconductors because these can be grown on foreign substrates, (2) developing new process techniques, (3) introducing new materials, and (4) striking a compromise between device performance and low process temperatures tolerated by polymer foil substrates. Direct fabrication on flexible substrates is a hotbed of process research. New process techniques include the printing of etch masks [27, 28], the additive printing of active device materials [29–31], and the introduction of electronic functions by local chemical reaction [32]. Nanocrystalline silicon and printable polymers for OLEDs [33] are also materials of intense research. We will concentrate on the direct fabrication on flexible substrates, as it is the most direct, and sometimes more innovative, approach to the manufacturing of large-area electronic surfaces.

1.2.1 Degrees of Flexibility

Flexibility can mean many different properties to manufacturers and users. As a mechanical characteristic, it is conveniently classified in the three categories illustrated by Fig. 1.1 : (1) bendable or rollable, (2) permanently shaped, and (3) elastically stretchable. The tools for microfabrication have been developed for flat substrates. Therefore, at present all manufacturing is done on a flat workpiece that is shaped only as late as possible in the process. This approach benefits from the tremendous technology base established by the planar integrated circuit and display industries.

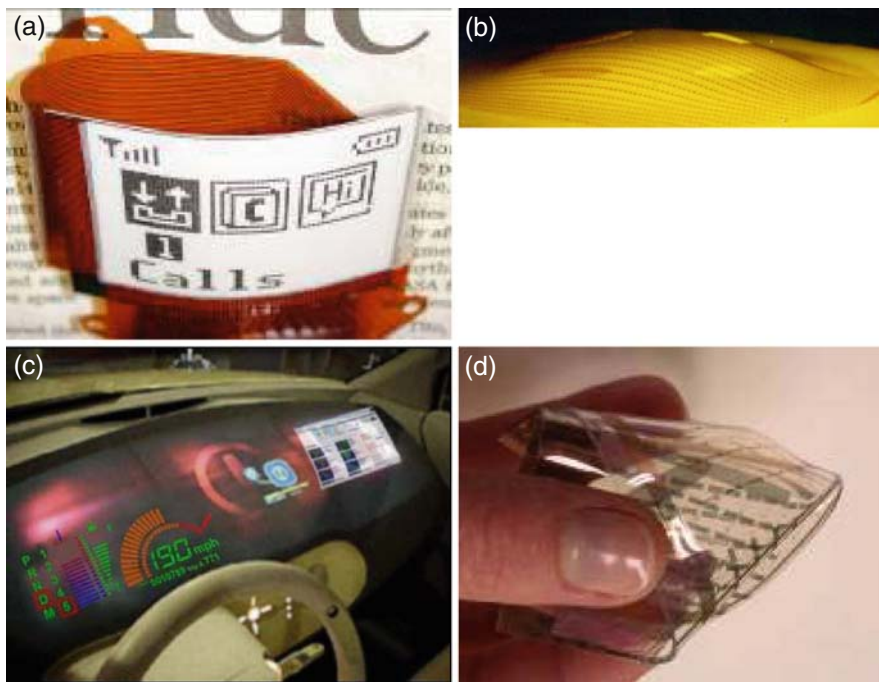


Fig. 1.1 (a) A bendable wristband display [Courtesy of Dr. Yu Chen, E Ink Corporation, 2001]. (b) Silicon islands on a spherically shaped foil substrate [34]. (c) Concept for a conformably shaped digital dashboard [Courtesy Professor Miltiadis Hatalis, Lehigh University]. (d) Stretchable interconnects on an elastomer [Dr. Stéphanie P. Lacour, Princeton University]

When a mechanically homogeneous sheet of thickness d is bent to a cylindrical radius r , perpendicularly to the axis of bending, its outside surface expands and its inside surface is compressed by the bending strain $\varepsilon = d/2r$. When the sheet is not homogeneous, as is the case for an a-Si:H TFT layer on a plastic foil, the strain in the surfaces is modified from this simple expression, which however remains a useful approximation. In TFT backplanes or in entire displays, the strain ε must be kept below a critical value. The straightforward approach to keeping ε low even in sharp bending, to small r , is to make the structure thin. In this way, the strain experienced by the active devices in bendable or rollable electronics can be kept small, particularly when the devices are placed in the neutral plane.

Conformally shaped electronic surfaces are also made by existing planar fabrication techniques. Continuous, unbroken, surfaces are shaped to the desired geometry by plastic deformation [35, 36]. The extent of deformation can easily exceed the critical tensile strain, for fracture or necking, of thin-film inorganic semiconductors or metals, which typically lies between 0.1 and 1%. Therefore, the devices are protected by placement onto rigid islands. However, if only materials that can

undergo large plastic deformation are employed, a flat electronic surface may be shaped without causing damage to unprotected devices [37].

Elastically stretchable electronics can undergo large and reversible deformation. When the substrate is an elastomer, devices are placed on rigid islands and are interconnected with elastically stretchable conductors [38, 39]. Alternatively, a substrate configured as a net-like open surface can be deformed reversibly without damaging the electronics that are made on the ribs of the net [40].

1.2.2 Substrates

Flexible substrates that are to serve as drop-in replacements for plate glass substrates must meet many requirements:

- (1) Optical properties – Transmissive or bottom-emitting displays need optically clear substrates. In addition, substrates for LCDs must have low birefringence.
- (2) Surface roughness – The thinner the device films, the more sensitive their electrical function is to surface roughness. Asperities and roughness over short distance must be avoided, but roughness over long distance is acceptable. As-received metal substrates usually are rough on both scales, while plastic substrates may be rough only over long distance.
- (3) Thermal and thermomechanical properties – The working temperature of the substrate, for example the glass transition temperature (T_g) of a polymer, must be compatible with the maximum fabrication process temperature (T_{max}). Thermal mismatch between device films and substrate may cause films to break during the thermal cycling associated with fabrication. A rule of thumb for tolerable mismatch is $|\Delta CTE \cdot \Delta T| \leq 0.1\text{--}0.3\%$, where ΔCTE is the difference in coefficients of thermal expansion between substrate and device film, and ΔT is the temperature excursion during processing. Silicon-based circuits benefit from substrates with low CTE. High thermal conductivity may be important for the cooling of current-load circuits. Dimensional stability during processing is a concern with plastic substrates.
- (4) Chemical properties – The substrate should not release contaminants and should be inert against process chemicals. Of advantage are substrates that are good barriers against permeation by atmospheric gases: for OLED application the water vapor permeation rate should lie below 10^{-6} g/m²/day and the oxygen permeation rate below 10^{-3} to 10^{-5} cm³/m²/day.
- (5) Mechanical properties – A high elastic modulus makes the substrate stiff, and a hard surface supports the device layers under impact.
- (6) Electrical and magnetic properties – Conductive substrates may serve as a common node and as an electromagnetic shield. Electrically insulating substrates minimize coupling capacitances. Magnetic substrates can be used for the temporary mounting of the substrate during fabrication, or for affixing the finished product.

Table 1.1 Properties of substrates for flexible backplanes [after ref. 41]

Property	Unit	Glass (1737)	Plastics (PEN, PI)	Stainless steel (430)
Thickness	μm	100	100	100
Weight	g/m ²	250	120	800
Safe bending radius	cm	40	4	4
Roll-to-roll processable?	–	Unlikely	Likely	Yes
Visually transparent?	–	Yes	Some	No
Maximum process temperature	°C	600	180, 300	1,000
CTE	ppm/°C	4	16	10
Elastic modulus	GPa	70	5	200
Permeable to oxygen, water vapor		No	Yes	No
Coefficient of hydrolytic expansion	ppm/%RH	None	11, 11	None
Prebake required?	–	Maybe	Yes	No
Planarization required?	–	No	No	Yes
Buffer layer required? Why?	–	Maybe	yes: adhesion, chemical passivation	yes: electrical insulator, chemical passivation
Electrical conductivity	–	None	None	High
Thermal conductivity	W/m·°C	1	0.1–0.2	16
Plastic encapsulation to place electronics in neutral plane	Substrate thickness	5×	1×	8×
Deform after device fabrication	–	No	Yes	No

Three types of substrate materials are available for flexible applications: metals, organic polymers (plastics), and flexible glass. Properties of typical materials are listed in Table 1.1 for 100-μm-thick foils.

1.2.2.1 Thin Glass

Glass plates are the current standard substrates in flat panel display technology. Plate glass becomes flexible when its thickness is reduced to several 100 μm [42, 43]. Glass foils as thin as 30 μm can be produced by the downdraw method. Foil glass retains all advantages of plate glass: optical transmittance of >90% in the visible, low stress birefringence, smooth surface with RMS roughness of 1 nm or less, temperature tolerance of up to 600°C, high dimensional stability, a low coefficient of thermal expansion (CTE) of $\sim 4 \times 10^{-6}/^{\circ}\text{C}$, which matches those of silicon device materials, resistance to most process chemicals, no out-gassing, impermeability against oxygen and water, scratch resistance, and electrical insulation. However, flexible glass is fragile and difficult to handle. To reduce breakage during handling, foil glass can be made to resist crack propagation by

(1) laminating it with plastic foil, (2) applying a thin hard coat, or (3) applying a thick polymer coat.

1.2.2.2 Plastic Film

Polymer foil substrates are highly flexible, can be inexpensive, and permit roll-to-roll processing. However, they are thermally and dimensionally less stable than glass substrates and are easily permeated by oxygen and water. A glass transition temperature, T_g , compatible with the device process temperature is essential. However, a high T_g alone is not sufficient. Dimensional stability and a low CTE are also important factors. Typical polymer films are shrunk by heating and cooling cycles. They shrink less if prestabilized by prolonged annealing [44]. Because the elastic modulus of polymer substrates is a factor of 10–50 lower than that of inorganic device materials, a small thermal mismatch stress can make the free-standing workpiece curve and cause misalignment during the overlay registration of the flattened piece. A large CTE mismatch coupled with a large temperature excursion during processing can break a device film [45]. Polymer substrates with CTE below 20 ppm/°C are preferred as substrates for silicon-based device materials.

Candidate polymers for flexible substrates include (1) the thermoplastic semicrystalline polymers: polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), (2) the thermoplastic noncrystalline polymers: polycarbonate (PC) and polyethersulphone (PES), and (3) high- T_g materials: polyarylates (PAR), polycyclic olefin (PCO), and polyimide (PI). PC, PES, PAR, and PCO are optically clear and have relatively high T_g compared to PET and PEN, but their CTEs are 50 ppm/°C or higher, and their resistance to process chemicals is poor. Much research has been conducted with PET, PEN, and PI, with their relatively small CTEs of 15, 13, and 16 ppm/°C (Kapton E), respectively, relatively high elastic moduli, and acceptable resistance to process chemicals. Both PET and PEN are optically clear with transmittance of >85% in the visible. They absorb relatively little water (~0.14%), but their process temperatures are only ~150 and ~200°C, even after prestabilization by annealing. In contrast, PI has a high glass transition temperature of ~350°C, but it is yellow because it absorbs in the blue, and it absorbs as much as 1.8% moisture [46, 47]. No polymer meets the extremely demanding requirement for low permeability in OLED applications. The typical water and oxygen permeation rates of flexible plastic substrates are 1–10 g/m²/day and 1–10 cm³/m²/day, respectively, instead of the required 10⁻⁶ g/m²/day and 10⁻⁵ cm³/m²/day [48]. Barrier layer coatings can reduce absorption and permeability by gas, raise resistance to process chemicals, strengthen adhesion of device films, and reduce surface roughness.

1.2.2.3 Metal Foil

Metal foil substrates less than ~125 μm thick are flexible and are attractive substrates for emissive or reflective displays, which do not need transparent substrates. Stainless steel has been most commonly used in research because of its high

resistance to corrosion and process chemicals, and its long record of application in amorphous silicon solar cells. Stainless steel substrates can tolerate process temperature as high as 1,000°C, are dimensionally stable, present a perfect permeation barrier against moisture and oxygen, can serve as heat sink, and can provide electromagnetic shielding. Certain magnetic steels lend themselves to magnetic mounting and handling. In general, stainless steel substrates are more durable than plastic and glass foils.

A typical stainless steel foil comes with sharp rolling marks and micrometer-size inclusions, which may cause devices to fail. The most carefully rolled steel has a surface roughness of ~ 100 nm, in contrast to display glass with less than 1 nm. To ensure the electrical integrity of the thin-film devices made on them, steel foil substrates must be either polished well [49, 50] or planarized with a film [14, 51, 52]. The planarization layer may be organic, inorganic, or a combination. Commercially available materials for planarization include (1) organic polymers, (2) methylsiloxane spin-on-glass, and (3) silicate spin-on-glass. The higher the organic content of the planarizing material, the thicker the film that can be applied without forming cracks and the smoother the resulting surface. This is particularly important for OLEDs, which need a surface roughness of less than 5-nm RMS. However, the organic content imposes a ceiling on any subsequent, sustained process temperature. An organic polymer-planarizing layer can be protected against excessive transient heating with an inorganic overlayer by pulsed-laser processing. The typical process steps for applying the planarization layer include spin-on, hot-plate bake, and high-temperature cure. As a rule of thumb, the final curing temperature sets the upper temperature limit for the subsequent device process. Incorporation of getter materials, for example phosphorus in a spin-on silicate film, enhances the barrier properties against possible contaminants that may originate in the steel substrate.

Metal substrates are electrically conducting. In some applications they can serve as back contact, as in solar cells. For other applications metal must be coated with an insulating layer to provide circuit isolation. SiN_x or SiO_2 layers are commonly used for this purpose on steel substrates. The electrical insulation also functions as adhesion layer and as barrier against process chemicals. $\text{SiN}_x\text{:H}$, a standard material in the a-Si:H TFT process, is also an excellent diffusion barrier. However, the high hydrogen content of $\text{SiN}_x\text{:H}$ may cause the film to crack or ablate during subsequent processing at high temperature or during laser annealing. In such cases, an SiO_2 film is deposited instead and provides the added advantage of a lower dielectric constant than that of $\text{SiN}_x\text{:H}$, which helps reduce the capacitive coupling between the substrate and the electronics. A barrier layer of 0.2–0.4 μm suffices for electrical insulation as it reduces the leakage current at a potential difference of 50 V to 1 nA/cm². An active-matrix circuit driven at video rate may require a thicker layer to reduce the coupling capacitance to 1 nF/cm².

1.2.3 Backplane Electronics

Backplanes provide or collect power and signal to or from frontplanes. Backplanes may be passive or active. The ideal flexible active-matrix backplane should be

ugged, rollable or bendable, capable of CMOS operation, and should lend itself to low-cost manufacturing. Today's TFT backplane technologies are best described by their active semiconductor, which may be amorphous, nanocrystalline, or polycrystalline silicon, a II–VI compound semiconductor, or an organic semiconductor in polymer or molecular form. As thin-film semiconductor technologies develop away from glass substrates and toward flexible substrates, the backplanes differentiate further by the type of substrate. The substrate material defines a region of TFT fabrication conditions in temperature–time space. The maximum tolerable process temperature is set by the type of substrate materials: <300 , <600 , and $<1,000^\circ\text{C}$ for organic polymer, glass, and steel substrates, respectively. We now briefly review the active materials for TFT backplanes and the associated fabrication technologies.

1.2.3.1 Silicon Thin-Film Transistors

Silicon-based materials benefit from the advantages of a well-established technology and a native oxide that is a high-quality insulator. Three approaches can be taken to preparing TFT-grade silicon on foil substrates: (1) direct deposition of the channel semiconductor, (2) deposition of a precursor film followed by crystallization, and (3) physical transfer of separately fabricated circuits. Techniques (1) and (2) are explored for large-area display applications. Direct deposition can provide the full range of devices, from low OFF current amorphous silicon (a-Si:H) TFTs to CMOS capable TFTs of nanocrystalline silicon (nc-Si:H). The highest ON current is obtained in TFTs of both polarities in polycrystalline silicon (poly-Si) made by the crystallization of an amorphous silicon precursor film.

a-Si:H made from a glow discharge was first reported in the late 1960s and the first a-Si:H TFT was demonstrated by Snell and coworkers in 1981 [53]. Since the mid-1990s, a-Si:H TFTs have been made on flexible substrates, including PI films [13] and stainless steel foil [14]. Today's baseline growth process for a-Si:H TFTs is PECVD at a substrate temperature of 250 – 350°C . a-Si:H is a material with reproducible optoelectronic properties that provides TFTs with electron field-effect mobilities of ~ 0.5 – $1\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. The a-Si:H growth process has been adapted to low-temperature polymer substrates with process temperatures of 150°C or less [54]. The only useful a-Si:H TFTs are n-channel devices as the hole mobility of $\sim 0.003\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ is too low to be useful.

nc-Si:H is a promising candidate material for fully integrated electronics on plastic because it is CMOS capable and can be made by PECVD at low substrate temperature. The top-gate geometry has produced the highest mobilities to date. However, the nc-Si:H TFT fabrication process needs considerably more research. The nc-Si:H growth schedule (direct or prenucleation), the location of source/drain contacts (in-plane or staggered), efficient source/drain doping (particularly p^+), the type of gate dielectric (SiO_2 or SiN_x), and the techniques for post-process annealing are not settled.

Poly-Si can be either directly deposited by low-pressure chemical vapor deposition (LPCVD) or formed by the crystallization of a precursor film, typically a-Si:H. Crystallization produces the superior material, with larger grain sizes and smoother surface than obtained by LPCVD. a-Si:H can be crystallized by furnace anneal at

600°C or higher, or at $\sim 550^\circ\text{C}$ by silicide-mediated crystallization (also known as metal-induced crystallization), and by pulsed excimer laser annealing. Poly-Si TFTs have been made on steel foil substrates since the late 1990s [55, 56]. While furnace crystallization is not compatible with organic polymer substrates, the spatial and temporal confinement of heat in excimer laser annealing permits making poly-Si on plastic, as first demonstrated with poly-Si TFTs made on plastic in 1997 [16]. Controlling the geometry of the laser spot produces large grain sizes [57], and poly-Si TFTs with high performance have been made on flexible steel substrates [58, 59].

1.2.3.2 Organic Thin-Film Transistors

The first demonstration of the field effect in a small-molecule organic material dates back to 1964 [60]. In 1983, the field effect in a polymer structure made by a solution process was reported [61]. Since then the performance of organic thin-film transistors (OTFTs) has been raised impressively by the introduction of new organic channel materials and by improved fabrication [62]. In the late 1990s, OTFTs with ON currents comparable to those of a-Si:H TFT were reported [63]. In 2000, pentacene TFTs with a hole field-effect mobility of $3.2\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and an ON/OFF ratio of $>10^9$ were demonstrated [64]. Because in most organic materials the hole mobility is higher than the electron mobility, most OTFTs are p-channel devices.

Organic polymers are soluble, and small molecules can be derivatized to soluble precursors. Therefore, OTFTs can be fabricated by solution processing near room temperature [31], compatible with low-temperature plastic substrates. Since the late 1990s, OTFTs and circuits have been made on flexible plastic substrates, including PI [32, 65], PEN[66], PET [67–69], PC [70, 71], and on paper [72]. More recently, displays have been made on OTFT backplanes on flexible polymeric substrates. The displays include reflective LCDs [73, 74], electrophoretic displays [75], and OLED displays [76–79].

1.2.3.3 Transparent Thin-Film Transistors

TFTs made of transparent materials [80, 81] may not need shielding from visible light to suppress photoconductance, and can raise the pixel aperture of transmissive displays, for example on windscreens of cars. They have been developed from the conventional wide-bandgap compound semiconductors: GaN or SiC, and from the transparent oxide semiconductors: ZnO [82], In_2O_3 [83, 84], and SnO_2 [85]. The first flexible transparent TFT was made by Nomura et al. in 2004 from the amorphous In–Ga–Zn–O system on PET. Saturation mobilities reached $6\text{--}9\text{ cm}^2\text{V}^{-1}\text{s}^{-2}$, and device characteristics were stable under mechanical bending [86].

More recently, flexible transparent TFTs have been demonstrated with organic channel materials, including a conductive polymer [69] and single-walled carbon nanotubes (SWNT). SWNTs have enabled flexible transparent organic TFTs with mobilities comparable to that of a-Si:H TFTs [87–89].

1.2.3.4 Materials for Interconnects and Contacts

Transparent Conductive Oxides

Typical electrode and contact materials are metallic. Displays and thin-film solar cells, however, need electrodes that are transparent electrical conductors. To date, these have been metal oxides [90–92]. The first transparent conducting oxide (TCO), CdO, was reported by Baedeker in 1907 [93]. Transparent conducting tin-doped indium oxide (ITO), originally developed for the defrosting of aircraft windshields, is the most widely used TCO. It is the transparent electrode in flat panel displays, is used for electromagnetic shielding, and is deposited on optical grade polyester (PET) substrates by roll-to-roll dc sputtering for touch screens. In the trade-off between electrical conductivity and optical transparency, ITO has reached a performance plateau at a resistivity of $\sim 10^{-4} \Omega \cdot \text{cm}$. New TCO materials based on ZnO and SnO_2 , and mixed ternary and quaternary oxides are under development.

Depositing ITO on organic polymer foil substrates presents two challenges: optoelectronic quality and mechanical integrity. The best-quality display grade ITO on glass is dc-magnetron sputtered at a substrate temperature of 300–400°C, or first sputtered on the cold substrate and then annealed at 200°C in a controlled oxygen environment. Because polymeric substrate materials are heat sensitive, ITO is deposited on them at low temperature as an amorphous phase. Fortunately, amorphous ITO films deposited at room temperature have an optical transparency and an electrical conductivity that is adequate for present display technologies. The mismatch in mechanical properties between the ITO and the polymeric substrate is a challenge. ITO is stiff and brittle with an elastic modulus of ~ 118 GPa. Depositing it on a compliant substrate may cause cracks and delamination during fabrication or in use. The mechanisms of cracking and the effect of cracking on the electrical properties of ITO films on PET substrates have been investigated by Cairns et al. The critical strain for cracking is reciprocal to the square root of film thickness, similar to what observed in a typical ceramic film [94]. ITO cracks at a strain of $\sim 1\%$. Prior to electrical failure, small cracks form and may grow by fatigue under cyclic loading. The onset of ITO conductivity loss in tension can be delayed by reducing the ITO layer thickness, by using a high-modulus but nonbrittle undercoat for the ITO, or by introducing compressive prestress into the ITO layer. Under compressive load, the brittle ITO film may delaminate and then buckle and crack. The strain at which buckling occurs depends on the strength of adhesion between the ITO and the substrate [95].

Conducting Organic Polymers

We just described how the mismatch of mechanical properties between inorganic device films and polymeric substrates can break the films during processing and use. These risks of film fracture provide one motive for using conductive polymers as contact and interconnect materials as part of all-organic flexible electronics [96]. In 1976, Heeger, MacDiarmid, and Shirakawa made the discovery that polyacetylene exhibits a high electrical conductivity when doped with the oxidant iodine.

Today, such “self-doped” conductive polymers are available commercially. Polyaniline (PANI) and polypyrrole (PPY) are used as antistatic materials, polythiophene derivatives, e.g., polyethylene dioxythiophene (PEDOT) replace inorganic ITO in some device applications and also function as hole injectors and transport layers in OLEDs, and polyphenylene vinylene (PPV) derivatives are active materials in polymer light-emitting diodes (PLEDs). Conductive polymers need much further research as they are not yet well defined and have suboptimal device properties.

Stretchable Interconnects

Flexible electronic surfaces that undergo large plastic deformation need stretchable interconnects. One-time deformation, for example to a conformally shaped surface, needs interconnects that can be deformed plastically. Under certain conditions, metal films can be deformed once and remain electrically conducting [35–37]. Repeated deformation, as experienced by electronic skin, requires elastic interconnects. Several approaches have been demonstrated to realizing elastically stretchable interconnects. They include making “filled” elastomers conducting by blending in conductive polymers [97–99] or by embedding metal particles [100]. Conductor-filled elastomers are used mainly for forming interconnects between rigid components. [101, 102]. Often the electrical conductivities of these conducting elastomers are insufficient for electrical interconnects. Because the filled-elastomer conductors are applied with thick-film techniques, they are not directly compatible with thin-film circuits. The search for elastic thin-film interconnects has focused on metal films deposited on or encased in elastomers. Microfabricated gold-film serpentes encased in a silicone elastomer conduct up to 54% tensile strain [103]. Stripes of thin gold film patterned on prestretched or flat elastomeric membranes remain electrically conducting when the membranes are stretched up to twice their initial length. Such stretchable interconnects were used in the demonstration of an inverter circuit made of a-Si:H TFTs on a silicone membrane [38, 104, 105].

1.2.4 Frontplane Technologies

Frontplanes carry the specific optoelectronic application. The frontplane materials of displays include liquid crystals for transmissive displays, reflective-mode liquid crystals and electrophoretic foils for reflective displays, and OLEDs for emissive displays. The frontplane might also be an X-ray sensor, an image sensor, a pressure sensor, a chemical sensor, an actuator or an artificial muscle in a smart textile.

1.2.4.1 Liquid Crystal Displays

The LCD is a light intensity filter that is controlled by the electric field between two transparent electrodes. These are fabricated on glass plates that are held $\sim 5\text{ }\mu\text{m}$ apart by transparent spacers [106]. To make the LCD flexible, the liquid is encapsulated in a polymer foil. The first examples were the polymer-dispersed liquid

crystal (PDLC) [107] and the nematic curvilinear aligned phase (NCAP) [108, 109]. The phase separation procedure developed for PDLCs can also be used for bistable cholesteric liquid crystal [110]. Today, the term PDLC is used to describe liquid crystal droplets in encapsulated form. The PDLC dispersion techniques do not require alignment layers or polarizers, and large devices are relatively simple to fabricate.

The first LCDs fabricated on flexible plastic substrates date back to 1981 [111, 112]. In the meantime, full-color reflective cholesteric displays on plastic substrates have been developed [113–116], and twisted nematic LCDs made on a transparent flexible plastic substrate were demonstrated with low-voltage operation and high contrast [117]. A paintable LCD technology, a sequence of coating and UV curing, is under development for making flexible LCDs [118].

1.2.4.2 Electrophoretic Displays

Electrophoretic displays are reflective-type bistable devices. Bistable displays consume power only when they are overwritten. Because they combine low-power consumption with adequate contrast and full viewing angle, they are particularly suitable for electronic books. In electrophoretic displays, the electric field across the electrophoretic material controls the location and orientation of charged objects that are suspended in a liquid. Metcalfe and Wright first used electrophoresis for creating an image in 1956 [119]. In the early 1970s, displays using electrophoresis to create reversible images were demonstrated [120, 121]. These electrophoretic displays suffered from sticking particles, discoloration of dyes, and migration of particles to electrode edges. To limit the lateral migration of the particles, microcellular electrophoretic films were developed in the late 1970s and early 1980s, by using photoresist to create a square grid of confining ribs [122, 123]. In the late 1990s, microencapsulated electrophoretic display films were developed by E-Ink Corporation [124] and by NOK Corporation [125]. Instead of filling the electrophoretic fluid into microcellular structures, the fluid is microencapsulated by means of polycondensation of urea and formaldehyde, which produces discrete, mechanically strong and optically clear, microcapsules. These microcapsules are subsequently spread on ITO-coated polyester foil, and then rear electrodes are printed. Microencapsulation not only solves the problem of particle clustering, agglomeration, and lateral migration, but also maintains the cell gap during deformation. Normally, electrophoretic displays are bicolor (black and white). Schemes for obtaining full color include (1) using three combinations of two-color electrophoretic fluids in a subpixelated scheme to form various combinations of red, green, and blue, (2) combining an external color filter over a black and white electrophoretic film, and (3) stacking three imaging films over each other [126].

The current electrophoretic film produced by E Ink Corporation is a dual-particle formulation. It contains positively charged white particles and negatively charged black particles that are suspended in a clear fluid. It has a black-to-white update time of less than 30 ms at 15 V drive voltage, and gray tones are obtained by partial addressing between black and white states [127]. Active-matrix electrophoretic displays with a-Si:H TFTs on steel foil substrates have been demonstrated by E Ink

[128, 129]. E Ink's microencapsulated electrophoretic films have been integrated with Plastic Logic Limited's active-matrix organic TFT backplane made by solution processing on a plastic substrate. Paper-like displays and prototypes of rollable displays based on E Ink's electrophoretic films have been demonstrated by Philips [130, 17].

1.2.4.3 Organic Light-Emitting Displays

Since the discovery of OLEDs in the late 1980s, the technology has developed rapidly and OLED displays encapsulated in glass are commercially available. OLEDs have wider viewing angles, faster response time, lower voltage operation, and possibly lower power consumption than backlit AMLCDs. Because of their thin-film structure, OLEDs are a natural choice for flexible displays. The two types of OLED materials are small-molecule, with the higher efficiency, and conjugated polymers. Small-molecule OLEDs are usually prepared by thermal evaporation, and polymer OLED by solution processing. The latter enables many potentially inexpensive fabrication steps, such as spin coating, ink-jet printing, and spraying, and is easily compatible with roll-to-roll manufacturing. Therefore, efforts are underway to develop solution-processable precursors for small-molecule OLED fabrication, as mentioned earlier.

Electroluminescence in organic materials was first studied in the 1960s [131–133]. Interest in organic electroluminescence was revived by Tang and VanSlyke's discovery of electroluminescence in small-molecule organic thin-film diodes made by thermal evaporation [134]. Visible light emission from polymer organic light-emitting diodes (PLEDs) reported by Burroughes et al. in 1990 attracted further attention. The PLED was deposited by spin coating a solution-processable precursor polymer, which then was converted to a conjugated polymer by heating to 250°C [135]. A year later, in 1991, Braun and Heeger reported the use of a soluble conjugated polymer that eliminated the need for high-temperature processing [136]. Soon thereafter a flexible OLED display on PET was demonstrated by Gustafsson et al., who employed solution-processable MEH–PPV as the active material and the conductive polymer PANI as the hole-injecting contact [137]. In 1997, a-Si:H TFTs on steel foil were integrated with a printed top-emitting OLED [33]. Many research groups now have demonstrated active-matrix OLEDs on flexible plastic or steel substrates [138–140]. A typical pixel cross section of an active-matrix bottom-emitting OLED on a clear plastic substrate is shown in Fig. 1.2.

In OLEDs and PLEDs, an ~100-nm-thick organic stack is sandwiched between an anode and a cathode. In bottom-emitting (through-the-substrate) OLEDs, the anode is usually ITO with high work function, and the cathode is a metal with low work function, such as Ca or Mg, which is covered by an interconnect metal like Al. Because top-emitting OLEDs need a transparent cathode, they are coated with a very thin layer of the cathode metal, which is then covered with ITO. Electrons and holes injected under forward bias combine to bound polaron–excitons. These radiatively decay via electron–hole recombination to produce the electroluminescence.

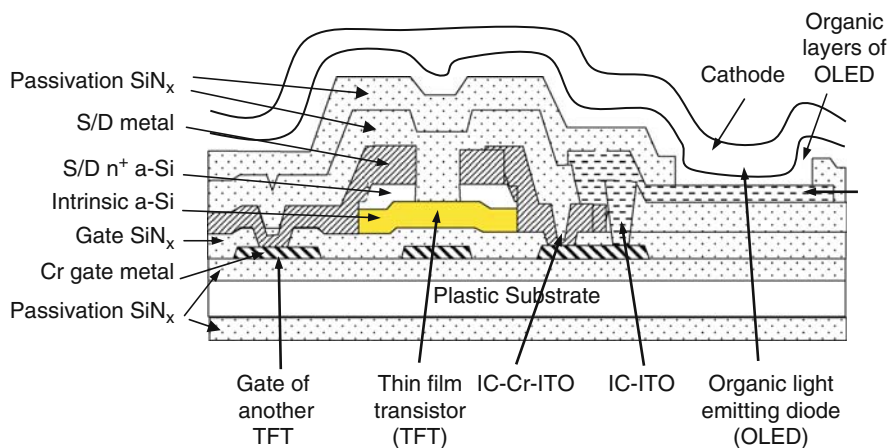


Fig. 1.2 Schematic cross section through an a-Si:H TFT and an OLED on a clear plastic substrate [Dr. Ke Long, Princeton University]

The OLED stack contains charge injection and transport layers that serve to keep the excitons away from nonradiatively recombining at the contacts. The injection and transport layers are also made of organic materials, for example PEDOT/polystyrene sulfonate or PANI [142]. Alternative OLED architectures include inverted top-emitting OLEDs that have the cathode in contact with the substrate, and transparent OLEDs whose anodes and cathodes both are transparent [143, 144]. The biggest challenge to making flexible OLED display is the demand for extremely low rates of permeation of moisture and oxygen to ensure acceptably long OLED lifetime. Oxidation at the organic–cathode interface can inhibit charge injection and results in black spots.

1.2.4.4 Sensors

Flexible sensors have captured the imagination for applications in biomedicine, artificial skin, and wearable electronics. We describe some recent examples. The shear-stress sensor skin by Xu et al. integrates microelectromechanical systems (MEMS) and ICs onto a flexible Parylene (poly-para-xylylene) “skin,” which can be affixed to the human body like a Band-Aid [145]. A hand posture and gesture monitoring glove has been made by integrating strain sensors with fabric [146]. The electrical characteristics of resistive, capacitive, or field-effect devices made of conducting or semiconducting polymers change upon gas absorption. This is the operating principle of chemical sensing transistors made on fibers for wearable electronics. [147]. A conformal H₂-sensing skin for the safety monitoring of H₂ fuel tanks is based on a piezoelectrically driven sound resonance cavity. The skin itself consists of a porous PVDF polymer layer that allows leaked H₂ to diffuse freely, and an impermeable silicone rubber that serves as the seal for the porous polymer [148]. Electronic skin developed by Someya and coworkers is made flexible and conformable by a net-like

structure that carries thermal and pressure sensors made of organic materials on its filaments. Conductive rubber functions as pressure sensor and organic diodes as thermal sensors [149–151, 40]. A plastic film with pentacene TFT-based electronic circuits is processed to form the net-like structure that allows the large deformation of the electronic skin. For ultra-high flexibility, the OTFTs are embedded at a neutral strain position [152]. A pressure sensor and microphone based on a ferroelectric polymer foil have been combined with an a-Si:H TFT on a PI foil substrate. Depending on the function, the TFT is used as a switch or amplifier [153].

1.2.4.5 Actuators

A soft electrically insulating polymer functions as dielectric in a capacitor with mechanically compliant electrodes. This electroactive polymer is compressed when the electrodes are charged and, by conservation of volume, expands parallel to the planes of the electrodes. Large deformation has been demonstrated in appropriately designed dielectric elastomer actuators [154, 155]. Electroactive polymer actuation has been switched by thin films on polymer foil, pointing to a possible technology for large-area actuation [156]. Potential applications include artificial muscles for biologically inspired robots, animatronics, prosthetics, conformally shaped loudspeakers, and smart skin which can modulate electromagnetic properties, control of airflow and heat transfer, and control of the texture of large surfaces.

1.2.4.6 Electronic Textiles

Low stiffness is inherent in textile fabric. E-textiles, or smart textiles, have electronic circuitry woven into or integrated onto the fabric [157, 158]. A circuit has been woven of yarns that carried a-Si:H TFTs or conductors, or functioned as insulating spacers [159]. Figure 1.3 illustrates the concept of an e-suit. E-textiles have been developed and test-marketed for wireless communication, entertainment, health, and safety. Electrically conducting fibers are a prerequisite. They can be made of wire or by coating fibers with metals, metallic salts, or conductive polymer. Input and output devices, sensors, actuators, and power supplies are integrated by application or weaving. One particular goal is a power supply obtained by integrating photovoltaics into the fabric. Nanotechnology and MEMS are expected to increasingly enable the direct integration of electronic devices. A number of practical issues that include conformal encapsulation of active-device yarn remain to be addressed.

1.2.5 Encapsulation

Thin-film encapsulation has been researched and applied for decades. Single-layer metallic barrier coatings [160–162] were followed by single-layer transparent barrier coatings [163–166] and now multilayer composite (oxide or nitride/polymer) barrier coatings. Since the early 1970s, thin aluminum films evaporated onto polymeric substrates have been applied commercially as gas barriers in food packaging.



Fig. 1.3 Concept of an e-suit [Givenchy Fall 1999 collection]

Today, metallized plastic foil is widely used for packaging not only of food but also of medical supplies and sensitive electronic components. A 10- to 100-nm-thick aluminum film reduces the permeability by atmospheric gases to 1/1,000 of that of the bare polymeric foil. For microwaveability and product visibility, transparent oxide barrier coatings applied by sputtering or chemical vapor deposition entered development in the 1980s. Today, polymeric substrates are routinely coated with thin layers of brittle oxides, which become flexible when made thin.

The typical inorganic barrier materials such as SiO_2 , SiN_x , and Al_2O_3 are highly impermeable to atmospheric gases. If it were perfect, a single thin layer could reduce the gas or vapor permeation to nondetectable values. However, microscopic defects, in particular granular film growth, cracks above occluded dust particles, and pinholes provide diffusion paths for gas and vapor [160, 166]. To slow down the ingress of atmospheric gas molecules, the length of their diffusion path is increased by stacking and alternating thin inorganic barrier layers and thick polymeric layers to a multilayer barrier. The polymeric layers stop the upward propagation of defects in the inorganic barrier layers, and make the composite structure more flexible than

a single thick inorganic barrier structure would be. The entire multilayer barrier is typically several micrometers thick. In 1994, aluminum layers as barriers alternating with acrylate polymer layers were found to reduce the oxygen permeation rate through a polypropylene substrate by four orders of magnitude [167]. In 1996, oxygen and water permeation rates below the detection limit of $<0.015 \text{ cm}^3/\text{m}^2/\text{day}$ were obtained by using a three-layer barrier structure of $1\text{-}\mu\text{m}$ acrylate/25-nm AlO_x /0.24- μm acrylate on a PET substrate [168].

Making impermeable thin-film barrier coatings has become the major challenge to making flexible OLED displays. Polymeric substrates needed a barrier on the substrate side (“passivation”) and on top (“encapsulation”) of the device to ensure long life. The barrier through which the light is emitted needs to meet the additional criteria of high optical transparency of 85–90% over the visible spectrum, control of optical microcavity effects, and, if on top of the OLED, low stress to avoid shear damage to the OLED, dense and conformal coating to avoid through-layer and edge leakage, and low process temperature. Multilayer organic/inorganic barrier coats have been proven to extend the operating life of OLEDs [48, 169–173]. For the purpose of reducing the cost and barrier complexity, single, dense, inorganic barrier layers of aluminum oxide made by atomic-layer deposition remain under study [174, 175].

An important complement to the development of the barrier technology itself is improved techniques for the evaluation of barrier quality, and with sufficient sensitivity for relevance to OLEDs. Direct identification and characterization of the defects that cause permeation are parts of this task in the development of flexible OLEDs.

1.3 Fabrication Technology for Flexible Electronics

1.3.1 Fabrication on Sheets by Batch Processing

Electronic devices and circuits and display panels are made by batch processing. Flexible foil substrates, cut to sheets, will be the drop-in replacement for the rigid glass plates or silicon wafers.

Flexible sheet substrates may be handled in several ways during processing:

- on a rigid carrier, facing up and loose;
- on a rigid carrier, facing up or down and bonded to the carrier for the duration of processing;
- in a tensioning frame, facing up or down;
- in a frame, facing down and loose;
- electrostatically bonded to a rigid carrier;
- magnetically attached to a rigid carrier.

Rigid substrates are best suited to free standing and loose mounting. The flexibility of the substrate is given by its flexural rigidity $D = Et^3/12(1-\nu^2)$, where E is Young’s modulus, t is the thickness of the substrate, and ν is its Poisson ratio.

PEN substrate as a function of relative humidity (RH) and time [15]. At 40% RH, the equilibrium moisture concentration in the film is expected to be about 957 ppm which is very high since for every 100 ppm of moisture absorbed, the film is estimated to expand by ~ 45 ppm. This is a very significant dimensional change and can deleteriously affect the TFT backplane process if it is not managed. Moisture absorption is reversible by heating the substrate in vacuum or in an inert atmosphere. Uncontrolled moisture absorption/desorption during the TFT backplane fabrication can potentially have far more impact on the substrate dimensional stability than the dimensional instability due to the inherent PEN substrate shrinkage. We will discuss this further in Section 4.4 on backplane fabrication.

Barrier Properties

The inherent barrier properties of PEN films are typically of the order of ca. $1 \text{ g/m}^2/\text{day}$ for water vapor transmission rates and an equivalent ca of $3 \text{ mL/m}^2/\text{day}$ for oxygen transmission rates. This is still a long way from the levels required for the protection of OLED displays, which require water vapor transmission rates of $<10^{-6} \text{ g/m}^2/\text{day}$ and oxygen transmission rates of $<10^{-5} \text{ mL/m}^2/\text{day}$. No polymer substrate meets these requirements, and the flexible substrates currently being developed need to use an effective barrier layer to encapsulate the OLED devices for protection against oxygen and moisture ingress to enhance the OLED lifetime. Note that the EPDs have far less sensitive to moisture, and thus do not impose such stringent requirements on the barrier layer performance. The progress in the barrier layer development is discussed in Section 4.2.1.3 in more detail.

4.2.2 TFT Technologies for Flexible Backplanes

Flexible substrate compatible TFT backplane technology development is a critical item for the fabrication of flexible active matrix displays. Both the well-established TFT technologies, namely a-Si TFT and LTPS TFT, are being considered for flexible display applications. In addition, emerging TFT technologies, namely O-TFT (organic TFT) and oxide semiconductor (such as ZnO) TFT technologies are also being developed for flexible backplane applications. The TFT processes developed for the flat rigid glass substrates cannot readily be applied for use with the flexible plastic substrates, due to reasons such as lower process temperature constraints, thermal stress limitations due to a larger CTE mismatch, and dimensional stability issues.

Currently, there are two main approaches being considered for producing flexible plastic backplanes:

- (1) Standard (high temperature) TFT fabrication on a conventional display glass substrate, followed by transfer of the TFT circuit (backplane) on to a flexible plastic substrate by adhesive bonding at a lower temperature (e.g., $<150^\circ\text{C}$). This process is referred to as Device Layer Transfer (DLT) process.
- (2) Fabrication of TFT array directly on the flexible plastic substrate using lower (plastic substrate compatible) temperature processes.

The DLT process [16, 17] can be a viable approach for flexible displays, when low cost is not a consideration. This approach can provide the most optimum TFT device performance with respect to mobility, leakage current, stability, and uniformity as the TFTs are fabricated using conventional LTPS (low-temperature polysilicon at $\sim 450^\circ\text{C}$) process, and then transferred on to the flexible plastic substrate at a low temperature. DLT will be a higher cost approach compared to the direct fabrication approach, due to wastage of the glass substrate and additional cost of the transfer process. While several companies have demonstrated this approach, it is not believed to be solution for the desired low-cost flexible displays ultimately.

Table 4.4 shows a comparison of the various TFT approaches. The conventional LTPS process used in the current AMLCDs uses a typical process temperature in the range of $\sim 450^\circ\text{C}$ using a polysilicon film produced by Excimer laser recrystallization of an a-Si film. Due to the high process temperature requirement, the conventional LTPS TFT approach may be appropriate for use with the stainless steel substrates, but not with plastic substrates with a process temperature limitation of less than 200°C . To overcome this problem using a plastic substrate, ultra low-temperature ($< 200^\circ\text{C}$) polysilicon (ULTPS) TFT processes are being developed [e.g., 18]. The ULTPS TFT approach has the potential for providing high mobility CMOS TFT devices suitable for driving the OLED pixels, as well as for fabricating the row and column drivers directly on the plastic substrate. Good progress has been made in producing TFTs with high mobility and satisfactory threshold voltages for the n- and p-channel devices. However, the leakage currents need to be reduced further for fabricating high-quality active matrix displays. The ULTPS technology continues to be developed to reduce the leakage currents and to further enhance its maturity and increase process yield.

a-Si TFT is currently the workhorse of the well-established AMLCD technology, and thus it will have several advantages if it can be adapted for use in flexible electronics and display manufacturing applications. However, for AMOLED applications, currently, a-Si TFT does have some issues that include the following:

- (1) Low TFT mobility ($\mu_{fe} \sim 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) which requires use of TFTs with a large W/L (W and L are the TFT channel width and length, respectively) ratio to achieve the desired pixel drive current. This results in a reduced pixel aperture ratio, and thus reduced pixel luminance in bottom emission OLED displays. As OLED materials and devices with improved efficiency are developed, this will be less of an issue. Top emission OLED pixel architecture alleviates this problem completely.
- (2) The low mobility does not allow integration of the row and column drivers on the display glass.
- (3) Only NMOS TFTs are available in a-Si, which restrict the choice of pixel circuit designs.
- (4) The TFT stability with respect to gate bias is poor. The impact of this is discussed in more detail below.

Table 4.4 TFT technology options for flexible displays

	DLT	Poly-Si		a-Si		Organic TFT	Oxide (e.g., ZnO)
		LTPS	ULTPS	Conventional a-Si	Low-temperature a-Si		
Process temperature (°C)	~450°C	~450°C	<200°C	~300°C	<200°C	<150°C	<200°C
Circuit type	CMOS	CMOS	CMOS	NMOS	NMOS	PMOS	NMOS
Device performance	–	–	–	–	–	–	–
– Mobility (cm ² V ^{−1} .s ^{−1})	~100	~100	~100	~1	~1	~1	~40
– Off-current	Excellent	OK	Issue	Excellent	Excellent	OK	OK?
– Uniformity	Good	Issue	Issue	Good	Good	OK	OK?
– Stability	Excellent	OK	Issue	Issue	Issue!	Issue !!	OK?
Cost	High	Medium	Medium	Low	Low	Very low?	Low
Maturity	Low	High	Low	High	Low	Very low	Very low

The conventional a-Si TFTs used in the current AMLCDs are fabricated at a typical process temperature of 300°C. Again for the obvious reason of high process temperature requirement, the conventional a-Si TFT process could not be used with the candidate plastic substrate with a process temperature limitation of less than 200°C. In recent years, significant advances have been made in the process temperature reduction, and a-Si TFTs have been successfully fabricated using low process temperatures of about 150°C [e.g., 19–21, 10], with a performance comparable to the 300°C process with respect to mobility, threshold voltage, and leakage current. However, the device stability under gate bias stress remains to be one item that needs to be improved particularly for the low-temperature processed a-Si TFTs. a-Si TFTs are known to exhibit threshold voltage, V_t , shifts under prolonged positive gate bias, particularly under higher operating temperature conditions. In AMOLED display operation, the drive TFT is typically subjected to positive gate voltage bias for the entire frame time (as opposed to only during the row address time as in an AMLCD). We will discuss this further under the next section on pixel drive electronics. One approach for increasing the a-Si TFT stability and decreasing the propensity for V_t shift is to reduce the display operating voltages and pixel current drive requirements. The recent progress in OLED materials toward lower drive voltages and pixel current requirements is very encouraging.

As opposed to fabricating the TFT backplane on a self-supporting flexible substrate, an alternate method involves bonding the flexible substrate to a rigid carrier substrate such as glass using a temporary adhesive, prior to the TFT array fabrication, for ease of handling during TFT array fabrication. After the TFT array is fabricated, the flexible substrate with the backplane circuit is separated from the temporary adhesive (and the carrier substrate). The issues in this approach include (1) temperature constraints imposed by the temporary adhesive, (2) potential chemical contamination by the temporary adhesive during the TFT processing, (3) yield of the bonding and debonding (of the flexible substrate/backplane from the rigid carrier substrate) operations with complete removal of the temporary adhesive, (4) cost of the bonding and debonding operations, and (5) cost of the temporary substrate if it is not reuseable.

An interesting variation of this approach is being developed by Philips, [22] which involves a-Si TFT backplane fabrication on a polyimide foil (10- μm -thick flexible substrate) that is spin coated on a rigid glass substrate. This process is named as the EPLaR (Electronics on Plastic by Laser Release) process. This process involves two extra process steps compared to a conventional a-Si TFT process on a rigid glass substrate. The first is an additive process of spin coating a 10- μm -thick polyimide layer (which subsequently becomes the self-supporting flexible substrate/backplane). The second is the laser release process. The temperature capability of this polyimide layer exceeds the requirements of the conventional a-Si TFT process; thus it can be processed in conventional a-Si TFT backplane fabrication facilities using standard processes. EPD media is then laminated to the TFT backplane, and the resulting display on the polyimide foil is then separated from the rigid carrier glass substrate, by a laser release process, which relies on the

appropriate glass surface treatments prior to the polyimide spin coating, and use of the appropriate type of polyimide. Flexible EPDs have been demonstrated using this process. This process has a potential to be adopted for the LTPS backplanes as well, and for other display media such as an OLED as well.

Direct fabrication on the self-supporting flexible substrate (i.e., without the use of a carrier substrate) is expected to have a lower cost, and has the advantage of a relatively easier transition to a roll-to-roll (RTR) process. However, due to the limited process temperature capability of the PEN substrate, development of a low-temperature plastic compatible a-Si TFT processes are required, and this is discussed in Section 4.2.2.1.

Currently, there is a lot of interest in the development of organic electronics involving TFTs fabricated using organic semiconductors. O-TFTs have the advantage of very low process temperature, and they could be fabricated using low-cost solution processing methods (e.g., spin coating, ink-jet printing, etc.) instead of the more expensive vacuum-based thin-film deposition methods. To date OTFTs fabricated using vacuum-deposited pentacene as the organic semiconductor have shown the best performance [e.g., 23] with a field-effect mobility of over $2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, near zero V_t , and “on”–“off” current ratio of over 10^8 . However, the solution processable organic semiconductor-based O-TFTs have shown a mobility in the range of about $0.05 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. One major advantage of O-TFTs with complete solution processing (e.g., ink-jet printing) is that it is easier to compensate for dimensional instability of the plastic substrate during backplane processing [24]. O-TFT backplanes are beginning to be commercialized using the EPD media for some initial applications. While impressive progress is being made on this approach, this technology is still developing and not yet satisfactory for flexible OLED displays. This topic “Organic and Polymeric TFTs for Flexible Displays and Circuits” is discussed in detail in Chapter 8.

Transparent oxide semiconductors such as zinc oxide (ZnO) are beginning to be actively investigated for use in low-temperature TFT backplanes for displays [25]. ZnO is a wide bandgap (-3.3 eV at 300 K) semiconductor and has the advantage of being deposited directly in a polycrystalline phase even at room temperature (such as by RF magnetron sputtering), and thus is compatible with the currently available flexible plastic substrates. Hirao et al. achieved a field-effect mobility and threshold voltage of $50.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and 1.1 V , respectively, for ZnO TFTs and demonstrated an AMLCD display. An additional feature of ZnO TFT is its transmission in the visible range. It has an average optical transmission (including the glass substrate) of about 80% in the visible part of the spectrum. The combination of transparency, high channel mobility, and room temperature processing makes the ZnO TFT very promising for flexible and transparent electronics and display applications.

In the following, we will discuss the recent progress in low-temperature a-Si TFT technology for flexible plastic backplanes and displays.

4.2.2.1 Low-temperature a-Si TFT

The conventional a-Si TFTs used in fabricating the backplanes on glass substrates for the AMLCD displays use a typical process temperature of about 300°C. The deposition conditions such as process gas flow rates, gas pressure, and RF power for producing the SiN_x gate dielectric and the a-Si semiconductor films are optimized at this high (~300°C) temperature to achieve high-quality SiN_x and a-Si films for the TFT devices. This ~300°C processed a-Si TFT is ideally suited for use for a rigid-glass substrate based AMLCD display as a pixel switch because it has adequate mobility (on-current, I_{on}) and low leakage current (off-current, I_{off}), with an I_{on}/I_{off} ratio of over 10^7 . The TFT performance characteristics are adequate for driving an OLED pixel as well using the currently available OLED material and device architectures to achieve the desired pixel luminance. However, the issue at hand is achieving this performance in a-Si TFTs fabricated at low process temperatures that are compatible with the available flexible plastic substrates. A straightforward reduction of the TFT process temperature (without changing the other process conditions) results in degraded mobility, and higher threshold voltage, leakage current, and sensitivity to gate bias stress-induced instability.

To achieve good quality SiN_x gate dielectric film and a-Si:H film at low deposition temperatures, and thereby to fabricate a-Si TFTs at these low temperatures without degrading the mobility, threshold voltage, and leakage currents, helium (He) and/or hydrogen (H²) dilution of the process gases has been used [e.g., 21, 20, 10]. The process gas dilution coupled with optimization of the other process conditions such as gas flow rates, pressure, and RF power density of the plasma, was found to improve the electronic properties of the SiN_x gate dielectric and the a-Si semiconductor films deposited at low temperatures (~150°C). For example, Table 4.5 shows the recent literature on low-temperature (~150°C) a-Si TFT fabricated on

Table 4.5 Typical reported characteristics of low-temperature a-Si TFTs on plastic substrates

Reference	Plastic substrate	Process temperature (°C)	TFT structure	Performance
Gleskova et al. [20]	PI	150	BCE	$\mu = 0.45 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ $V_{th} = 3 \text{ V}$ $SS = 0.5 \text{ V/dec}$
Sazanov et al. [26]	PI	120	CHP	$\mu = 0.07\text{--}0.8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ $V_{th} = 4\text{--}5 \text{ V}$ $SS = 0.5 \text{ V/dec}$
Won et al. [27]	PES	150	BCE	$\mu = 0.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ $V_{th} = 0.7 \text{ V}$ $SS = 0.82 \text{ V/dec}$
Sarma et al. [28]	PEN	150	CHP	$\mu = 0.863 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ $V_{th} = 2.5 \text{ V}$

fabricated at higher process temperatures [8, 9]. Further work is required to improve the stability of a-Si TFT against the gate bias stress in the OLED display applications. In parallel, OLED pixel circuit designs that result in minimizing gate bias stress, and that compensate for small V_t drifts on the display performance are being developed [e.g., 29, 30]

4.2.3 Display Media for Flexible Displays (LCD, Reflective-EP, OLED)

For active matrix flexible displays the popular display media being considered includes liquid crystal display (LCD), electrophoretic display (EPD), and organic light-emitting diode (OLED) display. These display media also happen to be most popular ones in use or under development using flat rigid glass substrates.

4.2.3.1 LCD Media

One of the significant issues with the use of LCD media for flexible displays is the LC (liquid crystal) cell gap control. LC cell gap value has a significant effect on the display optical performance (luminance, contrast ratio, viewing angle, etc.), and maintaining this cell gap is difficult as the display is bent or flexed. Second, the high performance transmissive LCD mode displays require a backlight that needs to be flexible and color filter array that needs to be fabricated on a flexible substrate as well. Reflective LCD mode does not require a backlight, and offers the opportunity for lower power operation for daytime use. However, it would need to be frontlit for night-time viewing, thereby giving up the advantage of lower power mode of operation. Some reflective LCD modes such as cholesteric mode [31] are bistable and do not require any power except when updating the image on the display, and thus have the ultimate low-power potential. However, the bistable LCDs are typically slow responding with a response time of the order of ~ 100 ms, and thus are not suitable for video applications

4.2.3.2 Electrophoretic Display Media

EPD is a reflective bistable (low-power) display that does not have the cell gap control issues as in LCDs. Recently, significant advances are made in the EPD [e.g., 32] technology in reducing the drive voltage, and improving the response time. However, response time in the present practical devices is still in the ~ 100 ms range and does not support video applications. Further, additional work remains to be done for realizing a viable color capable EPD. However, because the requirements of a barrier layer (for protection of the EPD media) and the requirements of the active matrix TFT backplane (for driving the EPD pixel) are not stringent, and the simplicity of the monochrome reflective, bistable EPD technology, currently several companies are actively commercializing flexible displays using this display media,

for applications such as e-books. We will discuss the recent status of these types of flexible displays in Section 4.5.

4.2.3.3 OLED Display Media

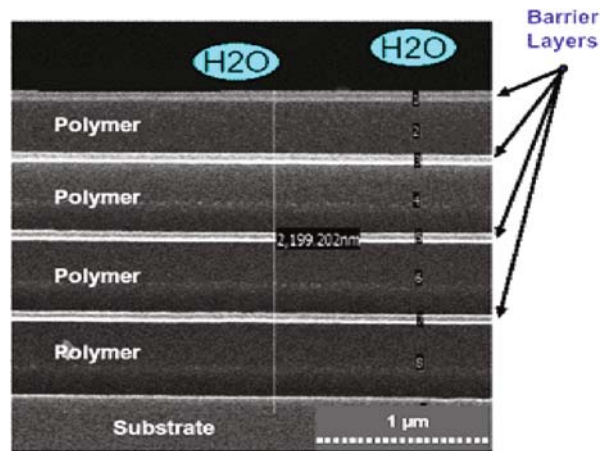
AMOLED display technology offers significant advantages over the current well-entrenched AMLCD with respect to superior image quality with wide viewing angle and fast response time, being lighter and thinner, lower cost (does not need back-light or color filters), and lower power. Because of this, many companies are actively developing and beginning to commercialize the AMOLED displays built using rigid flat glass substrates. Also, OLED media is believed to be natural choice for use in a flexible display as it represents the ultimate flexible display with a rugged solid-state display media and other attributes including full color, superior image quality, full-motion video, and low power. However, the OLED display media has very stringent requirements with respect to both the barrier layer specifications and the active matrix TFT backplane performance. Due to the long-term potential of flexible OLED displays, there is considerable interest in developing this technology. Also, OLED display application for flexible a-Si TFT backplanes is the focus of this chapter.

4.2.4 Barrier Layers

Lack of impermeability to moisture and oxygen is a serious deficiency of all the plastic substrates for the flexible display applications. All display media including LCDs, EPDs, and OLEDs degrade when exposed to oxygen and moisture in the ambient, even though at different rates with OLED having the most sensitivity to moisture and oxygen. For example, for the protection of an OLED display the plastic substrate (barrier layer) must have a permeability of less than 10^{-6} gm/m²/day for moisture and 10^{-5} mL/m²/day for oxygen. In comparison, LCD displays have a barrier requirement of 10^{-2} gm/m²/day for both oxygen and moisture, which is significantly less stringent compared to OLEDs. The base plastic substrates typically have about 10 gm/m²/day transmission rates for both oxygen and moisture, implying the need for incorporating a separate barrier layer.

In principle, a thin layer of an inorganic film such as SiO₂, SiN_x, and Al₂O₃ deposited on the flexible plastic substrate can serve as a barrier layer with the required impermeability to oxygen and moisture. However, in practice multilayer barrier film structures are believed to be required to counter the effects of the pinholes/cracks in single layer deposited barrier layers. Several organizations are currently developing optically transparent multilayer barrier coatings for flexible OLED displays [33]. Vitex Systems [34] uses such kind of an approach for their barrier film called BarixTM, which employs alternating layers of a polymer and a ceramic inorganic barrier coatings applied in vacuum, as shown in Fig. 4.4. The inorganic films serve as barrier films for oxygen and moisture, organic layers serve the planarization/smoothing function, and multilayers provide redundancy against

Fig. 4.4 Vitex barrier comprising a multilayer stack of organic and inorganic films [34]



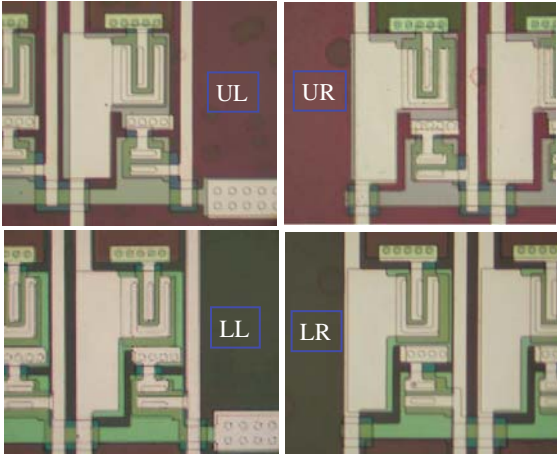
pinhole defects in the barrier films. The BarixTM layer is found to be an effective barrier layer, by minimizing the detrimental effects of pinholes and diffusion at grain boundaries. The film is about 3 μm thick and consists of about 500 Å thick Al₂O₃ ceramic films sandwiched between UV-cured acrylate films. BarixTM films were found to have water permeability in the range of 10⁻⁶ gm m⁻² day⁻¹.

Note that whether using a plastic substrate or a stainless steel substrate, the top side of the OLED must be protected with an impermeable encapsulation (barrier) layer.

4.3 Flexible Active Matrix Backplane Requirements for OLED Displays

As with LCDs, OLEDs can be addressed by either the passive matrix or the active matrix scheme. Passive matrix displays are the simplest to manufacture. The row and column addressing buses are connected directly to the cathode and anode terminals of the OLED pixel at the intersection of each row and column. Because the duty cycle of the pixel scales inversely with the number of rows, N , in the display to be addressed, the peak luminance, L_{peak} , has to increase to achieve the desired average pixel luminance, L_{av} ($L_{\text{av}} = L_{\text{peak}}/N$) as the display resolution increases. This results in a higher current density (higher voltage) operation for the OLED device, and a consequent decrease in OLED efficiency (and increase in power consumption) and shorter lifetime. In addition, the large currents cause significant voltage drops along the addressing bus lines resulting in display luminance nonuniformities. These issues limit the display resolution to perhaps less than QVGA resolution and maximum size achievable in passive matrix addressed OLEDs to less than 5 in. in size. Significant improvements in OLED efficiency and lifetime, at high luminance levels can somewhat alleviate but not eliminate the limitations to the passive matrix addressed OLED displays.

Fig. 4.9 Photograph illustrating that sufficient alignment accuracy is achieved at the four extreme regions of the fabricated $160\times160(\times3)$ pixel backplane for proper functioning of the backplane



4.4.2 Flexible OLED Display Fabrication

Table 4.6 shows the salient design features of the 64×64 pixel test display designed and fabricated. The basic design features of the $160\times160(\times3)$ pixel test display are similar to the ones in Table 4.6 except for a subpixel pitch of $100\text{ }\mu\text{m}\times300\text{ }\mu\text{m}$ and an active display area of $48\text{ mm}\times48\text{ mm}$ with an 80 cgpi resolution.

The OLED device fabrication involves first spin coating of a hole transport layer (PDOT) on the backplane. This is followed by spin coating of a yellow polymer emitter layer. Then a low work function cathode metal is evaporated through a shadow mask to achieve the desired cathode pattern on the active matrix substrate. This structure is then laminated to a cover glass with an adhesive to protect the OLED from the ambient oxygen and the moisture. Starting from coating of the fully processed active matrix backplane with PDOT until the completion of the display including the glass substrate lamination, all the processing is done inside a glove box with an inert ambient to exclude exposure of oxygen and moisture from the OLED structure.

Table 4.6 Specifications for the 64×64 pixel test display

Display resolution	64×64 pixels
Color	Monochrome yellow
Pixel pitch	80 dpi – $300\text{ }\mu\text{m}\times300\text{ }\mu\text{m}$
Active area	$19.2\text{ mm}\times19.2\text{ mm}$
Active matrix element	150°C a-Si TFT, inverted-staggered structure, CHP type
AMOLED pixel design	Two TFTs/pixel, voltage-programmed current drive
Backplane processing	Seven mask process
Display driving	External row/column drivers
Gray scale	Analog

Fig. 4.10 $160 \times 160 (\times 3)$ pixel display connected to the COF column drivers and flex cable connected to a row driver board



Appropriate drive electronics are designed to exercise and evaluate each test display. Both the test displays utilized a conventional AMLCD COTS row driver. Since no suitable commercial grayscale driver was available for a display of only 64 columns, a simple 64-channel sample and hold (S/H) circuit was devised for the column driver. For the $160 \times 160 (\times 3)$ pixel test display, an AMLCD-type column driver is used with a chip-on-flex (COF) implementation. The source drivers provide 8-bit voltage control to the display. The COF column drivers and a flex cable for the row driver board are then bonded to the column and row bus pads on the display with heat seal connections, to complete the display assembly as shown in Fig. 4.10. The display assembly is then connected to the display electronics system for test and evaluation.

Figure 4.11 shows the photographs of test images in the 64×64 pixel displays fabricated. As seen in Fig 4.11, while these display have some pixel and line defects, they are found to function as designed, validating the 150°C a-Si TFT process and the backplane design. The fabricated displays are found to be capable of displaying

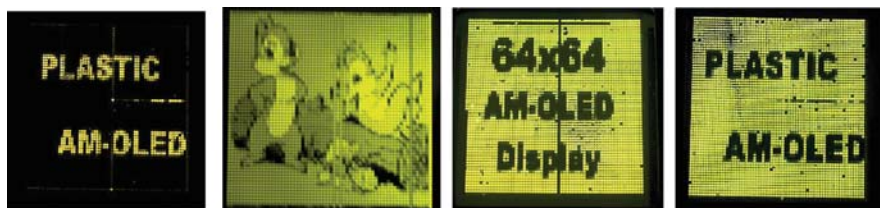


Fig. 4.11 Photographs of test images being displayed on a 64×64 pixel AMOLED fabricated using a flexible PEN plastic backplane built with low-temperature a-Si TFTs

Fig. 4.12 Photograph of a text image being displayed on a $160(\times 3) \times 160$ pixel AMOLED fabricated using a flexible PEN plastic backplane built with low-temperature a-Si TFTs



grayscale images and full-motion video. In general, the control displays fabricated using glass substrates were found to perform similarly except for having fewer pixel and line defects. The surface quality of the PEN plastic substrate was found to have a significant impact on the quality of the displays fabricated with respect to pixel and line defects observed. Displays fabricated on PEN substrates with improved surface quality exhibited significantly fewer display defects.

Similarly, Fig 4.12 shows a photograph of a text image on a $160(\times 3) \times 160$ pixel display. While this backplane was designed for a full-color display with R, G, and B pixels, only a monochrome (yellow) OLED media is used for the display fabrication to verify the design and fabrication of the backplane with 80 cgpi resolution. Complete functionality of this display does verify the feasibility of fabrication flexible OLED displays with this resolution.

4.4.3 Flexible AMOLED Display Fabrication with Thin-film Encapsulation

After verifying the feasibility of the low-temperature a-Si TFT backplanes for driving OLED displays using the displays encapsulated using glass substrates, Sarma et al. fabricated flexible AMOLED test displays using the same backplane designs, and OLED processing but using Barix thin-film encapsulation [34] for the OLED device protection. Figure 4.13 shows [36] a schematic cross section of the AMOLED display fabricated. The Barix (barrier film) is of the order of only a few microns. Thus, the thickness of the flexible display fabricated is about $\sim 130 \mu\text{m}$. Figure 4.14 [36] shows photographs of a flexible AMOLED test display fabricated along with its flexural capabilities. The fabricated displays were found to function essentially similar to the test displays in Figs. 4.11 and 4.12 using the glass substrate lamination. While systematic long-term lifetime measurements were not made, the general lifetime observations on the fabricated flexible OLED displays indicated the effectiveness of the thin-film encapsulation on the display lifetime.

The flexible display evaluations highlighted handling issues for the backplanes and displays during fabrication and subsequent use. The flexible displays can

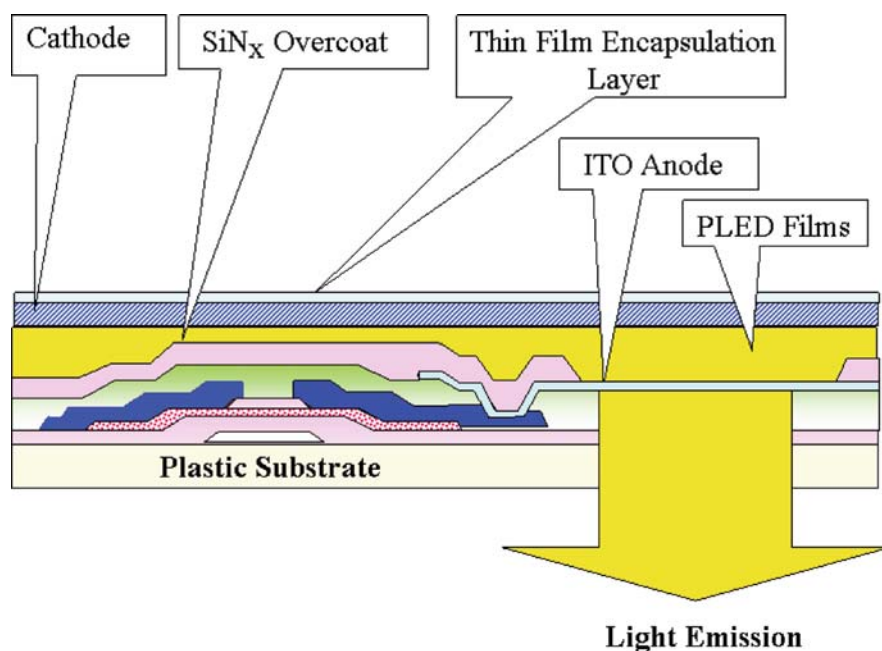


Fig. 4.13 Schematic cross section through the AMOLED test display with thin-film encapsulation

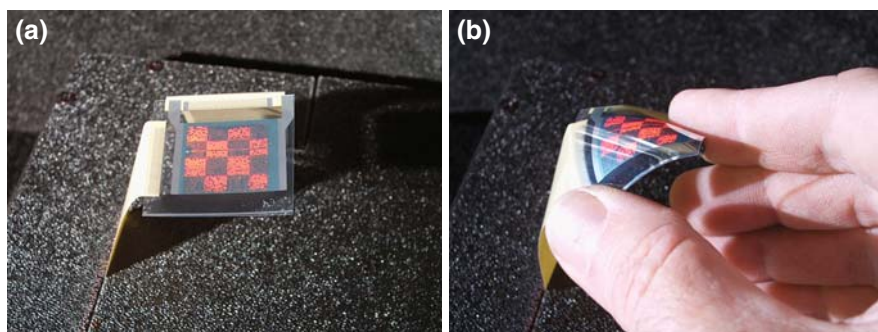


Fig. 4.14 Photographs of (a) a checker board image being displayed on a 64×64 pixel AMOLED fabricated using a flexible PEN plastic backplane built with low-temperature a-Si TFTs and thin-film encapsulation and (b) its flexural capability

tolerate flexing up to a critical minimum bend radius. However, when the backplanes and display get bent with a bend radius smaller than the critical value, it leads to cracking of the overcoat layer on the plastic substrate, and this crack can propagate through the address bus lines. The cracked bus structures cause the displays to exhibit intermittent line failures, gross line failures, or large regions of nonfunctioning areas in the display including complete display failure. The cracking can

occur during the backplane or display fabrication if the substrate gets bent by more than the critical radius. Thus, it is essential to have appropriate tooling and fixturing during fabrication to ensure successful fabrication.

The results on the backplane and OLED display fabrication and evaluation indicate the feasibility of fabricating $160 \times 160 (\times 3)$ displays with an 80-cgpi resolution and $48 \text{ mm} \times 48 \text{ mm}$ active area, using low-temperature a-Si TFT backplanes on PEN plastic substrates. Using this approach, it should be possible to fabricate large-size flexible AMOLED displays with higher resolutions (e.g., ~ 120 cgpi) by further improvements in the dimensional stability of the plastic substrates and by using a top emission OLED device architecture. In addition, further reductions in a-Si TFT backplane fabrication temperature and use of next generation alignment/lithography tools with substrate distortion compensation capability can further extend the size range of the flexible displays that can be fabricated using the PEN plastic substrates.

4.5 Flexible Electrophoretic Displays Fabricated using a-Si TFT Backplanes

While the focus of this chapter has been on low-temperature a-Si TFT backplanes on flexible plastic substrates for fabricating flexible OLED displays, for the sake of completeness, we will discuss status of the application of these same backplanes for fabricating EPDs.

Recently, significant progress has been made in adapting EPD media to the low-temperature a-Si TFT fabricated on flexible plastic substrates. EPD media is generally viewed as the logical first choice for the development and commercialization of flexible displays, as the requirements of the TFT backplane performance as well as the barrier layer performance are not stringent compared to the OLED display media. Figure 4.15 shows a photograph of a flexible Active Matrix Electro-Phoretic Display (AMEPD) [11] fabricated using 120°C a-Si TFT backplane on a flexible PEN plastic substrate. This is a $14.3''$ (A4 size) display with a 1280×900 pixel resolution with a $\pm 15 \text{ V}$ drive. While this is a monochrome display, it is targeted for the e-book applications.

4.6 Outlook for Low-Temperature a-Si TFT for Flexible Electronics Manufacturing

The advances in computers, communications, and displays, and the systems and applications enabled by these advances in recent years have been nothing short of revolutionary. Display is a central part and a significant enabler of these revolutionary advances. The recent developments in flat panel displays, and more particularly the active matrix TFT displays, have been extraordinary, having enabled applications that would not have been possible without them. Now active matrix TFT-LCDs are ubiquitous. The value proposition is compelling for replacing the

Chapter 5

Flexible Transition Metal Oxide Electronics and Imprint Lithography

Warren B. Jackson

5.1 Introduction

The previous chapters have discussed inorganic low-deposition temperature materials suitable for flexible applications, such as amorphous and nano-crystalline-silicon (Si) and organic conductors. This chapter presents the results of a recently developed inorganic low-temperature materials system, transition metal oxides (TMOs), that appears to be a very promising, new high-performance flexible electronic materials system. An equally, if not more, important part of this chapter, is the presentation of self-aligned imprint lithography (SAIL) a new fabrication method for flexible substrates that solves the layer-to-layer alignment problem.

The new *materials* system is TMO based consisting of one or more transition metals and oxygen. Some of the more common examples include zinc oxide, zinc tin oxide (ZTO), indium gallium zinc oxide (IGZO) and zinc indium oxide (ZIO). These low-temperature amorphous materials can form the active material for transistors with a performance that significantly exceeds that of amorphous and nanocrystalline Si and approaches that of larger grain poly-Si without the complexities and uncontrolled variability of polycrystalline materials. Thus, this technology can be used to drive organic light-emitting diodes (OLEDs) as well as create electronic circuits, such as shift registers, ring oscillators, and multiplexers on chip. An added feature is the possibility of creating transparent electronics with such materials systems. The entire transistor including the electrodes and the active material can have visible transmittances of 70% or greater. Thus, for applications such as displays, the active electronics would not impact the visual appearance of device and the fill factor of displays with such electronics could approach 100%. Finally, there is the possibility of creating p-type transistors that would permit fabrication of complementary metal oxide semiconductor (CMOS) circuits for flexible applications. Hence, the TMO material system possesses a number of intriguing new possible applications.

W.B. Jackson (✉)

Hewlett-Packard Laboratories, 1501 Page Mill Road, Mail Stop 1198, Palo Alto, CA 94304, USA
e-mail: warren.jackson@hp.com

For the purposes of this chapter, the most remarkable feature of the TMO transistors is that these features and performance can be achieved in devices with a maximum processing temperature that is compatible with flexible polymer substrates, such as polyimide (Glass transition temperature (T_g) = 300°C) and polyethylene naphthalate (PEN) (T_g = 200°C). Although most metal oxide work published thus far has been accomplished on higher temperature and rigid substrates, such as glass and c-Si, recent work has demonstrated large mobilities for flexible metal oxide transistors using photolithography and standard batch etching processes. However, flexible substrates are not dimensionally fixed during processing, making it virtually impossible to have precise layer-to-layer micron-scale alignment for large dimensionally variable substrates. This important problem of layer-to-layer registration on flexible substrates has been solved using SAIL, a solution that extends the TMO technology as well as amorphous and poly-Si to higher performance short channel devices.

This chapter presents the results in the field of TMO transistors relevant for the emerging field of flexible electronics in the following sections:

- (1) A brief discussion of the history of work and background information in the general area of metal oxide transistors relevant for flexible electronics.
- (2) The general properties of some of the leading TMO materials.
- (3) The device structures used in TMO and flexible electronics along with a description of SAIL
- (4) One of the most important sections presents SAIL and amorphous silicon (a-Si) results, indicating that the method can fabricate working devices.
- (5) Resulting TMO thin-film transistors (TFTs) on rigid substrates using shadow masks and photolithography on both flexible and rigid substrates along with TMO SAIL results on rigid substrates
- (6) Finally, future areas of research for improved large-area flexible electronics.

5.2 Previous Work

TMO materials have been used in transistors for quite some time. One of the first ZnO transistors was made in the 1960s [1]. However, little progress ensued using TMOs as semiconductors although ZnO found uses in surface acoustic devices [2], varistors [3], transparent PN diodes [4], and as a transparent conductor [5]. Interest in ZnO as transistors was revived in about 1997 by Prins et al. [6] and later in Kawasaki et al. and Ohtomo et al. [7, 8], where transistors with mobilities of $100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were fabricated using spin-on glass as the insulator on glass substrates. Subsequently, there have been many different experiments investigating various aspects of metal oxide transistors.

The current interest in TMO transistors started with Ohya et al. [9] and in the thesis by R. Hoffman 2002 [10], Masuda [11], Nomura [12], Hoffman [13], Nishii

Table 5.2 Electronic properties of Zn TMOs

Material	E_g (eV)	μ_H ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	ρ (Ωcm)	n (carriers cm^{-3})	References
ZnO	3.2–3.3	5–50	10^{-4}	10^{21}	[38–40]
ZnSnO ₃	3.5	7–12	5×10^{-3}	10^{20}	[40–42]
Zn ₂ SnO ₄	3.3–3.9	12–26	$1-5 \times 10^{-2}$	$6-30 \times 10^{18}$	[43–45]
Zn ₂ In ₂ O ₅	2.9	12–20	$1-4 \times 10^{-3}$	3.6×10^{20}	[43, 40, 46]
ZnInGaO	3.0	10		10^{20}	[29]

10^5 , and $V_T = 3.2$ V. These devices were deposited using electron beam evaporation through shadow masks. The ALD deposited dielectrics of these transistors are difficult to migrate to a production environment. More recently, ZTO transistors deposited on polyimide using shadow mask patterning have achieved mobilities of $15 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, on–off ratios of 10^6 , on-currents as high as 1.5 mA, and threshold voltages of -17 V [26]. These devices have been obtained using typical production compatible dielectrics such as radio frequency (RF) discharge produced SiN, SiO₂, and SiON, and shadow mask patterning, and processing temperatures below 250°C. This work highlighted the need for appropriate contacts such as indium tin oxide (ITO) or Al for high-current applications. Recent work has also been made on applying more flexible substrate-appropriate patterning methods such as SAIL for ZTO [28]. Issues such as channel length scaling and contact resistance have been investigated.

5.3 Properties of Transistor Materials

5.3.1 Semiconductors

The TMO materials space has many possible combinations of transition metals and oxygen each with a unique combination of electronic and materials properties. Many of these combinations in the TMO material space have not been fully investigated particularly the various ternary compounds (those with two or more transition metals). The Zn-based compounds however, are currently generating the most interest and serve as a good representative subclass of the larger TMO group.

The properties of ZnO and related compounds are shown in Table 5.2. The valence band is formed by hybridized Zn $4d$ levels and O $2p$ levels. The conduction band is formed predominantly by Zn $4s$ levels. The bandgap is direct and has a value of 3.2–3.3 eV for ZnO and increases to 3.5–3.9 eV with the addition of Sn (Table 5.2). The addition of In tends to lower the bandgap to 2.9 eV. These values are large enough that the material is transparent without much coloration. Hence, they make good candidates for transparent electronics.

The properties of TMOs make them uniquely suited for flexible electronics where low-temperature non-single crystalline materials must be used. The Hall mobility

(μ_H) of single crystalline ZnO is $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and the saturation velocity is large, making high-mobility devices feasible. The measured Hall mobilities in amorphous TMOs are around $5\text{--}50 \text{ cm}^2 \text{ V}^{-1} \text{ cm}^{-1}$, and the achieved field effect mobilities are roughly of comparable magnitude (Table 5.2). With field effect mobilities of $10\text{--}100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, milliamp on-currents for flexible devices are obtainable using typical TFT parameters. The high mobility for electrons in the disordered amorphous TMOs arises because of the overlap of the nondirectional 4s orbitals of Zn (or other transition metal cations) creating a conduction band regardless of the angle between nearest neighbors (Fig. 5.2). Hence, the mobility is relatively unaffected by

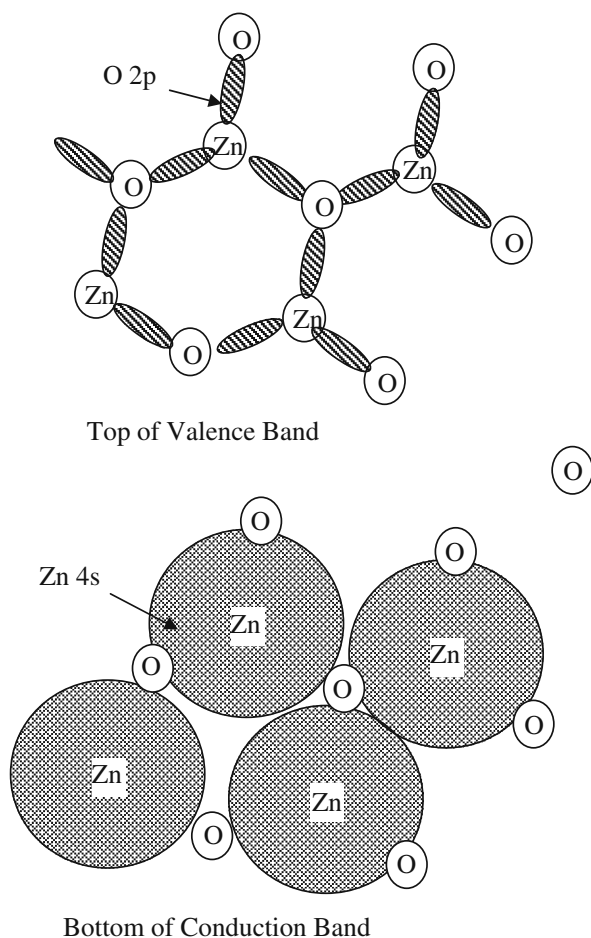


Fig. 5.2 Schematic of electron wavefunction structure for the *top* of the valence band (primarily O 2p) and the *bottom* of the conduction band (Zn 4s). The large overlap with neighboring Zn and spherical symmetry of the Zn 4s levels minimize sensitivity to disorder for the conduction band

Table 5.3 Various miscellaneous properties of ZnO [50]

Density (g cm ⁻³)	5.6
Dielectric constant	8.6
Refractive index	2.0
Average thermal expansion Coeff. (/K)	4×10 ⁻⁶

bond angle disorder. Moreover, the ionic nature of the transition metal oxide bonds causes the bonds to be less directional than the typical covalent bonds found in the usual Group IV or III–V semiconductors. Therefore, the large bond angle distortions found at grain boundaries are less apt to result in grain boundary gap state defects. The lack of gap states associated with deformed bonds results in large subthreshold slopes and small turn-on voltages in low-temperature transistors.

A further consequence of the lack of bandgap states and high electron mobility is that the materials often can be easily degenerately doped n type yielding small resistivities, ρ , below 10⁻² (Ω cm) (Table 5.2). The doping of ZnO occurs by substitutional dopants, Zn interstitials, O vacancies, and/or interstitial H. The typical substitutional dopants include N and P. Oxygen vacancies are used to make the materials highly conductive for use as transparent electrodes for solar cell and photosensor applications. The oxygen vacancies can readily be created by sputtering in an O poor atmosphere. In fact, in TMO transistor fabrication, care must be taken to keep the O-vacancy concentration low so that the channel is sufficiently resistive for enhancement mode transistor operation [15, 22]. There is increasing evidence that the O vacancies may be somewhat mobile resulting in some long-term device instabilities to be discussed later.

There also is evidence that H interstitials act as n-type dopants [47–49]. Exposure of semiconducting ZTO to an H plasma results in a significant enhancement of the conductivity while exposure to an Ar or O plasma does not. Moreover, the H diffusion rate is large even at 200°C. Thus, unintentional H doping during fabrication etching is a concern and must be controlled.

Other useful parameters for ZnO are shown in Table 5.3 [50]. Note that the dielectric constant is somewhat lower than that of a-Si. The values for other TMO are generally similar in magnitude.

5.3.2 Dielectrics

Dielectrics are often one of the most critical materials necessary for a transistor technology. In most electronic applications, shorts are extremely undesirable defects, particularly in array applications. Shorts not only cause the shorted device to fail but often result in failure of any connected device and cause an unacceptable power drain. They also mask failures by other devices. In addition to the highly

Table 5.4 Various dielectrics used in TMO transistor technology [10, 18]

Insulator	E_g (eV)	Relative dielectric constant	Breakdown field (MV/cm)
SiO ₂	11	3.8	6
SiN	9	7	9
Al ₂ O ₃	9.5	8	3.5–6
BaTa ₂ O ₅		22	3.5
HfO ₂	5.8	16	3
Ta ₂ O ₅	4.6	24	1.5–3
TiO ₂	3.7	60	0.2
Y ₂ O ₃	5.6	12	4
ZrO ₂	5	19.8	

deleterious effect of shorts, typical large-area applications consist of many devices and crossovers requiring a highly reliable dielectric. Dielectrics that have been successfully used for TMO TFTs are included in Table 5.4 [10, 18]. The dielectrics currently being used in large-area electronics, such as SiO₂ and SiN work reasonably well for TMO devices. Typically, if SiN is used, a thin SiO₂ buffer layer is used so that the SiN does not directly contact the TMO. One unresolved issue is that the presence of large amounts of H may be one of the problems with SiN in direct contact with the TMO [51]. More recently, evidence has emerged that O vacancies can be created during long-term operation of TMO transistors and result in long-term instability [52–56]. There is possible evidence that the silicon-based oxides are more reactive in creating vacancies. As a result there is interest in less reactive oxides, such as Y₂O₃, Al₂O₃, Ta₂O₅, and HfO₂ dielectrics [25, 29, 30, 36, 12]. These oxides have the advantage of having high dielectric constants as well as possibly generating fewer O-vacancy related instabilities. It is not yet clear whether the instability is actually O vacancies or rather H associated with the various dielectrics or due to the motion of metal interstitials. Hence, low H dielectrics may be necessary to solve the instability problem.

5.3.3 Contact Materials

The contact materials needed for TMO have not been completely investigated at this point. For many TMO systems, the metal–TMO contact has been sufficiently conductive to yield high-current devices. However, as shown in the section below, insertion of an intermediate layer between the metal and the TMO can result in significant decrease in the contact resistance. The metals Al, Ti, and TiW make reasonable contacts capable of making devices with more than 1 $\mu\text{A}/(\text{W/L})$ on-current per W/L. The current can be significantly increased, however, if a layer such as ITO is inserted between the TMO and the metal [26, 28]. In the case of ZTO, the ITO layer at the contact increases the on-current to 10 μA [26, 28].

5.4 Device Structures

The structures used for TMO TFTs on rigid substrates are largely the same as those used in other deposited material systems, such as a-Si. The various structures include the staggered bottom gate, collinear bottom gate, and top gate devices. Because fully versatile reproducible etching of the TMO semiconductors is still being developed, most of the early reported work has involved shadow mask structures and transistors on silicon wafers with thermal oxide. It is only recently that more fully photolithography patterned microstructures have been made.

Continuous Bottom Gate. The most prevalent structure for investigating basic material properties and the device potential of the metal oxide system is using a blanket deposited bottom gate structure (Fig. 5.3a,b). Either a layer of metal or a doped silicon wafer serves as the gate electrode. If a crystalline Si wafer is used, the dielectric is usually a thermal oxide, the source and drain electrodes are patterned on the oxidized Si wafer using either shadow masks or photolithography, and finally, the metal oxide material is deposited through a shadow mask to complete the structure. If the back contact is a continuous metal, the dielectric is a deposited dielectric and the other steps are similar to those of a silicon wafer. The shadow mask is used to define the active material to restrict current flow to a region near the contacts. Variations of this structure include the deposition of materials to improve the contact properties such as ITO or Ti. The contact material must be patterned along with the source and drain prior to deposition of metal oxide active material. Also, the contacts can be patterned first followed by deposition of the TMO as in Fig. 5.3b.

The advantages of this structure, particularly for the early phases of work with the new material systems, include the following:

- (1) The structure can be made quickly with a minimum number of steps.
- (2) The bulk dielectric is thermal Si oxide whose properties are well understood. Therefore any unusual results are solely attributable to the dielectric–metal oxide interface, the metal oxide bulk, or the contacts.
- (3) Finally, this structure can be subjected to a full range of temperatures in order to fully investigate the potential of the material system. The continuous gate devices can be deposited using shadow masks to define both the source–drain contacts as well as the TMO channel material.

Bottom gate staggered. In later work, as the ability to etch metal oxides has improved, photolithography has been used to define staggered bottom gate devices (Fig. 5.3c). In this structure, the bottom metal is patterned followed by deposition of the dielectric, the metal oxide active layer, any contact layer, and finally the contact metal. The active region around the device is patterned followed by patterning of the source and drain electrodes and any contact layer. This procedure requires precise alignment of the patterned gate and source–drain electrodes, hence the need for photolithography. The patterning of the source–drain contacts can first be followed by deposition of the semiconductor material (Fig. 5.3d).

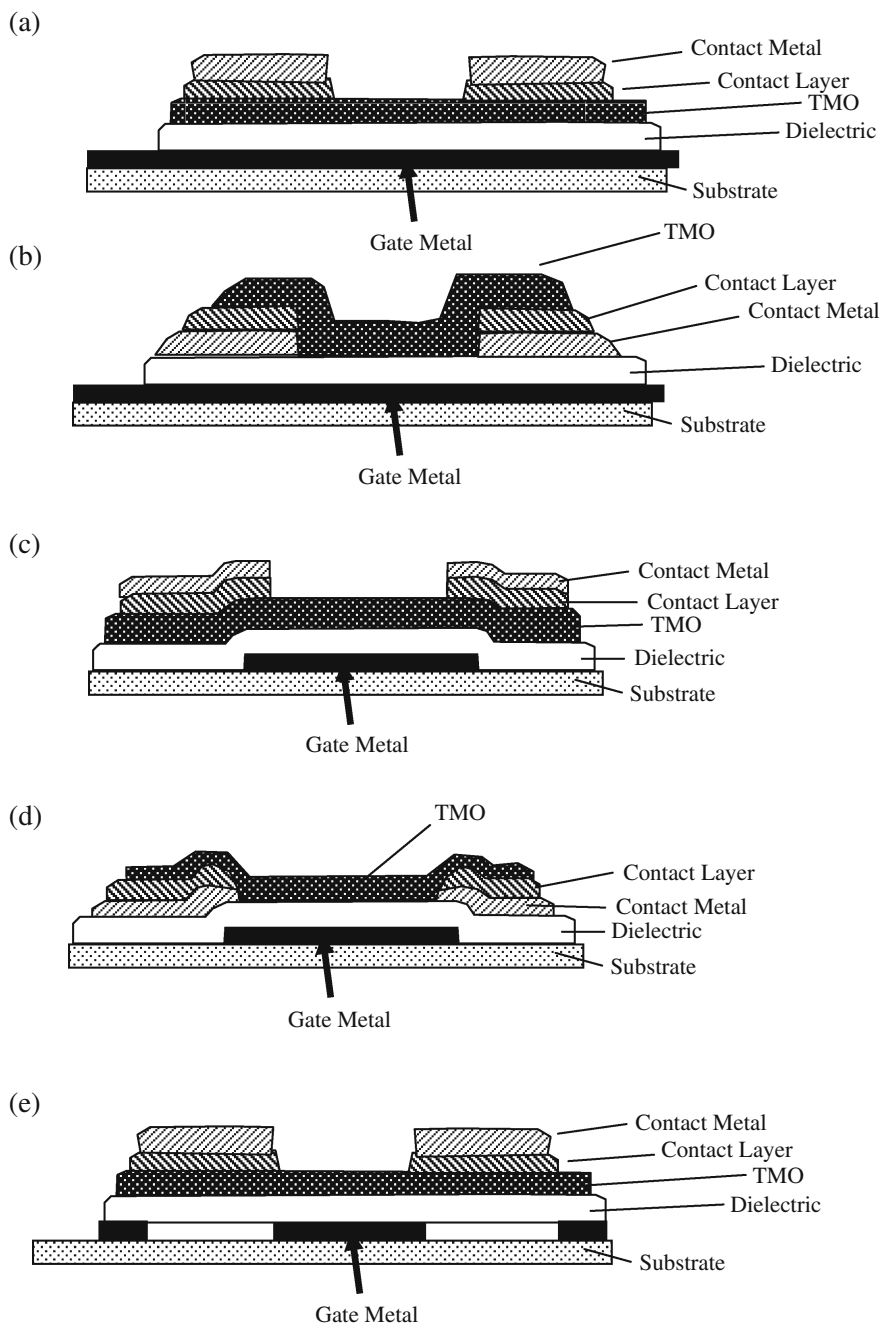


Fig. 5.3 Various transistor structures used in flexible transistors (a) continuous bottom gate staggered, (b) continuous bottom gate collinear, (c) bottom gate staggered, (d) bottom gate collinear, and (e) constant level transistor. Shadow mask for (a) and (b), photolithography for (c) and (d), and imprint lithography for (a) and (e)

5.6 Flexible TMO Device Results

The previous sections describing flexible transistor fabrication indicated that there are three main ways of fabricating TMO devices: shadow masks, photolithography, and imprint lithography. Section 5.1.2 summarized some important TMO transistor results on rigid substrates; further details can be found in Table 5.1 and the corresponding references. In this section, the performance of various flexible TMO transistors using the above-mentioned fabrication methods is described. While significant TMO work on rigid substrates has been undertaken, flexible TMO work and TMO work using imprint lithography are still in their infancy. It is expected that the TMO results on rigid substrates mentioned above represent appropriate performance benchmarks for flexible electronics because the rigid, higher temperature approaches can utilize any of the flexible technologies. Thus, the results in this section should be compared to rigid substrate results as well as alternative flexible platforms such as a-Si:H.

One of the first reports of devices fabricated on flexible substrates is by Carcia et al. [20], where a mobility of $0.4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, an on-off ratio of 10^4 , and $V_t = 7.5 \text{ V}$ was achieved. The transistor consisted of a fluoropolymer dielectric, an RF sputter deposited ZnO active layer, and a polyimide substrate and was fabricated at room temperature. The results are shown in Fig. 5.12. This work was one of the first to demonstrate that TMO TFTs could produce flexible transistors with capabilities comparable to a-Si although the off-current is a bit high. Subsequent work by these researchers using a Al_2O_3 dielectric, ZnO semiconductor, e-beam evaporation on polyimide, and temperatures below 120°C produced devices with mobilities of $50 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, on-off ratios of 10^5 , and $V_t = 3.2 \text{ V}$ [22, 37]. However, the off-current, roughly 10^{-9} A , was too high for a pixel transistor on an LCD. Such a large leakage requires unacceptably large refresh rates and concomitant power dissipation. The mobility and on-current, however, demonstrate that high-performance flexible electronics can be made using TMO as the channel material.

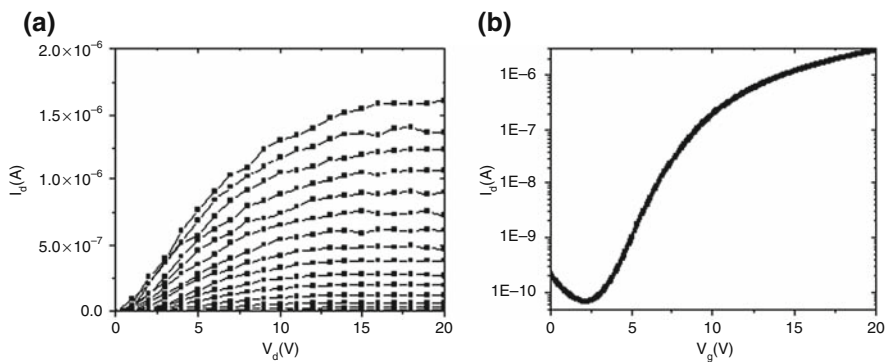


Fig. 5.12 Flexible ZnO TFT curves of (a) I_d versus V_d for $V_g = 0, 1, \dots, 20 \text{ V}$ and (b) of I_d versus V_g for $V_{ds} = 20 \text{ V}$. $W/L = 40 \mu\text{m}/400 \mu\text{m}$ from [20]

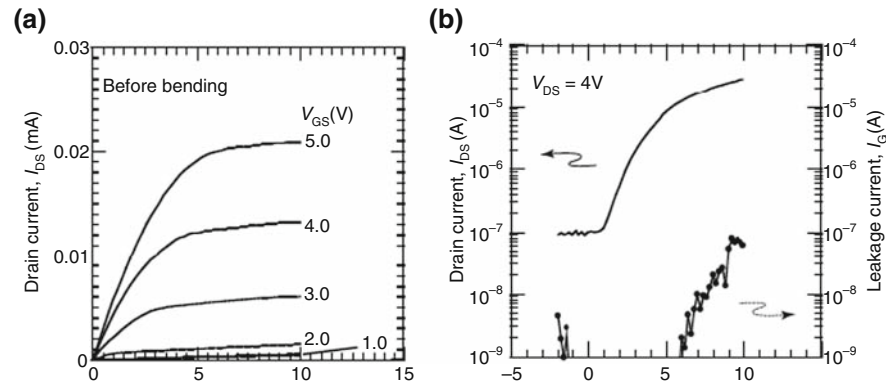


Fig. 5.13 From [29] on PET with a maximum temperature near room temperature

In [29], transistors were fabricated on PET using IGZO as the TMO and Y_2O_3 as the dielectric where the fabrication temperature was kept near room temperature (Fig. 5.13). A mobility of $8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ was achieved with an on-off ratio of 10^3 and an off-current of 10^{-7} A. Except for the large off-current this is a reasonable transistor. The importance of this work is that PET is clear unlike polyimide, so the devices could be used in principle as part of a backlit liquid crystal display (LCD). Also, this work represents an improvement of the transistor characteristics over the first flexible transistor work. These flexible TMO results are not as good as the results achieved on rigid substrates.

In order to further improve the performance of flexible TMO devices, the contacts must produce sufficient current. In Fig. 5.14, the output characteristics of a ZTO transistor on polyimide using shadow mask definition of ZTO on PECVD deposited SiON, 50- μm polyimide substrate, and a 250°C 10-min anneal [26]. The transistor output curves are shown for contacts consisting of Al on ZTO. The concave current

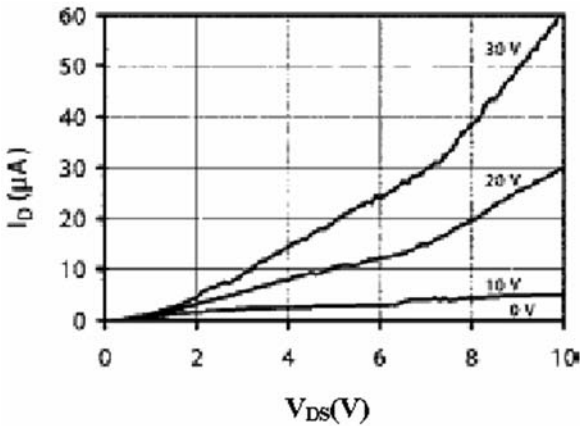
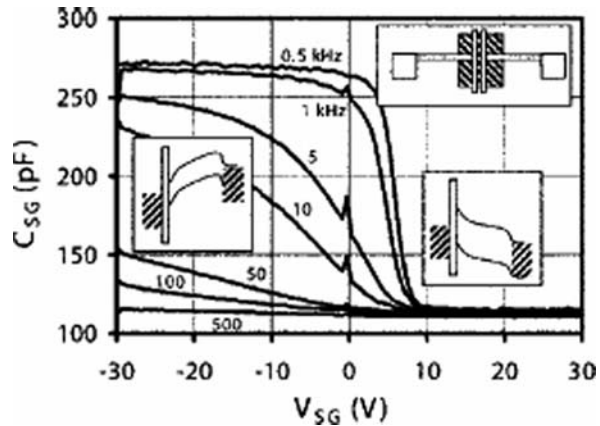


Fig. 5.14 The output characteristics for a ZTO transistor with Al contacts, SiON dielectric, and a maximum fabrication temperature of 250°C. The concave characteristics are indicative of blocking contacts and suggest that improved contacts can give rise to improved device performance [26]

Fig. 5.15 The source–gate capacitance versus dc source-to-gate voltage bias for various frequencies for the transistor with Al source and drain contacts. The measurement frequencies are 0.5, 1, 5, 10, 50, 100, and 500 kHz. The insets indicate the device layout (*upper right*) and the band structure for negative (*left*) and positive (*right*) dc bias conditions



crowding suggests that there is a problem with the contacts. This conclusion about the contacts was further verified by two methods: capacitance and four-probe transistor measurements. In Fig. 5.15, the capacitance of a transistor structure of the source with respect to the continuous gate is shown as a function of V_{sg} . The associated band structure is depicted in the insets and as well as the device geometry. For $V_{sg} > 10$, the device is in depletion and the channel does not conduct. Hence, the capacitance is just the capacitance of the source electrode with respect to the gate regardless of the frequency. For $V_{sg} < 0$ and low frequencies, the channel is turned on so that the capacitance consists of both the source–gate capacitance, the drain–gate capacitance, and the channel–gate capacitance. Moreover, the various capacitances are only the insulator capacitances and do not include the series capacitance of semiconductor. The additional area and lack of the semiconductor series capacitance result in the roughly factor of 3 increase in the capacitance. For higher frequencies, the RC time constant from contact and channel series resistances and the capacitances is large so there is not enough time within one cycle to charge up the channel–gate and drain–gate capacitances. By observing the frequency at which $AR_{contact}C_{ins}2\pi f = 1$, where A is the source–gate contact area, $R_{contact}$ is the contact resistance, C_{ins} is the insulator capacitance, and f is the frequency, the contact resistance $R_{contact}$ can be estimated. Because $C_{ins} = 15 \text{ nF/cm}^2$ the area of the device is 0.03 cm^2 and $R_{contact} \approx 30 \text{ k}\Omega$. This device is, therefore, not capable of passing much more than about $35 \mu\text{A}$ without a significant voltage drop across the contact.

A second means of estimating the contact resistance is to measure the voltage drop across the contact using a four-probe method (Fig. 5.16) [26, 28]. The source and drain probes drive a current through the source and drain contacts and the voltage of the two inner probes is measured using a very high impedance instrument, so no current is drawn through the probes. The potential difference between the source and the first contact yields the voltage drop across the source contact, while the voltage difference between the final voltage probe and the drain yields the voltage

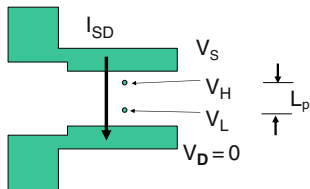


Fig. 5.16 Four-probe configuration for measuring the source and drain contact resistance. Two addition high impedance probes or electrodes are placed between the source and drain to measure the potential drop between the channel and the source and drain electrodes

drop across the drain. The potential drop between the two voltage probes yields the channel voltage drop. In particular, the channel resistance, R_{CH} , the source resistance, R_S , and the drain resistance, R_D are roughly given by

$$\begin{aligned} R_S &= (V_S - V_H)/I_{SD} \\ R_D &= V_L/I_{SD} \\ R_{CH} &= (V_H - V_L)/I_{SD} \end{aligned} \quad (1)$$

The expressions for R_S and R_D are approximate in that some channel resistances are included because the probes include at least several microns of the channel. Using these relations, the source, drain, and channel resistances can be estimated [26, 28]. For the Al and ZTO contact, this method yields approximately the same value of the contact. The four-probe method can be used to determine

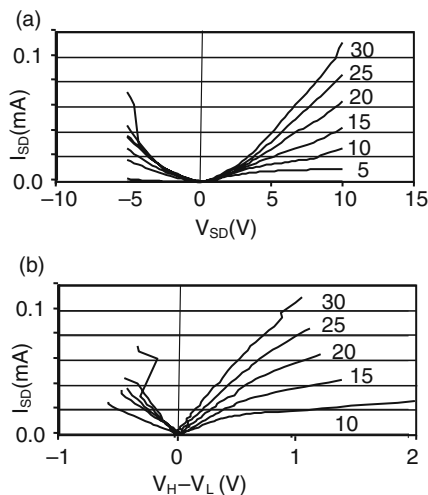


Fig. 5.17 The source–drain current in a ZTO transistor with Al contacts and no ITO layer to improve the contact resistance (a). The same current plotted against the voltage drop between the inner voltage sensing probes (b). Notice that the current crowding indicative of contact effects has been eliminated

the characteristics without contact impedance effects. In Fig. 5.17, the source–drain current through a ZTO transistor with PECVD SiON dielectric, Al contacts deposited directly on the ZTO, with $W/L = 2000 \mu\text{m}/200 \mu\text{m}$ is presented. The field effect mobility is about $0.2 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for the uncorrected curves. The normal output curves in Fig. 5.17a exhibit current crowding while plotted against the potential difference between the two electrodes eliminates the crowding (Fig. 5.17b). Notice also the difference in horizontal scales is almost a factor of 10. The mobility extracted from the contact corrected curves will, therefore, be about a factor of 10 larger and is about $1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Thus, the contact effects dramatically alter the extracted mobility. The four-probe methods enable the true channel mobility to be extracted by eliminating the contact effects. Clearly, however, the most important point is that the contacts must be improved.

By including an ITO layer between the Al and the ZTO, the contact resistance was decreased to about $3 \text{ k}\Omega$. In addition, if an oxide buffer layer is included between the SiON and the ZTO, the device performance is greatly improved. For this device the output and transfer characteristics are shown in Figs. 5.18 and 5.19. The incremental mobility is $14 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (Fig. 5.20) and the on–off ratio is 10^7 , and an off-current of 10^{-11} A was produced showing that the high off-current can be reduced while maintaining high on-currents. Moreover, this is a stable current and changes little with stressing. The threshold voltage is somewhat negative but this can be changed by adjusting the dielectric deposition conditions and/or injecting the appropriate charge into the dielectric to adjust the threshold voltage. The maximum incremental saturation mobility is $\sim 14 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (Fig. 5.20) [26, 28]. The threshold voltage is about -9 V (Fig. 5.21). In summary, the flexible transistor properties are nearly equivalent to a comparable rigid substrate device composed of similar materials. This bodes well for the future of flexible TMO devices.

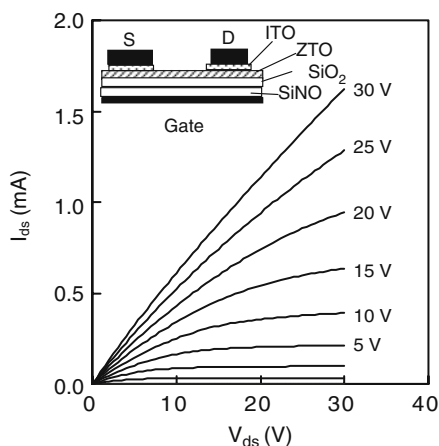


Fig. 5.18 A ZTO transistor deposited on $50 \mu\text{m}$ polyimide, PECVD SiON, ITO contact layer, Al contacts, and a SiO_2 buffer layer ($W/L = 1,000 \mu\text{m}/100 \mu\text{m}$)

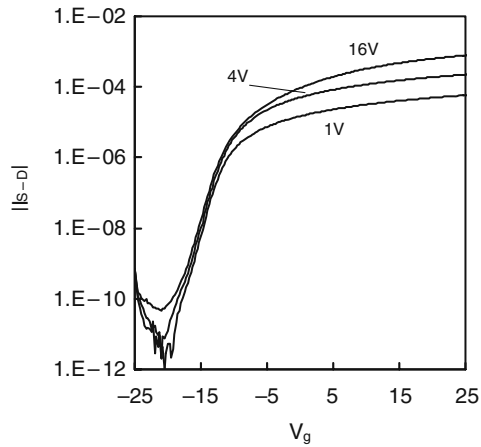


Fig. 5.19 The transfer characteristics of the device in Fig. 5.18

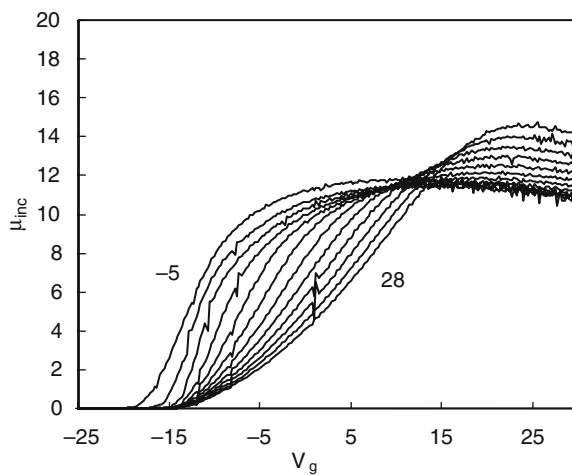


Fig. 5.20 The incremental mobility for the device in Fig. 5.18. The maximum mobility is $15 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$

5.7 Future Problems and Areas of Research

In order to realize the full promise of flexible TMO electronics, there are a number of areas in which further research is desirable. These include the following:

- (1) Better control of the carrier density in the TMO channel materials.
- (2) Improved low-temperature dielectrics.
- (3) Better etching processes for TMO materials.