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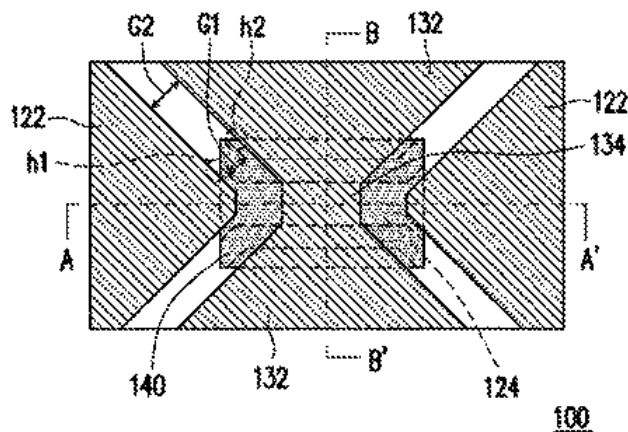
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### (54) Title of Invention

Touch Panel

### (57) Abstract

the present invention provides a touch panel, comprising a substrate, a plurality of first conductive units, a plurality of second conductive units, and a plurality of insulating patterns. Each first conductive unit comprises a plurality of first electrodes. Each second conductive unit includes a plurality of second electrodes. Each first electrode includes a first sub-electrode and a second sub-electrode sequentially stacked on a substrate. Each second electrode includes a third sub-electrode and a fourth sub-electrode sequentially stacked on a substrate. The first sub-electrode and the third sub-electrode belong to a first conductive layer, and the second sub-electrode and the fourth sub-electrode belong to a second conductive layer. The first conductive layer has a plurality of step differences. These step differences are at least located at the junction of the first conductive unit and the insulating pattern.



1. A touch panel, characterized by comprising:

A substrate;

A plurality of first conductive units arranged on the substrate, each of these units comprising a plurality of first electrodes and first connecting portions, with adjacent first electrodes electrically connected by at least one first connecting portion, and each electrode includes a first sub-electrode and a second sub-electrode stacked sequentially on the substrate.

A plurality of second conductive units are arranged on the substrate, each comprising multiple second electrodes and multiple second connecting portions. Adjacent second electrodes are electrically connected by at least one second connecting portion, and the second electrodes are composed of each a third sub-electrode and a fourth sub-electrode sequentially stacked on the substrate. The second conductive units are electrically insulated from and alternating with the first conductive units. The first connecting portions, the first sub-electrode, and the third sub-electrode belong to a first conductive layer, while the second connecting portions, the second sub-electrode, and the fourth sub-electrode belong to a second conductive layer; and

Multiple insulating patterns are arranged at the intersections of the first conductive units and the second conductive units, with the insulating patterns covering the first connection portions. Each insulating pattern covers at least one of a part of the first sub-electrode and a part of the third sub-electrode, wherein the first conductive layer has multiple step differences located at least at the junctions of the first conductive units and the insulating patterns.

2. The touch panel according to claim 1, characterized in that the step differences are located at the boundaries between the second conductive units and the insulating patterns.

3. The touch panel according to claim 1, characterized in that a portion of the step differences is located on the first sub-electrode.

4. The touch panel according to claim 1, characterized in that a portion of the step differences is located on the third sub-electrode.

5. The touch panel according to claim 1, characterized in that a portion of the step differences is located on the first connection portion.

6. The touch panel according to claim 1, characterized in that a portion of the step differences is located at the boundary between the first sub-electrode and the first connection portion.

7. The touch panel according to claim 1, characterized in that two adjacent first electrodes are electrically connected by two first connection portions.

8. The touch panel according to claim 1, characterized in that two adjacent second electrodes are electrically connected by two second connection portions.

9. The touch panel according to claim 1, characterized in that there exists a first gap between the first sub-electrode and the third sub-electrode covered by each insulating pattern, and a second gap between the first sub-electrode and the third sub-electrode not covered by each insulating pattern, wherein the first gap is different from the second gap.

10. The touch panel according to claim 9, characterized in that the first gap is smaller than the second gap.

11. The touch panel according to claim 9, characterized in that the first gap is larger than the second gap.

12. The touch panel according to claim 1, characterized in that each of the second connecting portions is disposed on one of the insulating patterns, and at least one of a portion of the second sub-electrode and a portion of the fourth sub-electrode is disposed on one of the insulating patterns.

13. The touch panel according to claim 1, characterized in that the first sub-electrode covered by each insulating pattern has a first protrusion which extends beyond the second sub-electrode, and the third sub-electrode covered by each insulating pattern has a second protrusion which extends beyond the fourth sub-electrode.

14. The touch panel according to claim 1, characterized in that the first sub-electrode covered by each insulating pattern has a first recessed portion that is recessed within the second sub-electrode, and the third sub-electrode covered by each insulating pattern has a second recessed portion that is recessed within the fourth sub-electrode.

15. The touch panel according to claim 1, characterized in that the thickness of the first conductive layer is greater than that of the second conductive layer.

16. The touch panel according to claim 15, characterized in that the first connecting portion belongs to the first conductive layer, the second connecting portion belongs to the second conductive layer, and the line width of the first connecting portion is smaller than the line width of the second connecting portion.

17. The touch panel according to claim 1, characterized in that the thickness of the first conductive layer is less than the thickness of the second conductive layer.

18. The touch panel according to claim 17, characterized in that the first connecting portion belongs to the first conductive layer, the second connecting portion belongs to the second conductive layer, and the line width of the first connecting portion is greater than the line width of the second connecting portion.

19. The touch panel according to claim 1, characterized in that the crystalline grain size of the second conductive layer is larger than that of the first conductive layer.

20. The touch panel according to claim 1, characterized in that the second gap is greater than 25 microns.

21. The touch panel according to claim 1, characterized in that it also includes a buffer layer covering the substrate and positioned between the substrate and the first conductive layer.

22. The touch panel according to claim 1, characterized in that it also includes a plurality of dummy patterns, arranged between the first electrodes and the second electrodes.

## Touch panel

### Technical field

[0001] The present invention relates to a touch panel, and more particularly to a touch panel with low conductive impedance and excellent touch sensing sensitivity.

### Background Art

[0002] A capacitive touch panel generally includes a plurality of first conductive units arranged along a first direction (e.g., vertical direction) and a plurality of second conductive units arranged along a second direction (e.g., horizontal direction). The driver of the capacitive touch panel can output driving signals to the first conductive units and receive corresponding sensing signals generated by the second conductive units, then the capacitive touch panel generates touch position signals based on the received sensing signals accordingly.

[0003] Generally speaking, the first sensing unit and the second sensing unit of a capacitive touch panel are formed from transparent conductive material. However, the resistance of transparent conductive materials typically affects the touch sensing performance of capacitive touch panels. In addition, if the conductive units are formed from non-transparent conductive materials (e.g. fine metal wires), visual issues may arise. Reducing line width to lessen visual effects may result in increased resistance and lower yield due to excessively narrow line width. Therefore, how to reduce the conduction impedance of the first and second conductive units in capacitive touch panels is a crucial topic.

### Summary of the Invention

[0004] The present invention provides a touch panel, wherein the impedance of the touch panel is low and the touch sensitivity is good.

[0005] The touch panel of the present invention includes a substrate, a plurality of first conductive units, a plurality of second conductive units, and a plurality of insulating patterns. The first conductive units are disposed on the substrate. Each first conductive unit includes a plurality of first electrodes and a plurality of first connecting portions. Two adjacent first electrodes are electrically connected by at least one first connecting portion. Each first electrode includes a first sub-electrode and a second sub-electrode sequentially stacked on a substrate. The second conductive units are disposed on the substrate. Each second conductive unit includes a plurality of second electrodes and a plurality of second connecting portions. Two adjacent second electrodes are electrically connected by at least one second connecting portion. Each second electrode includes a third sub-electrode and a fourth sub-electrode sequentially stacked on a substrate. The second conductive unit and the first conductive unit are electrically insulated from each other and staggered with each other. The first connecting portion, first sub-electrode, and third sub-electrode belong to a first conductive layer. The second connecting portion, second sub-electrode, and fourth sub-electrode belong to a second conductive layer. The insulating pattern is disposed at the staggered area between the first conductive unit and the second conductive unit. The insulating pattern covers the first connecting portion, and each insulating pattern covers at least one of a portion of the first sub-electrode and a portion of the third sub-electrode. The first conductive layer has a plurality of step differences. These step differences are located at the interface between the first conductive unit and the insulating pattern.

[0006] Based on the above, the touch panel of the present invention includes a plurality of conductive units, and each conductive unit includes a plurality of electrodes and connection portions, wherein the electrodes are composed of a double-layer conductive structure, thus possessing lower conduction impedance, thereby improving the touch sensitivity of the touch panel.

[0007] In order to illustrate the above features and advantages of the present invention more clearly, the following embodiments are provided and described in detail with the accompanying drawings.

### Brief Description of the Drawings

[0008] FIG. 1 is a top view schematic diagram of a touch panel in accordance with one embodiment of the present invention;

[0009] FIG. 2 is an detail schematic diagram of region M in FIG. 1;

- [0010] Figures 3, 4, and 5 respectively show the respective film layers in FIG. 2;
- [0011] FIG. 6 shows a cross-sectional schematic diagram along section lines A-A' and B-B' in FIG. 2;
- [0012] FIG. 7 is a top view schematic diagram of a touch panel according to another embodiment of the present invention;
- [0013] FIG. 8 is a partial top view schematic diagram of the touch panel 100 in FIG. 1;
- [0014] FIG. 9 is a cross-sectional schematic diagram along section lines C-C' of FIG. 8;
- [0015] FIG. 10 is a partial cross-sectional schematic diagram of a touch panel of another embodiment of the present invention;
- [0016] FIG. 11 is a partial top view schematic diagram of a touch panel of another embodiment of the present invention;
- [0017] FIG. 12 is a schematic diagram of the first conductive layer of the touch panel of FIG. 11;
- [0018] FIG. 13 is a schematic diagram of the first conductive layer of a touch panel of another embodiment of the present invention;
- [0019] FIG. 14 is a partial top view schematic diagram of a touch panel of another embodiment of the present invention;
- [0020] FIG. 15 is a schematic diagram of the first conductive layer of the touch panel of FIG. 14;
- [0021] FIG. 16 is a partial top view schematic diagram of a touch panel according to another embodiment of the present invention;
- [0022] FIG. 17 is a schematic diagram of the first conductive layer of the touch panel of FIG. 16;
- [0023] FIG. 18 is a partial top view schematic diagram of a touch panel according to another embodiment of the present invention;
- [0024] FIG. 19 is a schematic diagram of the first conductive layer of the touch panel of FIG. 18.
- [0025] Description of Reference Numerals:
- [0026] 100, 100a, 100b, 100c: Touch Panel;
- [0027] 110: Substrate;
- [0028] 112: Visible region;
- [0029] 114: Peripheral region;
- [0030] 120: First conductive unit;
- [0031] 122: First electrode;
- [0032] 124: First connecting portion;
- [0033] 130: Second conductive unit;
- [0034] 132: Second electrode;
- [0035] 134: Second connecting portion;
- [0036] 140: insulating pattern;
- [0037] 150: Dummy pattern;
- [0038] 160: Buffer layer;
- [0039] A-A', B-B', C-C': Section line;
- [0040] C1: First conductive layer;
- [0041] C2: Second conductive layer;
- [0042] d1: First direction;
- [0043] d2: Second direction;
- [0044] E1: First sub-electrode;
- [0045] Ela: First protruding portion;
- [0046] Elb: First recessed portion;

- [0047] E2: Second sub-electrode;
- [0048] E3: Third sub-electrode;
- [0049] E3a: Second protruding portion;
- [0050] E3b: Second recessed portion;
- [0051] E4: Fourth sub-electrode;
- [0052] G1: First gap;
- [0053] G2: Second gap;
- [0054] G: Gap;
- [0055] h1: First step difference;
- [0056] h2: Second step difference;
- [0057] M: Region;
- [0058] W1, W2: Line width.

### Detailed Embodiment

[0059] FIG. 1 is a top view schematic diagram of a touch panel According to one embodiment of the present invention. Please refer to FIG. 1, the touch panel 100 includes a substrate 110, a plurality of first conductive units 120, a plurality of second conductive units 130, and a plurality of insulating patterns 140 (shown in FIG. 2). The substrate 110 includes a visible region 112 and a peripheral region 114, wherein the peripheral region 114 is located on at least one side of the visible region 112. In this embodiment, the peripheral region 114 surrounds the visible region 112. The first conductive unit 120 and the second conductive unit 130 are disposed on the substrate 110 and are at least located within the visible region 112. In other words, the first conductive unit 120 and the second conductive unit 130 may also extend into the peripheral region 114. The peripheral region 114 is, for example, a non-visible region and may be used to set signal wires, pads, or other components that are not intended to be observed by the user. In addition, a decorative layer may be provided in the peripheral region 114 so that electronic devices with the touch panel 110 can have a good appearance while simultaneously achieving the effect of concealing components. The material of the decorative layer may be ceramics, diamond-like carbon, ink, photoresist or any combination of the aforementioned materials, but is not limited thereto.

[0060] The substrate 110 may be a rigid light-transmitting substrate or a flexible light-transmitting substrate, and its material may be, for example, glass, sapphire, or plastic, but is not limited thereto. The substrate 110 may be a substrate independent of the display or a component substrate integrated into the display. For example, the substrate 110 may be a cover lens, which is a rigid substrate with high mechanical strength to cover and protect the lower components. The cover lens can be a composite laminate of reinforced glass, Poly(methyl methacrylate) (PMMA), and polycarbonate (PC), UV-curable resin (e.g., ORGA resin), or other hard, light-transmitting materials to provide protective characteristics such as scratch resistance and high mechanical strength. In addition, the material of the substrate 110 may also include high-temperature resistant plastics, such as polyimide or cyclic olefin copolymers. The side of the substrate 110 not configured with conductive units may be equipped with a film layer such as an anti-glare film or an anti-reflection film, or/and a buffer layer, such as an inorganic film like silicon oxide. Furthermore, the side surface of the substrate 110 connected to the touch surface may have an arcuate structure or a trapezoidal structure. Additionally, the substrate 110 can also be a color filter substrate of a liquid crystal display or an encapsulating cover for an organic light-emitting diode display, but is not limited thereto.

[0061] These first conductive units 120 extend along a first direction d1 and are electrically insulated from each other. The first conductive unit 120 includes a plurality of first electrodes 122 and a plurality of first connecting portion 124, with two adjacent first electrodes 122 being electrically connected by one of the first connecting portion 124. However, the present invention is not limited thereto. In other embodiments, two adjacent first electrodes 122 may also be electrically connected by two first connecting portion 124, or other multiple connecting portions. The second conductive unit 130 extends along a second direction d2 and is electrically insulated from each other. The second conductive unit 130 includes a plurality of second electrodes 132 and a plurality of second connecting portions 134, with two adjacent second electrodes 132 being electrically connected by one of the second connecting portions 134. However, the present invention is not limited thereto. In other embodiments, two adjacent second electrodes 132 may also be electrically connected by a plurality of, for example, two second connecting portions 134. The first direction d1 intersects with the second direction d2 and is preferably perpendicular to each other. The second conductive unit 130 and the first conductive unit 120 are electrically insulated from each other and interlaced with each other. One of the first conductive unit 120 and the second conductive unit 130 is the driving unit, while the other is the sensing unit. Accordingly, the first conductive unit 120 and the second conductive unit 130 can, for instance, form a touch component to detect the position of a touch event.

[0062] FIG. 2 is an enlarged schematic view of region M in FIG. 1. FIG. 2 mainly provides a schematic diagram of the structure where the first conductive unit 120 and the second conductive unit 130 intersect. In order to explain the structure in detail, FIG. 3, FIG. 4, and FIG. 5 respectively show each film layer in FIG. 2. FIG. 6 shows a schematic cross-sectional view along section lines A-A' and B-B' in FIG. 2. Please refer to FIG. 2 to 6 simultaneously. The first electrode 122 comprises a first sub-electrode E1 and a second sub-electrode E2, stacked in sequence on substrate 110, with the first sub-electrode E1 positioned between substrate 110 and the second sub-electrode E2. The first sub-electrode E1 and the second sub-electrode E2 are formed from different conductive layers, both overlapping and in contact. Adjacent first sub-electrodes E1 are connected by a first connecting portion 124 and may be formed from the same conductive layer; thus, adjacent first electrodes 122 are electrically connected via the first connecting portion 124. Since the first electrode 122 is formed from two conductive layers, it has a larger thickness, allowing for lower conductive impedance.

[0063] The second electrode 132 consists of a third sub-electrode E3 and a fourth sub-electrode E4 sequentially stacked on the substrate 110, with the third sub-electrode E3 positioned between the substrate 110 and the fourth sub-electrode E4. The third sub-electrode E3 and the fourth sub-electrode E4 are formed by different conductive layers, which overlap and are in contact. Two adjacent fourth sub-electrodes E4 are connected by a second connecting portion 134 and can be formed by the same conductive layer; thus, two adjacent second electrodes 132 are electrically connected through the second connecting portion 134. The first sub-electrode E1 and the third sub-electrode E3 can be formed by the same conductive layer, and the second sub-electrode E2 and the fourth sub-electrode E4 can likewise be formed by the same conductive layer. Since the second electrode 132 is formed from two layers of conductive material, it has a greater thickness and can exhibit lower conductive impedance.

[0064] The insulating pattern 140 is located at the intersection of the first conductive unit 120 and the second conductive unit 130. In other words, the insulating pattern 140 is positioned between the first conductive unit 120 and the second conductive unit 130 to electrically isolate them from each other. The insulating pattern 140 may cover the first connecting portion 124. Additionally, the insulating pattern 140 may cover a portion of the first sub-electrode E1 and a portion of the third sub-electrode E3. However, the present invention is not limited thereto. In other embodiments, the insulating pattern 140 may cover only a portion of the first sub-electrode E1 or only a portion of the third sub-electrode E3. The second connecting portion 134 is disposed on the insulating pattern 140, and portions of the second sub-electrode E2 and fourth sub-electrode E4 are arranged on the insulating pattern 140. However, the present invention is not limited thereto. In other embodiments, only a portion of the second sub-electrode E2 may be disposed on the insulating pattern 140, or only a portion of the fourth sub-electrode E4 may be disposed on the insulating pattern 140.

[0065] According to this embodiment, the insulating pattern 140 covers a portion of the first sub-electrode E1 while exposing another portion of the same electrode. It similarly covers part of the third sub-electrode E3 and exposes another part of the third sub-electrode E3. There is a first gap G1 between the portions of the first sub-electrode E1 and the third sub-electrode E3 covered by the insulating pattern 140. Conversely, a second gap G2 exists between the portions of the first sub-electrode E1 and the third sub-electrode E3 that are not covered by the insulating pattern 140. The first gap G1 is different from the second gap G2, wherein the width of the first gap G1 may be smaller than the width of the second gap G2. However, the present invention is not limited thereto. The gap width of the second gap G2 may be greater than 25 micrometers, preferably greater than 30 micrometers. In other words, there may be a sufficient gap size between the first electrode 122 and the second electrode 124 to further ensure that short circuit problems are unlikely to occur between the first electrode 122 and the second electrode 124.

[0066] From another perspective, the first sub-electrode E1 and the second sub-electrode E2 that are not covered by the insulating pattern 140 have substantially the same contours, and the third sub-electrode E3 and the fourth sub-electrode E4 that are not covered by the insulating pattern 140 have substantially the same contours. Moreover, the profile of the first sub-electrode E1 covered by the insulating pattern 140 differs from that of the second sub-electrode E2 located on the insulating pattern 140, and the profile of the third sub-electrode E3 covered by the insulating pattern 140 differs from that of the fourth sub-electrode E4 located on the insulating pattern 140. More specifically, the first sub-electrode E1 covered by the insulating pattern 140 has a first protrusion E1a, and this first protrusion E1a protrudes from the second sub-electrode E2. The third sub-electrode E3 covered by the insulating pattern 140 features a second protrusion E3a, and this second protrusion E3a protrudes from the fourth sub-electrode E4. As a result, the edge of the first sub-electrode E1 may have a first step difference h1, and the first step difference h1 is located at the edge of the insulating pattern 140. Similarly, the edge of the third sub-electrode E3 may have a second step difference h2, and the second step difference h2 is located at the edge of the insulating pattern 140. However, the present invention is not limited thereto. When the first gap G1 is not equal to the second gap G2, the sidewalls of the first sub-electrode E1 covered by the insulating pattern 140 and the second sub-electrode E2 located on the insulating pattern 140 may also have substantially the same contours, and the sidewalls of the third sub-electrode E3 covered by the insulating pattern 140 and the fourth sub-electrode E4 located on the insulating pattern 140 may also have substantially the same contours.

[0067] Please refer to FIG. 2 and FIG. 3 again. In this embodiment, the first conductive layer C1 has a plurality of discontinuities (including the first step difference h1 and the second step difference h2), wherein the first step difference h1 is located at the boundary between the insulating pattern 140 and the first conductive unit 120, and is located, for example, on the first sub-electrode E1. However, the present invention is not limited thereto. In other embodiments, the first step difference h1 may also be located on the first connecting portion 124 or at the boundary between the first sub-electrode E1 and the first connecting portion 124. Furthermore, the second step difference h2 is located at the boundary between the insulating pattern 140 and the second conductive unit 130, and is located, for example, on the third sub-electrode E3. In all embodiments of the present invention, the partial contours of the first step difference h1 and the second step difference h2 are substantially formed along the contour of the insulating pattern 140; in other words, the partial contours of the first step difference h1 and the second step difference h2 conform to the corresponding contour of the insulating pattern 140 stacked on the first conductive layer C1. Therefore, the shapes of the first step difference h1 and the second step difference h2 are not limited to the structures disclosed in the illustrated embodiments of the present invention; that is to say, the partial contours of the first step difference h1 and the second step difference h2 can be, for example, arc-shaped, straight lines, wavy, serrated, etc.

[0068] The manufacturing process of the touch panel of FIG. 2 will be briefly explained below. First, referring to FIG. 2 and FIG. 3, a first conductive layer C1 can be formed on the substrate 110. The first conductive layer C1 includes a first connecting portion 124, a first sub-electrode to be formed, and a third sub-electrode to be formed (not shown). The first sub-electrode to be formed and the third sub-electrode to be formed have smooth edges F (i.e., they do not possess the first step difference h1 and the second step difference h2), thus there is a single type of gap between them, specifically the first gap G1. In other words, the first and third sub-electrodes to be formed exhibit a wider distribution range compared to the already-formed first sub-electrode E1 and third sub-electrode E3, with their edge F shown, for instance, as a dashed line in FIG. 3.

[0069] The first conductive layer C1 may be composed of transparent conductive materials, such as Indium Tin Oxide (ITO), Indium-Zinc Oxide (IZO), Gallium Zinc Oxide (GZO), Carbon Nanotubes, Nanometal wires (e.g., nanosilver wires, electrospinning), Conducting Polymers, Graphene, Silicene, or other high-conductivity light-transmitting materials, but not limited to these. For instance, opaque metal conductive materials may also be used. The first conductive layer C1 is preferably in the form of a continuous thin film, such as an ITO film, nanosilver wire film, or ITO/Ag/ITO film; however, mesh films may also be utilized, particularly for metal materials, like metal meshes, but are not limited to these.

[0070] Next, referring to FIG. 2 to 4, a plurality of insulating patterns 140 are formed. The insulating patterns 140 cover the first connection portion 124, a segment of the first sub-electrode to be formed, and a segment of the third sub-electrode to be formed.

[0071] Next, referring to FIG. 2 to 5, form a second conductive layer C2. The material of the second conductive layer C2 may refer to that of the first conductive layer C1. The second conductive layer C2 includes the second connecting portion 134, the second sub-electrode E2, and the fourth sub-electrode E4. The method for forming the second conductive layer C2 involves first forming a conductive material layer to fully cover the substrate 110, the first conductive layer C1, and the insulating pattern 140. Subsequent to this, a patterning process is executed to form the second conductive layer C2. The gap between the second sub-electrode E2 and the fourth sub-electrode E4 constitutes the second gap G2, where the width of the second gap G2 surpasses that of the first gap G1. In other words, the patterns of the second sub-electrode E2 and the fourth sub-electrode E4 are smaller than those of the first sub-electrode and third sub-electrode to be formed, thus during the aforementioned patterning process, parts of the first conductive layer C1 and the second conductive layer C2 are simultaneously removed. Moreover, since the second gap G2 is larger than the first gap G1, it ensures that thin film residues are less likely to remain between the first electrode E1 and the second electrode E2, thereby reducing the likelihood of short circuits between the first conductive unit 120 and the second conductive unit 130 (shown in FIG. 1). Moreover, since the insulating pattern 140 covers a portion of the first sub-electrode to be formed and the third sub-electrode to be formed, a first step difference h1 and a second step difference h2 can be formed at the junction of the first gap G1 and the second gap G2, where the unremoved portions of the first sub-electrode to be formed and the third sub-electrode to be formed form the first protruding part E1a and the second protruding part E3a.

[0072] Please refer to FIG. 2 and FIG. 6, the first connecting portion 124 is formed by the first conductive layer C1, and the second connecting portion 134 is formed by the second conductive layer C2, wherein the thickness of the first conductive layer C1 can be greater than the thickness of the second conductive layer C2. For example, the thickness of the first conductive layer C1 can be 1.05 to 8 times the thickness of the second conductive layer C2. The conductive impedance of the first conductive layer C1 may be less than that of the second conductive layer C2, allowing the line width W1 of the first connecting portion 124 to be smaller than the line width W2 of the second connecting portion 134. In this embodiment, the first conductive unit 120 is, for example, a sensing unit, and the second conductive unit 130 is, for example, a driving unit, wherein the length of the second connecting portion 134 of the second conductive unit 130 is shorter than the length of the first connecting portion 124 of the first conductive unit 120, and the line width of the second connecting portion 134 of the second conductive unit 130 is greater than the line width of the first connecting portion 124 of the first conductive unit 120. In this way, the first conductive unit 120 can have a good sensing effect, and the second conductive unit 130 can have a good driving effect, but the present invention is not limited thereto.

[0073] In another embodiment, the thickness of the first conductive layer C1 can also be smaller than the thickness of the second conductive layer C2, as shown in FIG. 7. Selectively, in the embodiment of FIG. 7, considering low conduction impedance, the line width W1 of the first connection portion 124 belonging to the first conductive layer C1 in FIG. 2 can be greater than the line width W2 of the first connection portion 134 belonging to the second conductive layer C2. However, the present invention is not limited thereto. In addition, if the patterning process for the second conductive layer C2 is an etching process, when the thickness of the second conductive layer C2 is greater than the thickness of the first conductive layer C1, it will aid in the reliable removal of the first conductive layer C1. Alternatively, increasing the crystallinity of the second conductive layer C2 compared to the first conductive layer C1, meaning that the crystalline grain size of the second conductive layer C2 is larger than that of the first conductive layer C1, can also contribute to the reliable removal of the first conductive layer C1 during the etching process. The thickness of the second conductive layer C2 is, for example, 1.05 to 8 times that of the first conductive layer C1. However, the present invention is not limited thereto. In other embodiments, the crystalline grain size of the second conductive layer C2 can also be smaller than that of the first conductive layer C1.

[0074] FIG. 8 is a partial top-view schematic diagram of the touch panel 100 of FIG. 1. FIG. 9 is a cross-sectional schematic diagram along the section line C~C' of FIG. 8. Please refer to FIG. 8 and FIG. 9, touch panel 100 may selectively include a plurality of dummy patterns 150 disposed between the first electrode 122 and the second electrode 132, where the gap G between the dummy pattern 150 and the first electrode 122 is equal to the second gap G2, and the gap G between the dummy pattern 150 and the second electrode 132 is also equal to the second gap G2. The arrangement of dummy patterns 150 can reduce the user's perception of the configuration of the first electrode 122 and the second electrode 132, thereby enhancing the visual effect of touch panel 100. The dummy pattern 150 can be composed of a portion of the first conductive layer C1 and a portion of the second conductive layer C2 to form a double-layer structure, but the present invention is not limited thereto. The dummy pattern 150 can also be composed of only a portion of the second conductive layer C2 to form a single-layer structure.

[0075] The touch panel 100 may further include a buffer layer 160, as shown in FIG. 10. The buffer layer 160 covers the substrate 110 and is located between the substrate 110 and the first conductive layer C1. The buffer layer 160 ensures that the first conductive layer C1 is effectively removed during the etching process without the problem of film residue. The material of the buffer layer 160 includes organic or inorganic materials. Preferred materials for the buffer layer 160 include polyimide, epoxy resin, siloxane, acrylic resin, or other transparent resins; however, it is not limited to these. For instance, zinc oxide, silicon oxide (SiO<sub>x</sub>), nitride oxide, or combinations thereof—such as silicon oxide combined with nitride oxide—may also be employed to render the contour of the patterned conductive layer less visible. For silicon dioxide, the thickness ranges from 300 Angstroms (Å) to 1000 Å. For resin, the thickness ranges from 0.1 micrometers (μm) to 3 micrometers (μm).

[0076] FIG. 11 is a partial top view schematic of another embodiment of the touch panel of the present invention. FIG. 12 is a schematic diagram of the first conductive layer of the touch panel shown in FIG. 11. Please refer to FIG. 11 and FIG. 12. Similar to the touch panel 100, the touch panel 100a is formed by the first conductive layer C1, insulating pattern 140, and second conductive layer C2, wherein the first conductive layer C1 has a plurality of first step difference h1 and a plurality of second step difference h2. Furthermore, the two adjacent first electrodes 122 in this embodiment are electrically connected by two first connecting portion 124. Moreover, the two adjacent second electrodes 132 of this embodiment are electrically connected by two second connecting portions 134. In addition, in this embodiment, the insulating pattern 140 covers the two first connecting portion 124 electrically connecting the two adjacent first electrodes 122, but the present invention is not limited thereto. In other embodiments, two insulating patterns 140 may each cover one of the first connecting portion 124, as shown in FIG. 13.

[0077] FIG. 14 is a partial top view schematic of a touch panel according to another embodiment of the present invention. FIG. 15 is a schematic diagram of the first conductive layer of the touch panel in FIG. 14. This embodiment of the touch panel 100b is similar to the aforementioned touch panel 100, except that the insulating pattern 140 only covers a portion of the third sub-electrode E3 but not a portion of the first sub-electrode E1. Additionally, the insulating pattern 140 completely covers the first connecting portion 124. Since the insulating pattern 140 covers the first connecting portion 124 but not the first sub-electrode E1, and completely covers the first connecting portion 124, after the second conductive layer C2 is completed, the first step difference h1 is located at the junction of the first sub-electrode E1 and the first connecting portion 124.

[0078] FIG. 16 is a partial top view schematic of another embodiment of the touch panel according to the present invention. FIG. 17 is a schematic diagram of the first conductive layer of the touch panel shown in FIG. 16. The touch panel 100c in this embodiment is similar to the aforementioned touch panel 100, except that the insulating pattern 140 covers the third sub-electrode E3 and does not cover the first sub-electrode E1. Additionally, the insulating pattern 140 covers one portion of the first connecting part 124 and exposes another portion of the first connecting part 124. Since the insulating pattern 140 does not cover the first sub-electrode E1 and a portion of the first connecting portion 124, after the second conductive layer C2 is completed, the first step difference h1 is positioned on the first connecting portion 124.

[0079] FIG. 18 is a partial top-view schematic of a touch panel according to another embodiment of the present invention. Please refer to FIG. 18. Similar to the aforementioned embodiments, the touch panel 100a is formed, for example, by the first conductive layer C1, the insulating pattern 140, and the second conductive layer C2. FIG. 19 is a schematic diagram of the first conductive layer of the touch panel in FIG. 18, and the structures of the insulating pattern 140 and the second conductive layer C2 of the touch panel 100a are the same as those in FIG. 4 and 5. Please refer to both FIG. 18 and FIG. 19. The touch panel 100a is similar to the touch panel 100, with the distinction being that the first gap G1 between the first sub-electrode E1 and the third sub-electrode E3 covered by the insulating pattern 140 is larger than the second gap G2 between the same electrodes not covered by the insulating pattern 140. Specifically, the first sub-electrode E1 covered by the insulating pattern 140 has a first recessed portion E1b, which is recessed within the boundary of the second sub-electrode E2. The third sub-electrode E3 covered by the insulating pattern 140 features a second recessed portion E3b, which is recessed within the boundary of the fourth sub-electrode E4. In addition, the manufacturing process of the touch panel 100a is similar to that of the touch panel 100; please refer to the aforementioned embodiment. The difference is in the structure of the first conductive layer C1. Specifically, in this embodiment, after the first conductive layer C1 is completed, there are two types of gaps between the first sub-electrode and the third sub-electrode to be formed, wherein the gap expected to be covered by the insulating pattern 140 is the first gap G1. Additionally, the gaps expected not to be covered by the insulating pattern 140 are, for example, smaller than the first gap G1 and larger than the second gap G2. Moreover, after the patterning process to form the second conductive layer C2, the gap not covered by the insulating pattern 140 becomes the second gap G2.

[0080] In summary, the touch panel of the present invention includes a plurality of conductive units, and each conductive unit comprises a plurality of electrodes and a plurality of connecting portions, wherein the electrodes are formed from a double-layer conductive structure, resulting in lower conduction impedance, thereby enhancing the touch panel's sensitivity.

[0081] Finally, it should be noted that: The above embodiments are intended to illustrate the technical solutions of the present invention and not to limit them; although the present invention has been described in detail with reference to the above embodiments, it should be understood by those skilled in the art that: Modifications or equivalent replacements may be made to the technical solutions recorded in the aforementioned embodiments, to some or all of the technical features therein, without departing from the essence of the technical solutions of the embodiments of the present invention.

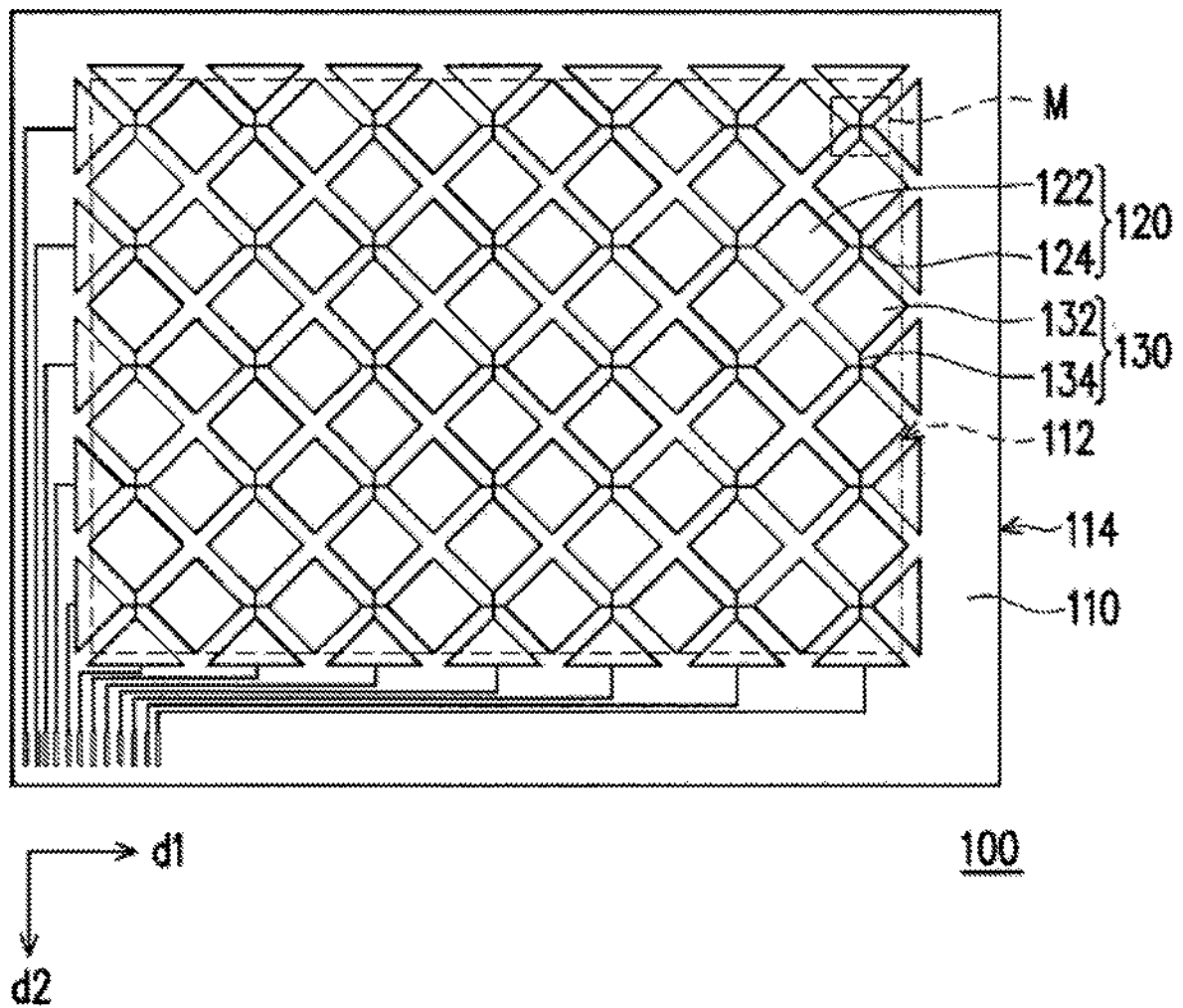


FIG. 1

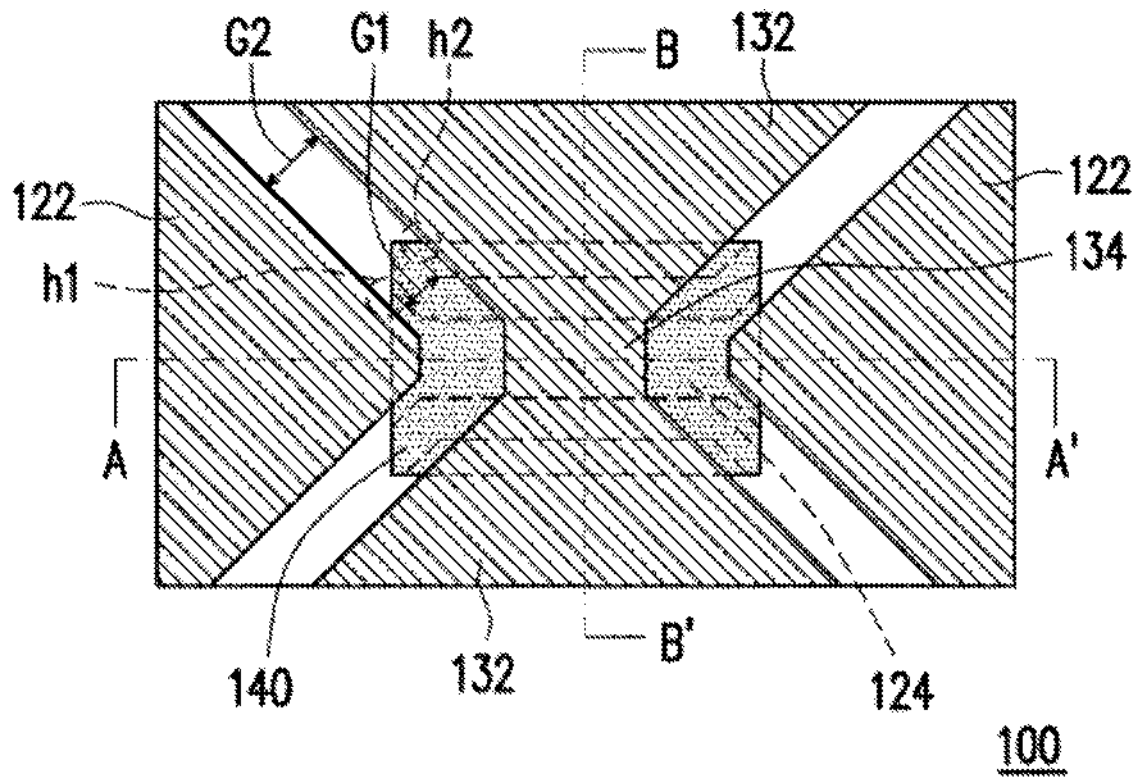


FIG. 2

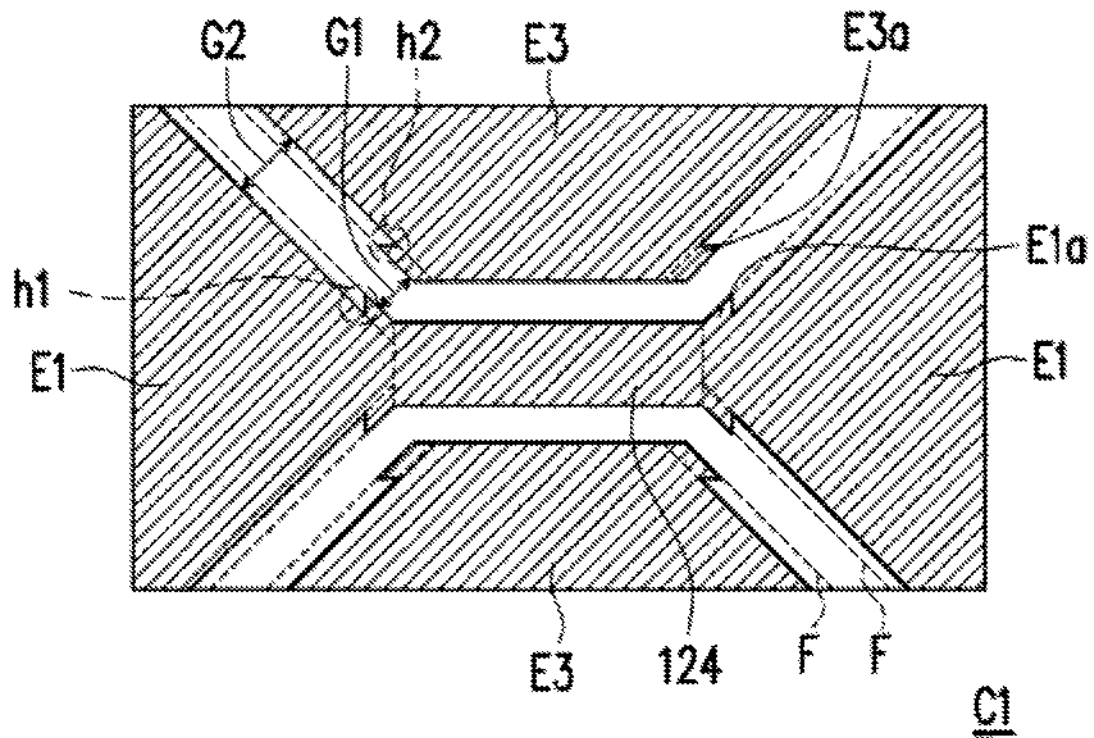


FIG. 3

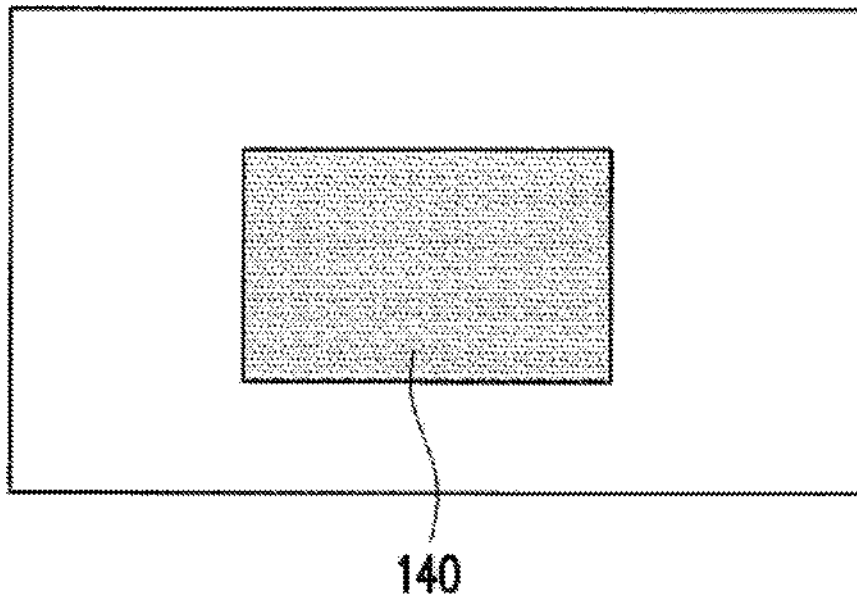


FIG. 4

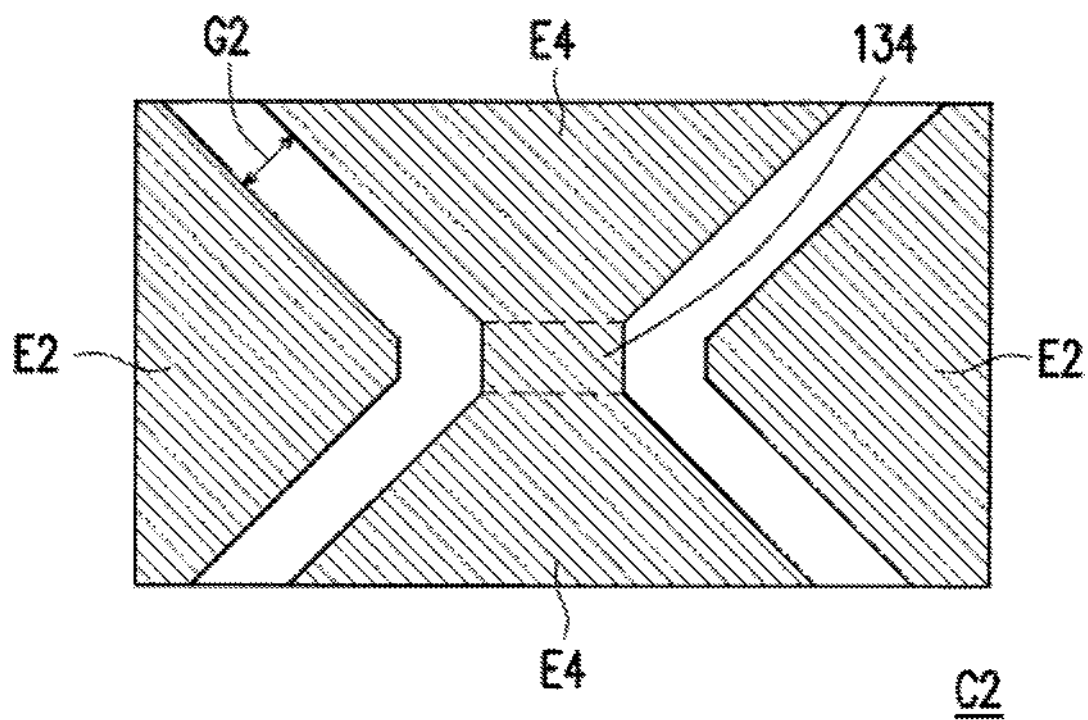


FIG. 5

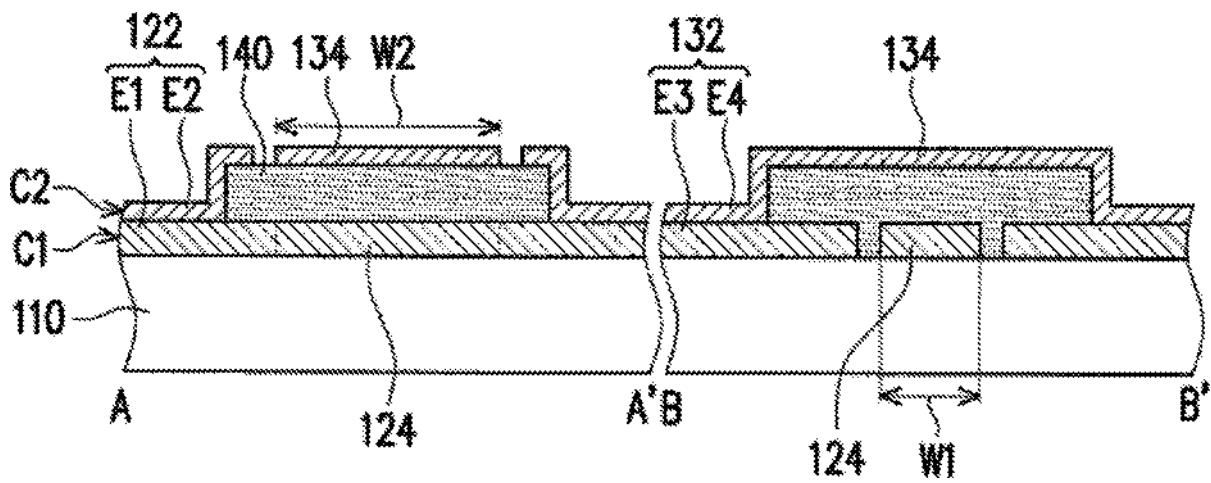


FIG. 6

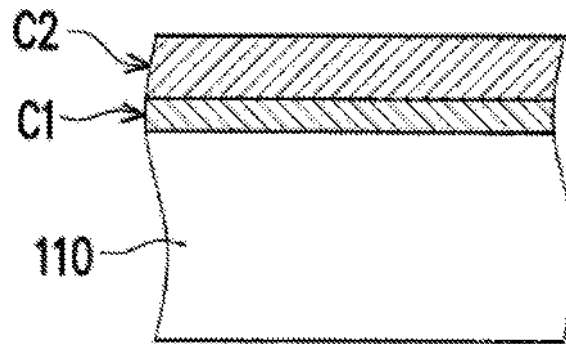


FIG. 7

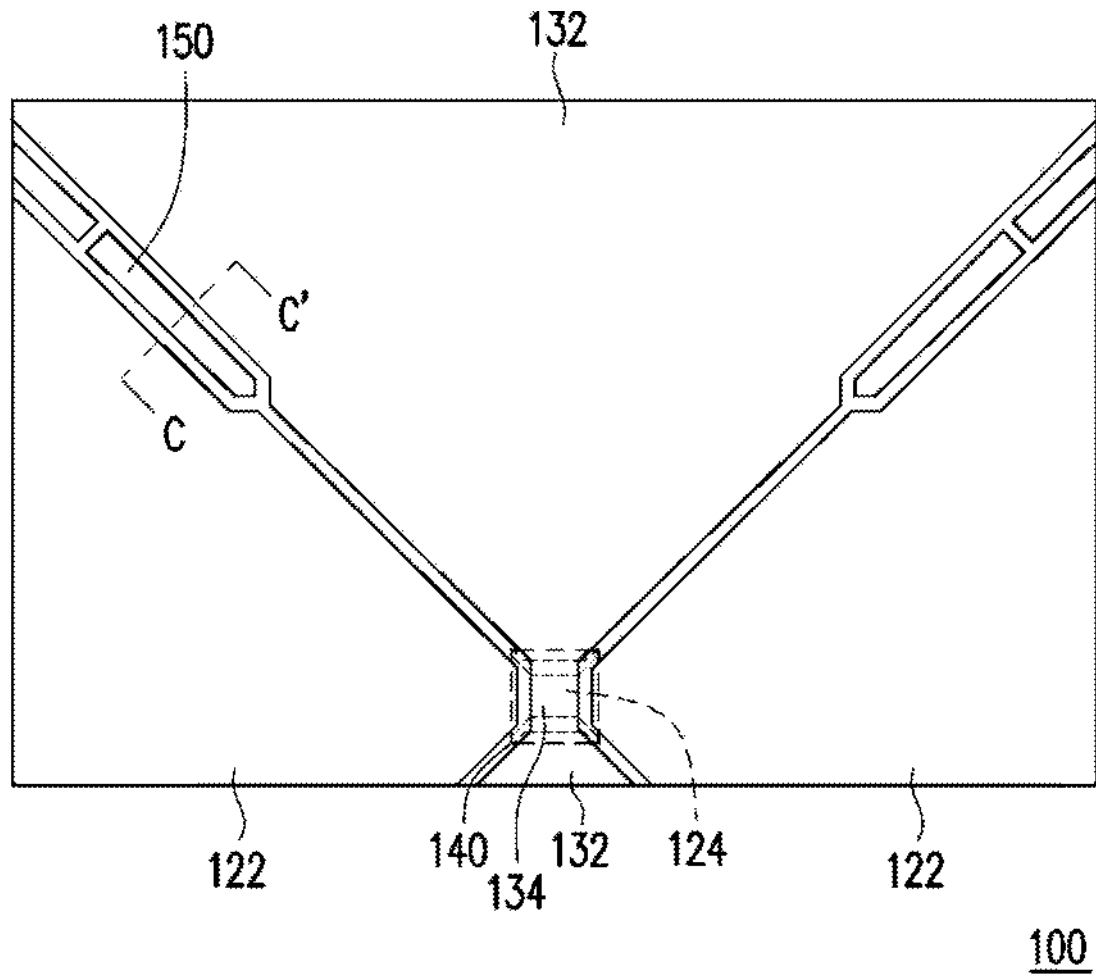


FIG. 8

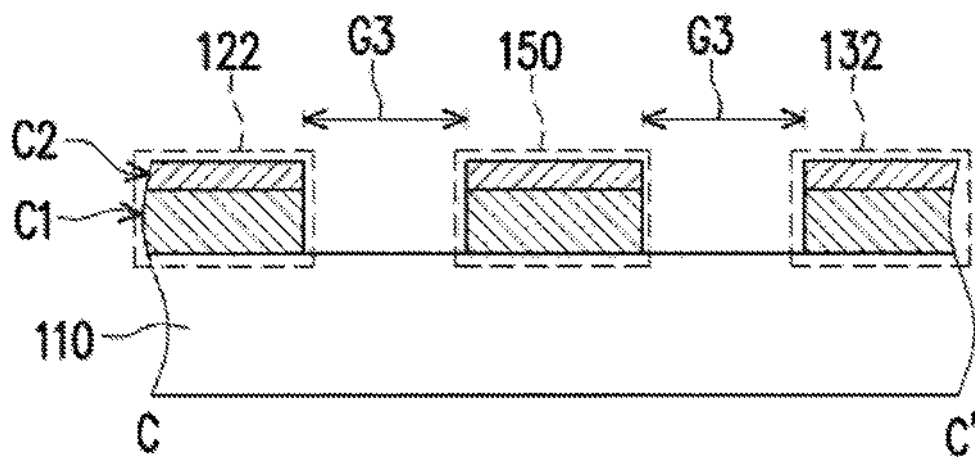


FIG. 9

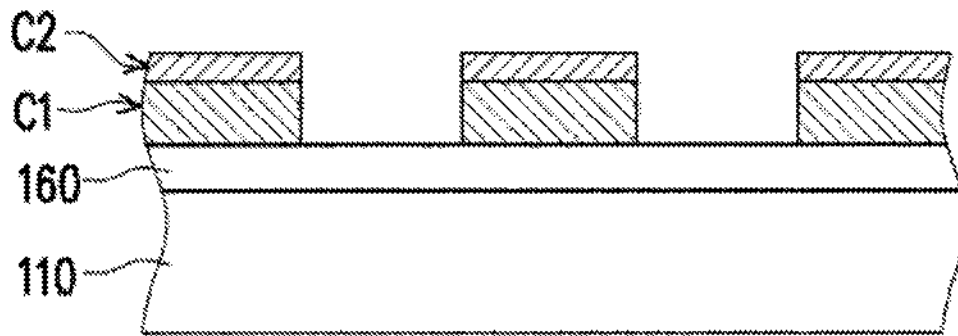


FIG. 10

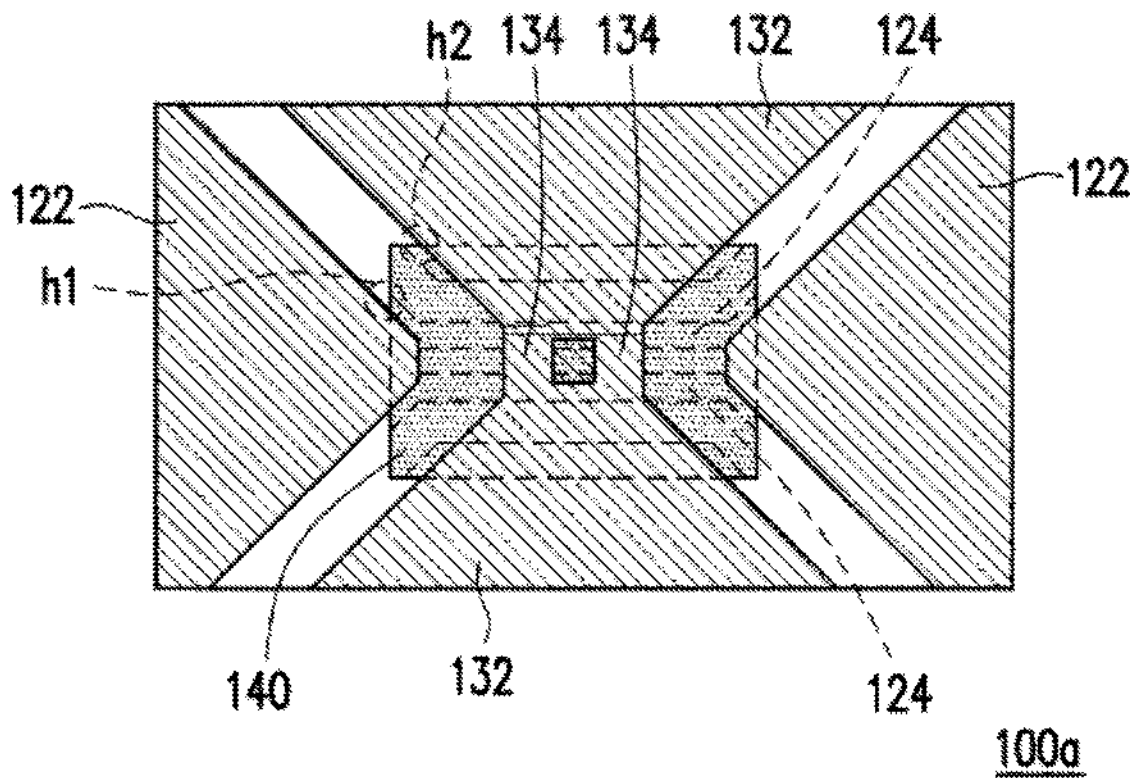


FIG. 11

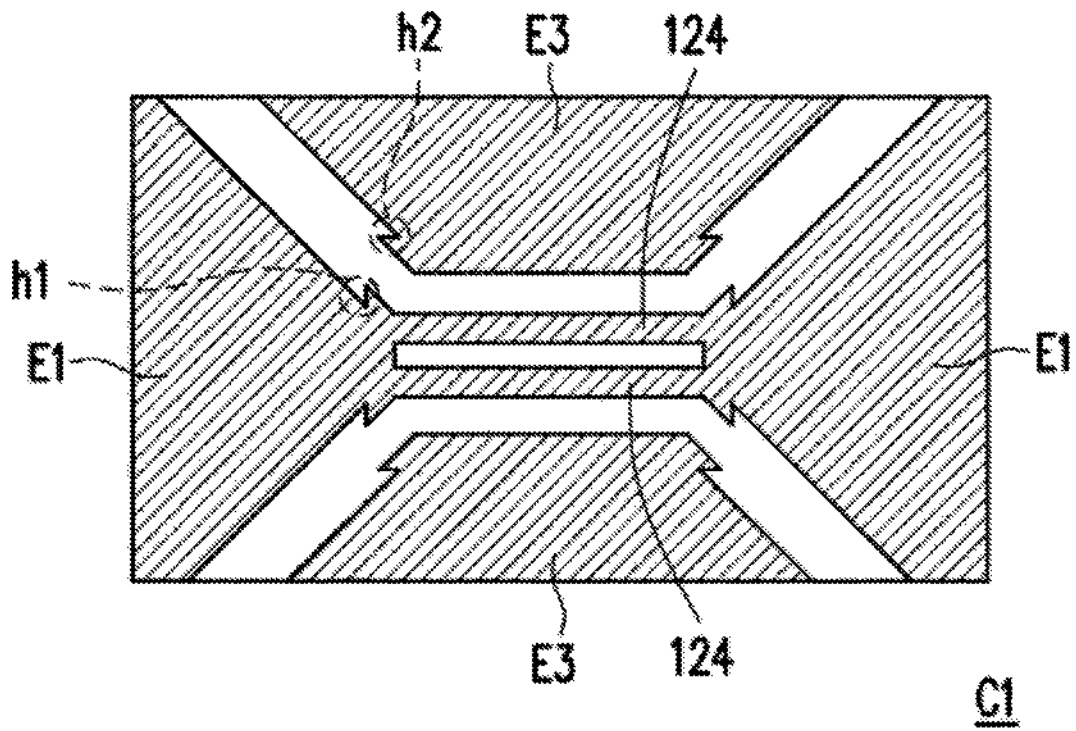


FIG. 12

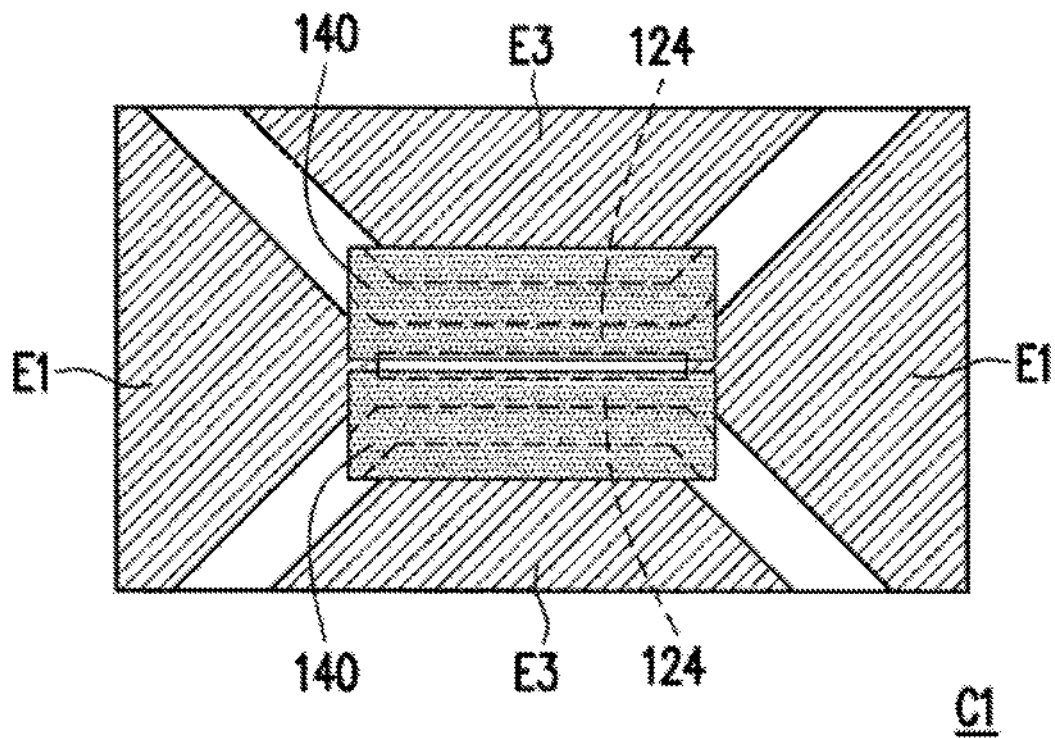


FIG. 13

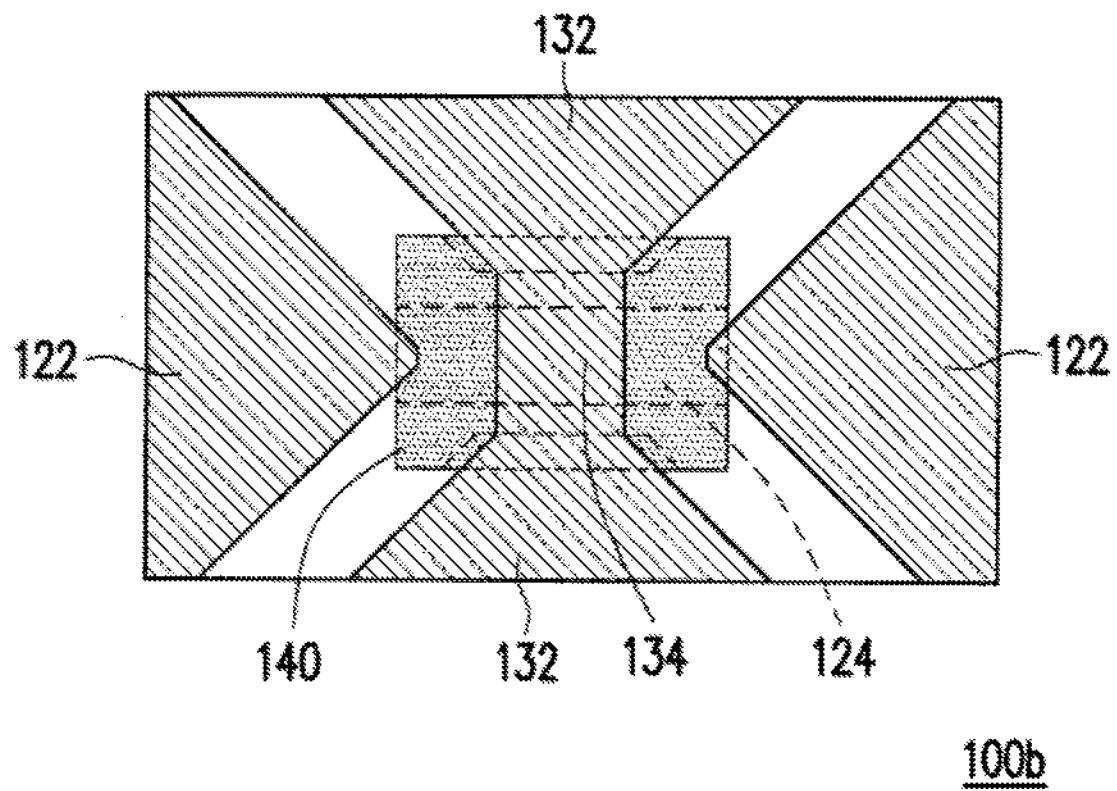


FIG. 14

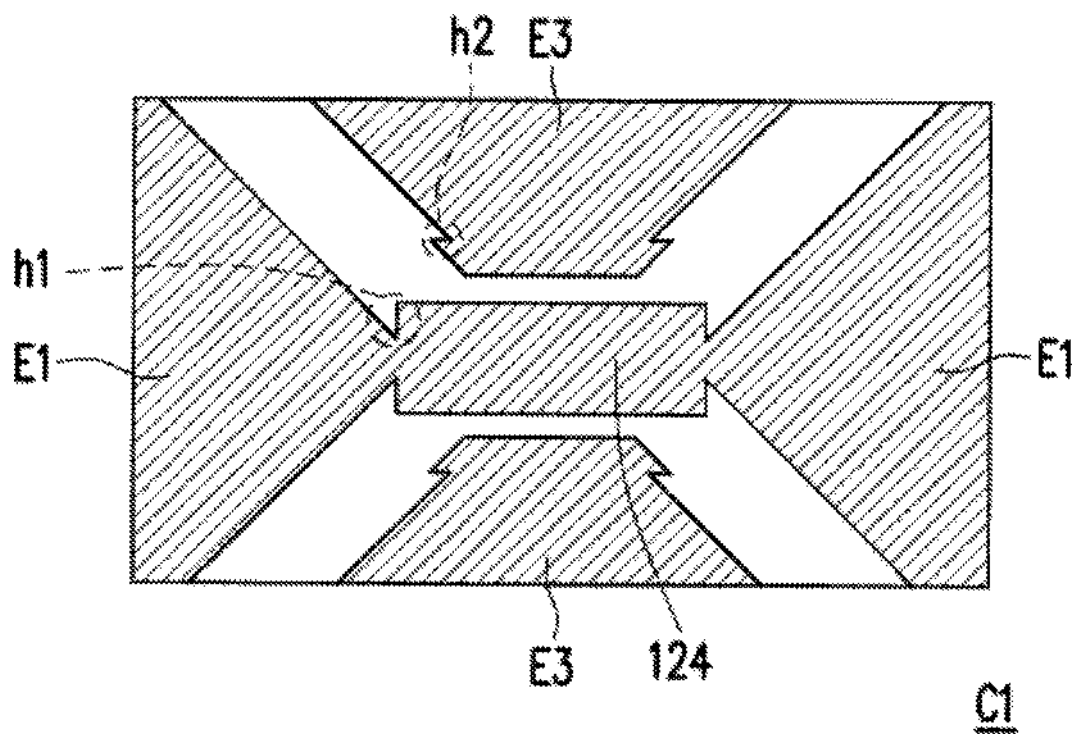


FIG. 15

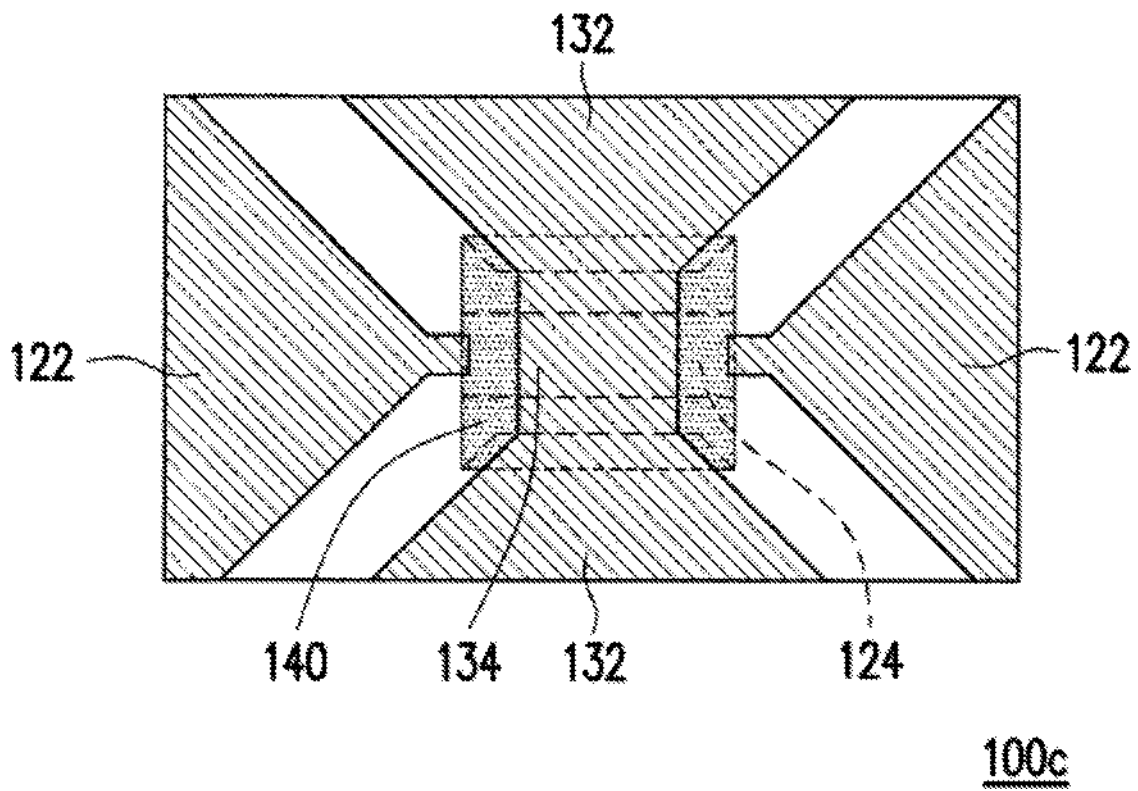


FIG. 16

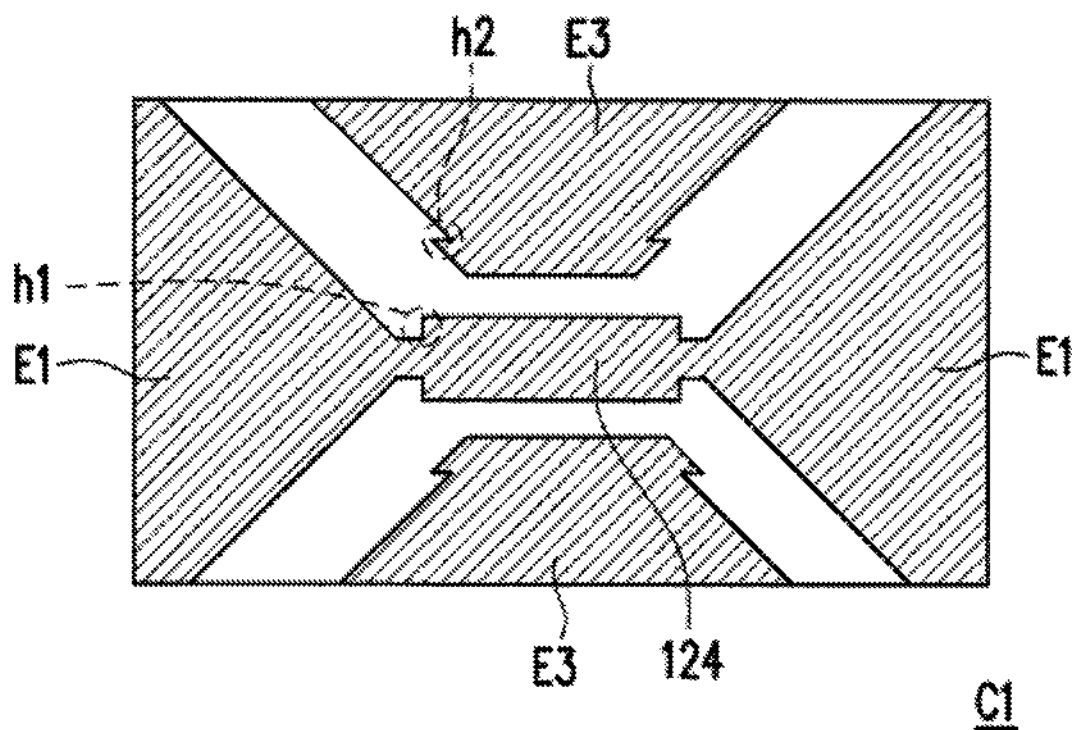


FIG. 17

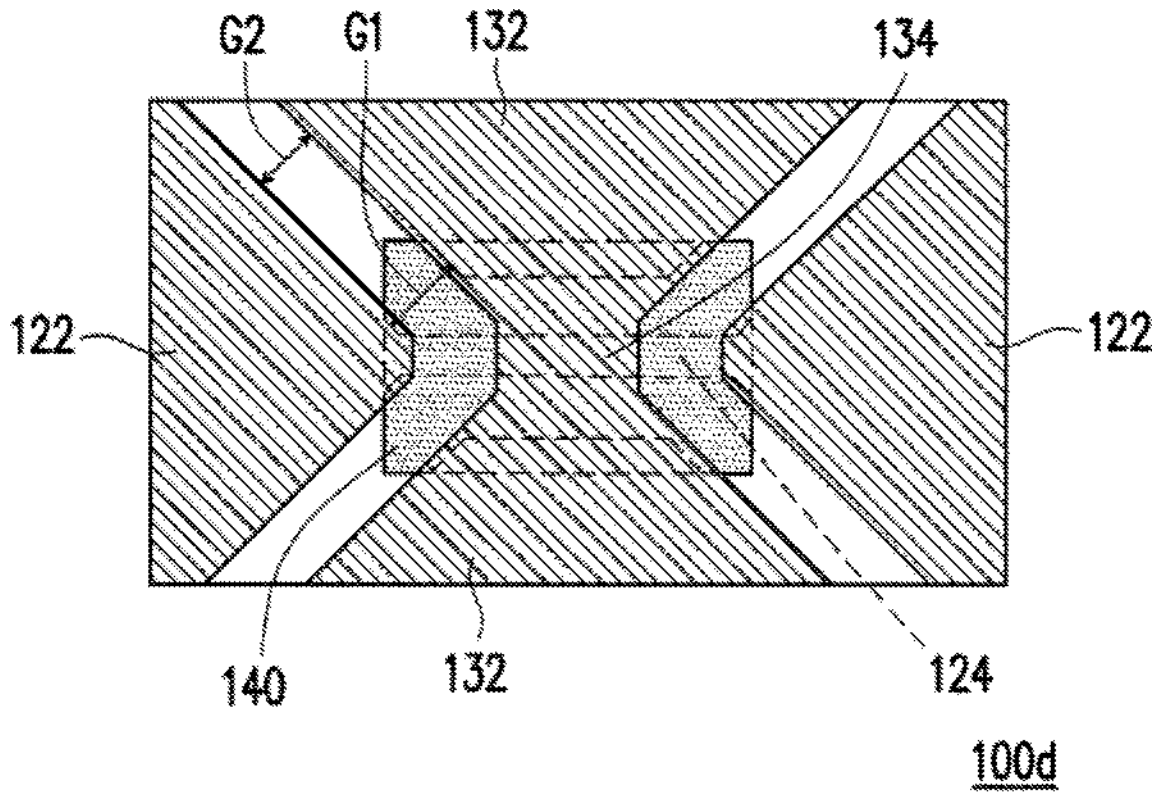


FIG. 18

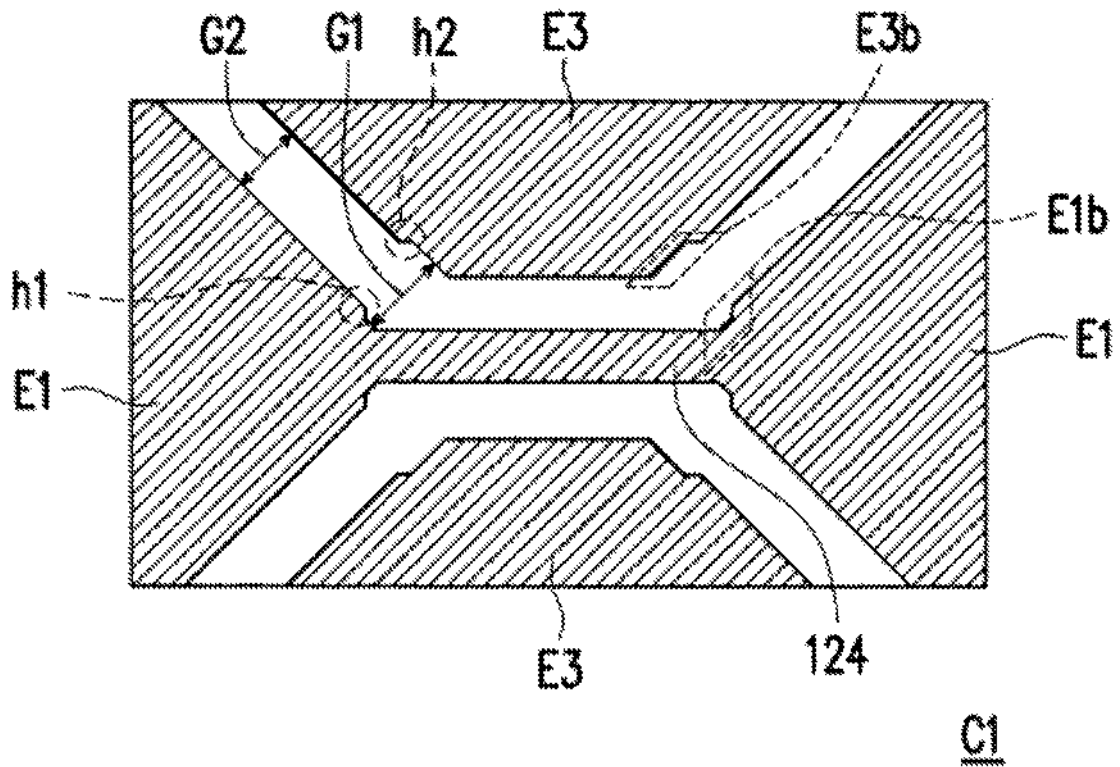


FIG. 19



## TRANSLATION CERTIFICATION

Date: July 15, 2025

### Translator's Declaration

I, Tony Zhou, hereby declare:

That I possess advanced knowledge of the Simplified Chinese and English languages. The attached Simplified Chinese into English translation has been translated by me and to the best of my knowledge and belief, it is a true and accurate translation of: CN105320372A Hsieh.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willfully false statements and the like are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code.

In signing this declaration, I understand that the translation and this declaration may be filed as evidence in a contested case. I acknowledge that I may be subject to cross-examination within the United States.

Tony Zhou

---

Signature

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Ex-1012

## TRANSLATION CERTIFICATION

Date: 2025/07/15

To whom it may concern:

This is to certify that the attached translation is an accurate representation of the documents received by this office. The translation was completed from:

- Chinese (PRC)

To:

- English (USA)

The documents are designated as:

- 'CN105320372A Hsieh.pdf'

Tania Duvernay, Project Manager in this company, attests to the following:

"To the best of my knowledge, the aforementioned documents are a true, full and accurate translation of the specified documents."



Signature of **Tania Duvernay**, Project Manager

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Ex-1012



(43) 申请公布日 2016.02.10

*G06F 3/044*(2006.01)

1. 一种触控面板,其特征在于,包括:

一基板;

多个第一导电单元,设置在该基板上,各该第一导电单元包括多个第一电极以及多个第一连接部,相邻两个第一电极由至少一个第一连接部电性连接,且各该第一电极包括于该基板上依序堆叠的第一子电极以及一第二子电极;

多个第二导电单元,设置在该基板上,各该第二导电单元包括多个第二电极以及多个第二连接部,相邻两个第二电极由至少一个第二连接部电性连接,且各该第二电极包括于该基板上依序堆叠的一第三子电极以及一第四子电极,该些第二导电单元与该些第一导电单元彼此电性绝缘且彼此交错,该些第一连接部、该第一子电极与该第三子电极属于一第一导电层,该些第二连接部、该第二子电极与该第四子电极属于一第二导电层;以及

多个绝缘图案,设置于该些第一导电单元与该些第二导电单元的交错处,该些绝缘图案覆盖该些第一连接部,且各该绝缘图案覆盖该第一子电极的一部分以及该第三子电极的一部分的至少其中一者,其中该第一导电层具有多个断差,该些断差至少位于该些第一导电单元与该些绝缘图案的交界。

2. 根据权利要求1所述的触控面板,其特征在于,该些断差位于该些第二导电单元与该些绝缘图案的交界。

3. 根据权利要求1所述的触控面板,其特征在于,一部分的该些断差位于该第一子电极上。

4. 根据权利要求1所述的触控面板,其特征在于,一部分的该些断差位于该第三子电极上。

5. 根据权利要求1所述的触控面板,其特征在于,一部分的该些断差位于该第一连接部上。

6. 根据权利要求1所述的触控面板,其特征在于,一部分的该些断差位于该第一子电极与该第一连接部的交界。

7. 根据权利要求1所述的触控面板,其特征在于,相邻的两个第一电极由两个第一连接部电性连接。

8. 根据权利要求1所述的触控面板,其特征在于,相邻的两个第二电极由两个第二连接部电性连接。

9. 根据权利要求1所述的触控面板,其特征在于,被各该绝缘图案覆盖的该第一子电极与该第三子电极之间具有一第一间隙,未被各该绝缘图案覆盖的该第一子电极与该第三子电极之间具有一第二间隙,其中该第一间隙不同于该第二间隙。

10. 根据权利要求9所述的触控面板,其特征在于,该第一间隙小于该第二间隙。

11. 根据权利要求9所述的触控面板,其特征在于,该第一间隙大于该第二间隙。

12. 根据权利要求1所述的触控面板,其特征在于,各该第二连接部设置于其中一个绝缘图案上,且该第二子电极的一部分以及该第四子电极的一部分的至少其中一者设置于其中一个绝缘图案上。

13. 根据权利要求1所述的触控面板,其特征在于,被各该绝缘图案覆盖的该第一子电极具有一第一突出部且该第一突出部突出于该第二子电极之外,被各该绝缘图案覆盖的该第三子电极具有一第二突出部且该第二突出部突出于该第四子电极之外。

14. 根据权利要求 1 所述的触控面板,其特征在于,被各该绝缘图案覆盖的该第一子电极具有一第一内缩部且该第一内缩部内缩于该第二子电极之内,被各该绝缘图案覆盖的该第三子电极具有一第二内缩部且该第二内缩部内缩于该第四子电极之内。

15. 根据权利要求 1 所述的触控面板,其特征在于,该第一导电层的厚度大于该第二导电层的厚度。

16. 根据权利要求 15 所述的触控面板,其特征在于,该第一连接部属于该第一导电层,该第二连接部属于该第二导电层,且该第一连接部的线宽小于该第二连接部的线宽。

17. 根据权利要求 1 所述的触控面板,其特征在于,该第一导电层的厚度小于该第二导电层的厚度。

18. 根据权利要求 17 所述的触控面板,其特征在于,该第一连接部属于该第一导电层,该第二连接部属于该第二导电层,且该第一连接部的线宽大于该第二连接部的线宽。

19. 根据权利要求 1 所述的触控面板,其特征在于,该第二导电层的结晶颗粒尺寸大于该第一导电层的结晶颗粒尺寸。

20. 根据权利要求 1 所述的触控面板,其特征在于,该第二间隙大于 25 微米。

21. 根据权利要求 1 所述的触控面板,其特征在于,还包括一缓冲层,覆盖该基板且位于该基板与该第一导电层之间。

22. 根据权利要求 1 所述的触控面板,其特征在于,还包括多个拟置图案,设置于该些第一电极与该些第二电极之间。

## 触控面板

### 技术领域

[0001] 本发明是有关于一种触控面板,且特别是有关于一种传导阻抗低且触控感测灵敏度良好的触控面板。

### 背景技术

[0002] 电容式触控面板通常会包含多个沿一第一方向(例如垂直方向)设置的第一导电单元,及多个沿一第二方向(例如水平方向)设置的第二导电单元。电容式触控面板的驱动器可输出驱动信号至第一导电单元,并接收第二导电单元产生的相对应感应信号,之后电容式触控面板再根据接收到的感应信号相对应产生触控位置信号。

[0003] 一般而言,电容式触控面板的第一感应单元及第二感应单元是由透明导电材料所形成。然而,透明导电材料的电阻值通常较会影响电容式触控面板的触控感测性能。此外,如果导电单元是由非透明导电材料(例如:金属细线)所形成,则较会有视效上的问题,若是通过降低线宽以减少视效所造成的影响,则可能会因线宽过小,而会有电阻升高及良率不高的问题。因此,如何降低电容式触控面板的第一导电单元及第二导电单元的传导阻抗是相当重要的课题。

### 发明内容

[0004] 本发明提供一种触控面板,其中触控面板的阻抗低且触控灵敏度良好。

[0005] 本发明的触控面板包括一基板、多个第一导电单元、多个第二导电单元以及多个绝缘图案。第一导电单元设置在基板上。各第一导电单元包括多个第一电极以及多个第一连接部。相邻两个第一电极由至少一个第一连接部电性连接。各第一电极包括于基板上依序堆叠的一第一子电极以及一第二子电极。第二导电单元设置在基板上。各第二导电单元包括多个第二电极以及多个第二连接部。相邻两个第二电极由至少一个第二连接部电性连接。各第二电极包括于基板上依序堆叠的一第三子电极以及一第四子电极。第二导电单元与第一导电单元彼此电性绝缘且彼此交错。第一连接部、第一子电极与第三子电极属于一第一导电层。第二连接部、第二子电极与第四子电极属于一第二导电层。绝缘图案设置于第一导电单元与第二导电单元的交错处。绝缘图案覆盖第一连接部,且各绝缘图案覆盖第一子电极的一部分以及第三子电极的一部分的至少其中一者。第一导电层具有多个断差。这些断差位于第一导电单元与绝缘图案的交界。

[0006] 基于上述,本发明的触控面板包括多个导电单元,且每一个导电单元包括多个电极和多个连接部,其中该些电极是由双层导电结构所构成,因此具有较低的传导阻抗,进而提升触控面板触控灵敏度。

[0007] 为了让本发明的上述特征和优点能更明显易懂,下文特举实施例,并配合附图作详细说明如下。

### 附图说明

- [0008] 图 1 为本发明一实施例的触控面板的上视示意图；
- [0009] 图 2 为图 1 的区域 M 的放大示意图；
- [0010] 图 3、图 4 以及图 5 分别示出图 2 中的各个膜层；
- [0011] 图 6 示出图 2 中的剖线 A-A' 以及 B-B' 的剖面示意图；
- [0012] 图 7 为本发明另一实施例的触控面板的上视示意图；
- [0013] 图 8 为图 1 的触控面板 100 的局部上视示意图；
- [0014] 图 9 为沿图 8 的剖线 C-C' 的剖面示意图；
- [0015] 图 10 为本发明另一实施例的触控面板的局部剖面示意图；
- [0016] 图 11 为本发明另一实施例的触控面板的局部上视示意图；
- [0017] 图 12 为图 11 的触控面板的第一导电层的示意图；
- [0018] 图 13 为本发明另一实施例的触控面板的第一导电层的示意图；
- [0019] 图 14 为本发明另一实施例的触控面板的局部上视示意图；
- [0020] 图 15 为图 14 的触控面板的第一导电层的示意图；
- [0021] 图 16 为本发明另一实施例的触控面板的局部上视示意图；
- [0022] 图 17 为图 16 的触控面板的第一导电层的示意图；
- [0023] 图 18 为本发明另一实施例的触控面板的局部上视示意图；
- [0024] 图 19 为图 18 的触控面板的第一导电层的示意图。
- [0025] 附图标记说明：
- [0026] 100、100a、100b、100c：触控面板；
- [0027] 110：基板；
- [0028] 112：可视区；
- [0029] 114：周边区；
- [0030] 120：第一导电单元；
- [0031] 122：第一电极；
- [0032] 124：第一连接部；
- [0033] 130：第二导电单元；
- [0034] 132：第二电极；
- [0035] 134：第二连接部；
- [0036] 140：绝缘图案；
- [0037] 150：拟置图案；
- [0038] 160：缓冲层；
- [0039] A-A'、B-B'、C-C'：剖线；
- [0040] C1：第一导电层；
- [0041] C2：第二导电层；
- [0042] d1：第一方向；
- [0043] d2：第二方向；
- [0044] E1：第一子电极；
- [0045] E1a：第一突出部；
- [0046] E1b：第一内缩部；

- [0047] E2 :第二子电极 ;
- [0048] E3 :第三子电极 ;
- [0049] E3a :第二突出部 ;
- [0050] E3b :第二内缩部 ;
- [0051] E4 :第四子电极 ;
- [0052] G1 :第一间隙 ;
- [0053] G2 :第二间隙 ;
- [0054] G :间隙 ;
- [0055] h1 :第一断差 ;
- [0056] h2 :第二断差 ;
- [0057] M :区域 ;
- [0058] W1、W2 :线宽。

### 具体实施方式

[0059] 图1为本发明一实施例的触控面板的上视示意图。请参照图1,触控面板100包括一基板110、多个第一导电单元120、多个第二导电单元130以及多个绝缘图案140(示出于图2)。基板110包括一可视区112以及一周边区114,其中周边区114位于可视区112的至少一侧。在本实施例中,周边区114环绕可视区112。第一导电单元120与第二导电单元130设置在基板110上且至少位于可视区112中。换言之,第一导电单元120与第二导电单元130也可以延伸至周边区114。周边区114例如是非可视区,且可用以设置信号导线、接垫或是其他不欲被使用者观察到的构件等等。此外,周边区114中也可以设置有装饰层,以使具有触控面板110的电子装置可以具有良好的外观并同时达到遮蔽构件的功效。装饰层的材料可为陶瓷、类钻碳、油墨、光阻或上述材料的任意组合,但不以此为限。

[0060] 基板110可为一硬式透光基板或一可挠式透光基板,其材质例如为玻璃、蓝宝石或塑料,但不以此为限。基板110可以是独立于显示器外的基板或是整合于显示器内的元件基板。举例而言,基板110例如是覆盖板(Cover lens),其为高机械强度的硬质基板以具有覆盖保护下部元件的作用。覆盖板可以为强化玻璃、聚甲基丙烯酸甲酯(Poly(methyl methacrylate);简称PMMA)与聚碳酸酯(Polycarbonate;简称PC)的复合叠层、紫外线固化型树脂(例如ORGA树脂)或其他硬质透光材质以具备耐刮及高机械强度等保护特性。此外,基板110的材料还可以包含有耐高温的塑料,例如聚酰亚胺(polyimide)或环烯烃共聚物。基板110上未配置有导电单元的一侧可以配置有例如抗眩膜或抗反射膜等膜层,或/及缓冲层,例如无机膜层,像是氧化硅。进一步地,基板110连接触控面的侧表面可以具有弧形结构或梯形结构。另外,基板110也可以是液晶显示器的彩色滤光基板、有机发光二极管显示器的封装盖板等,但不以此为限。

[0061] 这些第一导电单元120沿着一第一方向d1延伸且彼此电性绝缘。第一导电单元120包括多个第一电极122以及多个第一连接部124,相邻两个第一电极122由其中一个第一连接部124电性连接。但本发明不限于此,在其他实施例中,相邻两个第一电极122也可以由多个,例如是两个第一连接部124电性连接。第二导电单元130沿着一第二方向d2延伸且彼此电性绝缘。第二导电单元130包括多个第二电极132以及多个第二连接部134,相

邻两个第二电极 132 由其中一个第二连接部 134 电性连接。但本发明不限于此,在其他实施例中,相邻两个第二电极 132 也可以由多个,例如是两个第二连接部 134 电性连接。第一方向 d1 与第二方向 d2 相交,较佳为互相垂直。第二导电单元 130 与第一导电单元 120 彼此电性绝缘且彼此交错。第一导电单元 120 与第二导电单元 130 的其中一者为驱动单元,另一者为感测单元,据此,第一导电单元 120 与第二导电单元 130 例如可组成一触控元件,以感测触控事件的位置。

[0062] 图 2 为图 1 的区域 M 的放大示意图。图 2 主要是第一导电单元 120 与第二导电单元 130 交错之处的结构示意图。为了详细说明此处结构,图 3、图 4 以及图 5 分别示出图 2 中的各个膜层。图 6 示出图 2 中的剖面 A-A' 以及 B-B' 的剖面示意图。请同时参照图 2 至图 6,第一电极 122 包括于基板 110 上依序堆叠的一第一子电极 E1 以及一第二子电极 E2,第一子电极 E1 位于基板 110 与第二子电极 E2 之间。第一子电极 E1 与第二子电极 E2 由不同导电层所形成,两者重叠且接触。相邻的两个第一子电极 E1 由第一连接部 124 连接且可由同一导电层形成,故相邻两个第一电极 122 通过第一连接部 124 电性连接。由于第一电极 122 是由两层导电层所形成,故厚度大而可具有较低的传导阻抗。

[0063] 第二电极 132 包括于基板 110 上依序堆叠的一第三子电极 E3 以及一第四子电极 E4,第三子电极 E3 位于基板 110 与第四子电极 E4 之间。第三子电极 E3 与第四子电极 E4 由不同导电层所形成,两者重叠且接触。相邻的两个第四子电极 E4 由第二连接部 134 连接且可由同一导电层形成,故相邻两个第二电极 132 通过第二连接部 134 电性连接。第一子电极 E1 与第三子电极 E3 可由同一导电层形成,第二子电极 E2 与第四子电极 E4 可由同一导电层形成。由于第二电极 132 是由两层导电层所形成,故厚度大而可具有较低的传导阻抗。

[0064] 绝缘图案 140 位在第一导电单元 120 与第二导电单元 130 的交错处。换言之,绝缘图案 140 位在第一导电单元 120 与第二导电单元 130 之间以使两者彼此电性绝缘。绝缘图案 140 可覆盖第一连接部 124。而且绝缘图案 140 可覆盖第一子电极 E1 的一部分以及第三子电极 E3 的一部分。但本发明不限于此,在其他实施例中,绝缘图案 140 可以仅覆盖第一子电极 E1 的一部分或是仅覆盖第三子电极 E3 的一部分。第二连接部 134 设置在绝缘图案 140 上,且第二子电极 E2 的一部分以及第四子电极 E4 的一部分设置在绝缘图案 140 上。但本发明不限于此,在其他实施例中,可以是仅有第二子电极 E2 的一部分设置在绝缘图案 140 上,或是仅有第四子电极 E4 的一部分设置在绝缘图案 140 上。

[0065] 根据本实施例,绝缘图案 140 覆盖部分的第一子电极 E1 且暴露出另一部分的第一子电极 E1。绝缘图案 140 覆盖部分的第三子电极 E3 且暴露出另一部分的第三子电极 E3。被绝缘图案 140 覆盖的第一子电极 E1 与第三子电极 E3 之间具有一第一间隙 G1。未被绝缘图案 140 覆盖的第一子电极 E1 与第三子电极 E3 之间具有一第二间隙 G2。第一间隙 G1 不同于第二间隙 G2,其中第一间隙 G1 的间隙宽度可小于第二间隙 G2 的间隙宽度。但本发明不限于此。第二间隙 G2 的间隙宽度可大于 25 微米,较佳是大于 30 微米。换言之,第一电极 122 与第二电极 124 之间可具有足够的间隙大小,以进一步确保第一电极 122 与第二电极 124 之间不易有短路的问题发生。

[0066] 以另一角度来看,未被绝缘图案 140 覆盖的第一子电极 E1 与第二子电极 E2 的轮廓大致相同,未被绝缘图案 140 覆盖的第三子电极 E3 与第四子电极 E4 的轮廓大致相同。而

且,被绝缘图案 140 覆盖的第一子电极 E1 与位在绝缘图案 140 上的第二子电极 E2 的轮廓不同,被绝缘图案 140 覆盖的第三子电极 E3 与位在绝缘图案 140 上的第四子电极 E4 的轮廓不同。更详细而言,被绝缘图案 140 覆盖的第一子电极 E1 具有一第一突出部 E1a 且第一突出部 E1a 突出于第二子电极 E2 之外。被绝缘图案 140 覆盖的第三子电极 E3 具有一第二突出部 E3a 且第二突出部 E3a 突出于第四子电极 E4 之外。如此一来,第一子电极 E1 的边缘可具有第一断差 h1,且该第一断差 h1 位于绝缘图案 140 的边缘。相似地,第三子电极 E3 的边缘可具有第二断差 h2,且该第二断差 h2 位于绝缘图案 140 的边缘。但本发明不限于此,在第一间隙 G1 不等于第二间隙 G2 的情况下,被绝缘图案 140 覆盖的第一子电极 E1 与位在绝缘图案 140 上的第二子电极 E2 的侧壁也可以是轮廓大致相同的,被绝缘图案 140 覆盖的第三子电极 E3 与位在绝缘图案 140 上的第四子电极 E4 的侧壁也可以是轮廓大致相同的。

[0067] 请再参照图 2 与图 3,在本实施例中,第一导电层 C1 具有多个断差(包括第一断差 h1 以及第二断差 h2),其中第一断差 h1 位在绝缘图案 140 与第一导电单元 120 的交界,且例如是位于第一子电极 E1 上。但本发明不限于此,在其他实施例中,第一断差 h1 也可以是位在第一连接部 124 上或是位在第一子电极 E1 与第一连接部 124 的交界。再者,第二断差 h2 位在绝缘图案 140 与第二导电单元 130 的交界,且例如是位于第三子电极 E3 上。在本发明所有实施例中,第一断差 h1 与第二断差 h2 的部分轮廓实质上是沿着绝缘图案 140 的轮廓而形成,换言之,第一断差 h1 与第二断差 h2 的部分轮廓与堆叠在第一导电层 C1 的绝缘图案 140 的对应轮廓共形。因此,第一断差 h1 与第二断差 h2 的形状不限于本发明所有实施例中图示所揭露的结构,也就是说第一断差 h1 与第二断差 h2 的部分轮廓例如可以是弧形、直线、波浪、锯齿...等。

[0068] 以下将简单说明图 2 的触控面板的制造流程。首先,请参照图 2 与图 3,可以在基板 110 上形成一第一导电层 C1。第一导电层 C1 包括第一连接部 124、待成型的第一子电极以及待成型的第三子电极(未示出)。待成型的第一子电极与待成型的第三子电极具有平顺的边缘 F(即未具有第一断差 h1 与第二断差 h2),故待成型的第一子电极与待成型的第三子电极之间具有单一种间隙,即具有第一间隙 G1。换言之,待成型的第一子电极以及待成型的第三子电极相较于已成型的第一子电极 E1 与第三子电极 E3 具有更广的分布范围,其中待成型的第一子电极以及待成型的第三子电极的边缘 F 例如为图 3 中的虚线所示。

[0069] 第一导电层 C1 可由透明导电材料,例如氧化铟锡(Indium tin oxide, 简称 ITO)、氧化铟锌(Indium-Zinc Oxide, 简称 IZO)、氧化锌镓(GZO)、纳米碳管(Carbon Nanotube)、纳米金属线(例如纳米银丝、静电纺纱)、导电聚合物(conducting polymers)、石墨烯(graphene)、硅烯或其他高导电性的透光材质等所构成,但不以此为限,例如也可采用不透明的金属导电材料。且第一导电层 C1 的型态较佳为连续状薄膜,例如 ITO 薄膜、纳米银丝薄膜、ITO/Ag/ITO 薄膜等;当然,也可采用网格状薄膜,特别是针对金属材料,例如金属网格,但不以此为限。

[0070] 接着,请参照图 2 至图 4,形成多个绝缘图案 140。绝缘图案 140 覆盖第一连接部 124、待成型的第一子电极的一部分以及待成型的第三子电极的一部分。

[0071] 再来,请参照图 2 至图 5,形成一第二导电层 C2,第二导电层 C2 的材料可参考第一导电层 C1 的材料。第二导电层 C2 包括第二连接部 134、第二子电极 E2 以及第四子电极

E4。第二导电层 C2 的形成方法例如是先形成一导电材料层,以全面覆盖基板 110、第一导电层 C1 以及绝缘图案 140。接着,进行一图案化制程以形成第二导电层 C2。第二子电极 E2 与第四子电极 E4 之间的间隙为第二间隙 G2,第二间隙 G2 的间隙宽度大于第一间隙 G1 的间隙宽度。换言之,第二子电极 E2 与第四子电极 E4 的图案小于待成型的第一子电极与待成型的第三子电极的图案,故在进行上述图案化制程时,是一并将部分的第一导电层 C1 与第二导电层 C2 移除。而且,由于第二间隙 G2 大于第一间隙 G1,故可确保第一电极 E1 与第二电极 E1 之间不易有薄膜残留的现象,以减少第一导电单元 120 与第二导电单元 130 (示出于图 1) 短路的情况发生。而且,由于绝缘图案 140 覆盖待成型的第一子电极与待成型的第三子电极的一部分,故第一间隙 G1 与第二间隙 G2 的交界处可形成第一断差 h1 及第二断差 h2,其中未被移除的待成型的第一子电极与待成型的第三子电极的部分即形成了第一突出部 E1a 与第二突出部 E3a。

[0072] 请参照图 2 及图 6,第一连接部 124 是由第一导电层 C1 形成,第二连接部 134 是由第二导电层 C2 形成,其中第一导电层 C1 的厚度可大于第二导电层 C2 的厚度。第一导电层 C1 厚度例如是第二导电层 C2 厚度的 1.05 倍至 8 倍。第一导电层 C1 的传导阻抗可小于第二导电层 C2 的传导阻抗,故第一连接部 124 的线宽 W1 可小于第二连接部 134 的线宽 W2。本实施例的第一导电单元 120 例如是感测单元,第二导电单元 130 例如是驱动单元,其中第二导电单元 130 的第二连接部 134 的长度比第一导电单元 120 的第一连接部 124 的长度短,且第二导电单元 130 的第二连接部 134 的线宽比第一导电单元 120 的第一连接部 124 的线宽大。如此一来,第一导电单元 120 可具有良好的感测效果,且第二导电单元 130 可具有良好的驱动效果,但本发明不限于此。

[0073] 在另一实施例中,第一导电层 C1 的厚度也可小于第二导电层 C2 的厚度,如图 7 所示。选择性地,在图 7 的实施例中,基于低传导阻抗的考量,可以使图 2 中属于第一导电层 C1 的第一连接部 124 的线宽 W1 大于属于第二导电层 C2 的第二连接部 134 的线宽 W2。但本发明不限于此。此外,若图案化第二导电层 C2 的图案化制程为蚀刻制程,则第二导电层 C2 的厚度大于第一导电层 C1 的厚度时,将有助于第一导电层 C1 能够被确实地被移除。或者,使第二导电层 C2 的结晶性大于第一导电层 C1 的结晶性,即第二导电层 C2 的结晶颗粒尺寸大于第一导电层 C1 的结晶颗粒尺寸,也能有助于第一导电层 C1 能够在蚀刻制程中确实地被移除。第二导电层 C2 厚度例如是第一导电层 C1 厚度的 1.05 倍至 8 倍。但本发明不限于此。在其他实施例中,第二导电层 C2 的结晶颗粒尺寸也可以小于第一导电层 C1 的结晶颗粒尺寸。

[0074] 图 8 为图 1 的触控面板 100 的局部上视示意图。图 9 为沿图 8 的剖面 C-C' 的剖面示意图。请参照图 8 以及图 9,触控面板 100 可选择性地包括多个拟置图案 150 (dummy pattern)。拟置图案 150 设置于第一电极 122 与第二电极 132 之间,其中拟置图案 150 与第一电极 122 之间的间隙 G 等于第二间隙 G2,且拟置图案 150 与第二电极 132 之间的间隙 G 等于第二间隙 G2。拟置图 150 的设置可以减少使用者察觉第一电极 122 与第二电极 132 的设置,故能有助于改善触控面板 100 的视觉效果。拟置图案 150 可由第一导电层 C1 的一部分以及第二导电层 C2 的一部分共同构成而为双层结构,但本发明不限于此。拟置图案 150 也可以仅由第二导电层 C2 的一部分构成而为单层结构。

[0075] 触控面板 100 可以还包括一缓冲层 160,如图 10 所示。缓冲层 160 覆盖基板 110

且位于基板 110 与第一导电层 C1 之间。缓冲层 160 可以确保第一导电层 C1 在蚀刻制程中能够有效地被移除,而不易有薄膜残留的问题。缓冲层 160 的材料包括有机材料或无机材料。缓冲层 160 的材料较佳包括聚亚酰胺、环氧树脂、硅氧烷、亚克力树脂或其他透明性树脂,但不限于此,例如也可采用氧化铌、氧化硅 ( $\text{SiO}_x$ )、氧化氮或上述的组合,例如氧化硅搭配氧化氮,藉以使图案化后的导电层的轮廓较不易被看见。以二氧化硅为例,厚度介于 300 埃米 (Angstrom,  $\text{\AA}$ )  $\sim$  1000  $\text{\AA}$  之间。以树脂为例,厚度介于 0.1 微米 ( $\mu\text{m}$ )  $\sim$  3 微米 ( $\mu\text{m}$ ) 之间。

[0076] 图 11 为本发明另一实施例的触控面板的局部上视示意图。图 12 为图 11 的触控面板的第一导电层的示意图。请参照图 11 与图 12,与触控面板 100 类似地,触控面板 100a 例如是由第一导电层 C1、绝缘图案 140 以及第二导电层 C2 所形成其中第一导电层 C1 具有多个第一断差  $h_1$  以及多个第二断差  $h_2$ 。再者,本实施例的相邻两个第一电极 122 例如是由两个第一连接部 124 电性连接。而且,本实施例的相邻两个第二电极 132 例如是由两个第二连接部 134 电性连接。此外,在此实施例中,绝缘图案 140 例如是覆盖电性连接相邻两个第一电极 122 的两个第一连接部 124,但本发明不限于此。在其他实施例中,也可以是由两个绝缘图案 140 各自覆盖其中一个第一连接部 124,如图 13 所示。

[0077] 图 14 为本发明另一实施例的触控面板的局部上视示意图。图 15 为图 14 的触控面板的第一导电层的示意图。本实施例的触控面板 100b 与前述的触控面板 100 相似,其不同之处在于,绝缘图案 140 仅覆盖第三子电极 E3 的一部分而未覆盖第一子电极 E1 的一部分,而且绝缘图案 140 完全覆盖第一连接部 124。由于绝缘图案 140 覆盖第一连接部 124 而未覆盖第一子电极 E1 且完全覆盖第一连接部 124,因此,在第二导电层 C2 完成制作后,第一断差  $h_1$  位于第一子电极 E1 与第一连接部 124 的交界。

[0078] 图 16 为本发明另一实施例的触控面板的局部上视示意图。图 17 为图 16 的触控面板的第一导电层的示意图。本实施例的触控面板 100c 与前述的触控面板 100 相似,其不同之处在于,绝缘图案 140 仅覆盖第三子电极 E3 而未覆盖第一子电极 E1,而且绝缘图案 140 覆盖第一连接部 124 的一部分,且暴露出第一连接部 124 的另一部分。由于绝缘图案 140 未覆盖第一子电极 E1 以及第一连接部 124 的一部分,因此,在第二导电层 C2 完成制作后,第一断差  $h_1$  位于第一连接部 124 上。

[0079] 图 18 为本发明另一实施例的触控面板的局部上视示意图。请参照图 18,与前述实施例类似地,触控面板 100a 例如是由第一导电层 C1、绝缘图案 140 以及第二导电层 C2 所形成。图 19 为图 18 的触控面板的第一导电层的示意图,且触控面板 100a 的绝缘图案 140 以及第二导电层 C2 的结构与图 4 及图 5 相同。请同时参照图 18 以及图 19,触控面板 100a 与触控面板 100 相似,其不同之处在于,被绝缘图案 140 覆盖的第一子电极 E1 与第三子电极 E3 之间的第一间隙  $G_1$  大于未被绝缘图案 140 覆盖的第一子电极 E1 与第三子电极 E3 之间的第二间隙  $G_2$ 。具体而言,被绝缘图案 140 覆盖的第一子电极 E1 具有一第一内缩部 E1b 且第一内缩部 E1b 内缩于第二子电极 E2 之内。被绝缘图案 140 覆盖的第三子电极 E3 具有一第二内缩部 E3b 且第二内缩部 E3b 内缩于第四子电极 E4 之内。此外,触控面板 100a 的制程过程与触控面板 100 相似,请参考前述实施例,其差异之处在于第一导电层 C1 的结构不同。具体而言,在此实施例中,当第一导电层 C1 完成后,待成型的第一子电极与待成型的第三子电极之间就具有两种间隙,其中预计会被绝缘图案 140 覆盖的间隙即为第一间隙  $G_1$ 。

另外,预计不会被绝缘图案 140 覆盖的间隙例如是小于第一间隙 G1 且大于第二间隙 G2。而且,在进行图案化制程以形成第二导电层 C2 之后,未被绝缘图案 140 覆盖的间隙变成第二间隙 G2。

[0080] 综上所述,本发明的触控面板包括多个导电单元,且每一个导电单元包括多个电极和多个连接部,其中该些电极是由双层导电结构所构成,因此具有较低的传导阻抗,进而提升触控面板触控灵敏度。

[0081] 最后应说明的是:以上各实施例仅用以说明本发明的技术方案,而非对其限制;尽管参照前述各实施例对本发明进行了详细的说明,本领域的普通技术人员应当理解:其依然可以对前述各实施例所记载的技术方案进行修改,或者对其中部分或者全部技术特征进行等同替换;而这些修改或者替换,并不使相应技术方案的本质脱离本发明各实施例技术方案的范围。

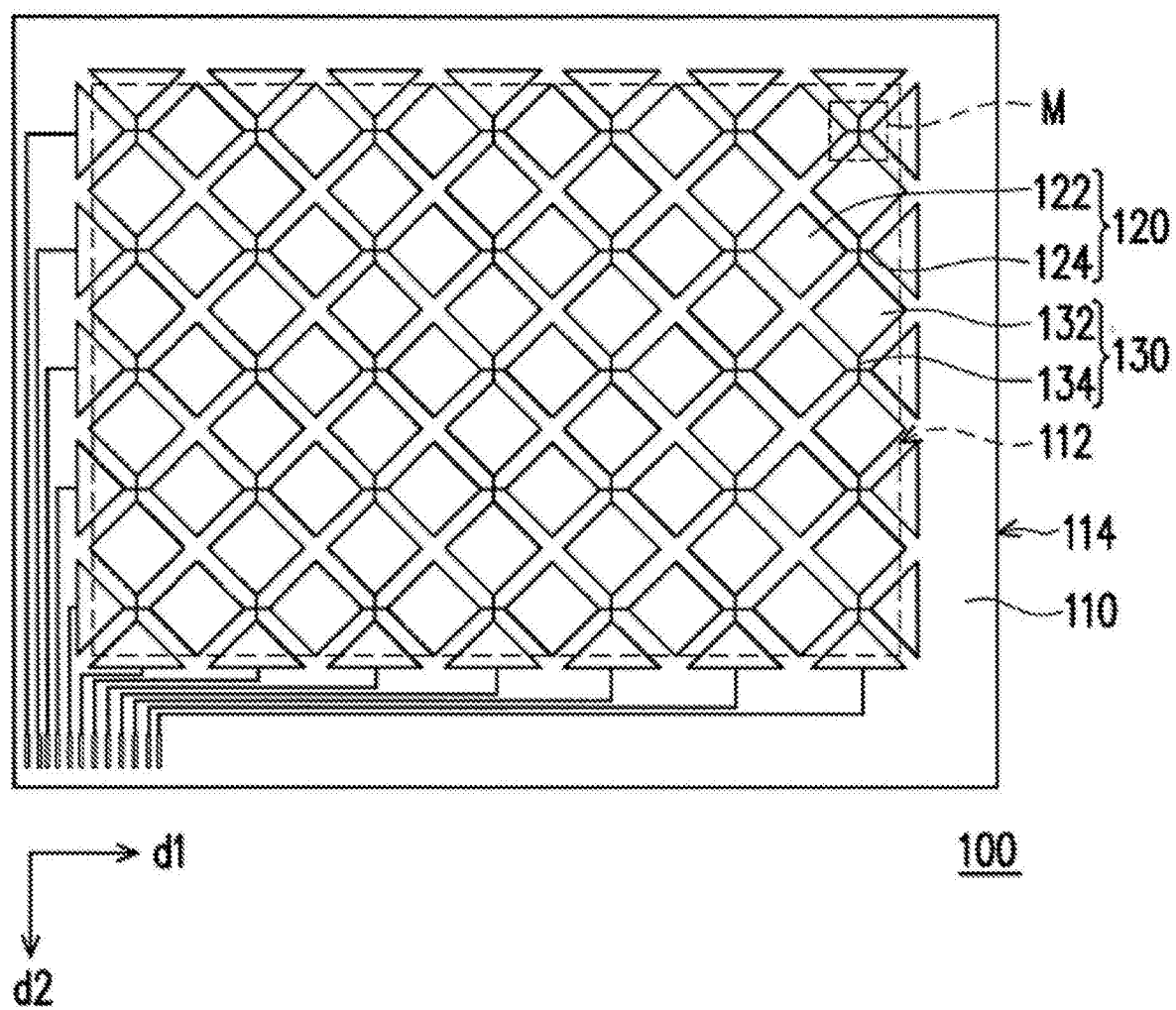


图 1

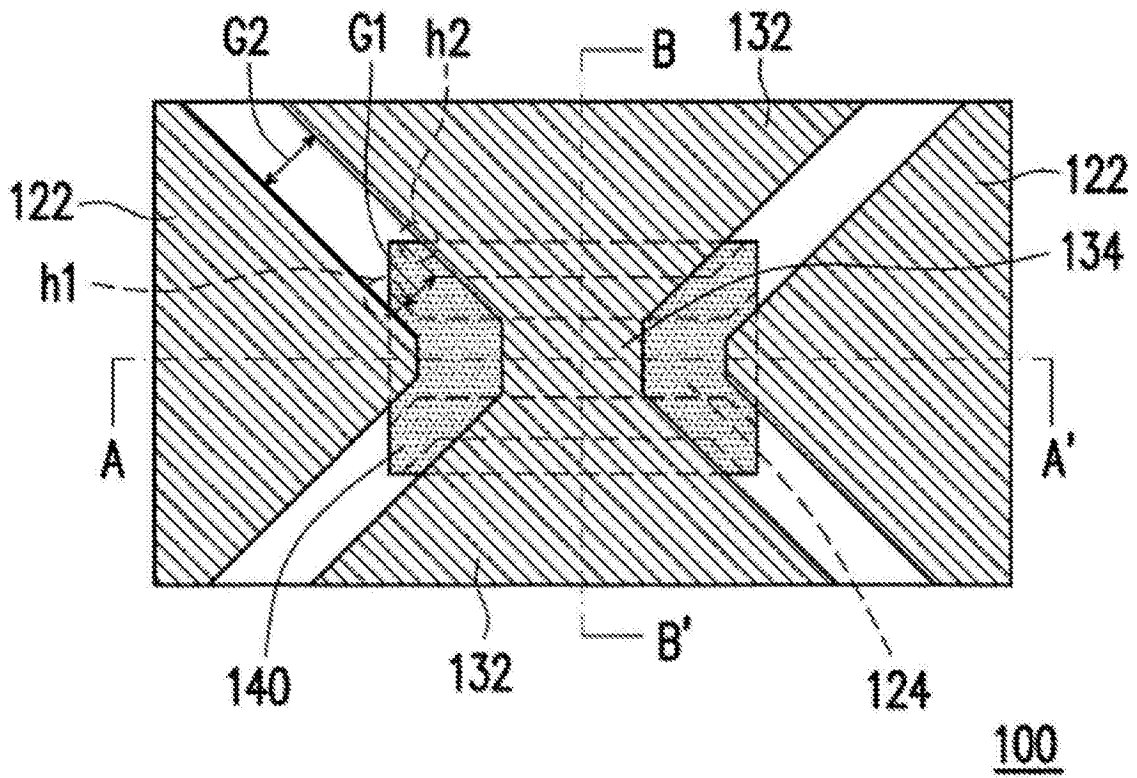


图 2

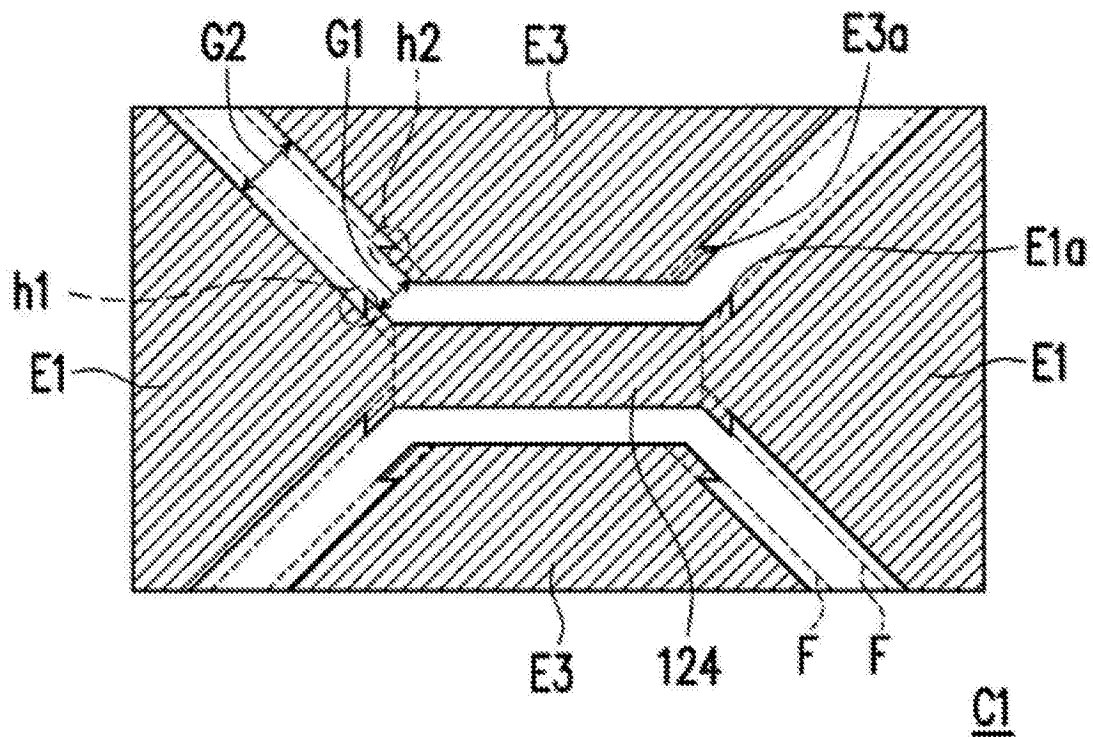


图 3

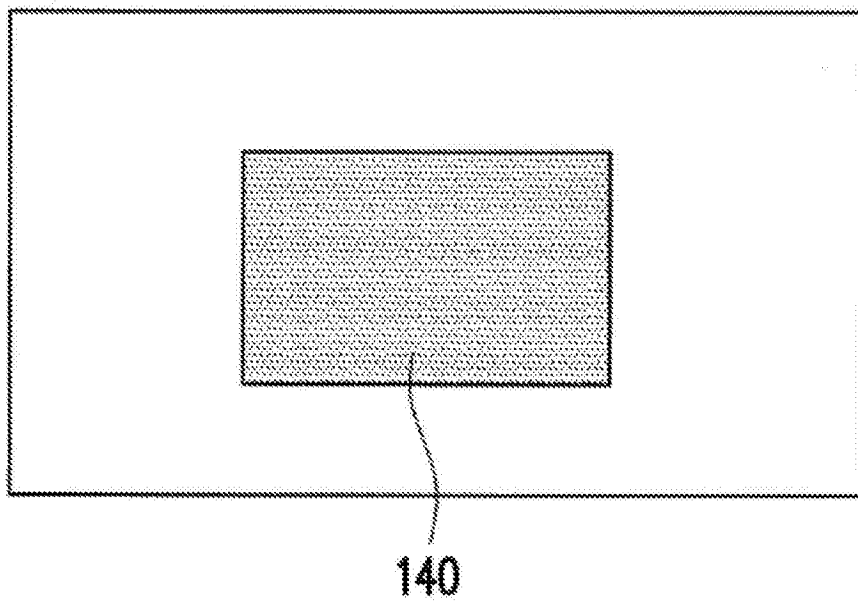


图 4

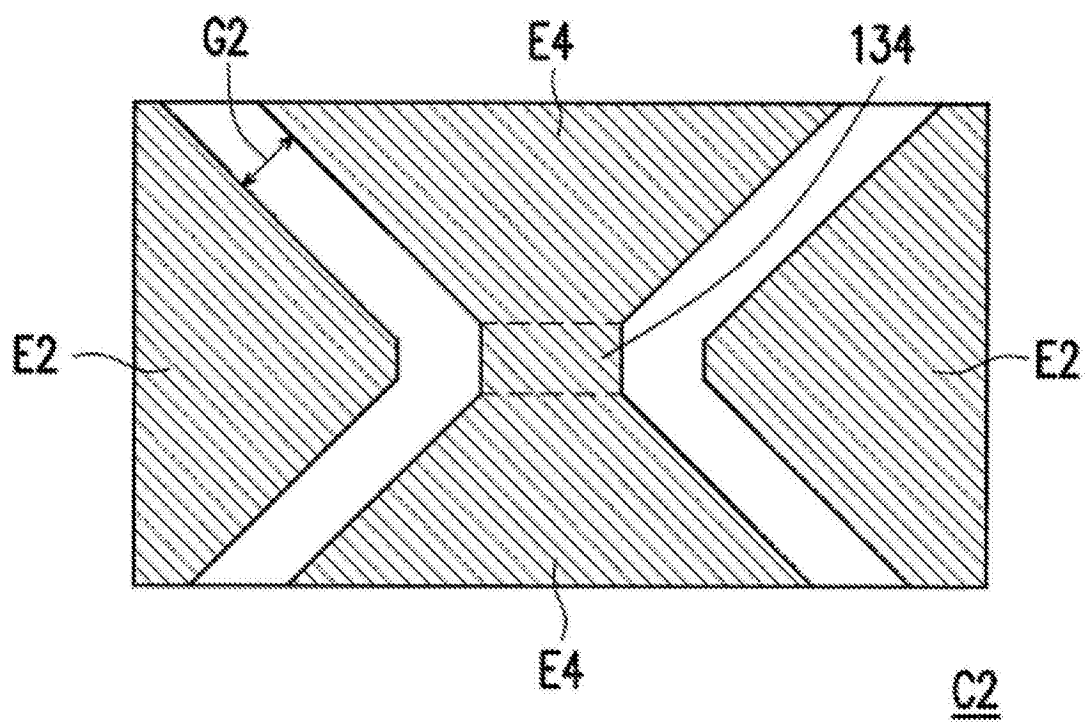


图 5

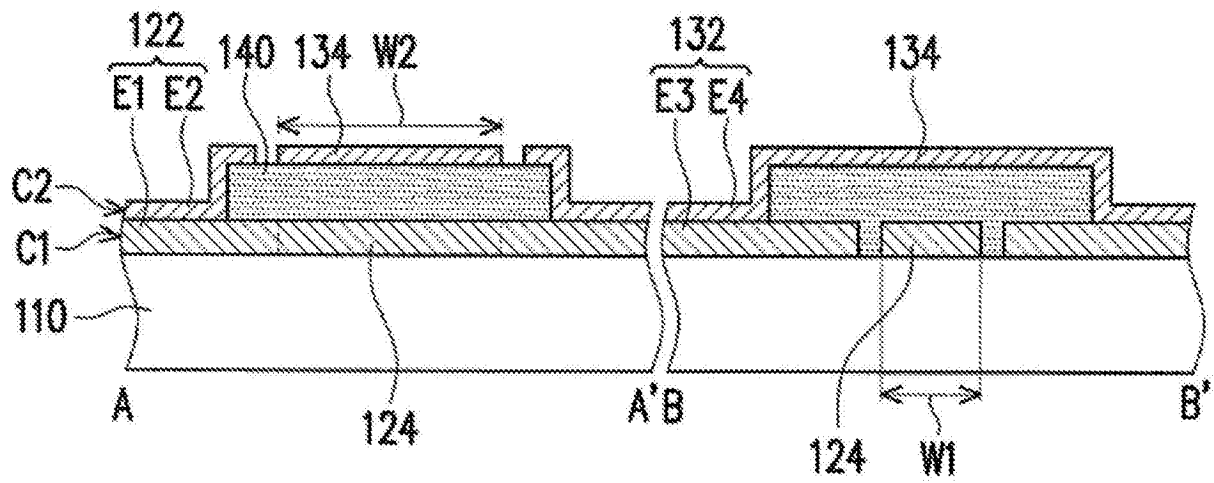


图 6

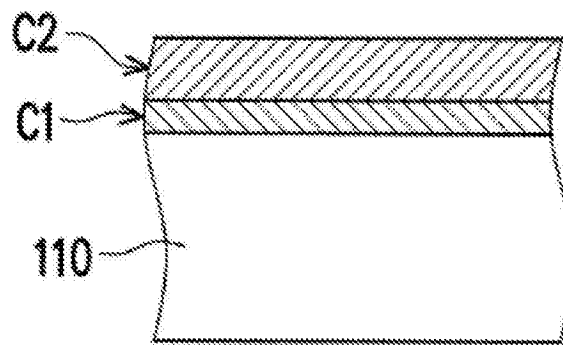


图 7

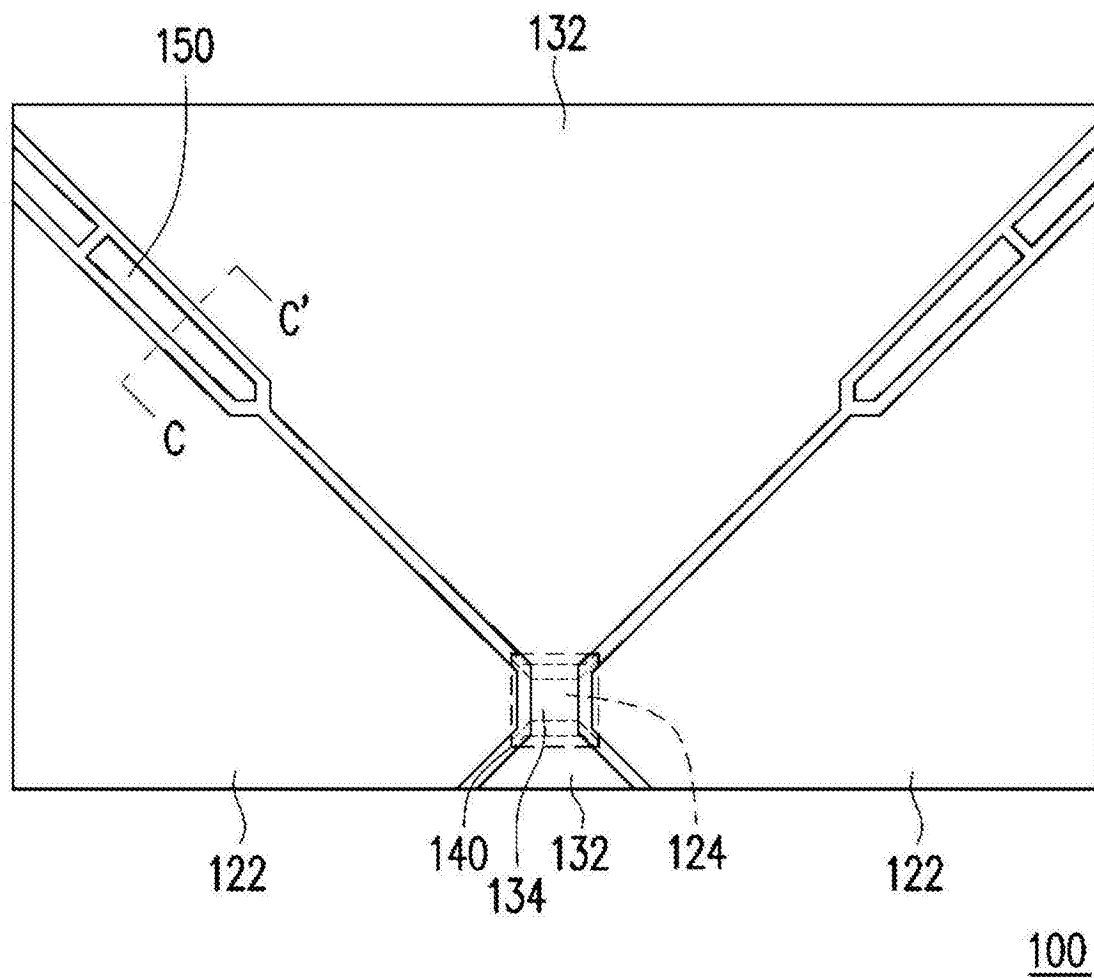


图 8

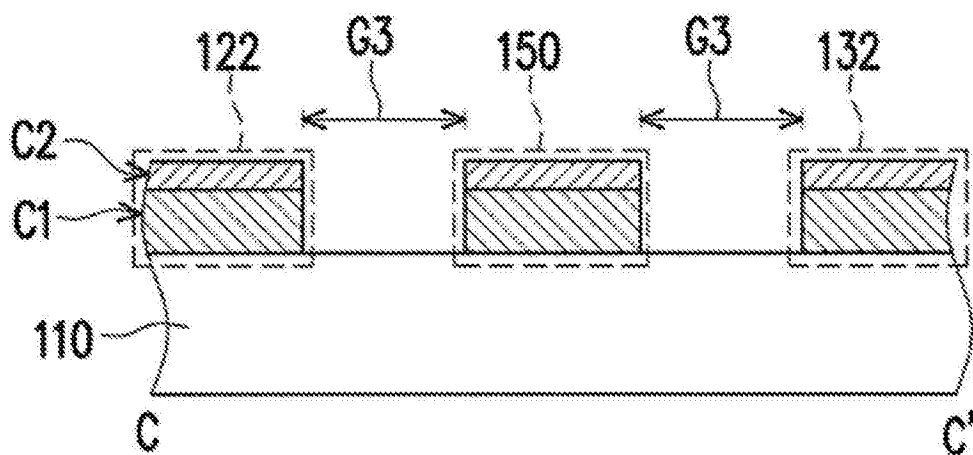


图 9

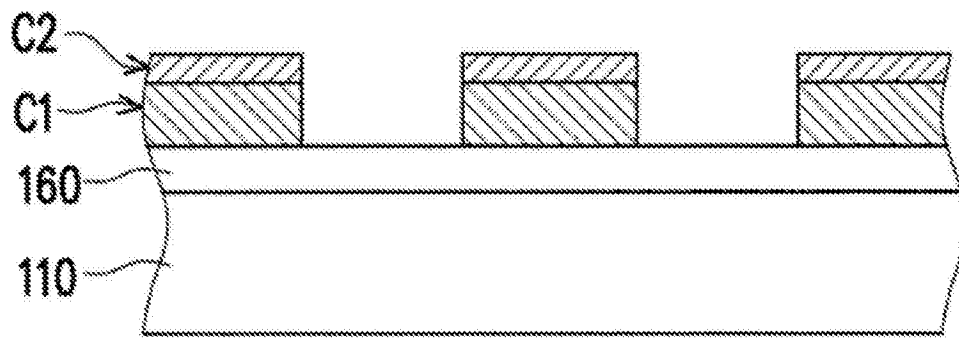


图 10

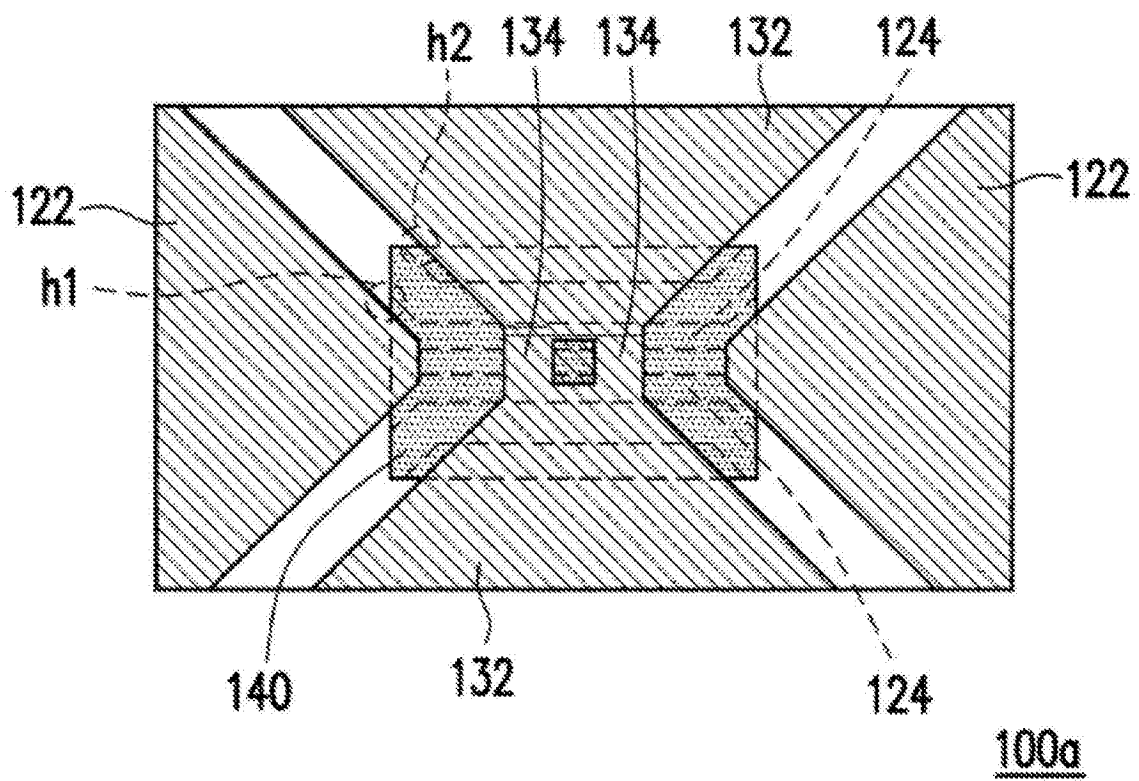


图 11

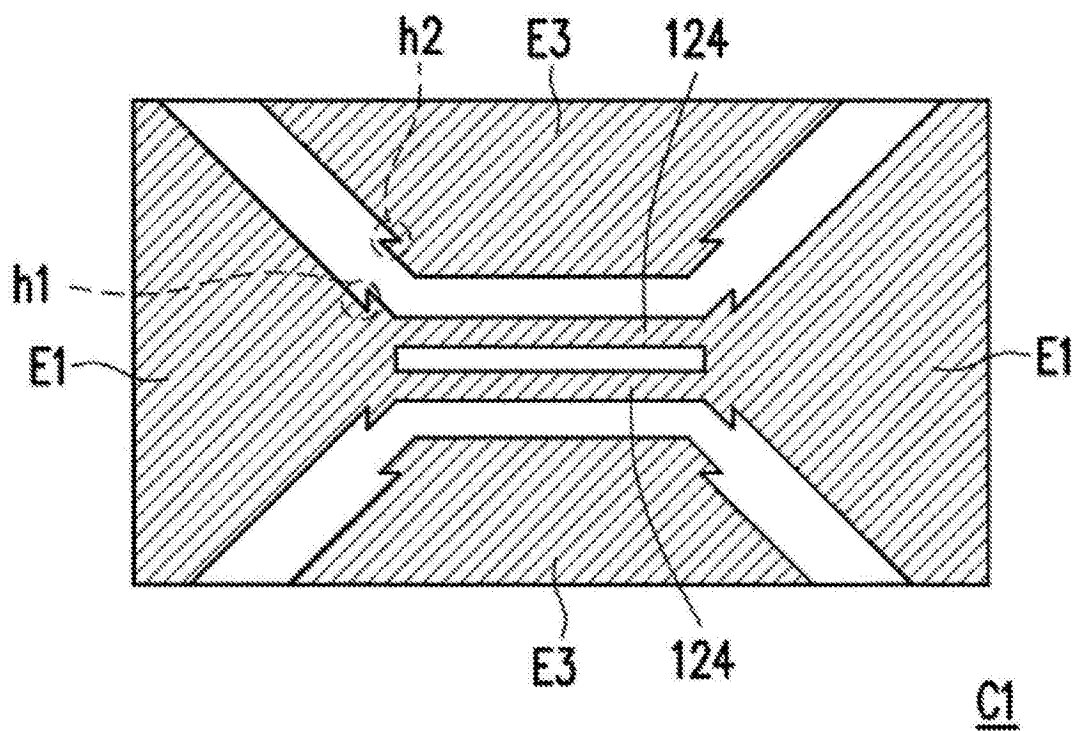


图 12

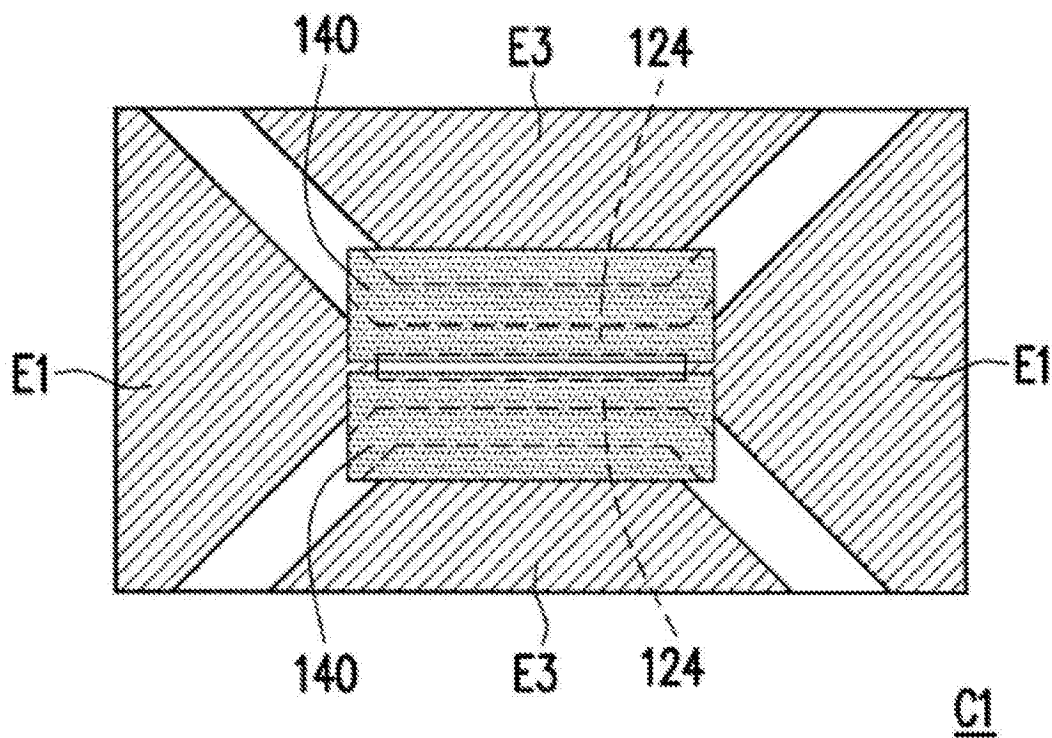


图 13

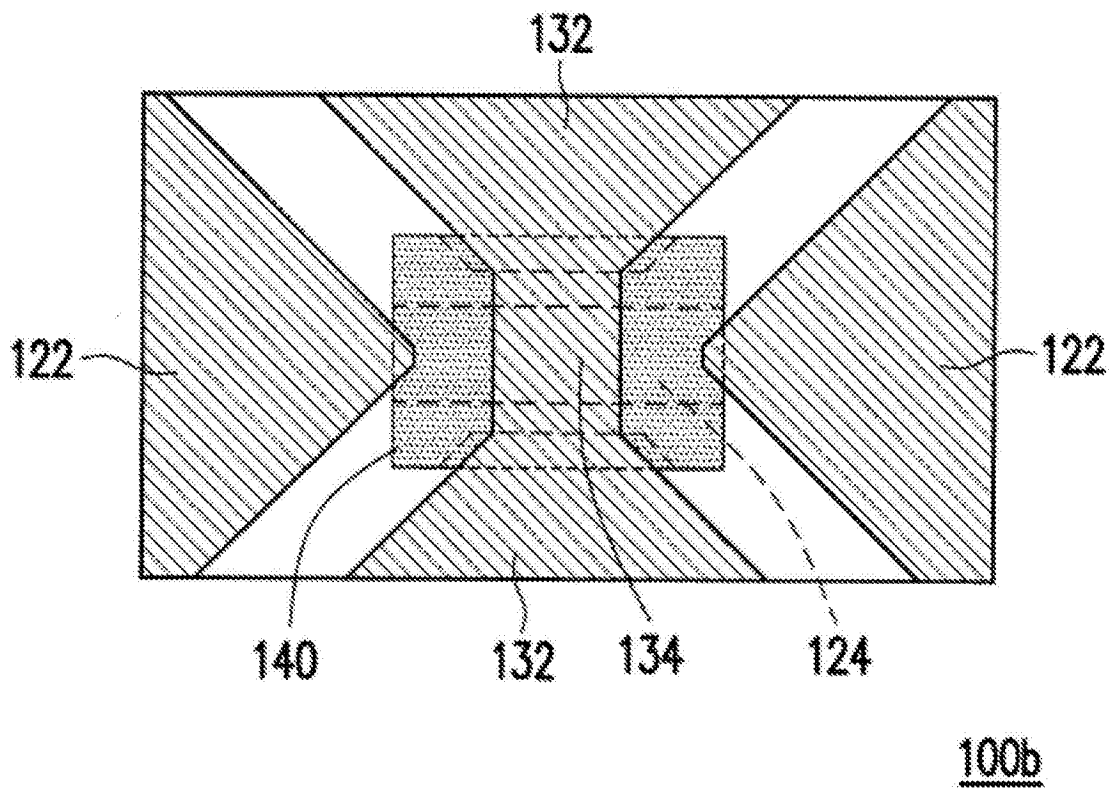


图 14

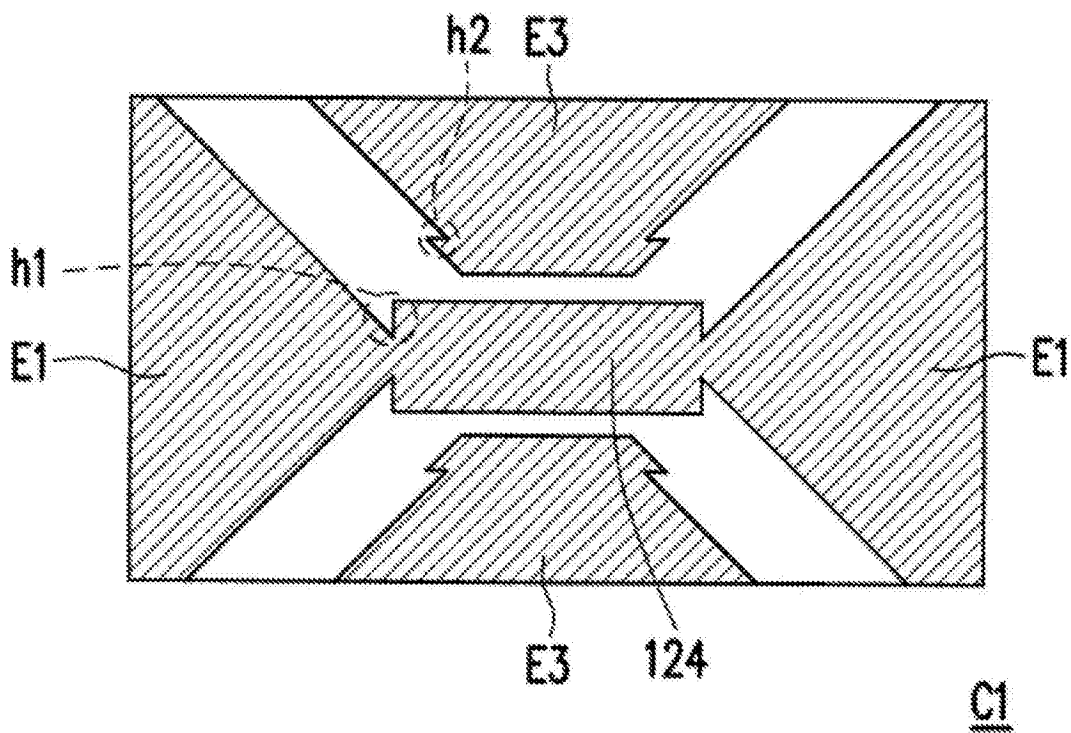


图 15

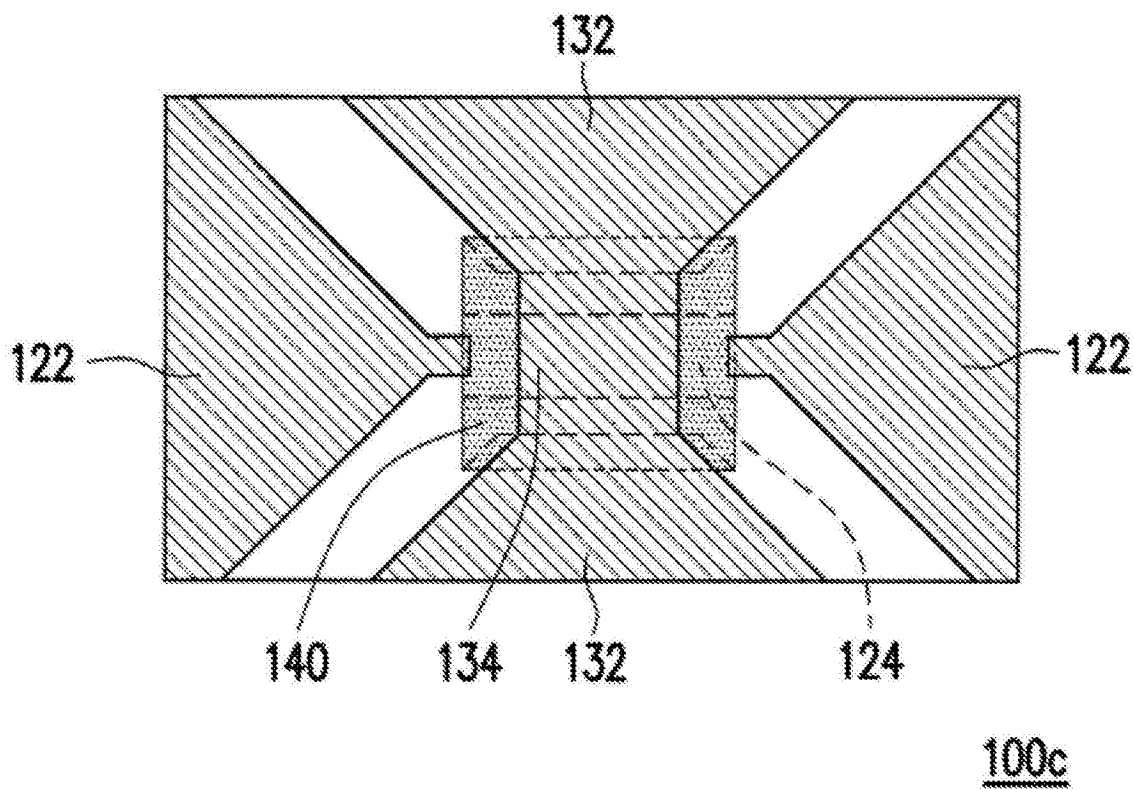


图 16

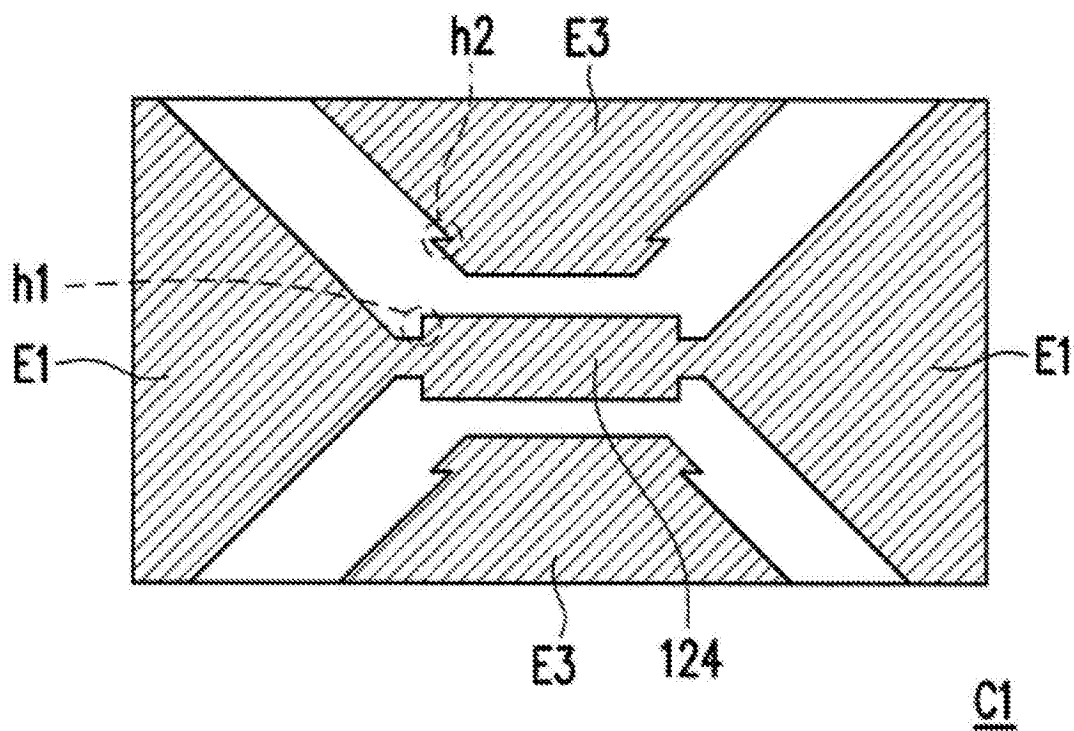


图 17

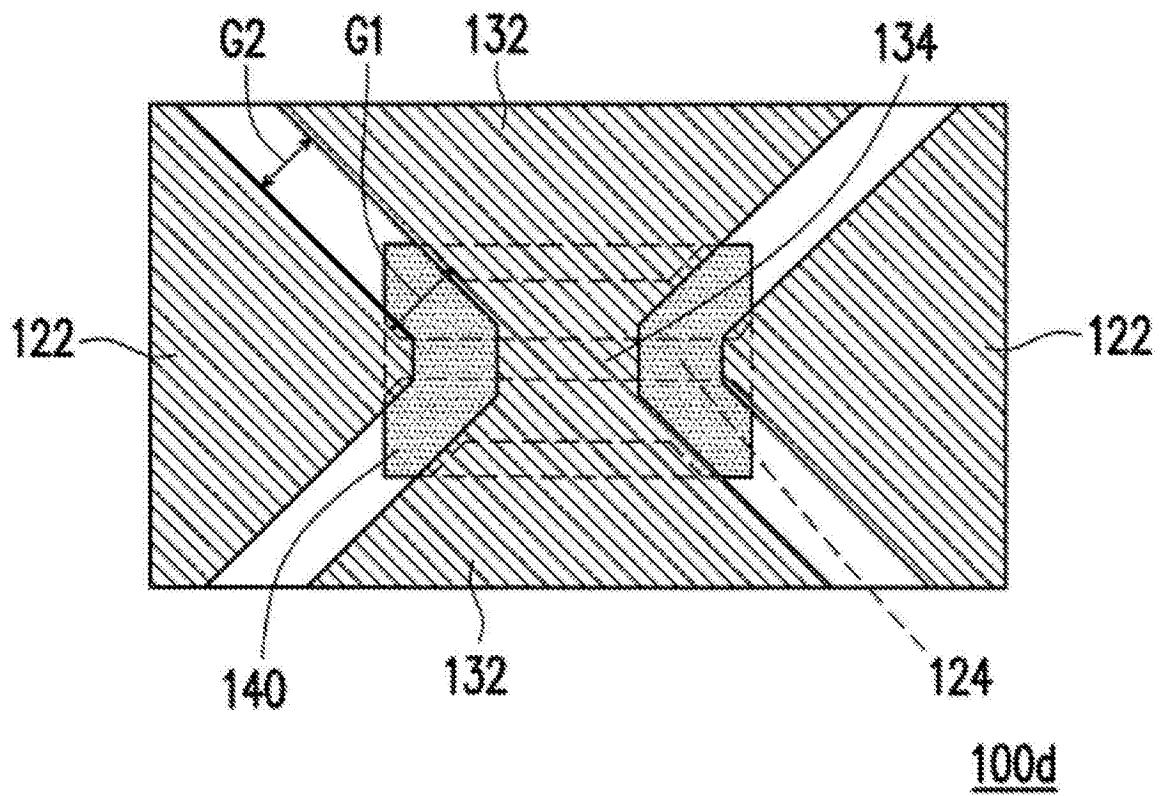


图 18

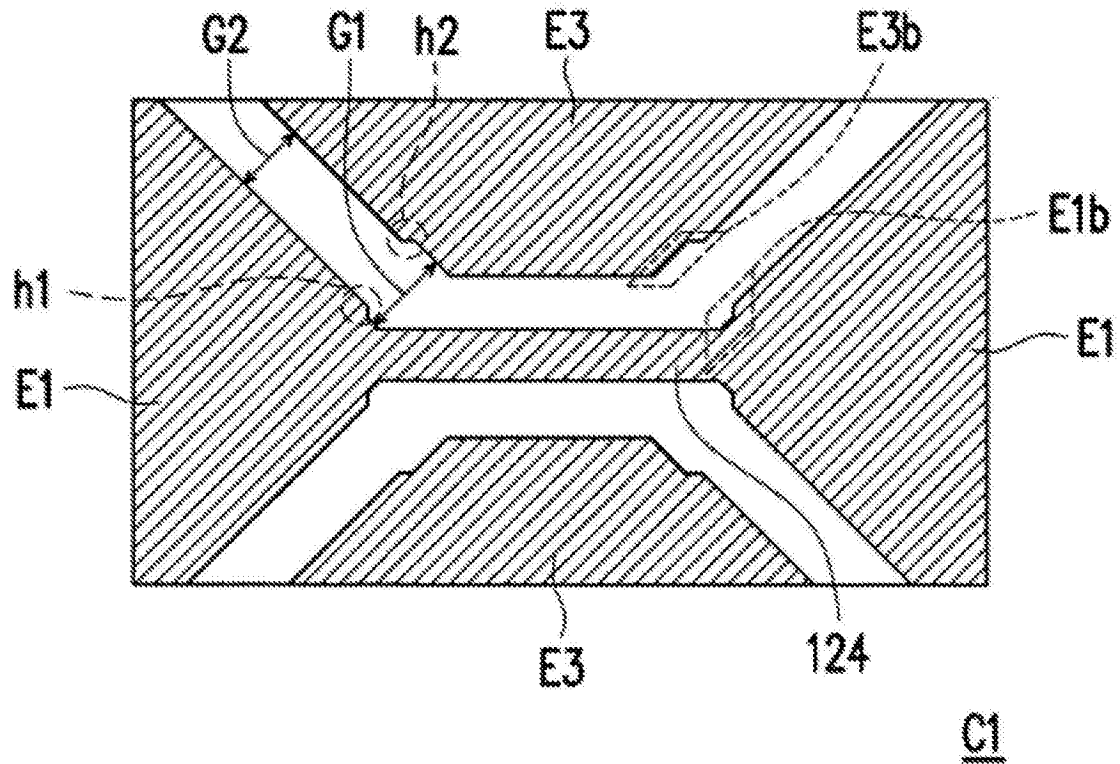


图 19