

Pixel Circuits for OLED Displays



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Abstract The structures, operating principles and technical issues of OLED pixel circuits are explained in this chapter. First, the necessity and role of the OLED pixel circuit is introduced. Then, three operating principles: diode-connection, source-follower and current programming schemes of in-pixel compensation techniques are explained. Other compensation techniques utilizing a complicated system outside the display panel are also introduced. Moreover, three examples of OLED pixel circuits employed in mobile display products are analysed in detail. Finally, the effect of the V_T extraction time and dimming method on low-grey-level mura, is discussed.

1 The Need for OLED Pixel Circuit

Unlike liquid crystal displays (LCD), organic light-emitting diode (OLED) displays require a circuit in every pixel. A single transistor as an on/off switch in each pixel is usually sufficient to operate an LCD, but at least two transistors are required for each pixel of an OLED display as shown in Fig. 1.

1.1 OLED Driving in a Display

OLEDs exhibit non-uniform luminance-to-voltage (L-V) characteristics even on a single substrate due to the non-uniformity of the fabrication process. In addition, non-uniform degradation of L-V characteristics occurs during operation because the cumulative light-emitting time differs from pixel to pixel. However, the luminance-to-current (L-I) characteristics are more uniform and stable against the process non-uniformity and long-term operation. Therefore, it is difficult to express precise grey levels with an OLED by adjusting the voltage across it, as shown in Fig. 2a, or by modulating the duty ratio with a constant supply voltage. On the other hand, the

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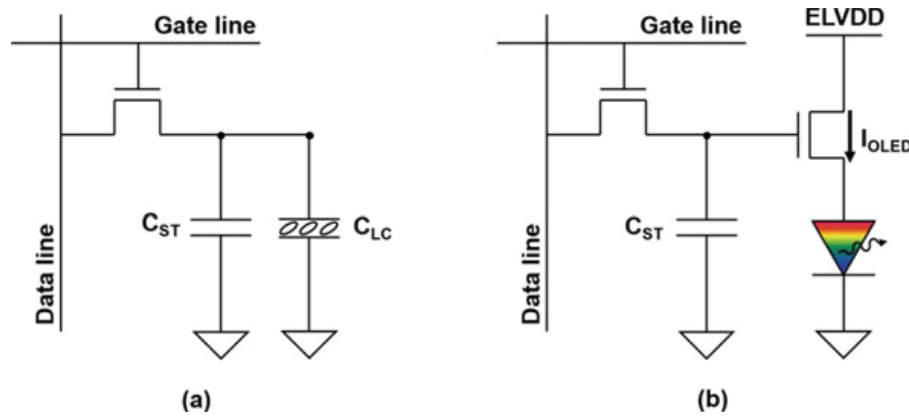


Fig. 1 Comparison of the pixel structures of **a** an LCD and **b** an OLED display

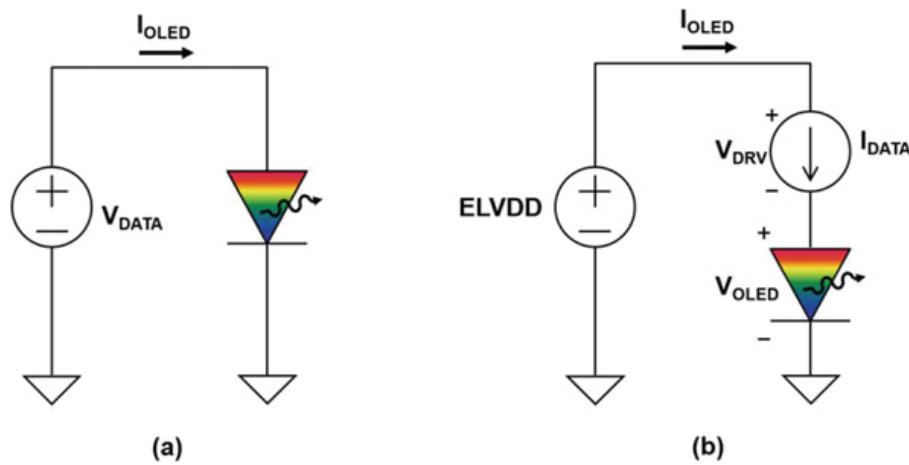


Fig. 2 **a** Voltage driving of OLED. **b** Current driving of OLED

current driving scheme shown in Fig. 2b is more likely to be utilized for uniform and stable grey-level expression. The current source in the current driving scheme gives rise to additional power consumption for the same OLED current compared with the voltage driving scheme.

1.2 Role of the OLED Pixel Circuit

The I-V characteristics of an OLED tend to degrade with operation time as illustrated in Fig. 3a. Therefore, the voltage across the OLED, V_{OLED} increases to keep the current, I_{OLED} constant as illustrated in Fig. 3b [1]. In this case, the voltage across the current driver, V_{DRV} , in Fig. 2b, decreases when the supply voltage, ELVDD, is constant. This function—the maintenance of a constant I_{OLED} against the inevitable V_{OLED} change—is the first role of the OLED pixel circuit. If this is not fulfilled

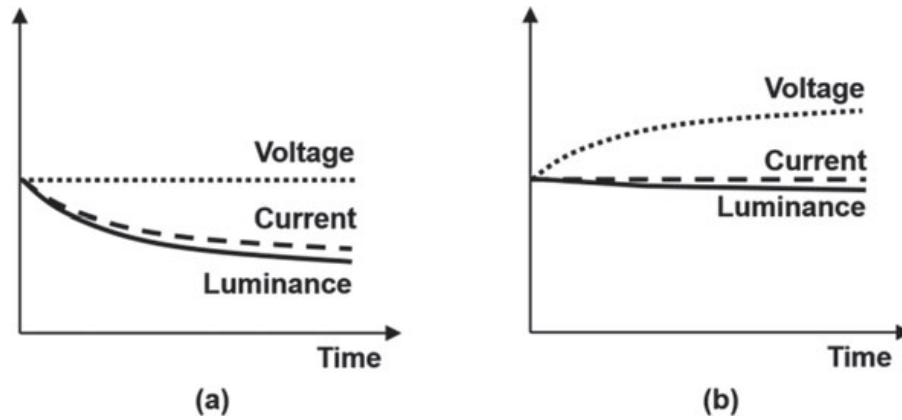
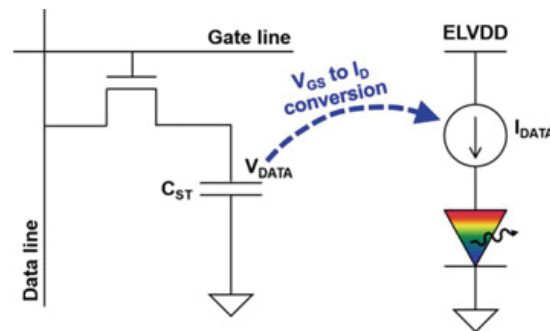


Fig. 3 Degradation of OLED performance: **a** in constant-voltage driving and **b** in constant-current driving

properly, OLED degradation will result in the appearance of severe image sticking on the screen.

The current driver is made of a thin-film transistor (TFT) in the saturation regime. Therefore, the drain-to-source voltage, V_{DS} , of the TFT has little effect on the drain current, which is the same as the I_{OLED} . The drain current of the TFT is predominantly determined by the gate-to-source voltage, V_{GS} , which is stored in a capacitor, C_{ST} , and refreshed every frame as in the case of active-matrix LCD driving. However, the I-V characteristics of many TFTs exhibit large deviations so the current of the TFT is not uniform from pixel to pixel although precise data voltage is stored in C_{ST} . Usually, 256 different voltage levels are stored in C_{ST} and 256 corresponding current levels should be precisely generated by the TFT, as shown in Fig. 4. The voltage difference between adjacent grey levels is as small as several millivolts in some cases. However, for example, the deviation of the threshold voltage, V_T , of the TFT is sometimes hundreds of millivolts, even on a single substrate. Therefore, without any special technique, the luminance of each pixel is not uniform. The second role of the OLED pixel circuit is to compensate for the non-uniform characteristics of the TFT and to generate uniform grey-level current according to the various data voltage levels. Figure 5 shows the display images of an OLED panel without and with the compensation function, respectively, in the pixel circuit [2].

Fig. 4 Analog voltage-to-current conversion in a pixel of an OLED display



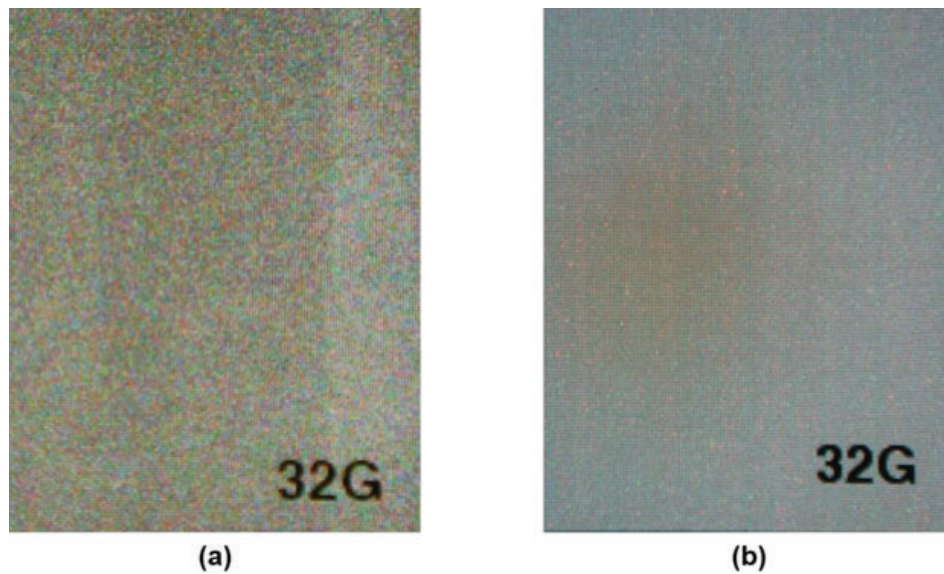


Fig. 5 Display images of OLED panel: **a** without compensation function, **b** with compensation function

The supply voltage ELVDD at a certain pixel drops compared with that at the input pad of the display panel because some current for OLED driving flows through the thin metal line of the ELVDD that has non-zero resistance. For a large-sized OLED display, this drop in supply voltage, the so-called IR drop, should not affect the I_{OLED} value. This requirement should also be satisfied by the OLED pixel circuit.

1.3 TFT-to-OLED Connection Structure

The OLED and the current driver TFT can be connected in two ways, as shown in Fig. 6. The first option is to connect the TFT to the anode of the OLED, as shown in Fig. 6a. This is called the common-cathode structure because the cathode is shared by all the pixels on a display panel and the anode is separated pixel by pixel. The second way is the common-anode structure where a TFT is connected to the cathode of the OLED and the anode is shared by all the pixels, as shown in Fig. 6b.

All the commercially produced OLED displayed so far have had the common-cathode structure because it can be easily fabricated with high resolution. The reason for this is as follows. The TFT fabrication process normally precedes the OLED deposition process, since the water, oxygen, plasma, etc. utilized in the TFT process severely degrade the performance of the OLED. In the OLED process, an anode made of ITO is normally deposited before the organic light-emitting layer, which is apt to be damaged by the plasma during the anode deposition process. As a result, the anode is placed between the TFT and the OLED layers, so it is easy to connect the TFT to the anode rather than the cathode of the OLED. In addition, without the delicate OLED layers, the via hole connecting the TFT and the OLED anode can be

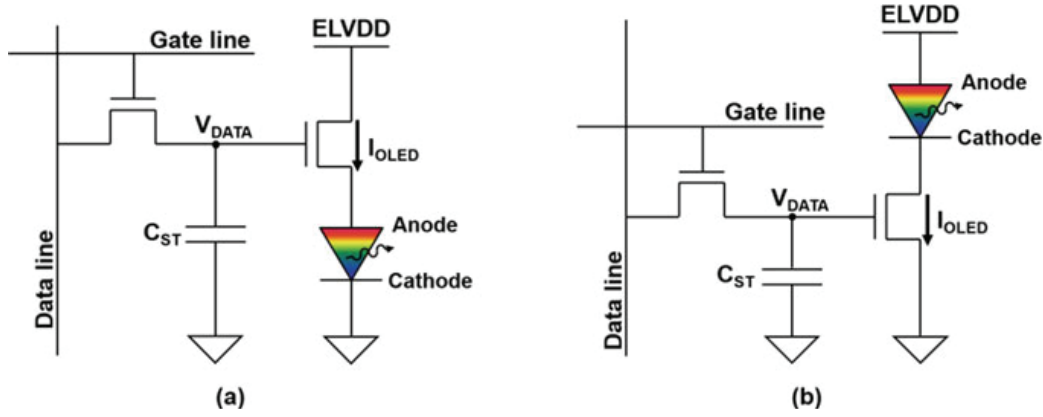


Fig. 6 Two ways of TFT and OLED connection: **a** common-cathode structure and **b** common-anode structure

formed using a photolithography process, resulting in a more efficient pixel layout than the common-anode structure, in which much larger connecting hole is required to connect the uppermost cathode and the TFT.

Figure 7 shows examples of C_{ST} connection in the pixel circuit. When an n-channel TFT is used as the current driver, C_{ST} should be connected between the gate and source terminals of the current driver TFT, as shown in Fig. 7b, because only this structure preserves the V_{GS} of the TFT against the variation in OLED characteristics. If C_{ST} is connected between the gate and a DC voltage, as shown in Fig. 7a, the V_{GS} of the current driver TFT is affected by V_{OLED} . So, this structure is vulnerable to severe image sticking. When a p-channel TFT is used as the current driver, C_{ST} can be connected between the gate of the TFT and any DC voltage, as shown in Fig. 7c. The variation of OLED I-V characteristics has little effect on I_{OLED} because the OLED only affects the V_{DS} of the TFT.

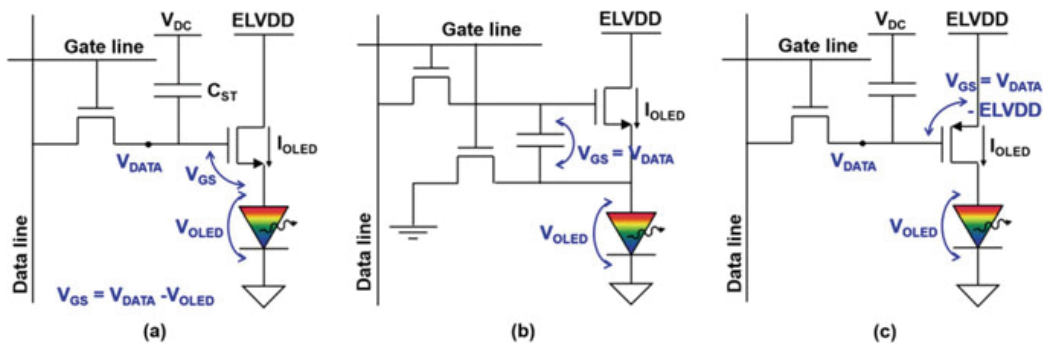


Fig. 7 **a** C_{ST} connection between the gate of an n-channel TFT and a DC voltage, **b** C_{ST} connection between the gate and source of an n-channel TFT, **c** C_{ST} connection between the gate of a p-channel TFT and a DC voltage

2 Operating Principles of OLED Pixel Circuit

There are many device parameters that determine the I-V characteristics of a TFT, e.g. threshold voltage V_T , field-effect mobility μ_{FE} and subthreshold swing S.S. Among these parameters, V_T is the most important because the current driver TFT operates with the V_{GS} value around V_T , where the drain current is exponentially dependent upon V_{GS} . So, the operation of an OLED pixel circuit is primarily focused on compensating for the V_T non-uniformity of the current driver TFT.

However, V_T is not everything. TFTs may have different μ_{FE} and S.S. values even if they have the same V_T . We need to compensate for the non-uniformity at every current level over the whole grey scale in use to completely remove the mura, which is practically impossible. In fact, the pixel circuit designed to compensate for the non-uniform V_T also compensates for the non-uniformity of μ_{FE} and S.S. Precisely speaking, such a circuit reduces the current deviation for the current level reached at the end of the compensation period. This is discussed in detail in Sect. 4.

2.1 In-Pixel Compensation

The current of the driver TFTs over the entire panel becomes uniform if the V_T of the driver TFT itself in each pixel is stored in C_{ST} , in addition to the data voltage V_{DATA} , as shown in Fig. 8. For this purpose, we need to extract the V_T of the current driver TFT in every pixel. Thus far, two methods have been developed to accomplish this. One method is to reduce the V_{GS} of the TFT by its own drain current until it turns off after initially applying a sufficiently large V_{GS} to turn on the TFT. In this method, here, V_T is extracted at the instant of TFT turn-off and stored in C_{ST} . The other method is to make the current with a specific value flow through the driver TFT. The V_{GS} of the driver TFT changes to make the drain current identical to the specific current value and is then stored in C_{ST} . The first method is called the voltage

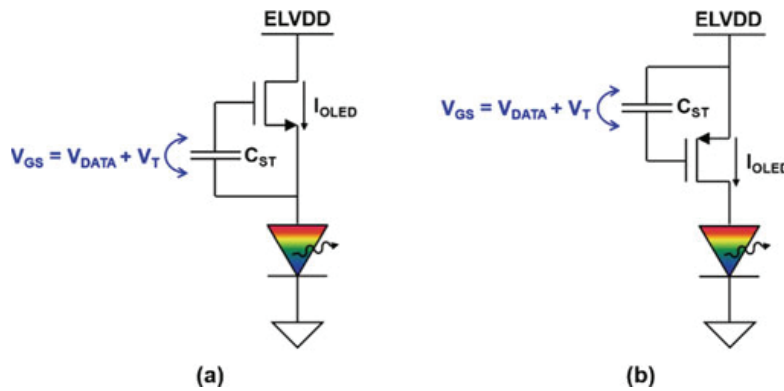


Fig. 8 Bias state of the current driver TFT during the light-emission period of OLED as a result of V_T compensation: **a** n-channel TFT case, **b** p-channel TFT case

programming scheme, since a data voltage is delivered to each pixel to express a certain grey level. In the second method, however, a data current is supplied to each pixel through the data line to set up an appropriate I_{OLED} in the driver TFT. This method is called the current programming scheme. Both methods can be carried out within each pixel circuit or by a system outside the display panel. In this subsection, the mechanisms for how it is performed in the pixel circuit are explained.

The first method mentioned above can be implemented in two ways. One is to change the gate voltage with the source voltage fixed and the other is to change the source voltage with the gate voltage fixed. In the former case, the drain and gate nodes of the TFT should be connected to each other—the so-called diode connection—for the drain current to charge or discharge the gate node. In the latter case, the source node is charged or discharged by the drain current and approaches the gate voltage until the TFT is turned off. Therefore, this is called the source-follower scheme.

2.1.1 Diode-Connection Scheme

The process of V_T compensation using the diode connection is shown in Fig. 9. Two switch TFTs, S1 and S2, are open to preserve the charge in C_{ST} during the light-emission period, as shown in Fig. 9a. A large V_{GS} , such as -7 V in Fig. 9b, is initially applied to the driver TFT to turn it on. This moment is called the reset or initialization period. The current of the driver TFT should not flow through the OLED during this period as such current flow precludes a high-quality expression of black. Then, S1 opens and S2 closes—diode connection—for the drain current to charge the gate node. The gate node is charged until the driver TFT is turned off—strictly speaking, it goes into the subthreshold regime rather than turn-off. At this instant, the drain current becomes negligibly small and the gate node voltage is almost saturated. The V_{GS} at this instant is simply regarded as the V_T of the driver TFT. In Fig. 9c, for example, the gate node voltage rises up to 9 V since the V_T is $-$

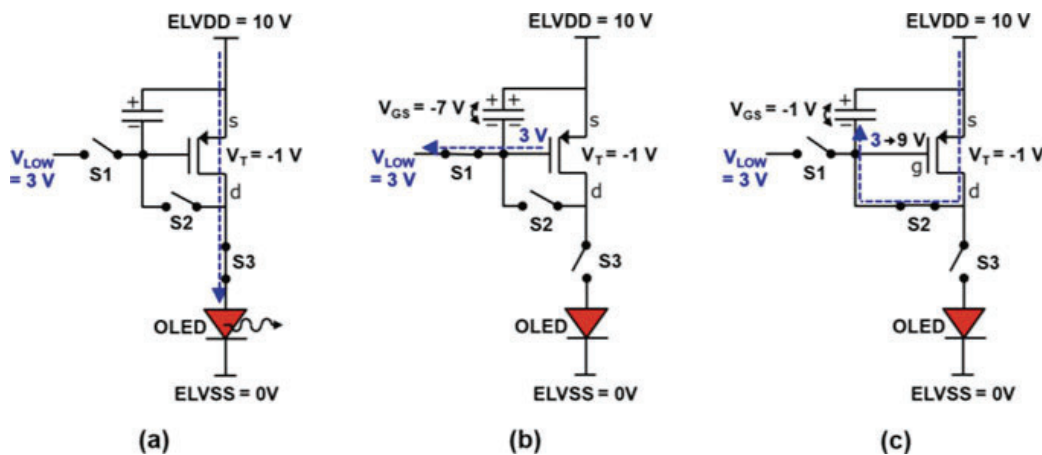


Fig. 9 The process of V_T compensation using the diode connection of driver TFT: **a** light-emission period, **b** reset or initialization period, **c** V_T extraction or compensation period

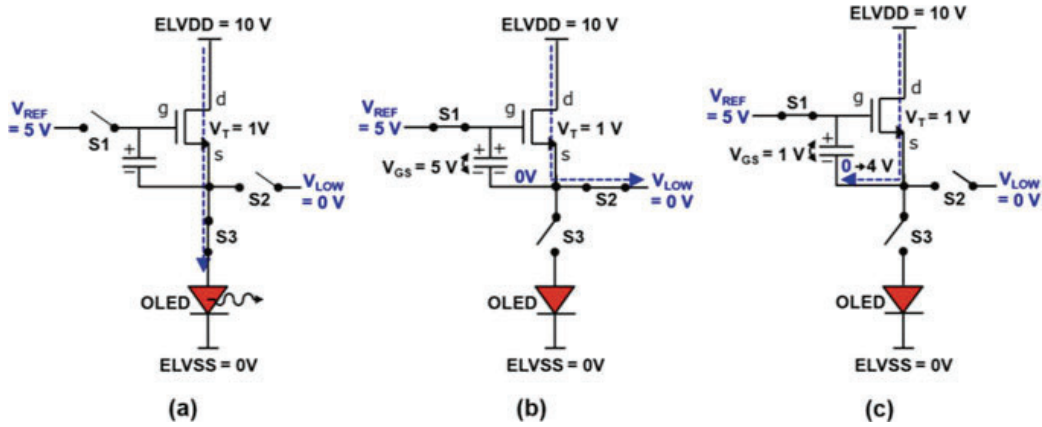


Fig. 10 The process of V_T compensation using the source-follower configuration: **a** light-emission period, **b** reset or initialization period, **c** V_T extraction or compensation period

1 V and ELVDD is 10 V. Finally, V_{DATA} is added to the extracted V_T in C_{ST} , which could happen in a variety of ways. Some examples are introduced in Sect. 3.

2.1.2 Source-Follower Scheme

The process of V_T compensation using the source-follower configuration is shown in Fig. 10. Two switch TFTs, S1 and S2, are open to preserve the charge in C_{ST} during the light-emission period as shown in Fig. 10a. A large V_{GS} , such as 5 V in Fig. 10b is applied to the driver TFT to turn it on during the initialization period. The current of the driver TFT should not flow through the OLED during this period as such current flow precludes a high-quality expression of black. Then, S2 opens with S1 still closed for the drain current to charge the source node. The source node voltage changes as it approaches the gate node voltage—source follower—until the driver TFT goes into the subthreshold regime. At this instant, the drain current becomes negligibly small and the source node voltage is almost saturated. The V_{GS} at this instant is simply regarded as the V_T of the driver TFT. In Fig. 10c, for example, the source node voltage rises up to 4 V since V_T is 1 V and the gate node voltage is 5 V. Finally, V_{DATA} is added to the extracted V_T in C_{ST} , which could happen in a variety of ways. Some examples are introduced in Sect. 3.

2.1.3 Current Programming Scheme

The process of current programming is shown in Fig. 11. During the light-emission period, the switch TFT S1 is open to preserve the charge in C_{ST} , as shown in Fig. 11a. S2 is also open while S3 is closed to make the drain current of the driver TFT the same as I_{OLED} . Before the next light-emission period, the data voltage in C_{ST} is refreshed, as shown in Fig. 11b. S1 and S2 are closed while S3 is open. The drain current of the

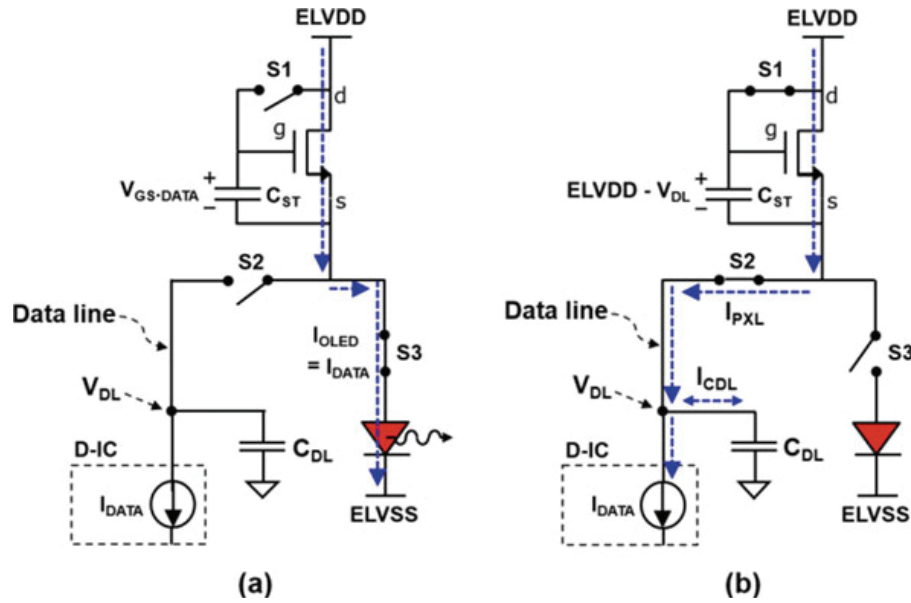


Fig. 11 Operation of current programming scheme: **a** light-emission period, **b** programming period

driver TFT, I_{PXL} , is determined by $ELVDD - V_{DL}$ alone because the driver TFT is in the saturation regime by diode connection, where V_{DL} is the voltage of the data line. The driver IC connected to the data line draws a data current, I_{DATA} . The difference between I_{PXL} and I_{DATA} is I_{CDL} , which charges or discharges the capacitance of the data line C_{DL} . When I_{PXL} is larger than I_{DATA} , C_{DL} is charged and V_{DL} rises to decrease I_{PXL} . When, on the contrary, I_{DATA} is larger than I_{PXL} , C_{DL} is discharged and V_{DL} falls to increase I_{PXL} . As a result, I_{PXL} eventually becomes the same as I_{DATA} . Then, $S1$ opens again and the voltage set up in C_{ST} — $V_{GS-DATA}$ is preserved. $S3$ is closed again as shown in Fig. 11a, and I_{OLED} becomes the same as I_{DATA} if the driver TFT operates in the saturation regime.

The current programming scheme, in principle, brings the best compensation results over a wide grey-scale range. I_{OLED} is exactly same as I_{DATA} regardless of the non-uniformity of V_T , μ_{FE} and S.S. if the drain current of the driver TFT is constant in the saturation regime. However, it is not used in the commercial product at all because it takes too long time for I_{PXL} to match I_{DATA} . It sometimes takes hundreds or thousands of times longer programming time than what is available in practical display driving. In addition, a driver IC which generates hundreds of uniform analog current outputs is very difficult to fabricate.

2.2 Ext-Panel Compensation

The characteristics of the current driver TFT and the OLED can be evaluated by a system outside the OLED display panel. For this, analog-to-digital converters (ADC) should be incorporated in the driver IC. The device parameters of the TFT and OLED

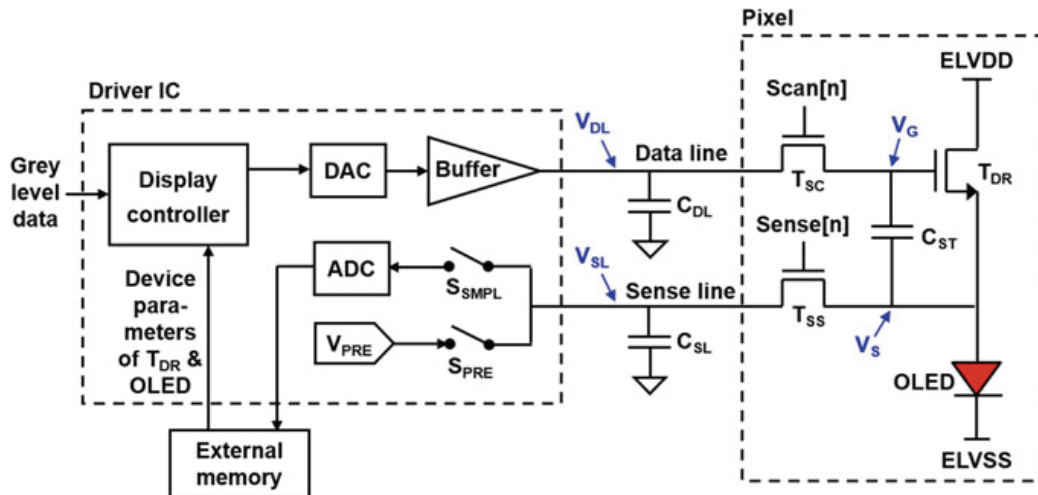


Fig. 12 Schematic diagram of an OLED display module for ext-panel compensation by measuring the voltage of the sense line

in every pixel are converted into digital data by the ADCs and saved in an external nonvolatile memory, as shown in Fig. 12. When the data voltage in each pixel is refreshed, the input grey-level data for each pixel are modified based on the device characteristics data stored in the memory to display an image without mura and then transferred to the digital-to-analog converters (DAC). The ext-panel compensation scheme is usually employed in large display products such as TVs due to its bulky form factor and the high cost of additional parts.

2.2.1 Voltage Sensing Scheme

The simplest pixel circuit for ext-panel compensation is composed of three n-channel TFTs and a capacitor, as shown in Fig. 12 [3]. This circuit is used in OLED TV products. Figure 13 shows the timing diagrams for the (a) V_T extraction and (b) μ_{FE} evaluation of T_{DR} . For V_T extraction, T_{DR} is initially turned on by a large V_{GS} . Then it becomes turned off as the sense line voltage, V_{SL} , rises by its own drain current while the data line voltage, V_{DL} , is kept constant with the scan switch TFT, T_{SC} turned on. V_{SL} is measured by ADC when it is almost saturated. The difference between V_{DL} and V_{SL} at this instant is regarded as the V_T of T_{DR} . Special care should be taken for V_{SL} not to exceed $ELVSS$ during this process, otherwise T_{DR} never turns off and some current will flow through T_{DR} and the OLED. As a result, we cannot obtain the correct V_T value. In addition, the pixels under evaluation do not display an appropriate image during this process and it takes a long time because the capacitance of the sense line, C_{SL} , is too large with respect to the drain current of T_{DR} approaching the threshold state. For this reason, this process cannot be carried out while the display is in use, but it is usually performed when the display becomes powered off.

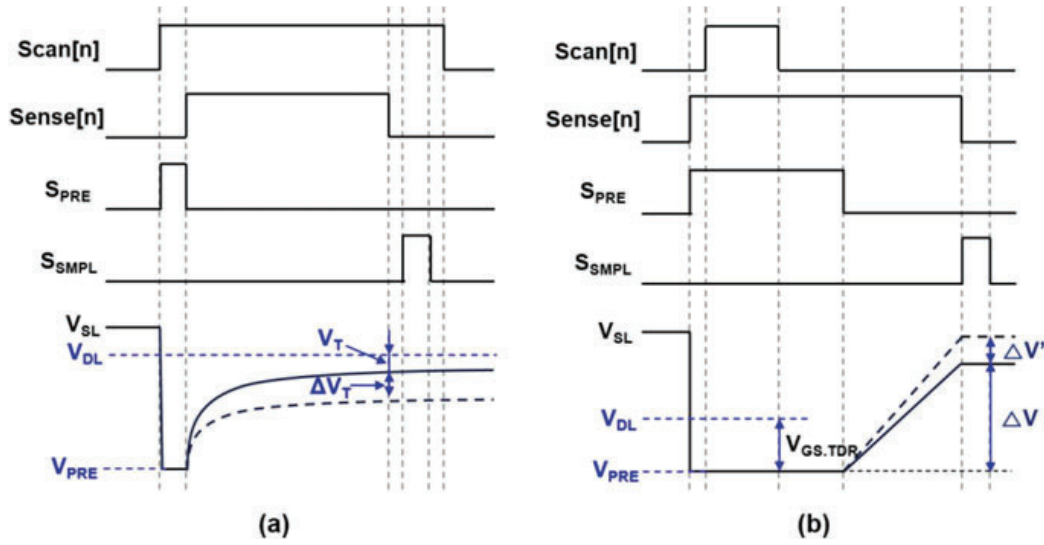


Fig. 13 Timing diagrams of an ext-panel compensation system employing a voltage sensing scheme for the **a** V_T extraction and **b** μ_{FE} evaluation of T_{DR}

For μ_{FE} evaluation, T_{DR} is initially turned on by a moderate V_{GS} , which is determined by the previously extracted V_T value. Then the T_{SC} in Fig. 12 is turned off. As a result, the V_{GS} of T_{DR} is kept constant by C_{ST} and a constant current flows through T_{DR} . C_{SL} begins to be charged by the constant current when the switch, S_{PRE} , opens. After a designated time, the sense switch TFT, T_{SS} turns off and V_{SL} is measured by ADC. The μ_{FE} of T_{DR} for a specific $V_{GS}-V_T$ bias is calculated from the measured V_{SL} . During this process, V_{SL} should not exceed ELVSS for correct evaluation results. The pixels under evaluation do not display an appropriate image either but this process does not take long because the constant drain current of T_{DR} is rather large. So, this process can be carried out while the display is in use and it is usually performed during a blank moment between each frame.

The degradation of L-I characteristics of OLED results in burn-in on a display, even if T_{DR} supplies the same current. The I-V characteristics of OLED are used to estimate the degradation of L-I characteristics and a larger current is supplied to the degraded OLED to hide the burn-in. For this purpose, the I-V characteristics of OLED are evaluated as follows. First, both T_{DR} and OLED are turned on by applying an appropriate V_G —corrected value based on the characteristics of T_{DR} . Then, V_S is determined depending on the I-V characteristics of the OLED. Next, T_{SC} is turned off to keep the V_{GS} of T_{DR} constant and V_{SL} is lowered sufficiently by V_{PRE} to prevent the OLED from turning on hereafter. Finally, S_{PRE} opens and V_{SL} begins to rise. The speed of the V_{SL} rise is determined by the V_{GS} of T_{DR} stored in C_{ST} , which is dependent on the I-V characteristics of the OLED.

3.1 7T-1C-6L PMOS Diode-Connection Pixel Circuit

The OLED pixel circuit in Fig. 15 is composed of seven p-channel TFTs, one capacitor and six lines—ELVDD, Em[n], Scan[n-1], Scan[n], Data and Init (7T-1C-6L). It was originally developed as a 6T-1C circuit [5]. The switch TFT T7 was added later for better black expression. It has nothing to do with the compensation effect. T1 is the current driver and T2–T7 are simple on/off switches. The V_{GS} of T1 is stored in C_{ST} and determines the I_{OLED} according to the grey-level data. Independent of the driver TFT T1, T5 and T6 can be used to block I_{OLED} under the control of the Em[n] signal. So, the Em[n] signal is used for the dimming control of the display panel.

The operation of data refresh with V_T compensation of T1 is carried out as follows. Initialization period 1 comes first with all the switch TFTs turned off, except T4, as shown in Fig. 16a. So, the gate voltage of the driver T1 is pulled down to V_{INIT} and T1 is initially turned on. Then, T4 is turned off. Next, a data voltage V_{DAT} is applied to the source of T1 and V_T extraction is performed as T2, T3 and T7 are turned on at the beginning of period 2, as shown in Fig. 16b. During period 2, the gate node voltage of T1 changes from V_{INIT} to $V_{DAT} + V_{TP}$, where V_{TP} is the V_T of T1. At the same time, the anode of the OLED is discharged through T7 to prevent charge accumulation in the intrinsic OLED capacitance, C_{OLED} , by a leakage current through T1. Otherwise, some light will be emitted even when black expression is wanted. Finally, the gate voltage of T1 is preserved by C_{ST} and the source of T1 is connected to ELVDD, as shown in Fig. 16c, during light-emission period 0. The V_T extraction time of this circuit is limited to one horizontal line selection time—1H time—since the nth data voltage should be maintained throughout V_T extraction period 2.

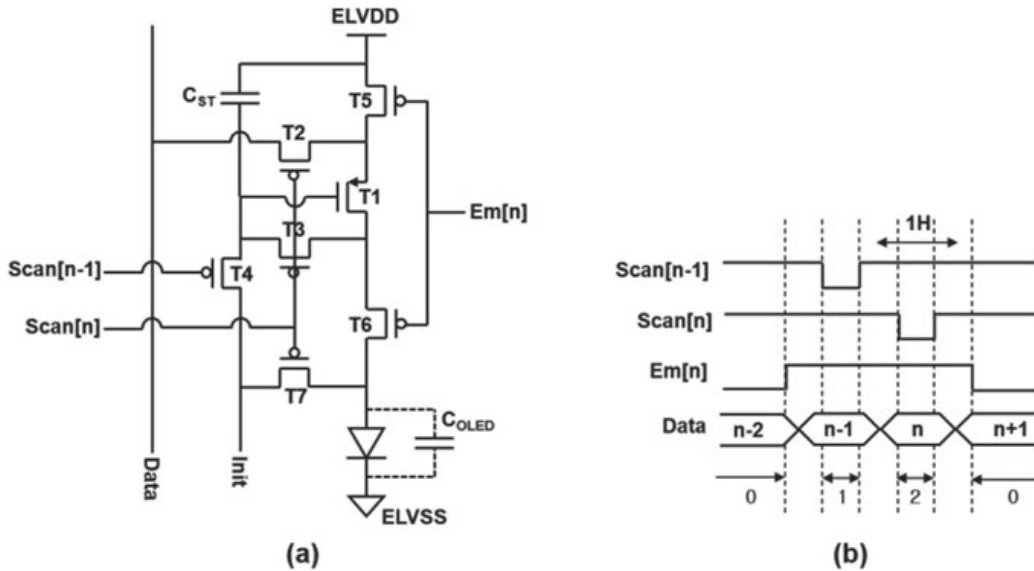


Fig. 15 **a** Circuit diagram and **b** timing diagram of the 7T-1C-6L PMOS diode-connection pixel circuit. 0: light-emission period, 1: initialization period, 2: data writing and V_T extraction period

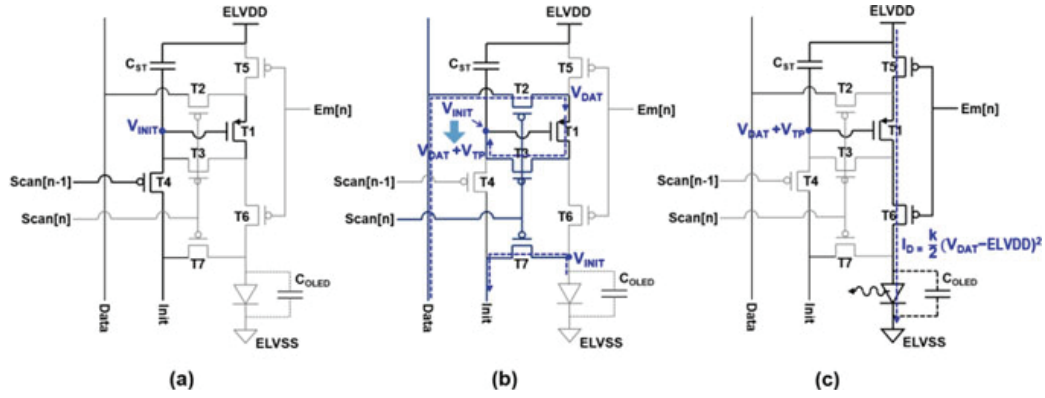


Fig. 16 Operation of the 7T-1C-6L PMOS diode-connection pixel circuit: **a** initialization, **b** data writing and V_T extraction, **c** light emission

3.2 4T-2C-6L NMOS Source-Follower Pixel Circuit

The OLED pixel circuit in Fig. 17 is composed of four n-channel TFTs, two capacitors and six lines—ELVDD, Em[n], Scan1[n], Scan2[n], Data and Init (4 T-2C-6L). T1 is the current driver and T2–T4 are simple on/off switches. The V_{GS} of T1 is stored in C_1 and determines I_{OLED} according to the grey-level data. Independent of the driver TFT T1, T4 can be used to block I_{OLED} under the control of the Em[n] signal. So, the Em[n] signal is used for the dimming control of the display panel.

The operation of V_T compensation and data refresh is carried out as follows. Initialization period 1 comes first with only switch TFTs T2 and T3 turned, as shown in Fig. 18a. A predefined voltage V_{REF} is applied through the data line during period 1 and 2. So, the V_{GS} of the driver T1 is set as $V_{REF} - V_{INIT}$ and T1 is initially turned on during period 1. Next, at the beginning of period 2, T2 is turned off and T4 is

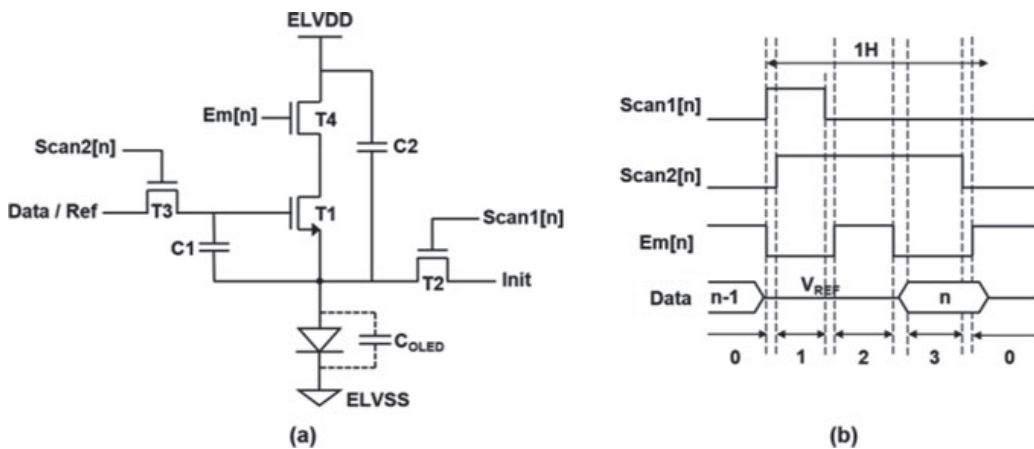


Fig. 17 **a** Circuit diagram and **b** timing diagram of the 4 T-2C-6L NMOS source-follower pixel circuit. 0: light-emission period, 1: initialization period, 2: V_T extraction period, 3: data writing period

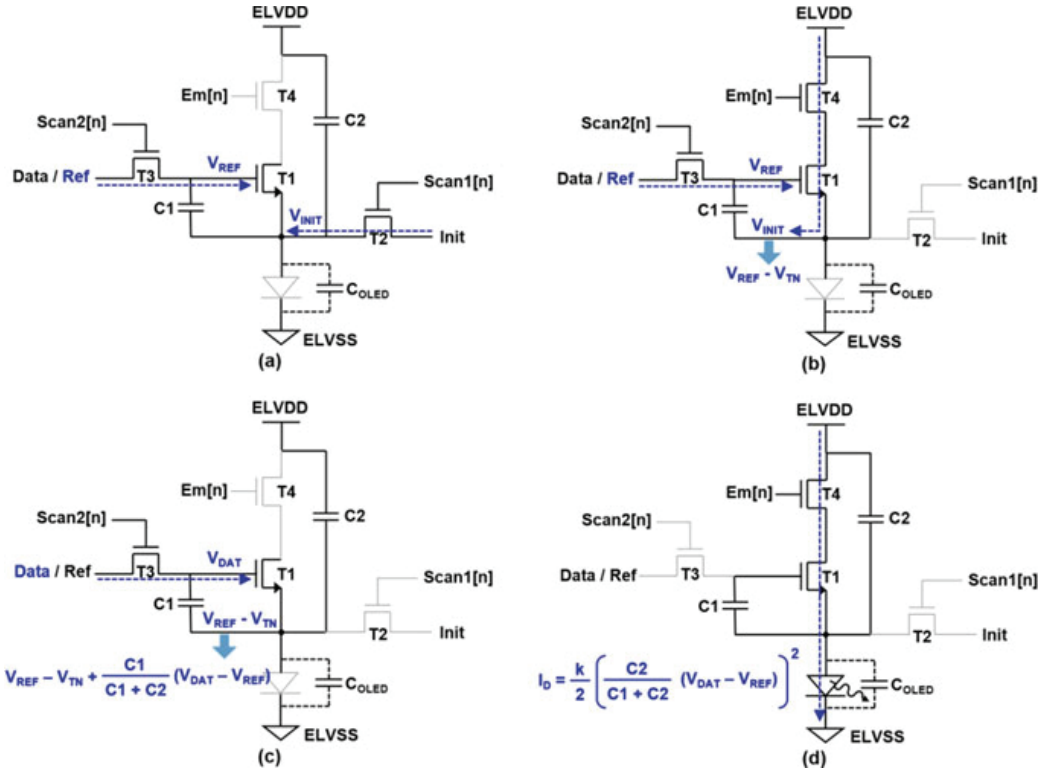


Fig. 18 Operation of the 4 T-2C-6L NMOS source-follower pixel circuit: **a** initialization, **b** V_T extraction, **c** data writing, **d** light emission

turned on to extract the V_T of T1, as shown in Fig. 18b. At the end of period 2, the gate voltage of T1 is V_{REF} and the source voltage of T1 becomes $V_{REF} - V_{TN}$, where V_{TN} is the V_T of T1. Then during period 3, T4 is turned off again and a data voltage V_{DAT} is applied to the gate of T1. As a result, the source node voltage of T1 changes as much as $(V_{DAT} - V_{REF}) C1/(C1 + C2)$ from $V_{REF} - V_{TN}$, as shown in Fig. 18c. Finally, T3 is turned off and the V_{GS} of T1 is maintained as $(V_{DAT} - V_{REF}) C2/(C1 + C2) + V_{TN}$ by $C1$ with the drain of T1 connected to ELVDD, as shown in Fig. 18d during light-emission period 0.

Special care should be taken for the source voltage of T1 not to exceed ELVSS during V_T extraction period 2, otherwise T1 will never be turned off and the V_T of T1 cannot be extracted. The anode of the OLED is discharged during the data refresh process, which is necessary for high-quality expression of black. The V_T extraction time of this circuit is limited to less than 1H time, since neither $(n - 1)$ th nor $(n + 1)$ th data voltage is allowed in the data line during periods 1–3.

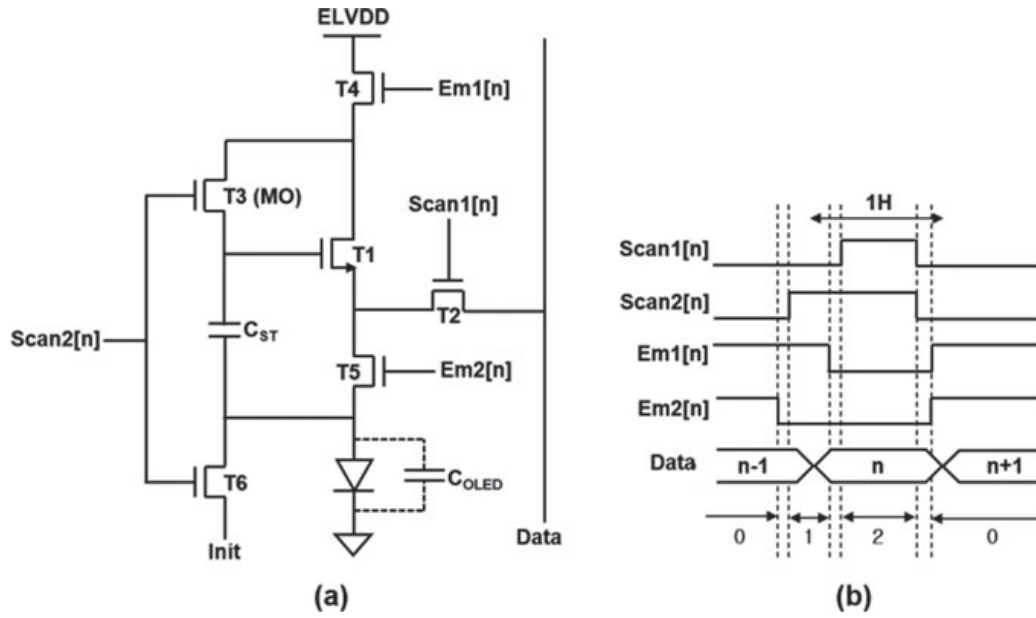


Fig. 19 **a** Circuit diagram and **b** timing diagram of the 6T-1C-7L LTPO diode-connection pixel circuit. 0: light-emission period, 1: initialization period, 2: data writing and V_T extraction period

3.3 6T-1C-7L LTPO Diode-Connection Pixel Circuit

The OLED pixel circuit in Fig. 19 is composed of six n-channel TFTs, one capacitor and seven lines—ELVDD, Em1[n], Em2[n], Scan1[n], Scan2[n], Data and Init (6T-1C-7L) [6, 7]. T1 is the current driver and T2–T6 are simple on/off switches. The V_{GS} of T1 is stored in C_{ST} and determines I_{OLED} according to the grey-level data. Independent of the driver TFT T1, T4 or T5 can be used to block I_{OLED} . So, they can be used for the dimming control of the display panel.

The voltage across C_{ST} is kept constant if T3 is completely turned off during light-emission period 0 in Fig. 20c. So, an IGZO TFT with extremely low off-state current, e.g. less than 10 fA, is used for T3 and the display is free from flicker problem even for very low frame rates such as 1 Hz. The combination of LTPS and MO TFTs, so-called LTPO, can be used to reduce the power consumption arising from data refresh by lowering the display frame rate [8].

The operation of data refresh with V_T compensation of T1 is carried out as follows. Initialization period 1 comes first as T5 is turned off but T3 and T6 are turned on, as shown in Fig. 20a. So, the gate voltage of the driver T1 is pulled up to ELVDD and T1 is initially turned on. At the same time, the anode of the OLED is discharged through T6 to discharge C_{OLED} for a high-quality expression of black. Then, T4 is turned off. Next, as T2 is turned on at the beginning of period 2, a data voltage, V_{DAT} , is applied to the source of T1 and V_T extraction is performed, as shown in Fig. 20b. During period 2, the gate node voltage of T1 changes from ELVDD to $V_{DAT} + V_{TN}$, where V_{TN} is the V_T of T1. At the end of period 2, T3 and T6 are turned off and $V_{DAT} + V_{TN} - V_{INIT}$ is stored in C_{ST} as the V_{GS} of T1. Finally, T4 and T5 are turned

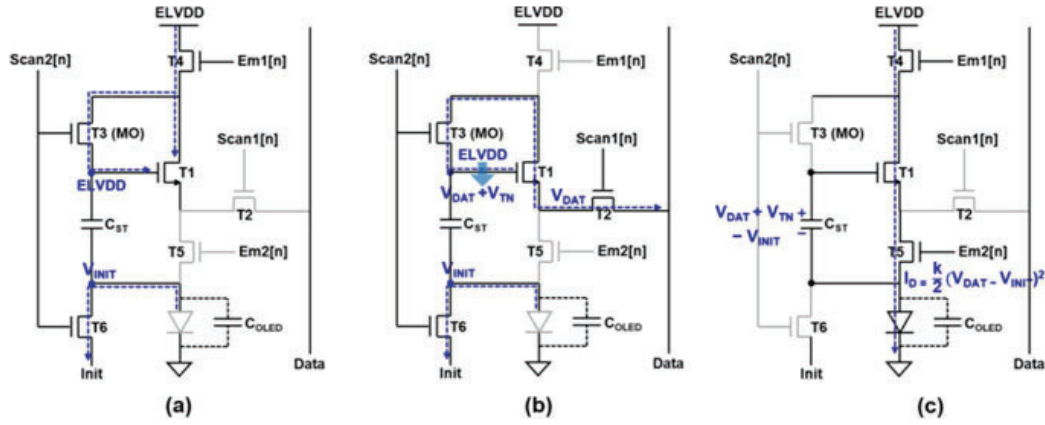


Fig. 20 Operation of the 6T-1C-7L LTPO diode-connection pixel circuit: **a** initialization, **b** data writing and V_T extraction, **c** light emission

on and a uniform I_{OLED} flows through T4, T1 and T5, as shown in Fig. 20c during light-emission period 0. The V_T extraction time of this circuit is limited to less than 1H time, since the n th data voltage should be maintained throughout V_T extraction period 2.

4 Limitations of In-Pixel Compensation Circuits

The pixel circuits of an OLED display do not eliminate mura, but only reduce it. For example, the LTPS TFT employed as the current driver in the mobile OLED display exhibits especially high short-range non-uniformity in the I-V characteristics, such as V_T , μ_{FE} and S.S. Therefore, the V_T compensation alone is not enough and some mura appears, even though the complicated pixel circuit is used.

4.1 Current Uniformity Versus V_T Extraction Time

The current driver TFT in the mobile OLED display operates mostly in the subthreshold regime since the current required in each pixel is below tens of nanoamperes. In principle, the pixel circuits introduced in the previous section do not compensate for the current non-uniformity of the driver TFT in the subthreshold regime if the S.S. is different among the TFTs. In addition, the extracted V_T value is in reality not a single value, but may change depending on the extraction time, as the subthreshold current flows continuously yet decreasingly during the V_T extraction period. Figure 21a shows how the current at the end of the V_T extraction period decreases with the extraction time, which means that the V_{GS} of the driver TFT does not saturate and that the extracted V_T is determined by the extraction time [9].

Figure 21 is the SPICE simulation results of I_D —the current of the driver TFT—in the 7T-1C-6L PMOS diode-connection pixel circuit of Fig. 15 versus the V_T extraction time, assuming 27 combinations of device parameter variations— $\Delta V_T = \pm 0.2$ V, $\Delta \mu_{FE} = \pm 20\%$, $\Delta S.S. = \pm 10\%$. Figure 21a shows the I_D values at the end of the V_T extraction period but Figs. 21b–d show the relative errors of I_D values for three current levels during the light-emission period. It should be noted that the relative standard deviation in Fig. 21a is very uniform—6–8%—though the absolute standard deviation σ certainly decreases as the V_T extraction time increases, meaning that the compensation effect is improved with longer V_T extraction time. The relative standard deviation of I_{OLED} decreases monotonically along with the V_T extraction time when the target I_{OLED} is small, as shown in Fig. 21b. However, it does not only

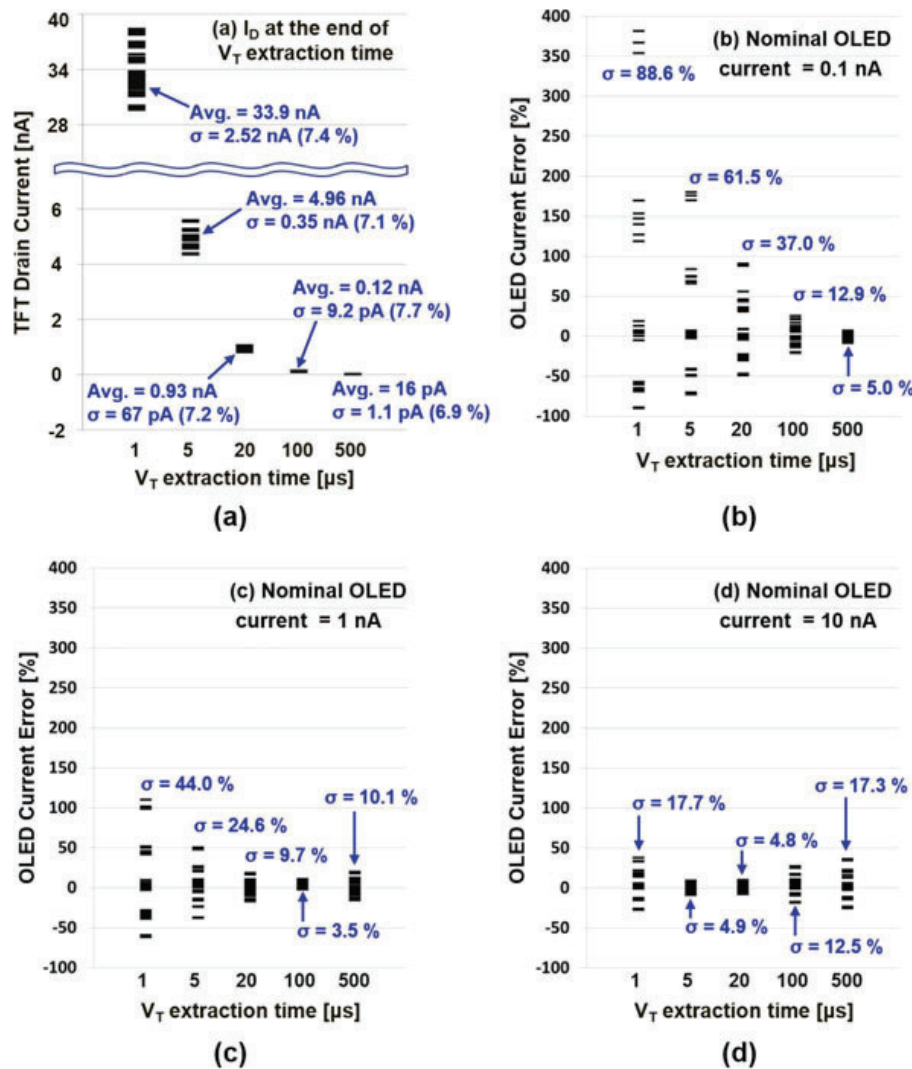


Fig. 21 Current deviations of the 7T-1C-6L PMOS diode-connection pixel circuit versus V_T extraction time for various TFT characteristics ($\Delta V_T = \pm 0.2$ V, $\Delta \mu_{FE} = \pm 20\%$, $\Delta S.S. = \pm 10\%$). **a** I_D values of driving TFTs at the end of the V_T extraction period. I_{OLED} values during the light-emission period for the target current of **a** 0.1, **b** 1 and **c** 10 nA

decrease but also increases along with the extraction time when the target I_{OLED} is large, as shown in Fig. 21c, d.

The reason why the relative error of I_{OLED} decreases with the extraction time is illustrated in Fig. 22. The I_{VT} s—the I_{DS} at the end of the V_T extraction time—of TFTs, T1 and T2, becomes similar, as shown in Fig. 21a. However, the I_{VT} is rather large for 1 μ s or 5 μ s—33.9 nA and 4.9 nA, respectively, in Fig. 21a—compared with the low grey-level I_{OLED} for mobile OLED displays—less than 1 nA. So, the V_{GS} for low grey-level is more positive than V_T , as shown in Fig. 22a. Therefore, I_{DS} at the low grey-level exhibits a large difference if the S.S.s of the TFTs are different. However, they become similar as the I_{VT} approaches the low grey-level current value with increasing V_T extraction time, as shown in Fig. 22b. On the other hand, the difference between the I_{DS} for the high grey-level may increase as the extraction

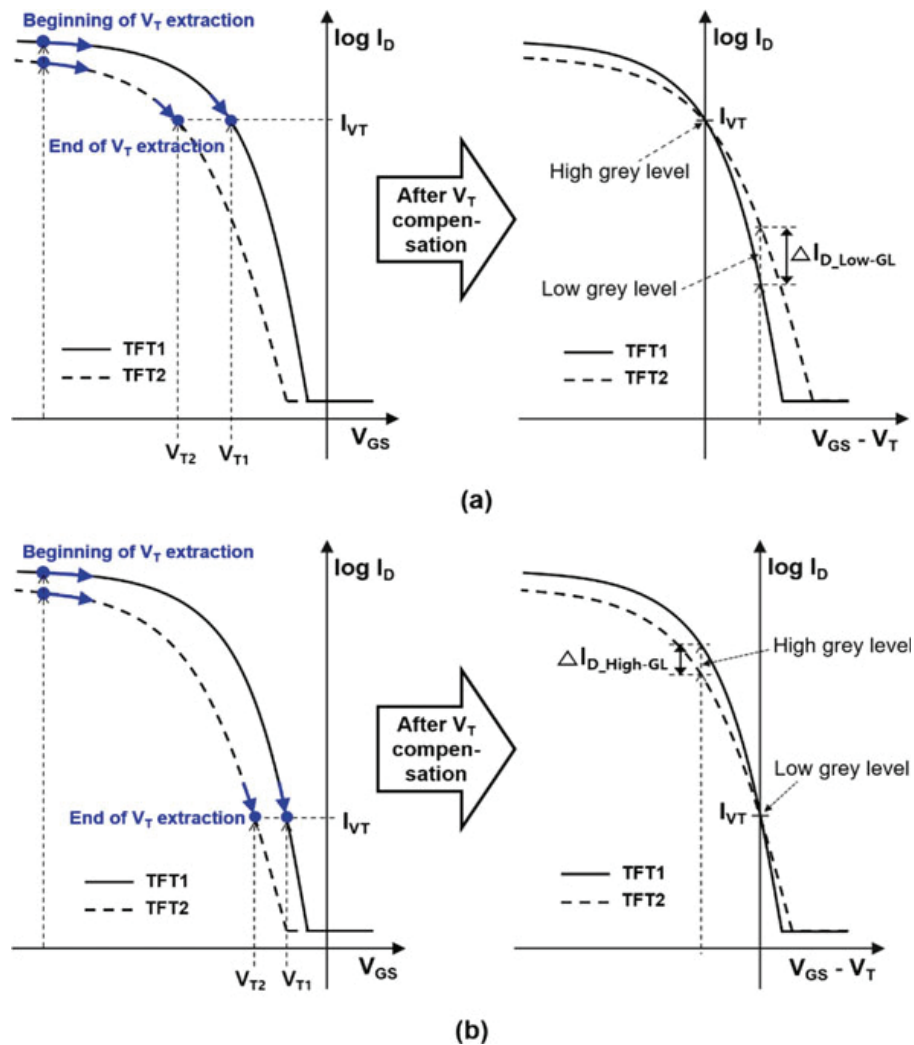


Fig. 22 Effects of different V_T extraction time on the current deviation after compensating for high and low grey levels. **a** short V_T extraction time, **b** long V_T extraction time

time increases too much, because the V_{GS} for the high grey-level once again differs from the extracted V_T value.

Figures 21c, d show that an optimum V_T extraction time exists to minimize the deviation of I_{OLED} and that it is different according to the target I_{OLED} value. The optimum time is such that it makes I_{VT} several times smaller than the target I_{OLED} value. This is because the absolute deviation among I_{VT} s decreases as the V_T extraction time increases, though the extracted V_T moves away from the V_{GS} of the driver TFT during the light-emission period.

4.2 Low Grey-Level Mura Versus Dimming Method

The grey scale of the OLED display is expressed by modulating I_{OLED} independently in each pixel. However, dimming of the panel can be controlled in two ways. The first option is to modulate the I_{OLED} in every pixel by a common rate over the entire panel. This method is referred to as pulse amplitude modulation (PAM). The other method is to modulate the light-emission time while keeping the I_{OLED} constant according to the grey-level data. This method is referred to as pulse width modulation (PWM). Figure 23 shows the high-speed photographs of the OLED displays driven by PAM or PWM dimming scheme. The photographs are taken with a shutter speed of 0.5 ms. Every pixel over the entire screen displays a certain grey level in PAM dimming, regardless of changes in brightness, as shown in Fig. 23a–c. On the contrary, four black horizontal bands are shown in PWM dimming and the width of the black bands decreases as brightness increases, as shown in Fig. 23d–f. These bands are not detected by the human eye because they move vertically very quickly, i.e. at the same speed as data refresh. The luminance of light-emitting regions is constant regardless of changes in brightness. PWM dimming is implemented by turning on and off the switch TFT in the path of I_{OLED} from ELVDD to the OLED in each pixel, rather than the current driver TFT.

PAM has an advantage over PWM in terms of OLED lifetime because the I_{OLED} range is shifted to lower levels for PAM dimming, whereas a constant I_{OLED} range is maintained for PWM dimming [10]. However, mura originating from non-uniform TFT characteristics is severer for PAM dimming than PWM dimming, as shown in Fig. 24. This is because the I_{OLED} range used for PAM at 10% brightness is ten times lower than for PWM at 10% brightness. The pixel circuit of the 7T-1C-6L PMOS diode-connection pixel circuit in Fig. 15 is used for both OLED displays and the V_T extraction time is approximately 5 μ s for both. Based on the results in Fig. 21, it is expected that a much longer V_T extraction time is required to compensate for the non-uniform characteristics of the driver TFT for such a low current level. The mura of the PAM dimming OLED display is reduced as the brightness increases to 50%, as shown in Fig. 24b. Accordingly, most OLED displays for mobile devices employ PWM dimming to suppress mura.

Recently, the vertical resolution of mobile OLED display is increasing to over 3 k and the frame rate is also on the rise from 60 to 120 Hz. These trends lead to shorter

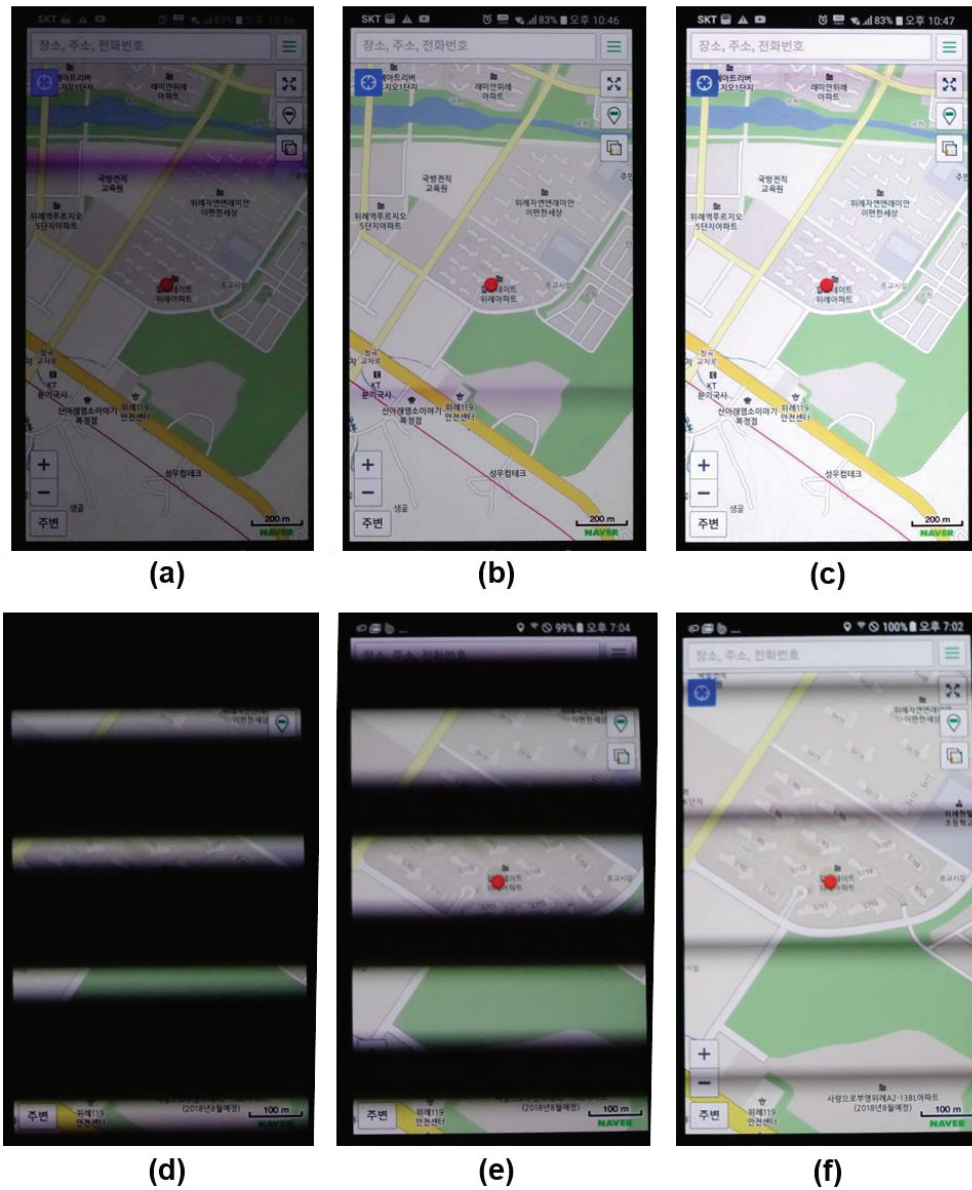


Fig. 23 High-speed photographs of OLED displays driven by the PAM or PWM dimming scheme. Shutter speed is 0.5 ms. **a** PAM 10% brightness, **b** PAM 50% brightness, **c** PAM 90% brightness, **d** PWM 10% brightness, **e** PWM 50% brightness, **f** PWM 90% brightness

V_T extraction time and higher power consumption. Adaptive frame rate driving, i.e. high frame rate for moving picture and low frame rate for still image, may be a good solution for suppressing the power consumption increase. However, a serious flicker problem occurs if the conventional LTPS backplane is used for the low frame rate display, e.g. below 10 Hz due to high off-state current. LTPO backplane can be used as a solution to the flicker problem of low frame rate driving owing to extremely low off-state current of the MO TFT. Accordingly, LTPO backplane with adaptive frame rate is expected to be widely used for the mobile OLED display [11]. The other

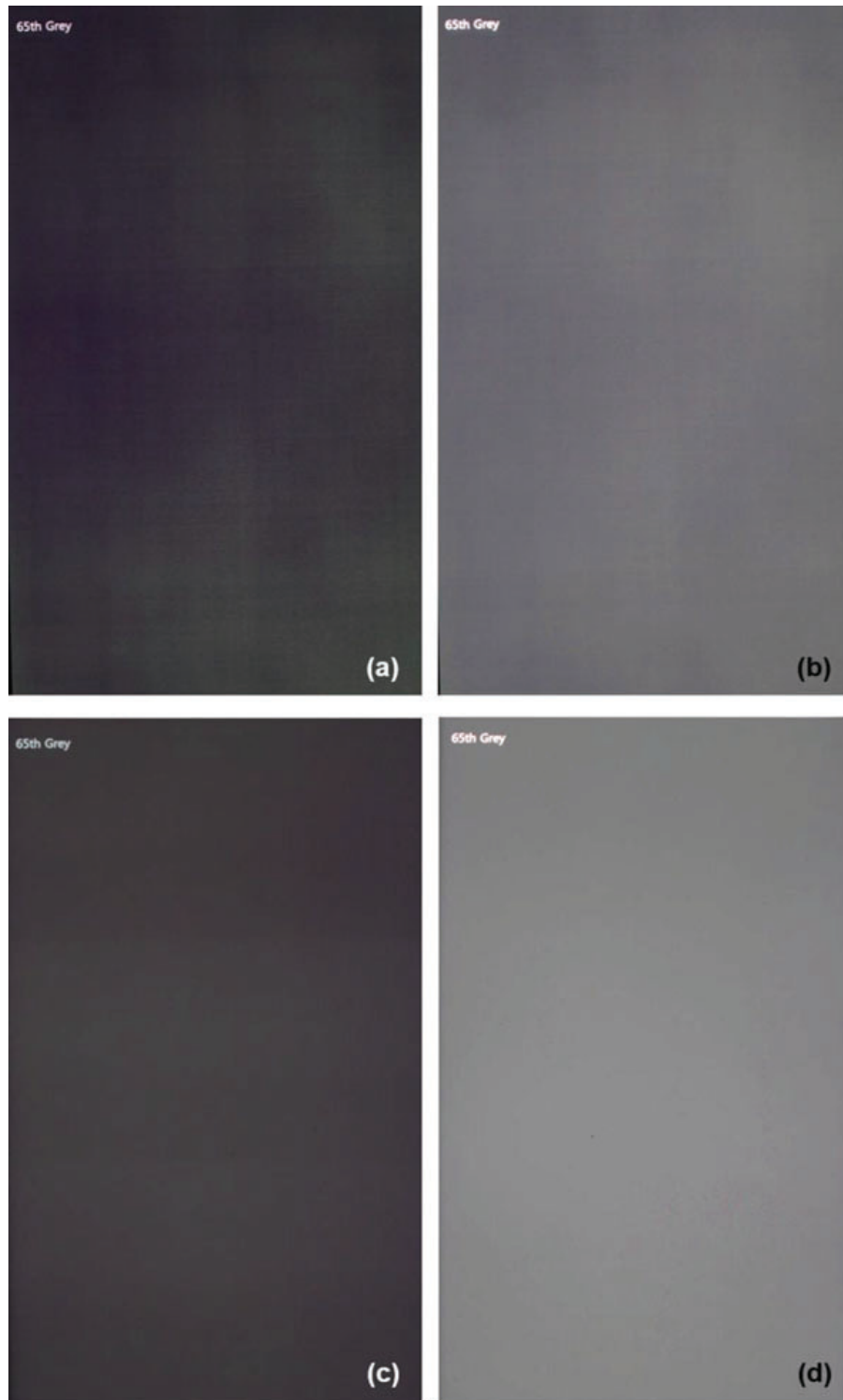


Fig. 24 Normal-speed photographs of OLED displays with a 7T-1C-6L PMOS diode-connection pixel circuit driven by a PAM or PWM dimming scheme. Shutter speed is 100 ms. Full-screen 65th grey level is displayed. **a** PAM at 10% brightness, **b** PAM at 50% brightness, **c** PWM at 10% brightness, **d** PWM at 50% brightness

problem, shorter V_T extraction time along with the improvement of OLED efficiency, makes the mura problem more and more serious because the difference between the current levels at the instant of V_T extraction and during the light emission increases. New pixel circuits with the V_T extraction time not limited to 1H time and extendable to hundreds of microseconds need to be developed [12]. The structure of the new OLED pixel circuit also needs to be as simple as the conventional circuit in order to be integrated within a small pixel area.

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