

A Novel LTPS TFT Pixel Circuit for Compensating IR Drop of Large Area AMOLED Display

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We have proposed a new AMOLED pixel design compensating IR drop besides threshold voltage (V_{th}) variation of LTPS TFTs without any additional signal. The SPICE simulation results show that the proposed pixel, which consists of 7 PMOS TFTs and 1 capacitor, successfully compensates not only V_{th} variation but also IR drop. V_{th} of the driving TFTs are detected and data voltage can be memorized when PMOS only inverter has high input voltage.

Introduction

Recently, active organic light emitting diode display (AMOLED) employing LTPS polycrystalline silicon (poly-Si) thin film transistor (TFT) have attracted a considerable attention due to high brightness, wide viewing angle and low power consumption (1, 2). Low temperature poly-Si TFTs employing excimer laser annealing (ELA) are widely used in AMOLED displays(2-4). However, the excimer laser annealed poly-Si TFTs suffer from a threshold voltage (V_{th}) variation in the pixel which causes non-uniform OLED current. Various compensation circuits have been reported(2-8). Most of the compensation circuit compensate V_{th} variation.

Furthermore, the voltage drop occurs in the metal lines (IR drop) because of the finite resistance of metal and the current for the pixel operation. As displays increase in size and resolution, the current flowing the metal line increases due to the increase of pixel number so that IR drop causes the non-uniform gray level in the large size panel. LTPS pixel which compensates V_{th} variation and IR drop are desirable.

The purpose of our work is to report p-type poly-Si pixel driving scheme in order to compensate not only V_{th} variation but also IR drop. There are few pixel structure, compensating IR drop using the sustain voltage (V_{SUS}) (7, 8). The current of the driving TFT is independent on the power voltage. However, in the previous work, the pixel structure consisted of CMOS⁷ or the V_{th} variation of OLED is not considered in the initializing step⁸. The proposed pixel circuit employs the seven PMOS TFTs and one capacitor and do not suffer from the OLED V_{th} variation. Our simulation results show that the proposed pixel circuit successfully compensate V_{th} variation and IR drop.

Proposed Pixel Circuit

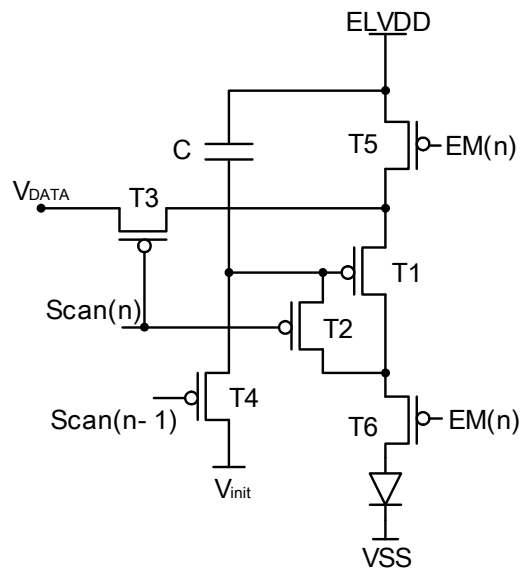
Figure 1 shows the pixel schematic and the timing diagram of the reported 6-TFT and 1-capacitor pixel circuit for progressive emission (6). When scan (n-1) is low, the gate voltage of the driving TFT (T1) is initialized as the initial voltage (V_{init}). When scan (n) is low, a data voltage (V_{DATA}) is memorized as $V_{DATA} - |V_{th}|$ at the gate of T1. Because the

drain current of T1 is the function of $(|V_{GS}| - |V_{th}|)$, V_{th} term can be cancelled in the emission time as below.

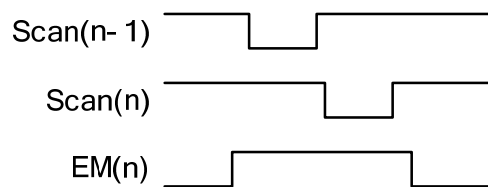
$$I_{DS} = \beta/2 * (|V_{GS}| - |V_{th}|)^2 = \beta/2 * \{ELVDD - (V_{DATA} - |V_{th}|) - |V_{th}|\}^2 = \beta/2 * (ELVDD - V_{DATA})^2 \quad [1]$$

From [1], however, it is found that IR drop problem is still remained. IR drop of the power line causes the long range non-uniformity. Even though the data voltage is memorized at the gate node of the driving pixel, ELVDD is decreased due to IR drop when the pixel is far from the input point of ELVDD. Therefore, OLED current is changed.

Figure 2 shows the proposed pixel scheme, the inverter consisting of p-type poly-Si TFTs. The diode-connected TFT2 is the load for the inverter operation. In this case, the output node cannot be pulled down completely. When the input is high, the output is higher than VSS as much as the V_{th} of TFT2 (V_{th_TFT2}). The V_{th} can be obtained in the PMOS only inverter. When in figure 1 TFT2 is considered as the driving TFT and V_{SS} is connected to the data line, the output node has $V_{DATA} + |V_{th_TFT2}|$. In this manner, V_{th} variation can be detected and V_{DATA} can be memorized at the same time.



(a)



(b)

Figure 1. (a) Pixel schematic and (b) the timing diagram of the reported 6-TFT and 1-capacitor pixel circuit

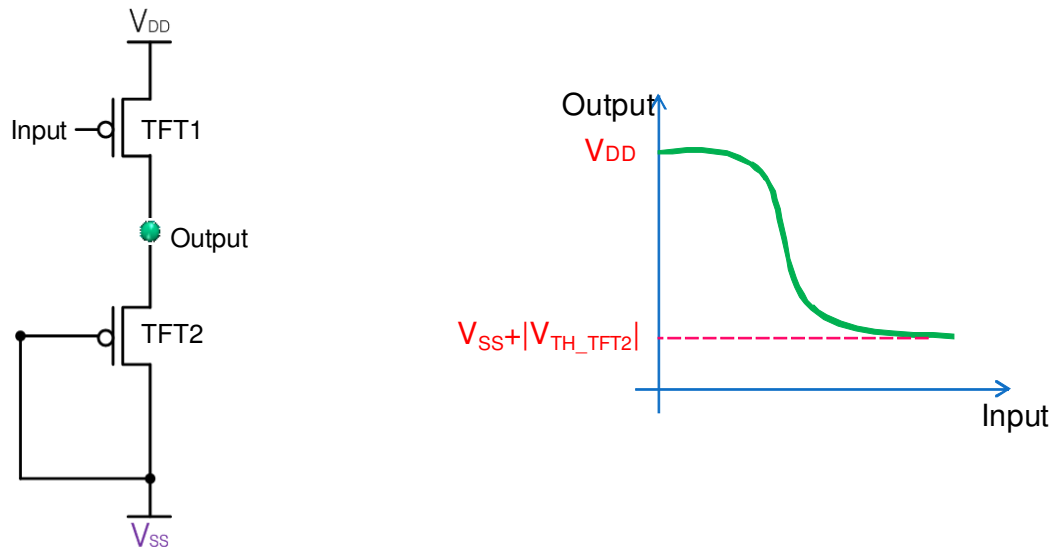
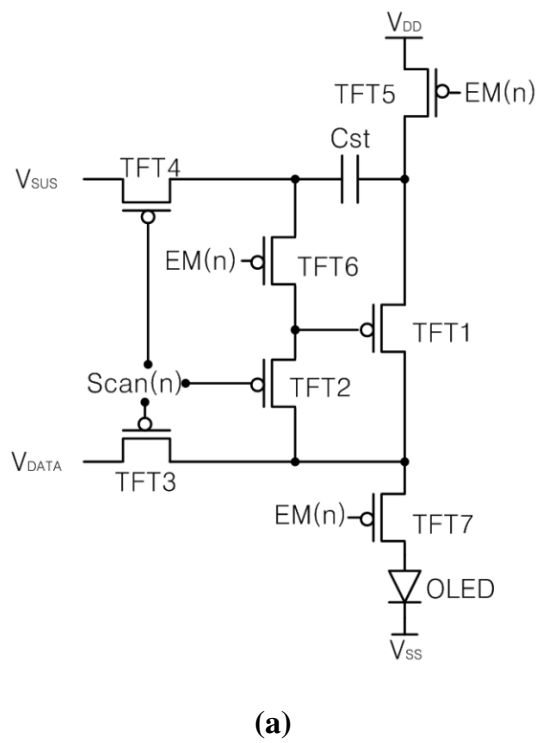
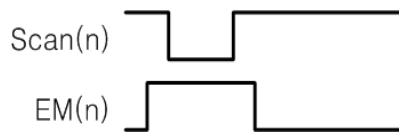


Figure 2. PMOS only inverter.

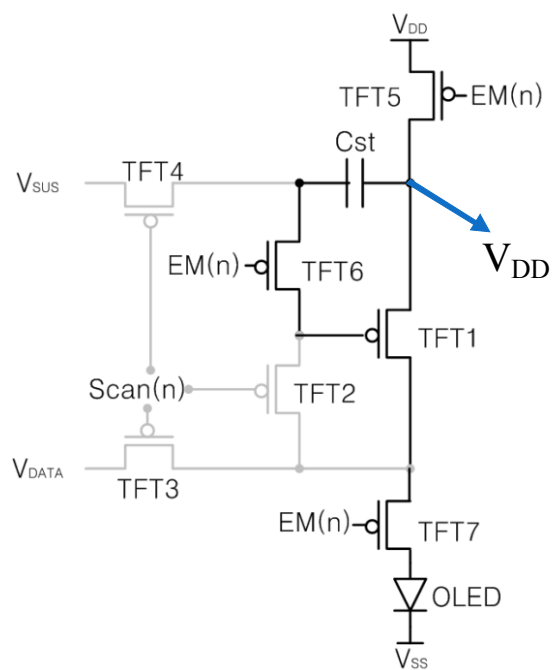
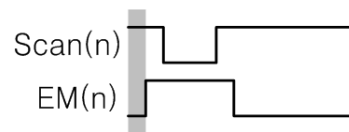


(a)

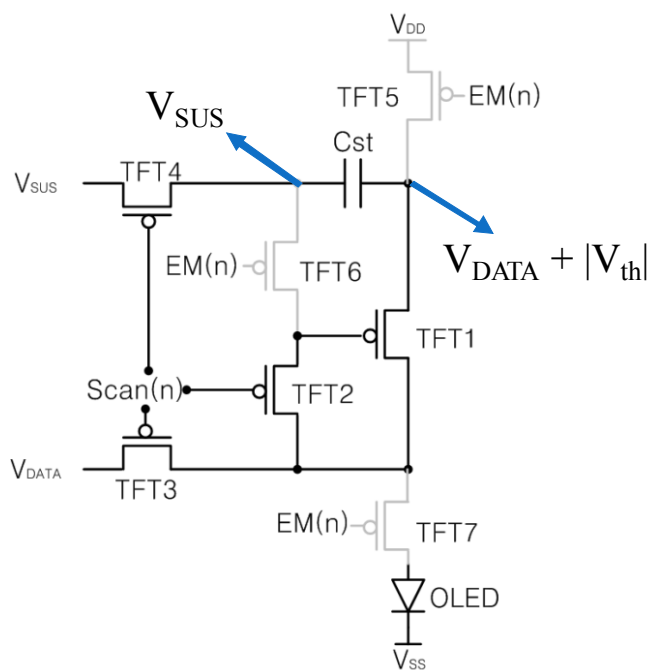
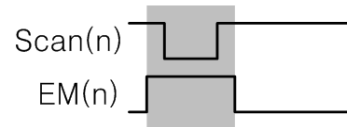


(b)

Figure 3. (a) Schematic and (b) timing diagrams of the proposed poly-Si TFT pixel driving circuit



(a)



(b)

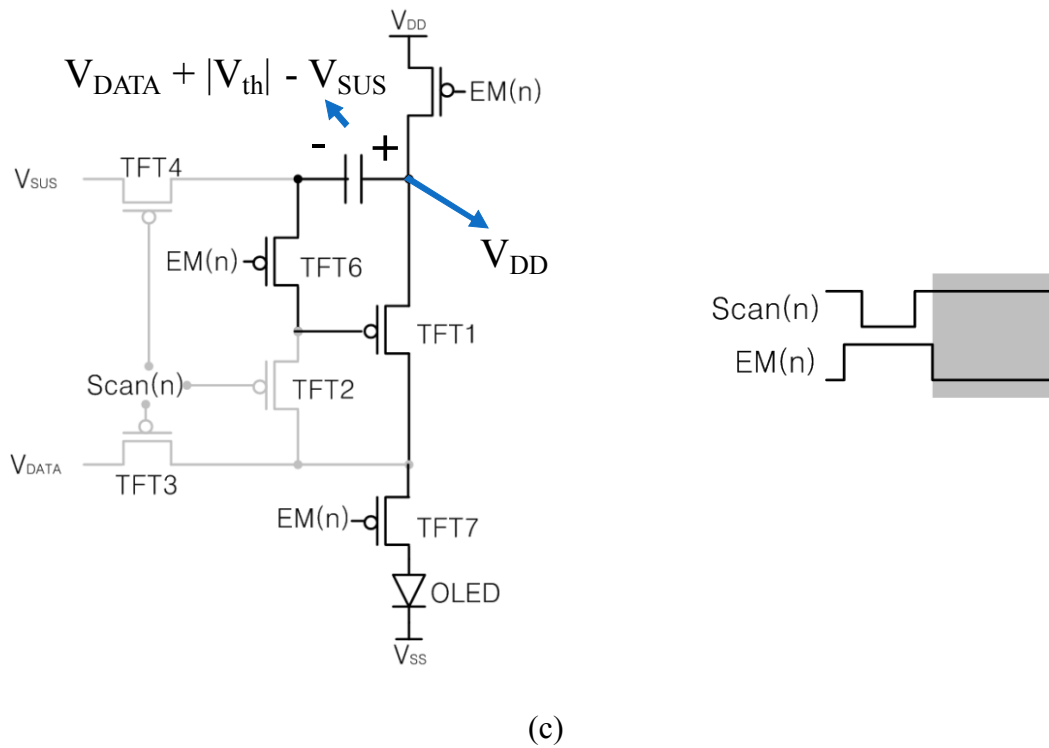


Figure 4. Compensation sequence of the proposed pixel circuit: (a) OLED emission, (b) V_{th} detection and data writing and (c) OLED emission.

Figure 3 shows the proposed pixel circuit and the timing diagram. The proposed pixel circuits consist of seven p-type poly-Si TFTs and one capacitor. The scanning and the emission signal is required. In the emission time, the source of the driving TFT (TFT1) has V_{DD} as shown in Figure 4 (a). When scan signal is low and emission signal is high, it decreases until $V_{DATA} + |V_{th_TFT2}|$ as shown in Figure 4 (b). In the conventional 6T1C circuit, the initializing step is required because the gate of T1 of Figure 1 (a) should have lower voltage than $V_{DATA} - |V_{th}|$ before the scanning. In the proposed pixel circuit, the source of the TFT1 should be higher than $V_{DATA} + |V_{th_TFT2}|$ before the scanning. However, Figure 4 (a) shows that it already has V_{DD} during the emission step. Therefore, the initialing step does not required in the proposed pixel circuit. Finally, $V_{DATA} + |V_{th_TFT2}| - V_{SUS}$ will be stored in the storage capacitor (C_{st}) during the scanning time. Because the stored voltage of C_{st} is $|V_{GS}|$ of the driving TFT, the current through the driving TFT is independent on the V_{th} and V_{DD} by following equation.

$$I_{DS} = \beta/2 * (|V_{GS}| - |V_{th}|)^2 = \beta/2 * \{ V_{DATA} + |V_{th}| - V_{SUS} - |V_{th}| \}^2 = \beta/2 * (V_{DATA} - V_{SUS})^2 \quad [2]$$

V_{SUS} does not act as a current source for OLED driving. It means that V_{SUS} does not suffer from IR drop. The proposed pixel can compensate not only V_{th} variation of LTPS TFTs, but also IR drop of power lines.

Simulation Result

To verify the proposed pixel circuit performance, we performed circuit simulation using smart SPICE. Figure 5 shows OLED current variation depending on V_{th} variation (-

$0.5 \text{ V} \leq \Delta V_{th} \leq -0.5 \text{ V}$) when OLED current of 50 nA, 100 nA and 200 nA is required at the circuit. Compared to 2T1C circuit, which does not compensate V_{th} variation, the proposed pixel circuit successfully compensates V_{th} variation of LTPS TFTs. From the simulation results, it is verified that the OLED current variation is less than 5 % when ΔV_{th} varied from -0.3 V to 0.3 V.

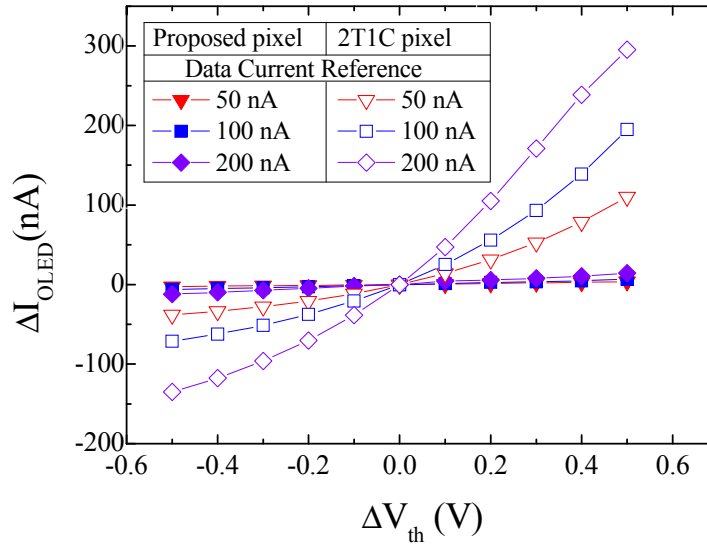


Figure 5. Simulation result: OLED current variation depending on V_{th} variation ($-0.5 \text{ V} \leq \Delta V_{th} \leq 0.5 \text{ V}$).

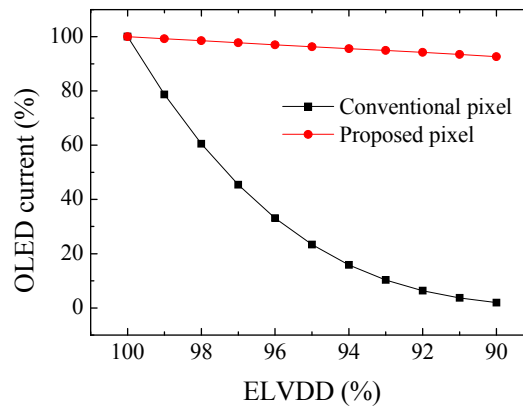


Figure 6. Simulation result: IR drop simulation

Figure 6 shows the result of IR drop simulation. OLED current of the proposed pixel circuit were compared with that of the conventional 6-TFT and 1-Capacitor pixel circuit according to V_{DD} . In conventional pixel circuit, the OLED current decreases to 2.0 % from the reference current (200 nA), when ELVDD voltage of the input point decreases to 90 %. However, the decrease of the OLED current is less than 8 % in the proposed pixel circuit in the same condition. From the results, the proposed pixel circuit shows the remarkably improved long-range uniformity.

Conclusion

We have proposed a new AMOLED pixel design compensating IR drop of the power lines. The simulation results showed that the proposed pixel structure, composed of 7-TFT and 1-capacitor, successfully compensate V_{th} variation of the excimer laser annealed poly-Si TFTs in the pixel and IR drop of the metal line.

Employing PMOS only inverter, V_{th} of the driving TFTs are detected and data voltage can be memorized. V_{GS} information of the driving TFT is programmed in the storage capacitor during the scanning period, so that OLED current is independent on the power voltage of each pixel and IR drop of the power line can be compensated.

SPICE simulation shows that V_{th} variation and IR drop is successfully compensated. OLED current variation was less than 5 % under $-0.5 \text{ V} \leq \Delta V_{th} \leq 0.5 \text{ V}$. Compared to widely used pixel circuit, the proposed pixel exhibited the improved long-range uniformity due to the IR drop compensation. It can be confirmed that the proposed pixel circuit might be suitable for the large area and high resolution AMOLED display.

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