

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.,
Patent Owner.

IPR2025-01478

U.S. Patent No. 11,574,990

**DECLARATION OF DR. JERZY KANICKI IN SUPPORT OF PETITION
FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,574,990**

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EXHIBIT LIST

No.	Exhibit
1001	U.S. Patent No. 11,574,990 (“’990 Patent” or “’990Pat.”)
1002	File History of the ’990 patent (“’990FH”)
1003	Declaration of Jerzy Kanicki, Ph.D.
1004	Curriculum Vitae of Jerzy Kanicki, Ph.D.
1005	U.S. Pat. Pub. No. 2012/0313100 (“Liu”)
1006	U.S. Pat. Pub. No. 2003/0089905 (“Udagawa”)
1007	Japanese Pat. Pub. No. 2003-167533 (“Nakayama”)
1008	U.S. Pat. Pub. No. 2008/0150846 (“Chung”)
1009	U.S. Pat. Pub. No. 2012/0001893 (“Jeong”)
1010	U.S. Pat. Pub. No. 2012/0199854 (“Noguchi-I”)
1011	Japanese Pat. Pub. No. 2008-008942 (“Murade”)
1012	U.S. Pat. Pub. No. 2012/0127220 (“Noguchi-II”)
1013	U.S. Pat. No. 7,626,199 (“Kim”)
1014	<i>Samsung Display Co. v. BOE Technology Group Co.</i> , No. 2:25-cv-00426-JRG (E.D. Tex.), Dkt. No. 1, Complaint
1015	Definition of “periphery”: The American Heritage Dictionary, 2d ed. (1991)
1016	Definition of “periphery”: Concise Oxford English Dictionary, 11th ed. (2009)

No.	Exhibit
1017	K.C. Park, <i>Pixel Circuits for OLED Displays</i> in <i>Advanced Display Technology</i> , Series in Display Science and Technology, I. B. Kang et al. (eds.), Springer Nature Singapore Pte Ltd. 2021 (“Park”)
1018	R. M. A. Dawson et al., <i>Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display</i> in 1998 SID Symp. Digest of Tech Papers, 1998 (“Dawson”)
1019	S. M. Choi et al., <i>A Self-Compensated Voltage Programming Pixel Structure for Active-Matrix Organic Light-Emitting Diodes</i> in Proceedings of International Display Workshops (IDW), pp. 535-538, 2003 (“Choi”)
1020	A. Bernanose, <i>Electroluminescence of Organic Compounds</i> in British Journal of Applied Physics 6, pp. S54-S56, 1955 (“Bernanose”)
1021	H. Kallmann et al., <i>Bulk Conductivity in Organic Crystals</i> in Nature 4718, pp. 31-33, 1960 (“Kallmann”)
1022	M. Pope, Autoionization in Anthracene in The Journal of Chemical Physics 47, 2197–2198, 1967 (“Pope”)
1023	M. Sano et al., Electroluminescence and Band Gap in Anthracene in The Journal of Chemical Physics 43, 2920–2921, 1965 (“Sano”)
1024	P.S. Vincett et al., <i>Electrical Conduction and Low Voltage Blue Electroluminescence in Vacuum-Deposited Organic Films</i> in Thin Solid Films 94, 171-183, 1982 (“Vincett”)
1025	C.W. Tang and S.A. VanSlyke, <i>Organic Electroluminescent Diodes</i> in Applied Physics Letters 51, 913-915, 1987 (“Tang”)
1026	J.H. Burroughes et al., <i>Light-Emitting Diodes Based on Conjugated Polymers</i> in Nature 347, 539-541, 1990 (“Burroughes”)

Dr. Jerzy Kanicki Declaration
Inter Partes Review of U.S. Patent 11,574,990

No.	Exhibit
1027	M.A. Baldo et al., <i>Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices</i> in Nature 395, 151-154, 1998 (“Baldo”)
1028	U.S. Pat. Pub. No. 2003/0129790 (“Yamazaki”)
1029	Min et al., <i>Electrical Characteristics of New LDD Poly-Si TFT Structure Tolerant to Process Misalignment</i> in IEEE Electron Device Letters, 20(7), 1999 (“Min”)
1030	Lee et al., <i>Asymmetric Electrical Properties of Fork a-Si:H Thin-Film Transistor and Its Application to Flat Panel Displays</i> in Journal of Applied Physics, 105, 2009 (“Lee-2009”)
1031	Kim et al., <i>40 Inch FHD AM-OLED Display with IR Drop Compensation Pixel Circuit</i> in 2009 SID Symp. Digest of Tech Papers, 2009 (“Kim-2009”)
1032	Lee et al., <i>A Novel LTPS TFT Pixel Circuit for Compensating IR Drop of Large Area AMOLED Display</i> in The Electrochemical Society (ECS) Transactions, 50(8), pp. 269-275, 2012 (“Lee-2012”)
1033	N. H. E. Weste et al., <i>CMOS VLSI Design: A Circuits and Systems Perspective</i> , Fourth Edition, Addison-Wesley, 2011 (“Weste”)
1034	U.S. Pat. Pub. No. 2003/0141811 (“Park ’811”)
1035	U.S. Pat. No. 9,461,102 (“Ono”)
1036	U.S. Pat. Pub. No. 2012/0211750 (“Kakinuma”)

LISTING OF CHALLENGED CLAIMS

11,574,990
Claim 1
1[pre] An organic light emitting diode display comprising:
1[a] a substrate;
1[b] a first voltage line;
1[c] a second voltage line;
1[d] a plurality of pixels, each of the pixels comprising an organic light emitting diode;
1[e] a plurality of driving circuits on the substrate, each of the organic light emitting diodes being electrically coupled to a respective driving circuit;
1[f] wherein each of the driving circuits comprises: a first thin film transistor coupled to a first scan line and a data line;
1[g] a second thin film transistor utilizing a semiconductor layer and electrically coupled to the first voltage line, the corresponding organic light emitting diode, and the first thin film transistor, the semiconductor layer being extended to and electrically coupled to the first thin film transistor;
1[h] an insulating layer covering the second thin film transistor;
1[ia] a storage capacitor electrically coupled to a gate electrode of the second thin film transistor, the storage capacitor comprising a first capacitor plate comprising a portion of the gate electrode of the second thin film transistor, a second capacitor plate over the first capacitor plate, and;
1[ib] a portion of the insulating layer between the first capacitor plate and the second capacitor plate, a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor being curved;

1[j] a third thin film transistor electrically coupled to the second thin film transistor, the corresponding organic light emitting diode, and the first capacitor plate, the semiconductor layer being extended to and electrically coupled to the third thin film transistor;

1[k] a fourth thin film transistor electrically coupled to the first voltage line and the second thin film transistor, the semiconductor layer being extended to and is electrically coupled to the fourth thin film transistor;

1[l] a fifth thin film transistor electrically coupled to the second thin film transistor, the third thin film transistor, and the corresponding organic light emitting diode, the semiconductor layer being extended to and is electrically coupled to the fifth thin film transistor; and

1[m] a sixth thin film transistor electrically coupled to the second voltage line, the third thin film transistor, and the first capacitor plate, the semiconductor layer being extended to and is electrically coupled to the sixth thin film transistor.

Claim 2

2. The organic light emitting diode display according to claim 1, wherein gate electrodes of the fourth and fifth thin film transistors are coupled together.

Claim 3

3. The organic light emitting diode display according to claim 2, wherein the gate electrodes of the fourth and fifth thin film transistors are configured to receive a signal from a light emission control line.

Claim 4

4. The organic light emitting diode display according to claim 1, wherein a gate electrode of the sixth thin film transistor is configured to receive a signal from a second scan line.

Claim 5

5. The organic light emitting diode display according to claim 1, wherein gate electrodes of the first and third thin film transistors are coupled together.

Claim 6
6. The organic light emitting diode display according to claim 5, wherein the gate electrodes of the first and third thin film transistors are configured to receive a signal from the first scan line.
Claim 7
7. The organic light emitting diode display according to claim 1, wherein the second capacitor plate is electrically coupled to the first voltage line.
Claim 8
8. The organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.
Claim 9
9. The organic light emitting diode display according to claim 1, wherein portions of the semiconductor layer are doped with N-type impurities.
Claim 10
10. The organic light emitting diode display according to claim 1, wherein portions of the semiconductor layer are doped with P-type impurities.
Claim 11
11. The organic light emitting diode display according to claim 1, further comprising a seventh thin film transistor electrically coupled to the second voltage line, the fifth thin film transistor, and the corresponding organic light emitting diode.
Claim 12
12. The organic light emitting diode display according to claim 11, wherein the semiconductor layer is extended to and is electrically coupled to the seventh thin film transistor.

Claim 13
13. The organic light emitting diode display according to claim 12, wherein a gate electrode of the seventh thin film transistor is configured to receive a signal from a bypass control line.
Claim 14
14. The organic light emitting diode display according to claim 11, wherein gate electrodes of the fourth and fifth thin film transistors are coupled together.
Claim 15
15. The organic light emitting diode display according to claim 14, wherein the gate electrodes of the fourth and fifth thin film transistors are configured to receive a signal from a light emission control line.
Claim 16
16. The organic light emitting diode display according to claim 11, wherein a gate electrode of the sixth thin film transistor is configured to receive a signal from a second scan line.
Claim 17
17. The organic light emitting diode display according to claim 11, wherein gate electrodes of the first and third thin film transistors are coupled together.
Claim 18
18. The organic light emitting diode display according to claim 17, wherein the gate electrodes of the first and third thin film transistors are configured to receive a signal from the first scan line.
Claim 19
19. The organic light emitting diode display according to claim 11, wherein the second capacitor plate is electrically coupled to the first voltage line.

Claim 20
20. The organic light emitting diode display according to claim 11, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.
Claim 21
21. The organic light emitting diode display according to claim 11, wherein portions of the semiconductor layer are doped with N-type impurities.
Claim 22
22. The organic light emitting diode display according to claim 11, wherein portions of the semiconductor layer are doped with P-type impurities.
Claim 23
23. The organic light emitting diode display according to claim 1, wherein the third thin film transistor is electrically coupled to the gate electrode and a drain electrode of the second thin film transistor.
Claim 24
24. The organic light emitting diode display according to claim 1, further comprising a protective layer covering the plurality of driving circuits, wherein each of the organic light emitting diodes further comprises a pixel electrode on the protective layer, the pixel electrode being electrically coupled to the second thin film transistor through a contact hole.
Claim 25
25. The organic light emitting diode display according to claim 1, further comprising a protective layer covering the plurality of driving circuits, wherein each of the organic light emitting diodes further comprises a pixel electrode on the protective layer, the pixel electrode being electrically coupled to a drain electrode of the fifth thin film transistor through a contact hole.

Claim 26
26. The organic light emitting diode display according to claim 1, wherein the first capacitor plate and the first scan line are in the same material layer.
Claim 27
27. The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “S”-shape.
Claim 28
28. The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a partial “S”-shape.
Claim 29
29. The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “M”-shape.
Claim 30
30. The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “W”-shape.

I Jerzy Kanicki, do hereby declare as follows:

I. INTRODUCTION

1. My name is Jerzy Kanicki, and I have been retained by counsel for Petitioner (“Petitioner” or “BOE”) as an expert witness to provide my opinion regarding certain prior art references and U.S. Patent No. 11,574,990 (the “’990 patent”).

2. I make this declaration based upon my own personal knowledge and, if called upon to testify, will testify competently to the matters stated herein.

3. I have been asked to provide my expert opinion in connection with the *Inter Partes* Review of the ’990 Patent to Kim *et al.* concerning whether it is unpatentable over certain prior art. This declaration is a statement of my opinions on issues relating to the patentability of claims 1-30 (the “Challenged Claims”) of the ’990 Patent. As I explain more fully below, it is my opinion that all of the Challenged Claims would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention.

4. I am being compensated for my work in this matter at my standard hourly rate. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

5. I have reviewed and considered the following documents in connection with my analysis of the '990 Patent:

- EX1001: U.S. Patent No. 11,574,990 (“’990 Patent” or “’990Pat.”)
- EX1002: File History of the ’990 Patent (“’990FH”)
- EX1005: U.S. Pat. Pub. No. 2012/0313100 (“Liu”)
- EX1006: U.S. Pat. Pub. No. 2003/0089905 (“Udagawa”)
- EX1007: Japanese Pat. Pub. No. 2003-167533 (“Nakayama”)
- EX1008: U.S. Pat. Pub. No. 2008/0150846 (“Chung”)
- EX1009: U.S. Pat. Pub. No. 2012/0001893 (“Jeong”)
- EX1010: U.S. Pat. Pub. No. 2012/0199854 (“Noguchi-I”)
- EX1011: Japanese Pat. Pub. No. 2008-008942 (“Murade”)
- EX1012: U.S. Pat. Pub. No. 2012/0127220 (Noguchi-II”)
- EX1013: U.S. Pat. No. 7,626,199 (“Kim”)
- EX1015: Definition of “periphery”: The American Heritage Dictionary, 2d ed. (1991)
- EX1016: Definition of “periphery”: Concise Oxford English Dictionary, 11th ed. (2009)
- EX1017: K.C. Park, Pixel Circuits for OLED Displays in Advanced Display Technology, Series in Display Science and Technology, I. B.

Kang et al. (eds.), Springer Nature Singapore Pte Ltd. 2021 (“Park”)

- EX1018: R. M. A. Dawson et al., Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display in 1998 SID Symp. Digest of Tech Papers, 1998 (“Dawson”)
- EX1019: S. M. Choi et al., A Self-Compensated Voltage Programming Pixel Structure for Active-Matrix Organic Light-Emitting Diodes in Proceedings of International Display Workshops (IDW), pp. 535-538, 2003 (“Choi”)
- EX1020: A. Bernanose, Electroluminescence of Organic Compounds in British Journal of Applied Physics 6, pp. S54-S56, 1955 (“Bernanose”)
- EX1021: H. Kallmann et al., Bulk Conductivity in Organic Crystals in Nature 4718, pp. 31-33, 1960 (“Kallmann”)
- EX1022: M. Pope, Autoionization in Anthracene in The Journal of Chemical Physics 47, 2197–2198, 1967 (“Pope”)
- EX1023: M. Sano et al., Electroluminescence and Band Gap in Anthracene in The Journal of Chemical Physics 43, 2920–2921, 1965 (“Sano”)
- EX1024: P.S. Vincett et al., Electrical Conduction and Low Voltage

Blue Electroluminescence in Vacuum-Deposited Organic Films in Thin Solid Films 94, 171-183, 1982 (“Vincett”)

- EX1025: C.W. Tang and S.A. VanSlyke, Organic Electroluminescent Diodes in Applied Physics Letters 51, 913-915, 1987 (“Tang”)
- EX1026: J.H. Burroughes et al., Light-Emitting Diodes Based on Conjugated Polymers in Nature 347, 539-541, 1990 (“Burroughes”)
- EX1027: M.A. Baldo et al., Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices in Nature 395, 151-154, 1998 (“Baldo”)
- EX1028: U.S. Pat. Pub. No. 2003/0129790 (“Yamazaki”)
- EX1029: Min et al., Electrical Characteristics of New LDD Poly-Si TFT Structure Tolerant to Process Misalignment in IEEE Electron Device Letters, 20(7), 1999 (“Min”)
- EX1030: Lee et al., Asymmetric Electrical Properties of Fork a-Si:H Thin-Film Transistor and Its Application to Flat Panel Displays in Journal of Applied Physics, 105, 2009 (“Lee-2009”)
- EX1031: Kim et al., 40 Inch FHD AM-OLED Display with IR Drop Compensation Pixel Circuit in 2009 SID Symp. Digest of Tech Papers, 2009 (“Kim-2009”)

- EX1032: Lee et al., A Novel LTPS TFT Pixel Circuit for Compensating IR Drop of Large Area AMOLED Display in The Electrochemical Society (ECS) Transactions, 50(8), pp. 269-275, 2012 (“Lee-2012”)
 - EX1033: N. H. E. Weste et al., CMOS VLSI Design: A Circuits and Systems Perspective, Fourth Edition, Addison-Wesley, 2011 (“Weste”)
 - EX1034: U.S. Pat. Pub. No. 2003/0141811 (“Park ’811”)
 - EX1035: U.S. Pat. No. 9,461,102 (“Ono”)
 - EX1036: U.S. Pat. Pub. No. 2012/0211750 (“Kakinuma”)
6. In forming the opinions expressed below, I have considered:
- the documents listed above;
 - the relevant legal standards as explained to me by the Petitioner’s counsel, including the standard for obviousness, and any additional authoritative documents as cited in the body of this declaration;
 - my own knowledge and experience based upon my work in the field of flat panel display as described below; and
 - any other documents not listed above but cited below.

7. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further, I may also consider additional documents and information in forming any necessary

opinions, including documents that may not yet have been provided to me.

8. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

9. Unless otherwise noted, all emphasis in any quoted material has been added.

II. QUALIFICATIONS AND PROFESSIONAL EXPERIENCE

10. I have studied, taught, and practiced in the field of flat panel displays (FPDs) and integrated circuits (ICs) fabrication for over 25 years, including design, thin film depositions, processing, fabrication, and photolithography of devices and circuits used in both applications. The flat panel displays include, for example, active-matrix liquid crystal displays, (AM-LCDs), active-matrix organic light emitting displays (AM-OLEDs) and other light transmissive, reflective and emitting display technologies. I received my Doctorate of Science (D.Sc.) from the Free University of Brussels, Belgium in 1982. My educational background also includes a B.S. (1976) and M.S. (1978) in Chemistry from the Free University of Brussels, Belgium.

11. From 1983 to 1995, I was a Research Staff Member at the IBM T.J.

Watson Research Center in Yorktown Heights, New York, involved in the research and development of flat panel display materials, devices, circuits, driving electronics, and manufacturing methods. During that period, I was a member of a team that developed the first IBM active-matrix liquid-crystal displays (AM-LCDs) manufacturing technology, leading to the introduction of the first color laptop computer (CL57-SX) on March 24, 1992. I, among others, was also responsible at IBM for the initial fundamental understanding of device physics and pixel design approaches used for, and manufacturing methods of, certain AM-LCDs for IBM's ThinkPad laptop computers.

12. Since 1995, I have been a member of the faculty at the University of Michigan College of Engineering, Ann Arbor, Michigan. During that period, I have held the position of Professor in the Department of Electrical Engineering and Computer Science (EECS). Between 1995 and 1999, I was group team leader within the University of Michigan Center of Display Technology and Manufacturing. For number of years, I also held the position of Professor in the Program of Macromolecular Science and Engineering (2000-2011) and Applied Physics. During my tenure at the University of Michigan, I have conducted leading work on various flat panel displays, device and circuit fabrication technologies, including, for example, design for various devices and integrated circuits to be used with flat-panel

displays (active-matrix arrays, data and gate drivers chips, and associated electronics), x-ray and optical imagers (pixel circuits, driving and readout chips, and associated electronics), chemical sensors (readout chips), solar cells (DC/AC converters), and fingerprint sensors (driving circuits and readout chips). As a faculty member, over the years I have graduated a number of PhD dissertations in the field of flat panel displays, semiconductor devices and circuits. Upon graduation, my PhD graduate students have moved either into industrial positions in the displays and electronics industries or into academic positions in the U.S. or abroad.

13. I have taught a number of different courses at the undergraduate and graduate levels, including “Solid-State Technology Laboratory” and “Digital Integrated Circuit Technologies”, within the EECS department at the University of Michigan. These courses have generally covered the physics, technology, design, and fabrication of solid-state devices and integrated circuits. I have also introduced two new courses, including “Flat Panel Displays” and “Thin Film Devices Technology” in 1997, which are still being offered annually. These courses have generally covered the thin-film devices and circuits technologies used in different display technologies including AM-OLEDs. As a faculty member, I direct at any given time the research of several graduate and undergraduate students in Solid-State Devices and Nanotechnology, including semiconductors, electronic materials,

devices, and circuits for various applications including FPDs. As part of my group research, I utilize the University of Michigan Lurie Nanofabrication Facility (LNF), <https://lnf.umich.edu/>, that among others has the capability to fabricate and test devices and circuits used in the FPDs and IC industries. Moreover, over the years I have also supervised the research of several post-doctoral fellows and visiting scientists from industry or/and other universities within my group doing research in the area of solid-state devices and circuits. More information about my professional activities can be found on my research group web page: www.eecs.umich.edu/omelab/.

14. From 2002 to 2003, I was on sabbatical at the University of California Santa Barbara (UCSB) within the Center for Polymers and Organic Solids. My research was related to organic polymer thin-film transistors, organic light-emitting devices and electrically injected lasers. My host was Professor Alan J. Heeger from Physics Department. He won the Nobel Prize for Chemistry in 2000 along with Alan G. MacDiarmid and Hideki Shirakawa "for their discovery and development of conductive polymers."

15. From 2009 to 2010, I was on sabbatical at the University of California San Diego (UCSD) within the California Institute for Telecommunications and Information Technology. My research was related to organic polymer thin-film

transistor chemical sensors, amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs), image sensors and solar cells. My host was Professor Andrew C. Kummel from the Department of Chemistry and Biochemistry.

16. From 2018 to 2019, I was on sabbatical at the Massachusetts Institute of Technology within Microsystems Technology Laboratories. My research was related to hydrogenated diamond devices and circuits, and Perovskites materials based opto-electronic devices. My host was Professor Jesus del Alamo from Department of Electrical Engineering and Computer Science.

17. From 2024 to 2025, I was on sabbatical at the Massachusetts Institute of Technology within Research Laboratory of Electronics (RTL). My research was related to pixel driving circuits for micro – LEDs and micro-LEDs fabrication and integration with the backplane electronics based on CMOS, low temperature polycrystalline silicon thin film transistors (poly-Si TFTs) or amorphous InGaZnO (a-IGZO) TFTs. My host was Professor Jeehwan Kim of the Department Materials Science and Engineering and Mechanical Engineering, respectively.

18. I am a member of several professional organizations including the Society for Information Display (SID) and the Institute of Electrical and Electronics Engineers (IEEE). My areas of expertise include chemistry, solid-state physics, material sciences, device physics, circuits, solid-state device and circuit fabrication

/ manufacturing methods, and nanotechnology. I have edited or co-edited several books, authored over 300 technical papers, and given over 350 presentations (among which over 70 were invited presentations) relating to thin film semiconductor devices, circuits, and associated FPD technologies. My papers have received over 12,000 citations, and I have an H-index of 60, i10-index of 204, RG score of 42.30 and D-index of 51. I was included in World Best Scientist 2025 and ranked 886 in the US and 2316 in the world, respectively. To be ranked you must meet the D-index inclusive threshold typically between 30–70 depending on discipline. I have also been the chair or co-chair at numerous national and international FPD conferences and symposia. I was an editor for IEEE Transactions on Electron Devices for eight years, and I am a reviewer for several prestigious international archival journals. I am also a reviewer of proposals for several federal agencies, such as the National Science Foundation (NSF), Department of Defense (DoD), and Defense Advanced Research Program Agency (DARPA). Among other distinctions, I was awarded the IBM External Honors, which recognizes the technical leadership of staff members in IBM's Research Division, three times. My research work at the University of Michigan has been supported by grants from the state of Michigan, federal agencies, and a number of international industries.

19. Through my experience and education, I am familiar with most aspects

of the manufacturing processes and circuits used in the flat panel displays and integrated circuits industries, including thin film deposition, etching chemistry, chemical mechanical polishing, devices and circuits processing, and photolithography, as they relate to device and circuit fabrication, applications and/or operations. My latest curriculum vitae, and a list of my publications and presentations, is appended as EX1004.

20. In the previous five years (2019 – 2024), I have testified as an expert at trial or by deposition or have submitted declarations in the following cases:

- 2023: Dispute related to AM-OLEDs between Samsung Display Co., Ltd. and AU Optronics Corp.: Perkins Coie LLP (Consultant for AUO).
- 2023: Case related to U.S. ITC Investigation No. 337-TA-1351. “Certain Active-Matrix Organic Light Emitting Diode Display Panels and Modules For Mobile Devices, and Components Thereof.” Adverse party in this action is Samsung Display Co Ltd.: Morrison & Foerster LLP (Consultant for Apple Inc.)
- 2021: Advanced Silicon Group Technologies, LLC v. Boviet Solar Technology Co., Ltd; Ningbo Boway Alloy Material Co., Ltd.; Boviet Renewable Power LLC; Boviet Solar USA Ltd (collectively, “Boviet,” northern District of California (3:21-cv-04510-LB) & ITC Inv. No.

337-TA-1271): Morgan Lewis & Bockius LLP (consultant and expert witness for Boviet) – prepared expert report & declaration, was deposited, prepared witness statement & rebuttal witness statement, attended hearing & testified at the trial in front of the US ITC

- 2021: Semiconductor Energy Laboratory Co., LTD v. TCL China Star Optoelectronics Technology Co., Ltd., et al, Civil Action #: 8:21-cv-00554 – JAK – ADS (CDCA): PV Law LLP (consultant and expert for TCL China Star Optoelectronics Technology Co., Ltd. – prepared four declarations in support of petition for for Inter Partes Reviews (IPRs) of several patents involved in this case
- 2020: Solas OLED Ltd. V. Samsung Electronics Co. Ltd., Samsung Electronics America, Inc., Samsung Display Co. Ltd (collectively “Samsung”), Case N. 2:20-cv-00307 – JRG (E.D. Texas) & ITC Inv. 337-3490, O’Melveny & Myers LPP (consultant and expert for Samsung)
- 2020: HP Inc. v. Solas OLED Ltd., Case N. 6:19-cv-00631-ADA (W.D. Texas); O’Melveny & Myers LLP (consultant and expert for HP Inc.)
- 2020: Apple Inc. v. Solas OLED Ltd., Case N. 6:19-cv-00537 – ADA (W.D. Texas), DLA Piper LLP (consultant and expert for Apple Corp.)

- 2020: Sharp v. Vizio et al., Case N. 8:20-cv-00490, US District Court for the Central District of California and DN 3451 before the International Trade Commission, K&L Gates LLP (consultant and expert witness for Sharp. Corp.)
- 2019: Hologic Inc. v. Direct Digital Imaging Tech. (Beijing) Inc., Case N. 1884-cv-01154 – BLSI, Litigation and Trade Secret, Mintz (consultant and expert for DDIT)
- 2019: LG Display v. Solas OLED Ltd.; Case N. 6:19-cv-235-ADA; Latham & Watkins LLP (consultant and expert for LG Display Co., Ltd.).

21. Considering the foregoing, I consider myself to be an expert in the field of flat panel displays and integrated circuits manufacturing, including OLED displays, and including thin film deposition techniques, etching chemistry, chemical-mechanical polishing, devices and circuits processing and photolithographic steps, and the designs used in the fabrication of devices and circuits, with the feature sizes ranging from micron to submicron for various industrial applications including FPDs. Therefore, I believe that I am qualified to provide an opinion as to what a person of ordinary skill in the art at the time of the invention (“POSITA”) would have understood, known, or concluded regarding the

subject matter of the patents involved in this case.

III. LEVEL OF ORDINARY SKILL IN THE ART

22. My analysis reflects the views of a person of ordinary skill in the art (POSITA) in the field of the '990 Patent as of August 2, 2012, which I understand is the alleged time of invention.

23. I have been advised by the Petitioner's counsel and understand there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including (1) the levels of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior art solutions to those problems. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from teachings of the prior art, including the art cited below.

24. Taking these factors into consideration, in my opinion, on or before August 2, 2012, a POSITA would have been someone knowledgeable and familiar with design or development of display circuits and systems that are pertinent to the '990 Patent. That person would have a bachelor's degree in electrical engineering, physics, materials science or engineering, or a related field and at least four years of practical experience with design or development of active-matrix OLED displays,

including pixel layout, or the equivalent. In my opinion, a lack of work experience can be remedied by additional education, and vice versa.

25. As of August 2, 2012, I met, and in fact exceeded, the qualifications of a person of ordinary skill in the art.

26. For purposes of this Declaration, in general, and unless otherwise noted, my statements and opinions, such as those regarding my experience and the understanding of a POSITA generally (and specifically related to the references I consulted herein), reflect the knowledge that existed in the field as of the earliest possible priority date of the '990 Patent (i.e., August 2, 2012). Unless otherwise stated, when I provide my understanding and analysis below, it is consistent with the level of a POSITA prior to the earliest alleged priority date of the '990 Patent.

IV. RELEVANT LEGAL STANDARDS

27. I am not an attorney. In preparing and expressing my opinions and considering the subject matter of the '990 Patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

28. I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious in view of what was known before the invention was made.

29. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally

includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

30. I understand that in this proceeding Petitioner has the burden of proving that the claims of the '990 Patent are anticipated by or obvious in view of the prior art by a preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not.

31. I understand that prior art to the '990 Patent in this proceeding includes patents and printed publications in the relevant art that predate the proper priority date of the alleged invention recited in the '990 Patent.

32. I understand that terms appearing in the patent claims are to be interpreted according to their “ordinary and customary meaning” in an IPR proceeding. In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning as they would have been understood by a POSITA at the time of the alleged invention, in light of the specification and file history. I understand that treatises and dictionaries may be consulted, albeit under limited circumstances, to determine the meaning attributed by a POSITA at the time of the alleged invention. I have followed this approach in my analysis and have applied the ordinary and customary meaning of those terms throughout my analysis in this Declaration.

33. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to “anticipate” the claim. Second, the prior art can be shown to have made the claim “obvious” to a person of ordinary skill in the art. In this declaration I focus on “obviousness.” My understanding of the legal standard for “obviousness” is set forth below.

34. I have been informed that a claimed invention is unpatentable as obvious if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. I have also been informed by counsel that the obviousness analysis takes into account factual inquiries including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter.

35. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non- obviousness

may be present in any particular case.

36. I have been informed by counsel that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include the following: (a) combining prior art elements according to known methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. I also understand that, at least in IPR proceedings, admissions in the patent or in the prosecution file history of the patent (referred to as Applicant Admitted Prior Art or “AAPA”) can be used to, among other things, establish background knowledge possessed by a POSITA.

37. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include,

among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

38. I am not aware of any allegations by the named inventor of the '990 Patent or any assignee of the '990 Patent that any secondary considerations are relevant to the obviousness analysis of any Challenged Claim of the '990 Patent.

39. I understand that a petition must identify, for any terms with means-plus-function limitations, the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function. I also understand a rebuttable presumption exists that without use of the term, “means,” a claim term is not interpreted as means-plus-function, but that other nonce words like “component” have been found to satisfy the rebuttable presumption and invoke a means-plus-function claim construction of such a claim term.

40. I also understand that a petitioner seeking to demonstrate that the prior art discloses a means-plus-function limitation must prove that the corresponding structure—or an equivalent—was present in the prior art and performing the same claimed function.

41. I understand that the standard for determining whether the prior art discloses the corresponding structure or an equivalent is whether there are insubstantial differences, which means that if the assertedly equivalent structure performs the claimed function in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification, it is equivalent.

42. I understand that proving structural equivalence does not require a component-by-component analysis, but rather that it is sufficient to show structure, materials, or acts that perform the claimed function in substantially the same way to achieve substantially the same result because the claim limitation is the overall structure corresponding to the claimed function and not individual components.

43. I understand that for a claim to be valid, its scope must be definite, and that improperly introducing a term can lead to an unascertainable scope of a term, rendering it indefinite. I understand that any claim element first addressed in the claims by the antecedent basis, “a” may then be identified later in the claims by the

antecedent basis, “the.” I understand that failing to follow this convention may lead to ambiguity in the identification of the particular claim element in question, leading to an indefinite scope of the claim’s term. For purposes of this proceeding, I identified and provided my best understanding of any such terms despite such ascertainable scope.

V. SUMMARY OF THE ’990 PATENT

A. Specification

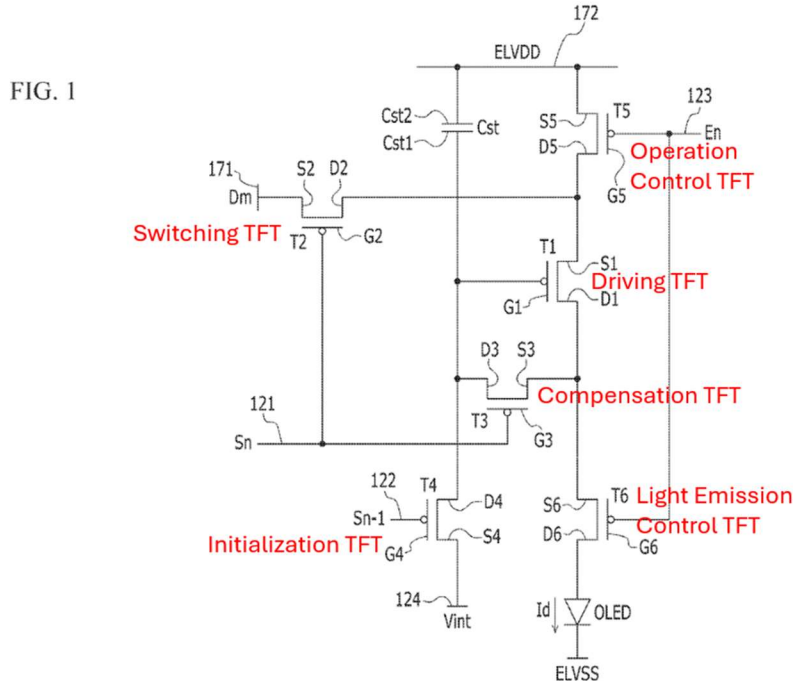
44. The ’990 patent describes an organic light emitting diode (OLED) display that includes a plurality of pixels, with each pixel including a plurality of signal lines, a plurality of thin film transistors (TFTs), a storage capacitor, and an OLED coupled to the plurality of signal lines. Ex. 1001, 1:45-46 and 6:12-19.

45. Pixels of existing OLED implementations, as described by the ’990 patent, include a switching TFT and a driving TFT such that in the switching TFT, a thin gate insulating layer is formed between a gate electrode and a semiconductor layer to enable rapid switching operation. *Id.*, 1:49-54. However, the ’990 patent explains that because the thickness of the gate insulating layer of the driving TFT, which is formed on the same layer as the switching TFT, is reduced, a driving range of a gate voltage applied to the gate electrode of the driving TFT becomes narrow, which may make it difficult to control the magnitude of the gate voltage V_{gs} of the driving TFT to ensure a large number of gray levels. *Id.*, 1:54-61.

46. The technology described in the '990 patent provides an OLED display broadening a driving range of a driving TFT to display a relatively large number of gray levels. *Id.*, 2:3-6. According to a described embodiment, this is achieved by longitudinally forming the channel region of the driving TFT by forming the semiconductor layer of the driving TFT to include a plurality of bent portions. *Id.* 4:48-53. Furthermore, low gray level stains can be avoided or prevented by setting a length of a first path semiconductor layer coupled to a compensation TFT to be smaller than a length of a second path semiconductor layer coupled to a light emission control TFT. *Id.*, 4:66-5:3.

47. The '990 patent describes an exemplary embodiment of an OLED display with reference to FIGS. 1 to 5. *Id.*, 6:9-11. The equivalent circuit of one pixel of the OLED display is shown in FIG. 1, with FIGS. 2 and 3 showing specific layout (or plan) views of the OLED display, and FIG. 4 and 5 showing cross-sectional views of the OLED display taken along different cut lines. *Id.*, 6:12-14 and 8:37-51.

48. I have annotated FIG. 1 below to explain the operation of one pixel of the OLED display as described in the '990 patent. As shown therein, the equivalent circuit includes a plurality of signal lines (121-124 and 171-172), a plurality of TFTs (T1-T6, and annotated in FIG. 1), a storage capacitor (Cst), and an OLED coupled to the plurality of signal lines. *Id.*, 6:14-19.



'990 patent, FIG. 1 (annotated).

49. In the context of Figure 1, the operation of one pixel (all transistors included in the pixel circuits are p-channel) of the OLED display begins with a low-level signal (e.g., negative gate voltages since p-channel TFTs are being used) prior scan signal S_{n-1} being supplied through the prior scan line 122 during an initialization period. Then, the initialization TFT T4 is turned on to initialize the gate voltage of the driving TFT T1 with an initialization voltage V_{int} . Subsequently, a low-level signal scan signal S_n is supplied through the scan line 121 to turn on compensation TFT T3 and switching TFT T2. This step will allow for data signal D_m to be transferred to source electrode of driving TFT T1. Since T3 is turned on, the gate electrode G1 and drain electrode D1 are connected together forming diode-

like connection TFT. Then, a compensation voltage ($D_m + V_{th}$) based on the data signal D_m supplied from data line 171 is applied to the gate electrode G1 of the driving TFT T1. The driving voltage ELVDD and the compensation voltage $D_m + V_{th}$ are applied to both ends Cst1 and Cst2 of the storage capacitor Cst, and a charge corresponding to a difference between voltages at both ends Cst1 and Cst2 is stored in the storage capacitor Cst. Subsequently, the level of the light emission control signal E_n during a light emission period is changed from a high level to a low level, which turns on the operation control TFT T5 and the light emission control TFT T6. Then, the driving current I_d is generated according to a difference between the voltage of the gate electrode G1 of the driving TFT T1 and the driving voltage ELVDD. Hence, the driving current I_d , which is proportional to $(D_m - ELVDD)^2$, is determined regardless of the threshold voltage V_{th} of the driving thin film transistor T1 and is supplied through the light emission control TFT T6 to the OLED. *Id.*, 7:56-8:36.

50. The '990 patent describes that the six TFTs T1-T6 are formed along the semiconductor layer 131, and the semiconductor layer 131 is bent to have various shapes. *Id.*, 9:4-10. The driving semiconductor layer 131a including a plurality of bent portions 33 results in the driving range of the gate voltage applied to the driving gate electrode 125a being broadened. This enables a gray level of light emitted from

an OLED to be more finely and precisely controlled by adjusting the magnitude of the gate voltage, and as a result, it is possible to increase a resolution of the organic light emitting diode display and improve display quality. *Id.*, 9:49-62.

51. The '990 patent further describes the storage capacitor Cst includes a first storage capacitor plate 125h and a second storage capacitor plate 127 with the second gate insulating layer 142 interposed therebetween. Herein, the driving gate electrode 125a also plays a role of the first storage capacitor plate 125h, the second gate insulating layer 142 becomes a dielectric material, and storage capacitance is determined by the charge accumulated in the storage capacitor Cst, and by the voltage between both capacitor plates 125a and 127. *Id.*, 10:14-23.

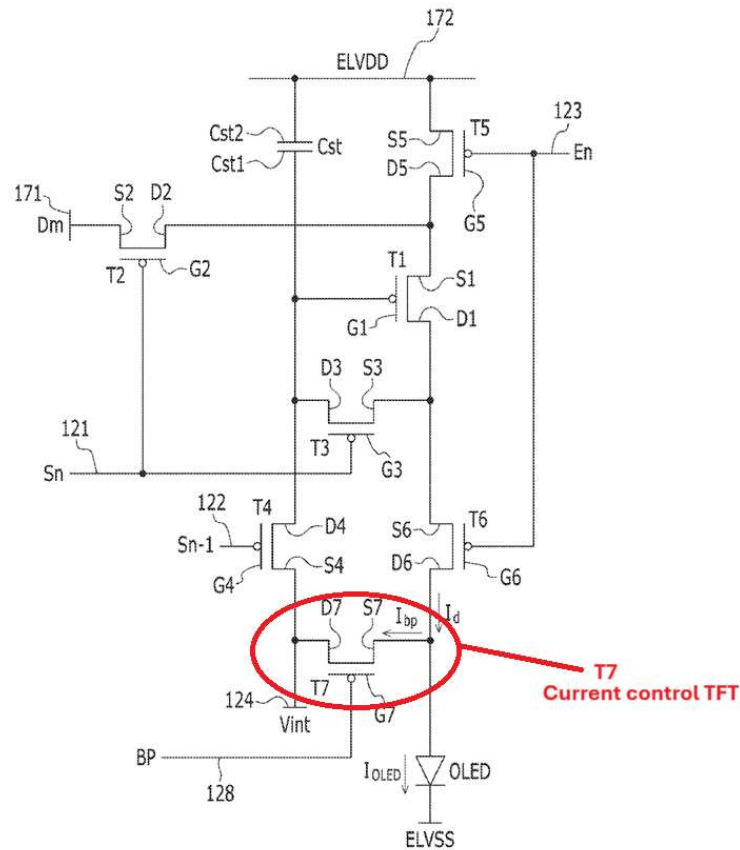
52. In the embodiment corresponding to Figure 1, the compensation TFT T3 includes the compensation semiconductor layer 131c, the compensation gate electrode 125c, the compensation source electrode 176c, and the compensation drain electrode 177c. Herein the compensation gate electrode 125c is defined as a separate dual gate electrode 25 to prevent a leakage current. *Id.*, 10:49-60.

53. With reference to Figure 6, the '990 patent discloses the driving semiconductor layer 131a being in the shape of an S. *Id.*, 10:5-6. In this embodiment, the storage capacitor Cst is formed thereon to overlap the driving gate electrode 125a, with the driving gate electrode 125a also playing a role of the first storage capacitor

plate 125h. *Id.*, 10:12-18. Furthermore, the first storage capacitor plate 125h is formed of the same material as the scan line 121, the prior scan line 122, the light emission control line 123, the switching gate electrode 125b, the compensation gate electrode 125c, the operation control gate electrode 125e, and the light emission control gate electrode 125f, which are on the same layer first storage capacitor plate 125h. *Id.*, 10:23-30. In addition, the second storage capacitor plate 127 is coupled to the adjacent pixel, and is formed of the same material as the initialization voltage line 124, and is formed on the same layer as the initialization voltage line 124. *Id.*, 10:31-34.

54. In an alternative embodiment, with reference to Figure 10 reproduced below and annotated, the '990 patent describes incorporating an additional current control (or bypass) TFT T7 into the circuit illustrated in Figure 1.

FIG. 10



'990 patent, FIG. 10 (annotated).

55. As shown in Figure 10, the gate electrode G7 of the bypass TFT T7 is coupled to the bypass control line 128, a source electrode S7 of the bypass TFT T7 is coupled to the drain electrode D6 of the light emission control TFT T6 and to the anode of the OLED, and a drain electrode D7 of the bypass TFT T7 is coupled to the initialization voltage line 124 and to the source electrode S4 of the initialization TFT T4. *Id.*, 19:36-43. The bypass TFT T7 of the OLED display is configured to disperse, or divert, a portion of the minimum current of the driving thin film transistor T1 as

a bypass current Ibp to a current path other than the current path of the organic light emitting diode. *Id.*, 19:59-65. Accordingly, a contrast ratio may be improved by implementing a precise black luminance image by using the bypass thin film transistor T7. *Id.*, 20:17-19.

B. Prosecution History

56. I understand that the '990 patent issued from U.S. Patent Application No. 17/853,551 that was filed on June 29, 2022, with a (Track One) Prioritized Examination Request, which was granted. The '990 patent claims priority to Korean Patent Application No. 10-2012-0084976 filed on August 2, 2012. For the purposes of this declaration, I treat August 2, 2012, as the priority date for the '990 patent.

57. By my review, Liu was cited in an Information Disclosure Statement (IDS) filed by the Application on June 29, 2022. '990FH, p. 319. As discussed in this declaration, had the Examiner considered Liu, and combined it with other references discussed below, one or more claims of the '990 patent would have been found to be obvious in view of the disclosure in Liu.

58. The Examiner issued a Non-Final Office Action dated September 2, 2022 in which the title was objected to for not being descriptive, certain claims were rejected for minor informalities, and claims 1-10, 11-15, 16-22, 24, 25, and 27-30 were rejected on nonstatutory double patenting grounds as being unpatentable over claims of U.S. Patent No. 10,483,342 (hereinafter the "Kim '342 patent") and further

in view of U.S. Patent No. 9,899,464 and U.S. Patent No. 9,660,012. *Id.*, pp. 139-146.

59. The '990 patent is a continuation application of the Kim '342 patent, and in response to the rejection on nonstatutory double patenting grounds, the Applicant filed a Terminal Disclaimer over the Kim '342 patent. *Id.*, pp. 131-132.

60. A Notice of Allowance mailed on October 4, 2022 stated "Claims 1-30 are allowed primarily because the prior art of record cannot anticipate or render obvious the following limitations, in combination as recited in independent claim 1: a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor being curved; a third thin film transistor electrically coupled to the second thin film transistor. .. the semiconductor layer being extended to and electrically coupled to the third thin film transistor." *Id.*, pp. 96-102.

61. Subsequent to the issuance Notice of Allowance, Applicant filed (1) an IDS on October 20, 2022, (2) an IDS on October 31, 2022, and Amendment under 37 C.F.R. § 1.312 to correct minor informalities on November 3, 2022, and (3) an IDS on December 2, 2022. *Id.*, pp. 43-46, 71-74, 86-89. Subsequent to each of the above-enumerated filings, a Corrected Notice of Allowability was issued, and the '990 patent issued on February 7, 2023. *Id.*, pp. 2-3, 37-38, 55-56.

VI. TECHNOLOGY BACKGROUND

A. OLED Displays—From Inception to 2012

62. Organic light-emitting diodes (OLEDs) are based on electroluminescence in organic materials, whose discovery can be traced back to the 1950s when light emission was observed by applying high voltage to thin films of acridine orange and quinacrine, which were dissolved in or deposited on thin-film cellulose or cellophane. *See generally* Bernanose. One mechanism identified in these processes involved excitation of electrons. Then in 1960 a team of investigators at New York University made ohmic dark – injecting electrode contacts to organic crystals and describe the necessary work functions (energy requirements) for hole and electron injecting electrode contacts. *See generally* Kallmann. These carrier injecting contacts are the source of charge injections in all present-day OLED devices. In the mid-1960s, Pope observed bright blue electroluminescence (EL) in single crystal anthracene by applying a high DC voltage (about 400V) across the crystal. *See generally* Pope. The proposed mechanism for light emission was termed field-accelerated electron excitation of molecular fluorescence. The same group later observed that in the absence of an external electric field, the EL in anthracene crystals results from recombination of electron and hole, and that the conducting-level energy of anthracene is higher than the exciton energy level. *See generally* Sano. Later, Vincett used evaporated thin film of anthracene and was able to reduce

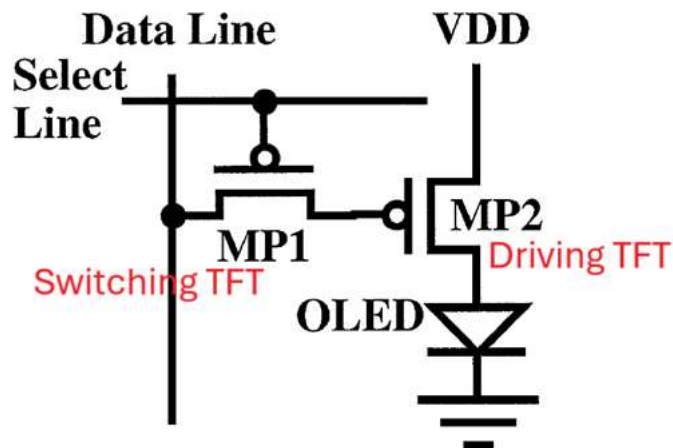
the drive voltage to below 30V. However, the quantum efficiency of this device was only about 0.05%. *See generally* Vincett. The first report of an organic LED was in the seminal work by Tang in the 1980s, which demonstrated a heterojunction device and developed a doping method by introducing a small number of fluorescent materials into a host matrix. *See generally* Tang. The OLED heterojunction is a basic device structure of all present-day OLED devices. The electroluminescence in conjugated polymer poly(p-phenylene-vinylene) (PPV) was reported in 1990. *See generally* Burroughes. This work was followed by a breakthrough in the late 1990s when phosphorescent light-emitting materials, which dramatically improved the quantum efficiency and brightness of the OLED devices, were discovered. *See generally* Baldo. Higher light emission efficiency will allow reduction of driving voltage used for driving thin film transistors (TFTs). It is expected that this will lead to more stable active-matrix (AM)-OLEDs. Today, phosphorescent OLED (PHOLED) is a cornerstone technology for low-power (e.g. low voltage) bright organic light emitting displays and energy-efficient light sources.

63. The various milestones in the evolution of the driving/control circuitry for the OLED pixel are now discussed to emphasize the gradual innovation of this technology from the late 1990's to the early 2010's. As I explain below, the purported novel and inventive features of the '990 patent existed before the priority

date of the '990 patent.

1. Two transistor (2T) and two transistor, one capacitor (2T1C) pixel circuits:

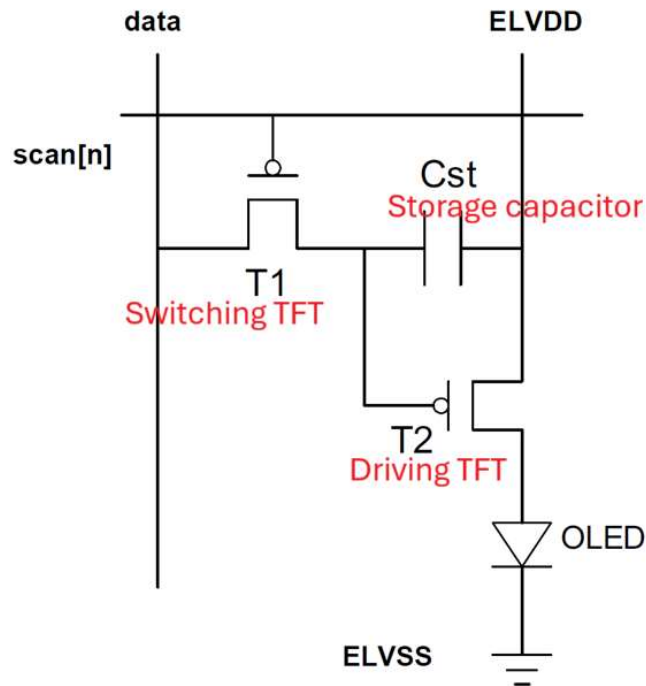
64. The two transistor (2T) circuit represents the minimal pixel circuit design required for AMOLEDs. Dawson, p. 2. In this basic pixel design, the first TFT is used for switching (e.g., selecting the pixel) and the second TFT is used for driving (e.g., as a current source). An example of such a 2T pixel circuit is shown in Figure 1 of Dawson (reproduced below and annotated).



Dawson, FIG. 1 (annotated).

65. The 2T circuit can be augmented with one storage capacitor (or “holding capacitor”) that is used to store driving TFT gate voltage, which will be responsible for keeping TFT turn on between refresh cycles. An example of such two transistor, one capacitor (2T1C) circuit, is shown in the figure below, prevents the pixel voltage from drifting due to leakage currents or parasitic effects. However,

the current resistance (IR) drop problem remains for the 2T1C circuit. Kim-2009, §3.1.



Kim-2009, FIG. 3 (annotated).

66. In the operation of the 2T1C circuit, when the pixel is selected, the switching TFT is turned on by the gate signal (voltage), allowing data signal (voltage) to be charged onto the storage capacitor, C_{st} . This voltage is also the gate voltage of the driving TFT. Depending on the amplitude of the gate voltage, OLED current at different levels will flow from power line (or anode) for a given voltage value, V_{DD} , to the ground (or cathode) through OLED device. The switching TFT is only on when the pixel is selected and the storage capacitor is charged. The key requirement for this transistor is low leakage current, which prevents the storage capacitor from

discharging. For the driving TFT, depending on the signals, it could be on during the whole frame time with current ability to conduct large currents. It is desirable for a TFT to operate in a saturation regime since it does a better job to keep a constant current when the OLED resistance changes over time.

67. In these 2T and 2T1C pixel driving circuits, n-channel TFTs, p-channel TFTs, or combination of n-channel TFTs and p-channel TFTs can be used. The OLED displays are driven by electric current, so small drain current variations due to the threshold variation, for example, can produce non-uniformity in display brightness. Furthermore, neither the 2T circuit nor the 2T1C circuit includes compensation for TFT threshold voltage (V_{th}) drift or IR drop across the display. These issues were addressed with the introduction of 4T1C and 5T1C circuits, as discussed below.

2. Four transistor, one capacitor (4T1C) and five transistor, one capacitor (5T1C) pixel circuits:

68. Since TFT threshold voltage variations can be observed during poly-Si TFT fabrication and over time during OLED display operation, there is need to compensate poly-Si TFT threshold voltage (V_{th}) variation to realize a good quality OLED display with uniform luminance. To fulfill this need, 4T1C and 5T1C pixel circuits have been introduced. *See, e.g., Dawson, p. 3 for 4T1C pixel circuit; Kim-2009, §3.2 for 5T1C pixel circuit.* The basic principle of V_{th} compensation is to store

the driver TFT V_{th} in the gate node as $V_G = V_D + V_{th}$, by connecting gate and drain nodes as shown in the figure below.

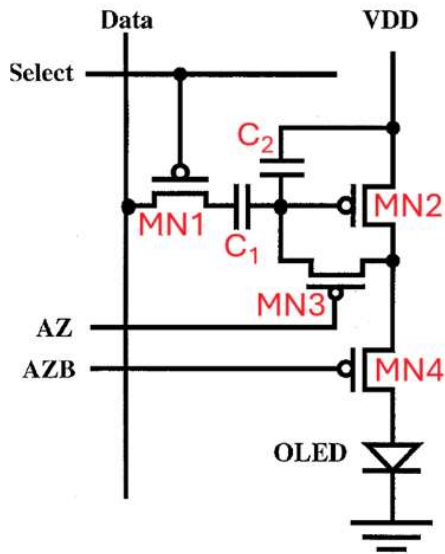


Fig. 3. Schematic of Four-Transistor AMOLED Pixel with Autozero.

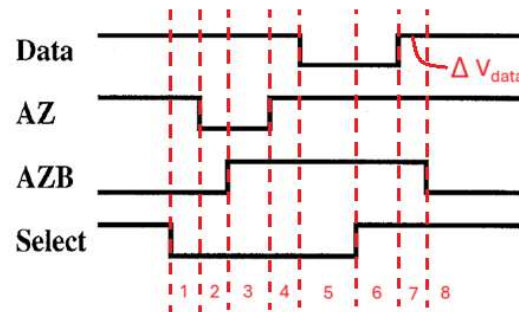


Fig. 4. Four-Transistor AMOLED Pixel Timing Diagram

Left: Dawson, FIG. 3 (annotated); Right: Dawson, FIG. 4 (annotated).

69. The pixel circuit in FIG. 3 above shows a threshold voltage (V_{th}) compensation circuit by voltage programming and is the likely prototype of most subsequently proposed compensation pixel circuits. With reference to FIG. 4 above, the operation of this circuit can be explained as follows: (1) The AZ line is set to negative voltage, and MN3 TFT turns on. (Note that the TFT is p-channel.). (2) The gate node and drain node of MN2 are connected, so the gate node of driver TFT (MN2) stores V_{th} information. (3) The data line signal voltage is added to the driver TFT gate node using capacitance coupling of C1. (4) As the gate node of the driver

TFT stores the data line signal plus V_{th} , the source – drain current of the driver TFT does not contain V_{th} information. Therefore, mura (non-uniformities) related to TFT V_{th} variation does not take place, due to the threshold cancellation mechanism. Voltage programming was the method most frequently used for actual OLED display products developed before 2012.

70. However, the IC driver voltage programming for the 4T1C and 5T1C circuits has some disadvantages such as the inability to compensate for either TFT mobility variations or OLED turn-on voltage variation and aperture ratio loss due to the space occupied by the programming circuit in bottom emission structure implementations. These drawbacks were mitigated by the introduction of six transistors, one capacitor (6T1C) pixel circuits and seven transistors, one capacitor (7T1C) pixel circuits.

3. Six transistors, one capacitor (6T1C) and seven transistors, one capacitor (7T1C) pixel circuits:

71. The 6T1C circuit added features like dual-gate or emission control transistors. This 6T1C pixel circuit is better than 4T1C or 5T1C pixel circuits because it compensates for both threshold voltage (V_{th}) variation and current resistance (IR) drop (*see generally* Lee-2012), but is limited at low grayscales, as explained in next section. The next section further explains that the 7T1C pixel circuit solved the lingering issues observed in 6T1C pixel circuits.

B. OLED Displays—State of the Art in 2012

72. 6T1C and 7T1C pixel circuits, and TFTs using a serpentine channel, represented the state of the art several years before 2012.

1. Six transistors, one capacitor (6T1C) Pixel Driving Circuits

73. In 4T1C and 5T1C pixel circuits, the characteristics of the two adjacent TFTs within a pixel could be different, e.g., different threshold voltages. In this case, the threshold voltage has not been compensated, and the quality of the image degrades. In an example, the mismatched electrical properties of the driving TFT and the compensating TFT in the same pixel circuit may result in not achieving enough compensating for the threshold voltage variation. This drawback is mitigated by using a new voltage programming AMOLED pixel circuit structure that can compensate for threshold voltage variation without additional mirror-type compensation TFTs, i.e., by using the 6T1C pixel structure.

74. The 6T1C pixel circuit was developed by graduate student S. Choi at Hanyang University Graduate School. His work was presented at the International Display Workshops (IDW) in 2003 and published in the proceedings thereof. *See generally* Choi. This initial work on 6T1C was followed by the introduction of the 7T1C pixel circuit thereby enabling the high-resolution AMOLED displays common today.

75. Figure 1 below shows a typical 6T1C pixel structure for AMOLEDs.

Therein, the M2, M3, M4, M5, and M6 are switching TFTs, and M1 is a driving TFT, which supplies emission current to OLED during a frame time. M4 creates a discharge path to initialize the gate voltage of M1, and C1 is a storage capacitor that stores the gate voltage of M1. Furthermore, and as shown in Figure 2 below, two row line times are needed to complete the data programming operation.

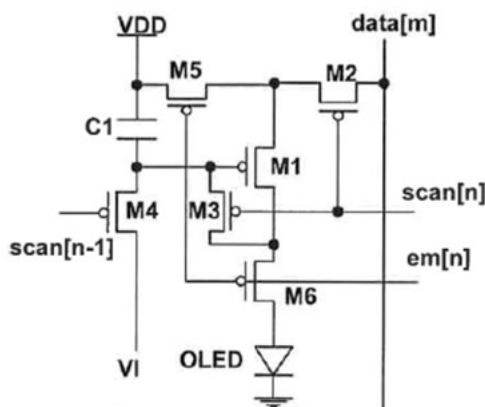


Figure 1. Proposed pixel structure.

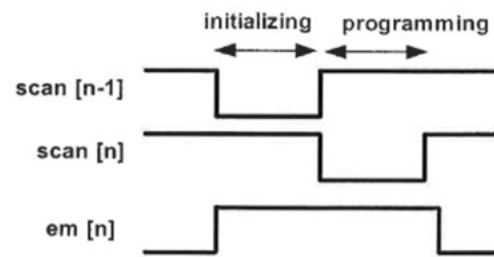


Figure 2. Timing diagram of proposed structure.

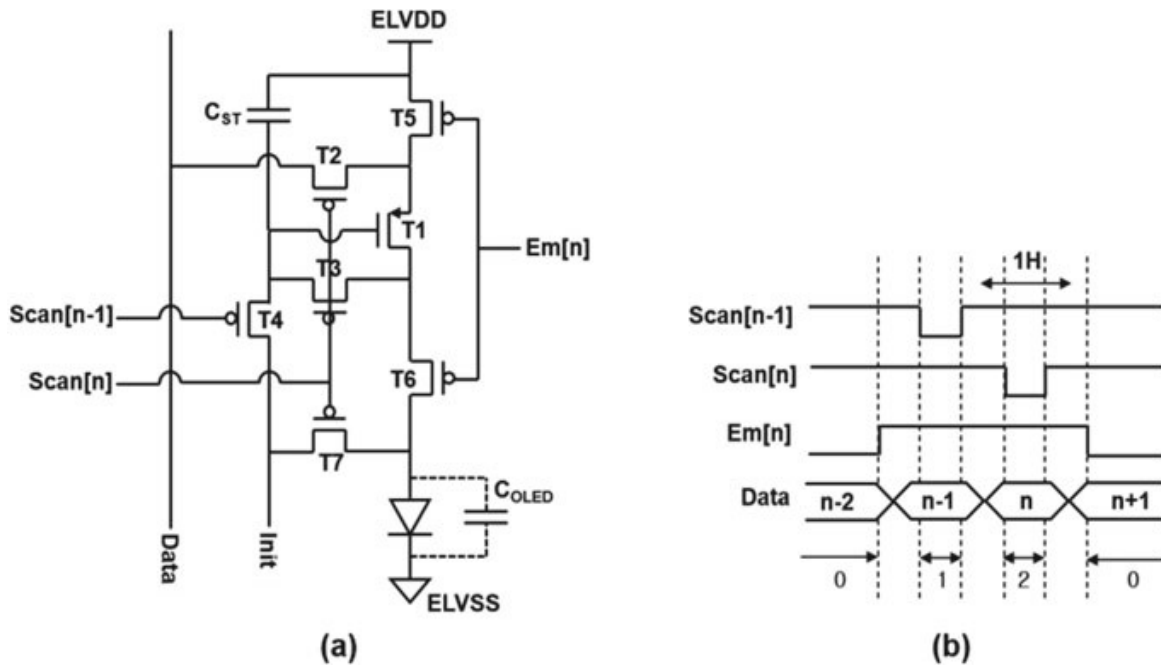
Left: Choi, FIG. 1; Right: Choi, FIG. 2.

76. As seen in the timing diagram in Figure 2, both scan[n] (current row scan signal) and scan [n-1] (previous row scan signal) are applied to program a single pixel of the OLED. During previous scan line time (when scan [n-1] signal is logic low), the gate voltage of M1 is discharged down to V1, whereas during current scan line time (when scan [n] signal is low), M2 and M3 are turned on so that data voltage is programmed to the gate node of M1 through diode-connected M1. At that time, the programmed data voltage is automatically reduced to $V_{\text{data}[m]} - V_{\text{th},M1}$, where

$V_{\text{data}[m]}$ and $V_{\text{th1},M1}$ are the programmed data voltage and threshold voltage of M1, respectively. After two line times, i.e., the previous and current line times, M5 and M6 are turned on by $\text{em}[n]$ signal, and the OLED emission current of programmed data, which is independent of the threshold voltage of M1, flows through M5, M1, and M6. The gate voltage of M1 already contains information of its threshold voltage, which is the desired effect of compensating for the threshold voltage mismatch of TFTs in the same pixel. This pixel structure can be modified to another pixel structure, based on display requirements.

2. Seven transistor, one capacitor (7T1C) Pixel Driving Circuit

77. The 7T1C pixel circuit for AMOLED displays emerged as an evolution of compensation circuits to address critical challenges in active-matrix OLED technology long before 2012. For example, Jeong, Chung, and Noguchi-II all disclose various examples of the 7T1C configuration. An example of a typical 7T1C pixel circuit, and its associated timing diagram, are shown below from Park. Although Park is after the priority date, it discusses the same subject matter that was available before 2012 and is presented for illustrative purposes only. In the timing diagram, the time durations denoted 0, 1, and 2 correspond to a light emission period, a data writing period, and a threshold voltage extraction period, respectively.



Park, FIGs. 15(a) and 15(b).

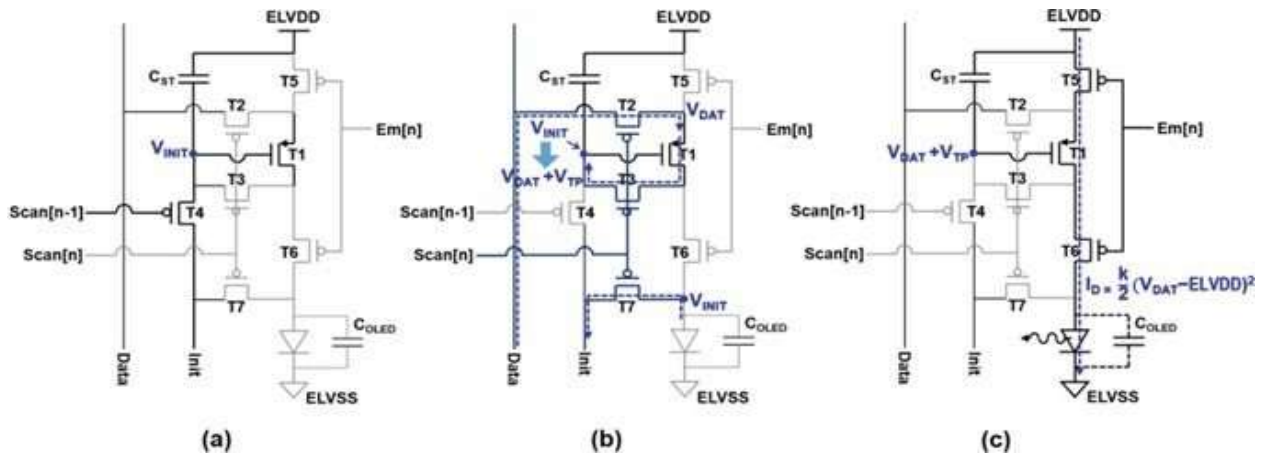
78. The 7T1C pixel circuit shown above has features such as anode reset (which initializes the OLED anode to a predefined voltage V_{in} , preventing residual voltage from previous frames) and cathode reset (which separately initializes the driving TFT's gate voltage, V_{ref}). This approach eliminates ghosting and improves low-gray accuracy. Also, the robust V_{th} compensation uses multiple phases (reset, compensation, data writing, emission) to isolate and store the driving TFT's V_{th} on the storage capacitor (C_{st}), which cancels V_{th} drift. Finally, this pixel circuit has emission control flexibility, e.g., dedicated transistors that decouple emission timing from data writing / compensation which enables the global emission (reduces flicker) and uses duty cycle control for brightness adjustment. The IR drop is mitigated

through compensation phases which account for voltage drops in power (V_{DD}) lines, ensuring uniform current flow.

79. The OLED pixel circuit shown in Figure 15(a) includes seven p-channel thin film transistors, one capacitor, and six lines – ELVSS (Electroluminescent Voltage Source), Vinit, Scan (n), Scan (n-1), Data, Em (n) and ELVDD (Electroluminescent Voltage Drain). Herein, T2 to T7 switching transistors have only on / off functionality, whereas T1 is a driving transistor whose current is controlled by the voltage applied to its gate through the DATA line. T2 corresponds to a scan transistor (or selection transistor) in the conventional 2T1C pixel circuit, T3 is diode-connected when it is turned on by the scan signal and is used to compensate for the threshold voltage of driving transistor T1, T4 is an initialization transistor, used to apply an initial voltage (Vinit) to the gate of the driving transistor, and T5 and T6 are emission control transistors to control current flow from ELVDD to OLED. T7, which is a black current bypass transistor that is used to remove a residual voltage of the anode of OLED after emission period, is discussed later. The capacitor overlaps with the driving transistor T1. The V_{GS} of T1 is stored in C_{ST} and determines the I_{OLED} according to the grey-level data. Independent of the driver TFT T1, T5 and T6 can be used to block I_{OLED} under the control of the Em[n] signal, which is consequently used for dimming control of the display panel.

80. Operation of the 7T1C pixel is shown in FIG. 16 of Park (which has been reproduced below), where (a), (b) and (c) correspond to initialization, data writing and threshold voltage extraction, and light emission period, respectively. The operation of data refresh with V_T compensation of T1 is carried out as follows. The initialization period begins with all the switch TFTs turned off, except T4, as shown in FIG. 16(a). Thus, the gate voltage of the driver T1 is pulled down to V_{INIT} and T1 is initially turned on. Then, T4 is turned off. Next, a data voltage V_{DAT} is applied to the source of T1 and V_T extraction is performed.

81. At the beginning of the data writing and threshold voltage extraction period, T2, T3 and T7 are turned on, as shown in FIG. 16(b) below. During this period, the gate node voltage of T1 changes from V_{INIT} to $V_{DAT} + V_{TP}$, where V_{TP} is the V_T of T1. At the same time, the anode of the OLED is discharged through T7 to prevent charge accumulation in the intrinsic OLED capacitance, C_{OLED} , by a leakage current through T1. Otherwise, some light will be emitted even when black expression is wanted. Finally, the gate voltage of T1 is stored by C_{ST} and the source of T1 is connected to ELVDD, as shown in FIG. 16(c), during light-emission period. The V_T extraction time of this circuit is limited to one horizontal line selection time—1H time—since the nth data voltage should be maintained throughout V_T extraction period.



Park, FIG. 16 (annotated).

82. In the 7T1C pixel circuit shown above, T7 is placed between T6 and OLED anode. The source of T7 (S7) is connected to OLED anode and the drain of T7 is connected to V_{int} (initialization voltage). At the node, the current I_d is divided into the current flowing to OLED and I_{bp}, which is referred to as bypass current. The T7 is black current bypass transistor, which is used to remove a residual voltage of the anode of OLED after emission period. When T7 is turned on by appropriate voltage applied to gate electrode (G7), the I_{bp} current can flow to V_{int} and OLED voltage at the anode becomes V_{int}. In other words, the anode of the OLED is discharged through T7 to prevent charge accumulation in the intrinsic OLED capacitance, by a leakage current through T1. Otherwise, some light will be emitted even when black expression is wanted. T7 can have a separate gate line or one connected to S_n line of T3.

3. TFTs Using Serpentine Channels

83. From the early 2000s (for example Udagawa), curved channel thin-film transistors (TFTs) represented a significant advancement in AMOLED display backplane design by efficiently addressing the critical need for high drive currents within the spatial constraints of high-resolution display pixels. Through innovative structuring—such as U-turns, S-shapes, and serpentine patterns—the transistor channel can be folded to dramatically increase the effective channel width (W_{eff}) without enlarging the overall device footprint. This increased channel width of the drive transistor substantially boosts the drive current (I_{ON}), which is essential for delivering sufficient pixel brightness, enabling fast pixel charging to support high refresh rates, and offsetting variations in OLED efficiency and degradation over time.

84. The foundational concept of curved channel designs has deep roots in semiconductor engineering, with seminal work dating back to the 1980s in silicon integrated circuits and subsequent adaptation for display technologies in the 1990s. The importance of this design approach grew markedly in the early 2000s alongside the proliferation of AMOLED displays, as shrinking pixel sizes created a growing demand for high current in confined areas. This challenge was further amplified in the 2010s with the adoption of oxide semiconductor backplanes (e.g., a-InGaZnO), which have lower carrier mobility than low-temperature polysilicon (LTPS) and therefore benefit greatly from channel geometries that maximize current capacity

and evenly distribute electrical stress and thermal load.

85. Thus, it is my opinion that the use of serpentine (curved) channels was well-established and widely known in the field of TFT design by 2012, with both academic literature and commercial practice recognizing their value for improving current delivery and device reliability in advanced display applications.

C. Architecture and Operation of OLED Display Pixels

86. In an AM-OLED, an image is divided into small elements called pixels. In a color AM-OLED, each pixel is further divided into three or four sub-pixels, one for each of the three primary colors red (R), green (G), and blue (B), e.g. tri-color OLEDs contain three different OLED emitters in one pixel. As explained above, each pixel (in a monochrome display) or sub-pixel (in a color display) contains at least two thin film transistors, a storage capacitor, and a pixel electrode (or more generally, a driving/control circuit), and an EL light emitting device. Hence, RGB OLEDs consist of one red, one green and one blue OLED. Also, each emitter is connected to a separate lead so they can be controlled independently. By independently adjusting brightness (or light intensity) of each of the three, RGB OLEDs the AM-OLED is capable of producing a wide range of colors.

87. The display format (i.e., the total number of pixels) and the display frame rate (i.e., how many times per second the image content will be updated) determine the required speed of the TFT switch. A typical display frame rate is 60

Hz, which implies that the image content will be updated every $1/60$ of a second, or 0.017 seconds. A typical computer monitor has the SXGA format (1280x1024 pixels). When such a display operates at a 60 Hz frame rate, the time that is allocated for updating or changing the voltage stored at the pixel's capacitor is $0.017/1024$ seconds, or about 17 microseconds. In order to ensure correct light output for the pixel, a pixel TFT must provide enough current to charge its pixel capacitor to the correct voltage level within the allocated time.

88. The architecture and operation of each driving/control integrated circuit, which independently controls each pixel of the OLED display, can be comprehensively understood through three distinct mechanisms: (1) the circuit diagram, (2) the layout (or plan) view, and (3) the cross-sectional view. I will now explain each of these mechanisms using the embodiments described in Liu.

1. Circuit Diagrams

89. A circuit diagram shows the logical and electrical connections between various components, the routing of data, control, and power signals, and how a certain component contributes to the overall operation. Liu provides a schematic circuit diagram of a pixel structure in Figure 1, which I have reproduced and annotated below. Liu, ¶13.

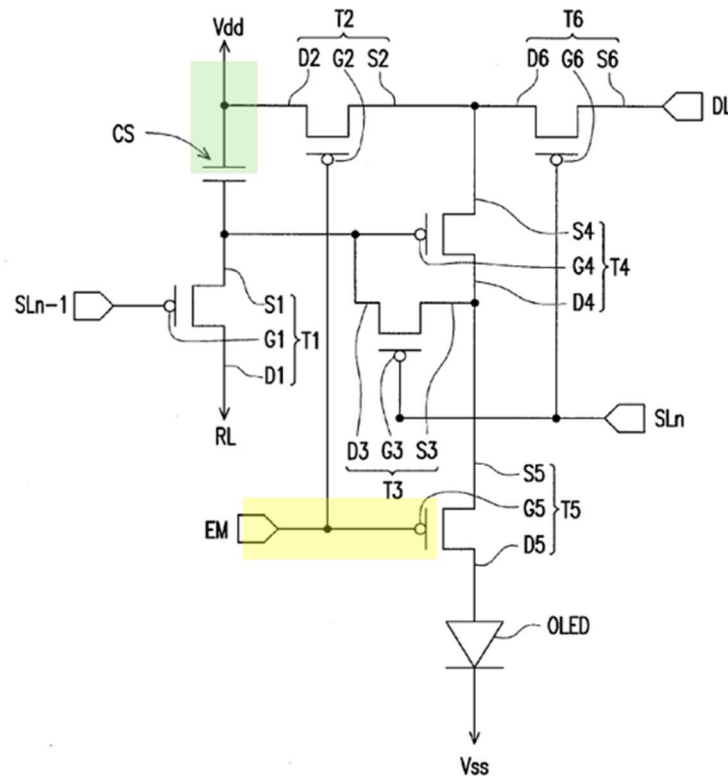


FIG. 1

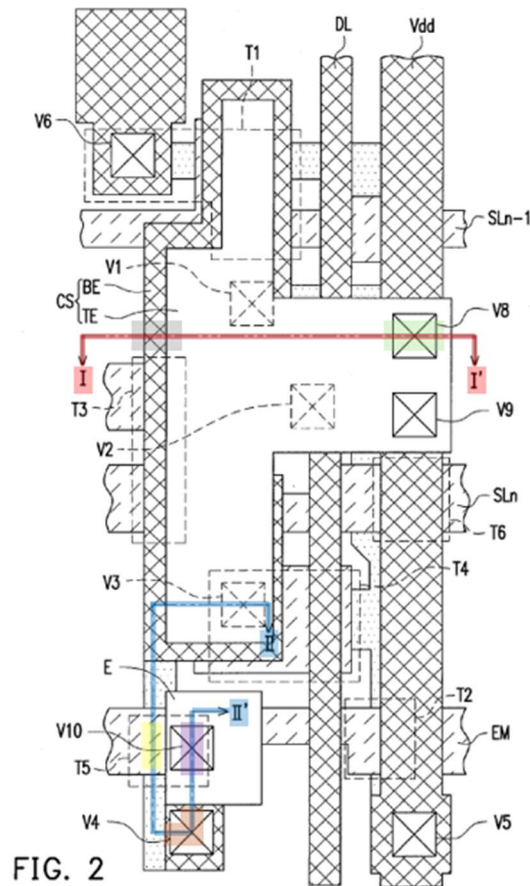
Liu, FIG. 1 (annotated).

90. As shown in Figure 1, the light emitting signal line EM is electrically connected to gate G5 of the fifth thin film transistor T5 (highlighted in yellow therein) and the top electrode TE is electrically connected to the power line Vdd (highlighted in green therein). Liu, ¶¶44, 64.

2. Plan Views

91. A plan (or layout) view shows the actual placement and routing of components (e.g., routing of metal layers and vias) and interconnections on the silicon die, which provides insight as to how efficiently the chip area is being used.

Liu further provides a top (or layout or plan) view of the pixel structure in Figure 2, which I have reproduced and annotated below. Liu, ¶14.



Liu, FIG. 2 (annotated).

92. To better understand the operation of the driving/control circuit of the OLED shown in Figures 1 and 2 of Liu, separating each of the layers described above allows one to appreciate the level of technology and state of the art that existed before the priority date of the '990 patent. Figures 3A-3D of Liu, which show the different layers of the pixel structure, are reproduced below.

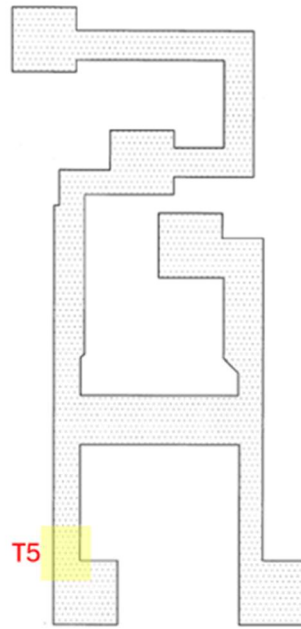


FIG. 3A

P0

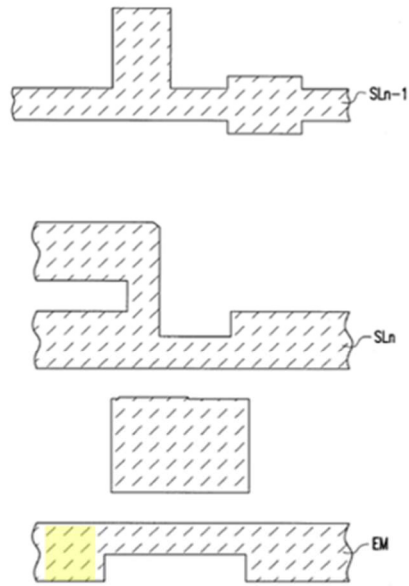


FIG. 3B

M1

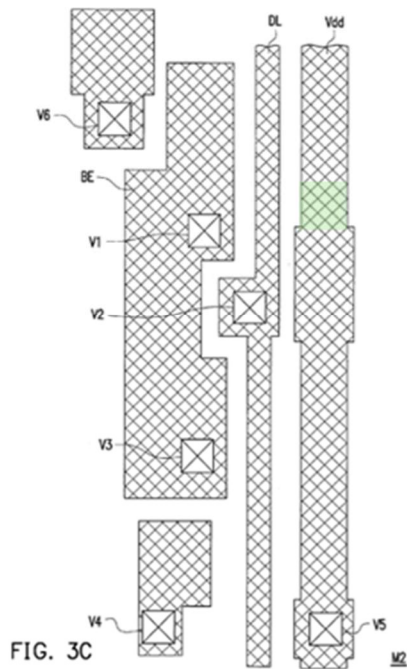


FIG. 3C

M2

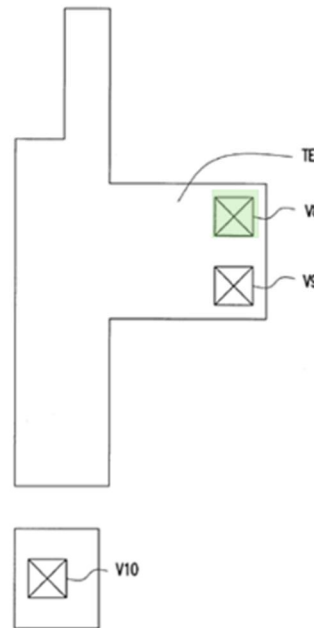


FIG. 3D

M3

Liu, FIGS. 3A-3D.

93. Referring to the pixel structure in Figure 2, the above figure illustrates the separate layers that include FIG. 3A showing a semiconductor layer, FIG. 3B showing a first conductive layer, FIG. 3C showing a second conductive layer, and FIG. 3D showing a third conductive layer. Liu, ¶¶14-18.

94. The semiconductor layer PO has a source region S5, a drain region D5 and a channel region CH5 in a region predetermined for forming a fifth thin film transistor T5. *Id.*, ¶35. The first conductive layer M1 has a gate G5 in the region predetermined for forming the fifth thin film transistor T5, and the light emitting signal line EM is electrically connected to the gate G5. *Id.*, ¶¶37, 64.

95. Figures 3A and 3B have been annotated (in yellow highlighting) to show the location of transistor T5 on the semiconductor layer and the location on the light emitting signal line EM in the first conductive layer (or first metal layer M1) that corresponds to the gate G5, respectively. Gate G5 being coincident with signal line EM (both on first metal layer M1) is consistent with gate G5 and EM being electrically connected as also shown in Figure 1 (in which this same connection is also highlighted in yellow). Furthermore, the yellow highlighted portion on M1 (with gate G5) is directly above the channel region of transistor T5 on the semiconductor layer PO.

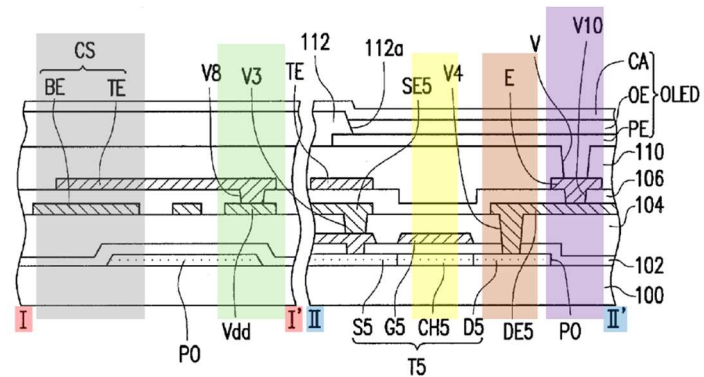
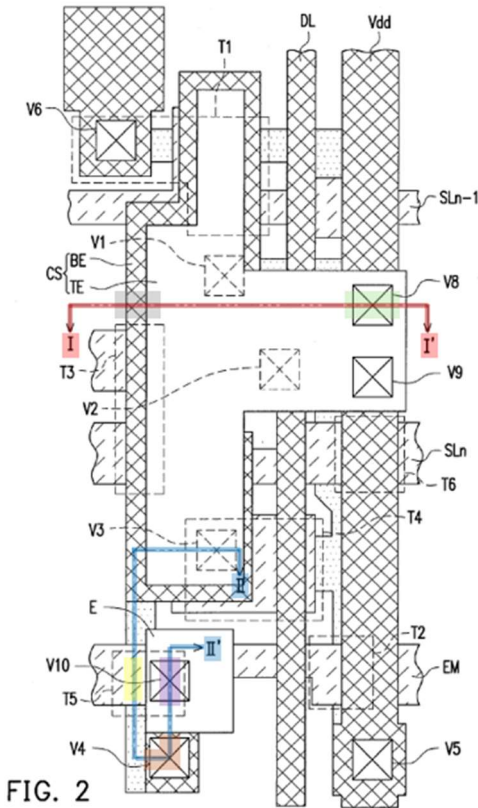
96. The second conductive layer M2 comprises a power line Vdd and the

third conductive layer M3 includes a top electrode TE of the capacitor CS. Liu, ¶¶42, 44. Furthermore, the top electrode TE is electrically connected to the power line Vdd through contact via structures V8~V9. *Id.*, ¶44.

97. Figures 3C and 3D have been annotated (in green highlighting) to show the location on Vdd on the second conductive layer (or second metal layer M2) and the location on the top electrode (TE) on the third conductive layer (or third metal layer M3), respectively, that are vertically overlapping on the plan (or layout) view and are electrically connected through contact via structure V8, as also shown in Figure 1 (in which this same connection is also highlighted in green).

3. Cross-Sectional Views

98. A cross-sectional view provides a vertical “slice” through the integrated circuit along a cross-sectional (or “cut”) line that shows the stacking and composition of various layers, e.g., polysilicon (PO) and metal (M1, M2, M3), which provides details about the fabrication process, e.g., isolation techniques. Liu further provides Figure 6, which is a schematic diagram (or cross-sectional view) showing the formation of an OLED on the pixel structure depicted in Figure 2. Liu, ¶21.



Left: Liu, FIG. 2 (annotated); Right: Liu, FIG. 6 (annotated).

99. Specifically, the cross-sections of the integrated circuit along the cross-sectional line I-I' (highlighted in red in Figure 2 above) and the cross-sectional line II-II' (highlighted in blue in Figure 2 above) are illustrated in Figure 6. Both Figures 2 and 6 have been annotated with different colors to show the corresponding portions across both figures. In an example, “gray” and “green” sections are highlighted along the (red) cross-sectional line I-I' (with the green highlighted section corresponding to TE being electrically connected to the power line Vdd). In another example, “yellow”, “peach” and “purple” sections are highlighted along the (blue) cross-

sectional line II-II' (with the yellow highlighted section corresponding to the gate G5 being above the channel region CH5 in transistor T5).

100. Referring to annotated Figures 2 and 6, the gray-highlighted portion shows the overlapping top electrode TE and bottom electrode BE of the storage capacitor CS (see Liu, ¶47), the peach-highlighted portion shows contact via structure V4 connecting the drain electrode DE5 (in the second conductive layer M2) being electrically connected to the drain region D5 (in the semiconductor layer PO) (see *Id.*, ¶40), and the purple-highlighted portion shows the conductive pattern E being electrically connected to the drain electrode DE5 through a contact via structure V10 (see *Id.*, ¶44).

VII. CLAIM CONSTRUCTION

101. It is my understanding that in order to properly evaluate the Challenged Patents, the terms of the claims must first be interpreted. It is my understanding that for the purposes of this inter partes review, the claims are to be construed under the so-called Phillips standard, under which claim terms are given their ordinary and customary meaning as would have been understood by one of ordinary skill in the art in light of the specification and prosecution history, unless the inventor has set forth a special meaning for a term. For the purposes of this declaration, I have given all the claim terms of the Challenged Claims their plain and ordinary meaning, as would have been understood by a person of ordinary skill in the art, at the time of

the alleged invention, which I have been asked to assume August 2, 2012, for all claims.

VIII. CLAIMS 1-30 ARE UNPATENTABLE

102. I have been asked to provide my opinion as to whether the Challenged Claims of the '990 Patent would have been obvious in view of the prior art. The discussion below provides a detailed analysis of how the prior art references identified below teach the limitations of the Challenged Claims of the '990 Patent.

103. As part of my analysis, I have considered the scope and content of the prior art and any differences between the alleged invention and the prior art. I describe in detail below the scope and content of the prior art, as well as any differences between the alleged invention and the prior art, on an element by element basis for each Challenged Claims of the '990 Patent. As described in detail below, the alleged invention of the Challenged Claims would have been obvious in view of the teachings of the identified prior art references as well as the knowledge of a POSITA.

Grounds	Claim(s)	Basis
1A	1-7, 9, 10, and 23-30	Liu, Udagawa
1B	8	Liu, Udagawa, Nakayama
1C	11-19, 21, and 22	Liu, Udagawa, Chung
1D	20	Liu, Udagawa, Chung, Nakayama
2A	1-10, 21-30	Noguchi-I, Udagawa
2B	11-22	Noguchi-I, Udagawa, Noguchi-II, Jeong
2C	1-30	Noguchi-I, Udagawa, Noguchi-II, Jeong, Kim

A. Ground 1A: Claims 1-7, 9, 10, and 23-30 are Unpatentable over Liu and Udagawa

1. Summary of Liu

104. Liu (Ex. 1005) discloses a pixel structure for an organic electroluminescence display comprising six thin film transistors and one capacitor (6T1C) is disclosed. Liu, ¶32. Compared to conventional 6T1C implementations, the disclosed pixel structure in Liu implements the capacitor CS using three conductive layers, which maintains a predetermined storage capacitance and results in a 20-30% reduction in the overall area of the pixel structure (compared to conventional 6T1C implementations). *Id.*, ¶¶47, 72.

105. In my opinion, Liu is analogous art to the '990 Patent because both Liu and the '990 patent are in the same field of endeavor. Both are directed to the pixel structure of an OLED display that is driven by the cooperation of multiple TFTs and a capacitor. *Id.*, ¶6. Similarly, both endeavor to reduce an area occupied by components of the pixel structure. *Id.*, ¶7.

106. Liu teaches a pixel structure disposed on a substrate 100 and comprising a semiconductor layer PO, a first insulating layer 102, a first conductive layer M1, a second insulating layer 104, a second conductive layer M2, a third insulating layer 106, a third conductive layer M3, and a pixel electrode PE. *Id.*, ¶32. Herein, the semiconductor layer PO mainly comprises channel regions, source regions and drain

regions of the six TFTs (denoted T1 through T6). *Id.*, ¶34. The first conductive layer M1, which is disposed on the first insulating layer 102, includes the gates of TFTs T1-T4 and T6, as well as scan lines SL_n and SL_n-1, a light emitting signal line EM, and a reference signal line RL. *Id.*, ¶¶37-38. The second conductive layer M2, which is disposed on the second insulating layer 104, includes the source electrodes and the drain electrodes of the six TFTs T1-T6, and the bottom electrode (BE) of the capacitor. *Id.*, ¶40. The third conductive layer M3, which is disposed on the third insulating layer 106, includes a conductive pattern (which is used to connect the pixel electrode to various electrodes of the TFTs) and the top electrode (TE) of the capacitor. *Id.*, ¶¶44-46.

2. Summary of Udagawa

107. Udagawa (Ex. 1006) discloses that the channel of the TFT has a length that is orders of magnitude longer than that of a channel of a conventional TFT, which lowers the dispersion in the electric current value of the TFT and enables the TFT to be turned to an on-state at a particularly higher gate voltage. Udagawa, ¶¶19, 23.

108. In my opinion, Udagawa is analogous art to the '990 Patent because it is in the same field of endeavor. Both are directed to displaying an image by using a plurality of TFTs in each pixel with the TFT(s) controlling the current amount flowing through the OLED. Udagawa, ¶¶8-9. Similarly, both the '990 patent and

Udagawa describe using polysilicon film to form the TFT, with the pixels and driving circuits being formed integrally over the same substrate, thereby reducing the number of connecting terminals and reducing the periphery of the pixel portion. *Id.*, ¶10.

109. Udagawa teaches that a TFT supplying an electric current to an OLED has a channel length that is much longer, specifically, several tens of to several hundreds of times longer than that of the related art, so that the TFT may be turned to an on-state at a gate voltage much higher than ever to drive and may have low channel conductance *gd.* *Id.*, ¶¶22, 26. Furthermore, by making the channel conductance (or conductivity of a channel) smaller, even when the OLED may be deteriorated for some reason, the current flowing to the OLED can be maintained at a constant value, resulting in maintaining a constant brightness. *Id.*, ¶¶28, 61.

3. Motivation to combine Liu and Udagawa

110. In my opinion, there are several reasons that motivate the combination of Liu and Udagawa.

111. Both Liu and Udagawa described drive circuits for OLED displays and both sought to improve the design and operation of OLEDs. Notably, Liu's invention focused on providing a design with a reduced-area pixel structure. Liu, ¶¶4, 10, 47, 56, 72. And, Udagawa described drive circuit configurations that improved OLED's reliability, and consequently, its operations and image quality. Udagawa, ¶12.

112. More specifically, Udagawa had recognized small TFTs resulted in unwanted dispersion effects, which was a main reason for display irregularities in a display device. Udagawa, ¶38. Thus, in my opinion, there was a motivation to reduce the dispersion in Liu's TFT drive circuits so that the pixels in the high-resolution display provided a more uniform brightness.

113. Furthermore, there is a motivation to combine Liu with Udagawa, and specifically to use Udagawa's driving TFT with the serpentine channel in Liu's OLED driving circuit because this combination would have conformed to Liu's objectives of reducing the size of the pixel structure; forming the gate channel in this way would allow for both a reduction of characteristics dispersion of each TFT leading to reduction of the brightness variation and a reduced size of the pixel area while enabling an improved operation of the driving TFT.

114. In my opinion, a POSITA would have been skilled enough to use Udagawa's TFT with a longer channel in Liu's OLED driving circuit to achieve the known and predictable result of reducing the characteristic dispersion of the driving TFT. Furthermore, elongating the channel length to reduce dispersion was well-known by 2012, as evidenced by the teachings of Udagawa and other known prior art references, such as Yamazaki, Min, and Lee-2009.

115. Additional details regarding the Liu-Udagawa combination are

provided below in connection with specific claim limitations.

4. Independent Claim 1

a. 1[pre]: “An organic light emitting diode display comprising:”

116. In my opinion, Liu teaches or suggests 1[pre].

117. Liu discloses a “pixel structure” of an organic light emitting diode (“OLED”) in a display using thin film transistors (“TFT”) and a capacitor. Liu, ¶¶3, 6. The “pixel structure **is applied to an organic electroluminescence display** and has a structure comprising six thin film transistors and one capacitor (6T1C),” but it is not limited to the disclosed structure.¹ *Id.*, ¶¶32, 48, 50, 53, 58, 73, 75. Liu further explains the pixel structure includes an OLED. Liu, ¶¶48, 58, FIGs. 1, 6.

118. Liu is further directed to reducing the area occupied by the pixel structure for use in high resolution displays. Liu, ¶¶6-7. For example, Liu explains that “[t]he pixel structure of FIG. 6 is a pixel structure **in an organic electroluminescence display.**” *Id.*, ¶50. As explained below, the embodiment shown in Figure 6 maps to the claims.

119. Accordingly, Liu discloses OLED pixel structures utilized in a display (“[a]n organic light emitting diode display”).

¹ All emphases are added unless otherwise noted.

b. 1[a]: “a substrate;”

120. In my opinion, Liu discloses this limitation.

121. Liu discloses “the pixel structure is disposed on a **substrate 100** and comprises a semiconductor layer PO, a first insulating layer 102, a first conductive layer[] M1[,] a second insulating layer 104, a second conductive layer M2, a third insulating layer 106, a third conductive layer M3, and a pixel electrode PE.” Liu, ¶32, FIG. 5 (annotated below). Liu explains the substrate may be made of glass, quartz, polymers, or ceramics, among other materials. *Id.*, ¶33.

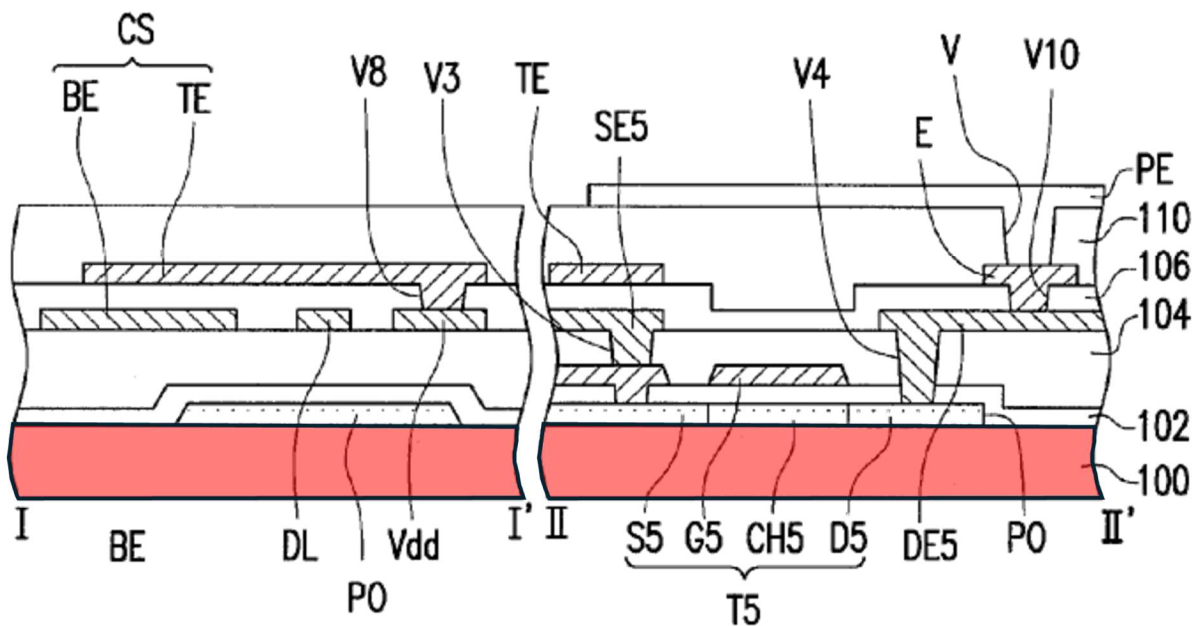


FIG. 5

Liu, FIG. 5 (annotated).

c. 1[b]: “a first voltage line;”

122. In my opinion, Liu discloses this limitation.

123. Liu discloses the “first voltage line” as a “power line Vdd” in the second metal layer M2. Liu, ¶42, FIG. 1 (annotated below). In my opinion, a POSITA would have understood Vdd is a “voltage line” because Vdd is common notation to denote a voltage to drive a transistor. Moreover, the '990 Patent uses the same notation, Vdd, to identify a “voltage line.” '990Pat, 6:25-37 (“a driving voltage line 172 for transferring a driving voltage ELVDD.”).

124. Figure 1 shows “a schematic circuit diagram of a pixel structure.” Liu, ¶31. Annotated Figure 1 of Liu has been reproduced above Figure 1 of the '990 Patent to show the similarities between the circuits and to show Vdd.

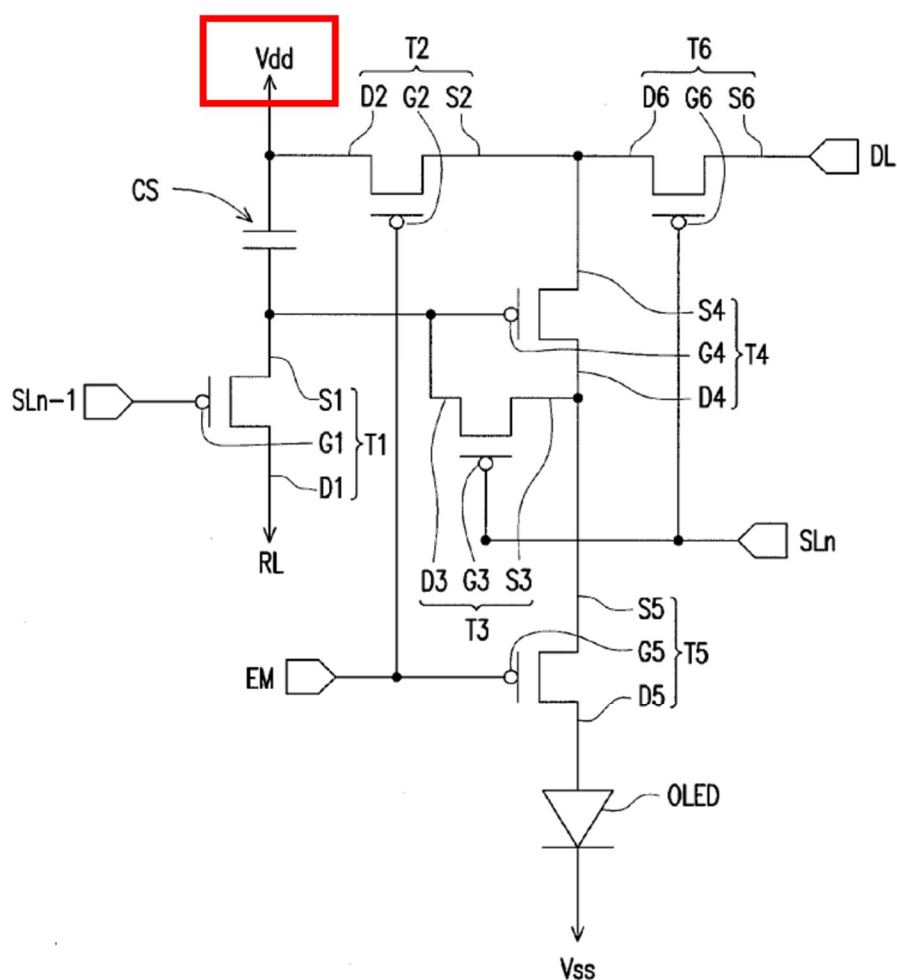
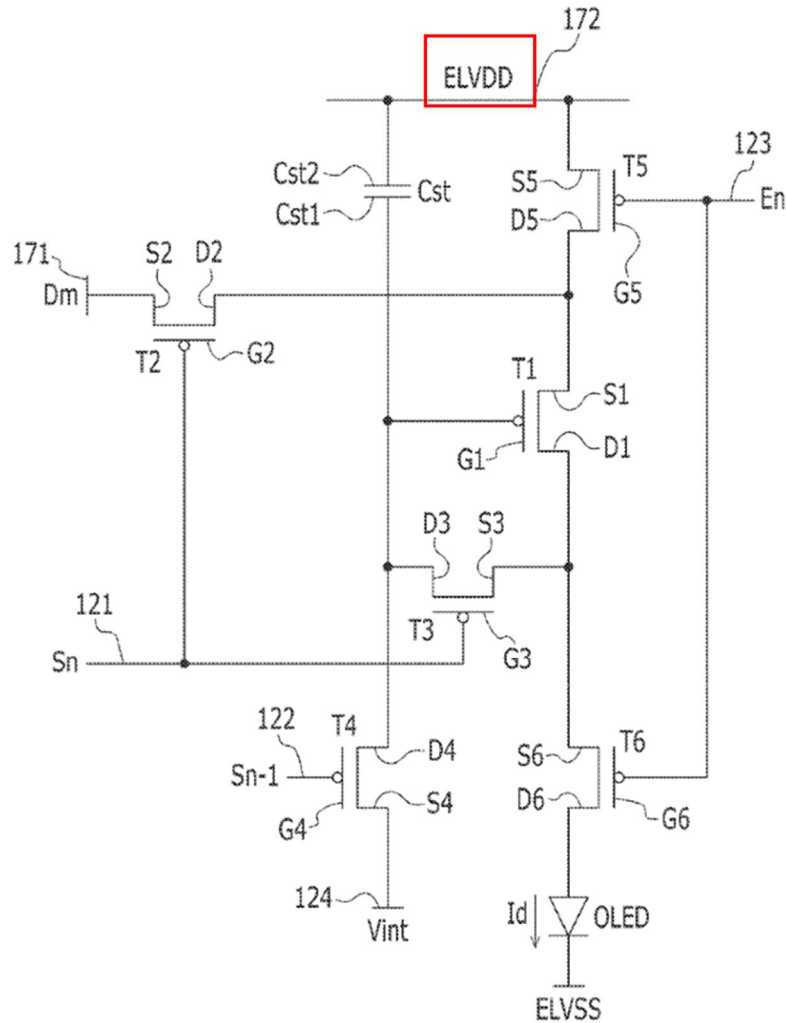


FIG. 1

Liu, FIG. 1 (annotated).

FIG. 1



'990Pat., FIG. 1 (annotated).

125. In addition, the table below has been provided to cross-reference each transistor and signal line of '990 Patent to the similarly-described elements in the disclosure of Liu.

Claim 1	'990	Liu	Function
1 st TFT	T2	T6	Data input switching TFT

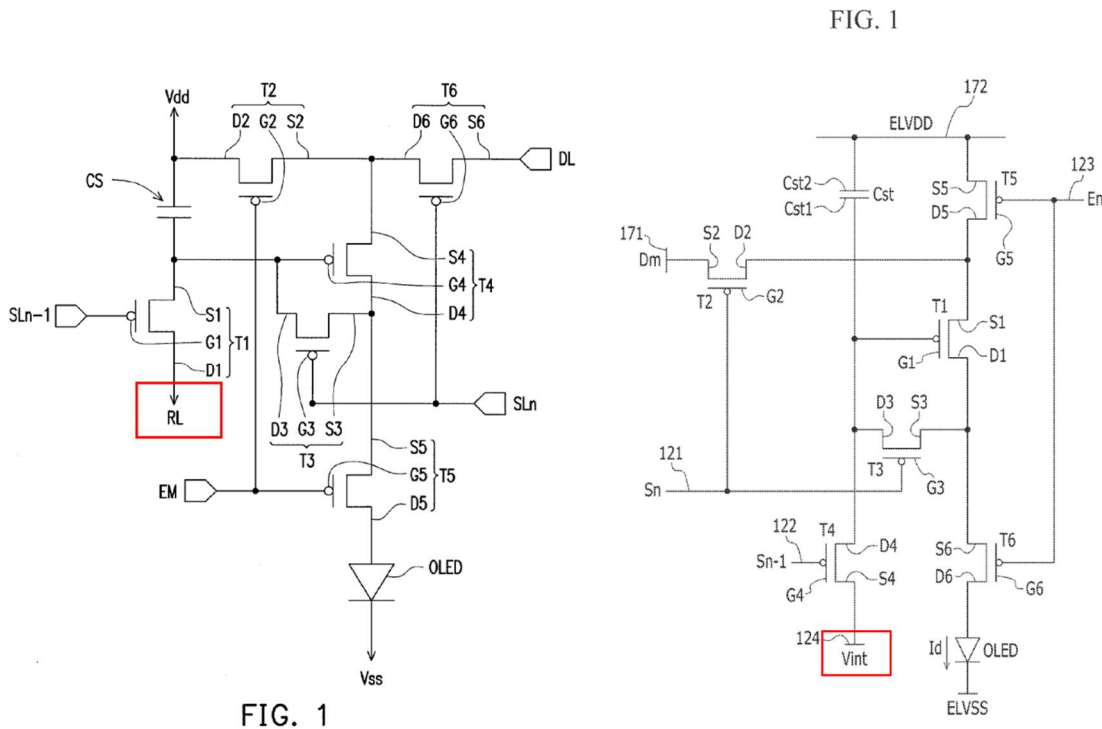
2 nd TFT	T1	T4	Driving TFT
3 rd TFT	T3	T3	Scan[n] / Compensation TFT
4 th TFT	T5	T2	Power supply / Operation control TFT
5 th TFT	T6	T5	Light emission control TFT
6 th TFT	T4	T1	Scan[n-1] / Init switch TFT
Capacitor	Cst	CS	Storage capacitor
First Capacitor Plate	125h	BE	
Second Capacitor Plate	127	TE	
1 st Voltage line	ELVDD	Vdd	Power supply
2 nd Voltage line	Vint	RL	Capacitor initialization voltage
OLED	OLED	OLED	
1 st Scan line	Sn	SLn	Current scan line
2 nd Scan line	Sn-1	SLn-1	Previous scan line
Light emission control line	En	EM	Light emission control
Data line	Dm	DL	Data/OLED intensity voltage

d. 1[c]: “a second voltage line;”

126. In my opinion, Liu discloses this limitation.

127. Liu discloses the “second voltage line” as a reference signal line “RL” that may be formed in the first metal layer M1. Liu, ¶38, FIG. 1 (annotated below). In my opinion, a POSITA would have understood the reference signal line, RL, is also a “voltage line” because “signal line” is common terminology for circuit components that transmit voltages in transistor circuits; in addition, Liu’s Figure 1 uses the same circuit symbol to represent the voltage lines Vss, Vdd, and RL, further corroborating RL’s role as a voltage line. Moreover, RL corresponds to Vint in

the '990 Patent, described as “initialization voltage line 124.” '990Pat, '990Pat, 6:25-37 (“an initialization voltage line 124 for transferring an initialization voltage Vint for initializing the driving thin film transistor T1”). Annotated Figure 1 of Liu has been reproduced alongside Figure 1 of the '990 Patent to show RL and Vint.



Left: Liu, FIG. 1 (annotated); Right: '990Pat., FIG. 1 (annotated).

e. 1[d]: “a plurality of pixels, each of the pixels comprising an organic light emitting diode;”

128. In my opinion, Liu teaches or suggests this limitation, and Udagawa confirms the teachings of Liu regarding the presence of multiple pixels in the display device.

129. As explained above in 1[pre], Liu discloses a pixel structure for use in

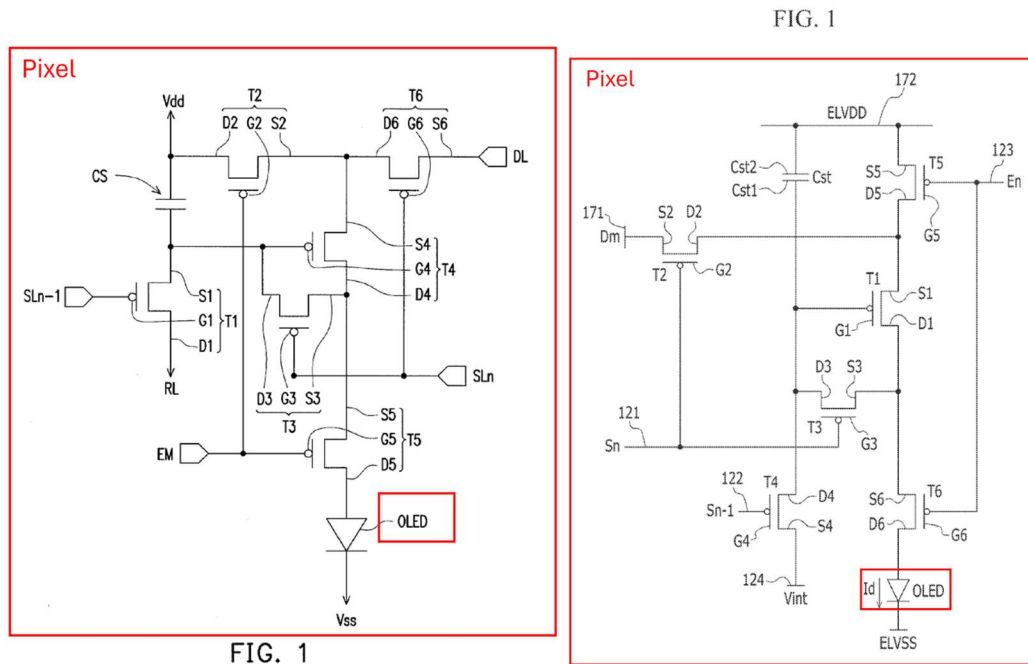
an OLED display. *See* ¶¶116-119. Each pixel structure includes TFTs, capacitor, and OLED. *Id.* Thus, Liu’s pixel structure constitutes one pixel in a display. Liu, ¶50. For example, as explained in Udagawa, pixels comprise the TFT driving circuits and OLEDs. Udagawa, ¶¶5-8.

130. Liu explains the pixel structure is limited in size and must be small for high resolution displays. Liu, ¶¶6-7. In my opinion, a POSITA would have understood that high resolution displays contain a plurality of pixel structures because each pixel structure containing an OLED makes up one light emitting portion (i.e., pixel) of the display, and the resolution is measured according to the number of pixels occupying the display area. Furthermore, the ’990 Patent admits and confirms a POSITA’s understanding that an “organic light emitting diode display includes a plurality of pixels, each including an organic light emitting diode that is a self-light emitting element, and a plurality of thin film transistors and capacitors for driving the organic light emitting diode.” ’990 Patent, 1:45-49.

131. Moreover, Liu discloses scan lines (SL_n and SL_{n-1}) in the TFT circuit. Liu, ¶38; ¶125 (table). Notably, Liu references these scan lines with the nomenclature “n” and “n-1” signifying a plurality of scan lines, not limited to the two shown in the circuit. Thus, in my opinion, a POSITA would have understood that Liu’s circuit (Figure 1-6) represents one of a plurality of pixel structures, all

used in the disclosed display.

132. Annotated Figure 1 of Liu has been reproduced alongside Figure 1 of the '990 Patent to show a pixel and the position of the OLED.



Left: Liu, FIG. 1 (annotated); Right: '990Pat., FIG. 1 (annotated).

133. Accordingly, as shown below in annotated Figure 1, Liu discloses “a plurality of pixels, each of the pixels comprising an organic light emitting diode.”

f. 1[e]: “a plurality of driving circuits on the substrate, each of the organic light emitting diodes being electrically coupled to a respective driving circuit;”

134. In my opinion, Liu teaches or suggests this limitation.

135. As explained above in 1[d], Liu teaches or suggests multiple pixel structures (i.e., pixels) in a display. See ¶¶128-133. Liu further describes a “plurality

of driving circuits” because it describes a driving circuit for each of the plurality of pixels, where each driving circuit comprises a plurality of TFTs to drive the OLED for that pixel. Liu, ¶¶6 (“A pixel structure of the organic light emitting device in the display is usually driven by the cooperation of a plurality of thin film transistors (TFTs) and a capacitor.”), 8, FIG. 1. Furthermore, the ’990 Patent admits a “plurality of thin film transistors and capacitors...driv[e] the organic light emitting diode.” ’990 Patent, 1:45-49.

136. As shown below, each of the TFT driving circuits is connected to an OLED (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). *Id.*, ¶31, FIG. 1 (annotated). Annotated Figure 1 of Liu has been reproduced alongside Figure 1 of the ’990 Patent to show the relationship of a pixel and driving circuit.

FIG. 1

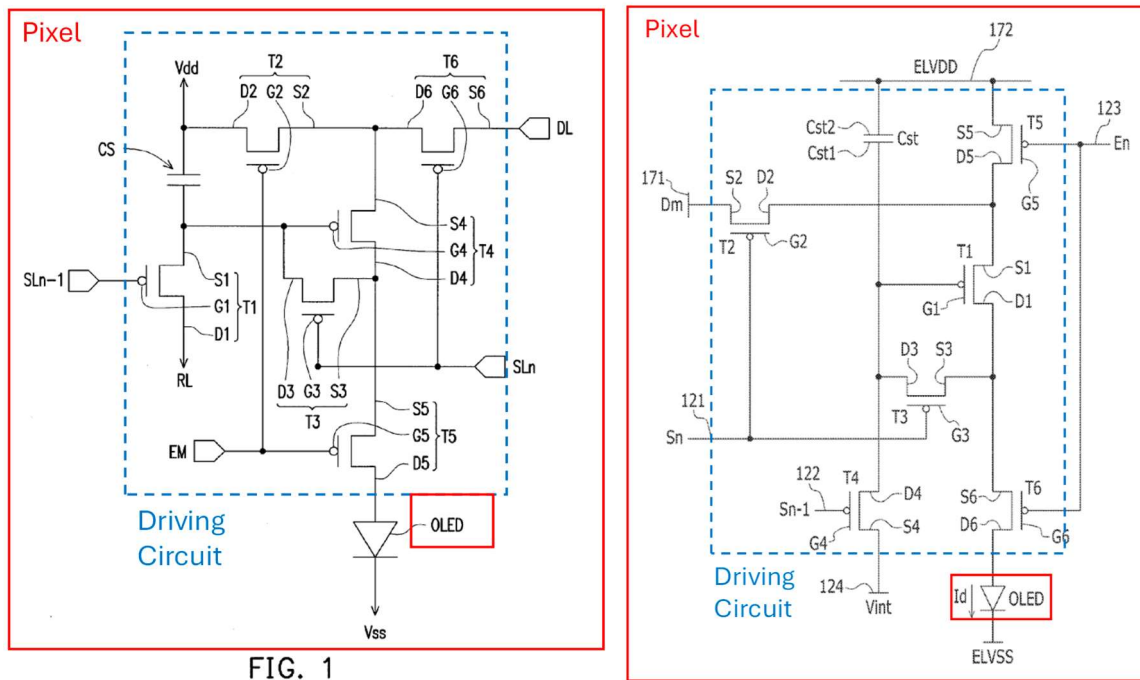


FIG. 1

Left: Liu, FIG. 1 (annotated); Right: '990Pat., FIG. 1 (annotated).

137. Liu explains that the TFTs are formed in a semiconductor layer that is formed on the substrate (“a plurality of driving circuits on the substrate”). *Id.*, ¶¶8, 34-35, FIGs. 1-6. The substrate is shown in annotated Figure 5 in 1[a]. *See* ¶121. Liu further explains that “the pixel structure is disposed on a substrate 100 and comprises a semiconductor layer PO” and that the substrate can be a “wafer.” Liu, ¶¶8, 33. In my opinion, a POSITA would have thus understood that the plurality of Liu’s driving circuits would have been formed on a single substrate because it was common practice at the time to use a single substrate (e.g. backplane or wafer) to fabricate a display comprising multiple pixels—without pixels there is no display.

138. Furthermore, as shown in annotated Figure 6 below, the OLED is directly connected to T5 (part of the “driving circuit”) through DE5, V10, and V (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). Liu, ¶¶44-48, FIG. 6 (annotated).

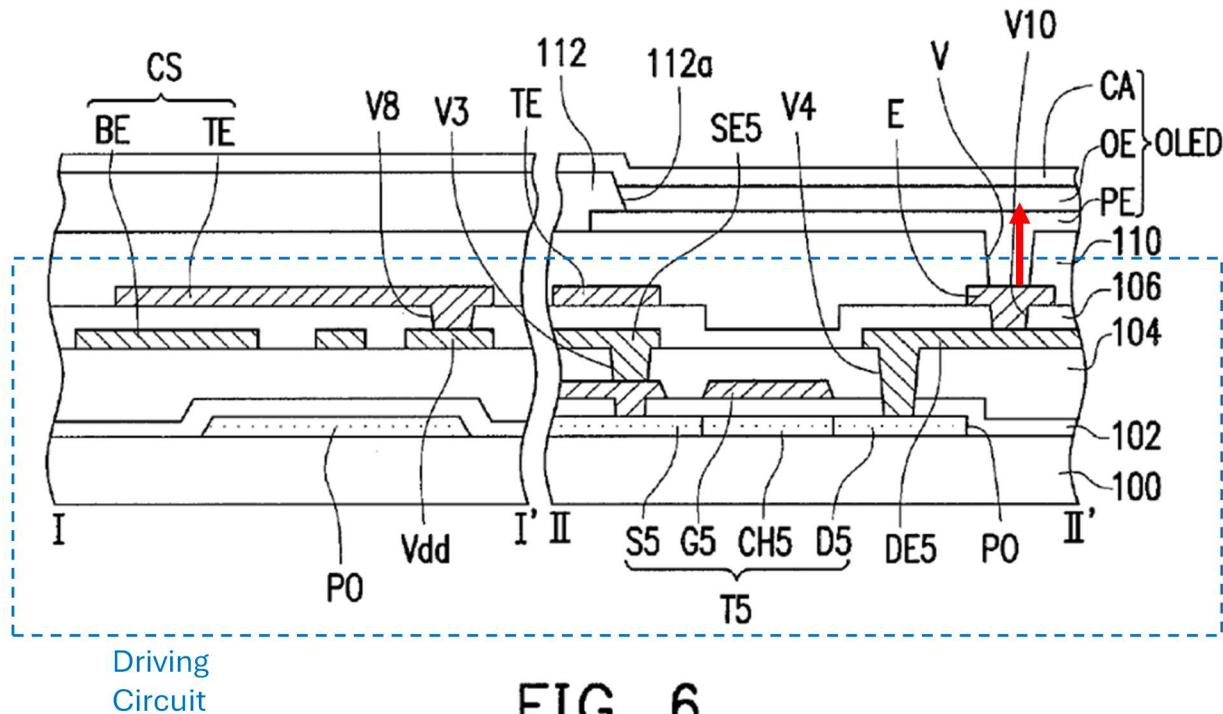


FIG. 6

Liu, FIG. 6 (annotated).

- g. 1[f]: “wherein each of the driving circuits comprises: a first thin film transistor coupled to a first scan line and a data line;”

139. In my opinion, Liu teaches or suggests this limitation.

140. Liu discloses the “first thin film transistor” as T6 that is coupled to “the

first scan line,” SL_n, and “a data line,” DL, as shown in Liu’s Figure 1. Liu, ¶¶38, 42. As explained in 1[e], each pixel structure includes several TFTs arranged in a driving circuit. *See* ¶¶134-138. Referring to the circuit diagram below, Liu explains that a data line “is electrically connected to the source region S6” of T6 (“first thin film transistor”), and scan line SL_n is connected to the gate G6 of T6. *Id.*, ¶38, FIG. 1 (annotated).

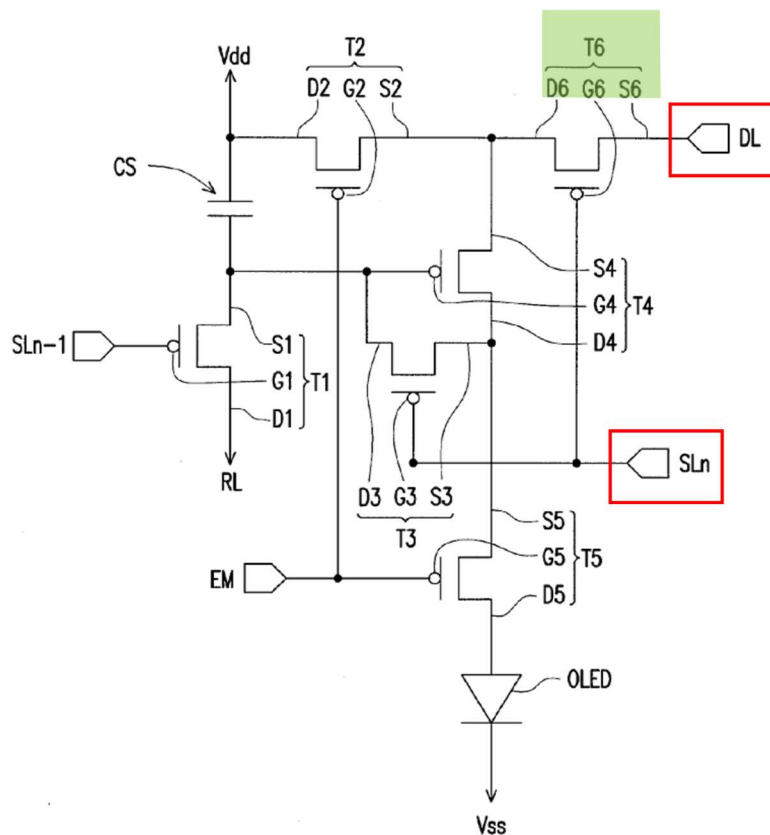


FIG. 1

Liu, FIG. 1 (annotated).

141. Furthermore, as will be explained below, Liu discloses each of the six transistors and capacitor recited in 1[g]-1[m]. The table in 1[b] above shows the

mapping of Liu's circuit components to those recited in the '990. *See* ¶125 (table).

- h. 1[g]: “a second thin film transistor utilizing a semiconductor layer and electrically coupled to the first voltage line, the corresponding organic light emitting diode, and the first thin film transistor, the semiconductor layer being extended to and electrically coupled to the first thin film transistor;”**

142. In my opinion, Liu teaches or suggests limitation 1[g].

143. As shown in Liu's Figure 1 circuit, Liu discloses the “second thin film transistor” as TFT T4, which is electrically coupled to “the first voltage line,” Vdd, through TFT T2. Liu's T4 is electrically coupled to the “corresponding organic light emitting diode,” OLED, through TFT T5, and is electrically coupled to the “first thin film transistor,” TFT T6, through a direct connection between S4 (source of T4) and D6 (drain of T6). *See* Liu, FIG. 1.

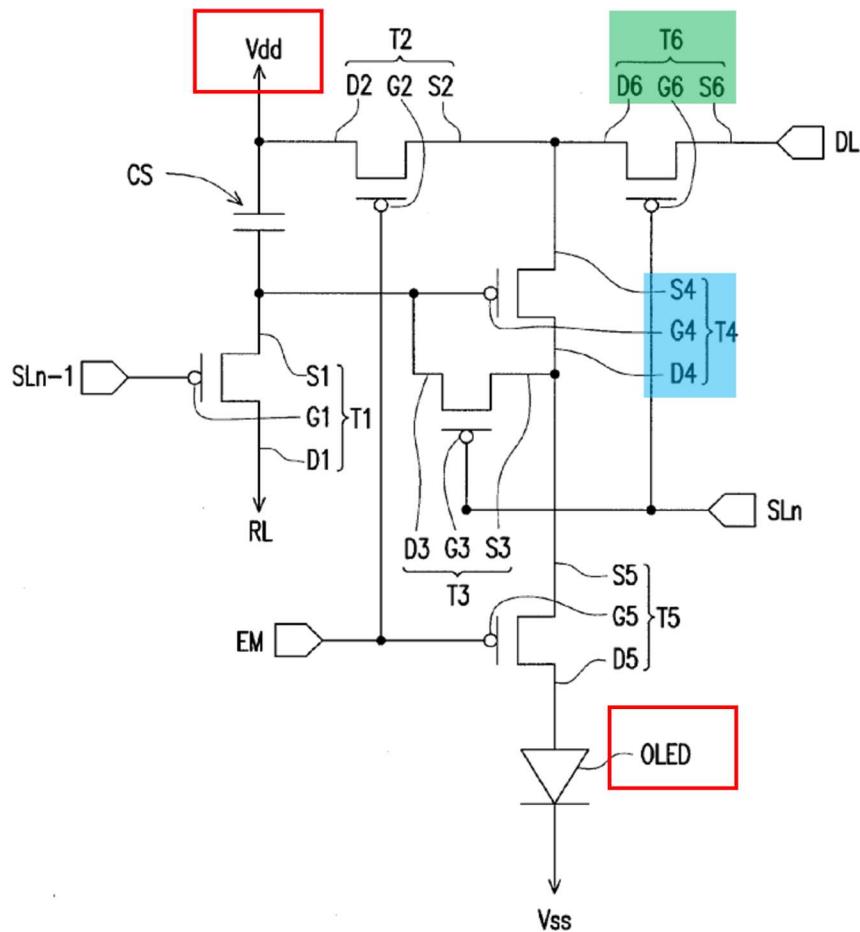
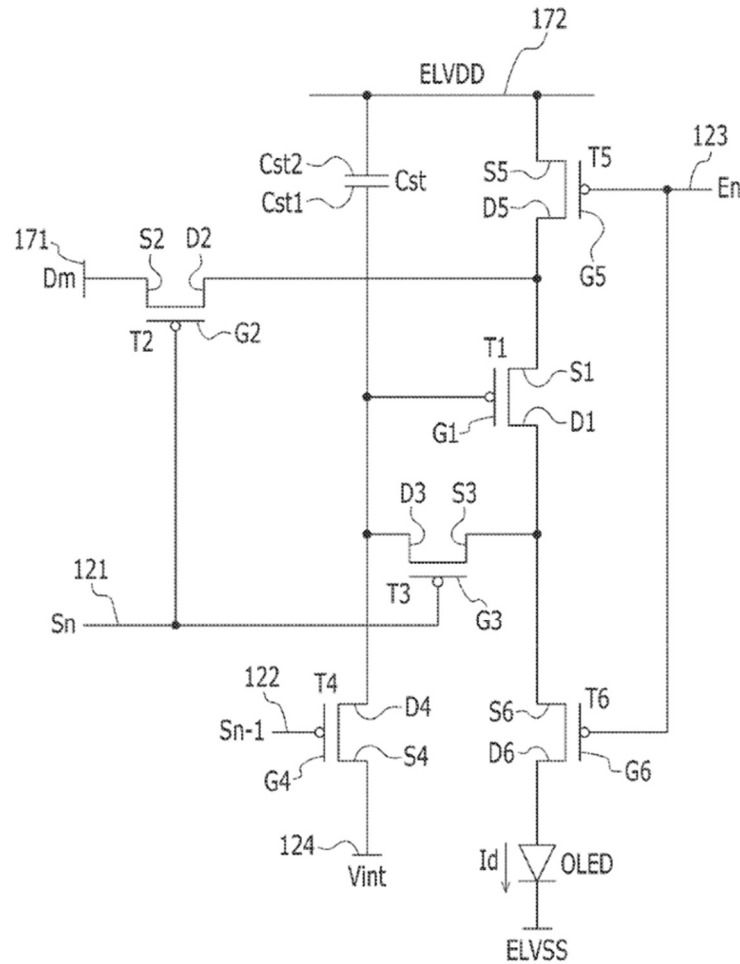


FIG. 1

Liu, FIG. 1 (annotated).

144. The above characterization of Liu’s TFT T4 being “electrically coupled” to the OLED and Vdd through intervening TFTs is consistent with the ’990 patent’s Figure 1 connectivity and its detailed description, which explains, e.g., “T1 is coupled via the operation control thin film transistor T5 to the driving voltage line” and “T1 is electrically coupled via the light emission control thin film transistor T6 to an anode of the OLED.” See ’990Pat., 6:38-45, FIG. 1.

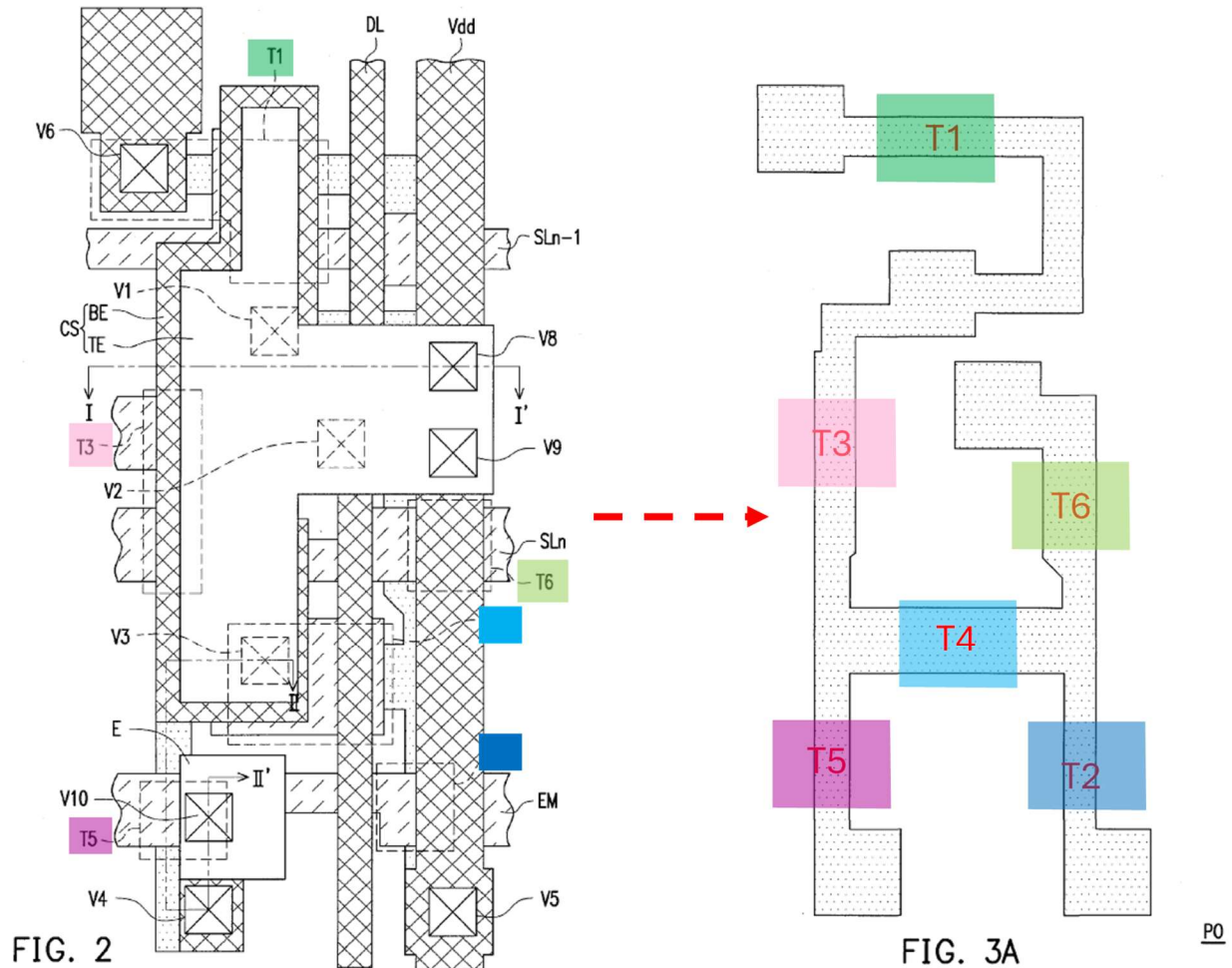
FIG. 1



'990 patent, FIG. 1.

145. Liu additionally discloses that T4 (“the second thin film transistor”) is included in a portion of the semiconductor layer (“utilizes a semiconductor layer”). Notably, Liu’s Figure 3A is “a top view showing a semiconductor layer of the pixel structure” (Liu, ¶[0015]), which has been annotated based on Liu’s Figure 2 (and other figures of Liu) to show the approximate locations of the various TFTs over the

depicted semiconductor pattern. *See, e.g.,* Liu, FIG. 2 (annotated below).



Left: Liu, FIG. 2 (annotated); Right: Liu, FIG. 3A (annotated).

146. As discussed in Section VI.C, the location of T5 annotated in FIG. 3A is determined based on the plan view in FIG. 3B (showing the first conductive layer M1) and the disclosure that the first conductive layer M1 has a gate G5 in the region predetermined for forming the fifth thin film transistor T5, and the light emitting signal line EM is electrically connected to the gate G5. Liu, ¶¶37, 64.

147. Similarly, and using the principles discussed in Section VI.C, the location of each the other TFTs annotated in FIG. 3A can be determined based on the plan view in FIG. 3B, and specific disclosures in Liu.

148. The location of TFT T1 is determined based on FIG. 3A (showing the semiconductor layer PO) and FIG. 3B (showing the first metal layer M1), and the disclosures that the semiconductor layer PO has a source region S1, a drain region D1 and a channel region (not shown) in a region predetermined for forming a first thin film transistor T1, the first conductive layer M1 has a gate G1 in the region predetermined for forming the first thin film transistor T1, and the scan line SLn-1 is electrically connected to the gate G1. *Id.*, ¶¶35, 38.

149. The location of TFT T2 is determined based on FIG. 3A (showing the semiconductor layer PO) and FIG. 3B (showing the first metal layer M1), and the disclosures that the semiconductor layer PO has a source region S2, a drain region D2 and a channel region (not shown) in a region predetermined for forming a second thin film transistor T2, the first conductive layer M1 has a gate G2 in the region predetermined for forming the second thin film transistor T2, and the light emitting signal line EM is electrically connected to the gate G2. *Id.*, ¶¶35, 38.

150. The location of TFT T3 is determined based on FIG. 3A (showing the semiconductor layer PO) and FIG. 3B (showing the first metal layer M1), and the

disclosures that the semiconductor layer PO has a source region S3, a drain region D3 and a channel region (not shown) in a region predetermined for forming a third thin film transistor T3, the first conductive layer M1 has a gate G3 in the region predetermined for forming the third thin film transistor T3, and the scan line SL_n is electrically connected to the gate G3. *Id.*, ¶¶35, 38.

151. The location of TFT T4 is determined based on FIG. 3A (showing the semiconductor layer PO), FIG. 3B (showing the first metal layer M1) and FIG. 3C (showing the second metal layer M2), and the disclosures that the semiconductor layer PO has a source region S4, a drain region D4 and a channel region (not shown) in a region predetermined for forming a fourth thin film transistor T4, the first conductive layer M1 has a gate G4 in the region predetermined for forming the fourth thin film transistor T4, and the second conductive layer M2 further comprises a bottom electrode BE in a region predetermined for forming a capacitor CS, and the bottom electrode BE is electrically connected to the source region S1, the drain region D3 and the gate G4. *Id.*, ¶¶35, 38, 42.

152. The location of TFT T6 is determined based on FIG. 3A (showing the semiconductor layer PO) and FIG. 3B (showing the first metal layer M1) and the disclosures that the semiconductor layer PO has a source region S6, a drain region D6 and a channel region (not shown) in a region predetermined for forming a sixth

thin film transistor T6, and the first conductive layer M1 has a gate G6 in the region predetermined for forming the sixth thin film transistor T6. *Id.*, ¶¶35, 38.

153. I have further annotated Figure 3 of the '990 Patent to show the positions of the transistors corresponding to the transistors in Liu. As shown, the positions are very similar. I have further annotated a portion of the semiconductor layer in the upper right of FIG. 3 of the '990 Patent with a dashed red box to note that the illustrated portion of the semiconductor layer is part of the pixel to the right of the pixel being shown in this figure. That is, a portion of the semiconductor layer for T4 is part of an adjacent pixel, and specifically, the left-adjacent pixel.

FIG. 3

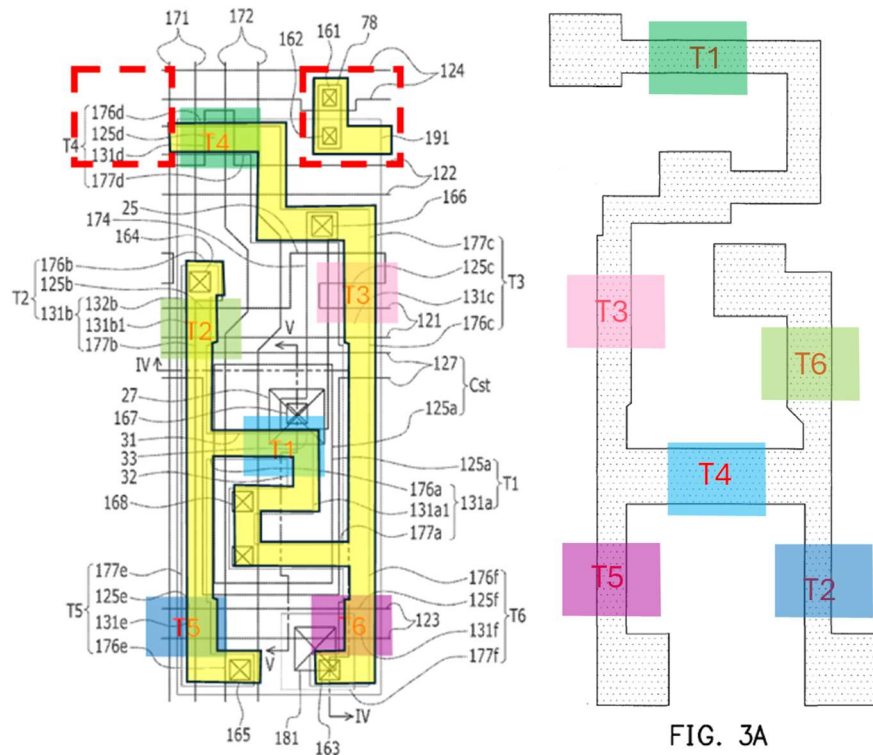


FIG. 3A

PO

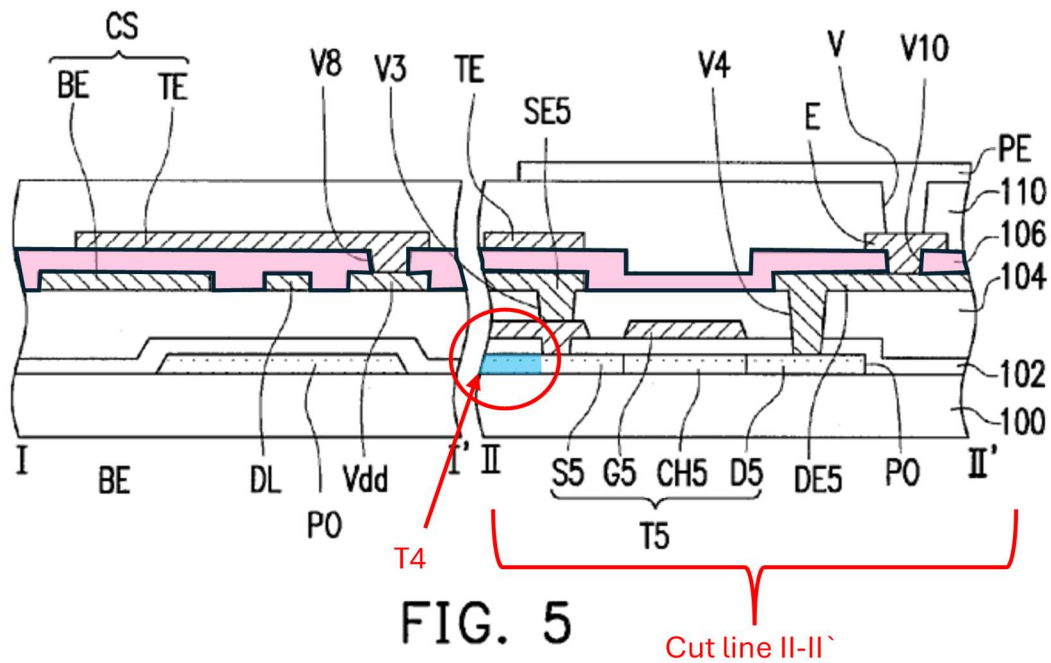
Left: '990Pat., FIG. 3 (annotated); Right: Liu, FIG. 3A (annotated).

154. In my opinion, Liu's Figure 3A and Liu's description that TFT T4 ("the second thin film transistor") includes a section of the semiconductor pattern is evidence of the semiconductor pattern being contiguously laid out in the same layer and extending to the adjacent TFT T6 ("first thin film transistor"). Liu ¶35, FIG. 3A (annotated). Furthermore, TFT T6 ("the first thin film transistor") can be understood as being electrically coupled to the semiconductor layer because it includes a section of the semiconductor pattern, which allows T6 to operate as a transistor.

i. 1[h]: "an insulating layer covering the second thin film transistor;"

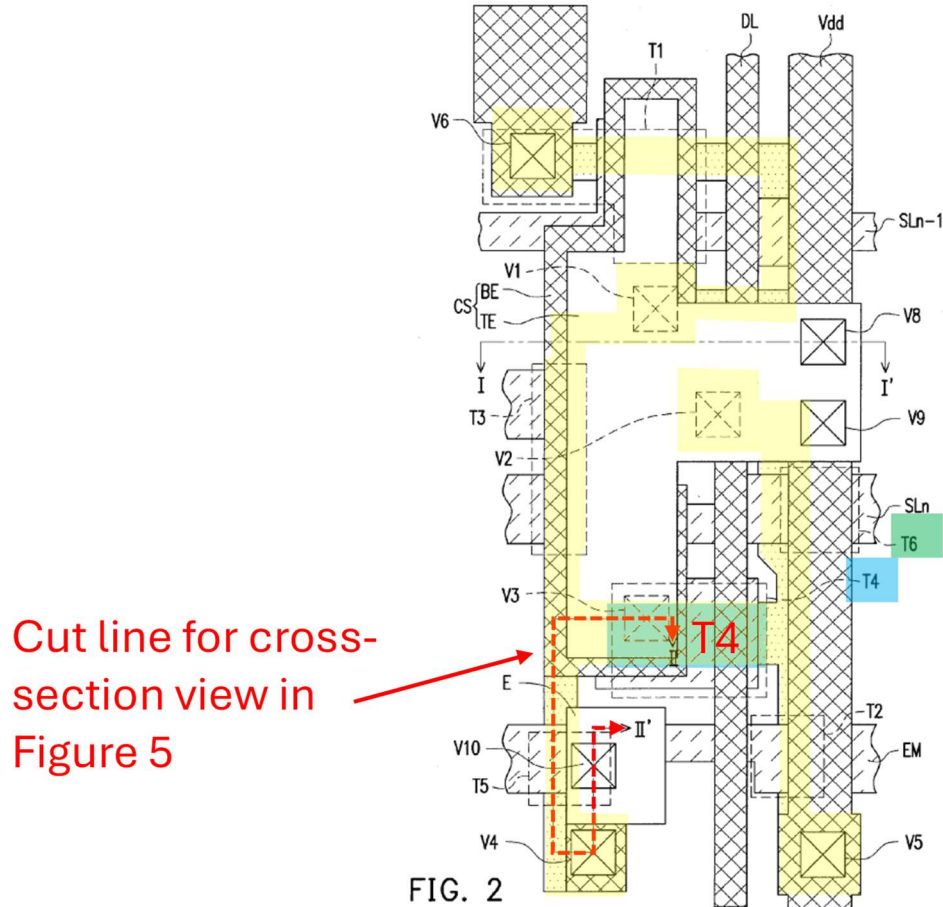
155. In my opinion, Liu teaches or suggests this limitation.

156. Liu discloses **insulating layer 106** "cover[ing] the second conductive layer M2." Liu, ¶¶32, 43. As shown below in annotated Figure 5, insulating layer 106 covers Liu's TFTs. Liu's successive insulating layers are deposited sequentially, and thus layer 106 covers all structures below it, just as layers 104 and 102 also cover all structures below them. Accordingly, Figure 5 discloses that insulating layer 106 specifically covers T4 ("second" TFT).



Liu, FIG. 5 (annotated).

157. In my opinion, this is evident because the cut line II-II' in Figure 2 passes directly through T4 at the (II) end, which is consistent with the annotation of T4 in Figure 5. Figure 2 has been annotated below to identify the semiconductor layer PO (yellow), TFT T6, TFT T4, and the cross-section lines for Figure 5.



Liu, FIG. 2 (annotated).

- j. **1[ia]: “a storage capacitor electrically coupled to a gate electrode of the second thin film transistor, the storage capacitor comprising a first capacitor plate comprising a portion of the gate electrode of the second thin film transistor, a second capacitor plate over the first capacitor plate, and a portion of the insulating layer between the first capacitor plate and the second capacitor plate,**

158. In my opinion, Liu teaches or suggests this limitation.

159. Liu discloses the “storage capacitor” as capacitor CS that is connected

on one side to the gate electrode of T4 (“a gate of the second transistor”), and includes a bottom electrode, BE, (“first capacitor plate”) and top electrode, TE (“second capacitor plate”). *See* Liu, ¶¶42, 44-45, 47, 53, FIGs. 1, 2, 3C, 3D, 4-6.

160. Liu’s capacitor CS is “disposed in the capacitor region CR and includes a bottom electrode BE and a top electrode TE.” Liu, ¶53. Liu explains that because the semiconductor layer is not used as an electrode for the capacitor (i.e., the capacitor plates are in the metal layers), CS “can be disposed overlapping with the semiconductor layer PO, so as to reduce an area occupied by components of the pixel structure.” Liu, ¶47. In other words, even though CS overlaps several of the TFTs (as shown in Figure 2), it does not activate them. Liu further discloses capacitor CS is connected to the gate electrode of T4 (“electrically coupled to a gate electrode of the second thin film transistor”), as shown by the red line in Figure 1. Liu, FIG. 1 (annotated).

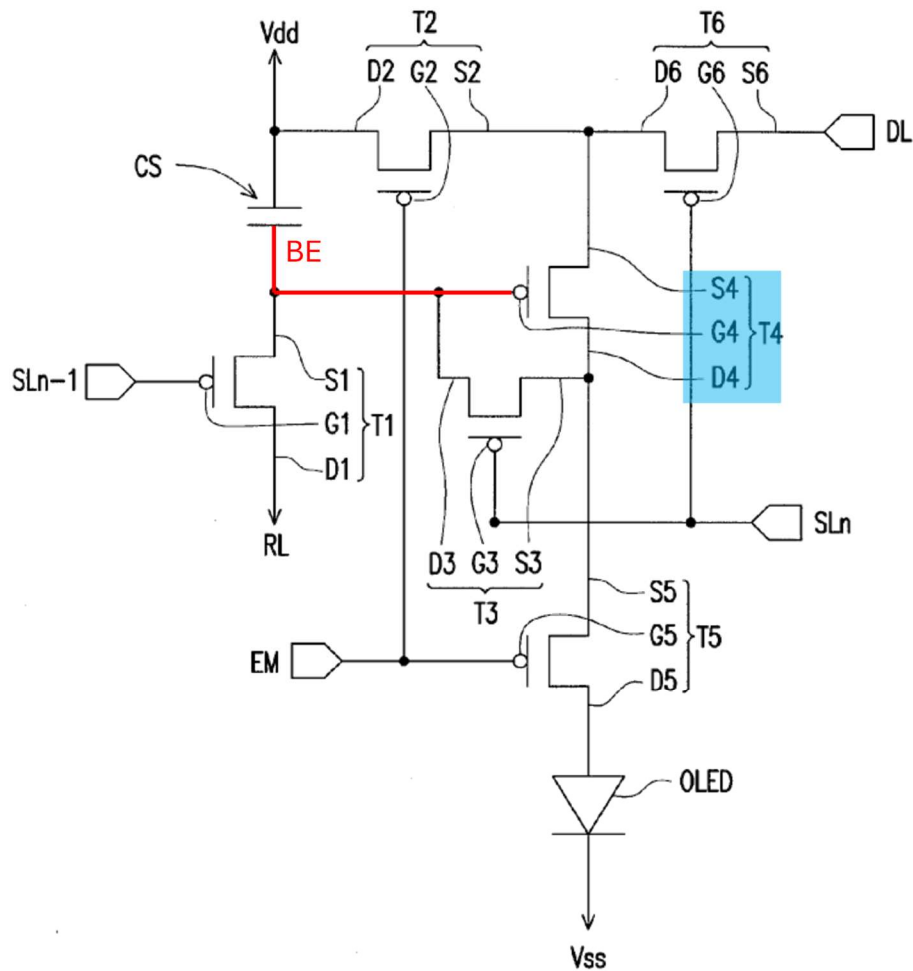


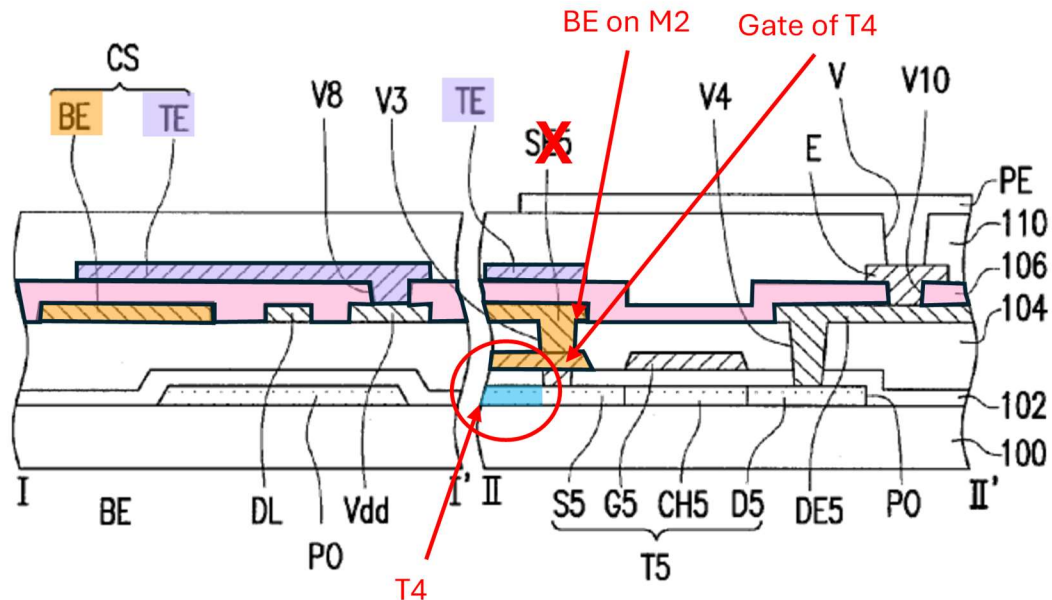
FIG. 1

Liu, FIG. 1 (annotated).

161. As explained above, capacitor CS comprises a **bottom electrode BE** (“a first capacitor plate”) and a **top electrode TE** (“a second capacitor plate”). Liu, ¶53. **Insulating layer 106** is disposed between BE and TE (“a portion of the insulating layer between the first capacitor plate and the second capacitor plate”). *Id.*, FIG. 5 (annotated). Liu further explains that the gate electrode of T4 is below and connected to BE. Liu, ¶¶41, 54. As shown in annotated Figure 5, the gate electrode of T4 that

is on M1 is directly connected to BE on M2 through via V3.² *See also* Liu, ¶¶41, 54, FIGs. 2, 3B, 3C, 3D. In my opinion, a POSITA would have thus recognized that BE comprises a portion of the gate electrode of T4 (“first capacitor plate comprising a portion of the gate electrode of the second thin film transistor”) because the via directly connects the two together, electrically and physically. Noguchi-I is another example of a lower capacitor electrode (or lower capacitor plate) acting as the gate electrode of a driving TFT (see §VIII.A.3.j). Thus, it was well-known to use capacitor electrodes (or capacitor plates) as gate electrodes.

² I note that the nomenclature in Liu uses abbreviations M1 and M2 to denote the first conductive layer and the second conductive layer, respectively; these layers provide electrical conductivity and are made of metal materials. *See* Liu, ¶¶32, 37, 40. A via or a “contact via” is a metal structure that connects one metal component to another metal component in a vertical direction. *See, e.g., Id.*, ¶44.



Liu, FIG. 5 (annotated).

162. With respect to Figure 5, I note that TE and BE are labeled correctly, however, SE5 is labeled incorrectly and should be labeled as BE. In my opinion, the labeling is incorrect because, while SE5 may be mentioned in the specification at paragraph 40, there are no vias or metal shown in Figures 3B-4 that would denote such a structure. In my opinion, in Figure 5, V3 is mislabeled and shown to be SE5, which conflicts with Figure 1 because such an equivalence would connect S5 to G4. But even with these errors in Figure 5, the connection of BE to the gate electrode is clearly shown.

163. Furthermore, the structure labeled as “Gate of T4” (the gate electrode of T4) in annotated Figure 5 above is on the M1 layer and is shown in Figure 3

(unlabeled), and via V3 directly connects the gate electrode of T4 to BE above it. V3 is further shown in Figure 3C, connecting BE to the level below (shown in Figure 3B).

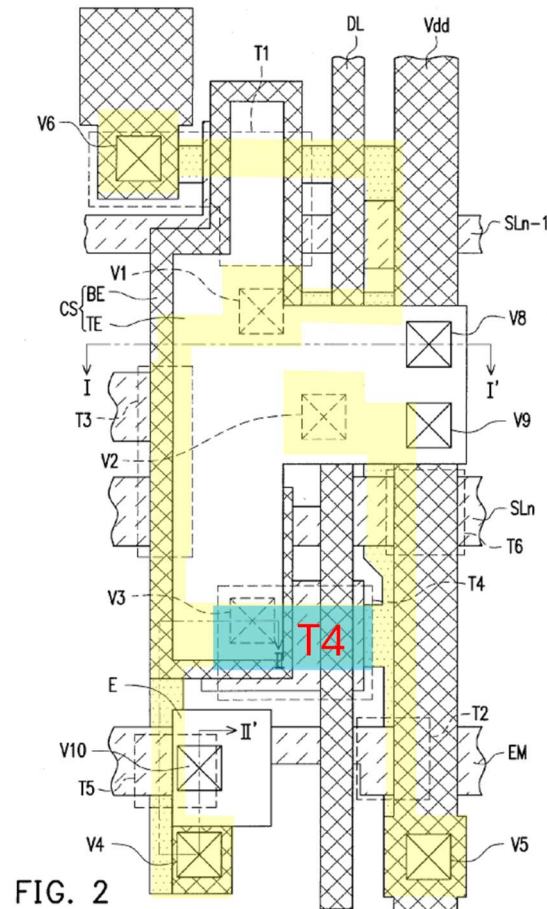
164. To the extent it is argued that the BE does not comprise a portion of the gate electrode of T4, it is obvious, in my opinion, to use BE directly as the gate electrode of T4 based on the teachings of Liu. For example, Liu explains various changes to the capacitor design that include adjusting the capacitor dielectric material or its thickness, allowing the size of the capacitor to be changed while maintaining a selected capacitance. Liu, ¶53. Liu explains that by, e.g., thinning the dielectric or changing the material, the area of CS can be reduced (i.e., the plate areas can be smaller), allowing it to be placed directly over the semiconductor layer: “the semiconductor layer PO may be disposed under the capacitor CS (not shown) to increase the design convenience.” *Id.* Using the capacitor plate directly as the gate electrode is well-known in the art, as shown in Park ’811, Ono, and Kakinuma. Furthermore, if any adjustments were needed to maintain the capacitance value, Liu describes various methods, such as changing the dielectric material and/or dielectric thickness. Liu, ¶53. Thus, it would have been obvious to a POSITA to position the bottom capacitor plate BE (“first capacitor plate”) directly over the semiconductor layer of T4 as taught by Liu (e.g., using the gate electrode of T4 as shown in Figure

3B); such a placement of BE would have made BE to include a portion of the gate electrode of T4. Accordingly, this modification would have been obvious because Liu expressly described it.

165. In my opinion, when moving BE to M1 to be directly over the semiconductor layer, TE may not be correspondingly moved. Moving or not moving TE to M2 is a design choice dependent on factors related to layout. If TE remains in M3, insulating layers 106 and 104 would be designed with the appropriate thickness. However, if TE were moved to M2, such that it was in the metal layer directly above BE, then dielectric layer 104, which also covers all TFTs (*see* 1[h], ¶¶155-157), is the “insulating layer” as claimed.

166. Liu further shows the channel region of T4 is directly under the gate electrode (shown in blue) (“a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor”). Liu, FIG. 2 (annotated). As shown below, Figure 2 has been annotated to show Figure 3A superimposed under it, thereby illustrating the channel of T4 being the region of T4 where M1 crosses it (denoted in blue in figure below). This is a common structure in semiconductor engineering, i.e., the channel of a thin film transistor is the region of the semiconductor layer that lies between the source and drain contacts and is under the gate electrode. Furthermore, it would have been well within the knowledge of a

POSITA to size the gate electrode (e.g., BE) according to the length and width of the channel.



Liu, FIG. 2 (annotated with FIG. 3A underlying it).

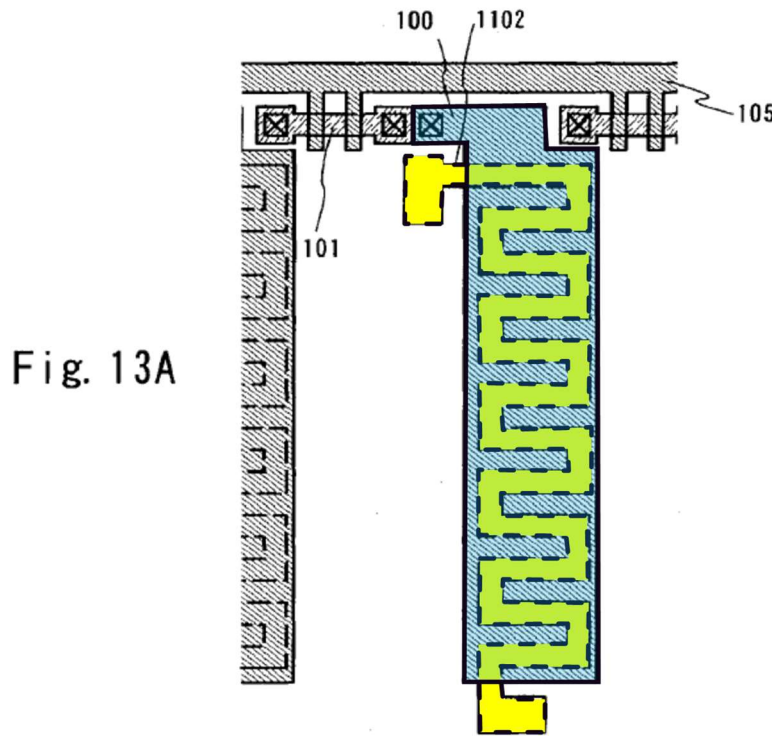
k. 1[ib] a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor being curved ;”

167. In my opinion, Liu in combination with Udagawa teaches or suggests this limitation.

168. Liu does not expressly disclose a “curved” channel portion of T4.

However, in my opinion, it would have been obvious for a POSITA to modify Liu to use Udagawa's serpentine ("curved") gate channel for drive transistor T4. Notably, Liu describes a polysilicon material for implementing its semiconductor layer. Liu, ¶34. It was well-known at the relevant time that the miniaturization of TFT circuits in polysilicon caused problems related to the electrical characteristics of the TFTs. Udagawa, ¶¶5-15. One issue is that dispersion between pixels increases because the channel length of the drive transistor decreases. *Id.*, ¶¶11-13, 16-17. In particular, it was known that dispersion was caused by the driving TFT. *Id.*, ¶17. Thus, in my opinion, a POSITA would have looked to other references, such as Udagawa, to reduce the dispersion effects of polysilicon TFTs in OLED driving circuits.

169. Udagawa discloses that dispersion is reduced "[w]hen the channel length of the TFT that supplies an electric current to the OLED is made longer." Udagawa, ¶22. Accordingly, Udagawa explains that various shapes can be used, such as a "snake" shape, as shown below. *Id.*, ¶31, FIG. 13A (annotated). Annotated below, Udagawa's Figure 13A shows a snake-like (i.e., curved or serpentine) channel 1102 (yellow) with the gate electrode 100 (blue) covering the channel region. Udagawa, ¶¶31, 102, 154.

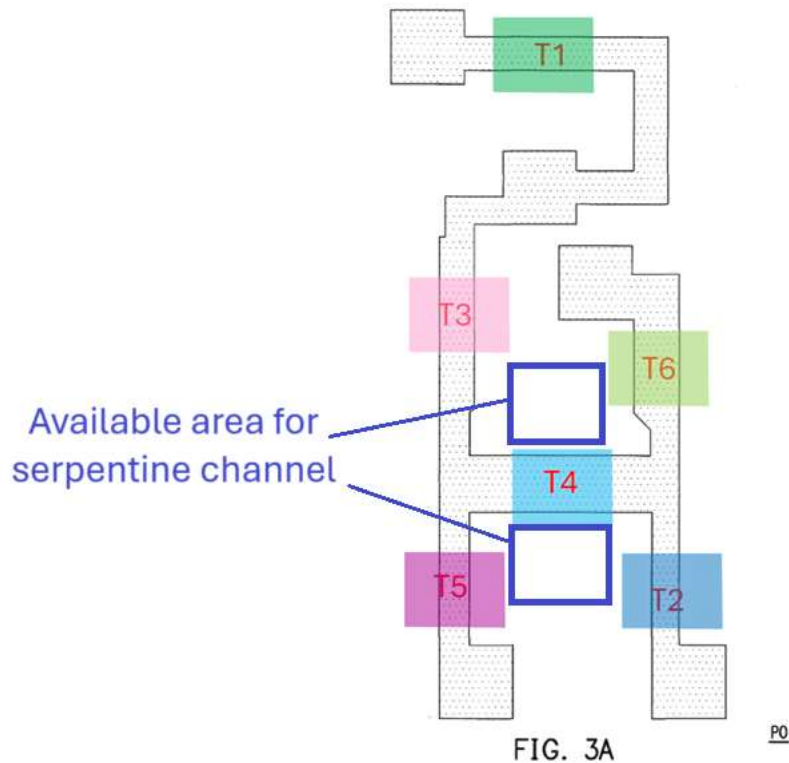


Udagawa, FIG. 13A (annotated).

170. For reasons explained in ¶¶110-115, a POSITA would have been motivated to incorporate Udagawa's driving TFT gate shapes (thereby increasing the channel length) in Liu's miniaturized OLED driving circuit to reduce the dispersion effects that accompany the reduction in size of the driving circuit. Furthermore, modifying Liu to use Udagawa's longer gate channel is in line with Liu's objectives of reducing the size of the pixel structure because forming the gate channel in this way allows for both a reduction of dispersion and a reduced size while enabling an improved operation of the driving TFT.

171. It is my opinion that the size of the pixel area would not appreciably

increase, thereby remaining consistent with the objectives of Liu. For example, Udagawa describes that different lengths and numbers of serpentine structures can implement the extended channel. Udagawa, ¶20. POSITAs would have similarly designed Liu's T4 channel region by choosing the length of the channel based on the constraints of a particular design. Figures 3 and 4 of Udagawa show this versatility in allowing various channel lengths. Moreover, using a channel that folds back on itself multiple times in a snake-like pattern (e.g., U-turns, S-shapes) multiplies the effective channel width without increasing the footprint. Second, as shown below in annotated FIG. 3A of Liu, the placement of driving transistor T4 in Liu's design includes available area both above and below the channel of T4 that can be used to incorporate the serpentine channel taught by Udagawa. Moreover, POSITAs would have been more than capable of sizing the gate electrode (BE) to cover an appropriate portion of the modified channel. *Id.*; §VIII.A.4.j.



Liu, FIG. 3A (annotated).

172. Accordingly, Liu as modified by Udagawa teaches a serpentine gate channel region under the gate electrode, which as explained above is the bottom capacitor electrode (“a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor being curved”).

l. 1[j]: “a third thin film transistor electrically coupled to the second thin film transistor, the corresponding organic light emitting diode, and the first capacitor plate, the semiconductor layer being extended to and electrically coupled to the third thin film transistor;”

1[k]: “a fourth thin film transistor electrically coupled to the first voltage line and the second thin film transistor, the semiconductor layer being extended to and is electrically coupled to the fourth thin film transistor;”

1[l]: “a fifth thin film transistor electrically coupled to the second thin film transistor, the third thin film transistor, and the corresponding organic light emitting diode, the semiconductor layer being extended to and is electrically coupled to the fifth thin film transistor; and”

1[m]: “a sixth thin film transistor electrically coupled to the second voltage line, the third thin film transistor, and the first capacitor plate, the semiconductor layer being extended to and is electrically coupled to the sixth thin film transistor.”

173. In my opinion, Liu discloses limitations 1[j]-1[m].

174. I have grouped each of the limitations 1[j]-1[m], which are directed to the third through sixth TFTs, for clarity and ease of discussion, and have further annotated FIGS. 1 and 3A of Liu to show the mapping of the transistors. Additionally, a table following the annotated figures of Liu shows the mapping for each transistor across Claim 1, the '990 Patent, and Liu.

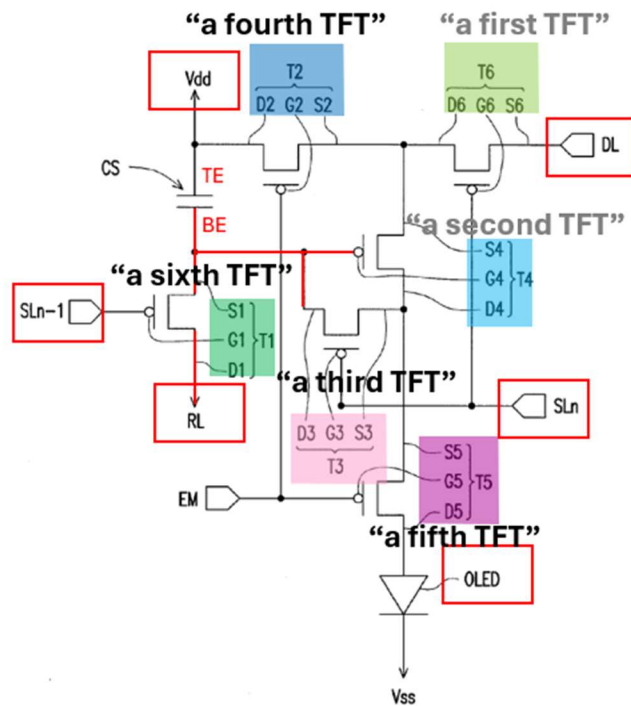


FIG. 1

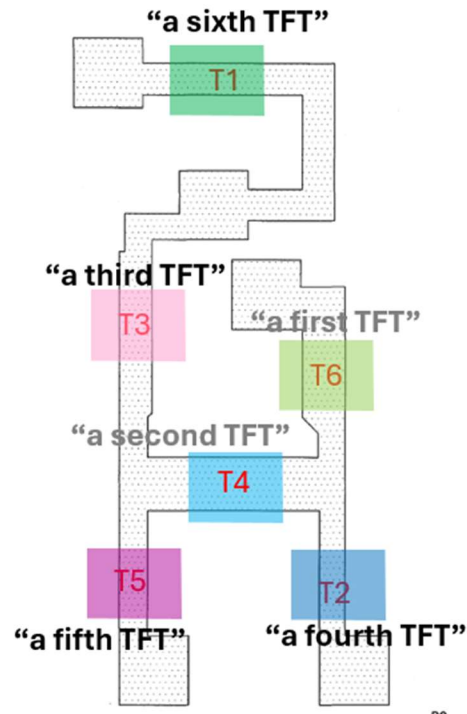


FIG. 3A

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Left: Liu, FIG. 1 (annotated); Right: Liu, FIG. 3A (annotated)

Claim 1	'990	Liu	Function
1 st TFT	T2	T6	Data input switching TFT
2 nd TFT	T1	T4	Driving TFT
3 rd TFT	T3	T3	Scan[n] / Compensation TFT
4 th TFT	T5	T2	Power supply / Operation control TFT
5 th TFT	T6	T5	Light emission control TFT
6 th TFT	T4	T1	Scan[n-1] Init switch TFT
Capacitor	Cst	CS	Storage capacitor
1 st Voltage line	ELVDD	Vdd	Power supply
2 nd Voltage line	Vint	RL	Capacitor initialization voltage
OLED	OLED	OLED	
1 st Scan line	Sn	SLn	Current scan line
2 nd Scan line	Sn-1	SLn-1	Previous scan line
Light emission control line	En	EM	Light emission control

Data line	Dm	DL	Data/OLED intensity voltage
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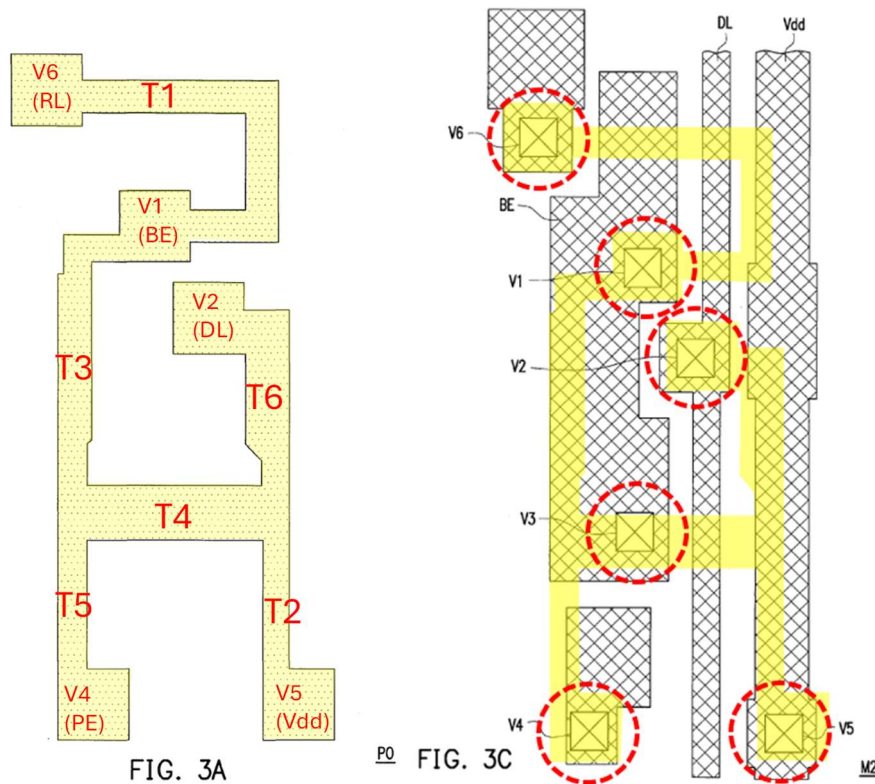
175. As explained in 1[pre] and 1[f], Liu discloses a TFT driving circuit with at least six transistors and one capacitor. *See* ¶¶116-119, 139-141. And as I explain below, Liu discloses each of the recited transistors and connections.

176. Regarding 1[j], Liu discloses T3 (“third thin film transistor”) connected to T4 and BE. Liu, FIG 1. T3 is additionally connected to OLED through T5, just as T4 is. In my opinion, and as explained above for 1[g], a POSITA would have understood that the arrangement of T3, with connection to OLED through adjacent TFTs is the same configuration as disclosed in the ’990 Patent. *See* ’990Pat., 6:61-65 (“T3 is coupled via the light emission control thin film transistor T6 to the anode 65 of the OLED”).

177. Regarding 1[k], Liu discloses T2 (“fourth thin film transistor”) connected to Vdd and T4. Regarding 1[l], Liu discloses T5 (“fifth thin film transistor”) connected to T4, T3, and OLED. Regarding 1[m], Liu discloses T1 (“sixth thin film transistor”) connected to RL, T3, and BE. Accordingly, Liu discloses the electrical connections in 1[k]-1[m].

178. Each of transistors T1 to T6 utilize and include a portion of the semiconductor layer, which is thus electrically coupled to the corresponding transistor. Liu, ¶35. Further, as shown in annotated Figure 3A, Liu’s semiconductor

layer is contiguous and reaches all transistors (“the semiconductor layer being extended to and electrically coupled to”). Liu, ¶35, FIG. 3A (annotated).



Left: Liu, FIG. 3A (annotated); Right: Figure A.

179. In the above annotated FIG. 3A of Liu, locations of transistors T1 through T6 and contact via structures V1 through V6 are overlaid on the semiconductor layer PO. I note that the locations of transistors T1 through T6 can be determined as discussed in ¶¶146-152, and the locations of the contact via structures V1 through V6 can be determined based on Figure A above. I have created Figure A as a compilation of FIGS. 3A and 3C, showing the semiconductor layer PO (yellow, extracted from FIG. 3A) and metal layer 2, M2 (cross-hatched). Liu,

¶¶15, 17, 34-35, 39-42.

180. Accordingly, Liu discloses each of the limitations 1[j]-1[m].

5. Claim 2: “The organic light emitting diode display according to claim 1, wherein gate electrodes of the fourth and fifth thin film transistors are coupled together.”

Claim 3: “The organic light emitting diode display according to claim 2, wherein the gate electrodes of the fourth and fifth thin film transistors are configured to receive a signal from a light emission control line.”

Claim 4: “The organic light emitting diode display according to claim 1, wherein a gate electrode of the sixth thin film transistor is configured to receive a signal from a second scan line.”

Claim 5: “The organic light emitting diode display according to claim 1, wherein gate electrodes of the first and third thin film transistors are coupled together.”

Claim 6: “The organic light emitting diode display according to claim 5, wherein the gate electrodes of the first and third thin film transistors are configured to receive a signal from the first scan line.”

Claim 7: “The organic light emitting diode display according to claim 1, wherein the second capacitor plate is electrically coupled to the first voltage line.”

Claim 23: “The organic light emitting diode display according to claim 1, wherein the third thin film transistor is electrically coupled to the gate electrode and a drain electrode of the second thin film transistor.”

181. In my opinion, Liu teaches or suggests claims 2-7 and 23.

182. I have grouped each of claims 2-7 and 23, which are directed to the

connectivity of various components in the driving circuit of the '990 Patent, for clarity and ease of discussion.

183. As explained in 1[pre], 1[f], 1[g], and 1[j], Liu discloses a TFT driving circuit with at least six transistors and one capacitor. *See* ¶¶116-119, 139-154, 173-180. As explained below and shown in annotated Figure 1, Liu discloses each of the recited transistors and connections.

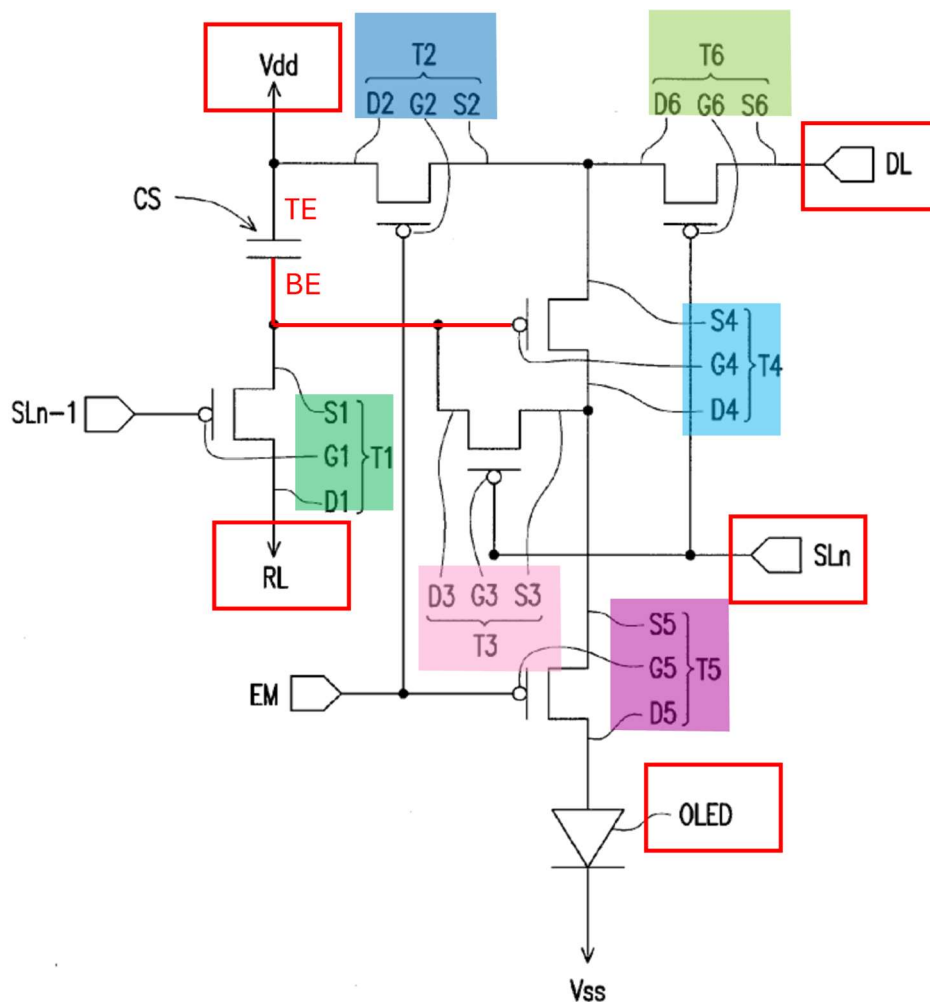


FIG. 1

Liu, FIG. 1 (annotated).

184. Claim 2: Liu discloses that the gates of T2 (“fourth” TFT) and T5 (“fifth” TFT) are connected together. Liu, FIGs. 1, 2.

185. Claim 3: Liu further discloses that the gates of T2 and T5 (G2, G5, respectively) receive the signal EM. Liu, ¶38. Liu explains that “EM” is “a light emitting signal line.” *Id.* In my opinion, a POSITA would have understood that EM was “a signal from a light emission control line” because when EM is applied to T2 and T5, the transistors turn on allowing drive transistor T4 to provide current to OLED, thus allowing the emission of light.

186. Claim 4: T1 (“sixth” TFT) receives S_L_{n-1} (“a second scan line”) at its gate, G1. Liu, ¶38, FIGs. 1, 2.

187. Claim 5: T6 (first” TFT) and T3 (“third” TFT) are connected together. Liu, FIGs. 1, 2.

188. Claim 6: Liu further discloses that the gates of T6 and T3 receive S_L_n (“first scan line”). Liu, ¶38.

189. Claim 7: Liu discloses TE (“second capacitor plate”) connected to V_{dd} (“first voltage line”). Liu, ¶44, FIGs. 1, 2.

190. Claim 23: as shown in Figure 1, the drain (D4) of T4 (“second” TFT) is connected to the source (S3) of T3 (“third” TFT). Liu, ¶35, FIGs. 1, 2. The gate (G4) of T4 is connected to the drain (D3) of T3. *Id.* Furthermore, the source of T3 is

connected to V1 as shown in annotated Figure 1 above and Figure B below, which is connected to BE (the gate electrode of T4). Liu, ¶41, FIGs. 1, 2, 3B, 3C.

191. Each of the transistors and gate connections can also be seen in annotated Figure B, below. I have created Figure B as a compilation of Figures 3A and 3B of Liu, showing the semiconductor layer PO (yellow, extracted from Figure 3A) and metal layer 1, M1 (parallel-hatched). Liu, ¶¶15-16, 34-35, 37-38.

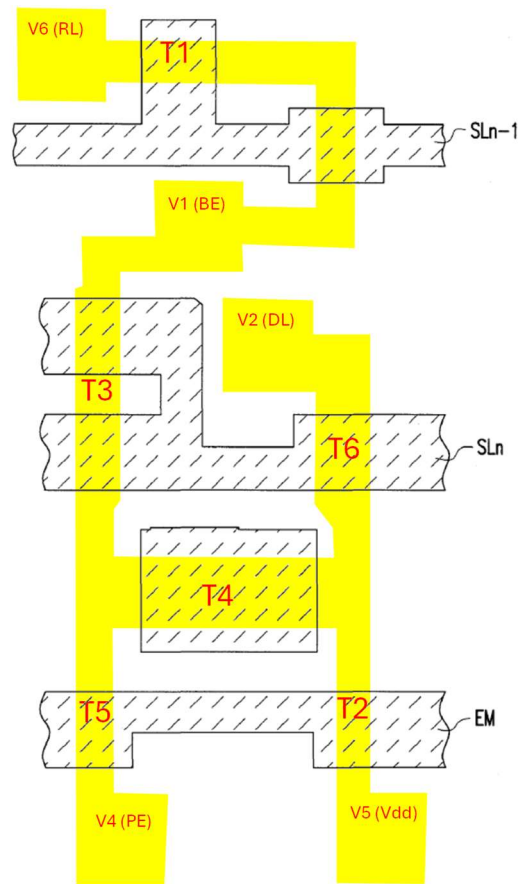
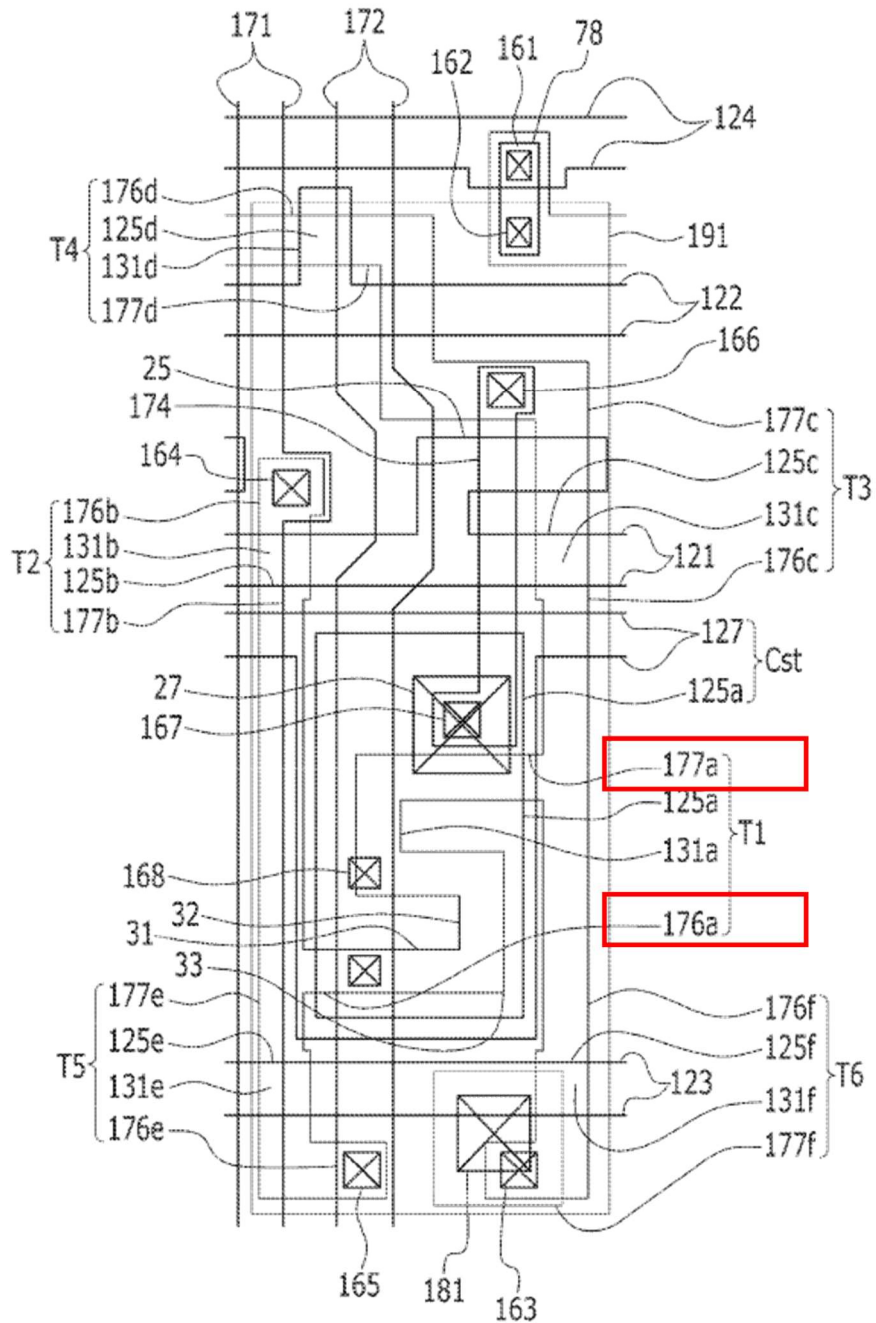


Figure B.

192. To the extent it is argued that Liu does not explicitly show a drain “electrode” of the second thin film transistor (T4), it would have been understood

that the drain and source regions of the semiconductor (corresponding to the transistor) are doped and themselves form drain and source “electrodes,” which are required for proper operation of TFTs. Therefore, the third TFT (T3) being electrically coupled to the drain electrode of the second TFT (T4) can be equivalently construed as being electrically coupled to each other through the existing semiconductor layer connecting the third TFT and the second TFT together. My understanding is corroborated by the description regarding Figure 6 in the ‘990 patent, which describes the doped semiconductor regions as the source and drain “electrodes,” and that “[t]he driving source electrode 176a corresponds to the driving source region 176a doped with the impurity in the driving semiconductor layer 131a, and the driving drain electrode 177 a corresponds to the driving drain region 177 a doped with the impurity in the driving semiconductor layer 131a.” ’990Pat., 10:7-9; FIG. 6.

FIG. 6



'990Pat., FIG. 6 (annotated).

193. Accordingly, Liu discloses claims 2-7 and 23.

6. **Claim 9: “The organic light emitting diode display according to claim 1, wherein portions of the semiconductor layer are doped with N-type impurities.**

Claim 10: “The organic light emitting diode display according to claim 1, wherein portions of the semiconductor layer are doped with P-type impurities.”

194. In my opinion, Liu in combination with Udagawa teaches or suggests claims 9 and 10.

195. Based on FIG. 1 of Liu, Liu discloses p-channel TFTs in its OLED drive circuit because each TFT is shown with a circle at its gate, which is the common symbol for a p-channel transistor. Liu, FIG. 1. Liu further discloses that the TFTs are formed in a semiconductor layer comprising “amorphous silicon, polysilicon, micro-silicon, mono-silicon, an organic semiconductor material, an oxide semiconductor material (e.g., indium zinc oxide, indium germanium zinc oxide, any other suitable material, or a combination of the above), any other suitable material, the aforesaid material having dopant, or a combination of the above.” Liu, ¶¶34-35. Liu, however, does not expressly disclose the dopant used in the semiconductor layer. However, it is my opinion that a POSITA would have understood that the source and drain contacts of TFTs must be heavily doped with N- or P-type impurities to achieve low contact resistance. This was common knowledge in IC or display industries when fabricating transistors. If required, the channel of TFTs can be slightly doped to realize a desirable threshold voltage.

196. Udagawa also discloses a TFT driving circuit using a semiconductor layer comprising polysilicon. Udagawa, ¶5, 9-11. Udagawa further discloses the use of p- channel TFTs, such as TFT 404 and TFT 406. *Id.*, ¶¶124 (“p-channel TFT 406 of the driving circuit”), 136 (“current control TFT 404 including p-channel TFT”), 139 (“p-channel TFT[] 404”). Udagawa explains that p-channel TFTs have less dispersion than n-channel TFTs. *Id.*, ¶41.

197. Udagawa explains that forming TFTs in the semiconductor layer involves at least five doping steps to implant n- and p-type impurities in the semiconductor. *Id.*, ¶¶123-130. In step one, doping of gate electrodes 304 and 307 is performed with n-type dopants phosphorus or arsenic. *Id.*, ¶123. In the second step, masking is used “to protect the channel formation region or the portion of the semiconductor layer for forming the p-channel TFT 406 of the driving circuit.” *Id.*, ¶124. Additional masking is used to protect the semiconductor layer forming TFT 404. *Id.* In this step, additional n-type doping is performed. *Id.*, ¶125.

198. In the third doping step, the masking is not removed and again, the semiconductor layer is doped in a third step with n-type impurities, such as phosphorous or arsenic, to a certain concentration. *Id.*, ¶126. In a fourth step, the masks are then removed, and new masking is performed before treating the semiconductor regions 318, 319, 332, and 333 (that I have shown in red in annotated

Figure 7 below) of TFT 404 and 406 (p-channel TFTs) with p-type impurities. *Id.*, ¶127. The p-type impurities are deposited in the semiconductor regions in concentrations to overcome the n-type impurities already deposited. As Udagawa explains, the regions 318, 319, 332, and 333 of the p-channel TFTs contain n-type dopants from the preceding step. *Id.*, ¶128 As a result, a sufficient amount of p-type dopants are added to produce the appropriate conductivity. *Id.* (“p-type doping impurity element is added at a density that is 1.5 to 3 times as high as that of phosphorous”).

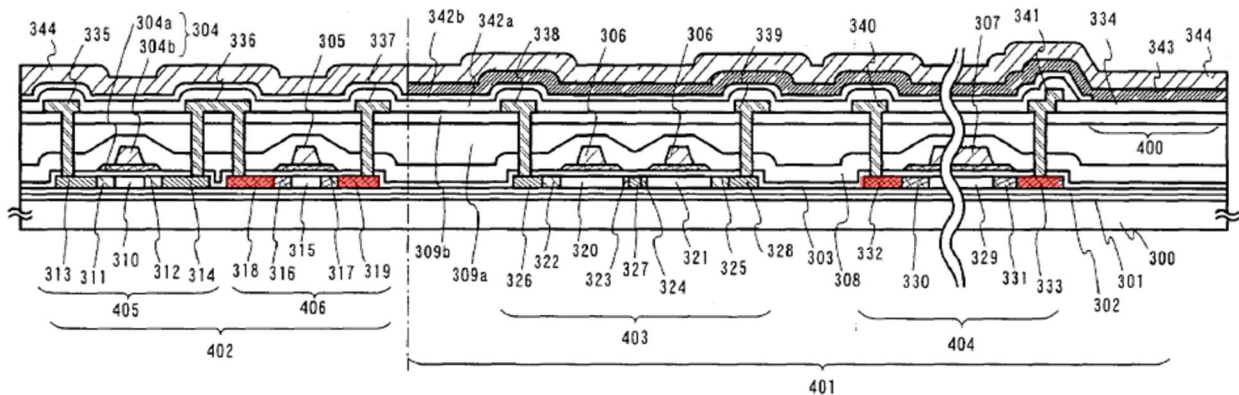


Fig. 7

Udagawa, FIG. 7 (annotated).

199. In the steps as explained above, Udagawa implants both n- and p-type impurities in the semiconductor layer for a mix of n-channel and p-channel TFTs. Although Liu expressly discloses only p-channel TFTs, Liu expressly states that it is not so limited. Liu, ¶32. In my opinion, Liu’s driving circuit could be implemented

using p-channel and/or n-channel TFTs. For example, Chung discloses, regarding its Figure 11, that both n- and p-channel TFTs can be use. Chung, ¶¶87-98. Regardless, in my opinion, Udagawa's method of ion implantations is not excluded by Liu's teachings, particularly because Udagawa discloses implantations of both n- and p-type impurities in a p-channel TFT. Thus, a POSITA using Udagawa's ion implantation method would have had a reasonable expectation of success in forming the semiconductor regions of Liu's TFTs. Accordingly, the semiconductor layer in Liu's design would have included both n-type (e.g., phosphorous or arsenic) impurities ("portions of the semiconductor layer are doped with N-type impurities") and p-type (e.g., boron, aluminum, gallium, or indium) impurities ("portions of the semiconductor layer are doped with P-type impurities"), depending on display design requirements, as claims 9 and 10 require.

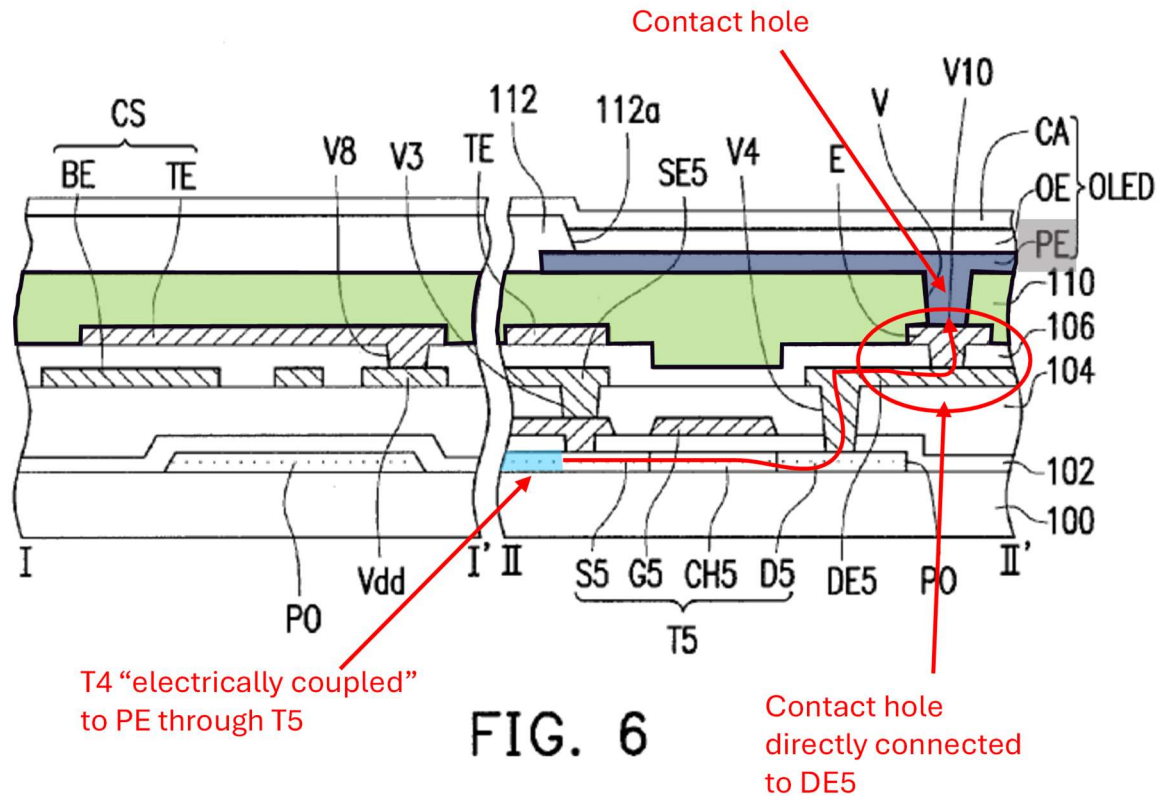
200. Accordingly, claims 9 and 10 are disclosed by Liu in combination with Udagawa.

7. **Claim 24: “The organic light emitting diode display according to claim 1, further comprising a protective layer covering the plurality of driving circuits, wherein each of the organic light emitting diodes further comprises a pixel electrode on the protective layer, the pixel electrode being electrically coupled to the second thin film transistor through a contact hole.”**

Claim 25: “The organic light emitting diode display according to claim 1, further comprising a protective layer covering the plurality of driving circuits, wherein each of the organic light emitting diodes further comprises a pixel electrode on the protective layer, the pixel electrode being electrically coupled to a drain electrode of the fifth thin film transistor through a contact hole.”

201. In my opinion, Liu in combination with Udagawa discloses claims 24 and 25.

202. Liu discloses a planarization layer 110 (“protective layer”) is disposed on the third insulating layer 106 covering the TFTs and capacitor (“covering the plurality of driving circuits”). Liu, ¶¶46, 55, FIGs. 5-6. A pixel electrode is disposed on the planarization layer 110 (“each of the organic light emitting diodes further comprises a pixel electrode on the protective layer”). *Id.* Liu further explains that the pixel electrode is connected to the drain of T5 through contact via structure V. *Id.* As explained above in 1[g], T4 (“second” TFT) is connected to OLED (and the pixel electrode) through T5 (“pixel electrode being electrically coupled to the second thin film transistor through a contact hole”). See ¶¶142-154.



Liu, FIG. 6 (annotated).

203. Claim 24 requires the pixel electrode to be “electrically coupled” to T4 through a contact hole, while claim 25 requires the pixel electrode to be “electrically coupled” to T5 through a contact hole. As shown above the pixel electrode, PE, is connected to T5 through a via (“contact hole”) and T4 is connected to T5. In my opinion, a POSITA would have known that a via or contact hole serves as a crucial electrical connection between different layers of the circuit, such as linking the gate, source, or drain electrodes to the underlying wiring or other functional layers. This enables the efficient transmission of signals and power across the multilayered

structure, ensuring proper operation of the display pixels. Without these connections, the circuit would not be able to route electrical signals between the necessary components, compromising the performance and reliability of the TFT display. Accordingly, the pixel electrode is “electrically coupled” to T5 and to T4.

204. Liu Figure 1 shows the connections of T4 and T5. *See* Liu, FIG. 1. Annotated FIG. 6 below shows the planarization layer, pixel electrode, and connections to the TFT driving circuit (T4 and T5). Liu, FIG. 6 (annotated). As shown therein, T4 is “electrically coupled” to pixel electrode PE through thin film transistor T5 via the semiconductor layer, the contact via structure V4, and contact via structure V because each of these components is electrically conductive.

205. Accordingly, claim 24 and 25 are disclosed by Liu.

8. Claim 26: “The organic light emitting diode display according to claim 1, wherein the first capacitor plate and the first scan line are in the same material layer.”

206. In my opinion, Liu teaches or suggests claim 26.

207. As explained above in 1[ia], Liu teaches a storage capacitor where the bottom electrode BE (“first capacitor plate”) is the gate electrode of T4. *See* ¶¶158-166. As also explained above, BE can be (a) reduced in size and placed directly over the semiconductor layer in M1, or (b) is directly connected to the gate electrode of T4 on M1. *Id.* In scenario (a), BE is directly the gate electrode of T4 and is in layer M1, and in scenario (b), BE directly connects to the gate electrode of T4 through

connector V3, as shown in Liu's Figure 6. In my opinion, the material in V3 would be the same as the material in BE and the gate electrode of T4 to bond well and make a good connection, and thus the capacitor plate, connector V3, and the gate electrode of T4 would form a contiguous connection surface. In either scenario (a) or (b), the material of M1 is used for BE. Liu further discloses that S_Ln ("first scan line") is in M1 ("the same material layer"). Liu, ¶38. Accordingly, M1 (and the BE portion connected to it in scenario (a)) would have been understood as constituting a single "material layer."

208. Accordingly, claim 26 is disclosed by Liu.

9. Claim 27: "The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a "S"-shape."

Claim 28: "The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a partial "S"-shape."

Claim 29: "The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a "M"-shape."

Claim 30: "The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a "W"-shape."

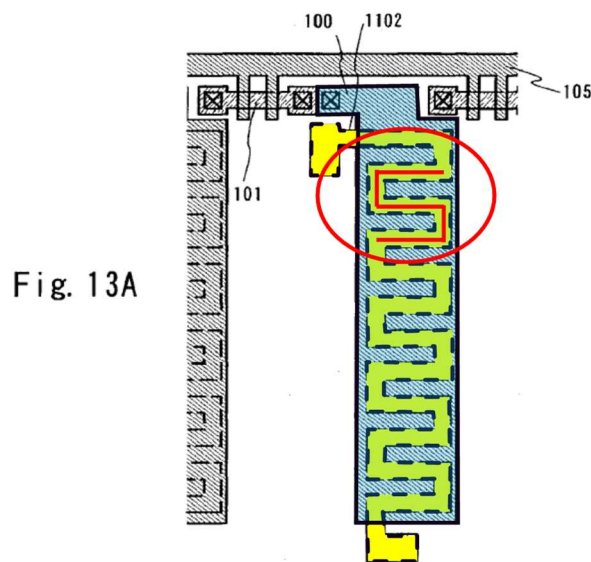
209. In my opinion, Liu in combination with Udagawa teaches or suggests claims 27-30.

210. I have grouped claims 27-30, which are directed to different

configurations of the curved (or serpentine) channel, for clarity and ease of discussion.

211. As explained above in 1[ib], Liu in combination with Udagawa teaches a “curved” channel of drive transistor T4. See ¶¶167-172. As explained below, utilizing Udagawa’s serpentine channel shape for drive transistor T4, many different apparent shapes are realized.

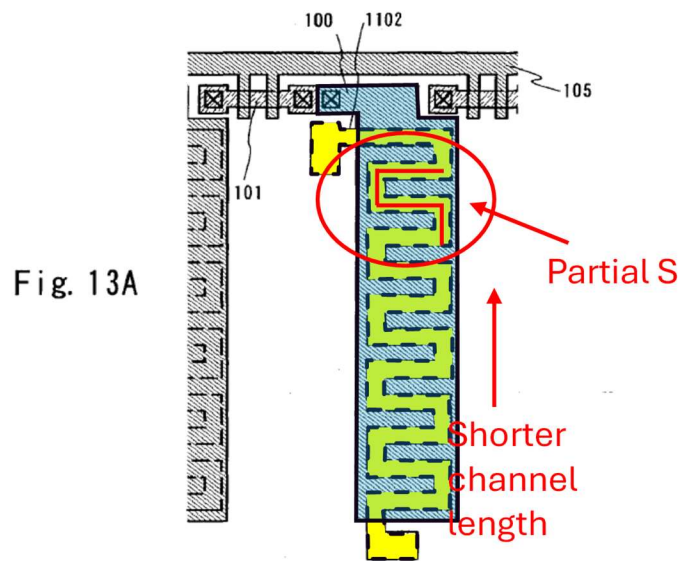
212. Regarding claim 27, incorporating Udagawa’s serpentine shape, produces an “S” shape structure in the gate channel of T4. For example, annotated Figure 13A from Udagawa shows an “S” shape.



Udagawa, FIG. 13A (annotated).

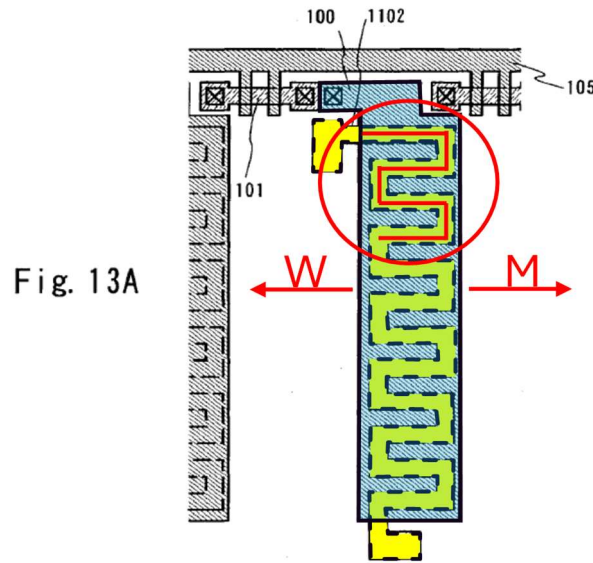
213. Claim 28: Udagawa discloses that the channel can be elongated by shorter or longer lengths. Udagawa, ¶23. Liu does not expressly disclose the length

of the channel of T4. In my opinion, a POSITA would have thus understood that the serpentine shape of Udagawa's could be shorter or longer, depending on the application. Accordingly, shortening the above "S" shape would yield a partial "s" shaped channel. Annotated Figure 13A, below, shows such a configuration.



Udagawa, FIG. 13A (annotated).

214. Claims 29 and 30: Udagawa discloses an "M" and "W" shape. In my opinion, an "M" shape and a "W" shape are merely the same shape viewed from different angles. The claims do not specify from which angle the channel should be viewed. Annotated Figure 13A, below, shows such a configuration.



Udagawa, FIG. 13A (annotated).

A. Ground 1B: Claim 8 is Unpatentable over Liu, Udagawa, and Nakayama

1. Summary of Nakayama

215. In my opinion, Nakayama is analogous art to the '990 Patent because it is in the same field of endeavor. Both are directed to reducing variations in a current (or equivalently, maintaining a constant current) supplied to the driving TFT of a circuit that drives (or controls) an OLED in an OLED display. *Id.*, ¶¶4-5. Nakayama teaches that variations in the drive currents supplied to different pixels may be caused by variations in the electrostatic capacitances of the holding and kick capacitors. *Id.*, ¶5. To suppress capacitance variation due to lateral misalignment, such as mask misalignment, Nakayama teaches the upper electrode of capacitors can be configured to have a larger surface area than the bottom electrodes thereof. *Id.*,

¶38.

2. Motivation to combine Liu, Udagawa, and Nakayama

216. In my opinion, there are several reasons that motivate combining the teachings of Liu and Nakayama.

217. As discussed above, Liu is directed to a reduced-size pixel structure. Liu, ¶¶4, 6, 10, 47, 56, 72. Nakayama is also related to OLED displays and OLED pixels. Nakayama, ¶¶5-6. In particular, Nakayama describes that capacitor configurations and variances in capacitance affect TFT driving circuits. Nakayama, ¶¶4-5. Thus, in my opinion, a POSITA would have been motivated to improve Liu's drive circuit operation based on the teachings of Nakayama to reduce variations in the operation of the driving TFT.

218. Nakayama recognized OLED operations can be improved by reducing capacitance variations (e.g., due to mask misalignment), which included configuring the upper electrode of a capacitor to have a larger surface area than the bottom electrode. Nakayama, ¶38. Thus, it would have been obvious to combine Liu with Nakayama, and specifically to use Nakayama's configuration of the larger upper capacitor electrode to improve Liu's OLED driving pixel circuit. This combination would not impact Liu's objectives of reducing the size of the pixel structure because, as explained below, TE's area is able to be increased. Furthermore, forming the top capacitor electrode of Liu to have a larger surface area than the bottom capacitor

electrode would have resulted in mitigating capacitance variations, which would have improved the operation of the driving TFT of Liu, while maintaining a reduced size.

219. In my opinion, a POSITA would have been skilled enough to shape the capacitor plates such that the upper plate has a larger area than the lower plate, as disclosed by Nakayama. Furthermore, shaping the capacitor plates in an integrated circuit for an OLED display was well-known by 2012, as evidenced by the teachings of Nakayama.

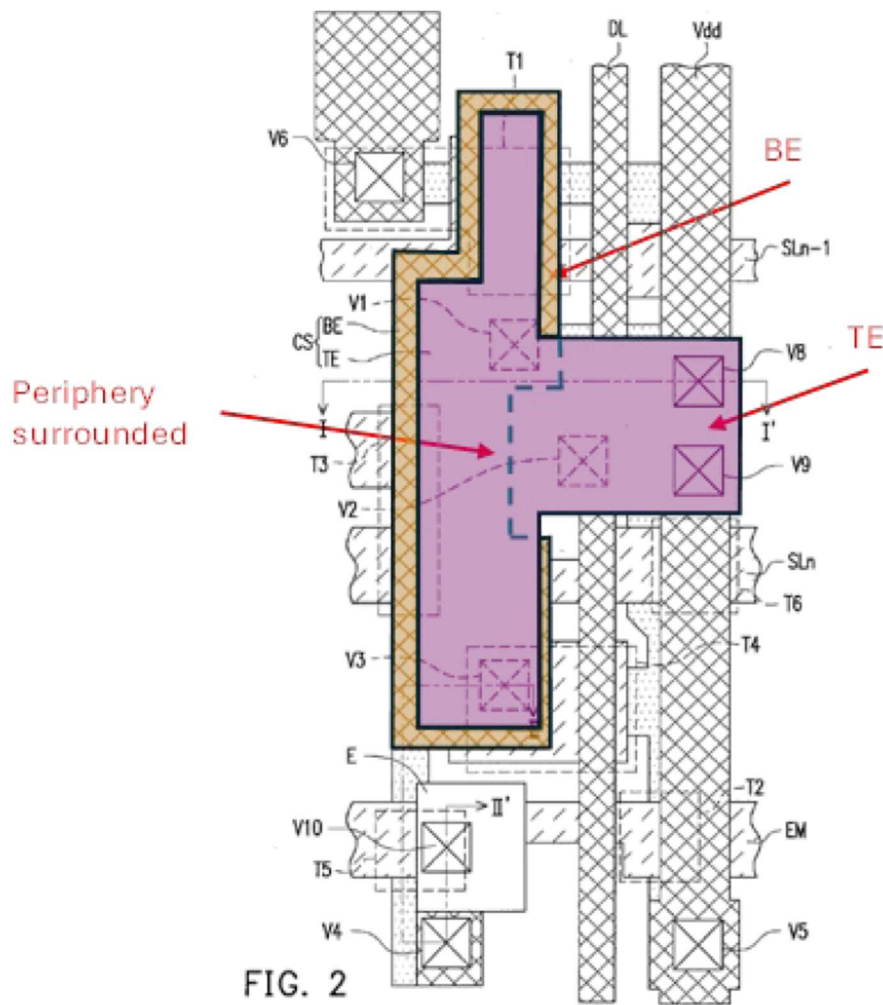
220. Furthermore, and as discussed above, the Liu reference can be combined individually with each of Udagawa and Nakayama. In each instance, the combination involves modifying a distinct aspect of Liu, and these modifications are independent of one another. For example, Udagawa teaches modifying the channel of the driving TFT and Nakayama teaches modifying the relative shapes of the storage capacitor plates. In my opinion, a POSITA would recognize that there is no interference among the proposed modifications based on the teachings of Udagawa and Nakayama.

221. Additional details regarding the Liu–Udagawa–Nakayama combination are provided below in connection with specific claim limitations.

3. Claim 8: “The organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.”

222. In my opinion, Liu in combination with Udagawa and Nakayama teaches or suggests claim 8.

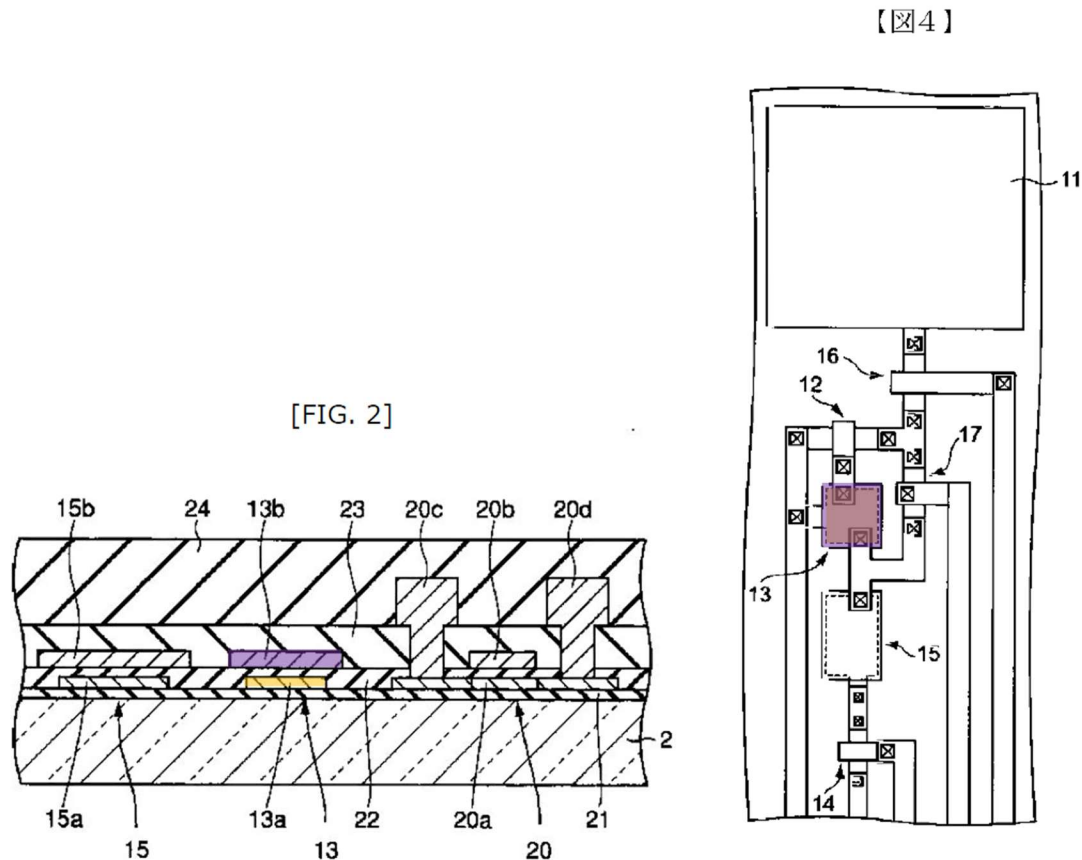
223. Liu teaches that TE (“second capacitor plate”) surrounds a portion of BE (as shown in annotated Figure 2 below); notably, the dashed line represents a periphery of the BE, which is surrounded by the top electrode plate (purple). Herein, the term “surround[ing] a periphery” is understood as that at least a portion around the outside of BE was surrounded by TE. EX1015 (“the outward bounds of something as distinguished from its internal regions or center”); EX1016, (“the outside boundary or surface of something”). Furthermore, claim 8 does not recite “entire periphery” or “entire surface area” to be surrounded and the ‘990 Patent’s detailed description also neither explains nor attaches any particular significance to “a periphery.”



Liu, FIG. 2 (annotated).

224. Regardless, to the extent that it is argued that TE does not “completely surround[] a periphery of” BE, it is my opinion that this would have been obvious in light of Nakayama. For example, Nakayama discloses forming the upper electrode of a holding capacitor to have a larger surface area than the bottom electrode. Nakayama, ¶38, FIGs. 2, 4. Further, as shown in Figures 2 and 4 of Nakayama, the lower capacitor electrode 13a (orange) is within the perimeter of the upper electrode

13b (purple). Nakayama, ¶¶35, 38. Nakayama explains that this configuration of capacitor electrodes suppresses the variation in the capacity of the capacitors with respect to the deviation in the X-Y placement of the top electrode. Nakayama, ¶38.



Left: Nakayama, FIG. 2 (annotated); Right: Nakayama, FIG. 4 (annotated).

225. As also explained above, Liu teaches BE is either directly connected to the gate electrode of T4 in M1 or can be reduced in size and placed directly over the semiconductor layer in M1. See ¶¶223-224. In the former, no other metal layer is present in metal layer 3. Liu, ¶44; FIG. 3D. Thus, using Nakayama's teachings, Liu's

top electrode (TE) would be increased in size to completely overlap BE so that any mask misalignments would not affect the capacitance of CS, i.e., the capacitance of the storage (or holding) capacitor. In other words, there is room for the top plate to move with respect to the bottom plate without affecting the capacitance. It would have been obvious to enlarge the TE because it would have allowed for fabrication variances to maintain the capacitance of CS, as Nakayama explains. §VIII.A.2. This is possible because the capacitance is determined by the smaller of the two electrodes in the capacitor. *See* Murade, ¶98 (explaining that the area of overlap between two capacitor plates determines the capacitance – a smaller overlap area creates a smaller capacitance).

226. For the latter (BE placed over the semiconductor layer), BE is directly above the gate electrode of T4 and TE may either remain in M3 or be moved to M2. *See* ¶¶158-166. As explained above, TE is unrestricted by other metal traces that would prevent extending it. It would have been obvious to enlarge TE to realize the advantages of Nakayama.

227. In my opinion, a POSITA or an engineer performing layout of OLED circuits could reason the relatively simple arrangement of signal lines and CS to achieve the arrangement disclosed in Nakayama. Rather than following a rigid set of instructions, such an individual applies professional judgment and technical

expertise to address the practical challenges encountered during circuit design. Any such changes to the capacitor design would have been well within a POSITA's skills and capabilities and would have amounted to routine design considerations, as these types of modifications are commonly made in the course of optimizing electronic layouts. In the context of OLED circuit design, engineers routinely adapt component placement and interconnections to accommodate manufacturing tolerances, improve electrical performance, or ensure seamless integration with other circuit elements. For example, selecting the appropriate capacitor size to fit within the available layout space, or choosing a suitable dielectric material to meet specific voltage and reliability requirements, are both considered routine design considerations. Additionally, engineers may adjust the routing of signal lines to minimize interference or crosstalk, or modify the shape and position of contact holes to enhance yield and manufacturability. These types of decisions are part of the everyday skill set of a POSITA and do not require inventive ingenuity.

228. The knowledge of a POSITA in this respect is further evidenced, for example, by textbooks such as *CMOS VLSI Design: A Circuits and Systems Perspective* (authored by N. Weste and D. Harris), which discusses, inter alia, layout design rules that “describe how small features can be and how closely they can be reliably packed in a particular manufacturing process” (*see* Weste, Chapter 1.5.3)

and wherein “[t]he rules are defined in terms of feature sizes (widths), separations, and overlaps, [and wherein] [t]he main objective of the layout rules is to build reliably functional circuits in as small an area as possible” (*see* Weste, Chapter 3.3). *See generally* Weste, Chapters 1, 3.

229. For the reasons explained above and in ¶¶216-221, there is a motivation to incorporate Nakayama’s capacitor plate sizing in Liu to maintain the capacitance of Liu’s CS capacitor.

230. Accordingly, Liu in combination with Udagawa and Nakayama disclose claim 8.

B. Ground 1C: Claims 11-19, 21, and 22 are Unpatentable over Liu, Udagawa, and Chung

1. Summary of Chung

231. Chung (Ex. 1008) discloses a pixel circuit of an organic light emitting display is configured similarly to the circuit shown in Figure 1 of the ’990 patent (i.e., with scan lines, signal lines, a driving transistor, five switching transistors, and a storage capacitor), but additionally includes a switching transistor SW_TR6 for applying a reverse bias, i.e., a seventh transistor. Chung, ¶57.

232. In my opinion, Chung is analogous art to the ’990 patent because it is in the same field of endeavor. For example, both are directed to compensating the threshold voltage of the driving transistor. Chung, ¶87.

233. Chung teaches that in an initialization period (i.e., a non-light emission period) of operating the pixel circuit, a low-level scan signal that is applied to the initial switching transistor SW_TR 5 is also applied to the switching transistor SW_TR6 for applying a reverse bias to the OLED, thereby preventing degradation of the organic light emitting diode OLED. *Id.*, ¶¶83-84.

2. Motivation to combine Liu, Udagawa, and Chung

234. In my opinion, there are several reasons that motivate the combination Liu and Chung.

235. As discussed above, Liu is directed to a reduced-size pixel structure, which includes a plurality of TFTs. Liu, ¶¶4, 6, 10, 47, 56, 72. Liu does not limit the number of TFTs in its OLED driving circuit. *Id.*, ¶32. Chung discloses an OLED drive circuit similar to those described in Liu, which additionally includes a seventh TFT that is configured to apply a reverse bias voltage to the OLED, which increases the lifespan of the OLED and the uniformity of brightness of the respective pixels by the elimination of the degradation. Chung, ¶¶11, 57.

236. Thus, the OLED driving circuit of Liu would be improved by introducing a seventh TFT, as described by Chung, for applying a reverse bias to the OLED, thereby preventing degradation of the OLED during an initialization period. Chung, ¶¶83-84. This would have been obvious, since it was motivated by Chung explicitly describing the implementation of a seventh TFT, and the introduction of a

single additional TFT not appreciably impacting the size of the driving circuit of Liu.

237. In my opinion, a POSITA would have been skilled enough to use an additional seventh TFT in a 6T1C pixel driving circuit, e.g., Liu's OLED driving circuit, to achieve the known and predictable result of preventing the degradation of the OLED during the initialization period. Furthermore, incorporating a seventh transistor into a 6T1C circuit was well-known by 2012, as evidenced by the teachings of Chung and other known prior art references, such as Ref1, Ref2, and Ref3.

238. Furthermore, and as discussed above, Liu can be combined individually with each of Udagawa and Chung. In each instance, the combination involves modifying a distinct aspect of Liu, and these modifications are independent of one another. For example, Udagawa teaches modifying the channel of the driving TFT and Chung teaches modifying the 6T1C circuit by incorporating a seventh TFT. In my opinion, a POSITA would recognize that there is no interference among the modifications, and each combination can be implemented without affecting the others.

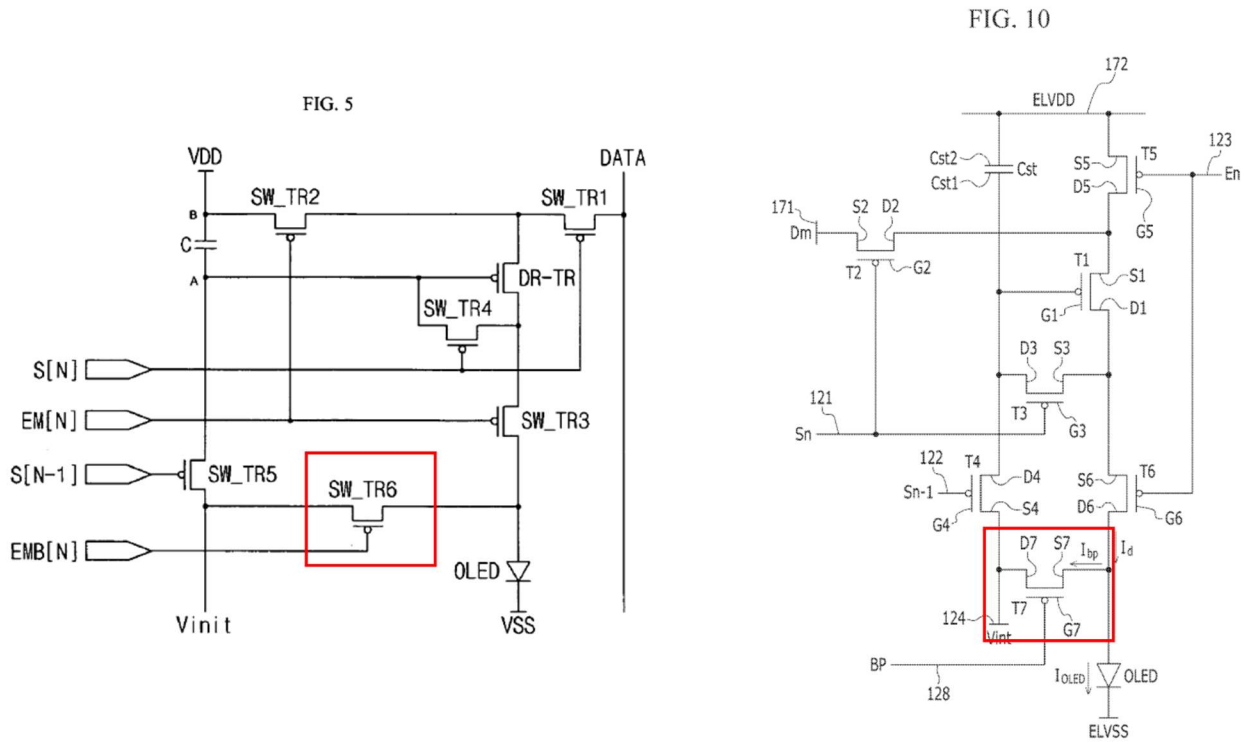
239. Additional details regarding the Liu–Udagawa–Chung combination are provided below in connection with specific claim limitations.

3. Claim 11: “The organic light emitting diode display according to claim 1, further comprising a seventh thin film transistor electrically coupled to the second voltage line, the fifth thin film transistor, and the corresponding organic light emitting diode.”

240. In my opinion, Liu in combination with Udagawa and Chung teaches or suggests claim 11.

241. As explained above in §VIII.A.2, there is a motivation to combine the teachings of Liu and Chung. Combining such teachings would not have impacted the above teachings in Ground 1A because the combination adds a single TFT to the driving circuit.

242. Liu discloses that its driving circuit could have more or less than six TFTs. Liu, ¶¶32, 58. As explained above, Chung discloses an OLED drive circuit similar to those described in Liu and in Figure 10 of the '990 patent, which additionally includes a seventh TFT. §VIII.A.1. Figure 10 from the '990 Patent and Figure 5 from Chung have been reproduced below, highlighting the seventh TFT.



Left: Chung, FIG. 5 (annotated); Right: '990 Patent, FIG. 10 (annotated).

243. As shown below, Chung's circuit is identical to Liu, except for the additional seventh TFT (SW_TR6).

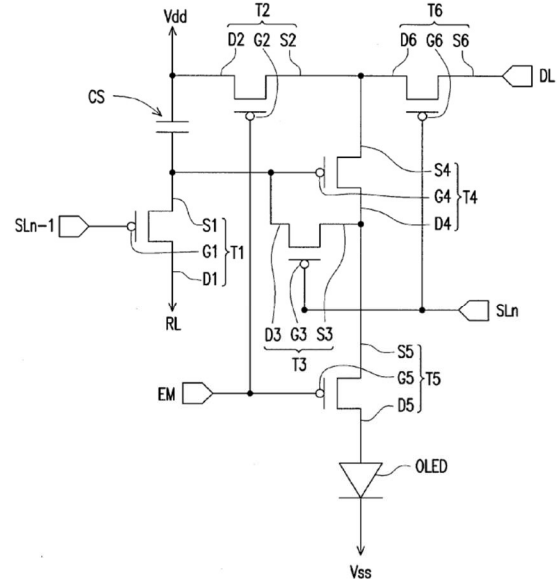
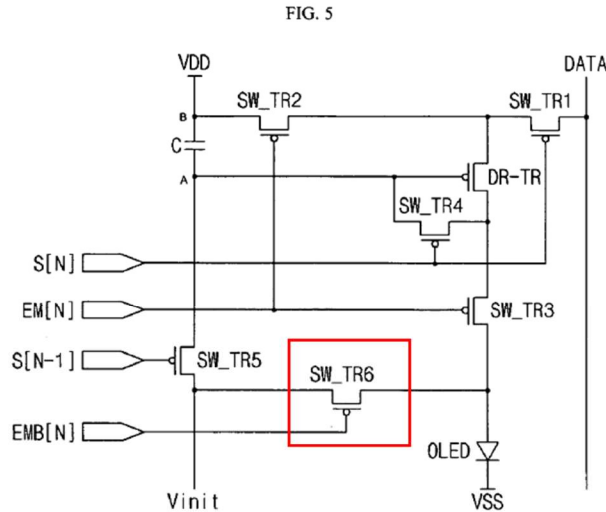


FIG. 1

Left: Chung, FIG. 5 (annotated); Right: Liu, FIG. 1.

244. Chung discloses SW_TR6 in Figure 5 connected to the OLED and initialization TFT (SW_TR5). Chung, ¶¶57, 60, 63. Chung explains that “the emission reverse control signal may be readily obtained by coupling an inverter to a previous end of an output end of the emission control signal driver outputting the emission control signal.” Chung, ¶63. Thus, it would have been understood that SW_TR6 was active when SW_TR3 was inactive (i.e., when the OLED is off). *See id.*, FIG. 6. Chung explains the addition of SW_TR6 prevents “degradation of the organic light emitting diode OLED” during the initialization period. Chung, ¶84.

245. In my opinion, the motivation to modify Liu to incorporate Chung’s seventh TFT would have been increasing the lifespan of the OLED and maintaining uniformity of brightness of the respective pixels. Such a modification would have

improved the performance of Liu drive circuit with minimal increase in size. Furthermore, as shown above, Chung and Liu's circuits are identical except for the additional TFT. A modified drive circuit incorporating Chung's TFT in Liu's drive circuit is shown below.

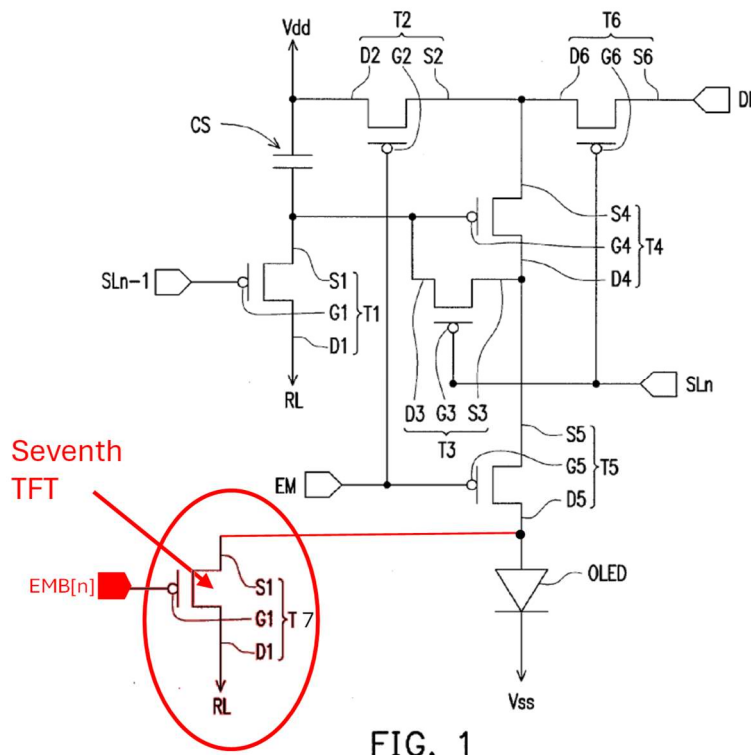


FIG. 1

Liu, FIG. 1 modified with Chung FIG. 5 (annotated).

246. For the reasons explained in §VIII.A.2, incorporating Chung's seventh TFT in Liu would enhance the drive circuit to prevent degradation of the OLED.

247. Accordingly, claim 11 is disclosed by Liu in combination with Udagawa and Chung.

4. Claim 12: “The organic light emitting diode display according to claim 11, wherein the semiconductor layer is extended to and is electrically coupled to the seventh thin film transistor.”

248. In my opinion, Liu in combination with Udagawa and Chung teaches or suggests claim 12.

249. As explained in 1[g] and 1[j], each of transistors T1 to T6 utilize and include a portion of the semiconductor layer, which is thus electrically coupled to the corresponding transistor. Liu, ¶35; §§VIII.A.4.h, VIII.A.4.i. When adding an additional TFT, it is understood that the same semiconductor layer would be used for that new TFT because it would have used the design disclosed in Liu. Furthermore, Liu discloses the semiconductor layer is contiguous between all TFTs. *See, e.g.*, Liu, FIG. 3A. Thus, it would have been obvious to incorporate an additional TFT in the semiconductor layer used for the other TFTs. Using a contiguous semiconductor layer would have been a natural choice to enhance fabrication yield and reduce cost, especially given that Liu’s layer was contiguous. Moreover, it was one of two options (contiguous or non-contiguous).

250. Accordingly, a seventh TFT and the semiconductor layer being extended to incorporate that TFT is disclosed by Liu in combination with Udagawa and Chung.

5. Claim 13: “The organic light emitting diode display according to claim 12, wherein a gate electrode of the seventh thin film transistor is configured to receive a signal from a bypass control line.”

251. In my opinion, Liu in combination with Udagawa and Chung teaches or suggests claim 13.

252. Chung discloses that the seventh TFT has a gate signal of EMB[n] (“bypass control line”). Chung explains that EMB is the “emission reverse control signal” and supplies a signal to effect a reverse bias of the OLED. Chung, ¶63. In my opinion, a POSITA would have recognized that activation of the seventh TFT would have bypassed and remove accumulated charge on the OLED and thus represents a “bypass” control signal for the voltage on the OLED.

6. **Claim 14: “The organic light emitting diode display according to claim 11, wherein gate electrodes of the fourth and fifth thin film transistors are coupled together.”**

Claim 15: “The organic light emitting diode display according to claim 14, wherein the gate electrodes of the fourth and fifth thin film transistors are configured to receive a signal from a light emission control line.”

Claim 16: “The organic light emitting diode display according to claim 11, wherein a gate electrode of the sixth thin film transistor is configured to receive a signal from a second scan line.”

Claim 17: “The organic light emitting diode display according to claim 11, wherein gate electrodes of the first and third thin film transistors are coupled together.”

Claim 18: “The organic light emitting diode display according to claim 17, wherein the gate electrodes of the first and third thin film transistors are configured to receive a signal from the first scan line.”

Claim 19: “The organic light emitting diode display according to claim 11, wherein the second capacitor plate is electrically coupled to the first voltage line.”

253. In my opinion, Liu in combination with Udagawa and Chung teaches claims 14-19.

254. As explained Ground 1A in §VIII.A.5, Liu discloses these claims. The addition on the seventh TFT does not alter Liu’s disclosure. Accordingly, for the same reasons as explained above in Ground 1A, Liu in combination with Udagawa and Chung teaches these claims.

7. **Claim 21: “The organic light emitting diode display according to claim 11, wherein portions of the semiconductor layer are doped with N-type impurities.”**

Claim 22: “The organic light emitting diode display according to claim 11, wherein portions of the semiconductor layer are doped with P-type impurities.”

255. In my opinion, Liu in combination with Udagawa and Chung teaches claims 21 and 22.

256. As explained above in Ground 1A, Udagawa discloses that P- and N-type impurities are doped into p-channel TFT transistors formed in the semiconductor layer PO. §VIII.A.6. The addition of Chung’s seventh TFT does not alter the structure of the semiconductor layer but only adds an additional p-channel TFT. Accordingly, for the same reasons as explained above in Ground 1A, Liu in combination with Udagawa and Chung teaches claims 21 and 22.

C. Ground 1D: Claim 20 is Unpatentable over Liu, Udagawa, Chung, and Nakayama

1. Motivation to combine Liu, Udagawa, Chung, and Nakayama

257. As previously discussed, the Liu reference can be combined individually with each of the cited references—Udagawa, Nakayama, and Chung. In each instance, the combination involves modifying a distinct aspect of Liu, and these modifications are independent of one another. For example, Udagawa teaches

modifying the channel of the driving TFT, Nakayama teaches modifying the relative shapes of the storage capacitor plates, and Chung teaches modifying the 6T1C circuit by incorporating a seventh TFT. In my opinion, a POSITA would recognize that there is no interference among the modifications, and each combination can be implemented without affecting the others.

258. Additional details regarding the Liu–Udagawa–Nakayama–Chung combination are provided below in connection with specific claim limitations.

2. Claim 20: “The organic light emitting diode display according to claim 11, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.”

259. In my opinion, Liu in combination with Udagawa, Chung, and Nakayama teaches or suggests claim 20.

260. As explained above in claim 8 in Ground 1B, Liu in combination with Udagawa and Nakayama teach to make TE completely surround a “periphery” of BE. §VIII.A.3. The addition of Chung’s seventh TFT does not alter the explanations above. For the same reasons the combination teaches claim 20.

261. Accordingly, claim 20 is disclosed by Liu in combination with Udagawa, Chung, and Nakayama.

**D. Ground 2A: Claims 1-10 and 21-30 are Unpatentable over
Noguchi-I and Udagawa**

1. Summary of Noguchi-I

262. Noguchi-I discloses a shield electrode is provided in a wiring layer between the pixel electrode and a wiring layer in which the gate electrode is provided such that the shield electrode forms a region covering the gate electrode, which reduces the parasitic capacitance formed between the gate electrode of the driving transistor and a pixel electrode (anode) of the organic EL element OLED. Noguchi-I, ¶35.

263. In my opinion, Noguchi-I is analogous art to the '990 Patent because Noguchi-I and the '990 patent are in the same field of endeavor. Both are directed to the pixel structure of an OLED display that is driven by scanning lines, power source lines, signal lines, and transistors T1 to T6. Noguchi-I, ¶70. Similarly, both endeavor to compensate for the variability of the threshold voltage of the driving TFT. *Id.*, ¶15.

264. Noguchi-I teaches a pixel of an organic EL display device that includes a first wiring layer disposed at a level closer to a substrate 100 than a second wiring layer. *Id.*, ¶69. Herein, the first wiring layer includes scanning lines, an emission control line, and an initialization voltage line (each extending in a horizontal direction), and the second wiring layer includes a power source line and a signal line

data (each extending in a vertical direction). *Id.*, ¶68. The first wiring layer, which further includes the gate electrode of the driving transistor, is disposed between the interlayer dielectric 110 and the interlayer dielectric 111, the second wiring layer is disposed between the interlayer dielectric 111 and the interlayer dielectric 112, and the pixel electrode 103 is disposed on the interlayer dielectric 112. *Id.*, ¶71.

2. Motivation to combine Noguchi-I and Udagawa

265. In my opinion, there are several reasons that motivate the combination of Noguchi-I and Udagawa.

266. Both Noguchi-I and Udagawa described drive circuits for OLED displays and both sought to improve the design and operation of OLEDs. Notably, Noguchi-I describes a pixel structure of an OLED display with reduced parasitic capacitance that improved image quality. Noguchi-I, ¶¶12, 15, 72. And, Udagawa describes drive circuit configurations that improved OLED's reliability, and consequently, its operations and image quality. Udagawa, ¶12. Therefore, a POSITA would have been motivated to combine the complementary teachings of Noguchi-I with Udagawa to achieve further improvements in the image quality of the OLED display.

267. More specifically, Udagawa disclosed that as the channel length of a TFT increases, the oxide film capacitance C_{ox} becomes larger, and at least a portion of this capacitance can be used as a retention capacitance of the OLED, thus

improving OLED's image quality. Udagawa, ¶64. In my opinion, a POSITA would have found it obvious to combine the complementary teachings of Udagawa with Noguchi-I, and specifically to use Udagawa's the serpentine channel in Noguchi-I's driving TFT to further improve the operations of the OLED. As discussed in ¶¶83-85, using a serpentine channel advantageously delivers sufficient pixel brightness, enables fast pixel charging to support high refresh rates, and offsets variations in OLED efficiency and degradation over time.

268. Furthermore, it is my opinion that a POSITA would have had a reasonable expectation of success, because using TFT with a longer channel to reduce dispersion and increase capacitance was well-known by 2012, evidenced by the teachings of Udagawa and other known prior art references, and such modifications were well within the skill set of a POSITA.

269. Additional details regarding the Noguchi-I–Udagawa combination are provided below in connection with specific claim limitations.

3. Independent Claim 1

a. 1[pre]: “An organic light emitting diode display comprising:”

270. In my opinion, Noguchi-I teaches or suggests 1[pre]. Noguchi-I describes a “pixel of a conventional organic EL display device” with reference to Figures 8 and 9. *Id.*, ¶11. It then presents four related embodiments that build upon

each other to address the perceived deficient response of the pixel. *Id.*, ¶¶66-95. All embodiments are based on the circuit diagram of Figure 1 (Noguchi-I, ¶¶66, 74, 79, 88) but progressively alter the construction of capacitor C1 and the gate electrode of T4 in different ways. *Id.*, ¶¶72, 77, 83, 91. My analysis below relies on the cumulative teachings of Noguchi-I embodiments that culminate in embodiment 4 (Figure 7). To the extent other figures of Noguchi-I are used below, they represent common features of Noguchi-I's invention.

271. Noguchi-I discloses “an organic EL **display device**” with “a current emissive element such as an organic EL element.” Noguchi-I, Abstract, ¶¶1, 41. The display comprises a plurality of “pixels” (*id.*, ¶¶3, 70 (identifying one “display unit” having one pixel), where the “organic EL element” is an OLED (*id.*, ¶11, FIG. 1).

272. Noguchi-I describes a “pixel of a conventional organic EL display device” with reference to Figures 8 and 9. *Id.*, ¶11. It then presents four related embodiments that build upon each other to address the perceived deficient response of the pixel. *Id.*, ¶¶66-95. Each of the embodiments uses the circuit diagram of Figure 1 (*id.*, ¶¶66, 74, 79, 88) but alters the construction of capacitor C1 and the gate electrode of T4 (*id.*, ¶¶72, 77, 83, 91).

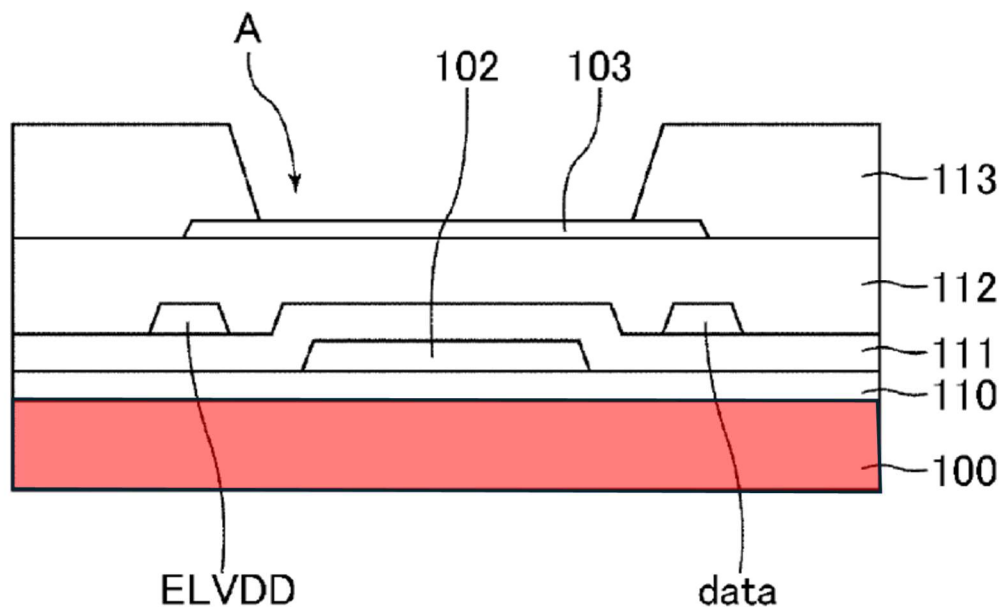
273. Accordingly, Noguchi-I discloses an OLED display comprising pixels (“[a]n organic light emitting diode display”).

b. 1[a]: “a substrate;”

274. In my opinion, Noguchi-I teaches or suggests 1[a].

275. Noguchi-I discloses a pixel comprising a “**substrate 100**,” among other things. Noguchi-I, ¶¶66-69, 98-114, FIGs. 3 (annotated below), 6, 9. It was well-known that substrates for OLED pixels comprised glass, among other materials, and needed to be non-conductive so that the circuits placed on them operated properly. *See, e.g.*, Liu, ¶33; Kim, 5:4-11.

Fig. 3



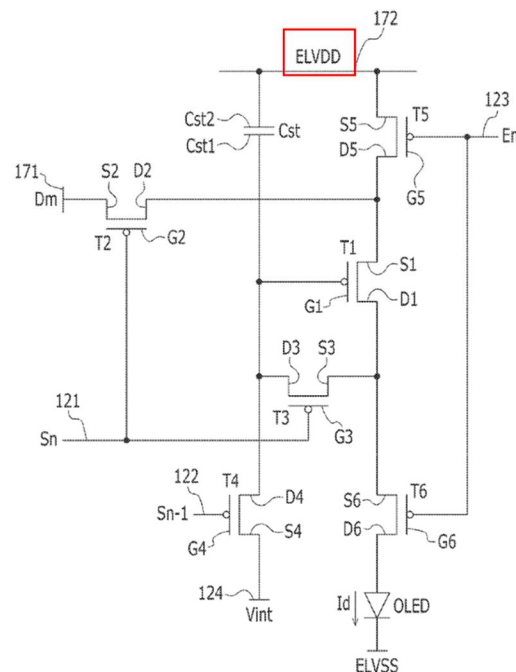
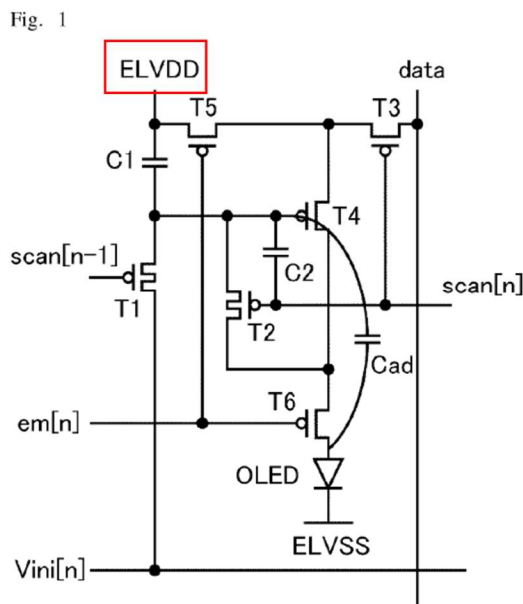
Noguchi-I, FIG. 3 (annotated).

c. 1[b]: “a first voltage line;”

276. In my opinion, Noguchi-I teaches or suggests 1[b].

277. Noguchi-I discloses the “first voltage line” as a “power source line ELVDD” in a second wiring layer. Noguchi-I, ¶71, FIG. 1 (annotated below). It would have been understood that ELVDD is a “voltage line” because ELVDD is positive power supply voltage, e.g., applied to the drain terminal of the driving transistor in an AMOLED pixel. The same symbol is also used in the ’990 Patent. ’990Pat, 6:25-37. Annotated Figure 1 of Noguchi-I has been reproduced alongside Figure 1 of the ’990 Patent to show the similarities between the circuits and to show ELVDD. Its primary function is to supply the current that causes the OLED emitter to light up.

FIG. 1



Left: Noguchi-I, FIG. 1 (annotated); Right: '990Pat., FIG. 1 (annotated).

278. In addition, a table has been provided below to cross-reference each transistor and signal line of the '990 Patent to the similarly-described elements in the disclosure of Noguchi-I. *See also* Noguchi-I, ¶¶98-114.

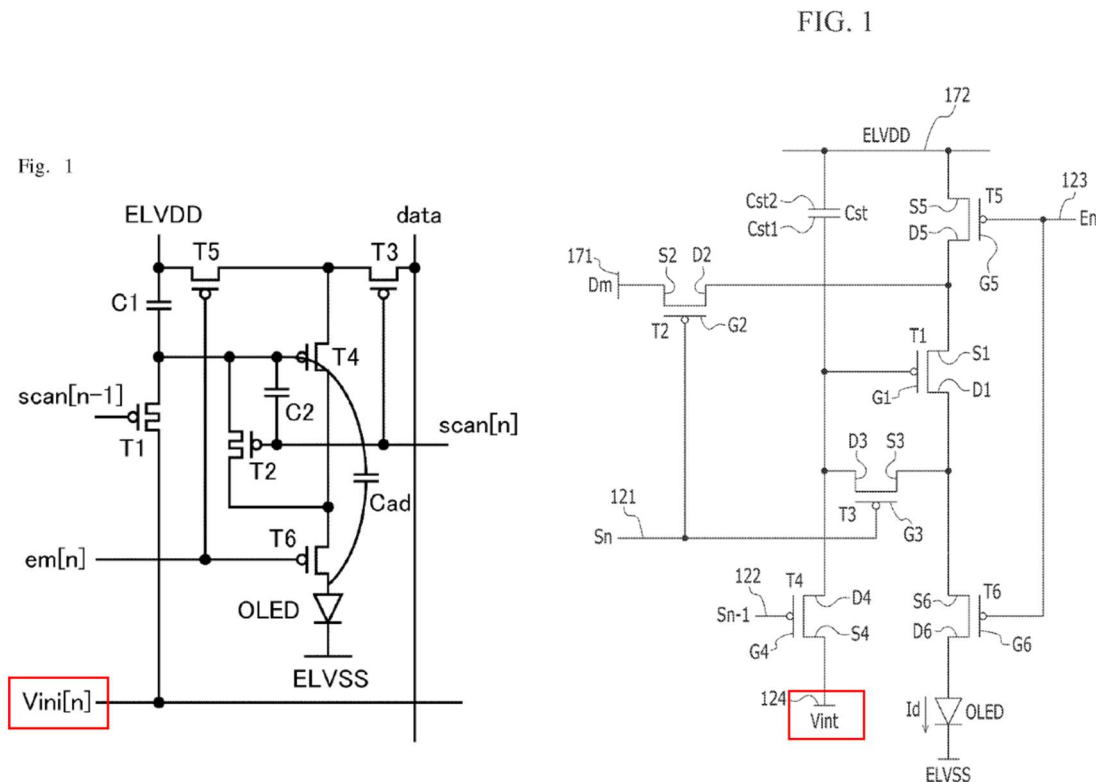
Claim 1	'990	Noguchi-I	Function
1 st TFT	T2	T3	Data input switching TFT
2 nd TFT	T1	T4	Driving TFT
3 rd TFT	T3	T2	Scan[n] / Compensation TFT
4 th TFT	T5	T5	Power supply / Operation control TFT
5 th TFT	T6	T6	Light emission control TFT
6 th TFT	T4	T1	Scan[n-1] Init switch TFT
Capacitor	Cst	C1	Storage Capacitor
First Capacitor Plate	125h	Gate electrode 102	
Second Capacitor Plate	127	Shield electrode 104	
1 st Voltage line	ELVDD	ELVDD	Power supply
2 nd Voltage line	Vint	Vini[n]	Initialization voltage
OLED	OLED	OLED	
1 st Scan line	Sn	scan[n]	Current scan line
2 nd Scan line	Sn-1	scan[n-1]	Previous scan line
Light emission control line	En	em[n]	Light emission control
Data line	Dm	data	Data/OLED intensity voltage

d. 1[c]: “a second voltage line;”

279. In my opinion, Noguchi-I teaches or suggests 1[c].

280. Noguchi-I discloses the “second voltage line” as initialization voltage line “Vini[n]” that may be formed in the first wiring layer. Noguchi-I, ¶68, FIG. 1

(annotated below). Vini[n] corresponds to Vint in the '990 Patent, described as “initialization voltage line 124.” '990Pat, '990Pat, 6:25-37. Annotated Figure 1 of Noguchi-I has been reproduced alongside Figure 1 of the '990 Patent to show Vini[n] and Vint.



Left: Noguchi-I, FIG. 1 (annotated); Right: '990Pat., FIG. 1 (annotated).

281. Accordingly, limitation 1[c] is disclosed by Noguchi-I.

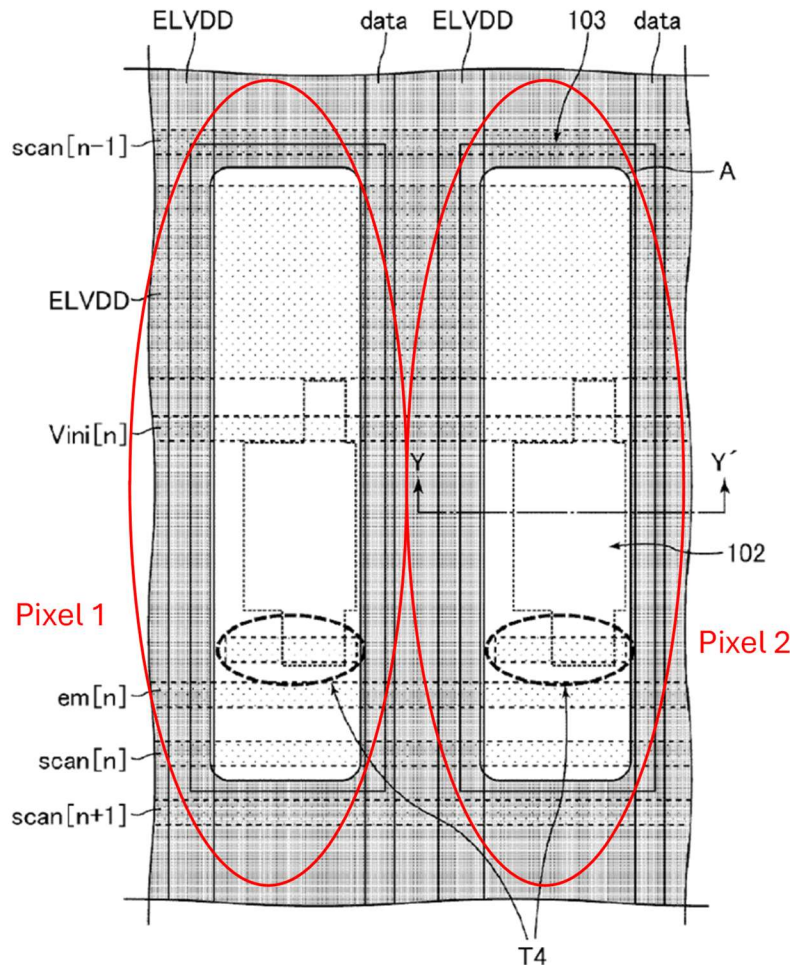
e. 1[d]: “a plurality of pixels, each of the pixels comprising an organic light emitting diode;”

282. In my opinion, Noguchi-I teaches or suggests 1[d].

283. As explained above in 1[pre], Noguchi-I discloses a display with a

plurality of pixels. §VIII.A.3.a. Each pixel structure includes TFTs, capacitor, and OLED. Noguchi-I, ¶¶11, 66-70, 74, 77, 79, 88, 91, FIG. 1. Noguchi-I further explains that item 103 in the figures is a pixel electrode of an OLED. Noguchi-I, ¶¶15, 110. As shown in Figure 1, there is only one OLED per pixel (“each of the pixels comprising an organic light emitting diode”). *Id.*, FIG. 1. As shown in Figures 2 (annotated below), 4, 5, 7, and 8, there are at least two pixels in the display (“a plurality of pixels”).

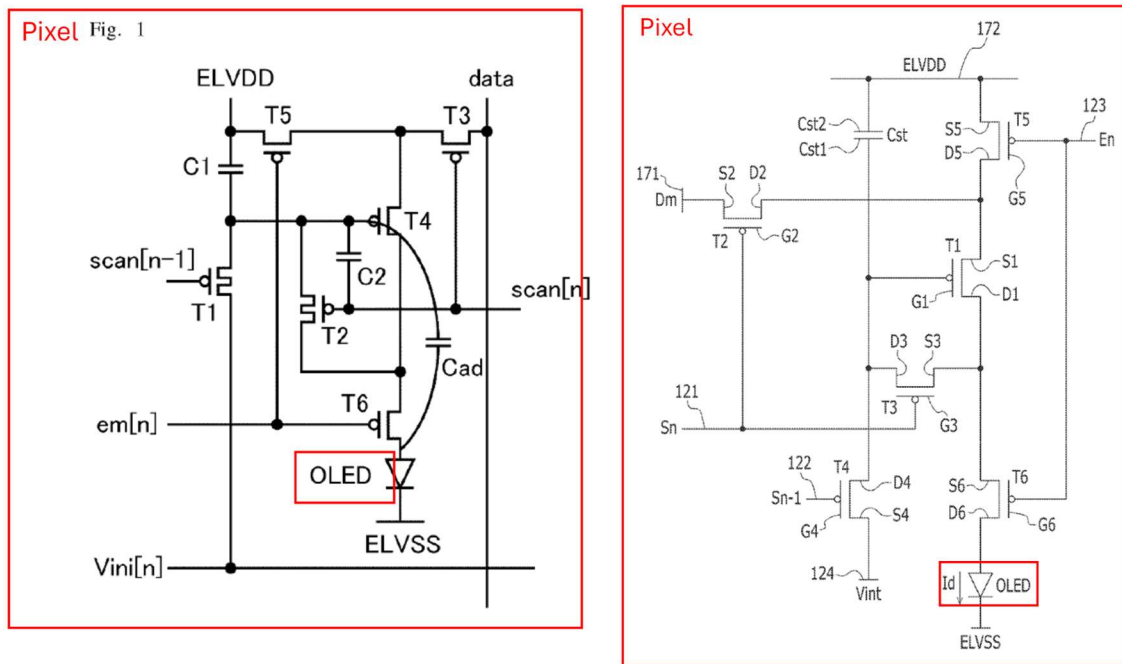
Fig. 2



Noguchi-I, FIG. 2 (annotated).

284. Annotated Figure 1 of Noguchi-I has been reproduced alongside Figure 1 of the '990 Patent to show the driving circuit that is part of each pixel and the pixel's OLED driven by the circuit.

FIG. 1



Left: Noguchi-I, FIG. 1 (annotated); Right: '990Pat., FIG. 1 (annotated).

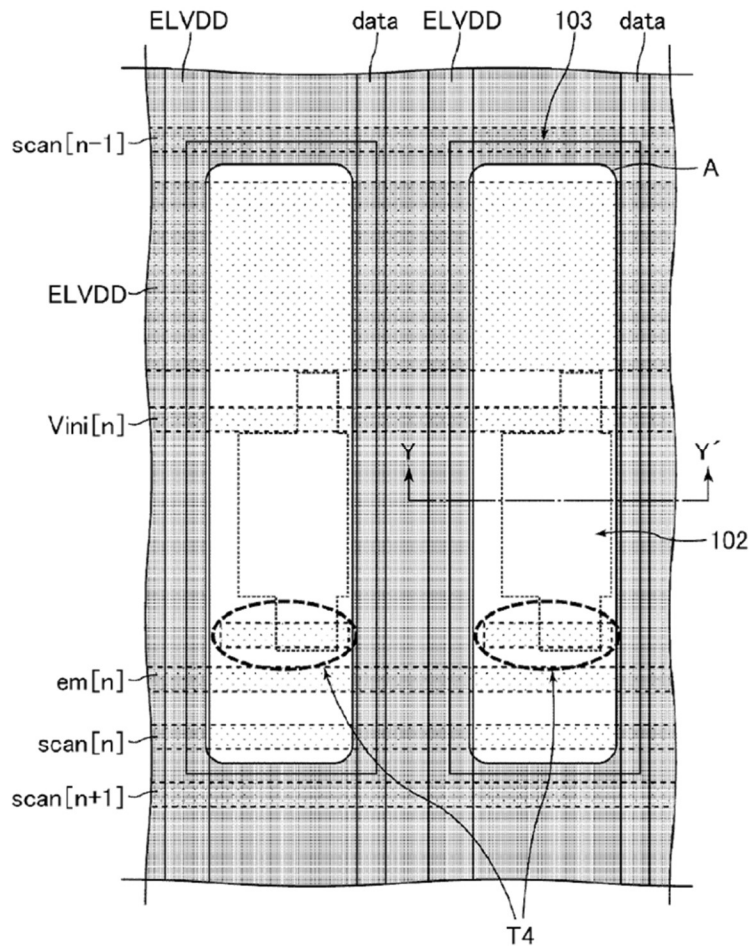
285. As shown above in annotated Figure 1, Noguchi-I discloses “a plurality of pixels, each of the pixels comprising an organic light emitting diode.”

- f. 1[e]: “a plurality of driving circuits on the substrate, each of the organic light emitting diodes being electrically coupled to a respective driving circuit;”

286. In my opinion, Noguchi-I teaches or suggests 1[e].

287. As explained above in 1[d], Noguchi-I teaches or suggests multiple pixels in a display. §VIII.A.3.e. Noguchi-I further describes a “plurality of driving circuits” because it describes a driving circuit for each of the plurality of pixels, where each driving circuit comprises a plurality of TFTs to drive the OLED for that pixel. Noguchi-I, ¶¶1, 11 (“The pixel has six transistors (T1 to T6), two capacitors (C1 and C2), and one organic EL element OLED.”), FIG. 1. The pixel driving circuits that are electrically coupled to OLED through drive transistor T4 are disposed on the substrate. TFTs are located in the pixel, and a region denoted by “A” in the figures “represents a pixel opening that functions as the display region of the organic EL display device.” Noguchi-I, ¶70, FIG. 2. Furthermore, the ’990 Patent admits a “plurality of thin film transistors and capacitors...driv[e] the organic light emitting diode.” ’990 Patent, 1:45-49.

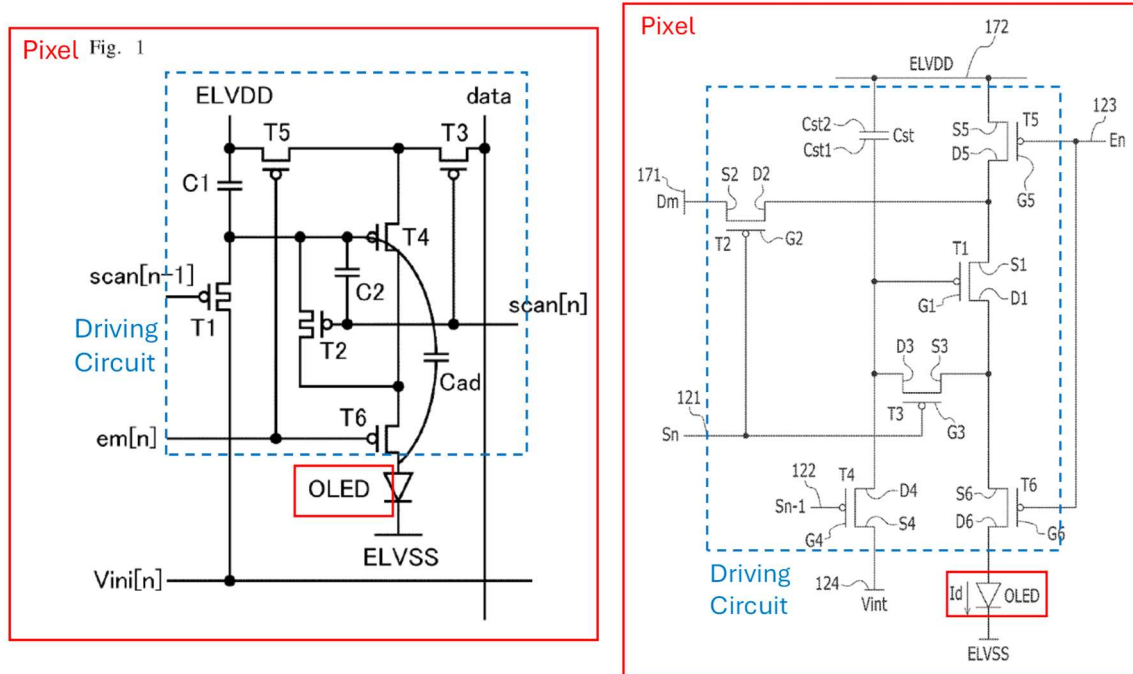
Fig. 2



Noguchi-I, FIG. 2.

288. As shown below, each of the TFT driving circuits is connected to an OLED (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). *Id.*, ¶31, FIG. 1 (annotated). Annotated Figure 1 of Noguchi-I has been reproduced alongside Figure 1 of the ’990 Patent to show the relationship of a pixel and driving circuit.

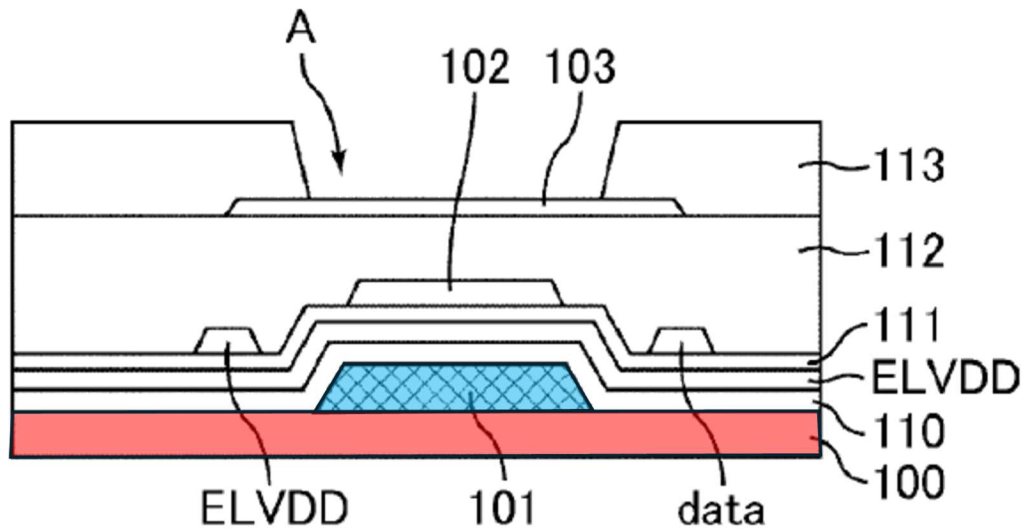
FIG. 1



Left: Noguchi-I, FIG. 1 (annotated); Right: '990 Pat., FIG. 1 (annotated).

289. Furthermore, Noguchi-I explains that the TFTs are formed in a semiconductor layer that is formed on the substrate (“a plurality of driving circuits on the substrate”). *Id.*, ¶¶64, 70, FIGs. 8, 9. The substrate and semiconductor layer (blue) are shown in annotated Figure 9 below. In my opinion, a POSITA would have thus understood that the plurality of Noguchi-I’s driving circuits, including the plurality of TFTs would have been formed on a single substrate including multiple pixels.

Fig. 9



Noguchi-I, FIG. 9 (annotated).

290. Accordingly, Noguchi-I discloses limitation 1[e].

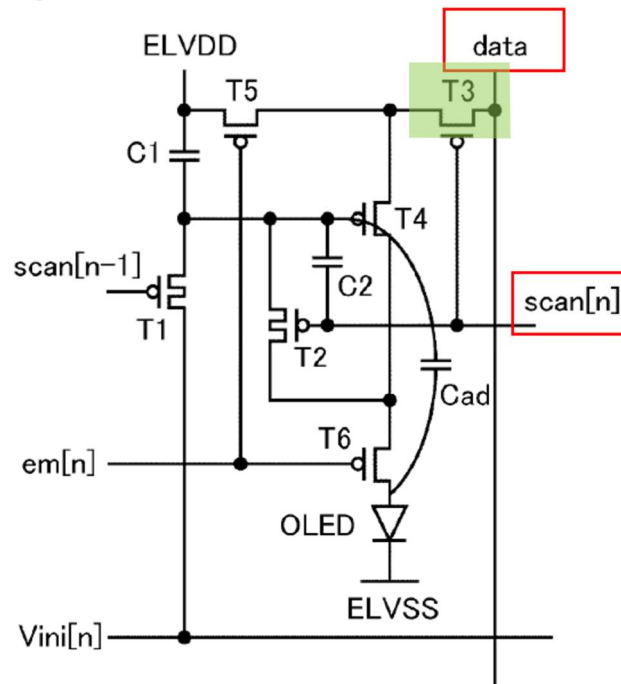
- g. 1[f]: “wherein each of the driving circuits comprises: a first thin film transistor coupled to a first scan line and a data line;”

291. In my opinion, Noguchi-I teaches or suggests 1[f].

292. Noguchi-I discloses the “first thin film transistor” as T3 that is coupled to “the first scan line,” scan[n], and to “a data line,” data, as shown in Noguchi-I’s Figure 1. As explained in 1[e], each pixel structure includes several TFTs arranged in a driving circuit. §VIII.A.3.f. Figure 1 is a “circuit diagram illustrating a pixel of an organic EL display device in an embodiment.” Noguchi-I, ¶44. Referring to the circuit diagram below, Noguchi-I explains that a “transistor T3 **responds to the scan**

signal inputted from the scanning line scan[n], and performs switching of the data signal inputted from the signal line data.” *Id.*, ¶11, FIG. 1 (annotated).

Fig. 1



Noguchi-I, FIG. 1 (annotated).

293. Accordingly, T3 (“first thin film transistor”) is electrically connected (“coupled”) to scan line scan[n] and a data line (“a first scan line and a data line”).

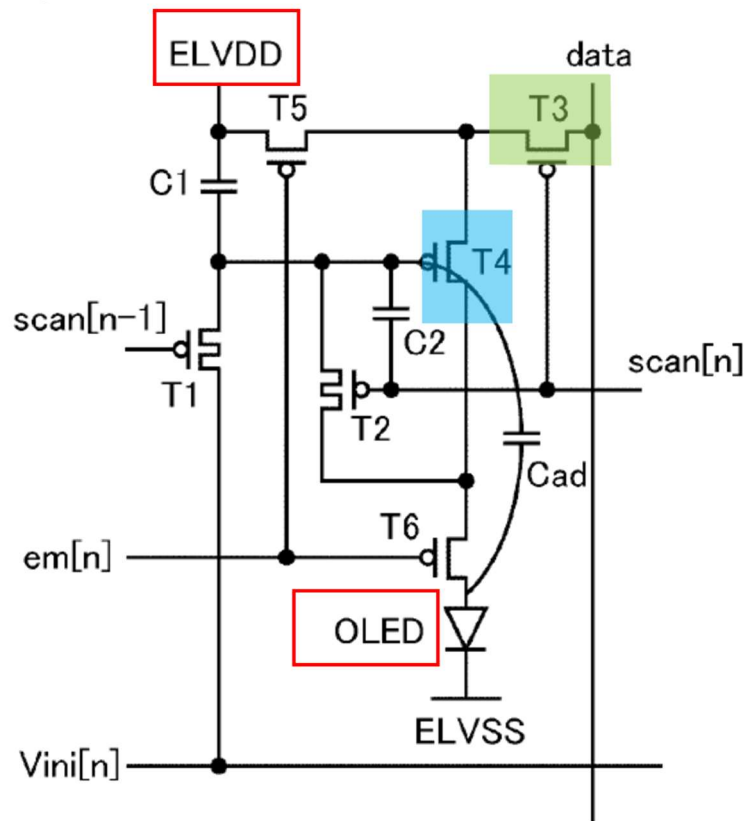
294. Furthermore, as will be explained below, Noguchi-I discloses each of the six transistors and capacitor recited in 1[g]-1[m]. The table in 1[b] above shows the mapping of Noguchi-I’s circuit components to those recited in the ’990. *See* §VIII.A.3.c (table).

- h. 1[g]: “a second thin film transistor utilizing a semiconductor layer and electrically coupled to the first voltage line, the corresponding organic light emitting diode, and the first thin film transistor, the semiconductor layer being extended to and electrically coupled to the first thin film transistor;”**

295. In my opinion, Noguchi-I teaches or suggests 1[g].

296. As shown in Noguchi-I’s Figure 1 circuit, Noguchi-I discloses the “second thin film transistor” as TFT T4, which is electrically coupled to “the first voltage line,” ELVDD, through TFT T5. Noguchi-I’s T4 is electrically coupled to the “corresponding organic light emitting diode,” OLED, through TFT T6, and is electrically coupled to the “first thin film transistor,” TFT T3, through a direct connection. *See* Noguchi-I, ¶11, FIG. 1.

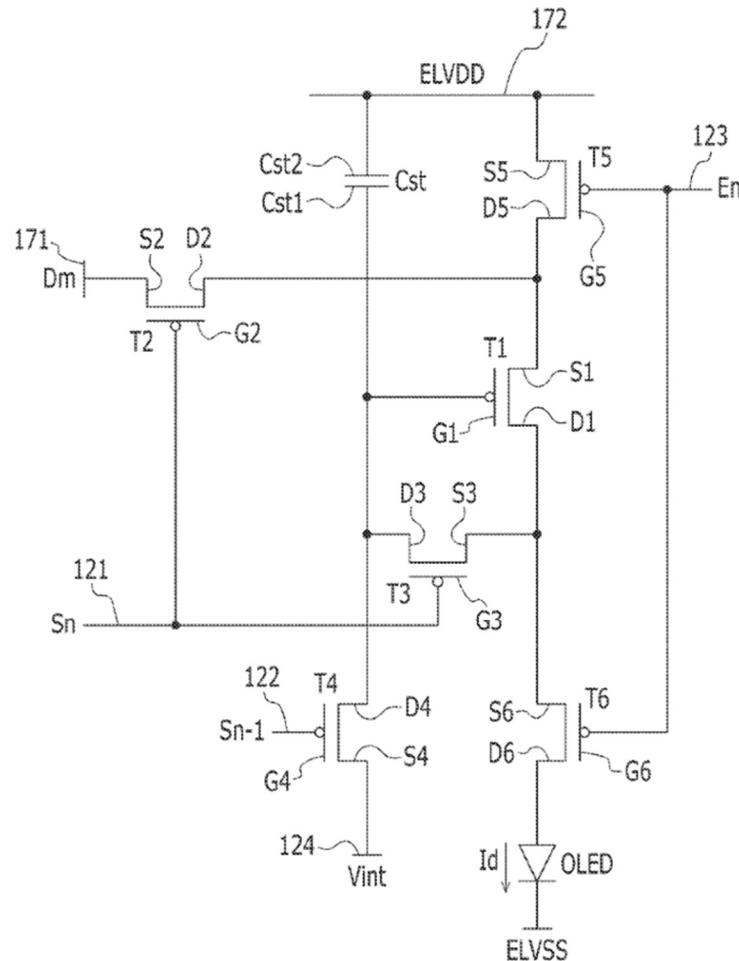
Fig. 1



Noguchi-I, FIG. 1 (annotated).

297. As explained in Ground 1A, the above characterization of Noguchi-I's TFT T4 being "electrically coupled" to the OLED and ELVDD through intervening TFTs is consistent with the '990 patent's Figure 1 connectivity and its detailed description, which explains, e.g., "T1 is coupled via the operation control thin film transistor T5 to the driving voltage line" and "T1 is electrically coupled via the light emission control thin film transistor T6 to an anode of the OLED." See '990Pat., 6:38-45, FIG. 1.

FIG. 1

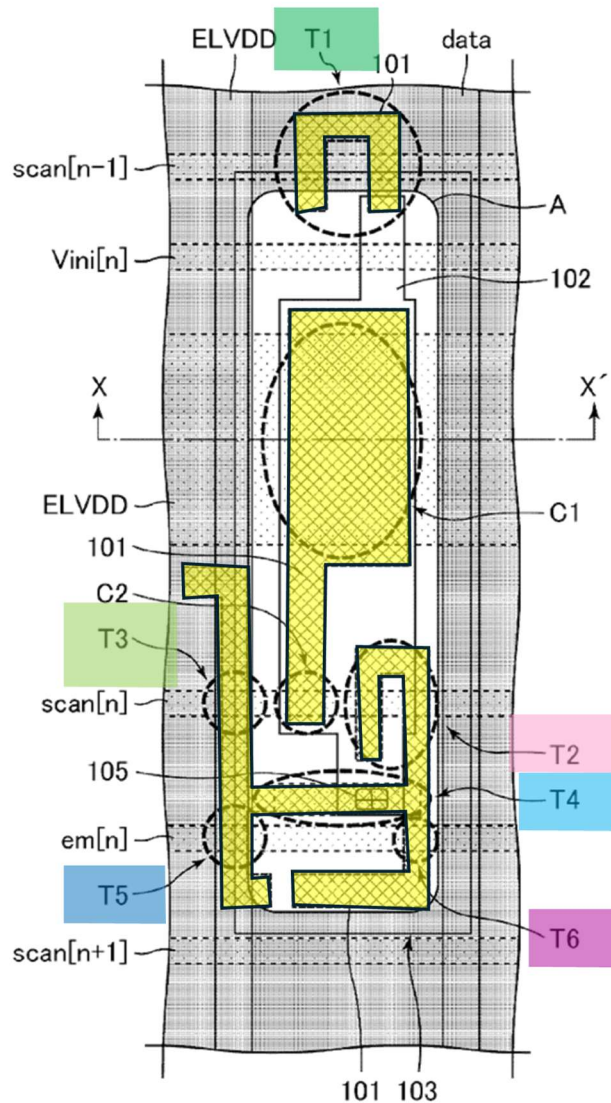


'990 patent, FIG. 1.

298. Noguchi-I additionally discloses that T4 (“the second thin film transistor”) is included in a portion of the semiconductor layer (“utilizes a semiconductor layer”). Notably, Noguchi-I’s Figure 8 is a “plan-view schematic diagram[] illustrating a pixel of a conventional organic EL display device provided with a compensation circuit.” (Noguchi-I, ¶11), which has been annotated to show

the locations of the various TFTs over the depicted semiconductor pattern (yellow).
Noguchi-I, FIG. 8 (annotated below); *see also* FIGs. 2, 4, 5, 7 (showing T4 in the same location).

Fig. 8



Noguchi-I, FIG. 8 (annotated).

299. In my opinion, it would have been understood from Noguchi-I's

description that TFT T4 (“the second thin film transistor”) includes a section of the semiconductor pattern, the semiconductor pattern is laid out in the same layer and extends to the adjacent TFT T3 (“first thin film transistor”). Noguchi-I ¶11, FIG. 8 (annotated). Furthermore, the figure makes clear that TFT T3 (“the first thin film transistor”) is electrically coupled to the semiconductor layer because it includes a section of the semiconductor pattern, which allows T3 to operate as a transistor.

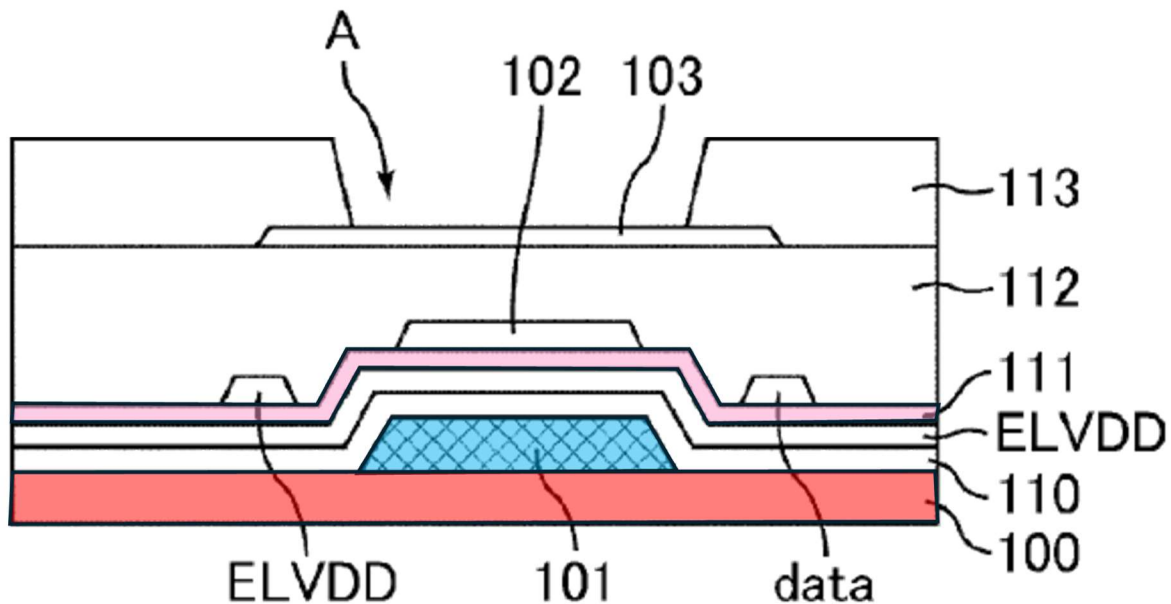
i. 1[h]: “an insulating layer covering the second thin film transistor;”

300. In my opinion, Noguchi-I teaches or suggests 1[h].

301. Noguchi-I discloses “an interlayer dielectric 110, an **interlayer dielectric 111** and an interlayer dielectric 112 are stacked [over second TFT (T4 in Noguchi-I) which is driving transistor], in this order, from the side of the substrate 100.” Noguchi-I, ¶71. As shown below in annotated Figure 9, interlayer dielectric 111 covers Noguchi-I’s semiconductor layer 101. Furthermore, it would have been understood that because Noguchi-I’s successive dielectric layers are stacked, interlayer dielectric 111 covers all structures below it, just as layers 110 and 112 also cover all structures below them. Noguchi-I further explains that the first wiring layer, which is the gate electrode of T4, is “disposed between the interlayer dielectric 110 and the interlayer dielectric 111.” Noguchi-I, ¶71. Thus, in my opinion, a POSITA would have understood that interlayer dielectric 111 specifically covers T4 (“second”

TFT).

Fig. 9



Noguchi-I, FIG. 9 (annotated).

- j. **1[ia]: “a storage capacitor electrically coupled to a gate electrode of the second thin film transistor, the storage capacitor comprising a first capacitor plate comprising a portion of the gate electrode of the second thin film transistor, a second capacitor plate over the first capacitor plate, and a portion of the insulating layer between the first capacitor plate and the second capacitor plate,**

302. In my opinion, Noguchi-I teaches or suggests 1[ia].

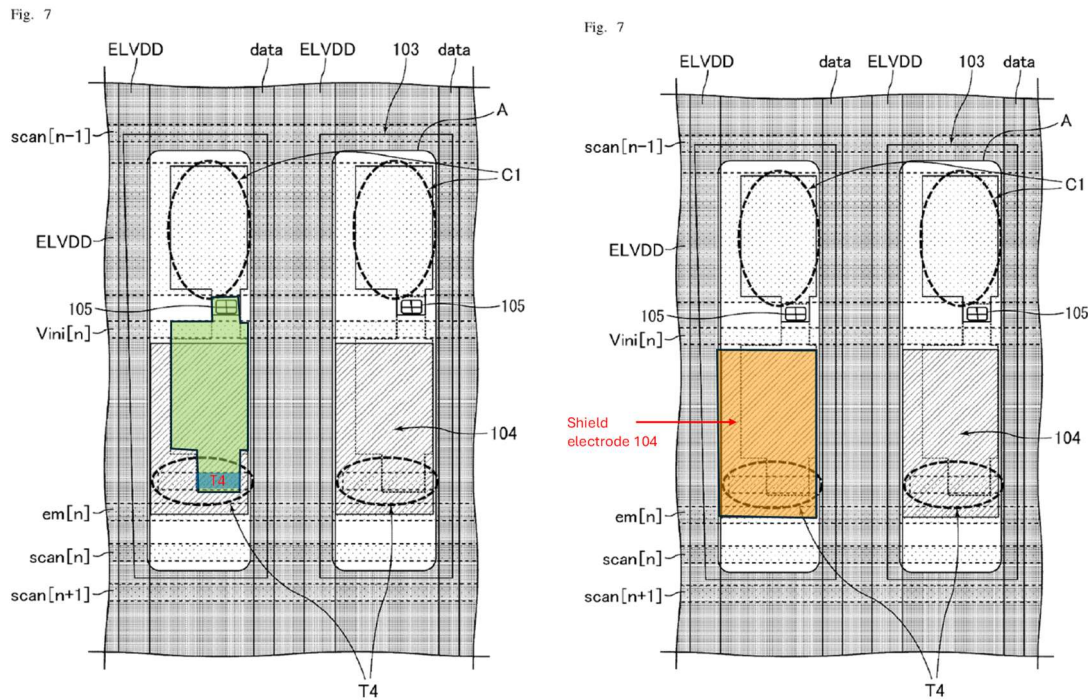
303. Noguchi-I discloses the “storage capacitor” as capacitor C1 that is connected on one side to the gate of T4 (“a gate of the second transistor”), and

includes a gate electrode 102, (“first capacitor plate”) and shield electrode 104 (“second capacitor plate”) in the second wiring layer. *See* Noguchi-I, ¶¶83-84, 86, 91-93, FIGs. 5, 7.

Noguchi-I’s Capacitor C1 Structure

304. Noguchi-I explains “capacitor C1 [is] formed through overlap of the gate electrode and the power source line ELVDD” (Noguchi-I, ¶91) and that shield electrode 104 is connected to ELVDD. *Id.*, ¶86. Furthermore, Noguchi-I explains that “[t]he gate electrode of T4 forms capacitance with the second wiring layer.” *Id.*, ¶95. Thus, Noguchi-I’s capacitor is formed in part between gate electrode 102 and shield electrode 104.

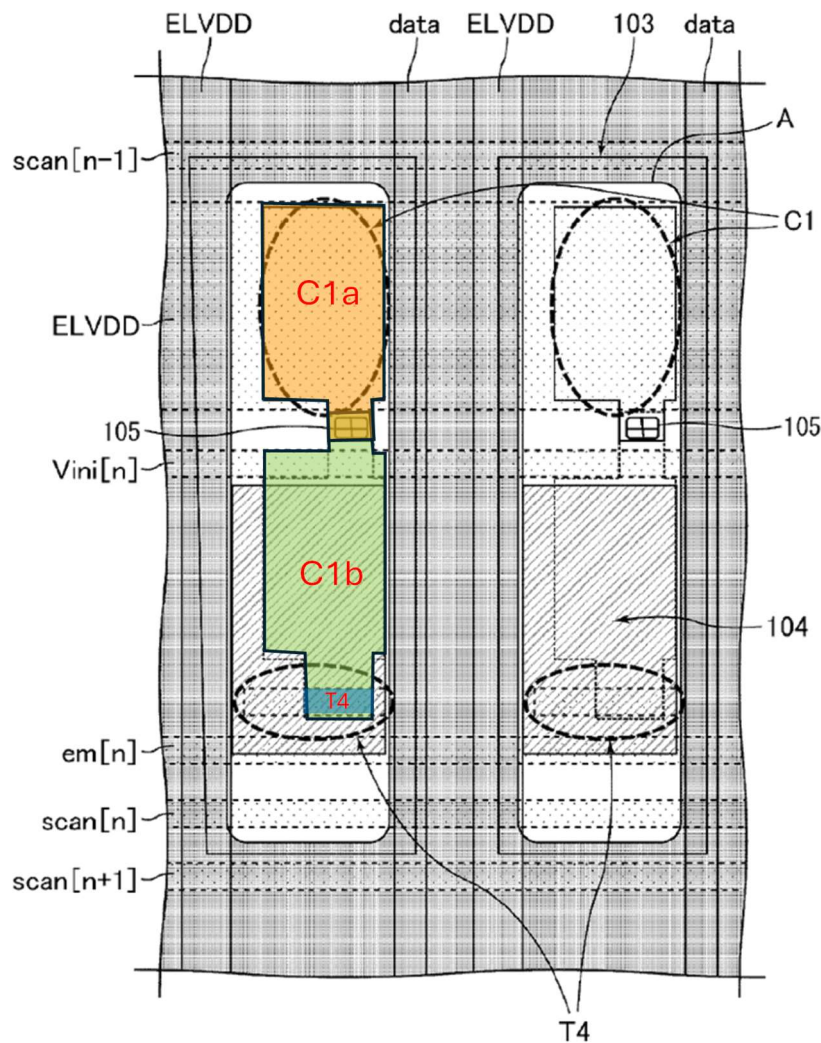
305. The capacitor configuration of Noguchi can be seen in Figure 7 (annotated below), where the gate electrode 102 (“first capacitor plate”), which operates as the gate electrode of T4, is annotated in green. Noguchi-I, ¶¶15, 70, 81, 95. Noguchi-I also shows the shield electrode 104 (“second capacitor plate”), annotated in orange.



Noguchi-I, FIG. 7 (annotated).

306. While the annotated of Figure 7 above only shows one part of capacitor C1 (C1b), Noguchi-I's capacitor C1 is made up of two parts, C1a and C1b, connected together through contact hole 105, as annotated below. *See also* Noguchi-I, ¶¶75, 77, 89, 91. Capacitor C1 has a capacitance equal to the series addition C1a and C1b. In my opinion, C1b meets the claim limitation of the storage capacitor comprising a first and second capacitor plate.

Fig. 7



Noguchi-I, FIG. 7 (annotated).

307. I have created Figure C below that illustrates a cross-section of annotated FIG. 7 (above), and more specifically, a vertical cross-section through contact via 105. I note that since the TFT in Figure C is a top-gated TFT, the source and drain contacts are formed below and are not explicitly shown in the figure.

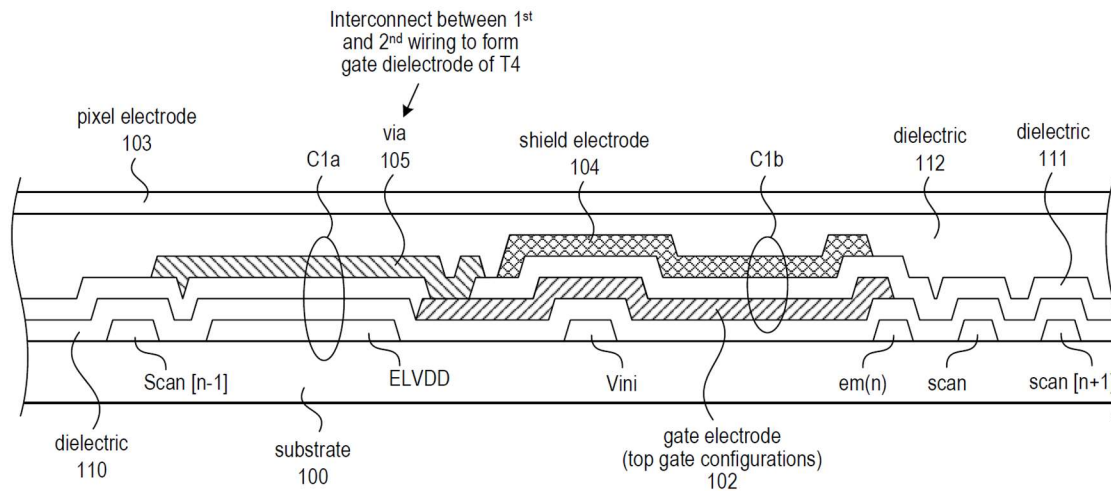
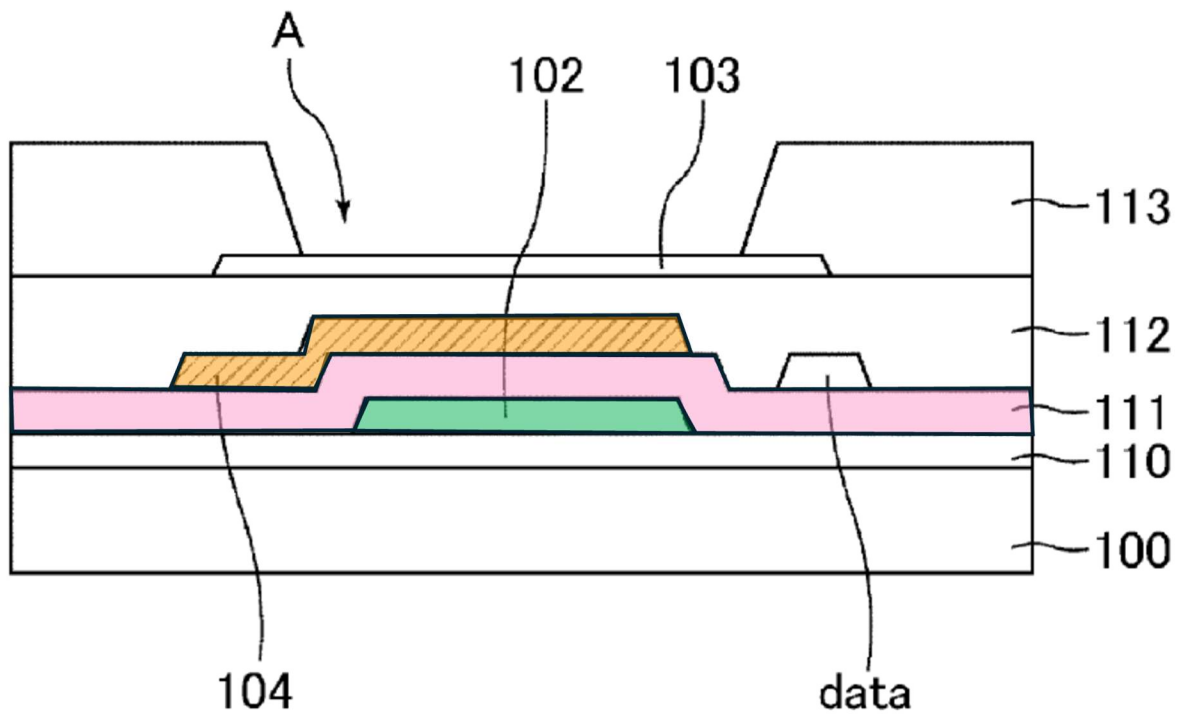


Figure C.

308. As explained above, and in view of Figure C, capacitor C1 comprises C1a and C1b, where C1b comprises a gate electrode 102 in the first wiring layer (“a first capacitor plate”) and a shield electrode 104 in the second wiring layer (“a second capacitor plate”). Noguchi-I, ¶¶91-95. Interlayer dielectric 111 is disposed between 102 and 104 (“a portion of the insulating layer between the first capacitor plate and the second capacitor plate”). *Id.*, FIG. 6 (annotated). Thus, the gate electrode 102 is part of the capacitor (“first capacitor plate comprising a portion of the gate electrode of the second thin film transistor”).

Fig. 6

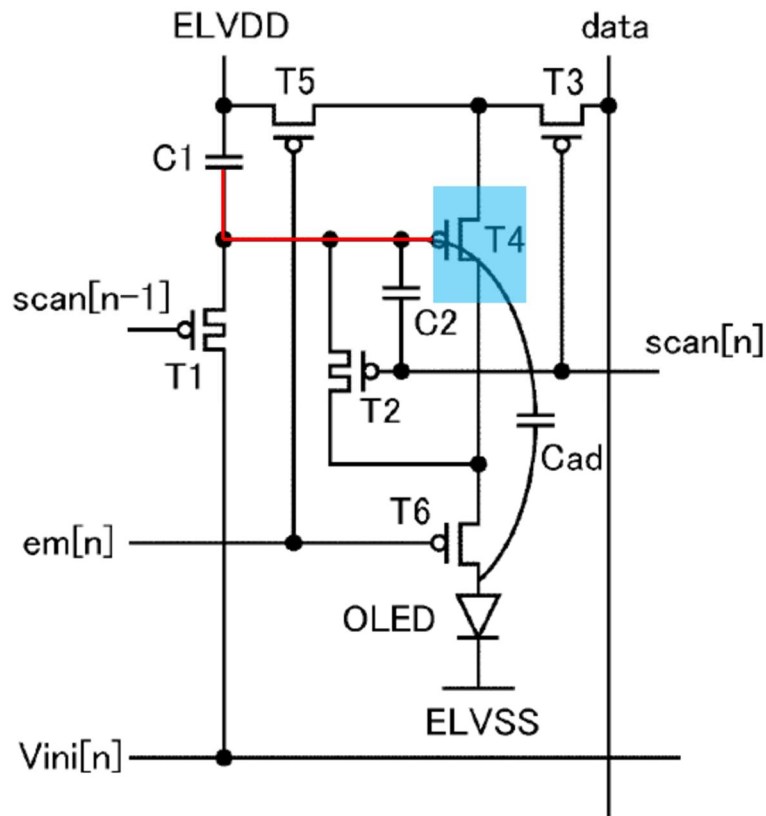


Noguchi-I, FIG. 6 (annotated).

C1 Connections

309. Noguchi-I further discloses capacitor C1 is connected to the gate electrode of T4 (“electrically coupled to a gate electrode of the second thin film transistor”), as shown by the red line in Figure 1. Noguchi-I, FIG. 1 (annotated).

Fig. 1

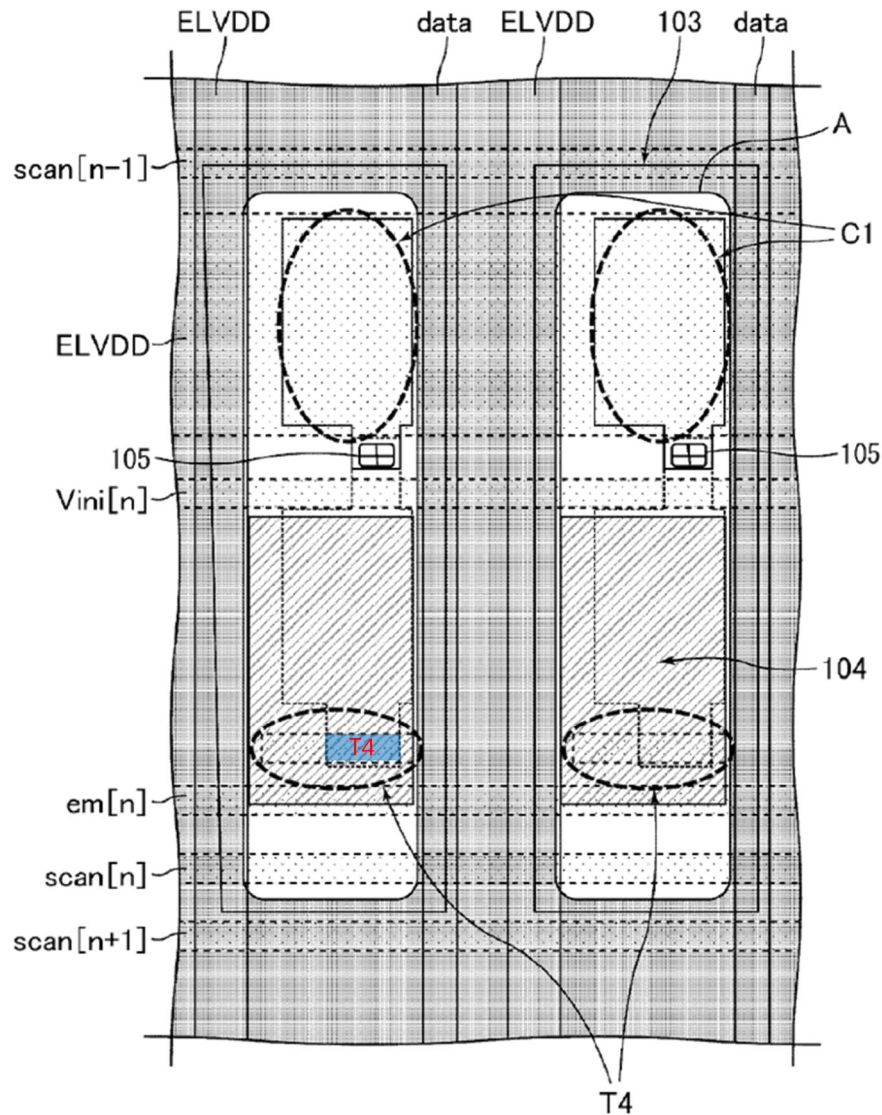


Noguchi-I, FIG. 1 (annotated).

310. Noguchi-I further indicates the position of T4 by a dashed box in Figure 7. In my opinion, the channel region of T4 is at least the portion shown in blue because it corresponds to the semiconductor layer directly under the gate electrode (“a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor”). Noguchi-I, FIG. 7 (annotated). The region indicated as T4 in Figure 7 corresponds to the same region for T4 in Figure 8, which

shows the semiconductor layer).

Fig. 7



Noguchi-I, FIG. 2 (annotated).

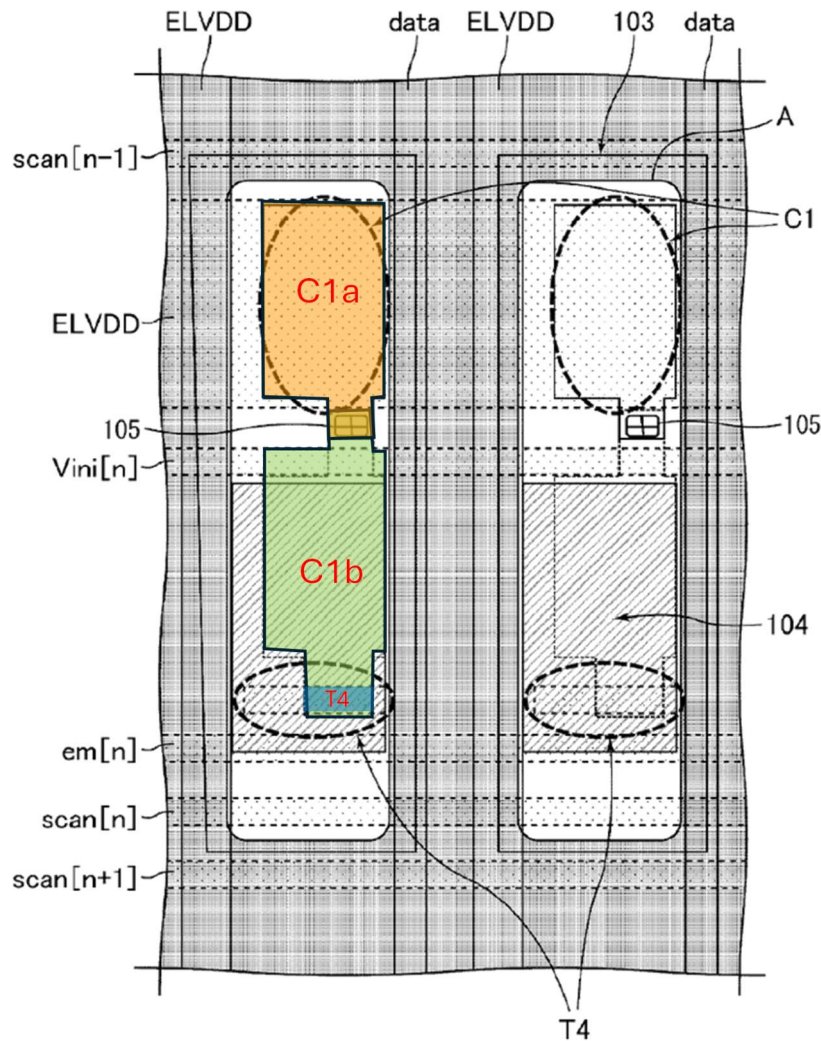
- k. 1[ib] a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor being curved ;”

311. In my opinion, Noguchi-I in view of Udagawa teaches or suggests 1[ib].

312. As explained above in Ground 1A for 1[ib], Udagawa teaches a “serpentine” or “curved” channel of drive transistor T4. §VIII.A.4.k. For the reasons explained in §VIII.A.1, a POSITA would have been motivated to incorporate Udagawa’s driving TFT gate shapes (thereby increasing the channel length) in Noguchi-I’s OLED driving circuit to reduce the dispersion effects that accompany the reduction in size of the TFT driving circuit without a curved channel. Furthermore, modifying Noguchi-I to use Udagawa’s longer gate channel is in line with Noguchi-I’s objectives of reducing the influence of parasitic capacitance, C_{ad} , because forming the gate channel in this way allows for a reduction of dispersion without significantly increasing C_{ad} because Noguchi-I’s shield electrode (second capacitor plate) effectively reduces the parasitic capacitance, while maintaining a compact footprint. Thus, for the same reasons as explain in §VIII.A.4.k, Noguchi-I in combination with Udagawa teaches or suggests “a channel region of the semiconductor layer...of the second thin film transistor being curved.”

313. Furthermore, as explained in 1[ia], capacitor C1 is comprised of C1a and C1b, as shown in annotated Figure 7 below. §VIII.A.3.j.

Fig. 7



Noguchi-I, FIG. 7 (annotated).

314. In my opinion, Noguchi-I indicates the position of T4 by a dashed box in Figure 7. In my opinion, a POSITA would have understood the channel region of T4 is at least the portion shown in blue because it corresponds to the semiconductor layer directly under the gate electrode. Noguchi-I, FIG. 7 (annotated). That is, in view of §VI.C that discusses interpreting circuit diagrams, plan layouts, and cross-

sectional views, the region indicated as T4 in FIG. 7 corresponds to the same region for T4 in FIG. 8 of Noguchi-I, which shows the semiconductor layer. Noguchi-I further discloses that the semiconductor layer is disposed within the region A, as shown in Figures 2, 4, 5, 7, and 8. Noguchi-I, ¶70. Thus, although the semiconductor layer is not shown in Figures 2, 4, 5, and 7, it is my opinion that a POSITA would have understood that the channel of T4 (as identified in the figures) would have the same configuration, comprising the vertical portion of the semiconductor layer of T2 or T6.

315. Thus, a POSITA would have found it obvious that the gate electrode of T4 (i.e., the green-annotated plate in the above figure) covers the channel region of T4, including its bent or curved region (“bent portion of the second portion of the semiconductor layer is under the first capacitor plate”) when modified by Udagawa.

316. Accordingly, limitation 1[ib] is disclosed by Noguchi-I in view of Udagawa.

I. 1[j]: “a third thin film transistor electrically coupled to the second thin film transistor, the corresponding organic light emitting diode, and the first capacitor plate, the semiconductor layer being extended to and electrically coupled to the third thin film transistor;”

1[k]: “a fourth thin film transistor electrically coupled to the first voltage line and the second thin film transistor, the semiconductor layer being extended to and is electrically coupled to the fourth thin film

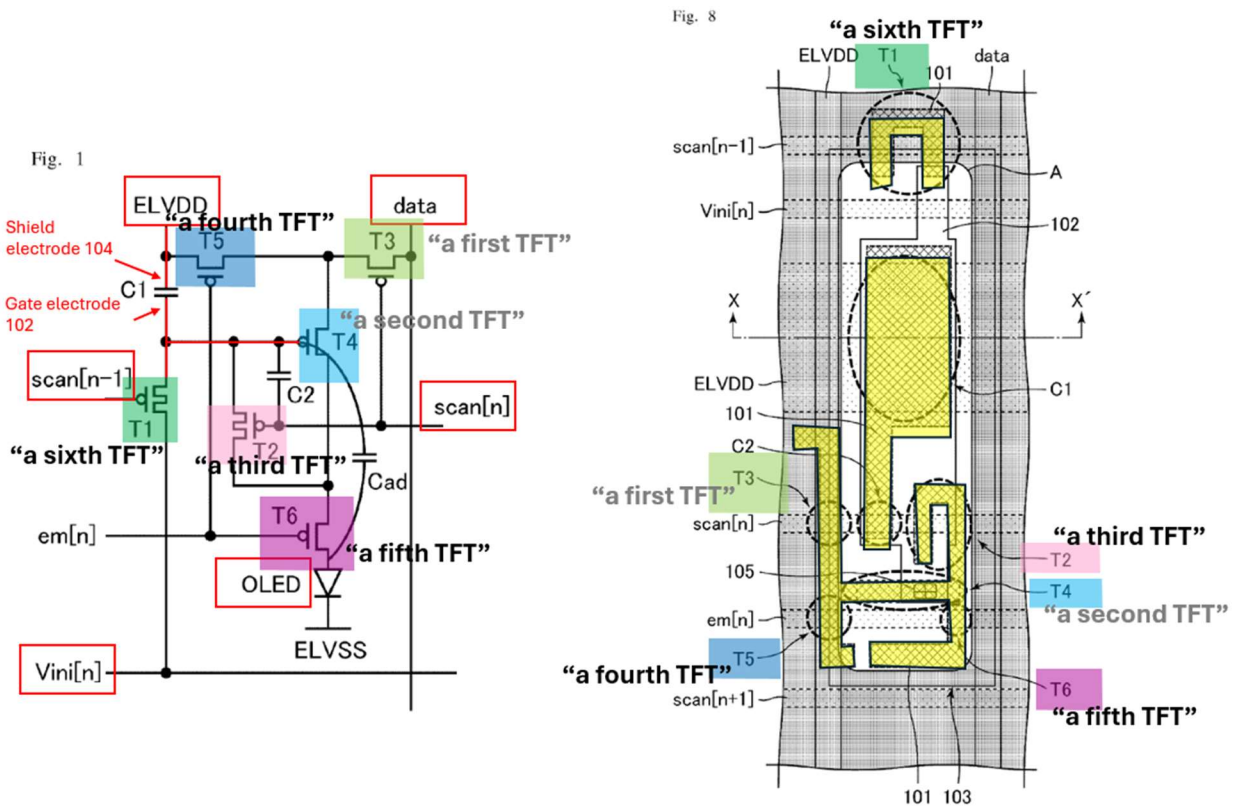
transistor;”

1[l]: “a fifth thin film transistor electrically coupled to the second thin film transistor, the third thin film transistor, and the corresponding organic light emitting diode, the semiconductor layer being extended to and is electrically coupled to the fifth thin film transistor; and”

1[m]: “a sixth thin film transistor electrically coupled to the second voltage line, the third thin film transistor, and the first capacitor plate, the semiconductor layer being extended to and is electrically coupled to the sixth thin film transistor.”

317. In my opinion, Noguchi-I discloses limitations 1[j]-1[m].

318. I have grouped each of the limitations 1[j]-1[m], which are directed to the third through sixth TFTs, for clarity and ease of discussion, and have further annotated FIGS. 1 and 8 of Noguchi-I to show the mapping of the transistors. Additionally, a table following the annotated figures of Noguchi-I shows the mapping for each transistor across Claim 1, the '990 Patent, and Noguchi-I.



Left: Noguchi-I, FIG. 1 (annotated); Right: Noguchi-I, FIG. 8 (annotated).

Claim 1	'990	Noguchi-I	Function
1 st TFT	T2	T3	Data input switching TFT
2 nd TFT	T1	T4	Driving TFT
3 rd TFT	T3	T2	Scan[n] / Compensation TFT
4 th TFT	T5	T5	Power supply / Operation control TFT
5 th TFT	T6	T6	Light emission control TFT
6 th TFT	T4	T1	Scan[n-1] Init switch TFT
Capacitor	Cst	C1	Storage Capacitor
First Capacitor Plate	125h	Gate electrode 102	
Second Capacitor Plate	127	Shield electrode 104	
1 st Voltage line	ELVDD	ELVDD	Power supply

2 nd Voltage line	V _{int}	V _{ini} [n]	Capacitor initialization voltage
OLED	OLED	OLED	
1 st Scan line	S _n	scan[n]	Current scan line
2 nd Scan line	S _{n-1}	scan[n-1]	Previous scan line
Light emission control line	E _n	em[n]	Light emission control
Data line	D _m	data	Data/OLED intensity voltage

319. As explained in 1[pre] and 1[f], Noguchi-I discloses a TFT driving circuit with at least six transistors and one capacitor. §§VIII.A.3.a, VIII.A.3.g. And as I explain below, Noguchi-I discloses each of the recited transistors and connections.

320. Regarding 1[j], Noguchi-I discloses T2 (“third thin film transistor”) connected to T4 and gate electrode 102. Noguchi-I, FIG 1. T2 is additionally connected to OLED through T6, just as T4 is. As explained above for 1[g], it is understood that the arrangement of T2, with connection to OLED through adjacent TFTs is the same configuration as disclosed in the ’990 Patent. *See* ’990Pat., 6:61-65 (“T3 is coupled via the light emission control thin film transistor T6 to the anode 65 of the OLED”).

321. Regarding 1[k], Noguchi-I discloses T5 (“fourth thin film transistor”) connected to V_{dd} and T4. Noguchi-I, FIG 1.

322. Regarding 1[l], Noguchi-I discloses T6 (“fifth thin film transistor”) connected to T4, T2, and OLED. *Id.*

323. Regarding 1[m], Noguchi-I discloses T1 (“sixth thin film transistor”) connected to Vini[n], T2, and gate electrode 102. *Id.*

324. Accordingly, Noguchi-I discloses the electrical connections in 1[k]-1[m].

325. Each of transistors T1 to T6 utilize and include a portion of the semiconductor layer, which is thus electrically coupled to the corresponding transistor. Noguchi-I, ¶¶11, 64, 70. Even though the portion of the semiconductor pattern that reaches transistor T1 in Noguchi-I is not contiguous with the remaining sections of the semiconductor pattern, Noguchi-I explains that each of the TFTs are disposed in a single layer. Noguchi-I, ¶70 (“A semiconductor layer of the Transistors T1 to T6”). Further, as shown in annotated FIG. 8 above,³ Noguchi-I’s semiconductor layer reaches all transistors (“the semiconductor layer being extended to and electrically coupled to”). Noguchi-I, ¶64, FIG. 8.

326. Accordingly, Noguchi-I discloses each of the limitations 1[j]-1[m].

³ Figure 8 provides an example layout for Noguchi-I’s pixel. To the extent that Figure 7 requires a modified layout, it would have been well within the knowledge and skill of a POSITA to move transistors.

4. **Claim 2: “The organic light emitting diode display according to claim 1, wherein gate electrodes of the fourth and fifth thin film transistors are coupled together.”**

Claim 3: “The organic light emitting diode display according to claim 2, wherein the gate electrodes of the fourth and fifth thin film transistors are configured to receive a signal from a light emission control line.”

Claim 4: “The organic light emitting diode display according to claim 1, wherein a gate electrode of the sixth thin film transistor is configured to receive a signal from a second scan line.”

Claim 5: “The organic light emitting diode display according to claim 1, wherein gate electrodes of the first and third thin film transistors are coupled together.”

Claim 6: “The organic light emitting diode display according to claim 5, wherein the gate electrodes of the first and third thin film transistors are configured to receive a signal from the first scan line.”

Claim 7: “The organic light emitting diode display according to claim 1, wherein the second capacitor plate is electrically coupled to the first voltage line.”

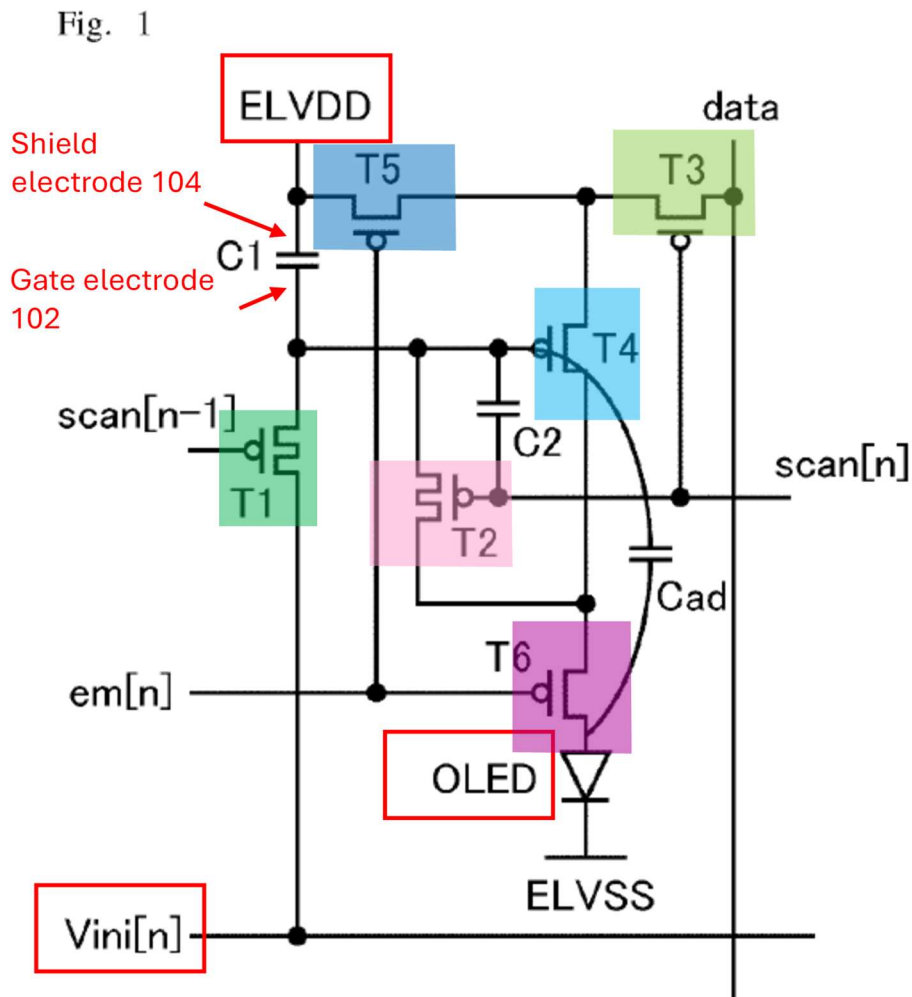
Claim 23: “The organic light emitting diode display according to claim 1, wherein the third thin film transistor is electrically coupled to the gate electrode and a drain electrode of the second thin film transistor.”

327. In my opinion, Noguchi-I in combination with Udagawa discloses claims 2-7 and 23.

328. I have grouped each of claims 2-7 and 23, which are directed to the connectivity of various components in the driving circuit of the '990 Patent, for

clarity and ease of discussion.

329. As explained in 1[pre], 1[f], 1[g], and 1[j], Noguchi-I discloses a TFT driving circuit with at least six transistors and one capacitor. §§VIII.A.3.a, VIII.A.3.g, VIII.A.3.h, VIII.A.3.i. As explained below and shown in annotated Figure 1, Noguchi-I discloses each of the recited transistors and connections.



Noguchi-I, FIG. 1 (annotated).

330. Claim 2: Noguchi-I discloses that the gates of T5 (“fourth” TFT) and T6 (“fifth” TFT) are connected together. Noguchi-I, FIGs. 1, 8.

331. Claim 3: Noguchi-I further discloses that the gates of T5 and T6 receive the signal em[n]. Noguchi-I, ¶11, FIG. 1, 8. Noguchi-I explains that “em[n] denotes an n-th emission control line.” *Id.* A POSITA would have understood that EM was “a signal from a light emission control line” because when EM is applied to T5 and T6, the transistors turn on allowing drive transistor T4 to provide current to OLED, thus allowing the emission of light.

332. Claim 4: Noguchi-I further discloses T1 (“sixth” TFT) receives scan[n-1] (“a second scan line”) at its gate. Noguchi-I, ¶11, FIGs. 1, 2.

333. Claim 5: Noguchi-I further discloses T3 (first” TFT) and T2 (“third” TFT) are connected together. Noguchi-I, FIGs. 1, 8.

334. Claim 6: Noguchi-I further discloses that the gates of T3 and T2 receive scan[n] (“first scan line”). Noguchi-I, ¶11.

335. Claim 7: Noguchi-I discloses shield 104 (“second capacitor plate”) connected to ELVDD (“first voltage line”). Noguchi-I, ¶¶86, 91, FIGs. 1, 6, 7.

336. Claim 23: as shown in Figure 1, the drain of T4 (“second” TFT) is connected to the source of T2 (“third” TFT). Noguchi-I, ¶11, FIGs. 1, 8. The gate electrode of T4 is connected to the drain of T2.

337. To the it is argued that Noguchi-I does not explicitly show a drain “electrode” of the second thin film transistor, as explained above in Ground 1, it would have been understood that, consistent with the ’990 patent’s description, the drain and source regions of the semiconductor are doped and themselves form drain and source “electrodes.” §VIII.A.5.

5. Claim 8: “The organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.”

338. In my opinion, Noguchi-I in combination with Udagawa teaches or suggests claim 8.

339. Noguchi-I teaches that shield electrode 104 (“second capacitor plate”) covers gate electrode 102 (as shown in annotated Figures 6 and 7 below). Noguchi-I, ¶83 (“shield electrode 104 forms a region covering the gate electrode 102”), ¶92 (same), FIGs. 6 (annotated), 7 (annotated). Shield electrode 104 (large orange box at bottom of Figure 7) in annotated Figure 7 below covers a periphery of gate electrode 102 (“completely surrounds a periphery of the first capacitor plate in a plan view”). As explained above in §VIII.A.3 (Ground 1B), it would have been understood that at least a portion around the outside of the first capacitor plate is surrounded.

6. **Claim 9: “The organic light emitting diode display according to claim 1, wherein portions of the semiconductor layer are doped with N-type impurities.**

Claim 10: “The organic light emitting diode display according to claim 1, wherein portions of the semiconductor layer are doped with P-type impurities.”

341. In my opinion, Noguchi-I in combination with Udagawa teaches or suggests claims 9 and 10.

342. Noguchi-I discloses that its driving circuit uses p-channel TFTs. Noguchi-I, FIG. 1. It further explains that it uses a semiconductor layer with ion implantation (doping) to form its TFTs. *Id.*, ¶63. Noguchi-I, however, does not expressly state what type of ion implantation it uses to form the TFTs.

343. As explained above in Ground 1A, Udagawa discloses that P- and N-type impurities are doped into p-channel TFT transistors formed in the semiconductor layer PO. §§VIII.A.6, VIII.A.7. Accordingly, for the same reasons as explained above in Ground 1A, the Noguchi-I-Udagawa combination teaches or suggests claims n-type and/or p-type impurities doped into portions of the semiconductor layer.

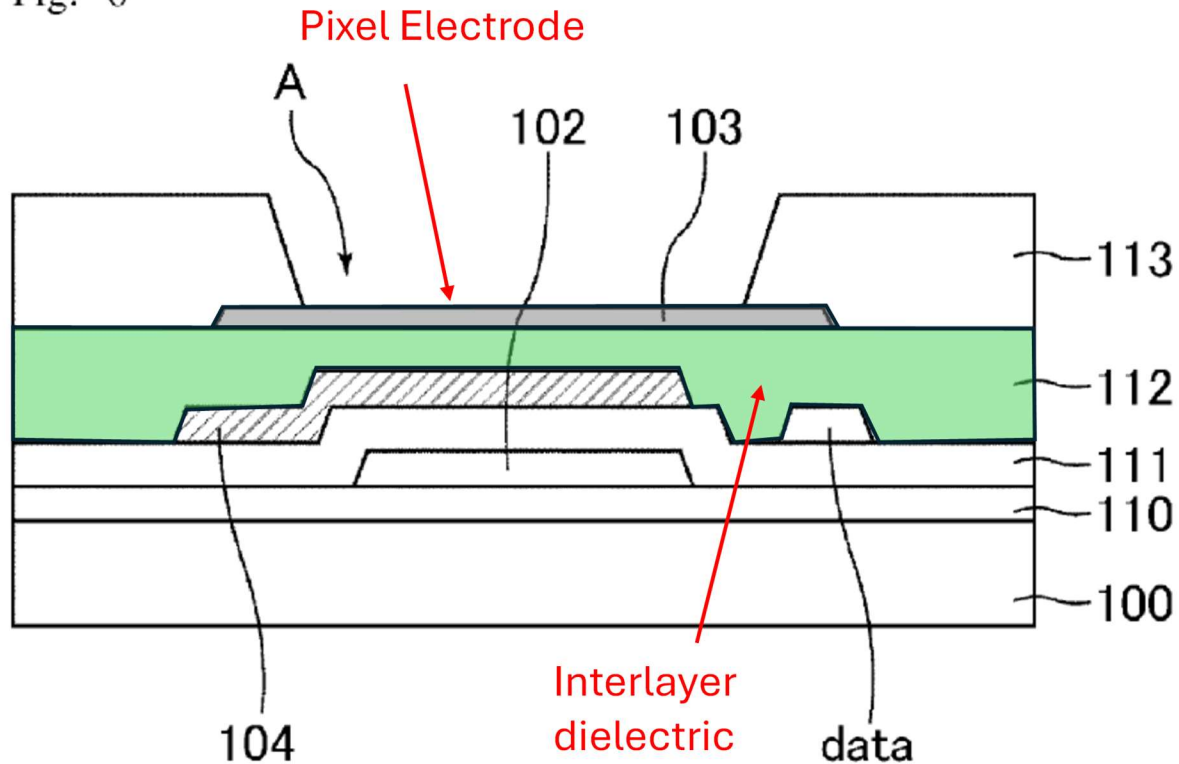
7. **Claim 24: “The organic light emitting diode display according to claim 1, further comprising a protective layer covering the plurality of driving circuits, wherein each of the organic light emitting diodes further comprises a pixel electrode on the protective layer, the pixel electrode being electrically coupled to the second thin film transistor through a contact hole.”**

Claim 25: “The organic light emitting diode display according to claim 1, further comprising a protective layer covering the plurality of driving circuits, wherein each of the organic light emitting diodes further comprises a pixel electrode on the protective layer, the pixel electrode being electrically coupled to a drain electrode of the fifth thin film transistor through a contact hole.”

344. In my opinion, Noguchi-I in combination with Udagawa discloses claims 24 and 25.

345. As shown in annotated FIG. 6, Noguchi-I discloses interlayer dielectric 112 (“protective layer”) is disposed on interlayer dielectric 111 and interlayer dielectric 110 covering the TFTs and capacitor (“covering the plurality of driving circuits”) and under a pixel electrode. Noguchi-I, ¶¶71, 87, FIGs. 3, 6, 9. The pixel electrode is disposed on the interlayer dielectric 112 (“each of the organic light emitting diodes further comprises a pixel electrode on the protective layer”).

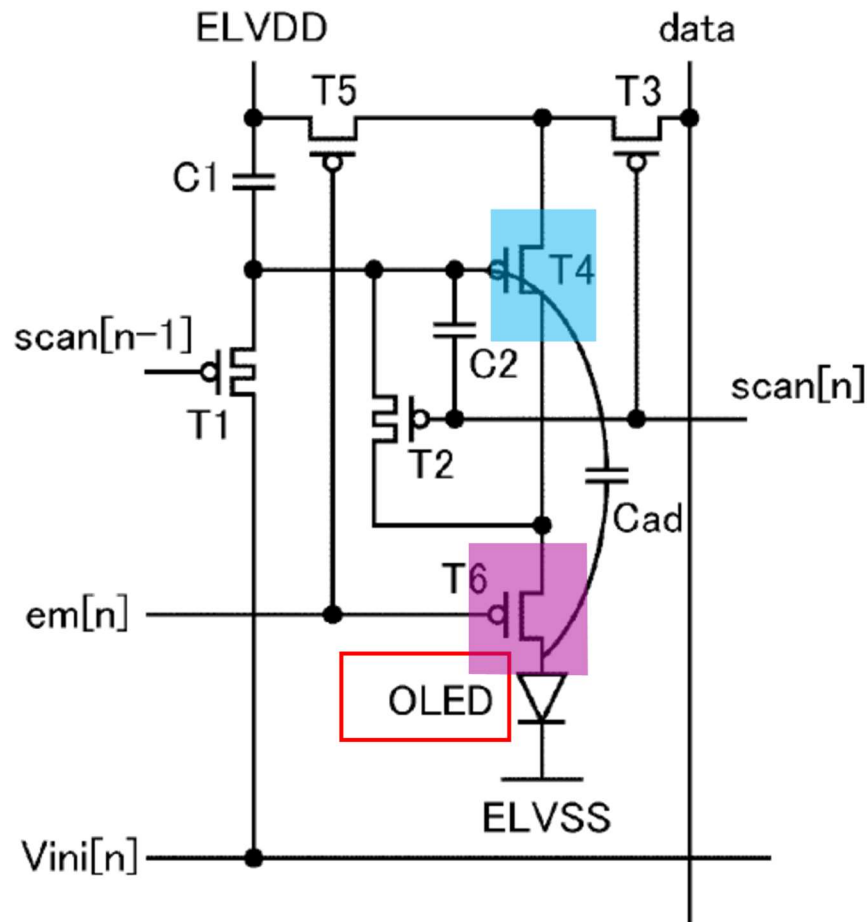
Fig. 6



Noguchi-I, FIG. 6 (annotated).

346. Noguchi-I further explains that the pixel electrode is connected to the drain of T6. *Id.*, ¶11, FIG. 1. As explained above in 1[g], T4 (“second” TFT) is connected to OLED (and the pixel electrode) through T6 (“pixel electrode being electrically coupled to the second thin film transistor”). §VIII.A.3.h.

Fig. 1



Noguchi-I, FIG. 1 (annotated).

347. Claim 24 requires the pixel electrode to be “electrically coupled” to T4 “through a contact hole,” while claim 25 requires the pixel electrode to be “electrically coupled” to T6 “through a contact hole.” As shown annotated Figure 1 above, the pixel electrode is connected to T6, and T4 is connected to T6. Therefore, Noguchi-I teaches that the pixel electrode is electrically coupled to both T4 and T6.

Additionally, a typical way to connect T6 to the pixel electrode (anode of OLED (Noguchi-I, ¶41)) is through a via (“contact hole”). Vias are well-known in the art and commonly used to connect structures on different levels of a semiconductor structure. Furthermore, Noguchi-I suggests using vias, as shown by its disclosure of contact hole 105. Noguchi-I, ¶¶75, 89. Thus, it would have been obvious to use a via to connect the drain of T6 to the pixel electrode, and to thereby “electrically couple[]” the pixel electrode to each of T6 and T6 through the contact hole.

348. Accordingly, Noguchi-I discloses claims 24 and 25.

8. Claim 26: “The organic light emitting diode display according to claim 1, wherein the first capacitor plate and the first scan line are in the same material layer.”

349. In my opinion, Noguchi-I alone in combination with Udagawa teaches or suggests claim 26.

350. As explained above in 1[ia], Noguchi-I teaches a storage capacitor where the gate electrode 102 (“first capacitor plate”) is the gate electrode of T4. §VIII.A.3.j. Noguchi-I explains that scan[n] (“the first scan line”) is in the first wiring layer. Noguchi-I, ¶68, FIG. 2. Noguchi-I further discloses that gate electrode 102 is also in the first wiring layer (“same material layer”). *Id.*, ¶75, FIG. 45. Noguchi-I further explains that a “wiring layer is ordinarily low-resistance wiring (metal wiring)” (*id.*, ¶63), which would have made it obvious that the metal components, including the first capacitor plate and the first scan line, in the first

wiring layer were made of the same material.

9. **Claim 27: “The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “S”-shape.”**

Claim 28: “The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a partial “S”-shape.”

Claim 29: “The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “M”-shape.”

Claim 30: “The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “W”-shape.”

351. As explained above in Ground 1A, utilizing Udagawa’s serpentine channel shape for drive transistor T4, many different apparent shapes are realized. §VIII.A.9. Noguchi-I in combination Udagawa teaches or suggests claims 27-30 for the same reasons as explained above. §VIII.A.9.

E. Ground 2B: claims 11-20 are Unpatentable over Noguchi-I, Udagawa, Noguchi-II, and Jeong

1. Summary of Noguchi-II

352. Noguchi-II discloses a circuit diagram of a pixel of an organic EL display device is configured similarly to the circuit shown in Figure 1 of the ’990 patent (i.e., with scan lines, data lines, and six transistors), but additionally includes a transistor T7 as an adjusting transistor for adjusting the voltage of a pixel electrode

of an organic EL element OLED, i.e., a seventh transistor. Noguchi-II, ¶¶77, 90-91.

353. In my opinion, Noguchi-II is analogous art to the '990 patent because it is in the same field of endeavor. For example, both are directed to compensating the threshold voltage of the driving transistor. Noguchi-II, ¶42. Furthermore, Noguchi-II, which shares the same inventor as Noguchi-I.

354. Noguchi-II teaches transistor T7 is an adjusting transistor for adjusting the voltage of a pixel electrode of an organic EL element OLED. *Id.*, ¶77. Herein, the source electrode and the drain electrode of the transistor T7 are connected in parallel to the organic EL element OLED. Consequently, the voltages of the anode and cathode of the organic EL element OLED may be the same as each other. This enables discharge of charge, which is stored in the Cad, through a power supply line ELVSS using the transistor T7 as a path for electric current. As a result, display characteristics without any occurrences of the stepwise response characteristics can be achieved. *Id.*, ¶91.

2. Summary of Jeong

355. Jeong (EX1009) describes a circuit of a pixel having an improved response time that is configured similarly to the circuit shown in Figure 1 of the '990 Patent and Noguchi-I (i.e., with scan lines, data lines, and six transistors). Jeong, Abstract. The 6T1C circuit of Jeong can be configured such that the initialization power supply for supplying the initialization voltage (VINT) of the pixel can be set

to the same voltage source as a power supply that supplies a low potential pixel power from the outside (ELVSS). *Id.*, ¶¶40, 52.

356. In my opinion, Jeong is analogous art to the '990 Patent because it is in the same field of endeavor. For example, both are directed to compensating the threshold voltage of the driving transistor. Jeong, ¶¶85-86, 89.

3. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, and Jeong

357. In my opinion, there are several reasons that motivate the combination of Noguchi-I and Noguchi-II.

358. As discussed above, Noguchi-I is directed to the pixel structure of an OLED display (in a 6T1C circuit configuration), which is susceptible to visual aberrations that are likely caused by the Cad. Noguchi-I, ¶¶12, 15, 17, 70.

359. Noguchi-II proposes adding an additional adjusting transistor, i.e., a seventh transistor, to the 6T1C circuit to achieve display characteristics without any occurrences of the visual aberration. Noguchi-II, ¶¶77, 91.

360. It would have been obvious to combine the complementary teachings of Noguchi-I with Noguchi-II to reduce the Cad, and specifically add Noguchi-II's seventh (adjusting) TFT to Noguchi-I's pixel structure of the OLED display.

361. In my opinion, a POSITA would have been skilled enough to add a seventh TFT to Noguchi-I's pixel structure to achieve the known and predictable

result of reducing the Cad. Furthermore, adding a seventh TFT to a 6T1C circuit to reduce parasitic capacitance was well-known by 2012, as evidenced by the teachings of Noguchi-II. Additionally, a POSITA would have also combined Noguchi-I with Jeong with the understanding that Vini[n] is the same voltage source as ELVSS. Jeong, ¶¶52, 54. Setting Vini[n] to ELVSS is merely a design choice. *Id.*, ¶52 (“initialization power supply supplying...may be supplied according to the design structure of the pixel”).

362. Furthermore, and as discussed above, the Noguchi-I reference can be combined individually with each of Udagawa and Noguchi-II. In each instance, the combination involves modifying a distinct aspect of Noguchi-I, and these modifications are independent of one another. For example, Udagawa teaches modifying the shape of T4’s gate channel to a serpentine shape and Noguchi-II teaches modifying the 6T1C circuit to incorporate a seventh TFT. A POSITA would have recognized that there is no interference among the modifications, and each combination can be implemented without affecting the others. Accordingly, a POSITA would have found it obvious to combine Noguchi-I with each of Udagawa and Noguchi-II and would have had a reasonable expectation of success.

363. Additional details regarding the Noguchi-I–Udagawa–Noguchi-II–Jeong combination are provided below in connection with specific claim

limitations.

4. **Claim 11: “The organic light emitting diode display according to claim 1, further comprising a seventh thin film transistor electrically coupled to the second voltage line, the fifth thin film transistor, and the corresponding organic light emitting diode.”**

364. In my opinion, Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong teach or suggest claim 11.

365. Noguchi-I discloses that its driving circuit can have more than or less than six TFTs. Noguchi-I, ¶95 (“TFTs and so forth have been omitted in the figures.”). As explained above, Noguchi-II discloses an OLED drive circuit similar to those described in Noguchi-I and in Figure 10 of the ’990 patent, which additionally includes a seventh TFT. §VIII.A.1. Figure 10 from the ’990 Patent and Figure 6 from Noguchi-II have been reproduced below, highlighting the seventh TFT.

Fig. 6

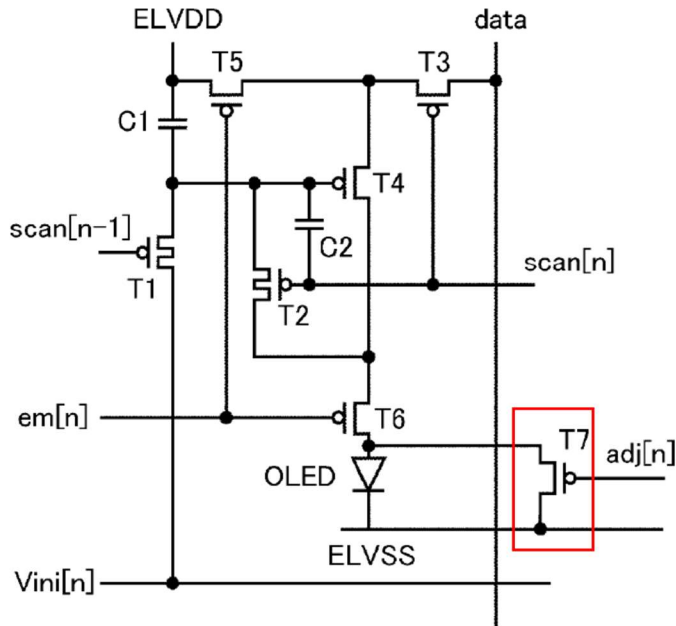
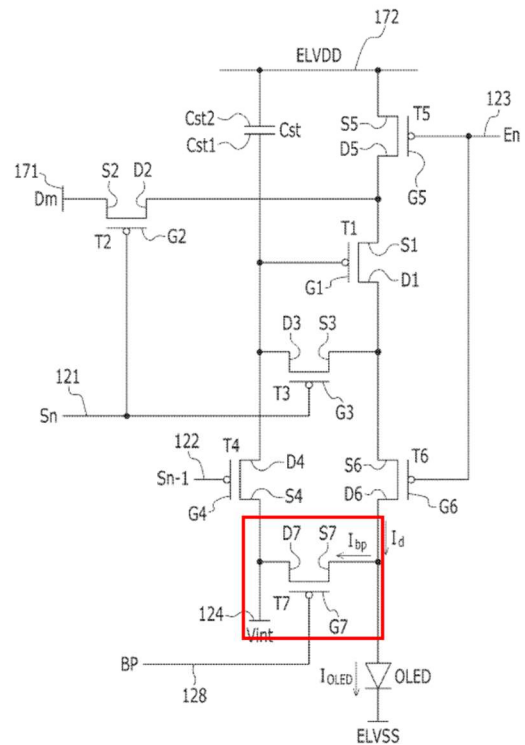


FIG. 10



Left: Noguchi-II, FIG. 6 (annotated); Right: '990Pat., FIG. 10 (annotated).

366. As shown below, Noguchi-II's circuit is nearly identical to Noguchi-I, except for the additional seventh TFT (T7).

Fig. 6

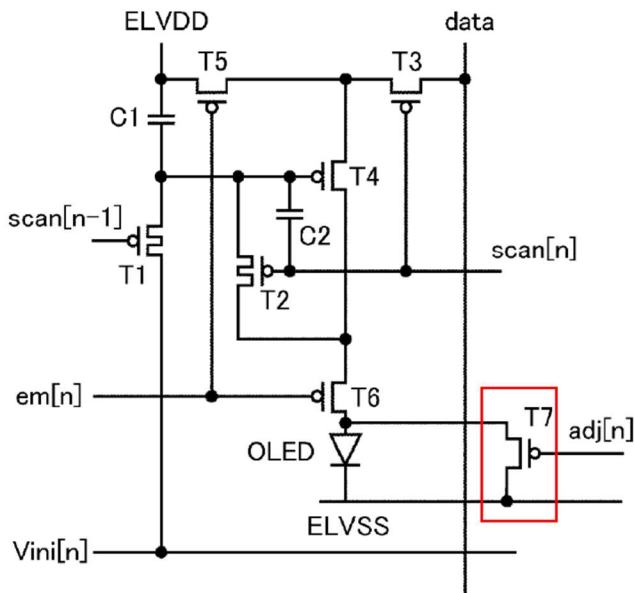
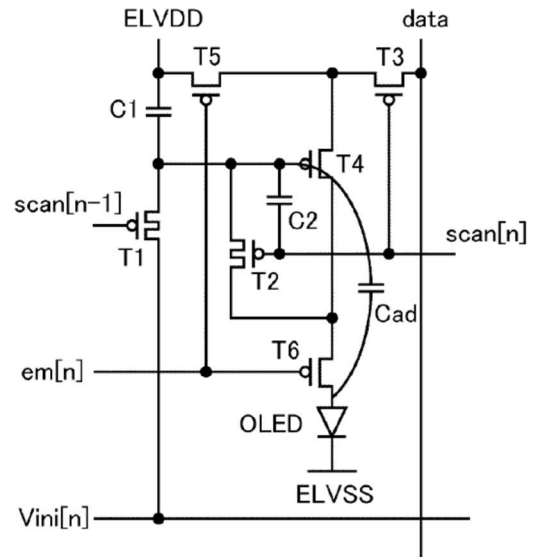


Fig. 1



Left: Noguchi-II, FIG. 6 (annotated); Right: Noguchi-I, FIG. 1.

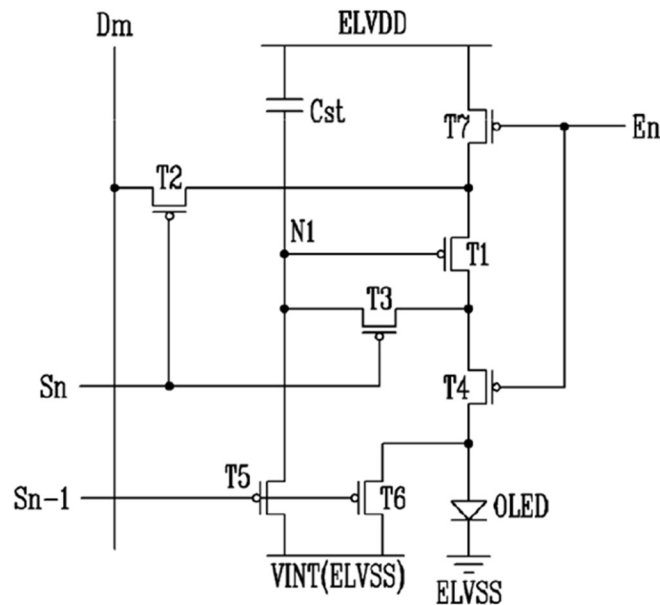
367. Noguchi-II discloses T7 in Figure 6 connected (“electrically coupled”) to T6 (“fifth thin film transistor”) and OLED (“the corresponding organic light emitting diode”). Noguchi-II, ¶¶77, 90-91. Noguchi-II explains the addition of T7 prevents “occurrence of the stepwise response characteristics” that occurs because of parasitic capacitance, Cad . *Id.*, ¶¶16, 91.

368. In my opinion, there is motivation to modify Noguchi-I to incorporate Noguchi-II’s seventh TFT to further reduce the effects of parasitic capacitance, Cad . For example, introducing the additional seventh transistor for adjusting voltage of the pixel electrode reduces the voltage difference between pixel electrode and gate voltage of drive transistor. Such a modification would have improved the

performance of Noguchi-I drive circuit with minimal increase in size. Furthermore, as shown above, Noguchi-II and Noguchi-I's circuits are identical except for the additional TFT.

369. While Noguchi-II shows the drain of T7 is connected to ELVSS (and the drain of T1 is connected to Vini[n]), it was well-known at the time of the '990 Patent that the initialization voltage Vini[n] and ELVSS could be connected together. The connection between Vini[n] and ELVSS is a fundamental design feature in AMOLEDs, and allows the establishment of a common reference point or "ground" for the entire display subsystem. By connecting Vint and ELVSS together, the designers tie the Vint ground to the ELVSS ground, which creates a single, unified 0V reference point for the entire display system. This is specifically shown in Jeong, ¶¶52 ("the third power supply supplying the third power (VINT)... may be set to the same voltage source as the second power supply supplying the second power (ELVSS)."), 54, FIG. 2. Thus, it would have been understood that Vini[n] ("second voltage line") and ELVSS are connected to the same voltage source (or line). Indeed, Noguchi-II confirms this understanding by explaining that Vini[n] discharges capacitors C1 and C2, which occurs when Vini[n] is set to ELVSS. Noguchi-II, ¶¶8, 24; Noguchi-I, ¶23. Accordingly, it would have been obvious that, in the combination, T7 is connected to Vini[n]/ELVSS ("second voltage line").

FIG. 2



Jeong, FIG. 2.

370. As explained above in §VIII.A.3, the motivation to combine such teachings, e.g., to incorporate an additional TFT into the 6T1C pixel circuit, would have been straightforward, and an obvious addition to improve the functionality of the drive circuit because Noguchi-I and Noguchi-II share the same inventor and describe the same pixel circuit. *Compare* Noguchi-I, FIGS. 1, 8-9, *with* Noguchi-II, FIGS. 7-9. Both Noguchi's are also concerned with reducing parasitic capacitance, Cad. Noguchi-I, ¶15; Noguchi-II, ¶54.

371. Accordingly, Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong teach claim 11.

5. Claim 12: “The organic light emitting diode display according to claim 11, wherein the semiconductor layer is extended to and is electrically coupled to the seventh thin film transistor.”

372. In my opinion, Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong teach or suggest claim 12.

373. As explained in 1[g] and 1[j], each of transistors T1 to T6 utilize and include a portion of the semiconductor layer, which is thus electrically coupled to the corresponding transistor. §§VIII.A.3.h, VIII.A.3.i. In my opinion, it would have been obvious that when adding an additional TFT that utilized the semiconductor layer, the deposited semiconductor layer would be extended to accommodate the new TFT, which is consistent with the design disclosed in Noguchi-I. In other words, it would have been obvious to continue the semiconductor layer to incorporate T7 because this approach would lead to reduced display fabrication cost and enhanced yield. Furthermore, the ‘990 patent attaches no significance to having a contiguous or non-contiguous semiconductor layer as discussed in §IV.E.4. Thus, the combination teaches or suggests a seventh TFT with the semiconductor layer extended to incorporate that TFT.

374. Accordingly, claim 12 is disclosed by Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong.

6. Claim 13: “The organic light emitting diode display according to claim 12, wherein a gate electrode of the seventh thin film transistor is configured to receive a signal from a bypass control line.”

375. In my opinion, Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong teach or suggest claim 13.

376. Noguchi-II discloses that the seventh TFT has a gate signal of adj[n] (“bypass control line”). Noguchi-II explains that activation of the seventh TFT would have bypassed and accumulated charge on the OLED. Noguchi-II, ¶91. Accordingly, in my opinion, a POSITA would have understood adj[[n] to be a “bypass” control signal for the voltage on the OLED.

377. Accordingly, claim 13 is disclosed by Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong.

7. **Claim 14: “The organic light emitting diode display according to claim 11, wherein gate electrodes of the fourth and fifth thin film transistors are coupled together.”**

Claim 15: “The organic light emitting diode display according to claim 14, wherein the gate electrodes of the fourth and fifth thin film transistors are configured to receive a signal from a light emission control line.”

Claim 16: “The organic light emitting diode display according to claim 11, wherein a gate electrode of the sixth thin film transistor is configured to receive a signal from a second scan line.”

Claim 17: “The organic light emitting diode display according to claim 11, wherein gate electrodes of the first and third thin film transistors are coupled together.”

Claim 18: “The organic light emitting diode display according to claim 17, wherein the gate electrodes of the first and third thin film transistors are configured to receive a signal from the first scan line.”

Claim 19: “The organic light emitting diode display according to claim 11, wherein the second capacitor plate is electrically coupled to the first voltage line.”

378. In my opinion, Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong teach or suggest claims 14-19.

379. I have grouped claims 14-19, which are directed to the connectivity of different components in the '990 Patent driving circuit, for clarity and ease of discussion.

380. As explained Ground 2A in §VIII.A.4, Noguchi-I discloses these

claims. The addition on the seventh TFT does not alter Noguchi-I's disclosure. Accordingly, for the same reasons as explained above in Ground 2A, the combination teaches these claims.

8. Claim 21: “The organic light emitting diode display according to claim 11, wherein portions of the semiconductor layer are doped with N-type impurities.”

Claim 22: “The organic light emitting diode display according to claim 11, wherein portions of the semiconductor layer are doped with P-type impurities.”

381. As explained in Grounds 1A and 1C, Udagawa discloses P- and N-type impurities are doped into p-channel TFT transistors formed in the semiconductor layer PO. §§VIII.A.6, VIII.A.7. The addition of Noguchi-II's seventh TFT does not alter the general structure of the semiconductor layer other than adding an additional p-channel TFT, just explained in Ground 1A for Chung. Accordingly, for the same reasons as explained above, Noguchi-I in combination with Udagawa, Jeong, and Noguchi-II teach claims 21 and 22.

F. Ground 2C: Claims 1-30 are Unpatentable over the Combination of Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim

1. Summary of Kim

382. Kim (EX1013) teaches contact errors in the dual-structure capacitor can be prevented by the active pattern (1) functioning as the first electrode of the first capacitor and being extended to be connected to the semiconductor layer included

in the transistor connected between a power source VDD that supplies a power supply voltage and a power source Vinit that supplies an initial voltage, and (2) functioning as the first electrode of the second capacitor and being extended to be connected to the semiconductor layer included in the transistor that transmits the data voltage to the driving transistor in response to the selection signal from the current scan line. Id., 5:41-6:16.

383. In my opinion, Kim is analogous art to the '990 Patent because both patents are in the same field of endeavor. For example, both are directed to compensating for threshold voltage deviation. Kim, 1:61-63.

2. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim

384. In my opinion, there are several reasons that motivate the combination of Noguchi-I and Kim.

385. Kim, similar to Noguchi-I, is related to OLED displays. Kim, 5:41-6:16. In particular, Noguchi-I and Kim both described similar OLED drive circuits that included six TFTs and two capacitors (6T2C circuits) (Noguchi-I, FIG. 1; Kim, FIG. 5), and both described forming TFTs on a substrate within an OLED pixel in strikingly similar configurations. Noguchi-I, FIG. 8; Kim, FIG. 2 (reproduced below).

Fig. 8

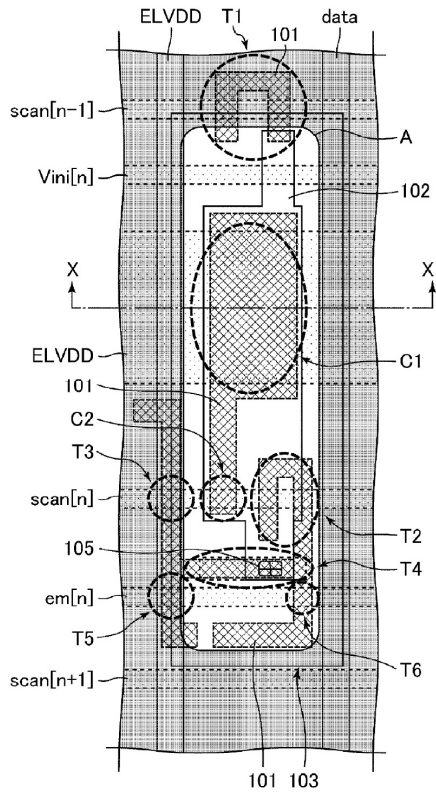
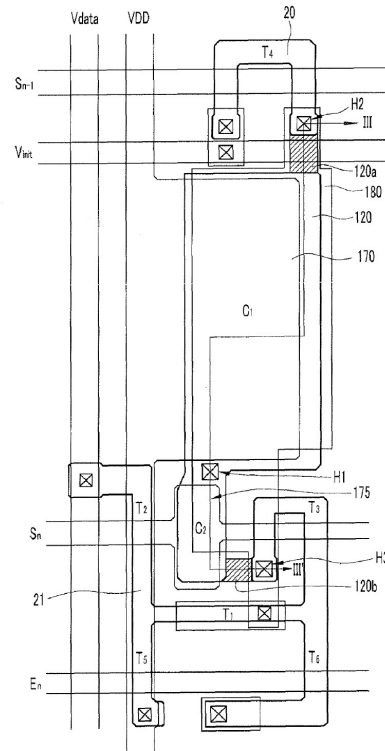


FIG. 2



Left: Noguchi-I, FIG. 8; Right: Kim, FIG. 2.

386. While Noguchi-I's semiconductor pattern starting around the bottom of the pixel area (at T6) and extending to the top of the pixel (at T1) includes discontinuities, Kim's semiconductor pattern does not. *See* Noguchi-I, FIG. 8; Kim, FIG. 2 (annotated below in §VIII.A.3). In this combination, the Noguchi-I pixel layout is modified based on the teachings of Kim to form a contiguous semiconductor pattern. *See* § IV.G.3. In my opinion, a POSITA would have found it obvious to make this modification because Kim's continuous semiconductor pattern constituted a known alternative to Noguchi-I's non-contiguous pattern.

Furthermore, such a modification amounted to a simple design choice that involved a routine task of making minor changes to the semiconductor pattern and was well within the skill set of a POSITA.

387. Additionally, and as previously discussed, the Noguchi-I reference can be combined individually with each of the cited references—Udagawa, Noguchi-II, Jeong, and Kim. In each instance, the combination involves modifying a distinct aspect of Noguchi-I, and these modifications are independent of one another. For example, Udagawa teaches modifying the channel of the driving TFT, Noguchi-II teaches modifying the 6T1C circuit by incorporating a seventh TFT, Jeong teaches using ELVSS as Vini[n], and Kim teaches modifying the extent of the semiconductor layer. A POSITA would recognize that there is no interference among the modifications, and each combination can be implemented without affecting the others. Accordingly, a POSITA would have found it obvious and would have been motivated to combine Noguchi-I with each of Udagawa, Noguchi-II, and Kim, and would have had a reasonable expectation of success.

388. Additional details regarding the Noguchi-I–Udagawa–Noguchi-II–Jeong–Kim combination are provided below in connection with specific claim limitations.

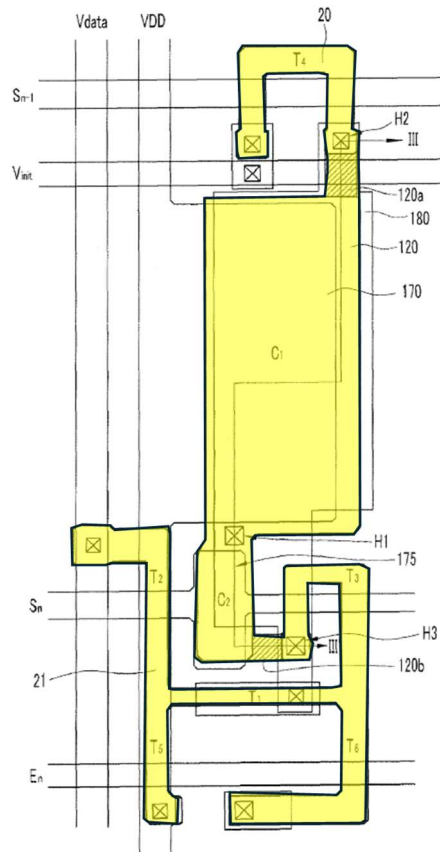
3. Claims 1-30

389. To the extent it is argued that Noguchi-I does not teach or suggest “the

semiconductor layer being extended to and electrically coupled to” TFT T1 because of a discontinuity in the portion of the semiconductor pattern that extends to T1, it would have been obvious to modify Noguchi-I to have a contiguous semiconductor pattern based on the teachings of Kim.

390. Kim describes TFT driving circuit similar to Noguchi-I’s Figure 1. *See* Kim, 7:34-8:51; FIG. 5. Kim further provides a layout of the transistors that is similar to Noguchi-I’s Figure 8. *See* Kim, 5:12-18, FIG. 2. Kim explains that **T4 in Figure 2 is connected to T3 using semiconductor patterns 120, 120a and 120b**. Kim, 6:29-49. Annotated Figure 2 below shows an example of the semiconductor layer of Kim, showing a contiguous semiconductor pattern that extends to all TFTs.

FIG. 2



Kim, FIG. 2 (annotated).

391. For reasons explained in ¶¶384-387, there is a motivation to utilize the teachings of Kim to modify Noguchi-I's semiconductor pattern to contiguously extend to TFT T1. The addition of Kim does not change my analysis above regarding claims 1-30 above.

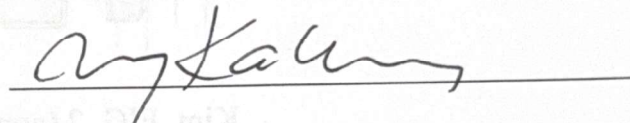
IX. CONCLUSION

392. Based on the foregoing analysis, it is my opinion that the challenged claims of the '990 patent are invalid.

Dr. Jerzy Kanicki Declaration
Inter Partes Review of U.S. Patent 11,574,990

This declaration and my opinions herein are made to the best of my knowledge and understanding, and based on the material available to me, at the time of signing this declaration. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United States Code.

Date: August 30, 2025


Jerzy Kanicki