

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,

Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.,

Patent Owner.

IPR2025-01478

U.S. Patent No. 11,574,990

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,574,990**

TABLE OF CONTENTS

[illegible]

1.	Chung	53
2.	Motivation to combine Liu, Udagawa, and Chung.....	53
3.	Claim 11	55
4.	Claim 12.....	58
5.	Claim 13.....	59
6.	Claims 14-19	59
7.	Claims 21-22	59
D.	Ground 1D: Claim 20 is Unpatentable over Liu, Udagawa, Chung, and Nakayama	60
1.	Motivation to combine Liu, Udagawa, Chung, and Nakayama.....	60
2.	Claim 20.....	60
E.	Ground 2A: Claims 1-10 and 21-30 are Unpatentable over Noguchi-I and Udagawa.....	61
1.	Noguchi-I	61
2.	Motivation to combine Noguchi-I and Udagawa	61
3.	Independent Claim 1	62
4.	Claims 2-7, 23	90
5.	Claim 8.....	92
6.	Claims 9-10.....	93
7.	Claims 24-25	94
8.	Claim 26	96
9.	Claims 27-30	97
F.	Ground 2B: claims 11-20 are Unpatentable over Noguchi- I, Udagawa, Noguchi-II, and Jeong	97
1.	Noguchi-II.....	97
2.	Jeong	98
3.	Motivation to combine Noguchi-I, Udagawa, Noguchi-II, and Jeong.....	99
4.	Claim 11	100

5.	Claim 12	104
6.	Claim 13	105
7.	Claims 14-19	105
8.	Claims 21-22	105
G.	Ground 2C: Claims 1-30 are Unpatentable over the Combination of Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim	106
1.	Kim.....	106
2.	Motivation to combine Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim.....	106
3.	Claims 1-30	108
V.	CONCLUSION.....	110
VI.	MANDATORY NOTICES	110
A.	Real Party in Interest	110
B.	Related Matters.....	110
C.	Notice of Counsel and Service Information.....	110
D.	Power of Attorney	112

EXHIBIT LIST

No.	Exhibit
1001	U.S. Patent No. 11,574,990 (“’990 Patent” or “’990Pat.”)
1002	File History of the ’990 patent (“’990FH”)
1003	Declaration of Jerzy Kanicki, Ph.D.
1004	Curriculum Vitae of Jerzy Kanicki, Ph.D.
1005	U.S. Pat. Pub. No. 2012/0313100 (“Liu”)
1006	U.S. Pat. Pub. No. 2003/0089905 (“Udagawa”)
1007	Japanese Pat. Pub. No. 2003-167533 (“Nakayama”)
1008	U.S. Pat. Pub. No. 2008/0150846 (“Chung”)
1009	U.S. Pat. Pub. No. 2012/0001893 (“Jeong”)
1010	U.S. Pat. Pub. No. 2012/0199854 (“Noguchi-I”)
1011	Japanese Pat. Pub. No. 2008-008942 (“Murade”)
1012	U.S. Pat. Pub. No. 2012/0127220 (“Noguchi-II”)
1013	U.S. Pat. No. 7,626,199 (“Kim”)
1014	<i>Samsung Display Co. v. BOE Technology Group Co.</i> , No. 2:25-cv-00426-JRG (E.D. Tex.), Dkt. No. 1, Complaint
1015	Definition of “periphery”: The American Heritage Dictionary, 2d ed. (1991)
1016	Definition of “periphery”: Concise Oxford English Dictionary, 11th ed. (2009)
1017	K.C. Park, <i>Pixel Circuits for OLED Displays</i> in <i>Advanced Display Technology</i> , Series in Display Science and Technology, I. B. Kang et al. (eds.), Springer Nature Singapore Pte Ltd. 2021 (“Park”)

No.	Exhibit
1018	R. M. A. Dawson et al., <i>Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display</i> in 1998 SID Symp. Digest of Tech Papers, 1998 (“Dawson”)
1019	S. M. Choi et al., <i>A Self-Compensated Voltage Programming Pixel Structure for Active-Matrix Organic Light-Emitting Diodes</i> in Proceedings of International Display Workshops (IDW), pp. 535-538, 2003 (“Choi”)
1020	A. Bernanose, <i>Electroluminescence of Organic Compounds</i> in British Journal of Applied Physics 6, pp. S54-S56, 1955 (“Bernanose”)
1021	H. Kallmann et al., <i>Bulk Conductivity in Organic Crystals</i> in Nature 4718, pp. 31-33, 1960 (“Kallmann”)
1022	M. Pope, Autoionization in Anthracene in The Journal of Chemical Physics 47, 2197–2198, 1967 (“Pope”)
1023	M. Sano et al., Electroluminescence and Band Gap in Anthracene in The Journal of Chemical Physics 43, 2920–2921, 1965 (“Sano”)
1024	P.S. Vincett et al., <i>Electrical Conduction and Low Voltage Blue Electroluminescence in Vacuum-Deposited Organic Films</i> in Thin Solid Films 94, 171-183, 1982 (“Vincett”)
1025	C.W. Tang and S.A. VanSlyke, <i>Organic Electroluminescent Diodes</i> in Applied Physics Letters 51, 913-915, 1987 (“Tang”)
1026	J.H. Burroughes et al., <i>Light-Emitting Diodes Based on Conjugated Polymers</i> in Nature 347, 539-541, 1990 (“Burroughes”)
1027	M.A. Baldo et al., <i>Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices</i> in Nature 395, 151-154, 1998 (“Baldo”)
1028	U.S. Pat. Pub. No. 2003/0129790 (“Yamazaki”)

No.	Exhibit
1029	Min et al., <i>Electrical Characteristics of New LDD Poly-Si TFT Structure Tolerant to Process Misalignment</i> in IEEE Electron Device Letters, 20(7), 1999 (“Min”)
1030	Lee et al., <i>Asymmetric Electrical Properties of Fork a-Si:H Thin-Film Transistor and Its Application to Flat Panel Displays</i> in Journal of Applied Physics, 105, 2009 (“Lee”)
1031	Kim et al., <i>40 Inch FHD AM-OLED Display with IR Drop Compensation Pixel Circuit</i> in 2009 SID Symp. Digest of Tech Papers, 2009 (“Kim-2009”)
1032	Lee et al., <i>A Novel LTPS TFT Pixel Circuit for Compensating IR Drop of Large Area AMOLED Display</i> in The Electrochemical Society (ECS) Transactions, 50(8), pp. 269-275, 2012 (“Lee-2012”)
1033	N. H. E. Weste et al., <i>CMOS VLSI Design: A Circuits and Systems Perspective</i> , Fourth Edition, Addison-Wesley, 2011 (“Weste”)
1034	U.S. Pat. Pub. No. 2003/0141811 (“Park ’811”)
1035	U.S. Pat. No. 9,461,102 (“Ono”)
1036	U.S. Pat. Pub. No. 2012/0211750 (“Kakinuma”)

LISTING OF CHALLENGED CLAIMS

11,574,990
Claim 1
1[pre] An organic light emitting diode display comprising:
1[a] a substrate;
1[b] a first voltage line;
1[c] a second voltage line;
1[d] a plurality of pixels, each of the pixels comprising an organic light emitting diode;
1[e] a plurality of driving circuits on the substrate, each of the organic light emitting diodes being electrically coupled to a respective driving circuit;
1[f] wherein each of the driving circuits comprises: a first thin film transistor coupled to a first scan line and a data line;
1[g] a second thin film transistor utilizing a semiconductor layer and electrically coupled to the first voltage line, the corresponding organic light emitting diode, and the first thin film transistor, the semiconductor layer being extended to and electrically coupled to the first thin film transistor;
1[h] an insulating layer covering the second thin film transistor;
1[ia] a storage capacitor electrically coupled to a gate electrode of the second thin film transistor, the storage capacitor comprising a first capacitor plate comprising a portion of the gate electrode of the second thin film transistor, a second capacitor plate over the first capacitor plate, and
1[ib] a portion of the insulating layer between the first capacitor plate and the second capacitor plate, a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor being curved;
1[j] a third thin film transistor electrically coupled to the second thin film transistor, the corresponding organic light emitting diode, and the first capacitor

plate, the semiconductor layer being extended to and electrically coupled to the third thin film transistor;
1[k] a fourth thin film transistor electrically coupled to the first voltage line and the second thin film transistor, the semiconductor layer being extended to and is electrically coupled to the fourth thin film transistor;
1[l] a fifth thin film transistor electrically coupled to the second thin film transistor, the third thin film transistor, and the corresponding organic light emitting diode, the semiconductor layer being extended to and is electrically coupled to the fifth thin film transistor; and
1[m] a sixth thin film transistor electrically coupled to the second voltage line, the third thin film transistor, and the first capacitor plate, the semiconductor layer being extended to and is electrically coupled to the sixth thin film transistor.
Claim 2
2. The organic light emitting diode display according to claim 1, wherein gate electrodes of the fourth and fifth thin film transistors are coupled together.
Claim 3
3. The organic light emitting diode display according to claim 2, wherein the gate electrodes of the fourth and fifth thin film transistors are configured to receive a signal from a light emission control line.
Claim 4
4. The organic light emitting diode display according to claim 1, wherein a gate electrode of the sixth thin film transistor is configured to receive a signal from a second scan line.
Claim 5
5. The organic light emitting diode display according to claim 1, wherein gate electrodes of the first and third thin film transistors are coupled together.
Claim 6

6. The organic light emitting diode display according to claim 5, wherein the gate electrodes of the first and third thin film transistors are configured to receive a signal from the first scan line.

Claim 7

7. The organic light emitting diode display according to claim 1, wherein the second capacitor plate is electrically coupled to the first voltage line.

Claim 8

8. The organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

Claim 9

9. The organic light emitting diode display according to claim 1, wherein portions of the semiconductor layer are doped with N-type impurities.

Claim 10

10. The organic light emitting diode display according to claim 1, wherein portions of the semiconductor layer are doped with P-type impurities.

Claim 11

11. The organic light emitting diode display according to claim 1, further comprising a seventh thin film transistor electrically coupled to the second voltage line, the fifth thin film transistor, and the corresponding organic light emitting diode.

Claim 12

12. The organic light emitting diode display according to claim 11, wherein the semiconductor layer is extended to and is electrically coupled to the seventh thin film transistor.

Claim 13

13. The organic light emitting diode display according to claim 12, wherein a gate electrode of the seventh thin film transistor is configured to receive a signal from a bypass control line.
Claim 14
14. The organic light emitting diode display according to claim 11, wherein gate electrodes of the fourth and fifth thin film transistors are coupled together.
Claim 15
15. The organic light emitting diode display according to claim 14, wherein the gate electrodes of the fourth and fifth thin film transistors are configured to receive a signal from a light emission control line.
Claim 16
16. The organic light emitting diode display according to claim 11, wherein a gate electrode of the sixth thin film transistor is configured to receive a signal from a second scan line.
Claim 17
17. The organic light emitting diode display according to claim 11, wherein gate electrodes of the first and third thin film transistors are coupled together.
Claim 18
18. The organic light emitting diode display according to claim 17, wherein the gate electrodes of the first and third thin film transistors are configured to receive a signal from the first scan line.
Claim 19
19. The organic light emitting diode display according to claim 11, wherein the second capacitor plate is electrically coupled to the first voltage line.
Claim 20

20. The organic light emitting diode display according to claim 11, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.
Claim 21
21. The organic light emitting diode display according to claim 11, wherein portions of the semiconductor layer are doped with N-type impurities.
Claim 22
22. The organic light emitting diode display according to claim 11, wherein portions of the semiconductor layer are doped with P-type impurities.
Claim 23
23. The organic light emitting diode display according to claim 1, wherein the third thin film transistor is electrically coupled to the gate electrode and a drain electrode of the second thin film transistor.
Claim 24
24. The organic light emitting diode display according to claim 1, further comprising a protective layer covering the plurality of driving circuits, wherein each of the organic light emitting diodes further comprises a pixel electrode on the protective layer, the pixel electrode being electrically coupled to the second thin film transistor through a contact hole.
Claim 25
25. The organic light emitting diode display according to claim 1, further comprising a protective layer covering the plurality of driving circuits, wherein each of the organic light emitting diodes further comprises a pixel electrode on the protective layer, the pixel electrode being electrically coupled to a drain electrode of the fifth thin film transistor through a contact hole.
Claim 26
26. The organic light emitting diode display according to claim 1, wherein the first capacitor plate and the first scan line are in the same material layer.

Claim 27
27. The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “S”-shape.
Claim 28
28. The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a partial “S”-shape.
Claim 29
29. The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “M”-shape.
Claim 30
30. The organic light emitting diode display according to claim 1, wherein the curved portion of the semiconductor layer has a “W”-shape.

Petitioner requests *inter partes review* (“IPR”) of claims 1-30 (“Challenged Claims”) of U.S. Patent No. 11,574,990 and has shown a reasonable likelihood of prevailing as to each Challenged Claim.

I. GROUNDS FOR STANDING

The ’990 Patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR. EX1014.

II. IDENTIFICATION OF CHALLENGE

Petitioner relies on Exhibits listed in the Table of Exhibits and declaration of Dr. Jerzy Kanicki (EX1003, “Kanicki”). Specific invalidity grounds are listed in the table below, where Liu is prior art under pre-AIA 35 U.S.C. §102(e), and the remaining references are prior art under pre-AIA 35 U.S.C. §102(b).

Ground 35 U.S.C. §103)	Claims	References
1A	1-7, 9, 10, 23-30	Liu, Udagawa
1B	8	Liu, Udagawa, Nakayama
1C	11-19, 21, 22	Liu, Udagawa, Chung
1D	20	Liu, Udagawa, Chung, Nakayama
2A	1-10, 21-30	Noguchi-I, Udagawa
2B	11-22	Noguchi-I, Udagawa, Noguchi-II, Jeong
2C	1-30	Noguchi-I, Udagawa, Noguchi-II, Jeong, Kim

III. THE '990 PATENT

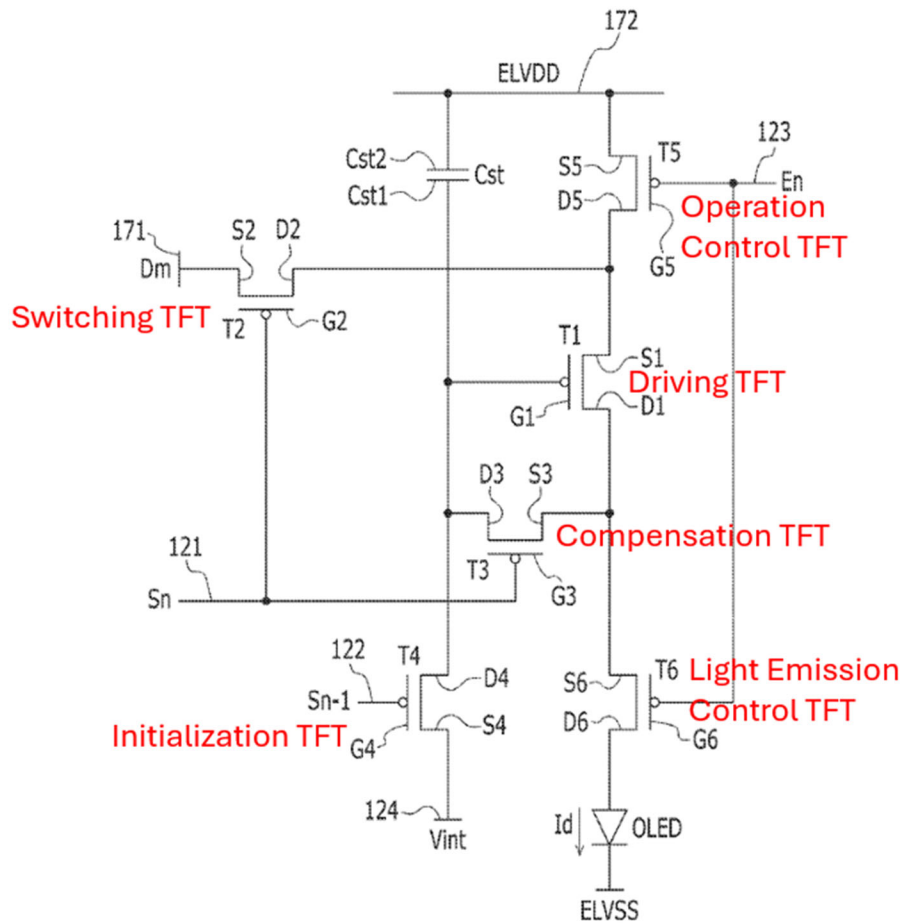
A. Overview

The '990 Patent describes an organic light emitting diode (OLED) display, including a plurality of pixels, signal lines (121-124, 171-172), six thin-film transistors (TFTs T1-T6), a storage capacitor (Cst), and an OLED connected to T6.¹ '990Pat., 1:45-46, 6:12-19, FIG. 1 (showing one pixel circuit); Kanicki, ¶¶44-55. The '990 Patent describes achieving a relatively large number of gray levels by forming the channel region of the driving TFT to include a plurality of bent portions. *Id.* 2:3-6, 4:48-53.

One pixel circuit is shown in Figure 1 (annotated below), with Figures 2 and 3 showing specific layout (or plan) views of the pixels, and Figure 4 and 5 showing cross-sectional views taken along different cut lines of Figure 3. *Id.*, 6:9-14, 8:37-51.

¹ OLED displays utilizing TFTs and capacitors are not new. Kanicki, ¶¶63-100; EX1017-1032.

FIG. 1



T1-T6 are formed along semiconductor layer 131 (Figure 3 below). *Id.*, 9:4-10. The driving semiconductor (T1) channel 131a includes bent portions 33, resulting in a broader driving range of T1. *Id.*, 9:28-47. This enables gray levels to be more finely and precisely controlled by adjusting the gate voltage magnitude, to increase the resolution and thus image quality of the display. *Id.*, 9:49-62. Figure 6, e.g., shows the driving semiconductor layer 131a being “S” shaped. *Id.*, 10:5-6.

FIG. 3

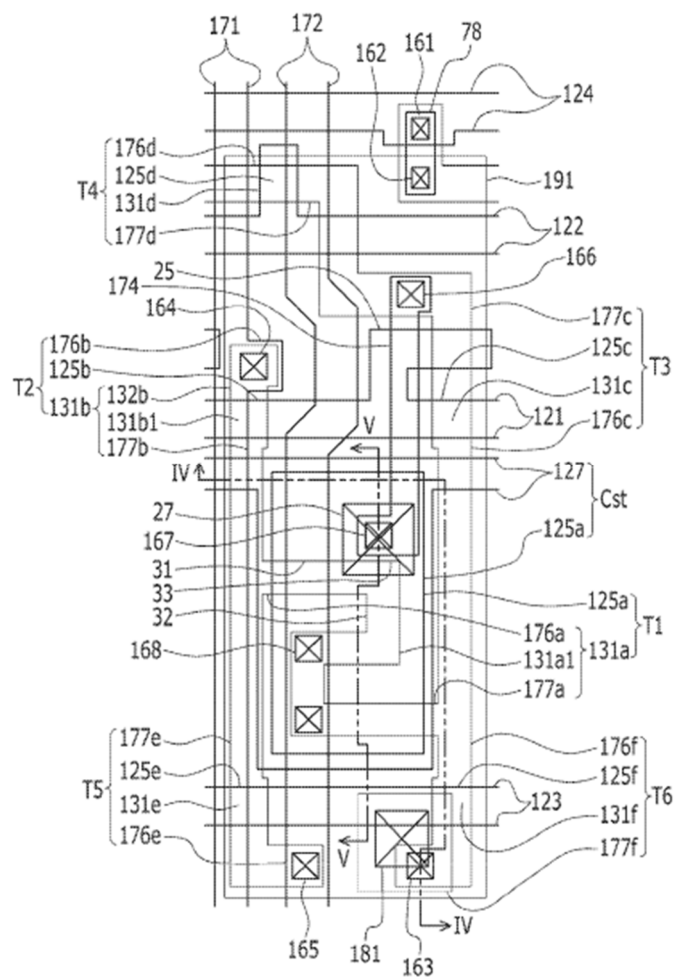
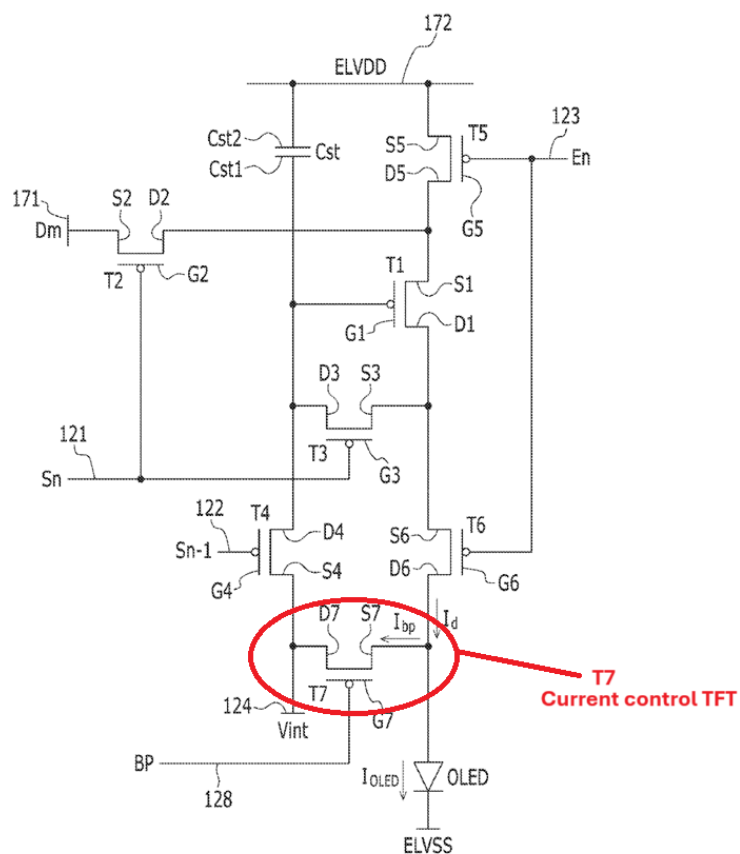


Figure 10, annotated below, describes incorporating an additional bypass T7 into the circuit. Kanicki, ¶¶54-55. T7 disperses, or diverts, a portion of the T1 current away from the OLED to obtain an improved contrast ratio. *Id.*, 19:59-65, 20:17-19.

FIG. 10



B. Prosecution History

The '990 Patent claims priority to Korean Patent Application No. 10-2012-0084976 filed on August 2, 2012.² Kanicki, ¶¶56-61.

² August 2, 2012, is assumed to be the priority date for the purposes of this Petition only.

The Examiner issued a Non-Final Office Action, objecting to the claims, in addition to a nonstatutory double patenting rejection. '990FH, 139-146.

Applicant filed a Terminal Disclaimer, and the Examiner allowed the claims, because the prior art of record cannot anticipate/render obvious: “a portion of a channel region of the semiconductor layer under the gate electrode of the second thin-film transistor being curved; a third thin-film transistor electrically coupled to the second thin-film transistor...the semiconductor layer being extended to and electrically coupled to the third thin-film transistor.” '990FH, 131-132.

Liu, used in this petition, was cited in an Information Disclosure Statement (IDS) (*Id.*, 319.) but was not used as a basis for claim rejections or otherwise discussed during the prosecution. Liu's use in this Petition is not cumulative over the prior examination at least because Liu is used in combination with other references, including Udagawa, and the Examiner lacked expert testimony regarding the use of Liu in combination with other references.

C. Level of Ordinary Skill

For the purposes of this petition, a person of ordinary skill in the art (“POSITA”) in August 2012 would have had a bachelor's degree in electrical engineering, physics, materials science or engineering, or a related field and at least four years of experience with design or development of OLED displays, including

pixel layout, or the equivalent. Additional education could substitute for industry experience and vice versa. Kanicki, ¶¶1-26.

D. Claim Construction

No express constructions are necessary to assess whether the prior art reads on the challenged claims. The claims should be given their plain and ordinary meaning. Kanicki, ¶101.

IV. SPECIFIC GROUNDS

A. Ground 1A: Claims 1-7, 9, 10, and 23-30 are Unpatentable over Liu and Udagawa

1. Liu

Liu (EX1005), in the same of endeavor as the '990 Patent, discloses a pixel structure for an organic electroluminescence display comprising six TFTs and one capacitor (6T1C) and an OLED (Liu, ¶¶32, 48) and, similar to the '990 patent, aims to reduce an area occupied by components of the pixel structure. *Id.*, ¶7; Kanicki, ¶¶104-106.

Liu's pixel structure is disposed on substrate 100, comprising a semiconductor layer PO, insulating layers (102, 104, 106), conductive layers (M1, M2, M3), and a pixel electrode PE. Liu, ¶32. The semiconductor layer PO comprises channel, source, and drain regions of the six TFTs (denoted T1-T6). *Id.*, ¶34.

2. Udagawa

Udagawa (EX1006) discloses lengthening the channel of a TFT in an OLED circuit to be longer than that of a channel of a conventional TFT. Udagawa, ¶23. This lowers the dispersion in the TFT's electric current value and enables the TFT to be turned on at a higher gate voltage. Udagawa, ¶¶19-23.

Udagawa is in the same field of endeavor as the '990 Patent because both are directed to display devices using a plurality of TFTs in each pixel to drive a current through an OLED. Udagawa, ¶¶8-9. Similarly, both the '990 patent and Udagawa describe using polysilicon film to form TFTs, with pixels and driving circuits being formed integrally over the same substrate, thereby reducing the number of connecting terminals and reducing the periphery of the pixel portion. *Id.*, ¶10; Kanicki, ¶¶107-109.

3. Motivation to combine Liu and Udagawa

Both Liu and Udagawa described drive circuits for OLED displays and both sought to improve the design and operation of OLEDs. Liu's invention focuses on a reduced-area pixel structure. Liu, ¶¶4, 10, 47, 56, 72. Udagawa describes drive circuit configurations improving OLED reliability, and consequently, its operation and image quality. Udagawa, ¶12. POSITAs would have been motivated to combine the complementary teachings of Liu with Udagawa to achieve improved operations of the OLED display. Kanicki, ¶¶110-111.

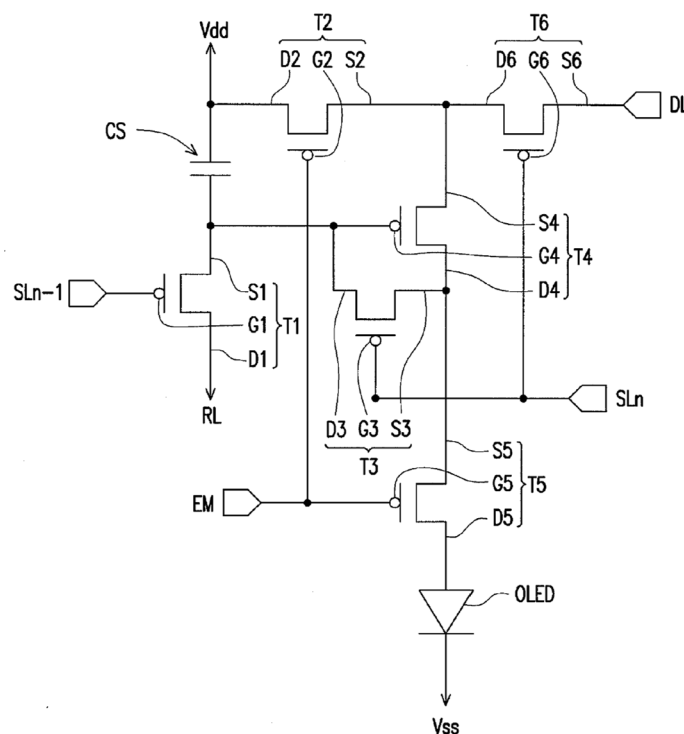
Udagawa recognized small TFTs resulted in unwanted dispersion effects, which was a main reason for display irregularities in a display device. Udagawa, ¶38. POSITAs would have been motivated to reduce the dispersion in Liu's TFT drive circuits so that the pixels in the high-resolution display provided a more uniform brightness. Kanicki, ¶112.

POSITAs would have been motivated to use Udagawa's driving TFT with serpentine channel in Liu's OLED driving circuit because this combination would have conformed to Liu's objectives of reducing the size of the pixel structure; forming the gate channel in this way would allow for both a reduction of dispersion and maintaining a reduced size of the TFT while enabling an improved operation of the driving TFT. *Id.*, ¶113.

POSITAs would have been motivated to apply Udagawa's known technique of reducing dispersion (using Udagawa's TFT with a longer channel) to a known device ready for improvement (Liu's OLED driving circuit) to yield predictable results (the dispersion of the driving TFT being reduced). POSITAs would have had a reasonable expectation of success because elongating the channel length to reduce dispersion was well-known by 2012, as evidenced by the teachings of Udagawa and other known prior art references, and such modifications were well within the skill set of POSITAs. *Id.*, ¶114 (citing EX1028-EX1030).

4. Independent Claim 1

Liu discloses a “pixel structure” in a display (“[a]n organic light emitting diode display”), using TFTs, a capacitor, and an “OLED”. Liu, ¶¶3, 6, 48, 58, FIGs. 1, 6. The “pixel structure **is applied to an organic electroluminescence display** and has a structure comprising six thin film transistors and one capacitor (6T1C),” but it is not limited to the disclosed structure.³ *Id.*, ¶¶32, 48, 50, 53, 58, 73, 75; Kanicki, ¶117.



³ All emphases are added unless otherwise noted.

Liu is further directed to reducing the area occupied by the pixel structure for use in high resolution displays. Liu, ¶¶6-7; Kanicki, ¶¶118-119. As explained below, Petitioner maps the embodiment shown in Figures 1-6 to the claims.

b. 1[a]

Liu discloses “the pixel structure is disposed on a **substrate 100.**” Liu, ¶32, FIG. 5 (annotated below); Kanicki, ¶¶120-121. Liu’s substrate may be made of glass, quartz, polymers, or ceramics, among other materials. *Id.*, ¶33.

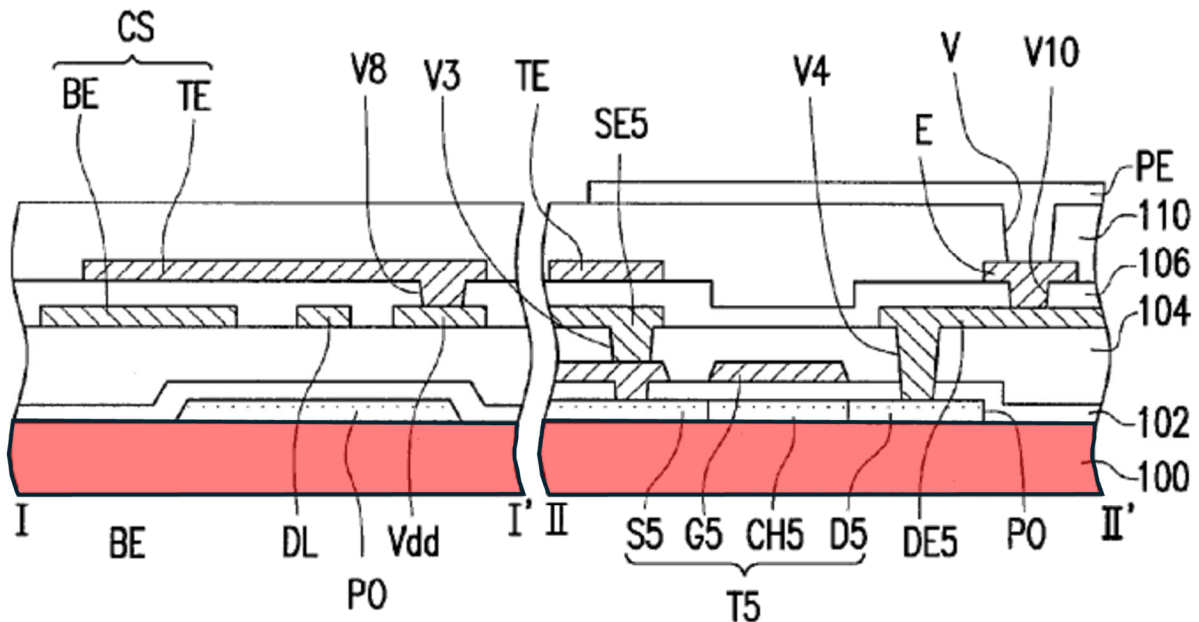


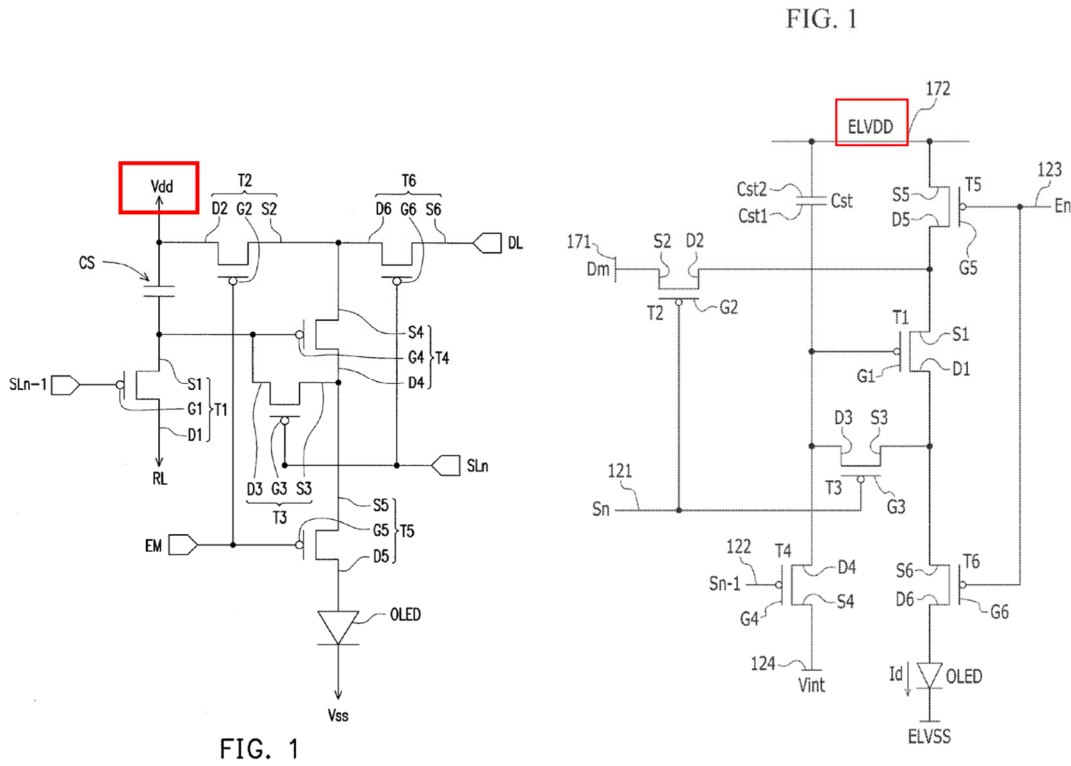
FIG. 5

c. 1[b]

Liu discloses the “first voltage line” as a “power line Vdd” in the second metal layer M2. Liu, ¶42, FIG. 1 (annotated below); Kanicki, ¶¶122-123. POSITAs would

have understood Vdd is a common notation to denote a voltage (Kanicki, ¶124), which is also used in the '990 Patent to identify a "voltage line." '990Pat., 6:25-37 ("a driving voltage line 172 for transferring a driving voltage ELVDD.").

Annotated Figure 1 of Liu (left) is shown alongside '990 Patent Figure 1(right) illustrating similarities between the circuits and Vdd. Liu, ¶31; Kanicki, ¶125.



Additionally, Petitioner cross-references each transistor and signal line of the '990 Patent to similar elements of Liu below. Kanicki, ¶125.

Claims	'990	Liu
1 st TFT	T2	T6
2 nd TFT	T1	T4
3 rd TFT	T3	T3
4 th TFT	T5	T2
5 th TFT	T6	T5

6 th TFT	T4	T1
Capacitor	Cst	CS
First Capacitor Plate	125h	BE
Second Capacitor Plate	127	TE
1 st Voltage line	ELVDD	Vdd
2 nd Voltage line	Vint	RL
OLED	OLED	OLED
1 st Scan line	Sn	SLn
2 nd Scan line	Sn-1	SLn-1
Light emission control line	En	EM
Data line	Dm	DL

d. 1[c]

Liu discloses the “second voltage line” as a reference signal line “RL” formed in the first metal layer M1. Liu, ¶38, FIG. 1 (annotated below); Kanicki, ¶¶126-127. POSITAs would have understood RL is also a “voltage line” because “signal line” is common terminology for circuit components that transmit voltages in transistor circuits; in addition, Liu’s Figure 1 uses the same circuit symbol to represent voltage lines Vss, Vdd, and RL, further corroborating RL as a voltage line. Kanicki, ¶127. RL corresponds to Vint in the ’990 Patent, described as “initialization voltage line 124.” ’990Pat., 6:25-37. Annotated Figure 1 of Liu (left) is shown alongside ’990 Patent Figure 1 (right) illustrating RL and Vint. Kanicki, ¶127.

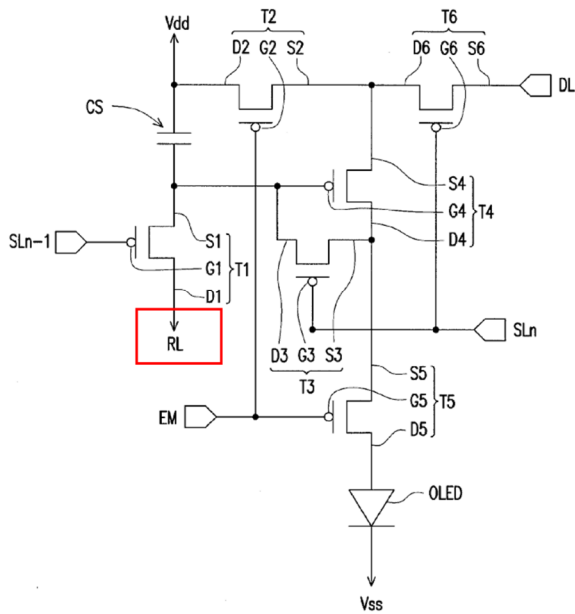


FIG. 1

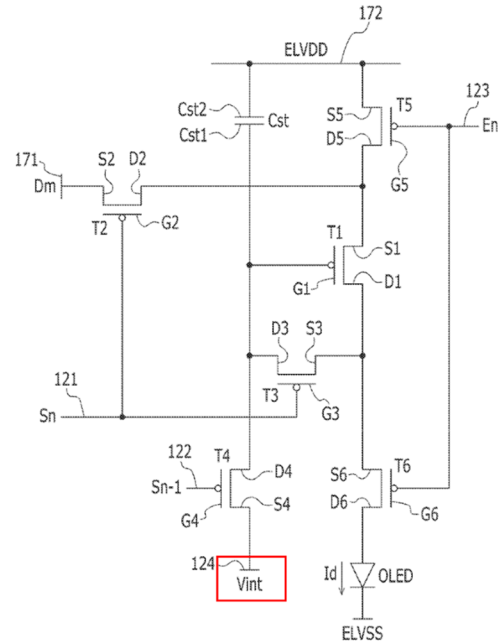


FIG. 1

e. 1[d]

Liu teaches or suggests this limitation, and Udagawa confirms the teachings of Liu regarding the presence of multiple pixels in the display device. Kanicki, ¶128.

Liu discloses pixel structures in an OLED displays. §IV.A.4.a. Each pixel structure (including TFTs, capacitor, and OLED) is a pixel (*id.*; Liu, ¶50) as confirmed by Udagawa, which explains pixels comprise the TFT driving circuits and OLEDs (Udagawa, ¶¶5-8) Kanicki, ¶129.

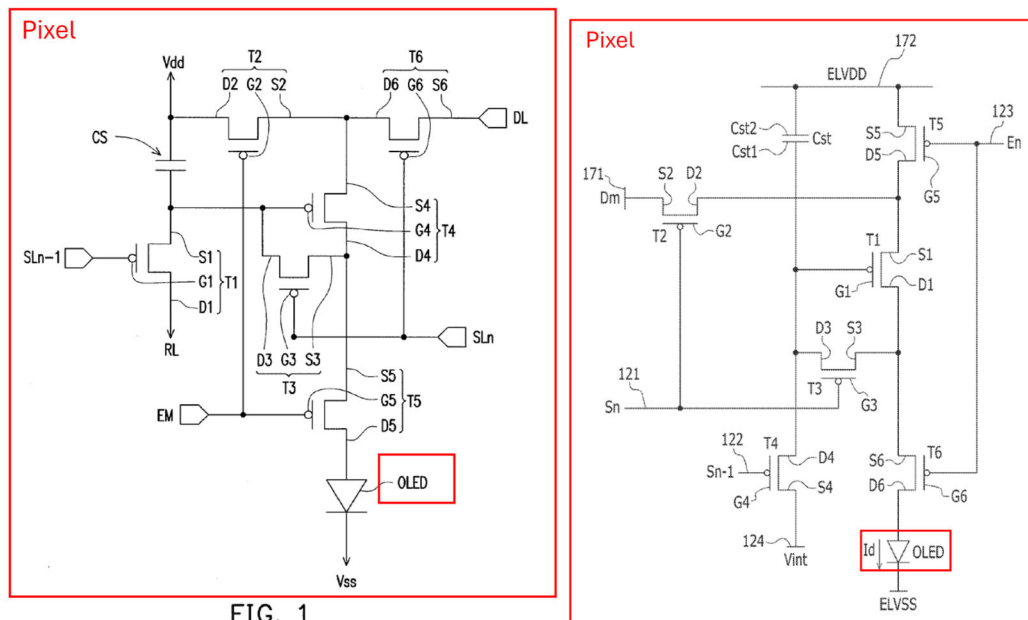
The pixel structure must be small for high resolution displays (Liu, ¶¶6-7), which contain a **plurality of pixel structures** because each pixel structure containing an OLED forms one light emitting portion (i.e., pixel) of the display, and

the resolution is measured according to the number of pixels occupying the display area. Kanicki, ¶130. Furthermore, the '990 Patent admits and confirms this understanding. '990Pat., 1:45-49.

Liu discloses scan lines (SL_n and SL_{n-1}) in the TFT circuit, with the nomenclature “n” and “n-1” signifying a plurality thereof, not limited to the two shown in the circuit. Liu, ¶38; §IV.A.4.c (table); Kanicki, ¶131. Thus, POSITAs would have understood that Liu’s circuit (Figures 1-6) represents one of a plurality of pixel structures, all used in the disclosed display (“a plurality of pixels, each of the pixels comprising an organic light emitting diode”). *Id.*, ¶¶131-132.

Liu’s annotated Figure 1 (left), similar to Figure 1 of the '990 Patent (right), shows a pixel and the position of the OLED. Kanicki, ¶132.

FIG. 1

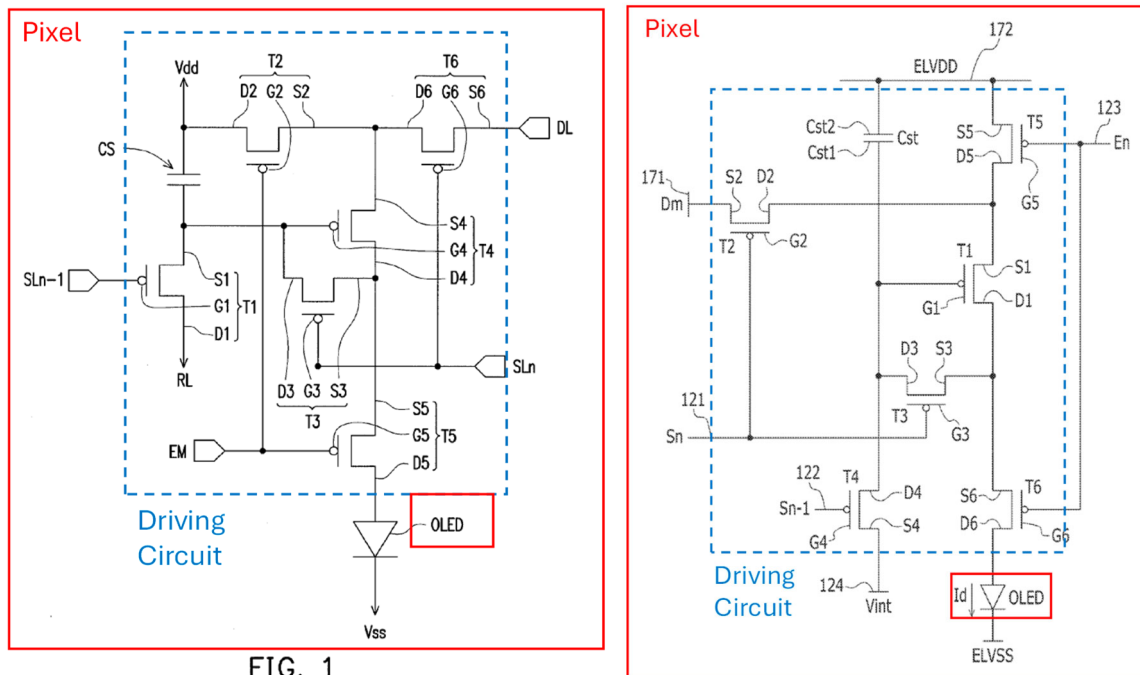


f. 1[e]

Liu teaches or suggests multiple pixel structures (i.e., pixels) in a display (1[d]). §IV.A.4.e. Liu further describes a “plurality of driving circuits” because it describes a driving circuit with a plurality of TFTs for each of the plurality of OLED pixels. Liu, ¶¶6, 8, FIG. 1.

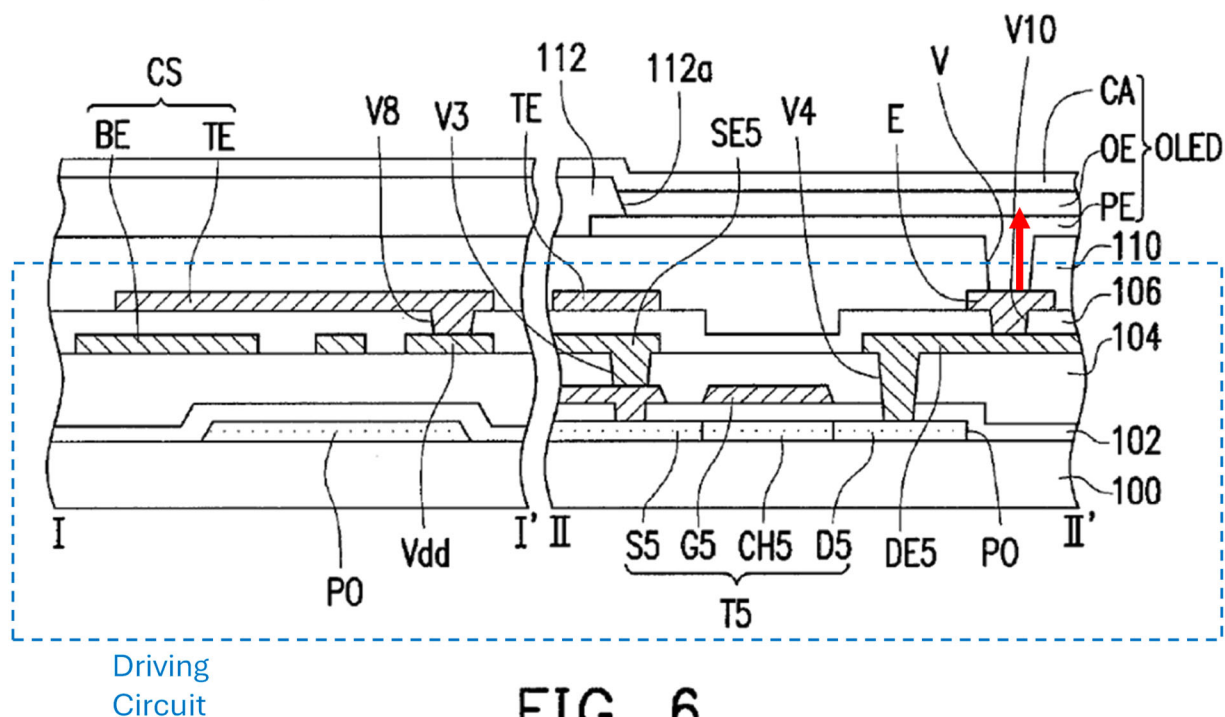
As shown below, each TFT driving circuit is connected to an OLED (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). *Id.*, ¶31, FIG. 1 (annotated); Kanicki, ¶¶134-136. Liu’s annotated Figure 1 (left), similar to Figure 1 of the ’990 Patent (right), illustrates the relationship of a pixel and driving circuit. Kanicki, ¶136.

FIG. 1



Liu explains that the TFTs are formed in a semiconductor layer on the substrate PO (“a plurality of driving circuits on the substrate”) and the substrate can be a “wafer.” *Id.*, ¶¶8, 33-35, FIGs. 1-6. POSITAs would have understood that the plurality of Liu’s driving circuits would have been formed on a single substrate because it was common practice at the time to use a single substrate (e.g. backplane or wafer) form to form multiple pixels. Kanicki, ¶137.

Annotated Figure 6, below, shows, the OLED directly connects to T5 through “E” and V (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). Liu, ¶¶44-48, FIG. 6; Kanicki, ¶138.



g. 1[f]

Liu discloses the “first thin film transistor” as T6 coupled to “the first scan line,” SL_n, and “a data line,” DL, as shown in Liu’s Figure 1. Liu, ¶¶38, 42. As explained in 1[e], each pixel structure includes several TFTs arranged in a driving circuit. §IV.A.4.f. Referring to Liu’s annotated Figure 1, the data line “is electrically connected to the source region S6” of T6, and scan line SL_n is connected to gate G6 of T6 of T6. *Id.*, ¶38, FIG. 1; Kanicki, ¶¶139-141.

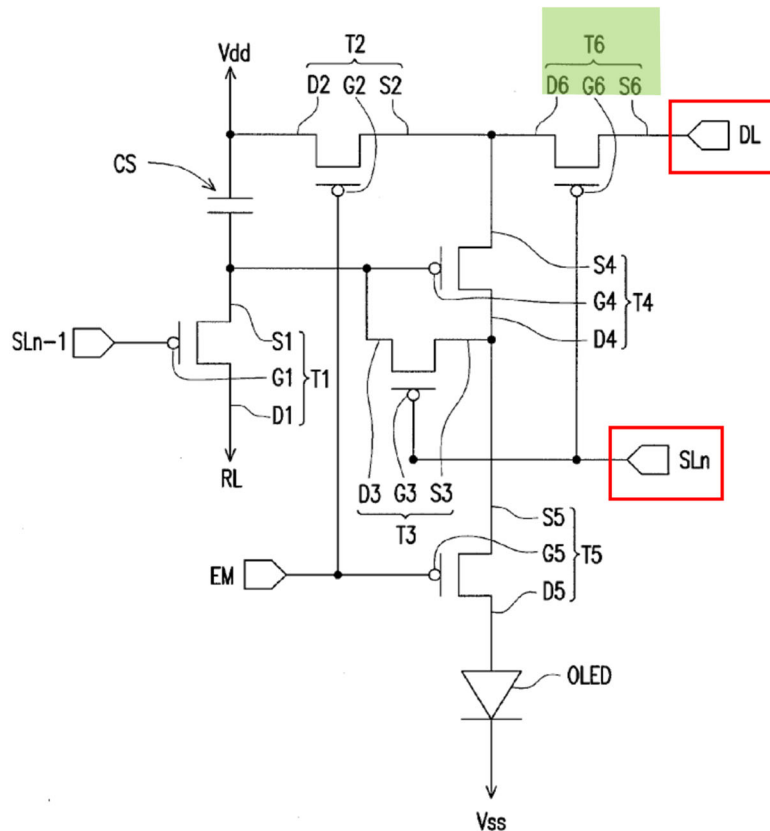


FIG. 1

h. 1[g]

Liu discloses the “second thin film transistor” as T4, electrically coupled to “the first voltage line,” Vdd, through T2, as shown in annotated Figure 1 below. Kanicki, ¶¶142-143. Liu’s T4 is electrically coupled to the “corresponding organic light emitting diode,” OLED, through T5, and is electrically coupled to the “first thin film transistor,” T6, through a direct connection between S4 (source of T4) and D6 (drain of T6). See Liu, FIG. 1.

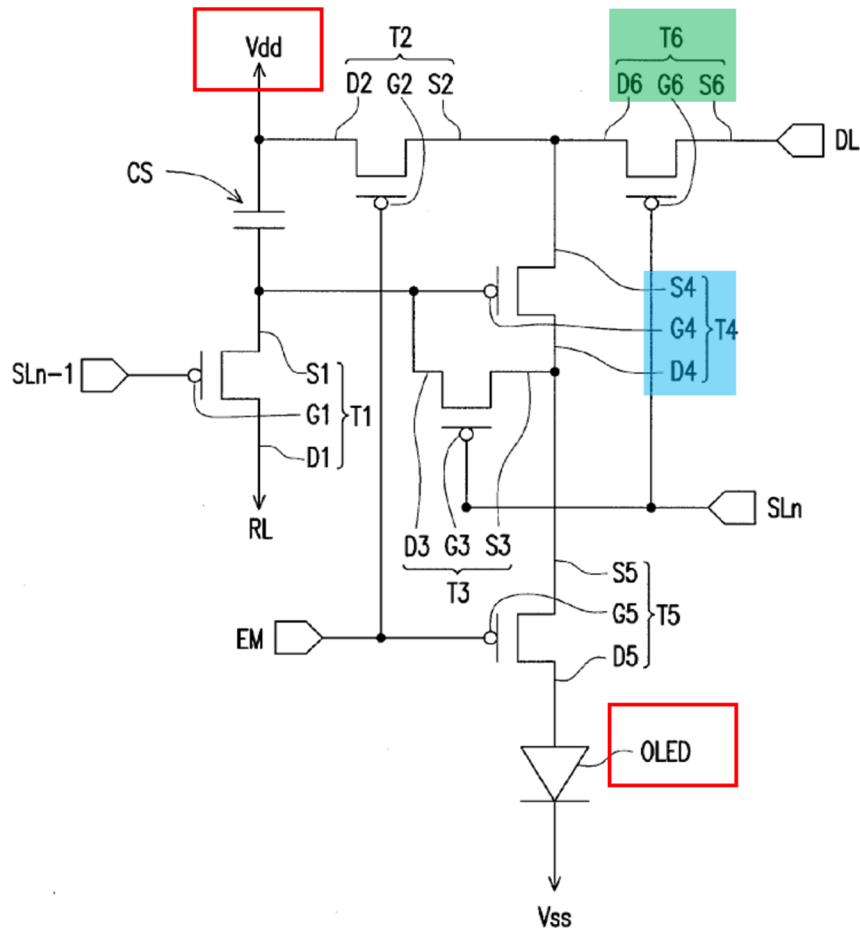
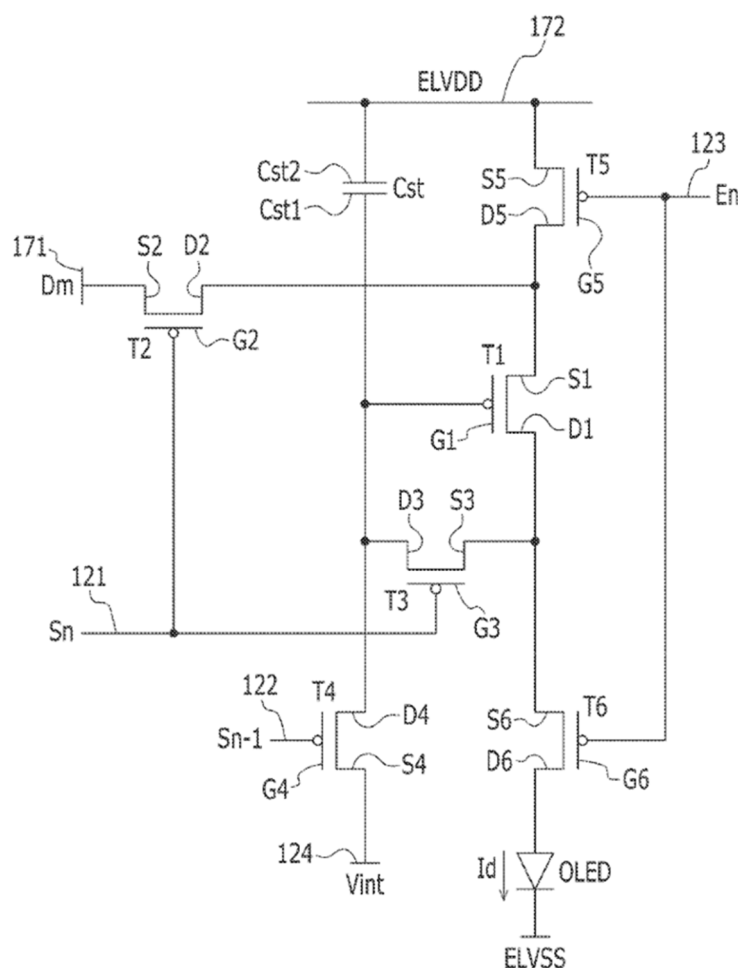


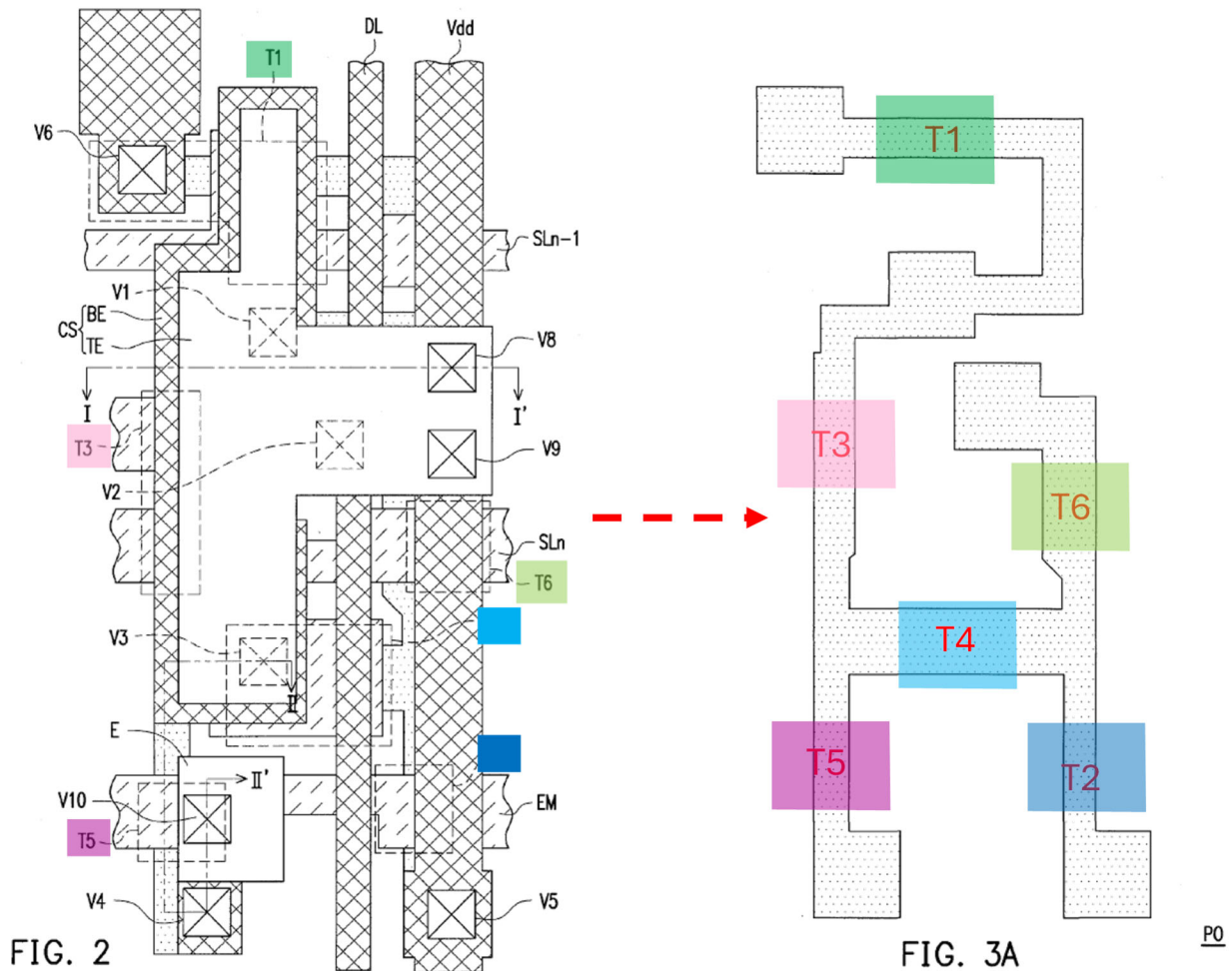
FIG. 1

The above characterization of Liu’s TFT T4 being “electrically coupled” to the OLED and Vdd through intervening TFTs is consistent with the ’990 Patent’s Figure 1 (below) and its detailed description, which explains, e.g., “T1 is coupled via the operation control thin film transistor T5 to the driving voltage line” and “T1 is electrically coupled via the light emission control thin film transistor T6 to an anode of the OLED.” *See* ’990Pat., 6:38-45, FIG. 1; Kanicki, ¶144.

FIG. 1



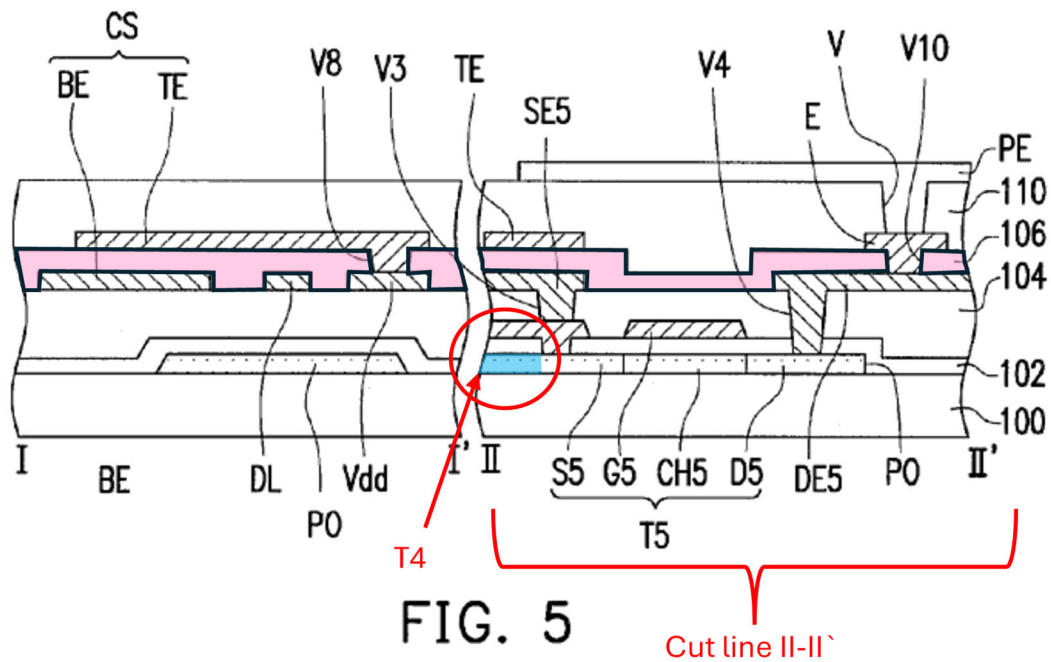
Liu additionally discloses T4 in a portion of the semiconductor layer (“utilizes a semiconductor layer”). Liu’s Figure 3A (right) is “a top view showing a semiconductor layer of the pixel structure” (Liu, ¶[0015]), which has been annotated by Petitioner based on Liu’s Figure 2 (left) (and other figures of Liu) to show the approximate locations of various TFTs over the semiconductor pattern. Kanicki, ¶¶145-153; Liu, ¶¶34-35, FIGs. 2, 3.



POSITAs would have understood from Liu's Figure 3A and Liu's description that T4 includes a section of the semiconductor pattern, which is contiguously laid out in the same layer and extends to the adjacent T6. Liu ¶35, FIG. 3A; Kanicki, ¶154. POSITAs would have further understood that T6 is electrically coupled to the semiconductor layer because it includes a section of the semiconductor pattern, which allows T6 to operate as a transistor. Kanicki, ¶154.

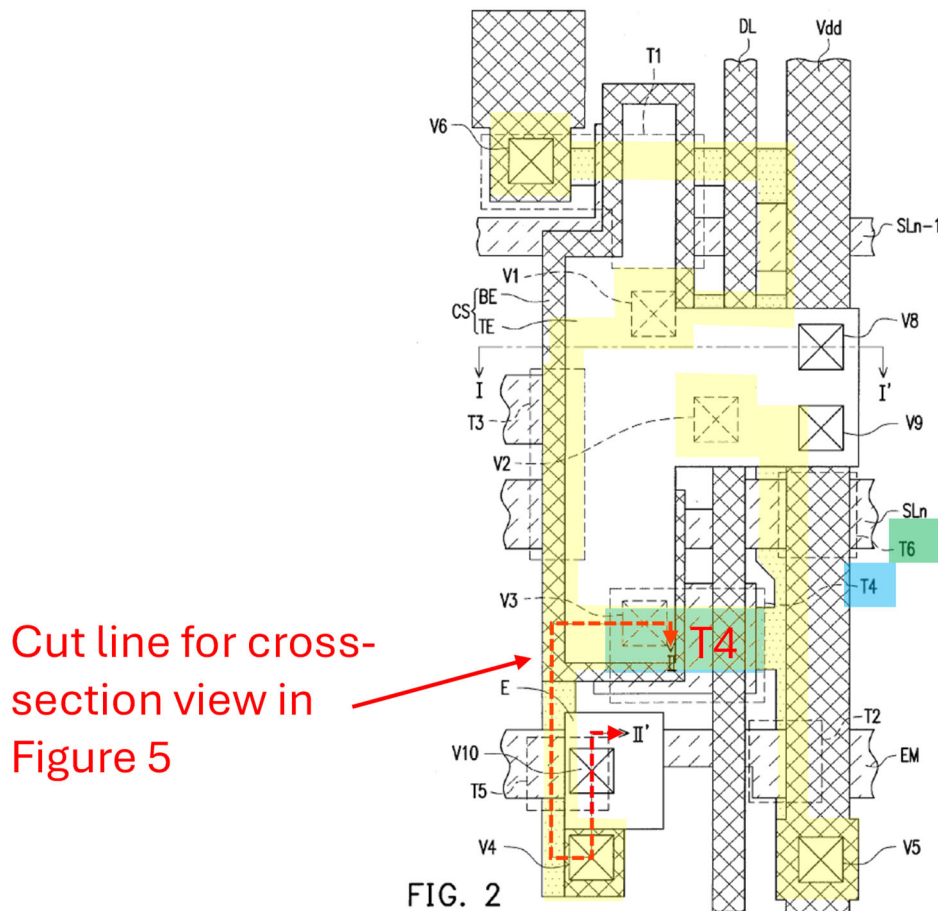
i. 1[h]

Liu discloses **insulating layer 106** “cover[ing] the second conductive layer M2.” Liu, ¶¶32, 43. Annotated Figure 5, below, shows insulating layer 106 covers Liu's TFTs. Kanicki, ¶¶155-156. POSITAs would have understood that Liu's successive insulating layers are deposited sequentially, so layer 106 covers all structures below it, just as layers 104 and 102 also cover all structures below them. *Id.* POSITAs would have further understood from Figure 5, that insulating layer 106 specifically covers T4 (“an insulating layer covering the second” TFT) . *Id.*



Liu, FIG. 5 (annotated).

POSITAs would have had this understanding because the cut line II-II' in Figure 2 passes directly through T4 and is shown in Figure 5. *Id.*, ¶157. Figure 2, is annotated below to illustrate the semiconductor layer PO (yellow), T6, T4, and the cross-section lines for Figure 5 *Id.*



Cut line for cross-section view in Figure 5

j. 1[ia]

Liu discloses the “storage capacitor” as capacitor CS connected on one side to the gate electrode of T4 (“a gate of the second transistor”), and includes a bottom electrode, BE, (“first capacitor plate”) and top electrode, TE (“second capacitor plate”). Liu, ¶¶42, 44-45, 47, 53, FIGs. 1, 2, 3C, 3D, 4-6; Kanicki, ¶¶158-159.

Liu explains CS “can be disposed overlapping with the semiconductor layer PO, so as to reduce an area occupied by components of the pixel structure.” Liu, ¶47. Liu further discloses capacitor CS is connected to the gate of T4 (“electrically

coupled to a gate electrode of the second thin film transistor”), as shown by the red line in Liu’s Figure 1. Liu, FIG. 1; Kanicki, ¶160.

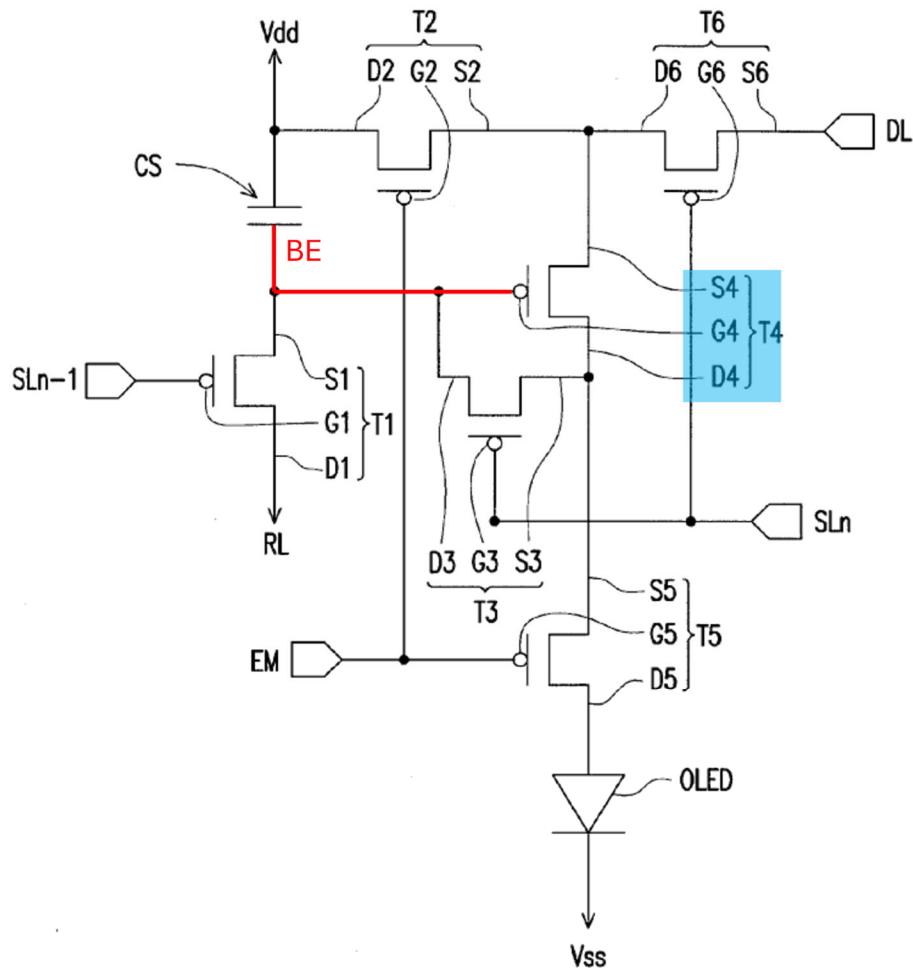


FIG. 1

As explained above, capacitor CS comprises a **bottom electrode BE** and a **top electrode TE**. Liu, ¶53. **Insulating layer 106** is disposed between BE and TE (“a portion of the insulating layer between the first capacitor plate and the second capacitor plate”). *Id.*, ¶¶45, 53, FIG. 5; Kanicki, ¶161. Liu’s Figure 5 is annotated to

show the gate electrode of T4 on M1, which is directly connected to BE on M2 through via V3.⁴ Kanicki, ¶161; Liu, ¶¶41, 54, FIGs. 2, 3B, 3C, 3D.

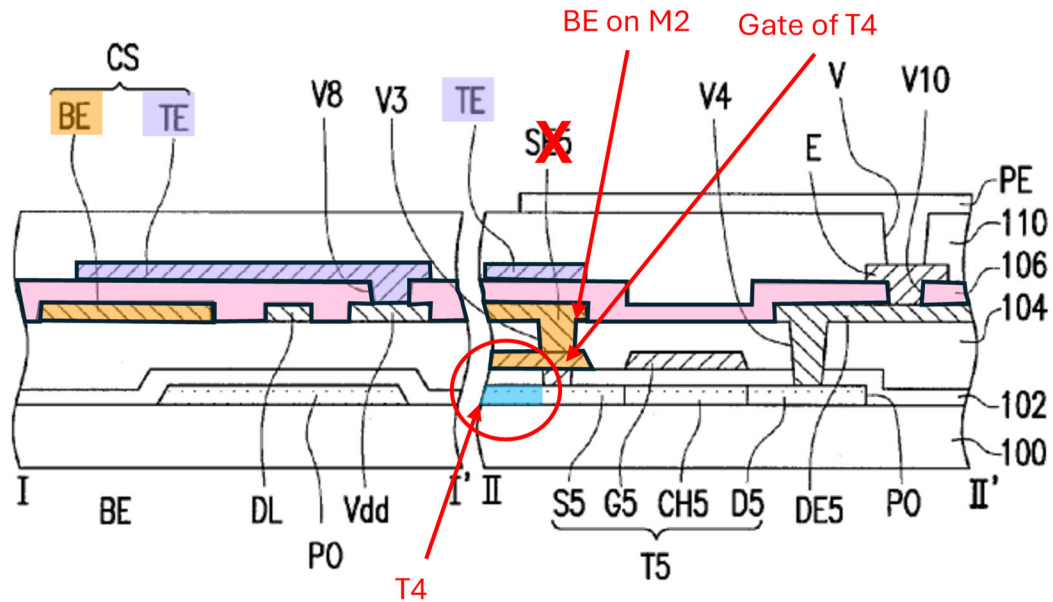


FIG. 5

POSITAs would have recognized that BE comprises a portion of the gate electrode of T4 (“first capacitor plate comprising a portion of the gate electrode of

⁴ Liu uses abbreviations M1 and M2 to denote the first conductive layer and the second conductive layer, respectively; these layers provide electrical conductivity and are made of metal materials. *See* Liu, ¶¶32, 37, 40. A “via” or a “contact via” is a metal structure that connects one metal component to another metal component in a vertical direction. *See, e.g., Id.* ¶44; Kanicki, ¶161n.2.

the second” TFT) because the via directly connects the two together, electrically and physically. Kanicki, ¶161 (citing Noguchi-I).

With respect to Figure 5, Dr. Kanicki notes that TE and BE are labeled correctly, however, SE5 is an incorrect label and the element should be labeled as BE, and POSITAs would have understood the incorrect labeling because, although SE5 is mentioned in the specification (paragraph 40), there are no vias or metal shown in Figures 3B-4 that would denote such a structure. *Id.*, ¶162. Furthermore, Figure 1 clearly shows that S5 is connected to D4, and as shown in Figure 3A, the connection is made in the semiconductor layer without any connections to other layers. *Id.* In Figure 5, V3 is shown to be SE5, which conflicts with Figure 1 because such an equivalence would connect S5 to G4. *Id.* Regardless, the connection of BE to the gate electrode is clearly shown.

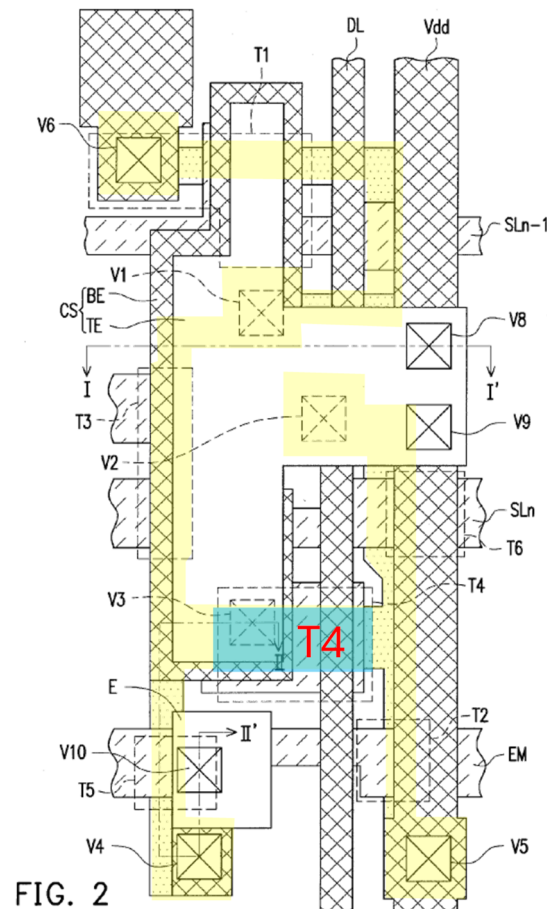
The structure labeled as “Gate of T4” in annotated Figure 5 above is on the M1 layer and is shown unlabeled in Figure 3B. Kanicki, ¶163; Liu, FIG. 3B. Via V3 directly connects the gate electrode of T4 to BE above it. Kanicki, ¶163 V3 is further shown in Figure 3C, connecting BE to the level below (shown in Figure 3B). *Id.*

If PO argues that the BE does not comprise a portion of the gate electrode of T4 based on the above structure of Liu, POSITAs would have found it obvious to use BE directly as the gate electrode of T4, which is also described Liu. Kanicki, ¶164. Liu explains various changes to the capacitor design that include adjusting the

capacitor dielectric material and/or its thickness, allowing the size of the capacitor to be changed while maintaining a selected capacitance. Liu, ¶53. For example, by thinning the dielectric, CS's area can be reduced (i.e., the plate areas can be smaller), allowing placement directly over the semiconductor layer. *Id.* (“...the semiconductor layer PO may be disposed under the capacitor CS.”); Kanicki, ¶164. POSITAs would have thus found it obvious to position BE directly over the semiconductor layer of T4 as taught by Liu (e.g., using the bottom electrode (BE) of the capacitor as gate electrode of T4 as shown in Figure 3B); such a placement of BE would have made BE (or least a part thereof) to include a portion of the gate electrode of T4. *Id.* (citing EX1034-1036). POSITAs would have found this modification obvious because Liu expressly described it. *Id.*

When moving BE to M1 to be directly over the semiconductor layer, TE may not be correspondingly moved. Kanicki, ¶165. Moving or not moving TE to M2 is a design choice dependent on factors related to layout. *Id.* If TE remains in M3, insulating layers 106 and 104 would be designed with the appropriate thickness. *Id.* However, if TE were moved to M2, such that it was in the metal layer directly above BE, then dielectric layer 104, which also covers all TFTs (*see* 1[h], §IV.A.4.i), is the “insulating layer” as claimed. *Id.* These choices and their implementations were well within the capabilities of POSITAs and would have been obvious in view of the express description of Liu regarding those design choices. *Id.*

Liu further shows the channel region of T4 is directly under the gate electrode (shown in blue) (“a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor”). Liu, FIG. 2. Figure 2 (annotated below) shows Figure 3A superimposed on FIG. 2. Kanicki, ¶166. The channel of T4 is the region of the semiconductor layer under the gate of T4. *Id.* This is a common structure in semiconductor engineering, and the gate electrode (e.g., BE) is sized according to the length and width of the channel. *Id.*



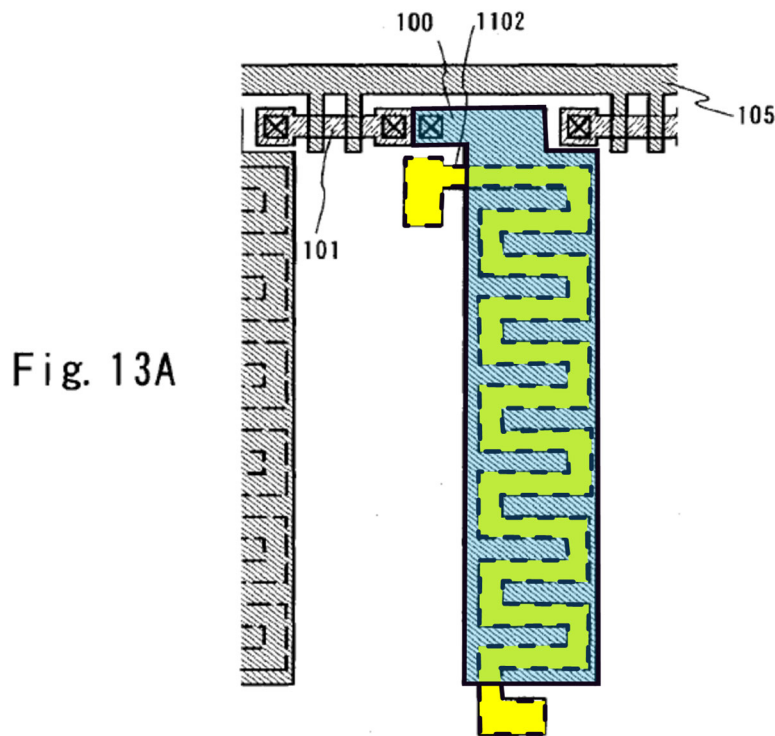
k. 1[ib]

As explained in 1[ia], BE is either directly connected to the gate electrode of T4 in M1 or can be reduced in size and placed directly over the semiconductor layer of T4 in M1. §IV.A.4.j. Accordingly, in either scenario, BE is above T4 (“a portion of a channel region of the semiconductor layer under the gate electrode of the second” TFT). *Id.*; Liu, ¶¶47, 53, FIG 2; Kanicki, ¶167.

While Liu does not expressly disclose a “curved” channel portion of T4, POSITAs would have found it obvious to modify Liu to use Udagawa’s serpentine (“curved”) gate channel for drive transistor T4. Kanicki, ¶168. Liu describes its semiconductor layer is polysilicon. Liu, ¶34. Furthermore, miniaturization of polysilicon TFT circuits causing problems related to the electrical characteristics of the TFTs was well-known. Udagawa, ¶¶5-15. One issue is an increase in dispersion between pixels because of smaller channel length of the drive transistor. *Id.*, ¶¶11-13, 16-17. It was known that dispersion was caused by the driving TFT. *Id.*, ¶17. Thus, POSITAs would have been motivated to look for existing solutions presented by others, such as by Udagawa, to reduce the dispersion effects of polysilicon TFTs in OLED driving circuits. Kanicki, ¶168.

Udagawa recognized this problem and explained dispersion is reduced “[w]hen the channel length of the TFT that supplies an electric current to the OLED is made longer.” Udagawa, ¶22. Udagawa discloses various shapes can be used, such

as a “snake” shape (shown below). *Id.*, ¶31, FIG. 13A; Kanicki, ¶169. Udagawa’s annotated Figure 13A shows a snake-like (i.e., curved or serpentine) channel 1102 (yellow) with gate electrode 100 (blue) covering the channel region. Udagawa, ¶¶31, 102, 154; *Id.*.



For reasons explained in §IV.A.3, POSITAs would have been motivated to incorporate Udagawa’s driving TFT gate shapes (thereby increasing the channel length) in Liu’s miniaturized OLED driving circuit to reduce the dispersion effects that accompany the size reduction of the driving circuit. Kanicki, ¶170. Furthermore, modifying Liu to use Udagawa’s longer gate channel aligns with Liu’s objectives of reducing the size of the pixel structure because forming the gate channel in this way

allows for both a reduction of dispersion and maintaining a reduced size due to the winding nature of the extended channel while enabling an improved operation of T4.

Id.

Udagawa describes different lengths and numbers of serpentine structures to implement the extended channel. Udagawa, ¶20. Thus, POSITAs would have similarly designed Liu's T4 channel region by choosing the length of the channel based on the constraints of a particular design. Kanicki, ¶171. Udagawa recognized this versatility in allowing various channel lengths, shown in Figures 3 and 4. *Id.*; Kanicki, ¶171. Thus, using Udagawa's serpentine gate channel structure would not have substantially increased Liu's pixel structure size because different lengths of the channel could be used. Kanicki, ¶171.

Additionally/alternatively, POSITAs would have understood Udagawa's serpentine channel can be implemented without changing the footprint of Liu's pixel structure by extending the channel area slightly above or slightly below its current position; due to the serpentine nature of the channel and the ability to select the extended channel length, any additional expansion would have been readily implemented within the existing pixel footprint. Kanicki, ¶171. Moreover, POSITAs would have been more than capable of sizing the gate electrode (BE) to cover an appropriate portion of the modified channel. *Id.*; §IV.A.4.j.

Accordingly, Liu as modified by Udagawa teaches a serpentine gate channel region under the gate electrode, which as explained is under BE (“a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor being curved”). Kanicki, ¶172.

I. 1[j]-1[m]

As explained above, Liu discloses a TFT driving circuit with at least six transistors and one capacitor. §§IV.A.4.a, IV.A.4.g. As explained below, Liu discloses each of the recited transistors and connections. The table in 1[b] also shows the transistor mappings. §IV.A.4.c. Liu discloses each transistor in Figure 1 (annotated below). Kanicki, ¶¶173-174.

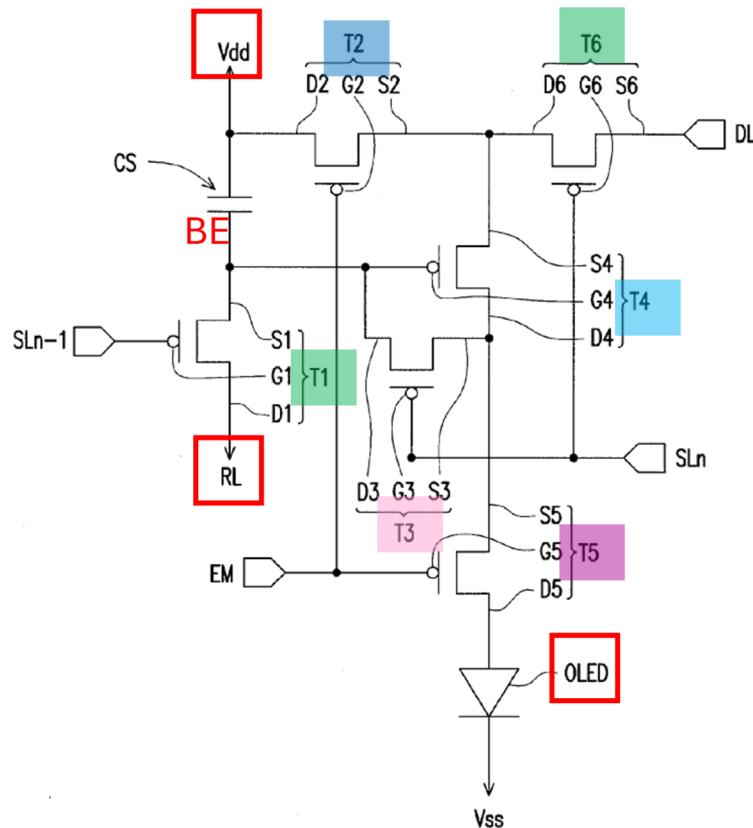


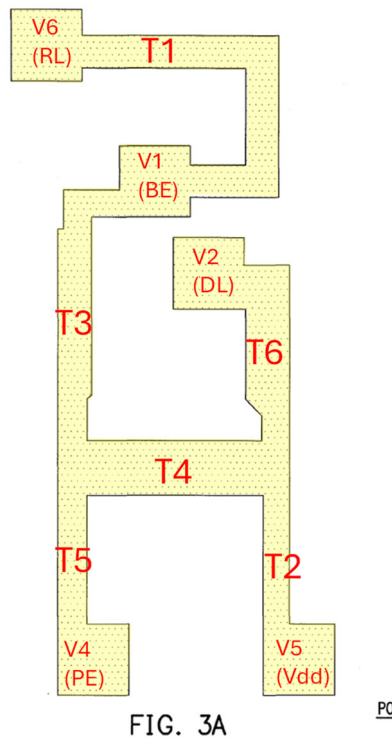
FIG. 1

Regarding 1[j], Liu discloses T3 (“third thin film transistor”) connected to T4 and BE. Liu, FIG 1. T3 is additionally connected to OLED through T5, just as T4 is. As explained above for 1[g], POSITAs would have understood that the arrangement of T3, with connection to OLED through adjacent TFTs, is the same configuration as disclosed in the ’990 Patent. *See* ’990Pat., 6:61-65. Kanicki, ¶176.

Regarding 1[k], Liu discloses T2 (“fourth thin film transistor”) connected to Vdd and T4. Regarding 1[l], Liu discloses T5 (“fifth thin film transistor”) connected to T4, T3, and OLED. Regarding 1[m], Liu discloses T1 (“sixth thin film transistor”)

connected to RL, T3, and BE. Accordingly, Liu discloses the electrical connections in 1[k]-1[m]. *Id.*, ¶177.

Transistors T1 to T6 each utilize and include a portion of the semiconductor layer, which is electrically coupled to the corresponding transistor. Liu, ¶35; Kanicki, ¶178. Further, annotated Figure 3A (below) shows Liu's semiconductor layer is contiguous and reaches all transistors ("the semiconductor layer being extended to and electrically coupled to"). Liu, ¶35, FIG. 3A (annotated); Kanicki, ¶¶178-180.



5. Claims 2-7, 23

As explained above, Liu discloses a TFT driving circuit with at least six transistors and one capacitor. §§IV.A.4.a, IV.A.4.g, IV.A.4.h, IV.A.4.l. As

explained below and shown in Liu's annotated Figure 1, Liu discloses each of the recited transistors and connections. Kanicki, ¶¶181-183.

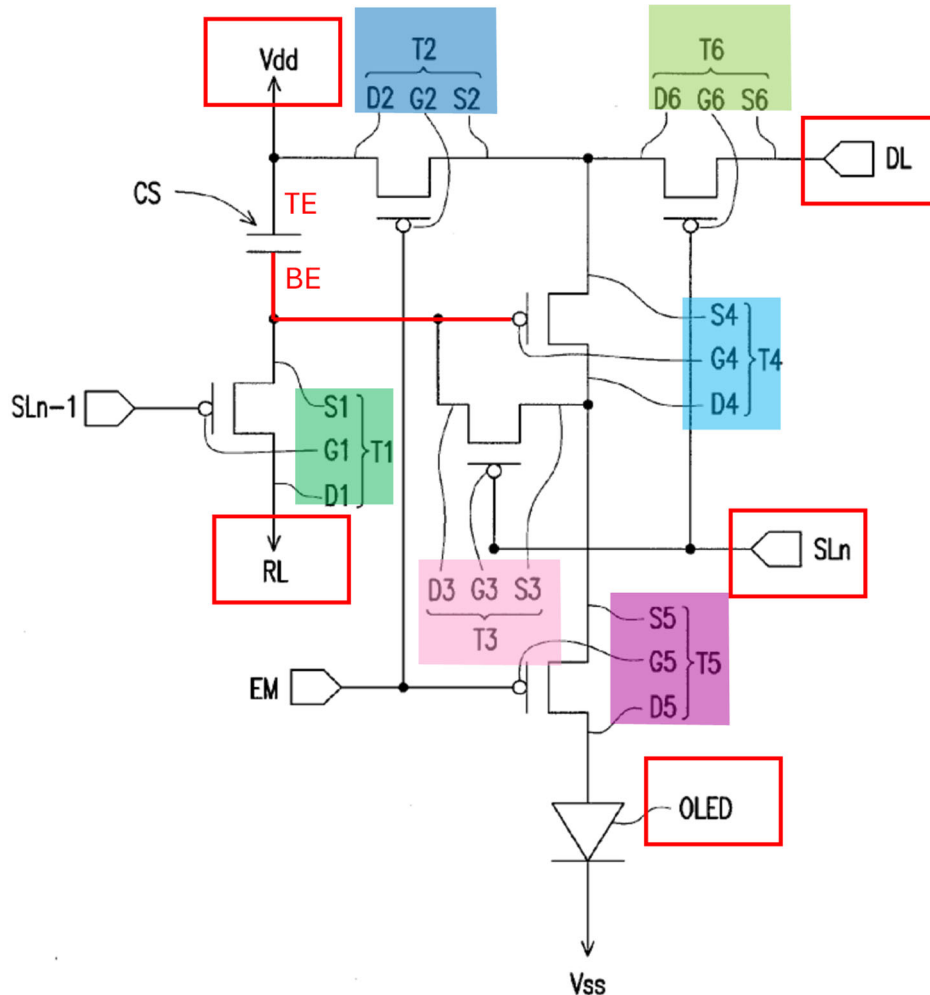


FIG. 1

Claim 2: The gates of T2 (“fourth” TFT) and T5 (“fifth” TFT) are connected together. Liu, FIGs. 1, 2; Kanicki, ¶184.

Claim 3: The gates of T2 and T5 (G2, G5, respectively) receive the signal “EM,” which is “a light emitting signal line.” Liu, ¶38. POSITAs would have understood that EM was “a signal from a light emission control line” because when

EM is applied to T2 and T5, the transistors turn on allowing drive transistor T4 to provide current to OLED, thus allowing the emission of light. *Id.*, ¶185.

Claim 4: T1 (“sixth” TFT) receives SLn-1 (“a second scan line”) at its gate, G1. Liu, ¶38, FIGs. 1, 2; Kanicki, ¶186.

Claim 5: T6 (first” TFT) and T3 (“third” TFT) are connected together. Liu, FIGs. 1, 2; Kanicki, ¶187.

Claim 6: The gates of T6 and T3 receive SLn (“first scan line”). Liu, ¶38, FIG. 1; Kanicki, ¶188.

Claim 7: TE (“second capacitor plate”) is connected to Vdd (“first voltage line”). Liu, ¶44, FIGs. 1, 2; Kanicki, ¶189.

Claim 23: Figure 1 shows the drain (D4) of T4 (“second” TFT) is connected to the source (S3) of T3 (“third” TFT). Liu, ¶35, FIGs. 1, 2. The gate (G4) of T4 is connected to the drain (D3) of T3. *Id.* Furthermore, the source of T3 is connected to V1, which is connected to BE (the gate electrode of T4). Liu, ¶41, FIGs. 1, 2, 3B, 3C; Kanicki, ¶190.

Each of the transistors and gate connections can also be seen in Figure B, below. Figure B is a compilation of Liu Figures 3A and 3B, showing the semiconductor layer PO (yellow) and metal layer 1, M1 (cross-hatched). Liu, ¶¶15-16, 34-35, 37-38; Kanicki, ¶190.

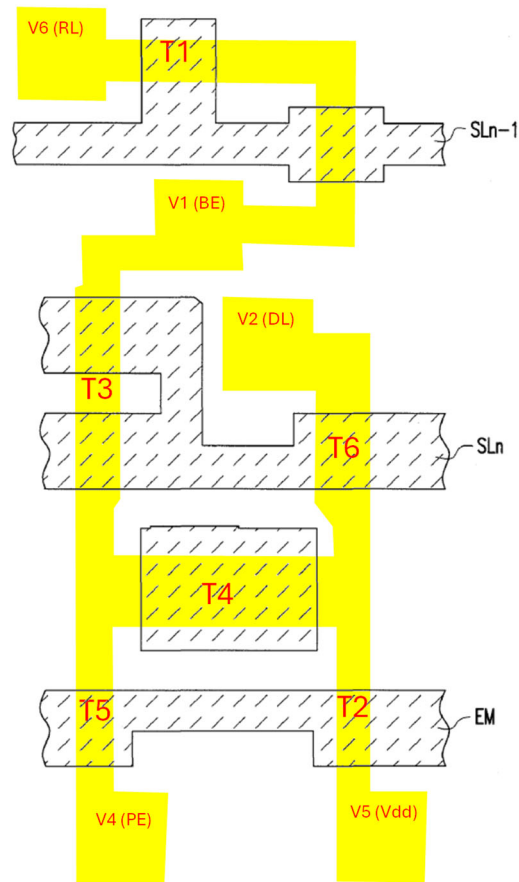
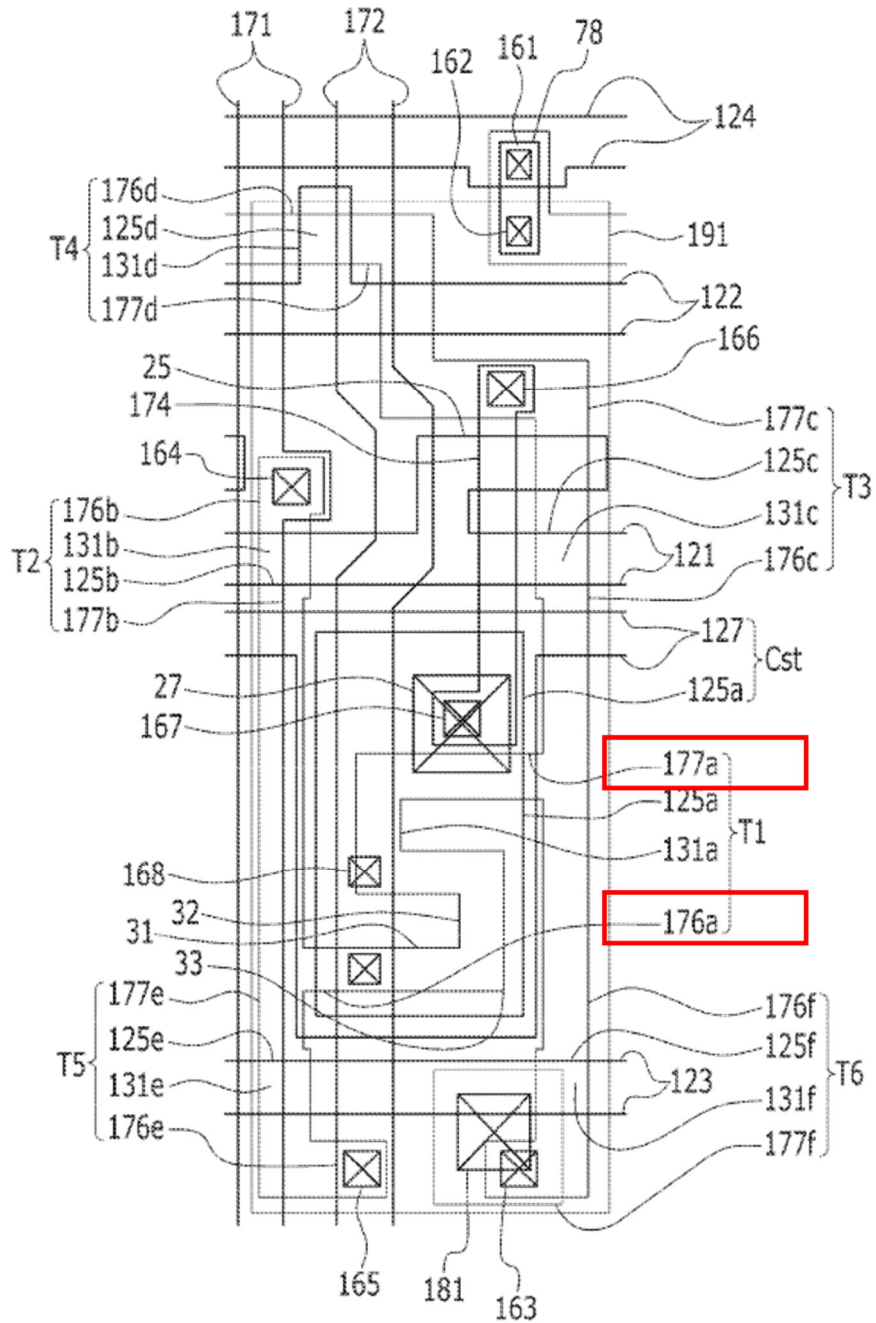


Figure B. Kanicki, ¶191.

If PO argues that Liu does not explicitly show a drain “electrode” of the second TFT, POSITAs would have understood that the drain and source regions of the semiconductor are doped and themselves form drain and source “electrodes.” Kanicki, ¶192. Therefore, being electrically coupled to the drain electrode is equivalently construed as being electrically coupled to the doped semiconductor that forms the drain region. *Id.* This understanding is corroborated by the ‘990 Patent, which describes the doped semiconductor regions as the source and drain

“electrodes,” as shown in annotated Figure 6 below. ’990Pat., 10:7-9; FIG. 6 (below);
Kanicki, ¶192.

FIG. 6



6. Claims 9-10

POSITAs would have understood Liu to disclose p-channel TFTs in its OLED drive circuit because each TFT is shown in Figure 1 with a circle at its gate, a common symbol for p-channel transistors. Liu, FIG. 1; Kanicki, ¶¶194-195. Furthermore, the TFTs are formed in a semiconductor layer comprising, e.g., polysilicon. Liu, ¶¶34-35. Liu, however, does not expressly disclose the dopant used in the semiconductor layer.

Udagawa discloses a TFT driving circuit using a semiconductor layer comprising polysilicon. Udagawa, ¶¶5, 9-11. Udagawa further discloses the use of p-channel TFTs, such as TFTs 404, 406. *Id.*, ¶¶124, 136, 139. Udagawa explains that p-channel TFTs have less dispersion than n-channel TFTs. *Id.*, ¶41.

Udagawa explains forming TFTs in the semiconductor layer involves at least five doping steps to implant n- and p-type impurities in the semiconductor. *Id.*, ¶¶123-130; Kanicki, ¶¶196-197. Udagawa explains that after proper masking of the p-channel TFTs, the semiconductor layer is doped in a third step with n-type impurities, such as phosphorous or arsenic, to a certain concentration. *Id.*, ¶¶124-126; Kanicki, ¶198. In a fourth step, the masks are removed, and new masking is performed before treating the semiconductor regions (i.e., regions 318, 319, 332, and 333 shown in red in annotated Udagawa Figure 7 below) of TFT 404 and 406 (p-channel TFTs) with p-type impurities. *Id.*, ¶127; Kanicki, ¶198. Udagawa notes that

regions 318, 319, 332, and 333 of the p-channel TFTs contain n-type dopants from the preceding step. *Id.*, ¶128. Thus, a sufficient amount of p-type dopants are added to produce the appropriate conductivity. *Id.*, ¶128; Kanicki, ¶198.

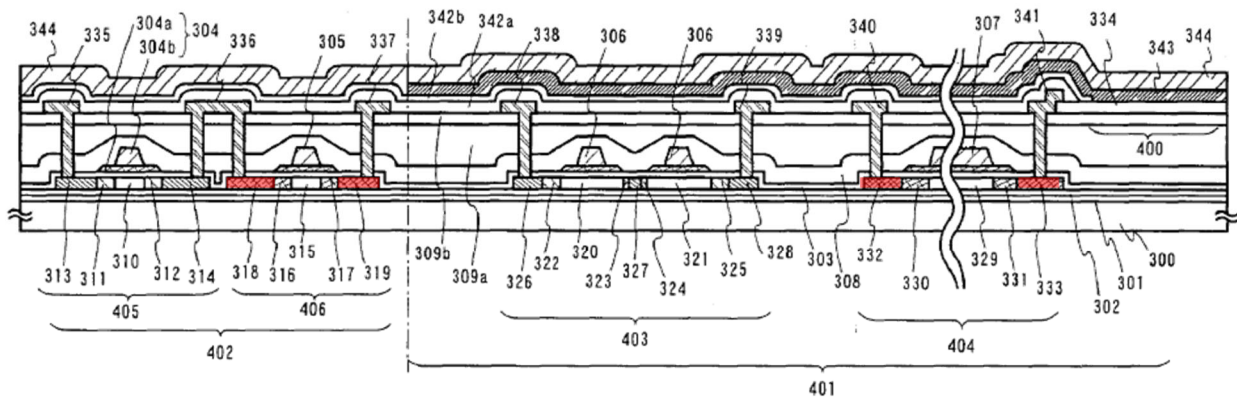
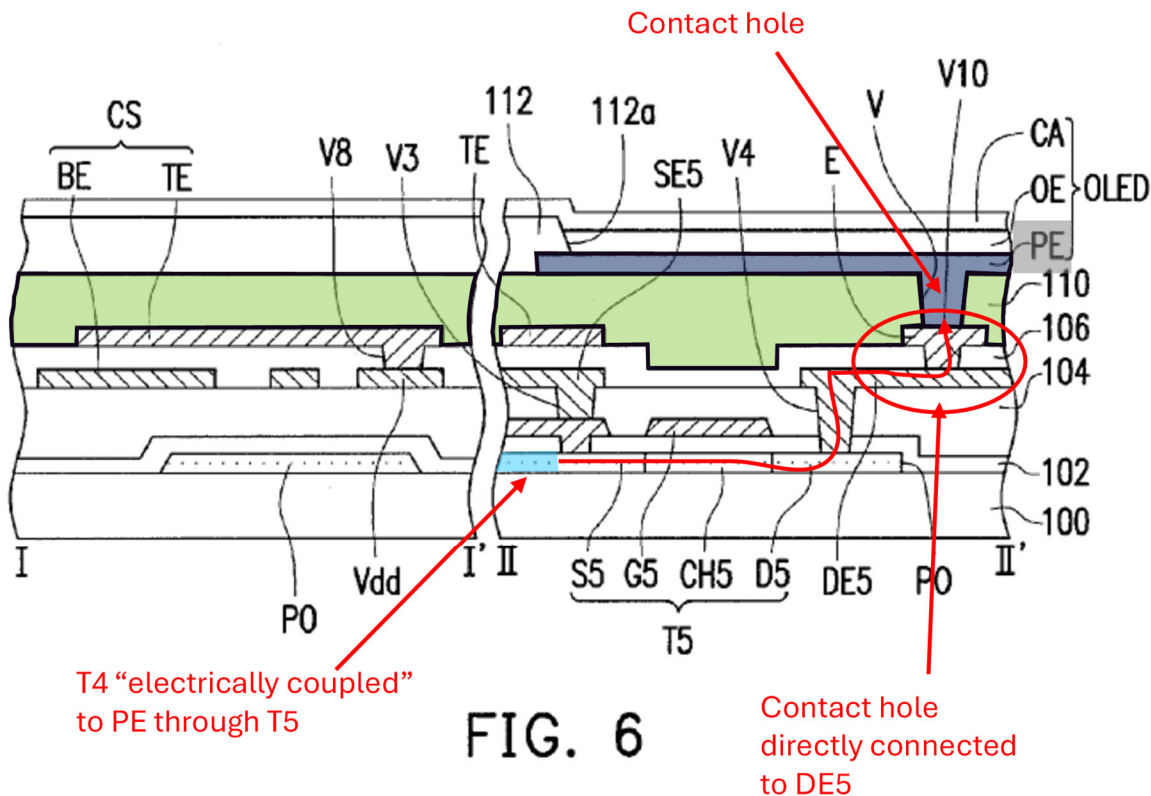


Fig. 7

Although Liu does not expressly disclose n-channel TFTs (as Udagawa does), Liu is not limited to only using p-channel TFTs. Liu, ¶32. Moreover, n-channel and p-channel TFTs can both be used in Liu’s design. Kanicki, ¶199 (discussing Chung’s Figure 11). Thus, Udagawa’s process of forming p-channel TFTs is not counter to Liu’s teachings. *Id.* Because at least one of the steps of Udagawa’s doping treatment consists of doping the semiconductor with an n-type dopant, “portions of the semiconductor layer are doped with N-type impurities” (Claim 9). And because at least one of the steps of the doping treatment consists of doping the semiconductor with a p-type dopant, “portions of the semiconductor layer are doped with P-type impurities” (Claim 10).

7. Claims 24-25

Liu discloses a **planarization layer 110** (“protective layer”) is disposed on third insulating layer 106 covering the TFTs and capacitor (“covering the plurality of driving circuits”). Liu, ¶¶46, 55, FIGs. 5-6. A pixel electrode is disposed on the planarization layer 110 (“each of the organic light emitting diodes further comprises a pixel electrode on the protective layer”). *Id.* Liu further explains that the pixel electrode is connected to the drain of T5 through via structure V. *Id.* As explained in 1[g], T4 (“second” TFT) is connected to OLED (and the pixel electrode) through T5 (“pixel electrode being electrically coupled to the second thin film transistor through a contact hole”). §IV.A.4.h; Kanicki, ¶¶210-202.



Claim 24 requires the pixel electrode to be “electrically coupled” to T4 through a contact hole, while claim 25 requires the pixel electrode to be “electrically coupled” to T5 through a contact hole. As shown above the pixel electrode, PE, is connected to T5 through a via (“contact hole”) and T4 is connected to T5. Kanicki, ¶203. Accordingly, the pixel electrode is “electrically coupled” to T5 and to T4. *Id.*

Liu’s Figure 1 shows the connections of T4 and T5. Annotated Figure 6 above shows the planarization layer, pixel electrode, and connections to the TFT driving circuit (T4 and T5). Liu, FIG. 6; Kanicki, ¶¶204-205.

8. Claim 26

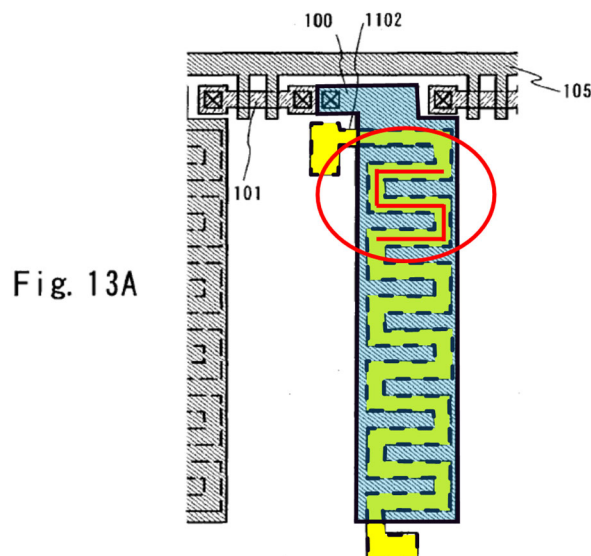
SLn is in material layer M1. Liu, ¶38. As explained in 1[ia], the storage capacitor bottom electrode BE is the gate electrode of T4. §IV.A.4.j. As also explained above, BE can be (a) reduced in size and placed directly over the semiconductor layer in M1, or (b) is directly connected to the gate electrode of T4 on M1. *Id.*; Kanicki, ¶¶206-207. In scenario (a), BE is directly the gate electrode of T4 and is in layer M1, and in scenario (b), BE directly connects to the gate electrode of T4 in M1 through connector V3, as shown in Liu’s Figure 6. POSITAs would have understood that the material in V3 would be the same as the material in BE and the gate electrode of T4 to bond well and make a good connection, and thus the capacitor plate, connector V3, and the gate of T4 would form a contiguous connection surface. *Id.* In either scenario (a) or (b), the material of M1 is used for

BE. Liu further discloses that SLn (“first scan line”) is in M1 (“the same material layer”). Liu, ¶38. Liu expressly discloses that the material used for M1, M2, and M2 can be the same material. Liu, ¶¶37, 40, 44. Accordingly, POSITAs would have understood that M1 (and the BE portion connected to it in scenario (b)) constitutes a single “material layer,” and BE and SLn include that material. Kanicki, ¶207.

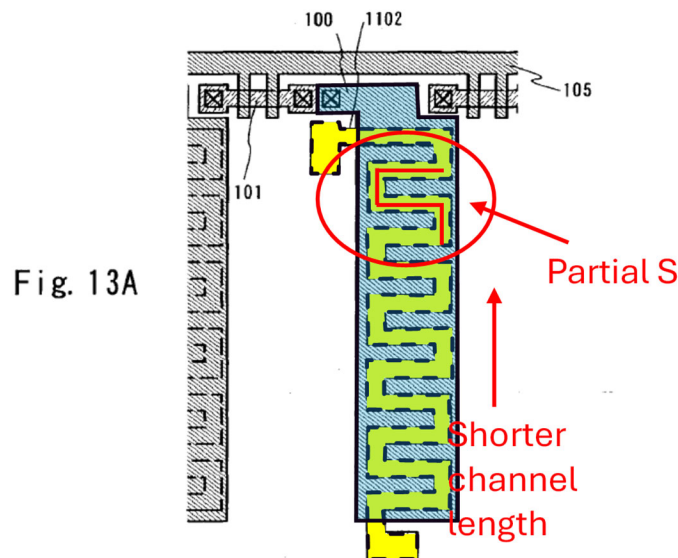
9. Claims 27-30

As explained in 1[ib], Liu-Udagawa teaches drive transistor T4’s “curved” channel. §IV.A.4.k. As explained below, utilizing Udagawa’s serpentine channel shape for drive transistor T4, many different apparent shapes are realized. Kanicki. ¶¶209-211.

Regarding claim 27, incorporating Udagawa’s serpentine shape, produces an “S” shape structure in the gate channel of T4. Kanicki, ¶212. One example is shown in annotated Figure 13A from Udagawa. *Id.*

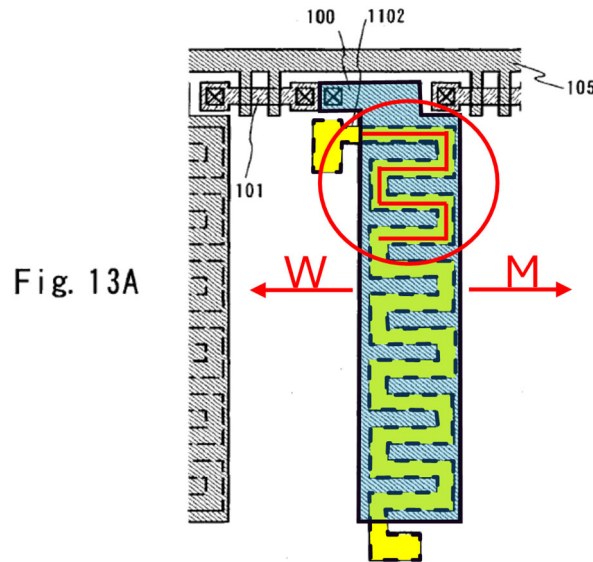


Claim 28: Udagawa discloses the channel can be elongated by shorter or longer lengths. Udagawa, ¶23. Liu does not expressly disclose the length of the channel of T4. POSITAs would have thus understood that the serpentine shape of Udagawa may be shorter or longer, depending on the application. Kanicki, ¶213. Accordingly, shortening the above “S” shape would yield a partial “S” shaped channel, as shown in annotated Figure 13A, below. *Id.*



Udagawa, FIG. 13A (annotated).

Claims 29 and 30: Udagawa discloses an “M” and “W” shape. Kanicki, ¶214. POSITAs would have understood that an “M” shape and a “W” shape are merely the same shapes viewed from different angles, and the claims do not specify from which angle the channel should be viewed. *Id.* Annotated Figure 13A, below, shows such a configuration. *Id.*



B. Ground 1B: Claim 8 is Unpatentable over Liu, Udagawa, and Nakayama

1. Nakayama

Nakayama (EX1007) describes variations in the drive currents supplied to different pixels may be caused by variations in the electrostatic capacitances of the holding and kick capacitors. *Id.*, ¶5. To suppress capacitance variation due to lateral misalignment, such as mask misalignment, Nakayama teaches the upper electrode of capacitors can be configured to have a larger surface area than the bottom electrodes thereof. *Id.*, ¶38.

Nakayama is analogous art to the '990 Patent because it is in the same field of endeavor. Both are directed to reducing variations in a current (or equivalently, maintaining a constant current) supplied to the driving TFT of in an OLED display. *Id.*, ¶¶4-5; Kanicki, ¶¶215.

2. Motivation to combine Liu, Udagawa, and Nakayama

As discussed above, Liu is directed to a reduced-size pixel structure. §IV.A.4.a. Nakayama is also related to OLED pixels and displays. Nakayama, ¶¶5-6. Accordingly, POSITAs would have recognized the complementary teachings of those references and would have been motivated to combine their teachings. Kanicki, ¶¶216-217.

Notably, Nakayama describes capacitor configurations and variances in capacitance affecting TFT driving circuits. Nakayama, ¶¶4-5. Thus, POSITAs would have been motivated to improve Liu's drive circuit operation based on the teachings of Nakayama to reduce variations of the driving TFT. Kanicki, ¶217.

Nakayama recognized OLED displays can be improved by reducing capacitance variations (e.g., due to mask misalignment), which included configuring the upper electrode of a capacitor to have a larger surface area than the bottom electrode. Nakayama, ¶38. POSITAs would have thus found it obvious and would have been motivated to combine Liu with Nakayama, and specifically to use Nakayama's configuration of the larger upper capacitor electrode to improve Liu's OLED driving circuit. Kanicki, ¶218. This combination would conform to Liu's objectives of reducing the size of the pixel structure. *Id.* And forming the top capacitor electrode of Liu to have a larger surface area than the bottom capacitor electrode would have resulted in mitigating capacitance variations, which would

have improved the operation of the driving TFT of Liu, while maintaining a reduced size. *Id.*

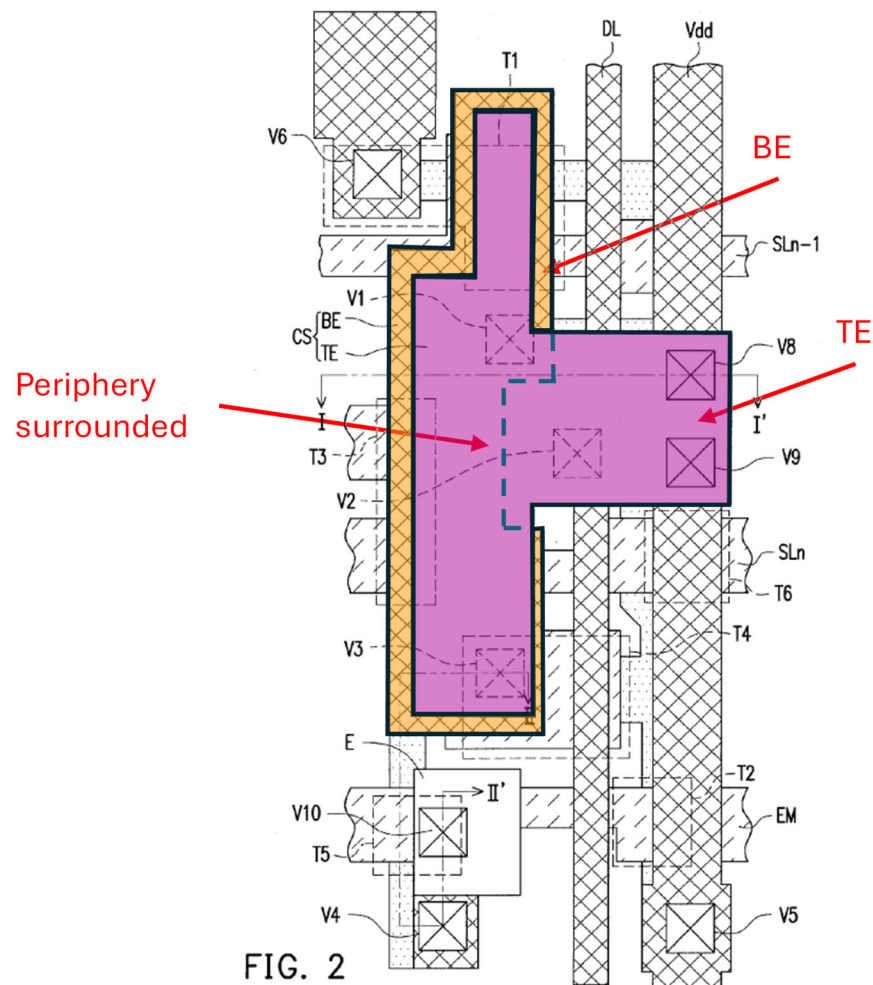
Notably, POSITAs would have been motivated to apply Nakayama's known technique (shaping the capacitor plates such that the upper plate has a larger area than the lower plate as Nakayama disclosed) to a known device ready for improvement (Liu's OLED driving circuit) to yield predictable results (the threshold voltage variation in the driving TFT being reduced). *Id.*, ¶219. POSITAs would have had a reasonable expectation of success, because shaping the capacitor plates in an integrated circuit for an OLED display was well-known by 2012, as evidenced by the teachings of Nakayama and other known prior art references, and such modifications were well within the skill set of POSITAs. *Id.*

Furthermore, the Liu reference can be combined individually with each of Udagawa and Nakayama. In each instance, the combination involves modifying a distinct aspect of Liu. *Id.*, ¶220. POSITAs would have recognized that there is no interference among the proposed modifications. *Id.* Accordingly, POSITAs would have found it obvious and been motivated to combine Liu with each of Udagawa and Nakayama, and would have had a reasonable expectation of success. *Id.*, ¶¶220-221.

3. Claim 8

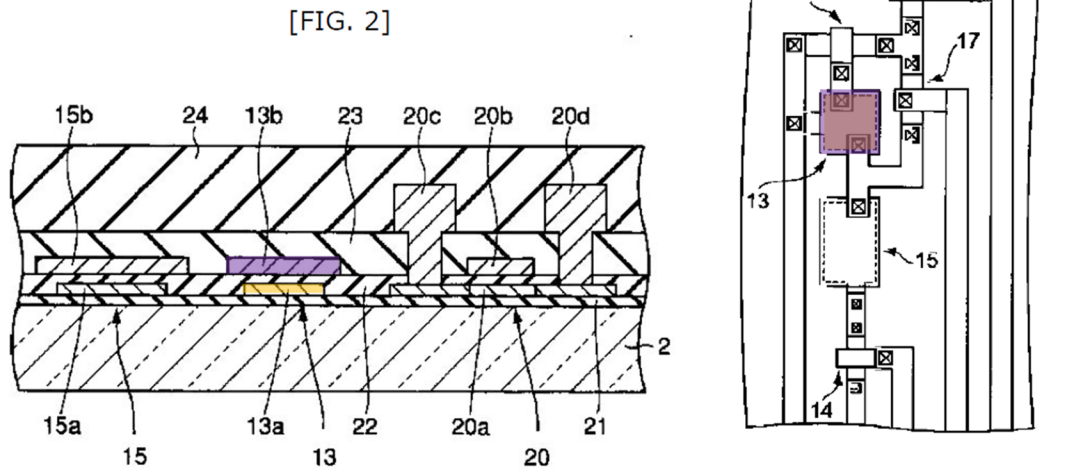
Liu teaches TE surrounds a portion of BE (see annotated Figure 2 below); the dashed line represents “a” periphery of the BE (orange), which is surrounded by TE (purple). Kanicki, ¶223. Based on the plain and ordinary meaning of “surround[ing] a periphery,” POSITAs would have understood that at least a portion around the outside of BE would be surrounded by TE.⁵ *Id.*; EX1015, 923 (“the outermost part or region within a precise boundary”); EX1016, 1066 (“the outer limits or edge of an area or object”).

⁵ Notably, claim 8 does not recite “entire periphery” or “entire surface area” to be surrounded; also the ‘990 Patent’s detailed description neither explains nor attaches any particular significance to a periphery. Kanicki, ¶223.



If PO argues that TE does not “completely surround[] a periphery of” BE, POSITAs would have found it obvious in light of Nakayama. Nakayama discloses an upper electrode of a holding capacitor having a larger surface area than the bottom electrode. Nakayama, ¶38, FIGs. 2, 4. Annotated Nakayama Figures 2 (left) and 4 (right) show the lower capacitor electrode 13a (orange) is within the perimeter of the upper electrode 13b (purple). Nakayama, ¶¶35, 38; Kanicki, ¶224. This capacitor electrode configuration suppresses the variation in capacitance with respect to the deviation in the X-Y placement of the top electrode. Nakayama, ¶38; Kanicki, ¶224.

【図4】



Liu's OLED pixel would have benefited from and accommodated this modification. As explained above, Liu describes BE is either directly connected to the gate electrode of T4 in M1 or can be reduced in size and placed directly over the semiconductor layer in M1. §IV.A.4.j; Kanicki, ¶225. In the former, no other metal layer is present in metal layer 3. Liu, ¶44; FIG. 3D. Thus, there is room for the top plate to expand relative to the bottom plate without affecting the capacitance. *Id.* POSITAs would have found it obvious to enlarge TE because it would have allowed for fabrication variances to maintain the capacitance of CS, as Nakayama explains.

Id.; §IV.B.2. This is possible because the capacitance is determined by the smaller of the two electrodes in the capacitor. Kanicki, ¶225 (discussing Murade, ¶98).

For the latter—BE placed over the semiconductor layer—BE is directly the gate of T4 and TE may either remain in M3 or be moved to M2. §IV.A.4.j. As explained above, TE is unrestricted and POSITAs would have found it obvious to enlarge TE to realize the advantages of Nakayama. Kanicki, ¶226. It would have also been within the skill of POSITAs to choose a dielectric and adjust the layout to accommodate TE over BE to obtain a particular capacitance value. Kanicki, ¶¶226-228. As Dr. Kanicki explains, POSITAs can reason the relatively simple arrangement of signal lines and CS to achieve the arrangement disclosed in Nakayama, *Id.* Any such changes to the capacitor design would have been well within POSITAs' skills and capabilities and would have amounted to routine design considerations. *Id.*, ¶228 (citing EX1033). Accordingly, for the reasons explained in §IV.B.2, POSITAs would have been motivated to incorporate Nakayama's capacitor plate sizing in Liu to maintain the capacitance of Liu's CS capacitor. Kanicki, ¶¶229-230.

C. Ground 1C: Claims 11-19, 21, and 22 are Unpatentable over Liu, Udagawa, and Chung

1. Chung

Chung (EX1008) describes an OLED display pixel circuit similar to the circuit shown in Figure 1 of the '990 Patent (i.e., with scan lines, signal lines, a driving transistor, five switching transistors, and a storage capacitor), but additionally includes a switching transistor SW_TR6 for applying a reverse bias, i.e., a seventh transistor. Chung, ¶57.

Chung teaches in an initialization period (i.e., a non-light emission period) of operating the pixel circuit, a low-level scan signal that is applied to the initial switching transistor SW_TR 5 is also applied to the switching transistor SW_TR6 for applying a reverse bias to the OLED, thereby preventing degradation of the OLED. *Id.*, ¶¶83-84.

Chung is analogous art to the '990 Patent because it is in the same field of endeavor. Kanicki, ¶¶231-233. For example, both are directed to compensating the threshold voltage of the driving transistor. Chung, ¶87.

2. Motivation to combine Liu, Udagawa, and Chung

As discussed above, Liu is directed to a reduced-size pixel structure, which includes a plurality of TFTs. §IV.A.4.a. Liu does not limit the number of TFTs in its OLED driving circuit. *Id.*, ¶32. Chung discloses an OLED drive circuit similar to Liu, which additionally includes a seventh TFT to apply a reverse bias voltage to the

OLED, which increases the OLED's lifespan and the uniformity of brightness of the respective pixels by the elimination of the degradation. Chung, ¶¶11, 57. Kanicki, ¶234.

POSITAs would have thus recognized Liu's OLED driving circuit would be improved by introducing a seventh TFT, as described by Chung, for applying a reverse bias to the OLED, thereby preventing degradation of the OLED. Chung, ¶¶83-84. Kanicki, ¶236.

POSITAs would have had a reasonable expectation of success because Chung explicitly described the implementation of a seventh TFT; the introduction of a single additional TFT would not have appreciably impacted the size of Liu's driving circuit, and such modification was well within the skill set of POSITAs. Kanicki, ¶237.

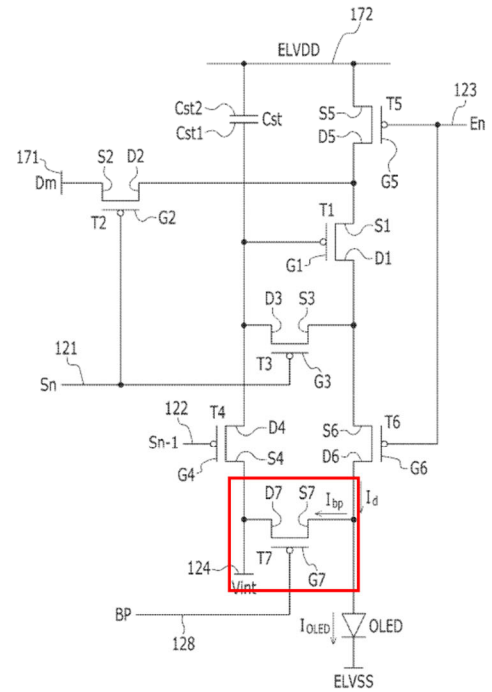
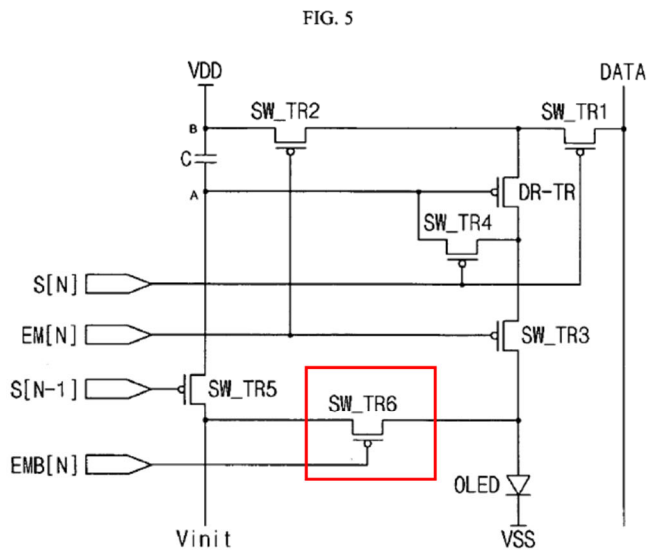
POSITAs would have been motivated to apply Chung's known technique (adding a seventh TFT) to a known device ready for improvement (Liu's 6T1C OLED driving circuit) to yield predictable results (preventing degradation of OLED during the initialization period). POSITAs would have had a reasonable expectation of success, because incorporating a seventh transistor into a 6T1C circuit was well-known by 2012, as evidenced by Chung and other known prior art references, and such modifications were well within the skill set of POSITAs. *Id.*, ¶237.

Furthermore, Liu can be combined individually with each of Udagawa and Chung. In each instance, the combination involves modifying a distinct aspect of Liu. POSITAs would recognize that there is no interference among the modifications, and each combination can be implemented without affecting the others. Accordingly, POSITAs would have found it obvious and would have been motivated to combine Liu with each of Udagawa and Chung. Such modifications would have been well within the skill set of POSITAs because it involved routine changes to the driver circuit, and POSITAs would have thus had a reasonable expectation of success in making those modifications. Kanicki, ¶¶237-238.

3. Claim 11

Liu discloses its driving circuit can have more or less than six TFTs. Liu, ¶¶32, 58. Chung discloses an OLED drive circuit similar to those described in Liu and in Figure 10 of the '990 Patent, which additionally includes a seventh TFT. §IV.C.1. Chung's annotated Figure 5 (left) below and '990 Patent's Figure 10 (right) highlight the seventh TFT. Kanicki, ¶¶240-242.

FIG. 10



As shown below, Chung’s circuit (left) is identical to Liu (right), except for the additional seventh TFT (SW_TR6). *Id.*, ¶243.

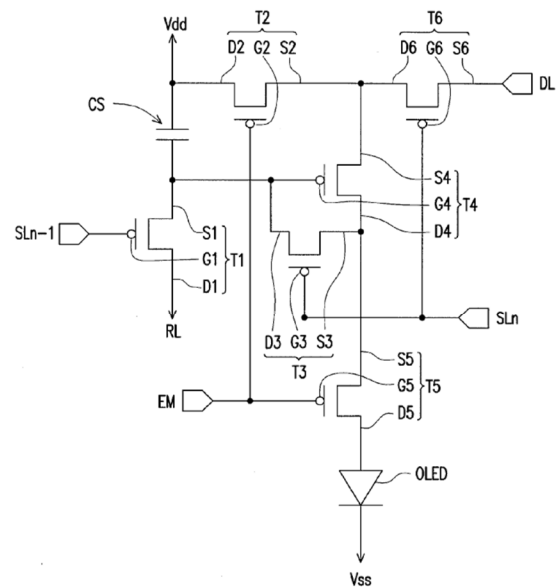
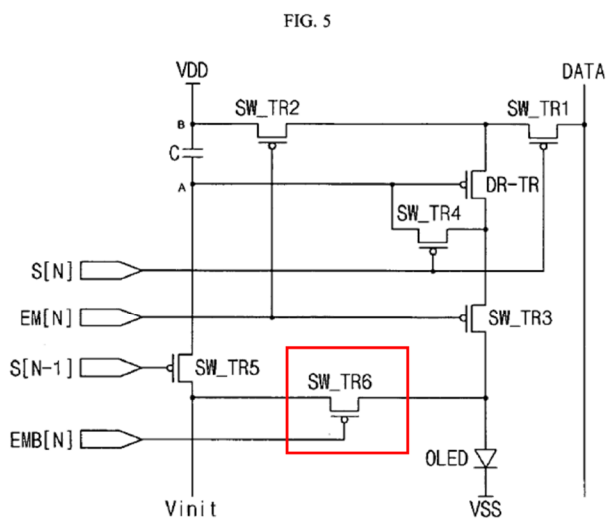
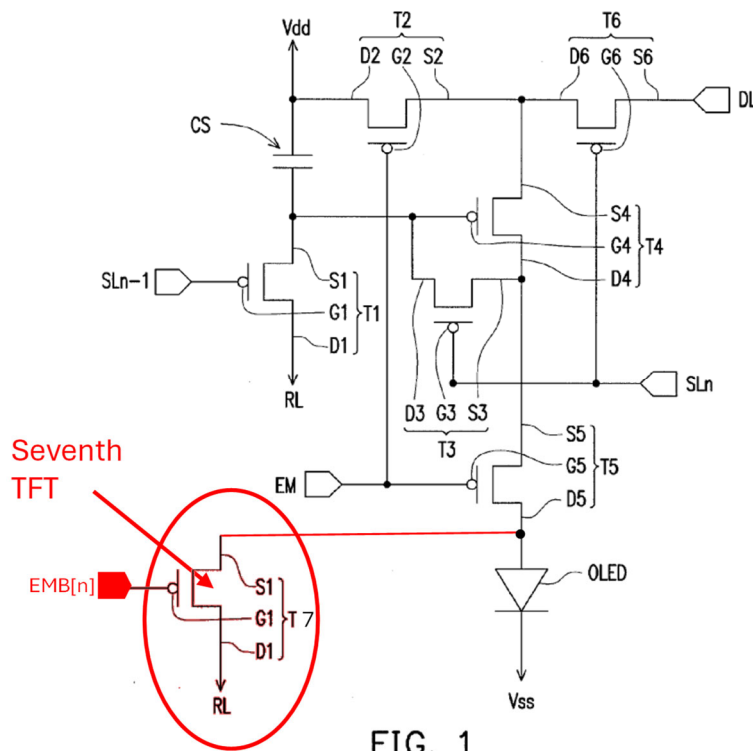


FIG. 1

Chung discloses SW_TR6 in Figure 5 connected to the OLED and initialization TFT (SW_TR5). Chung, ¶¶57, 60, 63. The addition of SW_TR6 prevents “degradation of the organic light emitting diode OLED” during the initialization period. Chung, ¶84.

POSITAs would have been motivated to modify Liu to incorporate Chung’s seventh TFT to increase lifespan of the OLED during initialization. Kanicki, ¶¶244-245. Such a modification would have improved the performance of Liu’s drive circuit with minimal increase in size. *Id.*, ¶245. Furthermore, as shown above, Chung and Liu’s circuits are identical except for the additional TFT. *Id.* An example modified drive circuit incorporating Chung’s TFT in Liu’s drive circuit is shown below in modified Figure 5. *Id.*



Accordingly, POSITAs would have been motivated to incorporate Chung's seventh TFT in Liu to maintain enhance the drive circuit to prevent degradation of the OLED. §IV.C.2; Kanicki, ¶¶246-247.

4. Claim 12

As explained in ¶1[g] and ¶1[j], each of transistors T1 to T6 utilize and include a portion of the semiconductor layer, which is electrically coupled to the corresponding transistor. Liu, ¶35; §§IV.A.4.h, IV.A.4.i. POSITAs would have understood that when adding an additional TFT, the semiconductor layer would be deposited for that new TFT because it would have used the design disclosed in Liu. Kanicki, ¶249. Furthermore, Liu discloses the semiconductor layer is contiguous

between all TFTs. Liu, FIG. 3A. As a practical matter, POSITAs would have found it obvious to continue the semiconductor layer to incorporate T7. Kanicki, ¶249. Using a contiguous semiconductor layer would have been a natural choice given Liu's layer was contiguous. *Id.* Moreover, it was one of two options (contiguous or non-contiguous). *Id.* Accordingly, Liu-Udagawa-Chung teaches or suggests a seventh TFT with the semiconductor layer extended to incorporate that TFT. *Id.*, ¶250

5. Claim 13

Chung discloses the seventh TFT has a gate signal of EMB[n] ("bypass control line"). Chung explains EMB is the "emission reverse control signal" and supplies a signal to effect a reverse bias of the OLED. Chung, ¶63. POSITAs would have recognized that activation of the seventh TFT would have bypassed and accumulated charge on the OLED and thus been a "bypass" control signal for the voltage on the OLED. Kanicki, ¶¶251-252.

6. Claims 14-19

As explained Ground 1A in §IV.A.5, Liu discloses these claims. The addition on the seventh TFT does not alter Liu's disclosure. Kanicki, ¶¶253-254.

7. Claims 21-22

As explained in Ground 1A, Udagawa discloses that P- and N-type impurities are doped into p-channel TFT transistors formed in the semiconductor layer PO.

§IV.A.6. The addition of Chung’s seventh TFT does not alter the structure of the semiconductor layer but only adds an additional n-channel or p-channel TFT. Kanicki, ¶¶255-256.

D. Ground 1D: Claim 20 is Unpatentable over Liu, Udagawa, Chung, and Nakayama

1. Motivation to combine Liu, Udagawa, Chung, and Nakayama

As previously discussed, the Liu reference can be combined individually with each of the cited references—Udagawa, Nakayama, and Chung. In each instance, the combination involves modifying a distinct aspect of Liu. For example, Udagawa modifies the channel of the driving TFT, Nakayama modifies the relative shapes of the storage capacitor plates, and Chung modifies the 6T1C circuit by incorporating a seventh TFT. A POSITA would recognize that there is no interference among the modifications, and each combination can be implemented without affecting the others. Accordingly, a POSITA would have found it obvious and would have been motivated to combine Liu with each of Udagawa, Nakayama, and Chung. Kanicki, ¶257.

2. Claim 20

As explained in claim 8 in Ground 1B, Liu-Udagawa-Nakayama combination teaches to make TE completely surround a “periphery” of BE. §IV.B.3. The addition of Chung’s seventh TFT does not alter the explanations above. Kanicki, ¶259-261.

**E. Ground 2A: Claims 1-10 and 21-30 are Unpatentable over
Noguchi-I and Udagawa**

1. Noguchi-I

Noguchi-I (EX1010) describes a storage capacitor for an OLED display utilizing a shield electrode provided in a wiring layer between the pixel electrode and a wiring layer in which the gate electrode is provided; the shield electrode forms a region covering the gate electrode, reducing the parasitic capacitance formed between the gate electrode of the driving transistor and a pixel electrode (anode) of the OLED. Noguchi-I, ¶35.

Noguchi-I and the '990 Patent are in the same field of endeavor; similar to the '990 Patent, Noguchi-I is directed to the pixel structure of an OLED display driven by scanning lines, power source lines, signal lines, and transistors T1 to T6. Noguchi-I, ¶70. Similarly, both endeavor to compensate for the variability of the threshold voltage of the driving TFT. *Id.*, ¶15; Kanicki, ¶262-264.

2. Motivation to combine Noguchi-I and Udagawa

Both Noguchi-I and Udagawa described drive circuits for OLED displays and both sought to improve the design and operation of OLEDs. Noguchi-I describes a pixel structure with reduced parasitic capacitance that improved image quality. Noguchi-I, ¶¶12, 15, 72. And, Udagawa describes drive circuit configurations that improved OLED's reliability, and consequently, its operations and image quality. Udagawa, ¶12. Therefore, POSITAs would have been motivated to combine the

complementary teachings of Noguchi-I with Udagawa to achieve further improvements in image quality of the OLED display. Kanicki, ¶¶265-266.

Specifically, Udagawa disclosed when the channel length of a TFT increases, the oxide film capacitance C_{ox} becomes larger, and at least a portion of this capacitance can be used as a retention capacitance of the OLED, thus improving OLED's image quality. Udagawa, ¶64; Kanicki, ¶267. POSITAs would have found it obvious and would have been motivated to combine the complementary teachings of Udagawa with Noguchi-I, and specifically to use Udagawa's serpentine channel in Noguchi-I's driving TFT to further improve the OLED operation. Kanicki, ¶267.

Notably, POSITAs would have been motivated to apply a known technique (using Udagawa's TFT with a longer channel) to a known device ready for improvement (Noguchi-I's pixel structure) to yield predictable results (capacitors being formed correctly and improving image quality). POSITAs would have had a reasonable expectation of success, because using TFT with a longer channel to reduce dispersion and increase capacitance was well-known by 2012, evidenced by the teachings of Udagawa and other known prior art references, and such modifications were well within the skill set of POSITAs. *Id.*, ¶¶268-269.

3. Independent Claim 1

Noguchi-I describes a “pixel of a conventional organic EL display device” with reference to Figures 8 and 9. *Id.*, ¶11. It then presents four related embodiments

that build upon each other to address the perceived deficient response of the pixel. *Id.*, ¶¶66-95; Kanicki, ¶270. All embodiments are based on the circuit diagram of Figure 1 (Noguchi-I, ¶¶66, 74, 79, 88) but progressively alter the construction of capacitor C1 and the gate electrode of T4 in different ways. *Id.*, ¶¶72, 77, 83, 91; Kanicki, ¶270. Petitioner relies on the cumulative teachings of Noguchi-I embodiments that culminate in embodiment 4 (Figure 7). To the extent other figures of Noguchi-I are used below, they represent common features of Noguchi-I's invention. *Id.*

a. 1[pre]

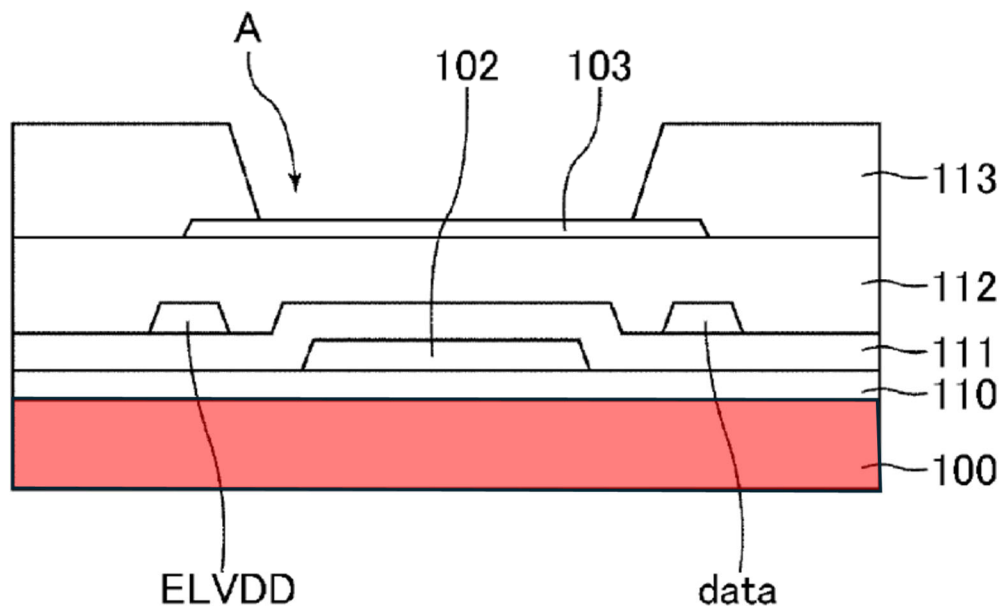
Noguchi-I discloses “an organic EL **display device**” with “a current emissive element such as an organic EL element.” Noguchi-I, Abstract, ¶¶1, 41. The display comprises a plurality of “pixels” (*id.*, ¶¶3, 70 (identifying one “display unit” having one pixel)), where the “organic EL element” is an OLED (*id.*, ¶11, FIG. 1); Kanicki, ¶¶271-273.

b. 1[a]

Noguchi-I discloses a pixel comprising a “**substrate 100**,” among other things. Noguchi-I, ¶¶66-69, 98-114, FIGs. 3 (annotated below), 6, 9; Kanicki, ¶¶274-275. It was well-known that substrates for OLED pixels comprised glass, among other

materials, and needed to be non-conductive so that the circuits placed on them operated properly. Kanicki, ¶275 (citing Liu, ¶33; Kim, 5:4-11).

Fig. 3

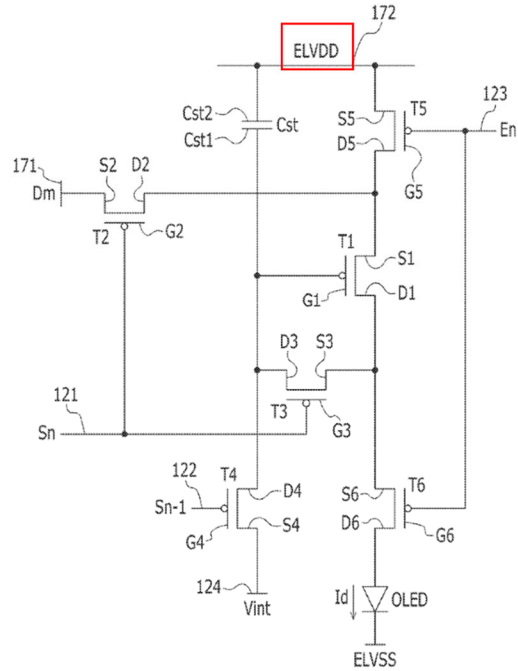
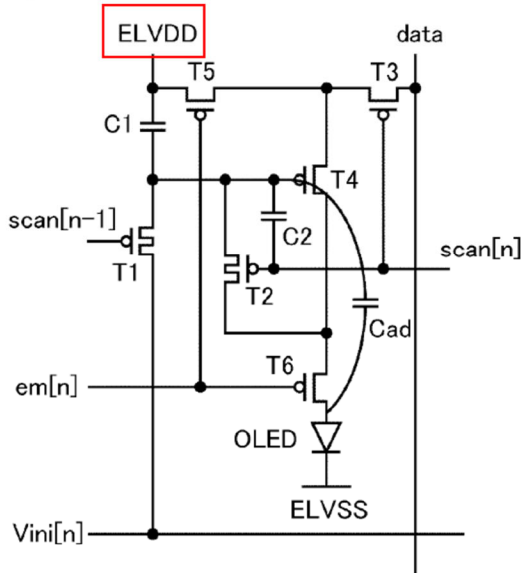


c. 1[b]

Noguchi-I discloses the “first voltage line” as a “power source line ELVDD” in a second wiring layer. Noguchi-I, ¶71, FIG. 1; Kanicki, ¶¶276-277. POSITAs would have understood ELVDD is a “voltage line” because ELVDD is common notation to denote a driving voltage applied to a transistor that is also used by the '990 Patent. '990Pat., 6:25-37; Kanicki, ¶277. Annotated Noguchi-I's Figure 1 (left) alongside the '990 Patent's Figure 1 (right) show ELVDD and the similarities between the circuits. Kanicki, ¶277.

FIG. 1

Fig. 1



Further, Petitioner has provided the table below to cross-reference each transistor and signal line of the '990 Patent to similar elements in Noguchi-I. Kanicki, ¶278; *see also* Noguchi-I, ¶¶98-114.

Claims	'990	Noguchi-I
1 st TFT	T2	T3
2 nd TFT	T1	T4
3 rd TFT	T3	T2
4 th TFT	T5	T5
5 th TFT	T6	T6
6 th TFT	T4	T1
Capacitor	Cst	C1
First Capacitor Plate	125h	Gate electrode 102
Second Capacitor Plate	127	Shield electrode 104
1 st Voltage line	ELVDD	ELVDD
2 nd Voltage line	Vint	Vini[n]
OLED	OLED	OLED

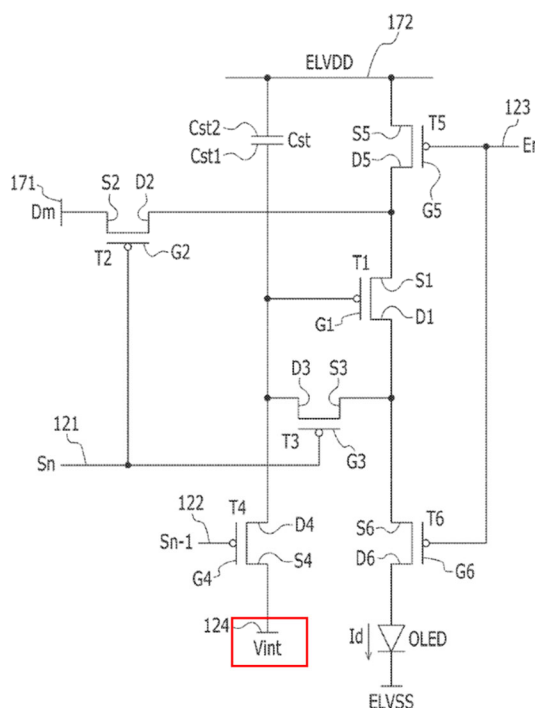
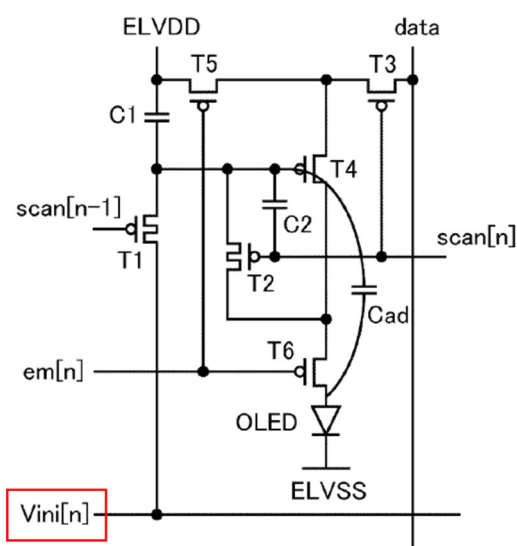
1 st Scan line	Sn	scan[n]
2 nd Scan line	Sn-1	scan[n-1]
Light emission control line	En	em[n]
Data line	Dm	data

d. 1[c]

Noguchi-I discloses the “second voltage line” as initialization voltage line “Vini[n]” that may be formed in the first wiring layer. Noguchi-I, ¶68, FIG. 1; Kanicki, ¶¶279-280. Vini[n] corresponds to Vint in the ’990 Patent, described as “initialization voltage line 124.” ’990Pat., 6:25-37. Annotated Noguchi-I’s Figure 1 (left) alongside ’990 Patent Figure 1 (right) show Vini[n] and Vint. Kanicki, ¶280.

FIG. 1

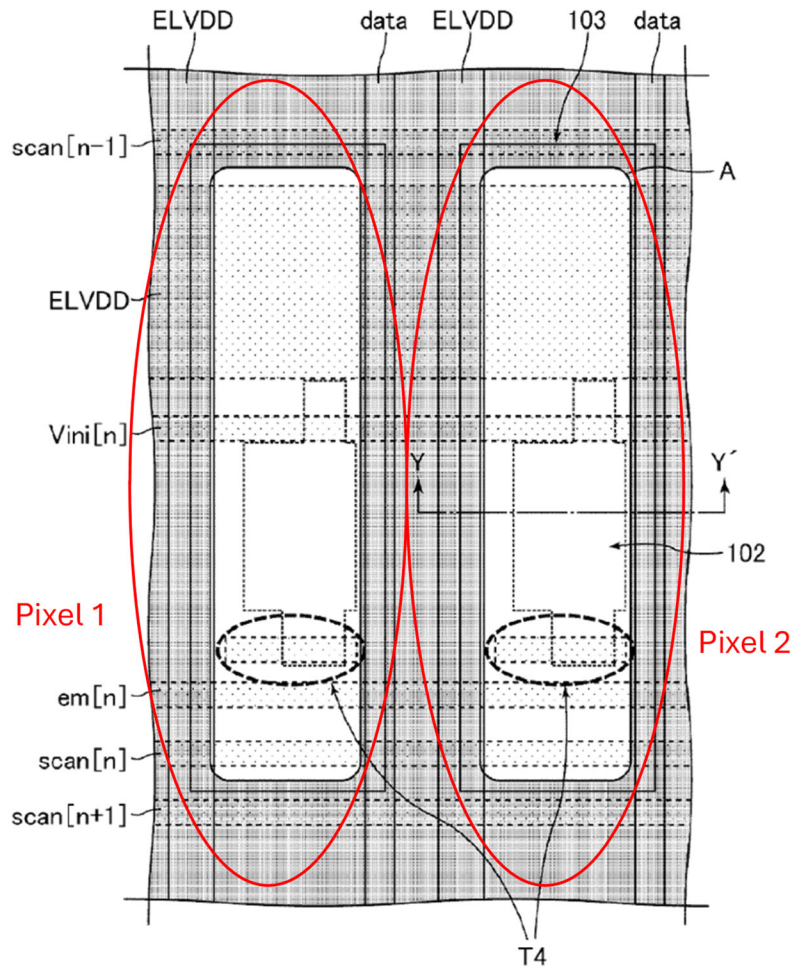
Fig. 1



e. 1[d]

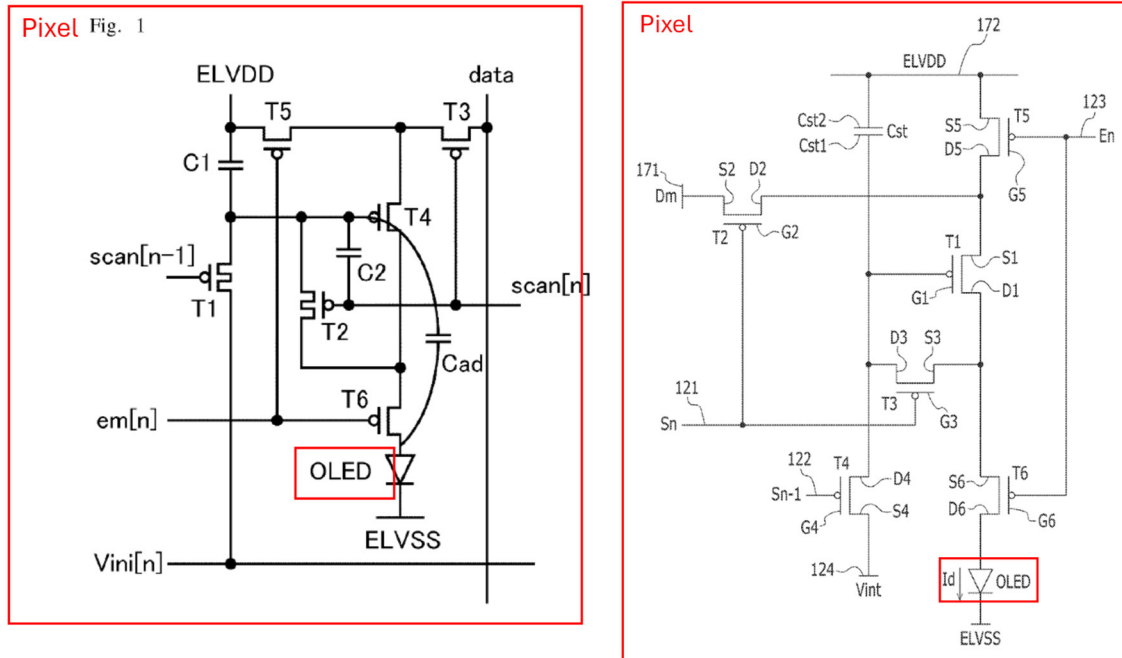
As explained in 1[pre], Noguchi-I discloses a display with a plurality of pixels. §IV.E.3.a. Each pixel includes TFTs, capacitor, and OLED. Noguchi-I, ¶¶11, 66-70, 74, 77, 79, 88, 91, FIG. 1; Kanicki, ¶¶282-283. Noguchi-I explains item 103 in the figures is an OLED pixel electrode. Noguchi-I, ¶¶15, 110. Figure 1 shows there is only one OLED per pixel (“each of the pixels comprising an organic light emitting diode”). *Id.*, FIG. 1; Kanicki, ¶283. Figures 2 (annotated below), 4, 5, 7, and 8 show at least two pixels in the display (“a plurality of pixels”). *Id.*

Fig. 2



Noguchi-I's annotated Figure 1 (left) alongside '990 Patent Figure 1 (right) show the OLED and associated driving circuit. Kanicki, ¶¶284-285.

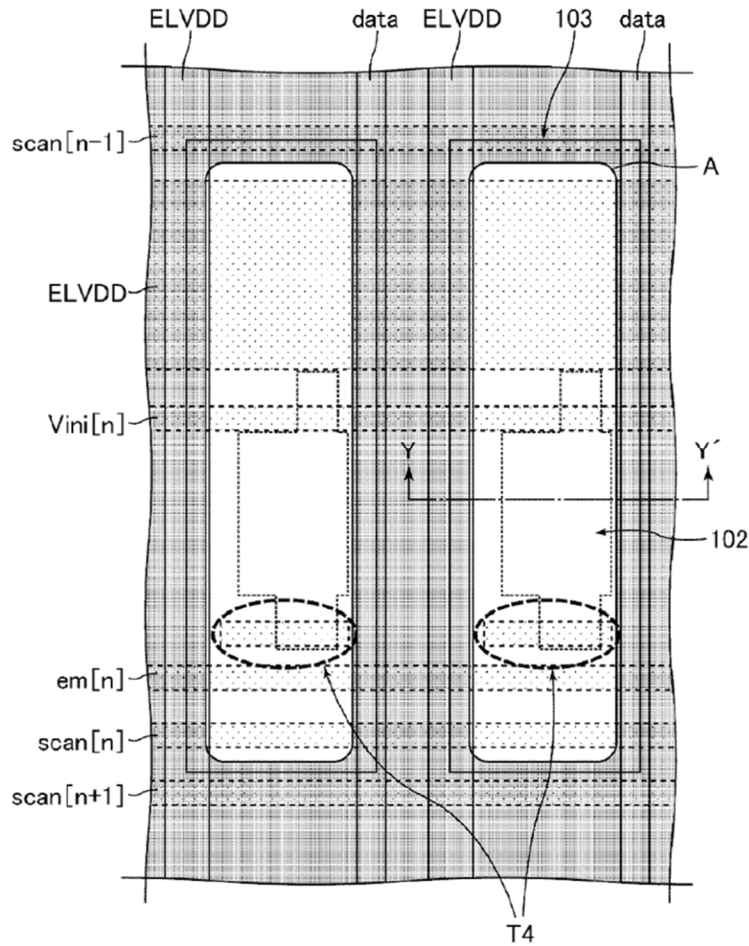
FIG. 1



f. 1[e]

As explained in 1[d], Noguchi-I teaches or suggests multiple pixels in a display. §IV.E.3.e. Noguchi-I further describes a “plurality of driving circuits” because it describes a driving circuit for each of the plurality of pixels, where each driving circuit comprises a plurality of TFTs to drive the OLED for that pixel. Noguchi-I, ¶¶1, 11, FIG. 1; Kanicki, ¶¶286-287. The TFTs are disposed in the pixel in a region denoted by “A.” Noguchi-I, ¶70, FIG. 2 (below); Kanicki, ¶287.

Fig. 2



Each driving circuit is connected to an OLED (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). *Id.*, ¶31, FIG. 1; Kanicki, ¶288. Petitioner has annotated Noguchi-I Figure 1 (left) alongside ’990 Patent Figure 1 (right) to show the relationship of a pixel and driving circuit. Kanicki, ¶288.

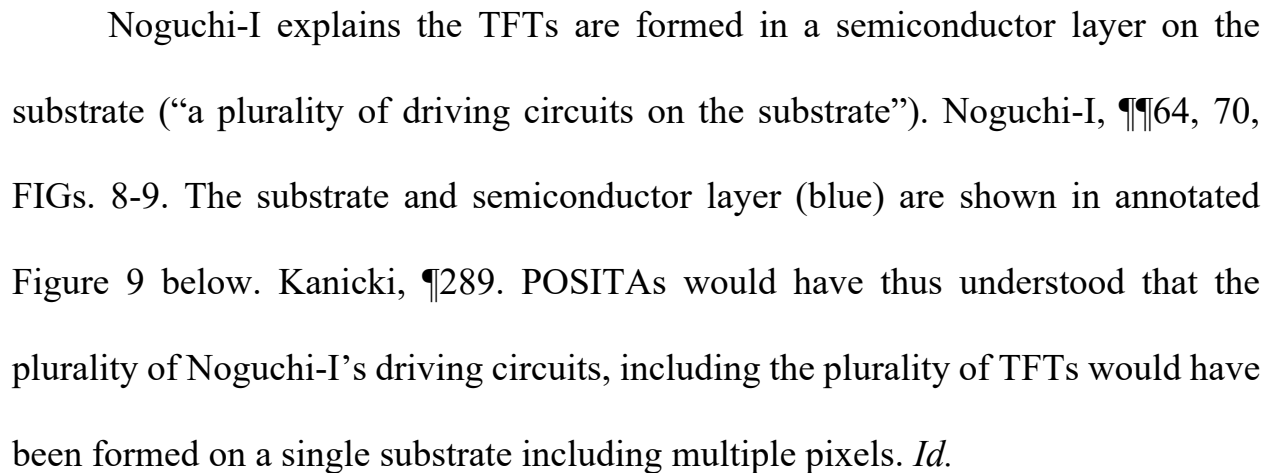
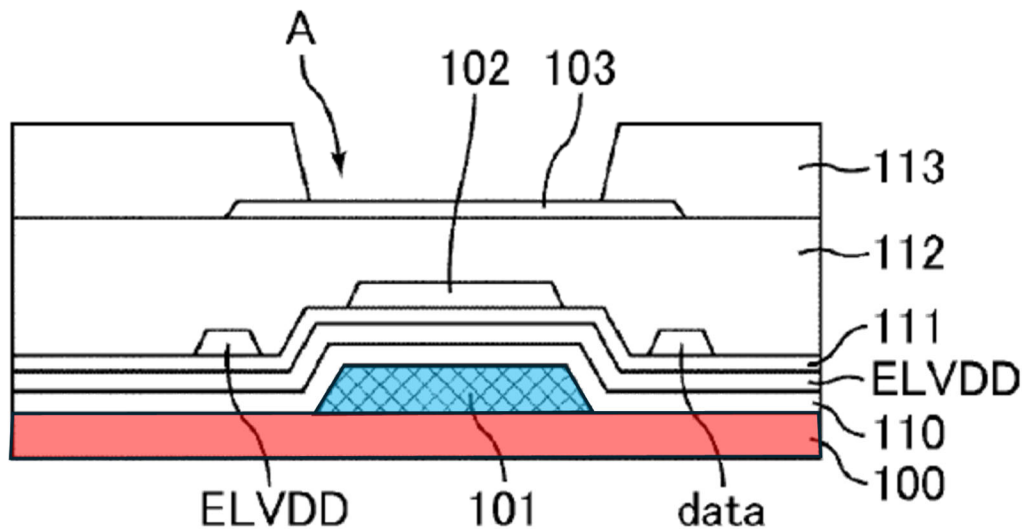


Fig. 9



Furthermore, annotated Figure 1 above shows the OLED is directly connected to T6 (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). Noguchi-I, FIG. 1.

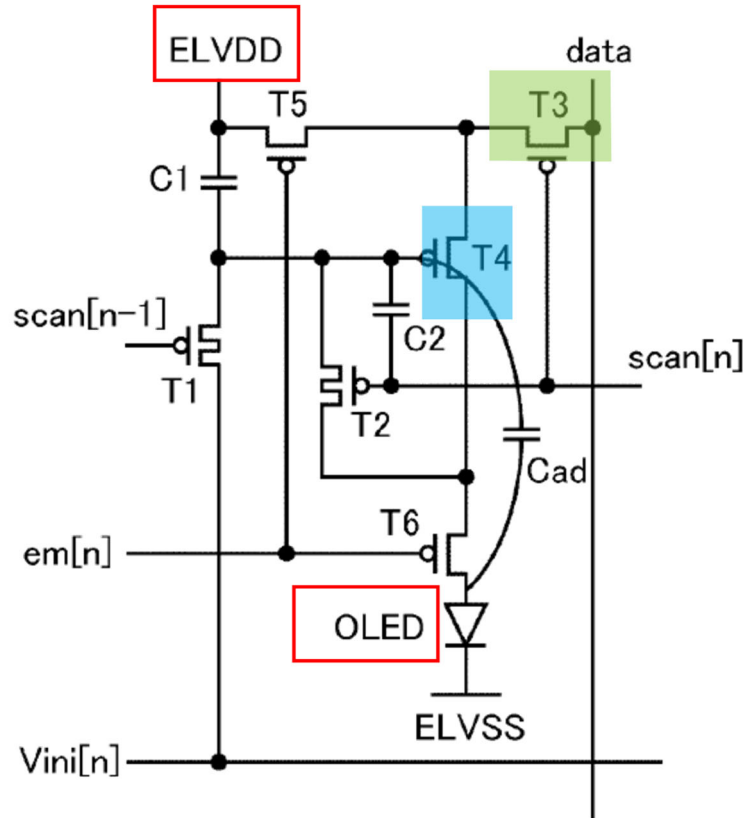
g. 1[f]

Noguchi-I discloses the “first thin film transistor” as T3 coupled to “the first scan line,” scan[n], and to “a data line,” data, shown in Noguchi-I’s Figure 1. As explained in 1[e], each pixel structure includes several TFTs arranged in a driving circuit. §IV.E.3.f. Referring to Annotated Figure 1 below, Noguchi-I explains that a “transistor T3 **responds to the scan signal inputted from the scanning line scan[n],** and performs switching of the **data signal inputted from the signal line data.**” *Id.*, ¶¶11, 44, FIG. 1; Kanicki, ¶¶291-294.

h. 1[g]

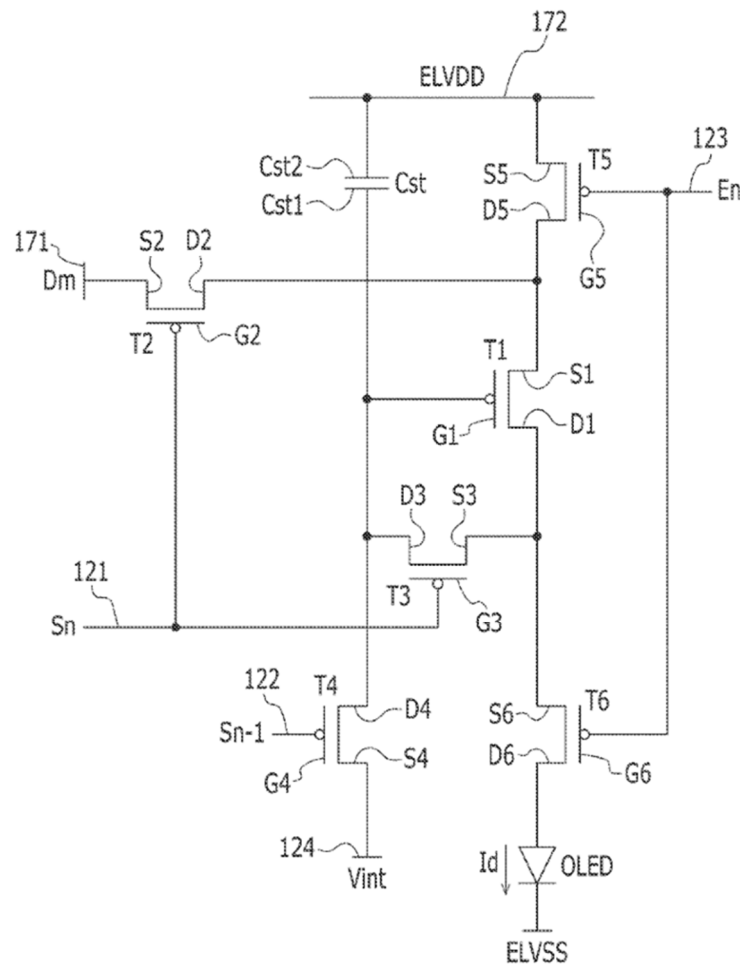
Noguchi-I discloses the “second thin film transistor” as T4 electrically coupled to “the first voltage line,” ELVDD, through T5. Noguchi-I, FIG. 1 (annotated); Kanicki, ¶¶295-296. Noguchi-I’s T4 is electrically coupled to the “corresponding organic light emitting diode,” OLED, through T6, and is electrically coupled to the “first thin film transistor,” T3, through a direct connection. *See* Noguchi-I, ¶11, FIG. 1.

Fig. 1



As explained in Ground 1A, the above characterization of Noguchi-I's T4 being "electrically coupled" to the OLED and ELVDD through intervening TFTs is consistent with the '990 Patent's Figure 1 connectivity and its detailed description. *See* '990Pat., 6:38-45, FIG. 1; Kanicki, ¶297.

FIG. 1

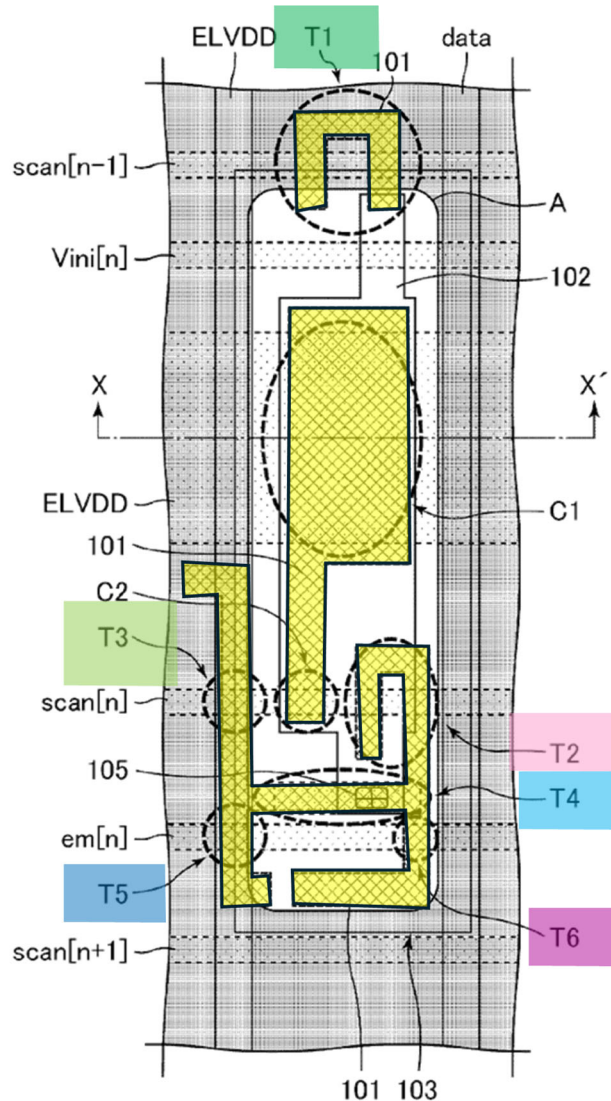


'990Pat., FIG. 1.

Noguchi-I additionally discloses T4 is included in a portion of the semiconductor layer (“utilizes a semiconductor layer”). The layout of Figure 8 provides the only semiconductor layout illustration in Noguchi-I and is an example of how the TFTs can be positioned within the pixel. Kanicki, ¶298. Petitioner has annotated Figure 8 to show the locations of various TFTs over the depicted

semiconductor pattern (yellow) in this example. *Id.*; Noguchi-I, FIG. 8 (annotated below); *see also* FIGs. 2, 4-5, 7 (showing T4 in the same location).

Fig. 8



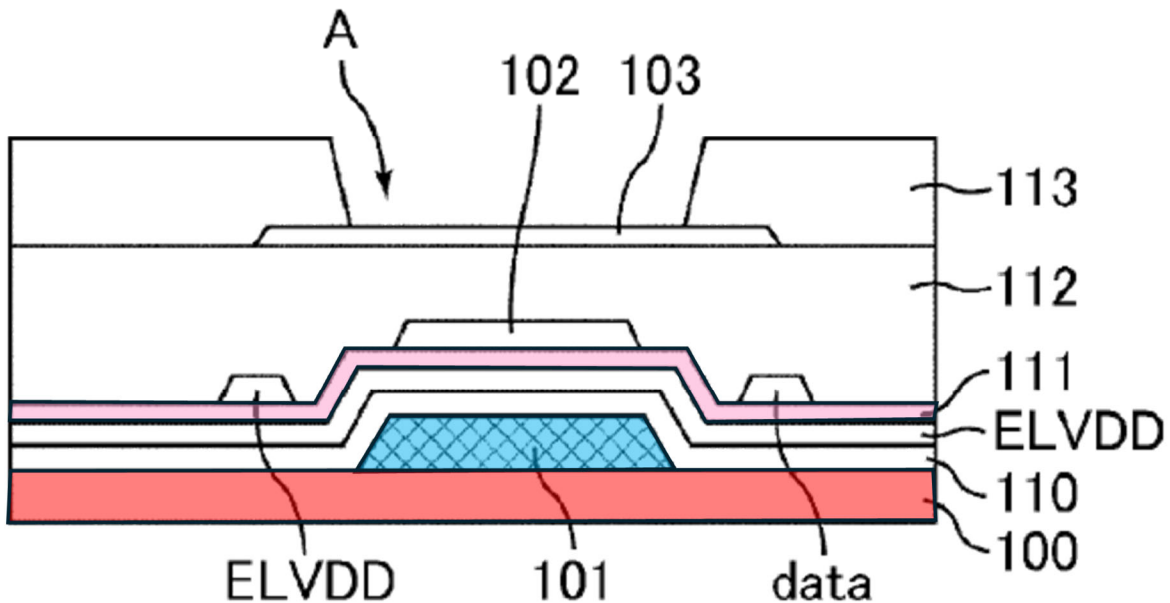
POSITAs would have understood from Noguchi-I's description of Figure 8 that T4 includes a section of the semiconductor pattern, the semiconductor pattern is laid out in the same layer and extends to the adjacent T3. Noguchi-I ¶11, FIG. 8; Kanicki, ¶299. POSITAs would have further understood that T3 is electrically

coupled to the semiconductor layer because it includes a section of the semiconductor pattern, which allows T3 to operate as a transistor. Kanicki, ¶299.

i. 1[h]

Noguchi-I discloses “an interlayer dielectric 110, an interlayer dielectric 111 and an interlayer dielectric 112 are stacked, in this order, from the side of the substrate 100.” Noguchi-I, ¶71. Annotated Figure 9 (below) shows interlayer dielectric 111 covers Noguchi-I’s semiconductor layer 101. Kanicki, ¶¶300-301. Furthermore, POSITAs would have understood that because Noguchi-I’s successive dielectric layers are stacked, interlayer dielectric 111 covers all structures below it, just as layers 110 and 112 also cover all structures below them. *Id.*, ¶301. Noguchi-I further explains that the first wiring layer, which is the gate of T4, is “disposed between the interlayer dielectric 110 and the interlayer dielectric 111.” Noguchi-I, ¶71, Thus, POSITAs would have understood that interlayer dielectric 111 specifically covers T4 (“second” TFT). Kanicki, ¶301.

Fig. 9



j. 1[ia]

Noguchi-I discloses the “storage capacitor” as capacitor C1 on one side the gate electrode of T4 (“a gate of the second transistor”), including a gate electrode 102 (“first capacitor plate”), and shield electrode 104 (“second capacitor plate”) in the second wiring layer. *See* Noguchi-I, ¶¶83-84, 86, 91-93, FIGs. 5, 7; Kanicki, ¶302-303.

Noguchi-I’s Capacitor C1 Structure

“[C]apacitor C1 [is] formed through overlap of the gate electrode and the power source line ELVDD” (Noguchi-I, ¶91) and shield electrode 104 is connected to ELVDD in the second wiring layer. *Id.*, ¶86. Furthermore, Noguchi-I explains

“[t]he gate electrode of T4 forms capacitance with the second wiring layer.” *Id.*, ¶95. Thus, POSITAs would have understood that C1 is formed in-part between gate electrode 102 and shield electrode 104. Kanicki, ¶304.

Petitioner has provided side-by-side annotations of Figure 7 (below) to illustrate the capacitor configuration of Noguchi-I, formed in-part between gate electrode 102 (green) (gate electrode of T4 (Noguchi-I, ¶¶15, 70, 81, 95)) and shield electrode 104 (orange). Kanicki, ¶305.

Fig. 7

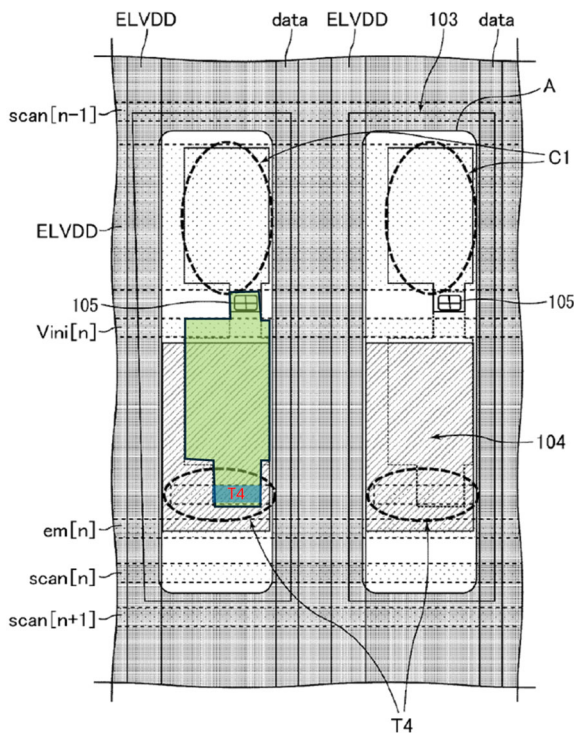
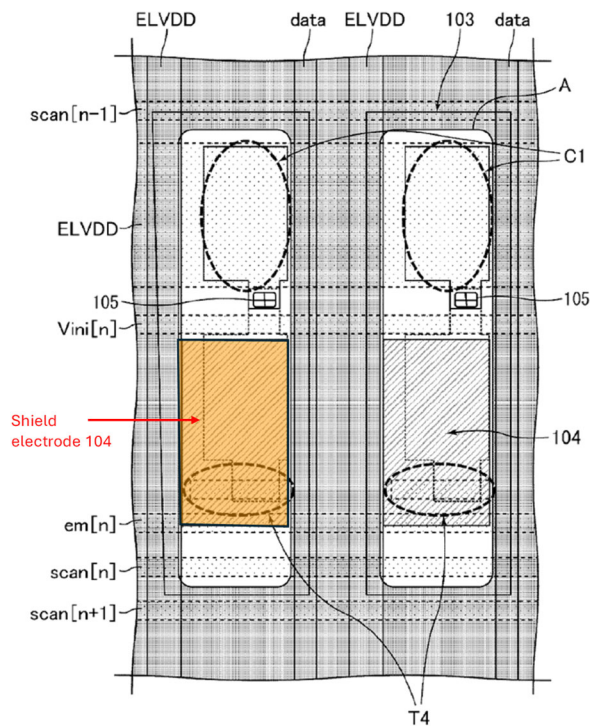


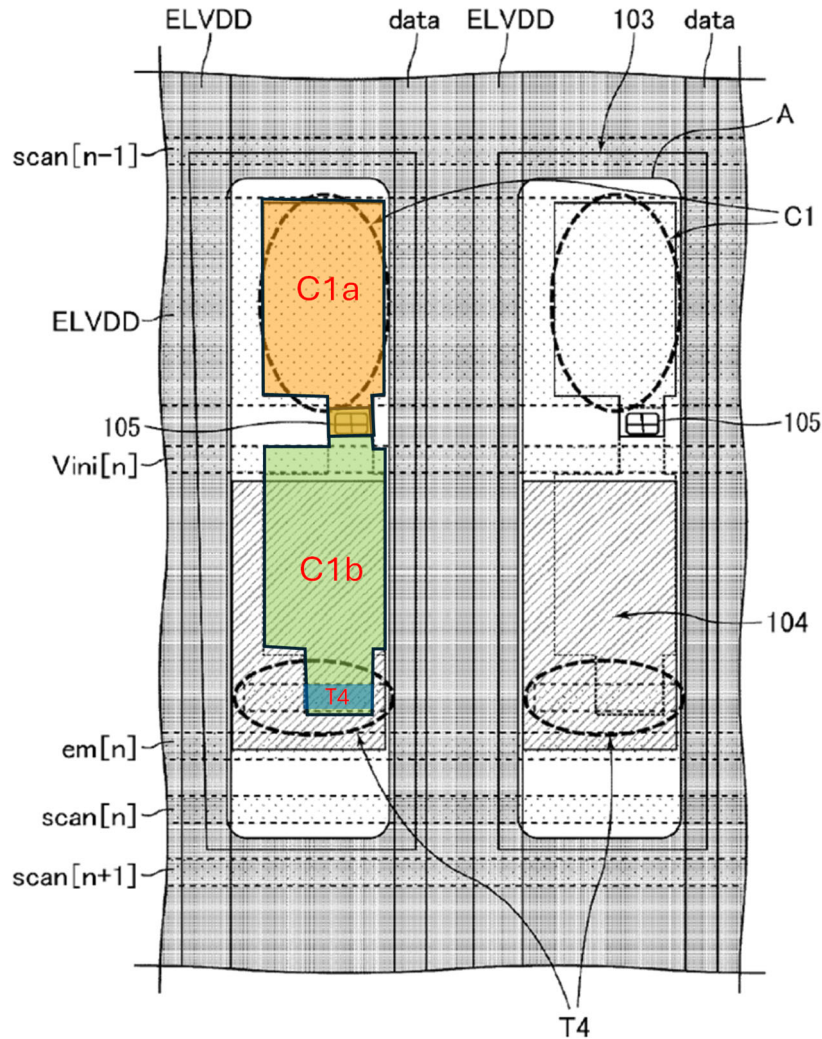
Fig. 7



While annotated Figure 7 above only shows one part of capacitor C1 (C1b), Noguchi-I’s capacitor C1 is made up of two parts, C1a and C1b, connected together through contact hole 105, as annotated below. Kanicki, ¶¶306-307; Noguchi-I, ¶¶75,

77, 89, 91. Capacitor C1 has a capacitance equal to the series addition C1a and C1b.
Kanicki, ¶306. Petitioner has pointed to C1b as meeting the claim limitation of the
storage capacitor comprising a first and second capacitor plate.

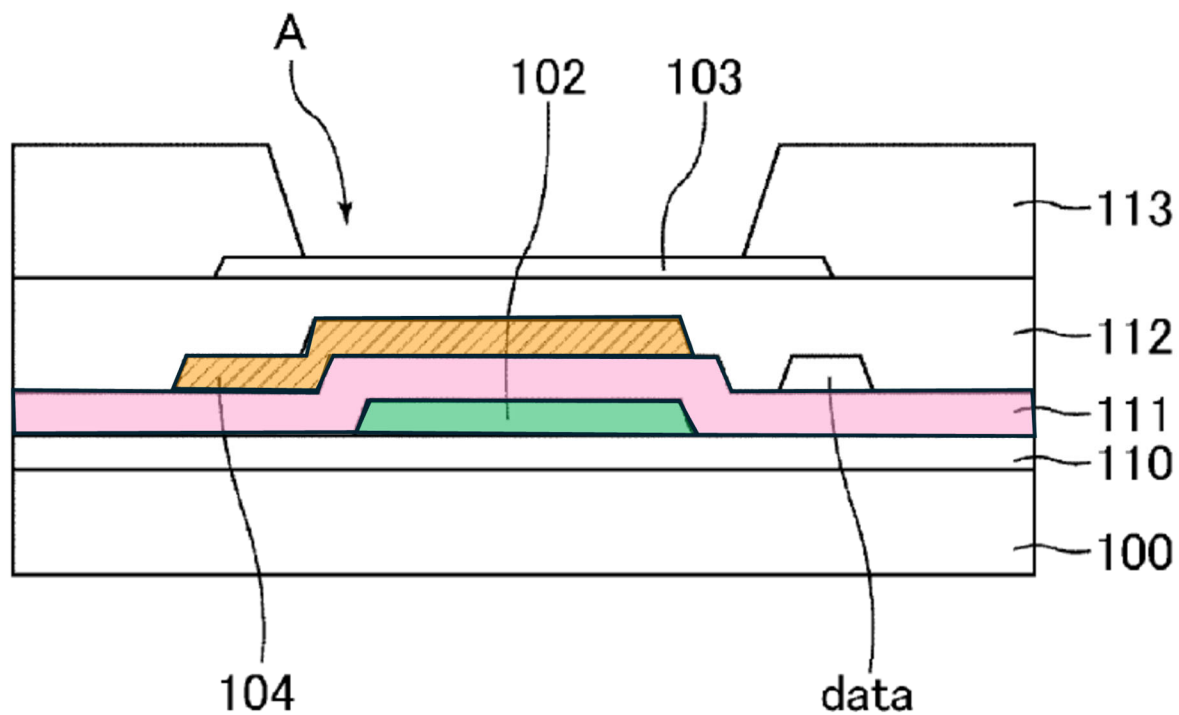
Fig. 7



Capacitor C1 comprises C1a and C1b, where C1b comprises a **gate electrode 102** in the first wiring layer and a **shield electrode 104** in the second wiring layer.
Noguchi-I, ¶¶91-95. **Interlayer dielectric 111** is disposed between 102 and 104 (“a

portion of the insulating layer between the first capacitor plate and the second capacitor plate”). *Id.*, FIG. 6 (annotated); Kanicki, ¶308. Thus, gate electrode 102 is part of the capacitor (“first capacitor plate comprising a portion of the gate electrode of the second thin film transistor”). *Id.*

Fig. 6

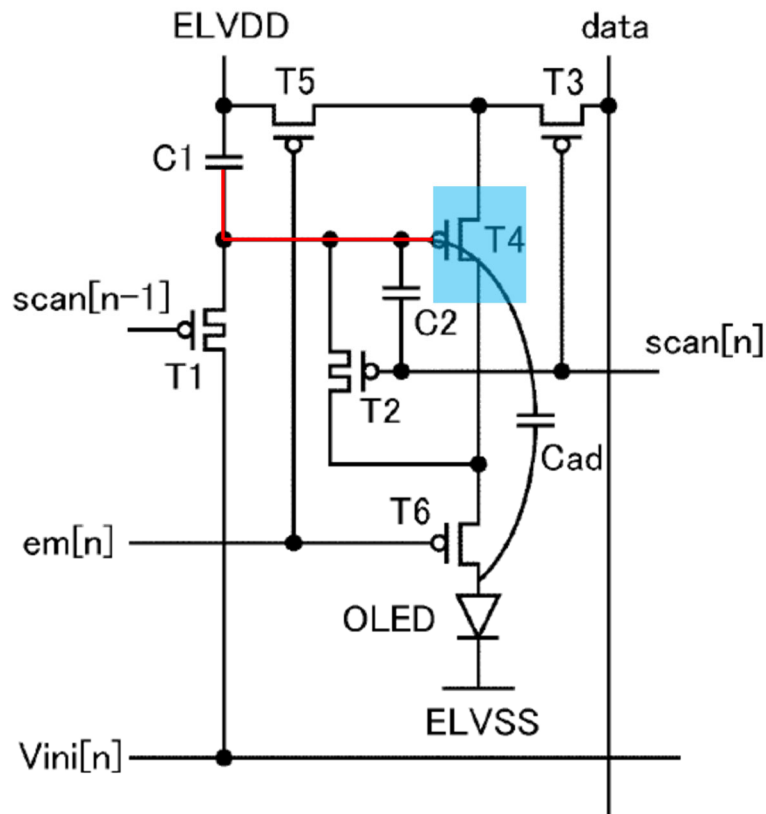


Noguchi-I, FIG. 6 (annotated).

C1 Connections

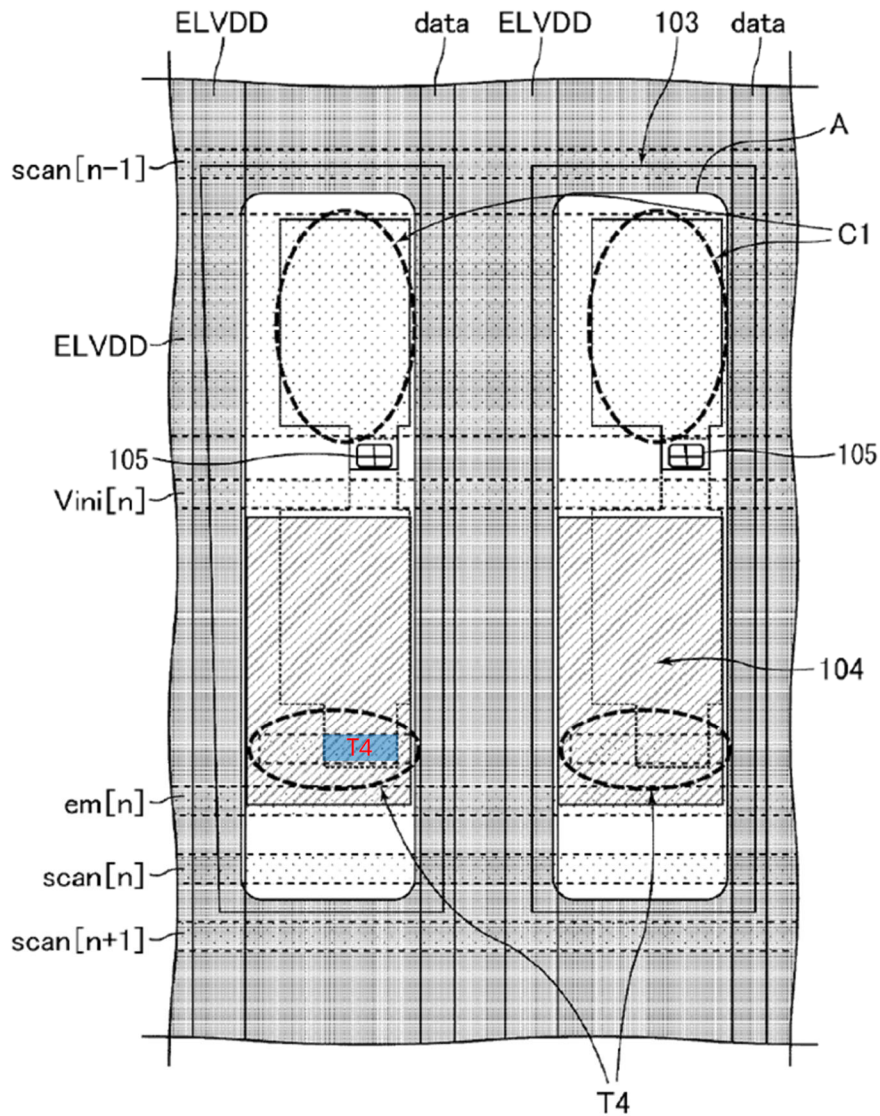
Noguchi-I discloses capacitor C1 is connected to the gate of T4 (“electrically coupled to a gate electrode of the second thin film transistor”), as shown below by the red line in annotated Figure 1. Noguchi-I, FIG. 1; Kanicki, ¶309.

Fig. 1



Noguchi-I indicates the position of T4 by a dashed box in Figure 7. POSITAs would have understood the channel region of T4 is at least the portion shown in blue in annotated Figure 7 below because it corresponds to the semiconductor layer directly under the gate electrode (“a portion of a channel region of the semiconductor layer under the gate electrode of the second thin film transistor”). Noguchi-I, FIG. 7; Kanicki, ¶310 (explaining the region indicated as T4 in Figure 7 corresponds to the same region for T4 in Figure 8, which shows the semiconductor layer).

Fig. 7



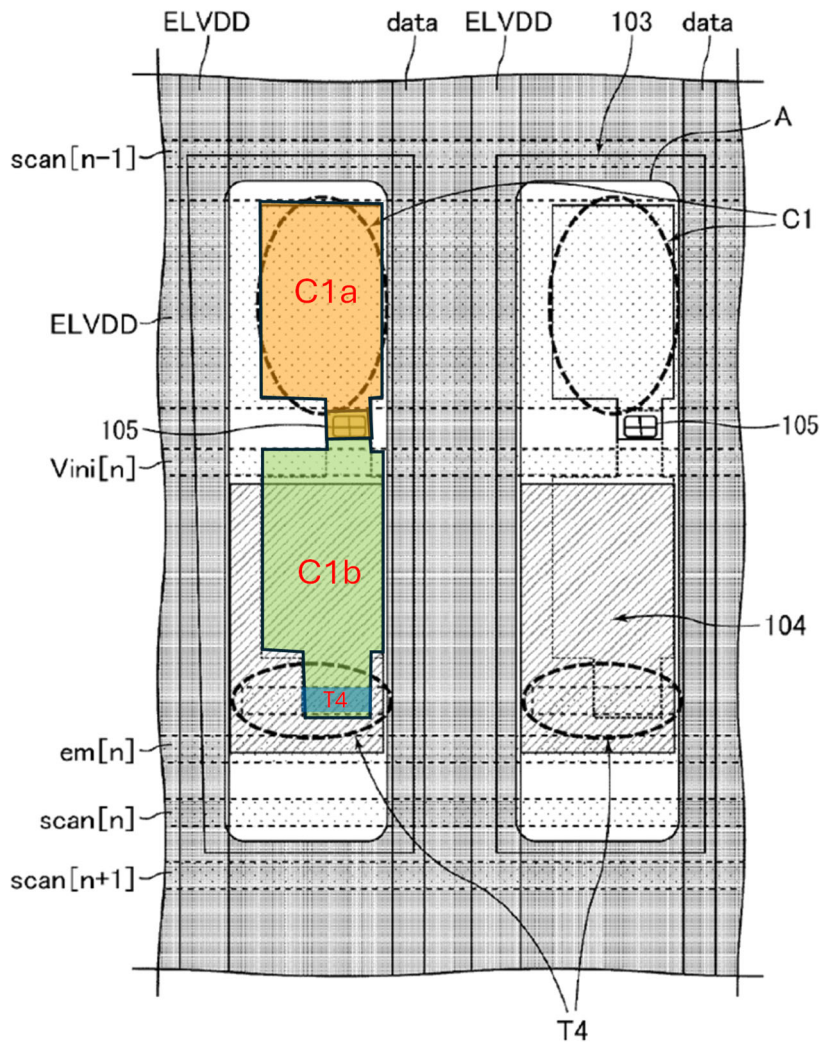
k. 1[ib]

As explained in Ground 1A for 1[ib], Udagawa teaches a “serpentine” (e.g., “curved”) channel of drive transistor T4. §IV.A.4.k. For the reasons explained in §IV.E.2, POSITAs would have been motivated to incorporate Udagawa’s driving TFT gate shapes (thereby increasing the channel length) in Noguchi-I’s OLED

driving circuit to reduce dispersion. Kanicki, ¶¶311-312. Furthermore, modifying Noguchi-I to use Udagawa's longer gate channel aligns with Noguchi-I's objectives of reducing the influence of parasitic capacitance, C_{ad} ; notably, forming the gate channel in this way allows for a reduction of dispersion without significantly increasing C_{ad} because Noguchi-I's shield electrode effectively reduces the parasitic capacitance, while maintaining a compact footprint. Kanicki, ¶312. Thus, for the same reasons as explained in §IV.A.4.k, Noguchi-I in combination with Udagawa teaches or suggests "a channel region of the semiconductor layer...of the second thin film transistor being curved." *Id.*

Furthermore, as explained in 1[ia], capacitor C1 is comprised of C1a and C1b, as shown in annotated Figure 7 below. §IV.E.3.j.

Fig. 7



Because the channel of T4 is at least under gate electrode 102 (shown in blue) in Figure 7, POSITAs would have found it obvious that gate electrode of T4 (i.e., the green-annotated plate in the above figure) covers the channel region of T4, including its bent or curved region (“bent portion of the second portion of the semiconductor layer is under the first capacitor plate”) when modified by Udagawa. Kanicki, ¶¶314-316. As explained in §IV.A.4.k, Udagawa describes different

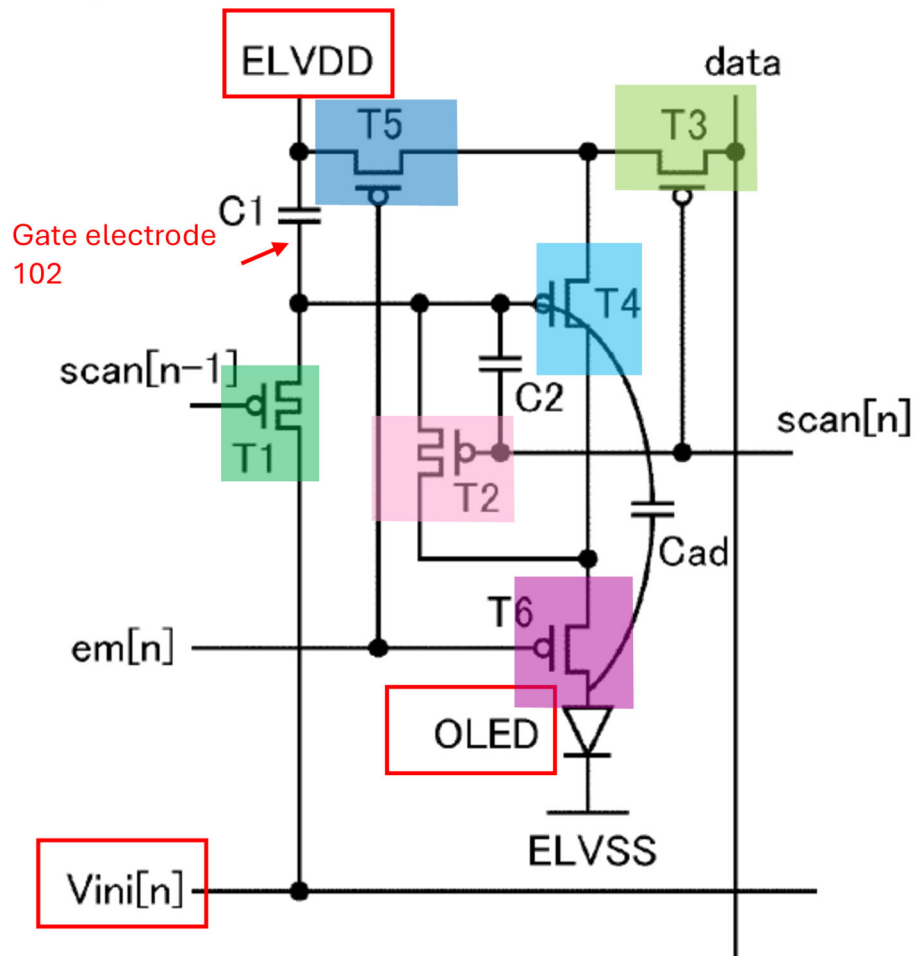
lengths and numbers of serpentine structures can implemented (Udagawa, ¶20), and a POSITA would have understood that gate electrode of T4 (green-annotated plate in the above figure or a part thereof) of Noguchi-I would overlap the extended channel in the combination.

I. 1[j]-1[m]

As explained in 1[pre] and 1[f], Noguchi-I discloses a TFT driving circuit with at least six transistors and one capacitor. §§IV.E.3.a, IV.E.3.g. As explained below, Noguchi-I discloses each of the recited transistors and connections. For reference, the table above in 1[b] shows the mapping for each transistor. §IV.E.3.c; Kanicki, ¶¶317-319.

As shown below in annotated Figure 1, Noguchi-I discloses each transistor. Kanicki, ¶318.

Fig. 1



Regarding 1[j], T2 (“third thin film transistor”) connects to T4 and gate electrode 102. Noguchi-I, FIG 1. T2 additionally connects to OLED through T6, just as T4 is. As explained for 1[g], POSITAs would have understood that the arrangement of T2, with connection to OLED through adjacent TFTs is the same configuration as disclosed in the ’990 Patent. *See* ’990Pat., 6:61-65; Kanicki, ¶320.

Regarding 1[k], T5 (“fourth thin film transistor”) connects to Vdd and T4. Noguchi-I, FIG 1; Kanicki, ¶321.

Regarding 1[l], T6 (“fifth thin film transistor”) connects to T4, T2, and OLED. Noguchi-I, FIG 1; Kanicki, ¶322.

Regarding 1[m], T1 (“sixth thin film transistor”) connects to Vini[n], T2, and gate electrode 102. Noguchi-I, FIG 1; Kanicki, ¶323

Accordingly, Noguchi-I discloses the electrical connections in 1[j]-1[m]. Kanicki, ¶324.

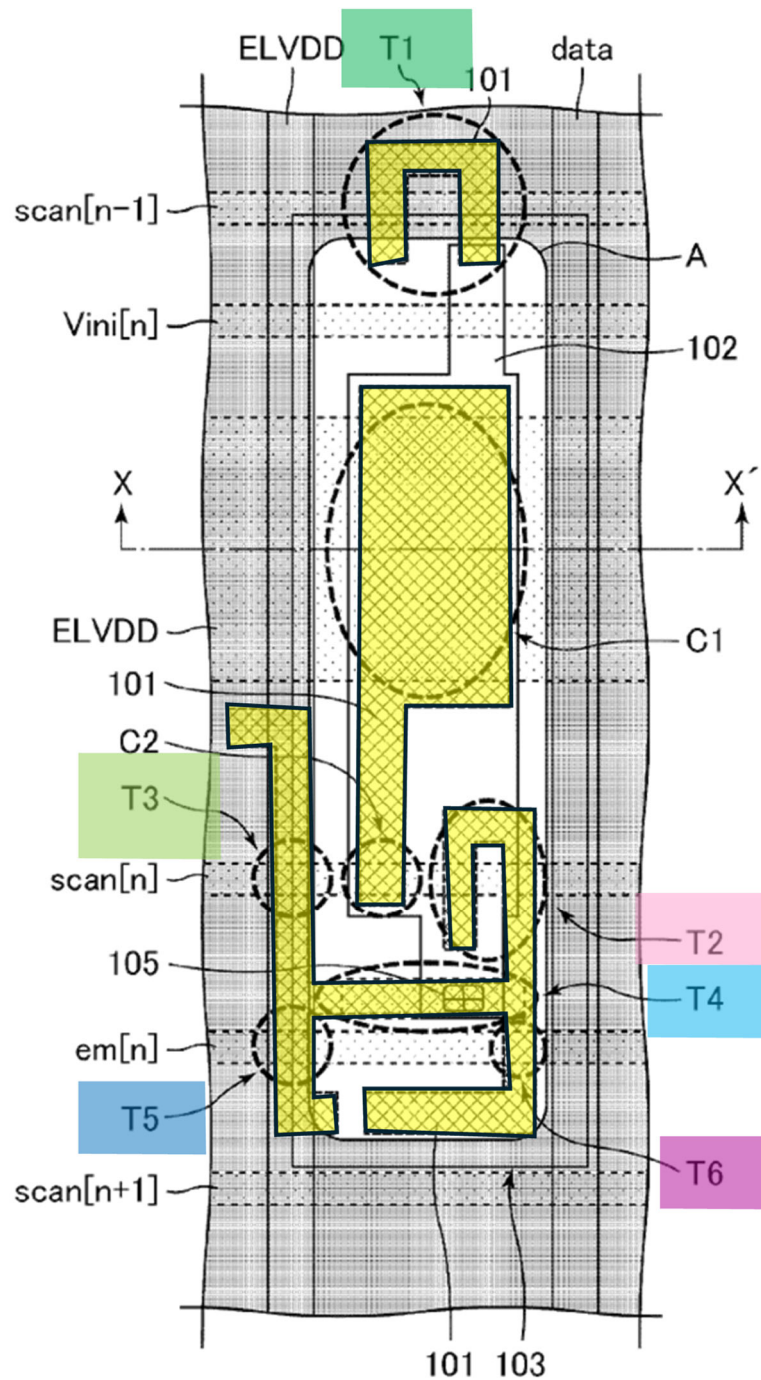
Transistor T1 to T6 each utilize and include a portion of the semiconductor layer, which is electrically coupled to the corresponding transistor. Noguchi-I, ¶¶11, 64, 70; Kanicki, ¶325. Although the semiconductor pattern that reaches transistor T1 in Noguchi-I is non-contiguous with the remaining sections of the semiconductor pattern, Noguchi-I explains all TFTs are disposed in a single layer. Noguchi-I, ¶70 (“A semiconductor layer of the Transistors T1 to T6”); Kanicki, ¶325. Further, as shown in annotated Figure 8,⁶ Noguchi-I’s semiconductor layer reaches all

⁶ Figure 8 provides an example layout for Noguchi-I’s pixel. To the extent that Figure 7 requires a modified layout, it would have been well within the knowledge and skill of POSITAs to move transistors. Kanicki, ¶325n.3.

transistors (“semiconductor layer being extended to and electrically coupled to”).

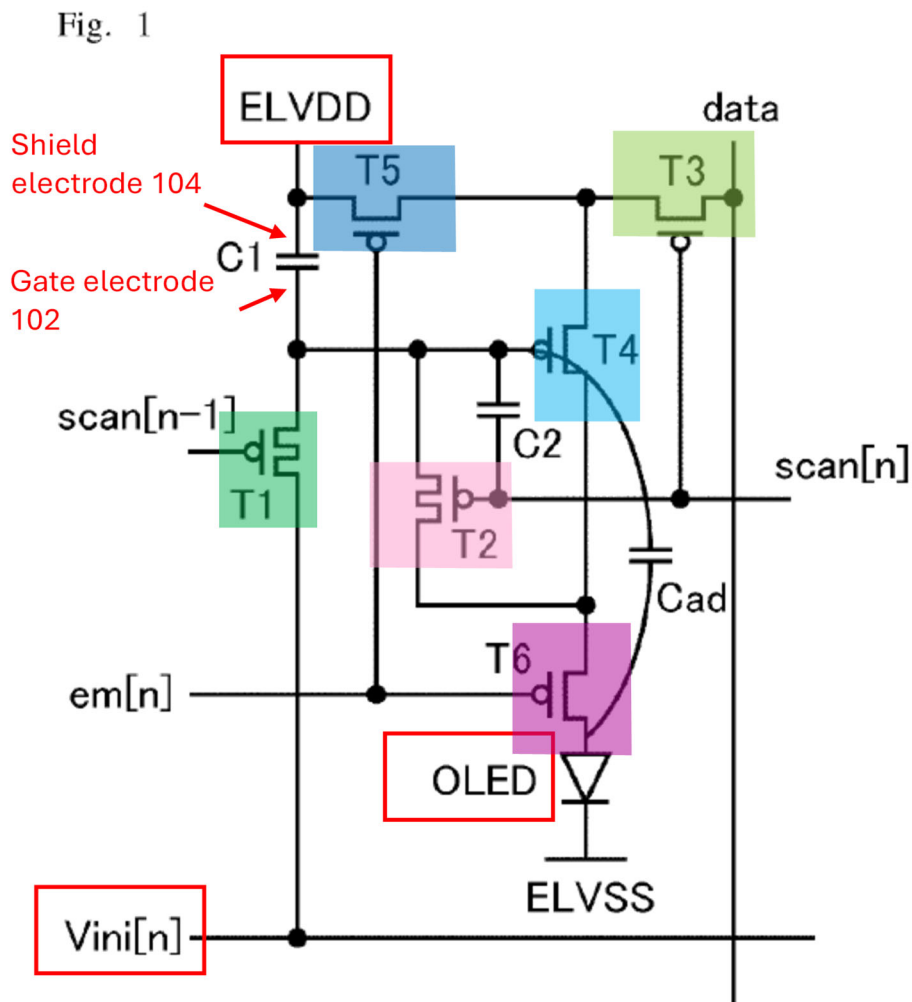
Noguchi-I, ¶64, FIG. 8; Kanicki, ¶¶318, 325.

Fig. 8



4. Claims 2-7, 23

As explained in 1[pre], 1[f], 1[g], and 1[j], Noguchi-I discloses a TFT driving circuit with at least six transistors and one capacitor. §§IV.E.3.a, IV.E.3.g, IV.E.3.h, IV.E.3.i. As explained below and shown in annotated Figure 1, Noguchi-I discloses each of the recited transistors and connections. Kanicki, ¶¶327-329.



Claim 2: Noguchi-I discloses the gates of T5 (“fourth” TFT) and T6 (“fifth” TFT) are connected together. Noguchi-I, FIGs. 1, 8; Kanicki, ¶330.

Claim 3: Noguchi-I discloses the gates of T5 and T6 receive the signal em[n]. Noguchi-I, ¶11, FIG. 1, 8. Noguchi-I explains that “em[n] denotes an n-th emission control line.” *Id.* POSITAs would have understood that EM was “a signal from a light emission control line” because when EM is applied to T5 and T6, the transistors turn on allowing drive transistor T4 to provide current to OLED, thus allowing the emission of light. Kanicki, ¶331.

Claim 4: T1 receives scan[n-1] at its gate. Noguchi-I, ¶11, FIGs. 1, 2; Kanicki, ¶332.

Claim 5: T3 and T2 are connected together. Noguchi-I, FIGs. 1, 8; Kanicki, ¶333.

Claim 6: Noguchi-I discloses the gates of T3 and T2 receive scan[n]. Noguchi-I, ¶11; Kanicki, ¶334.

Claim 7: Noguchi-I discloses shield 104 connected to ELVDD. Noguchi-I, ¶¶86, 91, FIGs. 1, 6, 7; Kanicki, ¶335.

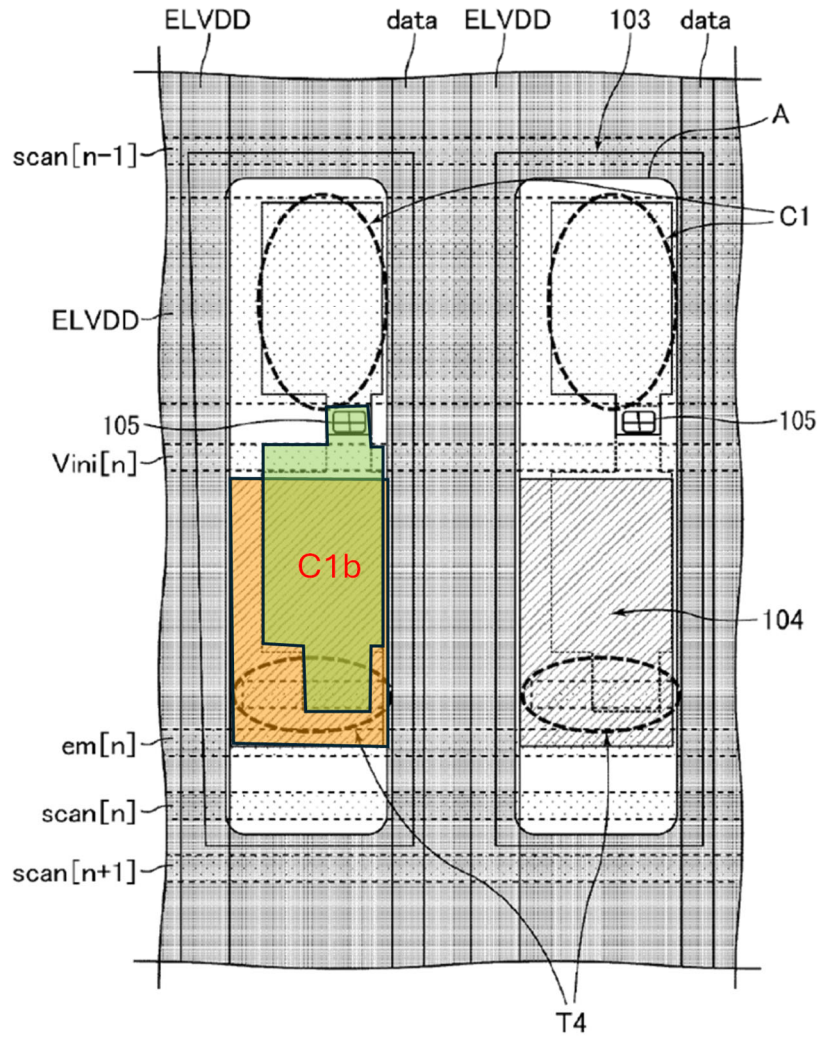
Claim 23: as shown in Figure 1, the drain of T4 is connected to the source of T2. Noguchi-I, ¶11, FIGs. 1, 8; Kanicki, ¶336. The gate of T4 is connected to the drain of T2. *Id.*

To the extent that PO argues that Noguchi-I does not explicitly show a drain “electrode” of the second TFT, as explained above in Ground 1A, POSITAs would have understood, consistent with the ’990 Patent’s description, the drain and source regions of the semiconductor are doped and themselves form drain and source “electrodes.” §IV.A.5; Kanicki, ¶337.

5. Claim 8

Noguchi-I teaches shield electrode 104 covers gate electrode 102 (see annotated Figures 6 and 7 below). Noguchi-I, ¶83 (“shield electrode 104 forms a region covering the gate electrode 102”), ¶92 (same), FIGs. 6, 7; Kanicki, ¶¶338-339. Shield electrode 104 (large orange box at bottom of annotated Figure 7) covers a periphery of gate electrode 102 (“completely surrounds a periphery of the first capacitor plate in a plan view”). As explained above in §IV.B.3 (Ground 1B), POSITAs would have understood that at least a portion around the outside of the first capacitor plate is surrounded. Kanicki, ¶339.

Fig. 7



6. Claims 9-10

Noguchi-I discloses its driving circuit uses p-channel TFTs. Noguchi-I, FIG. 1. It further explains that it uses a semiconductor layer with ion implantation (doping) to form its TFTs. *Id.*, ¶63; Kanicki, ¶¶341-342. Noguchi-I, however, does not expressly state what type of ion implantation it uses.

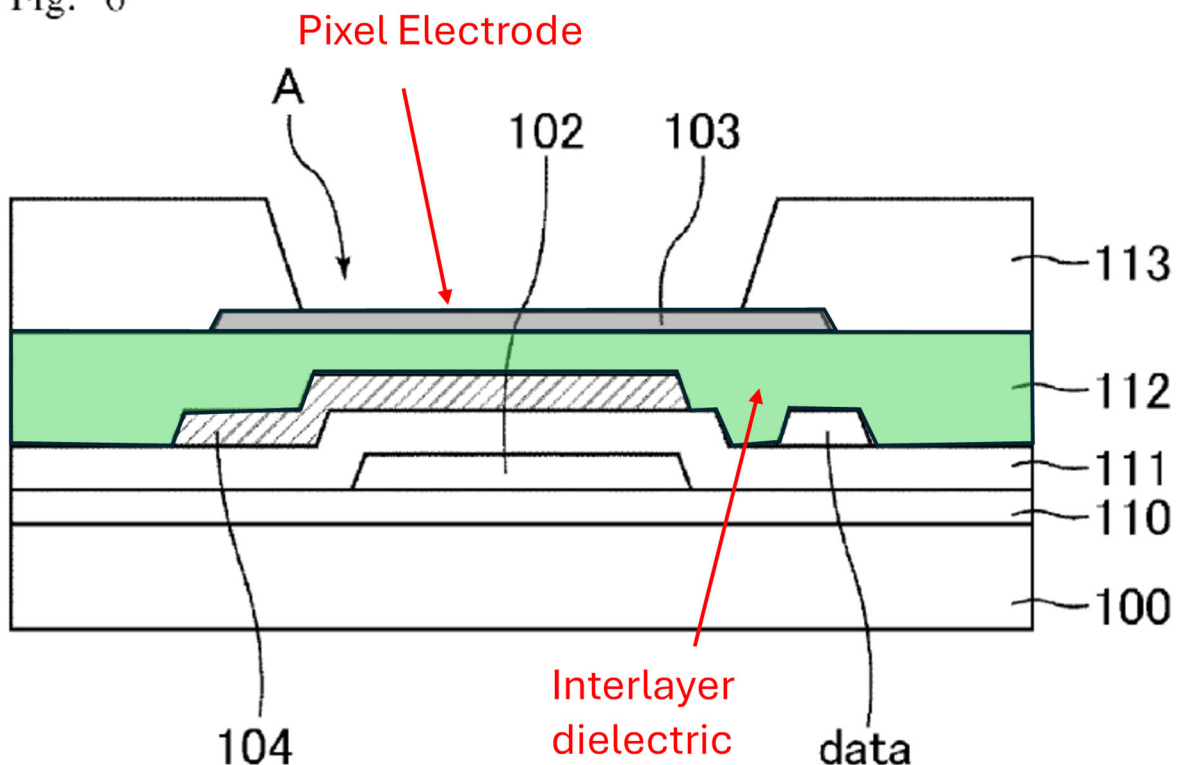
As explained in Ground 1A, Udagawa discloses that P- and N-type impurities are doped into p-channel TFT transistors formed in the semiconductor layer PO.

§§IV.A.6, IV.C.7. Accordingly, for the same reasons as explained above in Ground 1A, the Noguchi-I-Udagawa combination teaches or suggests n-type and/or p-type impurities doped into portions of the semiconductor layer. Kanicki, ¶343.

7. Claims 24-25

Annotated Figure 6 below shows **interlayer dielectric 112** (“protective layer”) disposed on interlayer dielectric 111 and interlayer dielectric 110 covering the TFTs and capacitor (“covering the plurality of driving circuits”) and under a pixel electrode. Noguchi-I, ¶¶71, 87, FIGs. 3, 6, 9. The pixel electrode is disposed on interlayer dielectric 112 (“each of the organic light emitting diodes further comprises a pixel electrode on the protective layer”). *Id.*; Kanicki, ¶345.

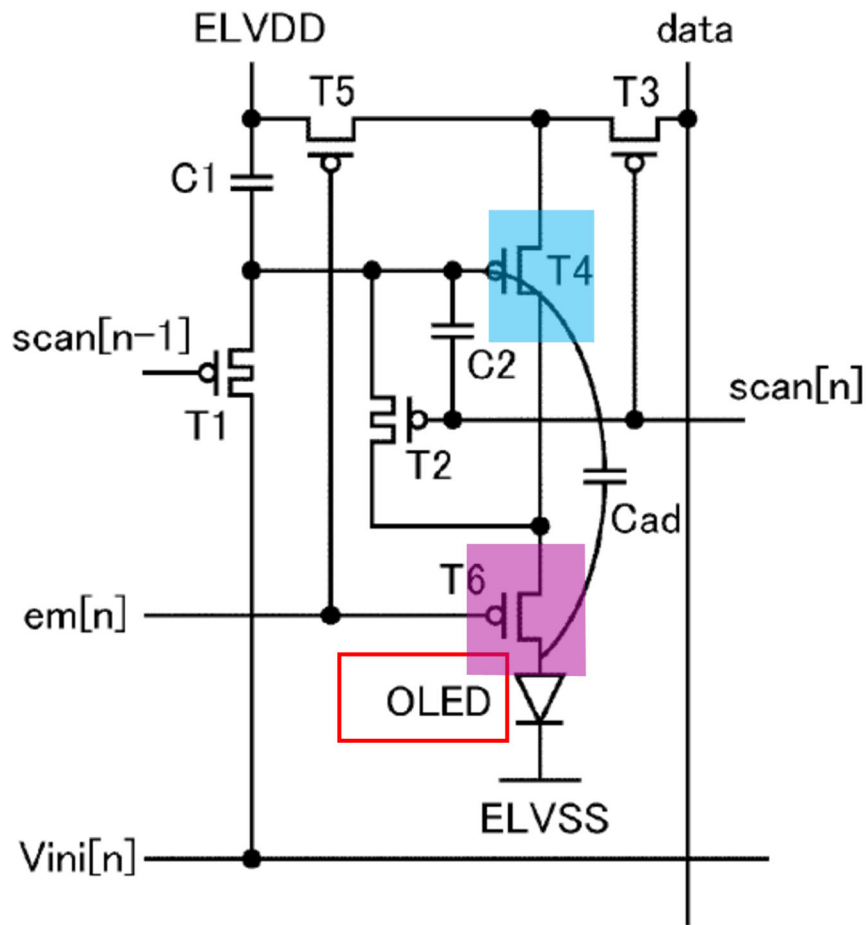
Fig. 6



Noguchi-I further explains the pixel electrode is connected to the drain of T6.

Id., ¶11, FIG. 1. As explained in 1[g], T4 is connected to OLED (and the pixel electrode) through T6 (“pixel electrode being electrically coupled to the second thin film transistor”). §IV.E.3.h; Kanicki, ¶346.

Fig. 1



Noguchi-I, FIG. 1 (annotated).

Claim 24 requires the pixel electrode to be “electrically coupled” to T4 “through a contact hole,” while claim 25 requires the pixel electrode to be “electrically coupled” to T6 “through a contact hole.” As shown annotated Figure 1 above, the pixel electrode is connected to T6, and T4 is connected to T6. Therefore, Noguchi-I teaches the pixel electrode electrically coupled to both T4 and T6. Additionally, POSITAs would have found it obvious that a typical way to connect T6 to the pixel electrode (anode of OLED (Noguchi-I, ¶41)) through a via (“contact hole”). Kanicki, ¶347. Vias are well-known in the art and commonly used to connect structures on different levels of a semiconductor structure as shown by Noguchi-I’s disclosure of contact hole 105. *Id.*

Accordingly, it would have been obvious to POSITAs to use a via to connect the drain of T6 to the pixel electrode, and to thereby “electrically couple[]” the pixel electrode to each of T4 and T6 through the contact hole. *Id.*

8. Claim 26

As explained in 1[ia], CS comprises gate electrode 102 that is the gate of T4. §IV.E.3.j. Noguchi-I explains that scan[n] is in the first wiring layer. Noguchi-I, ¶68, FIG. 2. The gate electrode 102 is also in the first wiring layer (“same material layer”). *Id.*, ¶75, FIG. 45. Noguchi-I explains that a “wiring layer is ordinarily low-resistance wiring (metal wiring)” (*id.*, ¶63), which would have suggested and made it obvious

that metal components, including the first capacitor plate and the first scan line, in the first wiring layer were made of the same material. Kanicki, ¶¶349-350.

9. Claims 27-30

As explained in Ground 1A, utilizing Udagawa's serpentine channel shape for drive transistor T4 allows many different apparent shapes. §IV.A.9. Noguchi-I-Udagawa teaches or suggests claims 27-30 for the same reasons as explained above. §IV.A.9; Kanicki, ¶¶351.

F. Ground 2B: claims 11-20 are Unpatentable over Noguchi-I, Udagawa, Noguchi-II, and Jeong

1. Noguchi-II

Noguchi-II (EX1012) describes a circuit of a pixel of an organic EL display device that is similar to the circuit in Figure 1 of the '990 Patent and Noguchi-I (i.e., with scan lines, data lines, and six transistors), but additionally includes a transistor T7 as an adjusting transistor for adjusting the voltage of a pixel electrode of an OLED. Noguchi-II, ¶¶77, 90-91.

T7 is connected in parallel to the OLED; consequently, OLED's anode and cathode voltages may be the same. Noguchi-II, ¶91, FIG. 6. This enables discharge of charge stored in the Cad through a power supply line ELVSS using the transistor T7 as a path for electric current. *Id.*, ¶91. Consequently, display characteristics

without any occurrences of the stepwise response characteristics can be achieved. *Id.*, ¶91.

Noguchi-II is in the same field of endeavor as the '990 Patent, and both are directed to compensating the threshold voltage of the driving transistor. Noguchi-II, ¶42. Furthermore, Noguchi-II, which shares the same inventor as Noguchi-I. Kanicki, ¶¶352-354

2. Jeong

Jeong (EX1009) describes a circuit of a pixel having an improved response time that is similar to the circuit in Figure 1 of the '990 Patent and Noguchi-I (i.e., with scan lines, data lines, and six transistors). Jeong, Abstract. Jeong's 6T1C circuit allows the initialization power supply for supplying the initialization voltage (VINT) of the pixel to be set to the same voltage source as a power supply that supplies a low potential pixel power from the outside (ELVSS). *Id.*, ¶¶40, 52.

Jeong is in the same field of endeavor as the '990 Patent. For example, both are directed to compensating the threshold voltage of the driving transistor. Jeong, ¶¶85-86, 89 Kanicki, ¶355-356.

3. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, and Jeong

Noguchi-I is directed to the pixel structure of an OLED display (6T1C circuit configuration), susceptible to visual aberrations caused by parasitic capacitance, Cad. Noguchi-I, ¶¶12, 15, 17, 70.

Noguchi-II proposes adding an additional adjusting transistor (a seventh transistor) to the 6T1C circuit to reduce visual aberration in the display. Noguchi-II, ¶¶77, 91.

POSITAs would have found it obvious and would have been motivated to combine the complementary teachings of Noguchi-I with Noguchi-II to reduce Cad, and specifically add Noguchi-II's seventh (adjusting) TFT to Noguchi-I's pixel driving circuit. This combination would have been obvious based on the shared objective of Noguchi-I's and Noguchi-II's to reduce Cad, and the additional improvement gained by implementing Noguchi-II's seventh TFT. Kanicki, ¶360.

Notably, POSITAs would have been motivated to apply a known technique (adding a seventh TFT) to a known device ready for improvement (Noguchi-I's pixel structure) to yield predictable results (the Cad being reduced). POSITAs would have had a reasonable expectation of success, because adding a seventh TFT to a 6T1C circuit to reduce parasitic capacitance was already described in Noguchi-II, and such modifications were well within the skill set of POSITAs. *Id.*, ¶361.

POSITAs would have also combined Noguchi-I with Jeong with the understanding that Vini[n] is the same voltage source as ELVSS. Jeong, ¶¶52, 54. Setting Vini[n] to ELVSS is merely a design choice. *Id.*, ¶52 (“initialization power supply supplying...may be supplied according to the design structure of the pixel”); Kanicki, ¶361.

Furthermore, Noguchi-I can be combined individually with each of Udagawa and Noguchi-II. In each instance, the combination involves modifying a distinct aspect of Noguchi-I. Kanicki, ¶362. POSITAs would have recognized there is no interference among the modifications, and each combination can be implemented without affecting the others. Accordingly, POSITAs would have found it obvious and would have been motivated to combine Noguchi-I with each of Udagawa and Noguchi-II and would have had a reasonable expectation of success. *Id.*, ¶362.

4. Claim 11

Noguchi-I’s driving circuit can have more than or less than six TFTs. Noguchi-I, ¶95. As explained above, Noguchi-II discloses an OLED drive circuit similar to those described in Noguchi-I and in Figure 10 of the ’990 Patent, which additionally includes a seventh TFT. **§Error! Reference source not found..** Noguchi-II’s Figure 6 (left) below and Figure 10 from the ’990 Patent (right) show the seventh TFT. Kanicki, ¶¶364-365.

Fig. 6

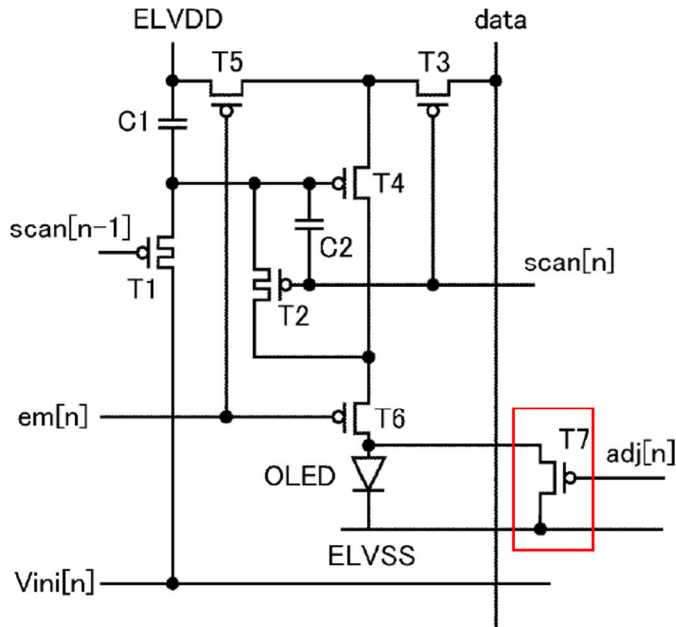
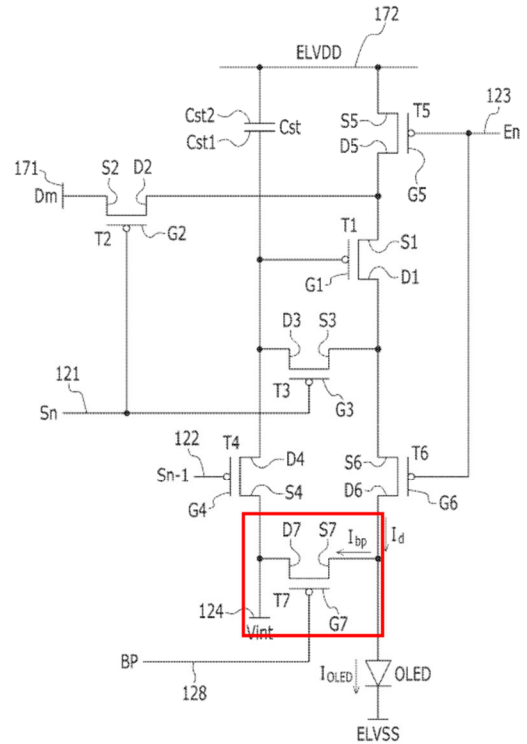


FIG. 10



As shown below, Noguchi-II's circuit (left) is nearly identical to Noguchi-I (right), except for the additional seventh TFT (T7). Kanicki, ¶366.

Fig. 6

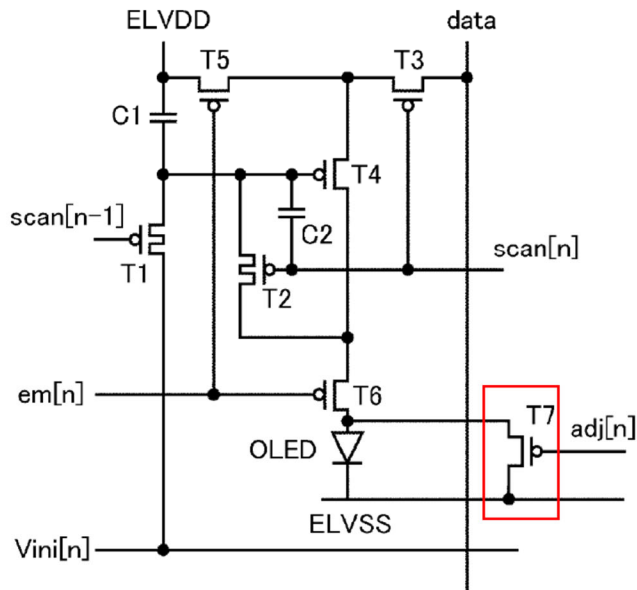
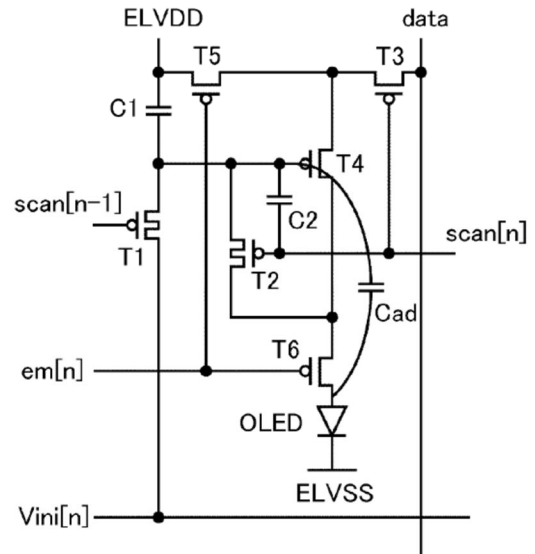


Fig. 1

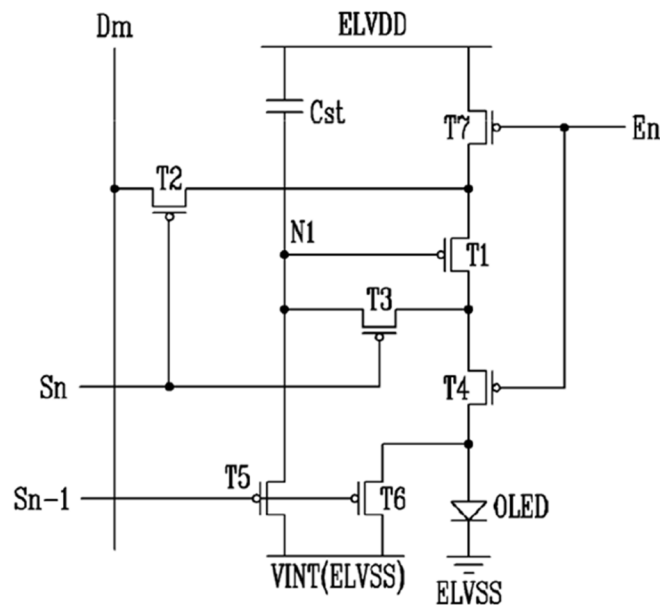


T7 in Figure 6 connects (“electrically coupled”) to OLED and T6. Noguchi-II, ¶¶77, 90-91. The addition of T7 prevents “occurrence of the stepwise response characteristics” that occurs because of parasitic capacitance, *Cad*. *Id.*, ¶¶16, 91; Kanicki, ¶367.

POSITAs would have been motivated to modify Noguchi-I to incorporate Noguchi-II’s seventh TFT to further reduce the effects of parasitic capacitance, *Cad*. Kanicki, ¶368. Such a modification would have improved the performance of Noguchi-I drive circuit with minimal increase in size. *Id.* Furthermore, as shown above, Noguchi-II and Noguchi-I’s circuits are identical except for the additional TFT. *Id.*

While Noguchi-II shows the drain of T7 is connected to ELVSS (and the drain of T1 is connected to Vini[n]), it was well-known and obvious at the time of the '990 Patent that the initialization voltage Vini[n] and ELVSS can be the same. This is specifically shown in Jeong. Jeong, ¶¶52 (“the third power supply supplying the third power (VINT)... may be set to the same Voltage source as the second power supply supplying the second power (ELVSS).”), 54, FIG. 2 (below); Kanicki, ¶369. POSITAs would have thus understood that Vini[n] and ELVSS are the same voltage line. Kanicki, ¶369. Thus, POSITAs would have found it obvious that in the combination T7 is connected to Vini[n]/ELVSS (“second voltage line”). *Id.*

FIG. 2



POSITAs would have been motivated to combine the teachings of Noguchi-I and Noguchi-II. §IV.F.2. Combining such teachings to incorporate an additional TFT would have been straightforward, within the skill set of POSITAs, and an obvious addition to improve the functionality of the drive circuit. Kanicki, ¶370. Noguchi-I and Noguchi-II share the same inventor and describe the same pixel circuit. *Compare* Noguchi-I, FIGS. 1, 8-9, *with* Noguchi-II, FIGS. 7-9; *see also* *ZUP, LLC v. Nash Mfg, Inc.*, 896 F.3d 1365, 1371-73 (Fed. Cir. 2018). Both Noguchi's are also concerned with reducing parasitic capacitance, *Cad.* Noguchi-I, ¶15; Noguchi-II, ¶54. Thus, POSITAs would have looked to other references, such as Noguchi-II, to reduce the effects of *Cad.* Kanicki, ¶370.

5. Claim 12

As explained in 1[g] and 1[j], T1 to T6 utilize and include a portion of the semiconductor layer, which is thus electrically coupled to the corresponding transistor. Kanicki, ¶373; §§IV.E.3.h, IV.E.3.i. POSITAs would have found it obvious that when adding an additional TFT that utilized the semiconductor layer, the semiconductor layer would be deposited for that new TFT to extend to the area where T7 would be located, consistent with the design disclosed in Noguchi-I. Kanicki, ¶373. POSITAs would have understood and found it obvious to continue the semiconductor layer to incorporate T7 as part of routine and obvious design choice. *Id.* Furthermore, the '990 Patent attaches no significance to having a

contiguous or non-contiguous semiconductor layer as discussed in §IV.E.4. Accordingly, the combination teaches or suggests a seventh TFT with the semiconductor layer extended to incorporate that TFT. *Id.*, ¶374.

6. Claim 13

Noguchi-II discloses the seventh TFT has a gate signal of adj[n] (“bypass control line”). Noguchi-II explains turning the seventh TFT on would have bypassed and accumulated charge on the OLED. Noguchi-II, ¶91. Accordingly, POSITAs would have understood adj[[n] to be a “bypass” control signal for the voltage on the OLED. Kanicki, ¶¶375-377.

7. Claims 14-19

As explained Ground 2A in §IV.E.4, Noguchi-I discloses these claims. The addition on the seventh TFT does not alter Noguchi-I’s disclosure. Kanicki, ¶¶378-380. Accordingly, for the same reasons as explained above in Ground 2A, the combination teaches these claims. *Id.*

8. Claims 21-22

As explained in Grounds 1A and 1C, Udagawa discloses P- and N-type impurities are doped into p-channel TFT transistors formed in the semiconductor layer PO. §§IV.A.6, IV.C.7. The addition of Noguchi-II’s seventh TFT does not alter the general structure of the semiconductor layer other than adding an additional p-channel TFT, just explained in Ground 1A for Chung. Kanicki, ¶381. Accordingly,

for the same reasons as explained above, the Noguchi-I-Udagawa-Jeong-Noguchi-II combination teaches claims 21 and 22. *Id.*

G. Ground 2C: Claims 1-30 are Unpatentable over the Combination of Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim

1. Kim

Kim (EX1013) teaches contact errors in the dual-structure capacitor can be prevented by the active pattern (1) functioning as the first electrode of the first capacitor and being extended to be connected to the semiconductor layer included in the transistor connected between a power source VDD that supplies a power supply voltage and a power source Vinit that supplies an initial voltage, and (2) functioning as the first electrode of the second capacitor and being extended to be connected to the semiconductor layer included in the transistor that transmits the data voltage to the driving transistor in response to the selection signal from the current scan line. *Id.*, 5:41-6:16. Kim is analogous art to the '990 Patent because both patents are in the same field of endeavor. Both are directed to compensating for threshold voltage deviation. Kim, 1:61-63; Kanicki, ¶¶382-383.

2. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim

Kim, similar to Noguchi-I, is related to OLED displays. Kim, 5:41-6:16. In particular, Noguchi-I and Kim both described similar OLED drive circuits that included six TFTs and two capacitors (6T2C circuits) (Noguchi-I, FIG. 1; Kim, FIG.

5), and both described forming TFTs on a substrate within an OLED pixel in strikingly similar configurations. Noguchi-I, FIG. 8; Kim, FIG. 2 (reproduced below).

Fig. 8

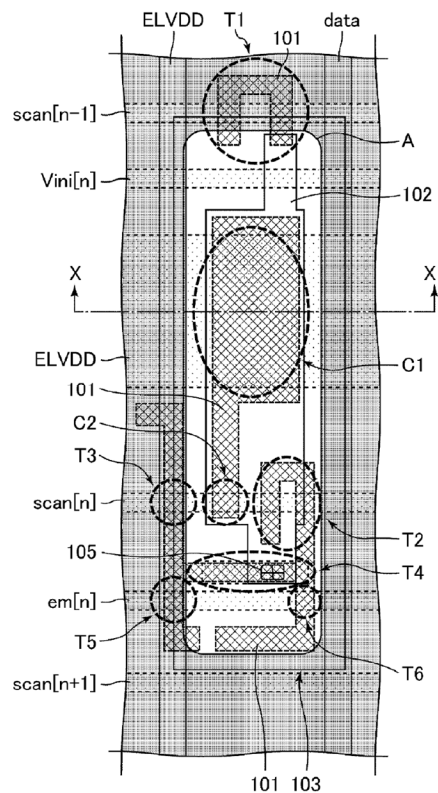
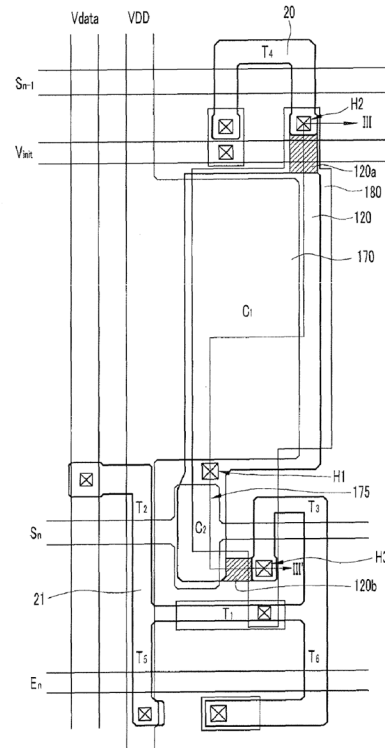


FIG. 2



Left: Noguchi-I, FIG. 8; Right: Kim, FIG. 2.

While Noguchi-I's semiconductor pattern includes discontinuities, Kim's semiconductor pattern does not. *See* Noguchi-I, FIG. 8; Kim, FIG. 2. In the Petition's combination, Noguchi-I's pixel layout is modified based on the teachings of Kim to form a contiguous semiconductor pattern. *See* § IV.G.3. POSITAs would have been motivated and found it obvious to make this modification because Kim's continuous

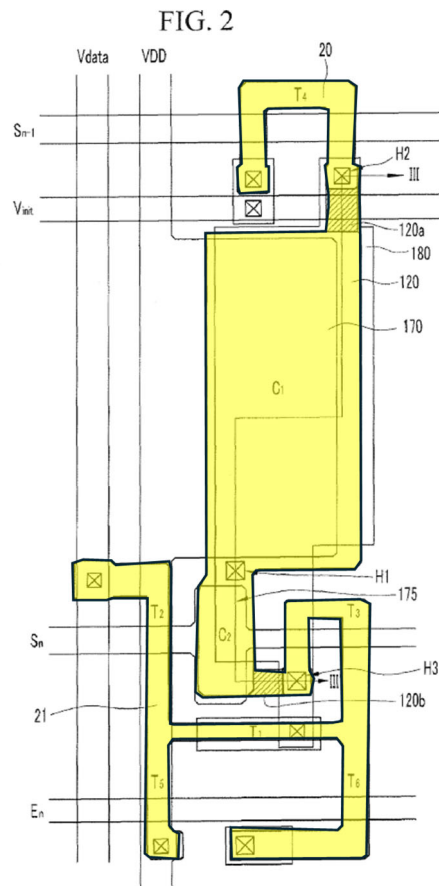
semiconductor pattern constituted a known alternative that required less masking to Noguchi-I's non-contiguous pattern. Kanicki, ¶¶384-386. Furthermore, incorporating Kim's semiconductor layer structure would allow for a "dual-structure" capacitor to increase capacitance. Kim, 1:64-65, 5:42-51. Such a modification amounted to a simple design choice that involved a routine task of making minor changes to the semiconductor pattern and was well within the skill set of POSITAs. Kanicki, ¶386.

Additionally, and as previously discussed, Noguchi-I can be combined individually with each of the cited references—Udagawa, Noguchi-II, Jeong, and Kim. In each instance, the combination involves modifying a distinct aspect of Noguchi-I, and these modifications are independent of one another. Accordingly, POSITAs would have found it obvious and would have been motivated to combine Noguchi-I with each of Udagawa, Noguchi-II, and Kim, and would have had a reasonable expectation of success. *Id.*, ¶387.

3. Claims 1-30

To the extent that PO argues that Noguchi-I does not teach or suggest "the semiconductor layer being extended to and electrically coupled to" TFT T1 in 1[m] because of a discontinuity in the portion of the semiconductor pattern that extends to T1, POSITAs would have found it obvious to modify Noguchi-I to have a contiguous semiconductor pattern based on the teachings of Kim. Kanicki, ¶389.

Kim describes a TFT driving circuit similar to Noguchi-I's Figure 1. *See* Kim, 7:34-8:51; FIG. 5; Kanicki, ¶390. Kim further provides a transistor layout similar to Noguchi-I's Figure 8. *See* Kim, 5:12-18, FIG. 2; Kim explains **T4 in Figure 2 is connected to T3 using semiconductor patterns 120, 120a and 120b**. Kim, 6:29-49. Annotated Figure 2 below shows the semiconductor layer of Kim, forming a contiguous pattern that extends to all TFTs. Kanicki, ¶390.



POSITAs would have been motivated to utilize the teachings of Kim to modify Noguchi-I's semiconductor pattern to contiguously extend to TFT T1. §IV.G.2; Kanicki, ¶391.

The addition of Kim does not change other analysis above regarding claims 1-30. Kanicki, ¶391; *see* §§IV.E-IV.F.8.

V. CONCLUSION

The Board should institute IPR and cancel the Challenged Claims.

VI. MANDATORY NOTICES

A. Real Party in Interest

Petitioner identifies itself as a real party in interest. The following are identified as additional real parties in interest: Mianyang BOE Optoelectronics Technology Co., Ltd., Ordos Yuansheng Optoelectronics Co., Ltd., Chengdu BOE Optoelectronics Technology Co., Ltd., Chongqing BOE Optoelectronics Technology Co., Ltd., Wuhan BOE Optoelectronics Technology Co., Ltd., Yunnan Invensight Optoelectronics Technology Co., Ltd. f/k/a/ BMOT f/k/a Kunming BOE Display Technology, and BOE Technology America, Inc.

B. Related Matters

To the best of Petitioner's knowledge, the '990 Patent has been involved in *Samsung Display Co. v. BOE Technology Group Co.*, No. 2:25-cv-00426-JRG (E.D. Tex.).

C. Notice of Counsel and Service Information

Petitioner consents to electronic service. All communications to the attorneys listed below may be sent to: PerkinsServiceBOESamsungIPRs@perkinscoie.com

LEAD COUNSEL	BACK-UP COUNSEL
Babak Tehranchi Reg. No. 55,937 Perkins Coie LLP 11452 El Camino Real, Suite 300 San Diego, CA 92130-2080 Phone: 858.720.5700 Fax: 858.720.5799 tehranchi-ptab@perkinscoie.com	Bing Ai Reg. No. 43,312 Perkins Coie LLP 11452 El Camino Real, Suite 300 San Diego, CA 92130-2080 Phone: 858.720.5700 Fax: 858.720.5799 ai-ptab@perkinscoie.com
BACK-UP COUNSEL	BACK-UP COUNSEL
Jessica C. Kaiser Reg. No. 58,937 Perkins Coie LLP 1900 16th St Mall #1400 Denver, CO 80202 Tel: 303.291.2300 Fax: 303.291.2400 kaiser-ptab@perkinscoie.com	John C. Moulder Reg. No. 70,490 Perkins Coie LLP 700 Thirteenth Street N.W. Suite 800 Washington, DC 20005-3960 Phone: 202.654.6200 Fax: 202.654.6211 moulder-ptab@perkinscoie.com
BACK-UP COUNSEL	BACK-UP COUNSEL
John Esterhay Reg. No. 73,512 Perkins Coie LLP 11452 El Camino Real, Suite 300 San Diego, CA 92130-2080 Phone: 858.720.5700 Fax: 858.720.5799 esterhay-ptab@perkinscoie.com	Wei Yuan Reg. No. 71,772 Perkins Coie LLP 11452 El Camino Real, Suite 300 San Diego, CA 92130-2080 Phone: 858.720.5700 Fax: 858.720.5799 yuan-ptab@perkinscoie.com

BACK-UP COUNSEL	
Gautam Thatte Reg. No. 75,568 Perkins Coie LLP 11452 El Camino Real, Suite 300 San Diego, CA 92130-2080 Phone: 858.720.5700 Fax: 858.720.5799 thatte-ptab@perkinscoie.com	

D. Power of Attorney

A power of attorney is filed herewith according to 37 C.F.R. §42.10(b).

Respectfully submitted,

/Babak Tehrani/

Babak Tehrani
Reg. No. 55,937
Attorney for Petitioner

PERKINS COIE LLP
11452 El Camino Real Ste 300
San Diego, CA 92130-2080

Date: August 30, 2025

CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(d)

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned Petition for *inter partes* review of U.S. Patent No. 11,574,990, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,942. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

/Babak Tehranchi/

Babak Tehranchi
Reg. No. 55,937
Attorney for Petitioner

Date: August 30, 2025
PERKINS COIE LLP
11452 El Camino Real Ste 300
San Diego, CA 92130-2080

CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of the Petition for *inter partes* review of U.S. Patent No. 11,574,990 and supporting materials (Exhibits and Power of Attorney) were served via USPS Priority Mail Express delivery on the Patent Owner at the correspondence address of record as listed on PAIR:

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel listed below:

Amanda Aline Abraham - aa@rothfirm.com
Jeffrey H. Lerner – jlerner@cov.com
Jared R. Frisch - jfrisch@cov.com
Daniel W. Cho - dwcho@cov.com
Kee Young Lee - kylee@cov.com
Robert T. Haslam - rhaslam@cov.com
Scott A. Schrader - sschrader@cov.com
Jesse Y. Chang - jychang@cov.com
Sean Hong - shong@cov.com

Respectfully submitted,

/Meghan Bright/

Meghan Bright
Patent Paralegal

Date: August 30, 2025