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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	02/07/2023	11574991	224721/411598-06509	1880

23363 7590 01/18/2023

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Se-Ho Kim, Yongin-si, KOREA, REPUBLIC OF;
Jin-Woo Park, Yongin-si, KOREA, REPUBLIC OF;
Won-Se Lee, Yongin-si, KOREA, REPUBLIC OF;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

SAMSUNG DISPLAY CO., LTD., Yongin-si, KOREA, REPUBLIC OF;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

BOE v. Samsung IPR2025-01479
Ex-1002

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

23363 7590 01/09/2023

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
01/09/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PLPrivatePair@lrrc.com
pto@lewisroca.com

Corrected ***Notice of Allowability***	**Application No.** 17/871,618	**Applicant(s)** Kim et al.	
	Examiner LEX H MALSAWMA	**Art Unit** 2892	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the IDS filed 12/27/2022 and the amendment filed 12/28/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some* c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/27/2022.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LEX H MALSAWMA/
Primary Examiner, Art Unit 2892

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Response to Rule 312 Communication	Application No.	Applicant(s)	
	17/871,618	Kim et al.	
	Examiner	Art Unit	AIA (FITF) Status
	LEX H MALSAWMA	2892	No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☑ The amendment filed on 28 December 2022 under 37 CFR 1.312 has been considered, and has been:

a) ☑ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

f) ☐ not entered because the supplemental or corrected Application Data sheet (ADS)

☐ was not accompanied by a petition to accept an unintentionally delayed claim under 37 CFR 1.55 or 27 CFR 1.78;

☐ did not identify the information being changed in accordance with 37 CFR 1.76(c)(2);

☐ was not properly signed in accordance with 37 CFR 1.76(e) (or 37 CFR 1.33(b) for applications filed prior to September 16, 2012).

/LEX H MALSAWMA/ Primary Examiner, Art Unit 2892	

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	17871618
Filing Date	2022-07-22
First Named Inventor	Se-Ho Kim
Art Unit	2892
Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
Attorney Docket Number	224721/411598-06509

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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If you wish to add additional U.S. Published Application citation information please click the Add button. Add

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EFS Web 2.1.18

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
Ex-1002

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17871618
	Filing Date	2022-07-22
	First Named Inventor	Se-Ho Kim
	Art Unit	2892
	Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
	Attorney Docket Number	224721/411598-06509

	1	US Notice of Allowance dated December 14, 2022, issued in US Patent Application No. 17/234,670 (7 pages).
	2	US Ex Parte Quayle Action dated December 20, 2022, issued in US Patent Application No. 17/853,368 (8 pages).

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/LEX H MALSAWMA/	Date Considered	01/05/2023

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
Ex-1002

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17871618
	Filing Date	2022-07-22
	First Named Inventor	Se-Ho Kim
	Art Unit	2892
	Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
	Attorney Docket Number	224721/411598-06509

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2022-12-27
Name/Print	Jun-Young E. Jeon	Registration Number	43693

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
Ex-1002

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
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OK TO ENTER: /L.H.M./

PATENT

Date of Notice
of Allowance : October 21, 2022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on December 28, 2022 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Marti Carrillo/
Marti Carrillo

Inventor : Se-Ho Kim, et al. Confirmation No. 1880

Application No. : 17/871,618
Filed : July 22, 2022

Title : ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

Grp./Div. : 2892
Examiner : Lalrinfamkim Hmar Malsawma

Docket No. : 224721

AMENDMENT UNDER 37 CFR § 1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
December 28, 2022

Commissioner:

Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 10 of this paper.

119291817.2

BOE v. Samsung IPR2025-01479
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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23363 7590 10/21/2022
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Si Vuong	(Typed or printed name)
/Si Vuong/	(Signature)
December 28, 2022 (E-filed)	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

TITLE OF INVENTION: ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	01/23/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
MALSAWMA, LALRINFAMKIM HMAR	2892	257-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Lewis Roca Rothgerber Christie LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Samsung Display Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Yongin-si, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies 0

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 03-1728

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jun-Young E. Jeon/ Date December 28, 2022

Typed or printed name Jun-Young E. Jeon Registration No. 43,693

BOE v. Samsung IPR2025-01479
Ex-1002

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/871,618	**12/28/2022 09:34:39 PM ET**	**224721/411598-06509**

Title of Invention

ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	1880	FILED BY	Si Vuong
PATENT CENTER #	61363662	FILING DATE	07/22/2022
CUSTOMER #	23363	FIRST NAMED INVENTOR	Se-Ho Kim
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Jun-Young Jeon

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
224721_IssueFeeTransmittal.pdf	1	Issue Fee Payment (PTO-85B)	237 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
224721_IssueFeeTransmittal.pdf	4418600776467FEB2C7E9455BEFAE8870F164E63E83B5AFF73521B3436F4C0D2748793A661C6DE66A08773A13824D322640AC15F1EE292027BE2B6C41A59134A

BOE v. Samsung IPR2025-01479
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

BOE v. Samsung IPR2025-01479
Ex-1002

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/871,618	12/28/2022 09:34:39 PM ET	224721/411598-06509

Title of Invention

ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	1880	FILED BY	Si Vuong
PATENT CENTER #	61363662	AUTHORIZED BY	Jun-Young Jeon
CUSTOMER #	23363	FILING DATE	07/22/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Se-Ho Kim

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 4792	E2022BRL35240249	Si Vuong

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1501	UTILITY ISSUE FEE	1200.00	1	1200.00
			TOTAL AMOUNT:	$1,200.00

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C.

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371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT

Date of Notice
of Allowance : October 21, 2022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on December 28, 2022 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Marti Carrillo/
Marti Carrillo

Inventor : Se-Ho Kim, et al. Confirmation No. 1880

Application No. : 17/871,618
Filed : July 22, 2022

Title : ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

Grp./Div. : 2892
Examiner : Lalrinfamkim Hmar Malsawma

Docket No. : 224721

AMENDMENT UNDER 37 CFR § 1.312

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
December 28, 2022

Commissioner:

Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 10 of this paper.

119291817.2

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An organic light emitting diode display comprising:

a non-conductive substrate;

a plurality of first voltage lines;

a plurality of scan lines;

a plurality of data lines;

a plurality of driving circuits formed on the substrate;

a plurality of organic light emitting diodes, wherein each of the plurality of organic light emitting diodes is electrically coupled to a respective one of the plurality of driving circuits;

wherein each of the driving circuits comprises:

a first thin film transistor implemented in a first portion of a semiconductor layer disposed on the substrate, and coupled to one of the plurality of scan lines and to one of the plurality of data lines;

a second thin film transistor implemented in a second portion of the semiconductor layer, wherein the semiconductor layer couples the second thin film transistor to the first thin film transistor, and wherein the second portion of the semiconductor layer has at least one bent portion;

a storage capacitor comprising:

a first capacitor plate that is configured to operate as [[the]] a gate electrode of the second thin film transistor;

a second capacitor plate electrically coupled to one of the plurality of first voltage lines and overlapping the first capacitor plate; and

an insulating layer between the first capacitor plate and the second capacitor plate;

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a third thin film transistor implemented in a third portion of the semiconductor layer, wherein the semiconductor layer couples the third thin film transistor to the first thin film transistor and to the second thin film transistor, and wherein the third thin film transistor is electrically coupled to one of the plurality of first voltage lines through the semiconductor layer; and

a fourth thin film transistor implemented in a fourth portion of the semiconductor layer, wherein the semiconductor layer couples the fourth thin film transistor to the second thin film transistor, and wherein the fourth thin film transistor is electrically coupled to the respective organic light emitting diode through the semiconductor layer; and

wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate.

2. (Original) An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

3. (Original) An organic light emitting diode display according to claim 2, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor electrically coupled to the first capacitor plate; and

a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,

wherein the sixth thin film transistor is coupled to the fifth thin film transistor.

4. (Original) An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

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5. (Original) An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

6. (Original) An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

7. (Original) An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode,

wherein the seventh thin film transistor is coupled to the fourth thin film transistor.

8. (Original) An organic light emitting diode display according to claim 4, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

9. (Original) An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.

10. (Original) An organic light emitting diode display according to claim 2, further comprising:

a plurality of second voltage lines;

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a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

a sixth thin film transistor implemented in a sixth portion of the semiconductor layer,

wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and

wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

11. (Original) An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

12. (Original) An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

13. (Original) An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

14. (Currently Amended) An organic light emitting diode display according to claim 11, further comprising a seventh thin film transistor implemented in [[a]] the sixth portion of the semiconductor layer,

wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

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wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

15. (Original) An organic light emitting diode display according to claim 11, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

16. (Original) An organic light emitting diode display according to claim 1, wherein a periphery of the first capacitor plate completely surrounds a periphery of the second capacitor plate in a plan view.

17. (Original) An organic light emitting diode display according to claim 1, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor electrically coupled to the first capacitor plate; and

a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,

wherein the sixth thin film transistor is coupled to the fifth thin film transistor.

18. (Original) An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

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19. (Original) An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

20. (Original) An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

21. (Original) An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode,

wherein the seventh thin film transistor is coupled to the fourth thin film transistor.

22. (Original) An organic light emitting diode display according to claim 18, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

23. (Original) An organic light emitting diode display according to claim 1, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

a sixth thin film transistor implemented in a sixth portion of the semiconductor layer, wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and wherein the sixth thin film transistor is electrically coupled to one

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of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

24. (Original) An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

25. (Original) An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

26. (Original) An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

27. (Currently Amended) An organic light emitting diode display according to claim 24, further comprising a seventh thin film transistor implemented in [[a]] the sixth portion of the semiconductor layer,

wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

28. (Original) An organic light emitting diode display according to claim 24, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

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wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

29. (Original) An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.

30. (Original) An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

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REMARKS/ARGUMENTS

Claims 1-30 are allowed and remain in the present application, of which claim 1 is independent. Claims 1, 14, and 27 are amended herein to correct minor clerical errors. No new matter has been entered.

This amendment was not presented earlier because Applicant did not notice the error until after the receipt of the Notice of Allowance. Accordingly, Applicant respectfully requests entry of the above amendments.

Respectfully submitted,
LEWIS ROCA ROTHGERBER CHRISTIE LLP

By */Kyle W. Kellar/*
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/mac

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PATENT AND TRADEMARK OFFICE

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/871,618	**12/28/2022 02:56:33 PM ET**	**224721/411598-06509**

Title of Invention

ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	1880	FILED BY	Marti Carrillo
PATENT CENTER #	61361335	FILING DATE	07/22/2022
CUSTOMER #	23363	FIRST NAMED INVENTOR	Se-Ho Kim
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Kyle Kellar

Documents

TOTAL DOCUMENTS: 3

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
224721_312_Amendment.pdf		10	-	117 KB
224721_312_Amendment-A.NA.pdf	(1-1)	1	Amendment after Notice of Allowance (Rule 312)	102 KB
224721_312_Amendment-CLM.pdf	(2-9)	8	Claims	90 KB
224721_312_Amendment-REM.pdf	(10-10)	1	Applicant Arguments/Remarks Made in an Amendment	101 KB

Digest

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DOCUMENT	MESSAGE DIGEST(SHA-512)
224721_312_Amendment.pdf	E1C5D2767A3807EA6134C37F05504F6E81FA5F7D0D9A408B2700FEF70DCB7F57F9E05663F63A0195EBC3F2D475A67F88F986FC3EBA1CA3E6C274056E038229F9
224721_312_Amendment-A.NA.pdf	D33B3B7FF6F9D6C28E16A29D5A5D1DBBD67E832118DA7301446715214DFB6D53C1621CEACF127D5442ADF48B3F0E02F0B2A6465E62EDD67CF94A2D0CB5B2BE66
224721_312_Amendment-CLM.pdf	7D347D0B7242BA5C94F6B0570F2D7D248C85B047DFF1DB15939FF57057C266DA2EA0E431154E4D61F7A95D1CF988660DCC70075CEAD690F6D08D00E9061FC874
224721_312_Amendment-REM.pdf	F69DB9F0F32797A43DC2F88F1FA9127D4DA2A1DDA291D68BBB72187B2B8DD2277DA100D407901509AFAB7E6C7C289572D63501ACF73321A254504D0B0762F809

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17871618
Filing Date	2022-07-22
First Named Inventor	Se-Ho Kim
Art Unit	2892
Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
Attorney Docket Number	224721/411598-06509

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17871618
	Filing Date	2022-07-22
	First Named Inventor	Se-Ho Kim
	Art Unit	2892
	Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
	Attorney Docket Number	224721/411598-06509

	1	US Notice of Allowance dated December 14, 2022, issued in US Patent Application No. 17/234,670 (7 pages).
	2	US Ex Parte Quayle Action dated December 20, 2022, issued in US Patent Application No. 17/853,368 (8 pages).

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17871618
	Filing Date	2022-07-22
	First Named Inventor	Se-Ho Kim
	Art Unit	2892
	Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
	Attorney Docket Number	224721/411598-06509

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2022-12-27
Name/Print	Jun-Young E. Jeon	Registration Number	43693

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/853,368	06/29/2022	Se-Ho Kim	224005/411598-06414	1932

23363 7590 12/20/2022

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
12/20/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PLPrivatePair@lrrc.com
pto@lewisroca.com

Office Action Summary	Application No. 17/853,368	Applicant(s) Kim et al.	
	Examiner LEX H MALSAWMA	Art Unit 2892	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 12/05/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☑ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-22 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☑ Claim(s) 1,3-4,6,8,10-12 and 14-22 is/are allowed.

7) ☐ Claim(s) _____ is/are rejected.

8) ☑ Claim(s) 2,5,7,9 and 13 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 06/29/2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 12/05/2022 has been entered.

Claim Objections

3. Claims 2, 5, 7, 9 and 13 are objected to because of the following informalities shown in **bold, underlined, and strikethrough** text:

2. (Original) The organic light emitting diode display according to claim 1, further comprising a fourth thin film transistor implemented in a fourth portion of the semiconductor layer and electrically coupled to **the** one of the first voltage lines,

wherein the semiconductor layer electrically couples the fourth thin film transistor to the second thin film transistor.

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5. (Original) The organic light emitting diode display according to claim 4, further comprising:

a seventh thin film transistor implemented in a seventh portion of the semiconductor layer and electrically coupled to **the** one of the ~~**plurality of**~~ second voltage lines and the one of the organic light emitting diodes,

wherein the semiconductor layer electrically couples the seventh thin film transistor to the fifth thin film transistor.

7. (Original) The organic light emitting diode display according to claim 4, wherein ~~**the**~~ **a** gate electrode of the sixth thin film transistor is configured to receive a signal from one of a plurality of second scan lines.

9. (Original) The organic light emitting diode display according to claim 1, wherein the second capacitor plate is electrically coupled to **the** one of the ~~**plurality of**~~ first voltage lines.

13. (Original) The organic light emitting diode display according to claim 5, wherein ~~**the**~~ **a** gate electrode of the seventh thin film transistor is configured to receive a signal from one of a plurality of bypass control lines.

The examiner interprets claims 2, 5, 7, 9 and 13 as shown above.

Appropriate correction is required.

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Allowable Subject Matter

4. Claims 1, 2(as interpreted), 3, 4, 5(as interpreted), 6, 7(as interpreted), 8, 9(as interpreted), 10-12, 13(as interpreted), and 14-22 are allowed for reasons stated in a prior Office action.

Remarks

5. The specification as originally filed does not explicitly disclose "first voltage lines", "driving circuits", and "second voltage lines", and to clarify the record, the examiner's interpretation of essential elements in the current claims are explained below and Fig. 8 is also reproduced below as an example to show essential elements of claims 1 and 4.

Applicant is requested to make any corrections/comments to the examiner's interpretation if necessary to clarify the record.

a) "a plurality of driving circuits" maps to the circuit in Figs. 1 and 10, wherein Figs. 1 and 10 show only one driving circuit for one pixel of the display.

b) "a plurality of first voltage lines" maps to element "172" in Figs. 1, 8, 10 and 11.

c) "a plurality of second voltage lines" maps to element 124 in Figs., 1, 8, 10 and 11.

d) the first TFT maps to T2 in Figs., 1, 8, 10 and 11.

e) the second TFT maps to T1 in Figs., 1, 8, 10 and 11.

f) the third TFT maps to T3 in Figs., 1, 8, 10 and 11.

g) the fourth TFT maps to T5 in Figs., 1, 8, 10 and 11.

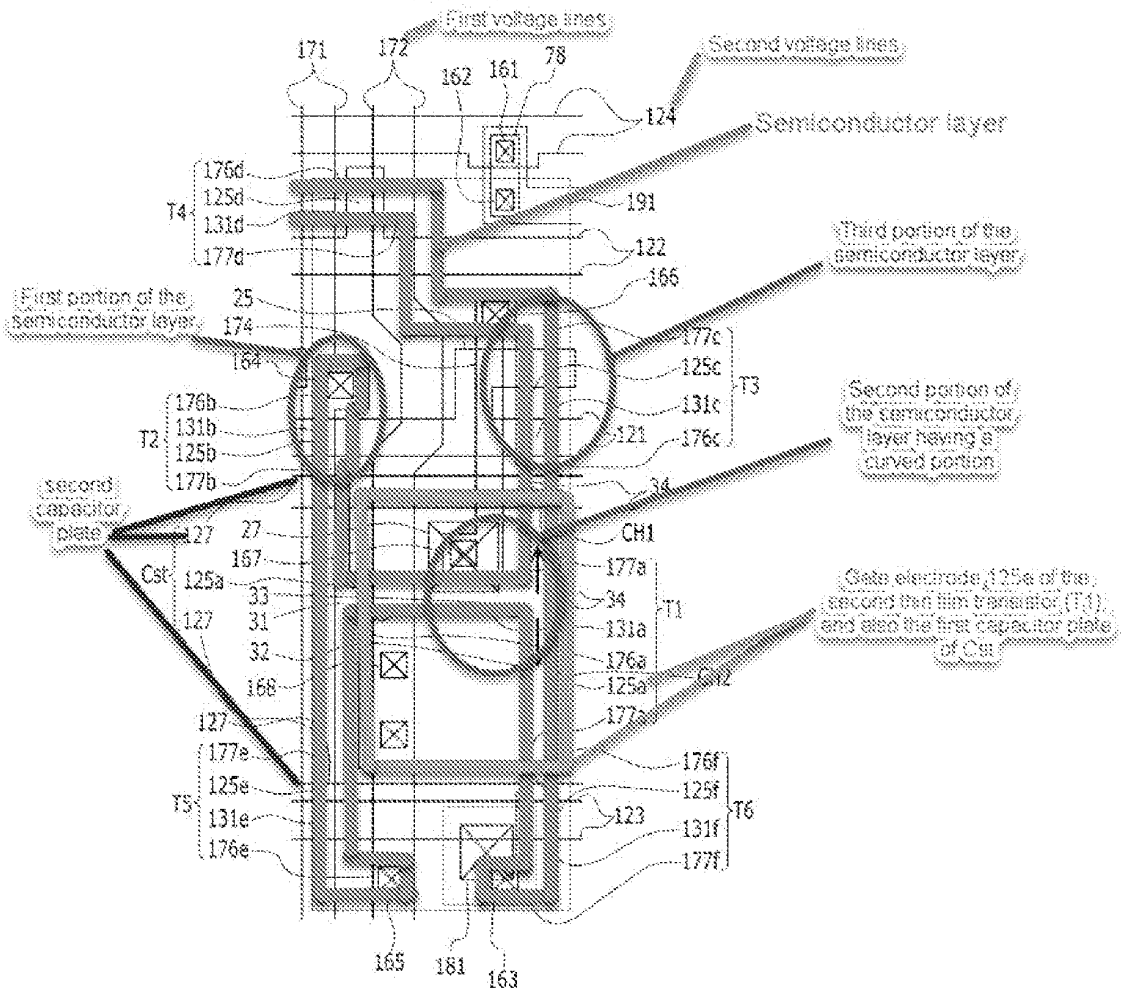
h) the fifth TFT maps to T6 in Figs., 1, 8, 10 and 11.

i) the sixth TFT maps to T4 in Figs., 1, 8, 10 and 11.

j) the seventh TFT maps to T7 in Figs., 1, 8, 10 and 11.

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FIG. 8


First voltage lines
Second voltage lines
Semiconductor layer
Third portion of the semiconductor layer
First portion of the semiconductor layer
Second portion of the semiconductor layer having a curved portion
Second capacitor plate
Gate electrode (125a of the second thin film transistor (T1)) and also the first capacitor plate of Cst
171
172
162
161
78
124
191
122
166
25
174
164
176d
125d
131d
177d
T4
176b
131b
125b
177b
T2
177c
125c
131c
176c
T3
121
34
CH1
27
167
Cst
125a
33
31
32
168
127
177a
34
131a
176a
125a
177a
T1
Cst2
176f
125f
123
131f
177f
T6
177e
125e
131e
176e
T5
165
181
163

Conclusion

6. This application is in condition for allowance except for the following formal matters:

Claims 2, 5, 7, 9 and 13 are objected to for reasons shown above.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 25 USPQ 74, 453 O.G. 213, (Comm'r Pat. 1935).

A shortened statutory period for reply to this action is set to expire **TWO (2) MONTHS** from the mailing date of this letter. Extensions of time may be granted under 37 CFR 1.136 but in no case can any extension carry the date for reply to this Office action beyond the maximum period of SIX MONTHS set by statute (35 U.S.C. 133).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEX H MALSAWMA whose telephone number is (571)272-1903. The examiner can normally be reached M-F (4-12 Hours, between 5:30AM-10PM).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit:

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https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LEX H MALSAWMA/
Primary Examiner, Art Unit 2892

BOE v. Samsung IPR2025-01479
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Electronic Patent Application Fee Transmittal

Application Number:	17871618
Filing Date:	22-Jul-2022
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION
First Named Inventor/Applicant Name:	Se-Ho Kim
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Attorney Docket Number:	224721/411598-06509

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

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Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

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Electronic Acknowledgement Receipt	
EFS ID:	47280959
Application Number:	17871618
International Application Number:	
Confirmation Number:	1880
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION
First Named Inventor/Applicant Name:	Se-Ho Kim
Customer Number:	23363
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Filer Authorized By:	Jun-Young E. Jeon
Attorney Docket Number:	224721/411598-06509
Receipt Date:	27-DEC-2022
Filing Date:	22-JUL-2022
Time Stamp:	18:29:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$260
RAM confirmation Number	E2022BQI29424185
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	224721_IDS.pdf	1042005 37641393f64282cc81d1db8ec223429454842d54	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Other reference-Patent/Application/ Search Documents	12-14-22_NOA_203633.pdf	629557 61b81e16b1364b4eff408311a03b85b5cc726794	no	7
Warnings:					
Information:					
3	Other reference-Patent/Application/ Search Documents	12-20-22_ExParteQuayle_224005.pdf	444957 867e71feba03bcffb80eead37c2a34ec1abdccc2	no	8
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	38387 e528cf6dcf1d136a1154904f31bf68b730c0a71d	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	2154906		

BOE v. Samsung IPR2025-01479
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

23363 7590 12/21/2022

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
12/21/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PLPrivatePair@lrrc.com
pto@lewisroca.com

Corrected ***Notice of Allowability***	**Application No.** 17/871,618	**Applicant(s)** Kim et al.	
	Examiner LEX H MALSAWMA	**Art Unit** 2892	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the IDS filed 12/02/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some* c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/2/2022.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LEX H MALSAWMA/
Primary Examiner, Art Unit 2892

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	17871618
Filing Date	2022-07-22
First Named Inventor	Se-Ho Kim
Art Unit	2892
Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
Attorney Docket Number	224721/411598-06509

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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	1							

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

EFS Web 2.1.18

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17871618
	Filing Date	2022-07-22
	First Named Inventor	Se-Ho Kim
	Art Unit	2892
	Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
	Attorney Docket Number	224721/411598-06509

	1	US Office Action dated November 10, 2022, issued in US Patent Application No. 17/234,670 (7 pages)

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/LEX H MALSAWMA/	Date Considered	12/17/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
Ex-1002

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17871618
	Filing Date	2022-07-22
	First Named Inventor	Se-Ho Kim
	Art Unit	2892
	Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
	Attorney Docket Number	224721/411598-06509

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2022-12-02
Name/Print	Jun-Young E. Jeon	Registration Number	43693

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
Ex-1002

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
Ex-1002

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17871618
Filing Date	2022-07-22
First Named Inventor	Se-Ho Kim
Art Unit	2892
Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
Attorney Docket Number	224721/411598-06509

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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	First Named Inventor	Se-Ho Kim
	Art Unit	2892
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	Attorney Docket Number	224721/411598-06509

	1	US Office Action dated November 10, 2022, issued in US Patent Application No. 17/234,670 (7 pages)

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Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2022-12-02
Name/Print	Jun-Young E. Jeon	Registration Number	43693

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	17871618
Filing Date:	22-Jul-2022
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION
First Named Inventor/Applicant Name:	Se-Ho Kim
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Attorney Docket Number:	224721/411598-06509

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

BOE v. Samsung IPR2025-01479
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Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

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Electronic Acknowledgement Receipt	
EFS ID:	47138279
Application Number:	17871618
International Application Number:	
Confirmation Number:	1880
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION
First Named Inventor/Applicant Name:	Se-Ho Kim
Customer Number:	23363
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Filer Authorized By:	Jun-Young E. Jeon
Attorney Docket Number:	224721/411598-06509
Receipt Date:	02-DEC-2022
Filing Date:	22-JUL-2022
Time Stamp:	19:55:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$260
RAM confirmation Number	E2022B2J56081784
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Other reference-Patent/Application/ Search Documents	11-10-22_OA_203633.pdf	349267 85f7140834982e2af44bbff4a85b7556415d102f	no	7
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	224721_IDS.pdf	1041931 a52ee3fac7446bec8b17bbb5109cb7a645ba6be0	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
3	Fee Worksheet (SB06)	fee-info.pdf	38388 7de7bdc9d2da3746e35356b7ab0e1da2c4270bb9	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1429586		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509

CONFIRMATION NO. 1880

23363
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

PUBLICATION NOTICE

OC000000136919762

Title:ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

Publication No.US-2022-0376030-A1
Publication Date:11/24/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

23363 7590 10/28/2022

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
10/28/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PLPrivatePair@lrrc.com
pto@lewisroca.com

Corrected ***Notice of Allowability***	**Application No.** 17/871,618	**Applicant(s)** Kim et al.	
	Examiner LEX H MALSAWMA	**Art Unit** 2892	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the IDS filed 10/20/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some* c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/20/2022.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LEX H MALSAWMA/
Primary Examiner, Art Unit 2892

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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First Named Inventor	Se-Ho Kim
Art Unit	2892
Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
Attorney Docket Number	224721/411598-06509

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	1	9660012	B2	2017-05-23	Kim et al.	
	2	9899464	B2	2018-02-20	Kim et al.	
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Ex-1002

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	Attorney Docket Number	224721/411598-06509

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NON-PATENT LITERATURE DOCUMENTS [Remove]

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	US Office Action dated September 2, 2022, issued in US Patent Application No. 17/853368 (6 pages)	
	2	US Office Action dated September 2, 2022, issued in US Patent Application No. 17/853551 (9 pages)	
	3	US Office Action dated September 14, 2022, issued in US Patent Application No. 17/853451 (7 pages)	
	4	US Notice of Allowance dated October 4, 2022, issued in US Patent Application No. 17/853368 (7 pages)	
	5	US Notice of Allowance dated October 4, 2022, issued in US Patent Application No. 17/853551 (7 pages)	
	6	US Notice of Allowance dated October 20, 2022, issued in US Patent Application No. 17/853451 (7 pages)	

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EXAMINER SIGNATURE

Examiner Signature	/LEX H MALSAWMA/	Date Considered	10/26/2022

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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OR

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See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Peter Hsueh/	Date (YYYY-MM-DD)	2022-10-20
Name/Print	Peter Hsueh	Registration Number	45574

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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BOE v. Samsung IPR2025-01479
Ex-1002

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
Ex-1002

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

23363 7590 10/21/2022
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	PAPER NUMBER
2892	

DATE MAILED: 10/21/2022

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

TITLE OF INVENTION: ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	01/23/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PTOL-85 (Rev. 02/11)

BOE v. Samsung IPR2025-01479
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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23363 7590 10/21/2022
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

TITLE OF INVENTION: ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	01/23/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
MALSAWMA, LALRINFAMKIM HMAR	2892	257-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

BOE v. Samsung IPR2025-01479
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

23363 7590 10/21/2022

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	PAPER NUMBER
2892	

DATE MAILED: 10/21/2022

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

BOE v. Samsung IPR2025-01479
Ex-1002

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

BOE v. Samsung IPR2025-01479
Ex-1002

Notice of Allowability	Application No. 17/871,618	Applicant(s) Kim et al.	
	Examiner LEX H MALSAWMA	Art Unit 2892	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to papers filed 09/29/2022.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some* c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/LEX H MALSAWMA/
Primary Examiner, Art Unit 2892

Remarks

1. The present application is being examined under the pre-AIA first to invent provisions.

2. The objection to the title is withdrawn in view of the amendment.

3. The terminal disclaimer filed on 09/29/2022 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of **U.S. Application No. 17/853,551** has been reviewed and is accepted. The terminal disclaimer has been recorded.

4. The following is an examiner's statement of reasons for allowance:

Claims 1-30 are allowed primarily because the prior art of record cannot anticipate or render obvious the following limitations, in combination as recited in independent claim 1: wherein the second portion of the semiconductor layer has at least one bent portion, and wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

BOE v. Samsung IPR2025-01479
Ex-1002

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEX H MALSAWMA whose telephone number is (571)272-1903. The examiner can normally be reached M-F (4-12 Hours, between 5:30AM-10PM).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LEX H MALSAWMA/
Primary Examiner, Art Unit 2892

BOE v. Samsung IPR2025-01479
Ex-1002

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/871,618	Kim et al.
	Examiner	Art Unit
	LEX H MALSAWMA	2892

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L 27/3276, 3248, 3258, 3262, 3265, 124, 1255	08/27/2022	LHM.
G09G 3/3225	08/27/2022	LHM
G09G 2300/0809	08/27/2022	LHM
above UPDATED	10/08/2022	LHM

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/LEX H MALSAWMA/ Primary Examiner, Art Unit 2892	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/871,618	Kim et al.
	Examiner	Art Unit
	LEX H MALSAWMA	2892

Search Notes		
Search Notes	**Date**	**Examiner**
H01L 27/3276, 3248, 3258, 3262, 3265, 124, 1255 (text limited, see PE2E SEARCH)	08/27/2022	LHM
G09G 3/3225 (text limited, see PE2E SEARCH)	08/27/2022	LHM
G09G 2300/0809 (text limited, see PE2E SEARCH)	08/27/2022	LHM
USPC 257/40 cross reference search	08/27/2022	LHM
Inventor and assignee search	08/27/2022	LHM
PE2E SEARCH	09/10/2022	LHM
US Patents 9450040, 9660012, 9899464, 10204976, 10483342, 10734470, 10985234	09/10/2022	LHM
above UPDATED	10/08/2022	LHM
PE2E SEARCH	10/08/2022	LHM
Interference search	10/08/2022	LHM

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
H01L	27/3276	10/08/2022	LHM

/LEX H MALSAWMA/ Primary Examiner, Art Unit 2892	

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/871,618	Kim et al.
	Examiner	**Art Unit**
	LEX H MALSAWMA	2892

CPC								
Symbol							**Type**	**Version**
H01L	/	27	/	3276			F	2013-01-01
H01L	/	27	/	3265			I	2013-01-01
H01L	/	27	/	3262			I	2013-01-01
H01L	/	27	/	3248			I	2013-01-01
H01L	/	27	/	3258			I	2013-01-01
G09G	/	3	/	3225			A	2013-01-01
G09G	/	2300	/	0809			A	2013-01-01
H01L	/	27	/	124			A	2013-01-01
H01L	/	27	/	1255			A	2013-01-01

CPC Combination Sets									
Symbol							**Type**	**Set**	**Ranking**	**Version**
	/		/							

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/LEX H MALSAWMA/ Primary Examiner, Art Unit 2892	08 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9

U.S. Patent and Trademark Office — Part of Paper No.: 20221008

BOE v. Samsung IPR2025-01479
Ex-1002

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/871,618	Kim et al.
	Examiner	**Art Unit**
	LEX H MALSAWMA	2892

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	27	/	32

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/LEX H MALSAWMA/ Primary Examiner, Art Unit 2892	08 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9

U.S. Patent and Trademark Office — Part of Paper No.: 20221008

BOE v. Samsung IPR2025-01479
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/871,618	Kim et al.
	Examiner	**Art Unit**
	LEX H MALSAWMA	2892

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10		19		28								
	2		11		20		29								
	3		12		21		30								
	4		13		22										
	5		14		23										
	6		15		24										
	7		16		25										
	8		17		26										
	9		18		27										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/LEX H MALSAWMA/ Primary Examiner, Art Unit 2892	08 October 2022	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	9

U.S. Patent and Trademark Office Part of Paper No.: 20221008

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CONFIRMATION NO. 1880

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
17/871,618	07/22/2022	257	2892	224721/411598-06509

APPLICANTS

SAMSUNG DISPLAY CO., LTD., Yongin-si, KOREA, REPUBLIC OF;

INVENTORS

Se-Ho Kim, Yongin-si, KOREA, REPUBLIC OF;
Jin-Woo Park, Yongin-si, KOREA, REPUBLIC OF;
Won-Se Lee, Yongin-si, KOREA, REPUBLIC OF;

**** CONTINUING DATA ***************************

This application is a CON of 17/234,670 04/19/2021
which is a CON of 16/984,045 08/03/2020 PAT 10985234
which is a CON of 16/659,372 10/21/2019 PAT 10734470
which is a CON of 16/261,450 01/29/2019 PAT 10483342
which is a CON of 15/900,715 02/20/2018 PAT 10204976
which is a CON of 15/603,309 05/23/2017 PAT 9899464
which is a CON of 15/238,449 08/16/2016 PAT 9660012
which is a CON of 13/952,508 07/26/2013 PAT 9450040

**** FOREIGN APPLICATIONS ***************************

REPUBLIC OF KOREA 10-2012-0084976 08/02/2012

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

08/01/2022

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /LEX HMAR MALSAWMA/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		KOREA, REPUBLIC OF	11	30	1

ADDRESS

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001
UNITED STATES

TITLE

ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION

FILING FEE RECEIVED		
2820	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____

BIB (Rev. 05/07).

BOE v. Samsung IPR2025-01479
Ex-1002

		❑ Credit

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L45	0	17/853,551	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L46	21	"10985234" "10734470" "10483342" "10204976" "9899464" "9660012" "94500040"	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L47	20	("5929464" | "6914642" | "20030222589" | "20040155242" | "20060082524" | "20070040193" | "20070159565" | "20080017866" | "20080129664" | "20100079361" | "20100253710" | "20120146004" | "20120313100" | "20140027728" | "20140070184" | "20140077176" | "20140098078").pn. OR ("9660012").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/10/08 03:00 PM
L48	56	("10134336" OR "10198992" OR "10198993" OR "10204976" OR "10347183" OR "10453395" OR "10483342" OR "10553158" OR "10699639" OR "10734470" OR "10818235" OR "10923030" OR "11302253" OR "20020149711" OR "20030222589" OR "20040155242" OR "20060082524" OR "20070040193" OR "20070159565" OR "20080017866" OR "20080129664" OR "20100079361" OR "20100253710" OR "20110227893" OR "20110273419" OR "20120026146" OR "20120097965" OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 03:00 PM

		"20120146004" OR "20120162275" OR "20120313100" OR "20130075766" OR "20130201172" OR "20130334508" OR "20140001445" OR "20140027728" OR "20140070184" OR "20140077176" OR "20140098078" OR "5929464" OR "6104067" OR "6914642" OR "7576354" OR "7649202" OR "7859054" OR "7999322" OR "8309404" OR "8717259" OR "8878827" OR "9287528" OR "9450040" OR "9501978" OR "9728130" OR "9892683" OR "9922597" OR "9959809" OR "9997108").pn.					
L49	774	((("KIM") near3 ("Se-Ho")) OR (("PARK") near3 ("Jin-Woo")) OR (("LEE") near3 ("Won-Se")))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/10/08 03:00 PM
L50	20348	((("SAMSUNG") near3 ("DISPLAY") near3 ("CO") near3 ("LTD"))).AS,AANM.	(USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L51	14	"10985234" "10734470" "10483342" "10204976" "9899464" "9660012" "94500040"	(USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L52	6	("10985234" "10734470" "10483342" "10204976" "9899464" "9660012" "94500040").pn.	(USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L53	7	("10985234" "10734470" "10483342" "10204976" "9899464" "9660012" "9450040").pn.	(USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L54	7	("10985234" "10734470" "10483342" "10204976" "9899464" "9660012"	(USPAT)	OR	ON	ON	2022/10/08 03:00 PM

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Ex-1002

		"9450040").pn.					
L55	3	16/984,045	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L56	1525	(L5 L6) AND ((curv$5 bend$4 bent) WITH channel)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L57	435	(L5 L6) AND ((curv$5 bend$4 bent) near2 channel)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L58	192	L12 AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L59	76550	H01L27/3276.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L60	30076	H01L27/3248.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO);	OR	ON	ON	2022/10/08 03:00 PM

			FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L61	32283	H01L27/3258.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L62	48274	H01L27/3262.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L63	16930	H01L27/3265.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L64	87751	H01L27/124.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L65	34771	H01L27/1255.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO;	OR	ON	ON	2022/10/08 03:00 PM

			DERWENT; IBM_TDB)				
L66	36105	G09G3/3225.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L67	19241	G09G2300/0809.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L68	28333	257/40.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L69	459	H01L25/046.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L70	2354	H01L27/28.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM

L71	12402	H01L51/00.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L72	2773	H01L2031/0344.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L73	8	H01L2251/00.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L74	287	(L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 L26 L27 L28 L29 L15) AND ((curv$5 bend$4 bent) WITH channel) AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L75	114	L30 NOT L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L76	27	(Artificial Intelligence)	(US-PGPUB; USPAT;	OR	ON	ON	2022/10/08

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Ex-1002

		More like doc: US-9660012-B2 Text: (US-20140034923-A1 OR EP-2693482-A2 OR US-9899464-B2 OR US-20170256601-A1 OR US-9450040-B2 OR EP-2693482-B1 OR EP-2693481-A2 OR EP-2693481-B1 OR TW-201411832-A OR US-20200365678-A1 OR EP-3780112-A1 OR US-20160358995-A1 OR US-20210242296-A1 OR US-10985234-B2 OR TW-I605582-B OR US-20190157376-A1 OR US-20180175134-A1 OR US-10483342-B2 OR US-10204976-B2 OR KR-20140018623-A).did.	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				03:00 PM
L77	20	("5929464" | "6914642" | "20030222589" | "20040155242" | "20060082524" | "20070040193" | "20070159565" | "20080017866" | "20080129664" | "20100079361" | "20100253710" | "20120146004" | "20120313100" | "20140027728" | "20140070184" | "20140077176" | "20140098078").pn. OR ("9660012").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/10/08 03:00 PM
L78	56	("10134336" OR "10198992" OR "10198993" OR "10204976" OR "10347183" OR "10453395" OR "10483342" OR "10553158" OR "10699639" OR "10734470" OR "10818235" OR "10923030" OR "11302253" OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 03:00 PM

BOE v. Samsung IPR2025-01479
Ex-1002

		"20020149711" OR "20030222589" OR "20040155242" OR "20060082524" OR "20070040193" OR "20070159565" OR "20080017866" OR "20080129664" OR "20100079361" OR "20100253710" OR "20110227893" OR "20110273419" OR "20120026146" OR "20120097965" OR "20120146004" OR "20120162275" OR "20120313100" OR "20130075766" OR "20130201172" OR "20130334508" OR "20140001445" OR "20140027728" OR "20140070184" OR "20140077176" OR "20140098078" OR "5929464" OR "6104067" OR "6914642" OR "7576354" OR "7649202" OR "7859054" OR "7999322" OR "8309404" OR "8717259" OR "8878827" OR "9287528" OR "9450040" OR "9501978" OR "9728130" OR "9892683" OR "9922597" OR "9959809" OR "9997108").pn.					
L79	0	17/853,451	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L80	192	L12 AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L81	287	(L16 L17 L18 L19 L20	(US-PGPUB; USPAT;	OR	ON	ON	2022/10/08

		L21 L22 L23 L24 L25 L26 L27 L28 L29 L15) AND ((curv$5 bend$4 bent) WITH channel) AND (third near2 (TFT (thin ADJ film)))	USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				03:00 PM
L82	0	17/781,618	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 03:00 PM
L83	287	(L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 L26 L27 L28 L29 L15) AND ((curv$5 bend$4 bent) WITH channel) AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L84	192	L12 AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L85	21	L12 AND (third NEAR (metal ADJ layer))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L86	570	(third NEAR (metal ADJ layer)) AND ((contact ADJ (hole opening)) WITH through WITH capacitor WITH (plate electrode))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM

L87	1101	((thin ADJ film ADJ transistor) TFT) WITH (electrical$2 NEAR (coupl$3 connect$3)) WITH (contact ADJ (hole opening)) WITH through WITH capacitor WITH (plate electrode)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L88	135	L43 AND (six$4 WITH ((thin ADJ film) TFT))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 03:00 PM
L89	0	((thin ADJ film ADJ transistor) TFT) AND ((curv$5 bent bend$5) WITH ((channel NEAR (layer region portion section part)) (semiconductor NEAR layer)) WITH (under over below beneath underneath) WITH (gate NEAR electrode) WITH cover$5 WITH (capacitor NEAR (plate electrode)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 07:17 PM
L90	0	((curv$5 bent bend$5) WITH ((channel NEAR (layer region portion section part)) (semiconductor NEAR layer)) WITH (under over below beneath underneath) WITH (gate NEAR electrode) WITH cover$5 WITH (capacitor NEAR (plate electrode)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 07:17 PM
L91	13	((curv$5 bent bend$5) WITH ((channel NEAR (layer region portion section part)) (semiconductor NEAR layer))) AND ((under over below beneath underneath) WITH (gate NEAR electrode)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO);	OR	ON	ON	2022/10/08 07:17 PM

		WITH cover$5 WITH (capacitor NEAR (plate electrode)))	FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L92	34	(Artificial Intelligence) Similar to: Unpublished Application # Text: (TW-I272556-B OR TW-586095-B OR US-20120261667-A1 OR TW-200721098-A OR TW-200306510-A OR US-8471259-B2 OR KR-20010050803-A OR EP-1501067-B1 OR CN-101093853-A OR US-20090315032-A1 OR TW-200707382-A OR EP-1720148-A3 OR KR-100354639-B1 OR JP-2001109404-A OR TW-200304103-A OR US-7989808-B2 OR TW-589594-B OR TW-200406135-A OR US-7554116-B2 OR KR-20050121697-A OR CN-101093853-B OR US-20050218452-A1 OR US-20110278578-A1 OR TW-435053-B OR JP-2012230383-A OR CN-101043770-A OR JP-2014044441-A OR KR-100460281-B1 OR KR-100557730-B1 OR US-9165991-B2 OR US-8207537-B2 OR TW-I291308-B OR JP-5648140-B2 OR US-7488972-B2 OR KR-100453634-B1 OR US-7122832-B2 OR JP-2000173779-A OR TW-432894-B OR TW-200417949-A OR TW-508974-B OR JP-5376734-B2 OR US-8927994-B2 OR JP-5376738-B2 OR US-20090127559-A1 OR TW-200401455-A OR TW-200303504-A OR US-20150108515-A1 OR US-6958740-B1 OR JP-2014078027-A OR	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO))	OR	ON	ON	2022/10/08 07:23 PM

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		JP-2013061667-A) did.					
L93	45	(Artificial Intelligence) Similar to: 17/871,618 with 0 CPC Selections and 0 Text Selections Text: (TW-200721098-A OR TW-200707382-A OR TW-I272556-B OR EP-1720148-A3 OR US-20120261667-A1 OR CN-101043770-A OR US-20090315032-A1 OR KR-20050121697-A OR US-7989808-B2 OR TW-432894-B OR US-8471259-B2 OR US-20050218452-A1 OR US-20110278578-A1 OR JP-2012230383-A OR US-7554116-B2 OR CN-1858838-A OR CN-1858838-B OR US-9165991-B2 OR JP-2000173779-A OR JP-5648140-B2 OR CN-101847362-B OR CN-1511432-A OR JP-5376734-B2 OR US-8927994-B2 OR JP-4395367-B2 OR CN-101847362-A OR JP-2004522283-A OR JP-2014044441-A OR KR-20060114650-A OR EP-1720148-A2 OR US-7623091-B2 OR US-20060244391-A1 OR JP-5376738-B2 OR KR-101222539-B1 OR US-8207537-B2 OR US-20150108515-A1 OR US-7102281-B2 OR US-20170186780-A1 OR JP-3423232-B2 OR JP-2014078027-A OR CN-100487780-C OR KR-20010050803-A OR US-20210327986-A1 OR JP-5005051-B2 OR JP-2010166063-A OR KR-101247222-B1 OR KR-100453634-B1 OR EP-2264690-A1 OR KR-100768392-B1 OR KR-20000035710-	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO))	OR	ON	ON	2022/10/08 08:33 PM

		A).did.					
L94	15	((curv$5 bent bend$5) WITH ((channel NEAR (layer region portion section part)) (semiconductor NEAR layer)) WITH (under over below beneath underneath) WITH (capacitor NEAR (plate electrode)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/08 08:43 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N1	1	(((curv$5 bent bend$5) WITH ((channel NEAR (layer region portion section part)) (semiconductor NEAR layer))) AND ((under over below beneath underneath) WITH (gate NEAR electrode) WITH cover$5 WITH (capacitor NEAR (plate electrode)))).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 07:21 PM
N2	2	(((curv$5 bent bend$5) WITH ((channel NEAR (layer region portion section part)) (semiconductor NEAR layer)) WITH (under over below beneath underneath) WITH (capacitor NEAR (plate electrode)))).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2022/10/08 08:55 PM

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17871618
Filing Date	2022-07-22
First Named Inventor	Se-Ho Kim
Art Unit	2892
Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
Attorney Docket Number	224721/411598-06509

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9660012	B2	2017-05-23	Kim et al.	
	2	9899464	B2	2018-02-20	Kim et al.	
	3	10985234	B2	2021-04-20	Kim et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17871618
	Filing Date	2022-07-22
	First Named Inventor	Se-Ho Kim
	Art Unit	2892
	Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
	Attorney Docket Number	224721/411598-06509

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NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	US Office Action dated September 2, 2022, issued in US Patent Application No. 17/853368 (6 pages)	
	2	US Office Action dated September 2, 2022, issued in US Patent Application No. 17/853551 (9 pages)	
	3	US Office Action dated September 14, 2022, issued in US Patent Application No. 17/853451 (7 pages)	
	4	US Notice of Allowance dated October 4, 2022, issued in US Patent Application No. 17/853368 (7 pages)	
	5	US Notice of Allowance dated October 4, 2022, issued in US Patent Application No. 17/853551 (7 pages)	
	6	US Notice of Allowance dated October 20, 2022, issued in US Patent Application No. 17/853451 (7 pages)	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

EFS Web 2.1.18

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17871618
	Filing Date	2022-07-22
	First Named Inventor	Se-Ho Kim
	Art Unit	2892
	Examiner Name	MALSAWMA, LALRINFAMKIM HMAR
	Attorney Docket Number	224721/411598-06509

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Peter Hsueh/	Date (YYYY-MM-DD)	2022-10-20
Name/Print	Peter Hsueh	Registration Number	45574

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	17871618
Filing Date:	22-Jul-2022
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION
First Named Inventor/Applicant Name:	Se-Ho Kim
Filer:	Peter C. Hsueh/Elizabeth Gomez
Attorney Docket Number:	224721/411598-06509

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

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Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

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Electronic Acknowledgement Receipt	
EFS ID:	46864031
Application Number:	17871618
International Application Number:	
Confirmation Number:	1880
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION
First Named Inventor/Applicant Name:	Se-Ho Kim
Customer Number:	23363
Filer:	Peter C. Hsueh/Elizabeth Gomez
Filer Authorized By:	Peter C. Hsueh
Attorney Docket Number:	224721/411598-06509
Receipt Date:	20-OCT-2022
Filing Date:	22-JUL-2022
Time Stamp:	23:26:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$260
RAM confirmation Number	E20220JN26473093
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	224721_IDS.pdf	1042185 4baaa81ceff58680c38d1cb8b03f16982c9d13ce	no	4
Warnings:					
Information:					
2	Other reference-Patent/Application/ Search Documents	9-2-22_OA_224005.pdf	400343 5158daaa213dcb54e8bb407c465b88ef56aa7d4b	no	6
Warnings:					
Information:					
3	Other reference-Patent/Application/ Search Documents	9-2-22_OA_224007.pdf	547827 25b356bea36e8b0846a7dac23175b86b95a6c835	no	9
Warnings:					
Information:					
4	Other reference-Patent/Application/ Search Documents	9-14-22_OA_224006.pdf	436988 cb1f58baff50f28582d9645c347cb8bc201bb171	no	7
Warnings:					
Information:					
5	Other reference-Patent/Application/ Search Documents	10-4-22_NOA_224005.pdf	645936 70c5c2d75d5e7b08eea0d867cf6b53df2ef99e93	no	7
Warnings:					
Information:					
6	Other reference-Patent/Application/ Search Documents	10-4-22_NOA_224007.pdf	641521 701864ede4f3b9d85f666c751902d7be9f5df354	no	7
Warnings:					
Information:					

BOE v. Samsung IPR2025-01479
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7	Other reference-Patent/Application/ Search Documents	10-20-22_NOA_224006.pdf	640155 c1f3b8d11d36ffcd8a374655cb1d8a2296351a76	no	7
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	38385 df24b626896937fa3df21716fabfd53db75b7766	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	4393340		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

BOE v. Samsung IPR2025-01479
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Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/25 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION**
Application Number	17871618
Filing Date	22-Jul-2022
First Named Inventor	Se-Ho Kim
Attorney Docket Number	224721/411598-06509
Title of Invention	ORGANIC LIGHT EMITTING DIODE DISPLAY

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Samsung Display Co., Ltd.	100%

The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)

17853551 filed on 06/29/2022

as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

BOE v. Samsung IPR2025-01479
Ex-1002

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ○ Small Entity ○ Micro Entity ◉ Regular Undiscounted I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number 71165 ○ A sole inventor ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ○ A joint inventor; all of whom are signing this request	
Signature	/Kyle W Kellar/
Name	Kyle W. Kellar

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

BOE v. Samsung IPR2025-01479
Ex-1002

Electronic Patent Application Fee Transmittal

Application Number:	17871618
Filing Date:	22-Jul-2022
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Se-Ho Kim
Filer:	Kyle W. Kellar/Marti Carrillo
Attorney Docket Number:	224721/411598-06509

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	170	170
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

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Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**170**

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Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 17871618

Filing Date: 22-Jul-2022

Applicant/Patent under Reexamination: Kim

Electronic Terminal Disclaimer filed on September 29, 2022

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

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Electronic Acknowledgement Receipt	
EFS ID:	46723390
Application Number:	17871618
International Application Number:	
Confirmation Number:	1880
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Se-Ho Kim
Customer Number:	23363
Filer:	Kyle W. Kellar/Marti Carrillo
Filer Authorized By:	Kyle W. Kellar
Attorney Docket Number:	224721/411598-06509
Receipt Date:	29-SEP-2022
Filing Date:	22-JUL-2022
Time Stamp:	15:41:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$170
RAM confirmation Number	E20229SF41051148
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	43757 7779d5ab8c0f19ae60fad8d802ab341c2357904c	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37835 4cecb9fa94a2fa07e1b9e5b2b8008e2bd4321161	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	81592		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on September 29, 2022 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Marti Carrillo/
Marti Carrillo

Appl No.	: 17/871,618	Confirmation No. 1880
Inventor	: Se-Ho Kim, et al.	
Filed	: July 22, 2022	
Title	: ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION (as amended)	
TC/A.U.	: 2892	
Examiner	: Lalrinfamkim Hmar Malsawma	
Docket No.	: 224721	
Customer No.	: 23363	

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
September 29, 2022

Commissioner:

This paper is in response to the Office action of September 16, 2022, which set an initial period for reply to expire on December 16, 2022. Any extension of time fee required by this paper is paid concurrently herewith. As such, this response is timely filed. Please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

A Listing of the Claims begins on page 3 of this paper.

Remarks/Arguments begin on page 11 of this paper.

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Amendments to the Specification:

Please amend the title on page 1 as follows:

-- ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION --

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Listing of Claims:

1. (Original) An organic light emitting diode display comprising:

a non-conductive substrate;

a plurality of first voltage lines;

a plurality of scan lines;

a plurality of data lines;

a plurality of driving circuits formed on the substrate;

a plurality of organic light emitting diodes, wherein each of the plurality of organic light emitting diodes is electrically coupled to a respective one of the plurality of driving circuits;

wherein each of the driving circuits comprises:

a first thin film transistor implemented in a first portion of a semiconductor layer disposed on the substrate, and coupled to one of the plurality of scan lines and to one of the plurality of data lines;

a second thin film transistor implemented in a second portion of the semiconductor layer, wherein the semiconductor layer couples the second thin film transistor to the first thin film transistor, and wherein the second portion of the semiconductor layer has at least one bent portion;

a storage capacitor comprising:

a first capacitor plate that is configured to operate as the gate electrode of the second thin film transistor;

a second capacitor plate electrically coupled to one of the plurality of first voltage lines and overlapping the first capacitor plate; and

an insulating layer between the first capacitor plate and the second capacitor plate;

a third thin film transistor implemented in a third portion of the semiconductor layer, wherein the semiconductor layer couples the third thin film

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transistor to the first thin film transistor and to the second thin film transistor, and wherein the third thin film transistor is electrically coupled to one of the plurality of first voltage lines through the semiconductor layer; and

a fourth thin film transistor implemented in a fourth portion of the semiconductor layer, wherein the semiconductor layer couples the fourth thin film transistor to the second thin film transistor, and wherein the fourth thin film transistor is electrically coupled to the respective organic light emitting diode through the semiconductor layer; and

wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate.

2. (Original) An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

3. (Original) An organic light emitting diode display according to claim 2, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor electrically coupled to the first capacitor plate; and

a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,

wherein the sixth thin film transistor is coupled to the fifth thin film transistor.

4. (Original) An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

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5. (Original) An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

6. (Original) An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

7. (Original) An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode,

wherein the seventh thin film transistor is coupled to the fourth thin film transistor.

8. (Original) An organic light emitting diode display according to claim 4, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

9. (Original) An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.

10. (Original) An organic light emitting diode display according to claim 2, further comprising:

a plurality of second voltage lines;

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a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

a sixth thin film transistor implemented in a sixth portion of the semiconductor layer,

wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and

wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

11. (Original) An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

12. (Original) An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

13. (Original) An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

14. (Original) An organic light emitting diode display according to claim 11, further comprising a seventh thin film transistor implemented in a sixth portion of the semiconductor layer,

wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

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wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

15. (Original) An organic light emitting diode display according to claim 11, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

16. (Original) An organic light emitting diode display according to claim 1, wherein a periphery of the first capacitor plate completely surrounds a periphery of the second capacitor plate in a plan view.

17. (Original) An organic light emitting diode display according to claim 1, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor electrically coupled to the first capacitor plate; and

a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,

wherein the sixth thin film transistor is coupled to the fifth thin film transistor.

18. (Original) An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

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19. (Original) An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

20. (Original) An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

21. (Original) An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode,

wherein the seventh thin film transistor is coupled to the fourth thin film transistor.

22. (Original) An organic light emitting diode display according to claim 18, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

23. (Original) An organic light emitting diode display according to claim 1, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

a sixth thin film transistor implemented in a sixth portion of the semiconductor layer, wherein the semiconductor layer couples the sixth thin film transistor to the fifth

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thin film transistor, and wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

24. (Original) An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

25. (Original) An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

26. (Original) An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

27. (Original) An organic light emitting diode display according to claim 24, further comprising a seventh thin film transistor implemented in a sixth portion of the semiconductor layer,

wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

28. (Original) An organic light emitting diode display according to claim 24, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of

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second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

29. (Original) An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.

30. (Original) An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

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REMARKS/ARGUMENTS

Claims 1-30 remain in the present application, of which claim 1 is independent. No claims are amended herein. Applicant respectfully requests reconsideration and allowance of claims 1-30.

Objection to the Title

The title is objected to as allegedly not being descriptive. Without acquiescing to the propriety of the rejection, and solely to expedite allowance, the title is amended herein as suggested at page 2 of the Office action.

Double Patenting Rejections

Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 16, 17, 18, 19, 20, 21, 23, 24, 25, 26 and 27 were provisionally rejected on the ground of nonstatutory double patenting as allegedly being unpatentable over claims 1, 8, 8, (8+26), (8+26), (8+26), (8+26+12), (8+26), (8+26), (8+26), (8+26+4), (8+26+12), 8, 1, 26, 26, 26, 26, 1, 26, 26, 26 and 26, respectively, of co-pending U.S. Patent Application No. 17/853,551.

Without acquiescing to the propriety of the rejection, and solely to expedite allowance, a Terminal Disclaimer over co-pending U.S. Patent Application No. 17/853,551 is being filed concurrently herewith. Accordingly, Applicant respectfully requests that these double patenting rejection be withdrawn and claims 1-30 be allowed.

Concluding Remarks

In view of the foregoing amendments and remarks, Applicant earnestly solicits a timely issuance of a Notice of Allowance with claims 1-30. If there are any remaining issues that can be addressed over the telephone, the Examiner is cordially invited to call Applicant's attorney at the number listed below.

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Payment of any fee required to enter and process this response is provided. The Director is authorized to charge any underpayment of fees or credit any overpayment of fees to Deposit Account No. 03-1728.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By */Kyle W. Kellar/*
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/mac

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Electronic Acknowledgement Receipt

EFS ID:	46723711
Application Number:	17871618
International Application Number:	
Confirmation Number:	1880
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Se-Ho Kim
Customer Number:	23363
Filer:	Kyle W. Kellar/Marti Carrillo
Filer Authorized By:	Kyle W. Kellar
Attorney Docket Number:	224721/411598-06509
Receipt Date:	29-SEP-2022
Filing Date:	22-JUL-2022
Time Stamp:	15:48:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		224721_Amendment.pdf	123807 c3fed63dcbf90d1739a7ce423949dad796c8b7e4	yes	12

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	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Request for Reconsideration-After Non-Final Rejection	1	1
	Specification	2	2
	Claims	3	10
	Applicant Arguments/Remarks Made in an Amendment	11	12
Warnings:			
Information:			
	Total Files Size (in bytes):	123807	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PTO/SB/06 (09-11)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/871,618	Filing Date 07/22/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	09/29/2022	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 30	Minus	** 30	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/MARCUS A PRIDGEN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

23363 7590 09/16/2022

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	

ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
09/16/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PLPrivatePair@lrrc.com
pto@lewisroca.com

Office Action Summary	Application No. 17/871,618	Applicant(s) Kim et al.	
	Examiner LEX H MALSAWMA	Art Unit 2892	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 07/22/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-30 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-7,10-14,16-21 and 23-27 is/are rejected.

8) ☑ Claim(s) 8-9,15,22 and 28-30 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☑ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 07/22/2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 07/22/2022.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. For example, a more descriptive title could be, "ORGANIC LIGHT EMITTING DIODE DISPLAY WITH SEMICONDUCTOR LAYER HAVING BENT PORTION".

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

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A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 *et seq.* for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

4. Claims 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 16, 17, 18, 19, 20, 21, 23, 24, 25, 26 and 27 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 8, 8, (8+26), (8+26), (8+26), (8+26+12), (8+26), (8+26), (8+26), (8+26+4), (8+26+12), 8, 1, 26, 26, 26, 26, 1, 26, 26, 26 and 26, respectively, of copending Application No. 17/853,551 (reference application).

Although the claims at issue are not identical, they are not patentably distinct from each other because the current claims are essentially broader in scope than the corresponding claims in

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the reference application. Specifically, current claim 1 does not require fifth and sixth thin film transistors are recited in claim 1of the reference application. Also, the recitation of "a plurality of" first voltage lines, scan lines, and data lines in current claim 1, are deemed obvious variants of claim 1 of the reference application because a typical display requires numerous voltage lines, scan lines and data lines. Furthermore, the recitation, in current claim 1, of the semiconductor layer has at least one bent portion, is deemed to be essentially the same as the recitation, in claim 1 of the reference application, of the semiconductor layer…being curved. Lastly, in both the current application and the reference application, all thin film transistors and other parts are considered to be coupled and/or electrically coupled, especially because the thin film transistors and capacitor would be part of the same display that comprises a common ground.

Specifically, with regard to current claims 4-7 and 10-14, these claims are deemed obvious variants of a combination of claims 8, 26 and 12 (or 4) of the referenced application.

Therefore, given the reference application, one of ordinary skill in the art would have deemed the invention of the current claims to be an obvious variant of the invention in the corresponding claims of the reference application.

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Allowable Subject Matter

5. Claims 8, 9, 15, 22, and 28-30 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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6. The following is a statement of reasons for the indication of allowable subject matter:

Claim 8 is allowed primarily because the prior art of record cannot anticipate or render obvious the limitations in this claim (when combined with claim 4);

Claim 9 is allowed primarily because the prior art of record cannot anticipate or render obvious the limitations in this claim (when combined with claim 3);

Claim 22 is allowed primarily because the prior art of record cannot anticipate or render obvious the limitations in this claim (when combined with claim 18);

Claim 28 is allowed primarily because the prior art of record cannot anticipate or render obvious the limitations in this claim (when combined with claim 24); and

Claims 29-30 are allowed primarily because the prior art of record cannot anticipate or render obvious the limitations in claim 29 (when combined with claim 24, and claim 30 depends from claim 29).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEX H MALSAWMA whose telephone number is (571)272-1903. The examiner can normally be reached M-F (4-12 Hours, between 5:30AM-10PM).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le can be reached on 571-272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/LEX H MALSAWMA/
Primary Examiner, Art Unit 2892

BOE v. Samsung IPR2025-01479
Ex-1002

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/871,618	Kim et al.
	Examiner	Art Unit
	LEX H MALSAWMA	2892

CPC - Searched*		
Symbol	Date	Examiner
H01L 27/3276, 3248, 3258, 3262, 3265, 124, 1255	08/27/2022	LHM.
G09G 3/3225	08/27/2022	LHM
G09G 2300/0809	08/27/2022	LHM

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
H01L 27/3276, 3248, 3258, 3262, 3265, 124, 1255 (text limited, see PE2E SEARCH)	08/27/2022	LHM
G09G 3/3225 (text limited, see PE2E SEARCH)	08/27/2022	LHM
G09G 2300/0809 (text limited, see PE2E SEARCH)	08/27/2022	LHM
USPC 257/40 cross reference search	08/27/2022	LHM
Inventor and assignee search	08/27/2022	LHM
PE2E SEARCH	09/10/2022	LHM

/LEX H MALSAWMA/ Primary Examiner, Art Unit 2892	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	LEX H MALSAWMA	2892

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/LEX H MALSAWMA/ Primary Examiner, Art Unit 2892	

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/871,618	Kim et al.
	Examiner	Art Unit
	LEX H MALSAWMA	2892

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	09/10/2022								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	O								
	9	O								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	O								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								
	21	✓								
	22	O								
	23	✓								
	24	✓								
	25	✓								
	26	✓								
	27	✓								
	28	O								
	29	O								
	30	O								

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224721
	Application Number	To Be Determined
	Filing Date	July 22, 2022
	Inventor(s)	Se-Ho Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - Kind Code[2] (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		5,929,464 A	07-27-1999	Yamazaki et al.
		6,104,067 A	08-15-2000	Zhang et al.
		6,914,642 B2	07-05-2005	Yamazaki et al.
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		10,347,183 B2	07-09-2019	Takahara et al.
		10,453,395 B2	10-22-2019	Takahara et al.

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

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BOE v. Samsung IPR2025-01479
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
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	Application Number	To Be Determined
	Filing Date	July 22, 2022
	Inventor(s)	Se-Ho Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - Kind Code[2] (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		10,483,342 B2	11-19-2019	Kim et al.
		10,553,158 B2	02-04-2020	Takahara et al.
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		2012/0146004 A1	06-14-2012	Lee et al.

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		2014/0098078 A1	04-10-2014	Jeon et al.

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EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (✓)
		CN 1917205 A	02-21-2007	Yoshiharu	Abstract and Corresponds to U.S. Publication 2007/0040193 A1 listed above
		CN 101110422 A	01-23-2008	Sato	Abstract, and Corresponds to U.S. Publication 2008/0017866 A1, listed above
		CN 101673508 A	03-17-2010	Mitsuaki et al.	Abstract
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		CN 102194404 A	09-21-2011	Samsung Mobile Display Co., Ltd	Abstract
		CN 102386209 A	03-21-2012	AU OPTRONICS +	Espacenet Engliish Abstract

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		JP 2008-46619 A	02-28-2008	Sato	Japan Patent Abstract
		JP 2010-19950 A	01-28-2010	Seiko Epson Corp	Abstract
		JP 4452075 B2	02-05-2010	Takahara et al.	Corresponds to USP 9,728,130 B2 listed above
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		JP 2012-14136 A	01-19-2012	Jeong et al.	Japan Patent Abstract
		JP 2012-133170 A	07-12-2012	Mochizuki	Japan Patent Abstract

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		KR 10-1999-0066077	08-16-1999	Kim	English Abstract
		KR 10-2009-0119599	11-19-2009	Koo et al.	Korean Patent Abstracts
		KR 10-0297868 B1	10-24-2001	Yamazaki et al.	Corresponds to US Pat. No. 6,914,642 B2 listed above
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		KR 10-1176540 B1	08-24-2005	Yin et al.	Corresponds to USP 7,859,054 listed above
		KR 10-2007-0074748 A	07-18-2007	Takashi et al.	Korean Patent Abstracts
		KR 10-1056233B1	08-11-2011	Bae et al.	Corresponds to US Publ No. 2013/0075766 A1 listed above
		KR 10-1839533 B1	03-19-2018	Park	Corresponds to USP 8,717,259 listed above
		WO 2007/111202 A1	10-04-2007	Ochi	
		WO 2009/056877 A1	05-07-2009	Rankov et al.	

OTHER DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		SIPO Office Action dated December 14, 2016, for corresponding Chinese Patent Application No. 201310331836.5 (5 pages)
		JPO Office Action dated December 20, 2016, for corresponding Japanese Patent Application No. 2013-026588 (8 pages)

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	Examiner Name	To Be Determined

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		Korean Patent Abstract, Publication No. 10-2000-0038925 A, dated 05-07-2000 for corresponding Korean Patent 10-0439944 listed above (2 pages)
		European Search Report dated October 28, 2015, for corresponding European Patent Application No. 13179090.9 (9 pages)
		European Search Report dated November 12, 2015, for corresponding European Patent Application No. 13179091.7 (10 pages)
		EPO Office Action dated December 5, 2017, for corresponding European Patent Application No. 13179090.9 (4 pages)

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07/22/22 11:17AM

EXAMINER SIGNATURE	/LEX H MALSAWMA/	DATE CONSIDERED	09/09/2022

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

JEJ/smv

Sheet 6 of 6

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.H.M./

BOE v. Samsung IPR2025-01479
Ex-1002

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	0	17/853,551	(US-PGPUB; USPAT)	OR	ON	ON	2022/08/22 03:18 PM
L2	21	"10985234" "10734470" "10483342" "10204976" "9899464" "9660012" "94500040"	(US-PGPUB; USPAT)	OR	ON	ON	2022/08/22 03:19 PM
L3	20	("5929464" | "6914642" | "20030222589" | "20040155242" | "20060082524" | "20070040193" | "20070159565" | "20080017866" | "20080129664" | "20100079361" | "20100253710" | "20120146004" | "20120313100" | "20140027728" | "20140070184" | "20140077176" | "20140098078").pn. OR ("9660012").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/08/22 03:35 PM
L4	56	("10134336" OR "10198992" OR "10198993" OR "10204976" OR "10347183" OR "10453395" OR "10483342" OR "10553158" OR "10699639" OR "10734470" OR "10818235" OR "10923030" OR "11302253" OR "20020149711" OR "20030222589" OR "20040155242" OR "20060082524" OR "20070040193" OR "20070159565" OR "20080017866" OR "20080129664" OR "20100079361" OR "20100253710" OR "20110227893" OR "20110273419" OR "20120026146" OR "20120097965" OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/08/22 04:17 PM

		"20120146004" OR "20120162275" OR "20120313100" OR "20130075766" OR "20130201172" OR "20130334508" OR "20140001445" OR "20140027728" OR "20140070184" OR "20140077176" OR "20140098078" OR "5929464" OR "6104067" OR "6914642" OR "7576354" OR "7649202" OR "7859054" OR "7999322" OR "8309404" OR "8717259" OR "8878827" OR "9287528" OR "9450040" OR "9501978" OR "9728130" OR "9892683" OR "9922597" OR "9959809" OR "9997108").pn.					
L5	774	((("KIM") near3 ("Se-Ho")) OR (("PARK") near3 ("Jin-Woo")) OR (("LEE") near3 ("Won-Se"))).INV.	(US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT)	OR	ON	ON	2022/08/22 07:49 PM
L6	20099	((("SAMSUNG") near3 ("DISPLAY") near3 ("CO") near3 ("LTD"))).AS,AANM.	(USPAT)	OR	ON	ON	2022/08/23 06:00 AM
L7	14	"10985234" "10734470" "10483342" "10204976" "9899464" "9660012" "94500040"	(USPAT)	OR	ON	ON	2022/08/23 06:08 AM
L8	6	("10985234" "10734470" "10483342" "10204976" "9899464" "9660012" "94500040").pn.	(USPAT)	OR	ON	ON	2022/08/23 06:08 AM
L9	7	("10985234" "10734470" "10483342" "10204976" "9899464" "9660012" "9450040").pn.	(USPAT)	OR	ON	ON	2022/08/23 06:09 AM
L10	7	("10985234" "10734470" "10483342" "10204976" "9899464" "9660012"	(USPAT)	OR	ON	ON	2022/08/23 06:09 AM

		"9450040").pn.					
L11	3	16/984,045	(US-PGPUB; USPAT)	OR	ON	ON	2022/08/27 01:06 PM
L12	1491	(L5 L6) AND ((curv$5 bend$4 bent) WITH channel)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:43 PM
L13	430	(L5 L6) AND ((curv$5 bend$4 bent) near2 channel)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:43 PM
L14	188	L12 AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:45 PM
L15	74433	H01L27/3276.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:56 PM
L16	29243	H01L27/3248.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO);	OR	ON	ON	2022/08/27 01:57 PM

			FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L17	31379	H01L27/3258.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:57 PM
L18	47157	H01L27/3262.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:57 PM
L19	16523	H01L27/3265.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:57 PM
L20	86517	H01L27/124.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:57 PM
L21	34202	H01L27/1255.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO;	OR	ON	ON	2022/08/27 01:57 PM

			DERWENT; IBM_TDB)				
L22	35153	G09G3/3225.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:58 PM
L23	19048	G09G2300/0809.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:58 PM
L24	28344	257/40.ccls.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:58 PM
L25	459	H01L25/046.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:58 PM
L26	2340	H01L27/28.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:58 PM

L27	12184	H01L51/00.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:59 PM
L28	2741	H01L2031/0344.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:59 PM
L29	8	H01L2251/00.cpc.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 01:59 PM
L30	281	(L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 L26 L27 L28 L29 L15) AND ((curv$5 bend$4 bent) WITH channel) AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 02:00 PM
L31	112	L30 NOT L14	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/08/27 02:00 PM
L32	27	(Artificial Intelligence)	(US-PGPUB; USPAT;	OR	ON	ON	2022/08/27

		More like doc: US-9660012-B2 Text: (US-20140034923-A1 OR EP-2693482-A2 OR US-9899464-B2 OR US-20170256601-A1 OR US-9450040-B2 OR EP-2693482-B1 OR EP-2693481-A2 OR EP-2693481-B1 OR TW-201411832-A OR US-20200365678-A1 OR EP-3780112-A1 OR US-20160358995-A1 OR US-20210242296-A1 OR US-10985234-B2 OR TW-I605582-B OR US-20190157376-A1 OR US-20180175134-A1 OR US-10483342-B2 OR US-10204976-B2 OR KR-20140018623-A).did.	USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				05:06 PM
L33	20	("5929464" | "6914642" | "20030222589" | "20040155242" | "20060082524" | "20070040193" | "20070159565" | "20080017866" | "20080129664" | "20100079361" | "20100253710" | "20120146004" | "20120313100" | "20140027728" | "20140070184" | "20140077176" | "20140098078").pn. OR ("9660012").urpn. AND (PGPB | USPT | USOC).dbnm.	(US-PGPUB; USPAT; USOCR)	OR	ON	ON	2022/08/27 05:07 PM
L34	56	("10134336" OR "10198992" OR "10198993" OR "10204976" OR "10347183" OR "10453395" OR "10483342" OR "10553158" OR "10699639" OR "10734470" OR "10818235" OR "10923030" OR "11302253" OR	(US-PGPUB; USPAT)	OR	ON	ON	2022/08/27 11:06 PM

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Ex-1002

		"20020149711" OR "20030222589" OR "20040155242" OR "20060082524" OR "20070040193" OR "20070159565" OR "20080017866" OR "20080129664" OR "20100079361" OR "20100253710" OR "20110227893" OR "20110273419" OR "20120026146" OR "20120097965" OR "20120146004" OR "20120162275" OR "20120313100" OR "20130075766" OR "20130201172" OR "20130334508" OR "20140001445" OR "20140027728" OR "20140070184" OR "20140077176" OR "20140098078" OR "5929464" OR "6104067" OR "6914642" OR "7576354" OR "7649202" OR "7859054" OR "7999322" OR "8309404" OR "8717259" OR "8878827" OR "9287528" OR "9450040" OR "9501978" OR "9728130" OR "9892683" OR "9922597" OR "9959809" OR "9997108").pn.					
L35	0	17/853,451	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/07 02:38 PM
L36	188	L12 AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/07 02:39 PM
L37	281	(L16 L17 L18 L19 L20	(US-PGPUB; USPAT;	OR	ON	ON	2022/09/07

		L21 L22 L23 L24 L25 L26 L27 L28 L29 L15) AND ((curv$5 bend$4 bent) WITH channel) AND (third near2 (TFT (thin ADJ film)))	USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				02:39 PM
L38	0	17/781,618	(US-PGPUB; USPAT)	OR	ON	ON	2022/09/10 11:28 AM
L39	282	(L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 L26 L27 L28 L29 L15) AND ((curv$5 bend$4 bent) WITH channel) AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/10 12:42 PM
L40	189	L12 AND (third near2 (TFT (thin ADJ film)))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/10 12:43 PM
L41	20	L12 AND (third NEAR (metal ADJ layer))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/10 03:33 PM
L42	564	(third NEAR (metal ADJ layer)) AND ((contact ADJ (hole opening)) WITH through WITH capacitor WITH (plate electrode))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/10 03:59 PM

L43	1100	((thin ADJ film ADJ transistor) TFT) WITH (electrical$2 NEAR (coupl$3 connect$3)) WITH (contact ADJ (hole opening)) WITH through WITH capacitor WITH (plate electrode)	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/10 04:01 PM
L44	135	L43 AND (six$4 WITH ((thin ADJ film) TFT))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/09/10 04:02 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

UNITED STATES PATENT AND TRADEMARK OFFICE

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BIB DATA SHEET

CONFIRMATION NO. 1880

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
17/871,618	07/22/2022	257	2892	224721/411598-06509

APPLICANTS

SAMSUNG DISPLAY CO., LTD., Yongin-si, KOREA, REPUBLIC OF;

INVENTORS

Se-Ho Kim, Yongin-si, KOREA, REPUBLIC OF;
Jin-Woo Park, Yongin-si, KOREA, REPUBLIC OF;
Won-Se Lee, Yongin-si, KOREA, REPUBLIC OF;

**** CONTINUING DATA ***************************

This application is a CON of 17/234,670 04/19/2021
which is a CON of 16/984,045 08/03/2020 PAT 10985234
which is a CON of 16/659,372 10/21/2019 PAT 10734470
which is a CON of 16/261,450 01/29/2019 PAT 10483342
which is a CON of 15/900,715 02/20/2018 PAT 10204976
which is a CON of 15/603,309 05/23/2017 PAT 9899464
which is a CON of 15/238,449 08/16/2016 PAT 9660012
which is a CON of 13/952,508 07/26/2013 PAT 9450040

**** FOREIGN APPLICATIONS ***************************

REPUBLIC OF KOREA 10-2012-0084976 08/02/2012

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

08/01/2022

Foreign Priority claimed ☑ Yes ☐ No 35 USC 119(a-d) conditions met ☑ Yes ☐ No Verified and Acknowledged /LEX HMAR MALSAWMA/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		KOREA, REPUBLIC OF	11	30	1

ADDRESS

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001
UNITED STATES

TITLE

ORGANIC LIGHT EMITTING DIODE DISPLAY

FILING FEE RECEIVED		
2820	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

BOE v. Samsung IPR2025-01479
Ex-1002

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UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/871,618	07/22/2022	Se-Ho Kim	224721/411598-06509	1880

23363 7590 08/23/2022
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

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PTOL-90A (Rev. 04/07)

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Decision Granting Request for Prioritized Examination (Track I)	**Application No.** 17/871,618	**Applicant(s)** Kim et al.	
	Examiner FIKIRTE A GEREMEW	**Art Unit** OMBL	**AIA (FITF) Status** No

1. THE REQUEST FILED 22 July 2022 IS **GRANTED** .

The above-identified application has met the requirements for prioritized examination

A. ☑ for an original nonprovisional application (Track I).
B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination**. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

A. filing a **petition for extension of time** to extend the time period for filing a reply;

B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims** , or a multiple dependent claim;

C. filing a **request for continued examination** ;

D. filing a notice of appeal;

E. filing a request for suspension of action;

F. mailing of a notice of allowance;

G. mailing of a final Office action;

H. completion of examination as defined in 37 CFR 41.102; or

I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to FIKIRTE GEREMEW at (703) 756-1930. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.

/FIKIRTE A GEREMEW/ PROGRAM SUPPORT ASSISTANT, OMBL	

U.S. Patent and Trademark Office
PTO-2298 (Rev. 02-2012)

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대 한 민 국 특 허 청
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This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

출 원 번 호 : 10-2012-0084976
Application Number

출 원 년 월 일 : 2012년 08월 02일
Filing Date Aug. 02, 2012

출 원 인 : 삼성디스플레이 주식회사
Applicant(s) Samsung Display Co., Ltd.

2022년 08월 04일

특 허 청
COMMISSIONER

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제출 일자 : 2012-08-02

【서지사항】

【서류명】 특허출원서

【참조번호】 3553

【출원구분】 특허출원

【출원인】

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【특허고객번호】 1-2012-016455-2

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【대리인번호】 9-2007-100081-9

【지정된변리사】 김동명, 민기원, 김재만

【포괄위임등록번호】 2012-029467-3

【발명의 국문명칭】 유기 발광 표시 장치

【발명의 영문명칭】 ORGANIC LIGHT EMITTING DIODE DISPLAY

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【심사청구】 청구

【취지】 위와 같이 특허청장에게 제출합니다.

대리인 팬코리아특허법인 (서명 또는 인)

【수수료】

【출원료】 0 면 38,000 원

【가산출원료】 58 면 0 원

【우선권주장료】 0 건 0 원

【심사청구료】 20 항 930,000 원

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【합계】 968,000 원

【수수료 자동납부번호】 064-094949-04-013

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【발명의 설명】

【발명의 명칭】

유기 발광 표시 장치{ORGANIC LIGHT EMITTING DIODE DISPLAY}

【기술분야】

【0001】 본 발명은 유기 발광 표시 장치에 관한 것이다.

【발명의 배경이 되는 기술】

【0002】 유기 발광 표시 장치는 두 개의 전극과 그 사이에 위치하는 유기 발광층을 포함하며, 하나의 전극으로부터 주입된 전자(electron)와 다른 전극으로부터 주입된 정공(hole)이 유기 발광층에서 결합하여 여기자(exciton)를 형성하고, 여기자가 에너지를 방출하면서 발광한다.

【0003】 이러한 유기 발광 표시 장치는 자발광 소자인 유기 발광 다이오드를 포함하는 복수개의 화소를 포함하며, 각 화소에는 유기 발광 다이오드를 구동하기 위한 복수개의 박막 트랜지스터 및 캐패시터(Capacitor)가 형성되어 있다. 복수개의 박막 트랜지스터는 기본적으로 스위칭 박막 트랜지스터 및 구동 박막 트랜지스터를 포함한다.

【0004】 스위칭 박막 트랜지스터는 빠른 스위칭 동작을 위해 게이트 전극과 반도체층 사이에 얇은 두께의 게이트 절연막을 형성한다. 이 때, 스위칭 박막 트랜지스터와 동일한 층에 형성되는 구동 박막 트랜지스터의 게이트 절연막의 두께도 얇아지므로 구동 박막 트랜지스터의 게이트 전극에 인가되는 게이트 전압의 구동

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범위(driving range)는 좁아지게 된다. 따라서, 구동 박막 트랜지스터의 게이트 전압(Vgs)의 크기를 조절하여 풍부한 계조를 가지도록 제어하기 어렵다.

【발명의 내용】

【해결하고자 하는 과제】

【0005】본 발명은 전술한 배경 기술의 문제점을 해결하기 위한 것으로서, 구동 박막 트랜지스터의 구동 범위를 넓혀 풍부한 계조를 표현할 수 있는 유기 발광 표시 장치에 관한 것이다.

【과제의 해결 수단】

【0006】본 발명의 일 실시예에 따른 유기 발광 표시 장치는 기판, 상기 기판 위에 형성되어 있으며 스캔 신호를 전달하는 스캔선, 상기 스캔선과 교차하며 데이터 신호 및 구동 전압을 각각 전달하는 데이터선 및 구동 전압선, 상기 스캔선 및 상기 데이터선과 연결되어 있는 스위칭 박막 트랜지스터, 상기 스위칭 박막 트랜지스터의 스위칭 드레인 전극과 연결되어 있는 구동 박막 트랜지스터, 상기 구동 박막 트랜지스터의 구동 드레인 전극에 연결되어 있는 유기 발광 다이오드를 포함하고, 상기 구동 박막 트랜지스터의 구동 반도체층은 굴곡되어 있을 수 있다.

【0007】상기 구동 반도체층을 덮고 있는 제1 게이트 절연막, 상기 제1 게이트 절연막 위에 형성되어 있으며 상기 구동 반도체층과 중첩하고 있는 스토리지 캐패시터를 더 포함할 수 있다.

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【0008】 상기 스토리지 캐패시터는 상기 제1 게이트 절연막 위에 형성되어 있으며 상기 구동 반도체층과 중첩하고 있는 제1 스토리지 축전판, 상기 제1 스토리지 축전판을 덮고 있는 제2 게이트 절연막, 상기 제2 게이트 절연막 위에 형성되어 있으며 상기 제1 스토리지 축전판과 중첩하고 있는 제2 스토리지 축전판을 포함할 수 있다.

【0009】 상기 구동 반도체층은 복수개의 굴곡부를 포함할 수 있다.

【0010】 상기 구동 반도체층은 제1 방향으로 연장되어 있는 복수개의 제1 연장부와 상기 제1 방향과 다른 제2 방향으로 연장되어 있는 복수개의 제2 연장부를 포함하고, 상기 굴곡부는 상기 제1 연장부와 상기 제2 연장부를 연결할 수 있다.

【0011】 상기 구동 박막 트랜지스터의 문턱 전압을 보상하며 상기 구동 박막 트랜지스터에 연결되어 있는 보상 박막 트랜지스터를 더 포함할 수 있다.

【0012】 발광 제어선에 의해 전달된 발광 제어 신호에 의해 턴온되어 구동 전압을 상기 구동 박막 트랜지스터에서 상기 유기 발광 다이오드로 전달하는 발광 제어 박막 트랜지스터를 더 포함하고, 상기 발광 제어 박막 트랜지스터는 상기 구동 박막 트랜지스터의 구동 드레인 전극과 상기 유기 발광 다이오드 사이에 위치할 수 있다.

【0013】 상기 보상 박막 트랜지스터의 보상 소스 전극과 상기 발광 제어 박막 트랜지스터의 발광 제어 소스 전극은 트랜지스터 연결부를 통해 서로 연결되어 있고, 상기 스토리지 캐패시터는 연장되어 상기 트랜지스터 연결부와 중첩하고 있

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을 수 있다.

【0014】 상기 구동 반도체층은 연장되어 상기 트랜지스터 연결부와 중첩하고 있을 수있다.

【0015】 상기 트랜지스터 연결부는 상기 데이터선과 동일한 층에 형성되어 있으며, 상기 층간 절연막에 형성된 접촉 구멍을 통해 상기 보상 소스 전극과 상기 발광 제어 소스 전극과 연결되어 있을 수 있다.

【0016】 상기 구동 반도체층은 상기 굴곡부에서 분기되는 분기부를 더 포함할 수 있다.

【0017】 상기 스토리지 캐패시터는 연장되어 상기 분기부와 중첩하고 있을 수 있다.

【0018】 상기 구동 반도체층은 상기 보상 박막 트랜지스터와 연결되는 제1 경로 반도체층, 상기 발광 제어 박막 트랜지스터와 연결되는 제2 경로 반도체층을 포함하고, 상기 제1 경로 반도체층의 길이는 상기 제2 경로 반도체층의 길이보다 짧을 수 있다.

【0019】 상기 스토리지 캐패시터는 연장되어 상기 제1 경로 반도체층 및 상기 제2 경로 반도체층과 중첩하고 있을 수 있다.

【0020】 상기 제2 스토리지 축전판을 덮고 있는 층간 절연막, 상기 층간 절연막 위에 형성되어 있으며, 상기 제2 게이트 절연막 및 상기 층간 절연막에 형성된 접촉 구멍을 통해 상기 제1 스토리지 축전판과 연결되어 있는 연결 부재, 상기

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층간 절연막 및 상기 연결 부재를 덮고 있는 보호막을 더 포함하고, 상기 연결 부재는 상기 보상 박막 트랜지스터의 보상 드레인 전극과 연결되어 있을 수 있다.

【0021】 상기 스캔선은 상기 제1 스토리지 축전판과 동일한 층에 형성되어 있고, 상기 데이터선 및 구동 전압선은 상기 연결 부재와 동일한 층에 형성되어 있을 수 있다.

【0022】 상기 구동 전압선은 상기 층간 절연막에 형성된 접촉 구멍을 통해 상기 제2 스토리지 축전판과 연결되어 있을 수 있다.

【0023】 상기 발광 제어선에 의해 전달된 발광 제어 신호에 의해 턴온되어 상기 구동 전압을 상기 구동 박막 트랜지스터로 전달하는 동작 제어 박막 트랜지스터를 더 포함하고, 상기 동작 제어 박막 트랜지스터는 상기 구동 전압선과 상기 구동 박막 트랜지스터의 구동 소스 전극 사이에 위치할 수 있다.

【0024】 이전 스캔선을 통해 전달받은 이전 스캔 신호에 따라 턴 온되어 초기화 전압을 상기 구동 박막 트랜지스터의 구동 게이트 전극에 전달하는 초기화 박막 트랜지스터를 더 포함하고, 상기 초기화 박막 트랜지스터는 상기 초기화 전압선과 상기 구동 박막 트랜지스터의 구동 게이트 전극 사이에 위치할 수 있다.

【0025】 바이패스 제어선에 의해 전달된 바이패스 제어 신호에 의해 상기 구동 박막 트랜지스터가 전달하는 구동 전류의 일부를 바이패스시키는 바이패스 박막 트랜지스터를 더 포함하고, 상기 바이패스 박막 트랜지스터는 상기 초기화 전압선과 상기 발광 제어 박막 트랜지스터의 발광 제어 드레인 전극 사이에 위치할 수 있

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다.

【발명의 효과】

【0026】 본 발명에 따르면, 복수개의 굴곡부를 포함하는 구동 반도체층을 형성함으로써, 구동 반도체층의 구동 채널 영역을 길게 형성할 수 있으므로 구동 게이트 전극에 인가되는 게이트 전압의 구동 범위(driving range)를 넓힐 수 있다.

【0027】 따라서, 게이트 전압의 구동 범위가 넓으므로 게이트 전압의 크기를 변화시켜 유기 발광 다이오드(OLED)에서 방출되는 빛의 계조를 보다 세밀하게 제어할 수 있으며, 그 결과 유기 발광 표시 장치의 해상도를 높이고 표시 품질을 향상시킬 수 있다.

【0028】 또한, 굴곡부를 가지는 구동 반도체층에 의해 줄어든 스토리지 캐패시터의 영역을 확보하기 위해 구동 반도체층과 중첩하여 스토리지 캐패시터를 형성함으로써, 고해상도에서도 스토리지 캐패시턴스를 충분히 확보할 수 있다.

【0029】 또한, 보상 박막 트랜지스터와 연결되는 제1 경로 반도체층의 길이를 발광 제어 박막 트랜지스터와 연결되는 제2 경로 반도체층의 길이보다 짧게 형성함으로써, 저계조 얼룩을 방지할 수 있다.

【도면의 간단한 설명】

【0030】 도 1은 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 하나의 화소의 등가 회로도이다.

도 2는 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 복수개의 박막

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트랜지스터 및 캐패시터의 위치를 개략적으로 도시한 도면이다.

도 3은 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 하나의 화소의 구체적인 배치도이다.

도 4는 도 3의 유기 발광 표시 장치를 IV-IV선을 따라 자른 단면도이다.

도 5는 도 3의 유기 발광 표시 장치를 V-V선을 따라 자른 단면도이다.

도 6은 본 발명의 제2 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터의 확대 배치도이다.

도 7은 본 발명의 제3 실시예에 따른 유기 발광 표시 장치의 배치도이다.

도 8은 본 발명의 제4 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터의 확대 배치도이다.

도 9는 본 발명의 제5 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터의 확대 배치도이다.

도 10은 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 하나의 화소의 등가 회로도이다.

도 11은 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 배치도이다.

【발명을 실시하기 위한 구체적인 내용】

【0031】 이하, 첨부한 도면을 참고로 하여 본 발명의 여러 실시예들에 대하여 본 발명이 속하는 기술 분야에서 통상의 지식을 가진 자가 용이하게 실시할 수 있도록 상세히 설명한다. 본 발명은 여러 가지 상이한 형태로 구현될 수 있으며

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여기에서 설명하는 실시예들에 한정되지 않는다.

【0032】 본 발명을 명확하게 설명하기 위해서 설명과 관계없는 부분은 생략하였으며, 명세서 전체를 통하여 동일 또는 유사한 구성요소에 대해서는 동일한 참조 부호를 붙이도록 한다.

【0033】 또한, 도면에서 나타난 각 구성의 크기 및 두께는 설명의 편의를 위해 임의로 나타내었으므로, 본 발명이 반드시 도시된 바에 한정되지 않는다.

【0034】 도면에서 여러 층 및 영역을 명확하게 표현하기 위하여 두께를 확대하여 나타내었다. 그리고 도면에서, 설명의 편의를 위해, 일부 층 및 영역의 두께를 과장되게 나타내었다. 층, 막, 영역, 판 등의 부분이 다른 부분 "위에" 또는 "상에" 있다고 할 때, 이는 다른 부분 "바로 위에" 있는 경우뿐 아니라 그 중간에 또 다른 부분이 있는 경우도 포함한다.

【0035】 또한, 명세서 전체에서, 어떤 부분이 어떤 구성요소를 "포함" 한다고 할 때, 이는 특별히 반대되는 기재가 없는 한 다른 구성요소를 제외하는 것이 아니라 다른 구성요소를 더 포함할 수 있는 것을 의미한다. 또한, 명세서 전체에서, "~상에"라 함은 대상 부분의 위 또는 아래에 위치함을 의미하는 것이며, 반드시 중력 방향을 기준으로 상 측에 위치하는 것을 의미하는 것은 아니다.

【0036】 그러면 본 발명의 제1 실시예에 따른 유기 발광 표시 장치에 대하여 도 1 내지 도 5를 참고로 상세하게 설명한다.

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【0037】 도 1은 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 하나의 화소의 등가 회로도이다.

【0038】 도 1에 도시한 바와 같이, 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 하나의 화소는 복수의 신호선(121, 122, 123, 124, 171, 172), 복수의 신호선에 연결되어 있는 복수개의 박막 트랜지스터(T1, T2, T3, T4, T5, T6), 스토리지 캐패시터(storage capacitor, Cst) 및 유기 발광 다이오드(organic light emitting diode, OLED)를 포함한다.

【0039】 박막 트랜지스터는 구동 박막 트랜지스터(driving thin film transistor)(T1), 스위칭 박막 트랜지스터(switching thin film transistor)(T2), 보상 박막 트랜지스터(T3), 초기화 박막 트랜지스터(T4), 동작 제어 박막 트랜지스터(T5) 및 발광 제어 박막 트랜지스터(T6)를 포함한다.

【0040】 신호선은 스캔 신호(Sn)를 전달하는 스캔선(121), 초기화 박막 트랜지스터(T4)에 이전 스캔 신호(Sn-1)를 전달하는 이전 스캔선(122), 동작 제어 박막 트랜지스터(T5) 및 발광 제어 박막 트랜지스터(T6)에 발광 제어 신호(En)를 전달하는 발광 제어선(123), 스캔선(121)과 교차하며 데이터 신호(Dm)를 전달하는 데이터선(171), 구동 전압(ELVDD)을 전달하며 데이터선(171)과 거의 평행하게 형성되어 있는 구동 전압선(172), 구동 박막 트랜지스터(T1)를 초기화하는 초기화 전압(Vint)을 전달하는 초기화 전압선(124)을 포함한다.

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【0041】 구동 박막 트랜지스터(T1)의 게이트 전극(G1)은 스토리지 캐패시터(Cst)의 일단(Cst1)과 연결되어 있고, 구동 박막 트랜지스터(T1)의 소스 전극(S1)은 동작 제어 박막 트랜지스터(T5)를 경유하여 구동 전압선(172)과 연결되어 있으며, 구동 박막 트랜지스터(T1)의 드레인 전극(D1)은 발광 제어 박막 트랜지스터(T6)를 경유하여 유기 발광 다이오드(OLED)의 애노드(anode)와 전기적으로 연결되어 있다. 구동 박막 트랜지스터(T1)는 스위칭 박막 트랜지스터(T2)의 스위칭 동작에 따라 데이터 신호(Dm)를 전달받아 유기 발광 다이오드(OLED)에 구동 전류(Id)를 공급한다.

【0042】 스위칭 박막 트랜지스터(T2)의 게이트 전극(G2)은 스캔선(121)과 연결되어 있고, 스위칭 박막 트랜지스터(T2)의 소스 전극(S2)은 데이터선(171)과 연결되어 있으며, 스위칭 박막 트랜지스터(T2)의 드레인 전극(D2)은 구동 박막 트랜지스터(T1)의 소스 전극(S1)과 연결되어 있으면서 동작 제어 박막 트랜지스터(T5)을 경유하여 구동 전압선(172)과 연결되어 있다. 이러한 스위칭 박막 트랜지스터(T2)는 스캔선(121)을 통해 전달받은 스캔 신호(Sn)에 따라 턴 온되어 데이터선(171)으로 전달된 데이터 신호(Dm)을 구동 박막 트랜지스터(T1)의 소스 전극으로 전달하는 스위칭 동작을 수행한다.

【0043】 보상 박막 트랜지스터(T3)의 게이트 전극(G3)은 스캔선(121)에 연결되어 있고, 보상 박막 트랜지스터(T3)의 소스 전극(S3)은 구동 박막 트랜지스터(T1)의 드레인 전극(D1)과 연결되어 있으면서 발광 제어 박막 트랜지스터(T6)를 경유하여 유기 발광 다이오드(OLED)의 애노드(anode)와 연결되어 있으며, 보상 박막

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트랜지스터(T3)의 드레인 전극(D3)은 스토리지 캐패시터(Cst)의 일단(Cst1), 초기화 박막 트랜지스터(T4)의 드레인 전극(D4) 및 구동 박막 트랜지스터(T1)의 게이트 전극(G1)과 함께 연결되어 있다. 이러한 보상 박막 트랜지스터(T3)는 스캔선(121)을 통해 전달받은 스캔 신호(Sn)에 따라 턴 온되어 구동 박막 트랜지스터(T1)의 게이트 전극(G1)과 드레인 전극(D1)을 서로 연결하여 구동 박막 트랜지스터(T1)를 다이오드 연결시킨다.

【0044】초기화 박막 트랜지스터(T4)의 게이트 전극(G4)은 이전 스캔선(122)과 연결되어 있고, 초기화 박막 트랜지스터(T4)의 소스 전극(S4)은 초기화 전압선(124)과 연결되어 있으며, 초기화 박막 트랜지스터(T4)의 드레인 전극(D4)은 스토리지 캐패시터(Cst)의 일단(Cst1), 보상 박막 트랜지스터(T3)의 드레인 전극(D3) 및 구동 박막 트랜지스터(T1)의 게이트 전극(G1)과 함께 연결되어 있다. 이러한 초기화 박막 트랜지스터(T4)는 이전 스캔선(122)을 통해 전달받은 이전 스캔 신호(Sn-1)에 따라 턴 온되어 초기화 전압(Vint)을 구동 박막 트랜지스터(T1)의 게이트 전극(G1)에 전달하여 구동 박막 트랜지스터(T1)의 게이트 전극(G1)의 전압을 초기화시키는 초기화 동작을 수행한다.

【0045】동작 제어 박막 트랜지스터(T5)의 게이트 전극(G5)은 발광 제어선(123)과 연결되어 있으며, 동작 제어 박막 트랜지스터(T5)의 소스 전극(S5)은 구동 전압선(172)와 연결되어 있고, 동작 제어 박막 트랜지스터(T5)의 드레인 전극(D5)은 구동 박막 트랜지스터(T1)의 소스 전극(S1) 및 스위칭 박막 트랜지스터(T2)의 드레인 전극(S2)와 연결되어 있다.

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【0046】 발광 제어 박막 트랜지스터(T6)의 게이트 전극(G6)은 발광 제어선(123)과 연결되어 있으며, 발광 제어 박막 트랜지스터(T6)의 소스 전극(S6)은 구동 박막 트랜지스터(T1)의 드레인 전극(D1) 및 보상 박막 트랜지스터(T3)의 소스 전극(S3)과 연결되어 있고, 발광 제어 박막 트랜지스터(T6)의 드레인 전극(D6)은 유기 발광 다이오드(OLED)의 애노드(anode)와 전기적으로 연결되어 있다. 이러한 동작 제어 박막 트랜지스터(T5) 및 발광 제어 박막 트랜지스터(T6)는 발광 제어선(123)을 통해 전달받은 발광 제어 신호(En)에 따라 동시에 턴 온되어 구동 전압(ELVDD)이 유기 발광 다이오드(OLED)에 전달되어 유기 발광 다이오드(OLED)에 구동 전류(Id)가 흐르게 된다.

【0047】 스토리지 캐패시터(Cst)의 타단(Cst2)은 구동 전압선(172)과 연결되어 있으며, 유기 발광 다이오드(OLED)의 캐소드(cathode)는 공통 전압(ELVSS)과 연결되어 있다. 이에 따라, 유기 발광 다이오드(OLED)는 구동 박막 트랜지스터(T1)로부터 구동 전류(Id)를 전달받아 발광함으로써 화상을 표시한다.

【0048】 이하에서 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 한 화소의 구체적인 동작 과정을 상세히 설명한다.

【0049】 우선, 초기화 기간 동안 이전 스캔선(122)을 통해 로우 레벨(low level)의 이전 스캔 신호(Sn-1)가 공급된다. 그러면, 로우 레벨의 이전 스캔 신호(Sn-1)에 대응하여 초기화 박막 트랜지스터(T4)가 턴 온(Turn on)되며, 초기화 전압선(124)으로부터 초기화 박막 트랜지스터(T4)를 통해 초기화 전압(Vint)이 구동 박막 트랜지스터(T1)의 게이트 전극에 연결되고, 초기화 전압(Vint)에 의해 구동

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박막 트랜지스터(T1)가 초기화된다.

【0050】 이 후, 데이터 프로그래밍 기간 중 스캔선(121)을 통해 로우 레벨의 스캔 신호(Sn)가 공급된다. 그러면, 로우 레벨의 스캔 신호(Sn)에 대응하여 스위칭 박막 트랜지스터(T2) 및 보상 박막 트랜지스터(T3)가 턴 온된다.

【0051】 이 때, 구동 박막 트랜지스터(T1)는 턴 온된 보상 박막 트랜지스터(T3)에 의해 다이오드 연결되고, 순방향으로 바이어스 된다.

【0052】 그러면, 데이터선(171)으로부터 공급된 데이터 신호(Dm)에서 구동 박막 트랜지스터(T1)의 문턱 전압(Threshold voltage, Vth)만큼 감소한 보상 전압(Dm+Vth, Vth는 (-)의 값)이 구동 박막 트랜지스터(T1)의 게이트 전극에 인가된다.

【0053】 스토리지 커패시터(Cst)의 양단에는 구동 전압(ELVDD)과 보상 전압(Dm+Vth)이 인가되고, 스토리지 커패시터(Cst)에는 양단 전압 차에 대응하는 전하가 저장된다. 이 후, 발광 기간 동안 발광 제어선(123)으로부터 공급되는 발광 제어 신호(En)가 하이 레벨에서 로우 레벨로 변경된다. 그러면, 발광 기간 동안 로우 레벨의 발광 제어 신호(En)에 의해 동작 제어 박막 트랜지스터(T5) 및 발광 제어 박막 트랜지스터(T6)가 턴 온된다.

【0054】 그러면, 구동 박막 트랜지스터(T1)의 게이트 전극의 전압과 구동 전압(ELVDD) 간의 전압차에 따르는 구동 전류(Id)가 발생하고, 발광 제어 박막 트랜지스터(T6)를 통해 구동 전류(Id)가 유기 발광 다이오드(OLED)에 공급된다. 발광 기간동안 스토리지 캐패시터(Cst)에 의해 구동 박막 트랜지스터(T1)의 게이트-소스

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전압(Vgs)은 '(Dm+Vth)-ELVDD'으로 유지되고, 구동 박막 트랜지스터(T1)의 전류-전압 관계에 따르면, 구동 전류(Id)는 소스-게이트 전압에서 문턱 전압을 차감한 값의 제곱 '$(Dm-ELVDD)^2$'에 비례한다. 따라서 구동 전류(Id)는 구동 박막 트랜지스터(T1)의 문턱 전압(Vth)에 관계 없이 결정된다.

【0055】그러면 도 1에 도시한 유기 발광 표시 장치의 화소의 상세 구조에 대하여 도 2 내지 도 5를 도 1과 함께 참고하여 상세하게 설명한다.

【0056】도 2는 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 복수개의 박막 트랜지스터 및 캐패시터의 위치를 개략적으로 도시한 도면이고, 도 3은 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 하나의 화소의 구체적인 배치도이고, 도 4는 도 3의 유기 발광 표시 장치를 IV-IV선을 따라 자른 단면도이고, 도 5는 도 3의 유기 발광 표시 장치를 V-V선을 따라 자른 단면도이다.

【0057】도 2 내지 도 5에 도시한 바와 같이, 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 화소는 스캔 신호(Sn), 이전 스캔 신호(Sn-1), 발광 제어 신호(En) 및 초기화 전압(Vint)을 각각 인가하며 행 방향을 따라 형성되어 있는 스캔선(121), 이전 스캔선(122), 발광 제어선(123) 및 초기화 전압선(124)을 포함하고, 스캔선(121), 이전 스캔선(122), 발광 제어선(123) 및 초기화 전압선(124) 모두와 교차하고 있으며 화소에 데이터 신호(Dm) 및 구동 전압(ELVDD)을 각각 인가하는 데이터선(171) 및 구동 전압선(172)을 포함한다.

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【0058】 또한, 화소에는 구동 박막 트랜지스터(T1), 스위칭 박막 트랜지스터(T2), 보상 박막 트랜지스터(T3), 초기화 박막 트랜지스터(T4), 동작 제어 박막 트랜지스터(T5), 발광 제어 박막 트랜지스터(T6), 스토리지 캐패시터(Cst), 그리고 유기 발광 다이오드(OLED)(70)가 형성되어 있다.

【0059】 구동 박막 트랜지스터(T1), 스위칭 박막 트랜지스터(T2), 보상 박막 트랜지스터(T3), 초기화 박막 트랜지스터(T4), 동작 제어 박막 트랜지스터(T5) 및 발광 제어 박막 트랜지스터(T6)는 반도체층(131)을 따라 형성되어 있으며, 반도체층(131)은 다양한 형상으로 굴곡되어 형성되어 있다. 이러한 반도체층(131)은 폴리 실리콘으로 이루어지며, 불순물이 도핑되지 않은 채널 영역과, 채널 영역의 양옆으로 불순물이 도핑되어 형성된 소스 영역 및 드레인 영역을 포함한다. 여기서, 이러한 불순물은 박막 트랜지스터의 종류에 따라 달라지며, N형 불순물 또는 P형 불순물이 가능하다. 이러한 반도체층은 구동 박막 트랜지스터(T1)에 형성되는 구동 반도체층(131a), 스위칭 박막 트랜지스터(T2)에 형성되는 스위칭 반도체층(131b), 보상 박막 트랜지스터(T3)에 형성되는 보상 반도체층(131c), 초기화 박막 트랜지스터(T4)에 형성되는 초기화 반도체층(131d), 동작 제어 박막 트랜지스터(T5)에 형성되는 동작 제어 반도체층(131e) 및 발광 제어 박막 트랜지스터(T6)에 형성되는 발광 제어 반도체층(131f)을 포함한다.

【0060】 구동 박막 트랜지스터(T1)는 구동 반도체층(131a), 구동 게이트 전극(125a), 구동 소스 전극(176a) 및 구동 드레인 전극(177a)을 포함한다. 구동 반도체층(131a)은 굴곡되어 있다. 구동 반도체층(131a)은 제1 방향으로 연장되어 있

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는 복수개의 제1 연장부(31), 제1 방향과 다른 제2 방향으로 연장되어 있는 복수개의 제2 연장부(32) 및 제1 연장부(31)와 제2 연장부(32)를 연결하는 복수개의 굴곡부(33)를 포함한다. 따라서, 구동 반도체층(131a)은 지그재그 형상으로 배치될 수 있다. 도 2 및 도 3에 도시한 구동 반도체층(131a)은 3개의 제1 연장부(31), 2개의 제2 연장부(32) 및 4개의 굴곡부(33)를 포함한다. 따라서, 구동 반도체층(131a)은 'ㄹ' 형상으로 길게 배치되어 있다.

【0061】 이와 같이, 복수개의 굴곡부(33)를 포함하는 구동 반도체층(131a)을 형성함으로써, 좁은 공간 내에 길게 구동 반도체층(131a)을 형성할 수 있다. 따라서, 구동 반도체층(131a)의 구동 채널 영역(131a1)을 길게 형성할 수 있으므로 구동 게이트 전극(125a)에 인가되는 게이트 전압의 구동 범위(driving range)는 넓어지게 된다. 따라서, 게이트 전압의 구동 범위가 넓으므로 게이트 전압의 크기를 변화시켜 유기 발광 다이오드(OLED)에서 방출되는 빛의 계조를 보다 세밀하게 제어할 수 있으며, 그 결과 유기 발광 표시 장치의 해상도를 높이고 표시 품질을 향상시킬 수 있다.

【0062】 이러한 구동 반도체층(131a)은 제1 연장부(31), 제2 연장부(32) 및 굴곡부(33)를 다양하게 배치하여 'S', 'M', 'W' 등의 다양한 실시예가 가능하다.

【0063】 도 6은 본 발명의 제2 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터의 확대 배치도이다.

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【0064】 도 6에 도시한 바와 같이, 구동 반도체층(131a)은 'S' 형상으로 배치될 수도 있다.

【0065】 한편, 구동 소스 전극(176a)은 구동 반도체층(131a)에서 불순물이 도핑된 구동 소스 영역(176a)에 해당하고, 구동 드레인 전극(177a)은 구동 반도체층(131a)에서 불순물이 도핑된 구동 드레인 영역(177a)에 해당한다. 구동 게이트 전극(125a)과 중첩하여 위에 스토리지 캐패시터(Cst)가 형성되어 있다.

【0066】 스토리지 캐패시터(Cst)는 제2 게이트 절연막(142)을 사이에 두고 배치되는 제1 스토리지 축전판(125a)과 제2 스토리지 축전판(127)을 포함한다. 여기서, 구동 게이트 전극(125a)은 제1 스토리지 축전판(125a)의 역할도 동시에 하며, 제2 게이트 절연막(142)은 유전체가 되며, 스토리지 캐패시터(Cst)에서 축전된 전하와 양 축전판(125a, 127) 사이의 전압에 의해 스토리지 캐패시턴스(Storage Capacitance)가 결정된다.

【0067】 제1 스토리지 축전판(125a)은 인접한 화소와 분리되어 사각 형상으로 형성되어 있으며, 스캔선(121), 이전 스캔선(122), 발광 제어선(123), 스위칭 게이트 전극(125b), 보상 게이트 전극(125c), 동작 제어 게이트 전극(125e), 발광 제어 게이트 전극(125f)과 동일한 물질로 동일한 층에 형성되어 있다.

【0068】 제2 스토리지 축전판(127)은 인접한 화소와 연결되어 있으며, 초기화 전압선(124)과 동일한 물질로 동일한 층에 형성되어 있다.

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【0069】 이와 같이, 굴곡부를 가지는 구동 반도체층(131a)에 의해 줄어든 스토리지 캐패시터의 영역을 확보하기 위해 구동 반도체층(131a)과 중첩하여 스토리지 캐패시터를 형성함으로써, 고해상도에서도 스토리지 캐패시턴스의 확보가 가능하다.

【0070】 스위칭 박막 트랜지스터(T2)는 스위칭 반도체층(131b), 스위칭 게이트 전극(125b), 스위칭 소스 전극(176b) 및 스위칭 드레인 전극(177b)을 포함한다. 스위칭 소스 전극(176b)은 데이터선(171)에서 돌출된 부분이며, 스위칭 드레인 전극(177b)은 스위칭 반도체층(131b)에서 불순물이 도핑된 스위칭 드레인 영역(177b)에 해당한다.

【0071】 보상 박막 트랜지스터(T3)는 보상 반도체층(131c), 보상 게이트 전극(125c), 보상 소스 전극(176c) 및 보상 드레인 전극(177c)을 포함하고, 보상 소스 전극(176c)은 보상 반도체층(131c)에서 불순물이 도핑된 보상 소스 영역(176c)에 해당하고, 보상 드레인 전극(177c)은 보상 반도체층(131c)에서 불순물이 도핑된 보상 드레인 영역(177c)에 해당한다. 보상 게이트 전극(125c)는 별도의 듀얼 게이트 전극(25)을 형성하여 누설 전류(leakage current)를 방지한다.

【0072】 초기화 박막 트랜지스터(T4)는 초기화 반도체층(131d), 초기화 게이트 전극(125d), 초기화 소스 전극(176d) 및 초기화 드레인 전극(177d)을 포함한다. 초기화 드레인 전극(177d)은 초기화 반도체층(131d)에서 불순물이 도핑된 초기화 드레인 영역(177d)에 해당한다. 초기화 소스 전극(176d)은 초기화 연결선(78)을 통해 초기화 전압선(124)와 연결되어 있다. 초기화 연결선(78)의 일단은 제2 게이

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트 절연막(142) 및 층간 절연막(160)에 형성된 접촉 구멍(161)을 통해 초기화 전압선(124)과 연결되어 있고, 초기화 연결선(78)의 타단은 게이트 절연막(141), 제2 게이트 절연막(142) 및 층간 절연막(160)에 형성된 접촉 구멍(161)을 통해 초기화 소스 전극(176d)과 연결되어 있다.

【0073】 동작 제어 박막 트랜지스터(T5)는 동작 제어 반도체층(131e), 동작 제어 게이트 전극(125e), 동작 제어 소스 전극(176e) 및 동작 제어 드레인 전극(177e)을 포함한다. 동작 제어 소스 전극(176e)은 구동 전압선(172)의 일부분이고, 동작 제어 드레인 전극(177e)은 동작 제어 반도체층(131e)에서 불순물이 도핑된 동작 제어 드레인 영역(177e)에 해당한다.

【0074】 발광 제어 박막 트랜지스터(T6)는 발광 제어 반도체층(131f), 발광 제어 게이트 전극(125f), 발광 제어 소스 전극(176f) 및 발광 제어 드레인 전극(177f)을 포함한다. 발광 제어 소스 전극(176f)은 발광 제어 반도체층(131f)에서 불순물이 도핑된 발광 제어 소스 영역(176f)에 해당한다.

【0075】 구동 박막 트랜지스터(T1)의 구동 반도체층(131a)의 일단은 스위칭 반도체층(131b) 및 보상 반도체층(131c)과 연결되어 있으며, 구동 반도체층(131a)의 타단은 동작 제어 반도체층(131e) 및 발광 제어 반도체층(131f)과 연결되어 있다. 따라서, 구동 소스 전극(176a)은 스위칭 드레인 전극(177b) 및 동작 제어 드레인 전극(177e)과 연결되고, 구동 드레인 전극(177a)은 보상 소스 전극(176c) 및 발광 제어 소스 전극(176f)과 연결된다.

【0076】 스토리지 캐패시터(Cst)의 제1 스토리지 축전판(125a)은 연결 부재

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(174)을 통해 보상 드레인 전극(177c) 및 초기화 드레인 전극(177d)과 함께 연결되어 있다. 이러한 연결 부재(174)는 데이터선(171)과 동일한 층에 형성되어 있으며, 연결 부재(174)의 일단은 제1 게이트 절연막(141), 제2 게이트 절연막(142) 및 층간 절연막(160)에 형성된 접촉 구멍(166)을 통해 보상 드레인 전극(177c) 및 초기화 드레인 전극(177d)과 연결되며, 연결 부재(174)의 타단은 제2 게이트 절연막(142) 및 층간 절연막(160)에 형성된 접촉 구멍(167)을 통해 제1 스토리지 축전판(125a)과 연결된다. 이 때, 제2 스토리지 축전판(127)에 형성된 스토리지 개구부(27)를 통해 연결 부재(174)의 타단은 제1 스토리지 축전판(125a)과 연결된다.

【0077】 스토리지 캐패시터(Cst)의 제2 스토리지 축전판(127)은 층간 절연막(160)에 형성된 접촉 구멍(168)을 통해 공통 전압선(172)과 연결되어 있다.

【0078】 한편, 스위칭 박막 트랜지스터(T2)는 발광시키고자 하는 화소를 선택하는 스위칭 소자로 사용된다. 스위칭 게이트 전극(125b)은 스캔선(121)에 연결되어 있고, 스위칭 소스 전극(176b)은 데이터선(171)에 연결되어 있으며, 스위칭 드레인 전극(177b)은 구동 박막 트랜지스터(T1) 및 동작 제어 박막 트랜지스터(T5)와 연결되어 있다. 그리고, 발광 제어 박막 트랜지스터(T6)의 발광 제어 드레인 전극(177f)은 보호막(180)에 형성된 접촉 구멍(181)를 통해 유기 발광 다이이드(70)의 화소 전극(191)과 직접 연결되어 있다.

【0079】 이하, 도 4 및 도 5를 참조하여 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 구조에 대해 적층 순서에 따라 구체적으로 설명한다.

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【0080】이 때, 구동 박막 트랜지스터(T1), 스위칭 박막 트랜지스터(T2) 및 발광 제어 박막 트랜지스터(T6)를 중심으로 박막 트랜지스터의 구조에 대해 설명한다. 그리고 나머지 박막 트랜지스터(T3, T4, T5)는 구동 박막 트랜지스터(T1), 스위칭 박막 트랜지스터(T2) 및 발광 제어 박막 트랜지스터(T6)의 적층 구조와 대부분 동일하므로 상세한 설명은 생략한다.

【0081】기판(110) 위에는 버퍼층(111)이 형성되어 있고, 기판(110)은 유리, 석영, 세라믹, 플라스틱 등으로 이루어진 절연성 기판으로 형성되어 있다.

【0082】버퍼층(111) 위에는 구동 반도체층(131a), 스위칭 반도체층(131b), 발광 제어 반도체층(131f)이 형성되어 있다. 구동 반도체층(131a)은 구동 채널 영역(131a1) 및 구동 채널 영역(131a1)을 사이에 두고 서로 마주보는 구동 소스 영역(176a) 및 구동 드레인 영역(177a)을 포함하고, 스위칭 반도체층(131b)은 스위칭 채널 영역(131b1) 및 스위칭 채널 영역(131b1)을 사이에 두고 서로 마주보는 스위칭 소스 영역(132b) 및 스위칭 드레인 영역(177b)을 포함하며, 발광 제어 박막 트랜지스터(T6)는 발광 제어 채널 영역(131f1), 발광 제어 소스 영역(176f) 및 발광 제어 드레인 영역(133f)을 포함한다.

【0083】구동 반도체층(131a)은 복수개의 굴곡부(33)를 포함하여 지그재그 형상, 구체적으로는 'ㄹ' 형상으로 형성되므로, 좁은 공간 내에 길게 형성할 수 있다. 따라서, 구동 반도체층(131a)의 구동 채널 영역(131a1)을 길게 형성할 수 있으므로 구동 게이트 전극(125a)에 인가되는 게이트 전압의 구동 범위(driving range)는 넓어지게 된다.

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【0084】 스위칭 반도체층(131a), 구동 반도체층(131b), 발광 제어 반도체층(131f) 위에는 질화 규소(SiNx) 또는 산화 규소(Si02) 따위로 형성된 제1 게이트 절연막(141)이 형성되어 있다.

【0085】 제1 게이트 절연막(141) 위에는 구동 게이트 전극(125a), 스위칭 게이트 전극(125b) 및 보상 게이트 전극(125c)을 포함하는 스캔선(121), 초기화 게이트 전극(125d)을 포함하는 이전 스캔선(122), 동작 제어 게이트 전극(125e) 및 발광 제어 게이트 전극(125f)을 포함하는 발광 제어선(123)을 포함하는 제1 게이트 배선이 형성되어 있다.

【0086】 구동 게이트 전극(125a)은 스캔선(121)과 분리되어 있으며, 플로팅 게이트 전극(25)은 구동 반도체층(131a)의 구동 채널 영역(131a1)과 중첩하고 있다. 그리고, 스위칭 게이트 전극(125a)은 스캔선(121)에 연결되어 있으며, 스위칭 게이트 전극(125b)은 스위칭 반도체층(131b)의 스위칭 채널 영역(131b1)과 중첩하고 있다. 그리고 발광 제어 게이트 전극(125f)은 발광 제어 반도체층(131f)의 발광 제어 채널 영역(131f1)과 중첩하고 있다.

【0087】 이 때, 스위칭 박막 트랜지스터(T2)는 스위칭 게이트 전극(125b)과 스위칭 반도체층(131b) 사이에 제1 게이트 절연막(141)만이 형성되므로 빠른 스위칭 동작이 가능하며, 구동 박막 트랜지스터(T1)은 구동 게이트 전극(125a)과 구동 반도체층(131a) 사이에 제1 게이트 절연막(141)만이 형성되어 있긴 하나, 구동 반도체층(131a)의 구동 채널 영역(131a1)의 길이가 길기 때문에 구동 게이트 전극(125a)에 인가되는 게이트 전압의 구동 범위(driving range)는 넓어지게 되어 유기

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발광 다이오드(OLED)에서 방출되는 빛의 계조를 보다 세밀하게 제어할 수 있다.

【0088】 제1 게이트 배선(125a, 125b, 125c, 125d, 125e, 125f, 121, 122, 123) 및 제1 게이트 절연막(141)은 제2 게이트 절연막(142)이 덮고 있다. 제2 게이트 절연막(142)은 질화 규소(SiNx) 또는 산화 규소(SiO2) 따위로 형성되어 있다.

【0089】 제2 게이트 절연막(142) 위에는 제2 스토리지 축전판(127) 및 초기화 전압선(124)을 포함하는 제2 게이트 배선이 형성되어 있다. 제2 스토리지 축전판(127)은 제1 스토리지 축전판(125a)와 중첩하여 스토리지 캐패시터(Cst)를 형성하고 있으며, 제1 스토리지 축전판(125a)는 구동 반도체층(131a)과 중첩하고 있다. 이와 같이, 구동 반도체층(131a)과 중첩하여 스토리지 캐패시터(Cst)를 형성함으로써, 굴곡부(33)를 가지는 구동 반도체층(131a)에 의해 줄어든 스토리지 캐패시터(Cst)의 영역을 확보하여 화소의 크기가 줄어드는 고해상도에서도 스토리지 캐패시턴스의 확보가 가능하다.

【0090】 한편, 제2 게이트 절연막(142), 제2 스토리지 축전판(127) 및 초기화 전압선(124) 위에는 층간 절연막(160)이 형성되어 있다. 제1 게이트 절연막(141), 제2 게이트 절연막(142) 및 층간 절연막(160)은 발광 제어 반도체층(131f)의 발광 제어 드레인 영역(131f1)을 드러내는 접촉 구멍(163)을 함께 갖는다. 층간 절연막(160)은 제1 게이트 절연막(141), 제2 게이트 절연막(142)과 마찬가지로, 질화 규소(SiNx) 또는 산화 규소(SiO2) 등의 세라믹(ceramic) 계열의 소재를 사용하여 만들어진다.

【0091】 층간 절연막(160) 위에는 스위칭 소스 전극(176b)를 포함하는 데이

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터선(171), 구동 전압선(172), 연결 부재(174), 발광 제어 드레인 전극(177f)을 포함하는 데이터 배선이 형성되어 있다.

【0092】 그리고 스위칭 소스 전극(176b)과 발광 제어 드레인 전극(177f)은 각각 층간 절연막(160), 제1 게이트 절연막(141) 및 제2 게이트 절연막(142)에 형성된 접촉 구멍(162, 163)을 통해 각각 스위칭 반도체층(131b)의 스위칭 소스 영역(131b1), 발광 제어 반도체층(131f)의 발광 제어 드레인 영역(131f1)과 연결된다.

【0093】 층간 절연막(160) 상에는 데이터 배선(171, 172, 174, 177f)을 덮는 보호막(180)이 형성되어 있고, 보호막(180) 위에는 화소 전극(191)이 형성되어 있다. 보호막(180)에 형성된 접촉 구멍(181)을 통해 화소 전극(191)은 발광 제어 드레인 전극(177f)과 연결된다.

【0094】 화소 전극(191)의 가장자리 및 보호막(180) 위에는 격벽(350)이 형성되어 있고, 격벽(350)은 화소 전극(191)을 드러내는 격벽 개구부(351)를 가진다. 격벽(350)은 폴리아크릴계 수지(polyacrylates resin) 및 폴리이미드계(polyimides) 등의 수지 또는 실리카 계열의 무기물 등으로 만들 수 있다.

【0095】 격벽 개구부(351)로 노출된 화소 전극(191) 위에는 유기 발광층(370)이 형성되고, 유기 발광층(370) 상에는 공통 전극(270)이 형성된다. 이와 같이, 화소 전극(191), 유기 발광층(370) 및 공통 전극(270)을 포함하는 유기 발광 다이오드(70)가 형성된다.

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【0096】 여기서, 화소 전극(191)은 정공 주입 전극인 애노드이며, 공통 전극(270)은 전자 주입 전극인 캐소드가 된다. 그러나 본 발명에 따른 일 실시예는 반드시 이에 한정되는 것은 아니며, 유기 발광 표시 장치의 구동 방법에 따라 화소 전극(191)이 캐소드가 되고, 공통 전극(270)이 애노드가 될 수도 있다. 화소 전극(191) 및 공통 전극(270)으로부터 각각 정공과 전자가 유기 발광층(370) 내부로 주입되고, 주입된 정공과 전자가 결합한 엑시톤(exiton)이 여기상태로부터 기저상태로 떨어질 때 발광이 이루어진다.

【0097】 유기 발광층(370)은 저분자 유기물 또는 PEDOT(Poly 3,4-ethylenedioxythiophene) 등의 고분자 유기물로 이루어진다. 또한, 유기 발광층(370)은 발광층과, 정공 주입층(hole injection layer, HIL), 정공 수송층(hole transporting layer, HTL), 전자 수송층(electron transporting layer, ETL), 및 전자 주입층(electron injection layer, EIL) 중 하나 이상을 포함하는 다중막으로 형성될 수 있다. 이들 모두를 포함할 경우, 정공 주입층이 양극인 화소 전극(710) 상에 배치되고, 그 위로 정공 수송층, 발광층, 전자 수송층, 전자 주입층이 차례로 적층된다. 공통 전극(270)은 반사형 도전성 물질로 형성되므로 배면 발광형의 유기 발광 표시 장치가 된다. 반사형 물질로는 리튬(Li), 칼슘(Ca), 플루오르화리튬/칼슘(LiF/Ca), 플루오르화리튬/알루미늄(LiF/Al), 알루미늄(Al), 은(Ag), 마그네슘(Mg), 또는 금(Au) 등의 물질을 사용할 수 있다.

【0098】 한편, 상기 제1 실시예에서 제1 스토리지 축전판(125a)가 사각 형상이었으나, 제1 스토리지 축전판(125a)의 일부를 확장하여 스토리지 캐패시턴스를

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증가시키는 제3 실시예도 가능하다.

【0099】 이하에서, 도 7을 참조하여, 본 발명의 제3 실시예에 따른 유기 발광 표시 장치에 대해 상세히 설명한다.

【0100】 도 7은 본 발명의 제3 실시예에 따른 유기 발광 표시 장치의 배치도이다.

【0101】 제3 실시예는 도 1 내지 도 5에 도시된 제1 실시예와 비교하여 구동 반도체층 및 스토리지 캐패시터만을 제외하고 실질적으로 동일한 바 반복되는 설명은 생략한다.

【0102】 도 7에 도시한 바와 같이, 본 발명의 제3 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터(T1)는 구동 반도체층(131a), 구동 게이트 전극(125a), 구동 소스 전극(176a) 및 구동 드레인 전극(177a)을 포함한다. 구동 반도체층(131a)은 굴곡되어 있다. 구동 반도체층(131a)은 제1 방향으로 연장되어 있는 복수개의 제1 연장부(31), 제1 방향과 다른 제2 방향으로 연장되어 있는 복수개의 제2 연장부(32) 및 제1 연장부(31)와 제2 연장부(32)를 연결하는 복수개의 굴곡부(33)를 포함한다.

【0103】 이러한 구동 반도체층(131a)은 측면으로 연장되어 데이터선(171)과 인접할 수 있다. 따라서, 구동 반도체층(131a)의 길이가 길어지므로 구동 게이트 전극(125a)에 인가되는 게이트 전압의 구동 범위(driving range)를 더욱 넓힐 수 있다.

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【0104】이 때, 보상 박막 트랜지스터(T3)의 보상 소스 전극(176c)과 발광 제어 박막 트랜지스터(T6)의 발광 제어 소스 전극(176f)은 동일한 층에 형성되어 있으나, 구동 반도체층(131a)과 중첩되지 않도록 보상 소스 전극(176c)과 발광 제어 소스 전극(176f)은 이격부(d)를 두고 서로 분리되어 있다.

【0105】연장된 구동 반도체층(131a)과 중첩하도록 구동 게이트 전극(125a) 즉, 제1 스토리지 축전판(125a)은 측면으로 연장되어 있으며, 제1 스토리지 축전판(125a)은 이격부(d)와 일부 중첩되어 있다. 그리고, 제1 스토리지 축전판(125a)와 중첩하도록 제2 스토리지 축전판(127)도 연장되어 있으며, 제2 스토리지 축전판(127)은 이격부(d)와 일부 중첩되어 있다.

【0106】서로 분리된 보상 소스 전극(176c)과 발광 제어 소스 전극(176f)은 데이터선(171)과 동일한 층에 형성되어 있는 트랜지스터 연결부(71)를 통해 서로 연결되어 있다. 트랜지스터 연결부(71)의 일단부는 제1 게이트 절연막(141), 제2 게이트 절연막(142) 및 층간 절연막(160)에 형성된 접촉 구멍(61)을 통해 보상 소스 전극(176c)과 연결되어 있고, 트랜지스터 연결부(71)의 타단부는 제1 게이트 절연막(141), 제2 게이트 절연막(142) 및 층간 절연막(160)에 형성된 접촉 구멍(62)을 통해 발광 제어 소스 전극(176f)과 연결되어 있다. 따라서, 스토리지 캐패시터(Cct)는 연장되어 트랜지스터 연결부(71)와 중첩하고 있고, 구동 반도체층(131a)은 연장되어 트랜지스터 연결부(71)와 중첩하고 있다.

【0107】이와 같이, 트랜지스터 연결부(71)를 통해 보상 소스 전극(176c)과 발광 제어 소스 전극(176f)을 연결함으로써, 보상 소스 전극(176c)과 발광 제어 소

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스 전극(176f) 사이의 이격부(d)까지 구동 반도체층(131a), 제1 스토리지 축전판(125a) 및 제2 스토리지 축전판(127)를 연장할 수 있으므로 스토리지 캐패시터(Cst)를 더욱 확장시킬 수 있다.

【0108】 한편, 상기 제1 실시예에서 구동 반도체층은 굴곡부에서 직접 보상 소스 전극으로 연결되지 않으나, 굴곡부에서 직접 보상 소스 전극으로 분기되는 분기부를 더 포함하는 제4 실시예도 가능하다.

【0109】 이하에서, 도 8을 참조하여, 본 발명의 제4 실시예에 따른 유기 발광 표시 장치에 대해 상세히 설명한다.

【0110】 도 8은 본 발명의 제4 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터의 확대 배치도이다.

【0111】 제4 실시예는 도 1 내지 도 5에 도시된 제1 실시예와 비교하여 구동 반도체층 및 스토리지 캐패시터만을 제외하고 실질적으로 동일한 바 반복되는 설명은 생략한다.

【0112】 도 8에 도시한 바와 같이, 본 발명의 제4 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터(T1)는 구동 반도체층(131a), 구동 게이트 전극(125a), 구동 소스 전극(176a) 및 구동 드레인 전극(177a)을 포함한다. 구동 반도체층(131a)은 굴곡되어 있다. 구동 반도체층(131a)은 제1 방향으로 연장되어 있는 제1 연장부(31), 제1 방향과 다른 제2 방향으로 연장되어 있는 제2 연장부(32) 및 제1 연장부(31)와 제2 연장부(32)를 연결하는 굴곡부(33) 및 굴곡부에서 직접 보상

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소스 전극(176c)으로 분기되는 분기부(34)를 포함한다. 이러한 구동 반도체층(131a)은 전체적으로 'ㅓ' 형상을 가진다. 따라서, 구동 반도체층(131a)의 길이가 길어지므로 구동 게이트 전극(125a)에 인가되는 게이트 전압의 구동 범위(driving range)를 더욱 넓힐 수 있다.

【0113】 분기부(34)는 보상 박막 트랜지스터(T3)와 연결되는 제1 경로 반도체층(CH1)에 해당하고, 제2 연장부(32)는 발광 제어 박막 트랜지스터(T6)와 연결되는 제2 경로 반도체층(CH2)에 해당한다. 그리고, 구동 게이트 전극 즉, 제1 스토리지 축전판(125a)는 구동 반도체층(131a)의 제1 경로 반도체층(CH1) 및 제2 경로 반도체층(CH2)과 중첩하며, 제2 스토리지 축전판(127)는 제1 스토리지 축전판(125a)와 중첩하고 있다. 따라서, 스토리지 캐패시터(Cst)의 면적이 넓어지므로 고해상도에서도 스토리지 캐패시턴스를 용이하게 확보할 수 있다.

【0114】 한편, 상기 제4 실시예에서 제1 경로 반도체층(CH1)과 제2 경로 반도체층(CH2)의 길이가 서로 동일하였으나, 제1 경로 반도체층(CH1)과 제2 경로 반도체층(CH2)의 길이가 서로 다른 제5 실시예도 가능하다.

【0115】 이하에서, 도 9를 참조하여, 본 발명의 제5 실시예에 따른 유기 발광 표시 장치에 대해 상세히 설명한다.

【0116】 도 9는 본 발명의 제5 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터의 확대 배치도이다.

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【0117】 제5 실시예는 도 8에 도시된 제4 실시예와 비교하여 구동 반도체층 및 스토리지 캐패시터만을 제외하고 실질적으로 동일한 바 반복되는 설명은 생략한다.

【0118】 도 9에 도시한 바와 같이, 본 발명의 제5 실시예에 따른 유기 발광 표시 장치의 구동 박막 트랜지스터(T1)는 구동 반도체층(131a), 구동 게이트 전극(125a), 구동 소스 전극(176a) 및 구동 드레인 전극(177a)을 포함한다. 구동 반도체층(131a)은 굴곡되어 있다. 구동 반도체층(131a)은 제1 방향으로 연장되어 있는 제1 연장부(31), 제1 방향과 다른 제2 방향으로 연장되어 있는 제2 연장부(32) 및 제1 연장부(31)와 제2 연장부(32)를 연결하는 굴곡부(33) 및 굴곡부에서 직접 보상 소스 전극(176c)으로 분기되는 분기부(34)를 포함한다. 따라서, 구동 반도체층(131a)의 길이가 길어지므로 구동 게이트 전극(125a)에 인가되는 게이트 전압의 구동 범위(driving range)를 더욱 넓힐 수 있다.

【0119】 분기부(34)는 보상 박막 트랜지스터(T3)와 연결되는 제1 경로 반도체층(CH1)에 해당하고, 제1 연장부(31), 제2 연장부(32) 및 굴곡부(33)를 포함하는 지그재그부(30)는 발광 제어 박막 트랜지스터(T6)와 연결되는 제2 경로 반도체층(CH2)에 해당한다. 그리고, 구동 게이트 전극 즉, 제1 스토리지 축전판(125a)는 구동 반도체층(131a)의 제1 경로 반도체층(CH1) 및 제2 경로 반도체층(CH2)과 중첩하며, 제2 스토리지 축전판(127)는 제1 스토리지 축전판(125a)와 중첩하고 있다. 따라서, 스토리지 캐패시터(Cst)의 면적이 넓어지므로 고해상도에서도 스토리지 캐패시턴스를 용이하게 확보할 수 있다.

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【0120】 또한, 제1 경로 반도체층(CH1)의 길이는 제2 경로 반도체층(CH2)의 길이보다 짧게 형성되어 있다. 이러한 구조를 숏 패스 다이오드(short pass diode) 구조라고 하며, 제1 경로 반도체층(CH1)의 길이와 제2 경로 반도체층(CH2)의 길이가 서로 다르므로 서로 다른 크기의 전류가 동시에 흐를 수 있다. 제1 경로 반도체층(CH1)의 길이는 짧으므로 비교적 큰 전류가 흐를 수 있고, 제2 경로 반도체층(CH2)의 길이는 길기 때문에 비교적 작은 전류가 동시에 흐를 수 있다. 이와 같이, 하나의 구동 박막 트랜지스터로 크기가 서로 다른 전류를 동시에 제공할 수 있는 특징을 이용하여 문턱 전압을 빠르게 보상하는 동시에 유기 발광 다이오드로 일정한 전류를 제공하여 특성 편차를 갖는 구동 박막 트랜지스터들 간의 전류 편차를 감소시킴으로써 전류의 크기 차이로 인한 얼룩을 방지할 수 있으며, 이러한 구동 동작에 대해 구동 동작에 대해 이하에서 상세히 설명한다.

【0121】 구동 박막 트랜지스터(T1)는 스캔 신호(Sn)에 따라 데이터 신호(Dm)에 대응하는 전압을 스토리지 캐패시터(Cst)에 충전하고, 스토리지 캐패시터(Cst)에 충전된 전압에 대응하는 전류를 유기 발광 다이오드(OLED)로 제공한다. 이 때, 구동 박막 트랜지스터(T1)는 시간의 경과에 따라 문턱 전압이 변화될 수 있기 때문에 보상 박막 트랜지스터(T3)는 스캔 신호(Sn)에 따라 구동 박막 트랜지스터(T1)를 다이오드 연결시켜 구동 박막 트랜지스터(T1)의 문턱 전압(Vth)을 보상한다.

【0122】 따라서, 데이터 신호(Dm)가 전달되는 동안 제1 경로 반도체층(CH1)을 통해 흐르는 비교적 큰 전류가 보상 박막 트랜지스터(T3)를 통해 스토리지 캐패

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시터(Cst)를 소정 전압(보상 전압)까지 빠르게 충전시킬 수 있기 때문에 문턱 전압(Vth) 보상이 빠르고 용이하게 이루어질 수 있다.

【0123】 또한, 제2 경로 반도체층(CH2)을 통해 흐른 비교적 작은 전류가 발광 제어 박막 트랜지스터(T6)를 통해 유기 발광 다이오드(OLED)로 제공되기 때문에 얼룩이 방지될 수 있다. 즉, 구동 박막 트랜지스터(T1)의 구동 게이트 전극에 인가되는 전압의 변화에 따른 전류의 변화율이 작기 때문에 전류제어전압폭(data swing range)을 증가시킬 수 있으며, 이에 의해 감마(gamma)를 표현하는 데이터 전압의 범위가 증가할 수 있고, 특성 편차(산포)를 갖는 구동 박막 트랜지스터들 간의 전류 편차가 감소됨으로써 전류의 크기 차이로 인한 얼룩이 방지될 수 있다.

【0124】 종래의 구동 박막 트랜지스터는 구동 반도체층(131a)을 통해 하나의 크기의 전류만을 흐르게 할 수 있으므로, 보상 박막 트랜지스터(T3) 및 발광 제어 박막 트랜지스터(T6)로 동일한 크기의 전류를 제공하게 된다. 이 때, 구동 박막 트랜지스터(T1)의 문턱 전압(Vth)을 빠르게 보상하도록 구동 박막 트랜지스터(T1)의 구동 반도체층(131a)의 길이를 짧게 형성할 경우 트랜지스터 특성곡선(transfer curve)의 s-팩터(factor)가 감소하여 구동 게이트 전극에 인가되는 전압의 변화에 따른 전류의 변화율이 커지기 때문에 유기 발광 다이오드(OLED)로 큰 전류가 제공되어 얼룩이 발생하게 된다.

【0125】 반대로, 얼룩이 방지되도록 구동 박막 트랜지스터(T1)의 구동 반도체층(131a)의 길이를 길게 형성할 경우 작은 전류에 의해 구동 박막 트랜지스터의 문턱 전압(Vth)이 느리게 보상되므로, 저계조 보상이 이루어지지 않아 얼룩이 발생

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하게 된다. 이러한 문제점은 해상도가 증가할수록 심각하게 나타난다. 즉, 해상도가 증가할수록 데이터 신호(Dm)가 인가되는 시간이 감소하기 때문에 문턱 전압(Vth)이 완전히 보상되기 전에 유기 발광 다이오드(OLED)로 전류가 흐르며, 이는 전류 편차를 유발하여 얼룩이 발생하게 된다.

【0126】 따라서, 보상 박막 트랜지스터(T3)와 연결되는 제1 경로 반도체층(CH1)의 길이를 발광 제어 박막 트랜지스터(T6)와 연결되는 제2 경로 반도체층(CH2)의 길이보다 짧게 형성함으로써, 저계조 얼룩을 방지할 수 있다.

【0127】 한편, 상기 제1 실시예는 6개의 박막 트랜지스터와 1개의 스토리지 캐패시터로 이루어진 6tr 1cap의 구조에서 구동 박막 트랜지스터의 구동 반도체층이 굴곡된 구조이나, 7개의 박막 트랜지스터와 1개의 스토리지 캐패시터로 이루어진 7tr 1cap의 구조에서 구동 박막 트랜지스터의 구동 반도체층이 굴곡된 구조인 제6 실시예도 가능하다.

【0128】 이하에서, 도 10 및 도 11을 참조하여, 본 발명의 제6 실시예에 따른 유기 발광 표시 장치에 대해 상세히 설명한다.

【0129】 도 10은 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 하나의 화소의 등가 회로도이고, 도 11은 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 배치도이다.

【0130】 제6 실시예는 도 1 내지 도 5에 도시된 제1 실시예와 비교하여 전류 제어 박막 트랜지스터가 추가된 것만을 제외하고 실질적으로 동일한 바 반복되는

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설명은 생략한다.

【0131】 도 10 및 도 11에 도시한 바와 같이, 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 하나의 화소는 복수의 신호선(121, 122, 123, 124, 128, 171, 172), 복수의 신호선에 연결되어 있는 복수개의 박막 트랜지스터(T1, T2, T3, T4, T5, T6, T7), 스토리지 캐패시터(storage capacitor, Cst) 및 유기 발광 다이오드(organic light emitting diode, OLED)를 포함한다.

【0132】 박막 트랜지스터는 구동 박막 트랜지스터(driving thin film transistor)(T1), 스위칭 박막 트랜지스터(switching thin film transistor)(T2), 보상 박막 트랜지스터(T3), 초기화 박막 트랜지스터(T4), 동작 제어 박막 트랜지스터(T5), 발광 제어 박막 트랜지스터(T6) 및 전류 제어 박막 트랜지스터(T7)를 포함한다.

【0133】 신호선은 스캔 신호(Sn)를 전달하는 스캔선(121), 초기화 박막 트랜지스터(T4)에 이전 스캔 신호(Sn-1)를 전달하는 이전 스캔선(122), 동작 제어 박막 트랜지스터(T5) 및 발광 제어 박막 트랜지스터(T6)에 발광 제어 신호(En)를 전달하는 발광 제어선(123), 스캔선(121)과 교차하며 데이터 신호(Dm)를 전달하는 데이터선(171), 구동 전압(ELVDD)을 전달하며 데이터선(171)과 거의 평행하게 형성되어 있는 구동 전압선(172), 구동 박막 트랜지스터(T1)를 초기화하는 초기화 전압(Vint)을 전달하는 초기화 전압선(124) 및 바이패스 박막 트랜지스터(T7)에 바이패스 신호(BP)를 전달하는 바이패스 제어선(128)을 포함한다.

【0134】 구동 박막 트랜지스터(T1)의 게이트 전극(G1)은 스토리지 캐패시터

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(Cst)의 일단(Cst1)과 연결되어 있고, 구동 박막 트랜지스터(T1)의 소스 전극(S1)은 동작 제어 박막 트랜지스터(T5)를 경유하여 구동 전압선(172)과 연결되어 있으며, 구동 박막 트랜지스터(T1)의 드레인 전극(D1)은 발광 제어 박막 트랜지스터(T6)를 경유하여 유기 발광 다이오드(OLED)의 애노드(anode)와 전기적으로 연결되어 있다.

【0135】 스위칭 박막 트랜지스터(T2)의 게이트 전극(G2)은 스캔선(121)과 연결되어 있고, 스위칭 박막 트랜지스터(T2)의 소스 전극(S2)은 데이터선(171)과 연결되어 있으며, 스위칭 박막 트랜지스터(T2)의 드레인 전극(D2)은 구동 박막 트랜지스터(T1)의 소스 전극(S1)과 연결되어 있으면서 동작 제어 박막 트랜지스터(T5)을 경유하여 구동 전압선(172)과 연결되어 있다.

【0136】 초기화 박막 트랜지스터(T4)의 게이트 전극(G4)은 이전 스캔선(122)과 연결되어 있고, 초기화 박막 트랜지스터(T4)의 소스 전극(S4)은 초기화 전압선(124)과 연결되어 있으며, 초기화 박막 트랜지스터(T4)의 드레인 전극(D4)은 스토리지 캐패시터(Cst)의 일단(Cst1), 보상 박막 트랜지스터(T3)의 드레인 전극(D3) 및 구동 박막 트랜지스터(T1)의 게이트 전극(G1)과 함께 연결되어 있다.

【0137】 바이패스 박막 트랜지스터(T7)의 게이트 전극(G7)은 바이패스 제어선(128)과 연결되어 있고, 바이패스 박막 트랜지스터(T7)의 소스 전극(S7)은 발광 제어 박막 트랜지스터(T6)의 드레인 전극(D6) 및 유기 발광 다이오드(OLED)의 애노드와 함께 연결되어 있고, 바이패스 박막 트랜지스터(T7)의 드레인 전극(D7)은 초기화 전압선(124) 및 초기화 박막 트랜지스터(T4)의 소스 전극(S4)에 함께 연결되

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어 있다.

【0138】 이하에서 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 바이패스 박막 트랜지스터(T7)의 구체적인 동작 과정을 상세히 설명한다.

【0139】 바이패스 박막 트랜지스터(T7)는 바이패스 제어선(128)으로부터 바이패스 신호(BP)를 전달받는다. 바이패스 신호(BP)는 바이패스 박막 트랜지스터(T7)를 항상 오프시킬 수 있는 소정 레벨의 전압으로서, 바이패스 박막 트랜지스터(T7)는 트랜지스터 오프 레벨의 전압을 게이트 전극(G7)에 전달받게 됨으로써, 바이패스 트랜지스터(T7)가 항상 오프되고, 오프된 상태에서 구동 전류(Id)의 일부는 바이패스 전류(Ibp)로 바이패스 트랜지스터(T7)를 통해 빠져나가게 한다.

【0140】 블랙 영상을 표시하는 구동 박막 트랜지스터의 최소 전류가 구동 전류로 흐를 경우에도 유기 발광 다이오드(OLED)가 발광하게 된다면 제대로 블랙 영상이 표시되지 않는다. 따라서, 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 바이패스 박막 트랜지스터(T7)는 구동 박막 트랜지스터(T1)의 최소 전류의 일부를 바이패스 전류(Ibp)로서 유기 발광 다이오드 쪽의 전류 경로 외의 다른 전류 경로로 분산시킬 수 있다. 여기서 구동 박막 트랜지스터의 최소 전류란 구동 박막 트랜지스터의 게이트-소스 전압(Vgs)이 문턱 전압(Vth)보다 작아서 구동 박막 트랜지스터가 오프되는 조건에서의 전류를 의미한다. 이렇게 구동 박막 트랜지스터를 오프시키는 조건에서의 최소 구동 전류(예를 들어 10pA 이하의 전류)가 유기 발광 다이오드에 전달되어 블랙 휘도의 영상으로 표현된다.

【0141】 블랙 영상을 표시하는 최소 구동 전류가 흐르는 경우 바이패스 전류

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(Ibp)의 우회 전달의 영향이 큰 반면, 일반 영상 또는 화이트 영상과 같은 영상을 표시하는 큰 구동 전류가 흐를 경우에는 바이패스 전류(Ibp)의 영향이 거의 없다고 할 수 있다. 따라서, 블랙 영상을 표시하는 구동 전류가 흐를 경우에 구동 전류(Id)로부터 바이패스 박막 트랜지스터(T7)를 통해 빠져나온 바이패스 전류(Ibp)의 전류량만큼 감소된 유기 발광 다이오드의 발광 전류(Ioled)는 블랙 영상을 확실하게 표현할 수 있는 수준으로 최소의 전류량을 가지게 된다.

【0142】 따라서, 바이패스 박막 트랜지스터를 이용하여 정확한 블랙 휘도 영상을 구현하여 콘트라스트비를 향상시킬 수 있다.

【0143】 그러면 도 10에 도시한 유기 발광 표시 장치의 화소의 상세 구조에 대하여 도 11을 도 10 및 도 3과 함께 참고하여 상세하게 설명한다.

【0144】 도 11은 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 배치도이다.

【0145】 도 10 및 도 11에 도시한 바와 같이, 본 발명의 제6 실시예에 따른 유기 발광 표시 장치의 화소는 스캔 신호(Sn), 이전 스캔 신호(Sn-1), 발광 제어 신호(En) 및 초기화 전압(Vint)을 각각 인가하며 행 방향을 따라 형성되어 있는 스캔선(121), 이전 스캔선(122), 발광 제어선(123), 초기화 전압선(124) 및 바이패스 제어선(128)을 포함하고, 스캔선(121), 이전 스캔선(122), 발광 제어선(123), 초기화 전압선(124) 및 바이패스 제어선(128) 모두와 교차하고 있으며 화소에 데이터 신호(Dm) 및 구동 전압(ELVDD)을 각각 인가하는 데이터선(171) 및 구동 전압선(172)을 포함한다.

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【0146】 또한, 화소에는 구동 박막 트랜지스터(T1), 스위칭 박막 트랜지스터(T2), 보상 박막 트랜지스터(T3), 초기화 박막 트랜지스터(T4), 동작 제어 박막 트랜지스터(T5), 발광 제어 박막 트랜지스터(T6), 바이패스 박막 트랜지스터(T7), 스토리지 캐패시터(Cst), 그리고 유기 발광 다이오드(OLED)(70)가 형성되어 있다.

【0147】 구동 박막 트랜지스터(T1), 스위칭 박막 트랜지스터(T2), 보상 박막 트랜지스터(T3), 초기화 박막 트랜지스터(T4), 동작 제어 박막 트랜지스터(T5), 발광 제어 박막 트랜지스터(T6) 및 바이패스 박막 트랜지스터(T7)는 반도체층(131)을 따라 형성되어 있으며, 반도체층(131)은 다양한 형상으로 굴곡되어 형성되어 있다. 이러한 반도체층(131)은 폴리 실리콘으로 이루어지며, 불순물이 도핑되지 않은 채널 영역과, 채널 영역의 양 옆으로 불순물이 도핑되어 형성된 소스 영역 및 드레인 영역을 포함한다. 여기서, 이러한 불순물은 박막 트랜지스터의 종류에 따라 달라지며, N형 불순물 또는 P형 불순물이 가능하다. 이러한 반도체층은 구동 박막 트랜지스터(T1)에 형성되는 구동 반도체층(131a), 스위칭 박막 트랜지스터(T2)에 형성되는 스위칭 반도체층(131b), 보상 박막 트랜지스터(T3)에 형성되는 보상 반도체층(131c), 초기화 박막 트랜지스터(T4)에 형성되는 초기화 반도체층(131d), 동작 제어 박막 트랜지스터(T5)에 형성되는 동작 제어 반도체층(131e), 발광 제어 박막 트랜지스터(T6)에 형성되는 발광 제어 반도체층(131f) 및 바이패스 박막 트랜지스터(T7)에 형성되는 바이패스 반도체층(131g)을 포함한다.

【0148】 구동 박막 트랜지스터(T1)는 구동 반도체층(131a), 구동 게이트 전극(125a), 구동 소스 전극(176a) 및 구동 드레인 전극(177a)을 포함한다. 구동 반

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도체층(131a)은 굴곡되어 있다. 구동 반도체층(131a)은 제1 방향으로 연장되어 있는 복수개의 제1 연장부(31), 제1 방향과 다른 제2 방향으로 연장되어 있는 복수개의 제2 연장부(32) 및 제1 연장부(31)와 제2 연장부(32)를 연결하는 복수개의 굴곡부(33)를 포함한다. 따라서, 구동 반도체층(131a)은 지그재그 형상으로 배치될 수 있다. 도 2 및 도 3에 도시한 구동 반도체층(131a)은 3개의 제1 연장부(31), 2개의 제2 연장부(32) 및 4개의 굴곡부(33)를 포함한다. 따라서, 구동 반도체층(131a)은 'ㄹ' 형상으로 길게 배치되어 있다.

【0149】 이와 같이, 복수개의 굴곡부(33)를 포함하는 구동 반도체층(131a)을 형성함으로써, 좁은 공간 내에 길게 구동 반도체층(131a)을 형성할 수 있다. 따라서, 구동 반도체층(131a)의 구동 채널 영역(131a1)을 길게 형성할 수 있으므로 구동 게이트 전극(125a)에 인가되는 게이트 전압의 구동 범위(driving range)는 넓어지게 된다. 따라서, 게이트 전압의 구동 범위가 넓으므로 게이트 전압의 크기를 변화시켜 유기 발광 다이오드(OLED)에서 방출되는 빛의 계조를 보다 세밀하게 제어할 수 있으며, 그 결과 유기 발광 표시 장치의 해상도를 높이고 표시 품질을 향상시킬 수 있다.

【0150】 바이패스 박막 트랜지스터(T7)는 바이패스 반도체층(131g), 바이패스 게이트 전극(125g), 바이패스 소스 전극(176g) 및 바이패스 드레인 전극(177g)을 포함한다. 바이패스 소스 전극(176g)은 바이패스 반도체층(131g)에서 불순물이 도핑된 바이패스 드레인 영역(177g)에 해당하고, 바이패스 드레인 전극(177g)은 바이패스 반도체층(131g)에서 불순물이 도핑된 바이패스 드레인 영역(177g)에 해당한

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다. 바이패스 소스 전극(176g)은 발광 제어 드레인 영역(133f)과 직접 연결되어 있다.

【0151】 바이패스 반도체층(131g)은 구동 반도체층(131a), 스위칭 반도체층(131b), 발광 제어 반도체층(131f) 등과 동일한 층에 형성되어 있고, 바이패스 반도체층(131g) 위에는 제1 게이트 절연막(141)이 형성되어 있다. 제1 게이트 절연막(141) 위에는 바이패스 제어선(128)의 일부인 바이패스 게이트 전극(125g)이 형성되어 있고, 바이패스 게이트 전극(125g) 및 제1 게이트 절연막(141) 위에는 제2 게이트 절연막(142)이 형성되어 있다.

【0152】 따라서, 바이패스 박막 트랜지스터(T7)는 바이패스 제어선(128)으로부터 바이패스 신호(BP)를 전달받아 바이패스 트랜지스터(T7)가 항상 오프되고, 오프된 상태에서 구동 전류(Id)의 일부가 바이패스 전류(Ibp)로 바이패스 트랜지스터(T7)를 통해 빠져나가게 한다. 따라서, 블랙 영상을 표시하는 구동 전류가 흐를 경우에 정확한 블랙 휘도 영상을 구현하여 콘트라스트비를 향상시킬 수 있다.

【0153】 본 발명을 앞서 기재한 바에 따라 바람직한 실시예를 통해 설명하였지만, 본 발명은 이에 한정되지 않으며 다음에 기재하는 특허청구범위의 개념과 범위를 벗어나지 않는 한, 다양한 수정 및 변형이 가능하다는 것을 본 발명이 속하는 기술 분야에 종사하는 자들은 쉽게 이해할 것이다.

【부호의 설명】

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【0154】31: 제1 연장부　　32: 제2 연장부

33: 굴곡부　　110: 기판

121: 스캔선　　122: 이전 스캔선

123: 발광 제어선　　124: 초기화 전압선

125a: 구동 게이트 전극　　125b: 스위칭 게이트 전극

131a: 구동 반도체층　　132b: 스위칭 반도체층

141: 제1 게이트 절연막　　142: 제2 게이트 절연막

171: 데이터선　　172: 구동 전압선

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【특허청구범위】

【청구항 1】

기판,

상기 기판 위에 형성되어 있으며 스캔 신호를 전달하는 스캔선,

상기 스캔선과 교차하며 데이터 신호 및 구동 전압을 각각 전달하는 데이터선 및 구동 전압선,

상기 스캔선 및 상기 데이터선과 연결되어 있는 스위칭 박막 트랜지스터,

상기 스위칭 박막 트랜지스터의 스위칭 드레인 전극과 연결되어 있는 구동 박막 트랜지스터,

상기 구동 박막 트랜지스터의 구동 드레인 전극에 연결되어 있는 유기 발광 다이오드

를 포함하고,

상기 구동 박막 트랜지스터의 구동 반도체층은 굴곡되어 있는 유기 발광 표시 장치.

【청구항 2】

제1항에서,

상기 구동 반도체층을 덮고 있는 제1 게이트 절연막,

상기 제1 게이트 절연막 위에 형성되어 있으며 상기 구동 반도체층과 중첩하고 있는 스토리지 캐패시터를 더 포함하는 유기 발광 표시 장치.

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【청구항 3】

제2항에서,

상기 스토리지 캐패시터는

상기 제1 게이트 절연막 위에 형성되어 있으며 상기 구동 반도체층과 중첩하고 있는 제1 스토리지 축전판,

상기 제1 스토리지 축전판을 덮고 있는 제2 게이트 절연막,

상기 제2 게이트 절연막 위에 형성되어 있으며 상기 제1 스토리지 축전판과 중첩하고 있는 제2 스토리지 축전판을 포함하는 유기 발광 표시 장치.

【청구항 4】

제3항에서,

상기 구동 반도체층은 복수개의 굴곡부를 포함하는 유기 발광 표시 장치.

【청구항 5】

제4항에서,

상기 구동 반도체층은 제1 방향으로 연장되어 있는 복수개의 제1 연장부와 상기 제1 방향과 다른 제2 방향으로 연장되어 있는 복수개의 제2 연장부를 포함하고,

상기 굴곡부는 상기 제1 연장부와 상기 제2 연장부를 연결하는 유기 발광 표시 장치.

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【청구항 6】

제5항에서,

상기 구동 박막 트랜지스터의 문턱 전압을 보상하며 상기 구동 박막 트랜지스터에 연결되어 있는 보상 박막 트랜지스터를 더 포함하는 유기 발광 표시 장치.

【청구항 7】

제6항에서,

발광 제어선에 의해 전달된 발광 제어 신호에 의해 턴온되어 구동 전압을 상기 구동 박막 트랜지스터에서 상기 유기 발광 다이오드로 전달하는 발광 제어 박막 트랜지스터를 더 포함하고,

상기 발광 제어 박막 트랜지스터는 상기 구동 박막 트랜지스터의 구동 드레인 전극과 상기 유기 발광 다이오드 사이에 위치하는 유기 발광 표시 장치.

【청구항 8】

제7항에서,

상기 보상 박막 트랜지스터의 보상 소스 전극과 상기 발광 제어 박막 트랜지스터의 발광 제어 소스 전극은 트랜지스터 연결부를 통해 서로 연결되어 있고,

상기 스토리지 캐패시터는 연장되어 상기 트랜지스터 연결부와 중첩하고 있는 유기 발광 표시 장치.

【청구항 9】

제8항에서,

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상기 구동 반도체층은 연장되어 상기 트랜지스터 연결부와 중첩하고 있는 유기 발광 표시 장치.

【청구항 10】

제9항에서,

상기 트랜지스터 연결부는 상기 데이터선과 동일한 층에 형성되어 있으며, 상기 층간 절연막에 형성된 접촉 구멍을 통해 상기 보상 소스 전극과 상기 발광 제어 소스 전극과 연결되어 있는 유기 발광 표시 장치.

【청구항 11】

제6항에서,

상기 구동 반도체층은 상기 굴곡부에서 분기되는 분기부를 더 포함하는 유기 발광 표시 장치.

【청구항 12】

제11항에서,

상기 스토리지 캐패시터는 연장되어 상기 분기부와 중첩하고 있는 유기 발광 표시 장치.

【청구항 13】

제6항에서,

상기 구동 반도체층은 상기 보상 박막 트랜지스터와 연결되는 제1 경로 반도체층, 상기 발광 제어 박막 트랜지스터와 연결되는 제2 경로 반도체층을 포함하고,

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상기 제1 경로 반도체층의 길이는 상기 제2 경로 반도체층의 길이보다 짧은 유기 발광 표시 장치.

【청구항 14】

제13항에서,

상기 스토리지 캐패시터는 연장되어 상기 제1 경로 반도체층 및 상기 제2 경로 반도체층과 중첩하고 있는 유기 발광 표시 장치.

【청구항 15】

제6항에서,

상기 제2 스토리지 축전판을 덮고 있는 층간 절연막,

상기 층간 절연막 위에 형성되어 있으며, 상기 제2 게이트 절연막 및 상기 층간 절연막에 형성된 접촉 구멍을 통해 상기 제1 스토리지 축전판과 연결되어 있는 연결 부재,

상기 층간 절연막 및 상기 연결 부재를 덮고 있는 보호막

을 더 포함하고,

상기 연결 부재는 상기 보상 박막 트랜지스터의 보상 드레인 전극과 연결되어 있는 유기 발광 표시 장치.

【청구항 16】

제15항에서,

상기 스캔선은 상기 제1 스토리지 축전판과 동일한 층에 형성되어 있고,

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상기 데이터선 및 구동 전압선은 상기 연결 부재와 동일한 층에 형성되어 있는 유기 발광 표시 장치.

【청구항 17】

제16항에서,

상기 구동 전압선은 상기 층간 절연막에 형성된 접촉 구멍을 통해 상기 제2 스토리지 축전판과 연결되어 있는 유기 발광 표시 장치.

【청구항 18】

제17항에서,

상기 발광 제어선에 의해 전달된 발광 제어 신호에 의해 턴온되어 상기 구동 전압을 상기 구동 박막 트랜지스터로 전달하는 동작 제어 박막 트랜지스터를 더 포함하고,

상기 동작 제어 박막 트랜지스터는 상기 구동 전압선과 상기 구동 박막 트랜지스터의 구동 소스 전극 사이에 위치하는 유기 발광 표시 장치.

【청구항 19】

제18항에서,

이전 스캔선을 통해 전달받은 이전 스캔 신호에 따라 턴 온되어 초기화 전압을 상기 구동 박막 트랜지스터의 구동 게이트 전극에 전달하는 초기화 박막 트랜지스터를 더 포함하고,

상기 초기화 박막 트랜지스터는 상기 초기화 전압선과 상기 구동 박막 트랜

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지스터의 구동 게이트 전극 사이에 위치하는 유기 발광 표시 장치.

【청구항 20】

제19항에서,

바이패스 제어선에 의해 전달된 바이패스 제어 신호에 의해 상기 구동 박막 트랜지스터가 전달하는 구동 전류의 일부를 바이패스시키는 바이패스 박막 트랜지스터를 더 포함하고,

상기 바이패스 박막 트랜지스터는 상기 초기화 전압선과 상기 발광 제어 박막 트랜지스터의 발광 제어 드레인 전극 사이에 위치하는 유기 발광 표시 장치.

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【요약서】

【요약】

본 발명에 따른 유기 발광 표시 장치는 기판, 상기 기판 위에 형성되어 있으며 스캔 신호를 전달하는 스캔선, 상기 스캔선과 교차하며 데이터 신호 및 구동 전압을 각각 전달하는 데이터선 및 구동 전압선, 상기 스캔선 및 상기 데이터선과 연결되어 있는 스위칭 박막 트랜지스터, 상기 스위칭 박막 트랜지스터의 스위칭 드레인 전극과 연결되어 있는 구동 박막 트랜지스터, 상기 구동 박막 트랜지스터의 구동 드레인 전극에 연결되어 있는 유기 발광 다이오드를 포함하고, 상기 구동 박막 트랜지스터의 구동 반도체층은 굴곡되어 있을 수 있다. 따라서, 본 발명에 따른 유기 발광 표시 장치는 복수개의 굴곡부를 포함하는 구동 반도체층을 형성함으로써, 구동 반도체층의 구동 채널 영역을 길게 형성할 수 있으므로 구동 게이트 전극에 인가되는 게이트 전압의 구동 범위(driving range)를 넓힐 수 있다.

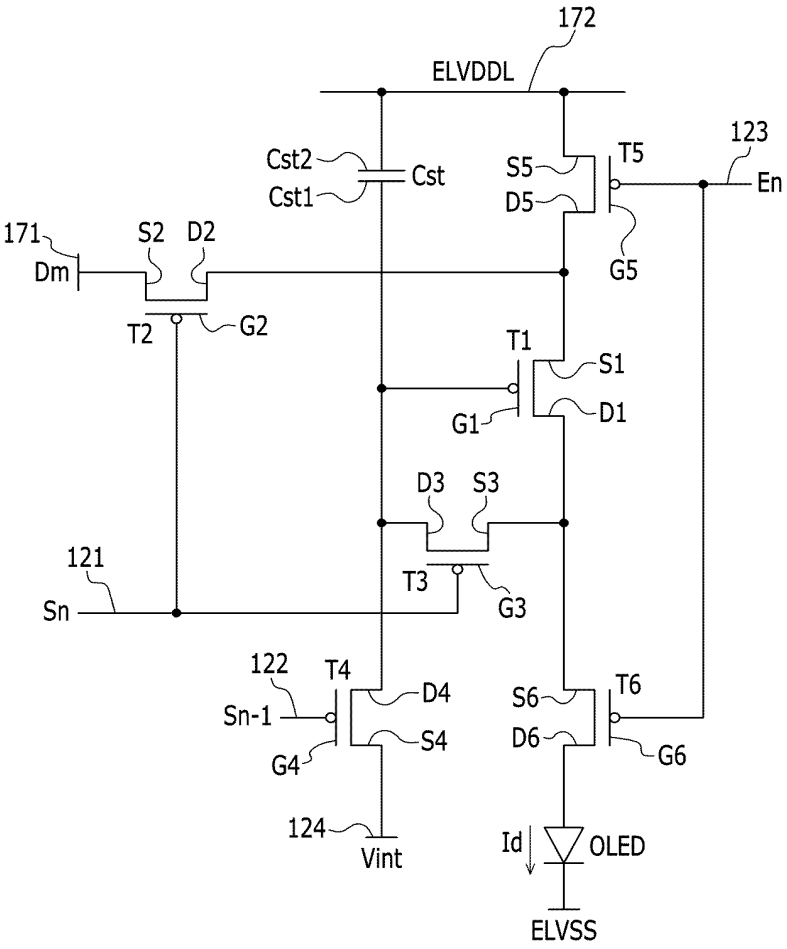
【대표도】

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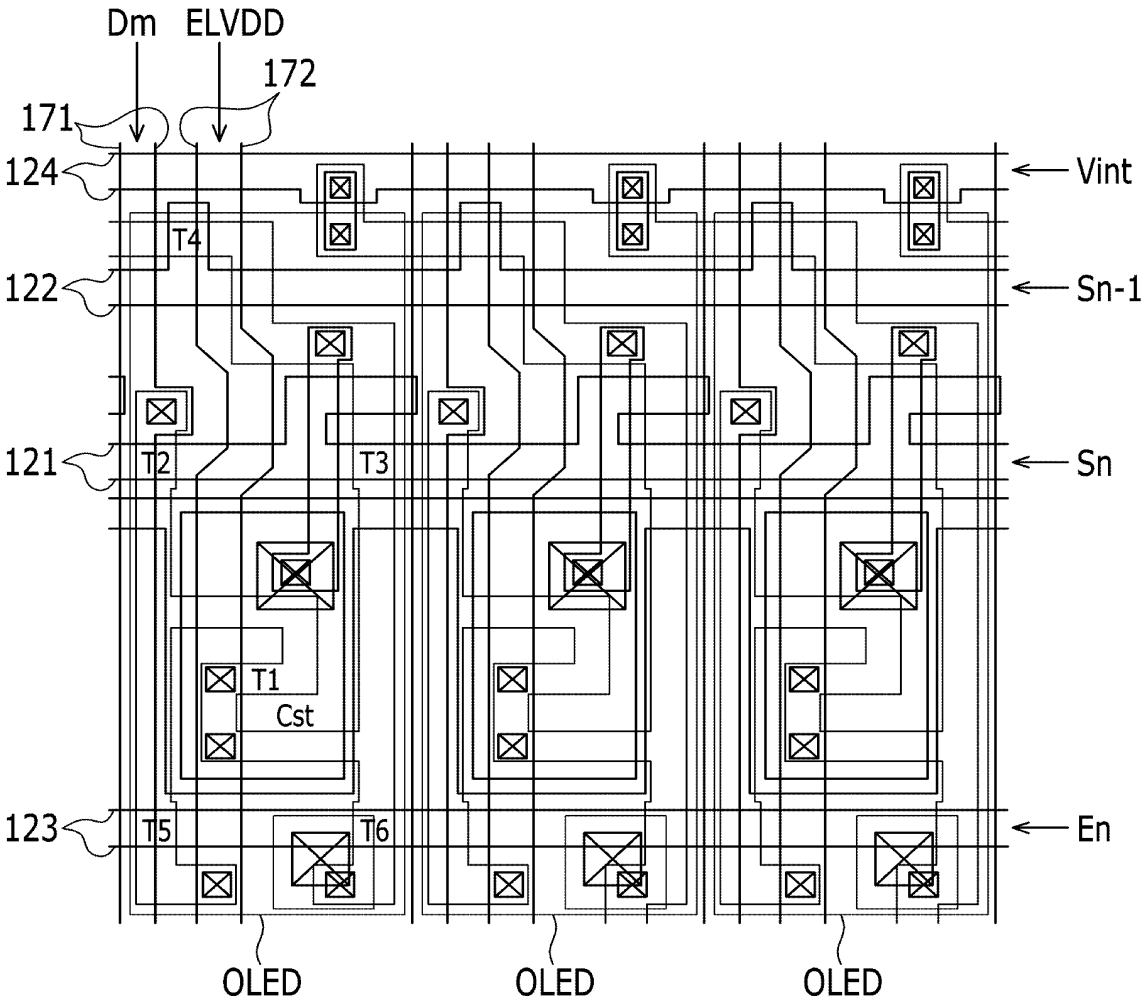
【도면】

【도 1】



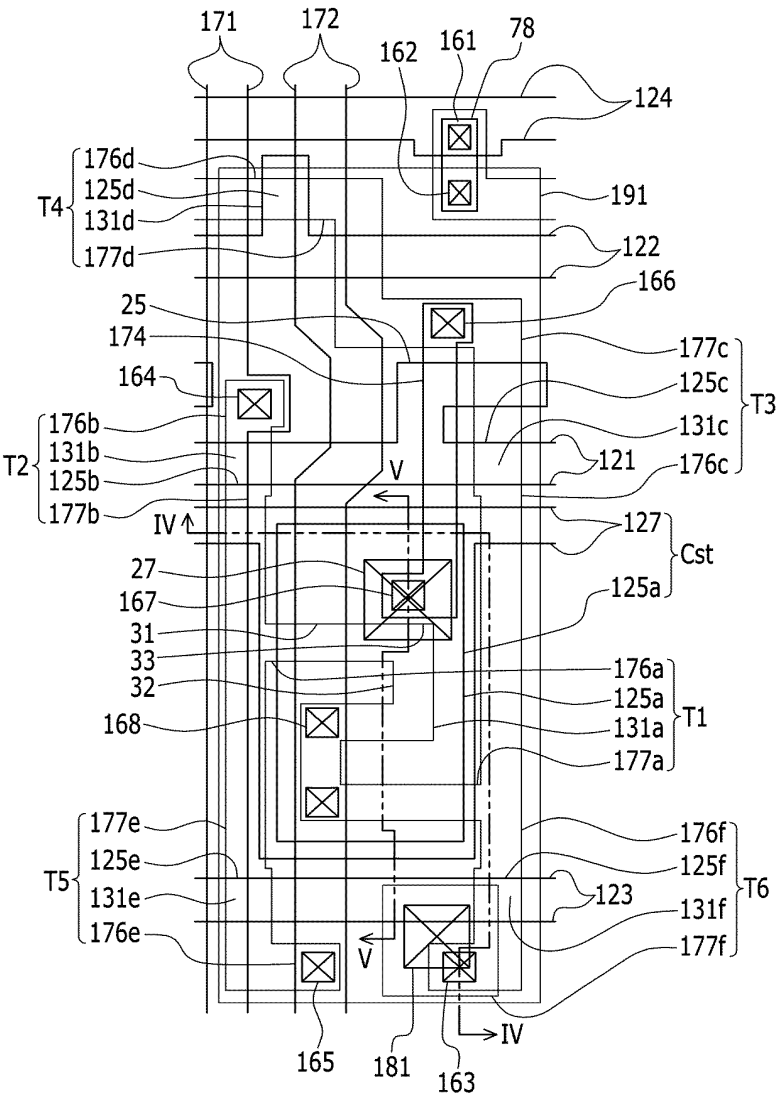
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【도 2】



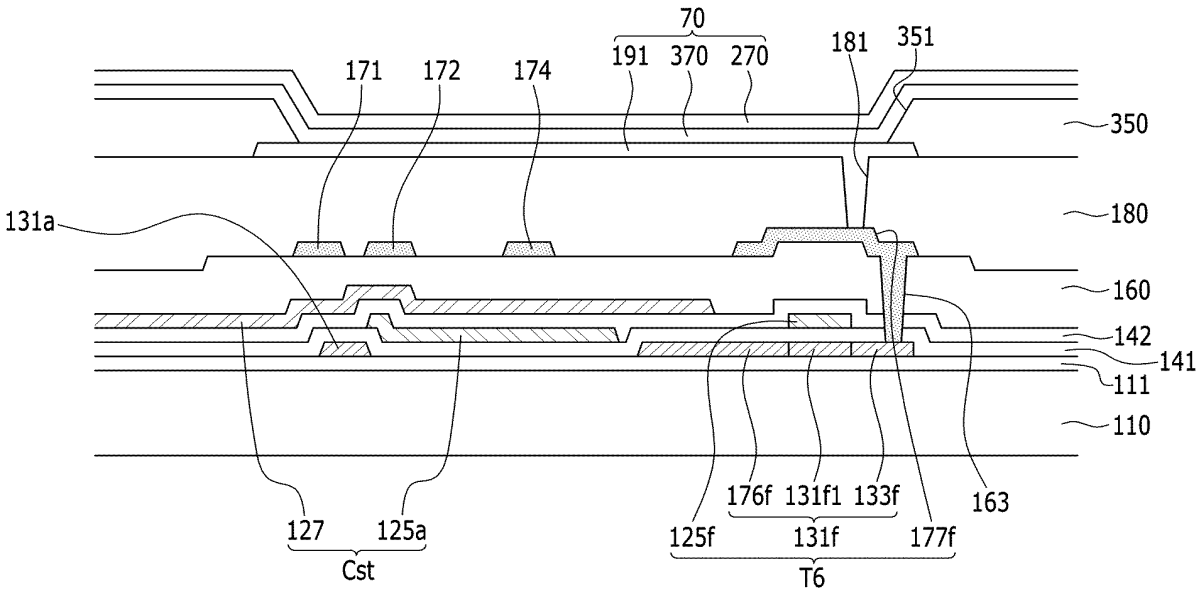
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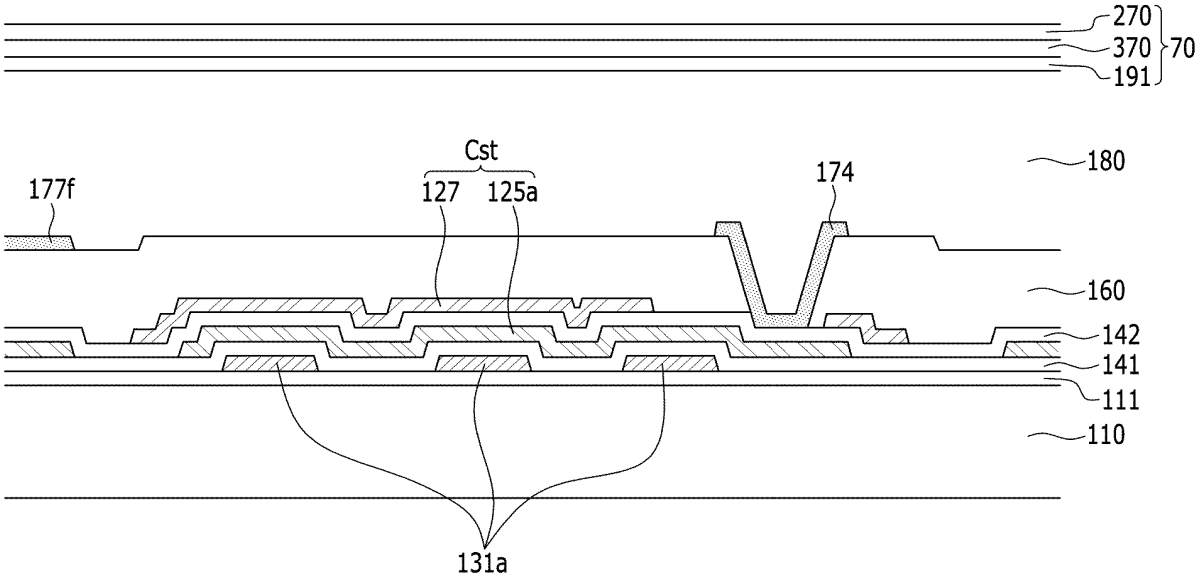


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【도 4】

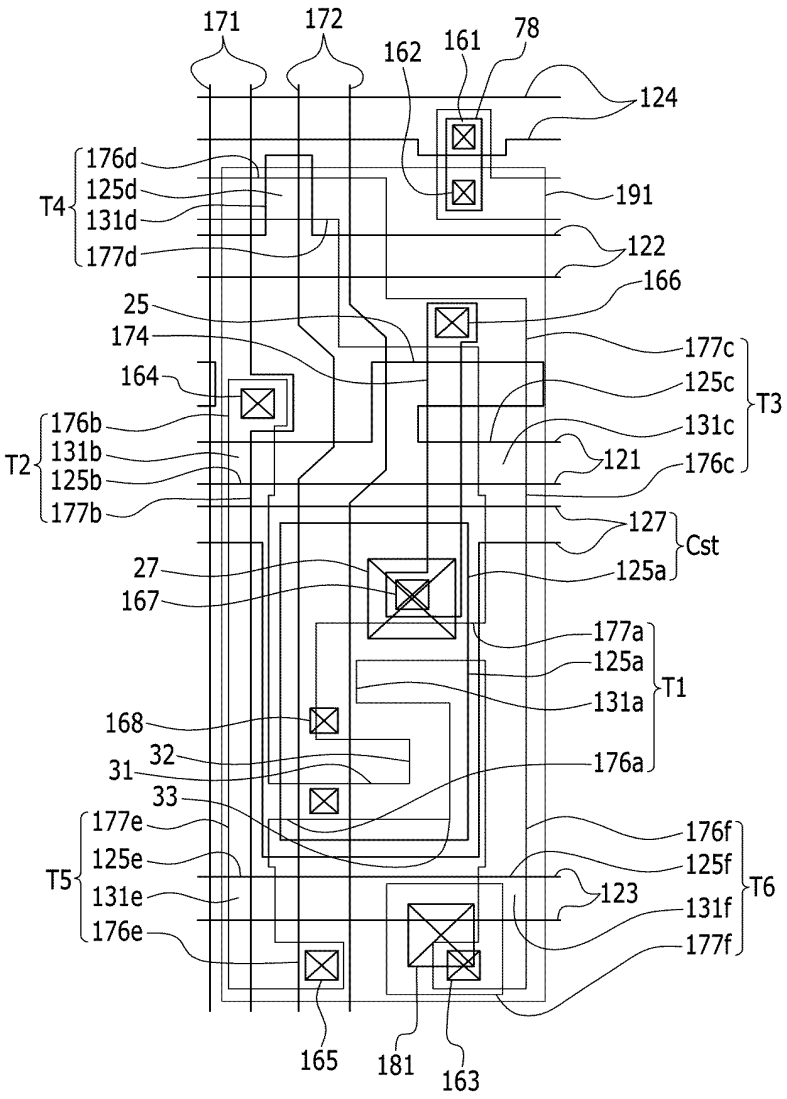


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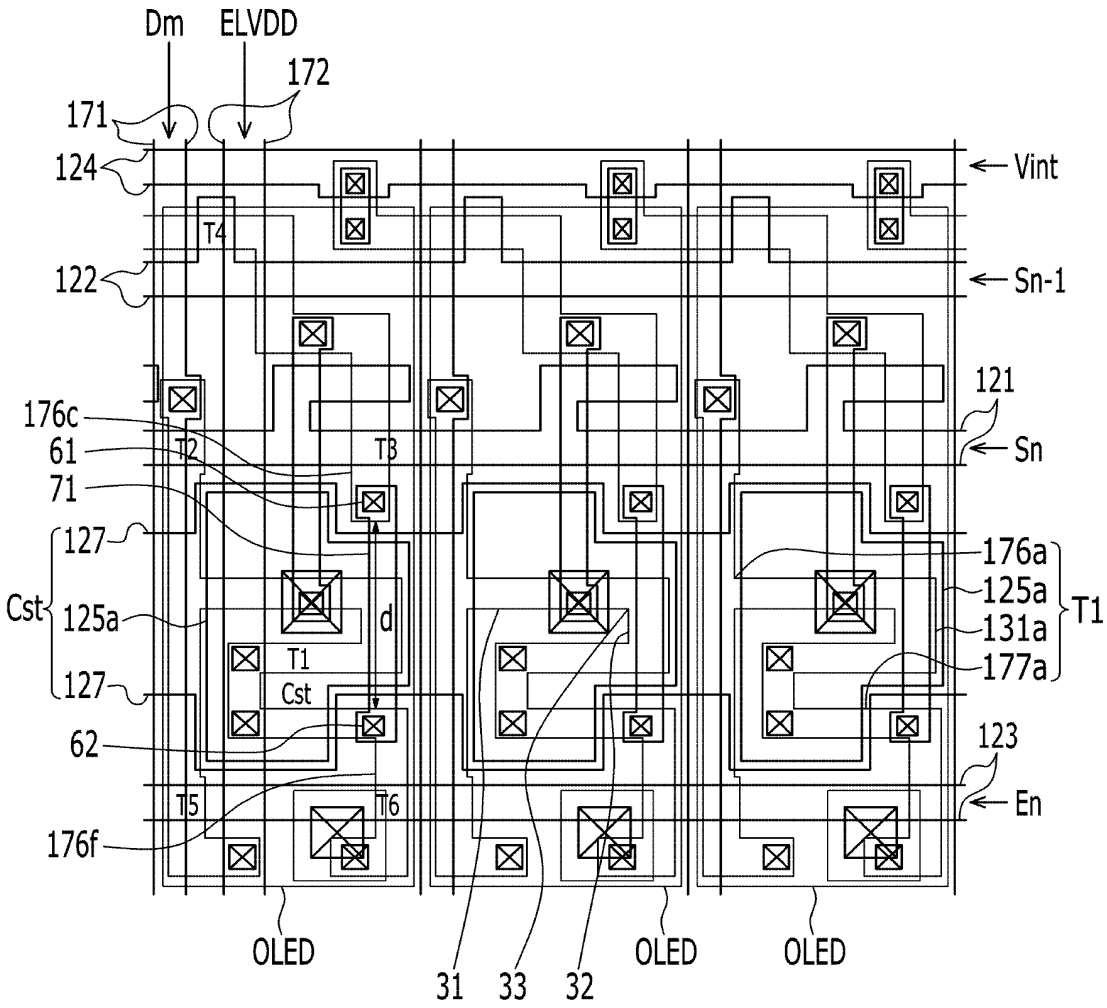
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【도 6】



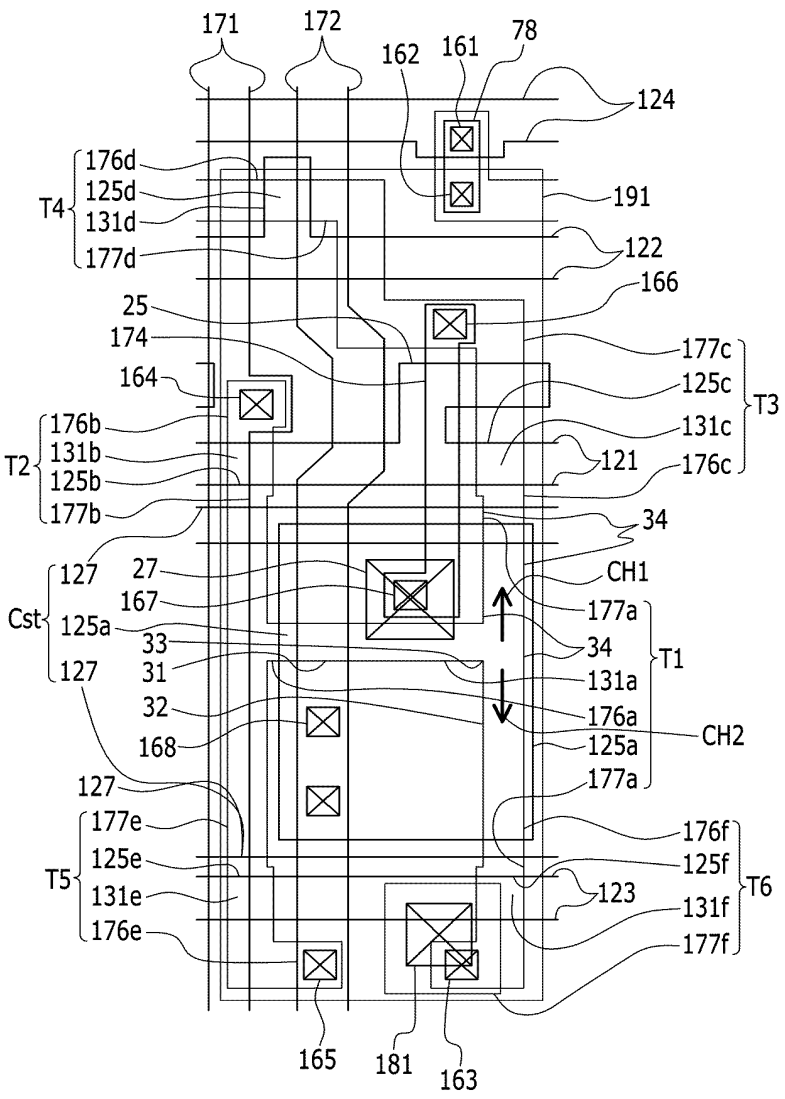
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【도 7】



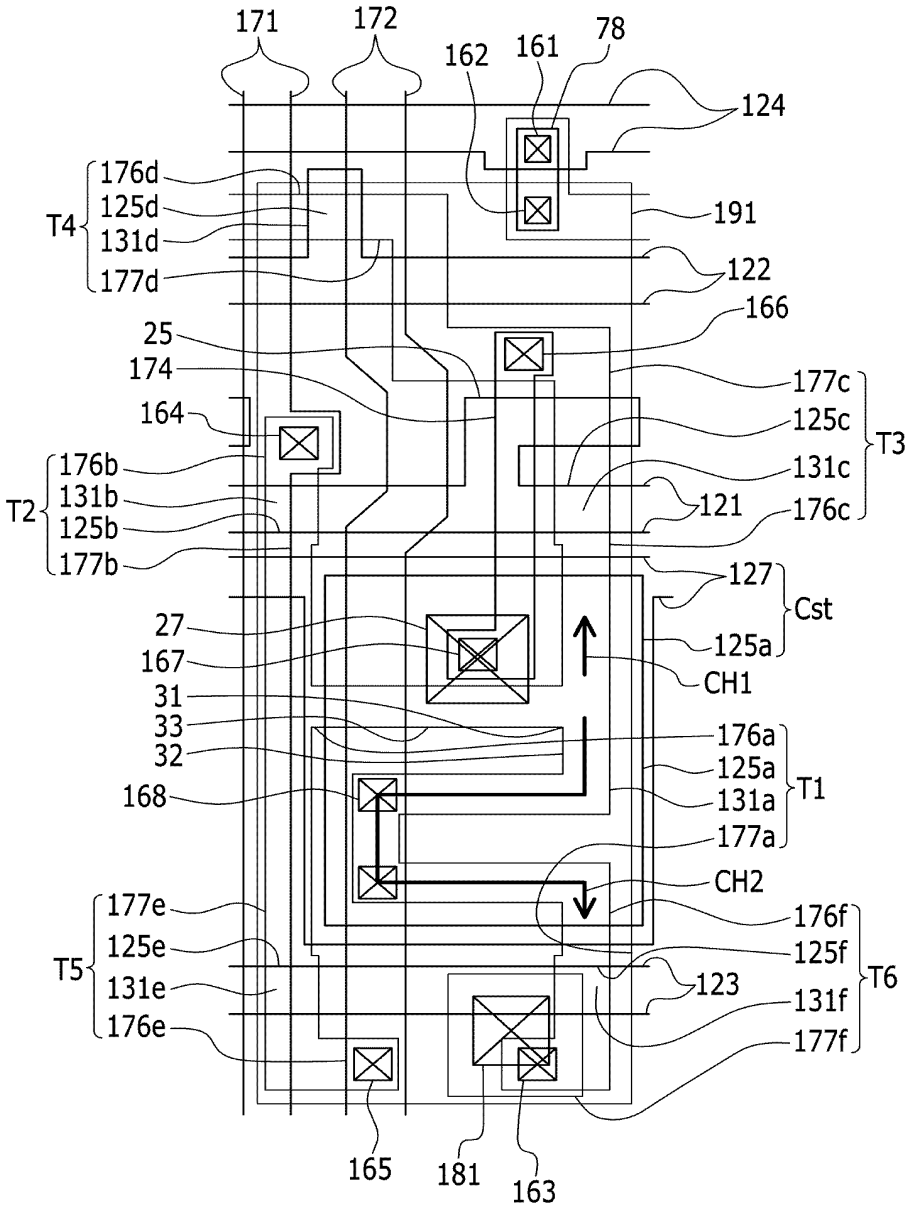
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【도 8】



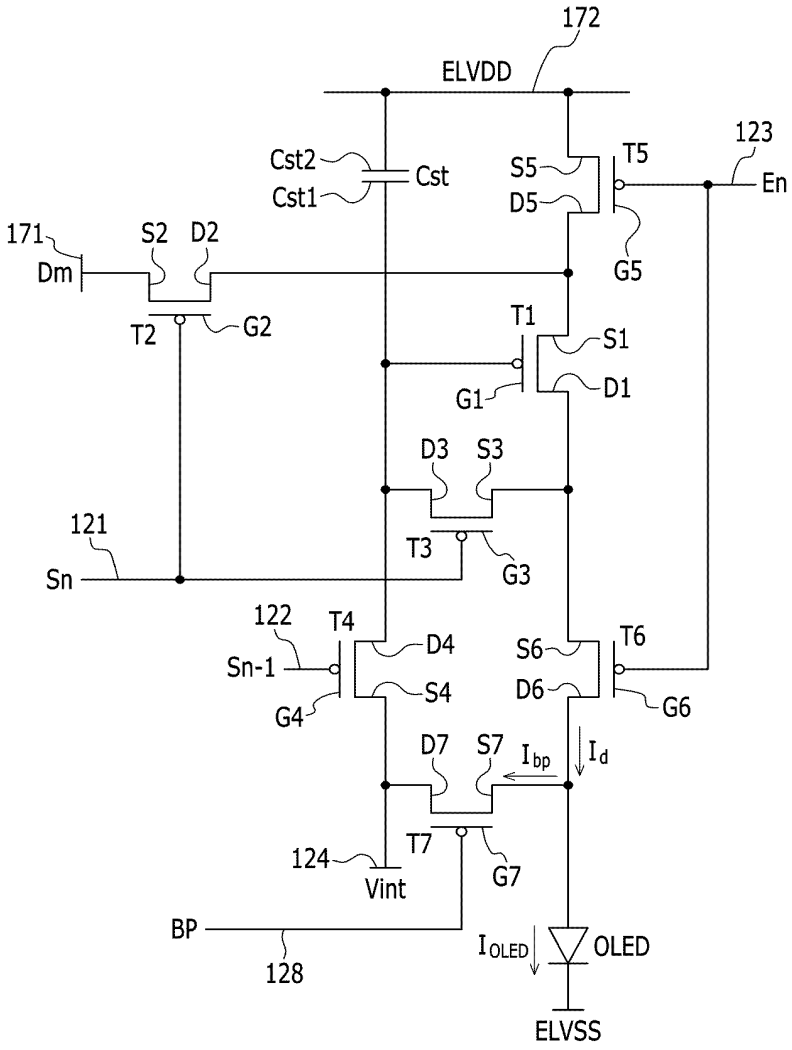
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【도 9】



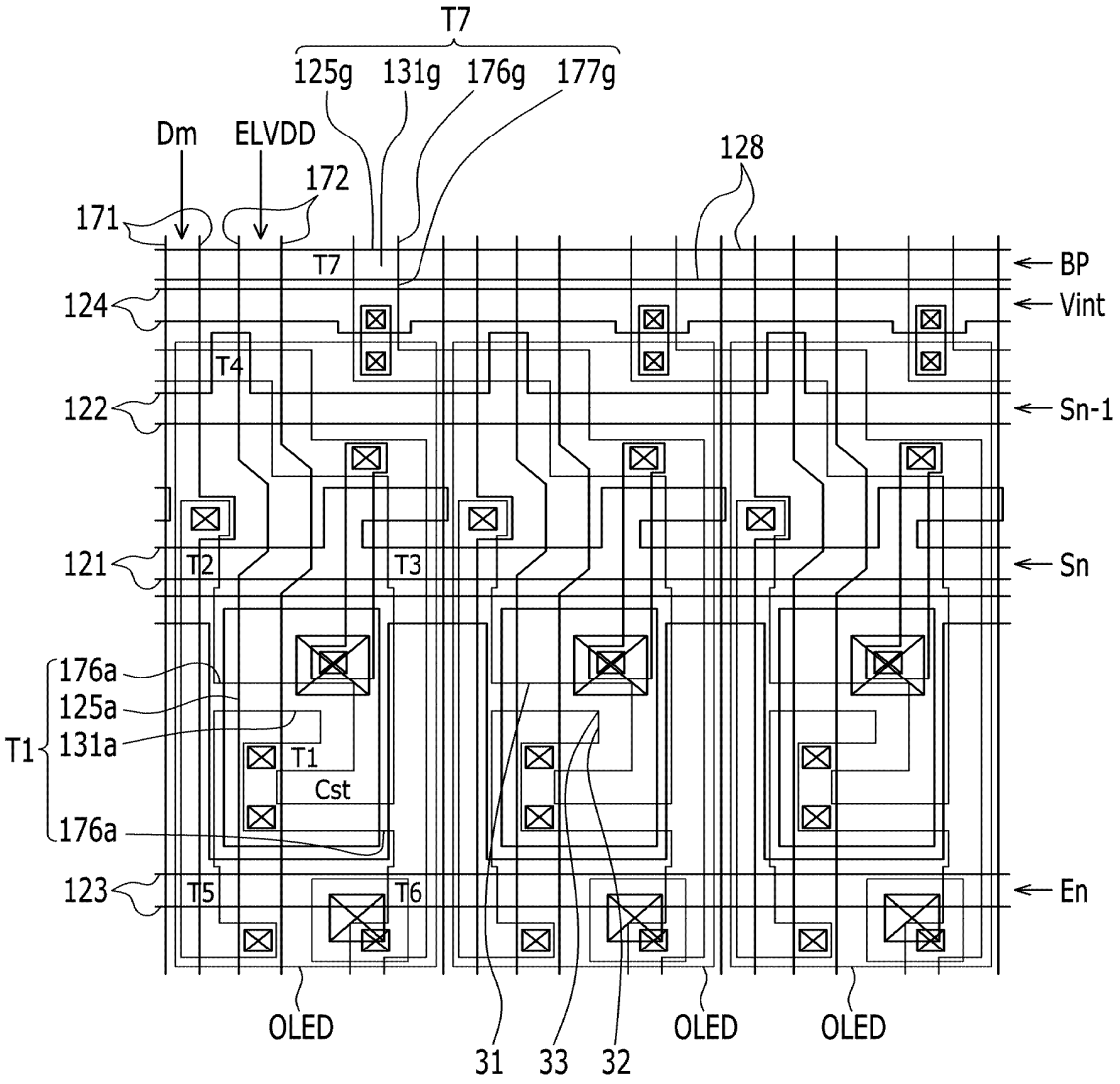
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【도 10】



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【도 11】



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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/871,618	07/22/2022	2871	2820	224721/411598-06509	30	1

CONFIRMATION NO. 1880

23363
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

FILING RECEIPT

OC000000135529270

Date Mailed: 08/03/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Se-Ho Kim, Yongin-si, KOREA, REPUBLIC OF;
Jin-Woo Park, Yongin-si, KOREA, REPUBLIC OF;
Won-Se Lee, Yongin-si, KOREA, REPUBLIC OF;

Applicant(s)

SAMSUNG DISPLAY CO., LTD., Yongin-si, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 23363

Domestic Priority data as claimed by applicant

This application is a CON of 17/234,670 04/19/2021
which is a CON of 16/984,045 08/03/2020 PAT 10985234
which is a CON of 16/659,372 10/21/2019 PAT 10734470
which is a CON of 16/261,450 01/29/2019 PAT 10483342
which is a CON of 15/900,715 02/20/2018 PAT 10204976
which is a CON of 15/603,309 05/23/2017 PAT 9899464
which is a CON of 15/238,449 08/16/2016 PAT 9660012
which is a CON of 13/952,508 07/26/2013 PAT 9450040

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
REPUBLIC OF KOREA 10-2012-0084976 08/02/2012 Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 08/01/2022

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/871,618**

Projected Publication Date: 11/10/2022

Non-Publication Request: No

Early Publication Request: No

Title

ORGANIC LIGHT EMITTING DIODE DISPLAY

Preliminary Class

349

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/871,618

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	30 minus 20 =	* 10			OR	x 100 =	1000
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2820

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

BOE v. Samsung IPR2025-01479
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Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Se-Ho Kim	Nonprovisional Application Number (if known):	
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Kyle W. Kellar/	Date 2022-07-21
Name (Print/Typed) Kyle W. Kellar	Practitioner Registration Number 71165

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☐ *Total of _____ forms are submitted.

BOE v. Samsung IPR2025-01479
Ex-1002

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

BOE v. Samsung IPR2025-01479
Ex-1002

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on July 22, 2022 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Marti Carrillo/
Marti Carrillo

Inventor(s) : Se-Ho Kim, et al. Confirmation No. To Be Determined

Application No. : To Be Determined
Filed : Herewith

Title : ORGANIC LIGHT EMITTING DIODE DISPLAY

Grp./Div. : To Be Determined
Examiner : To Be Determined

Docket No. : 224721

INFORMATION DISCLOSURE STATEMENT
FOR A CONTINUING NON-CPA APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
July 22, 2022

Commissioner:

In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, enclosed is an information disclosure statement. The references listed thereon are not enclosed because they were of record in the parent application, Application No. 17/234,670, filed April 19, 2021.

It is respectfully requested that these references be considered in the examination of this application, and identified in the list of references cited on the patent issuing on this application. Applicant also requests that an initialed copy of the information disclosure statement be entered in the application file and returned to applicant with the

next communication from the Office in accordance with MPEP § 609.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By */Kyle W. Kellar/*
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/mac
Information Disclosure Statement

BOE v. Samsung IPR2025-01479
Ex-1002

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224721
	Application Number	To Be Determined
	Filing Date	July 22, 2022
	Inventor(s)	Se-Ho Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - Kind Code[2] (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		5,929,464 A	07-27-1999	Yamazaki et al.
		6,104,067 A	08-15-2000	Zhang et al.
		6,914,642 B2	07-05-2005	Yamazaki et al.
		7,576,354 B2	08-18-2009	Son et al.
		7,649,202 B2	01-19-2010	Lee
		7,859,054 B2	12-28-2010	Yin et al.
		7,999,322 B2	08-16-2011	Yin et al.
		8,309,404 B2	11-13-2012	Yin et al.
		8,717,259 B2	05-06-2014	Park
		8,878,827 B2	11-04-2014	Han et al.
		9,287,528 B2	03-15-2016	Kim
		9,450,040 B2	09-20-2016	Kim et al.
		9,501,978 B2	11-22-2016	Park
		9,728,130 B2	08-08-2017	Takahara et al.
		9,892,683 B2	02-13-2018	Takahara et al.
		9,922,597 B2	03-20-2018	Takahara et al.
		9,959,809 B2	05-01-2018	Takahara et al.
		9,997,108 B2	06-12-2018	Takahara et al.
		10,134,336 B2	11-20-2018	Takahara et al.
		10,198,992 B2	02-05-2019	Takahara et al.
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		10,204,976 B2	02-12-2019	Kim et al.
		10,347,183 B2	07-09-2019	Takahara et al.
		10,453,395 B2	10-22-2019	Takahara et al.

EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

JEJ/smv

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224721
	Application Number	To Be Determined
	Filing Date	July 22, 2022
	Inventor(s)	Se-Ho Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - Kind Code[2] (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		10,483,342 B2	11-19-2019	Kim et al.
		10,553,158 B2	02-04-2020	Takahara et al.
		10,699,639 B2	06-30-2020	Takahara et al.
		10,734,470 B2	08-04-2020	Kim et al.
		10,818,235 B2	10-27-2020	Takahara et al.
		10,923,030 B2	02-16-2021	Takahara et al.
		11,302,253 B2	04-12-2022	Takahara et al.
		2002/0149711 A1	10-17-2002	Yamazaki et al.
		2003/0222589 A1	12-04-2003	Osame et al.
		2004/0155242 A1	08-12-2004	Segawa et al.
		2006/0082524 A1	04-20-2006	Kwon
		2007/0040193 A1	02-22-2007	Ajiki
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		2008/0017866 A1	01-24-2008	Sato
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		2010/0079361 A1	04-01-2010	Lee et al.
		2010/0253710 A1	10-07-2010	Rankov et al.
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		2011/0273419 A1	11-10-2011	Park
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		2012/0097965 A1	04-26-2012	Shin et al.
		2012/0162275 A1	06-28-2012	Park
		2012/0313100 A1	12-13-2012	Liu et al.
		2012/0146004 A1	06-14-2012	Lee et al.

EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

JEJ/smv

BOE v. Samsung IPR2025-01479
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224721
	Application Number	To Be Determined
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	Inventor(s)	Se-Ho Kim, et al.
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - Kind Code[2] (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		2013/0075766 A1	03-28-2013	Chang et al.
		2013/0201172 A1	08-08-2013	Jeong et al.
		2013/0334508 A1	12-19-2013	Moon
		2014/0001445 A1	01-02-2014	Kim
		2014/0027728 A1	01-30-2014	Yoon et al.
		2014/0077176 A1	03-20-2014	Lee et al.
		2014/0070184 A1	03-13-2014	Shin
		2014/0098078 A1	04-10-2014	Jeon et al.

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (✓)
		CN 1917205 A	02-21-2007	Yoshiharu	Abstract and Corresponds to U.S. Publication 2007/0040193 A1 listed above
		CN 101110422 A	01-23-2008	Sato	Abstract, and Corresponds to U.S. Publication 2008/0017866 A1, listed above
		CN 101673508 A	03-17-2010	Mitsuaki et al.	Abstract
		CN 102117598 A	07-06-2011	Lee et al.	Abstract
		CN 102194404 A	09-21-2011	Samsung Mobile Display Co., Ltd	Abstract
		CN 102386209 A	03-21-2012	AU OPTRONICS +	Espacenet Engliish Abstract

EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

JEJ/smv

BOE v. Samsung IPR2025-01479
Ex-1002

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224721
	Application Number	To Be Determined
	Filing Date	July 22, 2022
	Inventor(s)	Se-Ho Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (✓)
		CN 102456318 A	05-16-2012	LG DISPLAY CO., LTD	Abstract
		EP 2402932 A1	01-04-2012	Samsung Mobile Display Co. Ltd.	
		JP 2002-215096 A	07-31-2002	Kwon	Japan Patent Abstract
		JP 2003-295793 A	10-15-2003	Osame et al.	Japan Patent Abstract
		JP 2004-165241 A	06-10-2004	Segawa et al.	Japan Patent Abstract
		JP 2005-134838 A	05-26-2005	Sanyo Electric Co Ltd	Abstract
		JP 2005-316384 A	11-10-2005	Kwak	English Abstract
		JP 2006-11376 A	01-12-2006	Lee	Corresponds to US Pat. No. 7,649,202 B2 listed above
		JP 2006-65308 A	03-09-2006	Miyake et al.	Japan Patent Abstract
		JP 2006-65322 A	03-09-2006	Kwak et al.	Japan Patent Abstract
		JP 2007-140488 A	06-07-2007	Shishido	Japan Patent Abstract
		JP 2008-46619 A	02-28-2008	Sato	Japan Patent Abstract
		JP 2010-19950 A	01-28-2010	Seiko Epson Corp	Abstract
		JP 4452075 B2	02-05-2010	Takahara et al.	Corresponds to USP 9,728,130 B2 listed above
		JP 2011-507005 A	03-03-2011	Rankov et al.	Abstract and Corresponds to WO 2009/056877 A1 listed below
		JP 2012-14136 A	01-19-2012	Jeong et al.	Japan Patent Abstract
		JP 2012-133170 A	07-12-2012	Mochizuki	Japan Patent Abstract

EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

JEJ/smv

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224721
	Application Number	To Be Determined
	Filing Date	July 22, 2022
	Inventor(s)	Se-Ho Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (✓)
		KR 10-1999-0066077	08-16-1999	Kim	English Abstract
		KR 10-2009-0119599	11-19-2009	Koo et al.	Korean Patent Abstracts
		KR 10-0297868 B1	10-24-2001	Yamazaki et al.	Corresponds to US Pat. No. 6,914,642 B2 listed above
		KR 10-0439944 B1	11-03-2004	Kim et al.	Korean Patent Abstracts
		KR 10-1176540 B1	08-24-2005	Yin et al.	Corresponds to USP 7,859,054 listed above
		KR 10-2007-0074748 A	07-18-2007	Takashi et al.	Korean Patent Abstracts
		KR 10-1056233B1	08-11-2011	Bae et al.	Corresponds to US Publ No. 2013/0075766 A1 listed above
		KR 10-1839533 B1	03-19-2018	Park	Corresponds to USP 8,717,259 listed above
		WO 2007/111202 A1	10-04-2007	Ochi	
		WO 2009/056877 A1	05-07-2009	Rankov et al.	

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		SIPO Office Action dated December 14, 2016, for corresponding Chinese Patent Application No. 201310331836.5 (5 pages)
		JPO Office Action dated December 20, 2016, for corresponding Japanese Patent Application No. 2013-026588 (8 pages)

EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

JEJ/smv

BOE v. Samsung IPR2025-01479
Ex-1002

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224721
	Application Number	To Be Determined
	Filing Date	July 22, 2022
	Inventor(s)	Se-Ho Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		Korean Patent Abstract, Publication No. 10-2000-0038925 A, dated 05-07-2000 for corresponding Korean Patent 10-0439944 listed above (2 pages)
		European Search Report dated October 28, 2015, for corresponding European Patent Application No. 13179090.9 (9 pages)
		European Search Report dated November 12, 2015, for corresponding European Patent Application No. 13179091.7 (10 pages)
		EPO Office Action dated December 5, 2017, for corresponding European Patent Application No. 13179090.9 (4 pages)

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EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on July 22, 2022 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Marti Carrillo/
Marti Carrillo

Inventor : Se-Ho Kim, et al. Confirmation No. To be determined
Application No. : To be determined
Filed : July 22, 2022
Title : ORGANIC LIGHT EMITTING DIODE DISPLAY

Grp./Div. : To be determined
Examiner : To be determined

Docket No. : 224721

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS IN ACCORDANCE WITH 37 CFR. 1.5

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
July 22, 2022

Commissioner:

Attached herewith is a General Power of Attorney for the above-identified patent application.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By */Kyle W. Kellar/*
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/mac

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07/22/22 11:15AM

BOE v. Samsung IPR2025-01479
Ex-1002

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 23363

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SAMSUNG DISPLAY CO., LTD.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Dong-Ho Lee	Date (Optional)	
Name	Dong-Ho Lee		
Title	Group Leader, IP Prosecution Group		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

BOE v. Samsung IPR2025-01479
Ex-1002

UTILITY PATENT APPLICATION TRANSMITTAL
TRACK 1 PRIORITIZED EXAMINATION
(Only for new nonprovisional applications under 37 CFR 1.53(b))

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on July 22, 2022 at or before 11:59 p.m. Eastern Standard Time under the Rules of 37 CFR § 1.10.

/Marti Carrillo/
Marti Carrillo

Docket No. : 224271/411598-06509
Inventor(s) : Se-Ho Kim et al.
Title : ORGANIC LIGHT EMITTING DIODE DISPLAY

ADDRESS TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 22, 2022

1. __X__ **FEE TRANSMITTAL FORM**

2. **IF A CONTINUING APPLICATION**
__X__ This application is a continuation of patent application No. 17/234,670.

Prior application information: Examiner To be determined; Group Art Unit: OPAP.

_____ This application claims the benefit of Provisional Application No. _____ pursuant to 35 U.S.C. §119(e) and 37 CFR §1.78(a)(4).

3. **APPLICATION COMPRISED OF**

Specification
__47__ Specification, claims and Abstract (total pages)

Drawings
__11__ Sheets of formal drawing(s) (FIGS. 1 to 11)

Inventor's Declaration(s)
_____ Executed Declaration (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional)
__X__ Executed Declaration/Assignment (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional)

Power of Attorney by Applicant(s)
__X__ Executed (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional) with transmittal

Application Data Sheet
__X__ Newly executed ADS
_____ Unexecuted ADS

4. _____ **Microfiche Computer Program** *(Appendix)*

118255447.2

BOE v. Samsung IPR2025-01479
Ex-1002

UTILITY PATENT APPLICATION TRANSMITTAL
TRACK 1 PRIORITIZED EXAMINATION
(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.: 224721

5. _____ **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, all necessary)*
   _____ Computer Readable Copy
   _____ Paper Copy (identical to computer copy)
   _____ Statement verifying identity of above copies

6. **APPLICANT(S) STATUS UNDER 37 CFR § 1.27 or 1.29**
   _____ Applicant(s) and any others associated with it/them under § 1.27(a) are a SMALL ENTITY
   _____ Applicant(s) and any others associated with it/them under § 1.29(a) are a MICRO ENTITY
   _____ Certification of Micro Entity Status (Gross Income Basis)

7. **ALSO ENCLOSED ARE**
   __X__ Certification and Request for Prioritized Examination under 37 CFR 1.102(e)
   _____ Request and Certificate under 35 U.S.C. §122(b)(2)(B)(i) **(Request for Non-Publication)**
   _____ Preliminary Amendment
   _____ Includes "Cross-Reference to Related Applications"
   _____ A Petition for Extension of Time for the parent application and the required fee are being filed concurrently herewith.
   _____ This application is owned by _____ pursuant to an Assignment recorded at Reel _____, Frame _____
   __X__ Information Disclosure Statement (IDS)
   _____ Copies of IDS Citations
   _____ Certified copy of Priority Document(s) (*paper filing only, if foreign priority is claimed)*
   _____ English Translation Document *(if applicable)*
   _____ Return Receipt Postcard (MPEP 503) (should be specifically itemized).
   _____ Other: _____

8. **DIRECT ALL CORRESPONDENCE TO: CUSTOMER NUMBER 23363**

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By */Kyle W. Kellar/*
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

LEWIS ROCA ROTHGERBER CHRISTIE LLP, ***P.O. BOX 29001, GLENDALE, CA 91209-9001***

BOE v. Samsung IPR2025-01479
Ex-1002

FEE TRANSMITTAL
UTILITY PATENT APPLICATION
TRACK 1 PRIORITIZED EXAMINATION

DATE: July 22, 2022

Docket No. : 224721 Duplicate __
Inventor(s) : Se-Ho Kim et al.
Title : ORGANIC LIGHT EMITTING DIODE DISPLAY

FEE CALCULATION

CLAIMS AS FILED						
	Number Filed	Number Extra	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Total Claims	30 – 20	= 2	10 x $100.00	$50.00	$25.00	$1000.00
Independent Claims	1 – 3	= 0	0 x $480.00	$240.00	$120.00	$0.00
Multiple-Dependent Claims Fee			$860.00	$430.00	$215.00	$0.00

BASIC FILING, SEARCH, AND EXAMINATION FEES				
	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Basic Filing Fee	$320.00	$80.00	$80.00	$320.00
Search Fee	$700.00	$350.00	$175.00	$700.00
Examination Fee	$800.00	$400.00	$200.00	$800.00

APPLICATION SIZE FEE							
EFS Paper Size Equivalent	Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof (round up to whole number)	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
58 *.75	= 42 – 100	= 0/50	= 0	0 x $420.00	$210.00	$105.00	$0.00

TRACK 1 PRIORITIZED EXAMINATION				
	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Prioritized-Examination Fee	$4,200.00	$2,100.00	$1,050.00	$4,200.00
Processing Fee	$140.00	$70.00	$35.00	$140.00

OTHER				
	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Late Submission of Oath/Declaration Fee	$160.00	$80.00	$40.00	$0.00
Non-Electronic Filing Fee	$400.00	$200.00	$200.00	$0.00
			TOTAL AMOUNT OF FEES	$7,160.00
List Independent Claims: 1				

METHOD OF PAYMENT

__X__ Submitted herewith is the fee of $7,160.00.

__X__ The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required during the **entire pendency** of the application to Deposit Account No. 03-1728. Please show our docket number with any charge or credit to our Deposit Account.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By */Kyle W. Kellar/*
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/mac

118255447.2

BOE v. Samsung IPR2025-01479
Ex-1002

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Se-Ho Kim
Filer:	Kyle W. Kellar/Marti Carrillo
Attorney Docket Number:	224271/411598-06509

Filed as Large Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
REQUEST FOR PRIORITIZED EXAMINATION	1817	1	4200	4200
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	10	100	1000
Miscellaneous-Filing:				

BOE v. Samsung IPR2025-01479
Ex-1002

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**7160**

BOE v. Samsung IPR2025-01479
Ex-1002

Electronic Acknowledgement Receipt	
EFS ID:	46252681
Application Number:	17871618
International Application Number:	
Confirmation Number:	1880
Title of Invention:	ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Se-Ho Kim
Customer Number:	23363
Filer:	Kyle W. Kellar/Marti Carrillo
Filer Authorized By:	Kyle W. Kellar
Attorney Docket Number:	224271/411598-06509
Receipt Date:	22-JUL-2022
Filing Date:	
Time Stamp:	17:18:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$7160
RAM confirmation Number	E20227LH19180444
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	224721_ADS.pdf	2226678 96a220a64cde1193f59f399bd1ea9d007975b804	no	10
Warnings:					
Information:					
2		224271_Application.pdf	203525 fc5745e6232cc2807f23641ecc77aab4dd94cdd8	yes	47

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	38
Claims	39	46
Abstract	47	47

Warnings:					
Information:					
3	Drawings-only black and white line drawings	224721_Drawings.pdf	686459 02eadd5e099a04c8009b1cc703c567e6b961dcec	no	11
Warnings:					
Information:					
4	Oath or Declaration filed	224721_Declaration.pdf	98149 a96c75b101ad40d1bbe3cba15df13ed451920fe0	no	3
Warnings:					
Information:					
5	Track One Request	224721_REQ_Prioritized_Exam_Track_One.pdf	114360 55f7ddba20c2613ec0d0aa0b840d812cbcf7b38d	no	2

BOE v. Samsung IPR2025-01479
Ex-1002

Warnings:					
Information:					
6	Power of Attorney	224721_POA_Transmittal.pdf	137383 1e32ad1cfbec109b08e8d4fa9413839f22c8bc78	no	2
Warnings:					
Information:					
7	Transmittal Letter	224721_CON_IDS.pdf	106067 4d5519f88b9e90b0fbec17743d5f640912b4112a	no	2
Warnings:					
Information:					
8	Information Disclosure Statement (IDS) Form (SB08)	224721_PTOSB08.pdf	124209 a4954cbbd592d788055976beff5c1bfadd6176ec	no	6
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
9	Transmittal of New Application	224271_NewAppTransmittal.pdf	167743 87e322997b592da82cf86dbf7228dd169d6b5341	no	3
Warnings:					
Information:					
10	Fee Worksheet (SB06)	fee-info.pdf	50844 d364fe63780cee7375f5eef3ccb5eca690656b99	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3915417		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

BOE v. Samsung IPR2025-01479
Ex-1002

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	224721/411598-06509
	Application Number	
Title of Invention	ORGANIC LIGHT EMITTING DIODE DISPLAY	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Se-Ho		Kim	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

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State/Province	
Postal Code	17113
Country [i]	KR

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Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

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Country [i]	KR

Inventor 3 Remove

Legal Name

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Prefix	Given Name	Middle Name	Family Name	Suffix
	Won-Se		Lee	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Yongin-si	Country of Residence [i]	KR

Mailing Address of Inventor:

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City	Yongin-si, Gyeonggi-do	**State/Province**	
Postal Code	17113	**Country** [i]	KR

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	23363		
Email Address	pto@lewisroca.com	Add Email	Remove Email

Application Information:

Title of the Invention	ORGANIC LIGHT EMITTING DIODE DISPLAY		
Attorney Docket Number	224721/411598-06509	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	11	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

[i]

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
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Customer Number	23363		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17234670	2021-04-19

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17234670	Continuation of	16/984045	2020-08-03	10985234	2021-04-20

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/984045	Continuation of	16/659372	2019-10-21	10734470	2020-08-04

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/659372	Continuation of	16/261450	2019-01-29	10483342	2019-11-19

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Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/261450	Continuation of	15/900715	2018-02-20	10204976	2019-02-12
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/900715	Continuation of	15/603309	2017-05-23	9899464	2018-02-20
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/603309	Continuation of	15/238449	2016-08-16	9660012	2017-05-23
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/238449	Continuation of	13/952508	2013-07-26	9450040	2016-09-20

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Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
10-2012-0084976	KR	2012-08-02	HVG3KFkuo5

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Title of Invention	ORGANIC LIGHT EMITTING DIODE DISPLAY	

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

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A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

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The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

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Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	SAMSUNG DISPLAY CO., LTD.		
Mailing Address Information For Applicant:			
Address 1	1, Samsung-ro, Giheung-gu		
Address 2			
City	Yongin-si, Gyeonggi-do	**State/Province**	
Country	KR	Postal Code	17113
Phone Number		Fax Number	
Email Address			

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Assignee Information including Non-Applicant Assignee Information:

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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
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Signature:

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This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Kyle W. Kellar/			Date (YYYY-MM-DD)	2022-07-21
First Name	Kyle W.	Last Name	Kellar	Registration Number	71165

Additional Signature may be generated within this form by selecting the Add button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	224721/411598-06509
	Application Number	
Title of Invention	ORGANIC LIGHT EMITTING DIODE DISPLAY	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ORGANIC LIGHT EMITTING DIODE DISPLAY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 17/234,670, filed April 19, 2021; which is a continuation of U.S. Patent Application No. 16/984,045, filed August 3, 2020, now U.S. Patent No. 10,985,234, which is a continuation of U.S. Patent Application No. 16/659,372, filed October 21, 2019, now U.S. Patent No. 10,734,470, which is a continuation of U.S. Patent Application No. 16/261,450, filed January 29, 2019, now U.S. Patent No. 10,483,342, which is a continuation of U.S. Patent Application 15/900,715, filed February 20, 2018, now U.S. Patent No. 10,204,976, which is a continuation of U.S. Patent Application No. 15/603,309, filed May 23, 2017, now U.S. Patent No. 9,899,464, which is a continuation of U.S. Patent Application No. 15/238,449, filed August 16, 2016, now U.S. Patent No. 9,660,012, which is a continuation of U.S. Patent Application No. 13/952,508, filed July 26, 2013, now U.S. Patent No. 9,450,040, which claims priority to and the benefit of Korean Patent Application No. 10-2012-0084976 filed in the Korean Intellectual Property Office on August 2, 2012, the entire content of all of which are incorporated herein by reference.

BACKGROUND

1. Field

[0002] The described technology relates generally to an organic light emitting diode display.

2. Description of Related Art

[0003] An organic light emitting diode display includes two electrodes and an organic emission layer interposed therebetween, electrons injected from one electrode and holes injected from the other electrode are combined with each other in the organic

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emission layer to form an exciton, and light is emitted while the exciton discharges energy.

[0004] The organic light emitting diode display includes a plurality of pixels, each including an organic light emitting diode that is a self-light emitting element, and a plurality of thin film transistors and capacitors for driving the organic light emitting diode. The plurality of thin film transistors includes a switching thin film transistor and a driving thin film transistor.

[0005] In the switching thin film transistor, a thin gate insulating layer is formed between a gate electrode and a semiconductor layer to enable rapid switching operation. Because the thickness of the gate insulating layer of the driving thin film transistor, which is formed on the same layer as the switching thin film transistor, is reduced, a driving range of a gate voltage applied to the gate electrode of the driving thin film transistor becomes narrow. Therefore, it may be difficult to control the magnitude of the gate voltage Vgs of the driving thin film transistor to ensure a large number of gray levels.

[0006] The above information disclosed in this Background section is only for enhancement of understanding of the background of the described technology, and may therefore contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY

[0007] The described technology provides an organic light emitting diode display broadening a driving range of a driving thin film transistor to display a relatively large number of gray levels.

[0008] An exemplary embodiment of the present invention provides an organic light emitting diode display including a substrate, a scan line on the substrate for transferring a scan signal, a data line crossing the scan line and for transferring a data signal, a driving voltage line crossing the scan line and for transferring a driving voltage, a

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switching thin film transistor coupled to the scan line and the data line, a driving thin film transistor coupled to a switching drain electrode of the switching thin film transistor, and an organic light emitting diode (OLED) coupled to a driving drain electrode of the driving thin film transistor, wherein a driving semiconductor layer of the driving thin film transistor is bent and in a plane substantially parallel to the substrate.

[0009] The organic light emitting diode display may further include a first gate insulating layer covering the driving semiconductor layer, and a storage capacitor at the first gate insulating layer and overlapping the driving semiconductor layer.

[0010] The storage capacitor may include a first storage capacitor plate at the first gate insulating layer and overlapping the driving semiconductor layer, a second gate insulating layer covering the first storage capacitor plate, and a second storage capacitor plate at the second gate insulating layer and overlapping the first storage capacitor plate.

[0011] The driving semiconductor layer may include a plurality of bent portions.

[0012] The driving semiconductor layer may include a plurality of first extension portions extending in a first direction, and a plurality of second extension portions extending in a second direction that is different from the first direction, and wherein the bent portions couple respective ones of the first extension portions and the second extension portions.

[0013] The organic light emitting diode display may further include a compensation thin film transistor coupled to the driving thin film transistor and for compensating a threshold voltage of the driving thin film transistor.

[0014] The driving semiconductor layer may further include branched portions branched from the bent portions.

[0015] The storage capacitor may overlap the branched portions.

[0016] The organic light emitting diode display may further include a light emission control line for transferring a light emission control signal, and a light emission control thin film transistor configured to be turned on by the light emission control signal to

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transfer the driving voltage from the driving thin film transistor to the OLED, wherein the light emission control thin film transistor is between the driving drain electrode and the OLED.

[0017] The organic light emitting diode display may further include a transistor connection portion for coupling a compensation source electrode of the compensation thin film transistor to a light emission control source electrode of the light emission control thin film transistor, wherein the storage capacitor extends to overlap the transistor connection portion.

[0018] The driving semiconductor layer may extend to overlap the transistor connection portion.

[0019] The organic light emitting diode display may further include an interlayer insulating layer on the second gate insulating layer, wherein the transistor connection portion is at a same layer as the data line, and is coupled through a contact hole in the interlayer insulating layer to the compensation source electrode and the light emission control source electrode.

[0020] The driving semiconductor layer may include a first path semiconductor layer coupled to the compensation thin film transistor, and a second path semiconductor layer coupled to the light emission control thin film transistor, and a length of the first path semiconductor layer may be smaller than a length of the second path semiconductor layer.

[0021] The storage capacitor may overlap the first path semiconductor layer and the second path semiconductor layer.

[0022] The organic light emitting diode display may further include an interlayer insulating layer covering the second storage capacitor plate, a connection member at the interlayer insulating layer and coupled to the first storage capacitor plate through a first contact hole in the second gate insulating layer and the interlayer insulating layer, and a protective layer covering the interlayer insulating layer and the connection member,

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wherein the connection member is coupled to a compensation drain electrode of the compensation thin film transistor.

[0023] The scan line is at a same layer as the first storage capacitor plate, and the data line and the driving voltage line may be at a same layer as the connection member.

[0024] The driving voltage line may be coupled through a second contact hole in the interlayer insulating layer to the second storage capacitor plate.

[0025] The organic light emitting diode display may further include an operation control thin film transistor configured to be turned on by the light emission control signal transferred by the light emission control line to transfer the driving voltage to the driving thin film transistor, wherein the operation control thin film transistor is between the driving voltage line and a driving source electrode of the driving thin film transistor.

[0026] The organic light emitting diode display may further include a prior scan line for transferring a prior scan signal, an initialization voltage line for transferring an initialization voltage to the driving thin film transistor, and an initialization thin film transistor configured to be turned on according to the prior scan signal to transfer the initialization voltage to a driving gate electrode of the driving thin film transistor, wherein the initialization thin film transistor is between the driving gate electrode and the initialization voltage line .

[0027] The organic light emitting diode display may further include a bypass control line for transferring a bypass control signal, and a bypass thin film transistor for transferring a portion of a driving current transferred by the driving thin film transistor according to the bypass control signal, wherein the bypass thin film transistor is between the initialization voltage line and a light emission control drain electrode of the light emission control thin film transistor.

[0028] Another exemplary embodiment of the present invention provides an organic light emitting diode display including a substrate, a scan line on the substrate for transferring a scan signal, an initialization voltage line on the substrate for transferring an

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initialization voltage, a data line crossing the scan line for transferring a data signal, a driving voltage line crossing the scan line for transferring a driving voltage, a switching thin film transistor coupled to the scan line and the data line, a driving thin film transistor coupled to a switching drain electrode of the switching thin film transistor, an organic light emitting diode (OLED) coupled to a driving drain electrode of the driving thin film transistor, a light emission control thin film transistor between the driving drain electrode and the OLED, and a bypass thin film transistor between the initialization voltage line and a light emission control drain electrode of the light emission control thin film transistor, wherein the bypass thin film transistor transfers a portion of a driving current transferred by the driving thin film transistor according to a bypass control signal transferred by a bypass control line.

[0029] A driving semiconductor layer of the driving thin film transistor is bent and in a plane substantially parallel to the substrate.

[0030] The organic light emitting diode display may further include a first gate insulating layer covering the driving semiconductor layer, and a storage capacitor at the first gate insulating layer and overlapping the driving semiconductor layer.

[0031] The storage capacitor may include a first storage capacitor plate at the first gate insulating layer and overlapping the driving semiconductor layer, a second gate insulating layer covering the first storage capacitor plate, and a second storage capacitor plate at the second gate insulating layer and overlapping the first storage capacitor plate.

[0032] The driving semiconductor layer may include a plurality of bent portions.

[0033] The driving semiconductor layer may include a plurality of first extension portions extending in a first direction, and a plurality of second extension portions extending in a second direction that is different from the first direction. The bent portions may couple respective ones of the first extension portions and the second extension portions.

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[0034] The organic light emitting diode display may further include a compensation thin film transistor coupled to the driving thin film transistor and for compensating the threshold voltage of the driving thin film transistor.

[0035] The organic light emitting diode display may further include an interlayer insulating layer covering the second stroage capacitor plate, a connection member at the interlayer insulating layer and coupled to the first storage capacitor plate through a first contact hole in the second gate insulating layer and the interlayer insulating layer, and a protective layer covering the interlayer insulating layer and the connection member, The connection member may be coupled to a compensation drain electrode of the compensation thin film transistor.

[0036] The scanline may be at a same layer as the first storage capacitor plate, and the data line and the driving voltage line may be at a same layer as the connection member.

[0037] The driving voltage line may be coupled to the second storage capacitor plate through a second contact hole in the interlayer insulating layer.

[0038] According to an exemplary embodiment of the present invention, since a driving channel region of a driving semiconductor layer may be longitudinally formed by forming the driving semiconductor layer including a plurality of bent portions, a driving range of a gate voltage applied to a driving gate electrode may be broadened.

[0039] Therefore, since the driving range of the gate voltage is relatively broad, a gray level of light emitted from an organic light emitting diode (OLED) can be more precisely controlled by adjusting the magnitude of the gate voltage, and as a result, it is possible to increase a resolution of the organic light emitting diode display and to improve display quality.

[0040] Further, it is possible to sufficiently ensure storage capacitance even at a high resolution by forming a storage capacitor overlapping the driving semiconductor layer to

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ensure a region of the storage capacitor, which is reduced by the driving semiconductor layer having the bent portion.

[0041] Further, it is possible to avoid or prevent low gray level stains by setting a length of a first path semiconductor layer coupled to a compensation thin film transistor to be smaller than a length of a second path semiconductor layer coupled to a light emission control thin film transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0042] FIG. 1 is an equivalent circuit of one pixel of an organic light emitting diode display according to a first exemplary embodiment of the present invention.

[0043] FIG. 2 is a view schematically showing positions of a plurality of thin film transistors and capacitors of the organic light emitting diode display according to the first exemplary embodiment.

[0044] FIG. 3 is a layout view of one pixel of the organic light emitting diode display according to the first exemplary embodiment.

[0045] FIG. 4 is a cross-sectional view of the organic light emitting diode display of the first exemplary embodiment shown in FIG. 3, which is taken along the line IV-IV.

[0046] FIG. 5 is a cross-sectional view of the organic light emitting diode display of the first exemplary embodiment shown in FIG. 3, which is taken along the line V-V.

[0047] FIG. 6 is an enlarged layout view of a driving thin film transistor of an organic light emitting diode display according to a second exemplary embodiment of the present invention.

[0048] FIG. 7 is a layout view of an organic light emitting diode display according to a third exemplary embodiment of the present invention.

[0049] FIG. 8 is an enlarged layout view of a driving thin film transistor of an organic light emitting diode display according to a fourth exemplary embodiment of the present invention.

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[0050] FIG. 9 is an enlarged layout view of a driving thin film transistor of an organic light emitting diode display according to a fifth exemplary embodiment of the present invention.

[0051] FIG. 10 is an equivalent circuit of one pixel of an organic light emitting diode display according to a sixth exemplary embodiment of the present invention.

[0052] FIG. 11 is a layout view of the organic light emitting diode display according to the sixth exemplary embodiment.

DETAILED DESCRIPTION

[0053] Hereinafter, embodiments of the present invention will be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various ways, all without departing from the spirit or scope of the present invention.

[0054] To describe embodiments of the present invention, portions that do not relate to the description are omitted, and same or like constituent elements are designated by same reference numerals throughout the specification.

[0055] In addition, the size and thickness of each component shown in the drawings may be arbitrarily shown for understanding and ease of description, but the present invention is not limited thereto. In the drawings, the thickness of layers, films, panels, regions, areas, etc., may be exaggerated for clarity, for understanding, and for ease of description. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element, or intervening elements may be present.

[0056] In addition, unless explicitly described to the contrary, the word "comprise" and variations thereof, such as "comprises" or "comprising", will be understood to imply the inclusion of stated elements, but not necessarily to the exclusion of other elements.

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Further, in the specification, the word "on" means positioning on or below the object portion, but does not necessarily mean positioning on the upper side of the object portion based on a direction of gravity.

[0057] An organic light emitting diode display according to a first exemplary embodiment will be described in detail with reference to FIGS. 1 to 5.

[0058] FIG. 1 is an equivalent circuit of one pixel of an organic light emitting diode display according to a first exemplary embodiment. As shown in FIG. 1, one pixel of the organic light emitting diode display according to the first exemplary embodiment includes a plurality of signal lines 121, 122, 123, 124, 171, and 172, a plurality of thin film transistors T1, T2, T3, T4, T5, and T6, a storage capacitor Cst, and an OLED coupled to the plurality of signal lines.

[0059] The plurality of thin film transistors includes a driving thin film transistor T1, a switching thin film transistor T2, a compensation thin film transistor T3, an initialization thin film transistor T4, an operation control thin film transistor T5, and a light emission control thin film transistor T6.

[0060] The plurality of signal lines includes a scan line 121 for transferring a scan signal Sn, a prior scan line 122 for transferring a prior scan signal Sn-1 to the initialization thin film transistor T4, a light emission control line 123 for transferring a light emission control signal En to the operation control thin film transistor T5 and the light emission control thin film transistor T6, a data line 171 crossing the scan line 121 and for transferring a data signal Dm, a driving voltage line 172 for transferring a driving voltage ELVDD and formed to be almost parallel to the data line 171, and an initialization voltage line 124 for transferring an initialization voltage Vint for initializing the driving thin film transistor T1.

[0061] A gate electrode G1 of the driving thin film transistor T1 is coupled to an end Cst1 of the storage capacitor Cst, a source electrode S1 of the driving thin film transistor T1 is coupled via the operation control thin film transistor T5 to the driving voltage line

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172, a drain electrode D1 of the driving thin film transistor T1 is electrically coupled via the light emission control thin film transistor T6 to an anode of the OLED. The driving thin film transistor T1 receives the data signal Dm according to switching operation of the switching thin film transistor T2 to supply a driving current Id to the OLED.

[0062] A gate electrode G2 of the switching thin film transistor T2 is coupled to the scan line 121, a source electrode S2 of the switching thin film transistor T2 is coupled to the data line 171, a drain electrode D2 of the switching thin film transistor T2 is coupled via the operation control thin film transistor T5 to the driving voltage line 172 while being coupled to the source electrode S1 of the driving thin film transistor T1. The switching thin film transistor T2 is turned on according to the scan signal Sn transferred through the scan line 121 to perform a switching operation for transferring the data signal Dm transferred to the data line 171 to the source electrode of the driving thin film transistor T1.

[0063] A gate electrode G3 of the compensation thin film transistor T3 is coupled to the scan line 121, a source electrode S3 of the compensation thin film transistor T3 is coupled via the light emission control thin film transistor T6 to the anode of the OLED while being coupled to the drain electrode D1 of the driving thin film transistor T1, and a drain electrode D3 of the compensation thin film transistor T3 is coupled to an end Cst1 of the storage capacitor Cst, a drain electrode D4 of the initialization thin film transistor T4, and the gate electrode G1 of the driving thin film transistor T1 together. The compensation thin film transistor T3 is turned on according to the scan signal Sn transferred through the scan line 121 to couple the gate electrode G1 and the drain electrode D1 of the driving thin film transistor T1 to each other, thus performing diode-connection of the driving thin film transistor T1.

[0064] A gate electrode G4 of the initialization thin film transistor T4 is coupled to the prior scan line 122, a source electrode S4 of the initialization thin film transistor T4 is coupled to the initialization voltage line 124, and a drain electrode D4 of the initialization

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thin film transistor T4 is coupled to the end Cst1 of the storage capacitor Cst, the drain electrode D3 of the compensation thin film transistor T3, and the gate electrode G1 of the driving thin film transistor T1. The initialization thin film transistor T4 is turned on according to the prior scan signal Sn-1 transferred through the prior scan line 122 to transfer the initialization voltage Vint to the gate electrode G1 of the driving thin film transistor T1, thus performing an initialization operation for initializing the voltage of the gate electrode G1 of the driving thin film transistor T1.

[0065] A gate electrode G5 of the operation control thin film transistor T5 is coupled to the light emission control line 123, a source electrode S5 of the operation control thin film transistor T5 is coupled to the driving voltage line 172, and a drain electrode D5 of the operation control thin film transistor T5 is coupled to the source electrode S1 of the driving thin film transistor T1 and the drain electrode S2 of the switching thin film transistor T2.

[0066] A gate electrode G6 of the light emission control thin film transistor T6 is coupled to the light emission control line 123, a source electrode S6 of the light emission control thin film transistor T6 is coupled to the drain electrode D1 of the driving thin film transistor T1 and to the source electrode S3 of the compensation thin film transistor T3, and a drain electrode D6 of the light emission control thin film transistor T6 is electrically coupled to the anode of the OLED. The operation control thin film transistor T5 and the light emission control thin film transistor T6 are concurrently (e.g., simultaneously) turned on according to the light emission control signal En transferred through the light emission control line 123 to transfer the driving voltage ELVDD to the OLED, thus allowing a driving current Id to flow in the OLED.

[0067] Another end Cst2 of the storage capacitor Cst is coupled to the driving voltage line 172, and a cathode of the OLED is coupled to a common voltage ELVSS. Accordingly, the OLED receives the driving current Id from the driving thin film transistor T1 to emit light, thereby displaying an image.

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[0068] Hereinafter, operation of one pixel of the organic light emitting diode display according to the first exemplary embodiment will be described in detail.

[0069] First, a prior scan signal Sn-1 of a low level is supplied through the prior scan line 122 during an initialization period. Then, the initialization thin film transistor T4 is turned on corresponding to the prior scan signal Sn-1 of a low level, and the initialization voltage Vint is provided from the initialization voltage line 124 through the initialization thin film transistor T4 to the gate electrode G1 of the driving thin film transistor T1 to initialize the driving thin film transistor T1 with the initialization voltage Vint.

[0070] Subsequently, a low level scan signal Sn is supplied through the scan line 121 during a data programming period. Then, the switching thin film transistor T2 and the compensation thin film transistor T3 are turned on corresponding to a low level scan signal Sn, thereby causing the driving thin film transistor T1 to be diode-coupled by the turned on compensation thin film transistor T3, and biased in a forward direction.

[0071] Then, a compensation voltage Dm+Vth (Vth is a negative value), which is obtained by subtracting the threshold voltage Vth of the driving thin film transistor T1 from the data signal Dm supplied from the data line 171, is applied to the gate electrode G1 of the driving thin film transistor T1.

[0072] The driving voltage ELVDD and the compensation voltage Dm+Vth are applied to both ends Cst1 and Cst2 of the storage capacitor Cst, and a charge corresponding to a difference between voltages at both ends Cst1 and Cst2 is stored in the storage capacitor Cst. Subsequently, the level of the light emission control signal En supplied from the light emission control line 123 during the light emission period is changed from a high level to a low level. Then, the operation control thin film transistor T5 and the light emission control thin film transistor T6 are turned on by a low level light emission control signal En during the light emission period.

[0073] Then, the driving current Id is generated according to a difference between the voltage of the gate electrode G1 of the driving thin film transistor T1 and the driving

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voltage ELVDD, and the driving current Id is supplied through the light emission control thin film transistor T6 to the OLED. The gate-source voltage Vgs of the driving thin film transistor T1 is maintained at '(Dm+Vth)-ELVDD' by the storage capacitor Cst during the light emission period, and the driving current Id is proportional to a square of a difference between the threshold voltage and the source-gate voltage, that is, the driving current Id is proportional to '$(Dm-ELVDD)^2$', according to a current-voltage relationship of the driving thin film transistor T1. Accordingly, the driving current Id is determined regardless of the threshold voltage Vth of the driving thin film transistor T1.

[0074] A detailed structure of the pixel of the organic light emitting diode display shown in FIG. 1 will be described in detail with reference to FIGS. 2 to 5 together with FIG. 1. FIG. 2 is a view schematically showing positions of the plurality of thin film transistors T1-T6 and the capacitor Cst elements of the organic light emitting diode display according to the first exemplary embodiment, FIG. 3 is a specific layout view of one pixel of the organic light emitting diode display according to the first exemplary embodiment, FIG. 4 is a cross-sectional view of the organic light emitting diode display of the first exemplary embodiment shown in FIG. 3, which is taken along the line IV-IV, and FIG. 5 is a cross-sectional view of the organic light emitting diode display of the first exemplary embodiment shown in FIG. 3, which is taken along the line V-V.

[0075] As shown in FIGS. 2 to 5, the pixel of the organic light emitting diode display according to the first exemplary embodiment includes the scan line 121, the prior scan line 122, the light emission control line 123, and the initialization voltage line 124 formed in a row direction, and for respectively applying the scan signal Sn, the prior scan signal Sn-1, the light emission control signal En, and the initialization voltage Vint, and also includes the data line 171 and the driving voltage line 172 crossing the scan line 121, the prior scan line 122, the light emission control line 123, and the initialization voltage line 124, and for respectively applying the data signal Dm and the driving voltage ELVDD to the pixel.

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[0076] Further, in the pixel, the driving thin film transistor T1, the switching thin film transistor T2, the compensation thin film transistor T3, the initialization thin film transistor T4, the operation control thin film transistor T5, the light emission control thin film transistor T6, the storage capacitor Cst, and the OLED 70 are formed.

[0077] The driving thin film transistor T1, the switching thin film transistor T2, the compensation thin film transistor T3, the initialization thin film transistor T4, the operation control thin film transistor T5, and the light emission control thin film transistor T6 are formed along the semiconductor layer 131, and the semiconductor layer 131 is bent to have various shapes. The semiconductor layer 131 may be formed of polysilicon, and includes a channel region, which is not doped with an impurity, and a source region and a drain region formed at respective sides of the channel region to be doped with the impurity. The type of impurity corresponds to the type of thin film transistor, and an N-type impurity or a P-type impurity may be used. The semiconductor layer 131 includes a driving semiconductor layer 131a formed in the driving thin film transistor T1, a switching semiconductor layer 131b formed in the switching thin film transistor T2, a compensation semiconductor layer 131c formed in the compensation thin film transistor T3, an initialization semiconductor layer 131d formed in the initialization thin film transistor T4, an operation control semiconductor layer 131e formed in the operation control thin film transistor T5, and a light emission control semiconductor layer 131f formed in the light emission control thin film transistor T6.

[0078] The driving thin film transistor T1 includes the driving semiconductor layer 131a, the driving gate electrode 125a, the driving source electrode 176a, and the driving drain electrode 177a. The driving semiconductor layer 131a is bent, and includes a plurality of first extension portions 31 extending in a first direction, a plurality of second extension portions 32 extending in a second direction that is different from the first direction, and a plurality of bent portions 33 coupling respective ones of the first extension portions 31 and the second extension portions 32. Accordingly, the driving

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semiconductor layer 131a may be in a zigzag form. The driving semiconductor layer 131a shown in FIGS. 2 and 3 includes three first extension portions 31, two second extension portions 32, and four bent portions 33. Accordingly, the driving semiconductor layer 131a may be longitudinally arranged in a 'ㄹ' form (e.g., 3 substantially parallel and horizontal lines, wherein the top and center lines are coupled by a vertical line at one side, and wherein the center and bottom lines are coupled by another vertiacl line at an opposite side, as shown in FIG. 6).

[0079] As described above, the driving semiconductor layer 131a may be longitudinally formed in a narrow space by forming the driving semiconductor layer 131a including a plurality of bent portions 33. Accordingly, since the driving channel region 131a1 of the driving semiconductor layer 131a may be longitudinally formed, the driving range of the gate voltage applied to the driving gate electrode 125a is broadened. Therefore, since the driving range of the gate voltage is relatively broad, a gray level of light emitted from an OLED can be more finely and precisely controlled by adjusting the magnitude of the gate voltage, and as a result, it is possible to increase a resolution of the organic light emitting diode display and improve display quality.

[0080] In the driving semiconductor layer 131a, the first extension portion 31, the second extension portion 32, and the bent portion 33 may be variously located to implement various exemplary embodiments such as 'S', 'M', and 'W' (e.g., S-shaped, M-shaped, or W-shaped).

[0081] FIG. 6 is an enlarged layout view of a driving thin film transistor of an organic light emitting diode display according to a second exemplary embodiment of the present invention.

[0082] As shown in FIG. 6, the driving semiconductor layer 131a may be in the shape of an S.

[0083] The driving source electrode 176a corresponds to the driving source region 176a doped with the impurity in the driving semiconductor layer 131a, and the driving

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drain electrode 177a corresponds to the driving drain region 177a doped with the impurity in the driving semiconductor layer 131a. The storage capacitor Cst is formed thereon to overlap the driving gate electrode 125a.

[0084] The storage capacitor Cst includes a first storage capacitor plate 125h and a second storage capacitor plate 127 with the second gate insulating layer 142 interposed therebetween. Herein, the driving gate electrode 125a also plays a role of the first storage capacitor plate 125h, the second gate insulating layer 142 becomes a dielectric material, and storage capacitance is determined by the charge accumulated in the storage capacitor Cst, and by the voltage between both capacitor plates 125a and 127.

[0085] The first storage capacitor plate 125h is separated from the adjacent pixel to form a rectangle, and is formed of the same material as the scan line 121, the prior scan line 122, the light emission control line 123, the switching gate electrode 125b, the compensation gate electrode 125c, the operation control gate electrode 125e, and the light emission control gate electrode 125f, which are on the same layer first storage capacitor plate 125h.

[0086] The second storage capacitor plate 127 is coupled to the adjacent pixel, and is formed of the same material as the initialization voltage line 124, and is formed on the same layer as the initialization voltage line124.

[0087] As described above, it is possible to ensure sufficient storage capacitance even at a high resolution by forming the storage capacitor Cst overlapping the driving semiconductor layer 131a to ensure a region of the storage capacitor Cst, which is reduced by the driving semiconductor layer 131a having the bent portion.

[0088] The switching thin film transistor T2 includes the switching semiconductor layer 131b, the switching gate electrode 125b, the switching source electrode 176b, and the switching drain electrode 177b. The switching source electrode 176b is a portion protruding from the data line 171, and the switching drain electrode 177b corresponds to

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a switching drain region 177b doped with an impurity in the switching semiconductor layer 131b.

[0089] The compensation thin film transistor T3 includes the compensation semiconductor layer 131c, the compensation gate electrode 125c, the compensation source electrode 176c, and the compensation drain electrode 177c. The compensation source electrode 176c corresponds to the compensation source region 176c doped with the impurity in the compensation semiconductor layer 131c, and the compensation drain electrode 177c corresponds to the compensation drain region 177c doped with the impurity in the compensation semiconductor layer 131c. The compensation gate electrode 125c prevents a leakage current by forming a separate dual gate electrode 25.

[0090] The initialization thin film transistor T4 includes the initialization semiconductor layer 131d, the initialization gate electrode 125d, the initialization source electrode 176d, and the initialization drain electrode 177d. The initialization drain electrode 177d corresponds to the initialization drain region 177d doped with the impurity in the initialization semiconductor layer 131d. The initialization source electrode 176d is coupled through an initialization connection line 78 to the initialization voltage line 124. An end of the initialization connection line 78 is coupled through a contact hole 161 formed in the second gate insulating layer 142 and an interlayer insulating layer 160 to the initialization voltage line 124, and another end of the initialization connection line 78 is coupled through the contact hole 162 formed in the gate insulating layer 141, the second gate insulating layer 142, and the interlayer insulating layer 160 to the initialization source electrode 176d.

[0091] The operation control thin film transistor T5 includes the operation control semiconductor layer 131e, the operation control gate electrode 125e, the operation control source electrode 176e, and the operation control drain electrode 177e. The operation control source electrode 176e is a portion of the driving voltage line 172, and

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the operation control drain electrode 177e corresponds to the operation control drain region 177e doped with the impurity in the operation control semiconductor layer 131e.

[0092] The light emission control thin film transistor T6 includes the light emission control semiconductor layer 131f, the light emission control gate electrode 125f, the light emission control source electrode 176f, and the light emission control drain electrode 177f. The light emission control source electrode 176f corresponds to the light emission control source region 176f doped with the impurity in the light emission control semiconductor layer 131f.

[0093] An end of the driving semiconductor layer 131a of the driving thin film transistor T1 is coupled to the switching semiconductor layer 131b and the compensation semiconductor layer 131c, and another end of the driving semiconductor layer 131a is coupled to the operation control semiconductor layer 131e and the light emission control semiconductor layer 131f. Therefore, the driving source electrode 176a is coupled to the switching drain electrode 177b and to the operation control drain electrode 177e, and the driving drain electrode 177a is coupled to the compensation source electrode 176c and to the light emission control source electrode 176f.

[0094] The first storage capacitor plate 125h of the storage capacitor Cst is coupled through the connection member 174 to the compensation drain electrode 177c and to the initialization drain electrode 177d. The connection member 174 is formed on the same layer as the data line 171, an end of the connection member 174 is coupled through a contact hole 166 formed in the first gate insulating layer 141, in the second gate insulating layer 142, and in the interlayer insulating layer 160 to the compensation drain electrode 177c and to the initialization drain electrode 177d, and another end of the connection member 174 is coupled through a contact hole 167 formed in the second gate insulating layer 142 and in the interlayer insulating layer 160 to the first storage capacitor plate 125h. In this case, another end of the connection member 174 is coupled

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through a storage opening 27 formed in the second storage capacitor plate 127 to the first storage capacitor plate 125h.

[0095] The second storage capacitor plate 127 of the storage capacitor Cst is coupled through a contact hole 168 formed in the interlayer insulating layer 160 to a driving voltage line 172.

[0096] The switching thin film transistor T2 is used as a switching element for selecting the pixel that is to emit light. The switching gate electrode 125b is coupled to the scan line 121, the switching source electrode 176b is coupled to the data line 171, and the switching drain electrode 177b is coupled to the driving thin film transistor T1 and to the operation control thin film transistor T5. In addition, the light emission control drain electrode 177f of the light emission control thin film transistor T6 is directly coupled through a contact hole 181 formed in the protective layer 180 to a pixel electrode 191 of an organic light emitting diode 70.

[0097] Hereinafter, referring to FIGS. 4 and 5, a structure of the organic light emitting diode display according to the first exemplary embodiment will be described in detail according to the lamination order.

[0098] The structure of the thin film transistor will be described based on the driving thin film transistor T1, the switching thin film transistor T2, and the light emission control thin film transistor T6. In addition, the laminate structures of the film transistors T3, T4, and T5 are almost the same as the laminate structures of the driving thin film transistor T1, the switching thin film transistor T2, and the light emission control thin film transistor T6, and thus, the remaniing thin film transistors T3, T4, and T5 are not described in further detail.

[0099] A buffer layer 111 is formed on the substrate 110, and the substrate 110 may be formed of an insulating substrate made of glass, quartz, ceramics, plastics or the like.

[00100] The driving semiconductor layer 131a, the switching semiconductor layer 131b, and the light emission control semiconductor layer 131f are formed on the buffer

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layer 111. The driving semiconductor layer 131a includes a driving source region 176a and a driving drain region 177a facing each other with a driving channel region 131a1 interposed therebetween, the switching semiconductor layer 131b includes a switching source region 132b and a switching drain region 177b facing each other with a switching channel region 131b1 interposed therebetween, and the light emission control thin film transistor T6 includes a light emission control channel region 131f1, the light emission control source region 176f, and the light emission control drain region 133f.

[00101] Since the driving semiconductor layer 131a includes a plurality of bent portions 33 to be formed in a zigzag form, specifically, in a 'ㄹ' form, the driving semiconductor layer 131a may be longitudinally formed in a narrow space. Accordingly, since the driving channel region 131a1 of the driving semiconductor layer 131a may be longitudinally formed, the driving range of the gate voltage applied to the driving gate electrode 125a may be broadened.

[00102] The first gate insulating layer 141 formed of silicon nitride (SiNx) or silicon oxide (SiO2) is formed on the switching semiconductor layer 131a, the driving semiconductor layer 131b, and the light emission control semiconductor layer 131f.

[00103] The first gate wires including the scan line 121, which includes the driving gate electrode 125a, the switching gate electrode 125b, and the compensation gate electrode 125c, the prior scan line 122, which includes the initialization gate electrode 125d, and the light emission control line 123, which includes the operation control gate electrode 125e and the light emission control gate electrode 125f, are formed on the first gate insulating layer 141.

[00104] The driving gate electrode 125a is separated from the scan line 121, and the floating gate electrode 25 overlaps the driving channel region 131a1 of the driving semiconductor layer 131a. In addition, the switching gate electrode 125b is coupled to the scan line 121, and the switching gate electrode 125b overlaps the switching channel region 131b1 of the switching semiconductor layer 131b. In addition, the light emission

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control gate electrode 125f overlaps the light emission control channel region 131f1 of the light emission control semiconductor layer 131f.

[00105] Because, in the switching thin film transistor T2, only the first gate insulating layer 141 is formed between the switching gate electrode 125b and the switching semiconductor layer 131b, it is possible to perform a relatively rapid switching operation, and in the driving thin film transistor T1, only the first gate insulating layer 141 is formed between the driving gate electrode 125a and the driving semiconductor layer 131a, but since the length of the driving channel region 131a1 of the driving semiconductor layer 131a is relatively large, the driving range of the gate voltage applied to the driving gate electrode 125a is relatively broadened, such that it is possible to more finely, or precisely, control the gray level of light emitted from the OLED.

[00106] The first gate wires 125a, 125b, 125c, 125d, 125e, 125f, 121, 122, and 123 and the first gate insulating layer 141 cover the second gate insulating layer 142. The second gate insulating layer 142 may be formed of silicon nitride (SiNx) or silicon oxide (SiO2).

[00107] Second gate wires including the second storage capacitor plate 127 and the initialization voltage line 124 are formed on the second gate insulating layer 142. The second storage capacitor plate 127 overlaps the first storage capacitor plate 125h to form the storage capacitor Cst, and the first storage capacitor plate 125h overlaps the driving semiconductor layer 131a. As described above, it is possible to ensure the storage capacitance, even at a high resolution wherein the size of the pixel is reduced, by ensuring a region of the storage capacitor Cst reduced by the driving semiconductor layer 131a having the bent portion 33 by forming the storage capacitor Cst overlapping the driving semiconductor layer 131a.

[00108] The interlayer insulating layer 160 is formed on the second gate insulating layer 142, on the second storage capacitor plate 127, and on the initialization voltage line 124. The first gate insulating layer 141, the second gate insulating layer 142, and the

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interlayer insulating layer 160 together have a contact hole 163 through which the light emission control drain region 133f of the light emission control semiconductor layer 131f is exposed. Like the first gate insulating layer 141 and the second gate insulating layer 142, the interlayer insulating layer 160 may be made of a ceramic-based material such as silicon nitride (SiNx) or silicon oxide (SiO2).

[00109] Data wires including the data line 171, the switching source electrode 176b, the driving voltage line 172, the connection member 174, and the light emission control drain electrode 177f, are formed on the interlayer insulating layer 160.

[00110] In addition, the switching source electrode 176b and the light emission control drain electrode 177f are coupled through the contact holes 164 and 163 formed in the interlayer insulating layer 160, in the first gate insulating layer 141, and in the second gate insulating layer 142 to the switching source region 132b of the switching semiconductor layer 131b and to the light emission control drain region 133f of the light emission control semiconductor layer 131f, respectively.

[00111] The protective layer 180, which covers the data wires 171, 172, 174, and 177f, is formed on the interlayer insulating layer 160, and the pixel electrode 191 is formed on the protective layer 180. The pixel electrode 191 is coupled through the contact hole 181 formed in the protective layer 180 to the light emission control drain electrode 177f.

[00112] A barrier rib 350 is formed on an edge of the pixel electrode 191 and the protective layer 180, and the barrier rib 350 has a barrier rib opening 351 through which the pixel electrode 191 is exposed. The barrier rib 350 may be made of, for example, resins such as polyacrylates and polyimides or silica-based inorganic materials.

[00113] An organic emission layer 370 is formed on the pixel electrode 191 exposed through the barrier rib opening 351, and the common electrode 270 is formed on the organic emission layer 370. As described above, the organic light emitting diode 70 including the pixel electrode 191, the organic emission layer 370, and the common electrode 270 is formed.

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[00114] Herein, the pixel electrode 191 is an anode that is a hole injection electrode, and the common electrode 270 is a cathode that is an electron injection electrode. However, the present invention is not limited thereto, and the pixel electrode 191 may be the cathode, and the common electrode 270 may be the anode, according to the driving method of the organic light emitting diode display. Holes and electrons are respectively injected from the pixel electrode 191 and the common electrode 270 into the organic emission layer 370, and when the exciton, which results from the combined injected holes and electrons, falls from an excited state to a bottom state, light is emitted.

[00115] The organic emission layer 370 may be formed of a low molecular weight organic material, or a high molecular weight organic material such as, for example, PEDOT (poly 3,4-ethylenedioxythiophene). Further, the organic emission layer 370 may be formed of a multilayer structure including one or more of an emission layer, a hole injection layer HIL, a hole transport layer HTL, an electron transport layer ETL, and an electron injection layer EIL. In the case where all the layers are included, the hole injection layer HIL is located on the pixel electrode 710, which is the anode, and the hole transport layer HTL, the emission layer, the electron transport layer ETL, and the electron injection layer EIL are sequentially laminated thereon. Since the common electrode 270 is formed of a reflective conductive material, a rear surface light emission-type organic light emitting diode display is realized. Material such as lithium (Li), calcium (Ca), lithium fluoride/calcium (LiF/Ca), lithium fluoride/aluminum (LiF/Al), aluminum (Al), silver (Ag), magnesium (Mg), or gold (Au) may be used as the reflective material.

[00116] In the first exemplary embodiment, the first storage capacitor plate 125h has a rectangular shape. However, a third exemplary embodiment of the present invention enables increased storage capacitance by extending a portion of the first storage capacitor plate 125h.

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[00117] Referring now to FIG. 7, an organic light emitting diode display according to the third exemplary embodiment of the present invention will be described in detail, wherein FIG. 7 is a layout view of an organic light emitting diode display according to a third exemplary embodiment.

[00118] The third exemplary embodiment of the present invention is substantially the same as the first exemplary embodiment shown in FIGS. 1 to 5, with the exception of the driving semiconductor layer and the storage capacitor, and thus a repeated description of the similar features will be omitted.

[00119] As shown in FIG. 7, the driving thin film transistor T1 of the organic light emitting diode display according to the third exemplary embodiment includes the driving semiconductor layer 131a, the driving gate electrode 125a, the driving source electrode 176a, and the driving drain electrode 177a. The driving semiconductor layer 131a is bent, and includes a plurality of first extension portions 31 extending in a first direction, a plurality of second extension portions 32 extending in a second direction that is different from the first direction, and a plurality of bent portions 33 coupling respective ones of the first extension portions 31 and the second extension portions 32.

[00120] The driving semiconductor layer 131a may extend from a lateral surface of the data line 171 to be adjacent to the data line 171. Accordingly, since the length of the driving semiconductor layer 131a is increased, the driving range of the gate voltage applied to the driving gate electrode 125a may be broadened.

[00121] In the third exemplary embodiment, the compensation source electrode 176c of the compensation thin film transistor T3, and the light emission control source electrode 176f of the light emission control thin film transistor T6, are formed on the same layer, but the compensation source electrode 176c and the light emission control source electrode 176f are separated from each other with a spacing portion d therebetween so as to not overlap the driving semiconductor layer 131a.

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[00122] The driving gate electrode 125a, that is, the first storage capacitor plate 125h may extend in a lateral direction to overlap the extended driving semiconductor layer 131a, and the first storage capacitor plate 125h may partially overlap the spacing portion d. In addition, the second storage capacitor plate 127 extends so as to overlap the first storage capacitor plate 125h, and the second storage capacitor plate 127 partially overlaps the spacing portion d.

[00123] The compensation source electrode 176c and the light emission control source electrode 176f, which are partially separated from each other, are coupled to each other through the transistor connection portion 71 formed on the same layer as the data line 171. An end of the transistor connection portion 71 is coupled through a contact hole 61 formed in the first gate insulating layer 141, in the second gate insulating layer 142, and in the interlayer insulating layer 160, to the compensation source electrode 176c. Another end of the transistor connection portion 71 is coupled through a contact hole 62 formed in the first gate insulating layer 141, in the second gate insulating layer 142, and in the interlayer insulating layer 160, to the light emission control source electrode 176f. Accordingly, the storage capacitor Cst extends to overlap the transistor connection portion 71, and the driving semiconductor layer 131a extends to overlap the transistor connection portion 71.

[00124] As described above, since the compensation source electrode 176c and the light emission control source electrode 176f may be coupled through the transistor connection portion 71 to allow the driving semiconductor layer 131a, the first storage capacitor plate 125h, and the second storage capacitor plate 127 to extend to the spacing portion d between the compensation source electrode 176c and the light emission control source electrode 176f, the storage capacitor Cst may be further extended.

[00125] In the first exemplary embodiment, the driving semiconductor layer 131a is not directly coupled to the compensation source electrode 176c at the bent portion 33.

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However, in a fourth exemplary embodiment of the present invention, a branched portion 34 is directly branched from the compensation source electrode 176c at the bent portion 33.

[00126] Now referring to FIG. 8, an organic light emitting diode display according to the fourth exemplary embodiment will be described in detail. FIG. 8 is an enlarged layout view of a driving thin film transistor of an organic light emitting diode display according to the fourth exemplary embodiment. The fourth exemplary embodiment is substantially the same as the first exemplary embodiment shown in FIGS. 1 to 5, with the exception of the driving semiconductor layer and the storage capacitor, and thus, repeated description of the substantially similar features will be omitted.

[00127] As shown in FIG. 8, the driving thin film transistor T1 of the organic light emitting diode display according to the fourth exemplary embodiment includes the driving semiconductor layer 131a, the driving gate electrode 125a, the driving source electrode 176a, and the driving drain electrode 177a. The driving semiconductor layer 131a is bent, and includes the first extension portion 31 extending in a first direction, the second extension portion 32 extending in a second direction that is different from the first direction, the bent portion 33 coupling the first extension portion 31 and the second extension portion 32, and the branched portion 34 directly branched to the compensation source electrode 176c at the bent portion 33. The entire driving semiconductor layer 131a has a '┤' form (e.g., a vertical line having a horizontal line extending from near a center of the vertical line). Accordingly, since the length of the driving semiconductor layer 131a is increased, the driving range of the gate voltage applied to the driving gate electrode 125a may be broadened.

[00128] The branched portion 34 corresponds to a first path semiconductor layer CH1 coupled to the compensation thin film transistor T3, and the second extension portion 32 corresponds to a second path semiconductor layer CH2 coupled to the light emission control thin film transistor T6. In addition, the driving gate electrode 125a, that is, the first

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storage capacitor plate 125h, overlaps the first path semiconductor layer CH1 and the second path semiconductor layer CH2 of the driving semiconductor layer 131a, and the second storage capacitor plate 127 overlaps the first storage capacitor plate 125h. Accordingly, since the area of the storage capacitor Cst is increased, sufficient storage capacitance can be attained even at a high resolution.

[00129] In the fourth exemplary embodiment, the lengths of the first path semiconductor layer CH1 and the second path semiconductor layer CH2 are substantially the same as each other. However, in a fifth exemplary embodiment of the present invention, the lengths of the first path semiconductor layer CH1 and the second path semiconductor layer CH2 are different from each other.

[00130] Referring now to FIG. 9, an organic light emitting diode display according to the fifth exemplary embodiment of the present embodiment will be described in detail. FIG. 9 is an enlarged layout view of a driving thin film transistor of an organic light emitting diode display according to the fifth exemplary embodiment, which is substantially the same as the fourth exemplary embodiment shown in FIG. 8, with the exception of the driving semiconductor layer and the storage capacitor, and thus a repeated description of the similarities will be omitted.

[00131] As shown in FIG. 9, the driving thin film transistor T1 of the organic light emitting diode display according to the fifth exemplary embodiment includes the driving semiconductor layer 131a, the driving gate electrode 125a, the driving source electrode 176a, and the driving drain electrode 177a. The driving semiconductor layer 131a is bent. The driving semiconductor layer 131a includes the first extension portion 31 extending in a first direction, the second extension portion 32 extending in a second direction that is different from the first direction, the bent portion 33 coupling the first extension portion 31 and the second extension portion 32, and the branched portion 34 directly branched from the compensation source electrode 176c at the bent portion 33. Accordingly, since the length of the driving semiconductor layer 131a is increased, the

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driving range of the gate voltage applied to the driving gate electrode 125a may be broadened.

[00132] The branched portion 34 corresponds to the first path semiconductor layer CH1 coupled to the compensation thin film transistor T3, and a zigzag portion 30, which includes the first extension portion 31, the second extension portion 32, and the bent portion 33, corresponds to the second path semiconductor layer CH2 coupled to the light emission control thin film transistor T6. In addition, the driving gate electrode 125a, that is, the first storage capacitor plate 125h, overlaps the first path semiconductor layer CH1 and the second path semiconductor layer CH2 of the driving semiconductor layer 131a, and the second storage capacitor plate 127 overlaps the first storage capacitor plate 125h. Accordingly, since the area of the storage capacitor Cst is increased, sufficient storage capacitance can be ensured even at a high resolution.

[00133] Further, the length of the first path semiconductor layer CH1 is smaller than the length of the second path semiconductor layer CH2. This structure is called a short pass diode structure, and since the length of the first path semiconductor layer CH1 is different from the length of the second path semiconductor layer CH2, currents having different magnitudes may concurrently (e.g., simultaneously) flow. Since the length of the first path semiconductor layer CH1 is relatively small, a relatively large current may flow therein, and since the length of the second path semiconductor layer CH2 is relatively large, relatively small currents may flow therein (e.g., at a same time as the relatively large current in the first path semiconductor layer CH1). As described above, a constant current may be provided to the organic light emitting diode while a threshold voltage is rapidly compensated by using a characteristic of concurrently (e.g., simultaneously) providing currents having different magnitudes by one driving thin film transistor to reduce a current variation between the driving thin film transistors having different characteristics, thus preventing stains caused by a difference between

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magnitudes of the currents, and the driving operation thereof will be described in detail below.

[00134] The driving thin film transistor T1 charges the voltage corresponding to the data signal Dm in the storage capacitor Cst according to the scan signal Sn, and provides the current corresponding to the voltage charged in the storage capacitor Cst to the OLED. Because the threshold voltage Vth of the driving thin film transistor T1 may be changed over time, the compensation thin film transistor T3 performs diode-connection of the driving thin film transistor T1 according to the scan signal Sn to compensate the threshold voltage Vth of the driving thin film transistor T1.

[00135] Accordingly, since the relatively large current flowing through the first path semiconductor layer CH1 while the data signal Dm is transferred can rapidly charge the storage capacitor Cst through the compensation thin film transistor T3 (e.g., to a predetermined voltage/compensation voltage), the compensation of the threshold voltage Vth may be relatively rapidly and easily performed.

[00136] Further, the relatively small current flowing through the second path semiconductor layer CH2 is provided through the light emission control thin film transistor T6 to the OLED, stains may be avoided or prevented. That is, since a change in current according to a change in voltage applied to the driving gate electrode 125a of the driving thin film transistor T1 is small, a current control voltage width (data swing range) can be increased, such that the range of the data voltage displaying a gamma can be increased, and it is possible to avoid or prevent stains caused by a difference between magnitudes of the currents by reducing a current variation between the driving thin film transistors having different characteristics (e.g., distribution characteristics).

[00137] Since a known driving thin film transistor can allow only a current of one magnitude to flow through the driving semiconductor layer 131a, currents having the same magnitude are provided to the compensation thin film transistor T3 and the light emission control thin film transistor T6. Accordingly, when the length of the driving

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semiconductor layer 131a of the driving thin film transistor T1 is relatively small, so that the threshold voltage Vth of the driving thin film transistor T1 is rapidly compensated, because an s-factor of a transistor characteristic curve (transfer curve) is reduced, thereby increasing a ratio (e.g., change ratio) of a change in current to a change in voltage applied to the driving gate electrode, thereby causing a relatively large current to be provided to the OLED, potentially causing stains.

[00138] Conversely, when the length of the driving semiconductor layer 131a of the driving thin film transistor T1 is set to be relatively large in an attempt to avoid or prevent stains, because the threshold voltage Vth of the driving thin film transistor is compensated by the small current relatively slowly, low gray level compensation is not performed, causing stains. This problem becomes more noticeable as the resolution is increased. That is, because an amount of time during which the data signal Dm is applied is reduced as the resolution is increased, the current flows to the OLED before the threshold voltage Vth is completely compensated, causing the current variation to generate stains.

[00139] Accordingly, it is possible to avoid or prevent low gray level stains by setting the length of the first path semiconductor layer CH1 coupled to the compensation thin film transistor T3 to be smaller than the length of the second path semiconductor layer CH2 coupled to the light emission control thin film transistor T6.

[00140] The first exemplary embodiment has a structure where the driving semiconductor layer of the driving thin film transistor is bent in a “6tr 1cap” structure, which is formed of six thin film transistors and one storage capacitor. However, a sixth exemplary embodiment of the present embodiment has a structure where the driving semiconductor layer of the driving thin film transistor is bent in a “7tr 1cap” structure formed of seven thin film transistors and one storage capacitor.

[00141] Referring now to FIGS. 10 and 11, an organic light emitting diode display according to the sixth exemplary embodiment will be described in detail. FIG. 10 is an

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equivalent circuit of one pixel of an organic light emitting diode display according to the sixth exemplary embodiment, and FIG. 11 is a layout view of the organic light emitting diode display according to the sixth exemplary embodiment, which is substantially the same as the first exemplary embodiment shown in FIGS. 1 to 5, except that a current control thin film transistor is added, and thus a repeated description of similarities will be omitted.

[00142] As shown in FIGS. 10 and 11, one pixel of the organic light emitting diode display according to the sixth exemplary embodiment includes a plurality of signal lines 121, 122, 123, 124, 128, 171, and 172, and a plurality of thin film transistors T1, T2, T3, T4, T5, T6, and T7, the storage capacitor Cst, and the OLED coupled to a plurality of signal lines.

[00143] The plurality of thin film transistors includes the driving thin film transistor T1, the switching thin film transistor T2, the compensation thin film transistor T3, the initialization thin film transistor T4, the operation control thin film transistor T5, the light emission control thin film transistor T6, and the current control thin film transistor T7.

[00144] The signal line includes the scan line 121 for transferring the scan signal Sn, the prior scan line 122 for transferring the prior scan signal Sn-1 to the initialization thin film transistor T4, the light emission control line 123 for transferring the light emission control signal En to the operation control thin film transistor T5 and to the light emission control thin film transistor T6, the data line 171 crossing the scan line 121 and for transferring the data signal Dm, the driving voltage line 172, which is substantially parallel to the data line 171, for transferring the driving voltage ELVDD, the initialization voltage line 124 for transferring the initialization voltage Vint for initializing the driving thin film transistor T1, and a bypass control line 128 for transferring a bypass signal BP to a bypass thin film transistor T7.

[00145] The gate electrode G1 of the driving thin film transistor T1 is coupled to an end (e.g., a first end) Cst1 of the storage capacitor Cst, the source electrode S1 of the driving

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thin film transistor T1 is coupled via the operation control thin film transistor T5 to the driving voltage line 172, the drain electrode D1 of the driving thin film transistor T1 is electrically coupled via the light emission control thin film transistor T6 to an anode of the OLED.

[00146] The gate electrode G2 of the switching thin film transistor T2 is coupled to the scan line 121, the source electrode S2 of the switching thin film transistor T2 is coupled to the data line 171, the drain electrode D2 of the switching thin film transistor T2 is coupled via the operation control thin film transistor T5 to the driving voltage line 172, while also being coupled to the source electrode S1 of the driving thin film transistor T1.

[00147] The gate electrode G4 of the initialization thin film transistor T4 is coupled to the prior scan line 122, the source electrode S4 of the initialization thin film transistor T4 is coupled to the initialization voltage line 124, and the drain electrode D4 of the initialization thin film transistor T4 is coupled to the first end Cst1 of the storage capacitor Cst, to the drain electrode D3 of the compensation thin film transistor T3, and to the gate electrode G1 of the driving thin film transistor T1.

[00148] A gate electrode G7 of the bypass thin film transistor T7 is coupled to the bypass control line 128, a source electrode S7 of the bypass thin film transistor T7 is coupled to the drain electrode D6 of the light emission control thin film transistor T6 and to the anode of the OLED, and a drain electrode D7 of the bypass thin film transistor T7 is coupled to the initialization voltage line 124 and to the source electrode S4 of the initialization thin film transistor T4.

[00149] Hereinafter, operation of the bypass thin film transistor T7 of the organic light emitting diode display according to the sixth exemplary embodiment will be described.

[00150] The bypass thin film transistor T7 receives the bypass signal BP from the bypass control line 128. The bypass signal BP is a voltage (e.g., a voltage of a predetermined level) at which the bypass thin film transistor T7 can be always turned off, and the bypass thin film transistor T7 recieves the voltage of a level sufficient to turn the

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transistor off to the gate electrode G7 to turn off the bypass transistor T7, and allow a portion of the driving current Id to flow as a bypass current Ibp through the bypass transistor T7.

[00151] When the minimum current of the driving thin film transistor T1 for displaying a black image flows as the driving current Id, if the OLED emits light, the black image is not ideally displayed. Accordingly, the bypass thin film transistor T7 of the organic light emitting diode display according to the sixth exemplary embodiment may disperse, or divert, a portion of the minimum current of the driving thin film transistor T1 as a bypass current Ibp to a current path other than the current path of the organic light emitting diode. Herein, the minimum current of the driving thin film transistor refers to a current when the gate-source voltage Vgs of the driving thin film transistor T1 is smaller than the threshold voltage Vth, thus turning off the driving thin film transistor. The minimum driving current (e.g., current of 10 pA or less) when the driving thin film transistor is turned off is transferred to the organic light emitting diode to be displayed as an image of black luminance.

[00152] When the minimum driving current displaying the black image flows, a bypass transferring effect of the bypass current Ibp is large, but when the large driving current for displaying an image (such as a general image or a white image) flows, an effect of the bypass current Ibp is hardly present. Accordingly, when the driving current displaying the black image flows, a light emitting current Ioled of the organic light emitting diode, which corresponds to the driving current Id reduced by the bypass current Ibp through the bypass thin film transistor T7, has the minimum required current at which the black image can be displayed.

[00153] Accordingly, a contrast ratio may be improved by implementing a precise black luminance image by using the bypass thin film transistor T7.

[00154] A structure of the pixel of the organic light emitting diode display shown in FIG. 10 will be described with reference to FIG. 11 together with FIGS. 10 and 3. FIG. 11 is a

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layout view of the organic light emitting diode display according to the sixth exemplary embodiment.

[00155] As shown in FIGS. 10 and 11, the pixel of the organic light emitting diode display according to the sixth exemplary embodiment includes the scan line 121, the prior scan line 122, the light emission control line 123, the initialization voltage line 124, and the bypass control line 128 formed in a row direction for respectively applying the scan signal Sn, the prior scan signal Sn-1, the light emission control signal En, the initialization voltage Vint, and the bypass signal BP, and also includes the data line 171 and the driving voltage line 172 crossing the scan line 121, the prior scan line 122, the light emission control line 123, the initialization voltage line 124, and the bypass control line 128, and for respectively applying the data signal Dm and the driving voltage ELVDD to the pixel.

[00156] Further, in the pixel, the driving thin film transistor T1, the switching thin film transistor T2, the compensation thin film transistor T3, the initialization thin film transistor T4, the operation control thin film transistor T5, the light emission control thin film transistor T6, the bypass thin film transistor T7, the storage capacitor Cst, and the OLED 70 are formed.

[00157] The driving thin film transistor T1, the switching thin film transistor T2, the compensation thin film transistor T3, the initialization thin film transistor T4, the operation control thin film transistor T5, the light emission control thin film transistor T6, and the bypass thin film transistor T7 are formed along the semiconductor layer 131, which is bent to have various shapes. The semiconductor layer 131 may be formed of, for example, polysilicon, and includes a channel region not doped with an impurity, and a source region and a drain region formed at respective sides of the channel region and doped with an impurity. Herein, the impurity corresponds to a kind of thin film transistor, such as, for example, an N-type impurity or a P-type impurity. The semiconductor layer 131 includes the driving semiconductor layer 131a formed in the driving thin film

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transistor T1, the switching semiconductor layer 131b formed in the switching thin film transistor T2, the compensation semiconductor layer 131c formed in the compensation thin film transistor T3, the initialization semiconductor layer 131d formed in the initialization thin film transistor T4, the operation control semiconductor layer 131e formed in the operation control thin film transistor T5, the light emission control semiconductor layer 131f formed in the light emission control thin film transistor T6, and a bypass semiconductor layer 131g formed in the bypass thin film transistor T7.

[00158] The driving thin film transistor T1 includes the driving semiconductor layer 131a, the driving gate electrode 125a, the driving source electrode 176a, and the driving drain electrode 177a. The driving semiconductor layer 131a is bent, and includes a plurality of first extension portions 31 extending in a first direction, a plurality of second extension portions 32 extending in a second direction that is different from the first direction, and a plurality of bent portions 33 coupling respective ones of the first extension portions 31 and the second extension portions 32. Accordingly, the driving semiconductor layer 131a may be in a zigzag form. The driving semiconductor layer 131a shown in FIGS. 2 and 3 includes three first extension portions 31, two second extension portions 32, and four bent portions 33. Accordingly, the driving semiconductor layer 131a may be longitudinally in a 'ㄹ' form, or in a z form.

[00159] As described above, the driving semiconductor layer 131a may be longitudinally formed in a narrow space by forming the driving semiconductor layer 131a including a plurality of bent portions 33. Accordingly, since the driving channel region 131a1 of the driving semiconductor layer 131a may be longitudinally formed, the driving range of the gate voltage applied to the driving gate electrode 125a is broadened. Therefore, since the driving range of the gate voltage is relatively broad, a gray level of light emitted from an OLED can be more finely, or precisely, controlled by changing or adjusting the magnitude of the gate voltage, and as a result, it is possible to increase a resolution of the organic light emitting diode display and to improve display quality.

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[00160] The bypass thin film transistor T7 includes the bypass semiconductor layer 131g, the bypass gate electrode 125g, the bypass source electrode 176g, and the bypass drain electrode 177g. The bypass source electrode 176g corresponds to the bypass drain region 177g doped with the impurity in the bypass semiconductor layer 131g, and the bypass drain electrode 177g corresponds to the bypass drain region 177g doped with the impurity in the bypass semiconductor layer 131g. The bypass source electrode 176g is directly coupled to the light emission control drain region 133f.

[00161] The bypass semiconductor layer 131g is formed on the same layer as the driving semiconductor layer 131a, the switching semiconductor layer 131b, the light emission control semiconductor layer 131f, and the like. The first gate insulating layer 141 is formed on the bypass semiconductor layer 131g. The bypass gate electrode 125g, which is a portion of the bypass control line 128, is formed on the first gate insulating layer 141, and the second gate insulating layer 142 is formed on the bypass gate electrode 125g and the first gate insulating layer 141.

[00162] Accordingly, the bypass thin film transistor T7 receives the bypass signal BP from the bypass control line 128 to always turn off the bypass transistor T7, and a portion of the driving current Id is emitted under an off state as the bypass current Ibp through the bypass transistor T7 to the outside. Accordingly, when the driving current displaying the black image flows, a contrast ratio may be improved by implementing a more precise black luminance image.

[00163] While this disclosure has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, and their equivalents.

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Description of Some of the Reference Characters

31: First extension portion	32: Second extension portion
33: Bent portion	110: Substrate
121: Scan line	122: Prior scan line
123: Light emission control line	124: Initialization voltage line
125a: Driving gate electrode	125b: Switching gate electrode
131a: Driving semiconductor layer	132b: Switching semiconductor layer
141: First gate insulating layer	142: Second gate insulating layer
171: Data line	172: Driving voltage line

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WHAT IS CLAIMED IS:

1. An organic light emitting diode display comprising:

a non-conductive substrate;

a plurality of first voltage lines;

a plurality of scan lines;

a plurality of data lines;

a plurality of driving circuits formed on the substrate;

a plurality of organic light emitting diodes, wherein each of the plurality of organic light emitting diodes is electrically coupled to a respective one of the plurality of driving circuits;

wherein each of the driving circuits comprises:

a first thin film transistor implemented in a first portion of a semiconductor layer disposed on the substrate, and coupled to one of the plurality of scan lines and to one of the plurality of data lines;

a second thin film transistor implemented in a second portion of the semiconductor layer, wherein the semiconductor layer couples the second thin film transistor to the first thin film transistor, and wherein the second portion of the semiconductor layer has at least one bent portion;

a storage capacitor comprising:

a first capacitor plate that is configured to operate as the gate electrode of the second thin film transistor;

a second capacitor plate electrically coupled to one of the plurality of first voltage lines and overlapping the first capacitor plate; and

an insulating layer between the first capacitor plate and the second capacitor plate;

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a third thin film transistor implemented in a third portion of the semiconductor layer, wherein the semiconductor layer couples the third thin film transistor to the first thin film transistor and to the second thin film transistor, and wherein the third thin film transistor is electrically coupled to one of the plurality of first voltage lines through the semiconductor layer; and

a fourth thin film transistor implemented in a fourth portion of the semiconductor layer, wherein the semiconductor layer couples the fourth thin film transistor to the second thin film transistor, and wherein the fourth thin film transistor is electrically coupled to the respective organic light emitting diode through the semiconductor layer; and

wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate.

2. An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

3. An organic light emitting diode display according to claim 2, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor electrically coupled to the first capacitor plate; and

a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,

wherein the sixth thin film transistor is coupled to the fifth thin film transistor.

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4. An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

5. An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

6. An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

7. An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode,

wherein the seventh thin film transistor is coupled to the fourth thin film transistor.

8. An organic light emitting diode display according to claim 4, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

9. An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.

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10. An organic light emitting diode display according to claim 2, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

a sixth thin film transistor implemented in a sixth portion of the semiconductor layer,

wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and

wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

11. An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

12. An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

13. An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

14. An organic light emitting diode display according to claim 11, further comprising a seventh thin film transistor implemented in a sixth portion of the semiconductor layer,

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wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

15. An organic light emitting diode display according to claim 11, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

16. An organic light emitting diode display according to claim 1, wherein a periphery of the first capacitor plate completely surrounds a periphery of the second capacitor plate in a plan view.

17. An organic light emitting diode display according to claim 1, further comprising:

a plurality of second voltage lines;

a fifth thin film transistor electrically coupled to the first capacitor plate; and

a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,

wherein the sixth thin film transistor is coupled to the fifth thin film transistor.

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18. An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

19. An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

20. An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

21. An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode,

wherein the seventh thin film transistor is coupled to the fourth thin film transistor.

22. An organic light emitting diode display according to claim 18, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

23. An organic light emitting diode display according to claim 1, further comprising:

a plurality of second voltage lines;

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a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

a sixth thin film transistor implemented in a sixth portion of the semiconductor layer, wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

24. An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

25. An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.

26. An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.

27. An organic light emitting diode display according to claim 24, further comprising a seventh thin film transistor implemented in a sixth portion of the semiconductor layer,

wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

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wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

28. An organic light emitting diode display according to claim 24, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and

wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

29. An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.

30. An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

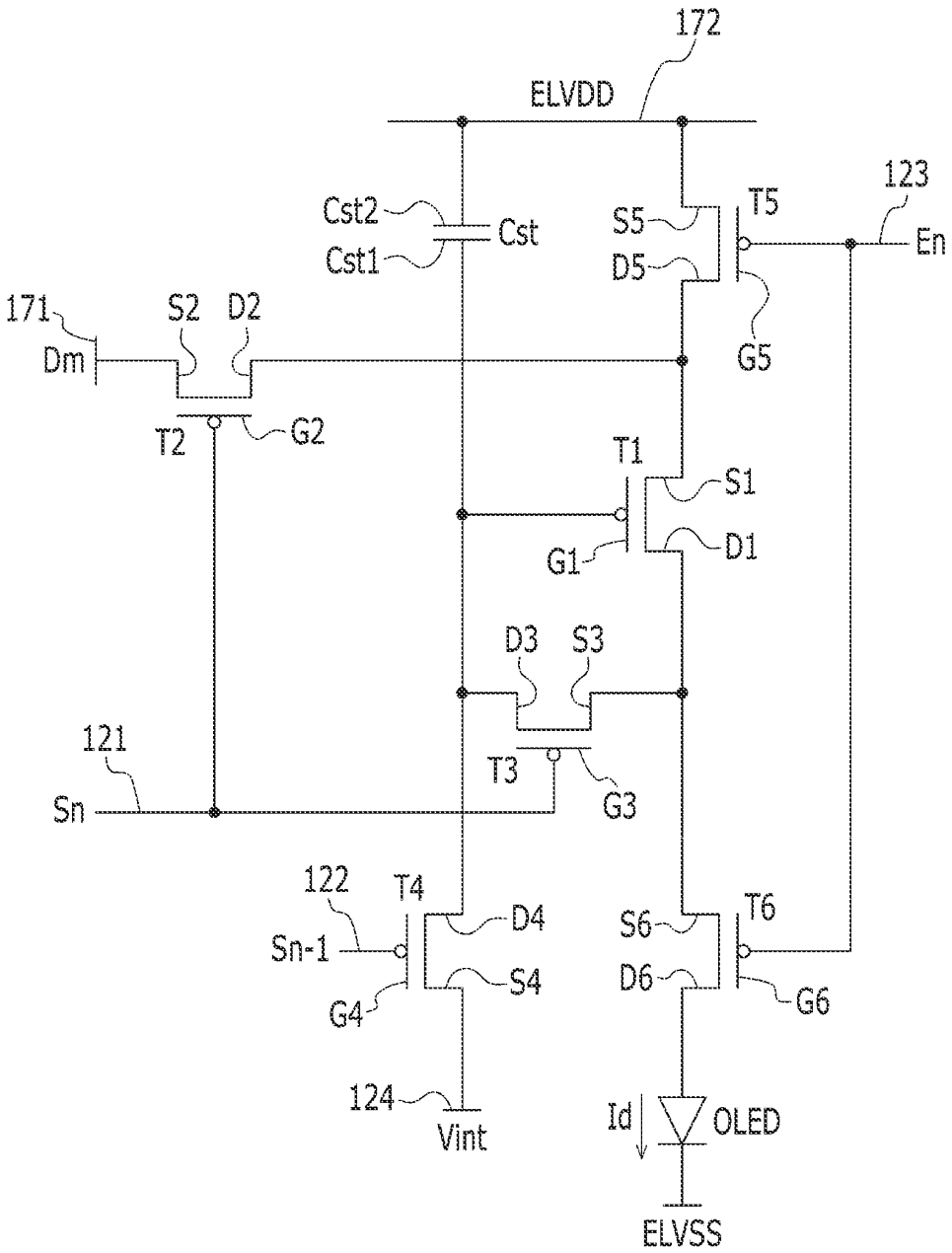
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ABSTRACT OF THE DISCLOSURE

An organic light emitting diode display includes a substrate, a scan line on the substrate for transferring a scan signal, a data line crossing the scan line and for transferring a data signal, a driving voltage line crossing the scan line and for transferring a driving voltage, a switching thin film transistor coupled to the scan line and the data line, a driving thin film transistor coupled to a switching drain electrode of the switching thin film transistor, and an organic light emitting diode (OLED) coupled to a driving drain electrode of the driving thin film transistor, wherein a driving semiconductor layer of the driving thin film transistor is bent and in a plane substantially parallel to the substrate.

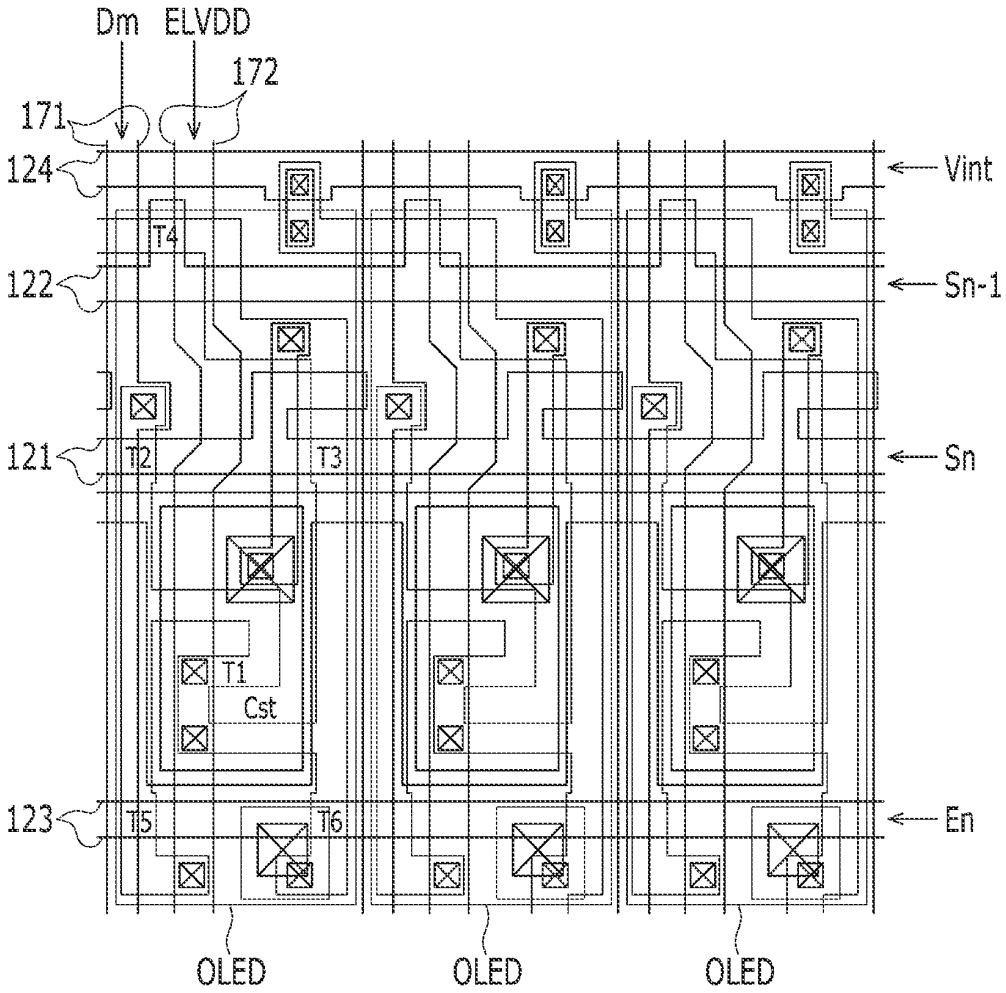
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FIG. 1



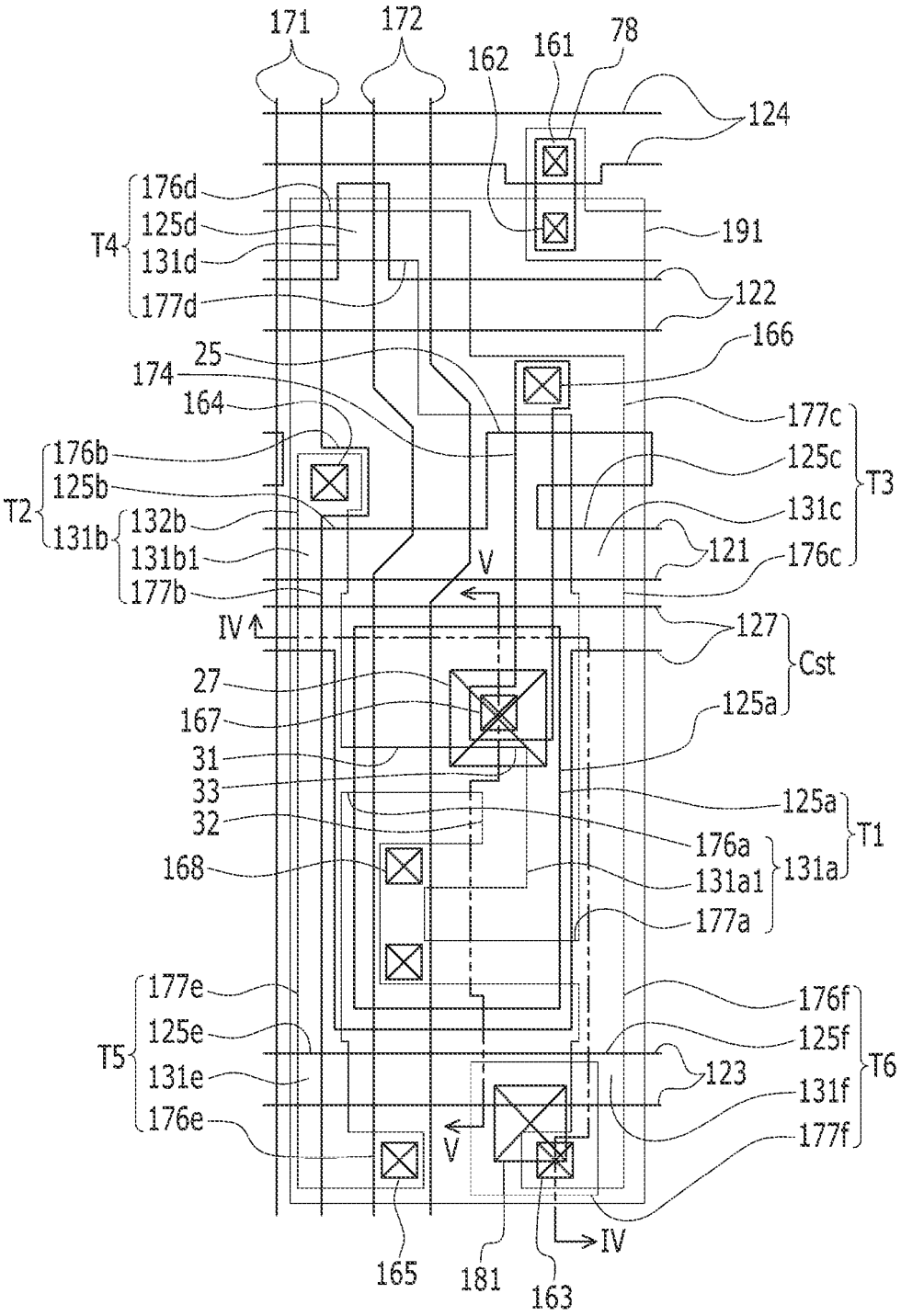
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FIG. 2



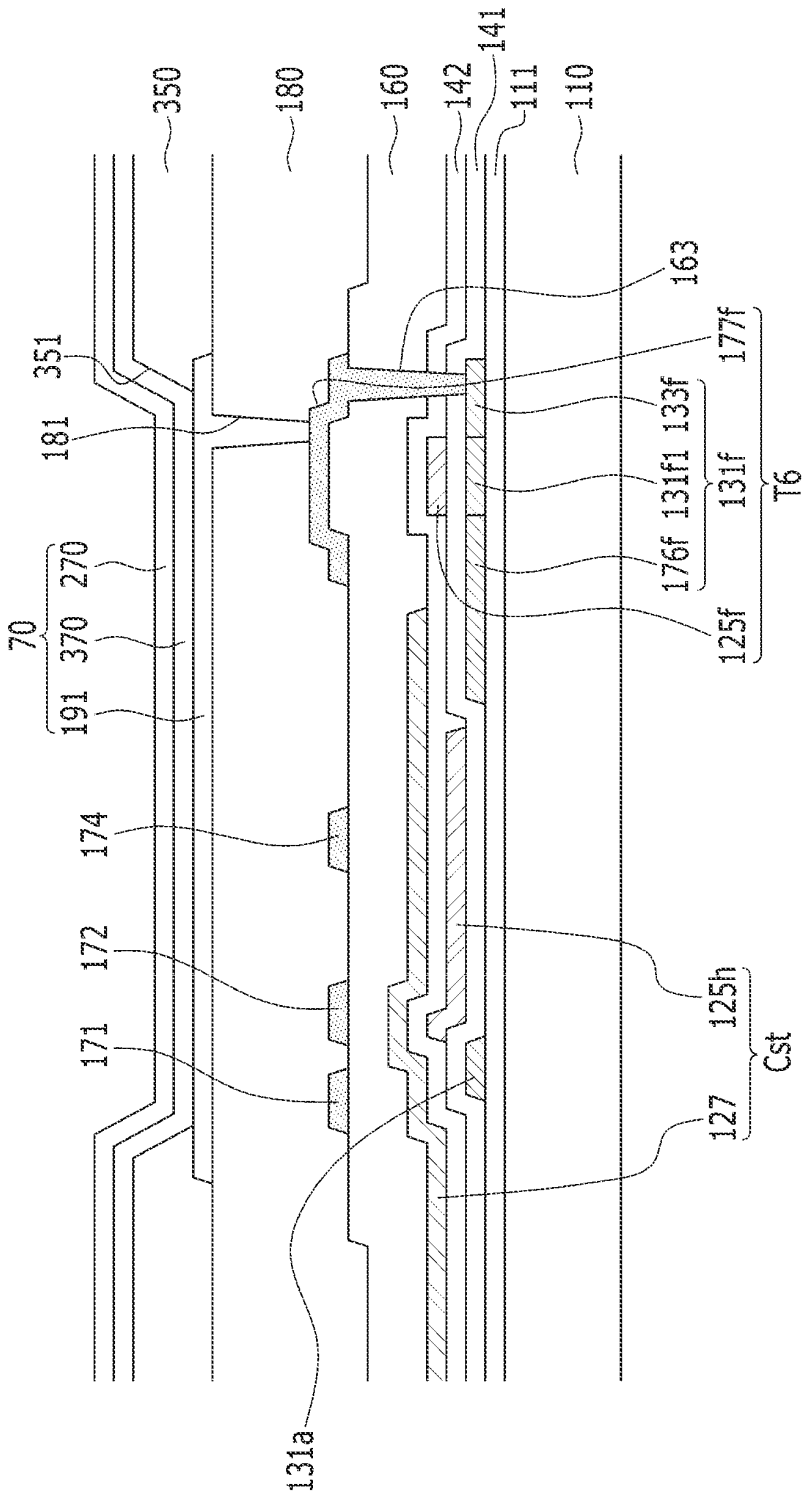
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FIG. 3



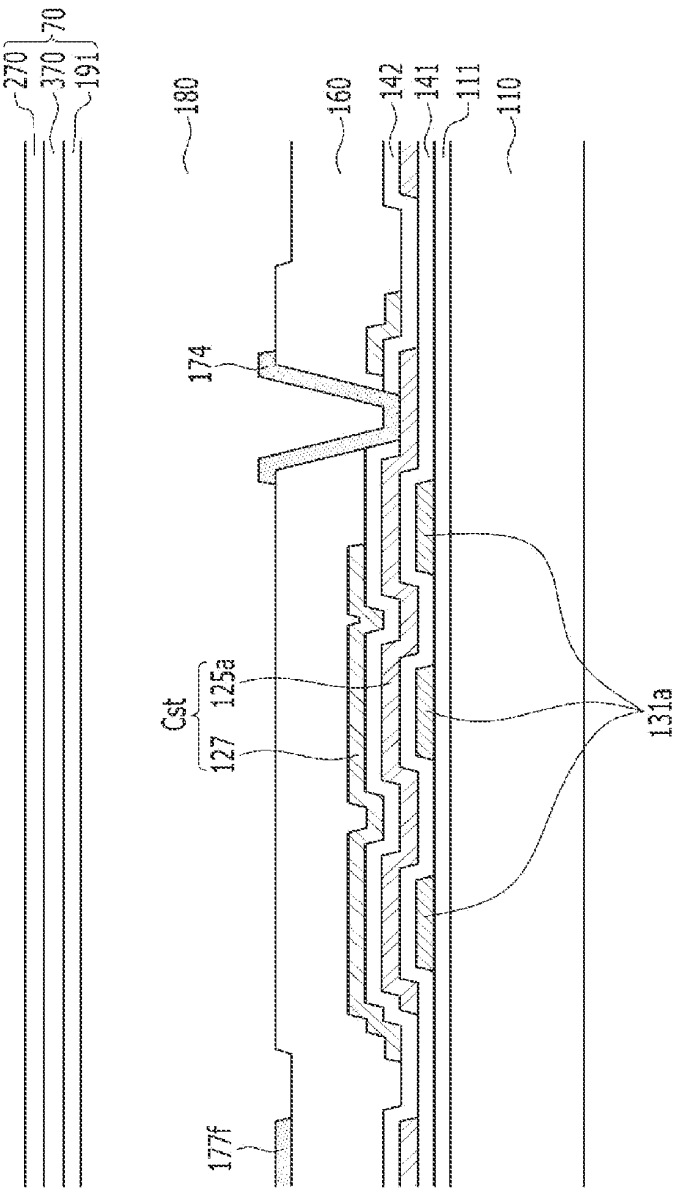
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FIG. 4



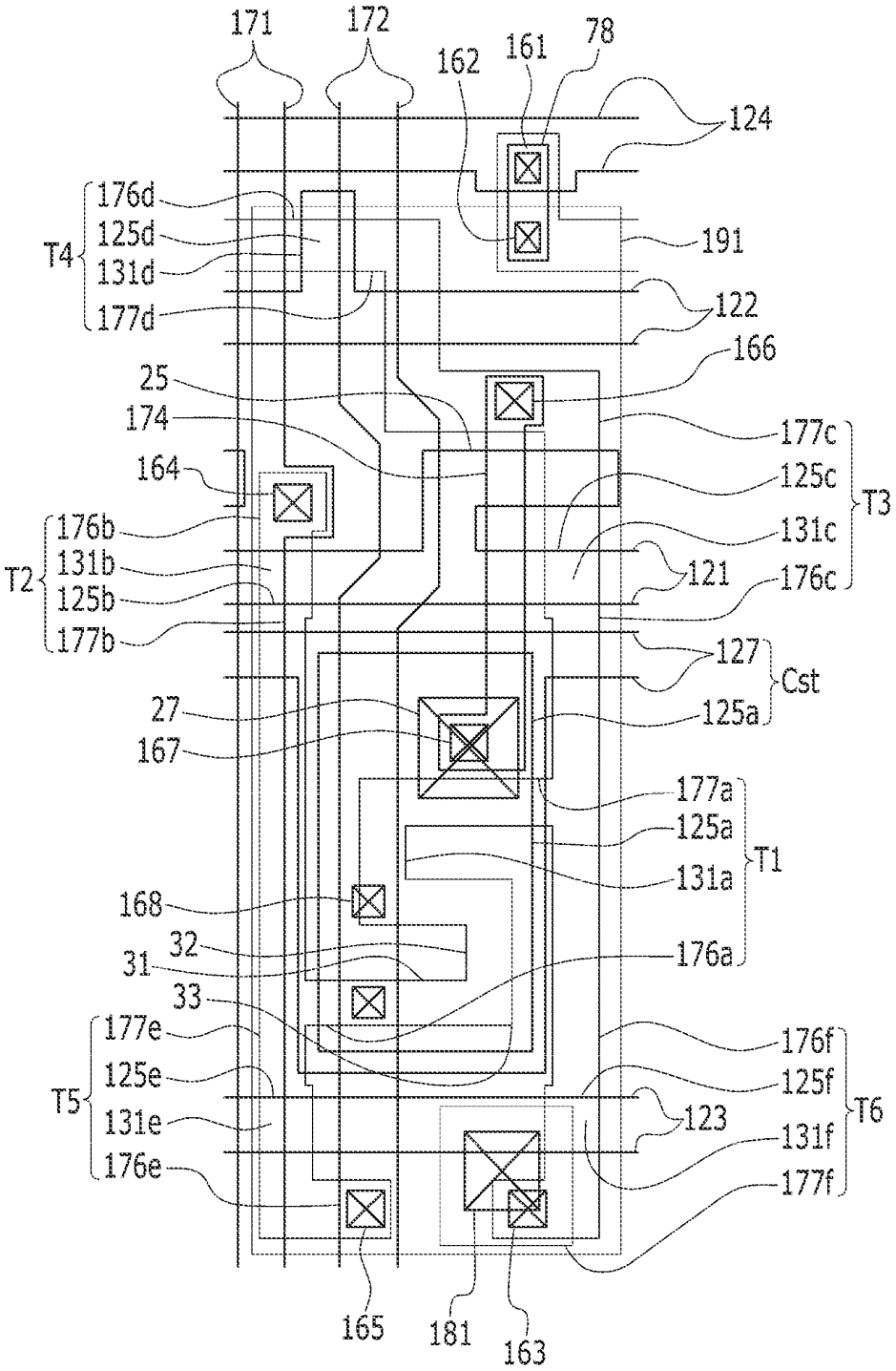
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FIG. 5



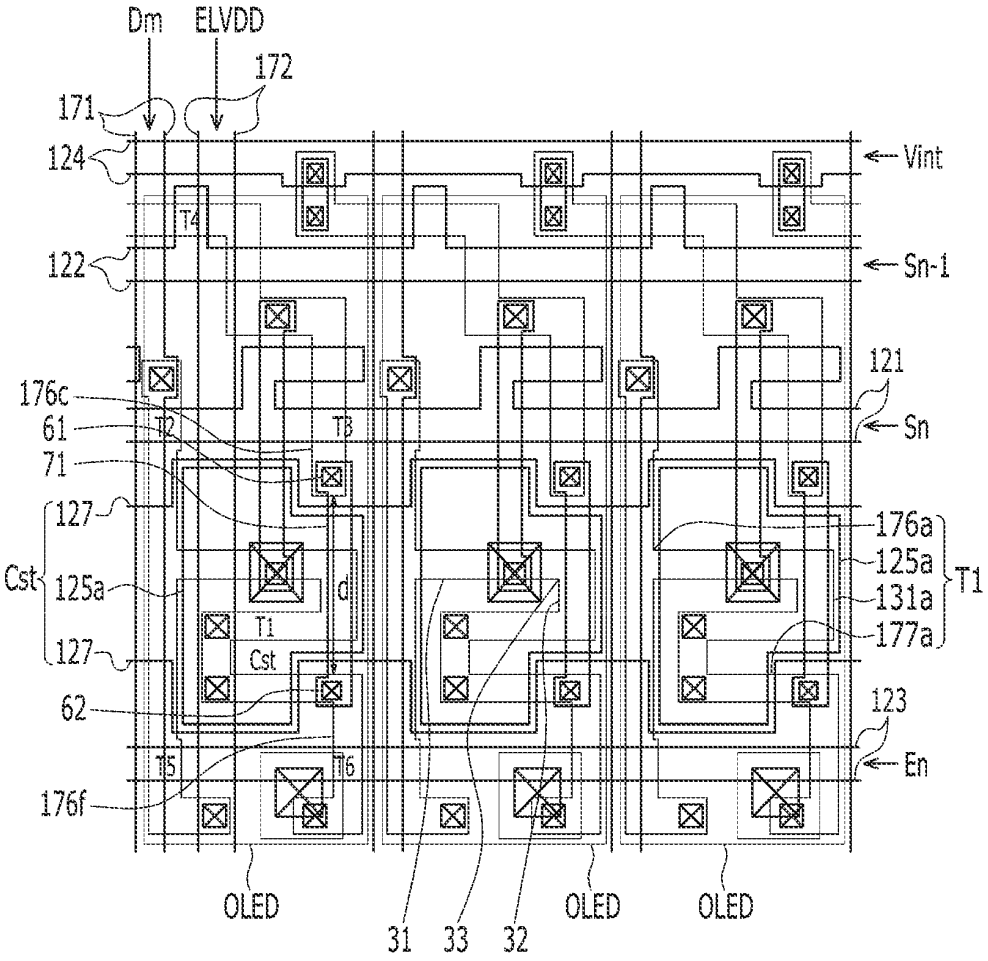
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FIG. 6



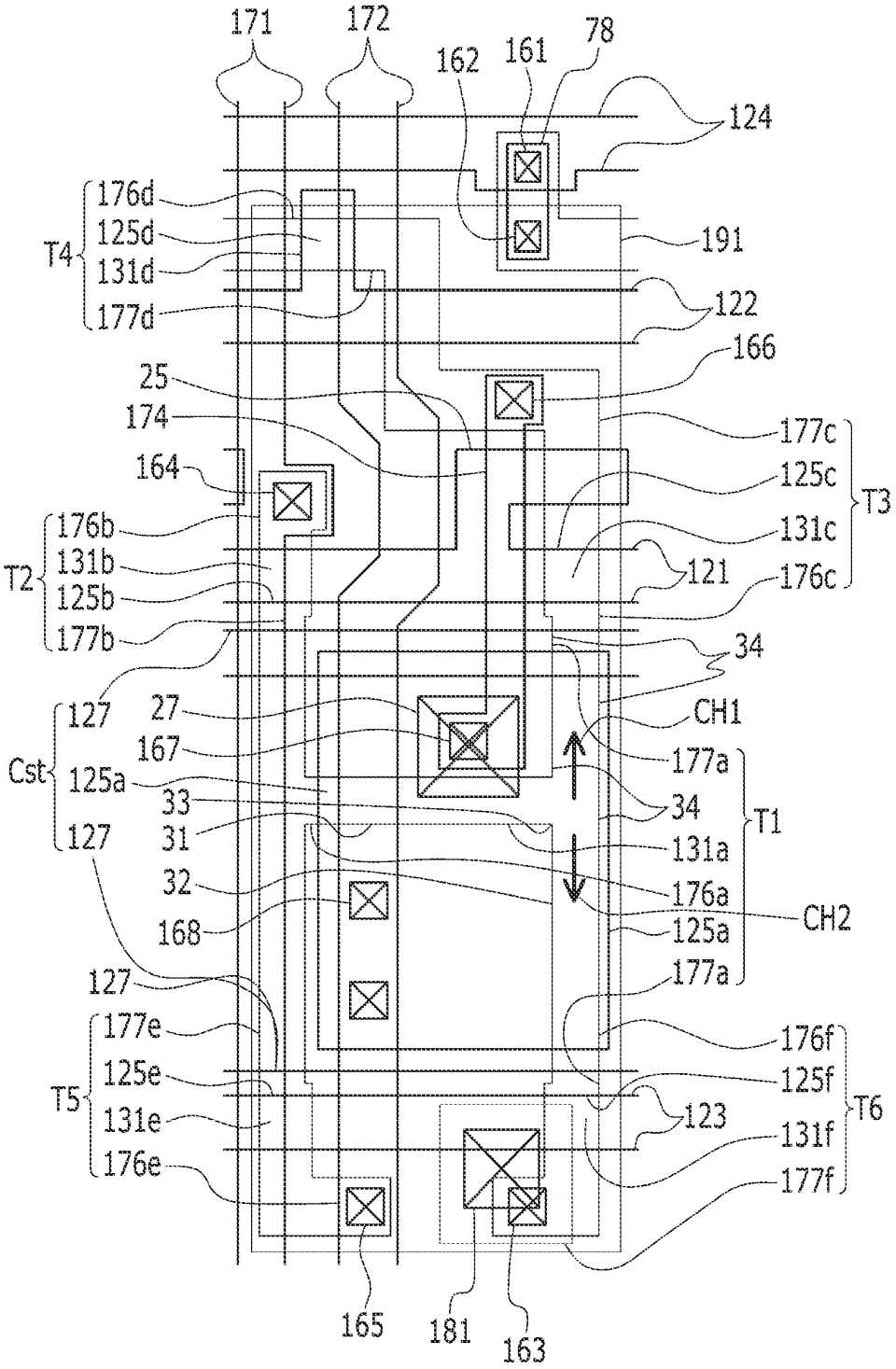
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FIG. 7



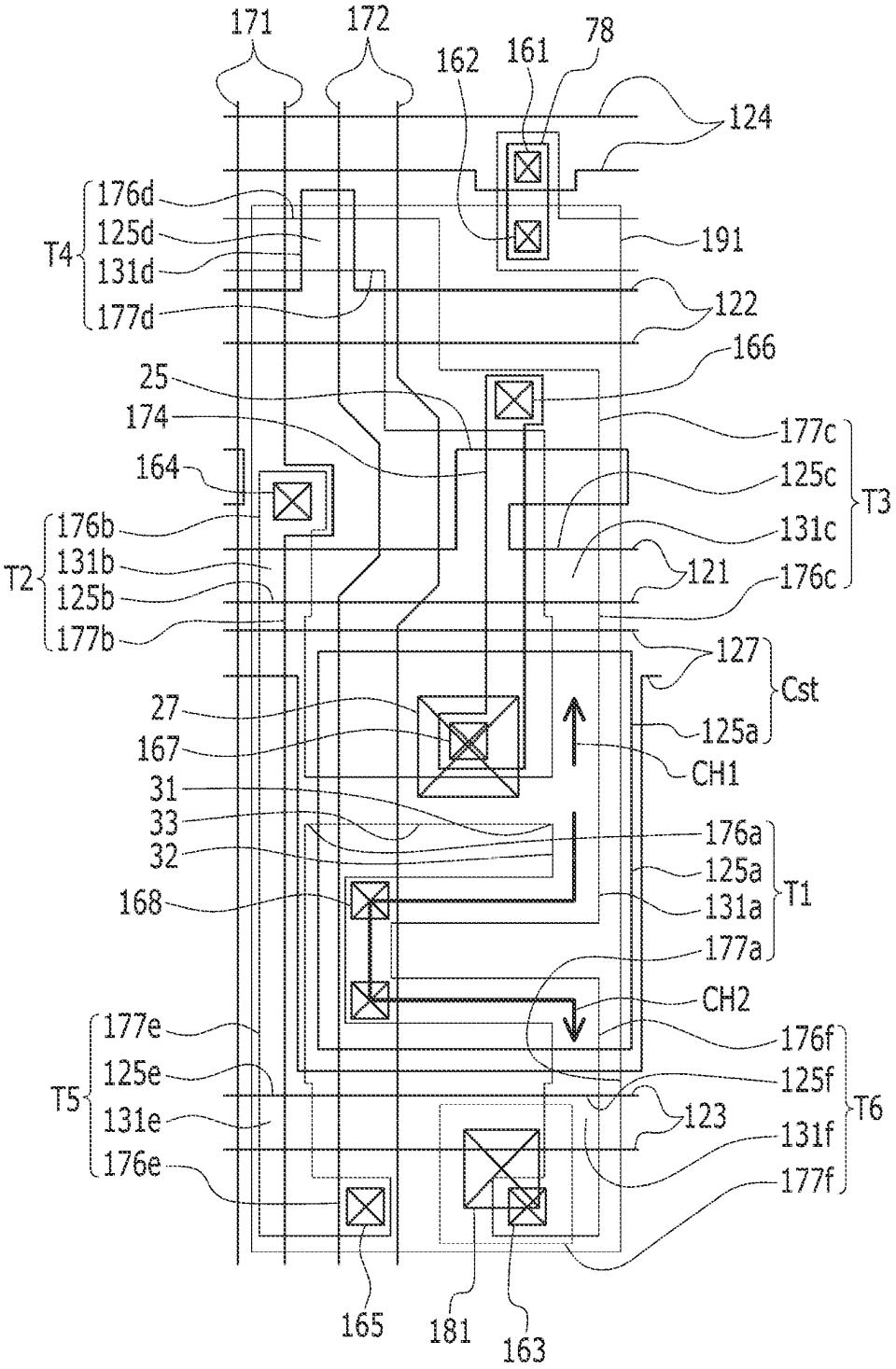
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FIG. 8



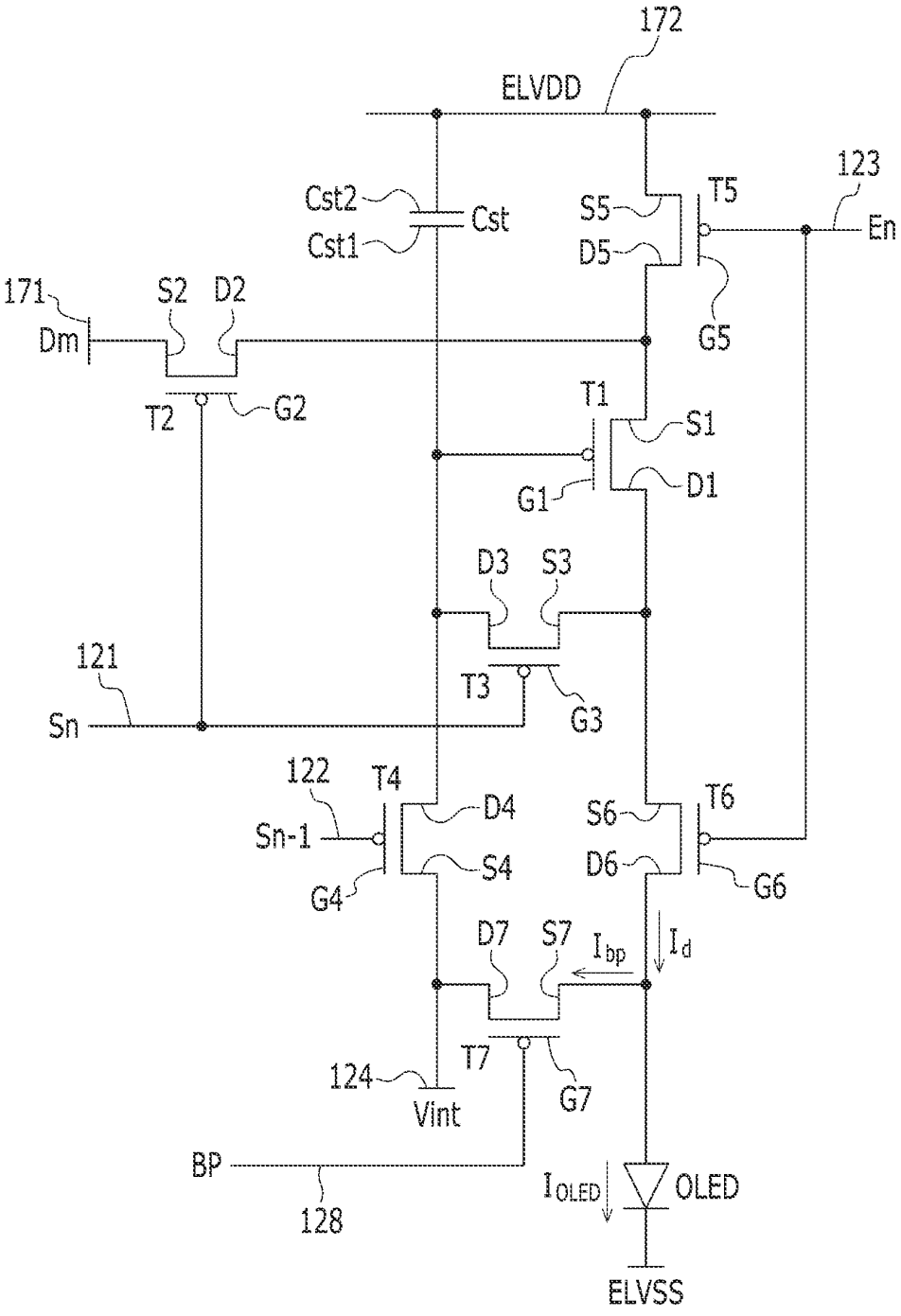
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FIG. 9



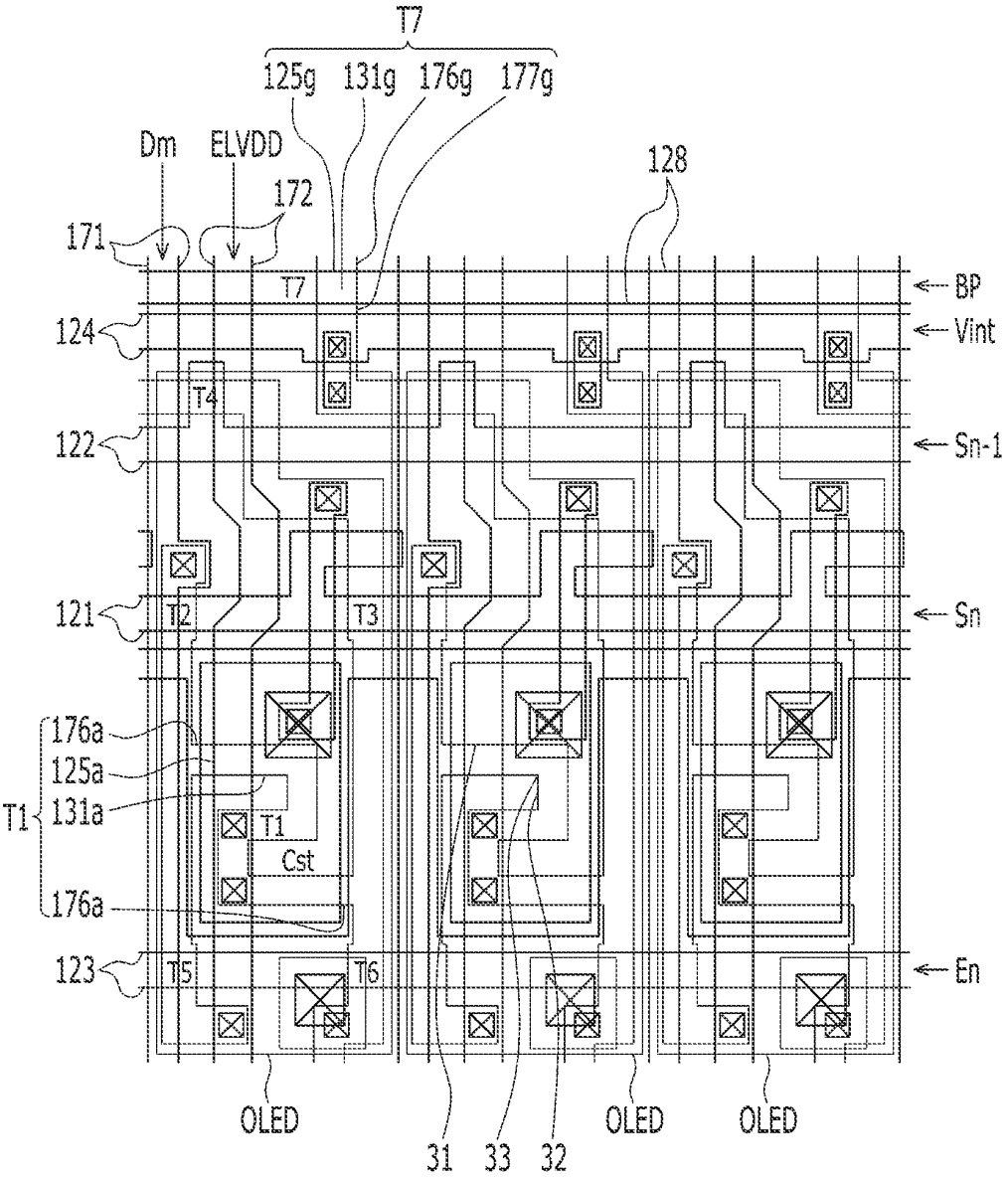
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FIG. 10



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FIG. 11



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INVENTOR'S DECLARATION AND ASSIGNMENT FOR PATENT APPLICATION PATENT

Title of Invention: ORGANIC LIGHT EMITTING DIODE DISPLAY

Docket No.: 70756/S1437

INVENTOR'S DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to:

__X__ The attached application; or

_____ United States Application or PCT International Application Number filed on .

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the above-identified application.

I have reviewed and understand the contents of the above-identified application, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, the undersigned,

(1) Se-Ho Kim, Jin-Woo Park, and Won-Se Lee

HEREBY SELL(S), ASSIGN(S) AND TRANSFER(S) TO

(2) Samsung Display Co., Ltd.

having a place of business at

(3) 95, Samsung 2-Ro, Giheung-gu, Yongin-City, Gyeonggi-do, 446-711 Republic of Korea

(hereinafter called "ASSIGNEE") the entire right, title and interest in and to any and all improvements which are disclosed in the application for United States Letters Patent entitled

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INVENTOR'S DECLARATION AND ASSIGNMENT FOR PATENT APPLICATION

Docket No. 70756/S1437

(4) ORGANIC LIGHT EMITTING DIODE DISPLAY

which application executed on even date herewith or was

(a) executed on (5a): July 12, 2013 ;

(b) filed on (5b): _____ ,

Application No.: _____ ;

(CHRISTIE, PARKER & HALE, LLP, P.O. Box 29001, Glendale, CA 91209-9001) is hereby authorized to insert in (b) the specified data, when known.

including any and all United States Patents which may be granted on said application, and any and all extensions, divisions, reissues, substitutes, renewals or continuations of said application and patents, and the right to all benefits under all international conventions for the protection of industrial property and applications for said improvements.

It is hereby authorized and requested that the Commissioner of Patents issue any and all of said Letters Patent, when granted, to said ASSIGNEE, its assigns or its successors in interest or its designee.

Upon said consideration, it is further agreed that, when requested, without charge to but at the expense of said ASSIGNEE, the undersigned will execute all divisional, continuing, substitute, renewal, and reissue patent applications; execute all rightful other papers; and generally do everything possible which said ASSIGNEE shall consider desirable for aiding in securing and maintaining patent protection as provided herein.

Se-Ho Kim
Legal Name of Inventor

July 12, 2013
Date

Se-Ho Kim
Signature

Jin-Woo Park
Legal Name of Inventor

July 12, 2013
Date

Jin-Woo Park
Signature

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INVENTOR'S DECLARATION AND ASSIGNMENT FOR PATENT APPLICATION

Docket No. 70756/S1437

Won-Se Lee
Legal Name of Inventor

July 12, 2013
Date

Won-Se Lee
Signature

WITNESSES:

SRH PAS1196564.1-*-07/9/13 12:35 PM

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