Electrical Characteristics of New LDD Poly-Si TFT Structure Tolerant to Process Misalignment

Byung-Hyuk Min and Jerzy Kanicki

***Abstract*—A new lightly doped drain (LDD) poly-Si TFT structure having symmetrical electrical characteristics independent of the process induced misalignment is described in this paper. Based on the experimental results, we have established that there is no difference between the bi-directional I_D–V_G characteristics, and a low leakage current, comparable to a conventional LDD poly-Si TFT, has been maintained for this new poly-Si TFT's. The maximum ON/OFF current ratio of about 1×10^8 is obtained for the LDD length of 1.0 μm. In addition, the kink effect in the output characteristics has been remarkably improved in the new TFT's in comparison to the conventional non-LDD single- or dual-gate TFT's.**

I. Introduction

POLYCRYSTALLINE silicon thin-film transistors (Poly-Si TFT's) can be used as switching devices or peripheral driving circuits in the active matrix liquid crystal display (AMLCD) [1], [2]. However, before poly-SI TFT can be used for the switching transistor, a leakage current must be reduced below 1 pA [3]. Dual-gate or lightly doped drain (LDD) structures have been proposed to reduce the leakage current of poly-Si TFT's [4], [5]. The leakage current in the dual-gate structure cannot be reduced completely, and its reduction is possible in LDD structures. However, in the LDD structure, the LDD length of the source and drain regions may not be exactly the same due to misalignment produced by photo-lithographic process. As a result, the LDD poly-Si TFT will exhibit asymmetrical device characteristics that threshold voltage and subthreshold slope will be different when the source and drain electrodes are switched [6]. The polarity between source and drain of poly-Si TFT in AMLCD must be altered to reduce the DC stress of liquid crystal. Therefore, the symmetric characteristics of LDD poly-Si TFT are essential features if the device is to be used as a switching transistor of pixel element. In this letter, we propose a novel LDD poly-Si TFT structure describing the symmetrical device characteristics independent of the process misalignment.

II. Device Structure

Fig. 1 shows the schematic structure of our novel LDD poly-Si TFT. The key feature of this novel device is a U-shaped active island, of which lower region acts as the channel region of the dual gate TFT structure. Both the source and drain regions are located on the same upper side of the U-shaped island (see Fig. 1), in contrast to the conventional co-planar TFT structure where the gate is between the source and drain electrodes. Even if the misalignment of the LDD lithographic process does exist, the misaligned length of both the source and drain will be varied in the same direction and their LDD lengths will always be identical.

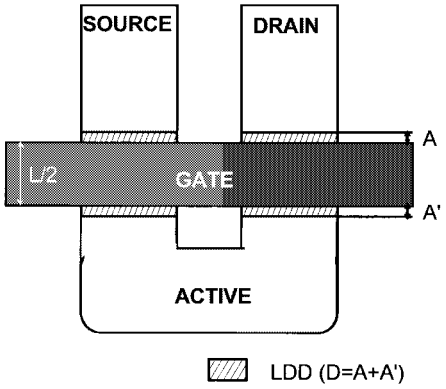


Fig. 1. Schematic structure of the novel LDD poly-Si TFT structure. The value of A (or A') is half of the total LDD length (D); A (or A') $= D/2$.

III. Device Fabrication

We have successfully fabricated both the conventional and novel poly-Si TFT's. First, the amorphous silicon films of 100 nm thickness were deposited on quartz substrate by LPCVD at 480 °C using Si_2H_6 gas. The active layer was crystallized at 600 °C for 30 h by solid phase crystallization (SPC) process [7]. After defining the active islands, 100-nm thick gate oxide was deposited by APCVD. A 200-nm thick amorphous silicon film was then deposited at 450 °C by LPCVD and was used as a gate electrode. The amorphous silicon and gate oxide was etched by RIE to form a gate electrode. A self-aligned phosphorous implantation of 5×10^{12} cm^{-2} at 30 KeV was carried out to form source and drain LDD region and the same implantation with the dose of 5×10^{15} cm^{-2} under the same conditions was performed, using LDD implantation mask, to produce source and drain electrodes. A passivation silicon oxide layer was deposited and the implanted ions were activated by thermal annealing at 600 °C for 20 h. Contact hole formation and metallization was carried out after ions activation. Finally, hydrogen passivation at 300 °C for 30 min was performed to improve the performance of the device [8].

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The authors are with the Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, MI 48109-2122 USA.

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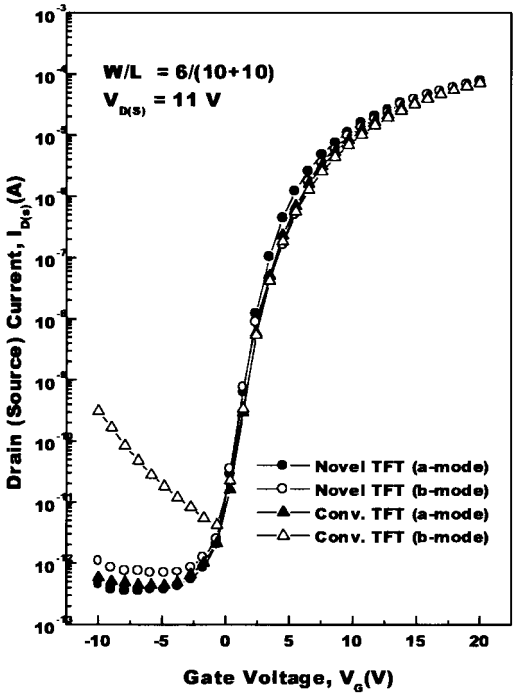


Fig. 2. I_D–V_G transfer characteristics of the conventional (Con.) and novel (New) poly-Si TFT's with the LDD length of 1.0 μm. "a-mode" means that the current flows from drain ($Vd = 11$ V) to source ($Vs = 0$ V). "b-mode" means that the current flows from source ($Vs = 11$ V) to drain ($Vd = 0$ V).

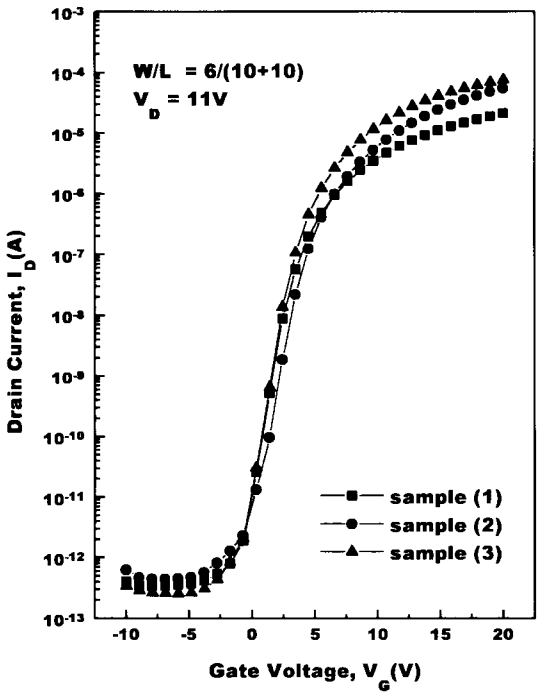


Fig. 3. I_D–V_G transfer characteristics of three novel poly-Si TFT samples where $D = 1.5$ μm. Sample (1): $A = 0$ μm, $A' = D$ μm; sample (2): $A = D$ μm, $A' = 0$ μm; and sample (3): $A = D/2$ μm, $A' = D/2$ μm.

IV. Experimental Results

First of all, we have characterized the electrical performance of both dual-gate and LDD TFT structures in order to examine the leakage current reduction. In the dual-gate TFT's, the leakage current does not decrease effectively although the gate gap increases from 2 μm to 6 μm. Moreover, the leakage current increases with negative gate voltages and is almost identical with a conventional single-gate TFT structure. From these results, we have concluded that the dual-gate poly-Si TFT's can not reduce completely the leakage current. We have also investigated the symmetrical characteristics of LDD poly-Si TFT's having various LDD lengths ranging from 0.5 μm to 3.0 μm. The leakage current is observed to have decreased remarkably as the LDD length is increased and the maximum ON/OFF current ratio in excess of 10^7 is obtained for the LDD length of 2.0 μm. In order to examine the symmetrical characteristics, we have compared bi-directional I_D–V_G characteristics when the voltages of the source and the drain electrodes are switched each other. In other words, 11 and 0 V are applied to the drain and the source electrodes for the a-mode and the same voltages are applied to the source and the drain electrodes for the b-mode (In Fig. 2). It has been found that the leakage current of the reverse mode characteristics is more different from that of the forward mode characteristics. This asymmetrical behavior of the leakage current may be attributed to the asymmetrical LDD length induced by the misalignment of the photo-lithographic process.

As shown in Fig. 2, the new LDD poly-Si TFT shows the symmetrical transfer characteristics in comparison to the conventional one. This indicates that the new device does not exhibit asymmetrical electrical performance such as threshold voltage shift and the variation of the sub-threshold slope when the source and drain electrodes are inter-exchanged with each other. In addition, the leakage current is considerably reduced as the LDD length is varied from 0 μm to 1.0 μm. The maximum ON/OFF current ratio of about 1×10^8 is obtained for the LDD length of 1.0 μm. In order to investigate the effect of LDD mask misalignment on the electrical characteristics of the novel device, we evaluated the transfer characteristics of three samples having the same LDD length (D). It should be noted that the LDD regions of these samples are placed

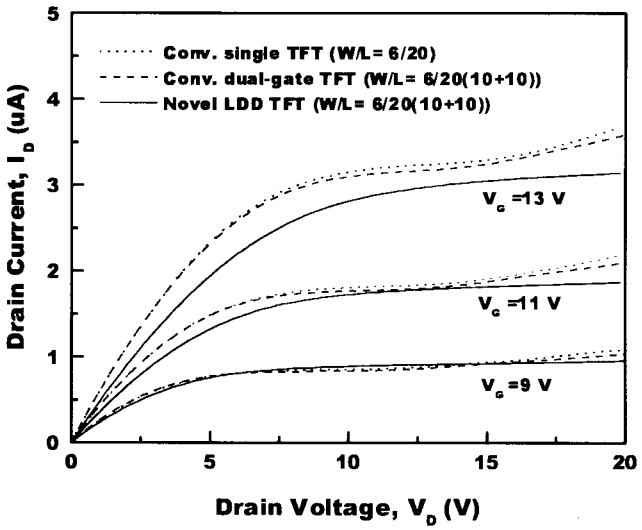


Fig. 4. Output characteristics of conventional single-, dual-gate, and novel LDD poly-Si TFT's.

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at different locations, while the total LDD lengths are kept constant for three samples: sample (1): $A = 0$ μm, $A' = D$ μm; sample (2): $A = D$ μm, $A' = 0$ μm; and sample (3): $A = D/2$ μm, $A' = D/2$ μm (see Fig. 1). Fig. 3 shows that the leakage currents and on-currents for these three samples are almost identical regardless of LDD locations, even though the on-current of sample (1) is slightly decreased. Therefore, we have clearly established that the novel poly-Si TFT has the misalignment margin of $D/2$, which is likely to be larger than the conventional poly-Si TFT structure. Also, Fig. 4 shows that the kink-effect in output characteristics has remarkably been improved in the novel poly-Si TFT in comparison to the conventional non-LDD single- or dual-gate poly-Si TFT's.

V. Conclusion

We have clearly demonstrated in this work that the novel poly-Si TFT is tolerant to the photo-lithographic misalignment and has symmetrical characteristics. Also, the leakage current remains constant independent of the negative gate biases and the ON/OFF current ratio of about 1×10^8 is obtained. The kink effect observed in output characteristics is remarkably improved in this new LDD poly-Si TFT's in comparison to the conventional non-LDD single- or dual-gate TFT's. Therefore, the new LDD poly-Si TFT is expected to function efficiently as a switching transistor of the pixel element for AMLCD's.

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