Asymmetric electrical properties of fork *a*-Si:H thin-film transistor and its application to flat panel displays

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Inverted stagger hydrogenated amorphous silicon (*a*-Si:H) fork-shaped thin-film transistors (TFTs) were fabricated with a five-photomask process used in the processing of the active-matrix liquid crystal displays (AM-LCDs). We investigated the asymmetric electrical characteristics of a fork-shaped *a*-Si:H TFT under different bias conditions. To extract the electrical device parameters, we developed asymmetric geometrical factors. Current-voltage measurements indicate that the ON-OFF current ratio of fork TFT can be enhanced significantly by choosing the outer electrode as the drain, while the field-effect mobility and threshold voltage have the identical values when different drain bias conditions are used. Finally, we developed concepts of its possible application to AM-LCDs. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3153968]

I. INTRODUCTION

Comblike contact electrodes have been generally used in bipolar power transistors to minimize current crowding,[1] while in metal oxide semiconductor field-effect transistors (MOSFETs), interdigitated electrodes were first adapted to achieve high W/L ratios in a limited layout space.[2,3] Organic thin-film transistors (TFTs) also employed these structures to improve ON-current characteristics.[4,5] Recently, the comb-shaped electrodes have been used in field-effect hydrogenated amorphous silicon (*a*-Si:H) solar cells to enhance output power.[6] In an *a*-Si:H TFT, one pair of interdigitated, so-called fork-shaped electrode was introduced to reduce gate-to-source capacitance and photoleakage current that are important for active-matrix liquid crystal displays (AM-LCDs).[7,8] However, so far, a detailed discussion of the geometrical effects of fork electrodes on *a*-Si:H TFT electrical properties and their possible application to flat panel displays have not been provided.

In this paper, first, we report on fork *a*-Si:H TFT electrical properties. More specifically, we studied the effects of drain bias polarity on fork TFT electrical properties. We also investigated the *a*-Si:H TFT geometrical effects on the extraction of key device electrical parameters such as subthreshold slope, field-effect mobility, and threshold voltage, which are important for AM-LCDs and active-matrix organic light-emitting devices (AM-OLEDs). Then, we discuss possible uses of this device in AM-LCDs as switching TFT. To our best knowledge, this paper represents the first investigation of the *a*-Si:H fork TFT asymmetric electrical characteristics and their impact on AM-LCDs and AM-OLEDs.

II. FORK *a*-Si:H TFT FABRICATION

The fork *a*-Si:H TFT consists of a rod-shaped inner electrode and a U-shaped outer electrode [Fig. 1(a)]. The bottom gate electrode is large enough to cover the entire area of device outer and inner electrodes. The fork *a*-Si:H TFT was fabricated using the normal AM-LCD five-photomask process steps.[9] More specifically, on the Corning Eagle2000 glass substrate, a bilayer of molybdenum (Mo, 500 Å) and aluminum-neodymium alloy (AlNd, 2000 Å) was deposited by a sputtering method. The Mo/AlNd gate electrode was then patterned by wet etching (mask 1). Following the gate electrode definition, a hydrogenated amorphous silicon nitride *a*-SiN_X:H (4000 Å)/*a*-Si:H (1700 Å)/phosphor-doped

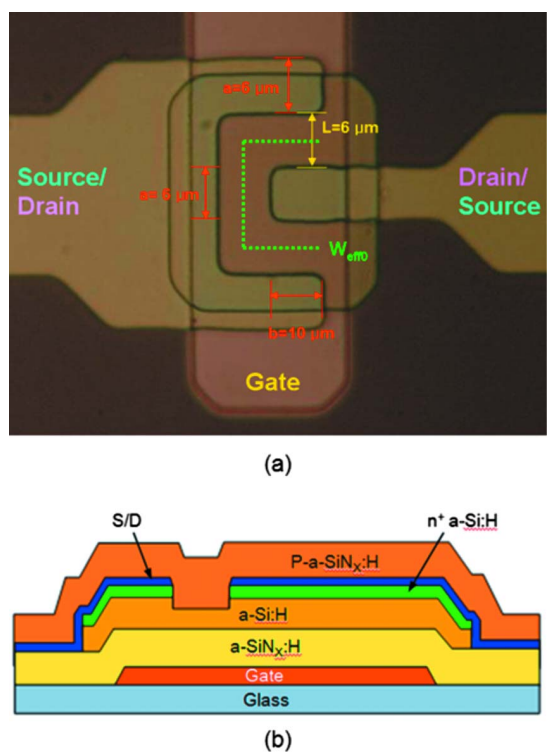

FIG. 1. (Color online) The configuration of fork TFT: (a) device top view and (b) cross-sectional view.

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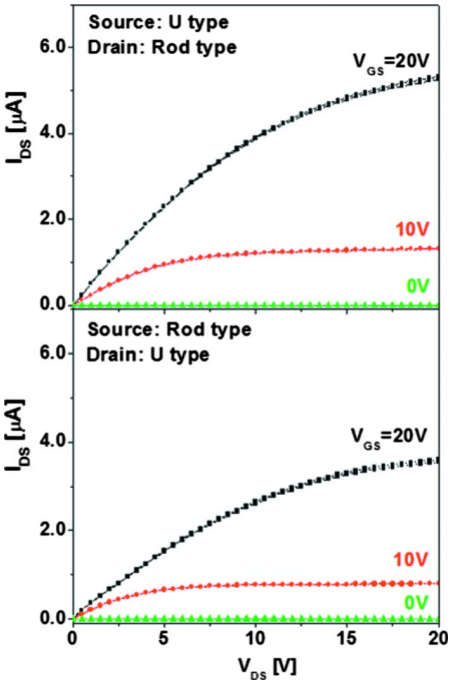

FIG. 2. (Color online) Output characteristics of fork *a*-Si:H TFT.

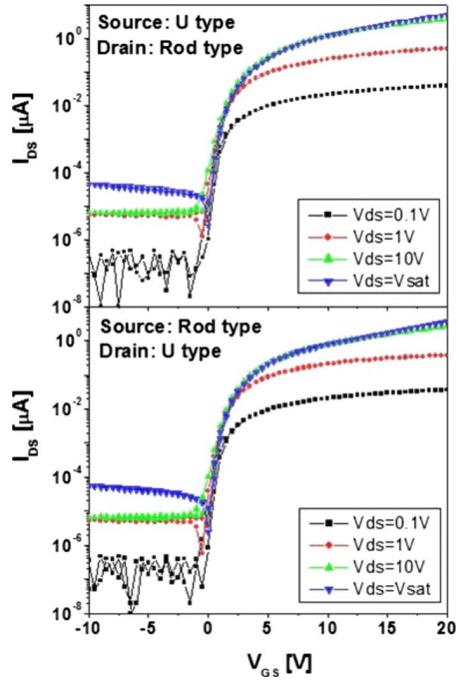

FIG. 3. (Color online) Transfer characteristics of fork *a*-Si:H TFT.

a-Si:H (n^+ *a*-Si:H, 300 Å) trilayer was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 350 °C to form a gate insulator and an active channel layer. After defining the device active island by reactive ion etching (RIE) (mask 2), a chromium (Cr, 1200 Å) layer was deposited by sputtering and source/drain (S/D) electrodes were patterned by wet etching (mask 3). Using a S/D metal and a photoresist as masks, the back-channel etching by RIE was performed. Then, we deposited *a*-SiN_X:H (3000 Å) as a passivation (*P*-*a*-SiN_X:H) layer by PECVD at 300 °C. To realize an electrical contact to electrodes (S/D and gate), vias were formed through the *P*-*a*-SiN_X:H layer by RIE (mask 4). After a contact via definition, indium tin oxide (500 Å) was deposited by a sputtering method at room temperature, and then pixel electrodes and probing pads were patterned by wet etching (mask 5). As a final step, the thermal annealing was performed for 1 h at 235 °C.

III. EXPERIMENTAL RESULTS

To characterize the electronic properties of fork *a*-Si:H TFT, we first measured the output characteristics (Fig. 2) by applying the drain bias under the following conditions: (1) ground was applied on the outer U-shaped source electrode, and drain voltage was applied on the inner rod-shaped drain electrode; (2) drain voltage was applied on the outer U-shaped drain electrode, and ground was applied on the inner rod-shaped source electrode. We swept the drain bias from 0 to 20 V for various gate voltages (0, 10, and 20 V). As shown in Fig. 2, at $V_{DS}=20$ V and $V_{GS}=20$ V, the output current for case (1) (5.3 μA) is 1.5 times higher than that for case (2) (3.6 μA).

Next, we measured the transfer characteristics of the fork *a*-Si:H TFT; we swept the gate bias from 25 to 0 V and swept it again from 0 to 25 V for various drain voltages (0.1, 1, 10, and 20 V). As shown in Fig. 3, at low drain voltage ($V_{DS}<1$ V), the ON currents are identical for both cases. However, at high $V_{DS}(>10$ V), the ON currents for case (1) are higher than those for case (2). Therefore, regardless of the gate bias and the direction of the drain bias applied, the ON currents would be the same for a low drain bias. However, when we apply a high drain bias, the ON-current levels can be increased significantly depending on the drain bias direction. However, at the same time, as the drain bias is increased from 0.1 to 10 V, the OFF currents for both cases (1) and (2) showed an identical behavior regardless of drain biases; they increased from $\sim 10^{-13}$ to $\sim 10^{-12}$. During gate bias sweeping, no significant hysteresis (ΔV_{GS}) in current-voltage characteristics was observed for both cases; at $V_{DS}=10$ V and $I_{DS}=0.1$ nA, both cases showed $\Delta V_{GS}=0.5$ $V_{case(1)}$ and 0.46 $V_{case(2)}$, which are acceptable for AM-LCDs.

IV. DISCUSSION OF *a*-Si:H TFT GEOMETRY EFFECT

The asymmetric behaviors of the fork *a*-Si:H TFT described above can be explained as follows. As the gate bias increases, a channel is formed in the active *a*-Si:H layer at the interface with the gate insulator. At low $V_{DS}(\sim 1$ V), since the channel is not affected by the drain voltage, the whole channel remains as the accumulation layer. Hence, effectively, the shape and length of the channel would be the same for both drain bias polarities, and we can define the device effective width $W_{eff0}(=a+2b+2L)$ as the peripheral line of the middle of the channel between source and drain electrodes, as shown in Fig. 1(a), where a is the width of the rod electrode, b is the overlapping distance between source and drain electrodes, and L is the channel length. This effective width can be used in both cases to extract the device field-effect mobility at low V_{DS} (linear regime) based on the

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ideal MOSFET model. The drain current is assumed to be constant at distance y from the drain electrode and can be expressed as $I_{DS}=W_{eff0}J_y$, where the current density J_y is a function of the electric field E_y and potential V_y: $J_y=\sigma E_y=\sigma dV_y/dy$. The resulting differential equation for the potential is expressed as

$$dV=\frac{I_{DS}}{W_{eff0}\sigma}dy, \tag{1}$$

where the conductivity $\sigma=\mu_{FE}C_{ox}[(V_{GS}-V_{th})-V_y]$, where C_{ox} is the oxide capacitance, μ_{FE} is the field-effect mobility, V_{GS} is the gate bias, and V_{th} is the threshold voltage of TFT. The integration of (1) from 0 to L yields the potential drop between the source and drain electrodes as

$$\int_0^{V_{DS}}[(V_{GS}-V_{th})-V_y]dV_y=\frac{I_{DS}}{W_{eff0}\mu_{FE}C_{ox}}\int_0^L dy. \tag{2}$$

Hence, the drain current for both bias polarities can be expressed as

$$I_{DS}=\frac{W_{eff0}C_{ox}\mu_{FE}}{L}[(V_{GS}-V_{th})V_{DS}-V_{DS}^2/2]. \tag{3}$$

However, output and transfer characteristics at high V_{DS} (>10 V) are quite different from those measured at a low V_{DS}. As discussed above, at high V_{DS}, ON current is higher for drain bias condition (1) than for drain bias condition (2). Assuming that the device is an ideal crystalline silicon MOSFET, field-effect mobility remains identical for both conditions; the current flowing through TFT can only be strongly dependent on the values of the channel width and length. Therefore, at high V_{DS}, we need to define different geometrical factors f_g for each drain bias condition to accommodate for differences in device electrical properties. When TFT operates in the saturation regime at high V_{DS}, we can assume that the channel depletion region at the drain electrode would be increased by a certain value. This change is referred to the channel length modulation factor (ΔL). However, in fork a-Si:H TFT, due to the unique device geometry, we can expect that ΔL would be different depending on the drain bias condition and the position of drain and source electrodes.[10] If the drain bias fully depletes the channel by ΔL from the edge of the drain electrode, the electric field at the depletion-region edge of the drain electrode can be expressed by Gauss' law; the charge contained in a volume (ρ) equals the permittivity ($\varepsilon_{a\text{-Si}}$) of a-Si:H times the electric field emanating from the volume,

$$\oint \rho dV=\varepsilon_{a\text{-Si}}E. \tag{4}$$

If the drain bias creates the same number of the depletion-region charge per unit volume (Q_d) for both drain bias conditions, the electric field for each condition can be expressed by

$$E_1\cong\frac{Q_d\times x_i\times(a+2\Delta L_1)\times(b+\Delta L_1)}{\varepsilon_{a\text{-Si}}}, \tag{5a}$$

$$E_2\cong\frac{Q_d\times x_i\times[2(a+2\Delta L_2)\times(b+\Delta L_2)+(a+2L-2\Delta L_2)\Delta L_2]}{\varepsilon_{a\text{-Si}}}, \tag{5b}$$

where x_i is the depletion width of the drain depletion region and W_R is the width of the outer ring electrode. Therefore, if the electric field at the drain depletion region would be the same for both conditions ($E_1=E_2$), since the size of the drain electrode is larger for condition (2) than for condition (1), the depletion region at the drain side for condition (1) is expected to be larger than that for condition (2) ($\Delta L_1>\Delta L_2$), as shown in Figs. 4(a) and 4(b). It should be noted that due to the unique bottom-gate fork TFT structure, the formed channel is expected to extend even below the source electrode, as shown in Fig. 4. However, it is well known that in a-Si:H TFT, the drain current does not flow through the whole source electrode length but is rather limited to a specific length, the so-called TFT characteristic length (L_T) (Ref. 11) near the electrode edge. Therefore, the characteristic length for drain bias conditions (1) and (2) can be defined as L_{T1} and L_{T2}, respectively. To estimate L_{T1} and L_{T2}, we measured the channel resistance (r_{ch}) and S/D contact resistance ($R_{S/D}$) for four fork TFTs with different channel lengths for each drain bias condition. From the measurements, the TFT characteristic lengths ($=R_{S/D}/r_{ch}$) were calculated as 1.5 μm ($=L_{T2}$) and 1.0 μm ($=L_{T1}$) at $V_{GS}=15$ V, respectively. From the experimental results, we can speculate that L_{T2} is larger than L_{T1} because the size of the electrode acting as an electron source is smaller for drain bias condition (2) than for drain bias condition (1).

Based on these assumptions, to derive the equation for the drain current in the saturation regime, the same methodology was applied here as one used for the derivation of Eq. (1); the integration of Eq. (2) from ΔL_1 to $L+L_{T1}$ for drain bias condition (1) and from $-L_{T2}$ to $L-\Delta L_2$ for drain bias condition (2) yields the potential drop between the source and drain electrodes for each case, respectively. At the same time, the effective channel width also changes due to different depletion regions for different bias conditions,

$$\int_0^{V_{DS}}[(V_{GS}-V_{th})-V_y]dV_y=\frac{I_{DS}}{W_{eff1}\mu_{FE}C_{ox}}\int_{\Delta L_1}^{L+L_{T1}}dy,$$
$$\text{where } W_{eff1}=a+2\Delta L_1+2(b+\Delta L_1), \tag{6a}$$

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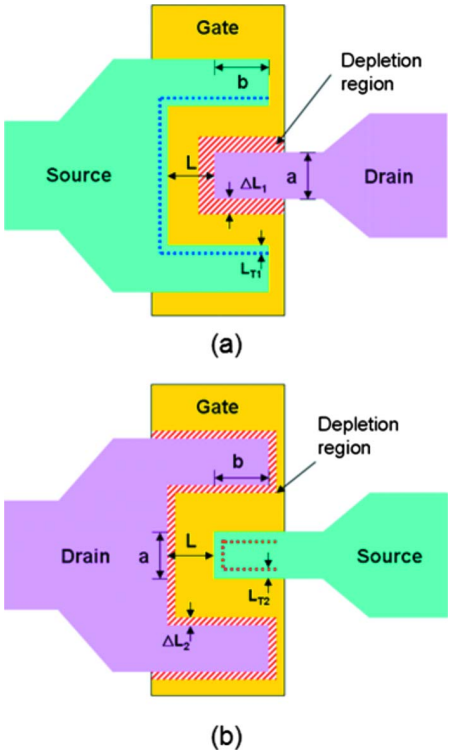

FIG. 4. (Color online) The schematic top views of depletion regions in fork *a*-Si:H TFT: case (1) where source is applied on U-shaped electrode and case (2) where source is applied on rod-shaped electrode.

$$\int_0^{V_{DS}} [(V_{GS} - V_{th}) - V_y] dV_y = \frac{I_{DS}}{W_{eff2}\mu_{FE}C_{ox}} \int_{-L_{T2}}^{L-\Delta L_2} dy,$$

$$\text{where } W_{eff2} = a + 2(b + \Delta L_2). \tag{6b}$$

It should be noted that electrons are assumed to move along the shortest path, the channel length (L) only, not at the corner of the U-shaped electrode for both bias conditions (1) and (2).

To find the values for ΔL_1 and ΔL_2 and the corresponding equations for the asymmetric drain current, we do the asymmetric current calculation of fork *a*-Si:H TFT based on the standard TFT with the same length as reference width $W=20$ μm and length $L=6$ μm. The output drain current of the conventional standard TFT was measured at $V_{GS}=20$ V and then normalized with its width over length ratio ($W/2L$) to be used as a reference value for the current calculation. Since both fork and standard *a*-Si:H TFTs have been fabricated over the same substrate at the same time, we expect that their normalized electrical properties are equivalent and only the geometries are different. Using the normalized output drain current of the standard TFT, we calculated the output drain current of the fork TFT for each bias condition by multiplying the normalized standard TFT characteristic by geometric factors defined in Eq. (7) (output current of fork TFT=normalized output current of standard TFT $\times$geometrical factor). By fitting several different values of ΔL_1 and ΔL_2 onto integrations above, we could find proper values for the channel length modulation factors empirically as $\Delta L_1 = L/4$ for condition (1) and $\Delta L_2 = L/10$ for condition (2), respectively. Hence, since $V_{DS}=(V_{GS}-V_{th})$ in the saturation regime, the drain current for each condition can be expressed with corresponding geometrical factors f_{g1} and f_{g2},

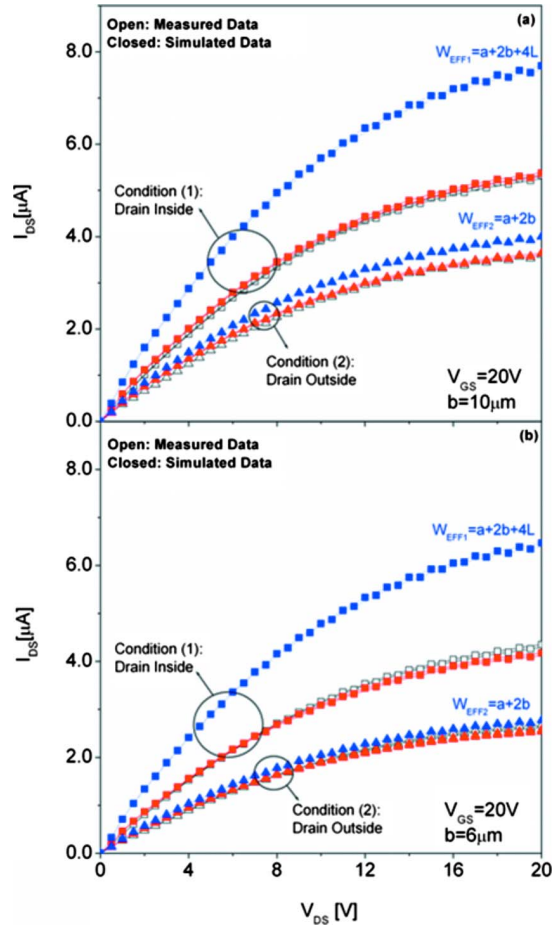

FIG. 5. (Color online) Measured (open symbol) and calculated (closed symbol) output characteristics of fork *a*-Si:H TFTs. (a) $a=6$ μm and $b=10$ μm. (b) $a=6$ μm and $b=6$ μm.

$$I_{DS}^{\text{condition (1)}} = f_{g1}\mu_{FE}C_{ox}(V_{GS} - V_{th})^2,$$

$$\text{where } f_{g1} = \frac{a + 2\Delta L_1 + 2(b + \Delta L_1)}{L + L_{T1} - \Delta L_1}, \tag{7a}$$

$$I_{DS}^{\text{condition (2)}} = f_{g2}\mu_{FE}C_{ox}(V_{GS} - V_{th})^2,$$

$$\text{where } f_{g2} = \frac{a + 2(b + \Delta L_2)}{L + L_{T2} - \Delta L_2}. \tag{7b}$$

As shown in Eq. (7), in the saturation regime, values of the geometrical factor can have a direct impact on drain current values. When a and b in Eq. (7) are replaced with the actual measured values ($a=6$ μm and $b=10$ μm), the geometrical factor in condition (1) turns out to be larger than that in condition (2) by about 1.5 times. Therefore, the ON current for drain bias condition (1) is expected to be larger than that for drain bias condition (2) by the difference in the geometrical factors. As shown in Fig. 5, we could exactly match the measured output drain current of the fork TFT for each drain bias condition. It should be noted that when the intuitive channel width [$W_{EFF1}=a+2b+4L$ for condition (1) and $W_{EFF2}=a+2b$ for condition (2)] is used as the circumference of the source electrode instead of the geometrical factors

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given by Eq. (7), the calculated drain current values are much larger than the experimental values [Fig. 5(a)]. To validate these equations of geometrical factor, we measured another set of fork TFT with different dimensions ($a=6$ μm and $b=6$ μm) for a smaller fork TFT. Again, the standard TFT is normalized by $W/2L$ to be used as a reference for the calculated drain current. As shown in Fig. 5(b), though there is a little deviation observed for drain bias condition (1), the measured output drain current of fork TFT could only be exactly matched when the normalized drain current of the standard TFT is multiplied for each bias condition by the defined geometrical factor as defined in Eq. (7). Again, when the intuitive channel width [$W_{\mathrm{EFF1}}=a+2b+4L$ for condition (1) and $W_{\mathrm{EFF2}}=a+2b$ for condition (2)] is used instead of the geometrical factor, the calculated output drain current of fork TFT shows a huge difference from the measured values especially for bias condition (1).

The OFF current in the a-Si:H TFT is originated from carriers generated in the depletion region on the drain side (at high V_{DS}) when the negative gate bias is applied. Under $V_{\mathrm{GS}}<0$, the a-Si:H is fully depleted and hole accumulation takes place near the $a-$Si:H/a-SiN$_X$:H interface, creating a hole current. The current level is limited by the n^+-a-Si:H S/D contact regions (these are hole blocking contacts). If we assume that two quasi-n^+-p junctions are formed between the drain and source n^+ regions and hole (p) conduction channel, the drain n^+-p junction is under a reverse bias ($V_{\mathrm{DS}}>0$), which is similar to an n^+-p junction in the OFF state. Indeed, in a regular n^+-p junction, the OFF current is carried by a minority carrier generated in the depletion region. The OFF current (J_g) in this region can be limited by the generation rate of carriers and the depletion width x_i, as shown in the following equation:

$$J_g=\frac{qn_ix_i}{2\tau_0}, \tag{8}$$

where q is the electron charge, n_i is the maximum generation rate, and τ_0 is the lifetime of the excess carrier in the depletion region. If we assume that the width of the depletion region and the generation rate are identical for both drain bias conditions at high V_{DS}, the OFF current can depend only on the volume of the depletion region (= the area of drain electrode $\times$ the depletion width, x_i) for each bias condition. Therefore, since the area of the drain electrode is larger in drain bias condition (2) than in drain bias condition (1), the OFF current for condition (2) is expected to be higher than that for condition (1).

V. DEVICE PARAMETER EXTRACTION

From the TFT data shown in Figs. 2, 3, and 6, we can extract the subthreshold slope (S), threshold voltage, and field-effect mobility values. We chose the center position (at $I_{\mathrm{DS}}=10^{-10}$ A) in the transfer curve of log(I_{DS}) versus V_{GS} and used the linear fitting by taking two log(I_{D}) values around the center point to extract the S value.

The field-effect mobility (μ_{FE}) and threshold voltage can be calculated as follows: from the transfer curve of I_{D} versus V_{GS}, we chose a specific value of I_{D} at $V_{\mathrm{GS}}=15$ V. By taking

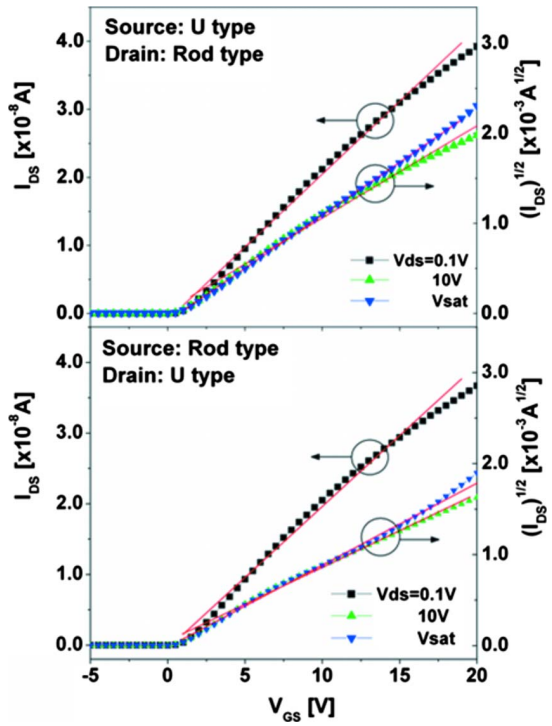

FIG. 6. (Color online) Transfer characteristics of fork a-Si:H TFT. Curves used for extraction of the threshold voltage and mobility are also shown.

90% and 10% of this selected I_{D} value, we define the fitting range in I_{D} versus V_{GS} experimental characteristics. From the slope and x-axis intercept of the calculated curve, the field-effect mobility and threshold voltage have been extracted using Eqs. (3) and (7) with different geometrical factors. Calculated device parameters are summarized in Table I for the linear (low V_{DS}) and saturation (high V_{DS}) regions, respectively. For comparison, we also calculated the field-effect mobility (μ_{FE}) and threshold voltage by using the maximum slope method,[12] which is usually used for crystalline silicon devices. The field-effect mobility is calculated from the transconductance maximum (g_m) value using the following equations:

$$\mu_{\mathrm{linear}}=\frac{Lg_{\mathrm{m\text{-}linear}}}{W_{\mathrm{eff0}}C_{\mathrm{ox}}V_{\mathrm{DS}}}, \tag{9a}$$

$$\mu_{\mathrm{saturation}}=\frac{g^2_{\mathrm{m\text{-}saturation}}}{f_{g1,2}C_{\mathrm{ox}}}, \tag{9b}$$

where $g_{\mathrm{m\text{-}linear}}$ is the maximum transconductace at $V_{\mathrm{DS}}=0.1$ V and $g_{\mathrm{m\text{-}saturation}}$ is the maximum transconductance at

TABLE I. Extracted parameters of fork TFT: case (1) where source is applied on U-shaped electrode and case (2) where source is applied on rod-shaped electrode.

	$V_{\mathrm{DS}}=0.1$ V		$V_{\mathrm{DS}}=V_{\mathrm{sat}}$	
Case	(1)	(2)	(1)	(2)
S (mV/decade)	386	375	485	494
V_{th} (V)	0.73	0.66	0.61	0.84
μ_{FE} (cm^2/V s)	0.32[a]	0.34[a]	0.35[b]	0.39[c]

[a]Geometrical factor W_{eff0}/L used to extract the parameter.
[b]Geometrical factor f_{g1} used to extract the parameter.
[c]Geometrical factor f_{g2} used to extract the parameter.

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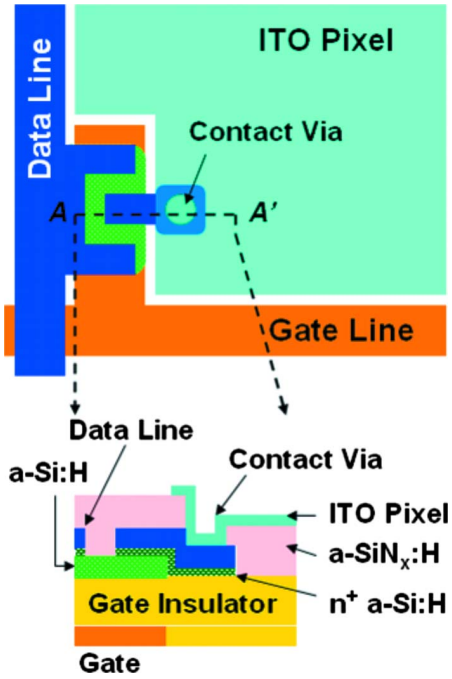

FIG. 7. (Color online) Top views and cross sections of fork *a*-Si:H TFT for AM-LCD.

$V_{DS}=V_{sat}$. From the V_{GS} value of the maximum g_m as a reference, two closest points are chosen for straight line fitting through the three points on the transfer curve of I_D-V_{GS}. The threshold voltage can be estimated from the *x*-axis intercept of this extrapolated line for each drain bias condition (Fig. 6). Resulting extracted parameters are summarized in Table I. It is clear from this table that those two calculation methods provide very similar mobility and threshold voltage values for fork *a*-Si:H TFTs (within experimental error).

As shown in the table, due to a lower OFF current, the subthreshold slope is much lower for drain bias condition (1), while the field-effect mobility and threshold voltage are similar for both bias conditions. Therefore, asymmetric biasing of the fork TFT can change the ON-current characteristics, while the OFF current and field-effect mobility remain the same regardless of bias conditions. Along with the minimized pixel (rod-shaped electrode)-to-gate capacitance (C_{GS}) compared to a normal TFT, these unperturbed characteristics can be very advantageous when the device is used as a switching device for AM-LCDs, which will be discussed in Sec. VI.

VI. POSSIBLE APPLICATIONS OF FORK *A*-SI:H TFTS TO FLAT PANEL DISPLAYS

When the device is used as a switching TFT, as shown in Fig. 7, and when the source is applied to a rod-shaped electrode, with a minimized overlapped area between the gate and pixel electrodes, the fork TFT has an advantage of having a much smaller parasitic pixel-to-gate capacitance (C_{GS}) than the normal TFT. By Eq. (10), this will provide a minimum pixel voltage drop (error voltage) with a gate pulse in the OFF state,[13]

$$\Delta V_p = \frac{C_{GS}(V_{GH} - V_{GL})}{C_{GS} + C_{LC} + C_{ST}}, \tag{10}$$

where V_{GH} is the switch turn-on gate voltage, V_{GL} is the switch turn-off gate voltage, C_{LC} is the capacitance of LC, and C_{ST} is the storage capacitance. By achieving a low error voltage, flicker and sticking image defects can be significantly reduced,[13] and as a result, the display quality of the *a*-Si:H TFT AM-LCD can be improved. In the AM-LCD driving scheme, the polarity of the data line bias usually changes from line to line with respect to the common line-inversion method;[14] hence, the positions of drain and source in the TFT should be opposite in odd and even data lines. In such a case, as mentioned above, fork TFTs in the active-matrix array will have different ON-current but same OFF-current values for different lines. Since the ON current is only used for charging the storage capacitor, the asymmetric ON current will not influence the storage capacitor voltage as long as the switch turn-on time is long enough. Since the TFT switch turn-off time is relatively very long compared with the switch-on time in the AM-LCD operation, the symmetric OFF-current behavior of the fork *a*-Si:H TFT regardless of the bias condition can make this device the optimum switching device for AM-LCDs. In addition, although there is a variation of 0.08 V (linear) ~0.33 V (saturation) on the threshold voltage under different bias conditions, since the scan voltage (>20 V) is much higher in comparison to the threshold voltage, the effect of this variation is negligible in the switching operation of AM-LCDs.

While the achievement of a minimized C_{GS} is critical in AM-LCDs due to the pixel voltage drop, this error voltage is not critical in AM-OLEDs. Since the organic light-emitting device is a self-luminescent device controlled by the current, the line- or dot-inversion programming method is not used in AM-OLEDs. Hence, achieving minimum C_{GS} to minimize the pixel voltage drop caused by the inversion programming is not so important for AM-OLEDs.

Since the fork TFT in comparison to the standard TFT has a relatively low ON current in spite of a large geometry, this device is not the best candidate for a switching or driving TFT for AM-OLEDs. Moreover, since the U- and rod-shaped electrodes provide a nonuniform electric-field distribution in the channel and create local electric-field crowding due to sharp corners, fork TFT is expected to have a more serious electrical instability in comparison to standard TFTs when used in AM-OLED pixel electrode circuits. We expect that by removing the sharp corners from the device electrodes, for example, by its patterning into circular shapes in Fig. 8, the locally intensified electric field in the channel can be alleviated to give a better device overall electrical performance and stability.[15]

VII. CONCLUSIONS

In this research, we have studied the electrical characteristics of the fork *a*-Si:H TFT under different drain bias conditions. Due to the unique fork device geometry, when the source is connected to the outer U-shaped electrode, the ON current is 1.5 times higher than when the source is applied to the inner rod-shaped electrode at high drain voltages

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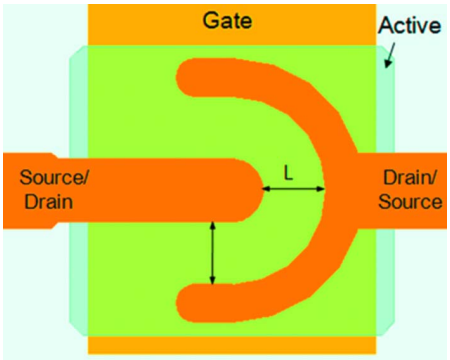

FIG. 8. (Color online) Schematic top view of circular shape electrode *a*-Si:H TFT.

(>10 V), while the OFF current remains the same for both cases. The subthreshold swing is small for both cases, while the threshold voltage and field-effect mobility show a small difference for each case.

We also found that the fork *a*-Si:H TFT might not be an adequate device as a switching or driving TFT for AM-OLEDs due to the relatively lower ON-current level in spite of a large size in comparison to the normal TFT. However, at the same time, thanks to its stable bidirectional OFF current as well as a very low gate-to-pixel capacitance, the fork *a*-Si:H TFT is a good candidate as a switching TFT for AM-LCDs.

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[1]R. F. Pierret, *Semiconductor Device Fundamentals* (Addison-Wesley, New York, 1996).
[2]E. E. Hollis, *Design of VLSI Gate Array ICs* (Prentice-Hall, NJ, 1987).
[3]W. H. Wolf, *Modern VLSI Design*, 2nd ed. (Prentice-Hall, NJ, 1998).
[4]R. Schmechel, A. Hepp, H. Heil, M. Ahles, W. Weise, and H. V. Seggern, Proc. SPIE **5217**, 101 (2003).
[5]R. F. Bianchi, R. K. Onmori, and R. M. Faria, J. Polym. Sci., Part B: Polym. Phys. **43**, 74 (2005).
[6]N. Matsuki, Y. Abiko, K. Miyazaki, M. Kobayashi, H. Fujioka, and H. Koinuma, Semicond. Sci. Technol. **19**, 61 (2004).
[7]H. Wakai, N. Yamamura, S. Sato, and M. Kanbara, U.S. Patent No. 5,055,899 (8 October 1991).
[8]J. Lee, J. Huh, and D. Kim, U.S. Patent No. 6,274,884 (14 August 2001).
[9]D. Pribat, Mater. Sci. Forum **455-456**, 56 (2004).
[10]E. F. Girczyc and A. R. Boothroyd, IEEE J. Solid-State Circuits **18**, 778 (1983).
[11]C. R. Kagan and P. Andry, *Thin-Film Transistors* (Marcel Dekker, New York, 2003).
[12]Y. P. Tsividis, *Operation and Modeling of the MOS Transistor* (McGraw-Hill, New York, 1987).
[13]Y. Kaneko, Y. Tanaka, N. Kabuto, and T. Tsukada, IEEE Trans. Electron Devices **36**, 2949 (1989).
[14]S. Saito and K. Kitamura, SID Int. Symp. Digest Tech. Papers **26**, 257 (1995).
[15]H. Lee, J. S. Yoo, C. D. Kim, I. J. Chung, and J. Kanicki, IEEE Trans. Electron Devices **54**, 654 (2007).

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