

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.,
Patent Owner.

IPR2025-01479

U.S. Patent No. 11,574,991

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,574,991**

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EXHIBIT LIST

No.	Exhibit
1001	U.S. Patent No. 11,574,991 (“’991 Patent” or “’991Pat.”)
1002	File History of the ’991 patent (“’991FH”)
1003	Declaration of Jerzy Kanicki, Ph.D.
1004	Curriculum Vitae of Jerzy Kanicki, Ph.D.
1005	U.S. Pat. Pub. No. 2012/0313100 (“Liu”)
1006	U.S. Pat. Pub. No. 2003/0089905 (“Udagawa”)
1007	Japanese Pat. Pub. No. 2003-167533 (“Nakayama”)
1008	U.S. Pat. Pub. No. 2008/0150846 (“Chung”)
1009	U.S. Pat. Pub. No. 2012/0001893 (“Jeong”)
1010	U.S. Pat. Pub. No. 2012/0199854 (“Noguchi-I”)
1011	Japanese Pat. Pub. No. 2008-008942 (“Murade”)
1012	U.S. Pat. Pub. No. 2012/0127220 (“Noguchi-II”)
1013	U.S. Pat. No. 7,626,199 (“Kim”)
1014	<i>Samsung Display Co. v. BOE Technology Group Co.</i> , No. 2:25-cv-00426-JRG (E.D. Tex.), Dkt. No. 1, Complaint
1015	Definition of “periphery”: The American Heritage Dictionary, 2d ed. (1991)
1016	Definition of “periphery”: Concise Oxford English Dictionary, 11th ed. (2009)
1017	K.C. Park, <i>Pixel Circuits for OLED Displays</i> in <i>Advanced Display Technology</i> , Series in Display Science and Technology, I. B. Kang et al. (eds.), Springer Nature Singapore Pte Ltd. 2021 (“Park”)

No.	Exhibit
1018	R. M. A. Dawson et al., <i>Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display</i> in 1998 SID Symp. Digest of Tech Papers, 1998 (“Dawson”)
1019	S. M. Choi et al., <i>A Self-Compensated Voltage Programming Pixel Structure for Active-Matrix Organic Light-Emitting Diodes</i> in Proceedings of International Display Workshops (IDW), pp. 535-538, 2003 (“Choi”)
1020	A. Bernanose, <i>Electroluminescence of Organic Compounds</i> in British Journal of Applied Physics 6, pp. S54-S56, 1955 (“Bernanose”)
1021	H. Kallmann et al., <i>Bulk Conductivity in Organic Crystals</i> in Nature 4718, pp. 31-33, 1960 (“Kallmann”)
1022	M. Pope, Autoionization in Anthracene in The Journal of Chemical Physics 47, 2197–2198, 1967 (“Pope”)
1023	M. Sano et al., Electroluminescence and Band Gap in Anthracene in The Journal of Chemical Physics 43, 2920–2921, 1965 (“Sano”)
1024	P.S. Vincett et al., <i>Electrical Conduction and Low Voltage Blue Electroluminescence in Vacuum-Deposited Organic Films</i> in Thin Solid Films 94, 171-183, 1982 (“Vincett”)
1025	C.W. Tang and S.A. VanSlyke, <i>Organic Electroluminescent Diodes</i> in Applied Physics Letters 51, 913-915, 1987 (“Tang”)
1026	J.H. Burroughes et al., <i>Light-Emitting Diodes Based on Conjugated Polymers</i> in Nature 347, 539-541, 1990 (“Burroughes”)
1027	M.A. Baldo et al., <i>Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices</i> in Nature 395, 151-154, 1998 (“Baldo”)
1028	U.S. Pat. Pub. No. 2003/0129790 (“Yamazaki”)

No.	Exhibit
1029	Min et al., <i>Electrical Characteristics of New LDD Poly-Si TFT Structure Tolerant to Process Misalignment</i> in IEEE Electron Device Letters, 20(7), 1999 (“Min”)
1030	Lee et al., <i>Asymmetric Electrical Properties of Fork a-Si:H Thin-Film Transistor and Its Application to Flat Panel Displays</i> in Journal of Applied Physics, 105, 2009 (“Lee-2009”)
1031	Kim et al., <i>40 Inch FHD AM-OLED Display with IR Drop Compensation Pixel Circuit</i> in 2009 SID Symp. Digest of Tech Papers, 2009 (“Kim-2009”)
1032	Lee et al., <i>A Novel LTPS TFT Pixel Circuit for Compensating IR Drop of Large Area AMOLED Display</i> in The Electrochemical Society (ECS) Transactions, 50(8), pp. 269-275, 2012 (“Lee-2012”)
1033	N. H. E. Weste et al., <i>CMOS VLSI Design: A Circuits and Systems Perspective</i> , Fourth Edition, Addison-Wesley, 2011 (“Weste”)
1034	U.S. Pat. Pub. No. 2003/0141811 (“Park ’811”)
1035	U.S. Pat. No. 9,461,102 (“Ono”)
1036	U.S. Pat. Pub. No. 2012/0211750 (“Kakinuma”)
1037	U.S. Pat. Pub. No. 2006/0256502 (“Li”)

LISTING OF CHALLENGED CLAIMS

11,574,991
Claim 1
1[pre] An organic light emitting diode display comprising:
1[a] a non-conductive substrate;
1[b] a plurality of first voltage lines;
1[c] a plurality of scan lines;
1[d] a plurality of data lines;
1[e] a plurality of driving circuits formed on the substrate;
1[f] a plurality of organic light emitting diodes, wherein each of the plurality of organic light emitting diodes is electrically coupled to a respective one of the plurality of driving circuits;
1[g] wherein each of the driving circuits comprises: a first thin film transistor implemented in a first portion of a semiconductor layer disposed on the substrate, and coupled to one of the plurality of scan lines and to one of the plurality of data lines;
1[h-1] a second thin film transistor implemented in a second portion of the semiconductor layer, wherein the semiconductor layer couples the second thin film transistor to the first thin film transistor, and
1[h-2] wherein the second portion of the semiconductor layer has at least one bent portion;
1[i] a storage capacitor comprising: a first capacitor plate that is configured to operate as a gate electrode of the second thin film transistor;
1[j] a second capacitor plate electrically coupled to one of the plurality of first voltage lines and overlapping the first capacitor plate; and

1[k] an insulating layer between the first capacitor plate and the second capacitor plate;
1[l] a third thin film transistor implemented in a third portion of the semiconductor layer, wherein the semiconductor layer couples the third thin film transistor to the first thin film transistor and to the second thin film transistor, and wherein the third thin film transistor is electrically coupled to one of the plurality of first voltage lines through the semiconductor layer; and
1[m] a fourth thin film transistor implemented in a fourth portion of the semiconductor layer, wherein the semiconductor layer couples the fourth thin film transistor to the second thin film transistor, and wherein the fourth thin film transistor is electrically coupled to the respective organic light emitting diode through the semiconductor layer; and
1[n] wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate.
Claim 2
2. An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.
Claim 3
3[a] An organic light emitting diode display according to claim 2, further comprising: a plurality of second voltage lines;
3[b] a fifth thin film transistor electrically coupled to the first capacitor plate; and
3[c] a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,
3[d] wherein the sixth thin film transistor is coupled to the fifth thin film transistor.
Claim 4
4. An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

Claim 5
5. An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.
Claim 6
6. An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.
Claim 7
7. An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor.
Claim 8
8 An organic light emitting diode display according to claim 4, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.
Claim 9
9. An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.
Claim 10
10[a] An organic light emitting diode display according to claim 2, further comprising: a plurality of second voltage lines;

10[b] a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and
10[c] a sixth thin film transistor implemented in a sixth portion of the semiconductor layer,
10[d] wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and
10[e] wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.
Claim 11
11. An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.
Claim 12
12. An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.
Claim 13
13. An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.
Claim 14
14[pre] An organic light emitting diode display according to claim 11, further comprising a seventh thin film transistor implemented in the sixth portion of the semiconductor layer,
14[a] wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

14[b] wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.
Claim 15
15[pre] An organic light emitting diode display according to claim 11, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.
Claim 16
16. An organic light emitting diode display according to claim 1, wherein a periphery of the first capacitor plate completely surrounds a periphery of the second capacitor plate in a plan view.
Claim 17
17[pre] An organic light emitting diode display according to claim 1, further comprising:
17[a] a plurality of second voltage lines;
17[b] a fifth thin film transistor electrically coupled to the first capacitor plate; and
17[c] a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,
17[d] wherein the sixth thin film transistor is coupled to the fifth thin film transistor.
Claim 18
18. An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.
Claim 19

19. An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.
Claim 20
20. An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.
Claim 21
21. An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor.
Claim 22
22[pre] An organic light emitting diode display according to claim 18, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.
Claim 23
23[pre] An organic light emitting diode display according to claim 1, further comprising:
23[a] a plurality of second voltage lines;
23[b] a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and
23[c] a sixth thin film transistor implemented in a sixth portion of the semiconductor layer, wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and wherein the sixth thin film

transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.
Claim 24
24. An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.
Claim 25
25. An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.
Claim 26
26. An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.
Claim 27
27[pre] An organic light emitting diode display according to claim 24, further comprising a seventh thin film transistor implemented in the sixth portion of the semiconductor layer,
27[a] wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and
27[b] wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.
Claim 28
28[pre] An organic light emitting diode display according to claim 24, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

Claim 29

29. An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.

Claim 30

30. An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

Petitioner requests *inter partes review* (“IPR”) of claims 1-30 (“Challenged Claims”) of U.S. Patent No. 11,574,991 and has shown a reasonable likelihood of prevailing as to each Challenged Claim.

I. GROUNDS FOR STANDING

The ’991 Patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR. EX1014.

II. IDENTIFICATION OF CHALLENGE

A. Prior Art

Petitioner relies on Exhibits listed in the Table of Exhibits and declaration of Dr. Jerzy Kanicki (EX1003, “Kanicki”). Specific invalidity grounds are listed in the table below, where Liu is prior art under pre-AIA 35 U.S.C. §102(e), and the remaining references are prior art under pre-AIA 35 U.S.C. §102(b).

Ground (35 U.S.C. §103)	Claims	References
1A	1-6, 8-13, 15-20, 22-26, 28-30	Liu, Udagawa
1B	2-6, 10-13	Liu, Udagawa, Nakayama
1C	7, 14, 21, 27	Liu, Udagawa, Chung
1D	7, 14	Liu, Udagawa, Chung, Nakayama
1E	9, 29-30	Liu, Udagawa, Murade
2A	1-6, 17-20	Noguchi-I, Udagawa

2B	10-13, 23-26	Noguchi-I, Udagawa, Kim
2C	7, 21	Noguchi-I, Udagawa, Noguchi-II, Jeong
2D	14, 27	Noguchi-I, Udagawa, Noguchi-II, Jeong, Kim

III. THE '991 PATENT

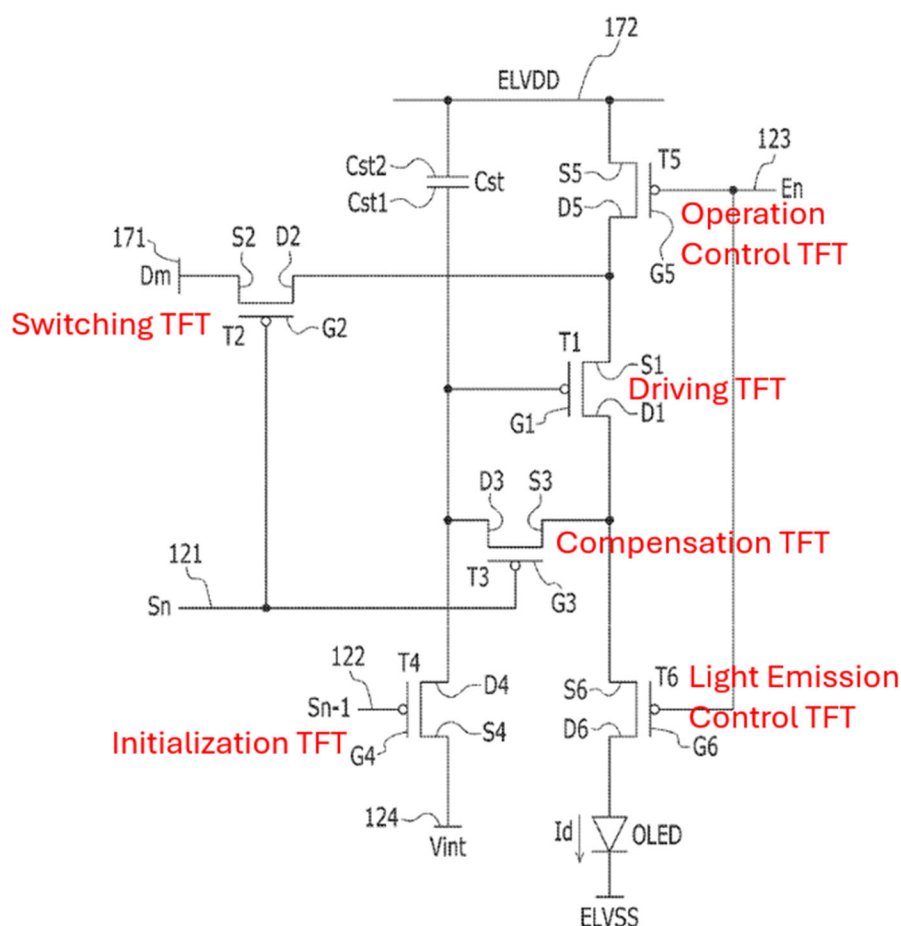
A. Overview

The '991 Patent describes an organic light emitting diode (OLED) display, including a plurality of pixels, signal lines (121-124, 171-172), six thin-film transistors (TFTs T1-T6), a storage capacitor (Cst), and an OLED connected to T6.¹ '991Pat., 1:45-46, 6:12-19, FIG. 1 (showing one pixel circuit). The '991 Patent describes achieving a relatively large number of gray levels by forming the channel region of the driving TFT to include a plurality of bent portions. *Id.* 2:3-6, 4:48-53.

One pixel circuit is shown in Figure 1 (annotated below), with Figures 2 and 3 showing specific layout (or plan) views of the pixels, and Figure 4 and 5 showing cross-sectional views taken along different cut lines of Figure 3. *Id.*, 6:9-14, 8:37-51.

¹ OLED displays utilizing TFTs and capacitors are not new. Kanicki, ¶¶58-96; EX1017-1032.

FIG. 1



T1-T6 are formed along semiconductor layer 131 (Figure 3 below). *Id.*, 9:4-10. The driving semiconductor (T1) channel 131a includes bent portions 33, resulting in a broader driving range of T1. *Id.*, 9:28-47. This enables gray levels to be more finely and precisely controlled by adjusting the gate voltage magnitude, to increase the resolution and thus image quality of the display. *Id.*, 9:49-62. Figure 6, e.g., shows the driving semiconductor layer 131a being “S” shaped. *Id.*, 10:5-6.

FIG. 3

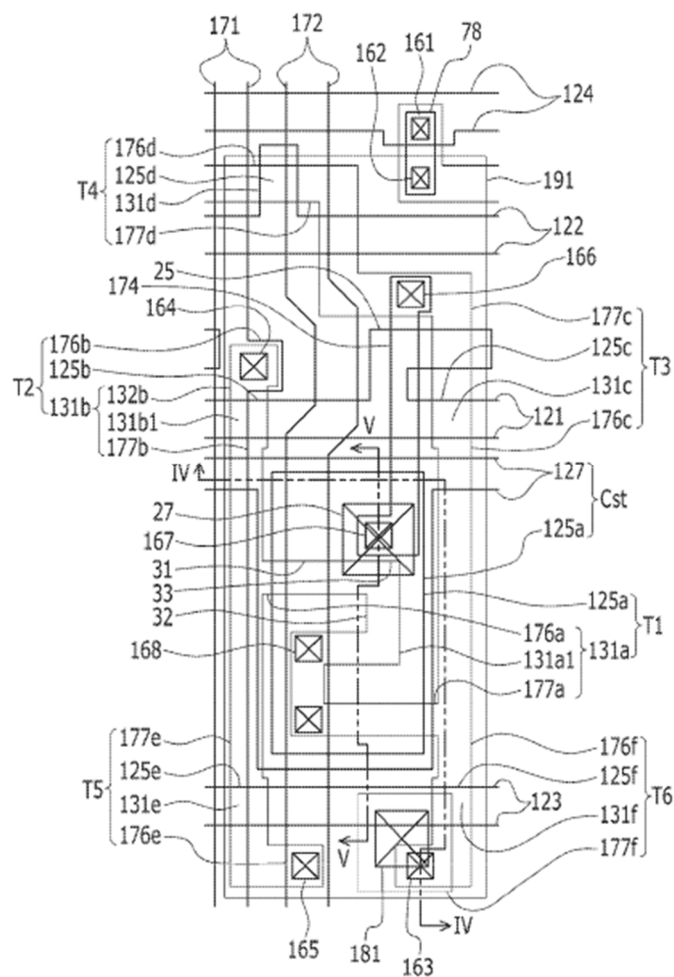
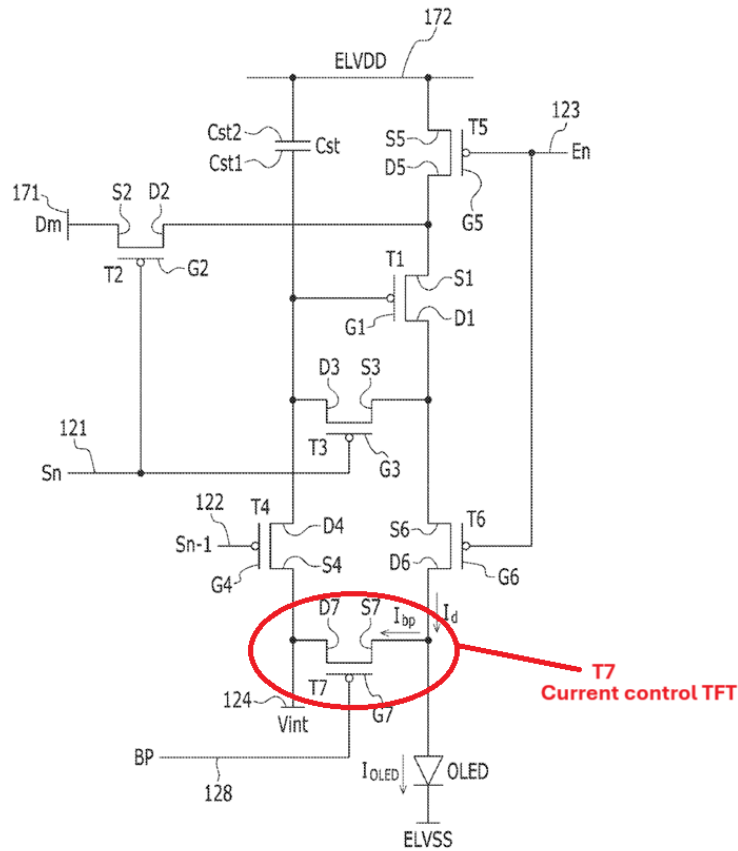


Figure 10, annotated below, describes incorporating an additional bypass T7 into the circuit. T7 disperses, or diverts, a portion of the T1 current away from the OLED to obtain an improved contrast ratio. *Id.*, 19:59-65, 20:17-19.

See Kanicki, ¶¶44-52.

FIG. 10



B. Prosecution History

The '991 Patent claims priority to Korean Patent Application No. 10-2012-0084976 filed on August 2, 2012.²

In a Non-Final Office Action Examiner objected to the claims and issued a nonstatutory double patenting rejection. '991FH, 124-130.

² August 2, 2012, is assumed to be the priority date for the purposes of this Petition only.

After filing a Terminal Disclaimer, the claims were allowed, “because the prior art of record cannot anticipate or render obvious...wherein the second portion of the semiconductor layer has at least one bent portion, and wherein the bent portion of the second portion layer is under the first capacitor plate.” ’991FH, 66-72.

Liu, used in this petition, was cited in an Information Disclosure Statement (IDS) (*Id.*, 227) but was not used as a basis for claim rejections or otherwise discussed during the prosecution. Liu’s use in this Petition is not cumulative over the prior examination at least because Liu is used in combination with other references, and the Examiner lacked expert testimony regarding the use of Liu in Petition’s combinations.

See Kanicki, ¶¶53.

C. Level of Ordinary Skill in the Art

For the purposes of this petition, a person of ordinary skill in the art (“POSITA”) in August 2012 would have had a bachelor’s degree in electrical engineering, physics, materials science or engineering, or a related field and at least four years of experience with design or development of OLED displays, including pixel layout, or the equivalent. Additional education could substitute for industry experience and vice versa. Kanicki, ¶¶10-26.

D. Claim Construction

No express constructions are necessary to assess whether the prior art reads on the challenged claims. The claims should be given their plain and ordinary meaning. Kanicki, ¶97.

IV. SPECIFIC GROUNDS

A. Ground 1A: Claims 1-6, 8-13, 15-20, 22-26, 28-30 are Unpatentable over Liu and Udagawa

1. Liu

Liu, in the same of endeavor as the '991 Patent, discloses an OLED pixel structure comprising six TFTs, one capacitor (6T1C) and an OLED (Liu, ¶¶32, 48) and, similar to the '990 patent, aims to reduce an area occupied by components of the pixel structure. *Id.*, ¶7.

Liu's pixel structure is disposed on substrate 100, comprising a semiconductor layer PO, insulating layers (102, 104, 106), conductive layers (M1, M2, M3), and a pixel electrode PE. *Id.*, ¶32. The semiconductor layer PO comprises channel, source, and drain regions of the six TFTs (denoted T1-T6). *Id.*, ¶34.

See Kanicki, ¶¶100-103.

2. Udagawa

Udagawa discloses lengthening the channel of a TFT in an OLED circuit to be longer than that of a channel of a conventional TFT. Udagawa, ¶23. This lowers

the dispersion in TFT's electric current value and enables the TFT to be turned on at a higher gate voltage. Udagawa, ¶¶19-23.

Udagawa is in the same field of endeavor as the '991 Patent because both are directed to display devices using a plurality of TFTs in each pixel to drive a current through an OLED. Udagawa, ¶¶8-9. Similarly, both describe using polysilicon film to form TFTs, with pixels and driving circuits being formed integrally over the same substrate, thereby reducing the number of connecting terminals and reducing the periphery of the pixel portion. *Id.*, ¶10

See Kanicki, ¶¶104-106.

3. Motivation to combine

Both Liu and Udagawa described drive circuits for OLED displays and sought to improve the design and operation of OLEDs. Liu's invention focuses on a reduced-area pixel structure. Liu, ¶¶4, 10, 47, 56, 72. Udagawa describes drive circuit configurations improving OLED reliability, and consequently, its operation and image quality. Udagawa, ¶12. POSITAs would have been motivated to combine the complementary teachings of Liu with Udagawa to achieve improved operations of the OLED display.

Udagawa recognized small TFTs resulted in unwanted dispersion effects, which was a main reason for display irregularities. Udagawa, ¶38. POSITAs would

have been motivated to reduce the dispersion in Liu's TFT drive circuits so that the pixels in the high-resolution display provided a more uniform brightness.

POSITAs would have been motivated to use Udagawa's driving TFT with serpentine channel in Liu's OLED driving circuit because this combination would have conformed to Liu's objectives of reducing the size of the pixel structure; forming the gate channel in this way would allow for both a reduction of dispersion and maintaining a reduced size of the TFT while enabling an improved operation of the driving TFT.

POSITAs would have been motivated to apply Udagawa's known technique of reducing dispersion (using TFT with a longer channel) to a known device ready for improvement (Liu's OLED circuit) to yield predictable results (reducing dispersion). POSITAs would have had a reasonable expectation of success because elongating the channel length to reduce dispersion was well-known by 2012, as evidenced by Udagawa and other known prior art references, and such modifications were well within the skillset of POSITAs.

See Kanicki, ¶¶107-112 (citing EX1028-EX1030).

4. Claim 1

a. 1[pre]

Liu discloses a "pixel structure" in a display, using TFTs, a capacitor, and an organic light emitting diode ("OLED"). Liu, ¶¶3, 6, 48, 58, FIGs. 1, 6. The "pixel

structure is applied to an organic electroluminescence display and has a...6T1C” structure, but it is not limited to the disclosed structure.³ *Id.*, ¶¶32, 48, 50, 53, 58, 73, 75.

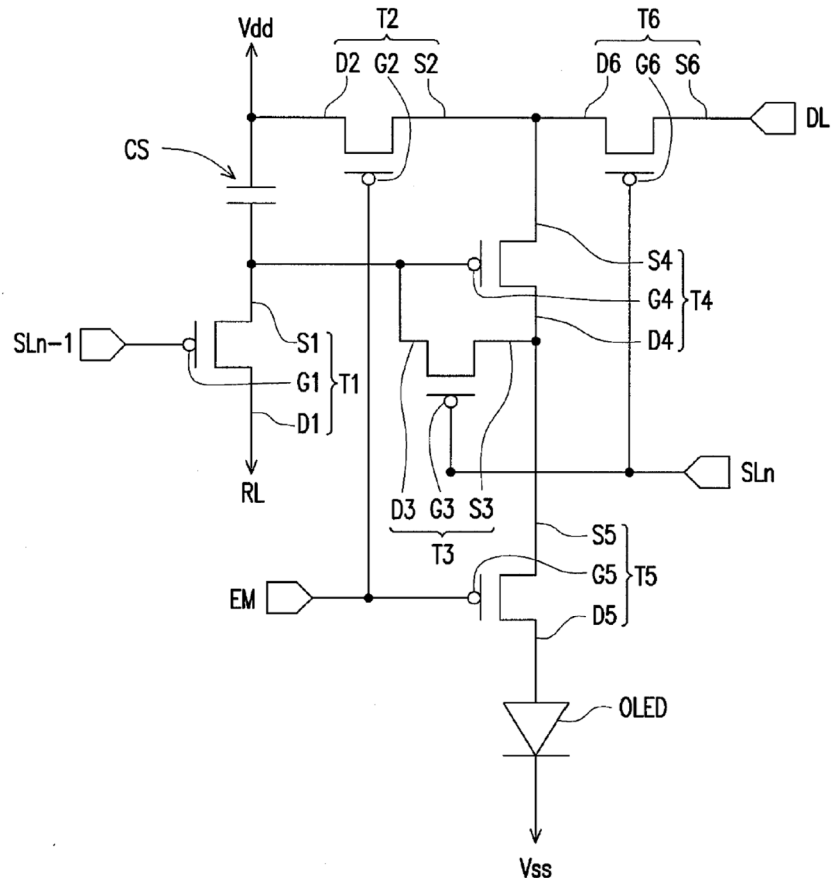


FIG. 1

Liu is directed to reducing the area occupied by the pixel structure for use in high resolution displays. *Id.*, ¶¶6-7. As explained below, Petitioner maps the embodiment shown in Figures 1-6 to the claims.

³ All emphases are added unless otherwise noted.

See Kanicki, ¶¶113-116.

b. 1[a]

Liu discloses “the pixel structure is disposed on a **substrate 100**.” Liu, ¶32, FIG. 5 (annotated below). Furthermore, substrates may be made of glass, quartz, polymers, or ceramics, among other materials, which are known non-conductive materials. *Id.*, ¶33; Kanicki, ¶¶117-118.

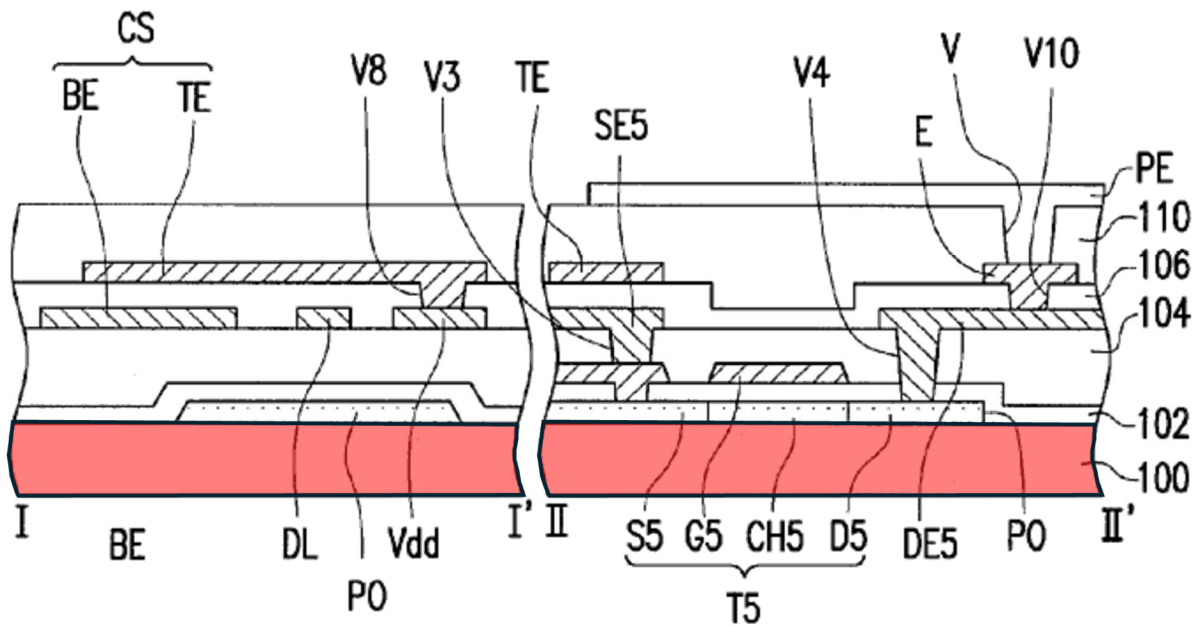


FIG. 5

c. 1[b]-1[d]

Plurality of Pixel Structures

Liu discloses a pixel structure in an OLED display. §IV.A.4.a. Each pixel structure would be considered a pixel. *Id.*; Liu, ¶50. For example, Udagawa explains pixels comprise the TFT driving circuits and OLEDs. Udagawa, ¶¶5-8.

POSITAs would have understood that high resolution displays contain a plurality of pixel structures, and the resolution is measured according to the number of pixels occupying the display area. Liu, ¶¶6-7;.

As explained below, POSITAs would have understood that Liu's pixel structures include "a plurality of" voltage lines, scan lines, and data lines to be supplied to them..

Plurality of First Voltage Lines (1[b]), Scan Lines (1[c]), and Data Lines (1[d])

The "first voltage line" is "power line Vdd" in the second metal layer M2. Liu, ¶42, FIG. 1 (annotated below). POSITAs would have understood Vdd is a "voltage line" because Vdd is common notation to denote a voltage. Moreover, the '991 Patent uses the same notation, Vdd, to identify a "voltage line." '991Pat., 6:25-37.

Liu discloses scan lines (SL_n and SL_{n-1}) in the TFT circuit and references them with the nomenclature "n" and "n-1" signifying a plurality thereof, not limited to the two shown in the circuit. Liu, ¶38; Table, *infra*. Each pixel structure further includes a data line, DL. Liu, ¶42; Table, *infra*.

Annotated Figure 1 of Liu (left) is shown alongside '991 Patent Figure 1 (right) illustrating similarities between the circuits and Vdd, scan lines, data lines. *Id.*, ¶31.

FIG. 1

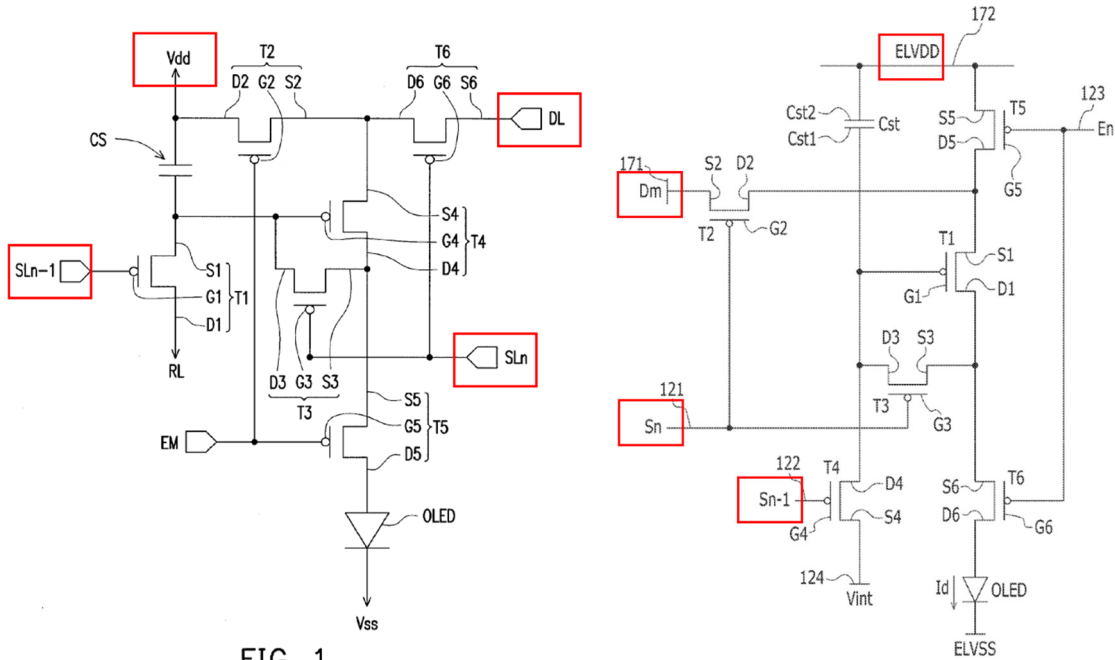


FIG. 1

Additionally, Petitioner cross-references each transistor and signal line of the '991 Patent to similar elements of Liu below.

See Kanicki, ¶¶119-131.

Claims	'991	Liu
1 st TFT	T2	T6
2 nd TFT	T1	T4
3 rd TFT	T5	T2
4 th TFT	T6	T5
5 th TFT	T3	T3
6 th TFT	T4	T1
Capacitor	Cst	CS
First Capacitor Plate	125h	BE
Second Capacitor Plate	127	TE
1 st Voltage line	ELVDD	Vdd
2 nd Voltage line	Vint	RL

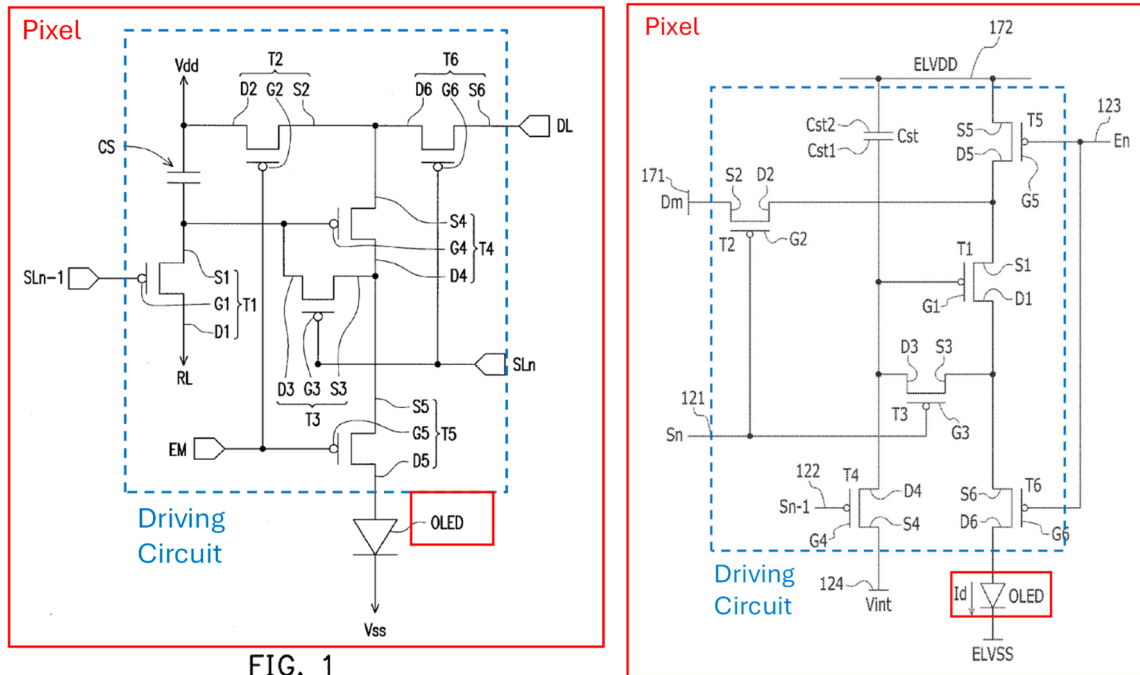
OLED	OLED	OLED
1 st Scan line	Sn	SLn
2 nd Scan line	Sn-1	SLn-1
Light emission control line	En	EM
Data line	Dm	DL

d. 1[e]-1[f]

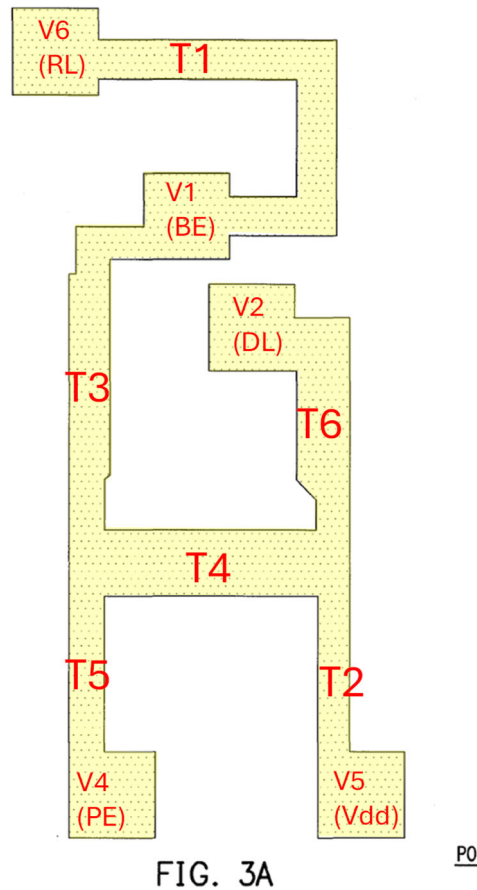
Liu teaches or suggests multiple pixel structures (i.e., pixels) in a display (§IV.A.4.c), where each driving circuit comprises a plurality of TFTs to drive the OLED for that pixel. Liu, ¶¶6, 8, FIG. 1.

Annotated Figure 1 of Liu alongside '991 Patent Figure 1 illustrate the relationship of pixels and driving circuits. *Id.*, ¶31, FIG. 1.

FIG. 1



The semiconductor layer includes TFTs on the substrate (“a plurality of driving circuits formed on the substrate”) and annotated in Figure 3A. *Id.*, ¶¶8, 15, 33-35, FIG. 3A; §IV.A.4.b. POSITAs would have understood that the plurality of Liu’s driving circuits would have been formed on a single substrate because it was common practice at the time to use a single substrate backplane or wafer form to form multiple pixels.

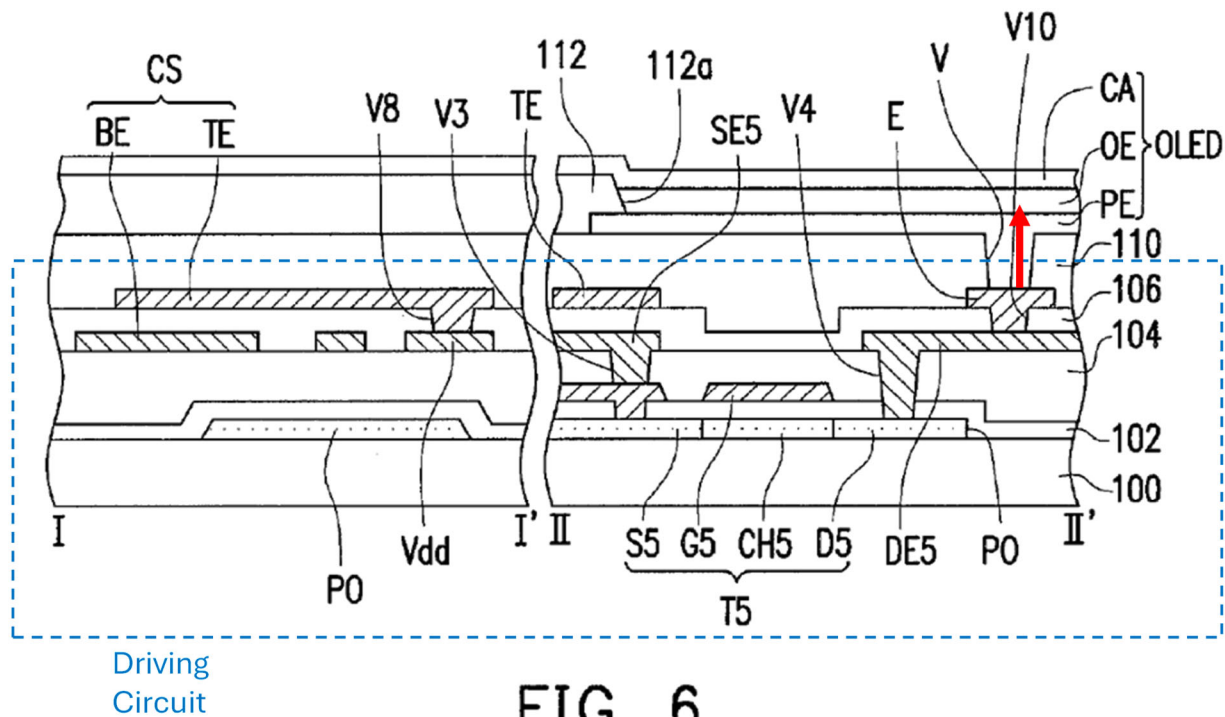


Annotated Figure 6 below shows the OLED directly connects to T5 through “E” and V (“each of the plurality of organic light emitting diodes is electrically

coupled to a respective one of the plurality of driving circuits”). Liu, ¶¶44-48, FIG.

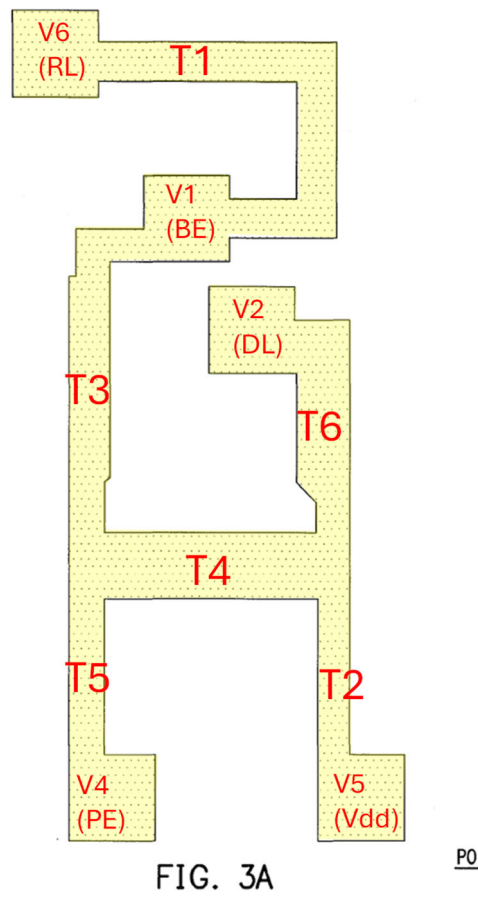
6.

See Kanicki, ¶¶132-137.



e. 1[g]

The “first thin film transistor” is T6 coupled to “the first scan line,” SL_n, and “a data line,” DL, as shown in Liu’s Figure 1. Liu, ¶¶38, 42; §IV.A.4.d. As explained above in 1[e], each TFT in the driving circuit is formed in a portion of the semiconductor layer on the substrate (“implemented in a first portion of a semiconductor layer disposed on the substrate”). *Id.*; Liu, ¶¶34-35 (“the...region predetermined for forming...transistor T6”); see FIG 3A (annotated below).



The data line “is electrically connected to the source region S6” of T6, and scan line SLn is connected to the gate G6 of T6. *Id.*, ¶38, FIG. 1 (annotated).

See Kanicki, ¶¶138-142.

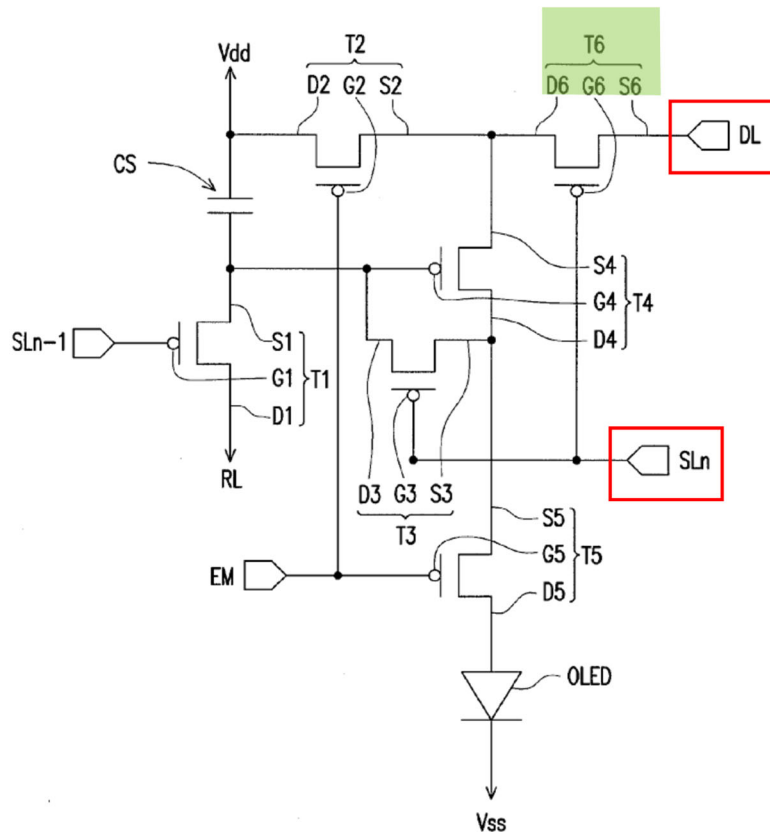
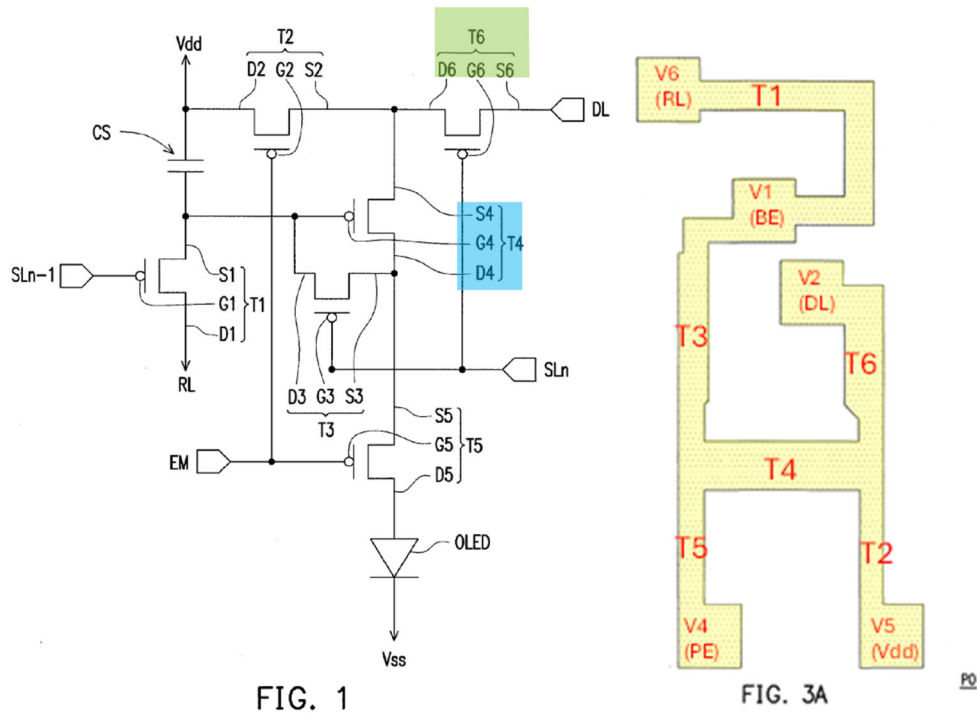


FIG. 1

f. 1[h-1]

The “second thin film transistor” is T4 formed in a portion of the semiconductor layer (“implemented in a second portion of the semiconductor layer”). §IV.A.4.d; Liu, ¶35 (“the...region predetermined for forming...transistor T6. T4 is formed in a different portion in the semiconductor layer and adjacent to T6 Figure 1 (left) and 3A (right). Because the semiconductor layer is continuous from T4 to T6, a POSITA would have understood “the semiconductor layer couples” T4 to T6..

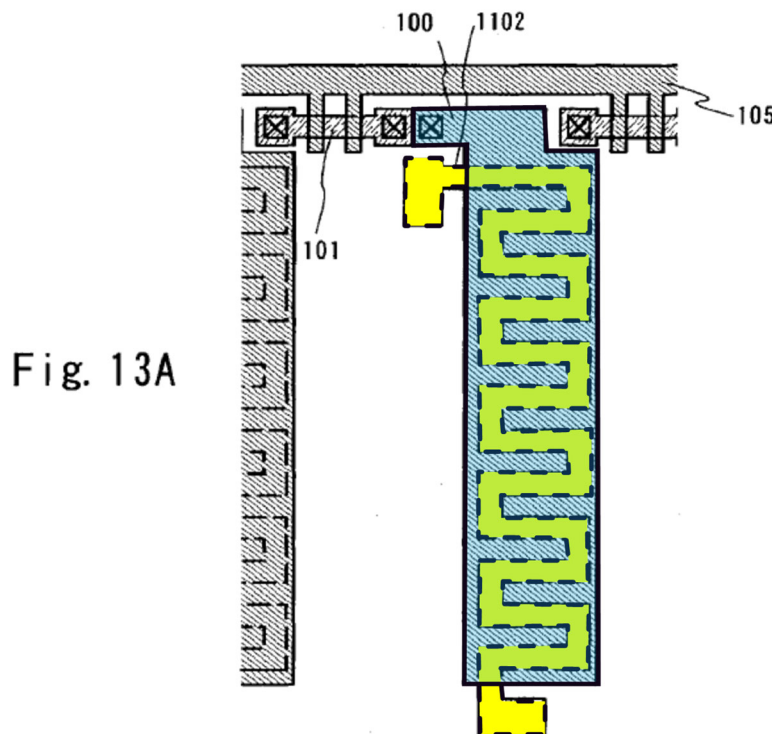
See Kanicki, ¶¶143-144.



g. 1[h-2]

While Liu does not expressly disclose a “bent” channel portion T4, POSITAs would have found it obvious to modify Liu to use Udagawa’s serpentine (“bent”) gate channel for drive transistor T4. Liu’s semiconductor layer is polysilicon. Liu, ¶34. It was well-known that the miniaturization of TFT circuits in polysilicon caused problems related to the electrical characteristics of the TFTs. Udagawa, ¶¶5-15. One involved an increase in dispersion between pixels because the channel length of the drive transistor decreases. *Id.*, ¶¶11-13, 16-17. Thus, POSITAs would have been motivated to look for existing solutions presented by others, such as by Udagawa, to reduce the dispersion effects of polysilicon TFTs in OLED driving circuits.

Udagawa recognized this problem and explained dispersion is reduced “[w]hen the channel length of the TFT that supplies an electric current to the OLED is made longer.” Udagawa, ¶22. Udagawa discloses various channel shapes, such as a “snake” shape, shown below. *Id.*, ¶31, FIG. 13A. Udagawa’s annotated Figure 13A shows a snake-like (i.e., bent or serpentine) channel 1102 (yellow) with gate electrode 100 (blue) covering the channel region. Udagawa, ¶¶31, 102, 154.



For reasons explained in §IV.A.3, POSITAs would have been motivated to incorporate Udagawa’s driving TFT gate shapes (thereby increasing the channel length) in Liu’s miniaturized OLED driving circuit to reduce the dispersion effects that accompany driving circuit size reduction. Furthermore, modifying Liu to use

Udagawa's longer gate channel aligns with Liu's objectives of reducing the pixel size because forming the gate channel in this way allows for both a reduction of dispersion and maintaining reduced size due to the winding nature of the extended channel while enabling an improved operation of T4.

Udagawa describes different lengths and numbers of serpentine structures can implement the extended channel. Udagawa, ¶20. Thus, POSITAs would have similarly designed Liu's T4 channel region by choosing the channel length based on a particular design's constraints. Udagawa recognizes this versatility of various channel lengths (Figures 3 and 4). Udagawa, ¶20. Thus, using Udagawa's serpentine gate channel structure would not have substantially increased Liu's pixel structure size because different lengths of the channel could be used.

Additionally/alternatively, POSITAs would have understood the serpentine channel of Udagawa can be implemented without changing the footprint of Liu's pixel structure by extending the channel area slightly above or slightly below its current position; due the serpentine nature of the channel and the ability to select the extended channel length, any additional expansion would have been readily implemented within the existing pixel footprint. Moreover, POSITAs would have been more than capable of sizing the gate electrode (BE) to cover an appropriate portion of the modified channel. *Id.*; §**Error! Reference source not found.**

See Kanicki, ¶¶145-151.

h. 1[i]

The “storage capacitor” is capacitor CS connected to the gate electrode of T4, including bottom electrode, BE, (“first capacitor plate”) and top electrode, TE (“second capacitor plate”). See Liu, ¶¶42, 44-45, 47, 53, FIGs. 1, 2, 3C, 3D, 4-6.

CS “can be disposed overlapping with the semiconductor layer PO, so as to reduce an area occupied by components of the pixel structure.” *Id.*, ¶47. Liu further discloses capacitor CS is connected to the gate of T4 (“configured to operate as a gate electrode of the second thin film transistor”). Liu, FIG. 1 (annotated red line).

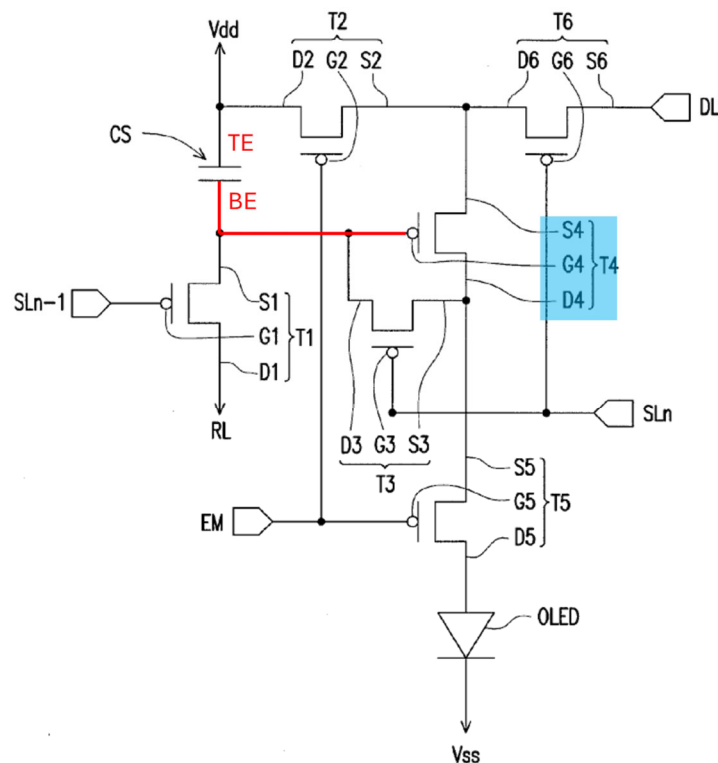


FIG. 1

bottom electrode BE on M2 through via V3. Liu, ¶¶41, 54, FIGs. 2, 3B, 3C, 3D.

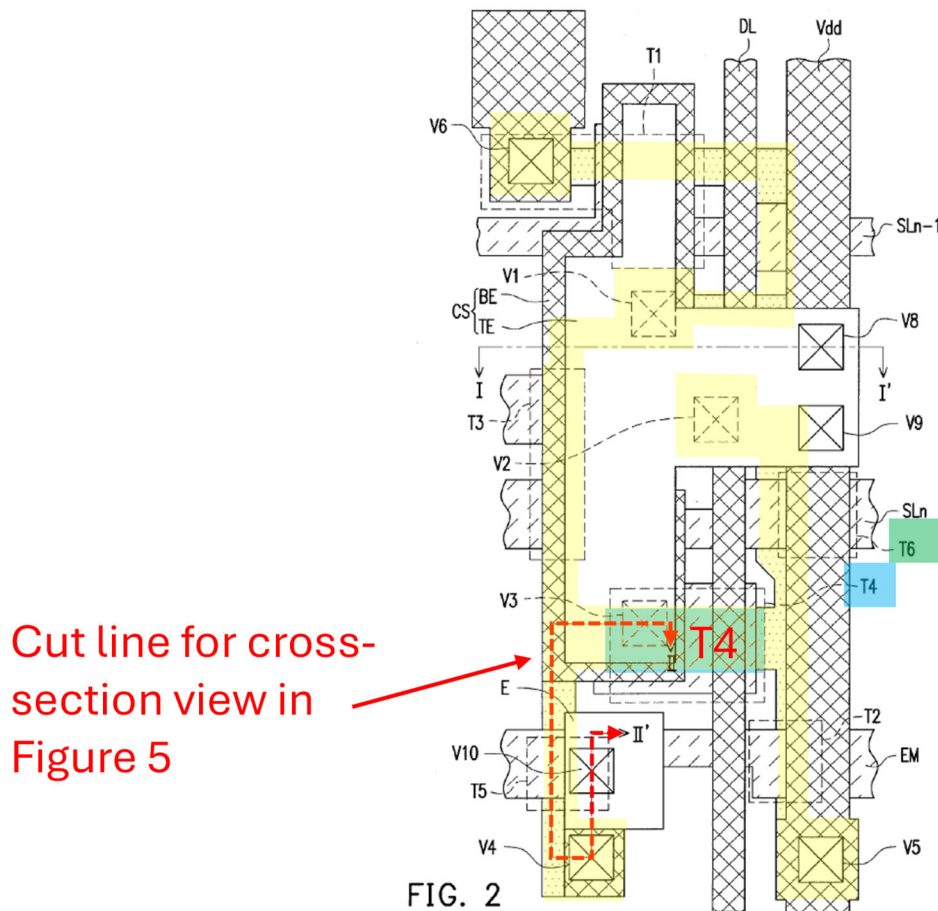


⁴ Liu uses abbreviations M1 and M2 to denote the first conductive layer and the second conductive layer, respectively; these layers provide electrical conductivity and are made of metal materials. *See* Liu, ¶¶32, 37, 40. A “via” or a “contact via” is a metal structure that connects one metal component to another metal component in a vertical direction. *See, e.g., Id.* ¶44; Kanicki, ¶155n.4.

Regarding Figure 5, Dr. Kanicki notes that BE is labeled correctly, however, SE5 is an incorrect label and the element should be labeled as BE, and POSITAs would have understood the incorrect labeling because, although SE5 is mentioned in the specification (paragraph 40), there are no vias or metal shown in Figures 3B-4 that would denote such a structure. Furthermore, Figure 1 clearly shows that S5 is connected to D4, and as shown in Figure 3A, the connection is made in the semiconductor layer without any connections to other layers. In Figure 5, V3 is shown to be SE5, which conflicts with Figure 1 because such an equivalence would connect S5 to G4. *Id.* Regardless, the connection of BE to the gate electrode is clearly shown.

The structure labeled as “Gate of T4” above is on the M1 layer and is shown unlabeled in Figure 3B. Liu, FIG. 3B. Via V3 directly connects the gate electrode of T4 to BE above it. *Id.* V3 is further shown in Figure 3C, connecting BE to the level below (shown in Figure 3B).

POSITAs would have this understanding because the cut line II-II' in Figure 2 passes directly through T4 and is shown in Figure 5. *Id.* Figure 2, annotated to show the semiconductor layer PO (yellow), T6, T4, and the cross-section lines for Figure 5 are shown below.



If PO argues that BE is not configured to operate as the gate electrode of T4, POSITAs would have found it obvious to use BE directly as the gate electrode of T4, which is also described Liu. Liu explains various changes to the capacitor design that include adjusting the capacitor dielectric material and/or its thickness, allowing the capacitor size to be changed while maintaining a selected capacitance. Liu, ¶53. For example, by thinning the dielectric, CS's area can be reduced, placement directly over the semiconductor layer. *Id.* POSITAs would have thus found it obvious to position BE directly over the channel of T4 as taught by Liu (e.g., using the gate electrode of T4 as shown in Figure 3B); BE (or least a part thereof) would operate

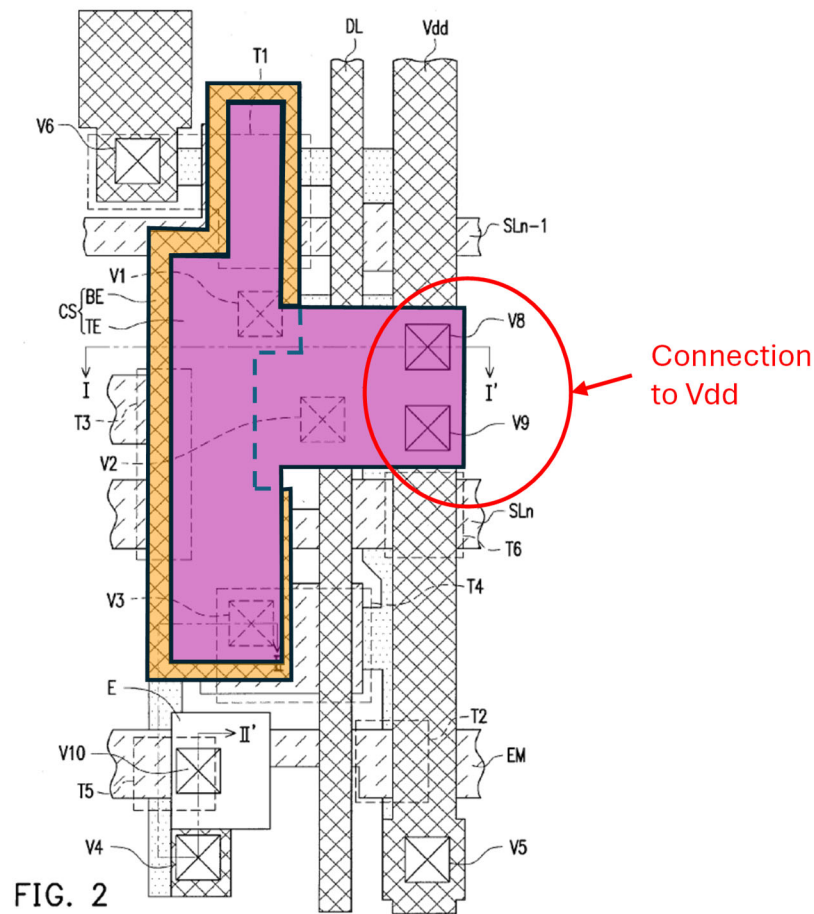
as the gate electrode of T4 with such a placement. POSITAs would have found this modification obvious because Liu expressly described it. Furthermore, POSITAs would have sized the gate electrode (e.g., BE) according to the length and width of the channel of T4.

See Kanicki, ¶¶152-160.

i. 1[j]

Annotated Figure 2 below shows **top electrode TE** in M3 overlaps **bottom electrode BE** in M2. Liu, ¶¶45, 53; §IV.A.4.h. Furthermore, “the top electrode TE is electrically connected to the power line Vdd through contact via structures V8-V9” (“electrically coupled to one of the plurality of first voltage lines”). Liu, ¶44, FIGs. 2, 3D, 5.

See Kanicki, ¶¶161-163.



j. 1[k]

Liu discloses this element: “**third insulating layer 106 between the bottom electrode TE and the bottom electrode BE.**” Liu, ¶45.

Furthermore, it would have been obvious based on the teachings in Liu to position BE directly over the semiconductor layer of T4 in M1. §IV.A.4.h; Liu, ¶32. When moving BE to M1 to be directly over the semiconductor layer, TE may not be correspondingly moved. Moving or not moving TE to M2 is a design choice dependent on factors related to layout. If TE remains in M3, insulating layers 106

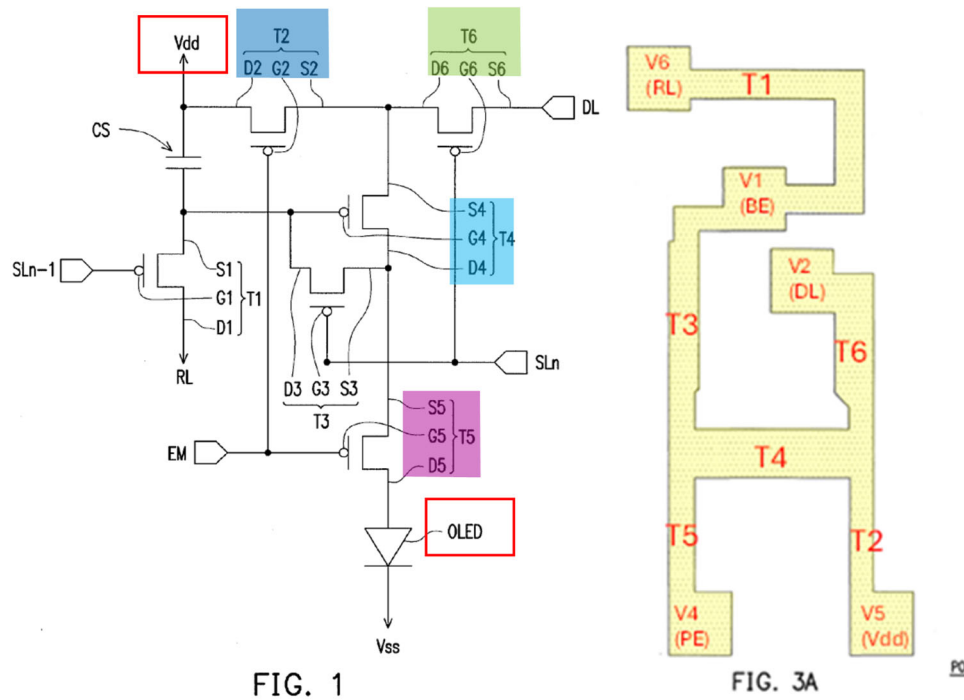
and 104 would be designed with appropriate thicknesses. However, if TE were moved to M2 (in the metal layer directly above BE), then dielectric layer 104, M1, is the “insulating layer” as claimed. These choices and their implementations were well within the capabilities of POSITAs and would have been obvious in view of the express description of Liu regarding those design choices.

See Kanicki, ¶¶164-167.

k. 1[l]-1[m]

Liu discloses a TFT driving circuit with at least six transistors and one capacitor. §§IV.A.4.a (1[pre]), IV.A.4.e (1[g]). As shown in annotated Figures 1 (left) and 3A (right), and partially produced Table from 1[b], Liu discloses each of the recited transistors and connections. §IV.A.4.c.

Claims	'991	Liu
1 st TFT	T2	T6
2 nd TFT	T1	T4
3 rd TFT	T5	T2
4 th TFT	T6	T5
5 th TFT	T3	T3
6 th TFT	T4	T1
Capacitor	Cst	CS



111: T2 (“third” TFT) is formed in a portion of the semiconductor layer on the substrate (“implemented in a third portion of the semiconductor layer”). Liu, ¶35 (“the...region predetermined for forming...transistor T2”).

T2 connects to Vdd (“electrically coupled to one of the plurality of first voltage lines”), and to T6 and T4 (“the third thin film transistor [coupled] to the first thin film transistor and to the second thin film transistor”). Liu, FIG. 1.

T2 connects to Vdd (“one of the plurality of first voltage lines”) through via V5 at the semiconductor layer. *Id.*, FIGs. 2, 3A (annotated), 3C.

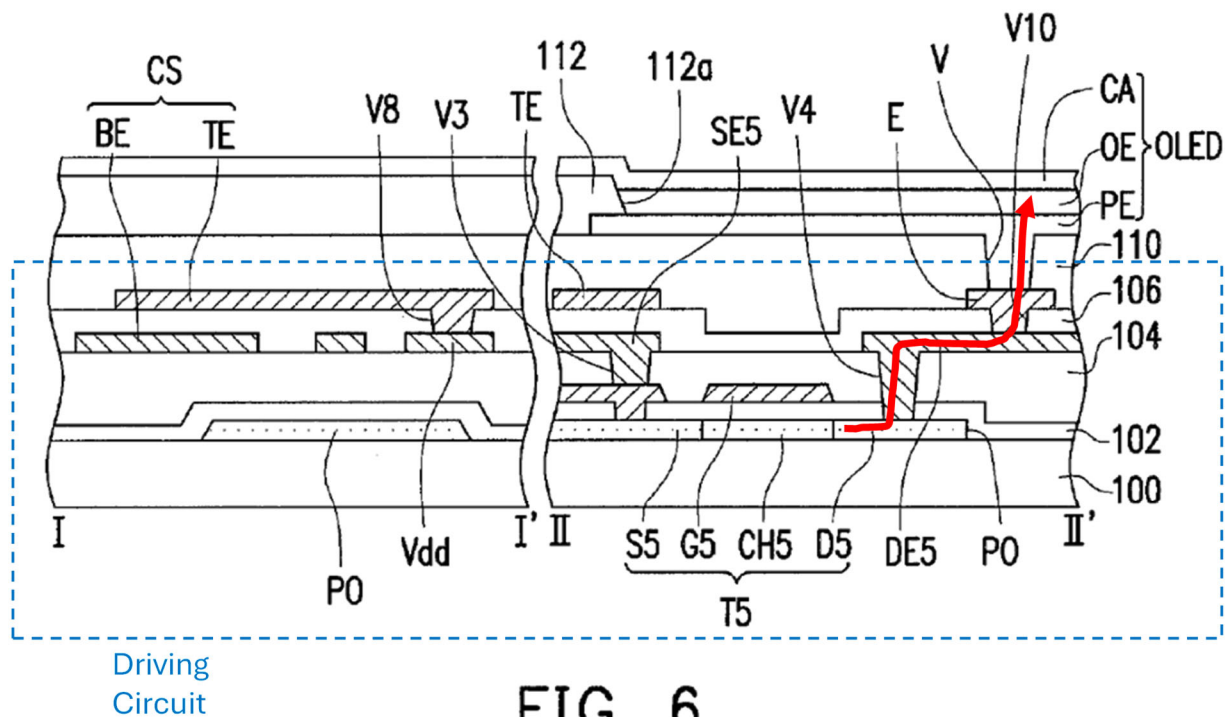
T2 is further connected to and adjacent to T4 and T6 in the semiconductor layer (“the semiconductor layer couples”). Liu, ¶35, FIG. 3A (annotated).

1[m]: T5 (“fourth” TFT) is formed in a portion of the semiconductor layer on the substrate (“implemented in a fourth portion of the semiconductor layer”). Liu, ¶35 (“the...region predetermined for forming...transistor T5”).

T5 connects to T4 (“the fourth thin film transistor [coupled] to the second thin film transistor”), and to OLED (shown in annotated Figure 6 below) (“fourth thin film transistor is electrically coupled to the respective organic light emitting diode”). *Id.*, ¶46, FIGs. 1, 2, 5.

T4 is further connected to T5 in the semiconductor layer. Liu, ¶35, FIG. 3A (annotated).

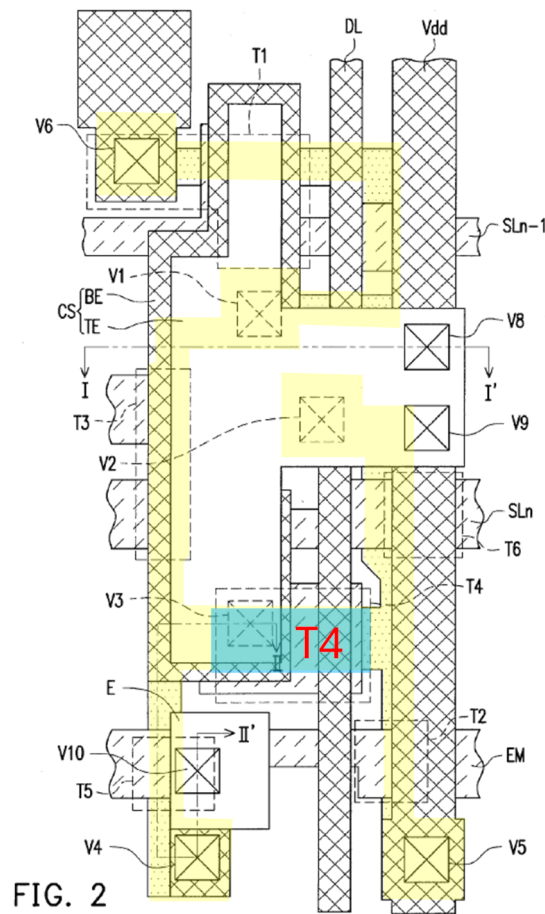
See Kanicki, ¶¶168-173.



I. 1[n]

BE is either directly connected to the gate electrode of T4 in M1 or can be reduced in size and placed directly over the semiconductor layer of T4 in M1. §IV.A.4.h (1[i]). In either scenario, BE is above T4. *Id.*; Liu, ¶¶47, 53, FIG 2. Figure 2 below has been annotated to show Figure 3A superimposed under it. The channel region of T4 is directly under BE (gate electrode) (shown in blue below) (“the [bent] portion of the second portion of the semiconductor layer is under the first capacitor plate”). Liu, FIG. 2 (annotated). This is a common structure in semiconductor engineering. While, in the combination, BE does not necessarily need to be adjusted in size to accommodate the addition of the serpentine structure as taught by Udagawa, POSITAs would have found the adjustment an obvious and a routine task to ensure that the modified channel area is under BE.

See Kanicki, ¶¶174-176.

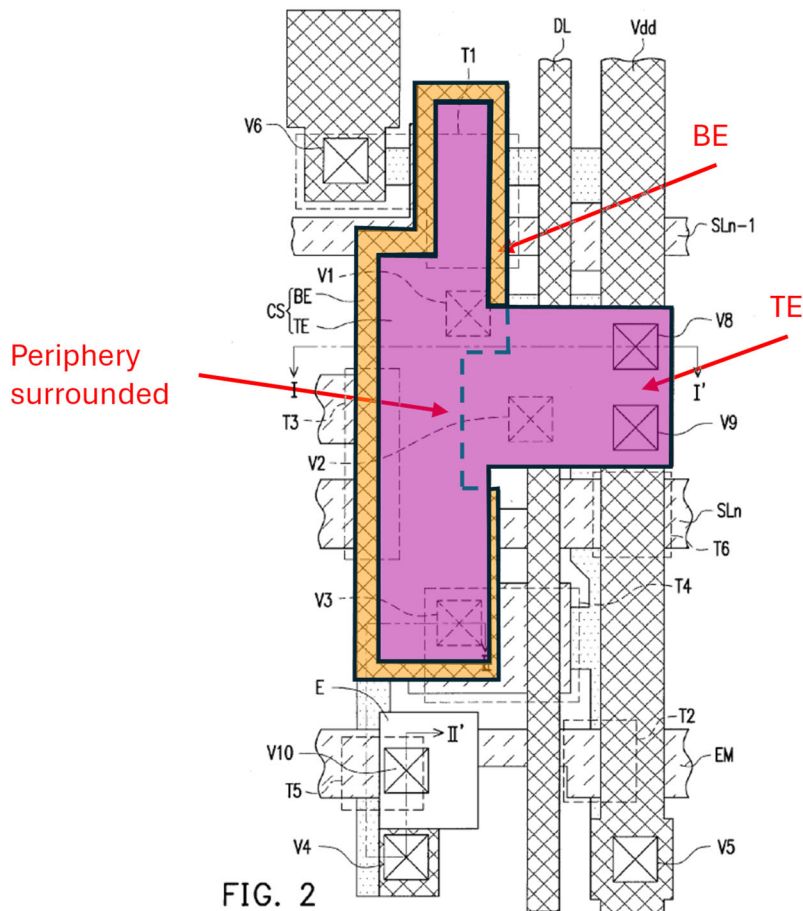


5. Claim 2

TE surrounds a portion of BE (as shown in annotated Figure 2 below); the dashed line represents “a” periphery of the BE (orange), which is surrounded by TE (purple). Based on the plain and ordinary meaning of “surround[ing] a periphery,” POSITAs would have understood that at least a portion around the outside of BE

would be surrounded by TE.⁵ *Id.*; EX1015, 923 (“the outermost part or region within a precise boundary”); EX1016, 1066 (“the outer limits or edge of an area or object”).

See Kanicki, ¶¶177-179.



Liu, FIG. 2 (annotated).

⁵ Claim 2 does not recite “entire periphery” or “entire surface area” to be surrounded; also ‘991 patent’s detailed description neither explains nor attaches any particular significance to a periphery. Kanicki, ¶178n.5.

6. Claim 3

a. 3[a]

The “second voltage line” is reference signal line “RL” . Liu, ¶38, FIG. 1 (annotated below). POSITAs would have understood the reference signal line, RL, is a “voltage line” because “signal line” is common terminology for circuit components transmitting voltages; plus, Liu’s Figure 1 uses the same circuit symbol for voltage lines Vss, Vdd, and RL. Liu’s Annotated Figure 1 (left) is shown alongside ’991 Patent Figure 1 (right) illustrating RL and Vint. Because Liu describes each of the plurality of pixel structures includes the line RL, a POSITA would have understood that Liu discloses a “plurality” of reference signal lines (“second voltage lines”). §IV.A.4.c.

See Kanicki, ¶¶180-182.

FIG. 1

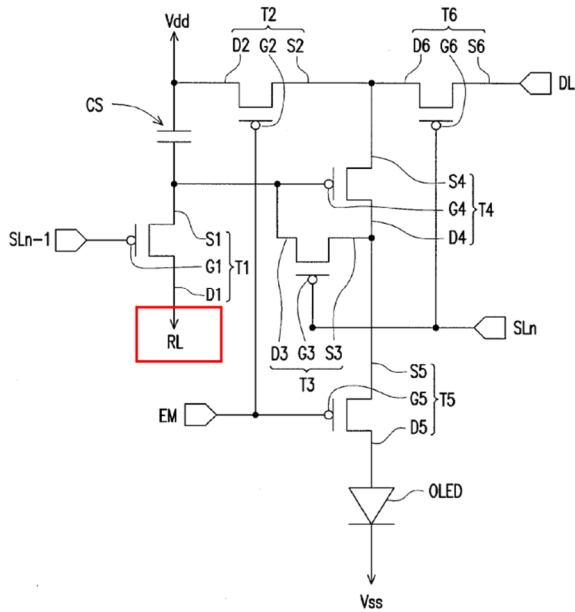
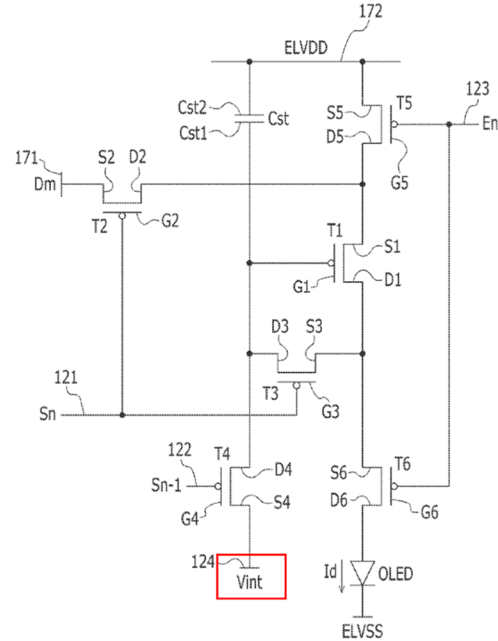


FIG. 1



b. 3[b]-3[d]

3[b]: Liu's T3 ("fifth" TFT) connects to T4 and BE ("first capacitor plate").

Liu, FIG 1.

3[c] and 3[d]: Liu's T1 ("sixth" TFT) connects to RL ("voltage line"), T3 ("fifth" TFT), and BE ("first capacitor plate"). Liu, FIG 1. As shown in annotated Figure 1, Liu discloses the TFTs and electrical connections in claim 3. Liu, FIG. 1.

See Kanicki, ¶¶183-187.

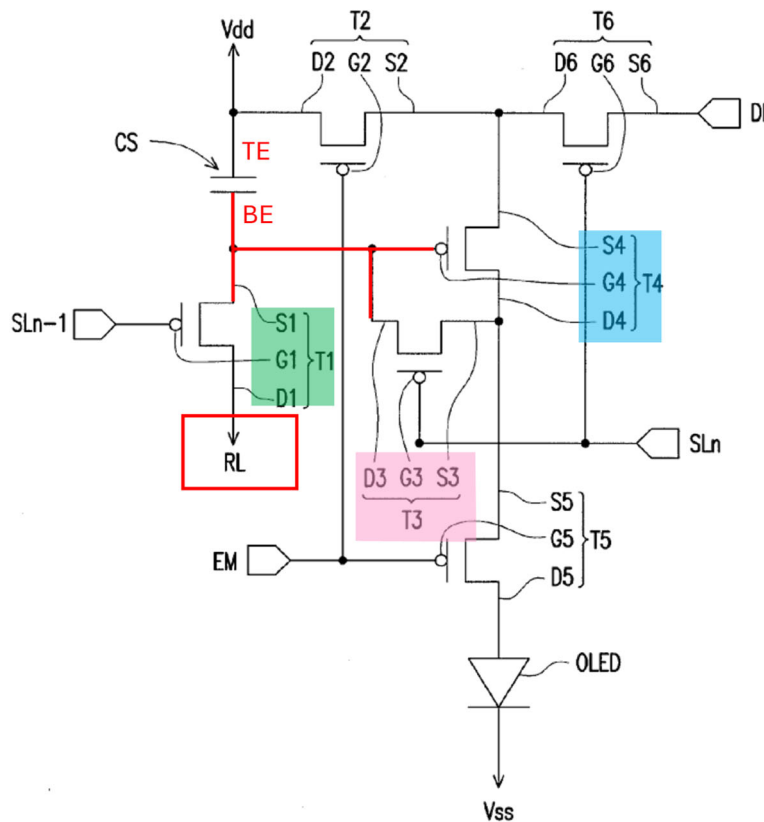


FIG. 1

7. Claims 4-5

BE can be (a) reduced in size and placed directly over the semiconductor layer in M1, or (b) is directly connected to the gate electrode of T4 on M1. §IV.A.4.h (1[i]). In (a), BE is in M1 and directly the gate electrode of T4; in (b), BE directly connects to the gate electrode of T4 through connector V3, as shown in Liu's Figure 6.

Claim 4: In scenario (a), that BE is located in M1 along with scan lines SLn and SLn-1. Liu, ¶38.

Claim 5: In either scenario (a) or (b), the material of M1 is used for BE and the scan lines—SL_n and SL_{n-1}. POSITAs would have found it obvious that the material in the via (V3) connecting BE to gate electrode of T4 (in M1) would be the metal material as the BE and the gate electrode of T4 in order to bond well and make a good connection. Furthermore, all of conductive layers, M1, M2 and M3, can be made of “made of metal materials” (Liu, ¶37), and thus it would have been obvious that the capacitor plate BE, connector V3, gate electrode of T4, and scan lines (all metal conductive components) would be made of the same metal material.

See Kanicki, ¶¶188-192.

8. Claim 6

Liu’s (“fifth” TFT) T3 connects to SL_n. Liu, FIG 1 (annotated below).

T1 (“sixth” TFT) connects to SL_{n-1}. *Id.*

See Kanicki, ¶¶193-195.

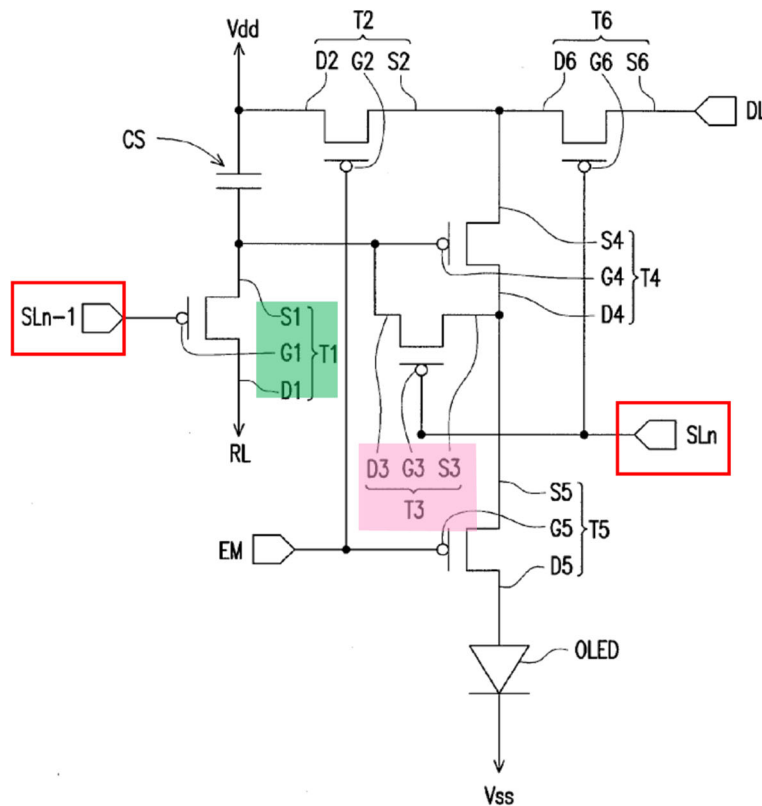


FIG. 1

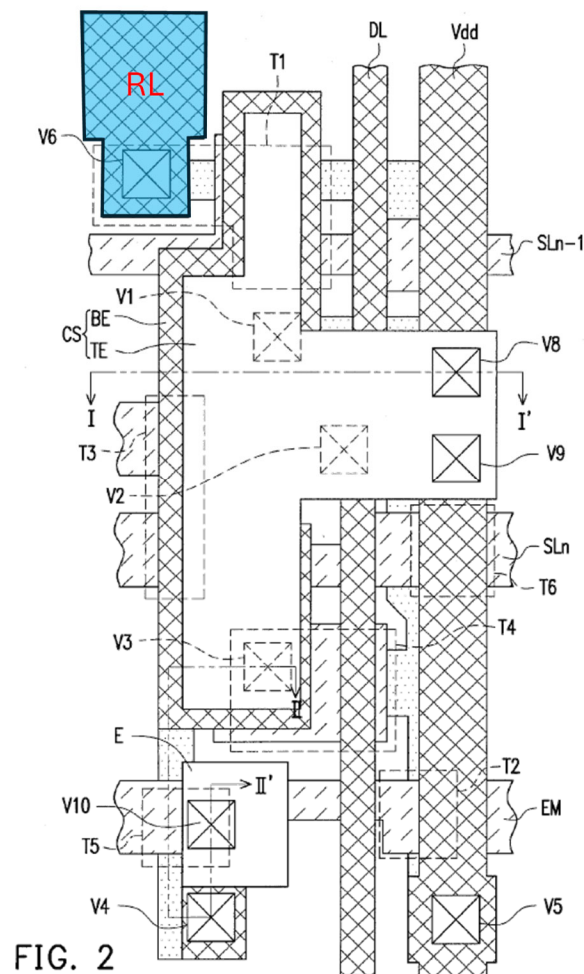
9. Claim 8

BE (and/or the gate electrode of T4) and the scan lines are in the same metal layer M1 (“first metal layer”)⁶. §IV.A.7 (claim 4). Furthermore, data lines (DL) and

⁶ A POSITA would have understood designators “first,” “second,” and “third” as used in claim 8 to modify a “metal layer” were merely for convenience and used to distinguish the claimed layers from each other. *Free Motion Fitness, Inc. v. Cybex Int'l, Inc.*, 423 F.3d 1343, 1348 (Fed. Cir. 2005).

Vdd are in the same metal layer M2 (“third metal layer”). Liu, ¶42. And TE is in metal layer M3 (“second metal layer”).

Furthermore, RL **may** be in metal layer M1 (Liu, ¶38) or M2 as shown in Figure 2 (i.e., in the same metal layer as DL and Vdd). Kanicki, ¶198 (explaining T1 is connected to BE through V1 on one side and to an unlabeled metal line (RL) through V6 on the other). RL is shown in annotated Figure 2 below.



POSITAs would have found it obvious to place RL in any of M1, M2, or M3 at least because Liu’s schematic layout does not place any other conductive

structures overlapping RL. Such a modification amounted to a simple design choice involving the routine task of making layout minor changes and was well within the skillset of POSITAs. *Id.* As modified, RL placed in M3 (“second metal layer”) would be in the same metal layer as TE. This is shown as Option A below.

	Claim 8	Liu’s Teachings	Proposed modification – Option A: TE not moved	Proposed modification Options B: TE moved down
Scan lines	1 st ML	M1	M1 (None)	M1 (None)
First voltage line (Vdd)	3 rd ML	M2	M2 (None)	M3 (Move)
Second voltage line (RL)	2 nd ML	M1, M2 (or M3)	Pick M3	M2 (None)
Data line (DL)	3 rd ML	M2	M2 (None)	M3 (Move)
First capacitor plate (BE)	1 st ML	M2 or M1	M1 (None)	M1 (None)
Second capacitor plate (TE)	2 nd ML	M3	M3 (None)	M2 (Move) ⁷

The above table illustrates claim 8’s requirements, the teachings of Liu, and the proposed modifications based on two different options for BE and TE placement.

⁷ As explained in 1[k], moving TE to M2 would have been obvious to a POSITA.

Kanicki, ¶200n.6

Liu's original configuration shown in Figures 2-4 can be modified to place BE directly on the semiconductor layer. §IV.A.4.j (1[k]). Furthermore, POSITAs would have found it obvious that the top capacitor plate can remain in place (Option A) or be moved to layer M2 below (Option B). §IV.A.4.j. The above table describes the changes (if any) a POSITA would have made in the two options.

In Option A, the choice would have simply been to pick M3 for placement of RL, as already suggested by Liu. In Option B, the modifications would have primarily included moving Vdd and DL to M3. A POSITA would have found this move obvious to avoid interference with TE. Such a modification amounted to a simple design choice that involved a routine task of making minor changes to the semiconductor pattern and was well within the skill set of a POSITA.

Placement of the elements as recited in claim 8 would have been obvious because (1) the '991 patent does not provide any significance, benefit or advantage gained by the specific placement of the element in a specific metal layer, (2) their position in one of three metal layers would have amounted to selecting one of limited number of alternative positions, and (3) Vdd and DL could only be placed in either M2 or M3 in Liu's design because placing them in M1 was not possible because they would have then formed a gate signal to any semiconductor layer below.

Accordingly, in Option B, it would have been obvious that TE and RL would be in M2 and Vdd and DL would be in M3,⁸ as explained above.

See Kanicki, ¶¶196-203.

10. Claim 9

BE operates as gate electrode of T4 and is over the semiconductor layer. §IV.A.4.i (1[i]). In this configuration, BE is located in M1 directly above the semiconductor layer. *Id.*; As explained, the top capacitor electrode (TE) can be moved down to layer M2 (Option B). §§IV.A.4.j, IV.A.9. Thus, TE would be directly over BE.

Liu's annotated Figure 1 (left) shows drain D3 of Liu's T3 and source S1 of T1 must still be connected to BE. In the configuration where BE is located in its original location in M2, D3 and S1 (in the semiconductor layer) are connected to BE through via "V1," as evident from annotated Figure 3A (right). Liu, ¶¶41-42, FIGs. 1, 2, 3A, 3C.

⁸ *See* footnote 6.

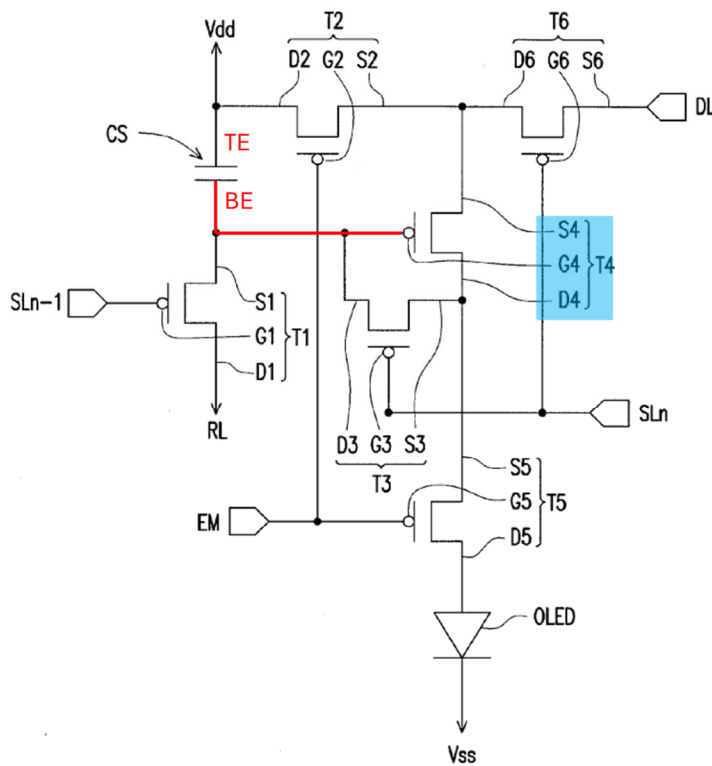


FIG. 1

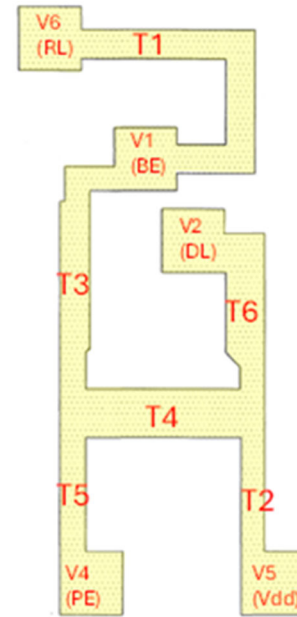


FIG. 3A

However, in the alternate embodiment of Liu where BE is moved down to M1 and TE is also moved down to M2 (see Option B in 1[k]), metal layer M2 is no longer available to make the D3-to-S1-to-BE connection. §IV.A.4.j. POSITAs would have found it obvious to extend via “V1” up to metal layer M3 and come back down to M1 at the appropriate location in order to make the connection to BE. This modification would have been obvious because when TE is moved from M3 to M2, M3 becomes available without any obstructions, and it would have provided a simple and easy way to enable routing the connection line to any circuit component. Thus, a connection from V1 on M3 to BE would be made. *Id.*

With the connection line on M3, POSITAs would have recognized that TE would prevent making a direct connection from M3 to BE because TE is directly above BE. In order to conserve space and reduce the size of the pixel structure according to Liu's teachings (Liu, ¶7), POSITAs would have found it obvious to use a via from M3 to M1, in order to connect the metal line on M3 (that connects to V1) to BE. Furthermore, to prevent shorting BE to TE, a POSITA would have found it obvious to use a "keep-out" in TE around the via "V3" from M3 to M1. Kanicki, ¶208 (discussing EX1037). A keep-out is an area in the layout where no metal is allowed to be placed, which is a well-known method to prevent shorting of metal traces in layout design. *Id.*; *see, e.g.*, EX1037, ¶¶45, 54, 65, 71-71, FIGs. 5, 8, 11, 13.

Liu itself suggests such wiring modifications based on changes to CS. In Liu's second embodiment (Figures 8-9D), CS is modified to have three electrodes (semiconductor layer, M1, and M2). Because of the modification, Liu teaches extending V1 to M3 and a signal line "L" in M3 to connect D3-to-S1-to-BE and the gate electrode of T4 through V3. Liu, ¶¶69-70, FIGs. 8, 9D; *see also* FIGs. 9A-9C. Annotated Figure 8 below shows the modified wiring of V1, M3, and V3.

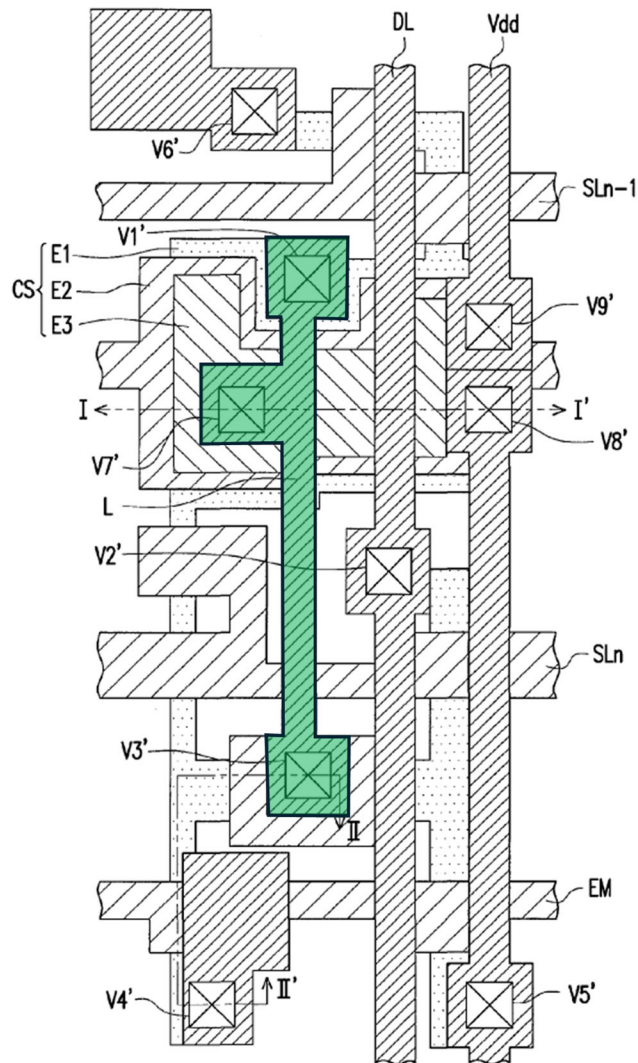
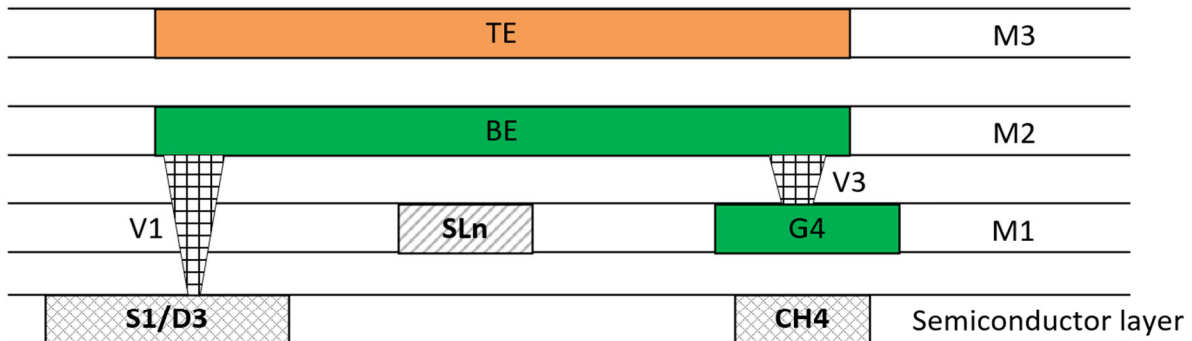
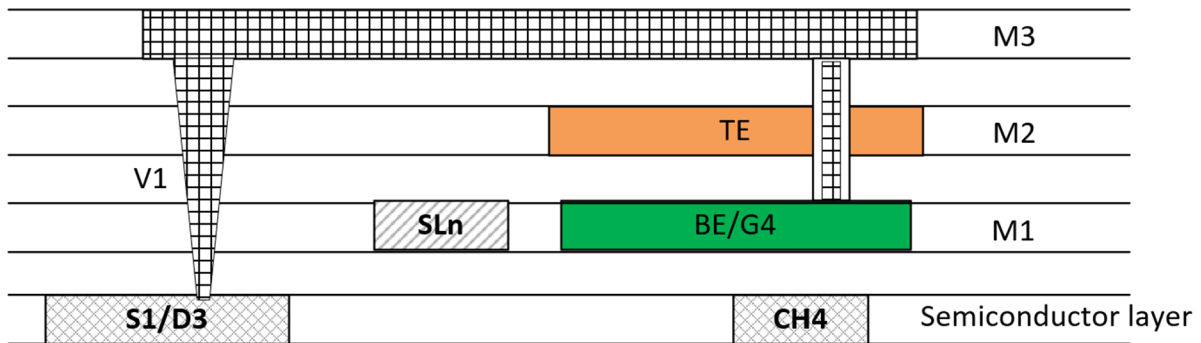


FIG. 8

To assist with visualizing the obvious modifications as described herein, Petitioner has prepared the below illustrative figures. The top figure shows the original configuration of Liu (Option A), whereas the second figure shows Liu's alternate configuration (Option B), as explained in 1[i].



Liu's original configuration (Option A)



Liu's alternate configuration (Option B)

When BE is moved down, the connection from S1/D3 to BE cannot be made through M2. POSITAs would have found it obvious to modify Liu's layout based on design choices necessitated by moving TE to M2, such that T1 and T3 are connected to BE through metal layer M3 ("electrically coupled to the first capacitor plate") by using a via through a keep-out region of TE ("through a contact hole that passes through the second capacitor plate").

See Kanicki, ¶¶204-214.

11. Claim 10

a. 10[a]

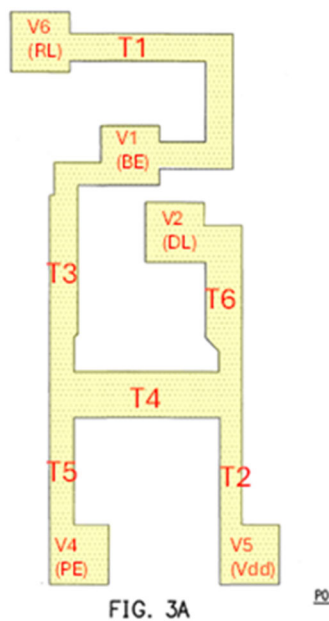
See discussion in 3[a]. §IV.A.6.a.; Kanicki, ¶215.

b. 10[b]

Liu's T3 ("fifth" TFT) is formed in a portion of the semiconductor layer on the substrate ("implemented in a fifth portion of the semiconductor layer"). Liu, ¶35.

T3 and T4 ("second" TFT) are adjacent (annotated Figure 3A) in the contiguous semiconductor layer ("the semiconductor layer couples the fifth thin film transistor to the second thin film transistor").

See Kanicki, ¶¶216-219.



Liu, FIG. 3A (annotated).

c. 10[c]-10[d]

T1 (“sixth” TFT) is formed in a portion of the semiconductor layer on the substrate (“implemented in a sixth portion of the semiconductor layer”). Liu, ¶35.

T1 and T3 (“fifth” TFT) (annotated Figure 3A) are adjacent in the contiguous semiconductor layer, coupling the two together.

See Kanicki, ¶¶220-224.

d. 10[e]

T1 is connected to RL (“voltage line”) and BE (“first capacitor plate”). §IV.A.6.b (3[c]). Furthermore, T1’s semiconductor layer is connected to RL through V6 and to BE through V1. §IV.A.9. Accordingly, semiconductor layer PO couples T1 to both RL and BE. Annotated Figures 1 (left) and 3A (right) show the electrical connections of T1 and the placement of vias on the semiconductor layer.

See Kanicki, ¶¶225-227.

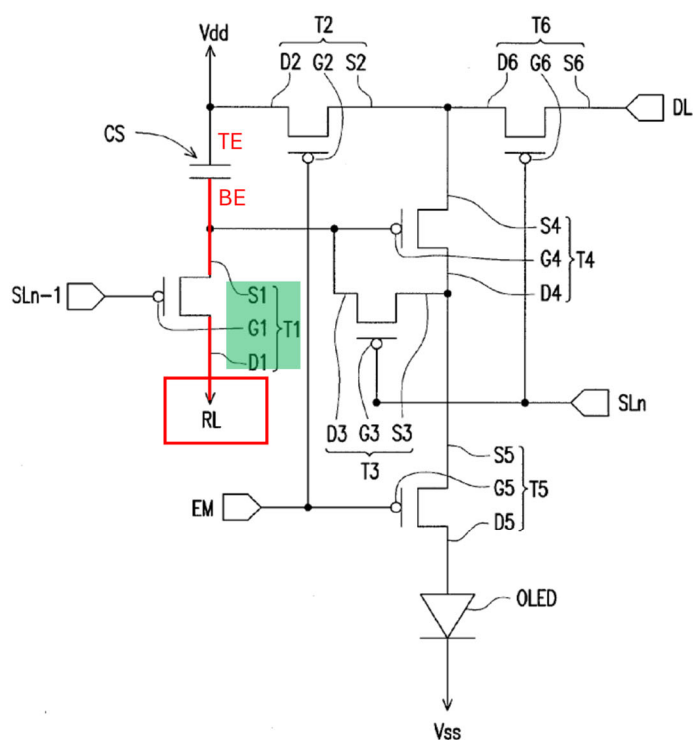


FIG. 1

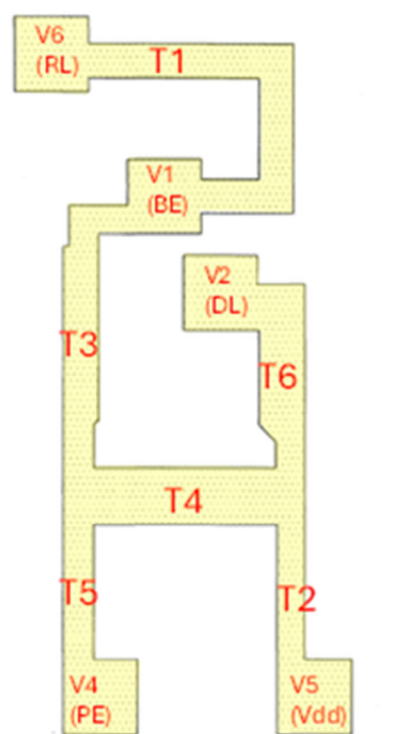


FIG. 3A

12. Claims 11-12

For claims 11 and 12, see discussion in claims 4 and 5, respectively. §IV.A.7; Kanicki, ¶228.

13. Claim 13

See discussion in claim 6. §IV.A.8; Kanicki, ¶229.

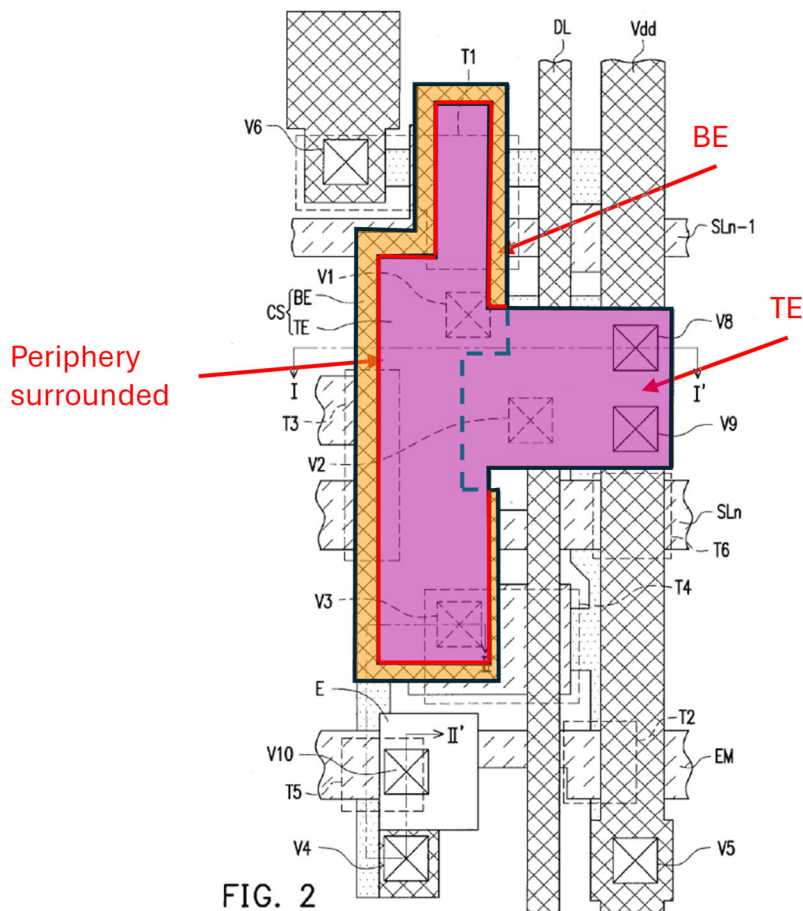
14. Claim 15

See discussion in claim 8. §IV.A.9; Kanicki, ¶230.

15. Claim 16

BE surrounds a portion of TE (Figure 2 below); the red line represents a periphery of the TE surrounded by the bottom electrode plate (orange). POSITAs would have understood that “surround[ing] a periphery” is understood as that at least a portion around the outside of BE was surrounded by TE. §IV.A.5.

See Kanicki, ¶¶231-233.



16. Claim 17

See discussion in claim 3. §IV.A.6; Kanicki, ¶234.

17. Claims 18-19

For claims 18 and 19, see discussion in claims 4 and 5, respectively. §IV.A.7; Kanicki, ¶235.

18. Claim 20

See discussion in claim 6. §IV.A.8; Kanicki, ¶236.

19. Claim 22

See discussion in claim 8. §IV.A.9; Kanicki, ¶237.

20. Claim 23

See discussion in claim 10. §IV.A.10; Kanicki, ¶238.

21. Claims 24-25

For claims 24 and 25, see discussions in claims 4 and 5, respectively. §IV.A.7; Kanicki, ¶239.

22. Claim 26

See discussion in claim 6. §IV.A.8; Kanicki, ¶240.

23. Claim 28

See discussion in claim 8. §IV.A.9; Kanicki, ¶241.

24. Claim 29

See discussion in claim 9. §IV.A.10; Kanicki, ¶242.

25. Claim 30

See discussion in claim 2. §IV.A.5; Kanicki, ¶243.

B. Ground 1B: Claims 2-6, 8, 10-13, and 15 are Unpatentable over Liu, Udagawa, and Nakayama

1. Nakayama

Nakayama describes variations in the drive currents supplied to different pixels may be caused by variations in the electrostatic capacitances of the holding and kick capacitors. *Id.*, ¶5. To suppress capacitance variation due to lateral misalignment, such as mask misalignment, Nakayama teaches the upper electrode of capacitors can be configured to have a larger surface area than the bottom electrodes thereof. *Id.*, ¶38.

Nakayama is analogous art to the '991 Patent because it is in the same field of endeavor. Both concern reducing variations in a current (or equivalently, maintaining a constant current) supplied to the driving TFT of in an OLED display. *Id.*, ¶¶4-5.

See Kanicki, ¶¶244-245.

2. Motivation to combine

As discussed above, Liu is directed to a reduced-size pixel structure. §IV.A.4.a. Nakayama is also related to OLED pixels and displays. Nakayama, ¶¶5-

6. Accordingly, POSITAs would have recognized the complementary teachings of those references and would have been motivated to combine their teachings.

Notably, Nakayama describes capacitor configurations and variances in capacitance affecting TFT driving circuits. Nakayama, ¶¶4-5. Thus, POSITAs would have been motivated to improve Liu's drive circuit operation based on the teachings of Nakayama to reduce variations of the driving TFT.

Nakayama recognized OLED displays can be improved by reducing capacitance variations (e.g., due to mask misalignment), which included configuring the upper electrode of a capacitor to have a larger surface area than the bottom electrode. Nakayama, ¶38. POSITAs would have thus found it obvious and would have been motivated to combine Liu with Nakayama, and specifically to use Nakayama's configuration of the larger upper capacitor electrode to improve Liu's OLED driving circuit. This combination would conform to Liu's objectives of reducing the size of the pixel structure. *Id.* And forming the top capacitor electrode of Liu to have a larger surface area than the bottom capacitor electrode would have mitigated capacitance variations, which would have improved the operation of the driving TFT of Liu, while maintaining a reduced size. *Id.*

Notably, POSITAs would have been motivated to apply Nakayama's known technique (shaping capacitor with a larger upper plate than lower plate as Nakayama disclosed) to a known device ready for improvement (Liu's OLED circuit) to yield

predictable results (reducing threshold voltage variation in the driving TFT). POSITAs would have had a reasonable expectation of success, because shaping the capacitor plates in an integrated circuit for an OLED display was well-known by 2012, as evidenced by Nakayama and other known prior art references, and such modifications were well within the skillset of POSITAs.

Furthermore, Liu can be combined individually with each of Udagawa and Nakayama. In each instance, the combination involves modifying a distinct aspect of Liu. POSITAs would have recognized that there is no interference among the proposed modifications. *Id.* Accordingly, POSITAs would have found it obvious and been motivated to combine Liu with each of Udagawa and Nakayama, and would have had a reasonable expectation of success.

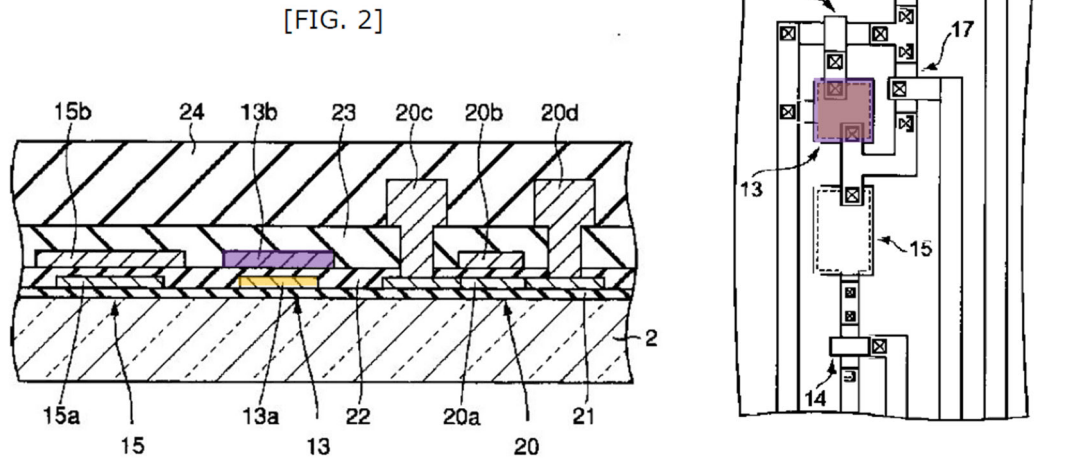
See Kanicki, ¶¶246-252.

3. Claim 2

TE surrounds a periphery of BE. §IV.A.5. If PO argues that TE does not “completely surround[] a periphery of” BE, POSITAs would have found it obvious in light of Nakayama. Nakayama discloses an upper electrode of a holding capacitor having a larger surface area than the bottom electrode. Nakayama, ¶38, FIGs. 2, 4. As shown in annotated Nakayama Figures 2 (left) and 4 (right) , the lower capacitor electrode 13a (orange) is within the perimeter of the upper electrode 13b (purple).

Nakayama, ¶¶35, 38. This configuration of capacitor electrodes suppresses the variation in the capacitance of the capacitors with respect to the deviation in the X-Y placement of the top electrode. Nakayama, ¶38.

【図4】



As explained above, BE is either directly connected to the gate electrode of T4 in M1 or can be reduced in size and placed directly over the semiconductor layer in M1. §IV.A.4.h. In the former, no other metal layer is present in metal layer 3. Liu, ¶44; FIG. 3D. Thus, there is ample room for TE to move with respect to BE without affecting the capacitance. POSITAs would have found it obvious to enlarge TE because it would have allowed for fabrication variances to maintain the capacitance

of CS, as Nakayama explains. §IV.B.2. This is possible because the capacitance is determined by the smaller of the two electrodes in the capacitor. Murade, ¶98.

For the latter, BE is directly the gate of T4 and TE may either remain in M3 or be moved to M2. §§IV.A.4.h-IV.A.4.j. TE is regardless unrestricted and a POSITA would have found it obvious to enlarge TE to realize the advantages of Nakayama. POSITAs could easily choose a dielectric and adjust the layout to accommodate TE over BE to produce the desired capacitance value. POSITAs can reason the relatively simple arrangement of signal lines and CS to achieve the arrangement disclosed in Nakayama. Any such changes to the capacitor design would have been well within POSITAs' skills and capabilities and would have amounted to routine design considerations. *Id.* (citing EX1033). Accordingly, for the reasons explained in §IV.B.2, POSITAs would have been motivated to incorporate Nakayama's capacitor plate sizing in Liu to maintain the capacitance of Liu's CS capacitor.

See Kanicki, ¶¶253-260.

4. Claim 3-6, 8, 10-13, 15

The addition of Nakayama does not change any analysis above regarding claims 2-6, 8, 10-13, and 15. §§IV.A.6-IV.A.14. Regarding claims 8 and 15, enlarging TE as explained in §IV.B.3 would not prevent RL from being moved to

M3, particularly when BE is directly over the semiconductor layer in M1 and TE is moved to M2. §§IV.A.9-IV.A.14.

See Kanicki, ¶261.

C. Ground 1C: Claims 7, 14, 21, and 27 are Unpatentable over Liu, Udagawa, and Chung

1. Chung

Chung describes an OLED display pixel circuit similar to the circuit in Figure 1 of '991 Patent (i.e., with scan lines, signal lines, a driving transistor, five switching transistors, and a storage capacitor) but additionally includes a switching transistor SW_TR6 for applying a reverse bias, i.e., a seventh transistor. Chung, ¶57.

Chung teaches in an initialization period (i.e., a non-light emission period) of operating the pixel circuit, a low-level scan signal that is applied to the initial switching transistor SW_TR 5 is also applied to the switching transistor SW_TR6 for applying a reverse bias to the OLED, thereby preventing degradation of the OLED. *Id.*, ¶¶83-84.

Chung is analogous art to the '990 Patent because it is in the same field of endeavor and is similarly directed to compensating the threshold voltage of the driving transistor. Chung, ¶87.

See Kanicki, ¶¶262-264.

2. Motivation to combine

Liu is directed to a reduced-size pixel structure, which includes a plurality of TFTs. §IV.A.4.a. Liu does not limit the number of TFTs in its OLED driving circuit. *Id.*, ¶32. Chung discloses a similar OLED drive circuit, which additionally includes a seventh TFT, which increases the OLED's lifespan and brightness uniformity of pixels. Chung, ¶¶11, 57.

POSITAs would have thus recognized Liu's OLED driving circuit and OLED's brightness uniformity would be improved by introducing Chung's seventh TFT for applying a reverse bias to the OLED, and preventing degradation of the OLED. Chung, ¶¶83-84.

POSITAs would have had a reasonable expectation of success because Chung explicitly described the implementation of a seventh TFT; the introduction of a single additional TFT would not have appreciably impacted the size of Liu's driving circuit.

POSITAs would have been motivated to apply Chung's known technique (adding a seventh TFT) to a known device ready for improvement (Liu's 6T1C OLED driving circuit) to yield predictable results (preventing degradation of OLED). POSITAs would have had a reasonable expectation of success, because incorporating a seventh transistor into a 6T1C circuit was well-known by 2012, as

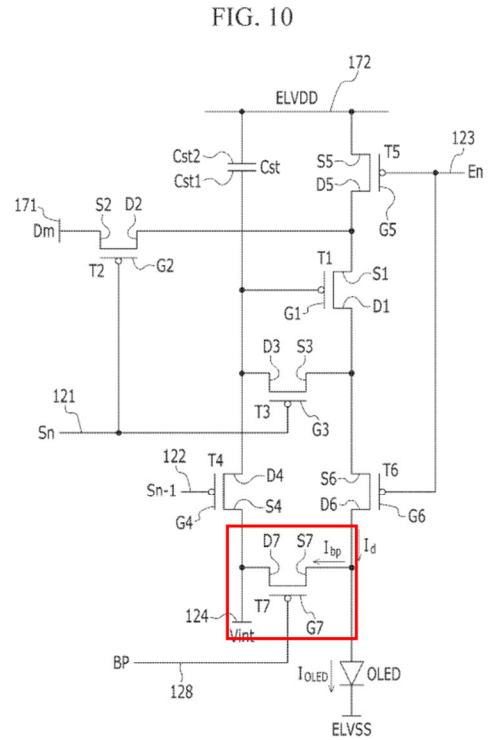
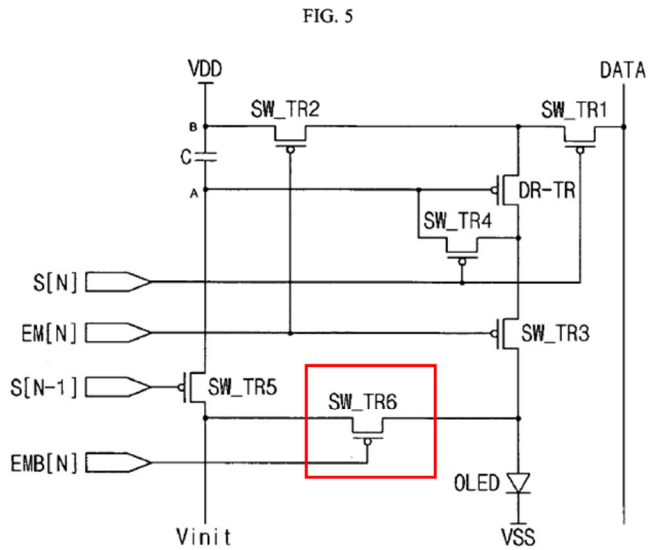
evidenced by Chung and other known prior art references, and such modifications were well within the skill set of POSITAs.

Furthermore, Liu can be combined individually with each of Udagawa and Chung. In each instance, the combination involves modifying a distinct aspect of Liu. POSITAs would recognize that each combination can be implemented without affecting the others. Accordingly, POSITAs would have found it obvious and would have been motivated to combine Liu with each of Udagawa and Chung. Such modifications would have been well within the skillset of POSITAs because it involved routine changes to the driver circuit, and POSITAs would have thus had a reasonable expectation of success in making those modifications.

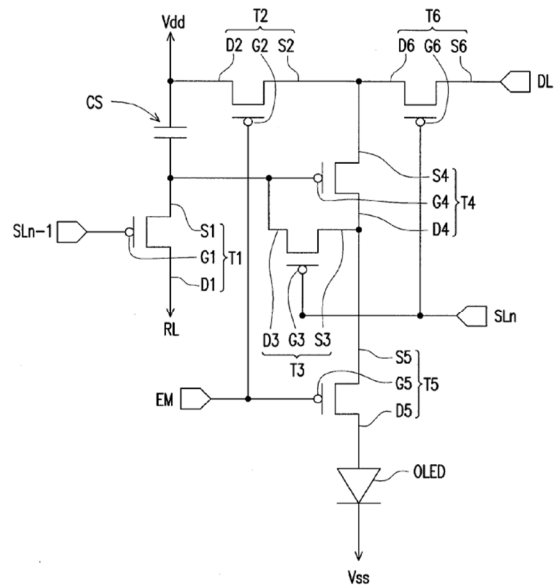
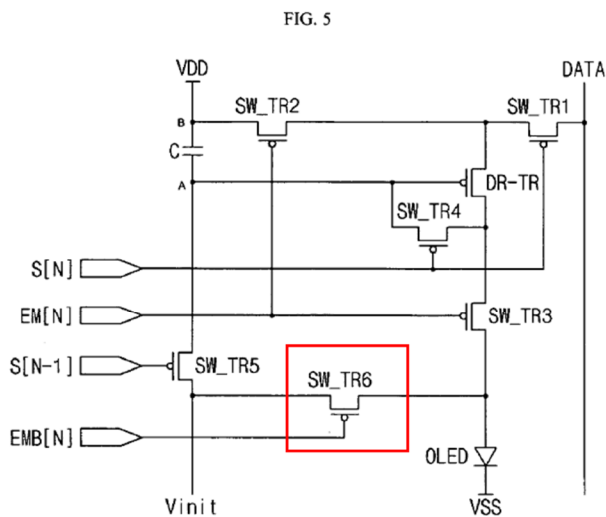
See Kanicki, ¶¶265-270.

3. Claim 7

The driving circuit could have more or less than six TFTs. Liu, ¶¶32, 58. Chung discloses an OLED drive circuit similar to those described in Liu and in Figure 10 of the '991 Patent, which additionally includes a seventh TFT. §IV.C.1. Annotated Figure 5 of Chung (left) is shown with '991 Patent Figure 10 (right) below, highlighting the seventh TFT.



As shown below, Chung's circuit is identical to Liu, except for the additional seventh TFT (SW_TR6).



Chung discloses SW_TR6 connected to the OLED and initialization TFT (SW_TR5). Chung, ¶¶57, 60, 63. The addition of SW_TR6 prevents “degradation of the organic light emitting diode OLED” during the initialization period. Chung, ¶84.

POSITAs would have been motivated to incorporate Chung’s seventh TFT to prevent degradation of the OLED during initialization. Such a modification of Liu would have improved the performance of Liu’s drive circuit with minimal increase in size. An example modified drive circuit incorporating Chung’s TFT in Liu’s drive circuit is shown below in modified Figure 5.

See Kanicki, ¶¶271-278.

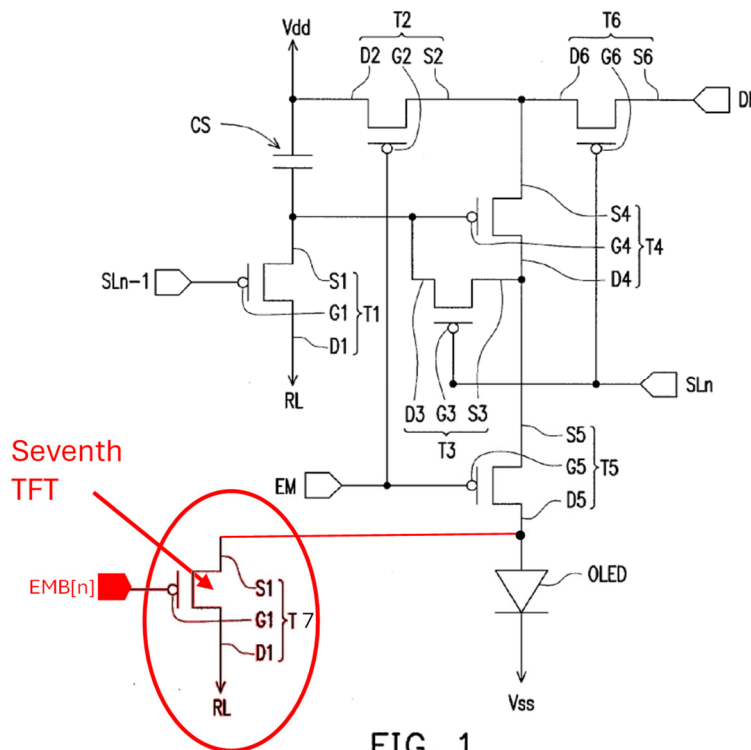


FIG. 1

4. Claim 14

Claim 14 is substantially similar to claim 7, except for reciting “the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor.”

Transistors T1 to T6 utilize a portion of the semiconductor layer coupled to the corresponding transistor. Liu, ¶35; §§IV.A.4.f (1[h-1]), IV.A.4.k (1[l]). POSITAs would have understood that when adding an additional TFT, the semiconductor layer would be deposited for that TFT because it would have used the design disclosed in Liu. Furthermore, Liu discloses the semiconductor layer is contiguous between all TFTs. *See, e.g.*, Liu, FIG. 3A. POSITAs would have found it obvious to continue the semiconductor layer to incorporate T7. Using a contiguous semiconductor layer would have been a natural choice given Liu’s layer was contiguous. Moreover, it was one of two options (contiguous or non-contiguous). *Id.* Accordingly, Liu-Udagawa-Chung teaches or suggests the semiconductor layer extended contiguously from T5 to a seventh TFT. This is particularly so because both the seventh TFT and T5 connect to the OLED and using the same connection point (V4) would eliminate the need for connecting the TFTs using other layers of the design.

For the additional reasons explained for claim 7, Liu-Udagawa-Chung teaches the remaining limitations of claim 14. §IV.C.3.

See Kanicki, ¶¶279-282.

5. Claim 21

See discussion in claim 7. §IV.C.3; Kanicki, ¶283.

6. Claim 27

See discussion in claim 12. §IV.C.4; Kanicki, ¶284.

D. Ground 1D: Claims 7 and 14 are Unpatentable over Liu, Udagawa, Chung, and Nakayama

1. Motivation to combine

As previously discussed, the Liu reference can be combined individually with each of the cited references—Udagawa, Nakayama, and Chung. Each combination involves modifying a distinct aspect of Liu. POSITAs would have recognized that each combination can be implemented without interfering with the others. Accordingly, POSITAs would have found it obvious and would have been motivated to combine Liu with each of Udagawa, Nakayama, and Chung.

See Kanicki, ¶¶285-286.

2. Claims 7 and 14

As explained above in Grounds 1A and 1B, Liu-Udagawa or Liu-Udagawa-Nakayama teach claims 1-4 and 10-11 from which claims 7 and 10 depend.

§§IV.A.4-IV.A.7, IV.B.3-IV.B.4; IV.A.11-IV.A.12. Chung provides the seventh TFT for claim 7. §IV.C.3.

POSITAs would have been motivated to combine Liu individually and together with Udagawa, Nakayama, and Chung. §IV.D.1. Accordingly, for the reasons explained above, Liu-Udagawa-Nakayama-Chung teaches claims 7 and 14.

See Kanicki, ¶¶287-290.

E. Ground 1E: Claims 9, 29, and 30 are Unpatentable over Liu, Udagawa and Murade

1. Murade

Murade discloses an electro-optical device with a high-quality image. Murade, Abstract. Like Liu, the device includes voltage lines, substrate, pixel electrode, storage capacitor, and TFTs. *Id.*, Abstract, ¶21 Murade discloses an additional capacitor connected to the data line with the same structure as the storage capacitor. *Id.*, Abstract, ¶¶12-13, 91. The data line is connected to the bottom plate 511-1 of the capacitor through “contact hole 581” that passes through a hole (591) in the upper capacitor plate 310a. *Id.*, ¶88-89, FIGs. 6-7.

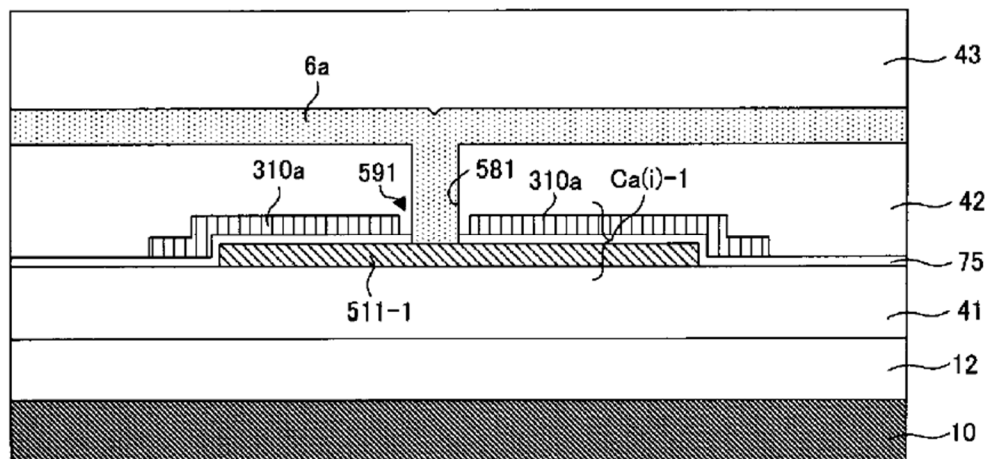
Murade and the '991 Patent are in the same field of endeavor; similar to the '991 Patent, both are directed to enhancing the display of electro-optical devices, while achieving high-density and downsizing the device. Murade, ¶7. Petitioner

relies on Murade for circuit routing connections. These teachings are agnostic to the type of display.

See Kanicki, ¶¶291-294.

2. Motivation to combine

As discussed above, Liu is directed to a reduced-size pixel structure. §IV.A.4.a. Murade is also related to reducing pixel size. Murade, ¶7. Murade further explains that in such a display, unevenness can occur because of degradation of the data line signal used by adjacent pixels. *Id.*, ¶¶4, 11. Murade's solution utilizes a capacitor with a hole (591) made in the top capacitor plate to connect a signal line to the bottom capacitor plate. *Id.*, ¶¶11, 88-89, FIGs. 6-7.



Murade, Figure 7.

POSITAs would have modified Liu's connections based on the teachings of Murade and understood that in a display layout configuration where a capacitor plate

prevented direct routing of a signal line from an upper layer to the lower capacitor plate, a hole can be made in the upper capacitor plate to enable the signal line connection. Additionally, connecting a capacitor in such a way is merely a design choice necessitated by the layout. *Id.*

POSITAs would have had a reasonable expectation of success because using a hole in an electrode to connect a line through it was well-known and such modification was well within the skill set of a POSITA.

See Kanicki, ¶¶295-297.

3. Claim 9

As explained above in Ground 1A for claim 9, POSITAs would have found it obvious to use metal layer 3 to connect T1 and T3 to BE because of Liu's teaching to move the storage capacitor plates to metal layers 1 and 2. §IV.A.10. Murade corroborates and confirms that making a hole in the top capacitor plate to route a signal line to the bottom capacitor plate was a known design technique. §IV.E.2. Thus, Liu in combination with Murade teaches to connect T3 ("fifth" TFT) and T1 ("sixth" TFT) to BE ("first capacitor plate") using a contact hole (e.g., via) through a hole in TE ("through a contact hole that passes through the second capacitor plate").

See Kanicki, ¶¶298-300.

4. Claim 29

See discussion in claim 9. §IV.E.3; Kanicki, ¶301.

5. Claim 30

See discussion in claim 2, Ground 1A. §IV.A.5; Kanicki, ¶302.

**F. Ground 2A: Claims 1-6, and 17-20 are Unpatentable over
Noguchi-I and Udagawa**

1. Noguchi-I

Noguchi-I describes a storage capacitor for an OLED display utilizing a shield electrode provided in a wiring layer between the pixel electrode and a wiring layer where the gate electrode resides; the shield electrode forms a region covering the gate electrode, reducing the parasitic capacitance between the gate electrode of the driving transistor and a pixel electrode (anode) of the OLED. Noguchi-I, ¶35.

Noguchi-I and the '991 Patent are in the same field of endeavor because Noguchi is also directed to the pixel structure of an OLED display driven by scanning lines, power source lines, signal lines, and transistors T1 to T6. Noguchi-I, ¶70. Similarly, both endeavor to compensate for the variability of the threshold voltage of the driving TFT. *Id.*, ¶15.

See Kanicki, ¶¶303-305.

2. Motivation to combine Noguchi-I and Udagawa

Both Noguchi-I and Udagawa described drive circuits for OLED displays and

both sought to improve the design and operation of OLEDs. Noguchi-I describes a pixel structure with reduced parasitic capacitance that improved image quality. Noguchi-I, ¶¶12, 15, 72. Udagawa describes drive circuit configurations that improved OLED's reliability, and consequently, its operations and image quality. Udagawa, ¶12. Therefore, POSITAs would have been motivated to combine the complementary teachings of Noguchi-I with Udagawa to achieve further improvements in image quality of the OLED display.

Specifically, Udagawa disclosed when the channel length of a TFT increases, the oxide film capacitance C_{ox} becomes larger, and at least a portion of this capacitance can be used as a retention capacitance of the OLED, thus improving OLED's image quality. Udagawa, ¶64. POSITAs would have found it obvious and would have been motivated to combine the complementary teachings of Udagawa with Noguchi-I, and specifically to use Udagawa's serpentine channel in Noguchi-I's driving TFT to further improve the OLED operation.

Notably, POSITAs would have been motivated to apply a known technique (using Udagawa's TFT with a longer channel) to a known device ready for improvement (Noguchi-I's pixel structure) to yield predictable results (capacitors being formed correctly and improving image quality). POSITAs would have had a reasonable expectation of success, because using TFT with a longer channel to reduce dispersion and increase capacitance was well-known by 2012, evidenced by

the teachings of Udagawa and other known prior art references, and such modifications were well within the skill set of POSITAs.

See Kanicki, ¶¶306-310.

3. Claim 1

Noguchi-I describes a “pixel of a conventional organic EL display device” with reference to Figures 8 and 9. Noguchi-I, ¶11. It then presents four related embodiments that build upon each other to address the perceived deficient response of the pixel. *Id.*, ¶¶66-95. All embodiments are based on the circuit diagram of Figure 1 (Noguchi-I, ¶¶66, 74, 79, 88) but progressively alter the construction of capacitor C1 and gate electrode of T4 in different ways (*id.*, ¶¶72, 77, 83, 91). Petitioner relies on the cumulative teachings of Noguchi-I embodiments that culminate in embodiment 4 (Figure 7). To the extent other figures of Noguchi-I are used below, they represent common features of Noguchi-I’s invention.

See Kanicki, ¶311.

a. 1[pre]

Noguchi-I discloses “an organic EL **display device**” with “a current emissive element such as an organic EL element.” Noguchi-I, Abstract, ¶¶1, 41. The display comprises a plurality of “pixels” (*id.*, ¶¶3, 70 (identifying one “display unit” having one pixel), where the “organic EL element” is an OLED (*id.*, ¶11, FIG. 1).

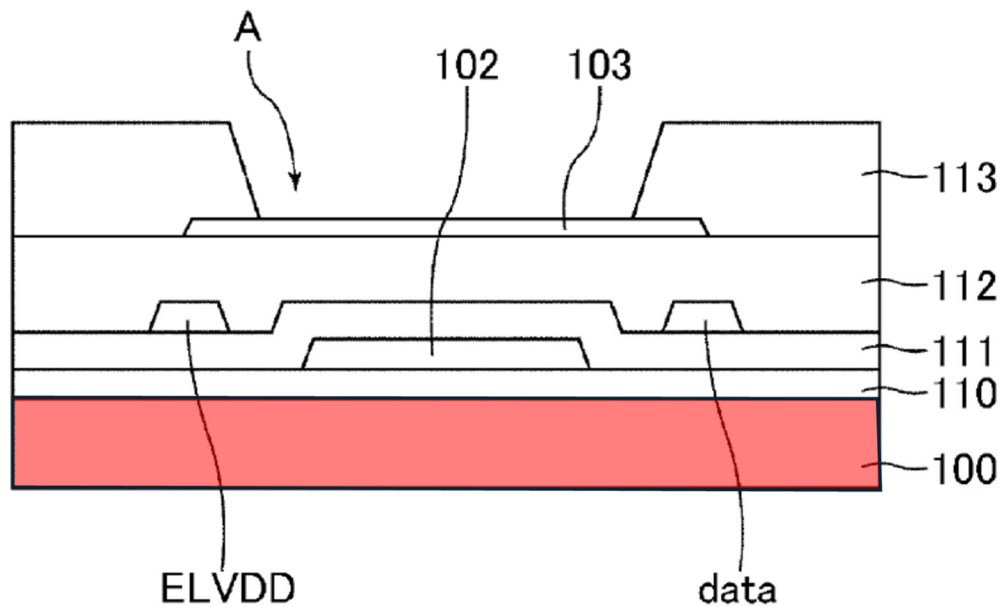
See Kanicki, ¶¶312-314.

b. 1[a]

Noguchi-I discloses a pixel comprising a “substrate 100.” Noguchi-I, ¶¶66-69, 98-114, FIGs. 3 (annotated below), 6, 9. It was well-known at the time that substrates for OLED pixels comprised glass, among other materials, and needed to be non-conductive so that the circuits placed on them operated properly. Liu, ¶33; Kim, 5:4-11.

See Kanicki, ¶¶315-317.

Fig. 3

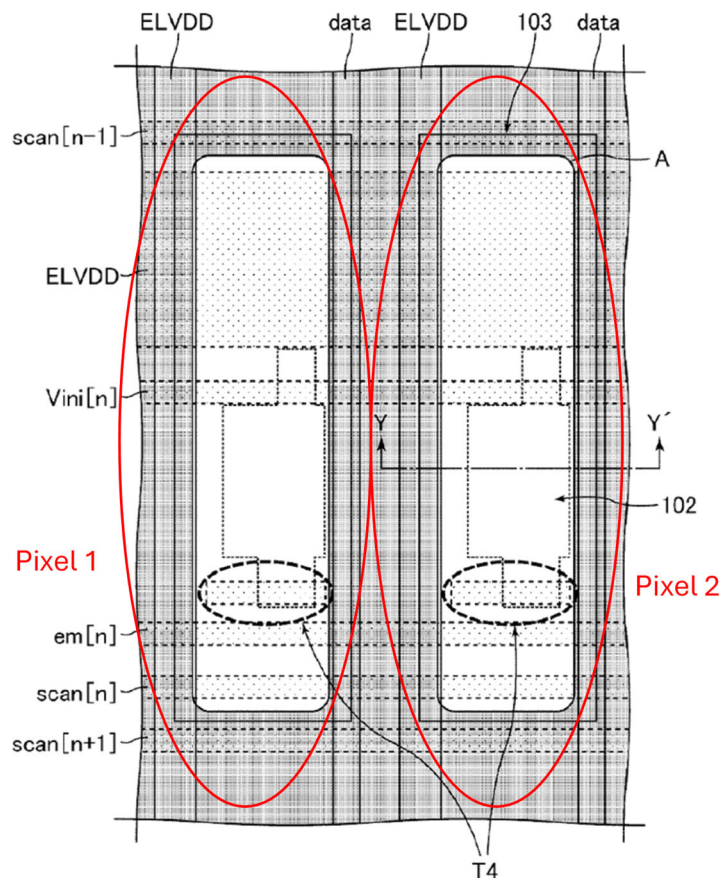


c. 1[b]-1[d]:

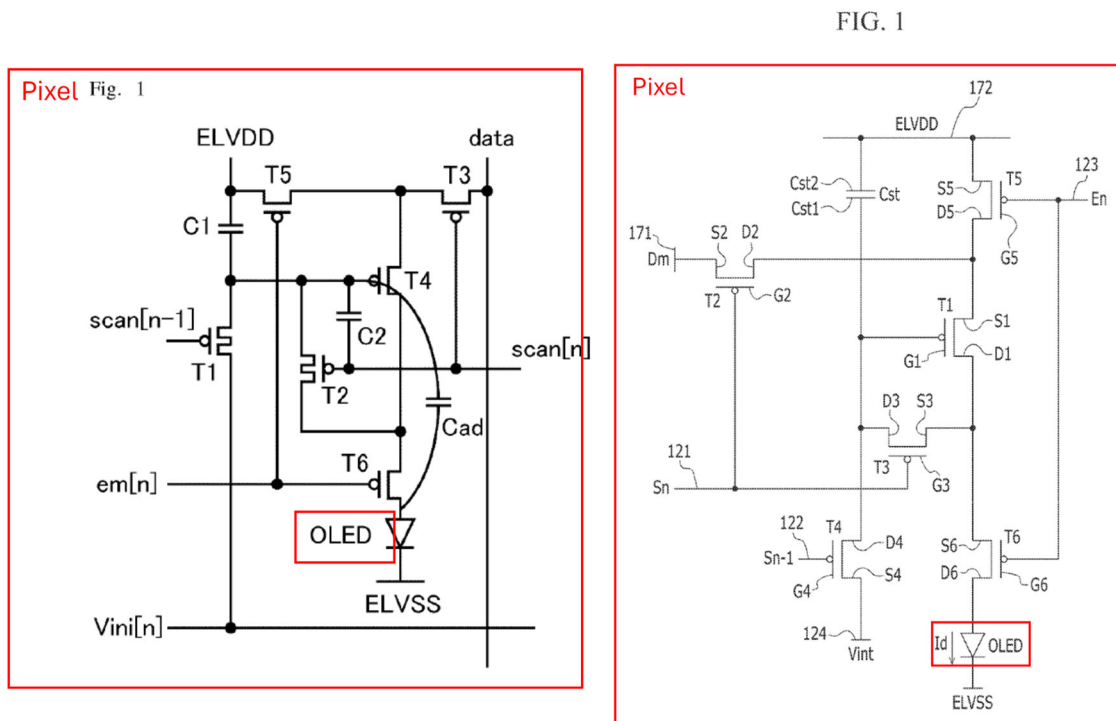
Plurality of Pixel Structures

Noguchi-I discloses a display with a plurality of pixels. *See* 1[pre], §IV.F.3.a. Each pixel structure includes TFTs, capacitor, and OLED. Noguchi-I, ¶¶11, 66-70, 74, 77, 79, 88, 91, FIG. 1. Noguchi-I explains item 103 in the figures is an OLED pixel electrode. *Id.*, ¶¶15, 110. Figure 1 shows there is only one OLED per pixel (“each of the pixels comprising an organic light emitting diode”). *Id.*, FIG. 1. Figures 2 (annotated below), 4, 5, and 7 show two pixels in the display (“a plurality of pixels”).

Fig. 2



Annotated Noguchi-I Figure 1 below (left) alongside '991 Patent Figure 1 (right) show the similarities between the driving circuits.



Plurality of First Voltage Lines (1[b]), Scan Lines (1[c]), and Data Lines (1[d])

Noguchi-I discloses the “first voltage line” as a “power source line ELVDD” in a second wiring layer. Noguchi-I, ¶71, FIG. 1. POSITAs would have understood ELVDD is a “voltage line” because ELVDD is common notation to denote a voltage, also used by the '991 Patent. '991Pat., 6:25-37.

Noguchi-I discloses scan lines (scan[n-1] and scan[n]) in the TFT circuit, stating they denote “an [n-1]-th and an [n]-th scanning line”—signifying a plurality of scan lines, not limited to the two shown in the circuit. Noguchi-I, ¶11; Table, *infra*.

Each pixel structure includes a data line, data, used in each pixel structure of a display. *Id.*

As explained above, POSITAs would have understood Noguchi-I's circuit represents one of a plurality of pixel structures, each requiring the voltage and signal lines to be supplied to it. Accordingly, Noguchi-I discloses "a plurality of" voltage, scan, and data lines to each pixel structure.

Annotated Noguchi-I Figure 1 below (left) alongside '991 Patent Figure 1 (right) shows the similarities between the circuits and show Vdd, scan lines, data lines.

Fig. 1

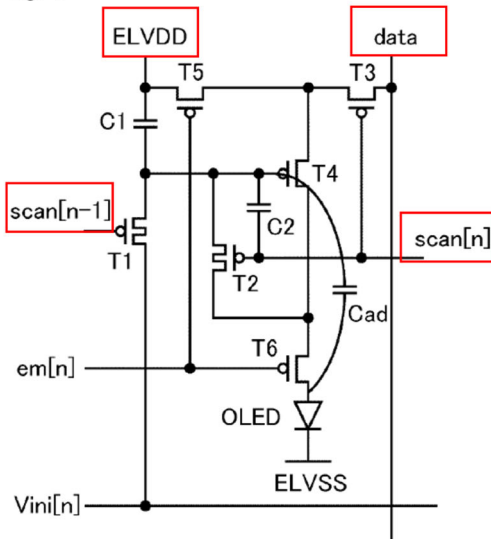
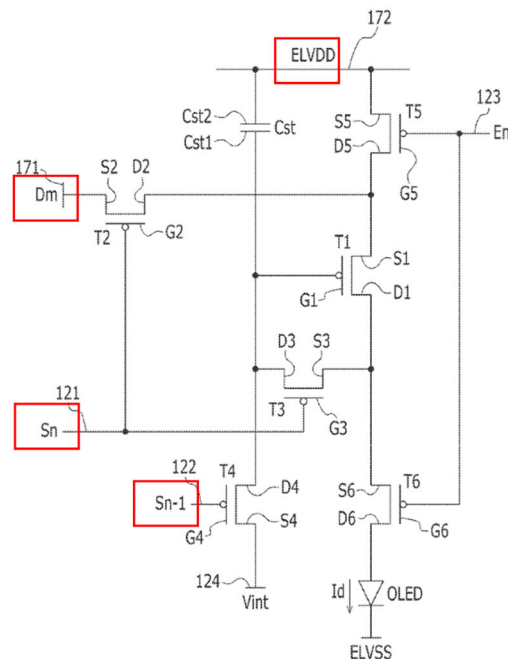


FIG. 1



Mapping of Noguchi-I to '991 Patent

Table below cross-references each transistor and signal line of '991 Patent Claims and detailed description to similar elements in Noguchi-I.

See Kanicki, ¶¶318-329.

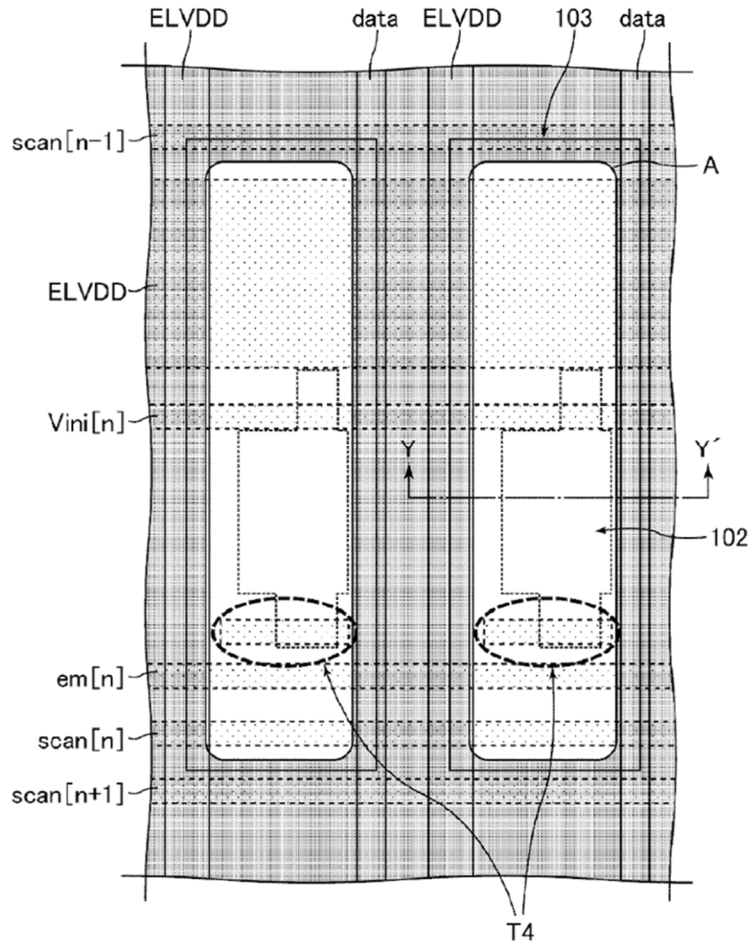
Claims	'991	Noguchi-I
1 st TFT	T2	T3
2 nd TFT	T1	T4
3 rd TFT	T5	T5
4 th TFT	T6	T6
5 th TFT	T3	T2
6 th TFT	T4	T1
Capacitor	Cst	C1
First Capacitor Plate	125h	Gate electrode 102
Second Capacitor Plate	127	Shield electrode 104
1 st Voltage line	ELVDD	ELVDD
2 nd Voltage line	Vint	Vini[n]
OLED	OLED	OLED
1 st Scan line	Sn	scan[n]
2 nd Scan line	Sn-1	scan[n-1]
Light emission control line	En	em[n]
Data line	Dm	data

d. 1[e]-1[f]

As explained in 1[b], Noguchi-I teaches or suggests multiple pixels in a display, each having a driving circuit (““plurality of driving circuits”) comprising a plurality of TFTs to drive the OLED for that pixel. §IV.F.3.c. Noguchi-I, ¶¶1, 11,

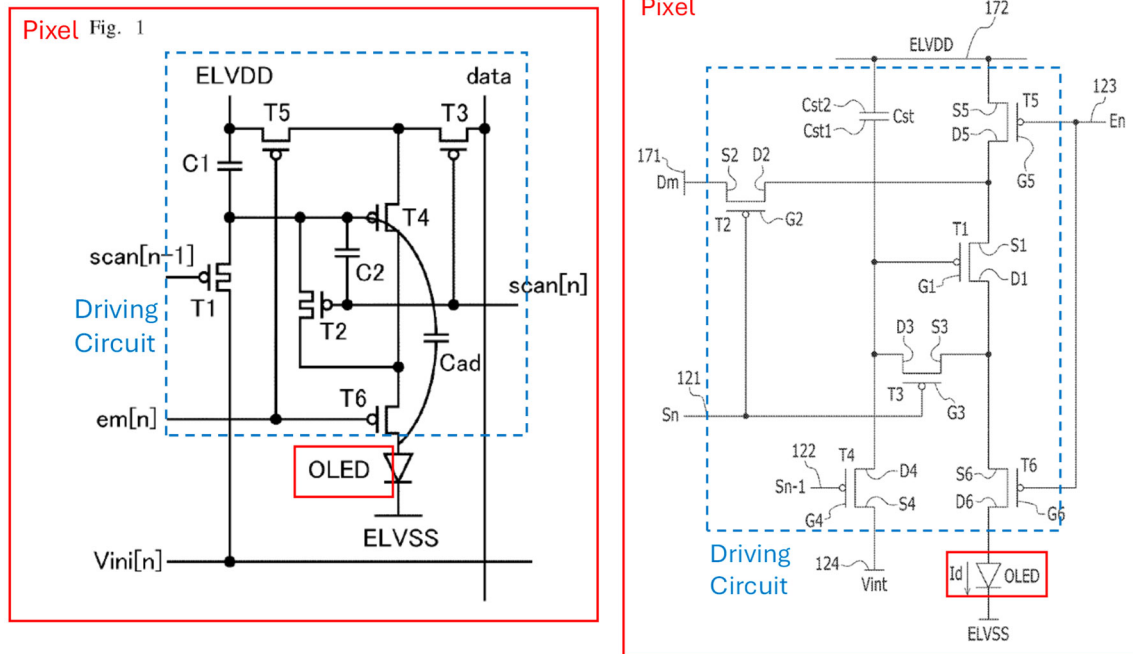
FIG. 1. Each TFT is disposed in the pixel, and a region denoted by “A.” Noguchi-I, ¶70, FIG. 2 (below).

Fig. 2



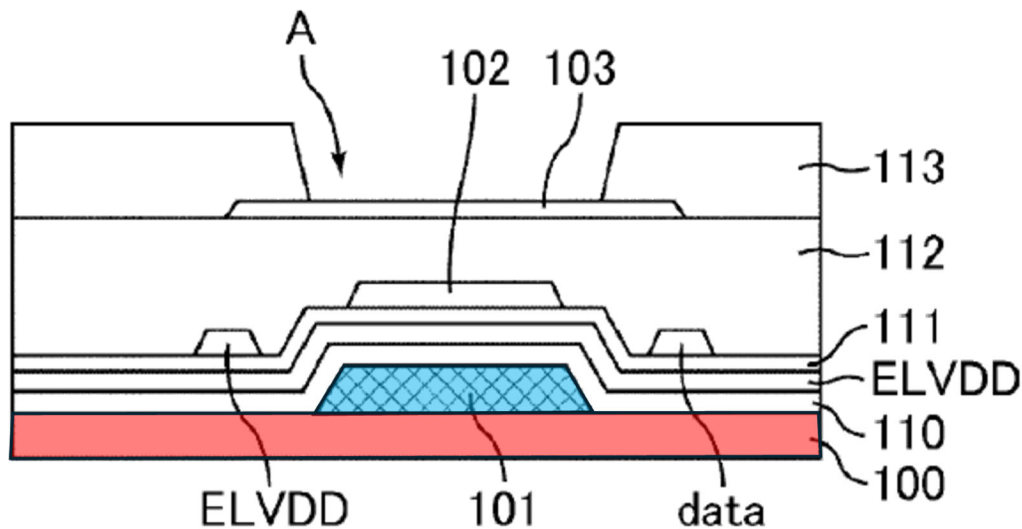
Each driving circuit is connected to an OLED (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). *Id.*, ¶31, FIG. 1. Annotated Noguchi-I’s Figure 1 below (left) alongside ’991 Patent Figure 1 (right) show the relationship of a pixel and driving circuit.

FIG. 1



Noguchi-I explains TFTs (T1-T6) are formed in a semiconductor layer on the substrate (“a plurality of driving circuits on the substrate”). Noguchi-I, ¶¶64, 70, FIGs. 8, 9. Figure 9 (annotated below) shows the substrate 100 (red) and semiconductor layer (blue). POSITAs would have understood that the plurality of Noguchi-I’s driving circuits, including the plurality of TFTs would have been formed on a single substrate including multiple pixels.

Fig. 9



Furthermore, annotated Figure 1 above shows the OLED is directly connected to a driving circuit (“each of the organic light emitting diodes being electrically coupled to a respective driving circuit”). Noguchi-I, FIG. 1.

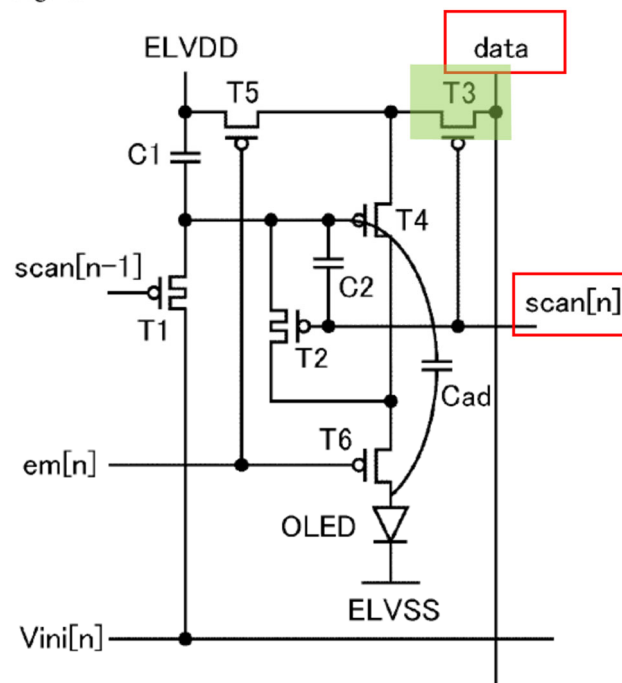
See Kanicki, ¶¶330-335.

e. 1[g]

Noguchi-I discloses the “first thin film transistor” as T3 coupled to “one of the plurality of scan lines,” scan[n], and to “a data line,” data, illustrated in Figure 1. T3 is formed in a portion of the semiconductor layer on the substrate (“implemented in a first portion of a semiconductor layer disposed on the substrate”). §IV.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9.

Noguchi-I explains “transistor T3 **responds to the scan signal inputted from the scanning line scan[n]**, and performs switching of the **data signal inputted from the signal line data.**” *Id.*, ¶11, FIG. 1. Accordingly, T3 is electrically connected (“coupled”) to scan line scan[n] and a data line (“one of the plurality of scan lines and to one of the plurality of data lines”).

Fig. 1



Furthermore, as explained below, Noguchi-I discloses each of the six transistors and capacitor recited in 1[h]-1[m]. *See also* §**Error! Reference source not found.** (table).

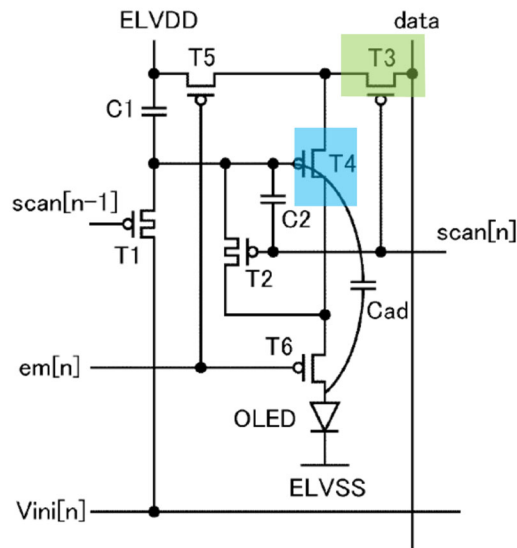
See Kanicki, ¶¶336-339.

Claims	'991	Noguchi-I
1 st TFT	T2	T3
2 nd TFT	T1	T4
3 rd TFT	T5	T5
4 th TFT	T6	T6
5 th TFT	T3	T2
6 th TFT	T4	T1
Capacitor	Cst	C1

- f. **1[h-1]: “a second thin film transistor implemented in a second portion of the semiconductor layer, wherein the semiconductor layer couples the second thin film transistor to the first thin film transistor, and”**

Noguchi-I discloses the “second thin film transistor” as TFT T4 connected to T3 (“first thin film transistor”). Noguchi-I, FIG. 1 (annotated).

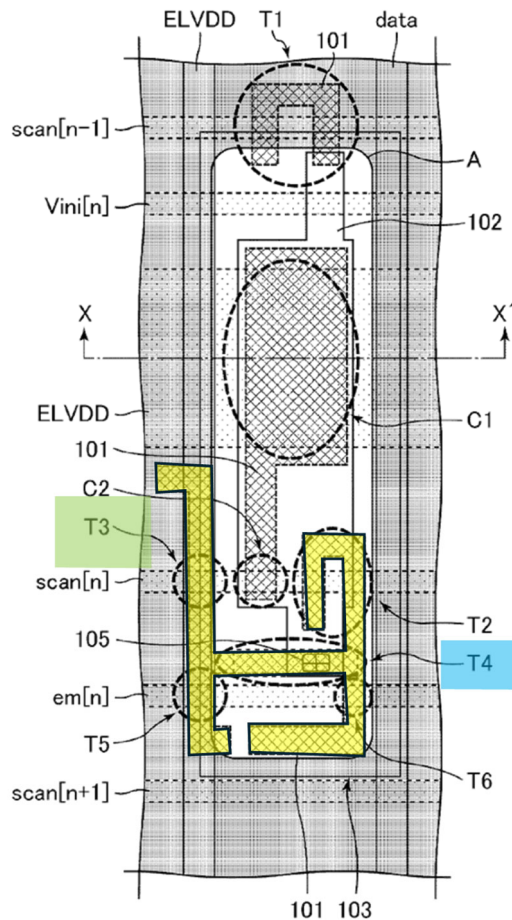
Fig. 1



As explained in 1[e], T4 is formed in a portion of the semiconductor layer on the substrate (“implemented in a second portion of a semiconductor layer disposed on the substrate”). §IV.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9. Figure 8 provides the only semiconductor layout illustration in Noguchi-I and is an example of how the TFTs are positioned within the pixel. Annotated Figure 8 (below) shows the locations of various TFTs over the semiconductor pattern (yellow). Notably, T4 is formed in a different portion in the semiconductor layer (yellow), adjacent to T3. In Figure 8 the semiconductor layer is continuous from T4 to T3, and a POSITA would have found it obvious that “the semiconductor layer couples” T4 (“second” TFT) to T3 (“first” TFT). Noguchi-I, FIG. 8, FIGs. 2, 4, 5, 7 (showing T4 in the same location). Having a semiconductor layer that connects or couples two TFTs was a routine aspect of pixel design and was well-known in 2012.

See Kanicki, ¶¶340-343.

Fig. 8



g. 1[h-2]

As explained in Ground 1A for 1[h-2] and 1[n], Udagawa teaches a “serpentine” (e.g., “bent”) channel of drive transistor T4. §§IV.A.4.g, IV.A.4.l. For the reasons explained in §0, POSITAs would have been motivated to incorporate Udagawa’s “serpentine” or bent channel (thereby increasing channel length) in Noguchi-I’s OLED driving circuit to reduce the dispersion that occur when pixels are reduced in. Modifying Noguchi-I to use Udagawa’s longer channel aligns with Noguchi-I’s objectives of reducing the influence of parasitic capacitance, Cad,

because forming the channel in this way reduces dispersion in reduced-size pixels, enabling improved operation of the driving TFT. Thus, the combination would have been obvious.

See Kanicki, ¶¶344-346.

h. 1[i]-1[k]

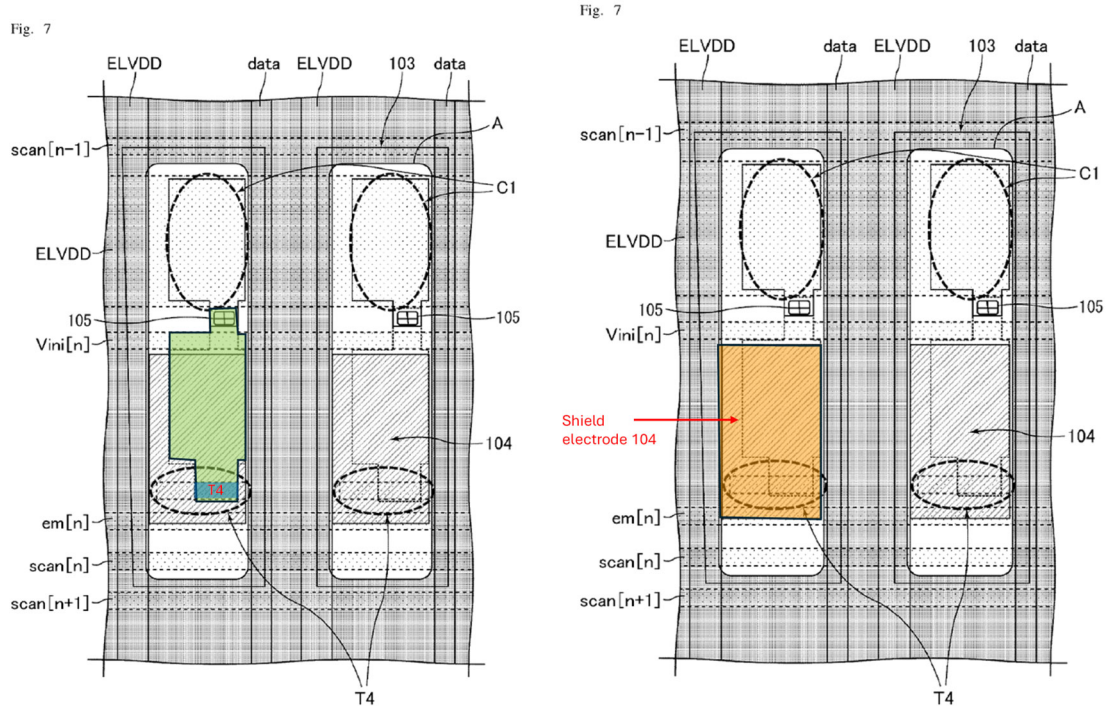
Noguchi-I discloses the “storage capacitor” as capacitor C1 connected between the gate electrode of T4 and ELVDD, and includes a gate electrode 102, which is also a capacitor plate (Noguchi-I, ¶77), (“first capacitor plate”) in the first wiring layer, and shield electrode 104 (“second capacitor plate”) in the second wiring layer. *See id.*, ¶¶83-84, 86, 91-93, FIGs. 5, 7.

Noguchi-I’s Capacitor C1 Structure

“[C]apacitor C1 [is] formed through overlap of the gate electrode and the power source line ELVDD” (Noguchi-I, ¶91) and shield electrode 104 is connected to ELVDD. *Id.*, ¶86. Furthermore, Noguchi-I explains “[t]he gate electrode of T4 forms capacitance with the second wiring layer.” *Id.*, ¶95. Thus, POSITAs would have understood that C1 is formed in-part between gate electrode 102 and overlapping shield electrode 104.

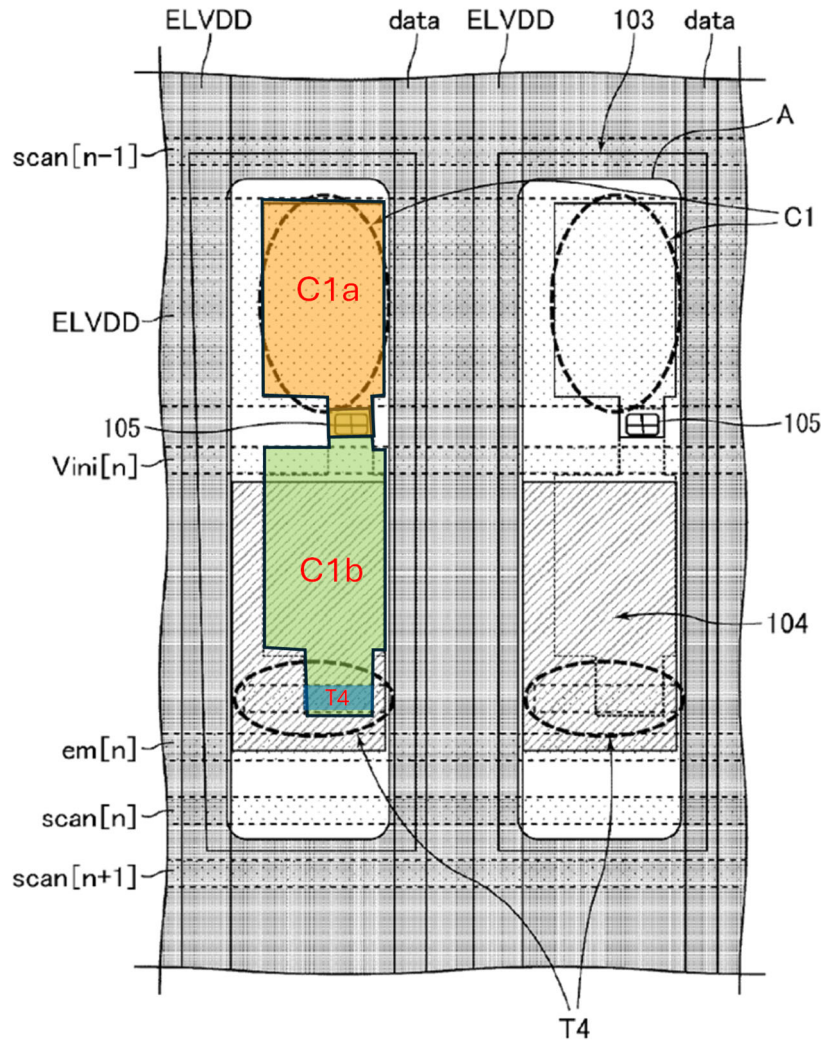
Figure 7 is separately annotated below to show the “first capacitor plate” (green), which is also gate electrode 102 of T4 (“configured to operate as a gate

electrode of the second thin film transistor”), and shield electrode 104 (orange) (“second capacitor plate”). Noguchi-I, ¶¶15, 70, 81, 95.



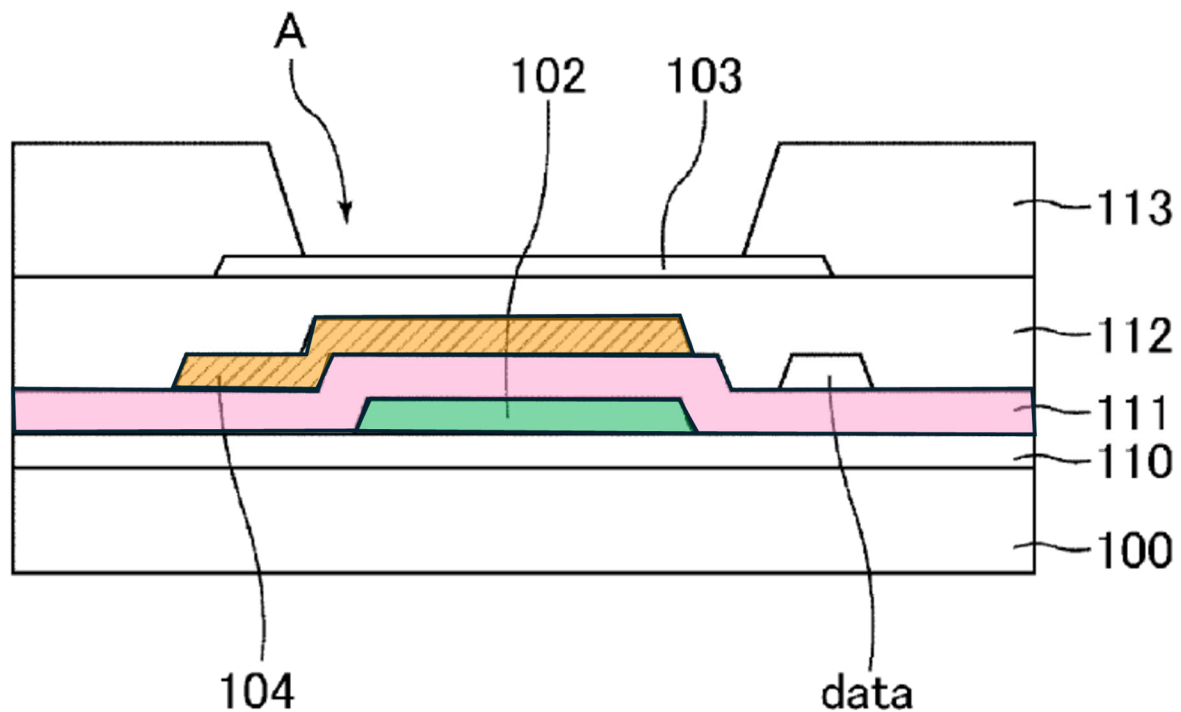
While annotated Figure 7 above only shows one part of capacitor C1 (C1b), Noguchi-I’s capacitor C1 is made up of two parts, as annotated below. Noguchi-I, ¶¶75, 77, 89, 91. Capacitor C1 has a capacitance equal to the series addition C1a and C1b. Petitioner has pointed to C1b as meeting the claim limitation of the storage capacitor comprising a first and second capacitor plate.

Fig. 7



C1b (“first” plate) operates as **gate electrode 102** for T4, and is in the first wiring layer, whereas **shield electrode 104** (“second” plate) is in the second wiring layer, with **Interlayer dielectric 111** disposed therebetween (“an insulating layer between the first capacitor plate and the second capacitor plate”). Noguchi-I, ¶¶91-95., FIG. 6 (annotated).

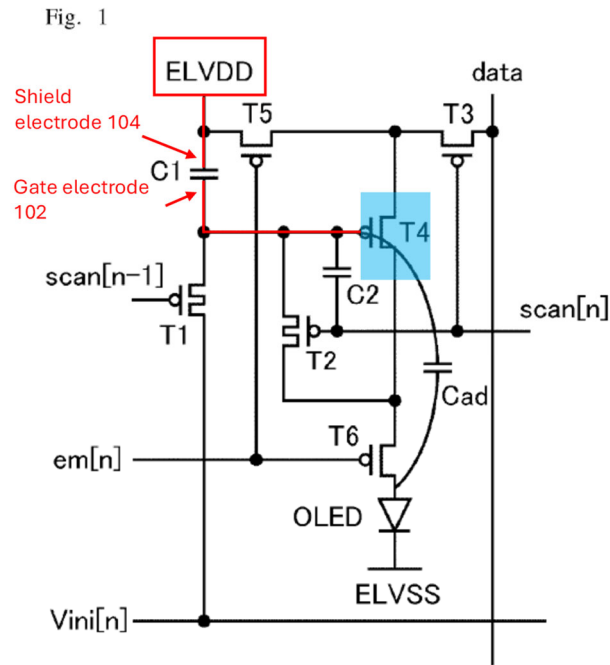
Fig. 6



C1 Connections

Noguchi-I's capacitor C1 is connected to gate of T4 and ELVDD, as shown by the red line in annotated Figure 1. Noguchi-I, FIG. 1 (annotated).

See Kanicki, ¶¶347-357.



i. 1[l]-1[m]

Below, the Table from 1[b] is partially reproduced, along with annotated Figures 1 (left) and 8 (right), to facilitate the mapping of limitations of 1[l]-1[m] to Noguchi-I. See §**Error! Reference source not found.** (table).

Claims	'991	Noguchi-I
1 st TFT	T2	T3
2 nd TFT	T1	T4
3 rd TFT	T5	T5
4 th TFT	T6	T6
5 th TFT	T3	T2
6 th TFT	T4	T1
Capacitor	Cst	C1

Fig. 1

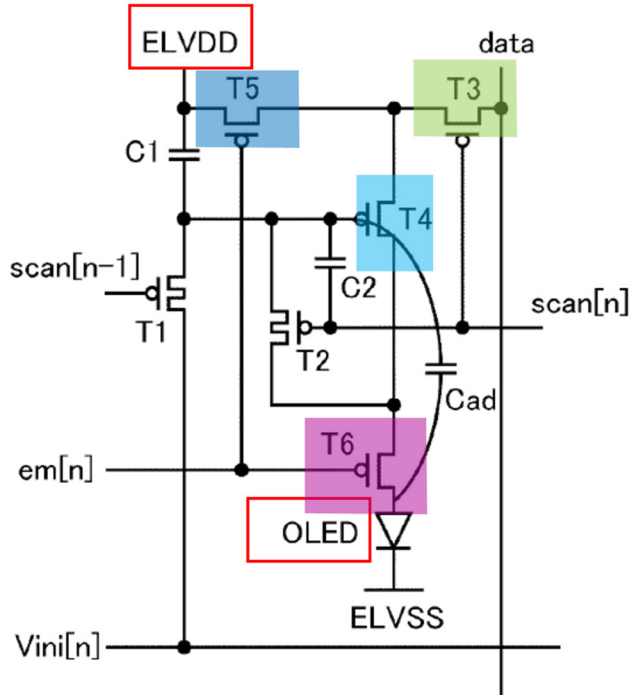
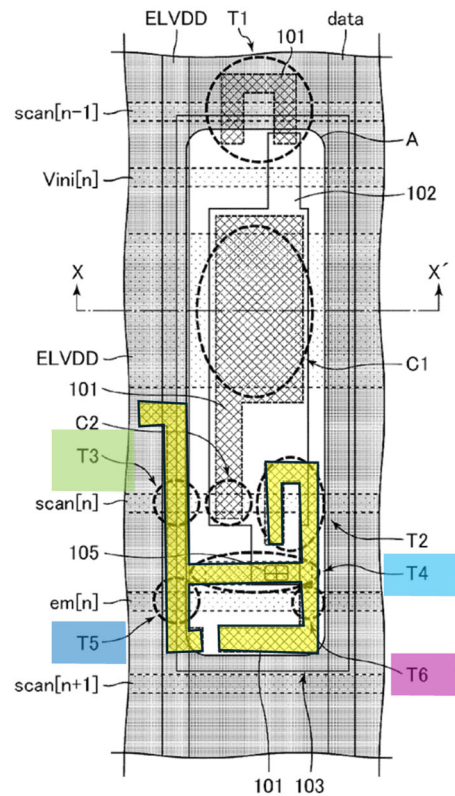


Fig. 8

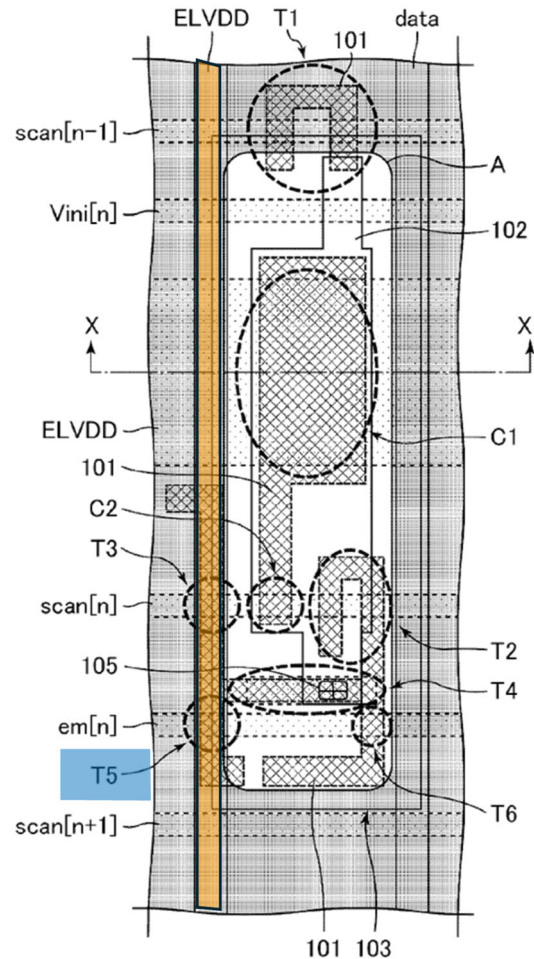


1111: T5 (“third” TFT) is formed in a portion of the semiconductor layer on the substrate (“implemented in a third portion of a semiconductor layer disposed on the substrate”). IV.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9.

Figure 1 illustrates source of T5 connects to ELVDD (“electrically coupled to one of the plurality of first voltage lines”); T5 is also connected to T3 (“first” TFT) and T4 (“second” TFT) (“the third thin film transistor [coupled] to the first thin film transistor and to the second thin film transistor”). Noguchi-I, FIG. 1.

Annotated Figure 8 shows T5 is positioned below ELVDD (“one of the plurality of first voltage lines”) and uses ELVDD to “perform[] switching of the current that is supplied to the transistor T4.” *Id.*, ¶11, FIG. 8.

Fig. 8



Although not shown, POSITAs would have found it obvious that a typical way to connect the source of T5 to ELVDD is through a via to the semiconductor layer (“electrically coupled...through the semiconductor layer”), an example of which is disclosed in Noguchi-I as contact hole 105. Vias are well-known in the art

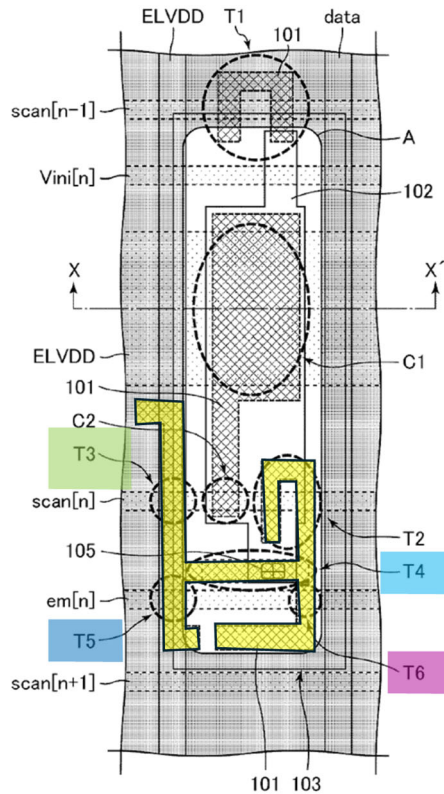
and commonly used to connect structures on different levels of a semiconductor structure. Therefore, a POSITA would have found it obvious that the source of T5 (part of “semiconductor layer” of “third” TFT) would couple T3 to ELVDD (“voltage line”).

1[m]: Noguchi’s T6 (“fourth thin film transistor”) is formed in a portion of the semiconductor layer on the substrate (“implemented in a fourth portion of the semiconductor layer”). IV.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9.

Figure 1 shows T6 connects to T4 (“the fourth thin film transistor [coupled] to the second thin film transistor”), and to OLED (“fourth thin film transistor is electrically coupled to the respective organic light emitting diode”). Noguchi-I, FIG. 1, ¶11. As explained above a POSITA would have found it obvious to use a via to connect T6 from the semiconductor layer to the OLED (“electrically coupled...through the semiconductor layer”).

As explained in 1[h-1], Figure 8 of Noguchi-I illustrates an example of the semiconductor layer that shows T5 is connected to and adjacent to T4 and T3 in the semiconductor layer (“the semiconductor layer couples” T5 to T3 and T4), as recited in 1[l]. Noguchi-I, ¶11, FIG. 8.

Fig. 8



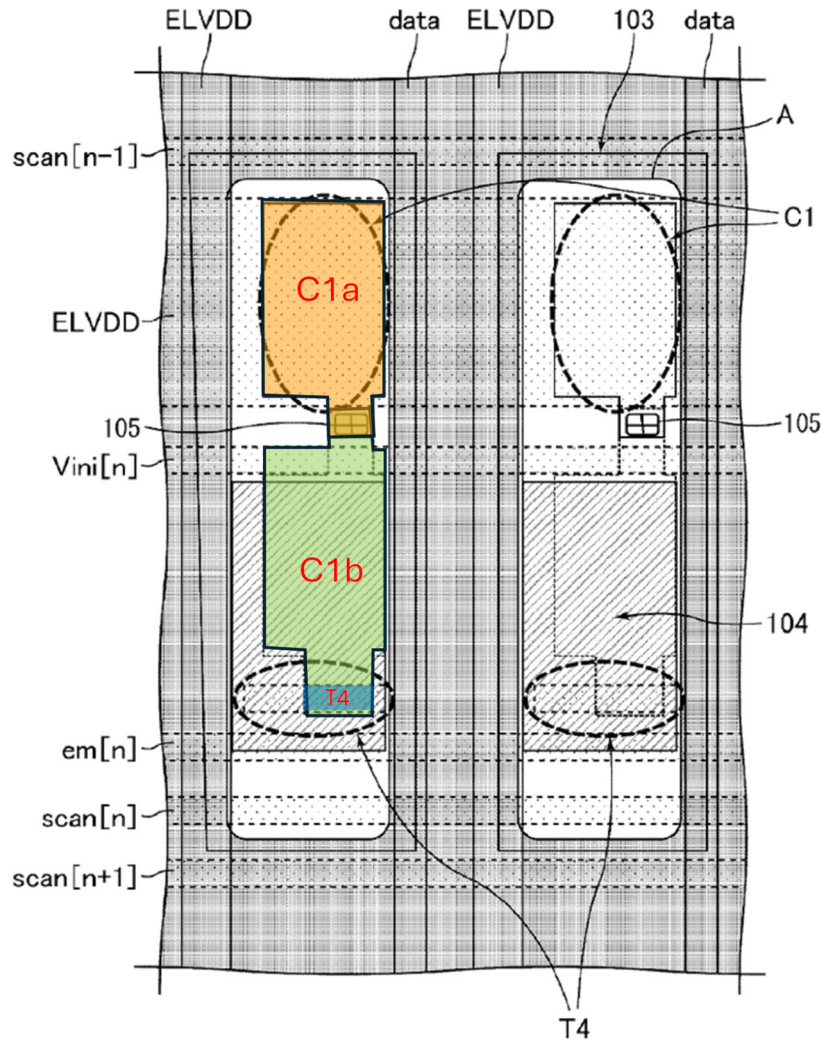
Regarding 1[m], Figure 8 similarly shows T6 is connected to and adjacent to T4 in the semiconductor layer (“the semiconductor layer couples” T6 to T4). Noguchi-I, ¶11, FIG. 8. Having a semiconductor layer that connects or couples two TFTs was a routine aspect of pixel design and was well known at the time of the alleged invention.

See Kanicki, ¶¶358-365.

j. 1[n]

As explained in 1[i]-1[k], capacitor C1 comprises C1a and C1b, shown in annotated Figure 7 below. §IV.F.3.h.

Fig. 7



Noguchi-I indicates the position of T4 by a dashed box (shown in blue) in Figure 7. Noguchi-I, FIG. 7; Kanicki, ¶368 (explaining that the region indicated as T4 in Figure 7 corresponds to the same region for T4 in Figure 8, which shows the semiconductor layer).

Because the channel of T4 is at least under gate electrode 102 (shown in blue) in Figure 7, POSITAs would have found it obvious that gate electrode of T4 (i.e.,

the green-annotate plate in the above figure) covers the channel region of T4, including its bent or curved region (“bent portion of the second portion of the semiconductor layer is under the first capacitor plate”) when modified by Udagawa. As explained in §IV.A.4.g, Udagawa describes different lengths and numbers of serpentine structures can implemented (Udagawa, ¶20), and a POSITA would have understood that gate electrode of T4 (green-annotated plate in the above figure or a part thereof) of Noguchi-I would overlap the extended channel in the combination.

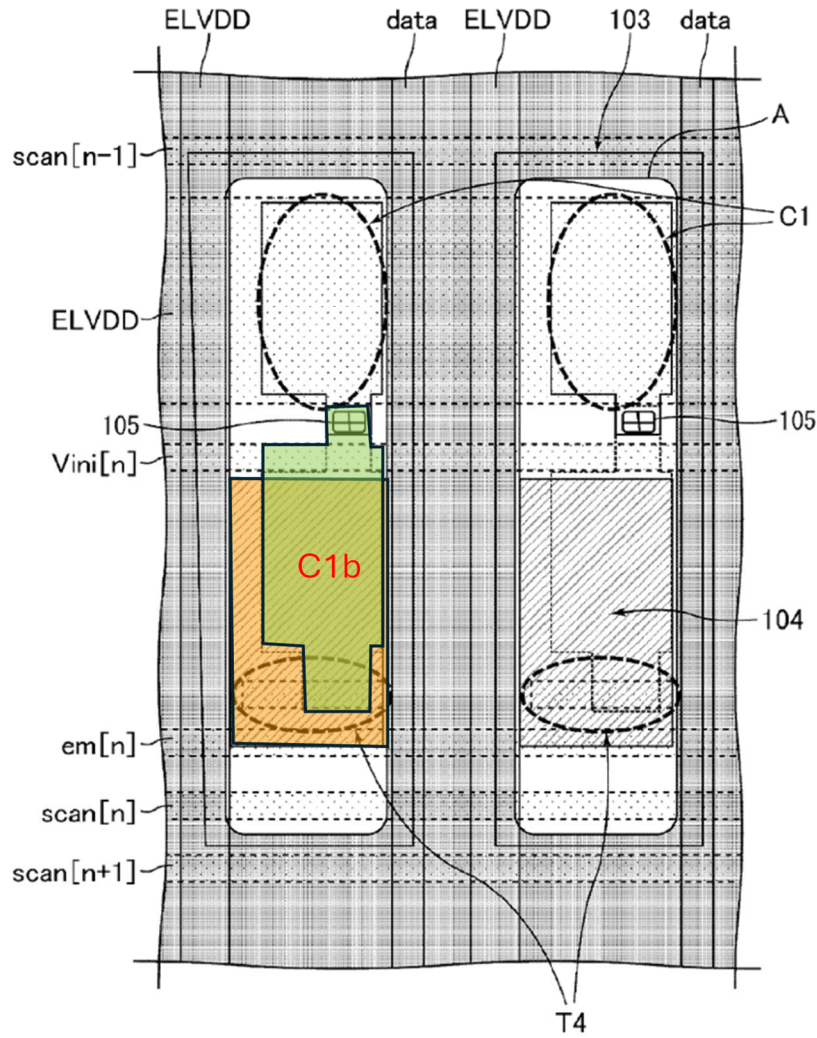
See Kanicki, ¶¶366-369.

4. Claim 2

Noguchi-I teaches shield electrode 104 covers gate electrode 102 (see annotated Figures 6 and 7 below). Noguchi-I, ¶83 (“shield electrode 104 forms a region covering the gate electrode 102”), ¶92 (same), FIGs. 6 (annotated), 7 (annotated). Shield electrode 104 (large orange box at bottom of Figure 7) covers a periphery of gate electrode 102 (“completely surrounds a periphery of the first capacitor plate in a plan view”). As explained in §IV.A.5 (Ground 1A), POSITAs would have understood that at least a portion around the outside of the first capacitor plate is surrounded.

See Kanicki, ¶¶370-372.

Fig. 7



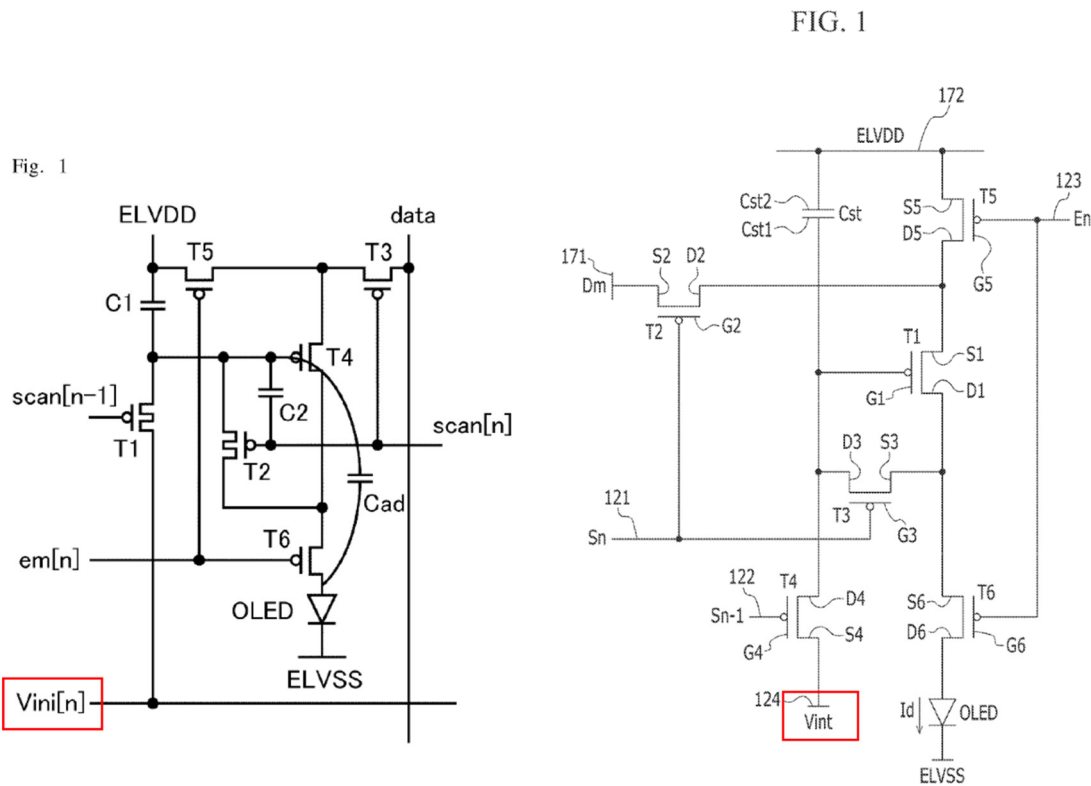
5. Claim 3

a. 3[a]

Noguchi-I discloses the “second voltage line” as initialization voltage line “Vini[n]” that may be formed in the first wiring layer. Noguchi-I, ¶68, FIG. 1 (annotated below). Vini[n] corresponds to Vint in the ’991 Patent, described as

“initialization voltage line 124.” ’991Pat., 6:25-37. Annotated Noguchi-I Figure 1 (left) below alongside ’991 Patent Figure 1 (right) show Vini[n] and Vint.

See Kanicki, ¶¶373-375.



b. 3[b]-3[d]

These limitations are shown in Noguchi-I’s Figure 1 (above).

3[b]: Noguchi’s T2 (“fifth” TFT) connects to gate electrode of T4, which is also the “first capacitor plate”. See 1[i].

3[c]: Noguchi’s T1 (“sixth” TFT) connects to Vini[n] (“one of the plurality of second voltage lines”), and to gate electrode 102 of T4 (“first capacitor plate”).

3[d]: Noguchi’s T1 (“sixth” TFT) is coupled to T2 (“fifth” TFT).

See Kanicki, ¶¶376-379.

6. Claims 4-5

Claim 4: as explained in 1[i], Noguchi-I teaches C1 having electrode 102, which operates as the gate of T4. §IV.F.3.h. Scan[n] (“the first scan line”) is in the first wiring layer. Noguchi-I, ¶68, FIG. 2. Noguchi-I further discloses gate electrode 102 is also in the first wiring layer (“same material layer”). *Id.*, ¶75, FIG. 45. Therefore, Noguchi-I’s scan lines and first capacitor plates are in the same first wiring layer.

Claim 5: Noguchi-I explains a “wiring layer is ordinarily low-resistance wiring (metal wiring)” (*id.*, ¶63), which would have made it obvious to POSITAs that the metal components, including the first capacitor plate and the first scan line, in the first wiring layer were made of the same material.

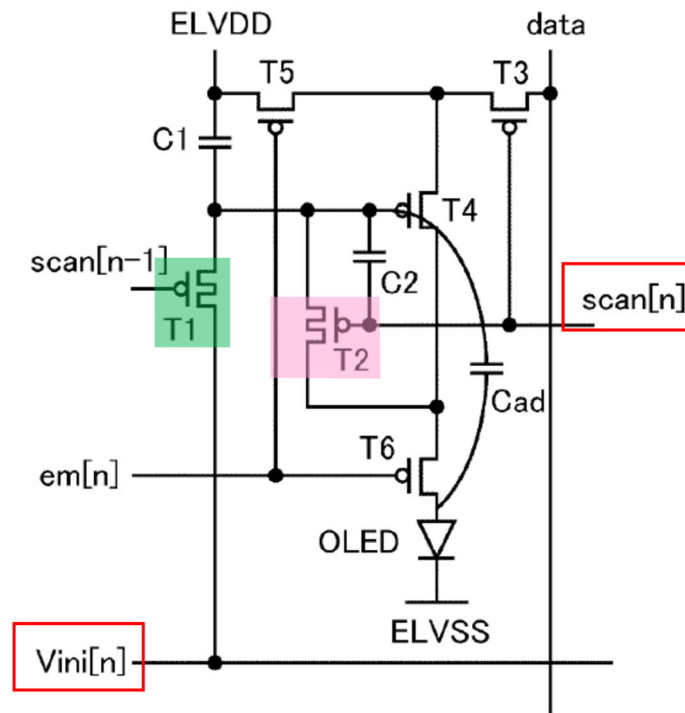
See Kanicki, ¶¶380-384.

7. Claim 6

Annotated Figure 1 below shows T2 (“fifth” TFT) connects to scan[n] (“one of the plurality of scan lines”). Noguchi-I, FIG 1. T1 (“sixth” TFT) connects to scan[n-1] (“another one of the plurality of scan lines”). *Id.*, FIG 1.

See Kanicki, ¶¶385-386.

Fig. 1



8. Claim 17

See claim 3. §IV.F.5; Kanicki, ¶388.

9. Claims 18-19

See claims 4 and 5, respectively. §IV.F.6; Kanicki, ¶389.

10. Claim 20

See claim 6. §IV.F.7; Kanicki, ¶390.

**G. Ground 2B: Claims 10-13 and 23-26 are Unpatentable over
Noguchi-I-Udagawa-Kim Combination**

1. Kim

Kim teaches contact errors in the dual-structure capacitor can be prevented by the active pattern (1) functioning as the first electrode of the first capacitor and being extended to be connected to the semiconductor layer included in the transistor connected between a power source VDD that supplies a power supply voltage and a power source Vinit that supplies an initial voltage, and (2) functioning as the first electrode of the second capacitor and being extended to be connected to the semiconductor layer included in the transistor that transmits the data voltage to the driving transistor in response to the selection signal from the current scan line. *Id.*, 5:41-6:16. Kim is analogous art to the '991 Patent because both patents are in the same field of endeavor. Both are directed to compensating for threshold voltage deviation. Kim, 1:61-63.

See Kanicki, ¶¶391-392.

2. Motivation to combine

Kim, similar to Noguchi-I, is related to OLED displays (Kim, 5:41-6:16) having drive circuits with six TFTs and two capacitors (6T2C circuits) (Noguchi-I, FIG. 1; Kim, FIG. 5), and TFTs formed on a substrate within an OLED pixel in

strikingly similar configurations. Noguchi-I, FIG. 8; Kim, FIG. 2 (reproduced below).

Fig. 8

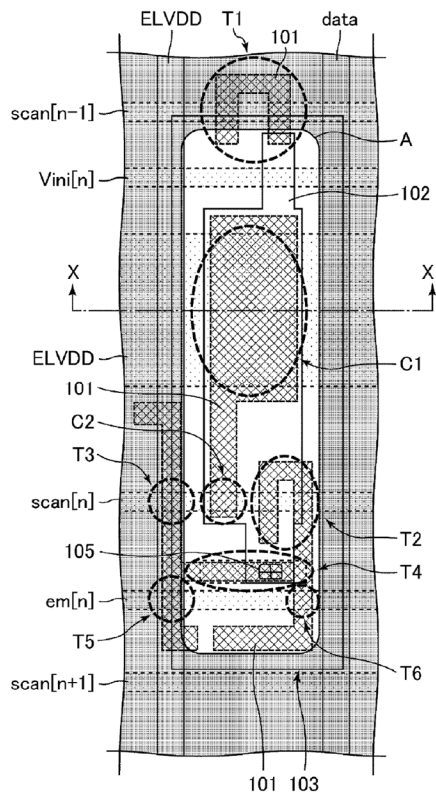
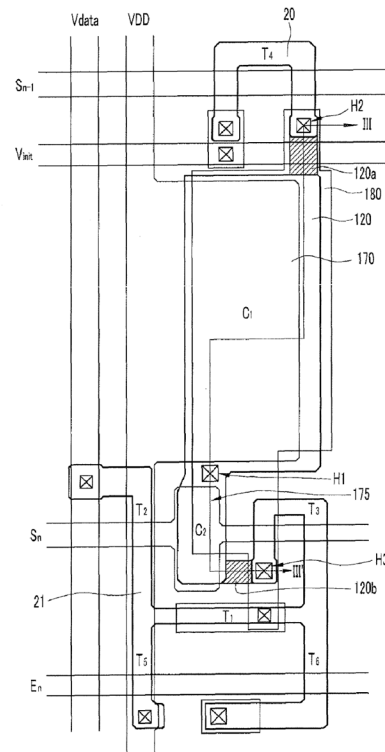


FIG. 2



Left: Noguchi-I, FIG. 8; Right: Kim, FIG. 2.

While Noguchi-I's semiconductor pattern includes discontinuities, Kim's semiconductor pattern does not. *See* Noguchi-I, FIG. 8; Kim, FIG. 2. In the Petition's combination, Noguchi-I's pixel layout is modified based on the teachings of Kim to form a contiguous semiconductor pattern. *See* §§IV.G.3-IV.G.7. POSITAs would have been motivated and found it obvious to make this modification because Kim's continuous semiconductor pattern constituted a known alternative that required less

masking to Noguchi-I's non-contiguous pattern. Furthermore, incorporating Kim's semiconductor layer structure would allow for a "dual-structure" capacitor to increase capacitance. Kim, 1:64-65, 5:42-51. Such a modification amounted to a simple design choice that involved a routine task of making minor changes to the semiconductor pattern and was well within the skill set of POSITAs.

Additionally, and as previously discussed, the Noguchi-I reference can be combined individually with each of the cited references—Udagawa, and Kim. In each instance, the combination involves modifying independent and distinct aspects of Noguchi-I. Accordingly, POSITAs would have found it obvious and would have been motivated to combine Noguchi-I with each of Udagawa and Kim, and would have had a reasonable expectation of success.

See Kanicki, ¶¶393-397.

3. Claim 10

a. 10[a]

Noguchi-I teaches this limitation as discussed in 3[a]. §IV.F.5.a; Kanicki, ¶398.

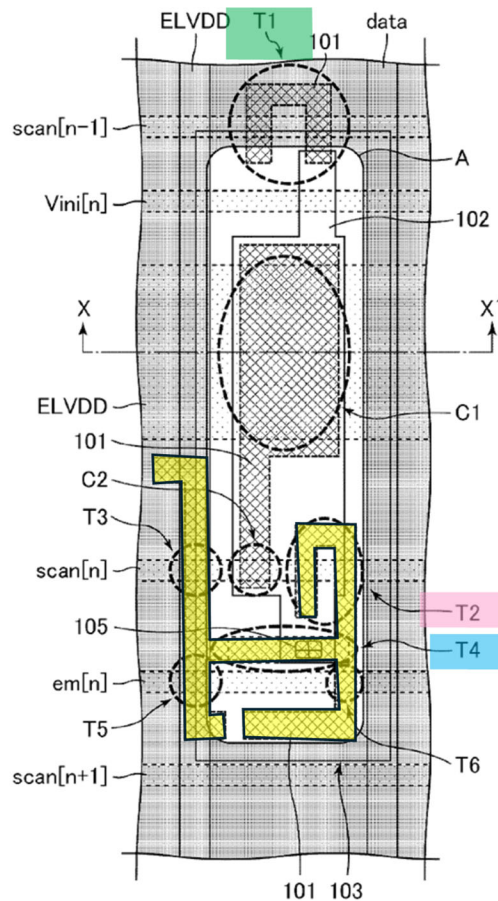
b. 10[b]

Noguchi's T2 ("fifth" TFT) is formed in a portion of the semiconductor layer on the substrate ("implemented in a fifth portion of the semiconductor layer"). §IV.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9; *see also* §IV.A.4.f.

Annotated Figure 8 below shows T2 ("fifth") and T4 ("second") TFTs are adjacent and connected together in the contiguous semiconductor layer ("the semiconductor layer couples the fifth thin film transistor to the second thin film transistor"). Having a semiconductor layer that connects or couples two TFTs was a routine aspect of pixel design and was well known at the time of the alleged invention.

See Kanicki, ¶¶399-402.

Fig. 8



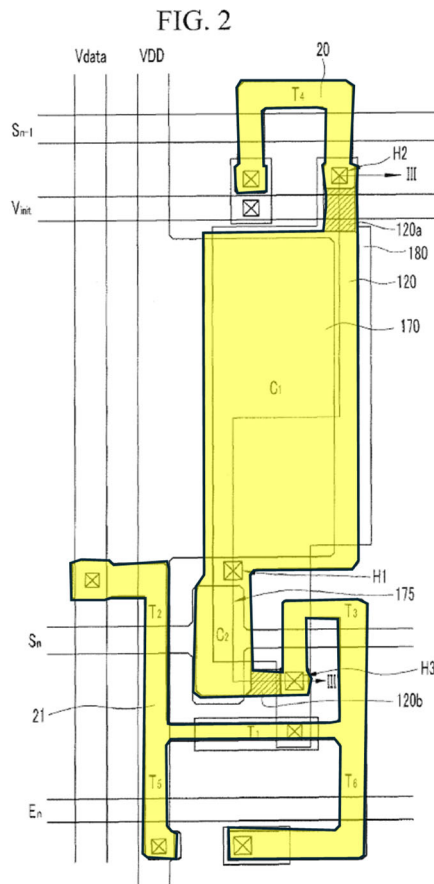
c. 10[c]-10[d]

Noguchi's T1 ("sixth" TFT) is formed in a portion of the semiconductor layer on the substrate ("implemented in a sixth portion of the semiconductor layer"). §IV.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9.

To the extent that PO argues that Noguchi-I does not teach or suggest the semiconductor layer couples the sixth TFT to the fifth TFT because of a discontinuity in the semiconductor portion that extends to T1, POSITAs would have

found it obvious to modify Noguchi-I to have a contiguous semiconductor pattern based on the teachings of Kim.

Kim describes a TFT driving circuit similar to Noguchi-I's Figure 1. *See* Kim, 7:34-8:51; FIG. 5. Kim further provides a transistor layout that is similar to Noguchi-I's Figure 8. *See* Kim, 5:12-18, FIG. 2. Kim explains that **T4 in Figure 2 is connected to T3 using semiconductor patterns 120, 120a and 120b.** Kim, 6:29-49. Annotated Figure 2 below shows an example of the semiconductor layer of Kim, showing a contiguous semiconductor pattern that extends to all TFTs.



POSITAs would have been motivated to utilize the teachings of Kim to modify Noguchi-I's semiconductor pattern to contiguously extend to TFT T1. §0.

Extending the connectivity of the semiconductor pattern based on Kim does not change any other analysis above regarding the above claims. *see* §IV.F.

See Kanicki, ¶¶403-408.

d. 10[e]

As explained in 3[c], T1 connects to Vini[n] and gate electrode 102 of T4. §IV.F.5.b.

Fig. 1

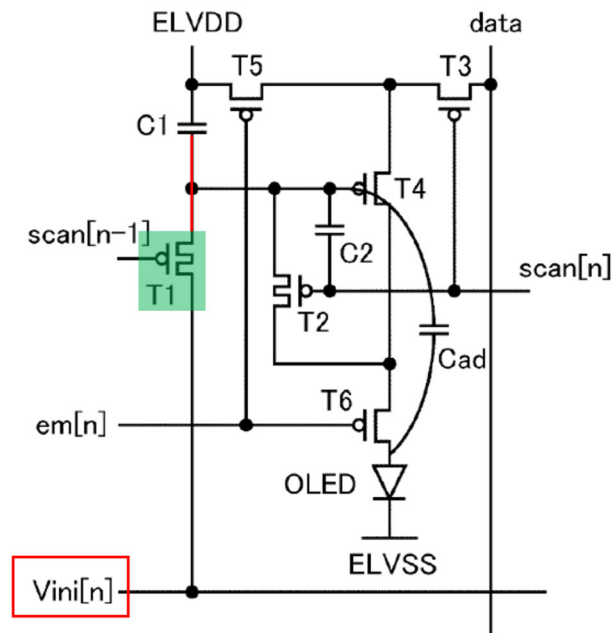


Figure 1 of Noguchi-I clearly shows the connection of T1 (“sixth” TFT) to the first capacitor plate on one side and to Vini on the other side.

As explained above in 1[l], vias (e.g., contact holes) were a well-known and common method of connecting a semiconductor layer to signal lines, such as Vini[n]. §IV.F.3.i. Thus, POSITAs would have found it obvious to implement the above connectivity by connecting the portion of the semiconductor layer of T1 (“sixth” TFT) to Vini[n] through a via because Vini resided on an upper layer (“electrically coupled...through the semiconductor layer”). POSITAs would have found it equally obvious to use a via to connect the semiconductor layer of T1 to gate electrode (“first capacitor plate”) 102 that also resided in a different layer (i.e., in the first wiring layer).

See Kanicki, ¶¶409-413.

4. Claims 11-12, 24-25

Noguchi-I teaches or suggests claims 11 and 24 for the same reasons as in claim 4 and teaches or suggests claims 12 and 25 for the same reasons as in claim 5. *See §IV.F.6; Kanicki, ¶414.*

5. Claim 13

See claim 6 discussion in §IV.F.7; Kanicki, ¶415.

6. Claim 23

See claim 10 discussion in §IV.G.3; Kanicki, ¶416.

7. Claim 26

See claim 6 discussion in §IV.F.7; Kanicki, ¶417.

H. Ground 2C: Claims 7 and 21 are Unpatentable over Noguchi-I, Udagawa, Noguchi-II, and Jeong

1. Noguchi-II

Noguchi-II describes a circuit of a pixel of an organic EL display device similar to Figure 1 of the '991 Patent and Noguchi-I (i.e., with scan lines, data lines, and six transistors) but additionally includes a transistor T7 for adjusting the OLED's pixel electrode voltage. Noguchi-II, ¶¶77, 90-91.

T7 is connected in parallel to the OLED; consequently, OLED's anode and cathode voltages may be the same. Noguchi-II, ¶91, FIG. 6. This enables discharge of charge stored in the parasitic capacitance C_{ad} through a power supply line ELVSS using transistor T7 as a path for electric current. *Id.*, ¶91. Consequently, display characteristics without any occurrences of the stepwise response characteristics can be achieved. *Id.*, ¶91.

Noguchi-II is in the same field of endeavor as the '991 Patent, and both are directed to compensating the threshold voltage of the driving transistor. Noguchi-II, ¶42. Furthermore, Noguchi-II, which shares the same inventor as Noguchi-I.

See Kanicki, ¶¶418-420.

2. Jeong

Jeong describes a circuit of a pixel similar to the circuit in Figure 1 of the '991 Patent and Noguchi-I (i.e., with scan lines, data lines, and six transistors). Jeong, Abstract. Jeong's 6T1C circuit allows the initialization power supply for supplying the initialization voltage (VINT) of the pixel to be set to the same voltage source as a power supply that supplies a low potential pixel power from the outside (ELVSS). *Id.*, ¶¶40, 52.

Jeong is in the same field of endeavor as the '991 Patent, as both are directed to compensating the threshold voltage of the driving transistor. Jeong, ¶¶85-86, 89.

See Kanicki, ¶¶421-422.

3. Motivation to combine

Noguchi-I is directed to the pixel structure susceptible to visual aberrations caused by parasitic capacitance, Cad. Noguchi-I, ¶¶12, 15, 17, 70. Noguchi-II proposes adding an additional adjusting transistor (a seventh transistor) to reduce visual aberration in the display. Noguchi-II, ¶¶77, 91.

POSITAs would have been motivated to combine the complementary teachings of Noguchi-I with Noguchi-II to reduce Cad, and specifically add Noguchi-II's seventh (adjusting) TFT to Noguchi-I's pixel driving circuit. This combination would have been obvious based on the shared objective of Noguchi-I's

and Noguchi-II's to reduce Cad, and the additional improvement gained by implementing Noguchi-II's seventh TFT.

POSITAs would have been motivated to apply a known technique (adding a seventh TFT) to a known device ready for improvement (Noguchi-I's pixel structure) to yield predictable results (the Cad being reduced). POSITAs would have had a reasonable expectation of success, because adding a seventh TFT to a 6T1C circuit to reduce parasitic capacitance was already described in Noguchi-II, and such modifications were well within the skill set of POSITAs.

POSITAs would have also combined Noguchi-I with Jeong with the understanding that Vini[n] is the same voltage source as ELVSS. Jeong, ¶¶52, 54. Setting Vini[n] to ELVSS is merely a design choice. *Id.*, ¶52 ("initialization power supply supplying...may be supplied according to the design structure of the pixel").

Furthermore, Noguchi-I can be combined individually with each of Udagawa and Noguchi-II. In each instance, the combination involves modifying a distinct aspect of Noguchi-I. POSITAs would have recognized each combination can be implemented without affecting the others. Accordingly, POSITAs would have found it obvious and would have been motivated to combine Noguchi-I with each of Udagawa and Noguchi-II and would have had a reasonable expectation of success.

See Kanicki, ¶¶423-430.

4. Claims 7, 21

Noguchi-I's driving circuit can have more than or less than six TFTs. Noguchi-I, ¶95 ("TFTs and so forth have been omitted in the figures."). As explained above, Noguchi-II discloses an OLED drive circuit similar to those described in Noguchi-I and in Figure 10 of the '991 Patent, which additionally includes a seventh TFT. **§Error! Reference source not found..** Noguchi-II's annotated Figure 6 (left) below and '991 Patent Figure 10 (right) highlight the seventh TFT.

Fig. 6

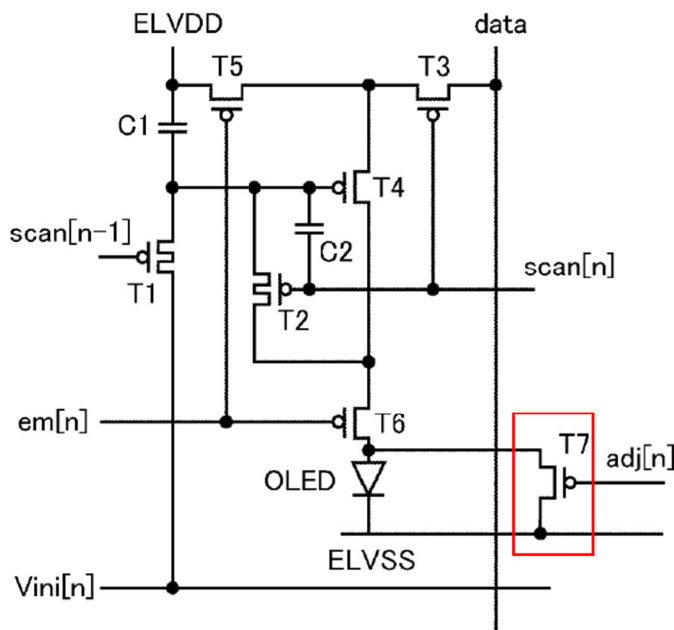
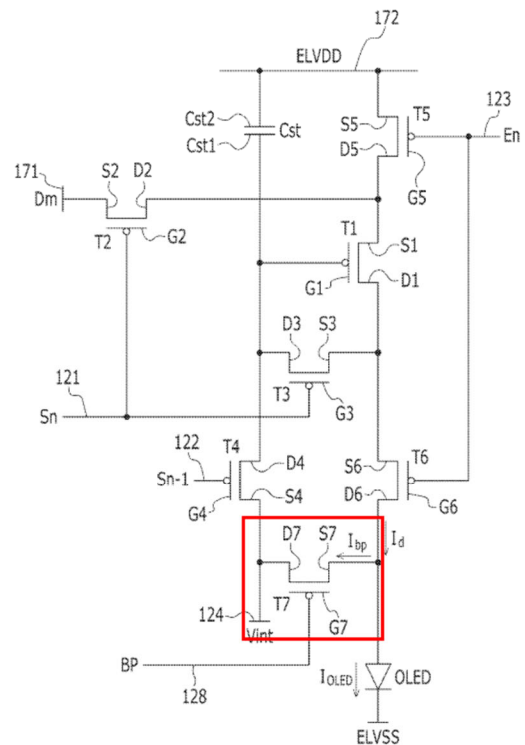


FIG. 10



As shown below, Noguchi-II's circuit (left) is nearly identical to Noguchi-I (right), except for the additional seventh TFT (T7).

Fig. 6

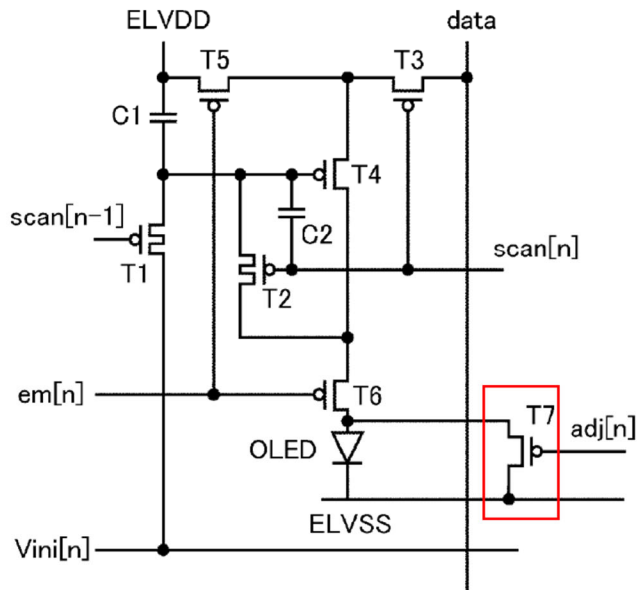
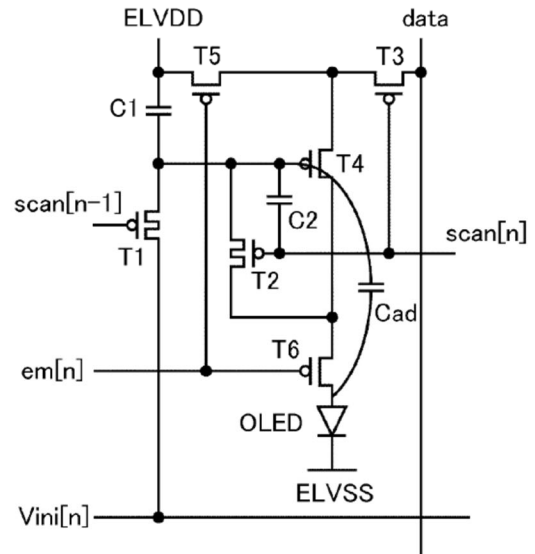


Fig. 1



T7 in Figure 6 connects (“electrically coupled”) to T6 (“fourth” TFT) and to OLED. Noguchi-II, ¶¶77, 90-91. The addition of T7 prevents “occurrence of the stepwise response characteristics” that occurs because of parasitic capacitance, *Cad*. *Id.*, ¶¶16, 91.

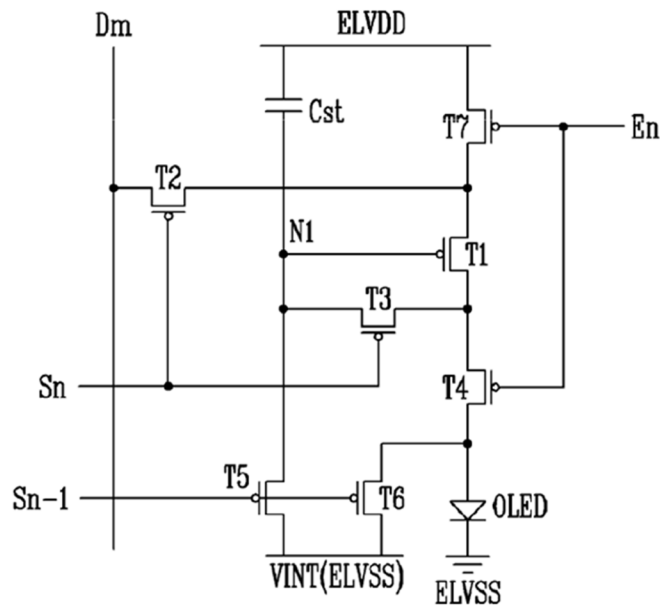
POSITAs would have been motivated to modify Noguchi-I to incorporate Noguchi-II’s seventh TFT to further reduce the effects of parasitic capacitance, *Cad*. Such a modification would have improved the performance of Noguchi-I drive circuit with minimal increase in size. Furthermore, as shown above, Noguchi-II and Noguchi-I’s circuits are identical except for the additional TFT.

While Noguchi-II shows the drain of T7 is connected to ELVSS (and the drain of T1 is connected to Vini[n]), it was well-known and obvious that the initialization

voltage $V_{ini}[n]$ and ELVSS can be the same. This is specifically shown in Jeong. Jeong, ¶¶52 (“the third power supply supplying the third power (VINT)... may be set to the same Voltage source as the second power supply supplying the second power (ELVSS).”), 54, FIG. 2. POSITAs would have thus understood that $V_{ini}[n]$ and ELVSS are the same voltage line. Thus, POSITAs would have found it obvious that in the combination T7 is connected to $V_{ini}[n]$ /ELVSS (“second voltage line”).

See Kanicki, ¶¶431-438.

FIG. 2



Jeong, FIG. 2.

I. Ground 2D: Claims 14 and 27 are Unpatentable over Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim

1. Motivation to combine

The Noguchi-I reference can be combined individually with each of the cited reference—Udagawa, Noguchi-II, Jeong, and Kim. In each instance, the combination involves modifying independent, distinct aspects of Noguchi-I. POSITAs would recognize that and each combination can be implemented without affecting the others. Accordingly, POSITAs would have found it obvious and would have been motivated to combine Noguchi-I with each of Noguchi-II, Jeong, Udagawa, and Kim, and would have had a reasonable expectation of success. Kanicki, ¶¶439-440. *See also* Motivations to combine in Grounds 2A-2C. §§IV.F.2, IV.G.2, IV.H.3.

2. Claim 14

Claim 14 is similar to claim 7, except for reciting “the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor.”

As explained in 1[h-1] and 1[l], transistors T1 to T6 utilize and include a portion of the semiconductor layer, which is thus electrically coupled to the corresponding transistor. Noguchi-I, ¶11; §§IV.F.3.f, IV.F.3.i. Moreover, as explained in Ground 2B, POSITAs would have been motivated to utilize Kim’s contiguous semiconductor layer for each of the TFTs in the drive circuit. §IV.G.

POSITAs would have understood that when adding an additional TFT, the semiconductor layer would be deposited for that new TFT because the design disclosed in the Noguchi-I combination with Kim would have been used. POSITAs would have found it obvious to continue the semiconductor layer to incorporate T7. Using a contiguous semiconductor layer would have been a natural choice and given the Noguchi-I combination's layer was contiguous. Moreover, it was one of two options (contiguous or non-contiguous). *Id.* Many possible layouts could have been realized based on Noguchi-II and Kim's teachings. Accordingly, the Noguchi-I combination teaches or suggests the semiconductor layer extended contiguously from T6 to a seventh TFT. *Id.* This is particularly so because both the seventh TFT and T6 connect to the OLED and using the same connection point would eliminate the need for connecting the TFTs using other layers of the design.

As explained for claim 7, the combination teaches the remaining limitations of claim 14. §IV.H.4.

See Kanicki, ¶¶441-445.

3. Claim 27

See claim 14 in §IV.I.2; Kanicki, ¶446.

V. CONCLUSION

IPR of the Challenged Claims is respectfully requested.

VI. MANDATORY NOTICES

A. Real Party in Interest

Petitioner identifies itself as a real party in interest. The following are identified as additional real parties in interest: Mianyang BOE Optoelectronics Technology Co., Ltd., Ordos Yuansheng Optoelectronics Co., Ltd., Chengdu BOE Optoelectronics Technology Co., Ltd., Chongqing BOE Optoelectronics Technology Co., Ltd., Wuhan BOE Optoelectronics Technology Co., Ltd., Yunnan Invensight Optoelectronics Technology Co., Ltd. f/k/a/ BMOT f/k/a Kunming BOE Display Technology, and BOE Technology America, Inc.

B. Related Matters

To the best of Petitioner's knowledge, the '991 Patent has been involved in the following matters:

- *Samsung Display Co. v. BOE Technology Group Co.*, No. 2:25-cv-00426-JRG (E.D. Tex.).

C. Notice of Counsel and Service Information

Petitioner consents to electronic service. All services and communications to the attorneys listed above may be sent to:

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D. Power of Attorney

A power of attorney is filed herewith according to 37 C.F.R. §42.10(b).

Respectfully submitted,

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Date: August 31, 2025

CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(d)

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned Petition for *inter partes* review of U.S. Patent No. 11,574,991, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,880. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of the Petition for *inter partes* review of U.S. Patent No. 11,574,991 and supporting materials (Exhibits and Power of Attorney) were served via USPS Priority Mail Express on the Patent Owner at the correspondence address of record as listed on PAIR:

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