UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

BOE TECHNOLOGY GROUP CO., LTD.,

Petitioner

v.

SAMSUNG DISPLAY CO., LTD.,

Patent Owner.

_____

IPR2025-01479

U.S. Patent No. 11,574,991

_____

DECLARATION OF DR. JERZY KANICKI IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,574,991

TABLE OF CONTENTS

I. INTRODUCTION 1
II. QUALIFICATIONS AND PROFESSIONAL EXPERIENCE 6
III. LEVEL OF ORDINARY SKILL IN THE ART 14
IV. RELEVANT LEGAL STANDARDS 15
V. SUMMARY OF THE '991 PATENT 21
A. Specification 21
B. Prosecution History 26
VI. TECHNOLOGY BACKGROUND 27
A. OLED Displays—From Inception to 2012 27
1. Two transistor (2T) and two transistor, one capacitor (2T1C) pixel circuits: 29
2. Four transistor, one capacitor (4T1C) and five transistor, one capacitor (5T1C) pixel circuits: 32
3. Six transistors, one capacitor (6T1C) and seven transistors, one capacitor (7T1C) pixel circuits: 34
B. OLED Displays—State of the Art in 2012 34
1. Six transistors, one capacitor (6T1C) Pixel Driving Circuits 35
2. Seven transistor, one capacitor (7T1C) Pixel Driving Circuit 37
3. TFTs Using Serpentine Channels 42
C. Architecture and Operation of OLED Display Pixels 43
1. Circuit Diagrams 44
2. Plan Views 45
3. Cross-Sectional Views 49
VII. CLAIM CONSTRUCTION 51

VIII. CLAIMS 1-30 ARE UNPATENTABLE 52

A. Ground 1A: Claims 1-6, 8-13, 15-20, 22-26, 28-30 are Unpatentable over Liu and Udagawa 52

1. Summary of Liu 52

2. Summary of Udagawa 55

3. Motivation to combine Liu and Udagawa 56

4. Independent Claim 1 57

5. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 89

6. Claim 3 91

7. Claim 4: "An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 5: "An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 94

8. Claim 6: "An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 95

9. Claim 8: "an organic light emitting diode display according to claim 4, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer." 96

10. Claim 9: "An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate." 101

11. Claim 10 107

12. Claim 11: "An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 12: "An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 110

13. Claim 13: "An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 111

14. Claim 15: An organic light emitting diode display according to claim 11, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer. 111

15. Claim 16: "An organic light emitting diode display according to claim 1, wherein a periphery of the first capacitor plate completely surrounds a periphery of the second capacitor plate in a plan view." 111

16. Claim 17 113

17. Claim 18: "An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 19: "An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 113

18. Claim 20: "An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 113

19. Claim 22: An organic light emitting diode display according to claim 18, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer. 114

20. Claim 23 114

21. Claim 24: "An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 25: "An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 115

22. Claim 26: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 115

23. Claim 28: An organic light emitting diode display according to claim 24, wherein the plurality of scan

lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer. 115

24. Claim 29: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate." 116

25. Claim 30: "An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 116

B. Ground 1B: Claims 2-6 and 10-13 are Unpatentable over the Combination of Liu, Udagawa, and Nakayama 116

1. Summary of Nakayama 116

2. Motivation to combine Liu, Udagawa, and Nakayama 117

3. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 119

4. Claim 3-6, and 10-13 123

C. Ground 1C: Claims 7, 14, 21, and 27 are Unpatentable over Liu, Udagawa, and Chung 123

1. Summary of Chung 123

2. Motivation to combine Liu, Udagawa, and Chung 124

3. Claim 7: "An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor." 126

4. Claim 14 130

5. Claim 21: "An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor." 131

6. Claim 27 132

D. Ground 1D: Claims 7 and 14 are Unpatentable over Liu, Udagawa, Chung, and Nakayama 132

1. Motivation to combine Liu, Udagawa, Chung, and Nakayama 132

2. Claims 7 and 14 133

E. Ground 1E: Claims 9, 29, and 30 are Unpatentable over Liu in combination with Udagawa and Murade 134

1. Summary of Murade, and Motivation to Combine Liu and Murade 134

2. Claim 9: "An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate." 137

3. Claim 29: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate

through a contact hole that passes through the second capacitor plate." 138

4. Claim 30: "An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 139

F. Ground 2A: Claims 1-6, and 17-20 are Unpatentable over Noguchi-I and Udagawa.....139

1. Summary of Noguchi-I 139

2. Motivation to combine Noguchi-I and Udagawa 140

3. Independent Claim 1 142

4. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 168

5. Claim 3 170

6. Claim 4: "An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 5: "An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 172

7. Claim 6: "An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 173

8. Claim 17 174

9. Claim 18: "An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 19: "An organic light

emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 174

10. Claim 20: "An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 175

G. Ground 2B: Claims 10-13 and 23-26 are Unpatentable over the Combination of Noguchi-I, Udagawa, and Kim 175

1. Summary of Kim 175

2. Motivation to combine Noguchi-I, Udagawa, and Kim 176

3. Claim 10 178

4. Claim 11: "An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 12: "An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." Claim 24: "An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 25: "An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 184

5. Claim 13: "An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 185

6. Claim 23 185

7. Claim 26: "An organic light emitting diode display according to claim 24, wherein the fifth thin film

transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 186

H. Ground 2C: claims 7 and 21 are Unpatentable over Noguchi-I, Udagawa, Noguchi-II, and Jeong 186

1. Summary of Noguchi-II 186

2. Summary of Jeong 187

3. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, and Jeong 188

4. Claim 7: "An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor." Claim 21: "An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor." 190

I. Ground 2D: Claims 14 and 27 are Unpatentable over the Combination of Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim 195

1. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim 195

2. Claim 14 196

3. Claim 27 198

IX. CONCLUSION 198

I. INTRODUCTION 1

II. QUALIFICATIONS AND PROFESSIONAL EXPERIENCE 6

III. LEVEL OF ORDINARY SKILL IN THE ART 14
IV. RELEVANT LEGAL STANDARDS 15
V. SUMMARY OF THE '991 PATENT 21
A. Specification 21
B. Prosecution History 26
VI. TECHNOLOGY BACKGROUND 27
A. OLED Displays—From Inception to 2012 27
1. Two transistor (2T) and two transistor, one capacitor (2T1C) pixel circuits: 29
2. Four transistor, one capacitor (4T1C) and five transistor, one capacitor (5T1C) pixel circuits: 32
3. Six transistors, one capacitor (6T1C) and seven transistors, one capacitor (7T1C) pixel circuits: 34
B. OLED Displays—State of the Art in 2012 34
1. Six transistors, one capacitor (6T1C) Pixel Driving Circuits 35
2. Seven transistor, one capacitor (7T1C) Pixel Driving Circuit 37
3. TFTs Using Serpentine Channels 42
C. Architecture and Operation of OLED Display Pixels 43
1. Circuit Diagrams 44
2. Plan Views 45
3. Cross-Sectional Views 49
VII. CLAIM CONSTRUCTION 51
VIII. CLAIMS 1-30 ARE UNPATENTABLE 52
A. Ground 1A: Claims 1-6, 8-13, 15-20, 22-26, 28-30 are Unpatentable over Liu and Udagawa 52
1. Summary of Liu 52
2. Summary of Udagawa 55

3. Motivation to combine Liu and Udagawa 56
4. Independent Claim 1 57
5. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 89
6. Claim 3 91
7. Claim 4: "An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 5: "An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 94
8. Claim 6: "An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 95
9. Claim 8: "an organic light emitting diode display according to claim 4, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer." 96
10. Claim 9: "An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate." 101

11. Claim 10 107

12. Claim 11: "An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 12: "An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 110

13. Claim 13: "An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 111

14. Claim 15: An organic light emitting diode display according to claim 11, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer. 111

15. Claim 16: "An organic light emitting diode display according to claim 1, wherein a periphery of the first capacitor plate completely surrounds a periphery of the second capacitor plate in a plan view." 111

16. Claim 17 113

17. Claim 18: "An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 19: "An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 113

18. Claim 20: “An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.” 113

19. Claim 22: An organic light emitting diode display according to claim 18, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer. 114

20. Claim 23 114

21. Claim 24: “An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.” Claim 25: “An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.” 115

22. Claim 26: “An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.” 115

23. Claim 28: An organic light emitting diode display according to claim 24, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second

capacitor plate is disposed in the second metal layer. 115

24. Claim 29: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate." 116

25. Claim 30: "An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 116

B. Ground 1B: Claims 2-6 and 10-13 are Unpatentable over the Combination of Liu, Udagawa, and Nakayama 116

1. Summary of Nakayama 116

2. Motivation to combine Liu, Udagawa, and Nakayama 117

3. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 119

4. Claim 3-6, and 10-13 123

C. Ground 1C: Claims 7, 14, 21, and 27 are Unpatentable over Liu, Udagawa, and Chung 123

1. Summary of Chung 123

2. Motivation to combine Liu, Udagawa, and Chung 124

3. Claim 7: "An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor." 126

4. Claim 14 130

5. Claim 21: "An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor." 131

6. Claim 27 132

D. Ground 1D: Claims 7 and 14 are Unpatentable over Liu, Udagawa, Chung, and Nakayama 132

1. Motivation to combine Liu, Udagawa, Chung, and Nakayama 132

2. Claims 7 and 14 133

E. Ground 1E: Claims 9, 29, and 30 are Unpatentable over Liu in combination with Udagawa and Murade 134

1. Summary of Murade, and Motivation to Combine Liu and Murade 134

2. Claim 9: "An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate." 137

3. Claim 29: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate." 138

4. Claim 30: "An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 139

F. Ground 2A: Claims 1-6, and 17-20 are Unpatentable over Noguchi-I and Udagawa 139

1. Summary of Noguchi-I 139

2. Motivation to combine Noguchi-I and Udagawa 140

3. Independent Claim 1 142

4. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view." 168

5. Claim 3 170

6. Claim 4: "An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 5: "An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 172

7. Claim 6: "An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 173

8. Claim 17 174

9. Claim 18: "An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 19: "An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 174

10. Claim 20: "An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan

lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 175

G. Ground 2B: Claims 10-13 and 23-26 are Unpatentable over the Combination of Noguchi-I, Udagawa, and Kim 175

1. Summary of Kim 175

2. Motivation to combine Noguchi-I, Udagawa, and Kim 176

3. Claim 10 178

4. Claim 11: "An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 12: "An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." Claim 24: "An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer." Claim 25: "An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material." 184

5. Claim 13: "An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 185

6. Claim 23 185

7. Claim 26: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines." 186

H. Ground 2C: claims 7 and 21 are Unpatentable over Noguchi-I, Udagawa, Noguchi-II, and Jeong 186

1. Summary of Noguchi-II 186
2. Summary of Jeong 187
3. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, and Jeong 188
4. Claim 7: "An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor." Claim 21: "An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor." 190

I. Ground 2D: Claims 14 and 27 are Unpatentable over the Combination of Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim 195
1. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim 195
2. Claim 14 196
3. Claim 27 198

IX. CONCLUSION 198

EXHIBIT LIST

No.	Exhibit
1001	U.S. Patent No. 11,574,991 ("'991 Patent" or "'991Pat.")
1002	File History of the '991 patent ("'991FH")
1003	Declaration of Jerzy Kanicki, Ph.D.
1004	Curriculum Vitae of Jerzy Kanicki, Ph.D.
1005	U.S. Pat. Pub. No. 2012/0313100 ("Liu")
1006	U.S. Pat. Pub. No. 2003/0089905 ("Udagawa")
1007	Japanese Pat. Pub. No. 2003-167533 ("Nakayama")
1008	U.S. Pat. Pub. No. 2008/0150846 ("Chung")
1009	U.S. Pat. Pub. No. 2012/0001893 ("Jeong")
1010	U.S. Pat. Pub. No. 2012/0199854 ("Noguchi-I")
1011	Japanese Pat. Pub. No. 2008-008942 ("Murade")
1012	U.S. Pat. Pub. No. 2012/0127220 ("Noguchi-II")
1013	U.S. Pat. No. 7,626,199 ("Kim")
1014	*Samsung Display Co. v. BOE Technology Group Co.*, No. 2:25-cv-00426-JRG (E.D. Tex.), Dkt. No. 1, Complaint
1015	Definition of "periphery": The American Heritage Dictionary, 2d ed. (1991)
1016	Definition of "periphery": Concise Oxford English Dictionary, 11th ed. (2009)
1017	K.C. Park, *Pixel Circuits for OLED Displays* in ***Advanced Display Technology***, Series in Display Science and Technology, I. B. Kang et al. (eds.), Springer Nature Singapore Pte Ltd. 2021 ("Park")

No.	Exhibit
1018	R. M. A. Dawson et al., *Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display* in 1998 SID Symp. Digest of Tech Papers, 1998 ("Dawson")
1019	S. M. Choi et al., *A Self-Compensated Voltage Programming Pixel Structure for Active-Matrix Organic Light-Emitting Diodes* in Proceedings of International Display Workshops (IDW), pp. 535-538, 2003 ("Choi")
1020	A. Bernanose, *Electroluminescence of Organic Compounds* in British Journal of Applied Physics 6, pp. S54-S56, 1955 ("Bernanose")
1021	H. Kallmann et al., *Bulk Conductivity in Organic Crystals* in Nature 4718, pp. 31-33, 1960 ("Kallmann")
1022	M. Pope, Autoionization in Anthracene in The Journal of Chemical Physics 47, 2197–2198, 1967 ("Pope")
1023	M. Sano et al., Electroluminescence and Band Gap in Anthracene in The Journal of Chemical Physics 43, 2920–2921, 1965 ("Sano")
1024	P.S. Vincett et al., *Electrical Conduction and Low Voltage Blue Electroluminescence in Vacuum-Deposited Organic Films* in Thin Solid Films 94, 171-183, 1982 ("Vincett")
1025	C.W. Tang and S.A. VanSlyke, *Organic Electroluminescent Diodes* in Applied Physics Letters 51, 913-915, 1987 ("Tang")
1026	J.H. Burroughes et al., *Light-Emitting Diodes Based on Conjugated Polymers* in Nature 347, 539-541, 1990 ("Burroughes")
1027	M.A. Baldo et al., *Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices* in Nature 395, 151-154, 1998 ("Baldo")
1028	U.S. Pat. Pub. No. 2003/0129790 ("Yamazaki")

No.	Exhibit
1029	Min et al., *Electrical Characteristics of New LDD Poly-Si TFT Structure Tolerant to Process Misalignment* in IEEE Electron Device Letters, 20(7), 1999 ("Min")
1030	Lee et al., *Asymmetric Electrical Properties of Fork a-Si:H Thin-Film Transistor and Its Application to Flat Panel Displays* in Journal of Applied Physics, 105, 2009 ("Lee-2009")
1031	Kim et al., *40 Inch FHD AM-OLED Display with IR Drop Compensation Pixel Circuit* in 2009 SID Symp. Digest of Tech Papers, 2009 ("Kim-2009")
1032	Lee et al., *A Novel LTPS TFT Pixel Circuit for Compensating IR Drop of Large Area AMOLED Display* in The Electrochemical Society (ECS) Transactions, 50(8), pp. 269-275, 2012 ("Lee-2012")
1033	N. H. E. Weste et al., *CMOS VLSI Design: A Circuits and Systems Perspective*, Fourth Edition, Addison-Wesley, 2011 ("Weste")
1034	U.S. Pat. Pub. No. 2003/0141811 ("Park '811")
1035	U.S. Pat. No. 9,461,102 ("Ono")
1036	U.S. Pat. Pub. No. 2012/0211750 ("Kakinuma")
1037	U.S. Pat. Pub. No. 2006/0256502 ("Li")

LISTING OF CHALLENGED CLAIMS

11,574,991
Claim 1
1[pre] An organic light emitting diode display comprising:
1[a] a non-conductive substrate;
1[b] a plurality of first voltage lines;
1[c] a plurality of scan lines;
1[d] a plurality of data lines;
1[e] a plurality of driving circuits formed on the substrate;
1[f] a plurality of organic light emitting diodes, wherein each of the plurality of organic light emitting diodes is electrically coupled to a respective one of the plurality of driving circuits;
1[g] wherein each of the driving circuits comprises: a first thin film transistor implemented in a first portion of a semiconductor layer disposed on the substrate, and coupled to one of the plurality of scan lines and to one of the plurality of data lines;
1[h-1] a second thin film transistor implemented in a second portion of the semiconductor layer, wherein the semiconductor layer couples the second thin film transistor to the first thin film transistor, and
1[h-2] wherein the second portion of the semiconductor layer has at least one bent portion;
1[i] a storage capacitor comprising: a first capacitor plate that is configured to operate as a gate electrode of the second thin film transistor;
1[j] a second capacitor plate electrically coupled to one of the plurality of first voltage lines and overlapping the first capacitor plate; and

1[k] an insulating layer between the first capacitor plate and the second capacitor plate;
1[l] a third thin film transistor implemented in a third portion of the semiconductor layer, wherein the semiconductor layer couples the third thin film transistor to the first thin film transistor and to the second thin film transistor, and wherein the third thin film transistor is electrically coupled to one of the plurality of first voltage lines through the semiconductor layer; and
1[m] a fourth thin film transistor implemented in a fourth portion of the semiconductor layer, wherein the semiconductor layer couples the fourth thin film transistor to the second thin film transistor, and wherein the fourth thin film transistor is electrically coupled to the respective organic light emitting diode through the semiconductor layer; and
1[n] wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate.
Claim 2
2 An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.
Claim 3
3[a] An organic light emitting diode display according to claim 2, further comprising: a plurality of second voltage lines;
3[b] a fifth thin film transistor electrically coupled to the first capacitor plate; and
3[c] a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,
3[d] wherein the sixth thin film transistor is coupled to the fifth thin film transistor.
Claim 4
4. An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.

Claim 5
5. An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.
Claim 6
6. An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.
Claim 7
7. An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor.
Claim 8
8 An organic light emitting diode display according to claim 4, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.
Claim 9
9. An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.
Claim 10
10[a] An organic light emitting diode display according to claim 2, further comprising: a plurality of second voltage lines;

10[b] a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and
10[c] a sixth thin film transistor implemented in a sixth portion of the semiconductor layer,
10[d] wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and
10[e] wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.
Claim 11
11. An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.
Claim 12
12. An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.
Claim 13
13. An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.
Claim 14
14[pre] An organic light emitting diode display according to claim 11, further comprising a seventh thin film transistor implemented in the sixth portion of the semiconductor layer,
14[a] wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

14[b] wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.
Claim 15
15[pre] An organic light emitting diode display according to claim 11, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.
Claim 16
16. An organic light emitting diode display according to claim 1, wherein a periphery of the first capacitor plate completely surrounds a periphery of the second capacitor plate in a plan view.
Claim 17
17[pre] An organic light emitting diode display according to claim 1, further comprising:
17[a] a plurality of second voltage lines;
17[b] a fifth thin film transistor electrically coupled to the first capacitor plate; and
17[c] a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,
17[d] wherein the sixth thin film transistor is coupled to the fifth thin film transistor.
Claim 18
18. An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.
Claim 19

19. An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.
Claim 20
20. An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.
Claim 21
21. An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor.
Claim 22
22[pre] An organic light emitting diode display according to claim 18, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.
Claim 23
23[pre] An organic light emitting diode display according to claim 1, further comprising:
23[a] a plurality of second voltage lines;
23[b] a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and
23[c] a sixth thin film transistor implemented in a sixth portion of the semiconductor layer, wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and wherein the sixth thin film

transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.
Claim 24
24. An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer.
Claim 25
25. An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material.
Claim 26
26. An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines.
Claim 27
27[pre] An organic light emitting diode display according to claim 24, further comprising a seventh thin film transistor implemented in the sixth portion of the semiconductor layer,
27[a] wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and
27[b] wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.
Claim 28
28[pre] An organic light emitting diode display according to claim 24, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

Claim 29
29. An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.
Claim 30
30. An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view.

I, Jerzy Kanicki, do hereby declare as follows:

I. INTRODUCTION

1. My name is Jerzy Kanicki, and I have been retained by counsel for Petitioner ("Petitioner" or "BOE") as an expert witness to provide my opinion regarding certain prior art references and U.S. Patent No. 11,574,991 (the "'991 patent").

2. I make this declaration based upon my own personal knowledge and, if called upon to testify, will testify competently to the matters stated herein.

3. I have been asked to provide my expert opinion in connection with the *Inter Partes* Review of the '991 Patent to Kim *et al*. concerning whether it is unpatentable over certain prior art. This declaration is a statement of my opinions on issues relating to the patentability of claims 1-30 (the "Challenged Claims") of the '991 Patent. As I explain more fully below, it is my opinion that all of the Challenged Claims would have been obvious to a person of ordinary skill in the art ("POSITA") at the time of the alleged invention.

4. I am being compensated for my work in this matter at my standard hourly rate. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

5. I have reviewed and considered the following documents in connection

with my analysis of the ’991 Patent:

- EX1001: U.S. Patent No. 11,574,991 (“’991 Patent” or “’991Pat.”)
- EX1002: File History of the ’991 Patent (“’991FH”)
- EX1005: U.S. Pat. Pub. No. 2012/0313100 (“Liu”)
- EX1006: U.S. Pat. Pub. No. 2003/0089905 (“Udagawa”)
- EX1007: Japanese Pat. Pub. No. 2003-167533 (“Nakayama”)
- EX1008: U.S. Pat. Pub. No. 2008/0150846 (“Chung”)
- EX1009: U.S. Pat. Pub. No. 2012/0001893 (“Jeong”)
- EX1010: U.S. Pat. Pub. No. 2012/0199854 (“Noguchi-I”)
- EX1011: Japanese Pat. Pub. No. 2008-008942 (“Murade”)
- EX1012: U.S. Pat. Pub. No. 2012/0127220 (Noguchi-II”)
- EX1013: U.S. Pat. No. 7,626,199 (“Kim”)
- EX1015: Definition of “periphery”: The American Heritage Dictionary, 2d ed. (1991)
- EX1016: Definition of “periphery”: Concise Oxford English Dictionary, 11th ed. (2009)
- EX1017: K.C. Park, Pixel Circuits for OLED Displays in Advanced Display Technology, Series in Display Science and Technology, I. B. Kang et al. (eds.), Springer Nature Singapore Pte Ltd. 2021 (“Park”)

- EX1018: R. M. A. Dawson et al., Design of an Improved Pixel for a Polysilicon Active-Matrix Organic LED Display in 1998 SID Symp. Digest of Tech Papers, 1998 ("Dawson")
- EX1019: S. M. Choi et al., A Self-Compensated Voltage Programming Pixel Structure for Active-Matrix Organic Light-Emitting Diodes in Proceedings of International Display Workshops (IDW), pp. 535-538, 2003 ("Choi")
- EX1020: A. Bernanose, Electroluminescence of Organic Compounds in British Journal of Applied Physics 6, pp. S54-S56, 1955 ("Bernanose")
- EX1021: H. Kallmann et al., Bulk Conductivity in Organic Crystals in Nature 4718, pp. 31-33, 1960 ("Kallmann")
- EX1022: M. Pope, Autoionization in Anthracene in The Journal of Chemical Physics 47, 2197–2198, 1967 ("Pope")
- EX1023: M. Sano et al., Electroluminescence and Band Gap in Anthracene in The Journal of Chemical Physics 43, 2920–2921, 1965 ("Sano")
- EX1024: P.S. Vincett et al., Electrical Conduction and Low Voltage Blue Electroluminescence in Vacuum-Deposited Organic Films in Thin Solid Films 94, 171-183, 1982 ("Vincett")

- EX1025: C.W. Tang and S.A. VanSlyke, Organic Electroluminescent Diodes in Applied Physics Letters 51, 913-915, 1987 ("Tang")
- EX1026: J.H. Burroughes et al., Light-Emitting Diodes Based on Conjugated Polymers in Nature 347, 539-541, 1990 ("Burroughes")
- EX1027: M.A. Baldo et al., Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices in Nature 395, 151-154, 1998 ("Baldo")
- EX1028: U.S. Pat. Pub. No. 2003/0129790 ("Yamazaki")
- EX1029: Min et al., Electrical Characteristics of New LDD Poly-Si TFT Structure Tolerant to Process Misalignment in IEEE Electron Device Letters, 20(7), 1999 ("Min")
- EX1030: Lee et al., Asymmetric Electrical Properties of Fork a-Si:H Thin-Film Transistor and Its Application to Flat Panel Displays in Journal of Applied Physics, 105, 2009 ("Lee-2009")
- EX1031: Kim et al., 40 Inch FHD AM-OLED Display with IR Drop Compensation Pixel Circuit in 2009 SID Symp. Digest of Tech Papers, 2009 ("Kim-2009")
- EX1032: Lee et al., A Novel LTPS TFT Pixel Circuit for Compensating IR Drop of Large Area AMOLED Display in The Electrochemical

Society (ECS) Transactions, 50(8), pp. 269-275, 2012 ("Lee-2012")

- EX1033: N. H. E. Weste et al., CMOS VLSI Design: A Circuits and Systems Perspective, Fourth Edition, Addison-Wesley, 2011 ("Weste")
- EX1034: U.S. Pat. Pub. No. 2003/0141811 ("Park '811")
- EX1035: U.S. Pat. No. 9,461,102 ("Ono")
- EX1036: U.S. Pat. Pub. No. 2012/0211750 ("Kakinuma")
- EX1037: U.S. Pat. Pub. No. 2006/0256502 ("Li")

6. In forming the opinions expressed below, I have considered:

- the documents listed above;
- the relevant legal standards as explained to me by the Petitioner's counsel, including the standard for obviousness, and any additional authoritative documents as cited in the body of this declaration;
- my own knowledge and experience based upon my work in the field of flat panel display as described below; and
- any other documents not listed above but cited below.

7. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further, I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

8. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

9. Unless otherwise noted, all emphasis in any quoted material has been added.

II. QUALIFICATIONS AND PROFESSIONAL EXPERIENCE

10. I have studied, taught, and practiced in the field of flat panel displays (FPDs) and integrated circuits (ICs) fabrication for over 25 years, including design, thin film depositions, processing, fabrication, and photolithography of devices and circuits used in both applications. The flat panel displays include, for example, active-matrix liquid crystal displays, (AM-LCDs), active-matrix organic light emitting displays (AM-OLEDs) and other light transmissive, reflective and emitting display technologies. I received my Doctorate of Science (D.Sc.) from the Free University of Brussels, Belgium in 1982. My educational background also includes a B.S. (1976) and M.S. (1978) in Chemistry from the Free University of Brussels, Belgium.

11. From 1983 to 1995, I was a Research Staff Member at the IBM T.J. Watson Research Center in Yorktown Heights, New York, involved in the research

and development of flat panel display materials, devices, circuits, driving electronics, and manufacturing methods. During that period, I was a member of a team that developed the first IBM active-matrix liquid-crystal displays (AM-LCDs) manufacturing technology, leading to the introduction of the first color laptop computer (CL57-SX) on March 24, 1992. I, among others, was also responsible at IBM for the initial fundamental understanding of device physics and pixel design approaches used for, and manufacturing methods of, certain AM-LCDs for IBM's ThinkPad laptop computers.

12. Since 1995, I have been a member of the faculty at the University of Michigan College of Engineering, Ann Arbor, Michigan. During that period, I have held the position of Professor in the Department of Electrical Engineering and Computer Science (EECS). Between 1995 and 1999, I was group team leader within the University of Michigan Center of Display Technology and Manufacturing. For number of years, I also held the position of Professor in the Program of Macromolecular Science and Engineering (2000-2011) and Applied Physics. During my tenure at the University of Michigan, I have conducted leading work on various flat panel displays, device and circuit fabrication technologies, including, for example, design for various devices and integrated circuits to be used with flat-panel displays (active-matrix arrays, data and gate drivers chips, and associated electronics), x-ray and optical imagers (pixel circuits, driving and readout chips, and

associated electronics), chemical sensors (readout chips), solar cells (DC/AC converters), and fingerprint sensors (driving circuits and readout chips). As a faculty member, over the years I have graduated a number of PhD dissertations in the field of flat panel displays, semiconductor devices and circuits. Upon graduation, my PhD graduate students have moved either into industrial positions in the displays and electronics industries or into academic positions in the U.S. or abroad.

13. I have taught a number of different courses at the undergraduate and graduate levels, including "Solid-State Technology Laboratory" and "Digital Integrated Circuit Technologies", within the EECS department at the University of Michigan. These courses have generally covered the physics, technology, design, and fabrication of solid-state devices and integrated circuits. I have also introduced two new courses, including "Flat Panel Displays" and "Thin Film Devices Technology" in 1997, which are still being offered annually. These courses have generally covered the thin-film devices and circuits technologies used in different display technologies including AM-OLEDs. As a faculty member, I direct at any given time the research of several graduate and undergraduate students in Solid-State Devices and Nanotechnology, including semiconductors, electronic materials, devices, and circuits for various applications including FPDs. As part of my group research, I utilize the University of Michigan Lurie Nanofabrication Facility (LNF), https://lnf.umich.edu/, that among others has the capability to fabricate and test

devices and circuits used in the FPDs and IC industries. Moreover, over the years I have also supervised the research of several post-doctoral fellows and visiting scientists from industry or/and other universities within my group doing research in the area of solid-state devices and circuits. More information about my professional activities can be found on my research group web page: www.eecs.umich.edu/omelab/.

14. From 2002 to 2003, I was on sabbatical at the University of California Santa Barbara (UCSB) within the Center for Polymers and Organic Solids. My research was related to organic polymer thin-film transistors, organic light-emitting devices and electrically injected lasers. My host was Professor Alan J. Heeger from Physics Department. He won the Nobel Prize for Chemistry in 2000 along with Alan G. MacDiarmid and Hideki Shirakawa "for their discovery and development of conductive polymers."

15. From 2009 to 2010, I was on sabbatical at the University of California Sand Diego (UCSD) within the California Institute for Telecommunications and Information Technology. My research was related to organic polymer thin-film transistor chemical sensors, amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs), image sensors and solar cells. My host was Professor Andrew C. Kummel from the Department of Chemistry and Biochemistry.

16. From 2018 to 2019, I was on sabbatical at the Massachusetts Institute

of Technology within Microsystems Technology Laboratories. My research was related to hydrogenated diamond devices and circuits, and Perovskites materials based opto-electronic devices. My host was Professor Jesus del Alamo from Department of Electrical Engineering and Computer Science.

17. From 2024 to 2025, I was on sabbatical at the Massachusetts Institute of Technology within Research Laboratory of Electronics (RTL). My research was related to pixel driving circuits for micro – LEDs and micro-LEDs fabrication and integration with the backplane electronics based on CMOS, low temperature polycrystalline silicon thin film transistors (poly-Si TFTs) or amorphous InGaZnO (a-IGZO) TFTs. My host was Professor Jeehwan Kim of the Department Materials Science and Engineering and Mechanical Engineering, respectively.

18. I am a member of several professional organizations including the Society for Information Display (SID) and the Institute of Electrical and Electronics Engineers (IEEE). My areas of expertise include chemistry, solid-state physics, material sciences, device physics, circuits, solid-state device and circuit fabrication / manufacturing methods, and nanotechnology. I have edited or co-edited several books, authored over 300 technical papers, and given over 350 presentations (among which over 70 were invited presentations) relating to thin film semiconductor devices, circuits, and associated FPD technologies. My papers have received over 12,000 citations, and I have an H-index of 60, i10-index of 204, RG score of 42.30

and D-index of 51. I was included in World Best Scientist 2025 and ranked 886 in the US and 2316 in the world, respectively. To be ranked you must meet the D-index inclusive threshold typically between 30–70 depending on discipline. I have also been the chair or co-chair at numerous national and international FPD conferences and symposia. I was an editor for IEEE Transactions on Electron Devices for eight years, and I am a reviewer for several prestigious international archival journals. I am also a reviewer of proposals for several federal agencies, such as the National Science Foundation (NSF), Department of Defense (DoD), and Defense Advanced Research Program Agency (DARPA). Among other distinctions, I was awarded the IBM External Honors, which recognizes the technical leadership of staff members in IBM's Research Division, three times. My research work at the University of Michigan has been supported by grants from the state of Michigan, federal agencies, and a number of international industries.

19. Through my experience and education, I am familiar with most aspects of the manufacturing processes and circuits used in the flat panel displays and integrated circuits industries, including thin film deposition, etching chemistry, chemical mechanical polishing, devices and circuits processing, and photolithography, as they relate to device and circuit fabrication, applications and/or operations. My latest curriculum vitae, and a list of my publications and presentations, is appended as EX1004.

20. In the previous five years (2019 – 2024), I have testified as an expert at trial or by deposition or have submitted declarations in the following cases:

- 2023: Dispute related to AM-OLEDs between Samsung Display Co., Ltd. and AU Optronics Corp.: Perkins Coie LLP (Consultant for AUO).
- 2023: Case related to U.S. ITC Investigation No. 337-TA-1351. "Certain Active-Matrix Organic Light Emitting Diode Display Panels and Modules For Mobile Devices, and Components Thereof." Adverse party in this action is Samsung Display Co Ltd.: Morrison & Foerster LLP (Consultant for Apple Inc.)
- 2021: Advanced Silicon Group Technologies, LLC v. Boviet Solar Technology Co., Ltd; Ningbo Boway Alloy Material Co., Ltd.; Boviet Renewable Power LLC; Boviet Solar USA Ltd (collectively, "Boviet," northern District of California (3:21-cv-04510-LB) & ITC Inv. No. 337-TA-1271): Morgan Lewis & Bockius LLP (consultant and expert witness for Boviet) – prepared expert report & declaration, was deposited, prepared witness statement & rebuttal witness statement, attended hearing & testified at the trial in front of the US ITC
- 2021: Semiconductor Energy Laboratory Co., LTD v. TCL China Star Optoelectronics Technology Co., Ltd., et al, Civil Action #: 8:21-cv-00554 – JAK – ADS (CDCA): PV Law LLP (consultant and expert for TCL China Star Optoelectronics Technology Co., Ltd. – prepared four declarations in support of petition for for Inter Partes Reviews (IPRs) of several patents involved in this case

- 2020: Solas OLED Ltd. V. Samsung Electronics Co. Ltd., Samsung Electronics America, Inc., Samsung Display Co. Ltd (collectively "Samsung"), Case N. 2:20-cv-00307 – JRG (E.D. Texas) & ITC Inv. 337-3490, O'Melveny & Myers LPP (consultant and expert for Samsung)
- 2020: HP Inc. v. Solas OLED Ltd., Case N. 6:19-cv-00631-ADA (W.D. Texas); O'Melveny & Myers LLP (consultant and expert for HP Inc.)
- 2020: Apple Inc. v. Solas OLED Ltd., Case N. 6:19-cv-00537 – ADA (W.D. Texas), DLA Piper LLP (consultant and expert for Apple Corp.)
- 2020: Sharp v. Vizio et al., Case N. 8:20-cv-00490, US District Court for the Central District of California and DN 3451 before the International Trade Commission, K&L Gates LLP (consultant and expert witness for Sharp. Corp.)
- 2019: Hologic Inc. v. Direct Digital Imaging Tech. (Beijing) Inc., Case N. 1884-cv-01154 – BLSI, Litigation and Trade Secret, Mintz (consultant and expert for DDIT)
- 2019: LG Display v. Solas OLED Ltd.; Case N. 6:19-cv-235-ADA; Latham & Watkins LLP (consultant and expert for LG Display Co., Ltd.).

21. Considering the foregoing, I consider myself to be an expert in the field of flat panel displays and integrated circuits manufacturing, including OLED displays, and including thin film deposition techniques, etching chemistry, chemical-mechanical polishing, devices and circuits processing and

photolithographic steps, and the designs used in the fabrication of devices and circuits, with the feature sizes ranging from micron to submicron for various industrial applications including FPDs. Therefore, I believe that I am qualified to provide an opinion as to what a person of ordinary skill in the art at the time of the invention ("POSITA") would have understood, known, or concluded regarding the subject matter of the patents involved in this case.

III. LEVEL OF ORDINARY SKILL IN THE ART

22. My analysis reflects the views of a person of ordinary skill in the art (POSITA) in the field of the '991 Patent as of August 2, 2012, which I understand is the alleged time of invention.

23. I have been advised by the Petitioner's counsel and understand there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including (1) the levels of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior art solutions to those problems. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from teachings of the prior art, including the art cited below.

24. Taking these factors into consideration, in my opinion, on or before

August 2, 2012, a POSITA would have been someone knowledgeable and familiar with design or development of display circuits and systems that are pertinent to the '991 Patent. That person would have a bachelor's degree in electrical engineering, physics, materials science or engineering, or a related field and at least four years of practical experience with design or development of active-matrix OLED displays, including pixel layout, or the equivalent. In my opinion, a lack of work experience can be remedied by additional education, and vice versa.

25. As of August 2, 2012, I met, and in fact exceeded, the qualifications of a person of ordinary skill in the art.

26. For purposes of this Declaration, in general, and unless otherwise noted, my statements and opinions, such as those regarding my experience and the understanding of a POSITA generally (and specifically related to the references I consulted herein), reflect the knowledge that existed in the field as of the earliest possible priority date of the '991 Patent (i.e., August 2, 2012). Unless otherwise stated, when I provide my understanding and analysis below, it is consistent with the level of a POSITA prior to the earliest alleged priority date of the '991 Patent.

IV. RELEVANT LEGAL STANDARDS

27. I am not an attorney. In preparing and expressing my opinions and considering the subject matter of the '991 Patent, I am relying on certain basic legal principles that counsel have explained to me. These principles are discussed below.

28. I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious in view of what was known before the invention was made.

29. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

30. I understand that in this proceeding Petitioner has the burden of proving that the claims of the '991 Patent are anticipated by or obvious in view of the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

31. I understand that prior art to the '991 Patent in this proceeding includes patents and printed publications in the relevant art that predate the proper priority date of the alleged invention recited in the '991 Patent.

32. I understand that terms appearing in the patent claims are to be interpreted according to their "ordinary and customary meaning" in an IPR proceeding. In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning as they would have been understood by a POSITA at the time of the alleged invention, in light of the specification and file history. I understand that treatises and dictionaries may be consulted, albeit under

limited circumstances, to determine the meaning attributed by a POSITA at the time of the alleged invention. I have followed this approach in my analysis and have applied the ordinary and customary meaning of those terms throughout my analysis in this Declaration.

33. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

34. I have been informed that a claimed invention is unpatentable as obvious if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. I have also been informed by counsel that the obviousness analysis takes into account factual inquiries including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter.

35. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;

- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non- obviousness

may be present in any particular case.

36. I have been informed by counsel that the Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include the following: (a) combining prior art elements according to known methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. I also understand that, at least in IPR proceedings, admissions in the patent or in the prosecution file history of the patent (referred to as Applicant Admitted Prior Art or "AAPA") can be used to, among other things, establish background knowledge possessed by a POSITA.

37. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

38. I am not aware of any allegations by the named inventor of the ’991 Patent or any assignee of the ’991 Patent that any secondary considerations are relevant to the obviousness analysis of any Challenged Claim of the ’991 Patent.

39. I understand that a petition must identify, for any terms with means-plus-function limitations, the specific portions of the specification that describe the structure, material, or acts corresponding to each claimed function. I also understand a rebuttable presumption exists that without use of the term, “means,” a claim term is not interpreted as means-plus-function, but that other nonce words like “component” have been found to satisfy the rebuttable presumption and invoke a

means-plus-function claim construction of such a claim term.

40. I also understand that a petitioner seeking to demonstrate that the prior art discloses a means-plus-function limitation must prove that the corresponding structure—or an equivalent—was present in the prior art and performing the same claimed function.

41. I understand that the standard for determining whether the prior art discloses the corresponding structure or an equivalent is whether there are insubstantial differences, which means that if the assertedly equivalent structure performs the claimed function in substantially the same way to achieve substantially the same result as the corresponding structure described in the specification, it is equivalent.

42. I understand that proving structural equivalence does not require a component-by-component analysis, but rather that it is sufficient to show structure, materials, or acts that perform the claimed function in substantially the same way to achieve substantially the same result because the claim limitation is the overall structure corresponding to the claimed function and not individual components.

43. I understand that for a claim to be valid, its scope must be definite, and that improperly introducing a term can lead to an unascertainable scope of a term, rendering it indefinite. I understand that any claim element first addressed in the claims by the antecedent basis, “a” may then be identified later in the claims by the

antecedent basis, "the." I understand that failing to follow this convention may lead to ambiguity in the identification of the particular claim element in question, leading to an indefinite scope of the claim's term. For purposes of this proceeding, I identified and provided my best understanding of any such terms despite such ascertainable scope.

V. SUMMARY OF THE '991 PATENT

A. Specification

44. The '991 Patent describes an organic light emitting diode (OLED) display that includes a plurality of pixels, with each pixel including a plurality of signal lines, a plurality of thin film transistors (TFTs), a storage capacitor, and an OLED coupled to the plurality of signal lines. '991Pat., 1:45-46 and 6:12-19. As a preliminary matter, I note that OLED displays utilizing TFTs and capacitors are not new.

45. Pixels of existing OLED implementations, as described by the '991 Patent, include a switching TFT and a driving TFT such that in the switching TFT, a thin gate insulating layer is formed between a gate electrode and a semiconductor layer to enable rapid switching operation. *Id.*, 1:49-54. However, the '991 Patent explains that because the thickness of the gate insulating layer of the driving TFT, which is formed on the same layer as the switching TFT, is reduced, a driving range of a gate voltage applied to the gate electrode of the driving TFT becomes narrow,

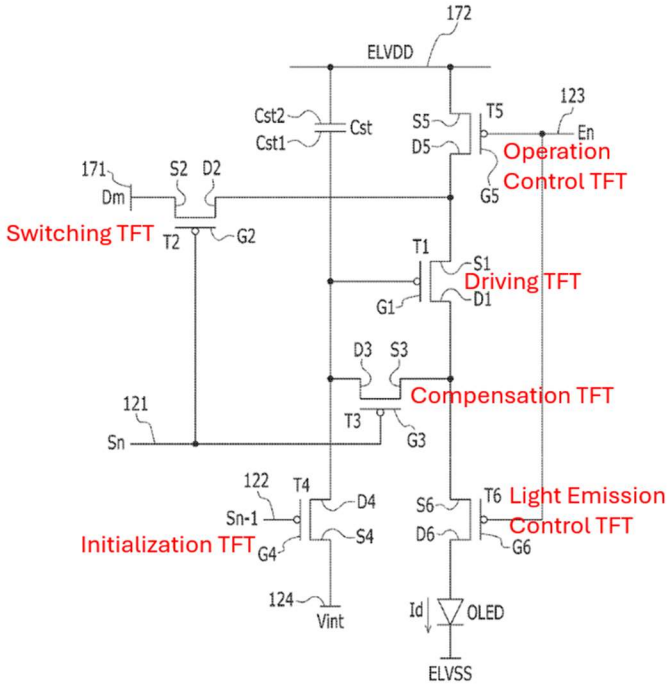
which may make it difficult to control the magnitude of the gate voltage Vgs of the driving TFT to ensure a large number of gray levels. *Id.*, 1:54-61.

46. The technology described in the ’991 Patent provides an OLED display broadening a driving range of a driving TFT to display a relatively large number of gray levels. *Id.*, 2:3-6. According to a described embodiment, this is achieved by longitudinally forming the channel region of the driving TFT by forming the semiconductor layer of the driving TFT to include a plurality of bent portions. *Id.* 4:48-53.

47. The ’991 Patent describes an exemplary embodiment of an OLED display with reference to FIGS. 1 to 5. *Id.*, 6:9-11. The equivalent circuit of one pixel of the OLED display is shown in Figure 1, with Figures 2 and 3 showing specific layout (or plan) views of the OLED display, and Figures 4 and 5 showing cross-sectional views of the OLED display taken along different cut lines. *Id.*, 6:12-14 and 8:37-51.

48. I have annotated Figure 1 below to explain the operation of one pixel of the OLED display as described in the ’991 Patent. As shown therein, the equivalent circuit includes a plurality of signal lines (121-124 and 171-172), a plurality of TFTs (T1-T6, and annotated in Figure 1), a storage capacitor (Cst), and an OLED coupled to the plurality of signal lines. *Id.*, 6:14-19.

FIG. 1



'991Pat., FIG. 1 (annotated).

49. In the context of Figure 1, the operation of one pixel (all transistors included in the pixel circuits are p-channel) of the OLED display begins with a low-level signal (e.g., negative gate voltages since p-channel TFTs are being used) prior scan signal Sn−1 being supplied through the prior scan line 122 during an initialization period. Then, the initialization TFT T4 is turned on to initialize the gate voltage of the driving TFT T1 with an initialization voltage Vint. Subsequently, a low-level signal scan signal Sn is supplied through the scan line 121 to turn on compensation TFT T3 and switching TFT T2. This step will allow for data signal Dm to be transferred to source electrode of driving TFT T1. Since T3 is turned on, the gate electrode G1 and drain electrode D1 are connected together forming diode-

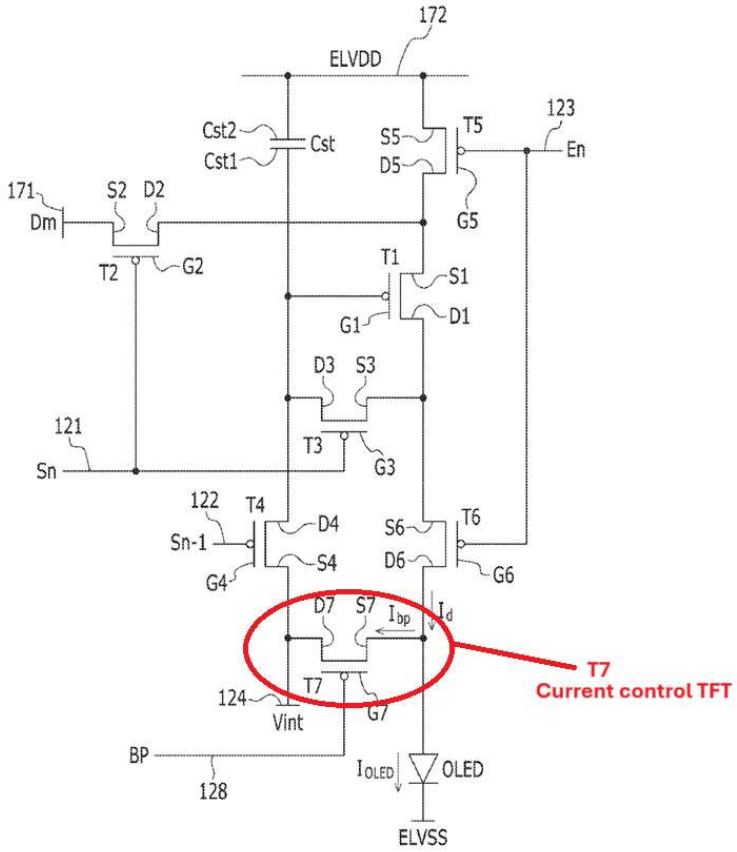
like connection TFT. Then, a compensation voltage (Dm+Vth) based on the data signal Dm supplied from data line 171 is applied to the gate electrode G1 of the driving TFT T1. The driving voltage ELVDD and the compensation voltage Dm+Vth are applied to both ends Cst1 and Cst2 of the storage capacitor Cst, and a charge corresponding to a difference between voltages at both ends Cst1 and Cst2 is stored in the storage capacitor Cst. Subsequently, the level of the light emission control signal En during a light emission period is changed from a high level to a low level, which turns on the operation control TFT T5 and the light emission control TFT T6. Then, the driving current Id is generated according to a difference between the voltage of the gate electrode G1 of the driving TFT T1 and the driving voltage ELVDD. Since the driving current Id, which is proportional to $(Dm - ELVDD)^2$, is determined regardless of the threshold voltage Vth of the driving thin film transistor T1, and is supplied through the light emission control TFT T6 to the OLED. *Id.*, 7:56-8:36.

50. The ’991 Patent describes that the six TFTs T1-T6 are formed along the semiconductor layer 131, and the semiconductor layer 131 is bent to have various shapes. *Id.*, 9:4-10. The driving semiconductor layer 131a including a plurality of bent portions 33 results in the driving range of the gate voltage applied to the driving gate electrode 125a being broadened. This enables a gray level of light emitted from an OLED to be more finely and precisely controlled by adjusting the magnitude of

the gate voltage, and as a result, it is possible to increase the resolution of the organic light emitting diode display and improve display quality. *Id.*, 9:49-62. For example, with reference to Figure 6, the '991 Patent discloses the driving semiconductor layer 131a being in the shape of an S. *Id.*, 10:5-6.

51. In an alternative embodiment, with reference to Figure 10 (which I have reproduced below and annotated), the '991 Patent describes incorporating an additional current control (or bypass) TFT T7 into the circuit illustrated in Figure 1.

FIG. 10



'991Pat., FIG. 10 (annotated).

52. The bypass TFT T7 of the OLED display is configured to disperse, or divert, a portion of the minimum current of the driving thin film transistor T1 as a bypass current Ibp to a current path other than the current path of the organic light emitting diode. *Id.*, 19:59-65. Accordingly, a contrast ratio may be improved by implementing a precise black luminance image by using the bypass thin film transistor T7. *Id.*, 20:17-19.

B. Prosecution History

53. I understand that the ’991 Patent issued from U.S. Patent Application No. 17/871,618 that was filed on July 22, 2022, claiming priority to Korean Patent Application No. 10-2012-0084976 filed on August 2, 2012.[1] For the purposes of this declaration, I treat August 2, 2012 as the priority date for the ’991 patent.

54. By my review, Liu was cited in an Information Disclosure Statement (IDS) filed by the Applicant on July 22, 2022. ’991FH, p. 227. As discussed in this declaration, had the Examiner carefully considered Liu, the claims of the ’991 patent would have been found to be obvious in view of Liu in combination with other references, including Udagawa.

[1] August 2, 2012, is assumed to be the priority date for the purposes of this Petition only.

55. The Examiner issued a Non-Final Office Action dated September 16, 2022, which included minor objections, in addition to rejections based on nonstatutory double patenting over claims of copending U.S. Patent Application No. 17/853,551 (which issued as U.S. Patent No. 11,574,990). *Id.*, pp. 124-130.

56. After the Applicant filed a Terminal Disclaimer, a Notice of Allowance was mailed on October 21, 2022, stating "Claims 1-30 are allowed primarily because the prior art of record cannot anticipate or render obvious the following limitations, in combination as recited in independent claim 1: wherein the second portion of the semiconductor layer has at least one bent portion, and wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate." *Id.*, pp. 66-72.

57. The '991 Patent issued on February 7, 2023.

VI. TECHNOLOGY BACKGROUND

A. OLED Displays—From Inception to 2012

58. Organic light-emitting diodes (OLEDs) are based on electroluminescence in organic materials, whose discovery can be traced back to the 1950s when light emission was observed by applying high voltage to thin films of acridine orange and quinacrine, which were dissolved in or deposited on thin-film cellulose or cellophane. *See generally* Bernanose. One mechanism identified in these processes involved excitation of electrons. Then in 1960 a team of investigators at

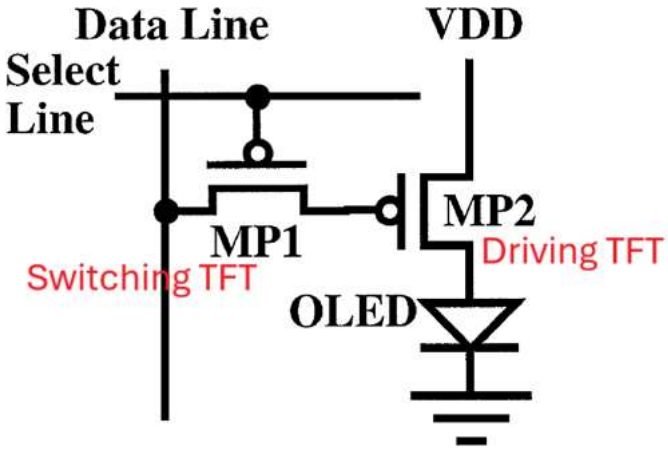
New York University made ohmic dark – injecting electrode contacts to organic crystals and describe the necessary work functions (energy requirements) for hole and electron injecting electrode contacts. *See generally* Kallmann. These carrier injecting contacts are the source of charge injections in all present-day OLED devices. In the mid-1960s, Pope observed bright blue electroluminescence (EL) in single crystal anthracene by applying a high DC voltage (about 400V) across the crystal. *See generally* Pope. The proposed mechanism for light emission was termed field-accelerated electron excitation of molecular fluorescence. The same group later observed that in the absence of an external electric field, the EL in anthracene crystals results from recombination of electron and hole, and that the conducting-level energy of anthracene is higher than the exciton energy level. *See generally* Sano. Later, Vincett used evaporated thin film of anthracene and was able to reduce the drive voltage to below 30V. However, the quantum efficiency of this device was only about 0.05%. *See generally* Vincett. The first report of an organic LED was in the seminal work by Tang in the 1980s, which demonstrated a heterojunction device and developed a doping method by introducing a small number of fluorescent materials into a host matrix. *See generally* Tang. The OLED heterojunction is a basic device structure of all present-day OLED devices. The electroluminescence in conjugated polymer poly(p-phenylene-vinylene) (PPV) was reported in 1990. *See generally* Burroughes. This work was followed by a breakthrough in the late 1990s

when phosphorescent light-emitting materials, which dramatically improved the quantum efficiency and brightness of the OLED devices, were discovered. *See generally* Baldo. Higher light emission efficiency will allow reduction of driving voltage used for driving thin film transistors (TFTs). It is expected that this will lead to more stable active–matrix (AM)-OLEDs. Today, phosphorescent OLED (PHOLED) is a cornerstone technology for low-power (e.g. low voltage) bright organic light emitting displays and energy-efficient light sources.

59. The various milestones in the evolution of the driving/control circuitry for the OLED pixel are now discussed to emphasize the gradual innovation of this technology from the late 1990's to the early 2010's. As I explain below, the purported novel and inventive features of the '991 patent existed before the priority date of the '991 patent.

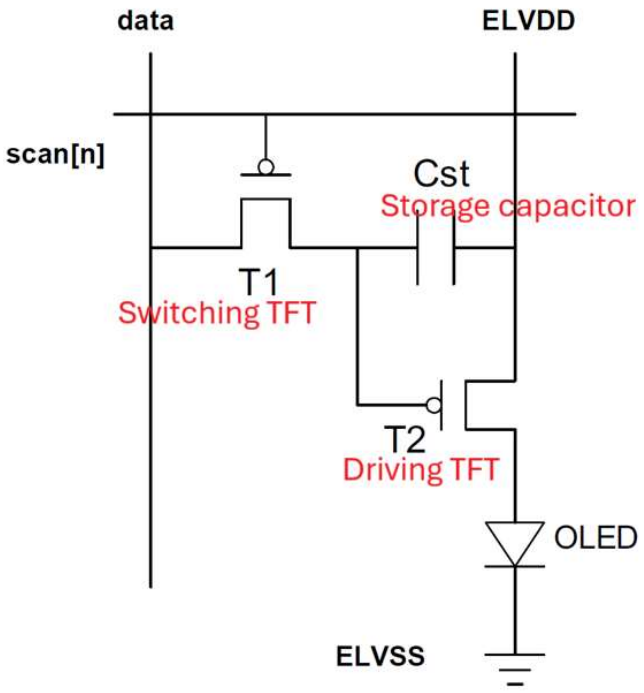
1. Two transistor (2T) and two transistor, one capacitor (2T1C) pixel circuits:

60. The two transistor (2T) circuit represents the minimal pixel circuit design required for AMOLEDs. Dawson, p. 2. In this basic pixel design, the first TFT is used for switching (e.g., selecting the pixel) and the second TFT is used for driving (e.g., as a current source). An example of such a 2T pixel circuit is shown in Figure 1 of Dawson (reproduced below and annotated).



Dawson, FIG. 1 (annotated).

61. The 2T circuit can be augmented with one storage capacitor (or "holding capacitor") that is used to store driving TFT gate voltage, which will be responsible for keeping TFT turn on between refresh cycles. An example of such two transistor, one capacitor (2T1C) circuit, is shown in the figure below, prevents the pixel voltage from drifting due to leakage currents or parasitic effects. However, the current resistance (IR) drop problem remains for the 2T1C circuit. Kim-2009, §3.1.



Kim-2009, FIG. 3 (annotated).

62. In the operation of the 2T1C circuit, when the pixel is selected, the switching TFT is turned on by the gate signal (voltage), allowing data signal (voltage) to be charged onto the storage capacitor, C_{st}. This voltage is also the gate voltage of the driving TFT. Depending on the amplitude of the gate voltage, OLED current at different levels will flow from power line (or anode) for a given voltage value, V_{DD}, to the ground (or cathode) through OLED device. The switching TFT is only on when the pixel is selected and the storage capacitor is charged. The key requirement for this transistor is low leakage current, which prevents the storage capacitor from discharging. For the driving TFT, depending on the signals, it could be on during the whole frame time with current ability to conduct large currents. It is desirable for a

TFT to operate in a saturation regime since it does a better job to keep a constant current when the OLED resistance changes over time.

63. In these 2T and 2T1C pixel driving circuits, n-channel TFTs, p-channel TFTs, or combination of n-channel TFTs and p-channel TFTs can be used. The OLED displays are driven by electric current, so small drain current variations due to the threshold variation, for example, can produce non-uniformity in display brightness. Furthermore, neither the 2T circuit nor the 2T1C circuit includes compensation for TFT threshold voltage (Vth) drift or IR drop across the display. These issues were addressed with the introduction of 4T1C and 5T1C circuits, as discussed below.

2. Four transistor, one capacitor (4T1C) and five transistor, one capacitor (5T1C) pixel circuits:

64. Since TFT threshold voltage variations can be observed during poly-Si TFT fabrication and over time during OLED display operation, there is need to compensate poly-Si TFT threshold voltage (V_{th}) variation to realize a good quality OLED display with uniform luminance. To fulfill this need, 4T1C and 5T1C pixel circuits have been introduced. *See, e.g.,* Dawson, p. 3 for 4T1C pixel circuit; Kim-2009, §3.2 for 5T1C pixel circuit. The basic principle of Vth compensation is to store the driver TFT V_{th} in the gate node as $V_G = V_D + V_{th}$, by connecting gate and drain nodes as shown in the figure below.

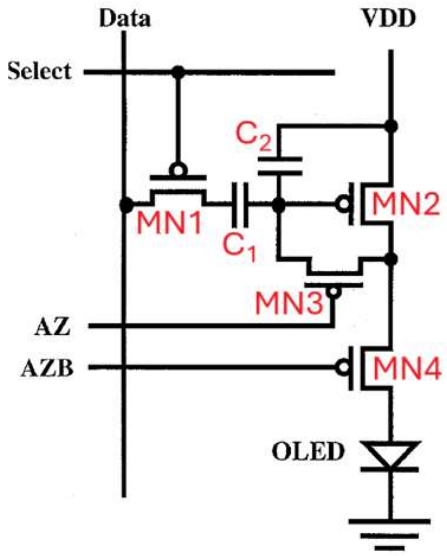


Fig. 3. Schematic of Four-Transistor AMOLED Pixel with Autozero.

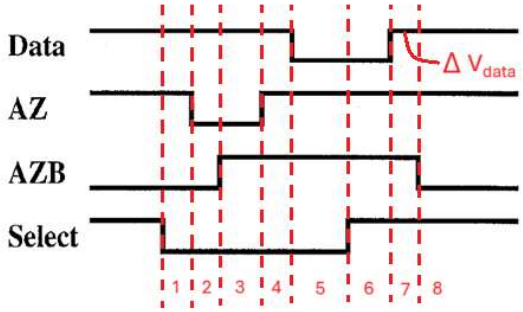


Fig. 4. Four-Transistor AMOLED Pixel Timing Diagram

Left: Dawson, FIG. 3 (annotated); Right: Dawson, FIG. 4 (annotated).

65. The pixel circuit in FIG. 3 above shows a threshold voltage (Vth) compensation circuit by voltage programming and is the likely prototype of most subsequently proposed compensation pixel circuits. With reference to FIG. 4 above, the operation of this circuit can be explained as follows: (1) The AZ line is set to negative voltage, and MN3 TFT turns on. (Note that the TFT is p-channel.). (2) The gate node and drain node of MN2 are connected, so the gate node of driver TFT (MN2) stores Vth information. (3) The data line signal voltage is added to the driver TFT gate node using capacitance coupling of C1. (4) As the gate node of the driver TFT stores the data line signal plus Vth, the source – drain current of the driver TFT does not contain Vth information. Therefore, mura (non-uniformities) related to TFT

Vth variation does not take place, due to the threshold cancellation mechanism. Voltage programming was the method most frequently used for actual OLED display products developed before 2012.

66. However, the IC driver voltage programming for the 4T1C and 5T1C circuits has some disadvantages such as the inability to compensate for either TFT mobility variations or OLED turn-on voltage variation and aperture ratio loss due to the space occupied by the programming circuit in bottom emission structure implementations. These drawbacks were mitigated by the introduction of six transistors, one capacitor (6T1C) pixel circuits and seven transistors, one capacitor (7T1C) pixel circuits.

3. Six transistors, one capacitor (6T1C) and seven transistors, one capacitor (7T1C) pixel circuits:

67. The 6T1C circuit added features like dual-gate or emission control transistors. This 6T1C pixel circuit is better than 4T1C or 5T1C pixel circuits because it compensates for both threshold voltage (Vth) variation and current resistance (IR) drop (*see generally* Lee-2012), but is limited at low grayscales, as explained in next section. The next section further explains that the 7T1C pixel circuit solved the lingering issues observed in 6T1C pixel circuits.

B. OLED Displays—State of the Art in 2012

68. 6T1C and 7T1C pixel circuits, and TFTs using a serpentine channel,

represented the state of the art several years before 2012.

1. Six transistors, one capacitor (6T1C) Pixel Driving Circuits

69. In 4T1C and 5T1C pixel circuits, the characteristics of the two adjacent TFTs within a pixel could be different, e.g., different threshold voltages. In this case, the threshold voltage has not been compensated, and the quality of the image degrades. In an example, the mismatched electrical properties of the driving TFT and the compensating TFT in the same pixel circuit may result in not achieving enough compensating for the threshold voltage variation. This drawback is mitigated by using a new voltage programming AMOLED pixel circuit structure that can compensate for threshold voltage variation without additional mirror-type compensation TFTs, i.e., by using the 6T1C pixel structure.

70. The 6T1C pixel circuit was developed by graduate student S. Choi at Hanyang University Graduate School. His work was presented at the International Display Workshops (IDW) in 2003 and published in the proceedings thereof. *See generally* Choi. This initial work on 6T1C was followed by the introduction of the 7T1C pixel circuit thereby enabling the high-resolution AMOLED displays common today.

71. Figure 1 below shows a typical 6T1C pixel structure for AMOLEDs. Therein, the M2, M3, M4, M5, and M6 are switching TFTs, and M1 is a driving TFT, which supplies emission current to OLED during a frame time. M4 creates a

discharge path to initialize the gate voltage of M1, and C1 is a storage capacitor that stores the gate voltage of M1. Furthermore, and as shown in Figure 2 below, two row line times are needed to complete the data programming operation.

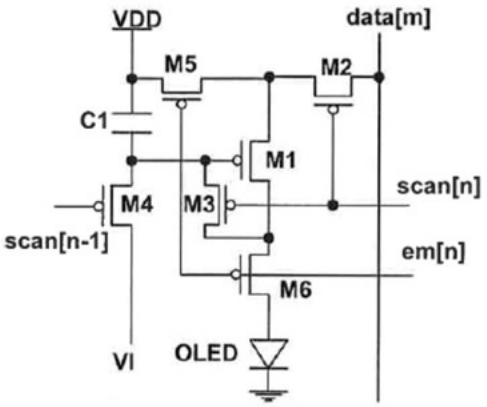


Figure 1. Proposed pixel structure.

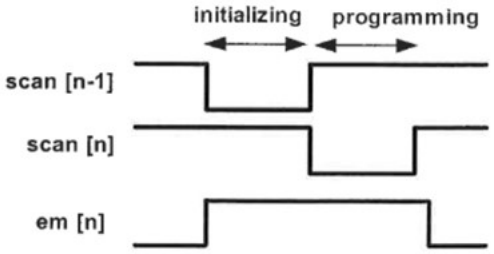


Figure 2. Timing diagram of proposed structure.

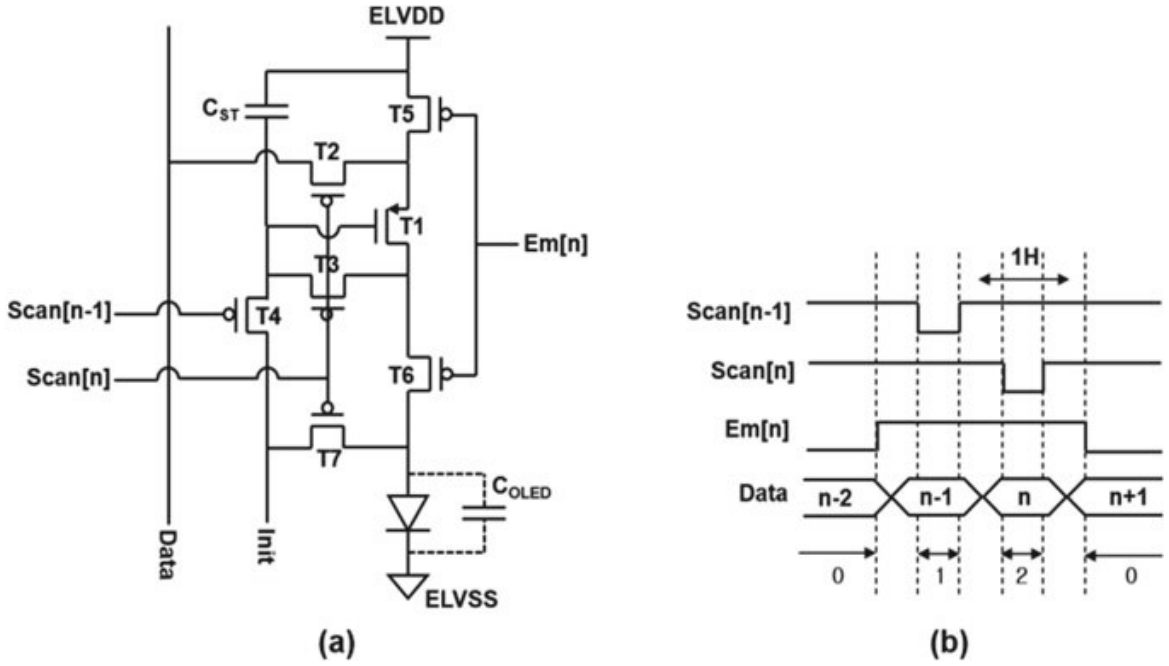
Left: Choi, FIG. 1; Right: Choi, FIG. 2.

72. As seen in the timing diagram in Figure 2, both scan[n] (current row scan signal) and scan [n-1] (previous row scan signal) are applied to program a single pixel of the OLED. During previous scan line time (when scan [n-1] signal is logic low), the gate voltage of M1 is discharged down to V1, whereas during current scan line time (when scan [n] signal is low), M2 and M3 are turned on so that data voltage is programmed to the gate node of M1 through diode-connected M1. At that time, the programmed data voltage is automatically reduced to $V_{data[m]} - V_{th,M1}$, where $V_{data[m]}$ and $V_{th1,M1}$ are the programmed data voltage and threshold voltage of M1, respectively. After two line times, i.e., the previous and current line times, M5 and

M6 are turned on by em[n] signal, and the OLED emission current of programmed data, which is independent of the threshold voltage of M1, flows through M5, M1, and M6. The gate voltage of M1 already contains information of its threshold voltage, which is the desired effect of compensating for the threshold voltage mismatch of TFTs in the same pixel. This pixel structure can be modified to another pixel structure, based on display requirements.

2. Seven transistor, one capacitor (7T1C) Pixel Driving Circuit

73. The 7T1C pixel circuit for AMOLED displays emerged as an evolution of compensation circuits to address critical challenges in active-matrix OLED technology long before 2012. For example, Jeong, Chung, and Noguchi-II all disclose various examples of the 7T1C configuration. An example of a typical 7T1C pixel circuit, and its associated timing diagram, are shown below from Park. Although Park is after the priority date, it discusses the same subject matter that was available before 2012 and is presented for illustrative purposes only. In the timing diagram, the time durations denoted 0, 1, and 2 correspond to a light emission period, a data writing period, and a threshold voltage extraction period, respectively.



Park, FIGs. 15(a) and 15(b).

74. The 7T1C pixel circuit shown above has features such as anode reset (which initializes the OLED anode to a predefined voltage V_{in}, preventing residual voltage from previous frames) and cathode reset (which separately initializes the driving TFT's gate voltage, V_{ref}). This approach eliminates ghosting and improves low-gray accuracy. Also, the robust V_{th} compensation uses multiple phases (reset, compensation, data writing, emission) to isolate and store the driving TFT's V_{th} on the storage capacitor (C_{st}), which cancels V_{th} drift. Finally, this pixel circuit has emission control flexibility, e.g., dedicated transistors that decouple emission timing from data writing / compensation which enables the global emission (reduces flicker) and uses duty cycle control for brightness adjustment. The IR drop is mitigated through compensation phases which account for voltage drops in power (V_{DD}) lines,

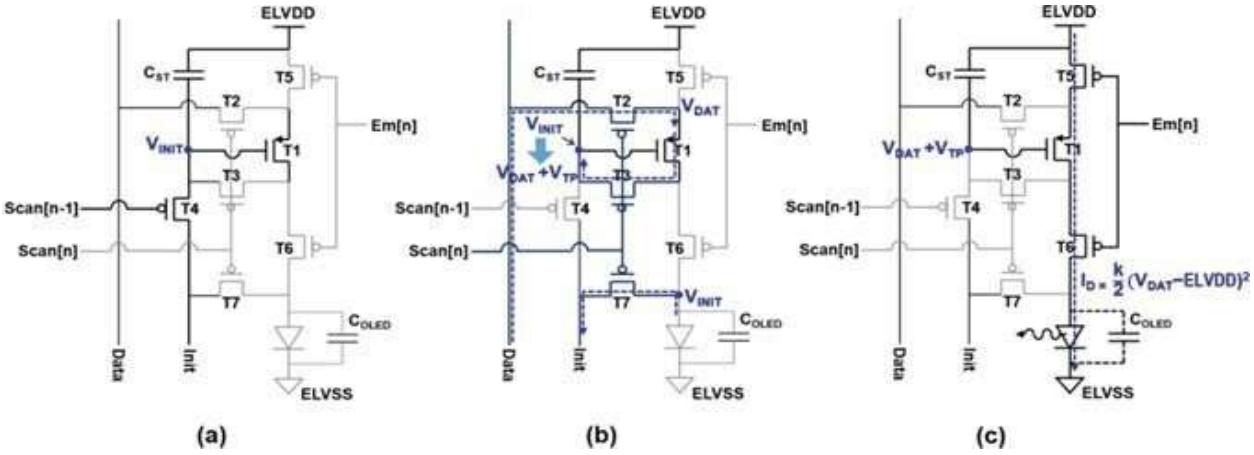
ensuring uniform current flow.

75. The OLED pixel circuit shown in Figure 15(a) includes seven p-channel thin film transistors, one capacitor, and six lines – ELVSS (Electroluminescent Voltage Source), Vinit, Scan (n), Scan (n−1), Data, Em (n) and ELVDD (Electroluminescent Voltage Drain). Herein, T2 to T7 switching transistors have only on / off functionality, whereas T1 is a driving transistor whose current is controlled by the voltage applied to its gate through the DATA line. T2 corresponds to a scan transistor (or selection transistor) in the conventional 2T1C pixel circuit, T3 is diode-connected when it is turned on by the scan signal and is used to compensate for the threshold voltage of driving transistor T1, T4 is an initialization transistor, used to apply an initial voltage (Vinit) to the gate of the driving transistor, and T5 and T6 are emission control transistors to control current flow from ELVDD to OLED. T7, which is a black current bypass transistor that is used to remove a residual voltage of the anode of OLED after emission period, is discussed later. The capacitor overlaps with the driving transistor T1. The V_{GS} of T1 is stored in C_{ST} and determines the I_{OLED} according to the grey-level data. Independent of the driver TFT T1, T5 and T6 can be used to block I_{OLED} under the control of the Em[n] signal, which is consequently used for dimming control of the display panel.

76. Operation of the 7T1C pixel is shown in FIG. 16 of Park (which has been reproduced below), where (a), (b) and (c) correspond to initialization, data

writing and threshold voltage extraction, and light emission period, respectively. The operation of data refresh with V_T compensation of T1 is carried out as follows. The initialization period begins with all the switch TFTs turned off, except T4, as shown in FIG. 16(a). Thus, the gate voltage of the driver T1 is pulled down to V_{INIT} and T1 is initially turned on. Then, T4 is turned off. Next, a data voltage V_{DAT} is applied to the source of T1 and V_T extraction is performed.

77. At the beginning of the data writing and threshold voltage extraction period, T2, T3 and T7 are turned on, as shown in FIG. 16(b) below. During this period, the gate node voltage of T1 changes from V_{INIT} to $V_{DAT} + V_{TP}$, where V_{TP} is the V_T of T1. At the same time, the anode of the OLED is discharged through T7 to prevent charge accumulation in the intrinsic OLED capacitance, C_{OLED}, by a leakage current through T1. Otherwise, some light will be emitted even when black expression is wanted. Finally, the gate voltage of T1 is stored by C_{ST} and the source of T1 is connected to ELVDD, as shown in FIG. 16(c), during light-emission period. The V_T extraction time of this circuit is limited to one horizontal line selection time—1H time—since the nth data voltage should be maintained throughout V_T extraction period.



Park, FIG. 16 (annotated).

78. In the 7T1C pixel circuit shown above, T7 is placed between T6 and OLED anode. The source of T7 (S7) is connected to OLED anode and the drain of T7 is connected to V_{int} (initialization voltage). At the node, the current I_d is divided into the current flowing to OLED and I_{bp}, which is referred to as bypass current. The T7 is black current bypass transistor, which is used to remove a residual voltage of the anode of OLED after emission period. When T7 is turned on by appropriate voltage applied to gate electrode (G7), the I_{bp} current can flow to Vint and OLED voltage at the anode becomes V_{int}. In other words, the anode of the OLED is discharged through T7 to prevent charge accumulation in the intrinsic OLED capacitance, by a leakage current through T1. Otherwise, some light will be emitted even when black expression is wanted. T7 can have a separate gate line or one connected to Sn line of T3.

3. TFTs Using Serpentine Channels

79. From the early 2000s (for example Udagawa), curved channel thin-film transistors (TFTs) represented a significant advancement in AMOLED display backplane design by efficiently addressing the critical need for high drive currents within the spatial constraints of high-resolution display pixels. Through innovative structuring—such as U-turns, S-shapes, and serpentine patterns—the transistor channel can be folded to dramatically increase the effective channel width (W_{eff}) without enlarging the overall device footprint. This increased channel width of the drive transistor substantially boosts the drive current (I_{ON}), which is essential for delivering sufficient pixel brightness, enabling fast pixel charging to support high refresh rates, and offsetting variations in OLED efficiency and degradation over time.

80. The foundational concept of curved channel designs has deep roots in semiconductor engineering, with seminal work dating back to the 1980s in silicon integrated circuits and subsequent adaptation for display technologies in the 1990s. The importance of this design approach grew markedly in the early 2000s alongside the proliferation of AMOLED displays, as shrinking pixel sizes created a growing demand for high current in confined areas. This challenge was further amplified in the 2010s with the adoption of oxide semiconductor backplanes (e.g., a-InGaZnO), which have lower carrier mobility than low-temperature polysilicon (LTPS) and therefore benefit greatly from channel geometries that maximize current capacity

and evenly distribute electrical stress and thermal load.

81. Thus, it is my opinion that the use of serpentine (curved) channels was well-established and widely known in the field of TFT design by 2012, with both academic literature and commercial practice recognizing their value for improving current delivery and device reliability in advanced display applications.

C. Architecture and Operation of OLED Display Pixels

82. In an AM-OLED, an image is divided into small elements called pixels. In a color AM-OLED, each pixel is further divided into three or four sub-pixels, one for each of the three primary colors red (R), green (G), and blue (B), e.g. tri-color OLEDs contain three different OLED emitters in one pixel. As explained above, each pixel (in a monochrome display) or sub-pixel (in a color display) contains at least two thin film transistors, a storage capacitor, and a pixel electrode (or more generally, a driving/control circuit), and an EL light emitting device. Hence, RGB OLEDs consist of one red, one green and one blue OLED. Also, each emitter is connected to a separate lead so they can be controlled independently. By independently adjusting brightness (or light intensity) of each of the three, RGB OLEDs the AM-OLED is capable of producing a wide range of colors.

83. The display format (i.e., the total number of pixels) and the display frame rate (i.e., how many times per second the image content will be updated) determine the required speed of the TFT switch. A typical display frame rate is 60

Hz, which implies that the image content will be updated every 1/60 of a second, or 0.017 seconds. A typical computer monitor has the SXGA format (1280x1024 pixels). When such a display operates at a 60 Hz frame rate, the time that is allocated for updating or changing the voltage stored at the pixel's capacitor is 0.017/1024 seconds, or about 17 microseconds. In order to ensure correct light output for the pixel, a pixel TFT must provide enough current to charge its pixel capacitor to the correct voltage level within the allocated time.

84. The architecture and operation of each driving/control integrated circuit, which independently controls each pixel of the OLED display, can be comprehensively understood through three distinct mechanisms: (1) the circuit diagram, (2) the layout (or plan) view, and (3) the cross-sectional view. I will now explain each of these mechanisms using the embodiments described in Liu.

1. Circuit Diagrams

85. A circuit diagram shows the logical and electrical connections between various components, the routing of data, control, and power signals, and how a certain component contributes to the overall operation. Liu provides a schematic circuit diagram of a pixel structure in Figure 1, which I have reproduced and annotated below. Liu, ¶13.

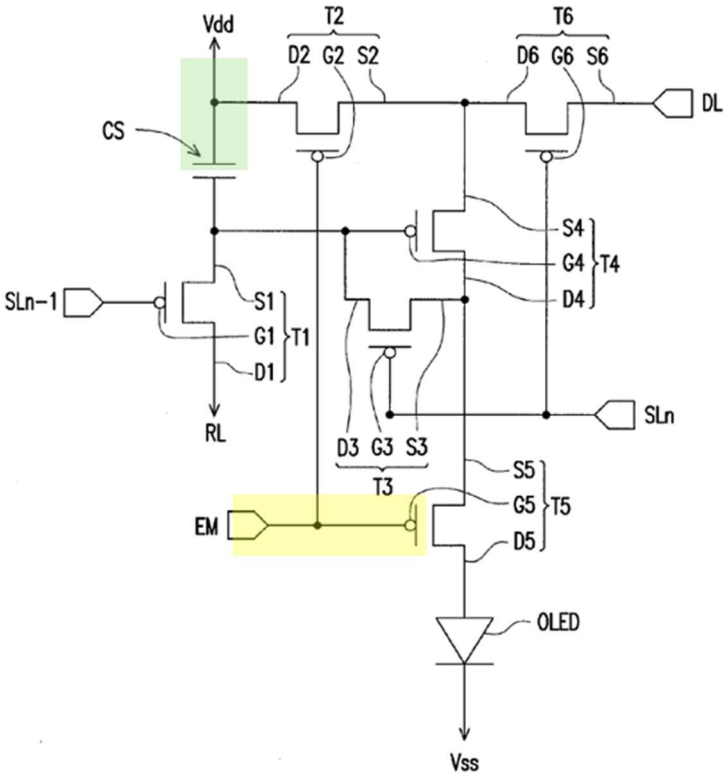


FIG. 1

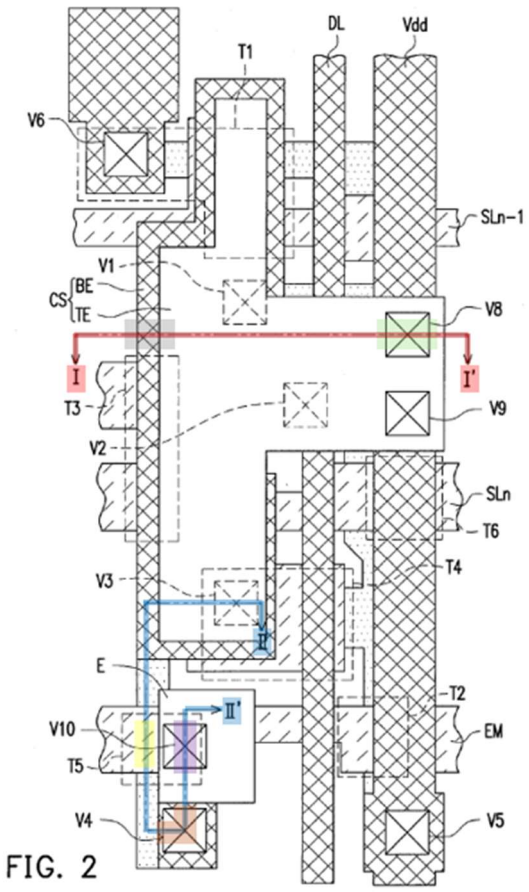
Liu, FIG. 1 (annotated).

86. As shown in Figure 1, the light emitting signal line EM is electrically connected to gate G5 of the fifth thin film transistor T5 (highlighted in yellow therein) and the top electrode TE is electrically connected to the power line Vdd (highlighted in green therein). Liu, ¶¶44, 64.

2. Plan Views

87. A plan (or layout) view shows the actual placement and routing of components (e.g., routing of metal layers and vias) and interconnections on the silicon die, which provides insight as to how efficiently the chip area is being used.

Liu further provides a top (or layout or plan) view of the pixel structure in Figure 2, which I have reproduced and annotated below. Liu, ¶14.



Liu, FIG. 2 (annotated).

88. To better understand the operation of the driving/control circuit of the OLED shown in Figures 1 and 2 of Liu, separating each of the layers described above allows one to appreciate the level of technology and state of the art that existed before the priority date of the ’991 patent. Figures 3A-3D of Liu, which show the different layers of the pixel structure, are reproduced below.

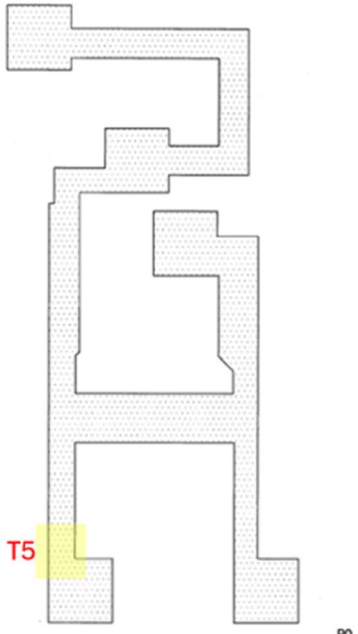


FIG. 3A

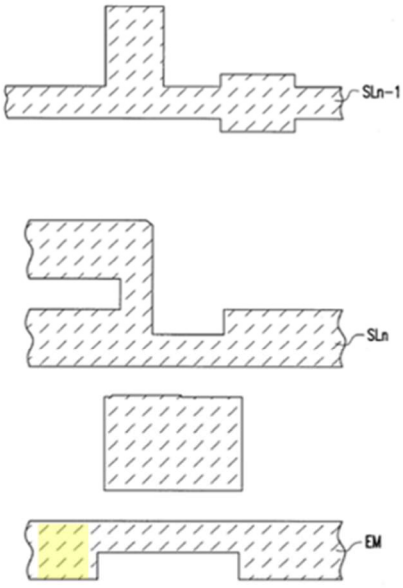


FIG. 3B

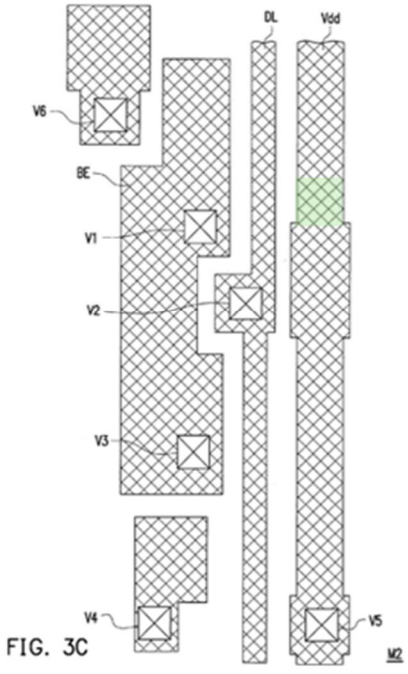


FIG. 3C

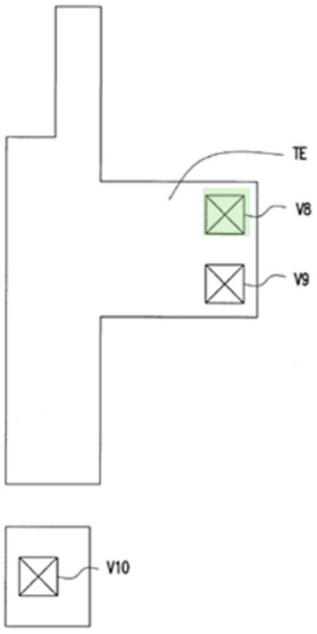


FIG. 3D

Liu, FIGS. 3A-3D.

89. Referring to the pixel structure in Figure 2, the above figure illustrates the separate layers that include FIG. 3A showing a semiconductor layer, FIG. 3B showing a first conductive layer, FIG. 3C showing a second conductive layer, and FIG. 3D showing a third conductive layer. Liu, ¶¶14-18.

90. The semiconductor layer PO has a source region S5, a drain region D5 and a channel region CH5 in a region predetermined for forming a fifth thin film transistor T5. *Id.*, ¶35. The first conductive layer M1 has a gate G5 in the region predetermined for forming the fifth thin film transistor T5, and the light emitting signal line EM is electrically connected to the gate G5. *Id.*, ¶¶37, 64.

91. Figures 3A and 3B have been annotated (in yellow highlighting) to show the location of transistor T5 on the semiconductor layer and the location on the light emitting signal line EM in the first conductive layer (or first metal layer M1) that corresponds to the gate G5, respectively. Gate G5 being coincident with signal line EM (both on first metal layer M1) is consistent with gate G5 and EM being electrically connected as also shown in Figure 1 (in which this same connection is also highlighted in yellow). Furthermore, the yellow highlighted portion on M1 (with gate G5) is directly above the channel region of transistor T5 on the semiconductor layer PO.

92. The second conductive layer M2 comprises a power line Vdd and the third conductive layer M3 includes a top electrode TE of the capacitor CS. Liu, ¶¶42,

44. Furthermore, the top electrode TE is electrically connected to the power line Vdd through contact via structures V8~V9. *Id.*, ¶44.

93. Figures 3C and 3D have been annotated (in green highlighting) to show the location on Vdd on the second conductive layer (or second metal layer M2) and the location on the top electrode (TE) on the third conductive layer (or third metal layer M3), respectively, that are vertically overlapping on the plan (or layout) view and are electrically connected through contact via structure V8, as also shown in Figure 1 (in which this same connection is also highlighted in green).

3. Cross-Sectional Views

94. A cross-sectional view provides a vertical "slice" through the integrated circuit along a cross-sectional (or "cut") line that shows the stacking and composition of various layers, e.g., polysilicon (PO) and metal (M1, M2, M3), which provides details about the fabrication process, e.g., isolation techniques. Liu further provides Figure 6, which is a schematic diagram (or cross-sectional view) showing the formation of an OLED on the pixel structure depicted in Figure 2. Liu, ¶21.

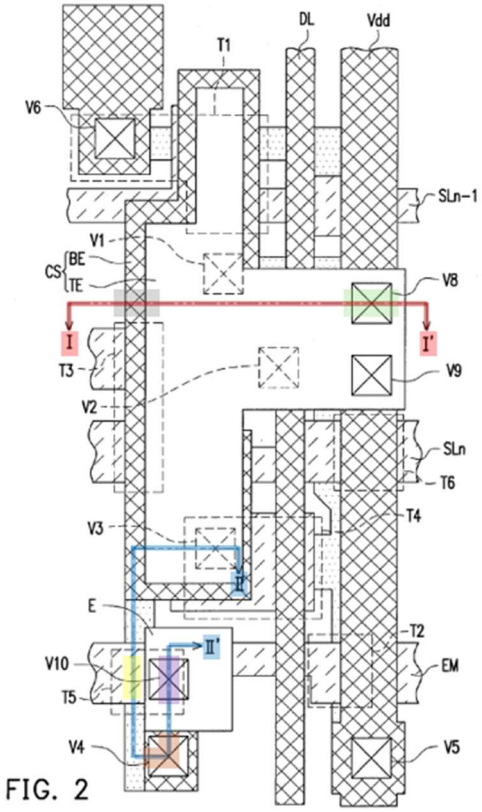


FIG. 2

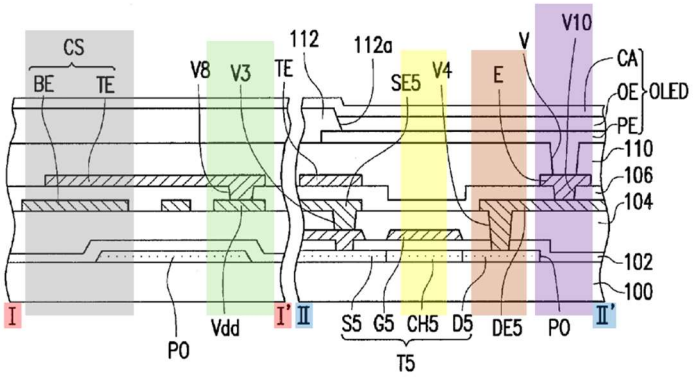


FIG. 6

Left: Liu, FIG. 2 (annotated); Right: Liu, FIG. 6 (annotated).

95. Specifically, the cross-sections of the integrated circuit along the cross-sectional line I-I' (highlighted in red in Figure 2 above) and the cross-sectional line II-II' (highlighted in blue in Figure 2 above) are illustrated in Figure 6. Both Figures 2 and 6 have been annotated with different colors to show the corresponding portions across both figures. In an example, "gray" and "green" sections are highlighted along the (red) cross-sectional line I-I' (with the green highlighted section corresponding to TE being electrically connected to the power line Vdd). In another example, "yellow", "peach" and "purple" sections are highlighted along the (blue) cross-sectional line II-II' (with the yellow highlighted section corresponding to the gate

G5 being above the channel region CH5 in transistor T5).

96. Referring to annotated Figures 2 and 6, the gray-highlighted portion shows the overlapping top electrode TE and bottom electrode BE of the storage capacitor CS (see Liu, ¶47), the peach-highlighted portion shows contact via structure V4 connecting the drain electrode DE5 (in the second conductive layer M2) being electrically connected to the drain region D5 (in the semiconductor layer PO) (see *Id.*, ¶40), and the purple-highlighted portion shows the conductive pattern E being electrically connected to the drain electrode DE5 through a contact via structure V10 (see *Id.*, ¶44).

VII. CLAIM CONSTRUCTION

97. It is my understanding that in order to properly evaluate the Challenged Patents, the terms of the claims must first be interpreted. It is my understanding that for the purposes of this inter partes review, the claims are to be construed under the so-called Phillips standard, under which claim terms are given their ordinary and customary meaning as would have been understood by one of ordinary skill in the art in light of the specification and prosecution history, unless the inventor has set forth a special meaning for a term. For the purposes of this declaration, I have given all the claim terms of the Challenged Claims their plain and ordinary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I have been asked to assume August 2, 2012, for all

claims.

VIII. CLAIMS 1-30 ARE UNPATENTABLE

98. I have been asked to provide my opinion as to whether the Challenged Claims of the ’991 Patent would have been obvious in view of the prior art. The discussion below provides a detailed analysis of how the prior art references identified below teach the limitations of the Challenged Claims of the ’991 Patent.

99. As part of my analysis, I have considered the scope and content of the prior art and any differences between the alleged invention and the prior art. I describe in detail below the scope and content of the prior art, as well as any differences between the alleged invention and the prior art, on an element by element basis for each Challenged Claims of the ’991 Patent. As described in detail below, the alleged invention of the Challenged Claims would have been obvious in view of the teachings of the identified prior art references as well as the knowledge of a POSITA.

A. Ground 1A: Claims 1-6, 8-13, 15-20, 22-26, 28-30 are Unpatentable over Liu and Udagawa

1. Summary of Liu

100. Liu (EX1005) is a U.S. Patent Application Publication entitled “Pixel Structure,” with a filing date of February 2, 2012 (published December 13, 2012; claiming the priority benefit of Taiwan Patent Application No. 100120435 filed June

10, 2011). In Liu, a pixel structure for an organic electroluminescence display comprising six thin film transistors and one capacitor (6T1C) is disclosed. Liu, ¶32.

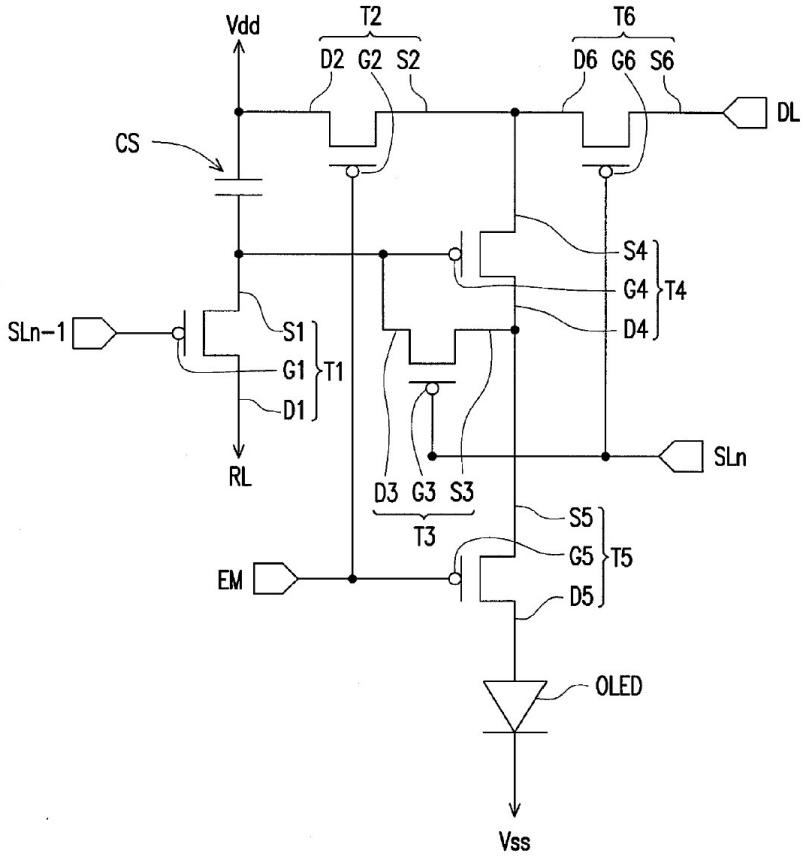


FIG. 1

101. Compared to conventional 6T1C implementations, the disclosed pixel structure in Liu implements the capacitor CS using three conductive layers, which maintains a predetermined storage capacitance and results in a 20-30% reduction in the overall area of the pixel structure (compared to conventional 6T1C implementations). *Id.*, ¶¶47, 72.

102. In my opinion, Liu is analogous art to the '991 Patent because both Liu

and the ’991 Patent are in the same field of endeavor. Both are directed to the pixel structure of an OLED display that is driven by the cooperation of multiple TFTs and a capacitor. *Id.*, ¶6. Similarly, both endeavor to reduce an area occupied by components of the pixel structure. *Id.*, ¶7.

103. Liu teaches a pixel structure disposed on a substrate 100 and comprising a semiconductor layer PO, a first insulating layer 102, a first conductive layer M1, a second insulating layer 104, a second conductive layer M2, a third insulating layer 106, a third conductive layer M3, and a pixel electrode PE. *Id.*, ¶32. Herein, the semiconductor layer PO mainly comprises channel regions, source regions and drain regions of the six TFTs (denoted T1 through T6). *Id.*, ¶34. The first conductive layer M1, which is disposed on the first insulating layer 102, includes the gates of TFTs T1-T4 and T6, as well as scan lines SLn and SLn−1, a light emitting signal line EM, and a reference signal line RL. *Id.*, ¶¶37-38. The second conductive layer M2, which is disposed on the second insulating layer 104, includes the source electrodes and the drain electrodes of the six TFTs T1-T6, and the bottom electrode (BE) of the capacitor. *Id.*, ¶40. The third conductive layer M3, which is disposed on the third insulating layer 106, includes a conductive pattern (which is used to connect the pixel electrode to various electrodes of the TFTs) and the top electrode (TE) of the capacitor. *Id.*, ¶¶44-46.

2. Summary of Udagawa

104. Udagawa (EX1006) is a U.S. Patent Application Publication entitled "Light Emitting Device," with a filing date of November 4, 2002 (published May 15, 2003; claiming the priority benefit of Japanese Patent Application No. 2001-344671 and Japanese Patent Application No. 2002-010766 filed November 9, 2001 and January 18, 2002, respectively). In Udagawa, the channel of the TFT has a length that is orders of magnitude longer than that of a channel of a conventional TFT, which lowers the dispersion in the electric current value of the TFT and enables the TFT to be turned to an on-state at a particularly higher gate voltage. Udagawa, ¶¶19, 23.

105. In my opinion, Udagawa is analogous art to the '991 Patent because it is in the same field of endeavor. Both are directed to displaying an image by using a plurality of TFTs in each pixel with the TFT(s) controlling the current amount flowing through the OLED. *Id.*, ¶¶8-9. Similarly, both the '991 Patent and Udagawa describe using polysilicon film to form the TFT, with the pixels and driving circuits being formed integrally over the same substrate, thereby reducing the number of connecting terminals and reducing the periphery of the pixel portion. *Id.*, ¶10.

106. Udagawa teaches that a TFT supplying an electric current to an OLED has a channel length that is much longer, specifically, several tens of to several hundreds of times longer than that of the related art, so that the TFT may be turned

to an on-state at a gate voltage much higher than ever to drive and may have low channel conductance gd. *Id.*, ¶¶22, 26. Furthermore, by making the channel conductance (or conductivity of a channel) smaller, even when the OLED may be deteriorated for some reason, the current flowing to the OLED can be maintained at a constant value, resulting in maintaining a constant brightness. *Id.*, ¶¶28, 61.

3. Motivation to combine Liu and Udagawa

107. In my opinion, there are several reasons that motivate combining the teachings of Liu and Udagawa.

108. Both Liu and Udagawa described drive circuits for OLED displays and both sought to improve the design and operation of OLEDs. Notably, Liu's invention focused on providing a design with a reduced-area pixel structure. Liu, ¶¶4, 10, 47, 56, 72. And, Udagawa described drive circuit configurations that improved OLED's reliability, and consequently, its operations and image quality. Udagawa, ¶12.

109. More specifically, Udagawa had recognized small TFTs resulted in unwanted dispersion effects, which was a main reason for display irregularities in a display device. Udagawa, ¶38. Thus, in my opinion, there was a motivation to reduce the dispersion in Liu's TFT drive circuits so that the pixels in the high-resolution display provided a more uniform brightness.

110. Furthermore, there is a motivation to combine Liu with Udagawa, and

specifically to use Udagawa's driving TFT with the serpentine channel in Liu's OLED driving circuit because this combination would have conformed to Liu's objectives of reducing the size of the pixel area for a TFT having a longer channel; forming the gate channel in this way would allow for a reduction of the characteristic dispersion of each TFT, leading to a reduction of the brightness variation and a reduced size of the pixel area while enabling an improved operation of the driving TFT.

111. In my opinion, a POSITA would have been skilled enough to use Udagawa's TFT with a longer channel in Liu's OLED driving circuit to achieve the known and predictable result of reducing the characteristic dispersion of the driving TFT. Furthermore, elongating the channel length to reduce dispersion was well-known by 2012, as evidenced by the teachings of Udagawa and other known prior art references, such as Yamazaki, Min, and Lee-2009.

112. Additional details regarding the Liu-Udagawa combination are provided below in connection with specific claim limitations.

4. Independent Claim 1

a. 1[pre]: An organic light emitting diode display comprising:"

113. In my opinion, Liu teaches or suggests 1[pre].

114. Liu discloses a "pixel structure" of an organic light emitting diode

("OLED") in a display using thin film transistors ("TFT") and a capacitor. Liu, ¶¶3, 6. The "pixel structure **is applied to an organic electroluminescence display** and has a structure comprising six thin film transistors and one capacitor (6TlC)," but it is not limited to the disclosed structure.[2] *Id.*, ¶¶32, 48, 50, 53, 58, 73, 75. Liu further explains the pixel structure includes an OLED. *Id.*, ¶¶48, 58, FIGs. 1, 6.

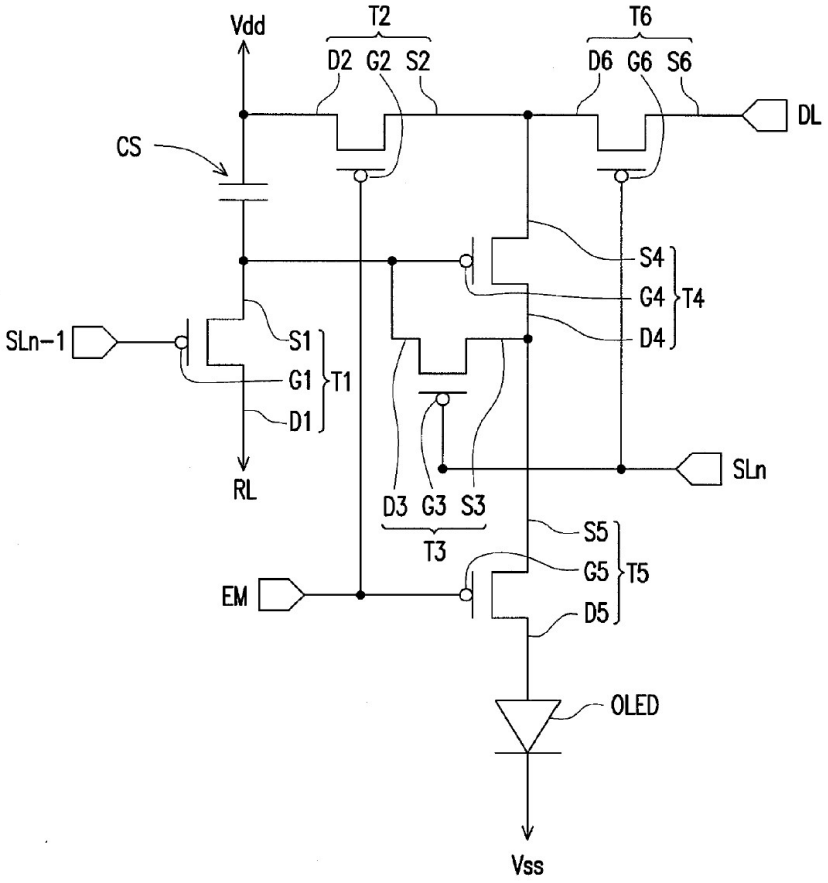


FIG. 1

115. Liu is further directed to reducing the area occupied by the pixel

[2] All emphases are added unless otherwise noted.

structure for use in high resolution displays. Liu, ¶¶6-7. For example, Liu explains that "[t]he pixel structure of Figure 6 is a pixel structure **in an organic electroluminescence display**." *Id.*, ¶50. As explained below, the embodiment shown in FIGS. 1-6 maps to the claims.

116. Accordingly, Liu discloses an OLED pixel structures utilized in a display ("[a]n organic light emitting diode display").

b. 1[a]: "a non-conductive substrate;"

117. In my opinion, Liu discloses this limitation.

118. Liu discloses "the pixel structure is disposed on a substrate 100 and comprises a semiconductor layer PO, a first insulating layer 102, a first conductive layer, Ml a second insulating layer 104, a second conductive layer M2, a third insulating layer 106, a third conductive layer M3 and a pixel electrode PE." Liu, ¶32, FIG. 5 (annotated below). Liu explains substrates may be made of glass, quartz, polymers, or ceramics, among other materials, which are known non-conductive materials. *Id.*, ¶33.

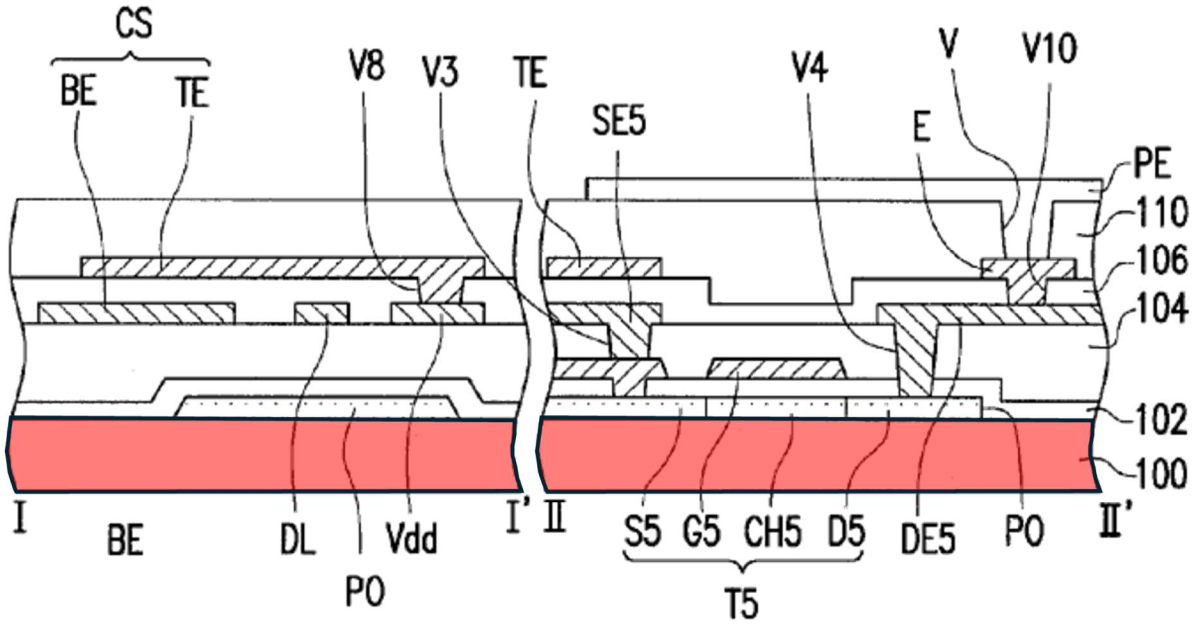


FIG. 5

Liu, FIG. 5 (annotated).

c. 1[b]: "a plurality of first voltage lines;"

1[c]: "a plurality of scan lines;"

1[d]: "a plurality of data lines;"

119. In my opinion, Liu discloses limitations 1[b]-1[d].

120. I have grouped each of the limitations 1[b]-1[d], which are directed to component connectivity in the pixel structure, for clarity and ease of discussion.

121. Plurality of Pixel Structures

122. As explained above in 1[pre], Liu discloses a pixel structure for use in an OLED display. §VIII.A.4.a. Each pixel structure includes TFTs, capacitor, and

OLED. *Id.* In my opinion, a POSITA would have understood that Liu's pixel structure constitutes one pixel in a display. Liu, ¶50. For example, as explained in Udagawa, pixels comprise the TFT driving circuits and OLEDs. Udagawa, ¶¶5-8.

123. Liu explains the pixel structure is limited in size and must be small for high resolution displays. Liu, ¶¶6-7. In my opinion, a POSITA would have understood that high resolution displays contain a plurality of pixel structures because each pixel structure containing an OLED makes up one light emitting portion (i.e., pixel) of the display, and the resolution is measured according to the number of pixels occupying the display area. Furthermore, the '991 Patent admits and confirms a POSITA's understanding that an "organic light emitting diode display includes a plurality of pixels." '991Pat., 1:45-49.

124. As explained below, because Liu teaches a plurality of pixels, Liu also teaches a plurality of voltage lines and driving circuits used in each pixel.

125. Plurality of First Voltage Lines (1[b]), Scan Lines (1[c]), and Data Lines (1[[d])

126. Liu discloses the "first voltage line" as a "power line Vdd" in the second metal layer M2. Liu, ¶42, FIG. 1 (annotated below). In my opinion, a POSITA would have understood Vdd is a "voltage line" because Vdd is common notation to denote a voltage to drive a transistor. Moreover, the '991 Patent uses the same notation, Vdd, to identify a "voltage line." '991Pat., 6:25-37 ("a driving voltage line 172 for

transferring a driving voltage ELVDD.").

127. Liu further discloses scan lines (SLn and SLn-1) in the TFT circuit. Liu, ¶38; Table, *infra*. Here, I note that Liu references these scan lines with the nomenclature "n" and "n-1" signifying a plurality of scan lines, not limited to the two shown in the circuit. Each pixel structure further includes a data line, DL, used in each pixel structure of a display. *Id.*, ¶42; Table, *infra*.

128. As explained above, a POSITA would have understood that Liu's circuit (Figures 1-6) represents one of a plurality of pixel structures, all used in the disclosed display and requiring voltage lines, scan lines, and data lines to be supplied to them. Accordingly, Liu discloses "a plurality of" voltage, scan, and data lines to each pixel structure.

129. Figure 1 shows "a schematic circuit diagram of a pixel structure." Liu, ¶31. I have also reproduced annotated Figure 1 of Liu alongside Figure 1 of the '991 Patent to show the similarities between the circuits and to show Vdd, scan lines, data lines.

FIG. 1

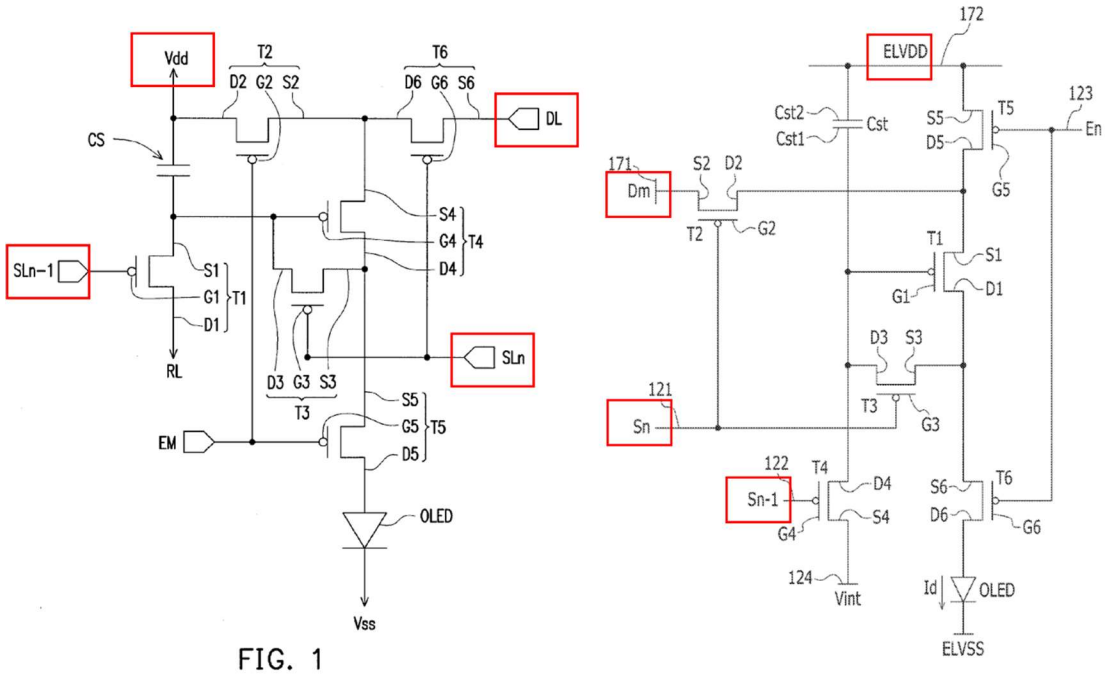


FIG. 1

Left: Liu, FIG. 1 (annotated); Right: '991Pat., FIG. 1 (annotated).

130. Mapping of Liu to '991 Patent

131. In addition, I have provided the table below to cross-reference each transistor and signal line of '991 Patent to the similarly-described elements in the disclosure of Liu.

Claims	'991	Liu	Function
1st TFT	T2	T6	Data input switching TFT
2nd TFT	T1	T4	Driving TFT
3rd TFT	T5	T2	Charging/Power supply / Operation Control TFT
4th TFT	T6	T5	Emission control TFT
5th TFT	T3	T3	Scan[n] switch TFT
6th TFT	T4	T1	Scan[n-1] Init switch TFT
Capacitor	Cst	CS	Storage Capacitor

First Capacitor Plate	125h	BE	
Second Capacitor Plate	127	TE	
1st Voltage line	ELVDD	Vdd	Power supply
2nd Voltage line	Vint	RL	Capacitor initialization voltage
OLED	OLED	OLED	
1st Scan line	Sn	SLn	Current scan line
2nd Scan line	Sn-1	SLn-1	Previous scan line
Light emission control line	En	EM	Light emission control
Data line	Dm	DL	Data/OLED intensity voltage

d. 1[e]: "a plurality of driving circuits formed on the substrate;"

1[f]: "a plurality of organic light emitting diodes, wherein each of the plurality of organic light emitting diodes is electrically coupled to a respective one of the plurality of driving circuits;"

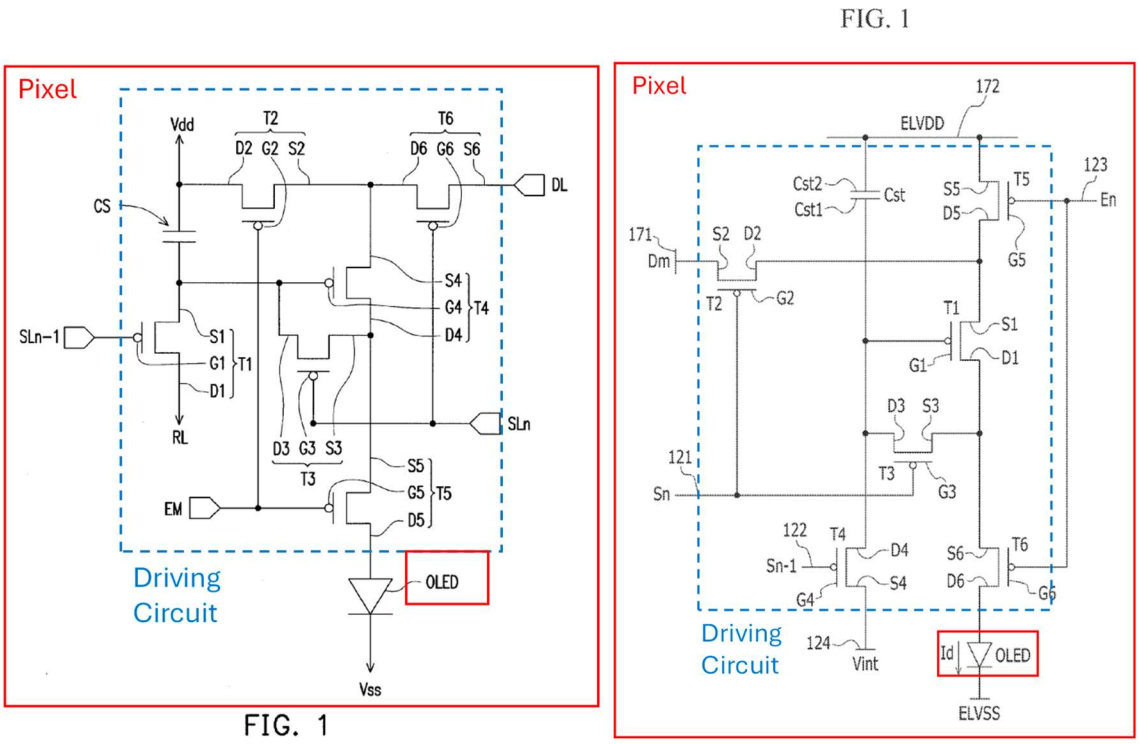
132. In my opinion, Liu teaches or suggests limitations 1[e] and 1[f].

133. I have grouped both these limitations 1[e] and 1[f], which are directed to components of the OLED display, for clarity and ease of discussion.

134. As explained above in 1[b], Liu teaches or suggests multiple pixel structures (i.e., pixels) in a display. §VIII.A.4.c. Liu further describes a "plurality of driving circuits" because it describes a driving circuit for each of the plurality of pixels, where each driving circuit comprises a plurality of TFTs to drive the OLED for that pixel. Liu, ¶¶6 ("A pixel structure of the organic light emitting device in the display is usually driven by the cooperation of a plurality of thin film transistors

(TFTs) and a capacitor."), 8, FIG. 1. Furthermore, I note that the '991 Patent admits a "plurality of thin film transistors and capacitors…driv[e] the organic light emitting diode," confirming the understanding of a POSITA in this regard. '991Pat., 1:45-49.

135. As shown below, each of the TFT driving circuits is connected to an OLED ("a plurality of organic light emitting diodes"). *Id.*, ¶31, FIG. 1 (annotated). I have reproduced and annotated Figure 1 of Liu alongside Figure 1 of the '991 Patent to show the relationship of a pixel and driving circuit.



Left: Liu, FIG. 1 (annotated); Right: '991Pat., FIG. 1 (annotated).

136. Furthermore, Liu explains that the TFTs are formed in a semiconductor layer that is formed on the substrate ("a plurality of driving circuits formed on the substrate"). *Id.*, ¶¶8, 34-35, FIGs. 1-6. The substrate is shown in annotated Figure 5

in 1[a]. §VIII.A.4.b. The TFTs of the driving circuit are annotated in Figure 3A, showing the semiconductor layer deposited on the substrate. *Id.*, ¶15, FIG. 3A (annotated)[3]. Liu further explains that "the pixel structure is disposed on a substrate 100 and comprises a semiconductor layer PO" and that the substrate can be a "wafer." Liu, ¶¶8, 33. In my opinion, a POSITA would have thus understood that the plurality of Liu's driving circuits, including the plurality of TFTs would have been formed on a single substrate because it was common practice at the time to use a single substrate in wafer form to form multiple pixels.

[3] FIG. 3A has been annotated based on the component positions shown in FIGS. 2 and 3C, and the explanations in Liu. Liu, ¶¶34-35, 41, 44, FIGs. 2, 3A, 3C.

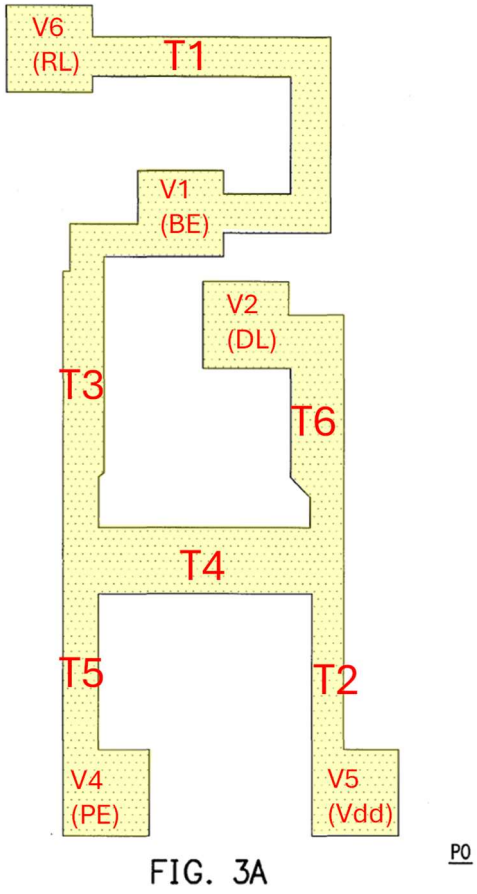


FIG. 3A

Liu, FIG. 3A (annotated).

137. Furthermore, as shown in annotated Figure 6 below, the OLED is directly connected to the "driving circuit" through "E" and V ("each of the plurality of organic light emitting diodes is electrically coupled to a respective one of the plurality of driving circuits"). Liu, ¶¶44-48, FIG. 6 (annotated).

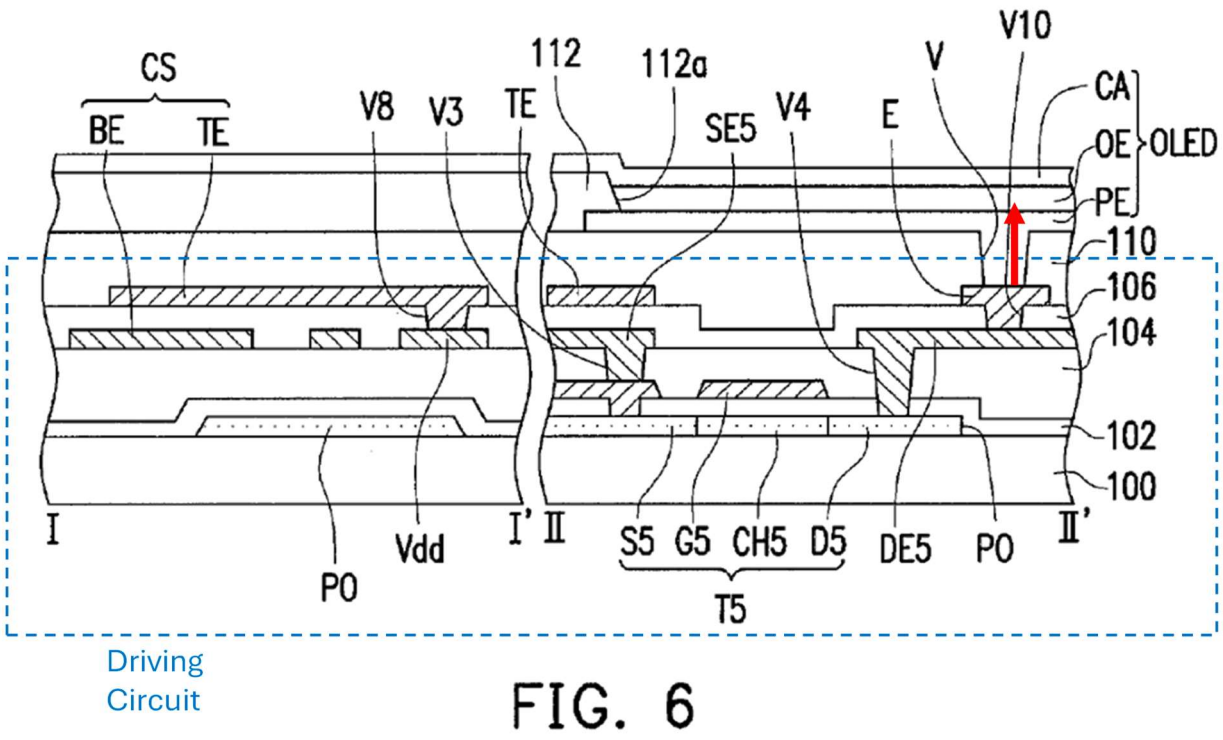


FIG. 6

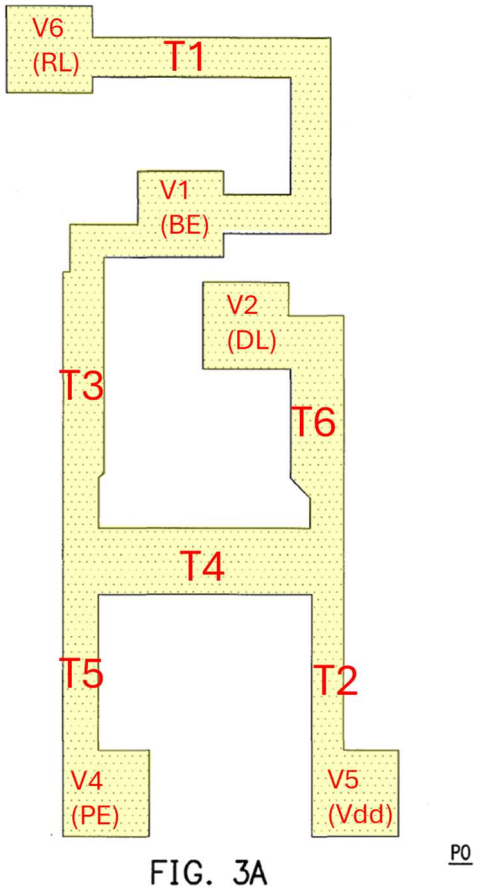
Liu, FIG. 6 (annotated).

e. 1[g]: "wherein each of the driving circuits comprises: a first thin film transistor implemented in a first portion of a semiconductor layer disposed on the substrate, and coupled to one of the plurality of scan lines and to one of the plurality of data lines;"

138. In my opinion, Liu teaches or suggests limitation 1[g].

139. Liu discloses the "first thin film transistor" as T6 that is coupled to "the first scan line," SLn, and "a data line," DL, as shown in Liu's Figure 1. Liu, ¶¶38, 42. As explained in 1[e], each pixel structure includes several TFTs arranged in a driving circuit. §VIII.A.4.d. As explained above in 1[e], each of the TFTs in the driving circuits is formed in a portion of the semiconductor layer on the substrate

("implemented in a first portion of a semiconductor layer disposed on the substrate"). *Id.*; Liu, ¶¶34-35 ("the semiconductor layer PO…region predetermined for forming…transistor T6"); *see also* FIG 3A (annotated below).



Liu, FIG. 3A (annotated).

140. I note, referring to Liu's circuit diagram below, that Liu explains that a data line "is electrically connected to the source region S6" of T6 ("first thin film transistor"), and scan line SLn is connected to the gate G6 of T6. *Id.*, ¶38, FIG. 1 (annotated).

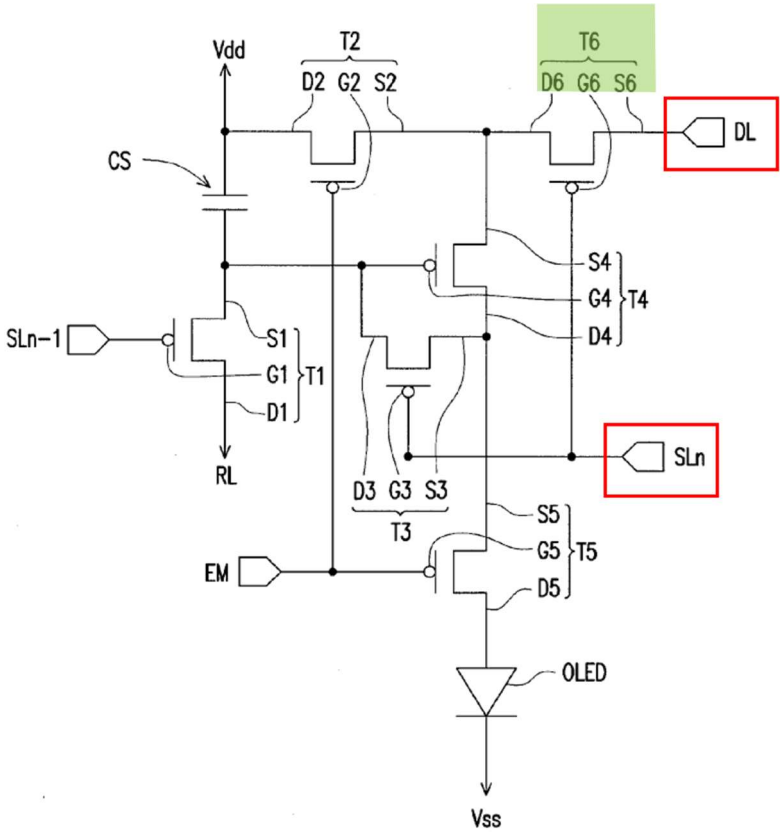


FIG. 1

Liu, FIG. 1 (annotated).

141. Furthermore, as will be explained below, Liu discloses each of the six transistors and the capacitor recited in 1[h]-1[m]. The table in 1[b] above shows the mapping of Liu's circuit components to those recited in the '991 Patent. *See* §VIII.A.4.c (table).

142. Accordingly, limitation 1[g] is disclosed by Liu.

f. 1[h-1]: "a second thin film transistor implemented in a second portion of the semiconductor layer, wherein the semiconductor layer couples the second thin film transistor to the first thin film transistor, and"

143. In my opinion, Liu teaches or suggests limitation 1[h-1].

144. As shown in Liu's Figure 1 circuit below, Liu discloses the "second thin film transistor" as TFT T4. As explained above in 1[e], T4 is formed in a portion of the semiconductor layer on the substrate ("implemented in a second portion of the semiconductor layer"). §VIII.A.4.d; Liu, ¶35 ("the semiconductor layer PO…region predetermined for forming…transistor T6"). As shown in Liu's annotated Figure 3A below, T4 is formed in a different portion in the semiconductor layer that includes T6 ("first thin film transistor") adjacent to T4. In my opinion, and because the semiconductor layer is continuous from T4 to T6, a POSITA would have understood "the semiconductor layer couples" T4 to T6.

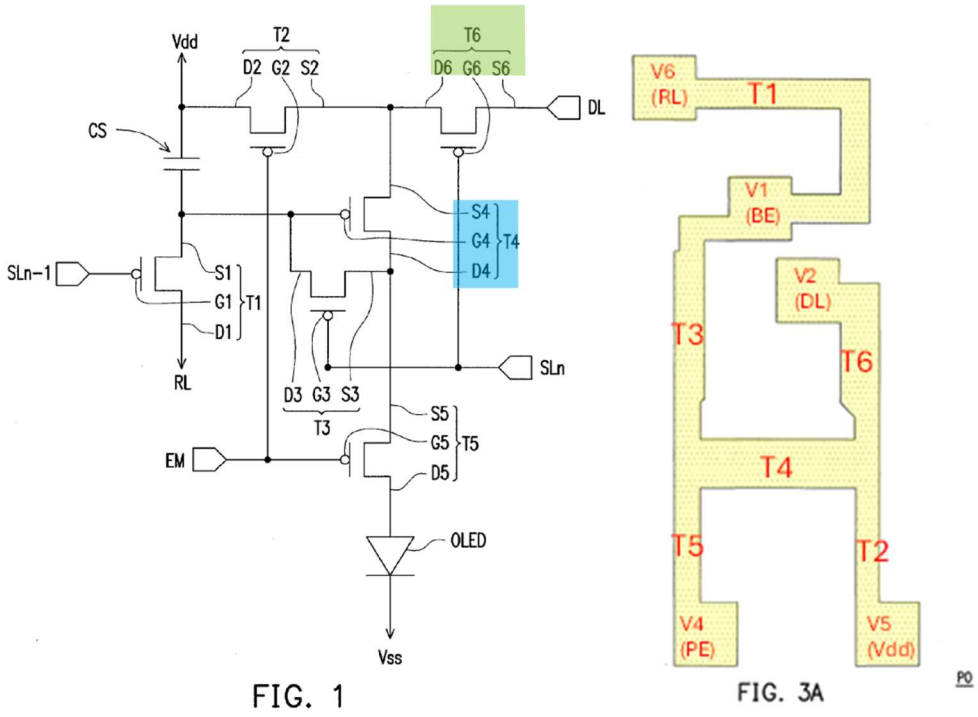


FIG. 1 FIG. 3A

Left: Liu, FIG. 1 (annotated); Right: Liu, FIG. 3A (annotated).

g. 1[h-2]: "wherein the second portion of the semiconductor layer has at least one bent portion;"

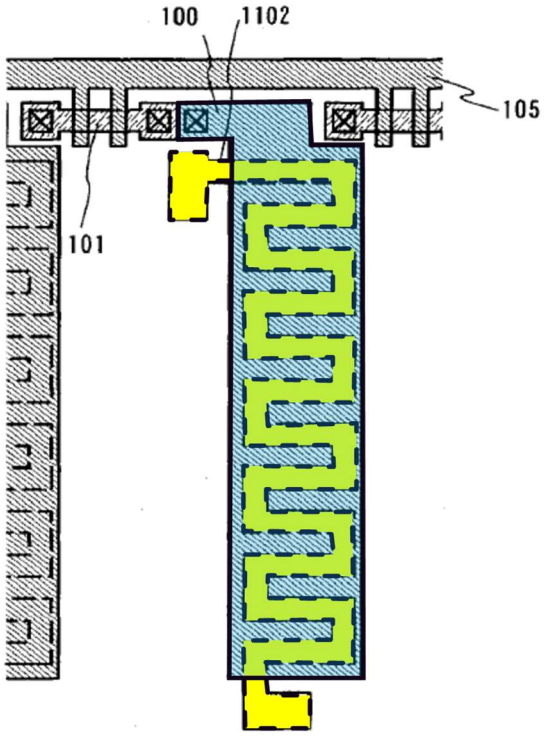
145. In my opinion, Liu in combination with Udagawa teaches or suggests limitation 1[h-2].

146. Although Liu does not expressly disclose a "bent" portion of the semiconductor layer for T4, it is my opinion that a POSITA would have found it obvious to modify Liu to use Udagawa's serpentine ("bent") gate channel for drive transistor T4 because, for example, Liu describes a polysilicon material for implementing its semiconductor layer. Liu, ¶34. It was well-known in 2012 that the miniaturization of TFT circuits in polysilicon caused problems related to the

electrical characteristics of the TFTs. Udagawa, ¶¶5-15. One issue is that dispersion between pixels increases because the channel length of the drive transistor decreases. *Id.*, ¶¶11-13, 16-17. In particular, it was known that dispersion was caused by the driving TFT. *Id.*, ¶17. Thus, a POSITA would have been motivated to look for other references, such as Udagawa, that recognized this problem and provided a solution to reduce the dispersion effects of polysilicon TFTs in OLED driving circuits.

147. Udagawa discloses that dispersion is reduced "[w]hen the channel length of the TFT that supplies an electric current to the OLED is made longer." Udagawa, ¶22. Accordingly, Udagawa explains that various shapes can be used, such as a "snake" shape, as shown below. *Id.*, ¶31, FIG. 13A (annotated). Annotated below, Udagawa's Figure 13A shows a snake-like (i.e., bent or serpentine) channel 1102 (yellow) with gate electrode 100 (blue) covering the channel region. Udagawa, ¶¶31, 102, 154.

Fig. 13A



Udagawa, FIG. 13A (annotated).

148. As I have explained in §VIII.A.3, a POSITA would have been motivated to incorporate Udagawa's driving TFT gate shapes (thereby increasing the channel length) in Liu's miniaturized OLED driving circuit to reduce the dispersion effects that accompany the reduction in size of the driving circuit. Furthermore, modifying Liu to use Udagawa's longer gate channel is in line with Liu's objectives of reducing the size of the pixel structure because forming the gate channel in this way allows for both a reduction of dispersion and maintaining a reduced size due to the winding nature of the extended channel while enabling an improved operation of the driving TFT.

149. Moreover, I note that since Udagawa described that different lengths and numbers of serpentine structures can be used to implement the extended channel (see Udagawa, ¶20), a POSITA would have understood that Liu's T4 channel region can be similarly designed by choosing the length of the channel based on the constraints of a particular design. Udagawa recognizes this versatility in selecting channel lengths in Figures 3 and 4. *Id*. For example, Udagawa explains that various channel lengths can be used. Udagawa, ¶20. Thus, using Udagawa's serpentine gate channel structure would not have substantially increased Liu's pixel structure size because a POSITA would have understood that the length of the channel, and thus the footprint that it occupied, can be selected to conform to the desired requirements.

150. Additionally, or alternatively, it is my opinion that a POSITA would have understood that the serpentine channel of Udagawa can be implemented without changing the footprint of Liu's pixel structure by extending the channel area slightly above or slightly below its current real estate; as noted above, due the serpentine nature of the channel and the ability to select the extended channel length, any additional expansion would have been readily implemented within the existing pixel footprint. It is also my opinion that a POSITA would have been more than capable of sizing the gate electrode (BE) to cover an appropriate portion of the modified channel.

151. Accordingly, Liu as modified by Udagawa teaches a serpentine gate

channel for T4 ("the second portion of the semiconductor layer has at least one bent portion").

h. 1[i]: "a storage capacitor comprising: a first capacitor plate that is configured to operate as a gate electrode of the second thin film transistor;"

152. In my opinion, Liu teaches or suggests limitation 1[i].

153. Liu discloses the "storage capacitor" as capacitor CS that is connected on one side to the gate electrode of T4 ("a gate of the second transistor"), and includes a bottom electrode, BE, ("first capacitor plate") and top electrode, TE ("second capacitor plate"). *See* Liu, ¶¶42, 44-45, 47, 53, FIGs. 1, 2, 3C, 3D, 4-6.

154. Liu's capacitor CS is "disposed in the capacitor region CR and includes a bottom electrode BE and a top electrode TE." Liu, ¶53. Liu explains that because the semiconductor layer is not used as an electrode for the capacitor (i.e., the capacitor plates are in the metal layers), CS "can be disposed overlapping with the semiconductor layer PO, so as to reduce an area occupied by components of the pixel structure." Liu, ¶47. In other words, even though CS overlaps several of the TFTs (as shown in Figure 2), it does not activate them. Liu further discloses capacitor CS is connected to the gate of T4 ("configured to operate as a gate electrode of the second thin film transistor"), as shown by the red line in Figure 1. Liu, FIG. 1 (annotated).

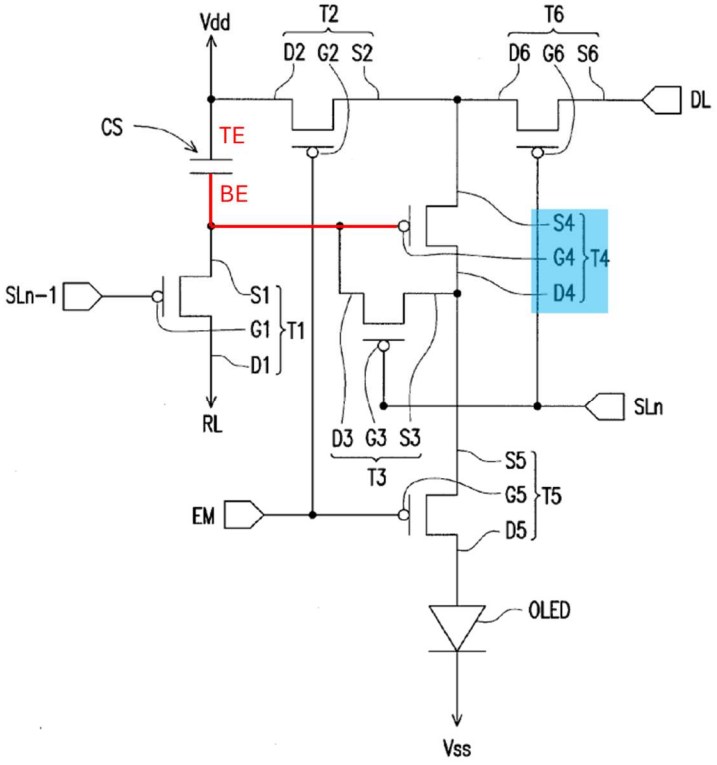


FIG. 1

Liu, FIG. 1 (annotated).

155. Liu further explains that the gate of T4 is below and connected to BE. Liu, ¶¶41, 54. As shown in annotated Figure 5, the gate of T4 that is on M1[4] is directly connected to bottom electrode BE ("a first capacitor plate") on M2 through

[4] A note on the nomenclature: Liu uses abbreviations M1 and M2 to denote the first conductive layer and the second conductive layer, respectively; these layers provide electrical conductivity and are made of metal materials. *See* Liu, ¶¶32, 37, 40. A "via" or a "contact via" is a metal structure that connects one metal component to another metal component in a vertical direction. *See, e.g., Id.* ¶44.

via V3. *See also* Liu, FIGs. 2, 3B, 3C, 3D. In my opinion, a POSITA would have thus recognized that BE comprises a portion of and operates as the gate electrode of T4 ("configured to operate as a gate electrode of the second thin film transistor") because the via directly connects the two together, electrically and physically. *Id.*

156. With respect to Figure 5, I note that BE is labeled correctly, however, SE5 is an incorrect label and the element should be labeled as BE. It is my opinion that a POSITA would have understood the incorrect labeling because, although SE5 is mentioned in the specification (paragraph 40), there are no vias or metal shown in Figures 3B-4 that would denote such a structure. Furthermore, Figure 1 clearly shows that S5 is connected to D4, and as shown in Figure 3A, the connection is made in the semiconductor layer without any connections to other layers. In Figure 5, V3 is shown to be SE5, which is in conflict with Figure 1 because such an equivalence would connect S5 to G4. Regardless, the connection of BE to the gate electrode is clearly shown.

157. I further note that the structure labeled as "Gate of T4" below is on the M1 layer and is shown in Figure 3 (unlabeled). *See* FIG. 3B (unlabeled portion), and that via V3 directly connects the gate electrode of T4 to BE above it. V3 is further shown in Figure 3C, connecting BE to the level below (shown in Figure 3B).

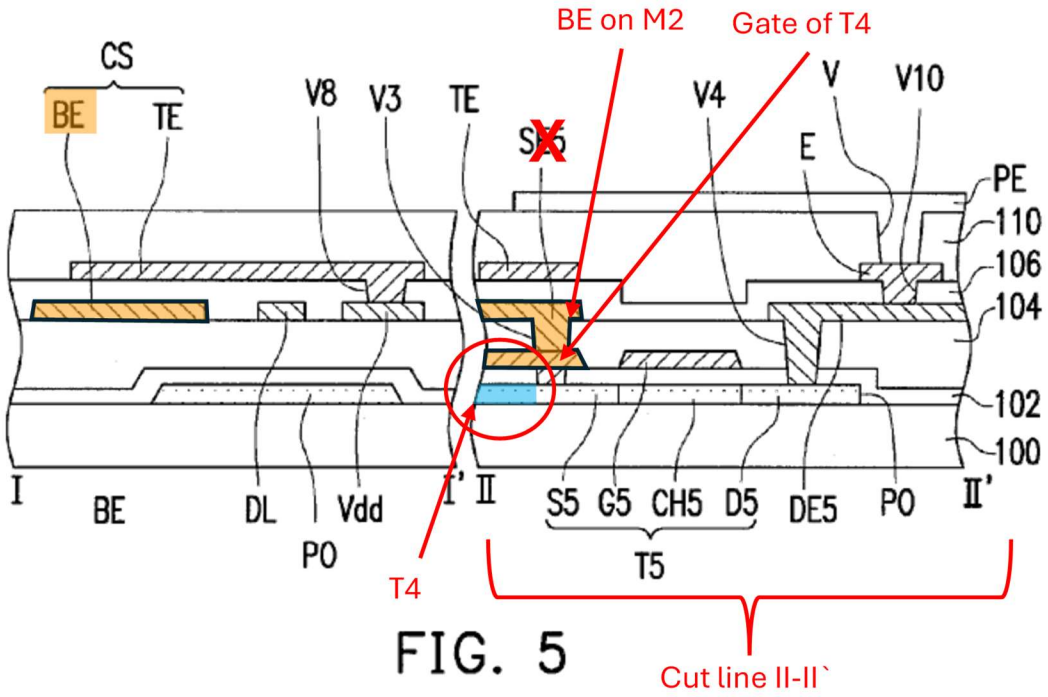
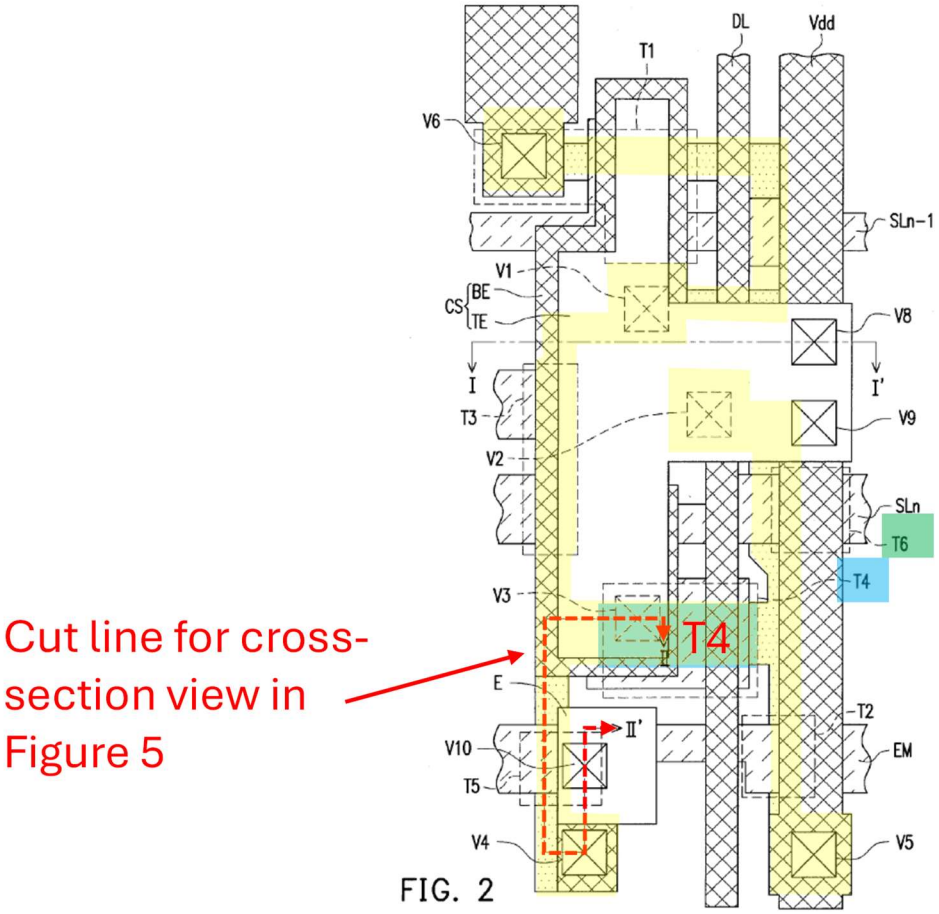


FIG. 5

Liu, FIG. 5 (annotated).

158. In my opinion, a POSITA would have this understanding because the cut line II-II` in Figure 2 passes directly through T4, and is shown in Figure 5. Additionally, Figure 2, which has been annotated to show the semiconductor layer PO (yellow), T6, T4, and the cross-section lines for Figure 5, is shown below.



Liu, FIG. 2 (annotated).

159. To the extent it is argued that BE is not configured to operate as the gate electrode of T4, it is my opinion that a POSITA would have found it obvious based on the teachings of Liu to use BE directly as the gate electrode of T4. I note that using the capacitor plate directly as the gate electrode is well-known in the art, as shown in Park '811, Ono, and Kakinuma. For example, Liu explains various changes to the capacitor design that include adjusting the capacitor dielectric material and/or its thickness, allowing the size of the capacitor to be changed while maintaining a selected capacitance. Liu, ¶53. For example, Liu explains that by

thinning the dielectric, the area of CS can be reduced, allowing it to be placed directly over the semiconductor layer: "the semiconductor layer PO may be disposed under the capacitor CS (not shown) to increase the design convenience." *Id.* A POSITA would have thus found it obvious to position the bottom capacitor plate BE ("first capacitor plate") directly over the semiconductor layer of T4 as taught by Liu (e.g., using the gate electrode of T4 as shown in Figure 3B); BE (or at least a part or portion of BE) would operate as the gate electrode of T4 with such a placement. Thus, in my opinion, a POSITA would have found this modification obvious because Liu expressly described it, and would have further sized the gate electrode of T4 (e.g., BE) based on the length and the width of the channel of T4.

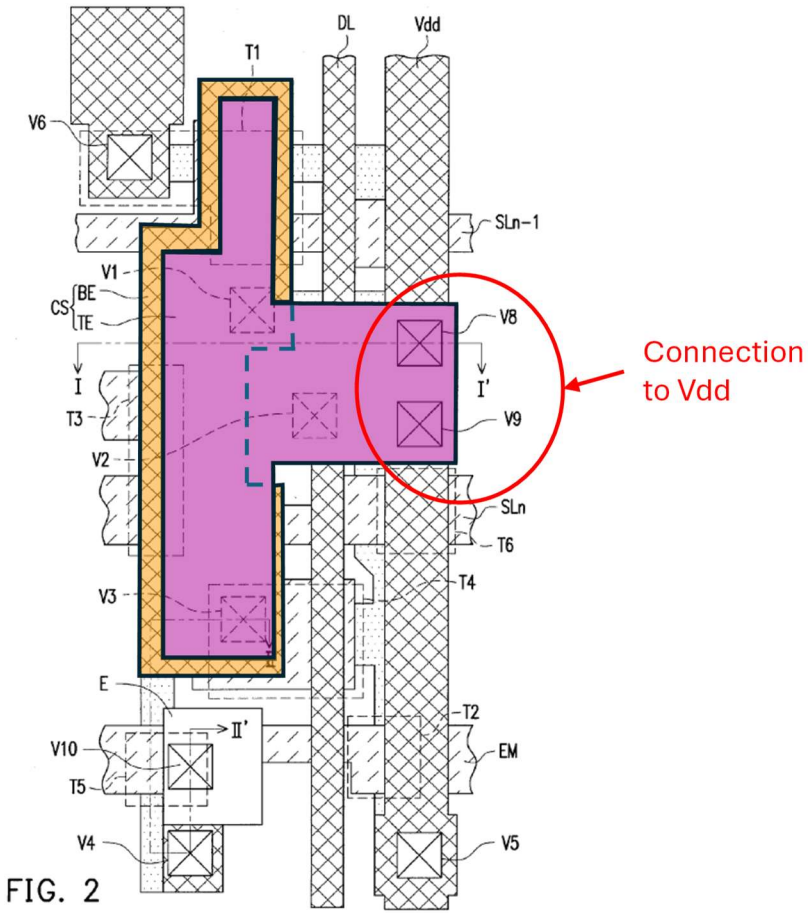
160. Accordingly, limitation 1[i] is disclosed by Liu.

i. 1[j]: "a second capacitor plate electrically coupled to one of the plurality of first voltage lines and overlapping the first capacitor plate; and"

161. In my opinion, Liu teaches or suggests limitation 1[j].

162. As explained above, capacitor CS comprises BE ("a first capacitor plate") and TE ("a second capacitor plate"). Liu, ¶53; §VIII.A.4.h. As shown in annotated Figure 2 below, top electrode TE, which is in M3, overlaps bottom electrode BE, which is in M2. Liu, ¶¶45. Furthermore, Liu discloses that "the top electrode TE is electrically connected to the power line Vdd through contact via

structures V8-V9." Liu, ¶44, FIGs. 2, 3D, 5. Thus, TE is connected to Vdd in the pixel structure ("electrically coupled to one of the plurality of first voltage lines."



Liu, FIG. 2 (annotated).

163. Accordingly, limitation 1[j] is disclosed by Liu.

j. 1[k]: "an insulating layer between the first capacitor plate and the second capacitor plate;"

164. In my opinion, Liu teaches or suggests limitation 1[k].

165. Liu discloses a first insulating layer 102 over PO, a second insulating layer 104 over M1, and a third insulating layer 106 over M2. Liu further discloses

"capacitor CS…formed with the top electrode TE of the third conductive layer M3, the bottom electrode BE of the second conductive layer M2 and the **third insulating layer 106 between the bottom electrode TE and the bottom electrode BE**." Liu, ¶45.

166. Furthermore, it would have also been obvious based on the teachings in Liu to position BE directly over the semiconductor layer of T4 in M1. §VIII.A.4.h. Liu, ¶32. It is my opinion that when moving BE to M1 to be directly over the semiconductor layer, TE need not be correspondingly moved. This is because moving or not moving TE to M2 is a design choice dependent on factors related to layout. If TE remains in M3, insulating layers 106 and 104 would be designed with the appropriate thickness. However, if TE were moved to M2, such that it was in the metal layer directly above BE, then dielectric layer 104, M1, is the "insulating layer" as claimed. It is my opinion that these choices and their implementations were well within the capabilities of a POSITA and would have been obvious in view of the express description of Liu regarding those design choices.

167. Accordingly, limitation 1[k] is disclosed by Liu.

k. 1[l]: "a third thin film transistor implemented in a third portion of the semiconductor layer, wherein the semiconductor layer couples the third thin film transistor to the first thin film transistor and to the second thin film transistor, and wherein the third thin film transistor is electrically coupled to one of the plurality of first voltage lines through the semiconductor layer; and"

1[m]: "a fourth thin film transistor implemented in a fourth portion of the semiconductor layer, wherein the semiconductor layer couples the fourth thin film transistor to the second thin film transistor, and wherein the fourth thin film transistor is electrically coupled to the respective organic light emitting diode through the semiconductor layer; and"

168. In my opinion, Liu teaches or suggests limitations 1[l] and 1[m].

169. I have grouped both limitations 1[l] and 1[m], which are directed to the third and fourth TFTs, for clarity and ease of discussion.

170. As I have explained in 1[pre] and 1[g], Liu discloses a TFT driving circuit with at least six transistors and one capacitor. §§VIII.A.4.a, VIII.A.4.e. As explained below and shown in annotated FIGS. 1 and 3A, Liu discloses each of the recited transistors and connections.

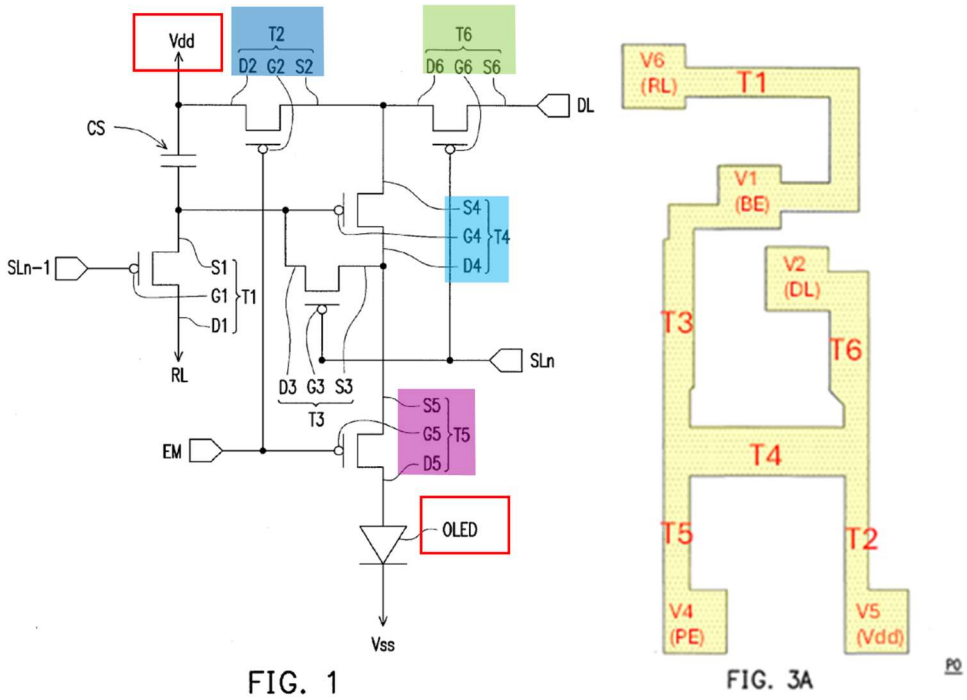


FIG. 1 FIG. 3A

Left: Liu, FIG. 1 (annotated); Right: Liu, FIG. 3A (annotated).

171. Regarding 1[l], Liu discloses T2 ("third thin film transistor") is formed in a portion of the semiconductor layer on the substrate ("implemented in a third portion of the semiconductor layer"). Liu, ¶35 ("the semiconductor layer PO…region predetermined for forming…transistor T2"). Liu further discloses T2 is connected to Vdd ("electrically coupled to one of the plurality of first voltage lines"), and T2 is connected to T6 and T4 ("the third thin film transistor [coupled] to the first thin film transistor and to the second thin film transistor"). *See* Liu, FIG. 1 (showing the connectivity of T2 to T4, T6 and Vdd). As also shown in annotated Figure 3A (above), T2 is connected to Vdd in the pixel structure ("one of the plurality of first voltage lines") through via V5 at the semiconductor layer. *Id.*, FIGs. 2, 3A, 3C. T2

is further connected to and adjacent to T4 and T6 in the semiconductor layer ("the semiconductor layer couples"). Liu, ¶35, FIG. 3A (annotated).

172. Regarding 1[m], Liu discloses T5 ("fourth thin film transistor") is formed in a portion of the semiconductor layer on the substrate ("implemented in a fourth portion of the semiconductor layer"). Liu, ¶35 ("the semiconductor layer PO…region predetermined for forming…transistor T5"). Liu further discloses T5 connected to T4 ("the fourth thin film transistor [coupled] to the second thin film transistor"), and OLED ("fourth thin film transistor is electrically coupled to the respective organic light emitting diode"). *See* Liu, FIG. 1 (showing the connectivity of T5 to T4 and OLED). As also shown in annotated Figure 6 below, T5 is connected to OLED in the pixel structure through vias V4 and V10 through the semiconductor layer ("respective organic light emitting diode through the semiconductor layer"). *Id.*, ¶46, FIGs. 2, 5. T2 is further connected to T4 in the semiconductor layer. Liu, ¶35, FIG. 3A (annotated).

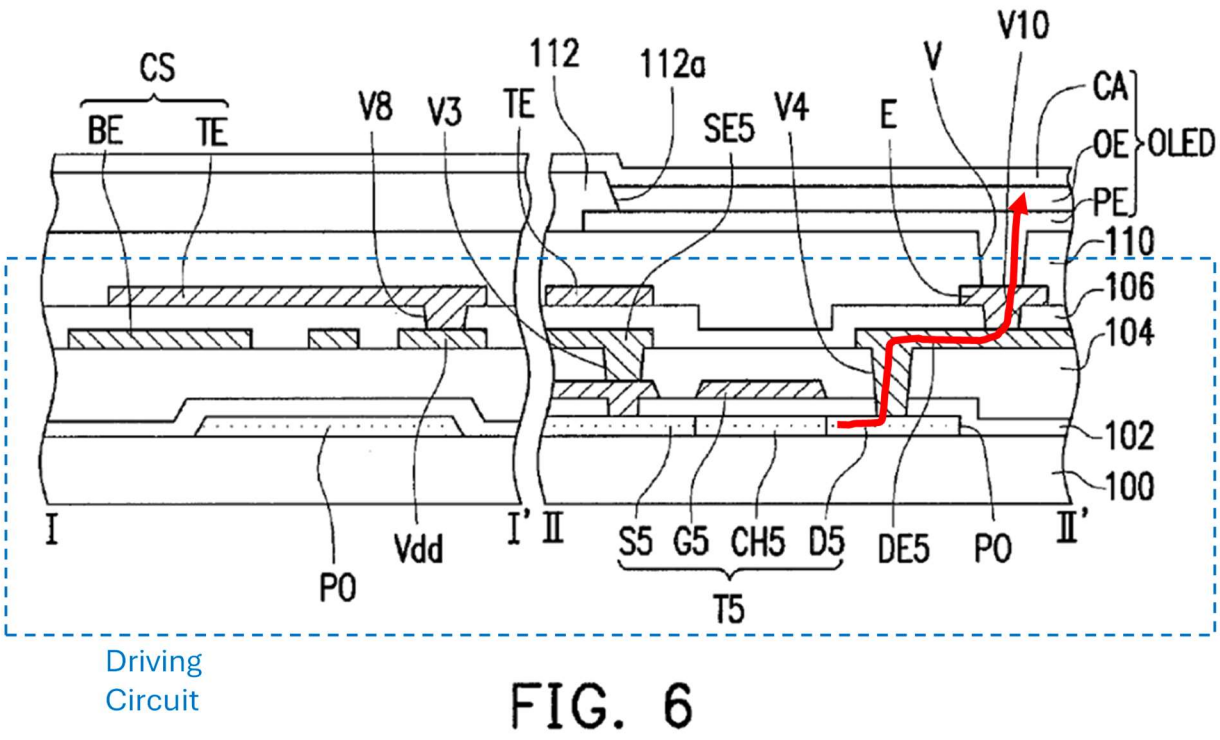


FIG. 6

Liu, FIG. 6 (annotated).

173. Accordingly, the electrical connections recited in limitations 1[l] and 1[m] are disclosed by Liu.

l. 1[n]: "wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate."

174. In my opinion, Liu in combination with Udagawa teaches or suggests limitation 1[n].

175. As also explained above in 1[i], in Liu, BE ("first capacitor plate") is either directly connected to the gate electrode of T4 in M1 or can be reduced in size and placed directly over the semiconductor layer of T4 in M1. §VIII.A.4.h.

Accordingly, in either scenario, BE is above T4. *Id.*; Liu, ¶¶47, 53, FIG 2. Liu further shows the channel region of T4 is directly under BE (gate electrode) (shown in blue) ("the [bent] portion of the second portion of the semiconductor layer is under the first capacitor plate"). Liu, FIG. 2 (annotated). As shown below, Figure 2 has been annotated to show Figure 3A superimposed under it. I note that the channel of T4 is the region of the semiconductor layer under the gate electrode of T4. This is a common structure in semiconductor engineering, and the gate electrode is typically sized base on the length and width of the channel. Accordingly, T4's modified serpentine channel, which is in the semiconductor layer, is under BE. While, in the combination, BE does not necessarily need to be adjusted in size to accommodate the addition of the serpentine structure as taught by Udagawa, it is my opinion that a POSITA would have found the adjustment an obvious and a routine task to ensure that the modified channel area is under BE.

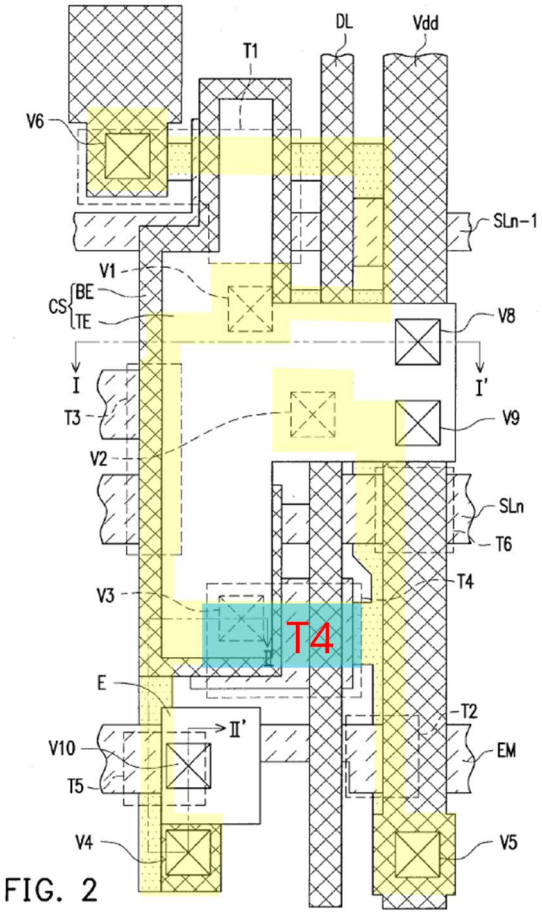


FIG. 2

Liu, FIG. 2 (annotated with FIG. 3A underlying it).

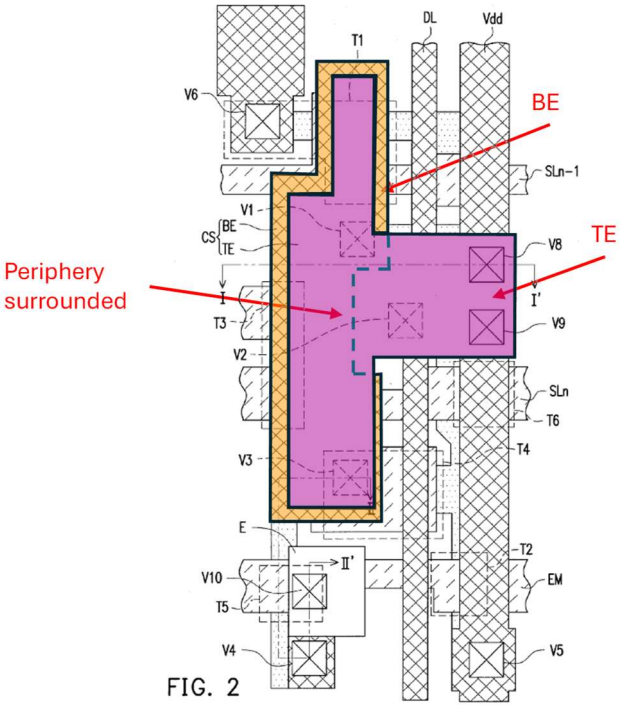
176. Accordingly, limitation 1[n] is disclosed by Liu in combination with Udagawa.

5. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view."

177. In my opinion, Liu teaches or suggests claim 2.

178. Liu teaches that TE ("second capacitor plate") surrounds a portion of BE (as shown in annotated Figure 2 below), and it is my opinion that the dashed line

represents "a" periphery of the BE (orange), which is surrounded by the top electrode plate (purple). Here, a POSITA, based on the plain and ordinary meaning of "surround[ing] a periphery," would have understood that at least a portion around the outside of BE would need to be surrounded by TE.[5] *Id.*; EX1015, 923 ("the outermost part or region within a precise boundary"); EX1016, 1066 ("the outer limits or edge of an area or object").



Liu, FIG. 2 (annotated).

[5] I note that claim 2 does not recite "entire periphery" or "entire surface area" to be surrounded; and the detailed description of the '991 patent neither explains nor attaches any particular significance to this limitation.

179. Accordingly, claim 2 is disclosed by Liu.

6. Claim 3

a. 3[a]: "An organic light emitting diode display according to claim 2, further comprising: a plurality of second voltage lines;"

180. In my opinion, Liu teaches or suggests limitation 3[a].

181. Liu discloses the "second voltage line" as a reference signal line "RL" that may be formed in the first metal layer M1 of each pixel structure. Liu, ¶38, FIG. 1 (annotated below). It is my opinion that a POSITA would have understood the reference signal line, RL, is also a "voltage line" because "signal line" is common terminology for circuit components that transmit voltages in transistor circuits; in addition, Liu's Figure 1 uses the same circuit symbol to represent the voltage lines Vss, Vdd, and RL, further corroborating RL's role as a voltage line. Moreover, RL corresponds to Vint in the '991 Patent, described as "initialization voltage line 124." '991Pat., 6:25-37 ("an initialization voltage line 124 for transferring an initialization voltage Vint for initializing the driving thin film transistor Tl"). I have reproduced annotated Figure 1 of Liu alongside Figure 1 of the '991 Patent to show RL and Vint. Furthermore, because Liu describes that each of the plurality of pixel structures includes the line RL, it is my opinion that a POSITA would have understood that Liu discloses a "plurality" of reference signal lines ("second voltage lines"). *See* §VIII.A.4.c.

FIG. 1

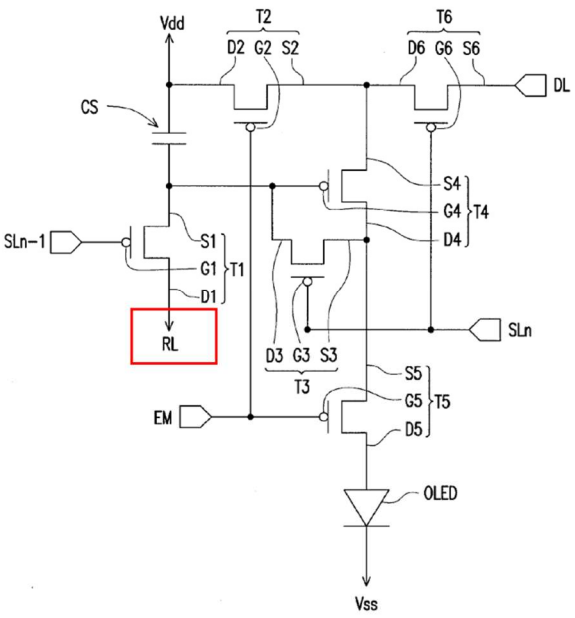
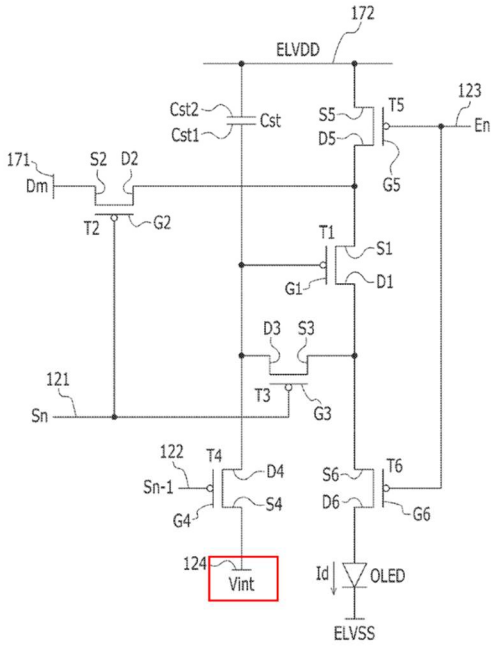


FIG. 1



Left: Liu, FIG. 1 (annotated); Right: '991Pat., FIG. 1 (annotated).

182. Accordingly, limitation 3[a] is disclosed by Liu.

b. 3[b]: "a fifth thin film transistor electrically coupled to the first capacitor plate; and"

3[c]: "a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,"

3[d]: "wherein the sixth thin film transistor is coupled to the fifth thin film transistor."

183. In my opinion, Liu teaches of suggests limitations 3[b]-3[d].

184. I have grouped each of limitations 3[b]-3[d], which are directed to the fifth and sixth TFTs, for clarity and ease of discussion.

185. Regarding 3[b], Liu discloses T3 ("fifth thin film transistor") connected to T4 and BE ("first capacitor plate"). Liu, FIG 1. Regarding 3[c] and 3[d], Liu discloses T1 ("sixth thin film transistor") connected to RL ("one of the plurality of second voltage lines"), T3, and BE. Liu, FIG 1. Accordingly, Liu discloses the TFTs and electrical connections in claim 3.

186. I have annotated Figure 1 of Liu (below) to show T3 and T1 and their respective connections.

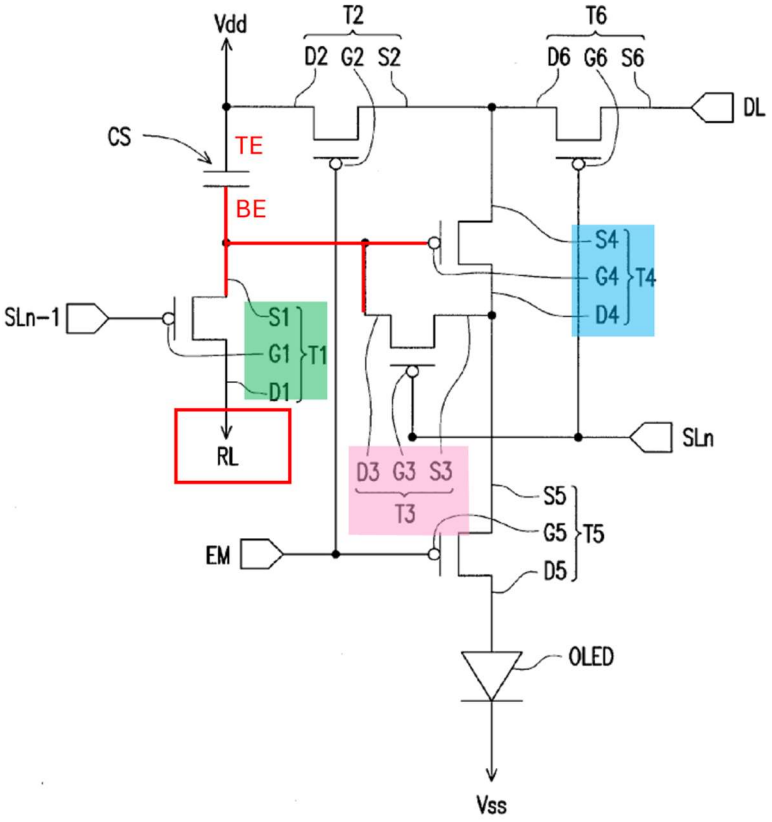


FIG. 1

Liu, FIG. 1 (annotated).

187. Accordingly, limitations 3[b]-3[d] are disclosed by Liu.

7. Claim 4: "An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer."

Claim 5: "An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material."

188. In my opinion, Liu teaches or suggests claims 4 and 5.

189. As I have explained above in 1[i], Liu teaches a storage capacitor where the bottom electrode BE ("first capacitor plate") operates as the gate electrode of T4. §VIII.A.4.h. As also explained, BE can be (a) reduced in size and placed directly over the semiconductor layer in M1, or (b) is directly connected to the gate electrode of T4 on M1. In scenario (a), BE is directly the gate of T4 and is in layer M1, and in scenario (b), BE directly connects to the gate electrode of T4 through connector V3, as shown in Liu's Figure 6.

190. Regarding claim 4, it is my opinion that a POSITA would have understood that Liu describes, at least in scenario (a), that BE ("first capacitor plate") is located in M1, along with scan lines SLn and SLn-1 ("plurality of scan lines"). Liu, ¶38 ("M1 has a gate G4…the first conductive layer M1 further comprises a scan line SLn, a scan line SLn-1").

191. Regarding claim 5, in either scenario (a) or (b), it is my opinion that a POSITA would have understood that the material of M1 is used for BE and the scan lines—SLn and SLn-1, and that a POSITA would have found it obvious that the

material in the via (V3) connecting BE to gate electrode of T4 (in M1) would be the metal material as the BE and the gate electrode of T4 in order to bond well and make a good connection. Furthermore, Liu describes that all of conductive layers, M1, M2 and M3, can be made of "made of metal materials" (Liu, ¶37), and thus it would have been obvious that the capacitor plate BE, connector V3, gate electrode of T4, and scan lines (all metal conductive components) would be made of the same metal material.

192. Accordingly, claims 4 and 5 are disclosed by Liu.

8. Claim 6: "An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines."

193. In my opinion, Liu teaches or suggests claim 6.

194. Liu discloses T3 ("fifth thin film transistor") connected to SLn. Liu, FIG 1. Liu further discloses T1 ("sixth thin film transistor") connected to SLn-1. Liu, FIG 1. Annotated Figure 1 below shows T3 and T1 and their respective connections.

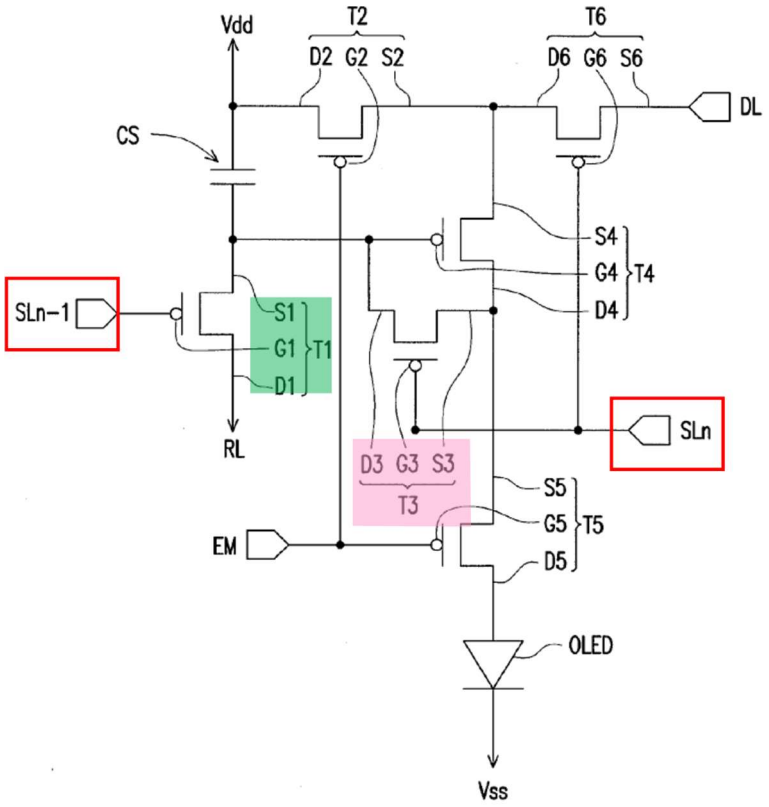


FIG. 1

Liu, FIG. 1 (annotated).

195. Accordingly, claim 6 is disclosed by Liu.

9. Claim 8: "an organic light emitting diode display according to claim 4, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer."

196. In my opinion, Liu teaches or suggests claim 8.

197. As explained regarding claim 4, Liu discloses that BE (and/or the gate

electrode of T4) and the scan lines are in the same metal layer M1 ("first metal layer"). §VIII.A.7. Liu further discloses that the data lines (DL) and Vdd ("first voltage lines") are in the same metal layer M2 ("third metal layer"). Liu, ¶42. Liu also discloses that TE is in metal layer M3 ("second metal layer").

198. Liu further discloses that RL ("second voltage lines") **may** be in metal layer M1. Liu, ¶38. Liu, however, does not **require** RL be in M1, and indeed shows RL in M2 in Figure 2 (i.e., in the same metal layer as DL and Vdd). I note here that T1 is shown connected to BE through V1 on one side and to an unlabeled metal line through V6 on the other, which corresponds to RL in Figure 1. RL is shown in annotated Figure 2 below.

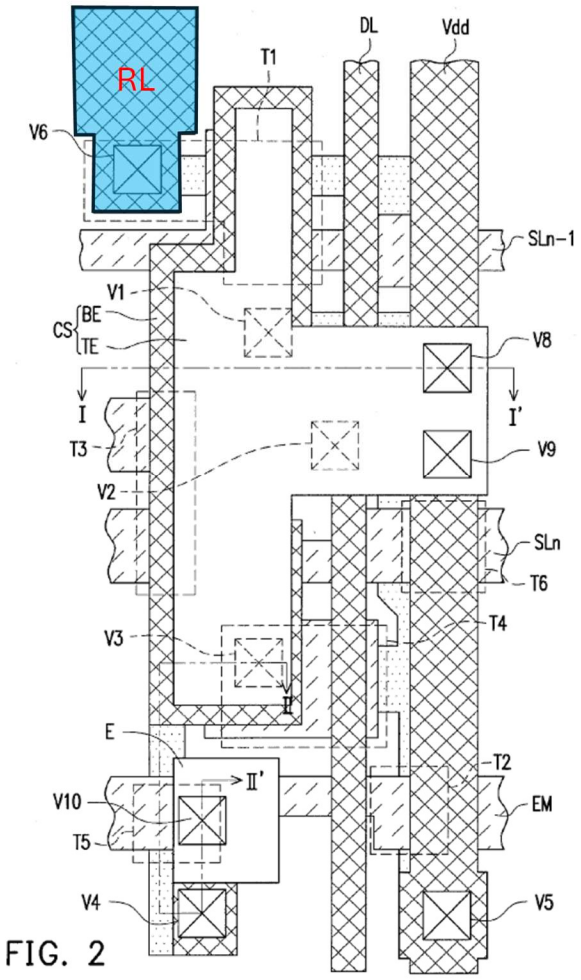


FIG. 2

Liu, FIG. 2 (annotated).

199. In my opinion, a POSITA would have understood and found it obvious that RL can be placed in any of M1, M2, or M3 at least because Liu's schematic layout does not place any other conductive structures overlapping RL. Such a modification amounted to a simple design choice that involved a routine task of making minor changes to the semiconductor pattern and was well within the skill set of a POSITA. Accordingly, RL as modified and placed in M3 ("second metal layer") would be in the same metal layer as TE. This is shown as Option A below.

	Claim 8	Liu's Teachings	Proposed modification – Option A: TE not moved	Proposed modification Options B: TE moved down
Scan lines	1st ML	M1	M1 (None)	M1 (None)
First voltage line (Vdd)	3rd ML	M2	M2 (None)	M3 (Move)
Second voltage line (RL)	2nd ML	M1, M2 (or M3)	Pick M3	M2 (None)
Data line (DL)	3rd ML	M2	M2 (None)	M3 (Move)
First capacitor plate (BE)	1st ML	M2 or M1	M1 (None)	M1 (None)
Second capacitor plate (TE)	2nd ML	M3	M3 (None)	M2 (Move)[6]

200. The above table illustrates the requirements of claim 8, the teachings of Liu, and the proposed modifications based on two different options for the placement of BE and TE. As explained above in 1[k], Liu teaches that its original configuration shown in Figures 2-4 can be modified to move the bottom capacitor electrode down and placed directly on the semiconductor layer. §4.j. As also explained in 1[k], a POSITA would have found it obvious that the top capacitor plate can remain in place (Option A) or be moved down to layer M2 below (Option B). §4.j. The above table

[6] As I have explained in 1[k], moving TE to M2 would have been obvious to a POSITA.

describes the changes (if any) a POSITA would have made in the two options.

201. In Option A, the choice would have simply been to pick M3 for placement of RL, as already suggested by Liu. In Option B, the modifications would have primarily included moving Vdd and DL to M3. In my opinion, a POSITA would have found this move obvious to avoid interference with TE. Such a modification amounted to a simple design choice that involved a routine task of making minor changes to the semiconductor pattern and was well within the skill set of a POSITA.

202. Moreover, it is my opinion that the placement of the elements as recited in claim 8 would have been obvious because (1) the ’991 patent does not provide any significance, benefit or advantage gained by the specific placement of the element in a specific metal layer, (2) their position in one of three metal layers would have amounted to selecting one of limited number of alternative positions, and (3) Vdd and DL could only be placed in either M2 or M3 in Liu’s design because a POSITA would have recognized that placing them in M1 was not possible because they would have then formed a gate signal to any semiconductor layer below. Accordingly, it would have been obvious that TE and RL would be in M2 (“second metal layer”) and Vdd and DL would be in M3 (“third metal layer”), as explained above.

203. Accordingly, claim 8 is disclosed by Liu.

10. Claim 9: "An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate."

204. In my opinion, Liu's teaching suggests claim 9.

205. As explained above in 1[i], Liu teaches that the capacitor's bottom electrode (BE) operates directly as the gate electrode of T4 and can be over the semiconductor layer (PO). §VIII.A.4.i. Thus, in this configuration, BE is located in M1 and is directly above the semiconductor layer. And as also explained in 1[k], a POSITA would have found it obvious that the top capacitor electrode (TE) can be moved down to layer M2 (Option B). ¶163, §VIII.A.9. Thus, TE would be directly over BE.

206. As shown in Liu's Figure 1, drain D3 of Liu's T3 ("fifth" TFT) and source S1 of T1 ("sixth" TFT) must still be connected to BE. In the configuration where BE is located in its original location in M2, D3 and S1 (in the semiconductor layer) are connected to BE (in M2) through via "V1," which can be construed from Figure 3A. Liu, ¶¶41-42, FIGs. 1, 2, 3A, 3C.

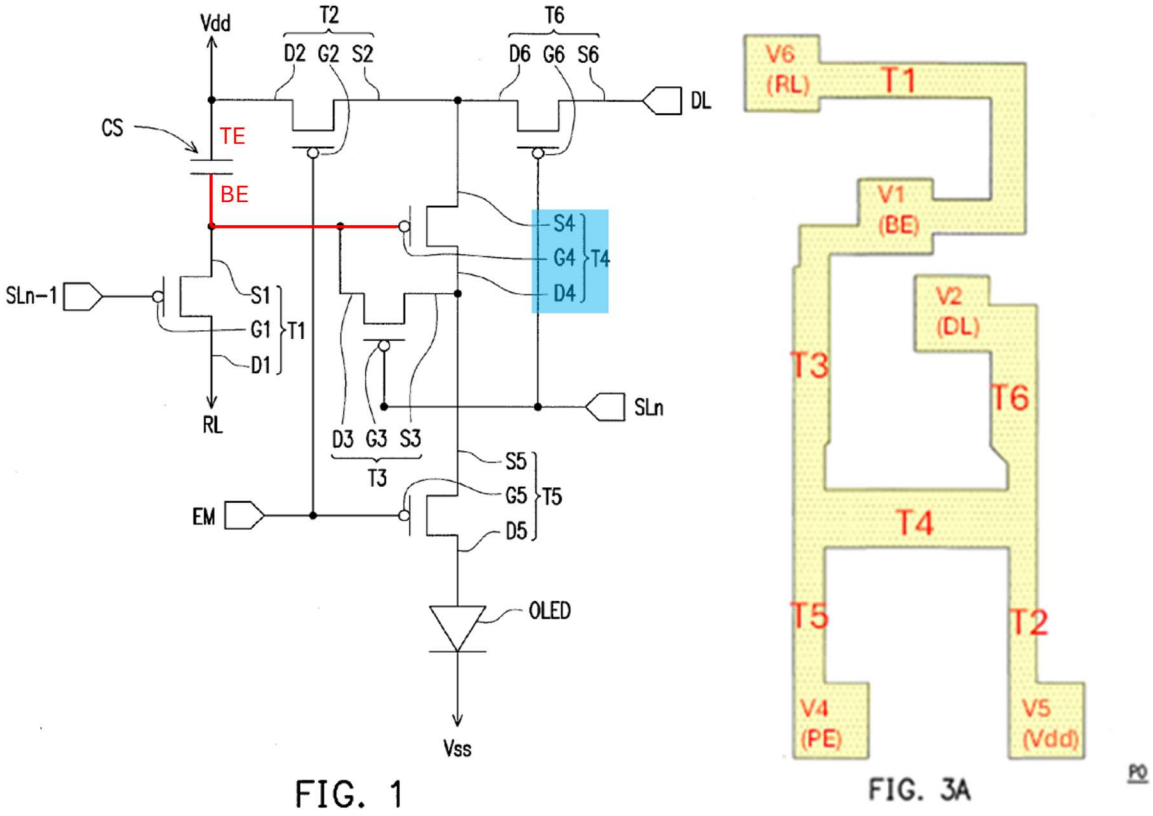


FIG. 1 FIG. 3A

Liu, FIGs. 1, 3A (annotated).

207. However, in the alternate embodiment of Liu where the bottom capacitor plate (BE) is moved down to M1 and the top capacitor plate (TE) can be also moved down to M2 (see Option B in 1[i]), metal layer M2 is no longer available to make the D3-to-S1-to-BE connection. It is my opinion that a POSITA would have found it obvious to extend via "V1" up to metal layer M3 and come back down to M1 at the appropriate location in order to make the connection to BE. This modification would have been obvious because when TE is moved from M3 to M2, M3 becomes available without any obstructions, and it would have provided a simple and easy way to enable routing the connection line to any circuit component.

Thus, a connection from V1 on M3 to BE would be made.

208. Once the connection line is on M3, it is my opinion that a POSITA would have recognized that TE would prevent making a direct connection from M3 to BE because TE is directly above BE. Accordingly, in order to conserve space and reduce the size of the pixel structure according to Liu's teachings (Liu, ¶7), a POSITA would have found it obvious to use a via from M3 to M1, in order to connect the metal signal line on M3 (that connects to V1) to BE. Furthermore, to prevent shorting BE to TE, it is my opinion that a POSITA would have found it obvious to use a "keep-out" in TE around the via "V3" from M3 to M1. Here, a keep-out is an area in the layout where no metal is allowed to be placed, which is a well-known method to prevent shorting of metal traces in layout design, e.g., Li, ¶45 ("Via 41 passes through a non-contact or keep-out area 42 of conductive plate 23 without electrically contacting conductive plate 23.").

209. Liu itself suggests and supports such wiring modifications (i.e., wiring modifications proposed in Option B) based on changes to the capacitor CS. In particular, I note that in Liu's second embodiment (Figures 8-9D), CS is modified to have three electrodes—the first electrode E1 of the semiconductor layer PO, the second electrode E2 of the first conductive layer M1, and the third electrode E3 of the second conductive layer M2. Liu, ¶72. Due to the change in the structure of the capacitor CS, Liu further describes the third conductive layer (M3) comprises a

signal line L, and that the third electrode E3 of the capacitor CS is electrically connected to the signal line L through a contact via structure V7. *Id.*, ¶70. That is, because of the capacitor CS modification, Liu's teaching suggests extending via structure V1 to the third conductive layer M3 and a signal line L in M3 to connect D3-to-S1-to-BE and the gate electrode of T4 through V3. Liu, ¶¶69-70, FIGs. 8, 9D; *see also* FIGs. 9A-9C. I have annotated Figure 8 of Liu below to show the modified wiring of V1, M3, and V3.

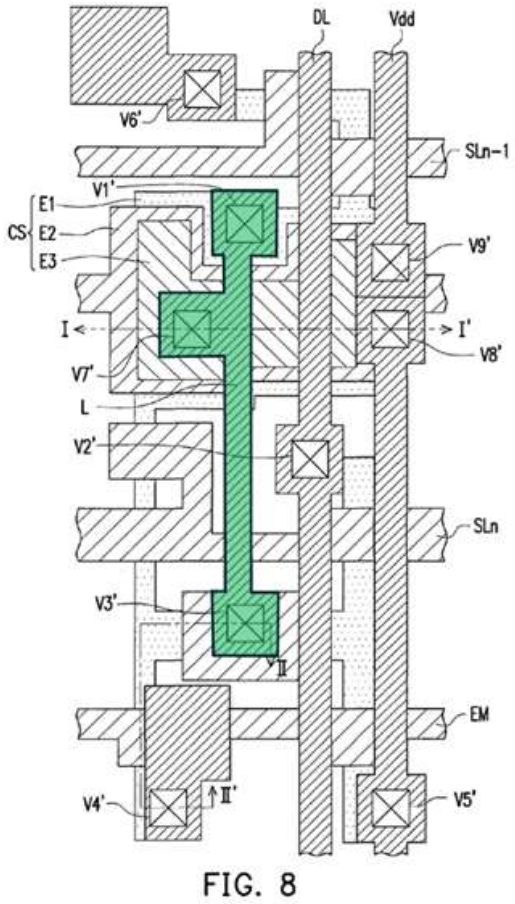
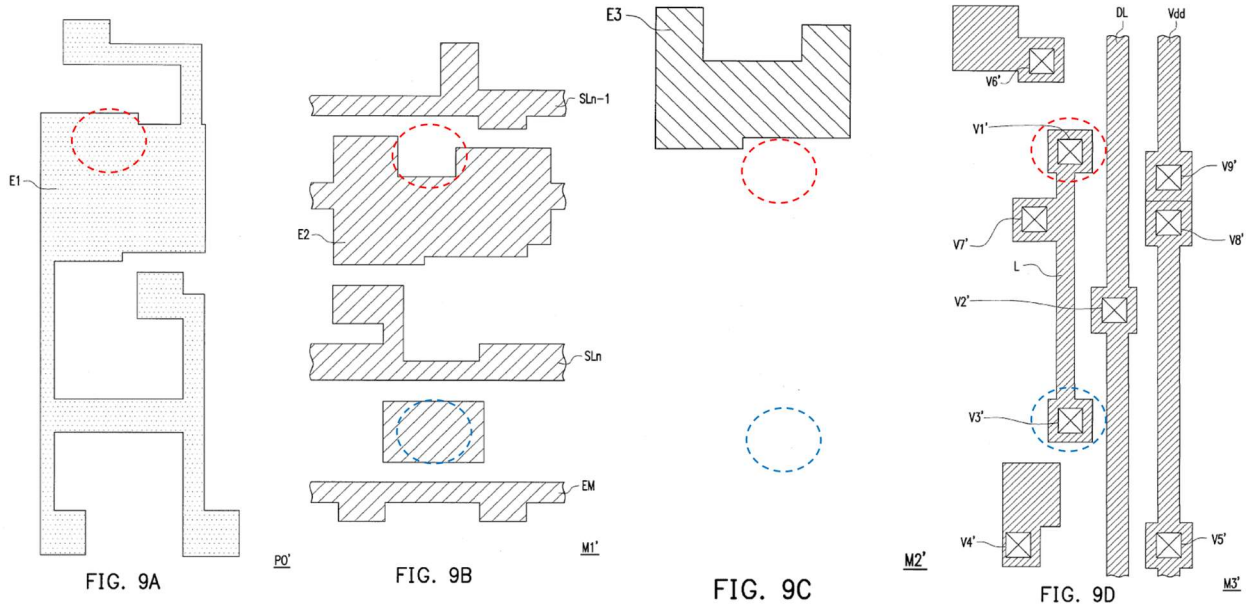


FIG. 8

Liu, FIG. 8 (annotated).

210. The individual layers of the layout from the semiconductor layer to the third conductive (or metal) (M3) for Liu's second embodiment are shown in Figures 9A-9D. I have annotated the figures below to show where the vias V1' and V3' are located in each figure, and consequently each layer. I have circled the position of V1' in red and V3' in blue. As shown, it is clear that Liu contemplated changes to the vias V1 and V3 and metal layer M3 to accommodate changes to CS.

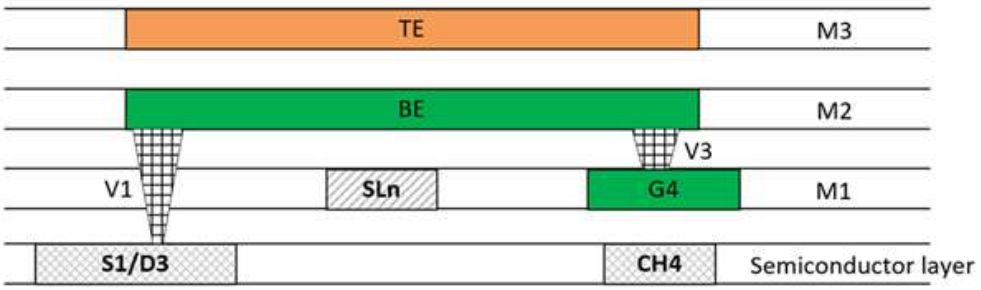


Liu, FIGS. 9A-9D (annotated).

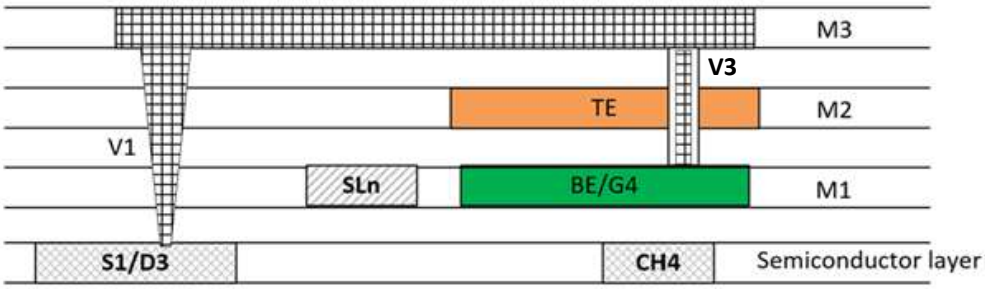
211. My discussion above regarding Figures 8-9D of Liu shows that Liu contemplated changes to the layout of its pixel structure, including changes to vias and metal signal lines, to accommodate changes to components, such as storage capacitor CS. In my opinion, a POSITA would have understood to use such knowledge to make other modifications to Liu's first embodiment, as explained

above, because BE is moved to metal layer 1 and TE is moved to metal layer M2.

212. To assist the Board with visualizing the obvious modifications as described herein, I have prepared the below illustrative figures show the obvious modifications to Liu's first embodiment (shown in Figures 1-7). The top figure shows the original configuration of Liu as shown in Figure 2 (Option A). *See* VIII.A.4.h. The second figure shows Liu's alternate configuration of Figure 2 (Option B), where CS is modified to move down one metal layer, as explained in 1[i] and supported by Liu's second embodiment (as explained immediately above). *See* VIII.A.4.h. For Option A, the connections for V1 and V3 are shown in Figure 2 and V1is additionally shown above in annotated Figure 3A.



Liu's original configuration (Option A)



Liu's alternate configuration (Option B)

213. As evident, in Liu's Option B, when BE is moved down, the connection from S1/D3 to BE cannot be made through M2. Accordingly, it is my opinion that a POSITA would have found it obvious to modify Liu's layout based on design choices necessitated by moving TE to M2, such that T1 and T3 are connected to BE through metal layer M3 ("electrically coupled to the first capacitor plate") by using a via through a keep-out region of TE ("through a contact hole that passes through the second capacitor plate").

214. Accordingly, claim 9 is disclosed by Liu.

11. Claim 10

a. 10[a] An organic light emitting diode display according to claim 2, further comprising: a plurality of second voltage lines;

215. Liu discloses limitation 10[a] for the same reasons as explained in limitation 3[a]. §VIII.A.6.a.

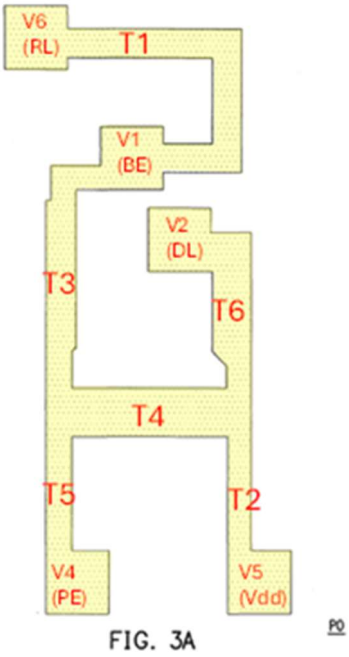
b. 10[b] a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

216. In my opinion, Liu teaches or suggests limitation 10[b].

217. Liu discloses T3 ("fifth thin film transistor") is formed in a portion of the semiconductor layer on the substrate ("implemented in a fifth portion of the semiconductor layer"). Liu, ¶35 ("the semiconductor layer PO…region

predetermined for forming…transistor T3").

218. As shown below in annotated Figure 3A, T3 and T4 are adjacent in the contiguous semiconductor layer ("the semiconductor layer couples the fifth thin film transistor to the second thin film transistor").



Liu, FIG. 3A (annotated).

219. Accordingly, limitation 10[b] is disclosed by Liu.

c. 10[c] a sixth thin film transistor implemented in a sixth portion of the semiconductor layer,

10[d] wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and

220. In my opinion, Liu teaches or suggests limitations 10[c] and 10[d].

221. I have grouped both of limitations 10[c] and 10[d], which are directed

to the sixth TFT, for clarity and ease of discussion.

222. Liu discloses T1 ("sixth thin film transistor") is formed in a portion of the semiconductor layer on the substrate ("implemented in a sixth portion of the semiconductor layer"). Liu, ¶35 ("the semiconductor layer PO…region predetermined for forming…transistor T1").

223. As shown above in annotated Figure 3A, T1 and T3 are adjacent in the contiguous semiconductor layer and thus "coupled" together by PO.

224. Accordingly, limitations 10[c] and 10[d] are disclosed by Liu.

d. 10[e] wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

225. In my opinion, Liu teaches or suggests limitation 10[e].

226. As I have explained in 3[c], T1 ("sixth" TFT) is connected to RL ("one of plurality of second voltage lines") and BE ("first capacitor plate"). §VIII.A.6.b. Furthermore, T1's semiconductor layer is connected on one side to RL through V6, and on the other side to BE through V1. §VIII.A.9. Accordingly, semiconductor layer PO couples T1 to both RL and BE. Annotated Figures 1 and 3A show the electrical connections of T1 and the placement of vias on the semiconductor layer.

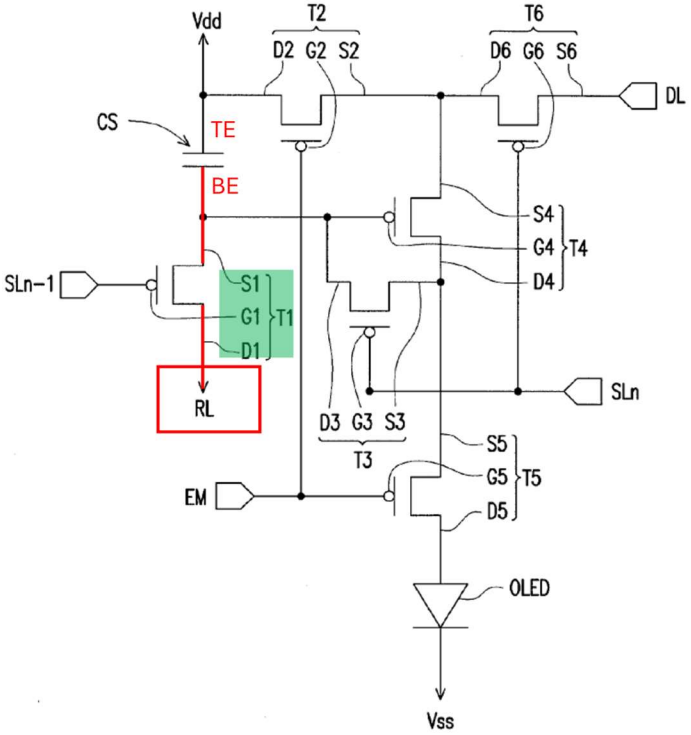


FIG. 1

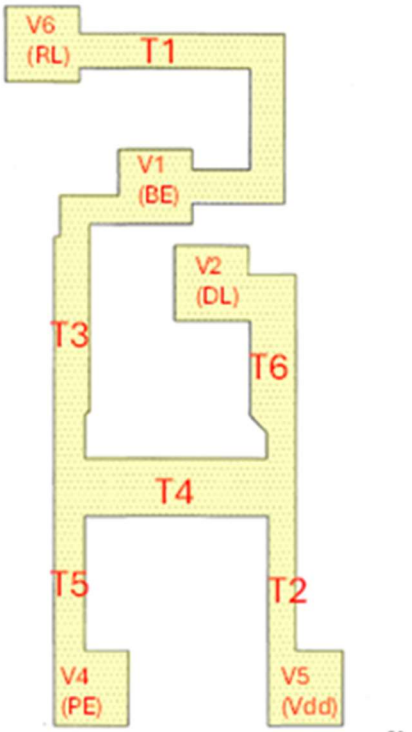


FIG. 3A

Right: Liu, FIG. 1 (annotated); Left: Liu, FIG. 3A (annotated).

227. Accordingly, limitation 10[e] is disclosed by Liu.

12. Claim 11: "An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer."

Claim 12: "An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material."

228. Liu discloses claims 11 and 12 for the same reasons as explained in claims 4 and 5, respectively. §VIII.A.7.

13. Claim 13: "An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines."

229. Liu discloses claim 13 for the same reasons as explained in claim 6. §VIII.A.8.

14. Claim 15: An organic light emitting diode display according to claim 11, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

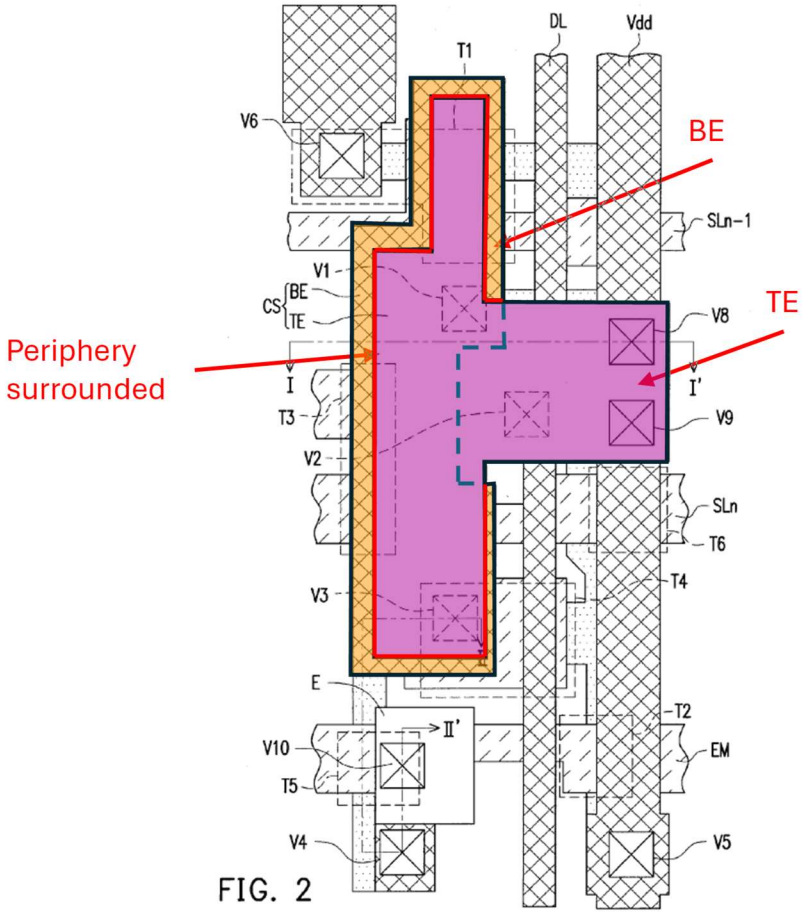
230. Liu discloses claim 15 for the same reasons as explained in claim 8. §VIII.A.9.

15. Claim 16: "An organic light emitting diode display according to claim 1, wherein a periphery of the first capacitor plate completely surrounds a periphery of the second capacitor plate in a plan view."

231. In my opinion, Liu teaches or suggests claim 16.

232. Liu teaches that BE ("first capacitor plate") surrounds a portion of TE ("second capacitor plate") (as shown in annotated Figure 2 below), and in my opinion, the red line represents a periphery of the TE surrounded by the bottom electrode plate (orange). A POSITA would have understood that "surround[ing] a

periphery" is understood as that at least a portion around the outside of BE was surrounded by TE. EX1015 ("the outward bounds of something as distinguished from its internal regions or center"); EX1016 ("the outside boundary or surface of something").



Liu, FIG. 2 (annotated).

233. Accordingly, Liu discloses claim 16.

16. Claim 17

a. 17[pre] An organic light emitting diode display according to claim 1, further comprising:

b. 17[a] a plurality of second voltage lines;

c. 17[b] a fifth thin film transistor electrically coupled to the first capacitor plate; and

d. 17[c] a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,

e. 17[d] wherein the sixth thin film transistor is coupled to the fifth thin film transistor.

234. Liu discloses claim 17 for the same reasons as explained in claim 3. §6.

17. Claim 18: "An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer."

Claim 19: "An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material."

235. Liu discloses claims 18 and 19 for the same reasons as explained in claims 4 and 5, respectively. §VIII.A.7.

18. Claim 20: "An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines."

236. Liu discloses claim 20 for the same reasons as explained in claim 6.

§VIII.A.8.

19. Claim 22: An organic light emitting diode display according to claim 18, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

237. Liu discloses claim 22 for the same reasons as discussed in claim 8.

§VIII.A.9.

20. Claim 23

a. 23[pre] An organic light emitting diode display according to claim 1, further comprising:

b. 23[a] a plurality of second voltage lines;

c. 23[b] a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

d. 23[c] a sixth thin film transistor implemented in a sixth portion of the semiconductor layer, wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

238. Liu discloses claim 23 for the same reasons as discussed in claim 10.

§VIII.A.10.

21. Claim 24: "An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer."

Claim 25: "An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material."

239. Liu teaches or suggests claims 24 and 25 for the same reasons as explained in claims 4 and 5, respectively. §VIII.A.7.

22. Claim 26: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines."

240. Liu discloses claim 26 for the same reasons as explained in claim 6. §VIII.A.8.

23. Claim 28: An organic light emitting diode display according to claim 24, wherein the plurality of scan lines are disposed in a first metal layer, the plurality of second voltage lines are disposed in a second metal layer, and the plurality of data lines and the plurality of first voltage lines are disposed in a third metal layer, and wherein the first capacitor plate is disposed in the first metal layer and the second capacitor plate is disposed in the second metal layer.

241. Liu discloses claim 28 for the same reasons as discussed in claim 8. §VIII.A.9.

24. Claim 29: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate."

242. Liu discloses claim 29 for the same reasons as discussed in claim 9. §VIII.A.10.

25. Claim 30: "An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view."

243. Liu discloses claim 30 for the same reasons as explained in claim 2. §VIII.A.5.

B. Ground 1B: Claims 2-6 and 10-13 are Unpatentable over the Combination of Liu, Udagawa, and Nakayama

1. Summary of Nakayama

244. Nakayama (EX1007) is a Japanese Patent Application Publication entitled "Display Device," with a filing date of December 4, 2001 (published June 13, 2003). In my opinion, Nakayama is analogous art to the '991 Patent because it is in the same field of endeavor. Both are directed to reducing variations in a current (or equivalently, maintaining a constant current) supplied to the driving TFT of a circuit that drives (or controls) an OLED in an OLED display. Nakayama, ¶¶4-5.

245. Nakayama teaches that variations in the drive currents supplied to different pixels may be caused by variations in the ratio of the electrostatic

capacitance of the holding to the electrostatic capacitance of the kick capacitor. *Id.*, ¶5. To suppress capacitance variation due to lateral misalignment, such as mask misalignment, Nakayama teaches the upper electrodes of the holding capacitor and the kick capacitor can be configured to have a larger surface area than the bottom electrodes thereof. *Id.*, ¶38.

2. Motivation to combine Liu, Udagawa, and Nakayama

246. In my opinion, there are several reasons that motivate combining the teachings of Liu and Nakayama.

247. As discussed above, Liu is directed to a reduced-size pixel structure. Liu, ¶¶4, 6, 10, 47, 56, 72. Nakayama is also related to OLED displays, and specifically, to reducing variations in the drive currents supplied to different OLED pixels. Nakayama, ¶¶5-6. Accordingly, a POSITA would have recognized the complementary teachings of those references, and would have been motivated to combine their teachings.

248. In particular, Nakayama described that variations in the threshold voltage of the driving TFT are affected by capacitor configurations in the circuit. Nakayama, ¶¶4-5. Thus, in my opinion, a POSITA would have been motivated to improve Liu's drive circuit operation based on the teachings of Nakayama to reduce variations in the threshold voltage of the driving TFT.

249. Nakayama recognized OLED operations can be improved by reducing capacitance variations (e.g., due to mask misalignment), which included configuring the upper electrode of a capacitor to have a larger surface area than the bottom electrode. Nakayama, ¶38. A POSITA would have thus found it obvious combine Liu with Nakayama, and specifically to use Nakayama's configuration of the larger upper capacitor electrode to improve Liu's OLED driving circuit. This combination would have resulted in mitigating threshold voltage variations, which would have improved the operation of the driving TFT of Liu, while maintaining a reduced area.

250. In my opinion, a POSITA would have been motivated to shape the capacitor plates such that the upper plate has a larger area than the lower plate, as disclosed by Nakayama, in Liu's OLED driving circuit to yield predictable results, i.e., the threshold voltage variation in the driving TFT being reduced. A POSITA would have had a reasonable expectation of success, because shaping the capacitor plates in an integrated circuit for an OLED display was well-known by 2012, as evidenced by the teachings of Nakayama, and such modifications were well within the skill set of a POSITA.

251. Furthermore, Liu can be combined individually with each of Udagawa and Nakayama. In each instance, the combination involves modifying a distinct aspect of Liu, and these modifications are independent of one another. For example, Udagawa teaches modifying the channel of the driving TFT and Nakayama teaches

modifying the relative shapes of the storage capacitor plates. A POSITA would recognize that there is no interference among the proposed modifications based on the teachings of Udagawa and Nakayama. Accordingly, in my opinion, a POSITA would have found it obvious and been motivated to combine Liu with each of Udagawa and Nakayama, and would have had a reasonable expectation of success.

252. Additional details regarding the Liu-Udagawa-Nakayama combination are provided below in connection with specific claim limitations.

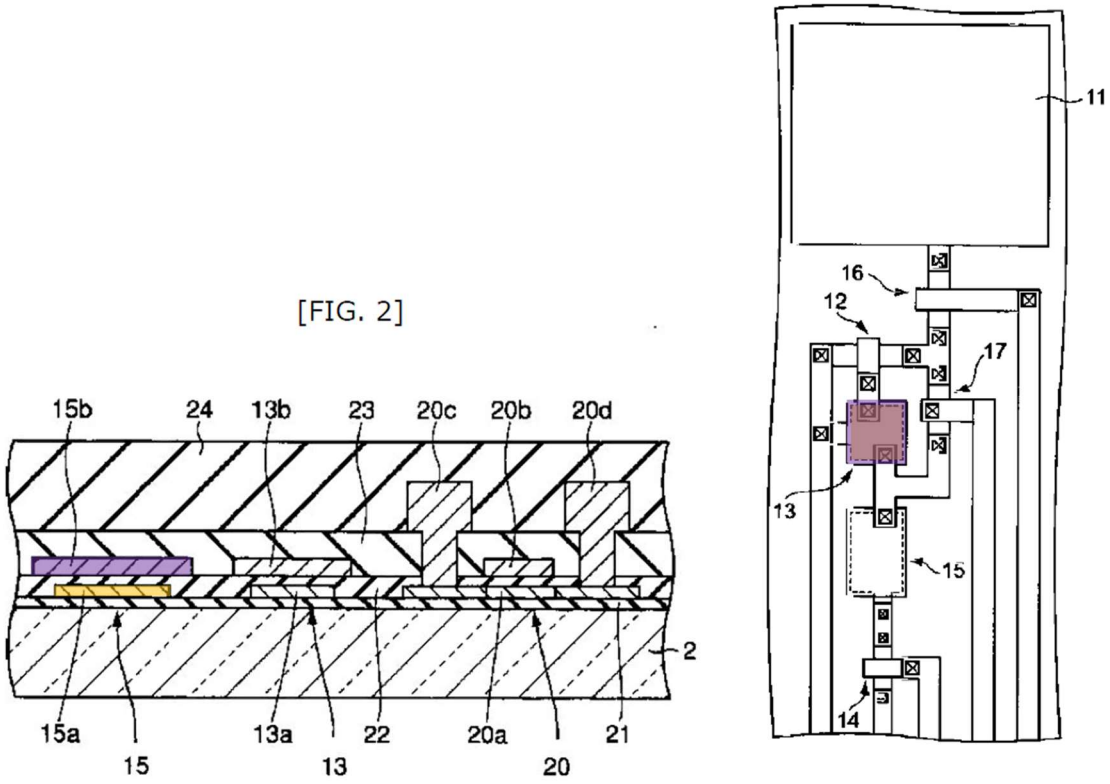
3. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view."

253. In my opinion, Liu in combination with Udagawa and Nakayama teach or suggest claim 8.

254. As explained above in Ground 1A, Liu in combination with Udagawa teaches that TE surrounds a periphery of BE. §VIII.A.5. To the extent that it is argued that TE does not "completely surround[] a periphery of" BE, a POSITA would have found it obvious in light of Nakayama. For example, Nakayama discloses forming the upper electrode of a holding capacitor to have a larger surface area than the bottom electrode. Nakayama, ¶38, FIGs. 2, 4. Further, as shown in Figure 2 of Nakayama, the lower capacitor electrode 15a (orange) is within the perimeter of the upper electrode 15b (purple). In Figure 4, only the upper electrode

is annotated given that it completely surrounds the lower electrode in the plan view. Nakayama, ¶¶35, 38. Nakayama explains that this configuration of capacitor electrodes suppresses the variation in the capacitance of the capacitors with respect to the deviation in the X-Y placement of the top electrode. Nakayama, ¶38.

【図4】



Left: Nakayama, FIG. 2 (annotated); Right: Nakayama, FIG. 4 (annotated).

255. As I have also explained above, in Liu, BE is either directly connected to the gate of T4 in M1 or can be reduced in size and placed directly over the semiconductor layer in M1. §VIII.A.4.h. In the former, no other metal layer is present in metal layer 3. Liu, ¶44; Figure 3D. In other words, there is ample room

for the top plate to move with respect to the bottom plate without affecting the capacitance. In my opinion, a POSITA would have found it obvious to enlarge the TE because it would have allowed for fabrication variances to maintain the capacitance of CS, as Nakayama explains. §VIII.B.2. This is possible because the capacitance is determined by the smaller of the two electrodes in the capacitor. Murade, ¶98.

256. For the latter (BE placed over the semiconductor layer), BE is directly the gate of T4 and TE may either remain in M3 or be moved to M2. §§VIII.A.4.h-163. As I have explained above, TE is unrestricted and a POSITA would have found it obvious to enlarge TE to realize the advantages of Nakayama. It would have also been within the skill of a POSITA to choose a dielectric and adjust the layout to accommodate TE over BE to produce the desired capacitance value.

257. In my opinion, a POSITA or an engineer performing layout of OLED circuits could reason the relatively simple arrangement of signal lines and CS to achieve the arrangement disclosed in Nakayama. Rather than following a rigid set of instructions, such an individual applies professional judgment and technical expertise to address the practical challenges encountered during circuit design. Any such changes to the capacitor design would have been well within a POSITA's skills and capabilities and would have amounted to routine design considerations, as these types of modifications are commonly made in the course of optimizing electronic

layouts. In the context of OLED circuit design, engineers routinely adapt component placement and interconnections to accommodate manufacturing tolerances, improve electrical performance, or ensure seamless integration with other circuit elements. For example, selecting the appropriate capacitor size to fit within the available layout space, or choosing a suitable dielectric material to meet specific voltage and reliability requirements, are both considered routine design considerations. Additionally, engineers may adjust the routing of signal lines to minimize interference or crosstalk, or modify the shape and position of contact holes to enhance yield and manufacturability. These types of decisions are part of the everyday skill set of a POSITA and do not require inventive ingenuity.

258. The knowledge of a POSITA in this respect is further evidenced, for example, by textbooks such as *CMOS VLSI Design: A Circuits and Systems Perspective* (authored by N. Weste and D. Harris), which discusses, inter alia, layout design rules that "describe how small features can be and how closely they can be reliably packed in a particular manufacturing process" (*see* Weste, Chapter 1.5.3) and wherein "[t]he rules are defined in terms of feature sizes (widths), separations, and overlaps, [and wherein] [t]he main objective of the layout rules is to build reliably functional circuits in as small an area as possible" (*see* Weste, Chapter 3.3). *See generally* Weste, Chapters 1 and 3.

259. For at least the reasons discussed above and explained in §VIII.B.2,

there is a motivation to incorporate Nakayama's capacitor plate sizing in Liu to maintain the capacitance of Liu's CS capacitor.

260. Accordingly, claim 2 is disclosed by Liu in combination with Udagawa and Nakayama.

4. Claim 3-6, and 10-13

261. The addition of Nakayama does not change any of the analysis above in Ground 1A regarding claims 2-6, 8, 10-13, and 15. *See* §§A.5-A.9, A.11-A.14. With respect to claims 8 and 15, enlarging TE as explained above in §VIII.B.3 would not prevent RL from being moved to M3, particularly when BE is directly over the semiconductor layer in M1and TE is moved to M2. *See* §§VIII.A.9, A.14.

C. Ground 1C: Claims 7, 14, 21, and 27 are Unpatentable over Liu, Udagawa, and Chung

1. Summary of Chung

262. Chung (EX1008) is a U.S. Patent Application Publication entitled "Organic Light Emitting Display and Driving Method Thereof," with a filing date of December 20, 2007 (published June 26, 2008; claiming the priority benefit of Korean Patent Application No. 2006-131962 filed December 21, 2006). In Chung, a pixel circuit of an organic light emitting display is configured similarly to the circuit shown in Figure 1 of the '991 Patent (i.e., with scan lines, signal lines, a driving transistor, five switching transistors, and a storage capacitor), but

additionally includes a switching transistor SW_TR6 for applying a reverse bias, i.e., a seventh transistor. Chung, ¶57.

263. In my opinion, Chung is analogous art to the '991 Patent because it is in the same field of endeavor. For example, both are directed to compensating the threshold voltage of the driving transistor. Chung, ¶87.

264. Chung teaches that in an initialization period (i.e., a non-light emission period) of operating the pixel circuit, a low-level scan signal that is applied to the initial switching transistor SW_TR 5 is also applied to the switching transistor SW_TR6 for applying a reverse bias to the OLED, thereby preventing degradation of the organic light emitting diode OLED. *Id.*, ¶¶83-84.

2. Motivation to combine Liu, Udagawa, and Chung

265. In my opinion, there are several reasons that motivate combining the teachings of Liu and Chung.

266. As discussed above, Liu is directed to a reduced-size pixel structure, which includes a plurality of TFTs. Liu, ¶¶4, 6, 10, 47, 56, 72. Liu does not limit the number of TFTs in its OLED driving circuit. *Id.*, ¶32. Chung discloses an OLED drive circuit similar to those described in Liu, which additionally includes a seventh TFT that is configured to apply a reverse bias voltage to the OLED, which increases the lifespan of the OLED and the uniformity of brightness of the respective pixels

by the elimination of the degradation. Chung, ¶¶11, 57.

267. In my opinion, a POSITA would have thus recognized that the OLED driving circuit of Liu would be improved by introducing a seventh TFT, as described by Chung, for applying a reverse bias to the OLED, thereby preventing degradation of the OLED during an initialization period. Chung, ¶¶83-84. Furthermore, a POSITA would have had a reasonable expectation of success because Chung explicitly described the implementation of a seventh TFT; the introduction of a single additional TFT would not have appreciably impacted the size of the driving circuit of Liu, and such modification was well within the skill set of a POSITA.

268. It is my opinion that a POSITA would have been motivated to use an additional seventh TFT in a 6T1C pixel driving circuit to Liu's OLED driving circuit, which is a 6T1C circuit, to prevent degradation of the OLED during the initialization period. A POSITA would have had a reasonable expectation of success, because incorporating a seventh transistor into a 6T1C circuit was well-known by 2012, as evidenced by the teachings of Chung and other known prior art references, and such modifications were well within the skill set of a POSITA.

269. Furthermore, Liu can be combined individually with each of Udagawa and Chung. In each instance, the combination involves modifying a distinct aspect of Liu, and these modifications are independent of one another. For example, Udagawa teaches modifying the channel of the driving TFT and Chung teaches

modifying the 6T1C circuit by incorporating a seventh TFT. A POSITA would recognize that there is no interference among the modifications, and each combination can be implemented without affecting the others. Accordingly, in my opinion, a POSITA would have found it obvious and would have been motivated to combine Liu with each of Udagawa and Chung, and would have had a reasonable expectation of success in making those modifications.

270. Additional details regarding the Liu-Udagawa-Chung combination are provided below in connection with specific claim limitations.

3. Claim 7: "An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor."

271. In my opinion, Liu in combination with Udagawa and Chung teaches or suggests claim 11.

272. As I have explained above in §VIII.C.2, a POSITA would have been motivated to combine the teachings of Liu and Chung. In my opinion, combining such teachings would not have impacted the above teachings in Ground 1A because the combination adds a single TFT to the driving circuit.

273. Liu discloses that its driving circuit could have more or less than six TFTs. Liu, ¶¶32, 58. As explained above, Chung discloses an OLED drive circuit

similar to those described in Liu and in Figure 10 of the '991 Patent, which additionally includes a seventh TFT. §VIII.C.1. I have reproduced Figure 10 from the '991 Patent and Figure 5 from Chung below, highlighting the seventh TFT.

FIG. 5

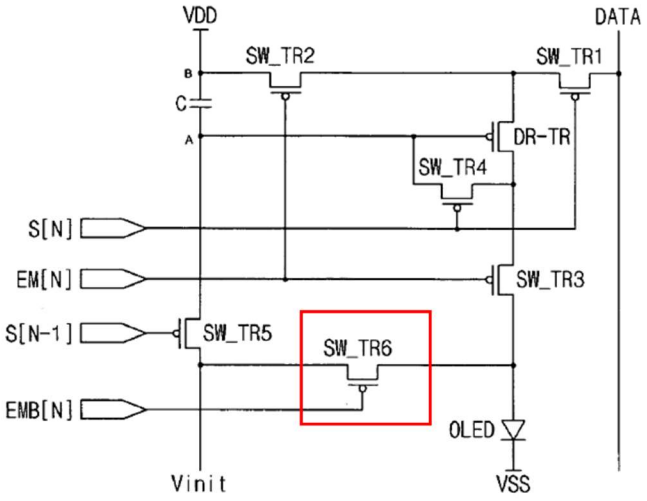
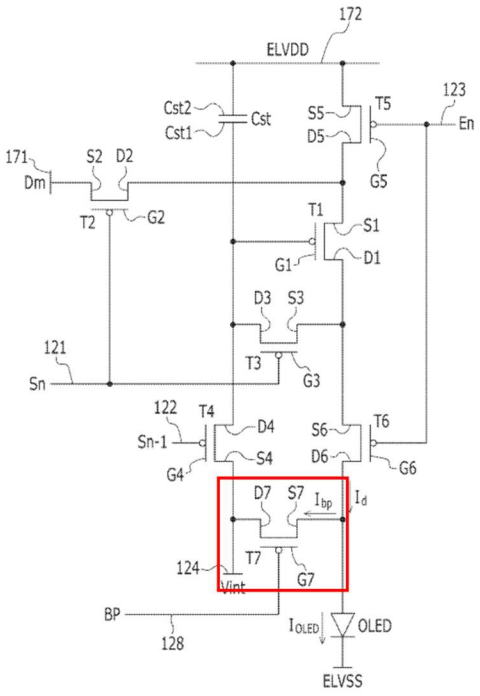
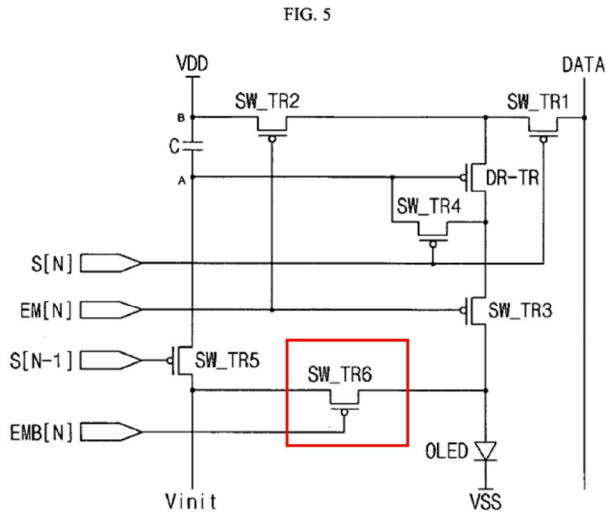


FIG. 10



Left: Chung, FIG. 5 (annotated); Right: '991Pat., FIG. 10 (annotated).

274. As shown below, Chung's circuit is identical to Liu, except for the additional seventh TFT (SW_TR6).



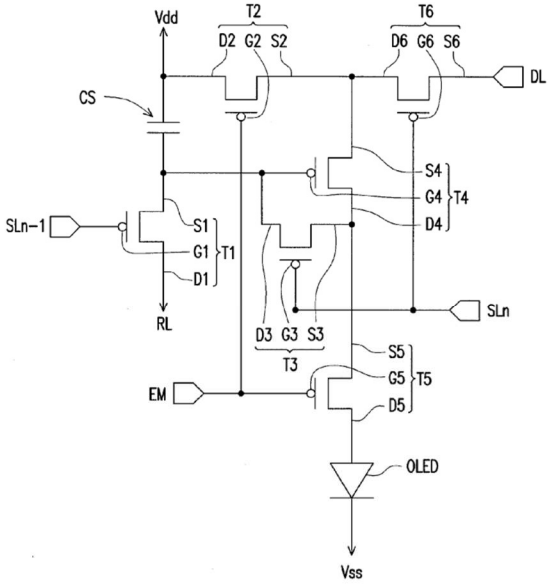


FIG. 1

Left: Chung, FIG. 5 (annotated); Right: Liu, FIG. 1.

275. Chung discloses SW_TR6 in Figure 5 connected to the OLED and initialization TFT (SW_TR5). Chung, ¶¶57, 60, 63. Chung explains that "the emission reverse control signal may be readily obtained by coupling an inverter to a previous end of an output end of the emission control signal driver outputting the emission control signal." Chung, ¶63. Thus, it is my opinion that a POSITA would have understood that SW_TR6 was active when SW_TR3 was inactive (i.e., when the OLED is off). *See id.*, FIG. 6. Chung explains the addition of SW_TR6 prevents "degradation of the organic light emitting diode OLED" during the initialization period. Chung, ¶84.

276. In my opinion, a POSITA would have been motivated to modify Liu to incorporate Chung's seventh TFT to prevent degradation of the OLED during

initialization. Such a modification would have improved the performance of Liu drive circuit with minimal increase in size. Furthermore, as shown above, Chung and Liu's circuits are identical except for the additional TFT. An example modified drive circuit incorporating Chung's TFT in Liu's drive circuit is shown below in modified Figure 5.

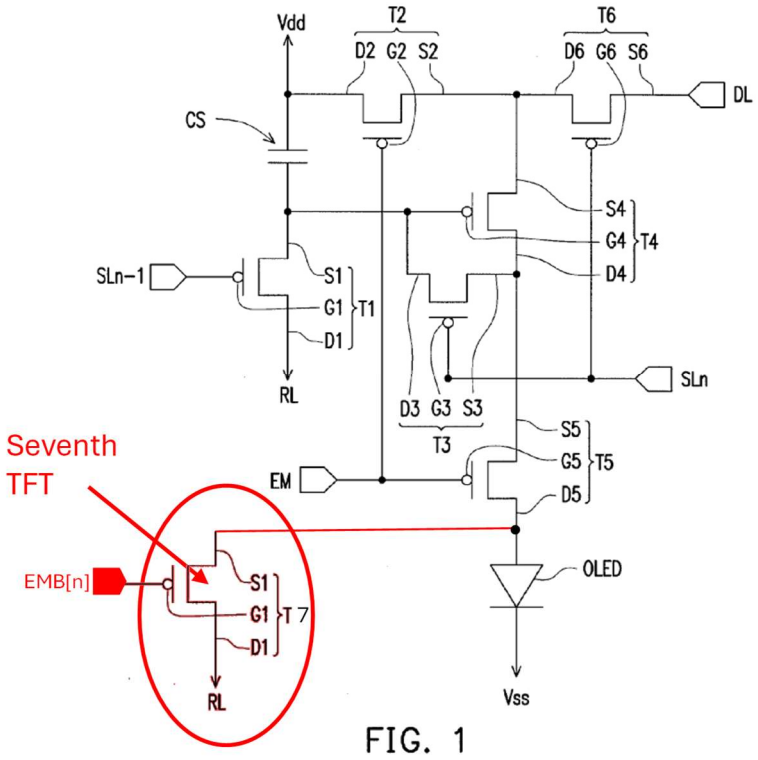


FIG. 1

Liu, FIG. 1 modified with Chung FIG. 5 (annotated).

277. Accordingly, for the reasons explained in §VIII.C.2, a POSITA would have been motivated to incorporate Chung's seventh TFT in Liu to maintain enhance the drive circuit and prevent degradation of the OLED.

278. Accordingly, claim 11 is disclosed by Liu in combination with

Udagawa and Chung.

4. Claim 14

a. 14[pre] An organic light emitting diode display according to claim 11, further comprising a seventh thin film transistor implemented in the sixth portion of the semiconductor layer,

b. 14[a] wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

c. 14[b] wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

279. In my opinion, Liu in combination with Udagawa and Chung teaches or suggests claim 14. Furthermore, claim 14 is substantially similar to claim 7, except that it recites "the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor."

280. As I have explained in 1[h-1] and 1[l], each of transistors T1 to T6 utilize and include a portion of the semiconductor layer, which is thus electrically coupled to the corresponding transistor. Liu, ¶35; §§VIII.A.4.f, VIII.A.4.k. Here, a POSITA would have understood that when adding an additional TFT, the semiconductor layer would be deposited for that new TFT because it would have used the design disclosed in Liu. Furthermore, Liu discloses the semiconductor layer is contiguous between all TFTs. *See, e.g.*, Liu, FIG. 3A. In my opinion, a POSITA

would have understood and found it obvious to continue the semiconductor layer to incorporate T7. Using a contiguous semiconductor layer would have been a natural choice and given Liu's layer was contiguous. Moreover, it was one of two options (contiguous or non-contiguous).

281. Here, I note that many possible layouts could have been realized based on Chung's teachings. Accordingly, Liu in combination with Udagawa and Chung teaches or suggests the semiconductor layer extended contiguously from T5 ("fourth" TFT) to a seventh TFT. This is particularly so because both the seventh TFT and T5 connect to the OLED and using the same connection point (V4) would eliminate the need for connecting the TFTs using other layers of the design.

282. For the additional reasons explained for claim 7, the remaining limitations of claim 14 are disclosed by Liu in combination with Udagawa and Chung. §VIII.C.3.

5. Claim 21: "An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor."

283. Liu in combination with Udagawa and Chung discloses claim 21 for the same reasons as explained in claim 7. §VIII.C.3.

6. Claim 27

a. 27[pre] An organic light emitting diode display according to claim 24, further comprising a seventh thin film transistor implemented in the sixth portion of the semiconductor layer,

b. 27[a] wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

c. 27[b] wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

284. Liu in combination with Udagawa and Chung discloses claim 27 for the same reasons as explained in claim 12. §VIII.C.4.

D. Ground 1D: Claims 7 and 14 are Unpatentable over Liu, Udagawa, Chung, and Nakayama

1. Motivation to combine Liu, Udagawa, Chung, and Nakayama

285. As previously discussed, the Liu reference can be combined individually with each of the cited references—Udagawa, Nakayama, and Chung. In each instance, the combination involves modifying a distinct aspect of Liu, and these modifications are independent of one another. For example, Udagawa teaches modifying the channel of the driving TFT, Nakayama teaches modifying the relative shapes of the storage capacitor plates, and Chung teaches modifying the 6T1C circuit by incorporating a seventh TFT. A POSITA would recognize that there is no

interference among the modifications, and each combination can be implemented without affecting the others. Accordingly, in my opinion, a POSITA would have found it obvious and would have been motivated to combine Liu with each of Udagawa, Nakayama, and Chung.

286. Additional details regarding the Liu-Udagawa-Nakayama-Chung combination are provided below in connection with specific claim limitations.

2. Claims 7 and 14

287. In my opinion, Liu in combination with Udagawa, Nakayama, and Chung teaches or suggests claims 7 and 14.

288. As explained above in Grounds 1A and 1B, Liu in combination with Udagawa or Liu in combination with Udagawa and Nakayama teach claims 2-4 and 10-11. §§VIII.A.5-VIII.A.7, VIII.A.11-VIII.A.12, VIII.B.3-VIII.B.4. As further explained above Chung provides the sevenths TFT for claim 7 and 14. §§VIII.C.3-VIII.C.4. As also explained above in §VIII.D.1, it is my opinion that a POSITA would have been motivated to combine Liu individually and together with Udagawa, Nakayama, and Chung.

289. Claim 7: As explained above in Grounds 1A and 1B, Liu in combination with Udagawa or Liu in combination with Udagawa and Nakayama teach claims 1-4 from which claim 7 depends. §§VIII.A.4-VIII.A.7, VIII.B.3-

VIII.B.4. As further explained above, Chung provides the seventh TFT for claim 7. §VIII.C.3. As also explained above in §VIII.D.1, a POSITA would have been motivated to combine Liu individually and together with Udagawa, Nakayama, and Chung. Accordingly, for the reasons explained above, claim 7 is disclosed by Liu in combination with Udagawa, Nakayama, and Chung.

290. Claim 14: As explained above in Grounds 1A and 1B, Liu in combination with Udagawa or Liu in combination with Udagawa and Nakayama teach claims 1-2, and 10-11 from which claim 14 depends. §§VIII.A.4-VIII.A.5, VIII.B.3-VIII.B.4. As further explained above, Chung provides the seventh TFT for claim 14. §VIII.C.4. As also explained above in §VIII.D.1, a POSITA would have been motivated to combine Liu individually and together with Udagawa, Nakayama, and Chung. Accordingly, for the reasons explained above, claim 14 is disclosed by Liu in combination with Udagawa, Nakayama, and Chung.

E. Ground 1E: Claims 9, 29, and 30 are Unpatentable over Liu in combination with Udagawa and Murade

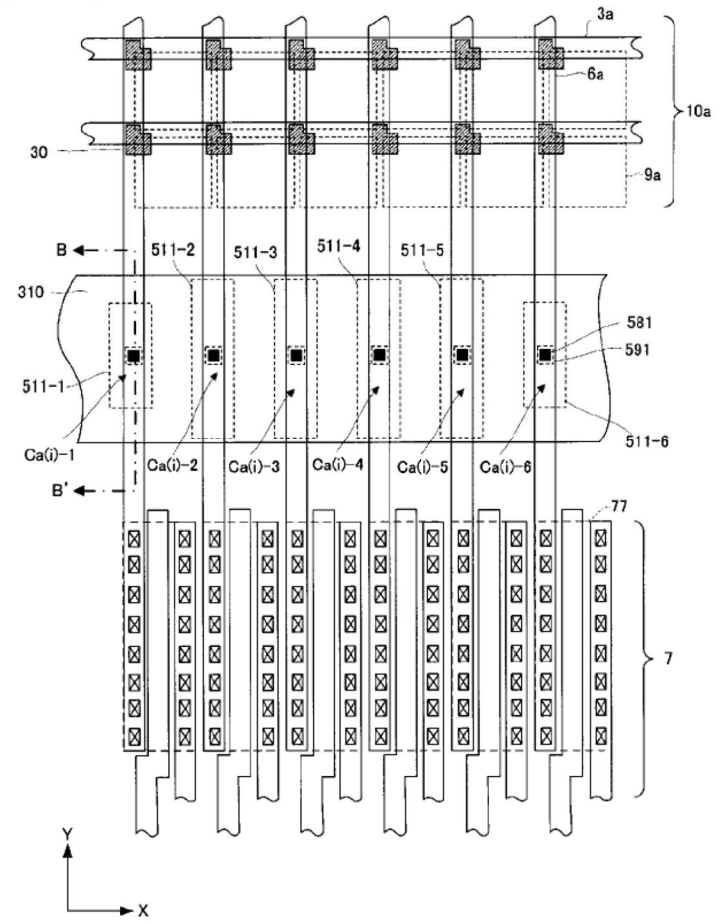
1. Summary of Murade, and Motivation to Combine Liu and Murade

291. Murade (EX1011) discloses an electro-optical device, such as an active–matrix liquid crystal display (AM-LCD) device, that includes a thin film transistor (TFT) array, a data line, scanning line, substrate, pixel electrode, and storage capacitor. Murade, Abstract, ¶2. Murade's device further includes an

additional capacitor having the same stacked structure as storage capacitor and electrically connected to the data line. *Id.*, Abstract, ¶¶12-13, 91. Furthermore, the additional capacitor can be formed on layers lower than the data line and closer to the switching TFTs, which is typically disposed on a layer lower than the storage capacitor and data lines, via an interlayer insulating film. *Id.*, ¶21.

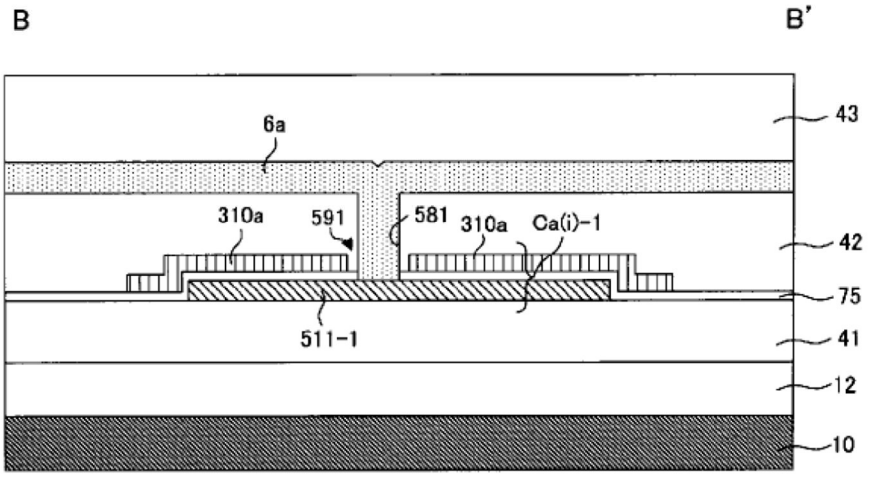
292. Figure 6 of Murade "is a plan view of the capacitors electrically connected to the data lines, and Figure 7 is a cross-sectional view taken along the line B-B' in FIG. 6," and have been reproduced below. *Id.*, ¶21.

[FIG. 6]



Murade, FIG. 6.

[FIG. 7]



Murade, FIG. 7.

293. Murade's Figure 7 and the associated description provide explanations about the additional capacitor and describe that the bottom plate 511-1 of the additional capacitor "is electrically connected to the data line 6a via a contact hole 581 opened through the interlayer insulating film 42 and the dielectric film 75." *Id.*, ¶88. Murade further explains that "contact hole 581 is provided inside an opening 591 provided in the fixed potential side electrode 310a." *Id.* The fixed potential side electrode is the additional capacitor's top electrode.

294. Murade continues by explaining that "the contact hole 581 enables electrical connection between the pixel potential side electrode 511-1 and the data line 6a while maintaining electrical insulation between the pixel potential side electrode 511-1 and the data line 6a, and the fixed potential side electrode 310a." *Id.*

295. In my opinion, both Murade and the ’991 Patent are related to flat-panel display technologies that use a thin film transistor active-matrix array backplane. The teachings of Murade used in combination with Liu merely relate to Murade’s teachings about routing of a circuit connection line through a hole in a capacitor plate, which is generally applicable to various display technologies.

296. In my opinion, a POSITA would have been guided by the teachings of Murade and understood that in a display layout configuration where a capacitor plate prevented direct routing of a signal line from an upper layer to the lower capacitor plate, a hole can be made in the upper capacitor plate to enable the signal line connection. Additionally, connecting a capacitor in such a way is merely a design choice necessitated by the layout.

297. I further note that a POSITA would have had a reasonable expectation of success because configuring a hole in an electrode to connect a line through it was well-known and such modification was well within the skill set of a POSITA.

2. Claim 9: “An organic light emitting diode display according to claim 3, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate.”

298. In my opinion, Liu in combination with Udagawa and Murade teaches or suggests claim 9.

299. As explained above in Ground 1A for claim 9, Liu's teaching to move the storage capacitor plates to metal layers 1 and 2 would have made it obvious to a POSTIA to use metal layer 3 to connect T1 and T3 to BE. §VIII.A.10. Murade corroborates and confirms that making a hole in the top capacitor plate to route a signal line to the bottom capacitor plate was a known design technique and would have been obvious to a POSITA. As I have explained above in §VIII.E.1, a POSITA would have been motivated, e.g., based on both Liu and Murade being related to flat-panel display technologies that use TFT active-matrix array backplanes, to use Murade's structure of connecting a line through a top plate to a bottom plate of a capacitor. Thus, Liu in combination with Murade teaches to connect T3 ("fifth" TFT) and T1 ("sixth" TFT) to BE ("first capacitor plate") using a contact hole (e.g., via) through a hole in TE ("through a contact hole that passes through the second capacitor plate"), thereby disclosing every element recited in claim 9.

300. Accordingly, claim 9 is disclosed by Liu in combination with Murade.

3. Claim 29: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor and the sixth thin film transistor are electrically coupled to the first capacitor plate through a contact hole that passes through the second capacitor plate."

301. Liu discloses claim 29 for the same reasons as explained in claim 9 of Ground 1A. §VIII.E.2.

4. Claim 30: "An organic light emitting diode display according to claim 29, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view."

302. Liu discloses claim 30 for the same reasons as explained in claim 2 of Ground 1A. §VIII.A.5.

F. Ground 2A: Claims 1-6, and 17-20 are Unpatentable over Noguchi-I and Udagawa

1. Summary of Noguchi-I

303. Noguchi-I (EX 1010) is a U.S. Patent Application Publication entitled "Active Matrix Substrate and Organic EL Display Device," with a filing date of April 11, 2012 (published August 9, 2012; claiming the priority benefit of Japanese Patent Application No. 2009-241319 filed October 20, 2009). In Noguchi-I, a shield electrode is provided in a wiring layer between the pixel electrode and a wiring layer in which the gate electrode is provided such that the shield electrode forms a region covering the gate electrode, which reduces the parasitic capacitance formed between the gate electrode of the driving transistor and a pixel electrode (anode) of the organic EL element OLED. Noguchi-I, ¶35.

304. In my opinion, Noguchi-I is analogous art to the '991 Patent because both are in the same field of endeavor. Both are directed to the pixel structure of an OLED display that is driven by scanning lines, power source lines, signal lines, and transistors T1 to T6. Noguchi-I, ¶70. Similarly, both endeavor to compensate for the

variability of the threshold voltage of the driving TFT. *Id.*, ¶15.

305. Noguchi-I teaches a pixel of an organic EL display device that includes a first wiring layer disposed at a level closer to a substrate 100 than a second wiring layer. *Id.*, ¶69. Herein, the first wiring layer includes scanning lines, an emission control line, and an initialization voltage line (each extending in a horizontal direction), and the second wiring layer includes a power source line and a signal line data (each extending in a vertical direction). *Id.*, ¶68. The first wiring layer, which further includes the gate electrode of the driving transistor, is disposed between the interlayer dielectric 110 and the interlayer dielectric 111, the second wiring layer is disposed between the interlayer dielectric 111 and the interlayer dielectric 112, and the pixel electrode 103 is disposed on the interlayer dielectric 112. *Id.*, ¶71.

2. Motivation to combine Noguchi-I and Udagawa

306. In my opinion, there are several reasons that motivate combining the teachings of Noguchi-I and Udagawa.

307. Both Noguchi-I and Udagawa described drive circuits for OLED displays and both sought to improve the design and operation of OLEDs. Notably, Noguchi-I describes a pixel structure of an OLED display with reduced parasitic capacitance that improved image quality. Noguchi-I, ¶¶12, 15, 72. And, Udagawa describes drive circuit configurations that improved OLED's reliability, and

consequently, its operations and image quality. Udagawa, ¶12. Therefore, it is my opinion that a POSITA would have been motivated to combine the complementary teachings of Noguchi-I with Udagawa to achieve further improvements in the image quality of the OLED display.

308. I further note Udagawa disclosed that as the channel length of a TFT increases, the oxide film capacitance C_{ox} becomes larger, and at least a portion of this capacitance can be used as a retention capacitance of the OLED, thus improving OLED's image quality. Udagawa, ¶64. Accordingly, in my opinion, a POSITA would have found it obvious to combine the complementary teachings of Udagawa with Noguchi-I, and specifically to use Udagawa's the serpentine channel in Noguchi-I's driving TFT to further improve the operations of the OLED.

309. In my opinion, a POSITA would have been motivated to use Udagawa's TFT with a longer channel to Noguchi-I's pixel structure to yield the predictable result of the capacitors being formed correctly and improving image quality. Additionally, a POSITA would have had a reasonable expectation of success, because using TFT with a longer channel to reduce dispersion and increase capacitance was well-known by 2012, evidenced by the teachings of Udagawa and other known prior art references (such as Yamazaki, Min, and Lee-2009), and such modifications were well within the skill set of a POSITA.

310. Additional details regarding the Noguchi-I−Udagawa combination are

provided below in connection with specific claim limitations.

3. Independent Claim 1

311. Noguchi-I describes a "pixel of a conventional organic EL display device" with reference to Figures 8 and 9. Noguchi-I, ¶11. It then presents four related embodiments that build upon each other to address the perceived deficient response of the pixel. *Id.*, ¶¶66-95. All embodiments are based on the circuit diagram of Figure 1 (Noguchi-I, ¶¶66, 74, 79, 88) but alter the construction of capacitor C1 and the gate electrode of T4 in different ways (*id.*, ¶¶72, 77, 83, 91). I rely on the cumulative teachings of Noguchi-I embodiments that culminate in embodiment 4 (Figure 7). To the extent other figures of Noguchi-I are used below, they represent common features of Noguchi-I's invention.

a. 1[pre]: An organic light emitting diode display comprising:"

312. In my opinion, Noguchi-I teaches or suggests 1[pre].

313. Noguchi-I discloses "an organic EL **display device**" with "a current emissive element such as an organic EL element." Noguchi-I, Abstract, ¶¶1, 41. The display comprises a plurality of "pixels" (*id.*, ¶¶3, 70 (identifying one "display unit" having one pixel), where the "organic EL element" is an OLED (*id.*, ¶11, FIG. 1).

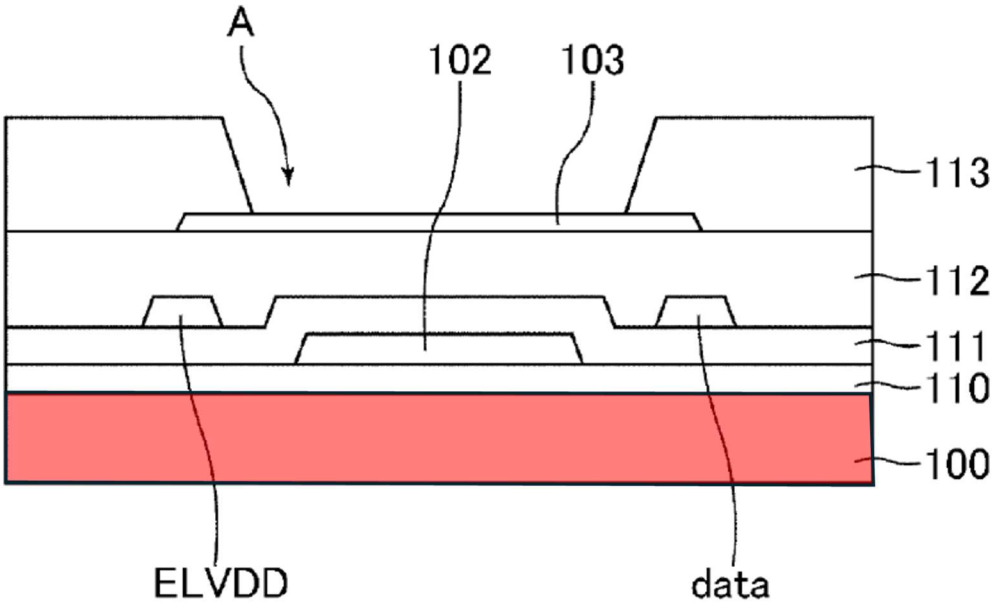
314. Accordingly, Noguchi-I discloses an OLED display comprising pixels ("[a]n organic light emitting diode display").

b. 1[a]: "a non-conductive substrate;"

315. In my opinion, Noguchi-I teaches or suggests limitation 1[a].

316. Noguchi-I discloses a pixel comprising a "substrate 100," among other things. Noguchi-I, ¶¶66-69, 98-114, FIGs. 3 (annotated below), 6, 9. It was well-known at the time that substrates for OLED pixels comprised glass, among other materials, and needed to be non-conductive so that the circuits placed on them operated properly. Liu, ¶33; Kim, 5:4-11. Accordingly, it would have been obvious that substrate 100 is "non-conductive."

Fig. 3



Noguchi-I, FIG. 3 (annotated).

317. Accordingly, limitation 1[a] is disclosed by Noguchi-I.

c. 1[b]: "a plurality of first voltage lines;"

1[c]: "a plurality of scan lines;"

1[d]: "a plurality of data lines;"

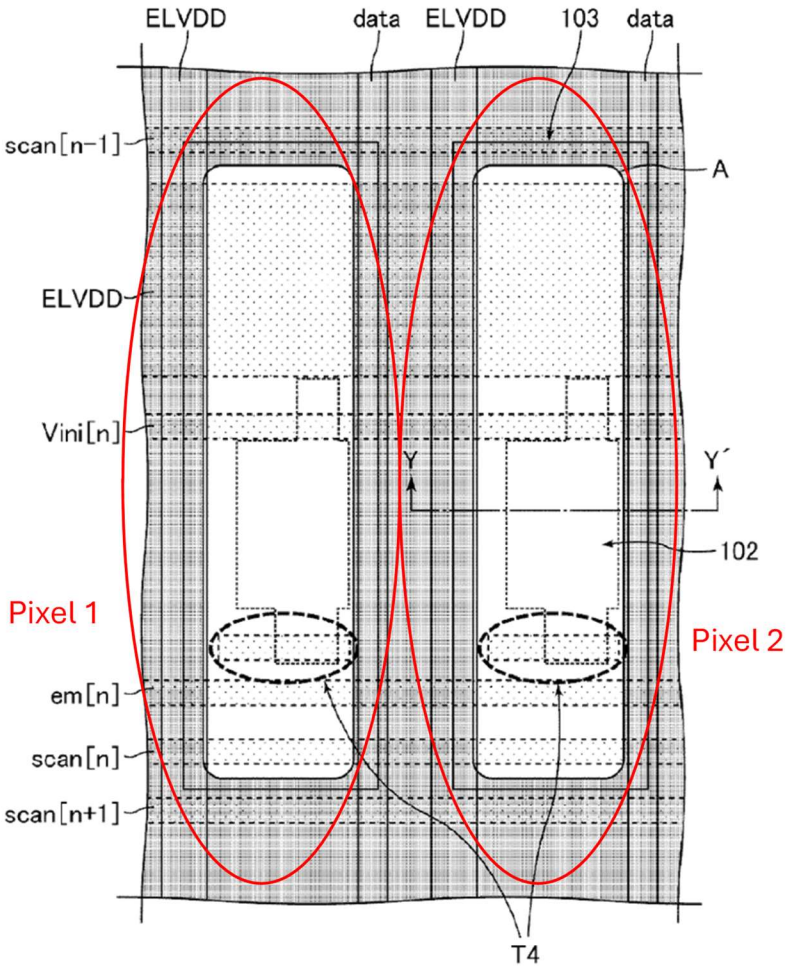
318. In my opinion, Noguchi-I teaches or suggests limitations 1[b]-1[d].

319. I have grouped each of the limitations 1[b]-1[d], which are directed to component connectivity in the pixel structure, for clarity and ease of discussion.

320. Plurality of Pixel Structures

321. As explained above in 1[pre], Noguchi-I discloses a display with a plurality of pixels. §VIII.F.3.a. Each pixel structure includes TFTs, capacitor, and OLED. Noguchi-I, ¶¶11, 66-70, 74, 77, 79, 88, 91, FIG. 1. Noguchi-I further explains that item 103 in the figures is a pixel electrode of an OLED. Noguchi-I, ¶¶15, 110. As shown in Figure 1, there is only one OLED per pixel ("each of the pixels comprising an organic light emitting diode"). *Id.*, FIG. 1. As shown in Figures 2 (annotated below), 4, 5, 7, and 8, there are at least two pixels in the display ("a plurality of pixels").

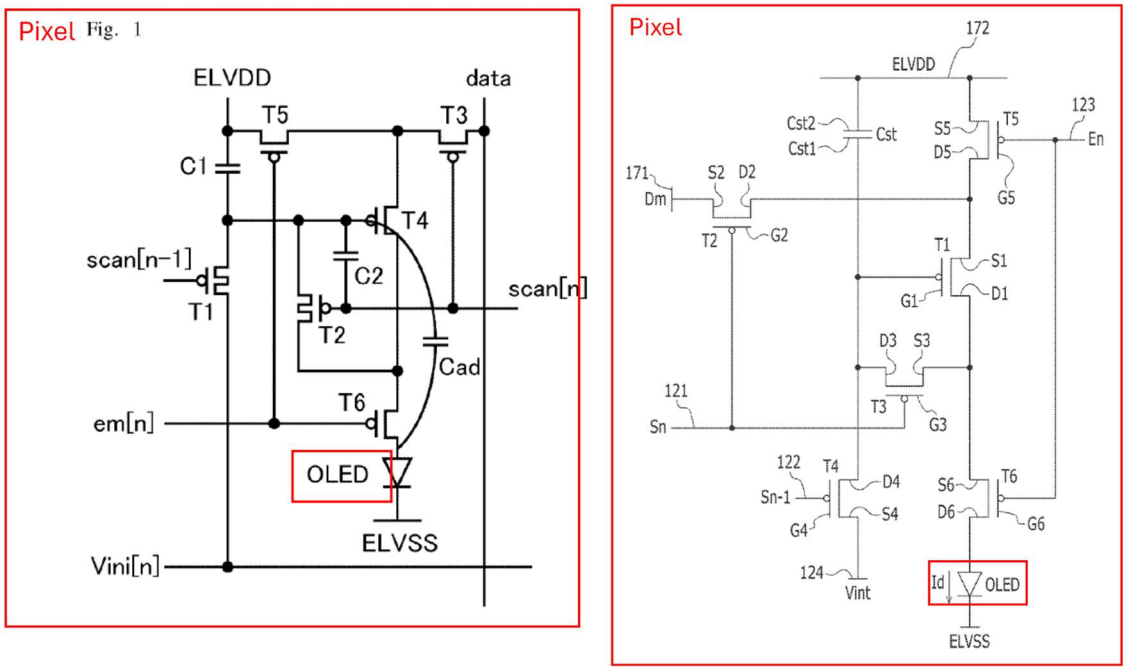
Fig. 2



Noguchi-I, FIG. 2 (annotated).

322. I have further annotated Figure 1 of Noguchi-I alongside Figure 1 of the ’991 Patent to show the driving circuit that is part of each pixel and the pixel’s OLED driven by the circuit.

FIG. 1



Left: Noguchi-I, FIG. 1 (annotated); Right: '991Pat., FIG. 1 (annotated).

323. Plurality of First Voltage Lines (1[b]), Scan Lines (1[c]), and Data Lines (1[[d]])

324. Noguchi-I discloses the "first voltage line" as a "power source line ELVDD" in a second wiring layer. Noguchi-I, ¶71, FIG. 1 (annotated below). In my opinion, a POSITA would have understood ELVDD is a "voltage line" because ELVDD is common notation to denote a voltage to drive a transistor that is also used by the '991 Patent. '991Pat., 6:25-37.

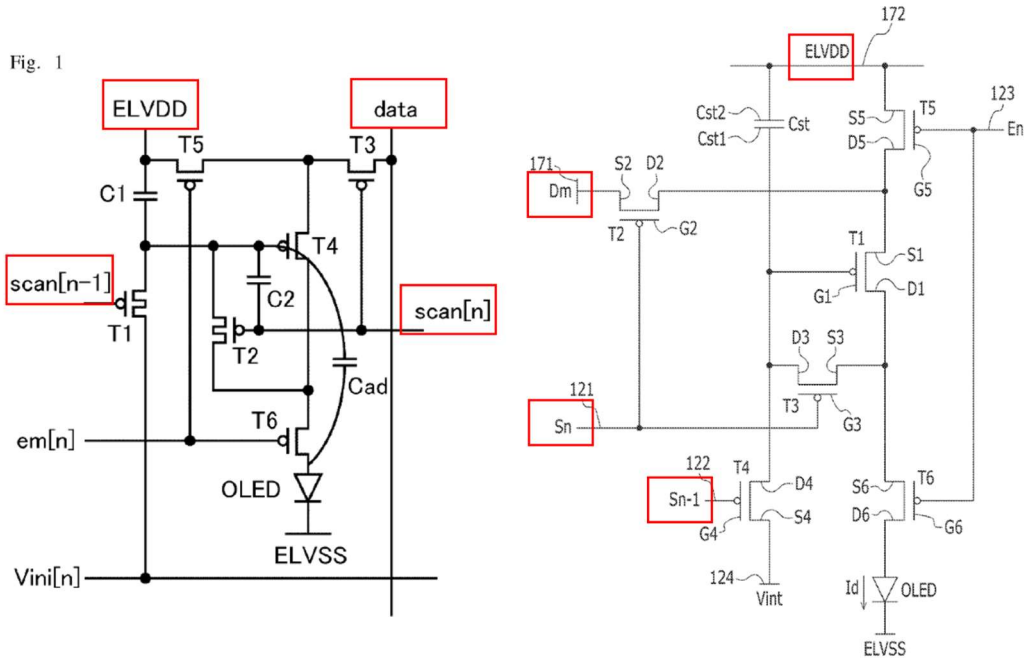
325. Noguchi-I further discloses scan lines (scan[n-1] and scan[n]) in the TFT circuit. Noguchi-I, ¶11; Table, *infra*. I note that Noguchi-I references these scan lines with the nomenclature "n-1" and "n" stating that they denote "an [n−1]-th and

an [n]-th scanning line"—signifying a plurality of scan lines, not limited to the two shown in the circuit. Each pixel structure further includes a data line, data, used in each pixel structure of a display. Noguchi-I, ¶11; Table, *infra*.

326. As I have explained above, a POSITA would have understood that Noguchi-I's circuit (Figures 1-10) represents one of a plurality of pixel structures, all used in the disclosed display and each requiring the voltage and signal lines to be supplied to it. Accordingly, Noguchi-I discloses "a plurality of" voltage, scan, and data lines to each pixel structure.

327. Figure 1 shows "a circuit diagram illustrating a pixel of an organic EL display device." Noguchi-I, ¶44. I have also reproduced annotated Figure 1 of Noguchi-I alongside Figure 1 of the '991 Patent to show the similarities between the circuits and to show Vdd, scan lines, data lines.

FIG. 1



Left: Noguchi-I, FIG. 1 (annotated); Right: '991Pat., FIG. 1 (annotated).

328. Mapping of Noguchi-I to '991 Patent

329. In addition, I have provided the table below to cross-reference each transistor and signal line of '991 Patent to the similarly-described elements in the disclosure of Noguchi-I.

Claims	'991	Noguchi-I	Function
1st TFT	T2	T3	Data input switching TFT
2nd TFT	T1	T4	Driving TFT
3rd TFT	T5	T5	Charging/Power supply / Operation Control TFT
4th TFT	T6	T6	Emission control TFT
5th TFT	T3	T2	Scan[n] switch TFT
6th TFT	T4	T1	Scan[n-1] Init switch TFT
Capacitor	Cst	C1	Storage Capacitor

First Capacitor Plate	125h	Gate electrode 102	
Second Capacitor Plate	127	Shield electrode 104	
1st Voltage line	ELVDD	ELVDD	Power supply
2nd Voltage line	Vint	Vini[n]	Capacitor initialization voltage
OLED	OLED	OLED	
1st Scan line	Sn	scan[n]	Current scan line
2nd Scan line	Sn-1	scan[n-1]	Previous scan line
Light emission control line	En	em[n]	Light emission control
Data line	Dm	data	Data/OLED intensity voltage

d. 1[e]: "a plurality of driving circuits formed on the substrate;"

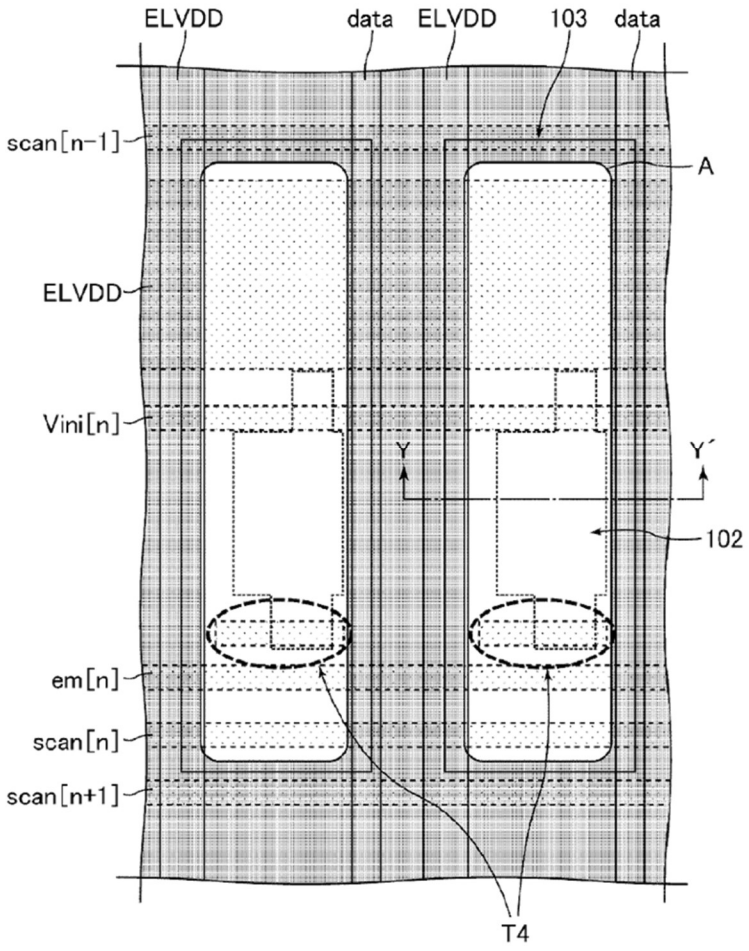
1[f]: "a plurality of organic light emitting diodes, wherein each of the plurality of organic light emitting diodes is electrically coupled to a respective one of the plurality of driving circuits;"

330. In my opinion, Noguchi-I teaches or suggests 1[e] and 1[f].

331. As explained above in 1[b], Noguchi-I teaches or suggests multiple pixels in a display. §VIII.F.3.c. Noguchi-I further describes a "plurality of driving circuits" because it describes a driving circuit for each of the plurality of pixels, where each driving circuit comprises a plurality of TFTs to drive the OLED for that pixel. Noguchi-I, ¶¶1, 11 ("The pixel has six transistors (T1 to T6), two capacitors (C1 and C2), and one organic EL element OLED."), FIG. 1. The TFTs are disposed in the pixel, and a region denoted by "A" in the figures "represents a pixel opening

that functions as the display region of the organic EL display device." Noguchi-I, ¶70, FIG. 2. Furthermore, the '991 Patent admits a "plurality of thin film transistors and capacitors…driv[e] the organic light emitting diode." '991Pat., 1:45-49.

Fig. 2

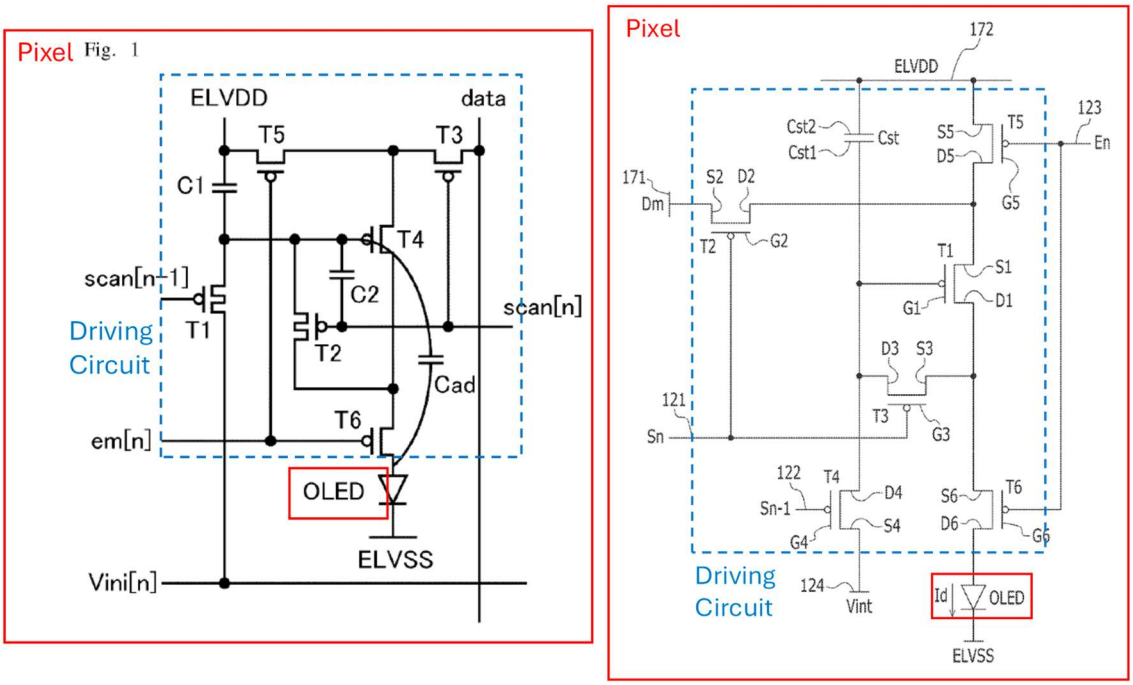


Noguchi-I, FIG. 2.

332. As shown below, each of the TFT driving circuits is connected to an OLED ("each of the organic light emitting diodes being electrically coupled to a respective driving circuit"). *Id.*, ¶31, FIG. 1 (annotated). I have reproduced annotated Noguchi-I's Figure 1 alongside Figure 1 of the '991 Patent to show the relationship

of a pixel and driving circuit.

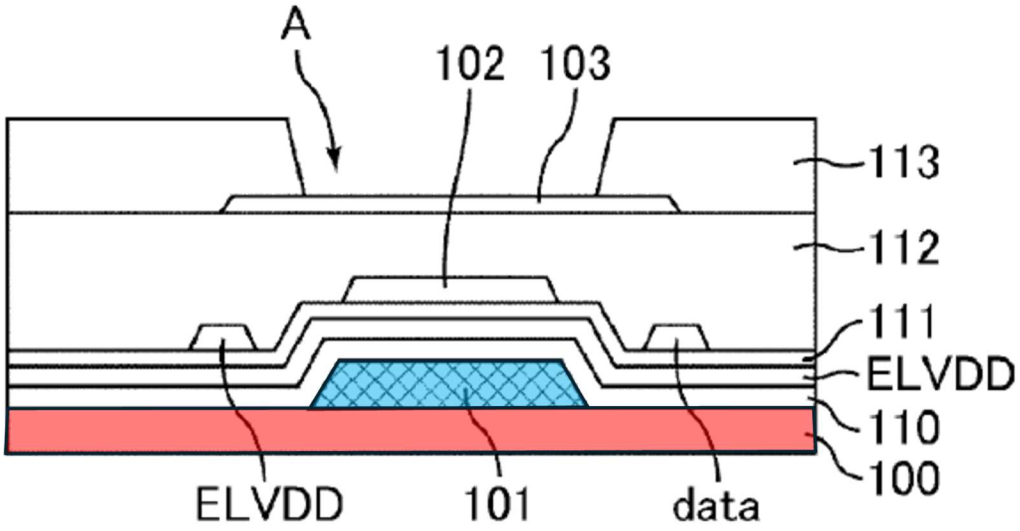
FIG. 1



Left: Noguchi-I, FIG. 1 (annotated); Right: '991Pat., FIG. 1 (annotated).

333. Furthermore, Noguchi-I explains that the TFTs (T1-T6) are formed in a semiconductor layer that is formed on the substrate ("a plurality of driving circuits on the substrate"). Noguchi-I, ¶¶64, 70, FIGs. 8, 9. The substrate and semiconductor layer (blue) are shown in annotated Figure 9 below. Thus, it is my opinion that a POSITA would have understood the plurality of Noguchi-I's driving circuits, including the plurality of TFTs, would have been formed on a single substrate that included multiple pixels.

Fig. 9



Noguchi-I, FIG. 9 (annotated).

334. Furthermore, as shown in annotated Figure 1 above, the OLED is directly connected to T6 ("each of the organic light emitting diodes being electrically coupled to a respective driving circuit"). Noguchi-I, FIG. 1.

335. Accordingly, limitations 1[e] and 1[f] are disclosed by Noguchi-I.

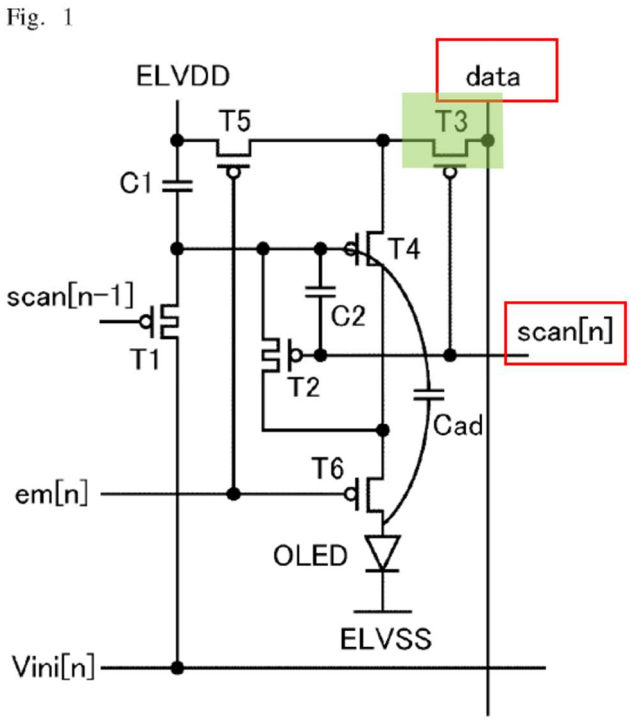
e. 1[g]: "wherein each of the driving circuits comprises: a first thin film transistor implemented in a first portion of a semiconductor layer disposed on the substrate, and coupled to one of the plurality of scan lines and to one of the plurality of data lines;"

336. In my opinion, Noguchi-I teaches or suggests limitation 1[g].

337. Noguchi-I discloses the "first thin film transistor" as T3 that is coupled to "one of the plurality of scan lines," scan[n], and to "a data line," data, as shown

in Noguchi-I's Figure 1. As explained above in 1[e], T3 is formed in a portion of the semiconductor layer on the substrate ("implemented in a first portion of a semiconductor layer disposed on the substrate"). VIII.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9.

338. Referring to the circuit diagram below, Noguchi-I explains that a "transistor T3 **responds to the scan signal inputted from the scanning line scan[n]**, and performs switching of the **data signal inputted from the signal line data**." *Id.*, ¶11, FIG. 1 (annotated). Accordingly, T3 ("first thin film transistor") is electrically connected ("coupled") to scan line scan[n] and a data line ("one of the plurality of scan lines and to one of the plurality of data lines").



Noguchi-I, FIG. 1 (annotated).

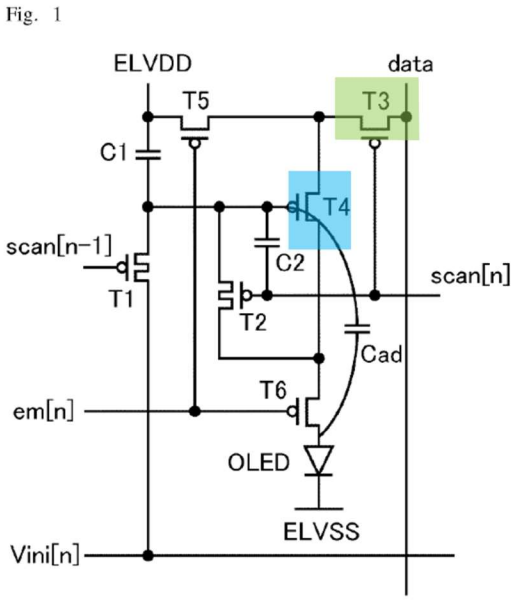
339. Furthermore, as will be explained below, Noguchi-I discloses each of the six transistors and capacitor recited in limitations 1[h]-1[m]. The table in 1[b] above shows the mapping of Noguchi-I's circuit components to those recited in the '991 Patent. *See* §VIII.A.4.c (table).

f. 1[h-1]: "a second thin film transistor implemented in a second portion of the semiconductor layer, wherein the semiconductor layer couples the second thin film transistor to the first thin film transistor, and"

340. In my opinion, Noguchi-I teaches or suggests limitation 1[h-1].

341. As shown in Noguchi-I's Figure 1 circuit, Noguchi-I discloses the

"second thin film transistor" as TFT T4 connected to T3 ("first thin film transistor").

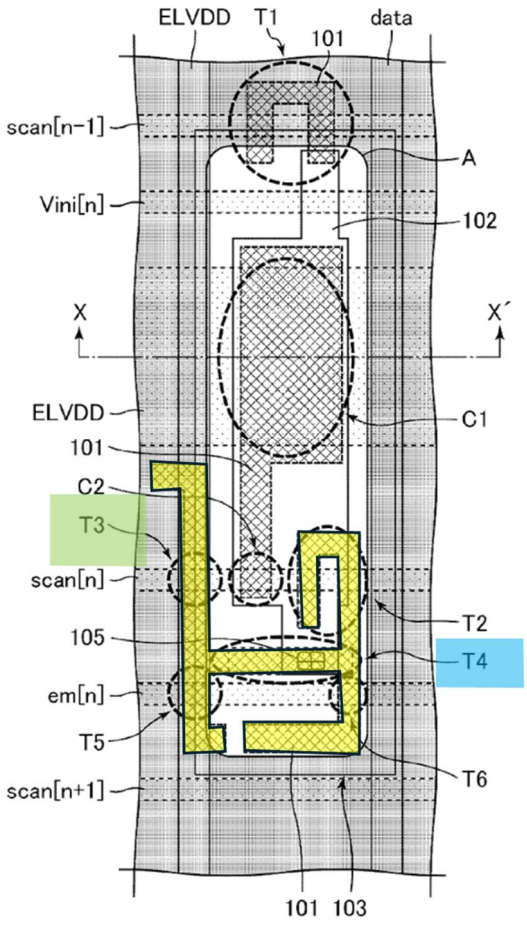


Noguchi-I, FIG. 1 (annotated).

342. As I have explained above in 1[e], T4 is formed in a portion of the semiconductor layer on the substrate ("implemented in a second portion of a semiconductor layer disposed on the substrate"). VIII.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9. I note that Noguchi-I's Figure 8 is a "plan-view schematic diagram[] illustrating a pixel of a conventional organic EL display device provided with a compensation circuit." (Noguchi-I, ¶11). The layout of Figure 8 provides the only illustration of the semiconductor layout in Noguchi-I and is an example of how the TFTs are positioned within the pixel. I have annotated Figure 8 to show the locations of the various TFTs over the depicted semiconductor pattern (yellow) in this

example. As shown therein, T4 is formed in a different portion in the semiconductor layer (yellow) that includes T3 ("first thin film transistor") adjacent to T4. As the example in Figure 8 illustrates, the semiconductor layer is continuous from T4 to T3, and, in my opinion, a POSITA would have found it obvious that "the semiconductor layer couples" T4 to T3. Noguchi-I, FIG. 8 (annotated below); *see also* FIGs. 2, 4, 5, 7 (showing T4 in the same location). Having a semiconductor layer that connects or couples two TFTs was a routine aspect of pixel design and was well known at the time of the alleged invention. *See generally* Kim and Liu.

Fig. 8



Noguchi-I, FIG. 8 (annotated).

343. Accordingly, limitation 1[h-1] is disclosed by Noguchi-I.

g. 1[h-2]: "wherein the second portion of the semiconductor layer has at least one bent portion;"

344. In my opinion, Noguchi-I in combination with Udagawa teaches or suggests 1[h-2].

345. As explained above in Ground 1A for 1[h-2] and 1[n], Udagawa teaches a "bent" channel of drive transistor T4. §§VIII.A.4.g, VIII.A.4.l. For the reasons explained in §VIII.F.2, it is my opinion that a POSITA would have been motivated to incorporate Udagawa's driving TFT gate shapes (thereby increasing the channel length) in Noguchi-I's OLED driving circuit to reduce the dispersion effects that accompany the reduction in size of the driving circuit. Furthermore, modifying Noguchi-I to use Udagawa's longer gate channel is in line with Noguchi-I's objectives of reducing the influence of parasitic capacitance, Cad, because forming the gate channel in this way allows for both a reduction of dispersion and a reduced size while enabling an improved operation of the driving TFT.

346. Accordingly, for the same reasons as I explain in §§VIII.A.4.g and VIII.A.4.l, limitation 1[h-2] is disclosed by Noguchi-I in combination with Udagawa.

h. 1[i]: "a storage capacitor comprising: a first capacitor plate that is configured to operate as a gate electrode of the second thin film transistor;"

1[j]: "a second capacitor plate electrically coupled to one of the plurality of first voltage lines and overlapping the first capacitor plate; and"

1[k]: "an insulating layer between the first capacitor plate and the second capacitor plate;"

347. In my opinion, Noguchi-I teaches or suggests limitations 1[i]-1[k].

348. I have grouped each of the limitations 1[i]-1[k], which are directed to the components of the storage capacitor, for clarity and ease of discussion.

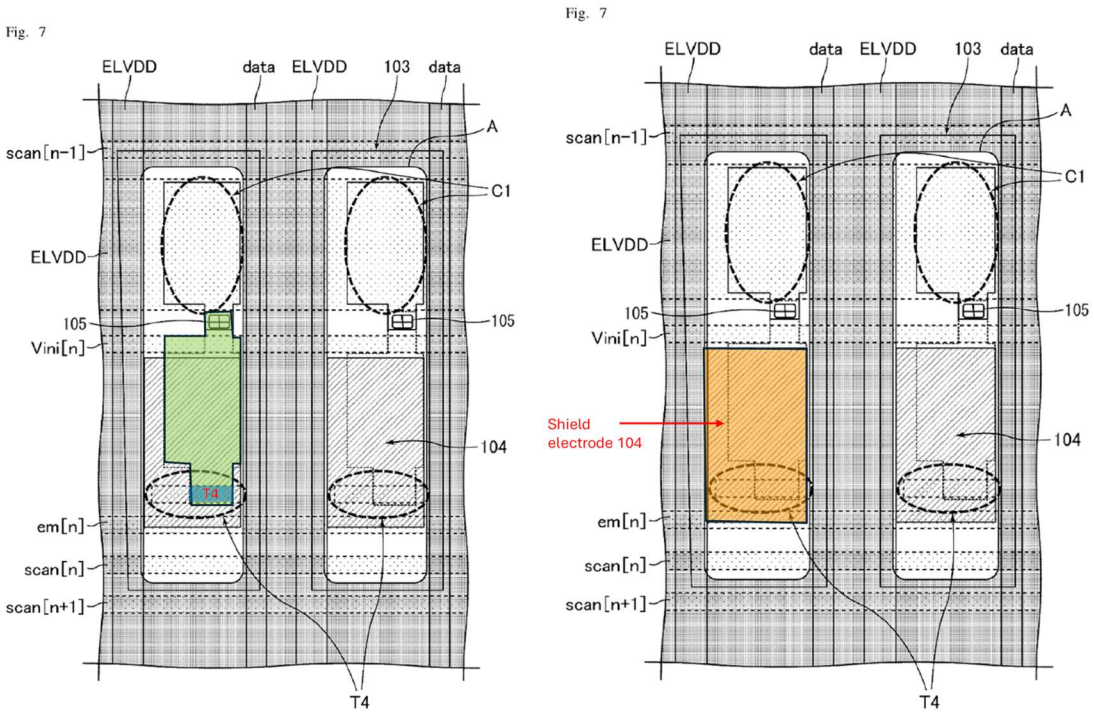
349. Noguchi-I discloses the "storage capacitor" as capacitor C1 that is on one side the gate electrode of T4, on the other side connected to ELVDD, including a gate electrode 102 ("first capacitor plate") in the first wiring layer, and shield electrode 104 ("second capacitor plate") in the second wiring layer. *See* Noguchi-I, ¶¶83-84, 86, 91-93, FIGs. 5, 7.

350. Noguchi-I's Capacitor C1 Structure

351. Noguchi-I explains "capacitor C1 [is] formed through overlap of the gate electrode and the power source line ELVDD" (Noguchi-I, ¶91) and that shield electrode 104 is connected to ELVDD in the second wiring layer. *Id.*, ¶86. Furthermore, Noguchi-I explains that "[t]he gate electrode of T4 forms capacitance with the second wiring layer." *Id.*, ¶95. Thus, it is my opinion that a POSITA would

have understood that Noguchi-I's capacitor is formed in part between gate electrode 102 and overlapping shield electrode 104.

352. The capacitor configuration of Noguchi can be seen in Figure 7 (annotated below), where the gate electrode 102 ("first capacitor plate"), which is the gate electrode of T4 ("configured to operate as a gate electrode of the second thin film transistor"), is annotated in green. Noguchi-I, ¶¶15, 70, 81, 95. Noguchi-I also shows the shield electrode 104 ("second capacitor plate"), annotated in orange.

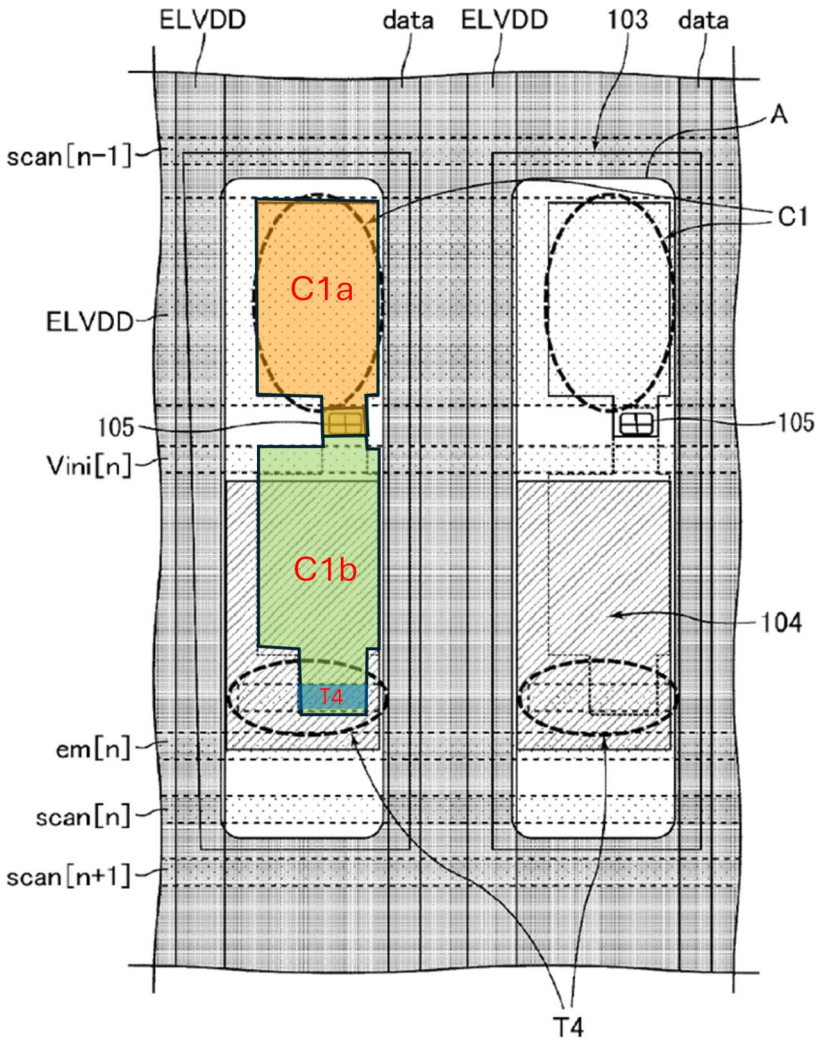


Noguchi-I, FIG. 7 (annotated).

353. While annotated Figure 7 above only shows one part of capacitor C1 (C1b), Noguchi-I's capacitor C1 is made up of two parts, C1a and C1b, connected together through contact hole 105, as annotated below. *see also* Noguchi-I, ¶¶75, 77,

89, 91. Capacitor C1 has a capacitance equal to the series addition C1a and C1b. I have pointed to C1b as meeting the claim limitation of the storage capacitor comprising a first and second capacitor plate.

Fig. 7

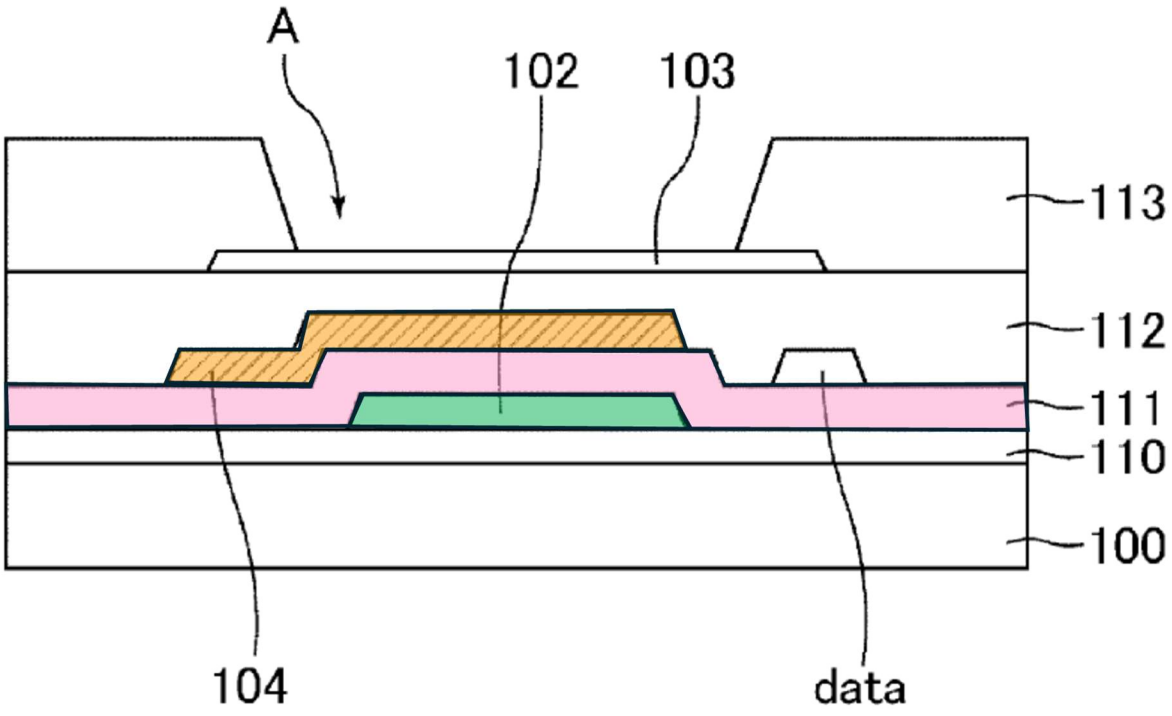


Noguchi-I, FIG. 7 (annotated).

354. As I have explained above, capacitor C1 comprises C1a and C1b, where C1b comprises a gate electrode 102 in the first wiring layer and a shield electrode

104 in the second wiring layer. Noguchi-I, ¶¶91-95. Interlayer dielectric 111 is disposed between 102 and 104 ("an insulating layer between the first capacitor plate and the second capacitor plate"). *Id.*, FIG. 6 (annotated). Noguchi-I further explains that "[t]he first wiring layer (gate electrode 102 of the transistor T4) is disposed between the interlayer dielectric 110 and the interlayer dielectric 111 [and] [t]he second wiring layer (power source line ELVDD and signal line data) is disposed between the interlayer dielectric 111 and the interlayer dielectric 112." Noguchi-I, ¶71. Thus, it is my opinion that a POSITA would have further understood that interlayer dielectric 111 specifically covers T4 ("second" TFT). *Id.*

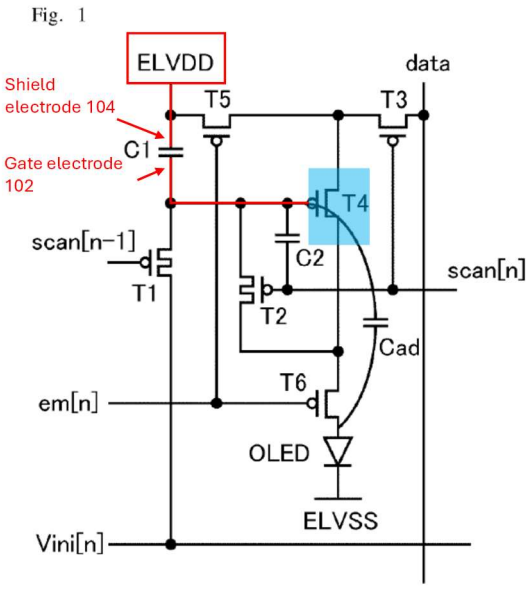
Fig. 6



Noguchi-I, FIG. 6 (annotated).

355. C1 Connections

356. Noguchi-I further discloses capacitor C1 is connected to the gate of T4 and ELVDD, as shown by the red line in Figure 1. Noguchi-I, FIG. 1 (annotated).



Noguchi-I, FIG. 1 (annotated).

357. Accordingly, limitations 1[i]-1[k] are disclosed by Noguchi-I.

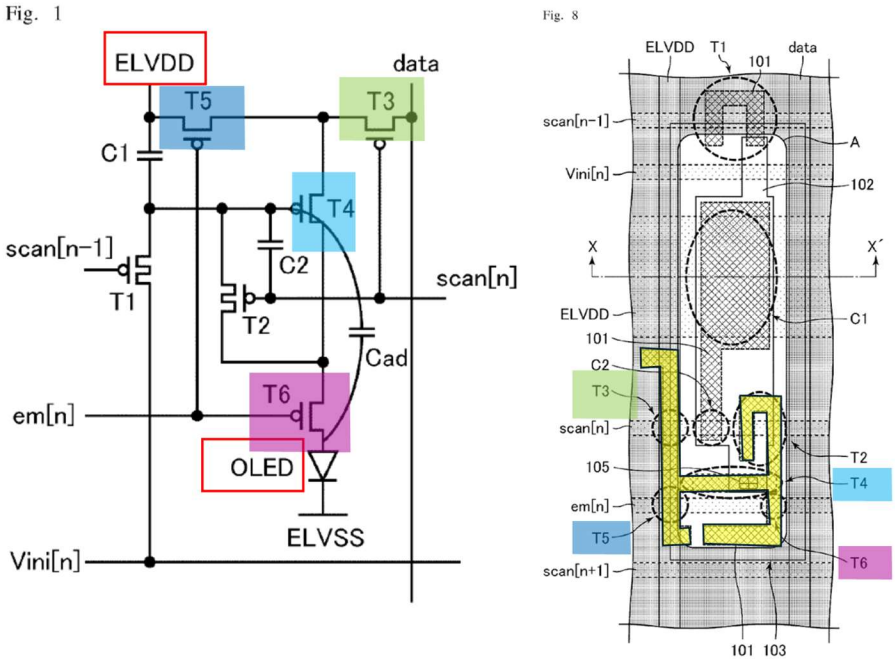
i. 1[l]: "a third thin film transistor implemented in a third portion of the semiconductor layer, wherein the semiconductor layer couples the third thin film transistor to the first thin film transistor and to the second thin film transistor, and wherein the third thin film transistor is electrically coupled to one of the plurality of first voltage lines through the semiconductor layer; and"

1[m]: "a fourth thin film transistor implemented in a fourth portion of the semiconductor layer, wherein the semiconductor layer couples the fourth thin film transistor to the second thin film transistor, and wherein the fourth thin film transistor is electrically coupled to the respective organic light emitting diode through the semiconductor layer; and"

358. In my opinion, Noguchi-I discloses limitations 1[l]-1[m].

359. I have grouped each of limitations 1[l] and 1[m], which are directed to the third and fourth TFTs, for clarity and ease of discussion.

360. As explained in 1[pre] and 1[g], Noguchi-I discloses a TFT driving circuit with at least six transistors and one capacitor. §§VIII.F.3.a, VIII.F.3.e. For reference, the table above in 1[b] shows the mapping for each transistor. §VIII.F.3.c. As explained below and shown in annotated Figures 1 and 8, Noguchi-I discloses each of the recited transistors and connections.



Left: Noguchi-I, FIG. 1 (annotated); Right: Noguchi-I, FIG. 8 (annotated).

361. Regarding 1[l], T5 ("third thin film transistor") is formed in a portion of the semiconductor layer on the substrate ("implemented in a third portion of a semiconductor layer disposed on the substrate"). VIII.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9. Noguchi-I further discloses T5 connected to ELVDD ("electrically coupled to one of the plurality of first voltage lines"), T3 and T4 ("the third thin film transistor [coupled] to the first thin film transistor and to the second thin film transistor"). Noguchi-I, FIG. 1. As shown in annotated Figure 8, T5 is under the ELVDD line ("one of the plurality of first voltage lines") and "performs switching of the current that is supplied to the transistor T4 from the power source line ELVDD." *Id.*, ¶11, FIG. 8.

362. Although not shown, it is my opinion that a POSITA would have found it obvious that a typical way to connect T5 to ELVDD is through a via to the semiconductor layer ("electrically coupled…through the semiconductor layer"), an example of which is disclosed in Noguchi-I as contact hole 105. Vias are well-known in the art and commonly used to connect structures on different levels of a semiconductor structure.

363. Regarding 1[m], Noguchi-I discloses T6 ("fourth thin film transistor") is formed in a portion of the semiconductor layer on the substrate ("implemented in a fourth portion of the semiconductor layer"). VIII.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9. Noguchi-I further discloses T6 connected to T4 ("the fourth thin film transistor [coupled] to the second thin film transistor"), and OLED ("fourth thin film transistor is electrically coupled to the respective organic light emitting diode"). Noguchi-I, FIG. 1. Noguchi-I explains that "T6 responds…performs switching of the current that is supplied to the organic EL element OLED from the transistor T4." *Id.*, ¶11. As explained above, it is my opinion that a POSITA would have found it obvious to use a via to connect T6 from the semiconductor layer to the OLED ("electrically coupled…through the semiconductor layer").

364. As explained in 1[h-1] above, Figure 8 of Noguchi-I illustrates an example of the semiconductor layer that shows T5 is connected to and adjacent to T4 and T3 in the semiconductor layer ("the semiconductor layer couples" T5 to T3

and T4), as recited in 1[l]. Noguchi-I, ¶11, FIG. 8 (annotated). Regarding 1[m], Figure 8 similarly shows T6 is connected to and adjacent to T4 in the semiconductor layer ("the semiconductor layer couples" T6 to T4). Noguchi-I, ¶11, FIG. 8 (annotated). I note that having a semiconductor layer that connects or couples two TFTs was a routine aspect of pixel design and was well known at the time of the alleged invention. *See generally* Kim and Liu.

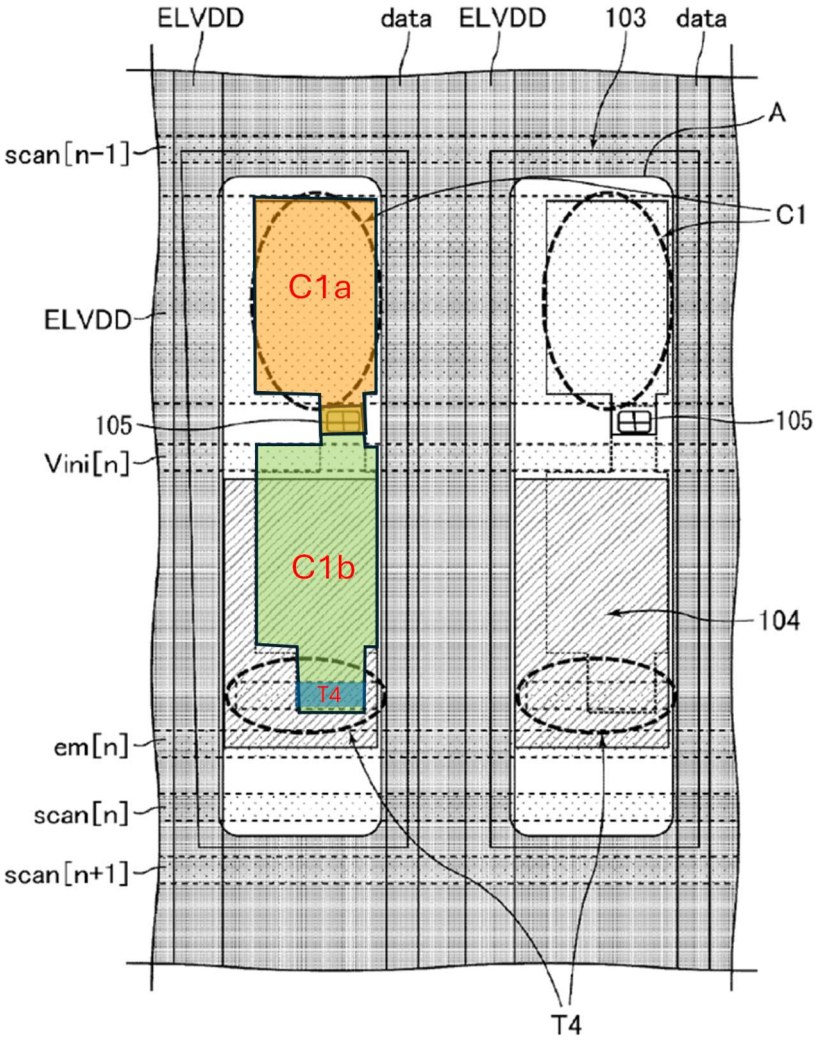
365. Accordingly, limitations 1[l] and 1[m] are disclosed by Noguchi-I.

j. 1[n]: "wherein the bent portion of the second portion of the semiconductor layer is under the first capacitor plate."

366. In my opinion, Noguchi-I teaches or suggests limitation 1[n].

367. As explained in 1[i]-1[k], capacitor C1 is comprised of C1a and C1b, as shown in annotated Figure 7 below. §VIII.F.3.h.

Fig. 7



Noguchi-I, FIG. 7 (annotated).

368. Noguchi-I indicates the position of T4 by a dashed box in Figure 7. Noguchi-I, FIG. 7 (annotated), and I note that the region indicated as T4 in Figure 7 corresponds to the same region for T4 in Figure 8, which shows the semiconductor layer. Thus, in my opinion, a POSITA would have found it obvious that the gate electrode of T4 (i.e., the green-annotated plate in the above figure) covers the

channel region of T4, which includes at least the blue portion in the dashed box in the annotated figure above, including its bent or curved region ("bent portion of the second portion of the semiconductor layer is under the first capacitor plate") when modified by Udagawa.

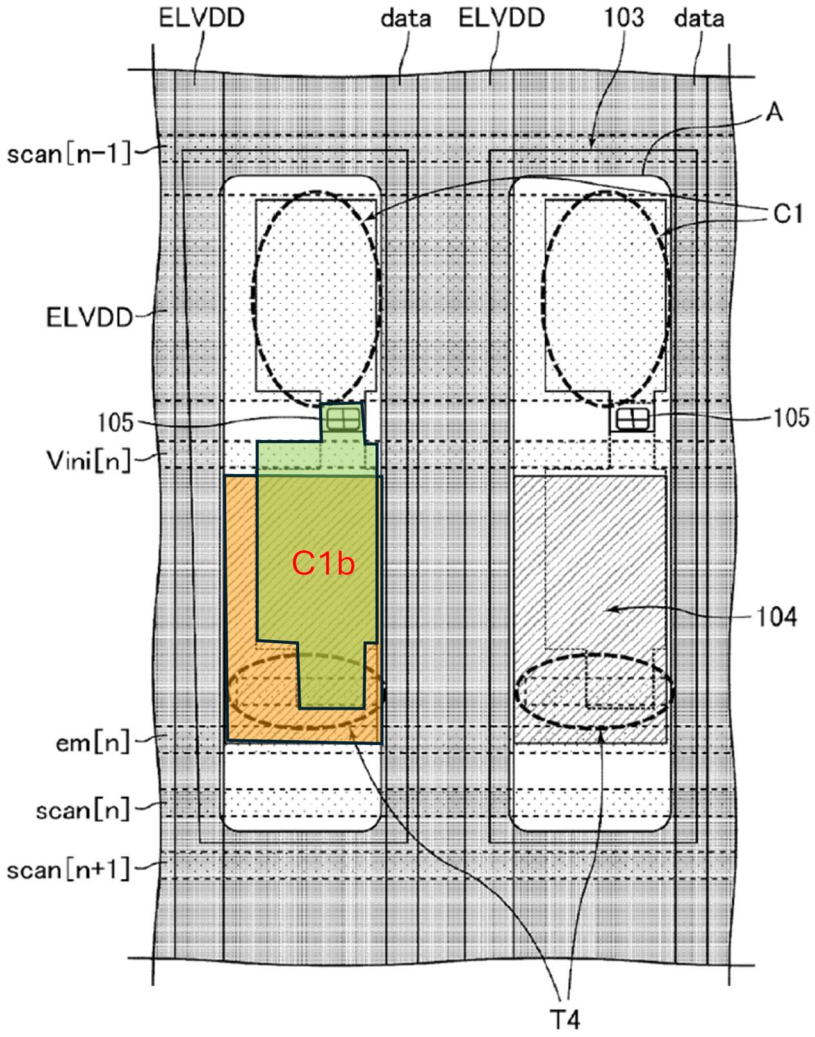
369. Accordingly, limitation 1[n] is disclosed by Noguchi-I.

4. Claim 2: "An organic light emitting diode display according to claim 1, wherein a periphery of the second capacitor plate completely surrounds a periphery of the first capacitor plate in a plan view."

370. In my opinion, Noguchi-I in combination with Udagawa teaches or suggest claim 8.

371. Noguchi-I teaches that shield electrode 104 covers gate electrode 102 (as shown in annotated Figures 6 and 7 below). Noguchi-I, ¶83 ("shield electrode 104 forms a region covering the gate electrode 102"), ¶92 (same), FIGs. 6 (annotated), 7 (annotated). Shield electrode 104 (large orange box at bottom of Figure 7) covers a periphery of gate electrode 102 ("completely surrounds a periphery of the first capacitor plate in a plan view"). As I have explained above in §VIII.A.5 (Ground 1A), a POSITA would have understood that at least a portion around the outside of the first capacitor plate is surrounded.

Fig. 7



Noguchi-I, FIG. 7 (annotated and modified with Noguchi-II).

372. Accordingly, claim 2 is disclosed by Noguchi-I in combination with Udagawa.

5. Claim 3

a. 3[a]: "An organic light emitting diode display according to claim 2, further comprising: a plurality of second voltage lines;"

373. In my opinion, Noguchi-I teaches or suggests limitation 3[a].

374. Noguchi-I discloses the "second voltage line" as initialization voltage line "Vini[n]" that may be formed in the first wiring layer. Noguchi-I, ¶68, FIG. 1 (annotated below). Vini[n] corresponds to Vint in the '991 Patent, described as "initialization voltage line 124." '991Pat., 6:25-37. I have reproduced annotated Figure 1 of Noguchi-I alongside Figure 1 of the '991 Patent to show Vini[n] and Vint.

FIG. 1

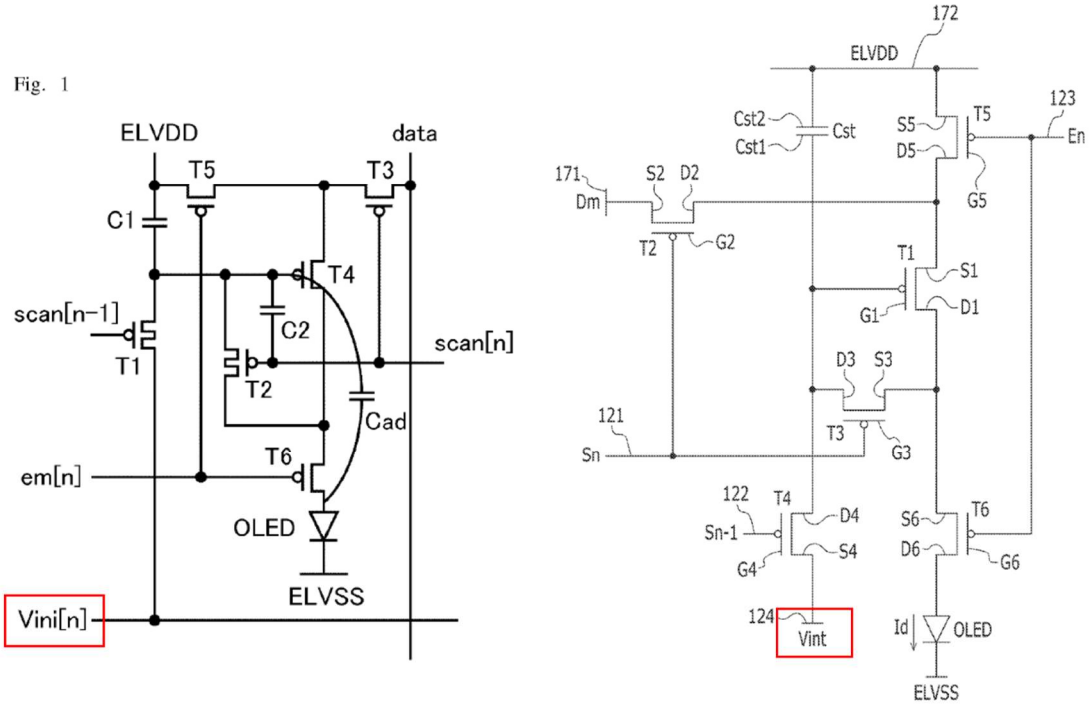


Fig. 1

Left: Noguchi-I, FIG. 1 (annotated); Right: '991Pat., FIG. 1 (annotated).

375. Accordingly, limitation 3[a] is disclosed by Noguchi-I.

b. 3[b]: "a fifth thin film transistor electrically coupled to the first capacitor plate; and"

3[c]: "a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,"

3[d]: "wherein the sixth thin film transistor is coupled to the fifth thin film transistor."

376. In my opinion, Noguchi-I teaches or suggests limitations 3[b]-3[d].

377. I have grouped each of limitations 3[b]-3[d], which are directed to the fifth and sixth TFTs, for clarity and ease of discussion.

378. In my opinion, these limitations are clearly shown in Noguchi-I's Figure 1 (above). Regarding 3[b], Noguchi-I discloses T2 ("fifth thin film transistor") connected to the gate electrode 102 of T4 ("first capacitor plate"). Noguchi-I, FIG 1. Regarding 3[c] and 3[d], Noguchi-I discloses T1 ("sixth thin film transistor") connected to Vini[n] ("one of the plurality of second voltage lines"), T2, and gate electrode 102 of T4. *Id.*, FIG 1.

379. Accordingly, the TFTs and electrical connections in claim 3 are disclosed by Noguchi-I.

6. Claim 4: "An organic light emitting diode display according to claim 3, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer."

Claim 5: "An organic light emitting diode display according to claim 4, wherein the first capacitor plate and the plurality of scan lines are composed of the same material."

380. In my opinion, Noguchi-I in combination with Udagawa teaches or suggests claims 4 and 5.

381. I have grouped each of claims 4 and 5, which are directed to the first capacitor plate and plurality of scan lines, for clarity and ease of discussion.

382. Regarding claim 4, as explained above in 1[i], Noguchi-I teaches a storage capacitor where the gate electrode 102 ("first capacitor plate") is the gate of T4. §VIII.F.3.h. Noguchi-I explains that scan[n] ("the first scan line") is in the first wiring layer. Noguchi-I, ¶68, FIG. 2. Noguchi-I further discloses that gate electrode 102 is also in the first wiring layer ("same material layer"). *Id.*, ¶75, FIG. 45. Therefore, Noguchi-I's scan lines and first capacitor plates were in the same first wiring later.

383. Regarding claim 5, Noguchi-I further explains that a "wiring layer is ordinarily low-resistance wiring (metal wiring)" (*id*., ¶63), which would have made it obvious to a POSITA that the metal components, including the first capacitor plate and the first scan line, in the first wiring layer were made of the same material.

384. Accordingly, claims 4 and 5 are disclosed by Noguchi-I in combination

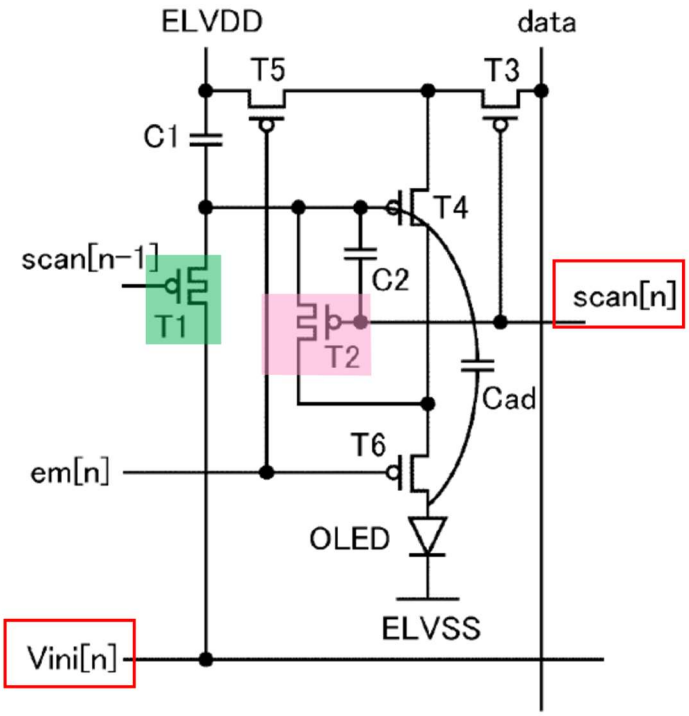
with Udagawa.

7. Claim 6: "An organic light emitting diode display according to claim 4, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines."

385. In my opinion, Noguchi-I teaches or suggests claim 6.

386. As shown below, Noguchi-I discloses T2 ("fifth thin film transistor") connected to scan[n] ("one of the plurality of scan lines"). Noguchi-I, FIG 1. Noguchi-I further discloses T1 ("sixth thin film transistor") connected to scan[n-1] ("another one of the plurality of scan lines"). *Id.*, FIG 1.

Fig. 1



Noguchi-I, FIG. 1 (annotated).

387. Accordingly, claim 6 is disclosed by Noguchi-I.

8. Claim 17

a. 17[pre] An organic light emitting diode display according to claim 1, further comprising:

b. 17[a] a plurality of second voltage lines;

c. 17[b] a fifth thin film transistor electrically coupled to the first capacitor plate; and

d. 17[c] a sixth thin film transistor electrically coupled to one of the plurality of second voltage lines and to the first capacitor plate,

e. 17[d] wherein the sixth thin film transistor is coupled to the fifth thin film transistor.

388. Noguchi-I discloses claim 17 for the same reasons as explained in claim 3. §VIII.F.5.

9. Claim 18: "An organic light emitting diode display according to claim 17, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer."

Claim 19: "An organic light emitting diode display according to claim 18, wherein the first capacitor plate and the plurality of scan lines are composed of the same material."

389. Noguchi-I discloses claims 18 and 19 for the same reasons as explained in claims 4 and 5, respectively. §VIII.F.6.

10. Claim 20: "An organic light emitting diode display according to claim 18, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines."

390. Noguchi-I discloses claim 20 for the same reasons as explained in claim 6. §VIII.F.7.

G. Ground 2B: Claims 10-13 and 23-26 are Unpatentable over the Combination of Noguchi-I, Udagawa, and Kim

1. Summary of Kim

391. Kim (EX1013) is a U.S. Patent entitled "Organic Light Emitting Diode Display," with a filing date of October 25, 2007 (published October 9, 2008; claiming the priority benefit of Korean Patent Application No. 10-2007-0033745 filed April 5, 2007). In Kim, the electrode structure of the OLED display is configured to prevent a contact error of a dual-capacitor. Kim, 3:50-52. In my opinion, Kim is analogous art to the '991 Patent because both patent are in the same field of endeavor. For example, both are directed to compensating for threshold voltage deviation. Kim, 1:61-63.

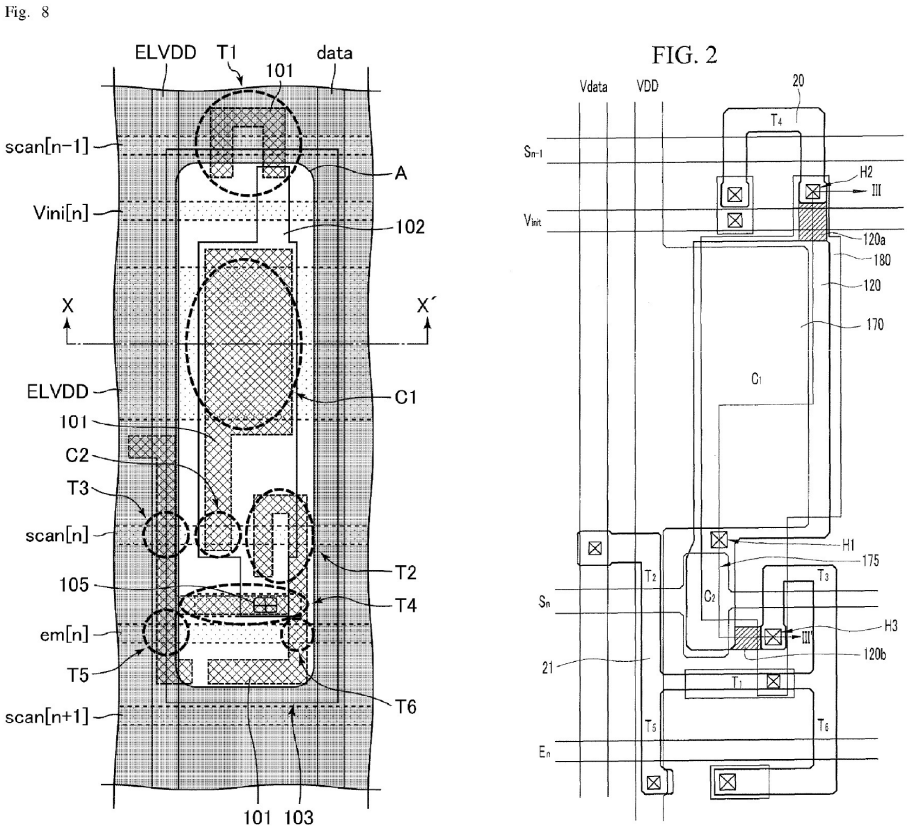
392. Kim teaches contact errors in the dual-structure capacitor can be prevented by the active pattern (1) functioning as the first electrode of the first capacitor and being extended to be connected to the semiconductor layer included in the transistor connected between a power source VDD that supplies a power

supply voltage and a power source Vinit that supplies an initial voltage, and (2) functioning as the first electrode of the second capacitor and being extended to be connected to the semiconductor layer included in the transistor that transmits the data voltage to the driving transistor in response to the selection signal from the current scan line. *Id.*, 5:41-6:16.

2. Motivation to combine Noguchi-I, Udagawa, and Kim

393. In my opinion, there are several reasons that motivate combining the teachings of Noguchi-I and Kim.

394. Kim, similar to Noguchi-I, is related to OLED displays. Kim, 5:41-6:16. In particular, Noguchi-I and Kim both described similar OLED drive circuits that included six TFTs and two capacitors (6T2C circuits) (Noguchi-I, FIG. 1; Kim, FIG. 5), and both described forming TFTs on a substrate within an OLED pixel in strikingly similar configurations. Noguchi-I, FIG. 8; Kim, FIG. 2 (reproduced below).



Left: Noguchi-I, FIG. 8; Right: Kim, FIG. 2.

395. While Noguchi's semiconductor pattern that started around the bottom of the pixel area (at T6) and extended to the top of the pixel (at T1) included discontinuities, Kim's semiconductor pattern did not. *See* Noguchi-I, FIG. 8; Kim, FIG. 2 (annotated below in §G.3.c). In this combination, the Noguchi-I pixel layout is modified based on the teachings of Kim to form a contiguous semiconductor pattern. *See* §IV.H.3. In my opinion, a POSITA would have been motivated and would have found it obvious to make this modification because Kim's continuous semiconductor pattern constituted a known alternative that required less masking to Noguchi-I's non-contiguous pattern. Furthermore, such a modification amounted to

a simple design choice that involved a routine task of making minor changes to the semiconductor pattern and was well within the skill set of a POSITA.

396. It is my opinion that a POSITA would further recognize that there is no interference among the modifications of Kim and Udagawa, and each combination can be implemented without affecting the others. Accordingly, in my opinion, a POSITA would have found it obvious and would have been motivated to combine Noguchi-I with each of Udagawa and Kim, and would have had a reasonable expectation of success.

397. Additional details regarding the Noguchi-I−Udagawa−Kim combination are provided below in connection with specific claim limitations.

3. Claim 10

a. 10[a] An organic light emitting diode display according to claim 2, further comprising: a plurality of second voltage lines;

398. Noguchi-I discloses limitation 10[a] for the same reasons as explained in limitation 3[a]. §VIII.F.5.a.

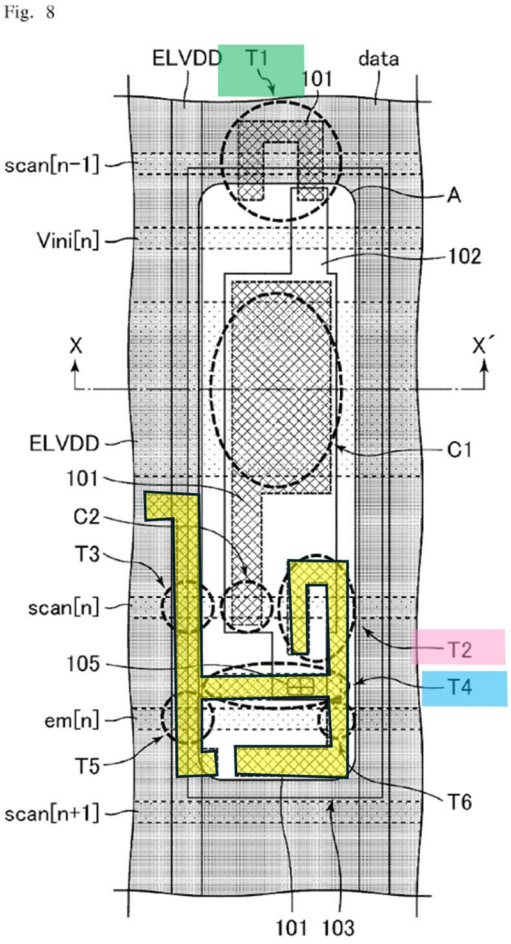
b. 10[b] a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

399. In my opinion, Noguchi-I teaches or suggests limitation 10[b].

400. Noguchi-I discloses T2 (“fifth thin film transistor”) is formed in a

portion of the semiconductor layer on the substrate ("implemented in a fifth portion of the semiconductor layer"). §VIII.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9. *See also* element 1[h-1] in Ground 1A.

401. As shown below in annotated example layout in Figure 8, T2 and T4 are adjacent in the contiguous semiconductor layer ("the semiconductor layer couples the fifth thin film transistor to the second thin film transistor"). Having a semiconductor layer that connects or couples two TFTs was a routine aspect of pixel design and was well known at the time of the alleged invention. *See generally* Kim and Liu.



Noguchi-I, FIG. 8 (annotated).

402. Accordingly, limitation 10[b] is disclosed by Noguchi-I.

c. 10[c] a sixth thin film transistor implemented in a sixth portion of the semiconductor layer,

10[d] wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and

403. In my opinion, Noguchi-I teaches or suggests limitations 10[c] and 10[d]. I have grouped each of limitations 10[c] and 10[d], which are directed to the

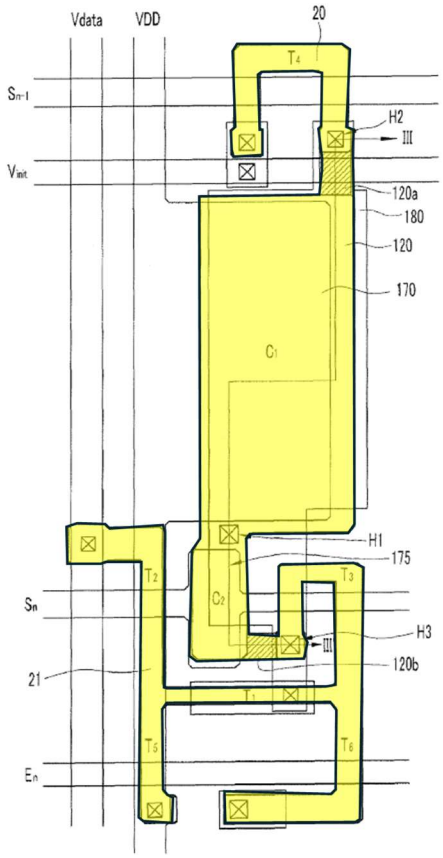
sixth TFT, for clarity and ease of discussion.

404. Noguchi-I discloses T1 ("sixth thin film transistor") is formed in a portion of the semiconductor layer on the substrate ("implemented in a sixth portion of the semiconductor layer"). §VIII.F.3.d; Noguchi-I, ¶¶64, 70, FIGs. 8, 9.

405. To the extent that it is argued that Noguchi-I does not teach or suggest "the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor" because of a discontinuity in the portion of the semiconductor pattern that extends to T1, it is my opinion that a POSITA would have found it obvious to modify Noguchi-I to have a contiguous semiconductor pattern based on the teachings of Kim.

406. Kim describes a TFT driving circuit similar to Noguchi-I's Figure 1. *See* Kim, 7:34-8:51; FIG. 5. Kim further provides a layout of the transistors that is similar to Noguchi-I's Figure 8. *See* Kim, 5:12-18, FIG. 2. Kim explains that **T4 in Figure 2 is connected to T3 using semiconductor patterns 120, 120a and 120b**. Kim, 6:29-49. Annotated Figure 2 below shows an example of the semiconductor layer of Kim, showing a contiguous semiconductor pattern that extends to all TFTs.

FIG. 2



Kim, FIG. 2 (annotated).

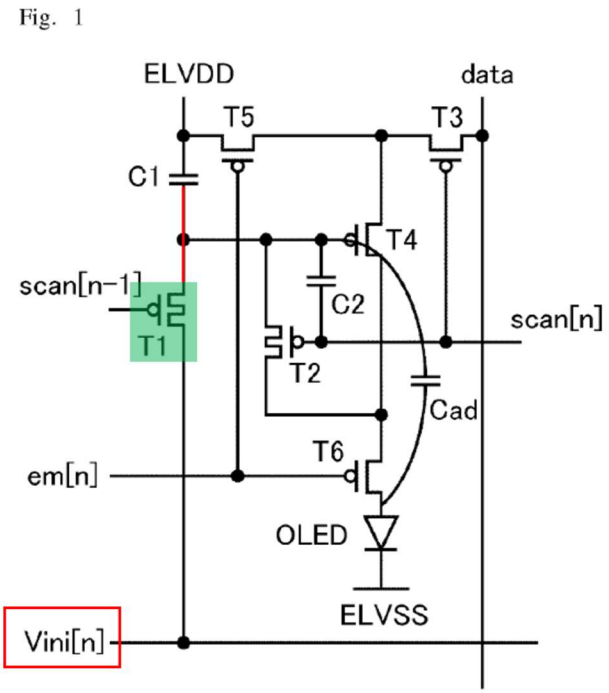
407. For reasons explained in §VIII.G.2, a POSITA would have been motivated to utilize the teachings of Kim to modify Noguchi-I's semiconductor pattern to contiguously extend to TFT T1.

408. In my opinion, extending the connectivity of the semiconductor pattern based on Kim does not change any other analysis above regarding the above claims. *See* §VIII.F. Accordingly, limitations 10[c] and 10[d] are disclosed by Noguchi-I.

d. 10[e] wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

409. In my opinion, Noguchi-I teaches or suggests limitation 10[e].

410. As explained in limitation 3[c], T1 is connected to Vini[n] and gate electrode 102 of T4. §VIII.F.5.b.



Noguchi-I, FIG. 1 (annotated).

411. While Figure 1 of Noguchi-I clearly shows the connection of T1 ("sixth" TFT) to the first capacitor plate on one side and T1 to Vini ("second voltage line") on the other side, it does not provide an explicit figure to illustrate the mechanism for making those connections.

412. As explained above in 1[l], vias (e.g., contact holes) were a well-known and common method of connecting a semiconductor layer to signal lines, such as Vini[n]. §VIII.F.3.i. Thus, in my opinion, a POSITA would have found it obvious to connect the portion of the semiconductor layer of T1 to Vini[n] through a via because Vini resided on an upper layer ("electrically coupled…through the semiconductor layer"), and would have found it equally obvious to use a via to connect the semiconductor layer of T1 to gate electrode ("first capacitor plate") 102 that also resided in a different layer (i.e., in the first wiring layer).

413. Accordingly, limitation 10[e] is disclosed by Noguchi-I.

4. Claim 11: "An organic light emitting diode display according to claim 10, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer."

Claim 12: "An organic light emitting diode display according to claim 11, wherein the first capacitor plate and the plurality of scan lines are composed of the same material."

Claim 24: "An organic light emitting diode display according to claim 23, wherein the first capacitor plate and the plurality of scan lines are disposed in the same layer."

Claim 25: "An organic light emitting diode display according to claim 24, wherein the first capacitor plate and the plurality of scan lines are composed of the same material."

414. Noguchi-I discloses claims 11 and 24 and claims 12 and 25 for the same

reasons as explained in claim 4 and claim 5, respectively. §VIII.F.6.

5. Claim 13: "An organic light emitting diode display according to claim 11, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines."

415. Noguchi-I discloses claim 13 for the same reasons as explained in claim 6. §VIII.F.7.

6. Claim 23

a. 23[pre] An organic light emitting diode display according to claim 1, further comprising:

b. 23[a] a plurality of second voltage lines;

c. 23[b] a fifth thin film transistor implemented in a fifth portion of the semiconductor layer, wherein the semiconductor layer couples the fifth thin film transistor to the second thin film transistor; and

d. 23[c] a sixth thin film transistor implemented in a sixth portion of the semiconductor layer, wherein the semiconductor layer couples the sixth thin film transistor to the fifth thin film transistor, and wherein the sixth thin film transistor is electrically coupled to one of the plurality of second voltage lines and the first capacitor plate through the semiconductor layer.

416. Noguchi-I discloses claim 23 for the same reasons as explained in claim 10. §VIII.G.3.

7. Claim 26: "An organic light emitting diode display according to claim 24, wherein the fifth thin film transistor is coupled to one of the plurality of scan lines, and the sixth thin film transistor is coupled to another one of the plurality of scan lines."

417. Noguchi-I discloses claim 26 for the same reasons as explained in claim 6. §VIII.F.7.

H. Ground 2C: claims 7 and 21 are Unpatentable over Noguchi-I, Udagawa, Noguchi-II, and Jeong

1. Summary of Noguchi-II

418. Noguchi-II (EX1012) is a U.S. Patent Application Publication entitled "Active Matrix Substrate, Display Device, and Organic EL Display Device," with a filing date of January 24, 2012 (published May 24, 2012; claiming the priority benefit of Japanese Patent Application No. 2009-175702 filed July 28, 2009). In Noguchi-II, a circuit diagram of a pixel of an organic EL display device is configured similarly to the circuit shown in Figure 1 of the '991 Patent (i.e., with scan lines, data lines, and six transistors), but additionally includes a transistor T7 as an adjusting transistor for adjusting the voltage of a pixel electrode of an organic EL element OLED, i.e., a seventh transistor. Noguchi-II, ¶¶77, 90-91.

419. In my opinion, Noguchi-II is analogous art to the '991 Patent because it is in the same field of endeavor. For example, both are directed to compensating the threshold voltage of the driving transistor. Noguchi-II, ¶42.

420. Noguchi-II teaches transistor T7 is an adjusting transistor for adjusting the voltage of a pixel electrode of an organic EL element OLED. *Id.*, ¶77. Herein, the source electrode and the drain electrode of the transistor T7 are connected in parallel to the organic EL element OLED. Consequently, the voltages of the anode and cathode of the organic EL element OLED may be the same as each other. This enables discharge of charge, which is stored in the Cad, through a power supply line ELVSS using the transistor T7 as a path for electric current. As a result, display characteristics without any occurrences of the stepwise response characteristics can be achieved. *Id.*, ¶91.

2. Summary of Jeong

421. Jeong (EX1009) describes a circuit of a pixel having an improved response time that is configured similarly to the circuit shown in Figure 1 of the ’991 Patent and Noguchi-I (i.e., with scan lines, data lines, and six transistors). Jeong, Abstract. The 6T1C circuit of Jeong can be configured such that the initialization power supply for supplying the initialization voltage (VINT) of the pixel can be set to the same voltage source as a power supply that supplies a low potential pixel power from the outside (ELVSS). *Id.*, ¶¶40, 52.

422. In my opinion, Jeong is analogous art to the ’991 Patent because it is in the same field of endeavor. For example, both are directed to compensating the

threshold voltage of the driving transistor. Jeong, ¶¶85-86, 89.

3. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, and Jeong

423. In my opinion, there are several reasons that motivate combining the teachings of Noguchi-I and each of Noguchi-II and Jeong.

424. As discussed above, Noguchi-I is directed to the pixel structure of an OLED display (in a 6T1C circuit configuration), which is susceptible to visual aberrations that are likely caused by the Cad. Noguchi-I, ¶¶12, 15, 17, 70. It is my opinion that Noguchi-II, which shares the same inventor as Noguchi-I, is analogous art to Noguchi-I because it is in the same field of endeavor.

425. Noguchi-II proposes adding an additional adjusting transistor, i.e., a seventh transistor, to the 6T1C circuit to achieve display characteristics without any occurrences of the visual aberration. Noguchi-II, ¶¶77, 91.

426. In my opinion, a POSITA would have found it obvious to combine the complementary teachings of Noguchi-I with Noguchi-II to reduce the Cad, and specifically add Noguchi-II's seventh (adjusting) TFT to Noguchi-I's pixel structure of the OLED display. This combination would have been obvious to a POSITA based on the shared objective of Noguchi-I's and Noguchi-II's to reduce the Cad, and the additional improvement gained by implementing Noguchi-II's seventh TFT.

427. I note that a POSITA would have been motivated to add a seventh TFT

to Noguchi-I's pixel structure to yield the predictable result of the Cad being reduced). In my opinion, a POSITA would have had a reasonable expectation of success, because adding a seventh TFT to a 6T1C circuit to reduce parasitic capacitance was already described in Noguchi-II, and such modifications were well within the skill set of a POSITA.

428. It is also my opinion that a POSITA would have also combined Noguchi-I with Jeong with the understanding that Vini[n] is the same voltage source as ELVSS. Jeong, ¶¶52, 54. Setting Vini[n] to ELVSS is merely a design choice. *Id.*, ¶52 ("initialization power supply supplying…may be supplied according to the design structure of the pixel").

429. Furthermore, and as discussed above, the Noguchi-I reference can be combined individually with each of Udagawa, Noguchi-II, and Jeong. In each instance, the combination involves modifying a distinct aspect of Noguchi-I, and these modifications are independent of one another. For example, Udagawa teaches modifying the shape of the gate electrode to a serpentine shape, Noguchi-II teaches modifying the 6T1C circuit by incorporating a seventh TFT, and Jeong teaches setting the initialization voltage (VINT) of the pixel to the same voltage source as a power supply that supplies a low potential pixel power from the outside (ELVSS). A POSITA would have recognized that there is no interference among the modifications, and each combination can be implemented without affecting the

others. Accordingly, in my opinion, a POSITA would have found it obvious and would have been motivated to combine Noguchi-I with each of Udagawa, Noguchi-II, and Jeong, and would have had a reasonable expectation of success.

430. Additional details regarding the Noguchi-I−Udagawa−Noguchi-II−Jeong combination are provided below in connection with specific claim limitations.

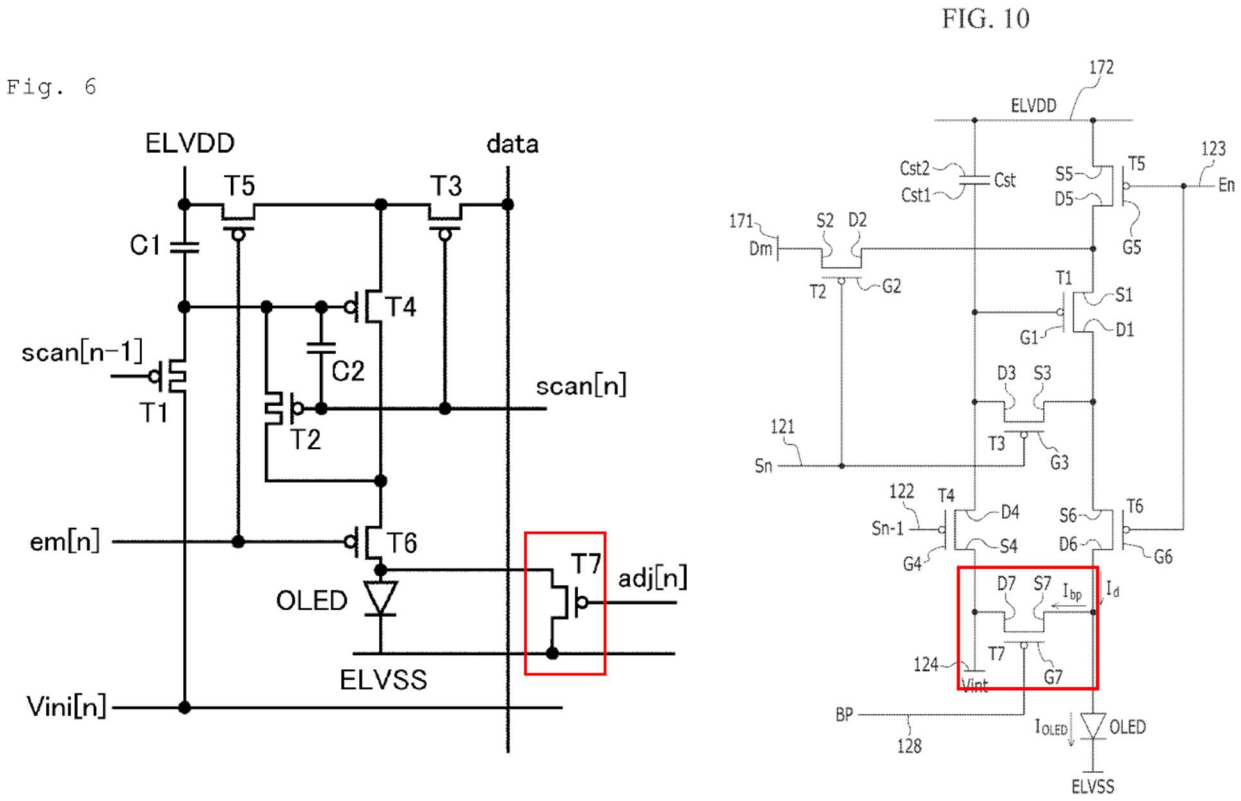
4. Claim 7: "An organic light emitting diode display according to claim 4, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor."

Claim 21: "An organic light emitting diode display according to claim 18, further comprising a seventh thin film transistor electrically coupled to one of the plurality of second voltage lines and the respective organic light emitting diode, wherein the seventh thin film transistor is coupled to the fourth thin film transistor."

431. In my opinion, Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong teach or suggest claims 7 and 21.

432. Noguchi-I discloses that its driving circuit can have more than or less than six TFTs. Noguchi-I, ¶95 ("TFTs and so forth have been omitted in the figures."). As explained above, Noguchi-II discloses an OLED drive circuit similar to those described in Noguchi-I and in Figure 10 of the '991 Patent, which

additionally includes a seventh TFT. §VIII.H.1. I have reproduced Figure 10 from the '991 Patent and Figure 6 from Noguchi-II below, highlighting the seventh TFT.



Left: Noguchi-II, FIG. 6 (annotated); Right: '991Pat., FIG. 10 (annotated).

433. As shown below, Noguchi-II's circuit is nearly identical to Noguchi-I, except for the additional seventh TFT (T7).

Fig. 6

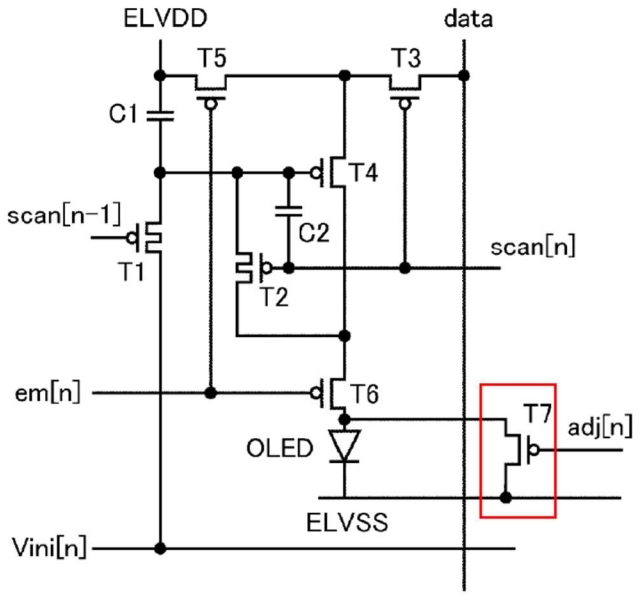
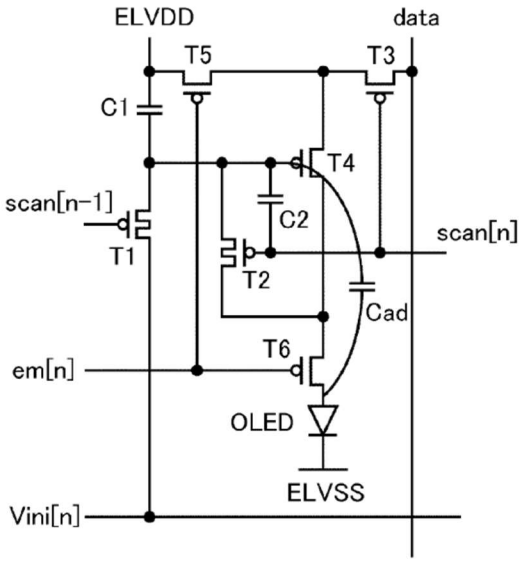


Fig. 1



Left: Noguchi-II, FIG. 6 (annotated); Right: Noguchi-I, FIG. 1.

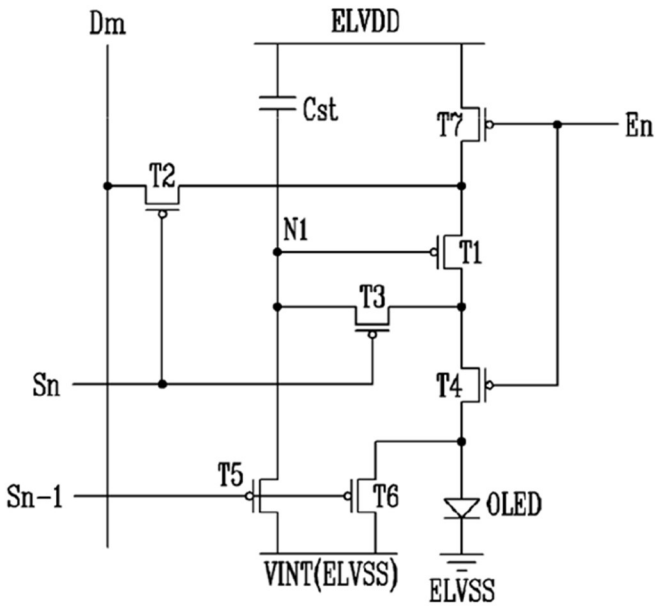
434. Noguchi-II discloses T7 in Figure 6 connected ("electrically coupled") to T6 ("fourth thin film transistor") and the OLED ("respective organic light emitting diode"). Noguchi-II, ¶¶77, 90-91. Noguchi-II explains the addition of T7 prevents "occurrence of the stepwise response characteristics" that occurs because of parasitic capacitance, Cad. *Id.*, ¶¶16, 91.

435. In my opinion, a POSITA would have been motivated to modify Noguchi-I to incorporate Noguchi-II's seventh TFT to further reduce the effects of parasitic capacitance, Cad. Such a modification would have improved the performance of Noguchi-I drive circuit with minimal increase in size. Furthermore, as shown above, Noguchi-II and Noguchi-I's circuits are identical except for the

additional TFT. *Id.*

436. While Noguchi-II shows the drain of T7 is connected to ELVSS (and the drain of T1 is connected to Vini[n]), it was well-known and obvious at the time of the '991 Patent that the initialization voltage Vini[n] and ELVSS could be connected together. The connection between Vini[n] and ELVSS is a fundamental design feature in AMOLEDs, and allows the establishment of a common reference point or "ground" for the entire display subsystem. By connecting Vint and ELVSS together, the designers tie the Vint ground to the ELVSS ground, which creates a single, unified 0V reference point for the entire display system. This is specifically shown in Jeong. Jeong, ¶¶52 ("the third power supply supplying the third power (VINT)… may be set to the same Voltage source as the second power supply supplying the second power (ELVSS)."), 54, FIG. 2. Thus, it would have been understood that Vini[n] ("second voltage line") and ELVSS are connected to the same voltage source (or line). Indeed, Noguchi-II confirms this understanding by explaining that Vini[n] discharges capacitors C1 and C2, which can occur when Vini[n] is set to ELVSS. Noguchi-II, ¶¶8, 24; Noguchi-I, ¶23. Accordingly, it would have been obvious that, in the combination, T7 is connected to Vini[n]/ELVSS ("second voltage line").

FIG. 2



Jeong, FIG. 2.

437. As explained above in §VIII.H.2, the motivation to combine such teachings, e.g., to incorporate an additional TFT, would have been straightforward, and an obvious addition to improve the functionality of the drive circuit because Noguchi-I and Noguchi-II share the same inventor and describe the same pixel circuit. *Compare* Noguchi-I, FIGS. 1, 8-9, *with* Noguchi-II, FIGS. 7-9. Both Noguchi's are also concerned with reducing parasitic capacitance, Cad. Noguchi-I, ¶15; Noguchi-II, ¶54.

438. Accordingly, claims 7 and 21 are disclosed by Noguchi-I in combination with Udagawa, Noguchi-II, and Jeong.

I. Ground 2D: Claims 14 and 27 are Unpatentable over the Combination of Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim

1. Motivation to combine Noguchi-I, Udagawa, Noguchi-II, Jeong, and Kim

439. As I have discussed above, the Noguchi-I reference can be combined individually with each of the cited reference—Udagawa, Noguchi-II, Jeong, and Kim. In each instance, the combination involves modifying a distinct aspect of Noguchi-I, and these modifications are independent of one another. For example, Udagawa teaches modifying the shape of the gate electrode to a serpentine shape, Noguchi-II teaches modifying the 6T1C circuit by incorporating a seventh TFT, Jeong teaches setting the initialization voltage (VINT) of the pixel to the same voltage source as a power supply that supplies a low potential pixel power from the outside (ELVSS), and Kim teaches modifying the extent of the semiconductor layer. In my opinion, a POSITA would recognize that there is no interference among the modifications, and each combination can be implemented without affecting the others. Accordingly, in my opinion, a POSITA would have found it obvious and would have been motivated to combine Noguchi-I with each of Udagawa, Noguchi-II, Jeong, and Kim, and would have had a reasonable expectation of success.

440. Additional details regarding the Noguchi-I−Udagawa−Noguchi-II−Jeong−Kim combination are provided below in connection with specific claim limitations.

2. Claim 14

a. 14[pre] An organic light emitting diode display according to claim 11, further comprising a seventh thin film transistor implemented in the sixth portion of the semiconductor layer,

b. 14[a] wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

c. 14[b] wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

441. In my opinion, Noguchi-I in combination with Udagawa, Noguchi-II, Jeong, and Kim teaches or suggests claim 14. Claim 14 is substantially similar to claim 7, except that it recites "the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor."

442. As explained in 1[h-1] and 1[l], each of transistors T1 to T6 utilizes and includes a portion of the semiconductor layer, which is thus electrically coupled to the corresponding transistor. Noguchi-I, ¶11; §§VIII.F.3.f, VIII.F.3.i. Moreover, as I have explained in Ground 2B, a POSITA would have been motivated to utilize Kim's contiguous semiconductor layer for each of the TFTs in the drive circuit. §VIII.G.

443. In my opinion, a POSITA would have thus understood that when adding an additional TFT, the semiconductor layer would be deposited for that new

TFT because it would have used the design disclosed in the Noguchi-I combination with Kim, and that it would have been obvious to continue the semiconductor layer to incorporate T7. Using a contiguous semiconductor layer would have been a natural choice and given the Noguchi-I combination's layer was contiguous. Moreover, it was one of two options (contiguous or non-contiguous).

444. Here, I note that many possible layouts could have been realized based on Noguchi-II's teachings. Accordingly, Noguchi-I in combination with Noguchi-II teaches or suggests the semiconductor layer extended contiguously from T6 ("fourth" TFT) to a seventh TFT. This is particularly so because both the seventh TFT and T6 connect to the OLED and using the same connection point would eliminate the need for connecting the TFTs using other layers of the design.

445. For the additional reasons explained for claim 7, the remaining limitations of claim 14 are disclosed by Noguchi-I in combination with Udagawa, Noguchi-II, Jeong, and Kim. §VIII.H.4.

3. Claim 27

a. 27[pre] An organic light emitting diode display according to claim 24, further comprising a seventh thin film transistor implemented in the sixth portion of the semiconductor layer,

b. 27[a] wherein the semiconductor layer couples the seventh thin film transistor to the fourth thin film transistor, and

c. 27[b] wherein the seventh thin film transistor is electrically coupled to one of the plurality of second voltage lines and to the respective organic light emitting diode through the semiconductor layer.

446. Noguchi-I in combination with Udagawa, Noguchi-II, Jeong, and Kim disclose claim 27 for the same reasons as explained above for claim 14. §VIII.I.2.

IX. CONCLUSION

447. Based on the foregoing analysis, it is my opinion that the challenged claims of the ’991 patent are invalid.

This declaration and my opinions herein are made to the best of my knowledge and understanding, and based on the material available to me, at the time of signing this declaration. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United States Code.

Date: August 31, 2025



Jerzy Kanicki