



APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/838,138	10/08/2019	10439015	148454/411598-03044	4358

23363 7590 09/18/2019

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Yangwan Kim, Yongin-si, KOREA, REPUBLIC OF;
Samsung Display Co., Ltd., Yongin-si, KOREA, REPUBLIC OF;
Wonkyu Kwak, Yongin-si, KOREA, REPUBLIC OF;
Jaedu Noh, Yongin-si, KOREA, REPUBLIC OF;
Jaeyong Lee, Yongin-si, KOREA, REPUBLIC OF;

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

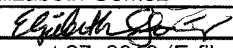
CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23363 7590 05/28/2019
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Elizabeth Gomez	(Typed or printed name)
	(Signature)
August 27, 2019 (E-filed)	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/838,138	12/11/2017	Yangwan Kim	148454/411598-03044	4358

TITLE OF INVENTION: DISPLAY APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	08/28/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
COLEMAN, WILLIAM D	2895	257-071000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Lewis Roca Rothgerber
1 Christie LLP

2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Samsung Display Co., Ltd.

Yongin-si, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____ 0

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 03-1728

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

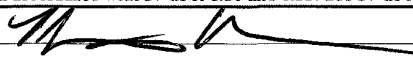
☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature 
Typed or printed name Peter C. Hsueh

Date August 27, 2019
Registration No. 45,574

Electronic Patent Application Fee Transmittal				
Application Number:		15838138		
Filing Date:		11-Dec-2017		
Title of Invention:		DISPLAY APPARATUS		
First Named Inventor/Applicant Name:		Yangwan Kim		
Filer:		Peter C. Hsueh/Elizabeth Gomez		
Attorney Docket Number:		148454/411598-03044		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt

EFS ID:	36988006
Application Number:	15838138
International Application Number:	
Confirmation Number:	4358
Title of Invention:	DISPLAY APPARATUS
First Named Inventor/Applicant Name:	Yangwan Kim
Customer Number:	23363
Filer:	Peter C. Hsueh/Elizabeth Gomez
Filer Authorized By:	Peter C. Hsueh
Attorney Docket Number:	148454/411598-03044
Receipt Date:	27-AUG-2019
Filing Date:	11-DEC-2017
Time Stamp:	12:11:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$1000
RAM confirmation Number	E20198QC11434870
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	148454_IssueFeeTransmittal. PDF	136234	no	1
			fb1a0365cf3777722e04c5e63e31cbc299d17c20		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30178	no	2
			fc12f88569b1b543d9c4883702c3b791d9dfc585		
Warnings:					
Information:					
Total Files Size (in bytes):			166412		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/838,138	12/11/2017	Yangwan Kim	148454/411598-03044	4358
23363	7590	08/13/2019		
Lewis Roca Rothgerber Christie LLP			EXAMINER	
PO BOX 29001			COLEMAN, WILLIAM D	
Glendale, CA 91209-9001				
			ART UNIT	PAPER NUMBER
			2895	
			NOTIFICATION DATE	DELIVERY MODE
			08/13/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pair_cph@firsttofile.com

pto@lrrc.com

Corrected Notice of Allowability	Application No. 15/838,138	Applicant(s) Kim et al.	
	Examiner WILLIAM D COLEMAN	Art Unit 2895	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--
 All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 07/16/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2-34. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☒ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 14/660,813.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>07/16/2019</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	---

/William Coleman/ Primary Examiner, Art Unit 2895	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Attorney Docket Number	148454
	Application Number	15/838,138
	Filing Date	December 11, 2017
	Inventor(s)	Yangwan Kim, et al.
	Group Art Unit	2895
	Examiner Name	COLEMAN, WILLIAM D

U.S. PATENT DOCUMENTS				
EXAMINER INITIALS	Cite No. ¹	DOCUMENT NUMBER Number - Kind Code ² (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
/WDC/		7,053,410 B2	05-30-2006	Kurashina et al.
/WDC/		10,032,953 B2	07-24-2018	Jeon et al.

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
/WDC/		CN 1459656 A	12-03-2003	YODA PHOTOELECTRIC CO LTD	Abstract
/WDC/		CN 1503041 A	06-09-2004	Kurashina et al.	Corresponds to U.S. Patent No. 7,053,410 B2, listed above
/WDC/		CN 103681751 A	03-26-2014	Jeon et al.	Corresponds to U.S. Patent No. 10,032,953 B2, listed above

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

YAG 108704447.1-*07/16/2019 1:26 PM

EXAMINER SIGNATURE	/William Coleman/	DATE CONSIDERED	08/08/2019
<small>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English Language Translation is attached.</small>			

JEJ/yav

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Attorney Docket Number	148454
	Application Number	15/838,138
	Filing Date	December 11, 2017
	Inventor(s)	Yangwan Kim, et al.
	Group Art Unit	2895
	Examiner Name	COLEMAN, WILLIAM D

U.S. PATENT DOCUMENTS				
EXAMINER INITIALS	Cite No. ¹	DOCUMENT NUMBER Number - Kind Code ² (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		7,053,410 B2	05-30-2006	Kurashina et al.
		10,032,953 B2	07-24-2018	Jeon et al.

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
		CN 1459656 A	12-03-2003	YODA PHOTOELECTRIC CO LTD	Abstract
		CN 1503041 A	06-09-2004	Kurashina et al.	Corresponds to U.S. Patent No. 7,053,410 B2, listed above
		CN 103681751 A	03-26-2014	Jeon et al.	Corresponds to U.S. Patent No. 10,032,953 B2, listed above

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

YAG 108704447.1-*07/16/2019 1:26 PM

EXAMINER SIGNATURE		DATE CONSIDERED	
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English Language Translation is attached.

JEJ/yav

Sheet 1 of 1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on July 16, 2019 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.


Yariira Vanegas

Inventor(s) : Yangwan Kim, et al.
Application No. : 15/838,138
Filed : December 11, 2017
Title : DISPLAY APPARATUS

Confirmation No. 4358

Grp./Div. : 2895
Examiner : COLEMAN, WILLIAM D

Docket No. : 148454

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT WITH FEE
UNDER 37 CFR §§ 1.97(d) AND 1.17(p)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
July 16, 2019

Commissioner:

In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, and in accordance with the provisions in the Manual of Patent Examining Procedure §§ 609 and 707.05(b), enclosed is an information disclosure statement listing the references that are known to applicant. Copies of each of the listed Foreign Patent Documents and Other Documents references are enclosed.

It is respectfully requested that the listed references be considered in the examination of this application and identified on the list of references cited on the patent issuing for this application. Applicant also requests that an initialed copy of the information disclosure statement be entered in the application file and returned to applicant with the next communication from the Office in accordance with MPEP § 609.

Applicant's undersigned attorney hereby certifies, in accordance with 37 CFR § 1.97(e)(1), that each item of information contained in the information disclosure

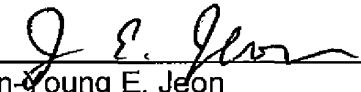
Application No. 15/838,138

statement was first cited in a communication from any foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

The processing fee of \$240.00 as required by 37 CFR § 1.17(p) is submitted herewith. The Commissioner is hereby authorized to charge any fees which may be required by this paper to Deposit Account No. 03-1728. Please show our docket number with any Deposit Account transaction.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By 
Jun-Young E. Jeon
Reg. No. 43,693
626/795-9900

JEJ/yav

Enclosures: Information Disclosure Statement, w/references

YAG 108703757.1-07/16/2019 1:25 PM



Bibliographic data: CN1459656 (A) — 2003-12-03

Active type organic electroluminous display and its making method

Inventor(s): LI XINHONG [CN]; SONG ZHIFENG [CN] ± (XINHONG LI, ; ZHIFENG SONG, ; XINHONG, SONG LI)

Applicant(s): YODA PHOTOELECTRIC CO LTD [CN] ± (YODA PHOTOELECTRIC CO., LTD)

Classification: - international: *G02F1/136; G02F1/15; H01L27/32;*
(IPC1-7): G02F1/136; G02F1/15

- cooperative:

Application number: CN2002120294 20020522

Priority number (s): CN2002120294 20020522

Also published as: CN1277148 (C)

Abstract of CN1459656 (A)

An active organic electroluminescent display is disclosed. Its each pixel region has at least two non-crystal silicon TFT elements whose channel is formed by one non-crystal silicon layer, a display region formed by an electrically conducting transparent layer, and a light mask layer to cover the region outside the display region for electric isolation and protection purposes.



[12] 发明专利申请公开说明书

[21] 申请号 02120294. X

[43] 公开日 2003 年 12 月 3 日

[11] 公开号 CN 1459656A

[22] 申请日 2002.5.22 [21] 申请号 02120294. X

[71] 申请人 友达光电股份有限公司

地址 台湾省新竹市

[72] 发明人 李信宏 宋志峰

[74] 专利代理机构 北京市柳沈律师事务所

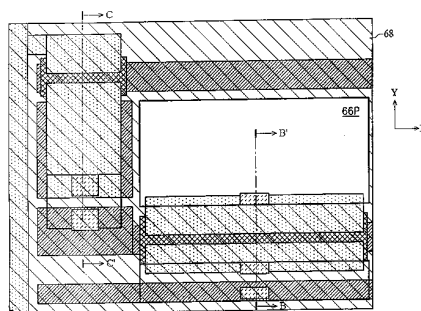
代理人 李晓舒 魏晓刚

权利要求书 3 页 说明书 7 页 附图 16 页

[54] 发明名称 主动式有机电致发光显示器及其制备方法

[57] 摘要

本发明提供一种主动式有机电致发光显示器。每一像素区域中包括有：至少两个非晶硅 TFT 元件，且非晶硅 TFT 元件的沟道由一非晶硅层所构成；一显示区域，由一透明导电层所构成；以及一光遮蔽层，覆盖于显示区域以外的区域上，其可电隔离像素区域以外的寄生有机电致发光显示器，并可屏蔽非晶硅层以防止被后续表面处理工艺损伤。



I S S N 1 0 0 8 - 4 2 7 4

1. 一种主动式有机电致发光显示器，其包含有多个阵列的像素区域，其中每一像素区域中包括有：
- 5 至少两个非晶硅 TFT 元件，该非晶硅 TFT 元件的沟道由一非晶硅层所构成；
- 一显示区域，由一透明导电层所构成；以及
- 一光遮蔽层，至少覆盖非晶硅 TFT 元件的该非晶硅层且暴露该显示区域。
- 10 2. 如权利要求 1 所述的主动式有机电致发光显示器，其中该光遮蔽层由不透明且绝缘的材料所构成。
3. 如权利要求 2 所述的主动式有机电致发光显示器，其中该光遮蔽层由 CrO_x 的单层结构、聚亚酰胺/碳黑的双层结构或是 SiO_x/Cr 的双层结构所构成。
- 15 4. 如权利要求 1 所述的主动式有机电致发光显示器，其中该光遮蔽层覆盖该显示区域以外的区域。
5. 如权利要求 1 所述的主动式有机电致发光显示器，其中该光遮蔽层覆盖该显示区域以外的该透明导电层，用以隔离一寄生有机电致发光显示器的区域。
- 20 6. 如权利要求 1 所述的主动式有机电致发光显示器，其中该透明导电层由 ITO 材料所构成。
7. 如权利要求 1 所述的主动式有机电致发光显示器，其中每一像素区域由垂直相交的一数据线以及一源极线定义而成，且每一像素区域内包含有至少一个电容器。
- 25 8. 如权利要求 1 所述的主动式有机电致发光显示器，其中每一像素区域表面上另覆盖有一有机发光材料层以及一阴极金属层。
9. 一种主动式有机电致发光显示器的制作方法，其包含有下列步骤：
- 提供一透明基底；
- 于该透明基底上形成一第一金属层，并将该第一金属层定义形成两个

沿 X 方向延伸的第一、第二扫描线以及一电容器下电极的图形，其中该电容器的下电极位于该第一、第二扫描线之间；

于该透明基底的整个表面上形成一第一绝缘层；

于该第一扫描线的一预定 TFT 元件区域上定义形成一岛状结构，其中
5 该岛状结构由一第二绝缘层以及一非晶硅层依序构成；

于该岛状结构的顶部形成一蚀刻终止层，以覆盖该预定 TFT 元件区域的栅极；

于该岛状结构的表面上依序形成一掺杂非晶硅层以及一第二金属层；

将该第二金属层定义形成一沿 Y 方向延伸的数据线图案以及一电容器
10 的上电极，并于该岛状结构的顶部形成一开口，以使该预定 TFT 元件区域的该第二金属层隔离成一线/漏极电极层，并使该预定 TFT 元件区域的该掺杂非晶硅层隔离成一线/漏极扩散区；

于该透明基底的整个表面上形成一保护层，并于该保护层中形成一第一通孔以及一第二通孔，其中该第一通孔暴露该第二扫描线之一端，该第二通孔暴露该电容器的上电极之一端；
15

于该透明基底的整个表面上形成一透明导电层，并将该透明导电层定义形成一显示区域的图形，同时使该透明导电层覆盖该第一通孔以及该第二通孔的暴露区域；以及

于该透明基底的整个表面上形成一光遮蔽层，其中该光遮蔽层至少覆盖该预定 TFT 元件区域的该非晶硅层，且该光遮蔽层暴露该显示区域。
20

10. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，另包含有下列步骤：

进行表面清洗工艺；

于该透明基底的整个表面上沉积一有机发光材料层；以及

25 于该有机发光材料层的整个表面上沉积一阴极金属层。

11. 如权利要求 10 所述的主动式有机电致发光显示器的制作方法，其中该表面清洗工艺为紫外线臭氧(UV/O₃)或 O₂ 等离子体表面清洗工艺。

12. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，其中该光遮蔽层由不透明且绝缘的材料所构成。

30 13. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，其

中该光遮蔽层由 CrO_x 的单层结构、聚亚酰胺/碳黑的双层结构或是 SiO_x/Cr 的双层结构所构成。

14. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，其中该光遮蔽层屏蔽该非晶硅 TFT 元件的非晶硅层。

5 15. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，其中该光遮蔽层覆盖该显示区域以外的该透明导电层，用以隔离一寄生有机电致发光显示器的区域。

16. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，其中该透明导电层由 ITO 材料所构成。

10 17. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，其中该显示区域的图案位于该第一、第二扫描线以及该数据线之间。

18. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，其中该透明导电层覆盖该第一通孔以及该第二通孔的暴露区域，可使该第二扫描线与该电容上电极之间产生电连接。

15 19. 如权利要求 9 所述的主动式有机电致发光显示器的制作方法，其中该第一扫描线上制作该预定 TFT 元件的同时，也在该第二扫描线上制作另一预定 TFT 元件。

主动式有机电致发光显示器及其制作方法

5

技术领域

本发明涉及一种以非晶硅薄膜晶体管(a-Si:H TFT)为驱动元件的主动式有机电致发光显示器(AM-OLED)，特别涉及一种具有光遮蔽结构的 AM-OLED，可电隔离像素区域以外的寄生 OLED，并可屏蔽非晶硅层以防止被

10 后续的表面处理工艺损伤。

背景技术

有机电致发光显示器(Organic Electroluminescence Device; Organic Light

15 Emitting Diode，以下简称 OLED)，依照其驱动方式可区分成主动式(active matrix)与被动式两种，其中主动式有机电致发光显示器(以下简称 AM-OLED)以电流驱动，每一个像素至少要有一开关薄膜晶体管(switch TFT)，作为图像数据进入储存开关及寻址之用；另外需要一个驱动薄膜晶体管(driving TFT)，根据电容储存电压的不同来调节驱动电流的大小，即控制像素明亮

20 及灰阶的不同。目前的主动式驱动方式有使用两个 TFT 驱动方式及四个 TFT 驱动方式。

一般而言，AM-OLED 的发光原理是在特定的有机薄膜积层施加电流以使电能转换成光能，其具有面发光的厚度薄、质量轻的特征以及自发光的高发光效率、低驱动电压等优点，且具有视角广、高对比、高响应速度、

25 全彩化及可挠曲的特性。至于 TFT 元件的制作上，则是采用液晶显示器的非晶硅(amorphous silicon, a-Si:H)的 TFT 技术。请参阅图 1，其显示现有非晶硅 TFT 的 AM-OLED 的俯视图。以采用两个非晶硅 TFT 的 AM-OLED 为例，其包含有多个阵列的像素区域 10，由沿 Y 方向延伸的数据线 12 以及沿 X 方向延伸的源极线(source line 或称 V_{dd} line) 14 所构成。在每一个像素区域

30 10 中，包含有两条沿 X 方向延伸的扫描线 16、两个非晶硅 TFT 元件 18、

一个由矩形的透明电极所构成的显示区域 20 以及一电容器 22。

请参阅图 2A, 它是沿图 1 的切线 A-A 显示现有的非晶硅 TFT 元件 18 的剖面示意图。以下以蚀刻终止型式(etching stopper type)的制作方法说明现有非晶硅 TFT 元件 18 的工艺。首先, 在一透明基底 30 表面上形成一第一金属层, 再将第一金属层定义形成源极线 14、扫描线 16 以及电容器 22 的下电极的图形。然后, 依序在透明基底 30 的表面上形成一第一绝缘层 32、一第二绝缘层 34 以及一非晶硅(a-Si:H)层 36, 再利用光刻蚀刻技术将部分第二绝缘层 34 以及非晶硅层 36 去除, 以使非晶硅 TFT 元件 18 的预定区域定义形成一岛状结构, 至于源极线 14 上方的第二绝缘层 34 以及非晶硅层 36 则是完全去除。接着, 在岛状结构的预定栅极区域上方定义形成一蚀刻终止层 38。随后, 依序在透明基底 30 的整个表面上形成一掺杂非晶硅层 40 以及一第二金属层 42, 再利用光刻蚀刻技术将部分掺杂非晶硅层 40 以及第二金属层 42 去除, 将第二金属层 42 定义形成数据线 12 以及电容器 22 的上电极的图形, 并同时保持掺杂非晶硅层 40 以及第二金属层 42 保留在岛状结构的表面上, 至于源极线 14 上方的掺杂非晶硅层 40 以及第二金属层 42 则是完全去除。跟着, 利用光刻蚀刻工艺, 于岛状结构的预定栅极区域上方定义形成一开口, 则可使第二金属层 42 区分成为一源极/漏极电极(42A 或 42B), 可使掺杂非晶硅层 40 区分成为一源极/漏极扩散区(40A 或 40B), 至于非晶硅层 36 是用来作为一沟道。

接下来, 于透明基底 30 的整个表面上形成一保护层 44, 再利用光刻蚀刻工艺在保护层 44 内至少形成一第一通孔 45I、一第二通孔 45II 以及一第三通孔 45III, 其中第一通孔 45I 以及第二通孔 45II 使得分别暴露出源极/漏极电极(42A 或 42B)附近的第二金属层 42, 而第三通孔 45III 则穿过第一绝缘层 32 以暴露出源极线 14 的部分区域。其后, 于透明基底 30 的表面上定义形成一具有透明导电效果的氧化铟锡(ITO)层 46 的图形, 以构成矩形显示区域 20, 并覆盖住第一通孔 45I、第二通孔 45II 以及第三通孔 45III 的暴露区域, 以提供电连接效果。

请参阅图 2B, 它是沿图 1 的切线 A-A 显示现有寄生 OLED 的剖面示意图。当上述非晶硅 TFT 元件 18 完成之后, 在进行蒸镀工艺之前需先进行表面处理程序, 再依序沉积一有机/高分子发光材料层 47 以及一阴极金属层

48, 便大致完成了 AM-OLED 的工艺。然而, 在现有的表面处理技术中, 通常采用紫外线臭氧(UV/O₃)或 O₂ 等离子体的表面清洗工艺, 而表面清洗工艺中的 UV 光会损伤非晶硅层 36, 进而导致阈值电压(threshold voltage)增加或漏电流(leakage current)增加的问题。对于一般的 TFT-LCD 工艺而言, 可以在 UV 清洗工艺之后进行退火处理, 其可修复表面的损伤结构, 以解决上述问题, 但是对于非晶硅 TFT 的 OLED 工艺而言, 碍于后续蒸镀有机/高分子材料层 47 的限制, 无法提供此道退火处理来解决非晶硅层 36 受损的问题。

除此之外, 对于现有的五道掩膜的非晶硅 TFT 工艺而言, ITO 层 46 的图形不只应用于显示区域 20 中, 还必须提供作为第二金属层与第二金属层之间或是第二金属层与第一金属层之间的电连接桥梁, 然而显示区域 20 以外的 ITO 层 46 这却会导致形成一寄生 OLED 区域 49, 此寄生 OLED 区域 49 亦会产生发光现象, 进而造成不必要的电力消耗以及视觉干扰。

发明内容

因此, 本发明的主要目的在于提供一种具有光遮蔽结构的 AM-OLED, 此光遮蔽结构覆盖显示区域以外的面积, 可屏蔽非晶硅层以防止后续电或 UV 光清洗工艺的损伤, 并可隔离寄生电容以确保 AM-OLED 的发光品质。

本发明则提供一种主动式有机电致发光显示器, 每一像素区域中包括有: 至少两个非晶硅 TFT 元件, 且非晶硅 TFT 元件的沟道由一非晶硅层所构成; 一显示区域, 由一透明导电层所构成; 以及一光遮蔽层, 覆盖于显示区域以外的区域上, 其可电隔离像素区域以外的寄生 OLED, 并可屏蔽非晶硅层以防止被后续表面处理工艺损伤。

根据上述目的, 本发明的一个特征在于提供一光遮蔽结构, 可屏蔽非晶硅层以防止其被后续表面清洗工艺中的 UV 光或等离子体损伤, 进而改善现有阈值电压增加或漏电流增加的问题。

本发明的另一特征在于提供一光遮蔽结构, 可隔离寄生 OLED 区域, 因此可有效避免寄生 OLED 区域产生发光现象, 进而减少不必要的电力消耗以及视觉干扰。

附图说明

图 1 显示现有非晶硅 TFT 的 AM-OLED 的俯视图;

5 图 2A 是沿图 1 的切线 A-A'显示现有非晶硅 TFT 元件的剖面示意图;

图 2B 是沿图 1 的切线 A-A'显示现有寄生 OLED 的剖面示意图;

图 3A 至 3F 是显示本发明非晶硅 TFT 的 AM-OLED 工艺方法的俯视图;

图 4A 至 4G 是沿图 3 的切线 B-B'显示本发明非晶硅 TFT 的 AM-OLED 工艺方法的剖面示意图; 以及

10 图 5A 至 5G 是沿图 3 的切线 C-C'显示本发明非晶硅 TFT 的 AM-OLED 工艺方法的剖面示意图。

附图中的附图标记说明如下:

现有技术:

像素区域~10; 数据线~12; 源极线~14; 扫描线~16; 非晶硅 TFT 元件
15 ~18; 显示区域~20; 电容器~22; 透明基底~30; 第一绝缘层~32; 第二绝缘层~34; 非晶硅层~36; 蚀刻终止层~38; 掺杂非晶硅层~40; 第二金属层~42; 保护层~44; 第一通孔~45I; 第二通孔~45II; 第三通孔~45III; ITO 层~46; 有机/高分子发光材料层~47; 阴极金属层~48; 寄生 OLED 区域~49。

本发明技术:

20 透明基底~50; 第一金属层~52; 源极线~52S; 第一扫描线~52I; 第二扫描线~52II; 电容器之下电极~52C; 第一绝缘层~54; 第二绝缘层~55; 非晶硅层~56; 第一通孔~57I; 蚀刻终止层~58; 掺杂非晶硅层~60; 第二金属层~62; 数据线~62D; 电容器之上电极~62C; 开口~63I、63II; 保护层~64; 第二通孔~57II; 第三通孔~57III; 第四通孔~57IV; 第五通孔~57V; 透明导
25 电层~66; 显示区域~66P; 光遮蔽层~68; 寄生 OLED 区域~69; 有机/高分子发光材料层~70; 阴极金属层~72; 第一非晶硅 TFT 元件~TFT1; 第二非晶硅 TFT 元件~TFT2。

具体实施方式

30

为了让本发明的上述和其它目的、特征、和优点能更明显易懂，下文特举出优选实施例，并配合附图，作详细说明如下：

实施例

本发明提供一种以非晶硅薄膜晶体管(a-Si:H TFT)为驱动元件的主动式有机电致发光显示器(AM-OLED)，其透明导电层上具有一光遮蔽结构，可以电隔离像素区域以外的寄生 OLED，并供以屏蔽后续分 OLED 工艺所产生的损伤。

以采用两个非晶硅 TFT 的 AM-OLED 为例，其包含有多个阵列的像素区域，由沿 Y 方向延伸的数据线以及沿 X 方向延伸的源极线(source line 或称 V_{dd} line)所构成。在每一个像素区域中，包含有两条沿 X 方向延伸的扫描线、两个非晶硅 TFT 元件、一个由矩形透明电极所构成的显示区域以及一电容器。一般的非晶硅 TFT 结构的制作方法，可分为蚀刻终止型(etching stopper type)以及底沟道型(back channel type)的制作方法，以下以蚀刻终止型的制作方法来说明本发明的非晶硅 TFT 的 AM-OLED。

图 3A 至 3F 是显示本发明非晶硅 TFT 的 AM-OLED 工艺方法的俯视图。图 4A 至 4G 是沿图 3 的切线 B-B'显示本发明非晶硅 TFT 的 AM-OLED 工艺方法的剖面示意图。图 5A 至 5G 是沿图 3 的切线 C-C'显示本发明非晶硅 TFT 的 AM-OLED 工艺方法的剖面示意图。

首先，如图 3A、4A 与 5A 所示，在一透明基底 50 表面上形成一第一金属层 52，再将第一金属层定义形成一沿 X 方向延伸的源极线 52S、一沿 X 方向延伸的第一扫描线 52I、一沿 X 方向延伸的第二扫描线 52II 以及一电容器的下电极 52C 的图形。然后，如图 3B、4B 与 5B 所示，依序在透明基底 30 的表面上形成一第一绝缘层 54、一第二绝缘层 55 以及一非晶硅层 56，其中第一绝缘层 54 的材料可选用 SiO_2 、 SiN 、 SiON ，第二绝缘层 55 的材料可选用 SiO_2 、 SiN 、 SiON 。再利用光刻蚀刻技术将部分第二绝缘层 55 以及非晶硅层 56 去除，可分别在第一扫描线 52I 以及第二扫描线 52II 的非晶硅 TFT 元件的预定区域上定义形成一岛状结构，至于源极线 52S 上方的第二绝缘层 55 以及非晶硅层 56 则是完全去除，并穿过第一绝缘层 54 以形成一第一通孔 57I，用以暴露出源极线 52S 的部分区域。接着，于岛状结构的预定栅极区域上方定义形成一蚀刻终止层 58。

如图 3C、4C 与 5C 所示,依序于透明基底 50 的整个表面上形成一掺杂非晶硅层 60 以及一第二金属层 62,其中掺杂非晶硅层 60 可使用 n^+ 掺杂的非晶硅材料。然后,利用光刻蚀刻技术将部分掺杂非晶硅层 60 以及第二金属层 62 去除,则可将第二金属层 62 定义形成一沿 Y 方向延伸的数据线 62D 以及一电容器的上电极 62C 的图形,并同时可将掺杂非晶硅层 60 以及第二金属层 62 保留在岛状结构的表面上,至于源极线 52S 上方的掺杂非晶硅层 60 以及第二金属层 62 则是完全去除。跟着,利用光刻蚀刻工艺,于岛状结构的预定栅极区域上方定义形成一开口 63I 与 63II,则可使第二金属层 62 区分成为一源极/漏极电极(62A 或 62B),可使掺杂非晶硅层 60 区分成为一源极/漏极扩散区(60A 或 60B),至于非晶硅层 56 则用来作为一沟道,如此便大致完成第一非晶硅 TFT 元件(TFT1)以及第二非晶硅 TFT 元件(TFT2)。

如图 3D、4D 与 5D 所示,在透明基底 50 的整个表面上形成一保护层 64,再用光刻蚀刻工艺在保护层 64 内至少形成一第二通孔 57II、一第三通孔 57III、一第四通孔 57IV 以及一第五通孔 57V,并同时暴露出第一通孔 57I。其中,第二通孔 57II 以及第三通孔 57III 分别暴露出第二非晶硅 TFT 元件(TFT2)的源极/漏极电极(62A 或 62B)附近的第二金属层 62,第四通孔 57IV 暴露出第二扫描线 52II 的一端,至于第五通孔 57V 则暴露出电容器的上电极 62C 的一部分区域。

如图 3E、4E 与 5E 所示,在透明基底 50 的表面上定义形成一具有透明导电层 66 的图形,可使用 ITO 材料,以构成矩形显示区域 66P、覆盖住第一通孔 57I、第二通孔 57II、第三通孔 57III、第四通孔 57IV 以及第五通孔 57V 的暴露区域,则第一透明导电层 66I 可以提供电容器的上电极 62C 与第二扫描线 52II 之间的电连接效果,而第二透明导电层 66II 可以提供源极线 52S 与第二扫描线 52II 之间的电连接效果。

如图 3F、4F 与 5F 所示,在透明基底 50 的整个表面上定义形成一光遮蔽层 68,其至少覆盖第一透明导电层 66I 以及第二透明导电层 66II,但需暴露显示区域 66P,则光遮蔽层 68 可屏蔽非晶硅层 56,并同时隔离寄生 OLED 区域 69。为了简化工序,光遮蔽层 68 的图案覆盖显示区域 66P 以外的面积。在优选实施例中,光遮蔽层 68 的材料可选用具有不透光且绝缘的

单层材料(如: CrO_x)或含有高分子树脂的双层结构(如: 聚亚酰胺/碳黑), 或是含有不透光金属的双层结构(如: SiO_x/Cr)。

最后, 如图 4G 与 5G 所示, 在进行蒸镀工艺之前需先进行表面处理程序, 可采用紫外线臭氧(UV/ O_3)或 O_2 等离子体表面清洗工艺, 然后再依序沉

5 积一有机/高分子发光材料层 70 以及一阴极金属层 72, 便大致完成 AM-OLED 的工艺。

与现有技术相比, 本发明在显示区域 66P 以外的表面上覆盖光遮蔽层 68, 可屏蔽非晶硅层 56 以防止其被后续表面清洗工艺中的 UV 光或等离子体损伤, 进而改善现有阈值电压增加或漏电流增加的问题。此外, 光遮蔽层 68 至少覆盖第一透明导电层 66I 以及第二透明导电层 66II, 可隔离寄生 OLED 区域 69, 因此可有效避免寄生 OLED 区域 69 产生发光现象, 进而减少不必要的电力消耗以及视觉干扰。

虽然本发明已以一优选实施例公开如上, 但是它并非用以限定本发明, 本领域技术人员, 在不脱离本发明的精神和范围内, 应当可以作各种更改与润饰, 因此本发明的保护范围由所附权利要求所定义为准。

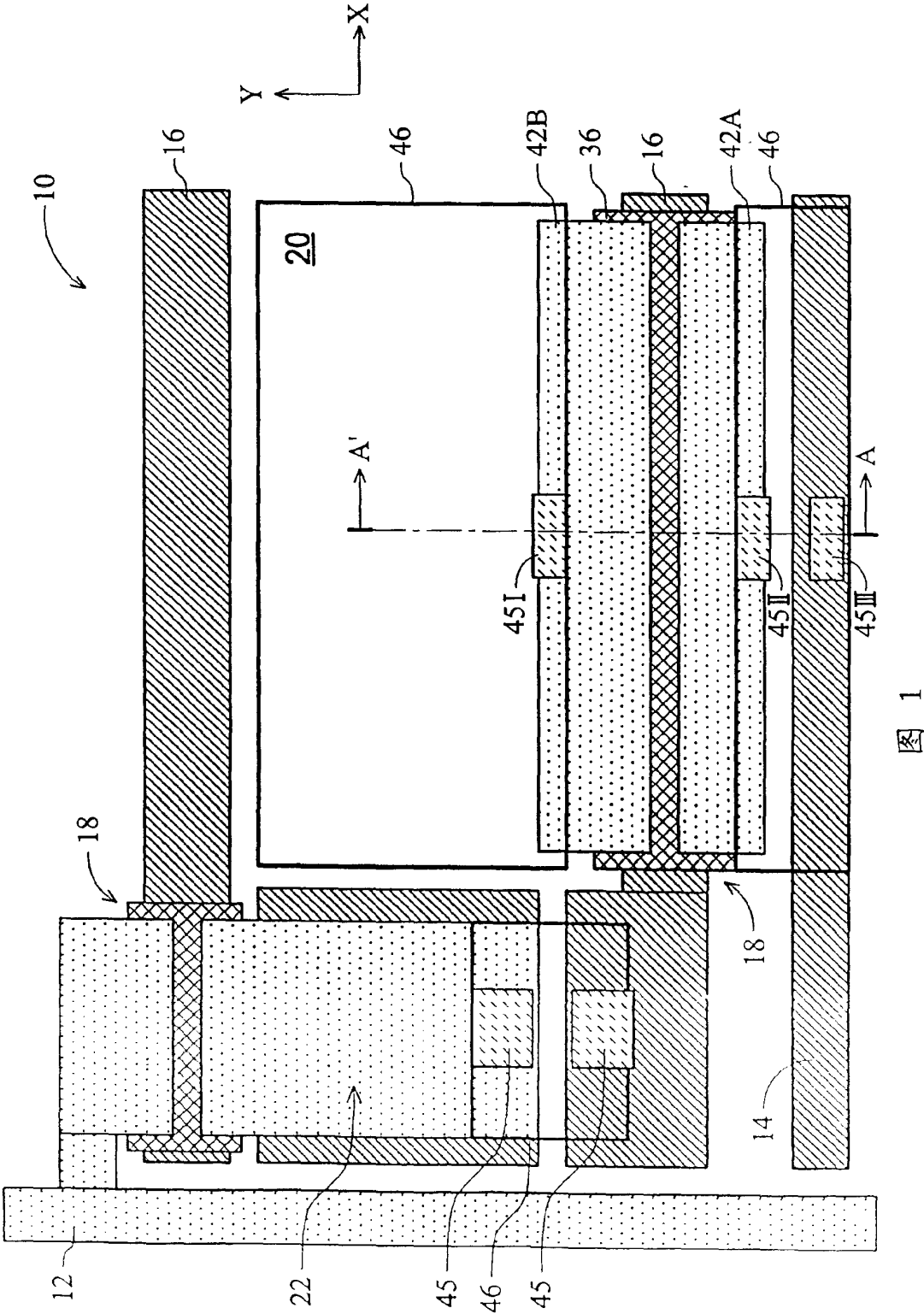


图 1

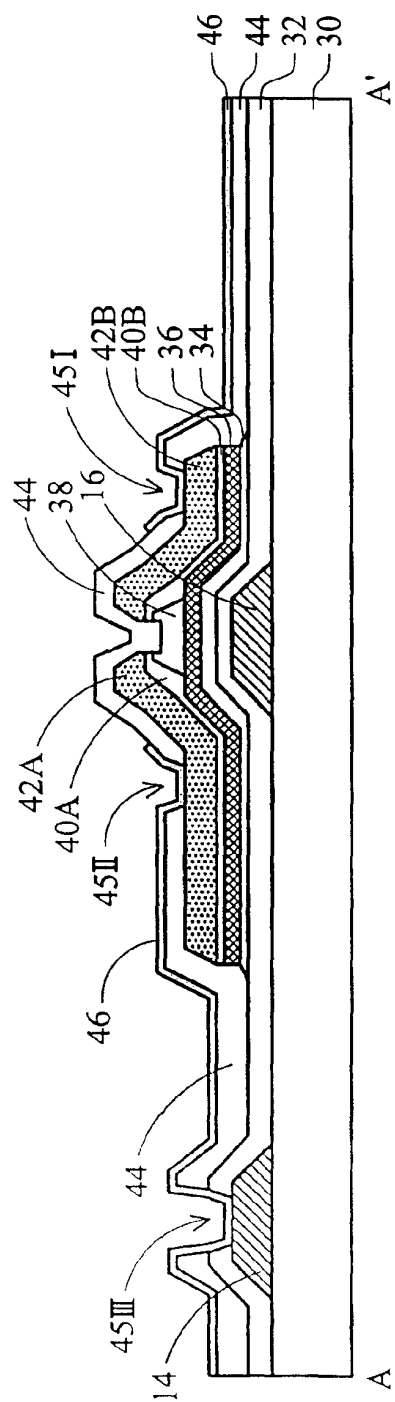


图 2A

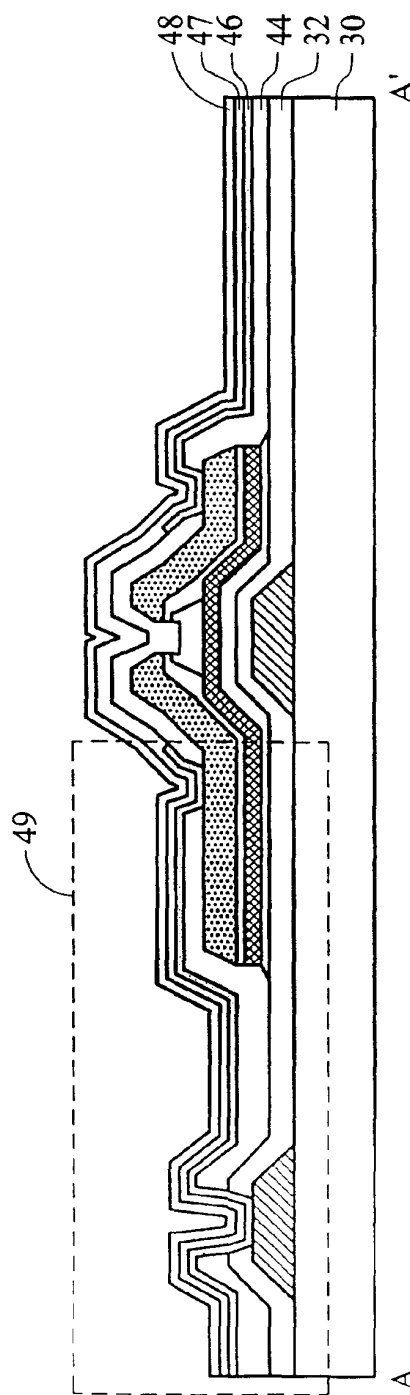


图 2B

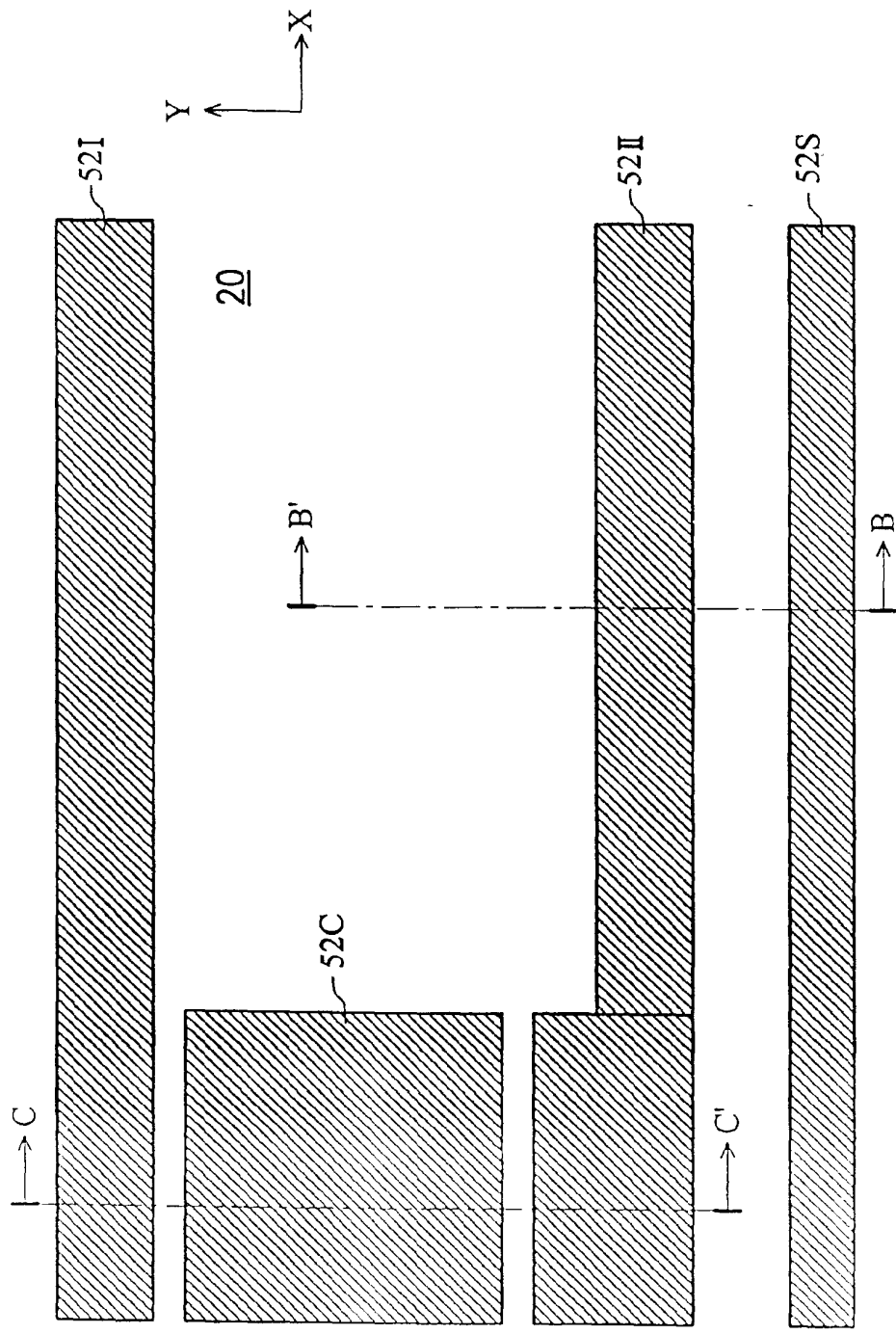


图 3A

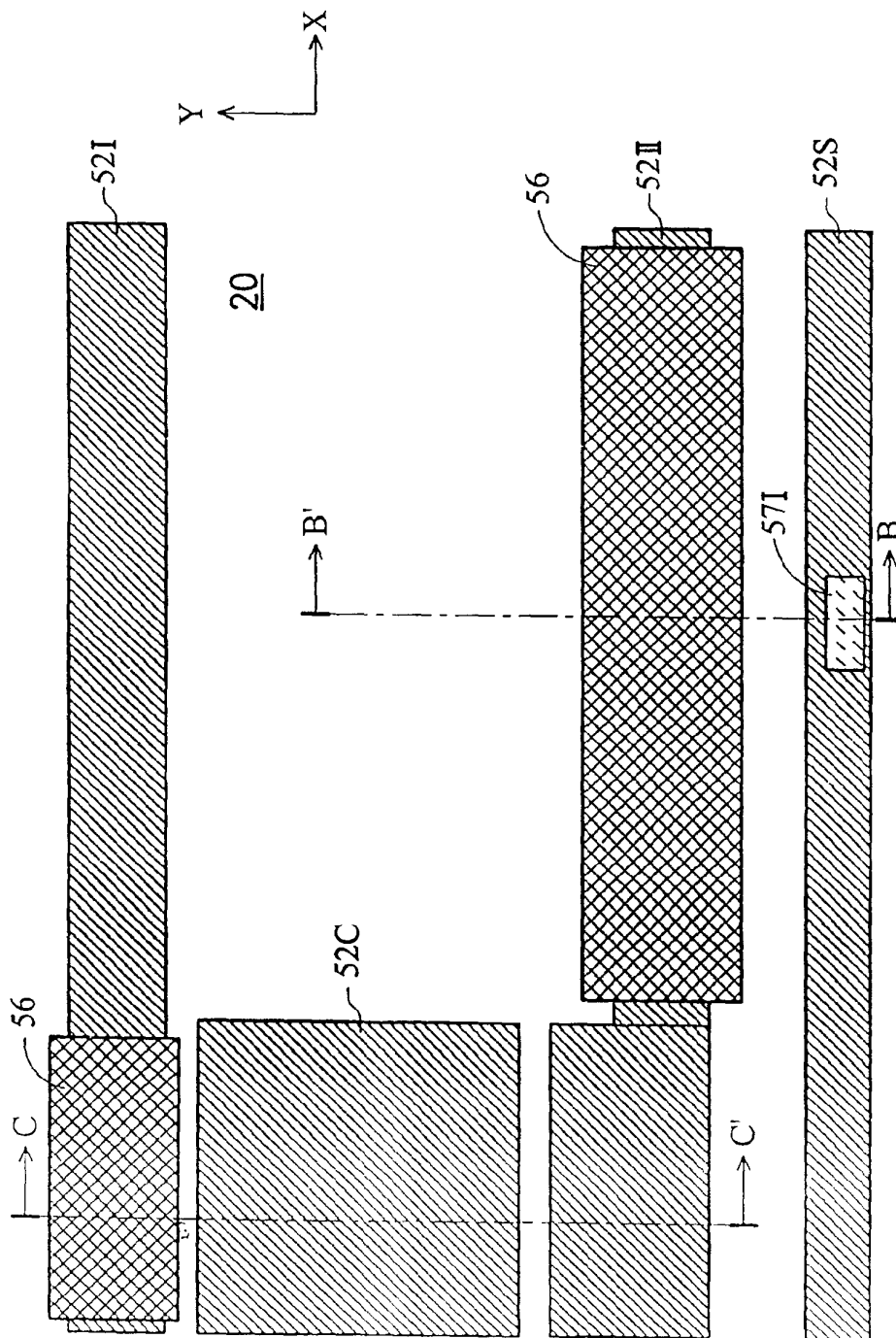
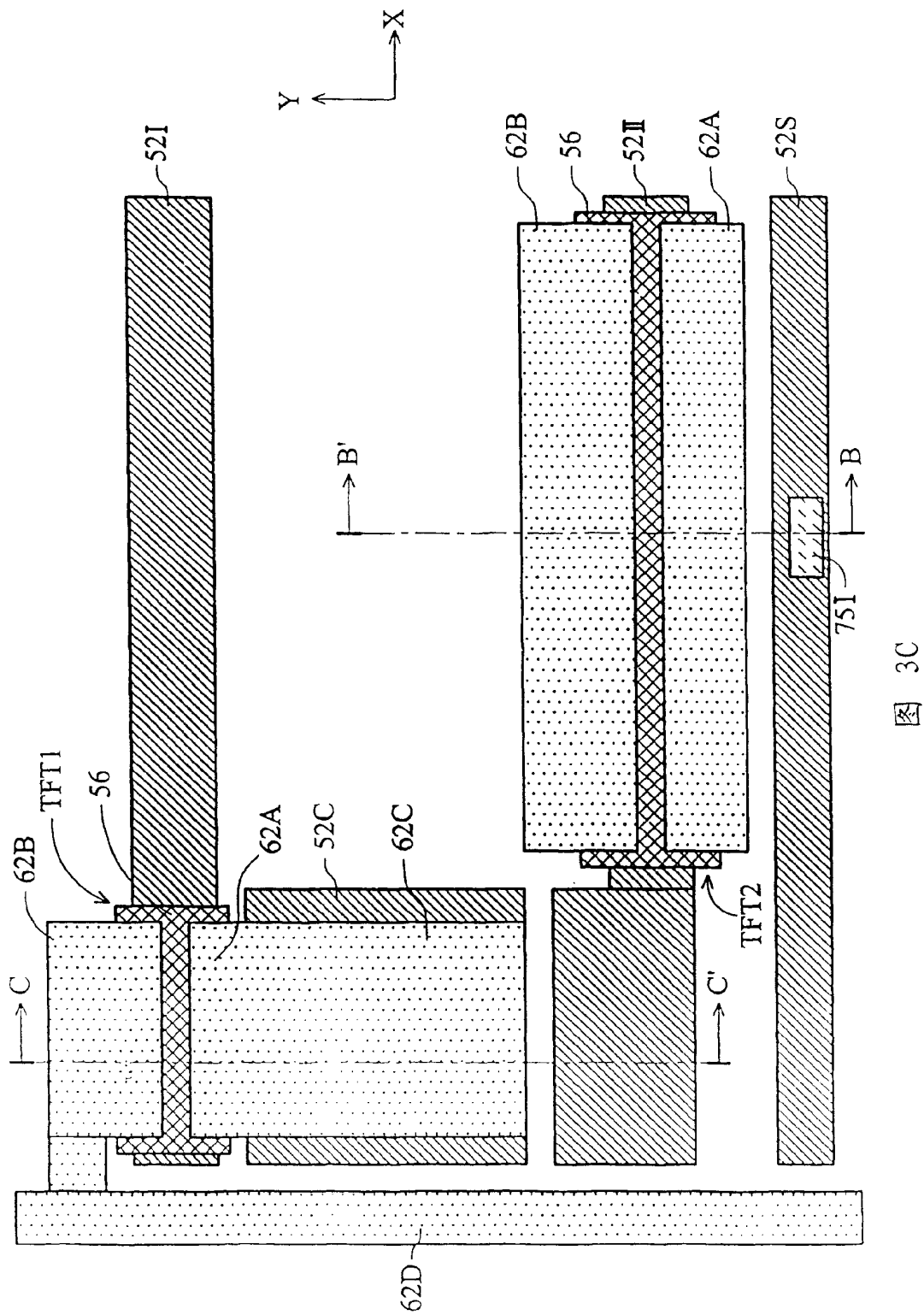
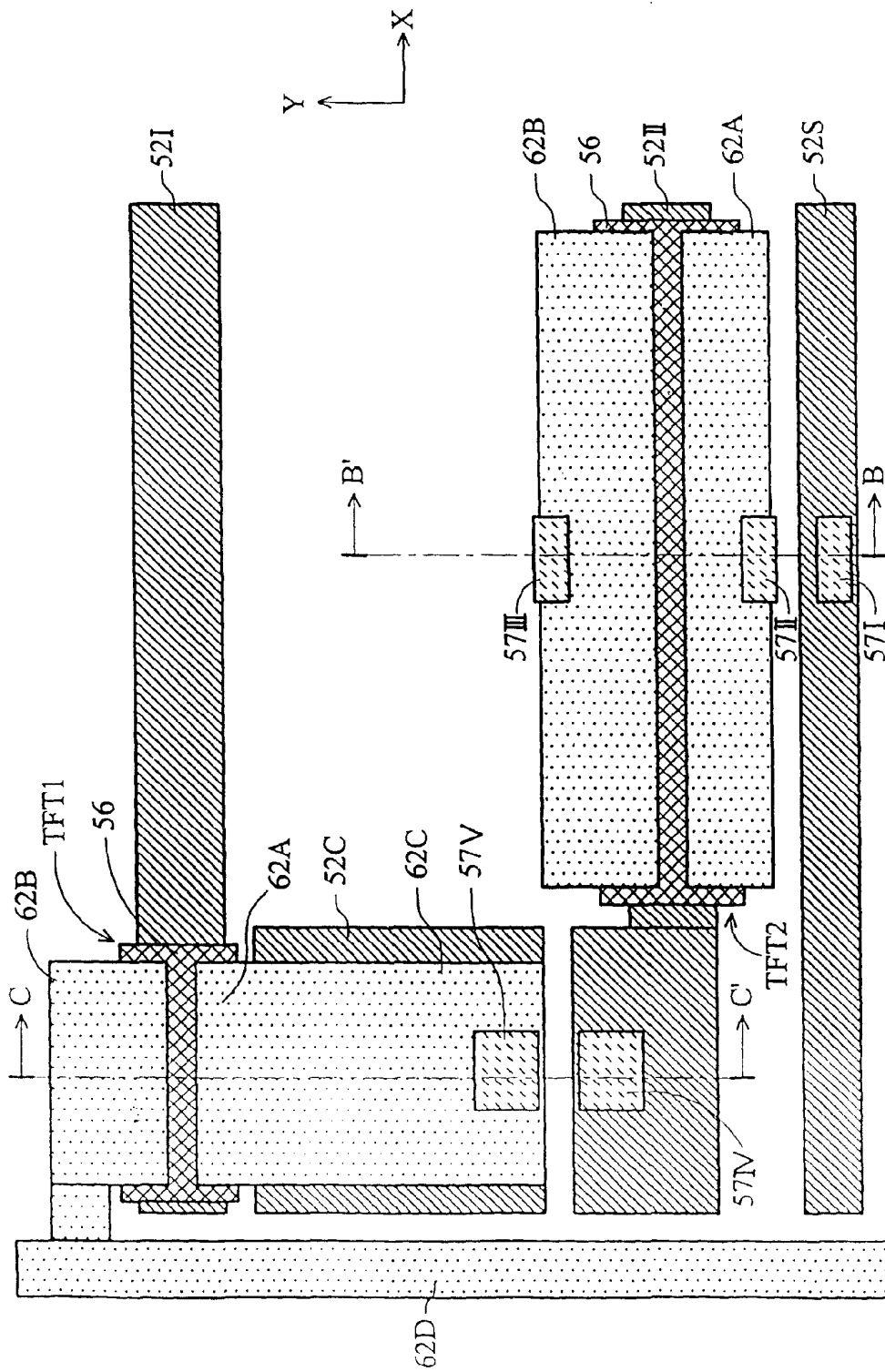


图 3B



3D 

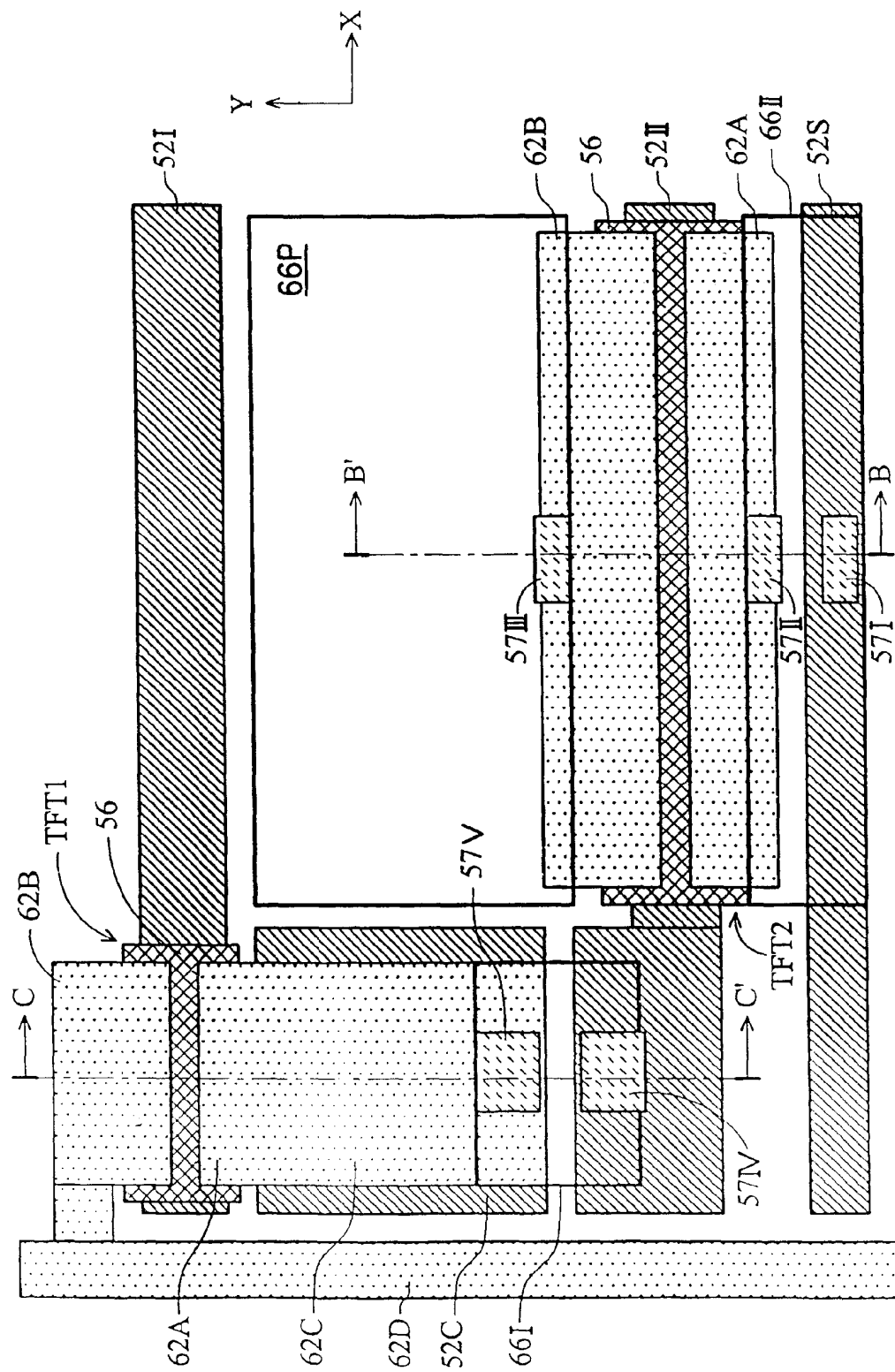


图 3E

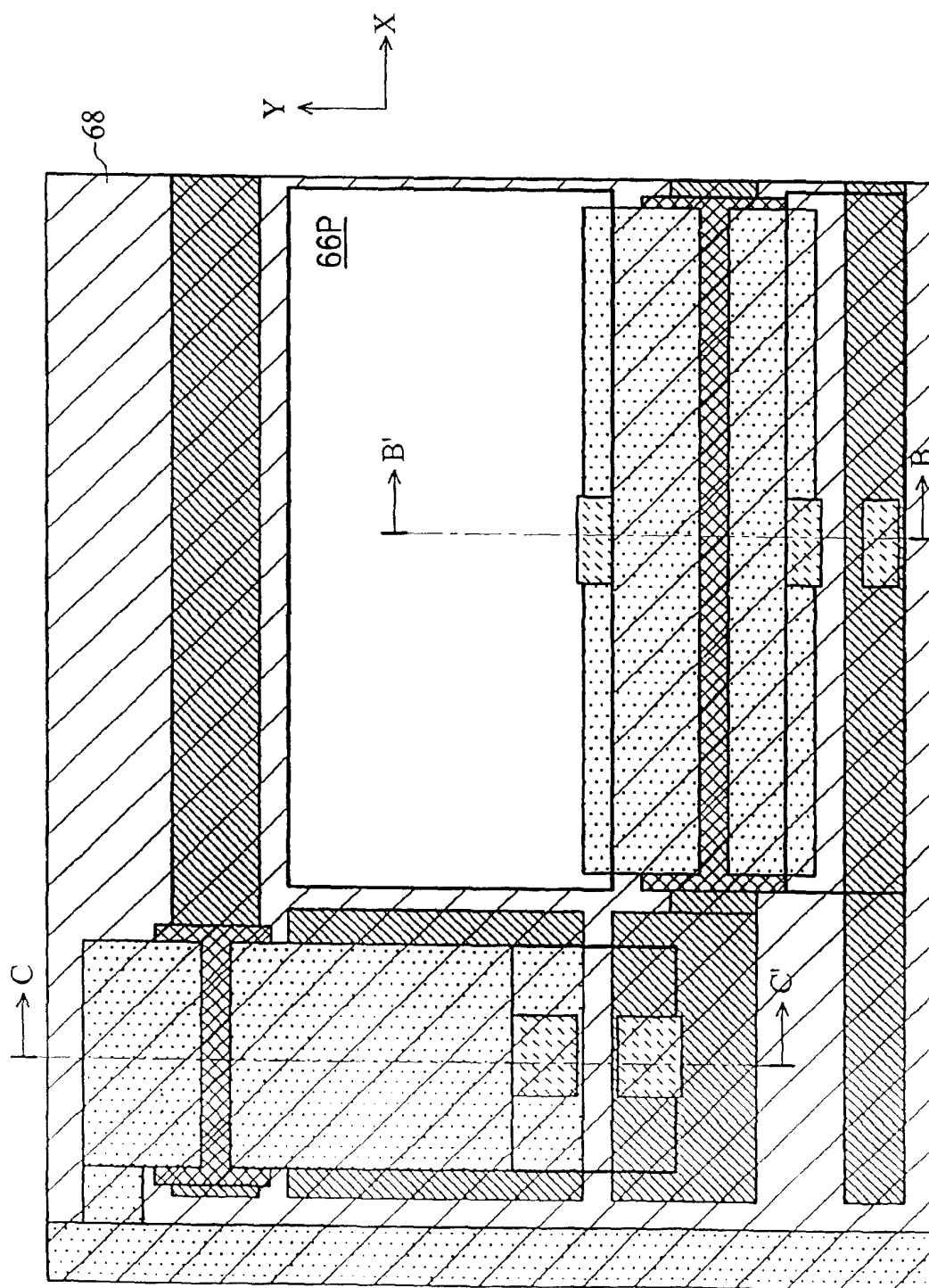


图 3F

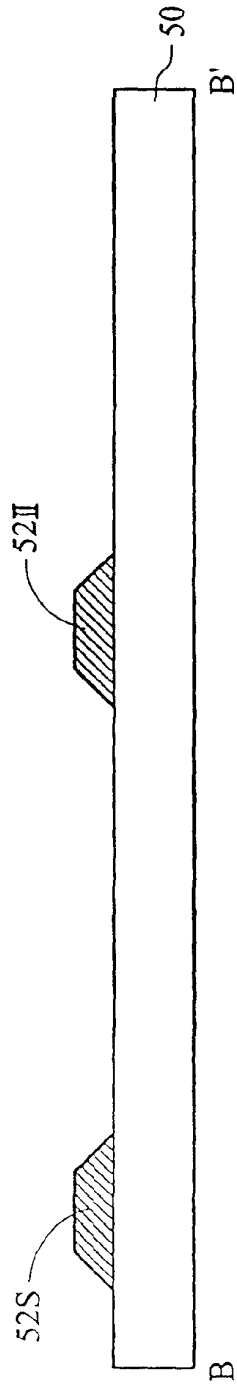


图 4A

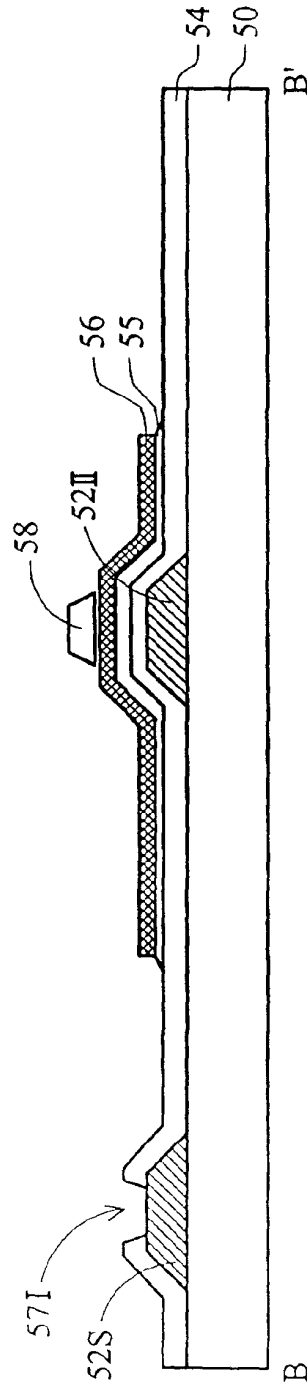
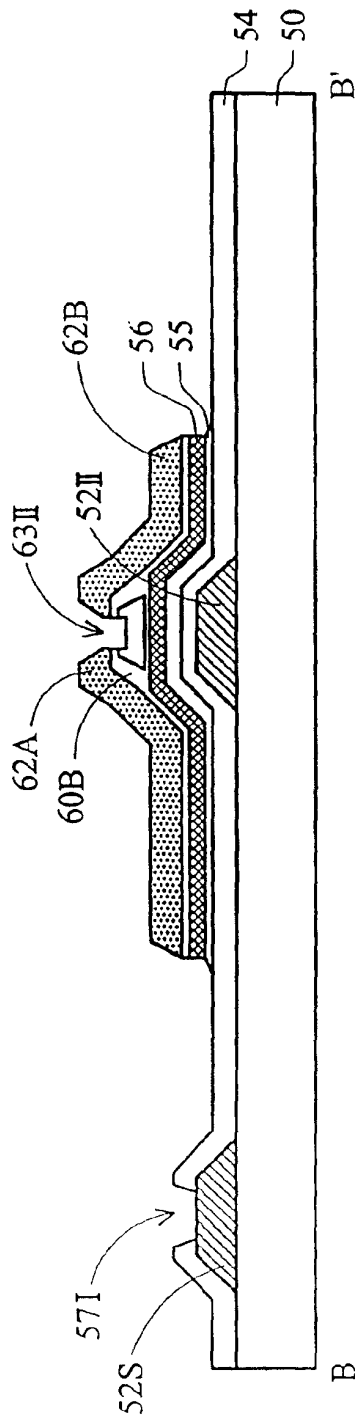
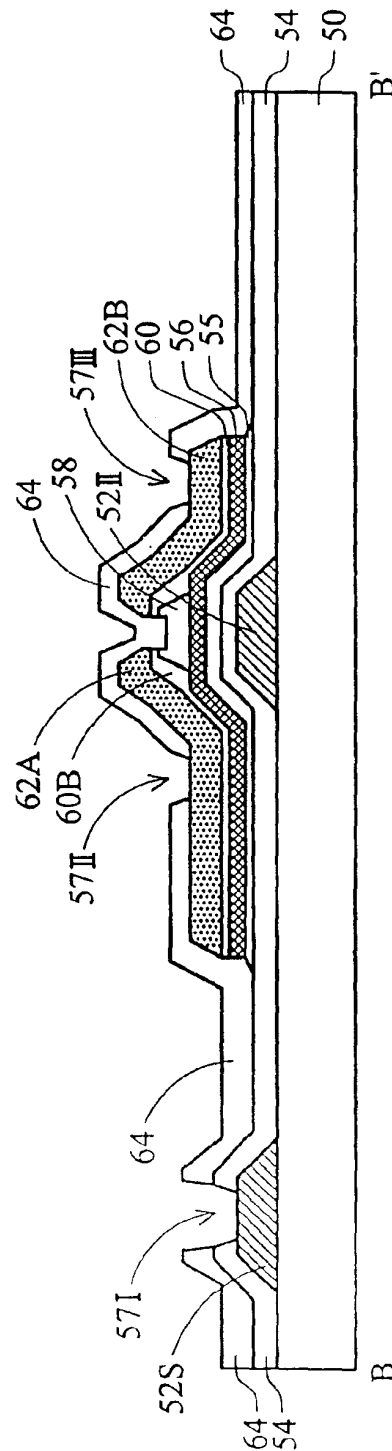


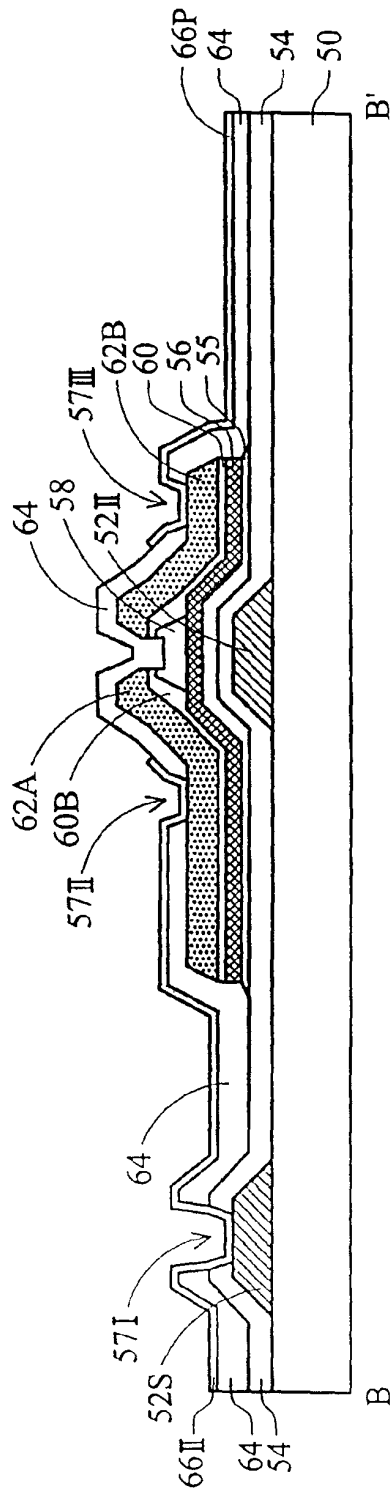
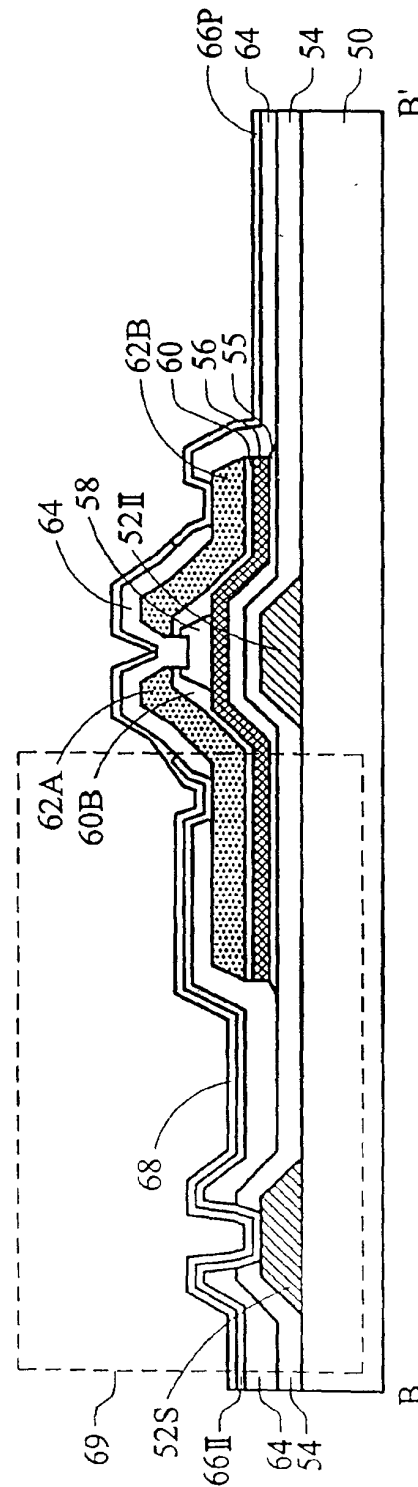
图 4B



4C



4D

4E
4F
图

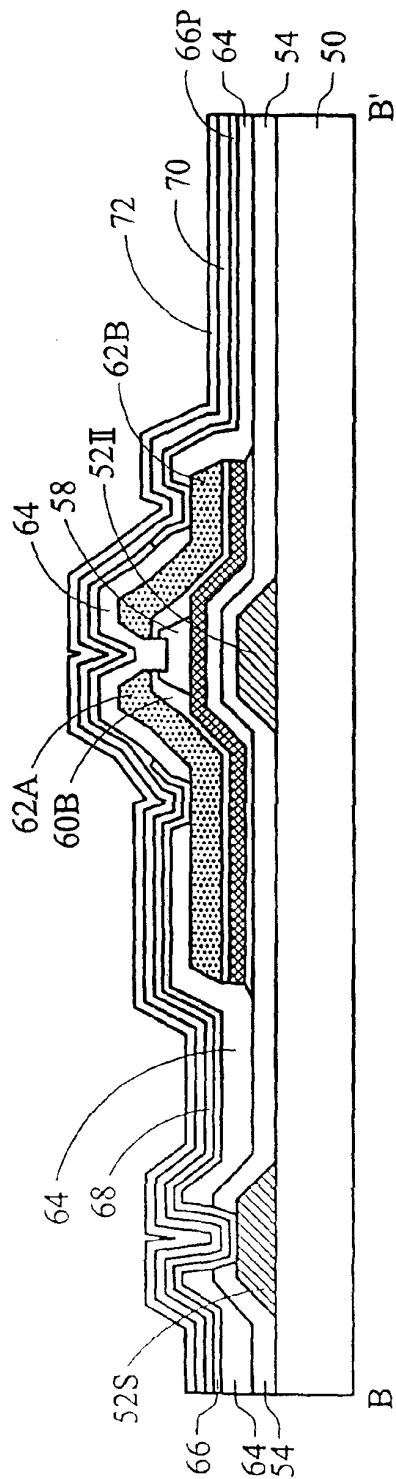


图 4G

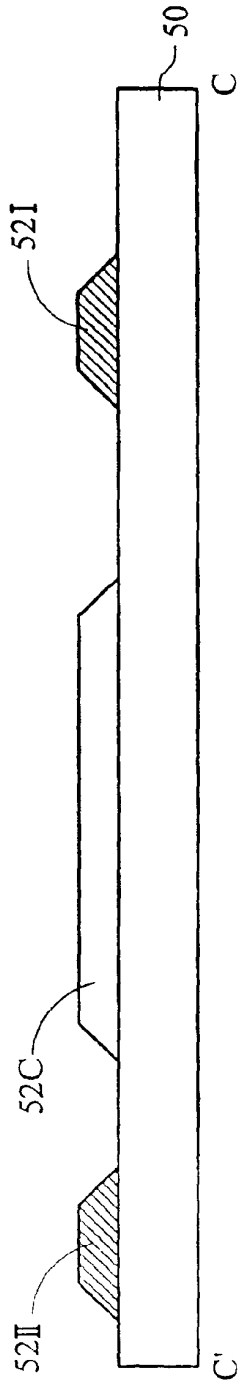


图 5A

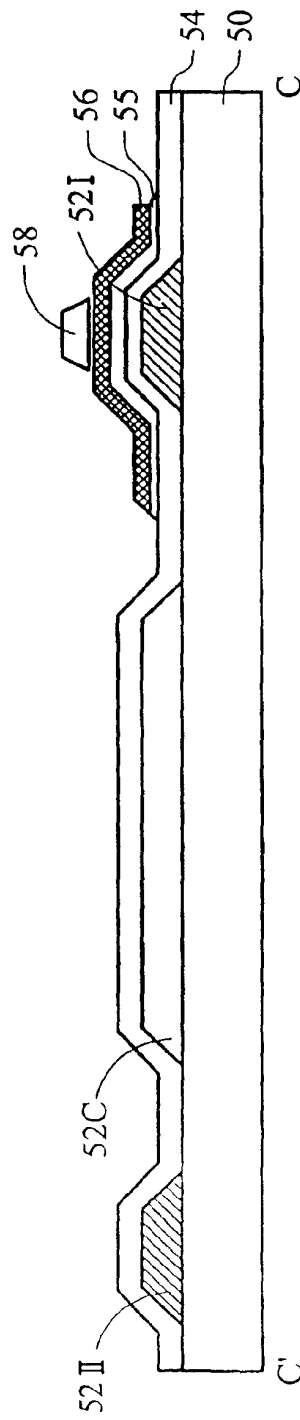
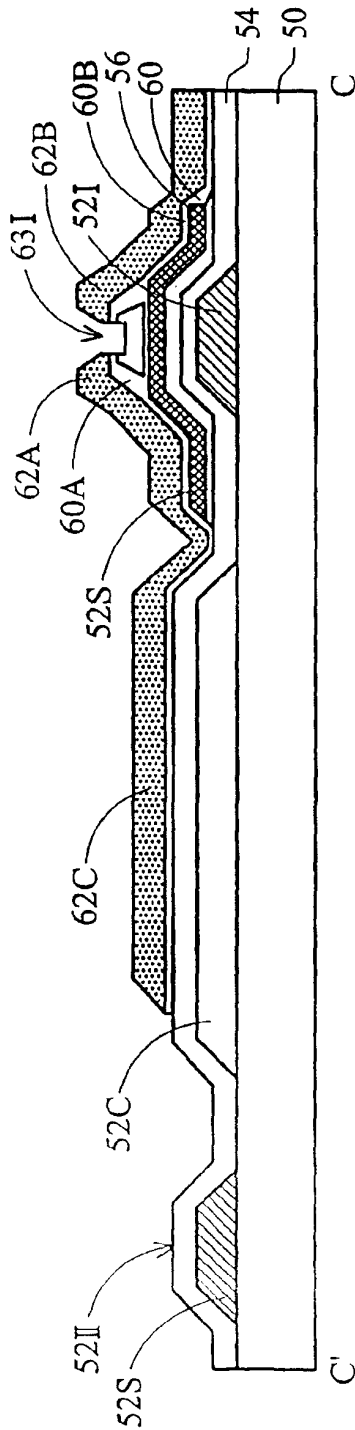
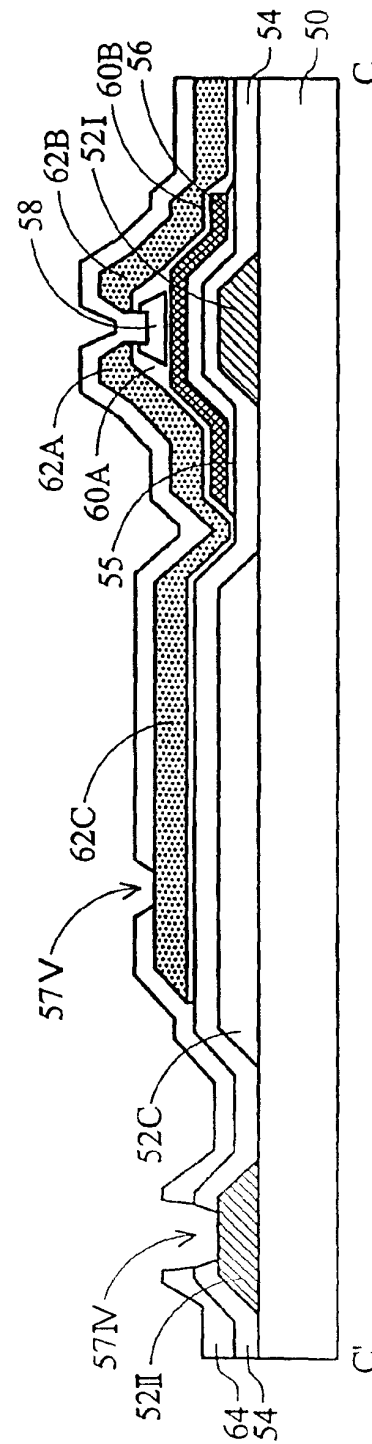


图 5B



50



5D

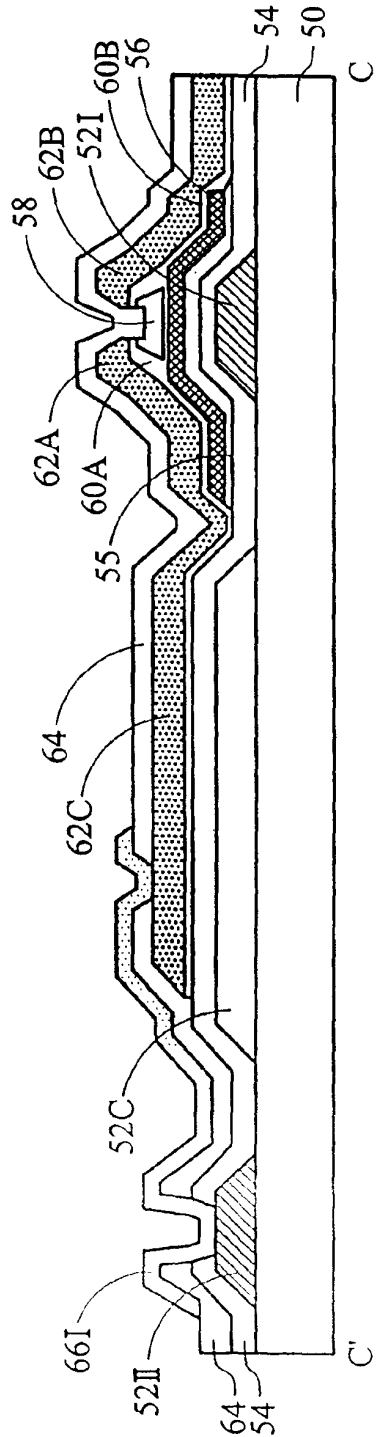


图 5E

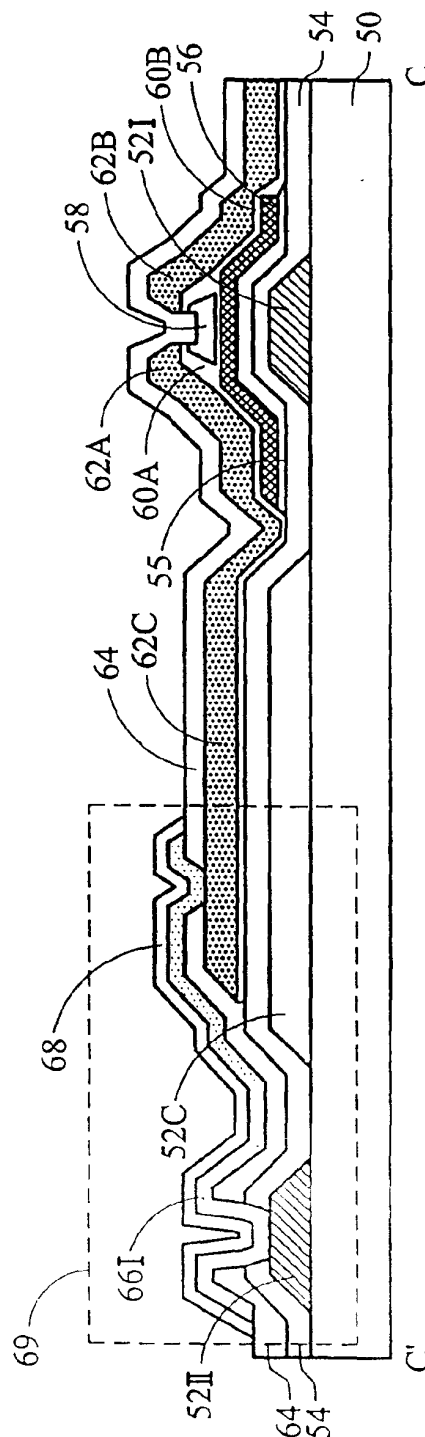


图 5F

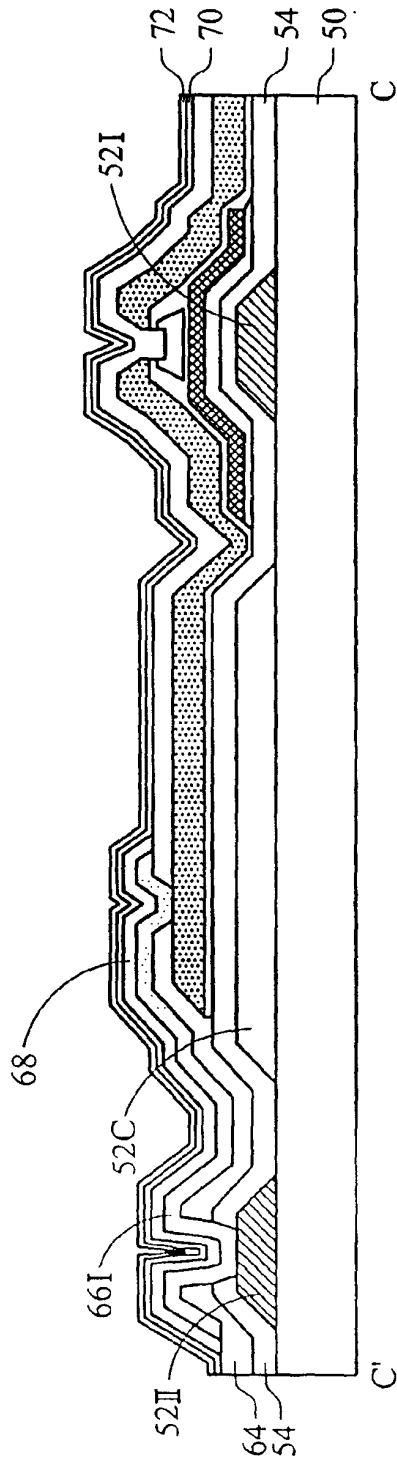


图 5G

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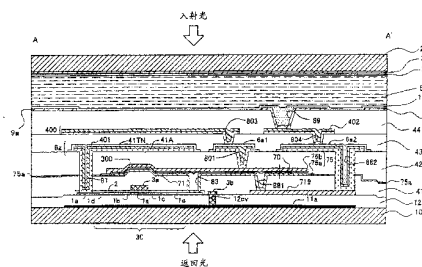
代理人 陈海红 段承恩

权利要求书 4 页 说明书 33 页 附图 9 页

[54] 发明名称 电光装置及其制造方法和电子设备

[57] 摘要

在电光装置中, 具备: 在基板上在第 1 方向上延伸的数据线; 在与上述数据线交叉的第 2 方向上延伸的扫描线; 被配置为与上述数据线和上述扫描线的交叉区域对应的像素电极和薄膜晶体管; 在从上述数据线算起的下层上形成, 电连到上述薄膜晶体管和上述像素电极上的存储电容器; 在从上述数据线算起的上层上形成的电容器线; 把上述存储电容器的像素电位侧电容器电极和上述像素电极间电连起来, 与上述数据线在同一层上形成的第 1 中继层; 把上述存储电容器的固定电位侧电容器电极和上述电容器线间电连起来, 与上述数据线在同一层上形成的第 2 中继层。此外, 在上述数据线、上述第 1 中继层、上述第 2 中继层中, 含有氮化膜。



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1. 一种电光装置，其特征在于，具备：

在基板上在第1方向上延伸的数据线；

在与上述数据线交叉的第2方向上延伸的扫描线；

被配置为与上述数据线和上述扫描线的交叉区域对应的像素电极和薄膜晶体管；

在比上述数据线往下的下层上形成，电连到上述薄膜晶体管和上述像素电极上的存储电容器；

在比上述数据线往上的上层上形成的电容器线；

把上述存储电容器的像素电位侧电容器电极和上述像素电极间电连起来，与上述数据线以同一层形成的第1中继层；

把上述存储电容器的固定电位侧电容器电极和上述电容器线间电连起来，与上述数据线以同一层形成的第2中继层，

在上述数据线、上述第1中继层、上述第2中继层中，含有氮化膜。

2. 据权利要求1所述的电光装置，其特征在于：上述数据线、上述第1中继层、上述第2中继层，在导电层上含有氮化膜。

3. 根据权利要求2所述的电光装置，其特征在于：上述数据线、上述第1中继层、上述第2中继层，是铝、氮化钛膜、氮化硅膜的3层结构。

4. 根据权利要求1所述的电光装置，其特征在于：上述第1中继层，中间存在着与上述电容器线以同一层形成的第3中继层电连到上述像素电极上。

5. 根据权利要求4所述的电光装置，其特征在于：上述电容器线和上述第3中继层，在导电层上含有氮化膜。

6. 根据权利要求5所述的电光装置，其特征在于：上述电容器线和上述第3中继层，是铝、氮化钛膜、氮化硅膜的3层结构。

7. 根据权利要求1所述的电光装置，其特征在于：上述像素电位侧电容器电极，中间存在着在形成上述薄膜晶体管的绝缘膜上形成的第4中继层地电连到上述第1中继层上。

8. 根据权利要求7所述的电光装置,其特征在于:上述第4中继层,与上述薄膜晶体管的栅电极以同一膜形成。

9. 根据权利要求1所述的电光装置,其特征在于:上述扫描线在上述薄膜晶体管的下层上设置,而且,通过接触孔与在上述薄膜晶体管的半导体层上设置的栅电极连接。

10. 根据权利要求1所述的电光装置,其特征在于:在上述存储电容器的上述像素电位侧电容器电极和上述固定电位侧电容器电极之间,是由含有不同的材料的多层构成,同时,其中的1层,是含有由介电系数比别的层高的材料构成的层的电介质膜。

11. 根据权利要求10所述的电光装置,其特征在于:
上述电介质膜,由氧化硅膜和氮化硅膜构成。

12. 根据权利要求1所述的电光装置,其特征在于:
上述电容器线,用遮光膜形成,同时,被形成为沿着上述数据线,而且宽度被形成为比上述数据线更宽。

13. 根据权利要求1所述的电光装置,其特征在于:
在作为上述像素电极的基底配置的第1绝缘膜,和作为上述电容器线的基底配置的第2绝缘膜之中,至少对上述第1绝缘膜的表面实施平坦化处理。

14. 一种电子设备,其特征在于:其构成为具备如下电光装置,该电光装置,具备:

在基板上在第1方向上延伸的数据线;

在与上述数据线交叉的第2方向上延伸的扫描线;

被配置为与上述数据线和上述扫描线的交叉区域对应的像素电极和薄膜晶体管;

在比上述数据线往下的下层上形成,电连到上述薄膜晶体管和上述像素电极上的存储电容器;

从上述数据线往上的上层上形成的电容器线;

把上述存储电容器的像素电位侧电容器电极和上述像素电极间电连起来,与上述数据线以同一层形成的第1中继层;

把上述存储电容器的固定电位侧电容器电极和上述电容器线间电连起来，与上述数据线以同一层形成的第2中继层，且

在上述数据线、上述第1中继层、上述第2中继层中，含有氮化膜。

15. 一种电光装置的制造方法，其特征在于：具备

在衬底上，形成薄膜晶体管的工序；

在上述薄膜晶体管的栅电极上，形成第1层间绝缘膜的工序；

在上述第1层间绝缘膜的上侧，从下边开始依次形成像素电位侧电容器电极、电介质膜和固定电位侧电容器电极，形成存储电容器的工序；

在上述存储电容器的上侧，形成第2层间绝缘膜的工序；

在上述第2层间绝缘膜的上侧，用含有氮化膜的导电材料，形成电连到上述薄膜晶体管的半导体层上的数据线、电连到上述像素电位侧电容器电极上的第1中继层、和电连到上述固定电位侧电容器电极上的第2中继层的工序；

在上述数据线、上述第1中继层、上述第2中继层的上侧，形成第3层间绝缘膜的工序；

在上述第3层间绝缘膜的上侧，形成电连到上述第1中继层上的第3中继层、和电连到上述第2中继层上的电容器线的工序；

在上述第3中继层、上述电容器线的上侧，形成第4层间绝缘膜的工序；在上述第4层间绝缘膜的上侧，形成电连到上述第3中继层上的像素电极的工序。

16. 根据权利要求15所述的电光装置的制造方法，其特征在于：

上述形成存储电容器的工序，由下述工序构成：

形成上述像素电位侧电容器电极的第1前驱膜的工序；

在上述第1前驱膜的上侧，形成上述电介质膜的第2前驱膜的工序；

在上述第2前驱膜的上侧，形成上述固定电位侧电容器电极的第3前驱膜的工序；

一举地使上述第1前驱膜、上述第2前驱膜和上述第3前驱膜图形化形成上述像素电位侧电容器电极、上述电介质膜和上述固定电位侧电容器电极的工序。

17. 根据权利要求 15 所述的电光装置的制造方法，其特征在于：

形成上述存储电容器的工序，由下述工序构成：

形成上述像素电位侧电容器电极的第 1 前驱膜的工序；

使上述第 1 前驱膜图形化形成上述像素电位侧电容器电极的工序；在
上述第 1 前驱膜的上侧，形成上述电介质膜的第 2 前驱膜的工序；

在上述第 2 前驱膜的上侧，形成上述固定电位侧电容器电极的第 3 前
驱膜的工序；

使上述第 3 前驱膜图形化形成上述电介质膜和上述固定电位侧电容器
电极的工序，

上述固定电位侧电容器电极和上述电介质膜，被形成为使得其面积成
为比上述像素电位侧电容器电极和上述电介质膜的面积更大。

电光装置及其制造方法和电子设备

技术领域

本发明属于液晶装置等的电光装置和具备该电光装置而构成的电子设备的技术领域。此外，本发明还属于电子纸(paper)等的电泳装置或 EL(电致发光)装置或使用电子发射元件的装置(电场发射显示器和表面传导电子发射显示器)等的技术领域。

背景技术

以往，人们知道可以采用把液晶等的电光物质挟持于一对基板间构成，使得贯通它们那样地使光透过的办法进行图像的显示的液晶装置等的电光装置。在这里，所谓‘图像的显示’，例如可以采用得益于对每一个像素都使电光物质的状态可变，而使光的透过率发生变化，因而对每一个像素都可以辨认灰度等级不同的光的办法实现。

作为这样的电光装置，采用在上述一对的基板的一方上，具备矩阵状地排列起来的像素电极和被设置为使得把该像素电极间连起来的扫描线和数据线，以及作为像素开关用元件的 TFT(薄膜晶体管)等的办法，已可以提供可进行有源矩阵驱动的电光装置。在该可有源矩阵驱动的电光装置中，上述 TFT，具备于像素电极和数据线间，控制两者的导通。此外，该 TFT 已与扫描线和数据线电连起来。借助于此，在可以通过扫描线控制 TFT 的导通·截止的同时，在该 TFT 为导通的情况下，就给像素电极施加通过数据线供给来的图像信号，就是说，变成为可以对每一个像素都使光透过率变化。

在以上那样的电光装置中，虽然结果变成为在一方的基板上制作上上述那样的各种构成，但是若将之平面性地展开，则结果就变成为需要大面积，因而存在着使像素开口率，就是说，使对基板整个面的区域的光应该透过的区域的比率降低的可能性。因此，在现有技术中，也采用立体地构

成上述的各种要部的手法，就是说采用中间存在着层间绝缘膜地使各种构成要部进行叠层起来构成上述的各种构成要部的手法。说得更为具体一点，就是在基板上首先形成TFT和具有作为该TFT的栅电极膜的功能的扫描线，在其上形成数据线，再在其上形成像素电极等。这样一来，除去可以实现装置的小型化之外，归因于适当地设定各种要部的配置，还可以实现像素开口率的提高等。

但是，在以往的电光装置中，却存在着如下问题。

这就是TFT的寿命比较短的问题。这是因为当水分混入到构成TFT的半导体层或栅绝缘膜内时，归因于水分子向栅绝缘膜和半导体层的界面上的扩散就会产生正电荷，使得阈值电压 V_{th} 在比较短的期间内上升的缘故。这样的现象，在P沟型TFT中，更为妥当。如上述，如果TFT是比较短命的，当然结果就会变成为对整个电光装置造成影响以及从比较早期的阶段就可以观察到图像品质的降低，甚至还存在着装置本身很快就不再工作的危险性。

发明内容

本发明就是鉴于上述那些问题而完成的，目的在于提供实现TFT的长寿命化，可以显示品质更高的图像的电光装置。此外，本发明的目的还在于提供其构成为具备这样的电光装置的电子设备。

本发明的电光装置，为了解决上述课题，具备：在基板上在第1方向上延伸的数据线；在与上述数据线交叉的第2方向上延伸的扫描线；被配置为与上述数据线和上述扫描线的交叉区域对应的像素电极和薄膜晶体管；在从上述数据线算起的下层上形成，电连到上述薄膜晶体管和上述像素电极上的存储电容器；在从上述数据线算起的上层上形成的电容器线；把上述存储电容器的像素电位侧电容器电极和上述像素电极间电连起来，与上述数据线在同一层上形成的第1中继层；把上述存储电容器的固定电位侧电容器电极和上述电容器线间电连起来，与上述数据线在同一层上形成的第2中继层。此外，在上述数据线、上述第1中继层、上述第2中继层中，含有氮化膜。

倘采用该电光装置,首先,由于具备扫描线和数据线以及像素电极和薄膜晶体管,故可进行有源矩阵驱动。此外,在该电光装置中,由于上述的各种构成要部构成叠层结构的一部分,故可以实现装置全体的小型化等,此外,由于实现各种构成要部的适当的配置,故还可以实现像素开口率的提高。

特别是在数据线、第1中继层、第2中继层中,含有氮化膜,该氮化膜由于阻挡水分的浸入或扩散的作用优良,故可以极力防止水分对薄膜晶体管的半导体层的浸入。借助于此,就可以极力防止薄膜晶体管的阈值电压上升这样的缺点,就可以长期地保持电光装置的工作寿命。

在本发明的电光装置的形态中,上述数据线、上述第1中继层、上述第2中继层,在导电层上可以含有氮化膜。特别是上述数据线、上述第1中继层、上述第2中继层,可以是铝、氮化钛膜、氮化硅膜的3层结构。

倘采用本形态,由于数据线含有本身为电阻比较低的材料的铝,故可以顺利地实现图像信号对薄膜晶体管、像素电极的供给。另一方面,由于在数据线上形成了阻挡水分的浸入的作用优良的氮化硅膜,故可以实现薄膜晶体管的抗湿性的提高,可以实现其长寿命化。另外,氮化硅膜理想的是等离子体氮化硅膜。

此外,第1中继层和第2中继层的氮化钛膜,起着要对第1中继层和第2中继层形成的接触孔的刻蚀的穿透防止的壁垒金属的作用。此外,由于与数据线一起阻挡水分的浸入,故可以实现薄膜晶体管的抗湿性的提高,可以实现其长寿命化。

此外,在本发明的电光装置的形态中,上述第1中继层,可中间存在着与上述电容器线用同一层形成的第3中继层电连到上述像素电极上。此外,上述电容器线和上述第3中继层,可在导电层上含有氮化膜。此外,上述电容器线和上述第3中继层,是铝、氮化钛膜、氮化硅膜的3层结构。

倘采用本形态,由于在数据线和像素电极间具备有屏蔽层,故可以防患于未然地防止在两者间形成电容耦合。就是说,可减少由于数据线的通电,产生像素电极的电位变动等的可能性,可以显示品质更高的图像。

此外,在本发明的电光装置的形态中,上述像素电位侧电容器电极,

中间存在着在形成上述薄膜晶体管的绝缘膜上形成的第4中继层地电连到上述第1中继层上。

倘采用本形态，由于像素电位侧电容器电极和像素电极，已经用像素电位侧电容器电极的下层进行电连，故在使存储电容器图形化时就可以防止刻蚀时的穿透。

此外，作为另一形态，上述第4中继层，与上述薄膜晶体管的栅电极用同一膜形成。

倘采用本形态，与经由特别的工序制造第4中继层等的情况比较，可以实现制造工序的简化或制造成本的低廉化。此外，在扫描线含有栅电极的情况下，在该扫描线中，至少对于该栅电极部分来说，例如也可以作为由导电性的多晶硅膜构成的构成，以便使得可以充分地发挥作为该栅电极的功能。在这样的情况下，结果就变成第4中继层也由导电性的多晶硅膜等构成。

另外，反之，由本形态的说明可知，本发明的“第4中继层”，并非一定要与栅电极作为同一膜形成不可，在该情况下，如上述，由于根本不会说用同一材料构成中继层和栅电极，故该中继层的材料，只要具有导电性，基本上可以自由选择。

在本形态中特别是在上述叠层结构中，上述扫描线和上述栅电极分别在不同的层上形成。

倘采用这样的构成，叠层结构具体地说例如形成这样的结构：扫描线位于更下层(或上层)，栅电极位于更上层(或下层)等。借助于此，在形成栅电极的层中，就像形成扫描线的情况下那样，就没有必要实施条带状的图形化，如果可以把薄膜晶体管矩阵状地排列起来，则为了形成该栅电极，只要进行与该矩阵状对应的那样的岛状的图形化等即可。即，结果变成为在形成该栅电极的层中，可以确保比较广大的剩余面积。

因此，如上述，在把栅电极和第4中继层形成成为同一膜的情况下，结果就变成为可以得到容易形成该中继层这样的优点。

在本形态中，上述扫描线还可以构成为使得具备向上述第1方向上突出出来的突出部分。

倘采用这样的构成，则在与栅电极或与此形成一体而不可分的薄膜晶体管不同的层上形成扫描线，而且，由于该扫描线具有向第1方向上突出出来的突出部分，故可使该扫描线起着对薄膜晶体管的下侧遮光膜的作用。就是说，由于可以防患于未然地防止光对薄膜晶体管的半导体层的入射，抑制光漏泄电流的产生，故可以显示没有闪烁等的高品质的图像。

另外，在该情况下，作为扫描线，理想的是由光吸收性比较好的导电性多晶硅，或钨硅化物(WSi)等构成。此外，上述电介质膜可由氧化硅膜及氮化硅膜构成。

此外，在本发明的电光装置的形态中，在上述存储电容器的上述像素电位侧电容器电极和上述固定电位侧电容器电极之间，是由含有不同的材料的多层构成，同时，其中的1层，是含有由与别的层比高介电系数材料构成的层的电介质膜。此外，上述电介质膜可由氧化硅膜及氮化硅膜构成。

倘采用本形态，则与现有技术比较，电荷存储特性更为优良，借助于此，可以进一步提高像素电极的电位保持特性，因而可以显示品质更高的图像。另外，作为在本发明中所说的‘高介电系数材料’，除后述的氮化硅之外，还可以举出其构成为含有TaO_x(氧化钽)、BST(钛酸锶钽)、PZT(钛酸锆酸盐)、TiO₂(氧化钛)、ZrO₂(氧化锆)、HfO₂(氧化铪)以及SiON(氧氮化硅)和SiN(氮化硅)之内的至少一种的绝缘材料等。特别是如果使用TaO_x、BST、PZT、TiO₂、ZrO₂、HfO₂等的高介电系数材料，则可以在有限的基板上区域内增大电容值。或者，若使用SiO₂(二氧化硅)以及SiON(氧氮化硅)和SiN(氮化硅)这样的含硅的材料，则可以减少在层间绝缘膜上的应力的发生。

除此之外，在本发明中，构成上述的存储电容器的像素电位侧电容器电极和像素电极，在叠层结构中，还通过位于它们各自的下层上的中继层电连起来。就是说，像素电位侧电容器电极和中继层之间的配置关系，变成前者位于更上层后者位于更下层，而且像素电极与中继层之间的配置关系也是前者位于更上层后者位于更下层。总之，在这3者之间结果就变成中继层位于最下层。此外，由于像素电位侧电容器电极和像素电极间的电连，通过上述中继层进行，故在该结构中，就可以在像素电位侧电容

器电极和像素电极中的每一者的下侧都具有电连接点，在其上侧都不具有电连接点。

在这里，像素电位侧电容器电极在其上侧不具有电连接点这件事，意味着就不需要像现有技术那样，为了实现像素电位侧电容器电极与像素电极之间的连接，进行就如从叠层结构的上方看可以看见该像素电位侧电容器电极的表面那样的处理或加工。例如，在像素电位侧电容器电极和固定电位侧电容器电极的配置关系为前者位于更下层、后者位于更上层这样的情况下，如果，假定进行使得可以看见像素电位侧电容器电极的表面那样的加工，则就必须使位于其上层的固定电位侧电容器电极图形化为具有规定形状。就是说，就必须把固定电位侧电容器电极图形化为使得固定电位侧电容器电极的面积变得比像素电位侧电容器电极的面积更小，换句话说，就必须使像素电位侧电容器电极的边缘从固定电位侧电容器电极的边缘说起来伸出去。

但是，这样的图形化结果伴随有很大的困难。之所以这么说，是因为一般地说固定电位侧电容器电极的刻蚀，虽然可以选择电介质膜的刻蚀速率比固定电位侧电容器电极更慢的刻蚀条件，以便使得刻蚀在电介质膜的途中停下来，但是，由于上述电介质膜通常被形成得更薄，此外，在本发明中，特别是电介质膜由 SiN 或 TaO_x 等的高介电系数材料构成等等，有时候刻蚀在电介质膜的途中不会停止，此外，还因为：在有的电介质膜的材料的情况下，由于不能使得电介质膜的刻蚀速率比固定电位侧电容器电极的刻蚀速率更慢那样地选择刻蚀条件，故如果进行上述那样的图形化，则在像素电位侧电容器电极中，发生所谓的‘穿透’等的可能性很大。如果发生了这样的事态，由于在不好的情况下，存在着使构成存储电容器的一对的电极间产生短路的危险性，故还可以产生使得该存储电容器已经不可能用做电容器等这样的情况。

然而，在本发明中，如上述，由于像素电位侧电容器电极的电连接点存在于其下侧，故不需要那种为了使该像素电位侧电容器电极的表面显现出来，而实施对固定电位侧电容器电极的困难的图形化处理。

归因于以上，倘采用本发明，由于在可以良好地实现像素电位侧电容器

电极和像素电极之间的电连的同时，还可以极力降低在存储电容器中产生无用的缺陷(例如，上述的那种像素电位侧电容器电极中的穿透或短路等)的危险性，故可以提供更为良好的工作的电光装置。此外，由于可以说具备上述那样的中继层、存储电容器等的配置关系的电光装置提供了满意的叠层结构，故可以比较容易地实现进一步的小型化・高精细化。

此外，本发明的上述电容器线可以用遮光膜形成，同时，可以沿着上述数据线而且形成宽度比上述数据线更宽。

此外，本发明，在作为上述像素电极的基底配置的第1绝缘膜，和作为上述电容器线的基底配置的第2绝缘膜之内，至少可对上述第1绝缘膜的表面实施平坦化处理。

倘采用本形态，由于在像素电极下边具备层间绝缘膜的同时，还对该层间绝缘膜的表面实施例如CMP(化学机械研磨)处理等的平坦化处理，故可以减少在液晶等的电光物质的取向状态中产生紊乱的可能性，因而可以显示品质更高的图像。这是因为由于在本发明中具备中继层，从可以考虑使像素电极下边的层间绝缘膜表面上的凹凸的程度成为更大那样的情况来看，在提供进行更为正确的工作的电光装置方面是有利的。

此外，如上述，在具备屏蔽层的电光装置的形态中，可以成为这样的构成：还具备作为上述屏蔽层的基底配置的别的层间绝缘膜，上述别的层间绝缘膜的表面已施行了平坦化处理。

倘采用这样的构成，由于在具备作为屏蔽层的基底配置的别的层间绝缘膜的同时，别的层间绝缘膜的表面已施行了例如CMP处理等的平坦化处理，故可以减少在液晶等的电光物质的取向状态中产生紊乱的可能性，因而可以显示品质更高的图像。

此外，在该形态中，若可具有一并实施像上述那样地配置在像素电极下边的层间绝缘膜的平坦化处理的形态，则结果就变成可以更为有效地享受上述的作用效果。

或者，在具备屏蔽层的电光装置的形态中，可以成为这样的构成：在上述衬底上具备有上述薄膜晶体管的栅电极的上述扫描线；作为该扫描线的上层，具备上述存储电容器的上层，具备上述数

据线；作为该数据线的上层，具备上述屏蔽层；作为该屏蔽层的上层，具备上述像素电极；该存储电容器具备从下层开始为上述像素电位侧电容器电极、上述电介质膜和上述固定电位侧电容器电极这样的配置，上述中继层被形成为与上述栅电极同一膜。

倘采用这样的构成，结果变成为作为要在衬底上构筑的叠层结构，可以提供将变成为最佳的配置或布局的一个形态。

本发明的电光装置的制造方法，为了解决上述课题，其特征在于：具备：在衬底上，形成薄膜晶体管的工序；在上述薄膜晶体管的栅电极上，形成第1层间绝缘膜的工序；在上述第1层间绝缘膜的上侧，从下边开始依次形成像素电位侧电容器电极、电介质膜和固定电位侧电容器电极，形成存储电容器的工序；在上述存储电容器的上侧，形成第2层间绝缘膜的工序；在上述第2层间绝缘膜的上侧，用含有氮化膜的材料，形成电连到上述薄膜晶体管的半导体层上的数据线、电连到上述像素电位侧电容器电极上的第1中继层、和电连到上述固定电位侧电容器电极上的第2中继层的工序；在上述数据线、上述第1中继层、上述第2中继层的上侧，形成第3层间绝缘膜的工序；在上述第3层间绝缘膜的上侧，形成电连到上述第1中继层上的第3中继层、和电连到上述第2中继层上的电容器线的工序；在上述第3中继层、上述电容器线的上侧，形成第4层间绝缘膜的工序；在上述第4层间绝缘膜的上侧，形成电连到上述第3中继层上的像素电极的工序。

倘采用这样的制造方法，则可以比较容易地形成上述的电光装置。

在本发明的电光装置的制造方法的一个形态中，形成上述存储电容器的工序，由下述工序构成：形成上述像素电位侧电容器电极的第1前驱膜的工序；在上述第1前驱膜的上侧，形成上述电介质膜的第2前驱膜的工序；在上述第2前驱膜的上侧，形成上述固定电位侧电容器电极的第3前驱膜的工序；一举地使上述第1前驱膜、上述第2前驱膜和上述第3前驱膜图形化以形成上述像素电位侧电容器电极、上述电介质膜和上述固定电位侧电容器电极的工序。

倘采用本形态，则形成存储电容器的工序，包括在一旦形成了像素电位

侧电容器电极、电介质膜和固定电位侧电容器电极中的每一者的第1、第2、第3前驱膜后，使它们一举地图形化的工序。就是说，倘采用本形态，典型地说构成存储电容器的3个要部的平面形状就变成为同一形状。借助于此，就可以制造具有比较大的电容值的存储电容器而不会有无用的平面扩展，就是说不会使像素开口率降低。此外，倘采用本形态，由于使上述3个要部一举地图形化，故不会具有像现有技术那样仅仅刻蚀固定电位侧电容器电极，电介质膜和像素电位侧电容器电极保持原状地残留下来这样的困难的课题。其结果是，若使用本发明，则可以容易地且可靠性高地制造存储电容器。

在本发明的电光装置的制造方法的另一形态中，形成上述存储电容器的工序，由下述工序构成：形成上述像素电位侧电容器电极的第1前驱膜的工序；使上述第1前驱膜图形化以形成上述像素电位侧电容器电极的工序；在上述第1前驱膜的上侧，形成上述电介质膜的第2前驱膜的工序；在上述第2前驱膜的上侧，形成上述固定电位侧电容器电极的第3前驱膜的工序；使上述第3前驱膜图形化以形成上述电介质膜和上述固定电位侧电容器电极的工序，上述固定电位侧电容器电极和上述电介质膜，被形成为使得其面积变得比上述像素电位侧电容器电极和上述电介质膜的面积更大。

倘采用本形态，则与上述不同，一旦要形成像素电位侧电容器电极，要实施第1前驱膜的图形化，然后，形成电介质膜和固定电位侧电容器电极。还有，在本形态中，固定电位侧电容器电极的面积，被形成为比像素电位侧电容器电极和电介质膜的面积更大。根据以上，就可以形成固定电位侧电容器电极和电介质膜具有把像素电位侧电容器电极覆盖起来那样的结构的存储电容器。因此，结果就变成为可以用更宽的电极面积挟持电介质膜，可以构成具有更大的电容值的存储电容器。具体地说例如在本形态中，就可以把上述3个要部的侧面也用做电容器，就可以期待由此得到的电容值的增大。此外，从这样的观点看，例如，只要预先把像素电位侧电容器电极形成得厚等，上述侧面的面积就会增大，就可以效率良好地得到电容值。再有，倘采用这样的形态，则可使之难于产生像素电位侧电容器电极和固定电位侧电容器电极间的短路。

另外，在本形态中，也可以作成为在实施对第3前驱膜的图形化时，与此同时实施对第2前驱膜的图形化。

本发明的电子设备，其构成为具备上述本发明的电光装置。其中，包括其各种形态。

倘采用本发明的电子设备，由于其构成为具备上述的本发明的电光装置，故可以实现存储电容器和像素电极间的良好电连，另外，由于可期待该存储电容器的正确的工作，可以显示更高品质的图像，同时可实现具备可靠性高的液晶装置等的电光装置构成的各种电子设备：投影式显示装置、液晶电视、移动电话、电子笔记本、文字处理机、取景器式或监视器直视式的视频录像机、工作站、电视电话、POS终端、触摸面板等。

本发明的这样的作用和其它的好处会从其次要说明的实施形态中了解明白。

附图说明

图1的电路图，示出了设置在构成本发明的实施形态的电光装置的图像显示区域的矩阵状的多个像素上的各种元件、布线等的等效电路。

图2是本发明的实施形态的电光装置的已形成了数据线、扫描线、像素电极等的TFT阵列基板的相邻接的多个像素群的平面图。

图3是仅仅抽出了图2之内的主要部分的平面图。

图4是图2的A-A'剖面图。

图5的部分剖面图，示出了目的为进行与图4的对比的结构。

图6的工序剖面图，按照顺序示出了本发明的实施形态的电光装置的制造方法(其1)。

图7的工序剖面图，按照顺序示出了本发明的实施形态的电光装置的制造方法(其2)。

图8是与在TFT阵列基板上形成的各个构成要部一起从对向基板一侧看本发明的实施形态的电光装置的TFT阵列基板的平面图。

图9是图8的H-H'剖面图。

图10是示意性的剖面图示出了作为本发明的电子设备的实施形态的本

身为投影式彩色显示装置的一个例子的彩色液晶投影仪。

具体实施方式

以下，边参看附图边说明本发明的实施形态。以下的实施形态，是把本发明的电光装置应用于液晶装置的实施形态。

(像素部分的构成)

首先，参看图 1 到图 4 对本发明的实施形态的电光装置的像素部分的构成进行说明。在这里，图 1 是构成电光装置的图像显示区域的矩阵状形成的多个像素的各种元件、布线等的等效电路图。图 2 是已形成了数据线、扫描线、像素电极等的 TFT 阵列基板的相邻接的多个像素群的平面图。另外，图 3 是仅仅抽出了图 2 之内的主要部分，具体地说，为了示出数据线、屏蔽层和像素电极间的配置关系，主要地仅仅抽出这些的平面图。图 4 是图 2 的 A-A' 剖面图。另外，在图 4 中，为了把各层和各个构件作成为在图面上可以识别的那种程度的大小，对于该各个层和各个构件都采用了不同的比例尺。

在图 1 中，在构成本实施形态的电光装置的图像显示区域的矩阵状地形成的多个像素上，分别形成有像素电极 9a 和用来开关控制该像素电极 9a 的 TFT30，供给图像信号的数据线 6a 被电连到该 TFT30 的源上。要写入到数据线 6a 上的图像信号 S1、S2、...、Sn，既可以按照该顺序线顺序地供给，也可以作成为对相邻的多条数据线 6a 彼此间每组供给。

此外，要构成为使得栅电极电连到 TFT30 的栅上，并以规定的定时，按照扫描信号 G1、G2、...、Gm 的顺序，线顺序地给扫描线 11a 和栅电极脉冲式地加上扫描信号。像素电极 9a 已电连到 TFT30 的漏上，采用使作为开关元件的 TFT30 仅仅在恒定的期间内才闭合其开关的办法，以规定的定时，把从数据线 6a 供给的图像信号 S1、S2、...、Sn 写入。

通过像素电极 9a 写入到作为电光物质的一个例子的液晶内的规定电平的图像信号 S1、S2、...、Sn 在与在对向基板上形成的对向电极之间可保持恒定期间。液晶采用借助于施加的电压电平使分子集合的取向或秩序变化的办法，对光进行调制，使得可以进行灰度等级显示。若是常态白色模式，

则根据在各个像素的单位中施加上的电压减小对入射光的透过率,若是常态黑色模式,则根据在各个像素的单位中施加上的电压增加对入射光的透过率,作为全体从电光装置出射具有与图像信号对应的对比度的光。

在这里,为了防止所保持的图像信号进行漏泄,要与在像素电极 9a 和对向电极之间形成的液晶电容并联地附加上存储电容器 70。该存储电容器 70,被设置为与扫描线 11a 并行,且含有固定电位侧电容器电极,同时,还含有已固定于恒定电位上的电容器电极 300。

以下,参看图 2 到图 4,对由上述数据线 6a、扫描线 11a、及栅电极、TFT30 等实施的实现上述那样的电路工作的电光装置的实际的构成进行说明。

首先,在图 2 中,在 TFT 阵列基板 10 上,矩阵状地设置多个像素电极 9a (用虚线部分示出了轮廓),分别沿着像素电极 9a 的纵横边界地设置数据线 6a 和扫描线 11a。数据线 6a 如后所述由含有铝膜等的叠层结构构成,扫描线 11a 例如由导电性的多晶硅膜等构成。此外,扫描线 11a 被电连到与半导体层 1a 之内用图中右上斜的斜线区域表示的沟道区 1a' 对向的栅电极 3a 上,该栅电极 3a 已变成为含于该扫描线 11a 内的形式。就是说,在栅电极 3a 与数据线 6a 之间的交叉的部位上,分别设置有含于扫描线 11a 内的栅电极 3a 对向配置在沟道区 1a' 上的像素开关用的 TFT30。换句话说,TFT30 的(除去栅电极)已变成为存在于栅电极 3a 和扫描线 11a 之间这样的形态。

其次,电光装置,如本身为图 2 的 A-A' 线剖面图的图 4 所示,例如,具备由石英基板、玻璃基板、硅基板构成的 TFT 阵列基板 10,和与之对向配置的例如由玻璃基板或石英基板构成的对向基板 20。

在 TFT 阵列基板 10 一侧,如图 4 所示,设置有上述像素电极 9a,在其上侧,设置有已施行了摩擦处理等的规定的取向处理的取向膜 16。像素电极 9a 例如由 ITO 膜等的透明导电性膜构成。另一方面,在对向基板 20 一侧,遍及其整个面地设置对向电极 21,在其下侧,设置有已施行了摩擦处理等的规定的取向处理的取向膜 22。其中,对向电极 21,与上述的像素电极 9a 同样,例如由 ITO 膜等的透明导电性膜构成,上述的取向膜 16 和 22,

例如，由聚酰亚胺膜等的透明的有机膜构成。

在像这样地对向配置的 TFT 阵列基板 10 和对向基板 20 之间，向由后述的密封材料(参看图 8 和 9)围起来的空间内，封入液晶等电光物质，形成液晶层 50。液晶层 50 在未施加来自像素电极 9a 的电场的状态下，借助于取向膜 16 和 22 得到规定的取向状态。液晶层 50 例如由把一种或数种的向列液晶混合起来的电光物质构成。密封材料是用来在 TFT 阵列基板 10 和对向基板 20 的周边把它们粘贴起来的例如光硬化树脂或热硬化树脂构成的粘接剂，已混入有用来使两基板间的距离变成为规定值的玻璃纤维或玻璃微珠等的间隙材料。

另一方面，在 TFT 阵列基板 10 上，除去上述的像素电极 9a 和取向膜 16 之外，形成叠层结构地具备包括它们的各种的构成。该叠层结构，如图 4 所示，从下边开始，按照顺序，由含有扫描线 11a 的第 1 层、含有含有栅电极 3a 的 TFT30 等的第 2 层、含有存储电容器 70 的第 3 层、含有数据线 6a 等的第 4 层、含有上述屏蔽层 400 等的第 5 层、含有上述像素电极 9a 和取向膜 16 等的第 6 层(最上层)构成。此外，在第 1 层和第 2 层之间设置有基底绝缘膜 12，在第 2 层和第 3 层之间设置有第 1 层间绝缘膜 41，在第 3 层和第 4 层之间设置有第 2 层间绝缘膜 42，在第 4 层和第 5 层之间设置有第 3 层间绝缘膜 43，在第 5 层和第 6 层之间设置有第 4 层间绝缘膜 44，防止上述的各个要部间产生短路。此外，在这些各种的绝缘膜 12、41、42、43 和 44 上，还设置有例如把 TFT30 的半导体层 1a 中的高浓度源区 1d 和数据线 6a 电连起来的接触孔等。以下，对于这些各个要部从下边开始依次进行说明。

首先，在第 1 层上，设置有由含有 Ti(钛)、Cr(铬)、W(钨)、Ta(钽)、Mo(钼)等的高熔点金属之内的至少一种的、金属单体、合金或金属硅化物、聚合硅化物或把它们叠层起来的叠层体或导电性多晶硅等构成的等构成的扫描线 11a。该扫描线 11a，从平面上看被图形化为沿图 2 的 X 方向的条带状。说得更为详细一点，条带状的扫描线 11a，具备沿着图 2 的 X 方向延伸的主线部分，和在数据线 6a 或屏蔽层 400 进行延伸的图 2 的 Y 方向上延伸的突出部分。另外，从相邻接的扫描线 11a 延伸出来的突出部分彼此不

会连接，因此，该扫描线 11a 变成 1 条 1 条分断开来的形式。

借助于此，扫描线 11a 结果就变成具有齐地控制在同一行上存在的 TFT30 的导通、截止的功能。此外，该扫描线 11a 由于被形成使得把未形成像素电极 9a 的区域大体上埋起来，故还具有遮挡要从下侧向 TFT30 入射的光的功能。借助于此，就可以抑制 TFT30 的半导体层 1a 中的光漏泄电流的发生，可以进行无闪烁的高品质的图像显示。另外，在导电性的多晶硅的情况下，具备光吸收性的功能。

其次，作为第 2 层，设置有含有栅电极 3a 的 TFT30。TFT30，如图 4 所示，具有 LDD(轻掺杂漏)结构，作为其构成要部，上述的栅电极 3a，具备：例如由多晶硅膜构成可借助于来自栅电极 3a 的电场形成沟道的半导体层 1a 的沟道区 1a'，含有使栅电极 3a 和半导体层 1a 绝缘的栅绝缘膜的绝缘膜 2，半导体层 1a 中的低浓度源区 1b、低浓度漏区 1c 以及高浓度源区 1d 和高浓度漏区 1e。

此外，在本实施形态中，特别是在该第 2 层上，作为与上述的栅电极 3a 同一膜形成有中继层 719。该中继层 719，从平面上看，如图 2 所示，使得位于各个像素电极 9a 的一边的大体上的中央那样地被形成成为岛状。由于中继层 719 和栅电极 3a 被形成成为同一膜，故在后者例如由导电性多晶硅膜等构成的情况下，前者也由导电性多晶硅膜等构成。

另外，上述的 TFT30，虽然理想的是具有图 4 所示的那样的 LDD 结构，但是既可以具有向低浓度源区 1b 和低浓度漏区 1c 不进行杂质注入的补偿(off set)结构，也可以是以栅电极 3a 为掩模高浓度地注入杂质，自我对准地形成高浓度源区和高浓度漏区的自对准型的 TFT。此外，在本实施形态中，虽然作成为在高浓度源区 1d 和高浓度漏区 1e 之间，仅仅配置 1 个栅电极的单个栅结构，但是也可以在它们之间配置 2 个以上的栅电极。若如上述地用双栅或三栅以上构成 TFT，则可以防止沟道与源和漏区之间的结部分的漏泄电流，可以减小截止时的电流。

此外，构成 TFT30 的半导体层 1a 非单晶层也罢单晶层也罢都可以。单晶层的形成，可以使用粘贴法等众所周知的方法。采用使半导体层 1a 变成单晶层的办法，就可以实现特别是外围电路的高性能化。

在以上所说明的扫描线 11a 上, 而且, 在 TFT30 的下边, 设置例如由氧化硅膜等构成的基底绝缘膜 12。基底绝缘膜 12, 归因于除去将扫描线 11a 与 TFT30 进行层间绝缘的功能外, 在 TFT 阵列基板 10 的整个面上形成, 故具有防止在 TFT 阵列基板 10 的表面研磨时的表面粗糙化或因清洗后剩下的污垢等引起的像素开关用的 TFT30 的特性变化的功能。

在该基底绝缘膜 12 上, 从平面上看半导体层 1a 的两边挖了与沿着后边讲述的数据线 6a 延伸的半导体层 1a 的沟道长度同一幅度, 或比沟道长度更长的沟(构成接触孔的沟) 12cv, 与该沟 12cv 对应地在其上方叠层上的栅电极 3a, 在下侧含有凹状地形成的部分。此外, 采用使得把该沟 12cv 全部填埋起来那样地形成栅电极 3a 的办法, 结果就变成为在该栅电极 3a 上延长设置与之一体地形成的侧壁部分 3b。借助于此, TFT30 的半导体层 1a, 就如在图 2 中很好地示出的那样, 从平面上看就从侧方被被覆起来, 至少可以抑制来自该部分的光的入射。

此外, 该侧壁部分 3b, 在被形成为把上述沟 12cv 埋起来的同时, 还被作为使得其下端与上述扫描线 11a 接连。在这里, 扫描线 11a 由于如上述被形成为条带状, 存在于某一行上的栅电极 3a 及扫描线 11a, 只要着眼于该行, 就总是变成为同电位。

在这里, 在本发明中, 也可以采用这样的结构: 使得与扫描线 11a 平行地形成含有栅电极 3a 的别的扫描线。在该情况下, 该扫描线 11a 和该别的扫描线, 结果就变成为形成冗余的布线结构。

借助于此, 结果就变成为, 例如, 即便是因在该扫描线 11a 的一部分中存在着不论什么缺陷, 而变得不能进行正常的通电的情况下, 只要与该扫描线 11a 存在于同一行上的别的扫描线是健全的, 就可以通过该别的扫描线依然正常地进行 TFT30 的工作控制。

接在上述第 2 层后边在第 3 层上, 设置存储电容器 70。存储电容器 70 采用中间存在着电介质膜 75 使作为已电连到 TFT30 的高浓度漏区 1e 和像素电极 9a 上的像素电位侧电容器电极的下部电极 71 和作为固定电位侧电容器电极的电容器电极 300 对向配置的办法形成。倘使用该存储电容器 70, 则可以显著地提高像素电极 9a 的电位保持特性。此外, 本实施形态的存储

电容器 70, 由图 2 的平面图可知, 由于被形成达不到与像素电极 9a 的形成区域大体上对应的光透过区域, 换句话说, 由于被形成收纳于遮光区域内, 故可以把电光装置全体的像素开口率维持得大, 借助于此, 就可以显示更为明亮的图像。

说得更详细点, 下部电极 71, 例如由导电性的多晶硅膜构成, 并起着像素电位侧电容器电极的作用。但是, 下部电极 71, 也可以由含有金属或合金的单一层膜或多层膜构成。此外, 该下部电极 71, 除去起着作为像素电位侧电容器电极的作用之外, 还具有对像素电极 9a 和 TFT30 的高浓度漏区 1e 进行中继连接的功能。因此, 在本实施形态中, 其特征在于: 特别是在这里所说的中继连接, 通过上述中继层 719 进行。这一点在后边再谈。

电容器电极 300, 起着存储电容器 70 的固定电位侧电容器电极的作用。在本实施形态中, 为了使电容器电极 300 变成为固定电位, 要采用与已变成为固定电位的屏蔽层 400 实现电连的办法进行。

此外, 在本实施形态中, 特别是该电容器电极 300, 在 TFT 阵列基板 10 上, 与各个像素相对应地被形成为岛状, 上述下部电极 71, 被形成为与该电容器电极 300 具有大体上同一形状。

借助于此, 本实施形态的存储电容器 70, 不具有在平面上无用的扩展, 就是说, 不会使像素开口率降低, 而且, 在该状况下结果就变成为可以实现最大限度的电容值。就是说, 在本实施形态中, 存储电容器 70 具有更小的面积更大的电容值。

说得更为详细一点, 在图 4 中, 可知: 电容器电极 300 的面积, 被形成为比下部电极 71 的面积稍大一点, 就是说被形成为使得前者把后者覆盖起来。倘采用这样的形态, 就如由图可以看得明白的那样, 由于也可以把该电容器电极 300 和该下部电极 71 的侧面用做电容器(参看图 4 中的存储电容器 70 的左方), 故可以实现电容值的增大化。此外, 也难于产生两者间的短路。另外, 从这样的观点看, 为了增大上述侧面的面积, 例如预先将下部电极 71 形成得比较厚一点也是有效的。

电介质膜 75, 如图 4 所示, 例如可以由膜厚 5 到 200nm 这样的比较薄的 HTO(高温氧化物)膜, LTO(低温氧化物)膜等的氧化硅膜或氮化硅膜等构

成。从增大存储电容 70 的观点看,只要可以充分地得到膜的可靠性,电介质膜 75 越薄越好。此外,在本实施形态中,特别是该电介质膜 75,如图 4 所示,已变成成为下层是氧化硅膜 75a,上层是氮化硅膜 75b 这样的具有 2 层结构的膜。上层的氮化硅膜 75b 被图形化为比像素电位侧电容器电极的下部电极 71 稍大一点的尺寸,使得收纳于遮光区域(非开口区域)内。借助于此,得益于介电系数比较大的氮化硅膜 75b 的存在,除去可以增大存储电容器 70 的电容值之外,得益于氧化硅膜 75a 的存在,则不会使存储电容器 70 的耐压性降低,而与存储电容器 70 的电容值的增大无关。这样一来,采用把电介质膜 75 作成为 2 层结构的办法,就可以享受相反的 2 个作用效果。此外,具有着色性的氮化硅膜 75b 被图形化为比下部电极 71 稍大一些的尺寸,未在可透过光的部分上形成。就是说,由于位于遮光区内,故可以防止透过率的降低。此外,由于氮化硅膜 75b 的存在,防患于未然地防止水对 TFT30 的浸入就成为可能。借助于此,在本实施形态中,就可以进行比较长期的装置的运行而不会招致 TFT30 的阈值电压的上升这样的事态的发生。另外,在本实施形态中,电介质膜 75,虽然变成为具有 2 层结构的膜,但是在有的情况下,例如也可以作成为具有例如氧化硅膜、氮化硅膜和氧化硅膜等这样的 3 层结构或具有 3 层以上叠层结构的构成。

在以上所说明的 TFT30 或栅电极 3a 以及中继层 719 上,而且,在存储电容器 70 的下边,形成例如 NSG(非硅酸盐玻璃)、PSG(磷硅酸盐玻璃)、BSG(硼硅酸盐玻璃)、BPSG(硼磷硅酸盐玻璃)等硅酸盐玻璃膜、氮化硅膜或氧化硅膜等,或者理想地说形成由 NSG 构成的第 1 层间绝缘膜 41。此外,在该第 1 层间绝缘膜 41 上,把 TFT30 的高浓度源区 1d 和后述的数据线 6a 电连起来的接触孔 81,在贯通后述第 2 层间绝缘膜 42 的同时形成开孔。此外,在第 1 层间绝缘膜 41 上,形成把 TFT30 的高浓度漏区 1e 和构成存储电容器 70 的下部电极 71 电连起来的接触孔 83 的开孔。

此外,在该第 1 层间绝缘膜 41 上,形成用来把作为构成存储电容器 70 的像素电位侧电容器电极的下部电极 71 和中继层 719 电连起来的接触孔 881 的开孔。除此之外,在第 1 层间绝缘膜 41 上,把中继层 719 和后述的第 2 中继层 6a2 电连起来的接触孔 882,在贯通后述第 2 层间绝缘膜的同

时形成开孔。

另外，在这些4个接触孔之内，在接触孔81和82的形成部分中，就可以不形成上述的电介质膜75，换句话说就可以在该电介质膜75上形成开口部分。这是因为在该接触孔81中，需要实现高浓度源区1b和数据线6a间的电连，而在接触孔882中，要使该接触孔882贯通第1和第2层间绝缘膜41、42的缘故。顺便提一下，如果在电介质膜75上设置有这样的开口部分，则在进行对TFT30的半导体层1a的氢化处理之类的情况下，也可以得到可以使在该处理中使用的氢通过该开口部分容易地到达半导体层1a的作用效果。

此外，在本实施形态中，对于第1层间绝缘膜41，也可以采用进行约1000℃的烘焙的办法，实现已注入到构成半导体层1a和栅电极3a的多晶硅膜内的离子的激活化。

接在上述的第3层后边在第4层上，设置数据线6a。该数据线6a，使得与TFT30的半导体层1a的延伸方向一致那样地，就是说与图2中的Y方向重叠那样地，被形成成为条带状。该数据线6a，如图4所示，形成从下层开始依次具有由铝构成的层(图4中的标号41A)、由氮化钛构成的层(图4中的标号41TN)、由氮化硅膜构成的层(图4中的标号401)这3层结构的膜。氮化硅膜401，被图形化为稍微大一点的尺寸，以便把其下层的铝层和氮化钛层被覆起来。其中数据线6a由于含有本身为电阻比较低的材料的铝，故可以实现无延迟地对TFT30、像素电极9a的图像信号的供给。另一方面，由于在数据线6a上形成有防止水分的浸入的作用比较优良的氮化硅膜，故可以实现TFT30的耐湿性，可以实现其寿命长期化。氮化硅膜理想的是等离子体氮化硅膜。

此外，在该第4层上，作为与数据线6a同一膜，形成有屏蔽层用中继层6a1和第2中继层6a2，这些，如图2所示，当从平面上看时，由于各者间被形成成为图形上分断开来而不是被形成成为具有于数据线6a连续起来的平面形状。就是说，当着眼于位于图2中最左方的数据线6a时，在其正右方形成有具有大体上四边形形状的屏蔽层用中继层6a1，此外，在其右方形成有具有比屏蔽层用中继层6a1稍大一点的面积的大体上四边形形状

的第2中继层6a2。屏蔽层用中继层6a1和第2中继层6a2,可用与数据线6a同一工序,形成为具有由从下层开始依次为由铝构成的层、由氮化钛构成的层和由等离子体氮化膜构成的层这么3层结构的膜。

此外,等离子体氮化膜,使得把其下层的铝层和氮化钛层覆盖起来那样地被图形化为稍大一点的尺寸。氮化钛层起着用来防止对屏蔽层用中继层6a1、第2中继层6a2形成的接触孔803、804的刻蚀穿透的壁垒金属的作用。

此外,采用在屏蔽层用中继层6a1和第2中继层6a2上,形成阻挡水分的浸入的作用比较优良的氮化硅膜的办法就可以实现TFT30的耐湿性的提高,就可以实现其长寿命化。另外,氮化硅膜,理想的是等离子体氮化硅膜。

在以上所说明的存储电容器70上,而且,在数据线6a的下边,形成有例如NSG、PSG、BSG、BPSG等的硅酸盐玻璃膜、氮化硅膜或氧化硅膜等,或者理想的是用使用TEOS气体的等离子体CVD法形成的第2层间绝缘膜42。在该第2层间绝缘膜42上,在形成把TFT30的高浓度源区1d和数据线6a电连起来的上述接触孔81的开孔的同时,形成把上述屏蔽层用中继层6a1和本身为存储电容器70的上部电极的电容器电极300电连起来的接触孔801的开孔。此外,在第2层间绝缘膜42上,形成有用来把第2中继层6a2和中继层719电连起来的上述接触孔882。

在接在上述第4层后边的第5层上,形成有屏蔽层400。该屏蔽层400,从平面上看,如图2和图3所示,被形成为分别在图中的X方向和Y方向上延伸的网格状。对于在该屏蔽层400之内在图中的Y方向上延伸的部分来说,特别要形成为使得把数据线6a被覆起来,而且,要形成得比该数据线6a的宽度更宽。此外,至于在图中的X方向上延伸的部分,为了确保形成后述的第3中继层402,在各个像素电极9a的一边的中央附近都具有切缺部分。

再有,在图2或图3中,在XY方向中的每一方向上延伸的屏蔽层400的交叉部分的拐角部分上,使得把该拐角部分埋起来那样地设置大体上三角形形状的部分。采用在屏蔽层400上设置该大体上三角形形状的部分的

办法,就可以有效地进行 TFT30 对半导体层 1a 的光的遮挡。就是说,结果就变成那些要从斜上方进入半导体层 1a 的光,在该三角形形状的部分处被反射或被吸收,结果达不到半导体层 1a。因此,可以抑制光漏泄电流的发生,可以显示无闪烁等的高品质的图像。

该屏蔽层 400,采用从配置有像素电极 9a 的图像显示区域 10a 向其周围延长设置,并与恒定电位源进行电连的办法,变成为固定电位。另外,这里所说的‘恒定电位源’,既可以是供往数据线驱动电路 101 的正电源或负电源的恒定电位源,也可以是供往对向基板 20 的对向电极 21 的恒定电位源。

如上述,如果存在着被形成为把数据线 6a 的全体都被覆起来,同时(参看图 3)已变成为固定电位的屏蔽层 400,则可以排除在该数据线 6a 和像素电极 9a 间产生的电容耦合的影响。就是说,可以防患于未然地避免因相应于给数据线 6a 的通电而使得像素电极 9a 的电位变动这样的事态,可以减低在图像上发生沿着该数据线 6a 的显示不均匀等。在本实施形态中,特别是由于屏蔽层 400 被形成为网格状,故即便是对扫描线 11a 的延长部分来说,也可以把它抑制为使得不会产生无用的电容耦合。

此外,在第 4 层上,作为与这样的屏蔽层 400 同一膜,形成作为在本发明中所说的‘中继层’的一个例子的第 3 中继层 402。该第 3 中继层 402,具有通过后述的接触孔 89 对第 2 中继层 6a2 和像素电极 9a 间的电连进行中继的功能。另外,在这些屏蔽层 400 和第 3 中继线 402 间,并不是平面形状地连续地形成,而是被形成为两者之间在图形上被分断开来。

另一方面,上述的屏蔽层 400 和第 3 中继层 402,具有下层是由铝构成的层,上层是由氮化钛构成的层的 2 层结构。此外,在第 3 中继层 402 中,下层的由铝构成的层与第 2 中继层 6a2 连接,上层的由氮化钛构成的层,与由 IT0 等构成的像素电极 9a 连接。在该情况下,结果就变成为特别是后者的连接可以良好地进行。这一点,与假如采用铝和 IT0 直接进行连接的形态,则在两者间就会产生电蚀,产生铝的断线、或者因氧化铝的形成而产生的绝缘等,故不能实现理想的电连的情况,形成鲜明的对照。如上述,在本实施形态中,由于可以良好地实现第 3 中继层 402 与像素电极 9a 之间

的电连,故可以良好地维持对该像素电极 9a 的电压施加、或该像素电极 9a 的电位保持特性。

此外,屏蔽层 400 和第 3 中继层 402,由于含有光反射性能比较优良的铝,而且还含有光吸收特性比较优良的氮化钛,故可以起着遮光层的作用。就是说,倘采用这些,则可以在其上侧阻挡对 TFT30 的半导体层 1a 的入射光(参看图 4)的前进。另外,就这样的事态来说,就如已经说明的那样,对于上述的电容器电极 300 和数据线 6a,可以说也是同样的。在本实施形态中,这些屏蔽层 400、第 3 中继层 402、电容器电极 300 和数据线 6a,在构成要在 TFT 阵列基板 10 上构筑的叠层结构的一部分的同时,还可以作为遮挡对 TFT30 的来自上侧的光入射的上侧遮光膜(或者,如果着眼于已构成‘叠层结构的一部分’这一点则是‘内置遮光膜’)发挥作用。另外,倘应用该‘上侧遮光膜’或‘内置遮光膜’的概念,则除去上述的构成外,还可以考虑为栅电极 3a 或下部电极 71 等以及含于其中的构件。总之,如果是在最为广义地进行理解的前提下,要在 TFT 阵列基板 10 上构筑的由不透明的材料构成的构成,则可以叫做‘上侧遮光膜’或‘内置遮光膜’。

在以上所说明的上述数据线 6a 上,而且,在屏蔽层 400 的下边,形成 NSG、PSG、BSG、BPSG 等硅酸盐玻璃膜、氮化硅膜或氧化硅膜等,或者理想地说形成用使用 TEOS 气体的等离子体 CVD 法形成的第 3 层间绝缘膜 43。在该第 3 层间绝缘膜 43 上,分别形成用来把上述屏蔽层 400 和屏蔽层用中继层 6a1 电连起来的接触孔 803,和用来把第 3 中继层 402 和第 2 中继层 6a2 电连起来的接触孔 804 的开孔。

另外,对于第 2 层间绝缘膜 42 来说,也可以作为采用不进行对于第 1 层间绝缘膜 41 所说的那样的烘焙的办法,实现在电容器电极 300 的界面附近产生的应力的缓和。

最后,在第 6 层上,如上述地矩阵状地形成像素电极 9a,在该像素电极 9a 上形成取向膜 16。此外,在该像素电极 9a 的下边,可以形成 NSG、PSG、BSG、BPSG 等硅酸盐玻璃膜、氮化硅膜或氧化硅膜等,或者理想地说形成由 BPSG 构成的第 4 层间绝缘膜 44。在该第 4 层间绝缘膜 44 上,形成用来把像素电极 9a 和上述第 3 中继层 402 间电连起来的接触孔 89 的开孔。

此外,在本实施形态中,特别是第4层间绝缘膜44的表面,已用CMP(化学机械研磨)处理等进行了平坦化,以减少起因于在其下方存在的各种布线或元件形成的台阶的液晶层50的取向不良。但是,也可以采用在TFT阵列基板10、基底绝缘膜12、第1层间绝缘膜41、第2层间绝缘膜42和第3层间绝缘膜43中的至少一者上挖沟,埋入数据线6a等的布线或TFT30等的办法,进行平坦化处理,来取代像上述那样地对第4层间绝缘膜4施行平坦化处理。

在作为这样的构成的本实施形态的电光装置中,特别是作为第2层,存在着被形成为与栅电极3a同一膜的中继层719,而且,位于第3层上的存储电容器70的下部电极71和位于第6层上的像素电极9a,通过该中继层719电连起来,这是该电光装置的特征。

如上述,下部电极71和像素电极9a,从它们每一者来看,由于通过位于更下层的中继层719连接起来,故结果变成为该中继层719和下部电极71之间的电连接点,特别是着眼于下部电极71时的电连接点,位于该下部电极71的下侧(参看图4中的接触孔881)。

倘采用这样的结构,结果就变成为在本实施形态的电光装置中,可以得到如下的作用效果。就这一点来说,如果设想不采用上述那样的结构的电光装置,进行与上述电光装置的对比,则更为明了。以下,边参看图5边对之进行说明。在这里,图5是示出了目的为进行与图4的对比的结构的同一视点的剖面图。另外,为了便于说明,决定在图4和图5间,在实质上指示同一要部的情况下,用同一标号进行说明。另外,该对比例不过是先前的实施形态的对比,该构成也包括在本发明内。

首先,在图4中,就如已经说明的那样,下部电极71和中继层719,通过在两者间形成的第1层间绝缘膜41上形成了开孔的接触孔881电连起来。因此,在下部电极71上的对中继层719的电连接点,可以说就位于该下部电极71的‘下侧’。

相对于此,在图5中,不存在中继层719,因此,下部电极71’与像素电极9a之间的电连接,可通过在该下部电极71’的上侧具有电连接点的接触孔8821实现。说得更为详细一点,可知接触孔8821已在第2层间绝缘

膜 42 和电介质膜 75a、75b 上形成了开孔，第 2 中继层 6a21 则被形成使得把该第 2 层间绝缘膜 42 的表面和接触孔 8821 埋起来。至于以后的更为上层的结构与图 4 大体上是同样的。

因此，倘采用这样的结构，为了实现下部电极 71' 与像素电极 9a 之间的电连接，由图 5 可知，就必须利用下部电极 71' 的 '上侧'。此外，与此同时，在该情况下，必须 '仅仅' 实施对构成存储电容器 70' 的电介质膜 75 和电容器电极 300 的刻蚀工序 (参看图中的虚线)。因为为了要实现与下部电极 71' 的上侧之间的电连，就必须表现出从上方看该下部电极 71' 的表面那样的状态。

但是，上述那样的刻蚀工序伴有很大的困难。之所以这么说，是因为下部电极 71' 或电介质膜 75 已被形成使得变成通常所可能达到的厚度那么薄。此外，在本实施形态中，特别是电介质膜 75，如上述含有氮化硅膜等，因此氧化硅膜就要变薄一个相应的量。例如在用多晶硅或钨硅化物、或它们的叠层膜形成电容器电极 300 时，电容器电极 300 的刻蚀就可以作为使得本身为电介质膜的氧化硅膜的刻蚀速率选择比电容器电极 300 的刻蚀速率更慢的刻蚀条件，并用电介质膜阻止电容器电极 300 的刻蚀。但是，当电介质膜中的氧化硅膜变薄后，刻蚀就会穿透电介质膜，此外，像素电极一侧电容器电极也将容易地进行刻蚀。因此，在这样的情况下，在下部电极 71' 中，产生所谓的 '穿透' 等的可能性很大。这样的话，在不好的情况下，就产生了在构成存储电容器 70 的电容器电极 300 和下部电极 71' 之间产生短路的可能性。

然而，在本实施形态中，如图 5 所示，由于完全没必要经由这样的困难的刻蚀工序，故可以良好地实现下部电极 71 和像素电极 9a 间的电连。这是由于通过中继层 719 实现了两者间的电连的缘故。再说，出于同样的理由，倘采用本实施形态，则在电容器电极 300 和下部电极 71 之间产生短路等的可能性极小。就是说，可以满意地形成无缺陷的存储电容器 70。

如上述，在本实施形态中，由于在可以良好地实现存储电容器 70 与像素电极 9a 间的电连的同时，还可以极大地降低在存储电容器 70 上产生无用的缺陷的可能性，故可以提供可进行更好的工作的电光装置。

另外，在上述实施形态中，中继层 719，虽然被形成为与栅电极 3a 同一膜，但是本发明并不限于这样的实施形态。例如，在上述实施形态中，由于也可以考虑出于种种的原因把在第 3 层上形成的存储电容器 70 形成在更上层的情况，故在该情况下，可以想像使中继层位于比栅电极 3a 更往上的上层的情况。此外，至于各个构成要部的立体的、平面的布局，本发明也并不限于上述实施形态那样的形态。可以考虑与图 1 到图 4 等不同的种种的形态。

此外，在上述中，存储电容器 70 虽然作成为从下边开始依次为像素电位侧电容器电极、电介质膜和固定电位侧电容器电极这样的 3 层结构，但是，在有的情况下也可以构成与之颠倒过来的结构。在该情况下，例如，把作为上部电极的像素电位侧电容器电极形成为使得具有比固定电位侧电容器电极的面积更大的面积，就是说被形成为使得前者对后者具有平面性的剩余的面，同时，可把该剩余的面配置为使得与通往中继层 719 的接触孔的形成位置相对应。这样的话，中继层 719 与像素电位侧电容器电极的电连，就可以借助于该接触孔容易地实现。

如上述，在本发明中所说的‘像素电位侧电容器电极’，也可以作成为使得构成存储电容器 70 的上部电极而不构成其‘下部’电极 71(参看上述实施形态)。

(制造工艺)

以下，边参看图 6 和图 7 边说明与上述实施形态类似的电光装置的制造方法。在这里，图 6 和图 7，是按照工序顺序示出了本实施形态的电光装置的制造方法的工序剖面图。

首先，如图 6 的工序(1)所示，准备石英基板、硬玻璃、硅基板等的 TFT 阵列基板 10。在这里，理想的是要先在 N_2 (氮气)等的惰性气体气氛中用约 900 到 1300℃ 的高温进行退火处理，然后，进行前处理，以减少在要实施的高温工序中在 TFT 阵列基板 10 上产生的变形。

接着，在经过了这样的处理的 TFT 阵列基板 10 的整个面上，借助于溅射法，把 Ti、Cr、W、Ta、Mo 等的金属或金属硅化物等的金属合金膜形成膜厚 100 到 500nm 左右，理想的是 200nm 的膜厚的前驱膜。然后，借助于

光刻和刻蚀,形成平面形状为条带状的扫描线 11a。其次,在扫描线 11a 上,例如,用常压或减压 CVD 法等,用 TEOS(四乙氧基硅烷)气体、TEB(硼酸四乙酯)气体、TMOP(正磷酸三甲酯)气体等,形成由 NSG(无掺杂硅酸盐玻璃)、PSB(磷硅酸盐玻璃)、BSG(硼硅酸盐玻璃)、BPSG(硼磷硅酸盐玻璃)等的硅酸盐玻璃膜,氮化硅膜或氧化硅膜等构成的基底绝缘膜 12。该基底绝缘膜 12 的膜厚,例如作为约 500 到 2000nm 左右。

接着,在基底绝缘膜 12 上,在约 450 到 550℃,理想的是在约 500℃左右的比较低的低温环境中,借助于使用流量约 400 到 600cc/min 的甲硅烷气体、乙硅烷气体等的减压 CVD(例如,压力约 20 到 40Pa 的 CVD),形成无定形硅膜。然后,采用在氮气气氛中,在约 600 到 700℃下,进行约 1 到 10 个小时,理想的是 4 到 6 个小时的热处理的办法,使 p-Si(多晶硅)膜进行固相生长,一直到变成为约 50 到 200nm 的厚度,理想的是变成为约 100nm 的厚度为止。作为使之进行固相生长的方法,既可以是使用 RTA 的退火处理,也可以是使用受激准分子激光等的激光退火。这时,也可以根据究竟要把像素开关用的 TFT30 作为 n 沟型还是 p 沟型,借助于离子注入等少量地掺入 V 族或 III 族元素的杂质。然后,借助于光刻和刻蚀,形成具有规定图形的半导体层 1a。

其次,如图 6 的工序(2)所示,借助于 900 到 1300℃的温度,理想的是约 1000℃的温度使构成 TFT30 的半导体层 1a 热氧化以形成下层的栅绝缘膜,在有的情况下,还要采用接在其后边用减压 CVD 法等形成上层栅绝缘膜的办法,形成一层或多层的高温氧化硅膜(HTO)或氮化硅膜构成的(含有栅绝缘膜)的绝缘膜 2。其结果是,半导体层 1a 变成为约 30 到 150nm 的厚度,理想的是变成为约 35 到 50nm 的厚度,绝缘膜 2 的厚度则变成为约 20 到 150nm,理想的是变成为约 30 到 100nm 的厚度。

接着,为了控制像素开关用的 TFT30 的阈值电压 V_{th} ,借助于离子注入等,向半导体层 1a 之内 n 沟道区或 p 沟道区掺入恰好预先设定好的规定量的硼等的杂质。

接着,对上述基底绝缘膜 12,形成通往扫描线 11a 的沟 12cv。该沟 12cv 要借助于反应性离子刻蚀、反应性离子束刻蚀等干法刻蚀形成。

其次,如图6的工序(3)所示,借助于减压CVD法等淀积多晶硅膜,然后使磷(P)进行热扩散,使该多晶硅膜导电化。也可以不使用该热扩散而代之以使用在多晶硅膜的成膜的同时导入P离子的掺杂硅膜。该多晶硅膜的膜厚约为100到500nm,理想的是约350nm左右。然后,借助于光刻和刻蚀,含有TFT30的栅电极部分在内地形成规定的图形的栅电极3a。因此,在本制造方法中,结果就变成为在该栅电极3a的形成时,还同时形成延长设置在其上的侧壁部分3b。该侧壁部分3b可采用也对沟12cv的内部施行上述的多晶硅膜的淀积的办法形成。这时,采用使该沟12cv的底与扫描线11a接连的办法,结果就变成为侧壁部分3b和扫描线11a进行电连。此外,在本制造方法中,特别是在该栅电极3a的图形化时,结果变成为可与之同时也形成中继层719。借助于图形化,中继层719就被形成为具有图2所示的那样的平面形状。

接着,对上述半导体层1a,形成低浓度源区1b和低浓度漏区1c,以及高浓度源区1d和高浓度漏区1e。

在这里,说明把TFT30变成为具有LDD结构的n沟型的TFT的情况。具体地说首先为了形成低浓度源区1b和低浓度漏区1c,以栅电极3a为掩模,以低浓度(例如,使P离子变成为 1 到 $3 \times 10^{13}/\text{cm}^2$ 的剂量)掺入P等的V族元素,借助于此,栅电极3a下边的半导体层1a就变成为沟道区1a'。这时,采用使栅电极3a起着掩模的作用的办法,结果就变成为可以自我对准地形成低浓度源区1b和低浓度漏区1c。

其次,为了形成高浓度源区1d和高浓度漏区1e,在栅电极3a上形成具有比栅电极3a还宽的平面图形的光刻胶层。然后,以高浓度(例如,使P离子为 1 到 $3 \times 10^{15}/\text{cm}^2$ 的剂量)掺入P等的V族元素杂质。

另外,也可以不像这样地分成低浓度和高浓度这2个阶段进行掺杂。例如,既可以不进行低浓度的掺杂地作为补偿(offset)结构的TFT,也可以以栅电极3a(栅电极)为掩模,借助于使用P离子·B离子等的离子注入技术作为自我对准型的TFT。借助于该杂质的掺杂还可以使栅电极3a进一步低电阻化。

其次,如图6的工序(4)所示,在栅电极3a上,例如借助于使用TEOS

气体、TEB 气体、TMOP 气体等的常压或减压 CVD 法等，形成由 NSG、PSG、BSG、BPSG 等的硅酸盐玻璃膜、氮化硅膜或氧化硅膜构成的第 1 层间绝缘膜 41。该第 1 层间绝缘膜 41 的膜厚，例如作为约 500 到 2000nm 左右。在这里理想的是要预先用 800℃ 左右的高温进行退火处理，提高第 1 层间绝缘膜 41 的膜质。

接着，借助于对第 1 层间绝缘膜 41 的反应性离子刻蚀、反应性离子束刻蚀等的干法刻蚀，形成接触孔 83 和接触孔 881 的开孔。这时，要分别形成为使得前者通往半导体层 1a 的高浓度漏区 1e，后者通往中继层 719。

其次，如图 6 的工序 (5) 所示，在第 1 层间绝缘膜 41 上，借助于溅设法，使 Pt 等的金属膜成膜为 100 到 500nm 左右的膜厚，形成具有规定图形的下部电极 71 的前驱膜。这时，上述的金属膜的成膜，要形成为使得把接触孔 83 和接触孔 881 这两者填埋起来，借助于此，就可以实现高浓度漏区 1e 和中继层 719 与下部电极 71 之间的电连。接着，采用实施对该下部电极 71 的前驱膜的图形化处理的办法，形成下部电极 71。

接着，在下部电极 71 上，形成电介质膜 75。该电介质膜 75，与绝缘膜 2 的情况同样，一般地说可用在形成 TFT 栅绝缘膜时使用的各种众所周知的技术形成。在本实施形态中，特别是首先用上述的热氧化或 CVD 法等形成氧化硅膜 75a，然后，用等离子体 CVD 法等形成氮化硅膜 75b。由于该电介质膜 75 越薄则存储电容器 70 就变得越大，故结局是以不产生膜破裂等的缺陷为条件把该电介质膜 75 形成为使得变成为膜厚 50nm 以下的极其薄的绝缘膜是有利的，接着，在电介质膜 75 上，借助于溅设法，使 Al 等的金属膜成膜为约 100 到 500nm 左右的膜厚，以形成电容器电极 300 的前驱膜。

其次，如图 6 的工序 (6) 所示，可以作成为把氮化硅膜 75b 的前驱膜形成为比像素电位侧电容器电极的下部电极 71 稍大一点的尺寸，对电容器电极 300 的前驱膜仅仅实施使之变成为与下部电极 71 大体上同一大小的图形化，而不实施对电介质膜 75 的氧化硅膜 75a 的前驱膜的图形化。在该情况下，结果变成为伴随着电容器电极 300 的形成，被该电容器电极 300 和上述下部电极 71 所挟持的部分，实质上就相当于电介质膜 75 (参看图 4)。

另外，在图7的工序(6)中，也可以采用一举地使上述的电介质膜75的前驱膜和电容器电极300的前驱膜图形化的办法，形成电介质膜75和电容器电极300，完成存储电容器70。

如上述，在本实施形态中，由于采用把作为固定电位侧电容器电极的电容器电极300的面积，形成为使得比作为像素电位侧电容器电极的下部电极71和电介质膜75的面积更大的办法形成该存储电容器70，故可以用更宽的电极面积挟持电介质膜，具体地说，可以把构成该存储电容器70的3个要部的侧面也用做电容器，因而可以期待由此产生的电容值的增大。就是说，倘采用本实施形态，则可以制造具有比较大的电容值的存储电容器，而不会具有无用的平面性的扩展，就是说不会使像素开口率降低。从这样的观点看，例如，只要预先把下部电极71形成得比较厚，则可以增大上述侧面的面积，可以效率良好地得到电容值。此外，就如由图可以看明白的那样，如果预先作成这样的形态，由于把电介质膜75形成为把下部电极71覆盖起来，故也可以减少产生电容器电极300和下部电极71间的短路的可能性。

此外，倘采用本形态，由于要实施上述那样的图形化，故不会具有像现有技术那样仅仅刻蚀固定电位侧电容器电极及电介质膜使位于其下的像素电位侧电容器电极保持原状地残留下来这样的困难的课题。其结果是，若使用本发明，则可以容易地且可靠性高地制造存储电容器。

其次，如图7的工序(7)所示，例如，借助于使用TEOS气体等的常压或减压CVD法，理想的是用等离子体CVD法，形成由NSG、PSG、BSG、BPSG等的硅酸盐玻璃膜、氮化硅膜或氧化硅膜等构成的第2层间绝缘膜42。在把电容器电极300使用铝的情况下，就必须用等离子体CVD进行低温成膜。该第2层间绝缘膜42的膜厚，例如，作成为约500到1500nm左右。接着，借助于对第2层间绝缘膜42的反应性离子刻蚀、反应性离子束刻蚀等的干法刻蚀，使接触孔81、801和882形成开孔。这时，分别形成为使得接触孔81通往半导体层1a的高浓度源区1d，使得接触孔801通往电容器电极300，使得接触孔882通往中继层719。

接着，如图7的工序(8)所示，向第2层间绝缘膜42上的整个面上，借

助于溅设法等,作为金属膜,淀积遮光性的Al等的低电阻金属或金属硅化物等,厚度为约100到500nm左右,理想的是约300nm。然后,借助于光刻和刻蚀,形成具有规定图形的数据线6a。这时,在该图形化时,也同时形成屏蔽层用中继层6a1和第2中继层6a2。屏蔽层用中继层6a1,在被形成为把接触孔801覆盖起来的同时,第2中继层6a2被形成为把接触孔882覆盖起来。接着,在它们的上层的整个面上用等离子体CVD法等形成了由氮化钛构成的膜后,使之仅仅在数据线6a上剩下来那样地实施图形化处理(参看图7的工序(8)中的标号41TN)。但是,既可以形成为使得在屏蔽层用中继层6a1和第2中继层6a2上也剩下由该氮化钛构成的层,在有的情况下,也可以形成为使得对于TFT阵列基板10的整个面上都剩下该层。此外,还可以在铝的成膜时同时成膜以一揽子地进行刻蚀(这一点,结果变成成为构成与图4有一些不同)。

其次,如图7的工序(9)所示,例如借助于使用TEOS气体等的常压或减压CVD法,理想的是借助于可以低温成膜的等离子体CVD法,使得把数据线6a等上覆盖起来那样地,形成由NSG、PSG、BSG、BPSG等的硅酸盐玻璃膜、氮化硅膜或氧化硅膜等构成的第3层间绝缘膜43。该层间绝缘膜43的膜厚,作成为例如约500到1500nm左右。接着,借助于对第3层间绝缘膜43的反应性离子刻蚀、反应性离子束刻蚀等的干法刻蚀使接触孔803和804形成开孔。这时,结果变成为要把接触孔803形成为通往上述屏蔽层用中继层6a1,把接触孔804形成为通往第2中继层6a2。

接着,在第3层间绝缘膜43上,用溅设法,或等离子体CVD法等,形成屏蔽层400。这里首先在第3层间绝缘膜43的正上方,形成用例如铝等的低电阻材料形成第1层,接着,在该第1层上,用例如氮化钛等构成其它后述的像素电极9a的ITO和不产生电蚀的材料形成第2层,最后,采用以第1层和第2层为基础进行图形化的办法,形成具有2层结构的屏蔽层400。另外,这时,与屏蔽层400一起,还同时形成第3中继层402。

接着,例如借助于使用例如TEOS气体等的常压或减压CVD法,形成由NSG、PSG、BSG、BPSG等的硅酸盐玻璃膜、氮化硅膜或氧化硅膜等构成的第4层间绝缘膜44。该第4层间绝缘膜44的膜厚,例如作成为约500到

1500nm 左右。接着,借助于对第 4 层间绝缘膜 44 的反应性离子刻蚀、反应性离子束刻蚀等的干法刻蚀使接触孔 89 形成开孔。这时,结果变成为把接触孔 89 形成为通往上述第 3 中继层 402。

接着,向第 4 层间绝缘膜 44 上,借助于溅设法等淀积厚度约 50 到 200nm 的 ITO 膜等的透明导电性膜。然后,借助于光刻和刻蚀,形成像素电极 9a。另外,在把该电光装置用做反射式的情况下,也可以用 Al 等的反射率高的不透明的材料形成像素电极 9a。接着,在向像素电极 9a 上,涂敷上聚酰亚胺系的取向膜的涂敷液之后,借助于使之具有规定的预倾斜角那样地,而且以规定方向实施研磨处理等,形成取向膜 16。

另一方面,就对向基板 20 来说,首先准备玻璃基板等,在作为框缘的遮光膜,例如溅设上金属铬之后,经由光刻和刻蚀后形成。另外,这些遮光膜没有必要是导电性的,除去 Cr、Ni、Al 等的金属材料外,也可以用使碳或 Ti 分散到光刻胶内的树脂黑等的材料形成。

然后,借助于溅设处理等,向对向基板 20 的整个面上淀积厚度约 50 到 200nm 的 ITO 等的透明导电性膜,借助于此,形成对向电极 21。然后,在向对向电极 21 的整个面上涂敷上聚酰亚胺系的取向膜的涂敷液之后,借助于使之具有规定的预倾斜角那样地,而且以规定方向实施研磨处理等,形成取向膜 22。

最后,如上述,使得取向膜 16 和 22 对向那样地用密封材料把已形成了各层的 TFT 阵列基板 10 和对向基板 20 粘贴到一起,借助于真空吸引等,向两个基板间的空间内采用吸引使例如多种的向列液晶混合起来形成的液晶的办法,形成规定层厚的液晶层 50。

借助于以上所说明的制造工艺,就可以制造上述的实施形态的电光装置。

另外,在上述中,存储电容器 70,虽然被制造为在首先形成了下部电极 71 后,再形成电介质膜 75 和电容器电极 300,但是,本发明也可以不这样,而代之以在形成了下部电极 71、电介质膜 75 和电容器电极 300 各自的前驱膜后,借助于对于它们的的同时的图形化处理来形成。

(电光装置的全体构成)

以下,参看图8和图9说明像以上那样地构成的本实施形态的电光装置的全体构成。另外,图8是与在TFT阵列基板上形成的各个构成要部一起,从对向基板20的一侧看该TFT阵列基板的平面图,图9是图8的H-H'剖面图。

在图8和图9中,在本实施形态的电光装置中,TFT阵列基板10和对向基板20对向配置。在TFT阵列基板10和对向基板20之间已封入了液晶层50,TFT阵列基板10和对向基板20,借助于设置在位于图像显示区域10a的周围的密封区域上的密封材料52彼此粘接起来。

密封材料52,为了把两个基板粘接起来,由例如紫外线硬化树脂、热硬化树脂等构成,可借助于紫外线、加热等使之硬化。此外,在该密封材料52中,如果本实施形态的电光装置是用于液晶装置是像投影仪用途那样小型且进行扩大显示的液晶装置,则散布有目的为使两基板间的距离(基板间间隙)变成为规定值的玻璃纤维或玻璃微珠等的间隙材料(衬垫材料)。或者,如果该电光装置是用于液晶显示器或液晶电视那样地大型且进行等倍显示的液晶装置,则在液晶层50中可以含有这样的间隙材料。

在密封材料52的外侧的区域中,采用用规定的定时向数据线6a供给图像信号的办法,沿着TFT阵列基板10的一边设置驱动该数据线6a的数据线驱动电路101和外部电路连接端子102,采用以规定的定时向扫描线11a和栅电极3a供给扫描信号的办法,沿着与该一边邻接的2边设置驱动栅电极3a的扫描线驱动电路104。

另外,若供往扫描线11a及栅电极3a的扫描信号延迟不会成为问题,则也可以仅仅在单侧设置扫描线驱动电路104,这是不言而喻的。此外,也可以沿着图像显示区域10a的边在两侧排列数据线驱动电路101。

在TFT阵列基板10的剩下的一边上,设置用来把设置在图像显示区域10a的两侧的扫描线驱动电路104间连接起来的多条布线105。

此外,在对向基板20的拐角部分中的至少一个地方上,设置在TFT阵列基板10和对向基板20间电导通用的导通构件106。在图9中,在TFT阵列基板10上,在形成像素开关用的TFT、扫描线、数据线等的布线后的像素电极9a上,形成取向膜。另一方面,在对向基板20上,除去对向电

极 21 之外,在最上层部分上还形成有取向膜。此外,液晶层 50,例如由把 1 种或数种的向列液晶混合起来的液晶构成,在这些一对的取向膜间,形成规定的取向状态。

另外,在 TFT 阵列基板 10 上,除去这些个数据线驱动电路 101、扫描线驱动电路 104 等之外,也可以形成以规定的定时向多条数据线 6a 施加图像信号的采样电路,先于图像信号分别向多条数据线 6a 供给规定的电压水平的预充电信号的预充电电路,用来在制造途中或出厂时检查该电光装置的品质,缺陷等的检查电路等。

另外,在上述的各个实施形态中,也可以不在 TFT 阵列基板 10 上设置数据线驱动电路 101 和扫描线驱动电路 104,而代之以例如通过 TFT 阵列基板 10 的周边部分上设置的各向异性导电薄膜把数据线驱动电路 101 和扫描线驱动电路 104 电连和机械连接到例如已装配到 TAB(带载自动键合)基板上的驱动用 LSI 上。此外,还可以在要入射对向基板 20 的投影光的一侧和要出射 TFT 阵列基板 10 的出射光的一侧上,分别与例如 TN(扭曲向列)模式、VA(垂直排列)模式、PDLC(聚合物分散液晶)模式等的工作模式,或常态白色模式 常态黑色模式的区别相对应地,以规定的方向配置偏振薄膜、相位差薄膜和偏振板等。

(电子设备)

其次,对本身为把以上详细地说明的电光装置用做光阀的电子设备的一个例子的投影式彩色显示装置的实施形态,对其全体构成、特别是光学上的构成,进行说明。在这里,图 10 是投影式彩色显示装置的图示性的剖面图。

在图 10 中,本身为本实施形态的投影式彩色显示装置的一个例子的液晶投影仪 1100 的构成为:准备 3 个含有在 TFT 阵列基板上装载有驱动电路的液晶装置的液晶模块,分别用做 RGB 用的光阀 100R、100G、100B。在液晶投影仪 1100 中,当从金属卤素灯泡等的白色光源的灯泡单元 1102 发出投影光后,借助于 3 块的反射镜 1106 和 2 块的分色镜 1108,分成与 RGB 的 3 原色对应的光成分 R、G 和 B,并分别导入与各色对应的光阀 100R、100G 和 100B 内。这时特别是 B 光,为了防止因光路长所带来的光损耗,要通过

由入射透镜 1122、中继透镜 1123 和出射透镜 1124 构成的中继透镜系统 1121 导入。然后，与分别用光阀 100R、100G 和 100B 进行调制后的 3 原色对应的光成分，借助于分色镜 1112 再次合成后，通过投影透镜 1114 作为彩色图像被投影到屏幕 1120 上。

本发明并不限于上述的实施形态，在不违背从技术方案的范围和说明书全体中可能读到的发明的要旨或思想的范围内，适宜变更是可能的，伴随着这样的变更的电光装置和其制造方法及电子设备也包括在本发明的技术范围内。作为电光装置，可以在电泳装置或 EL 装置或使用电子发射元件的装置等中应用。

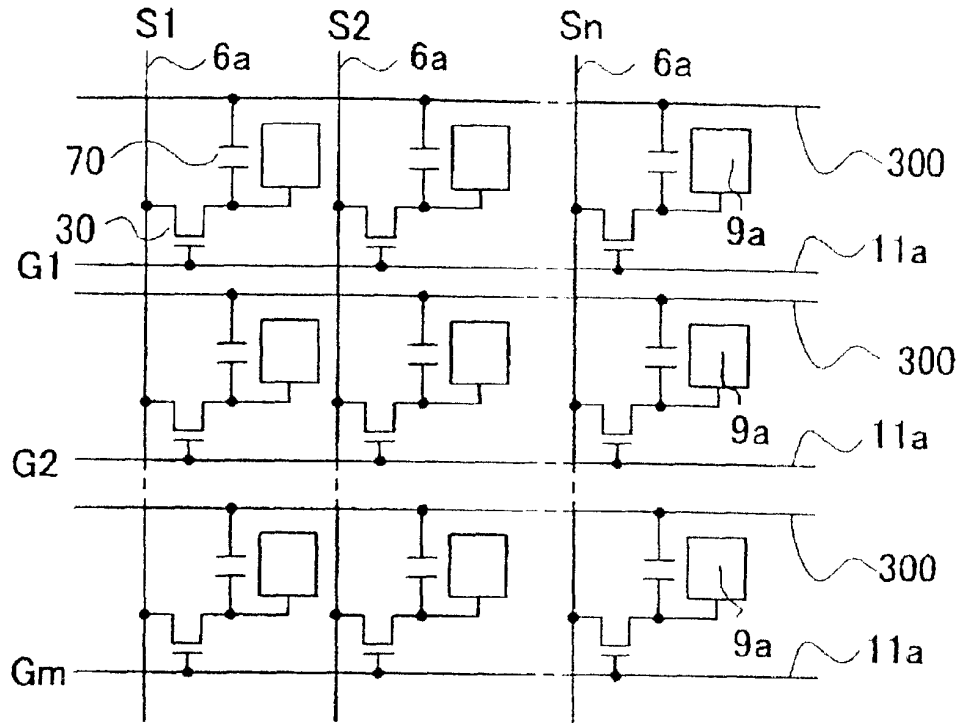


图 1

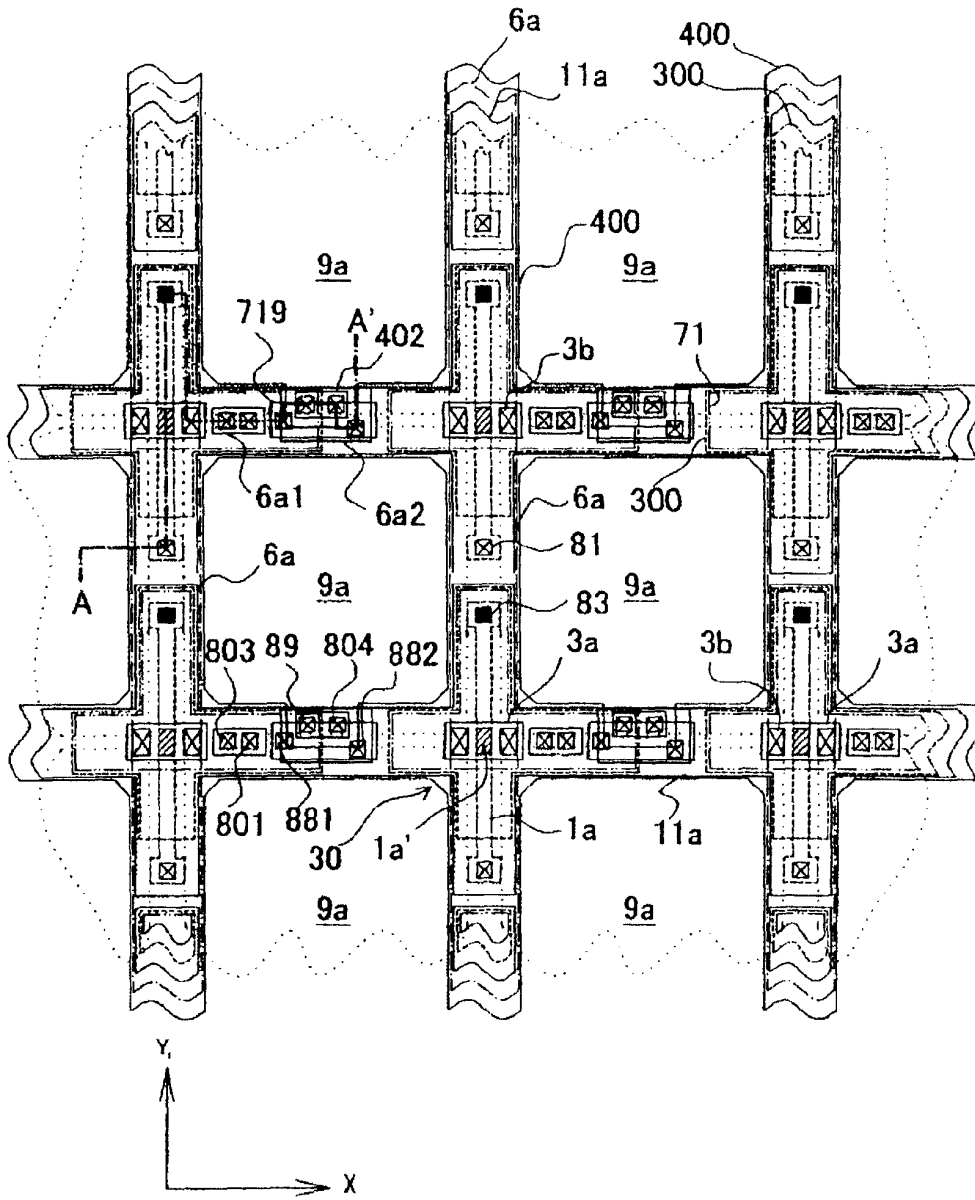


图 2

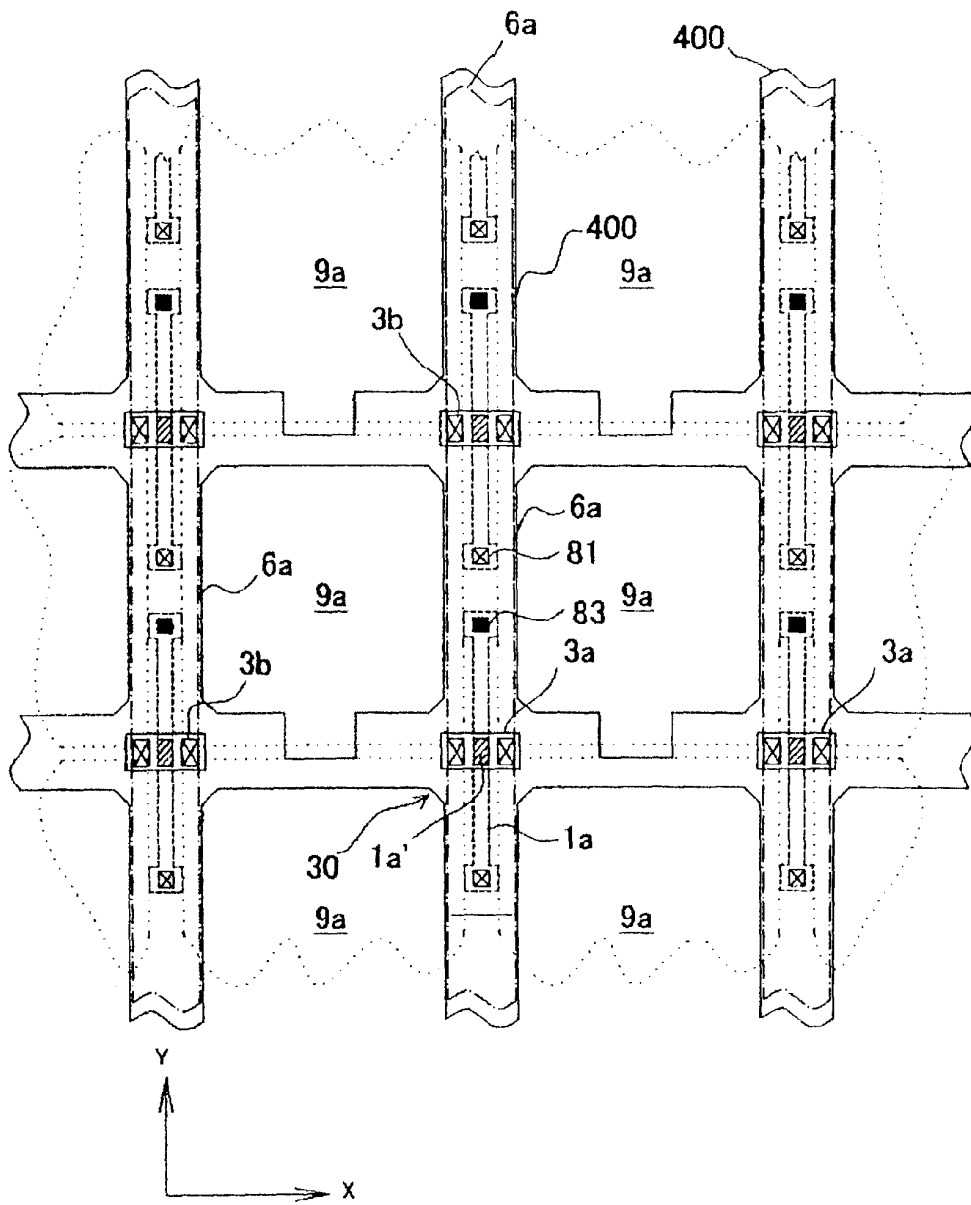
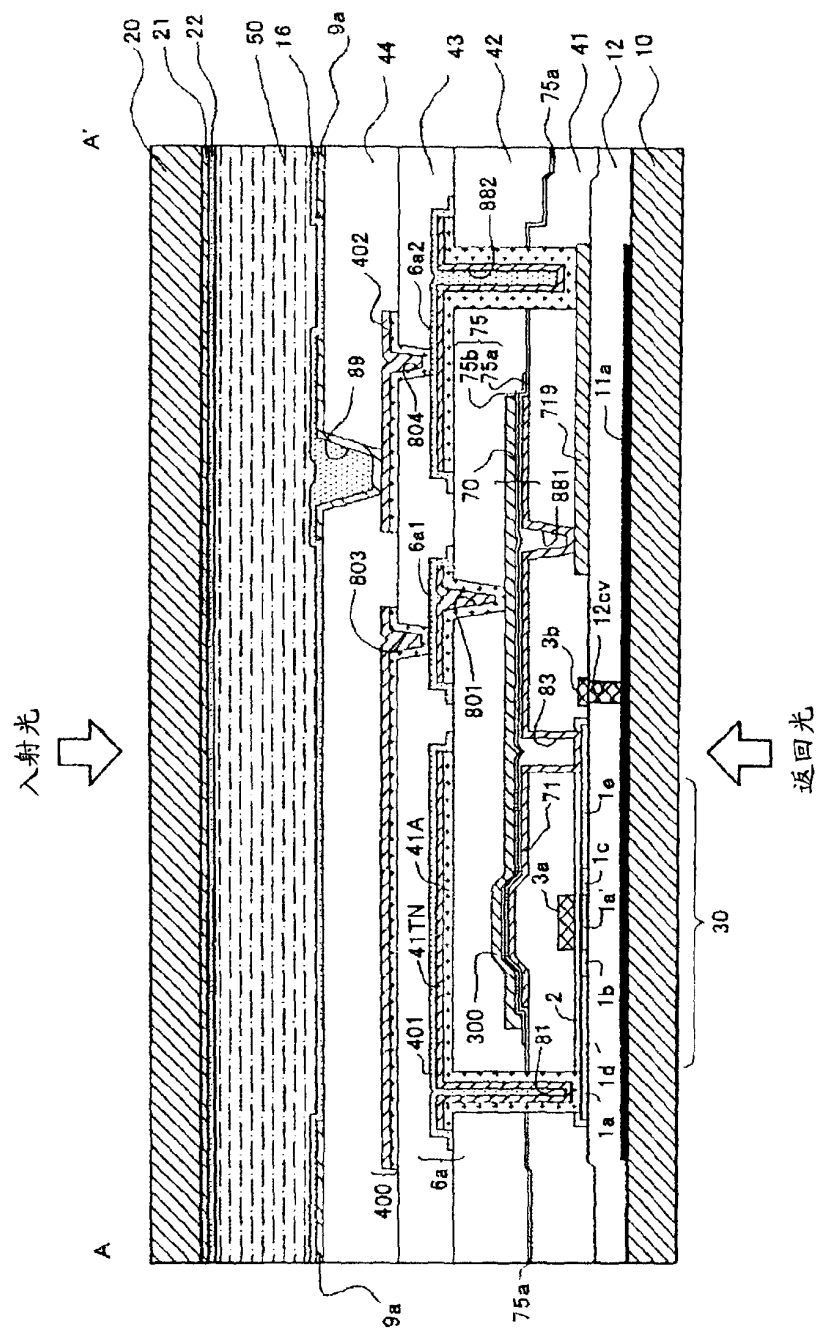
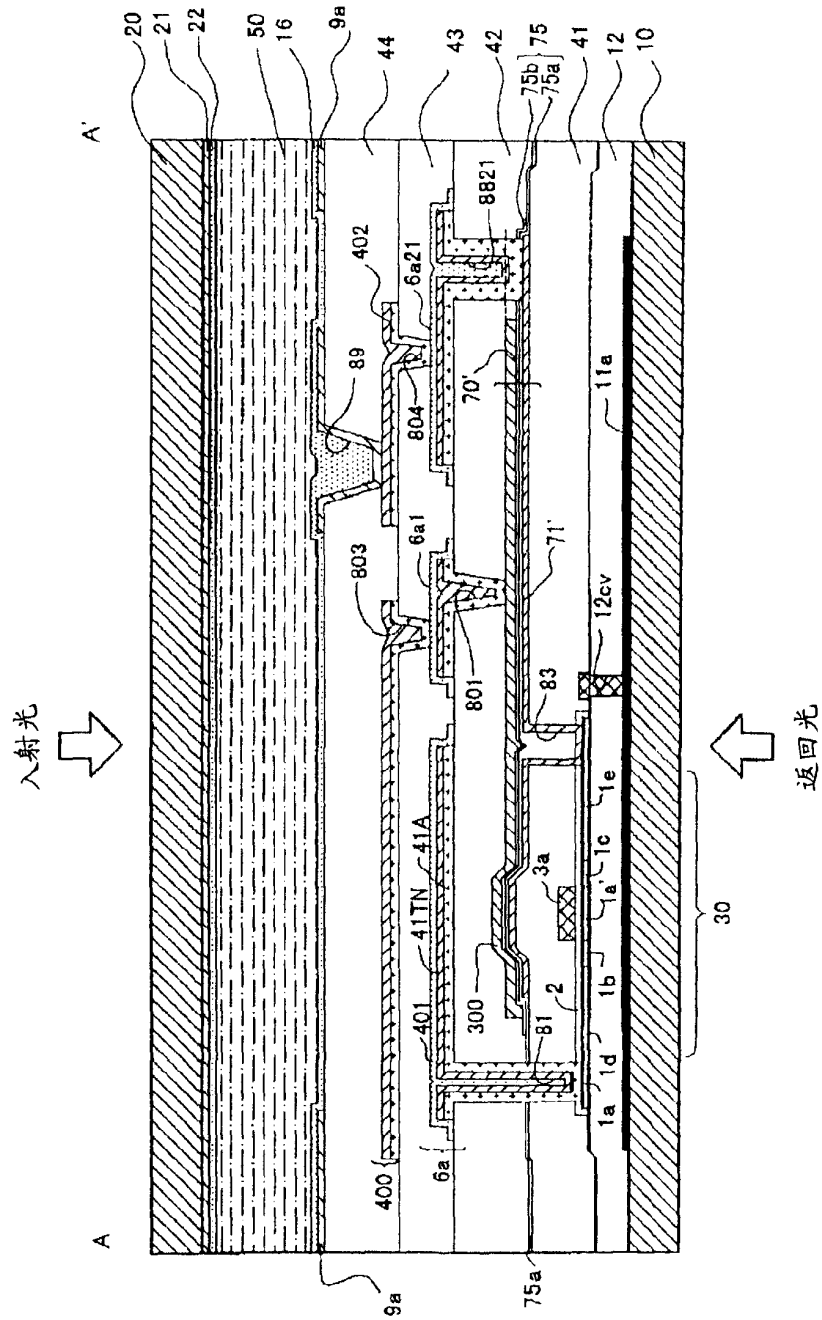
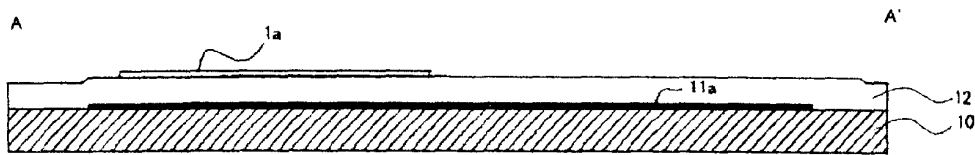


图 3

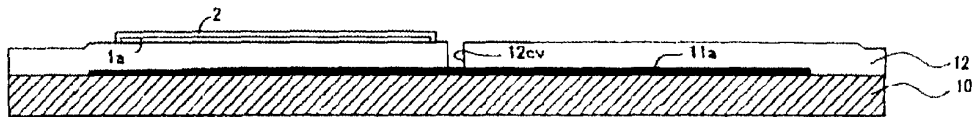
4
图



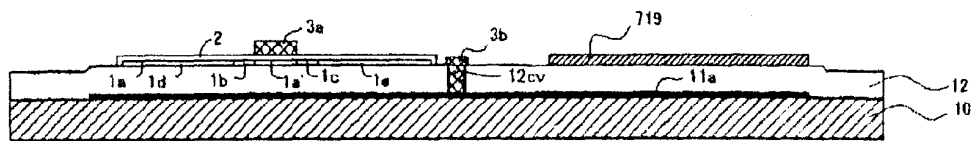
工序(1)



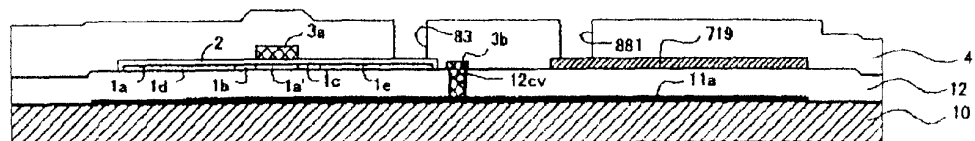
工序(2)



工序(3)



工序(4)



工序(5)

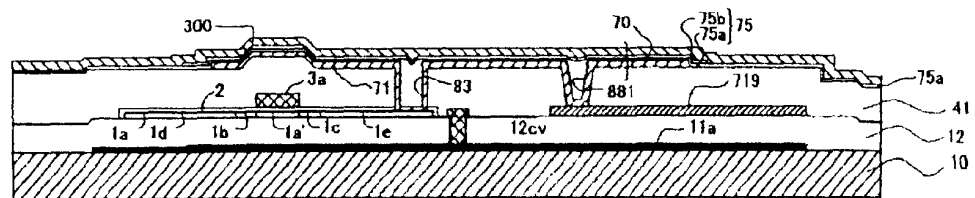
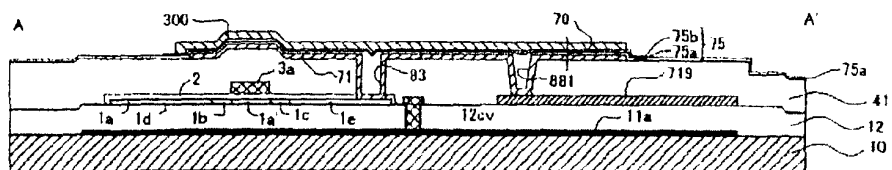
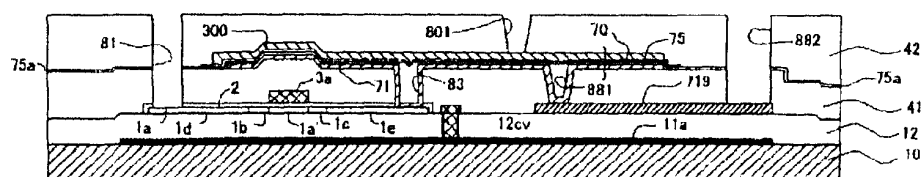


图 6

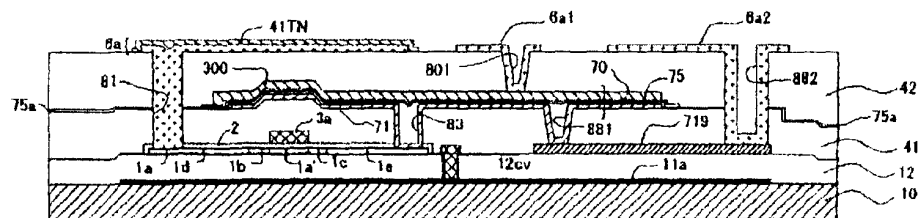
工序(6)



工序(7)



工序 (8)



工序 (9)

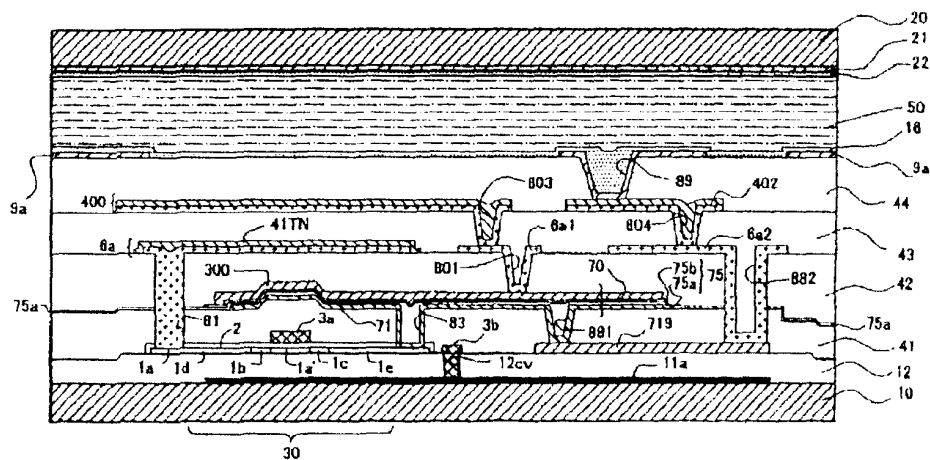


图 7

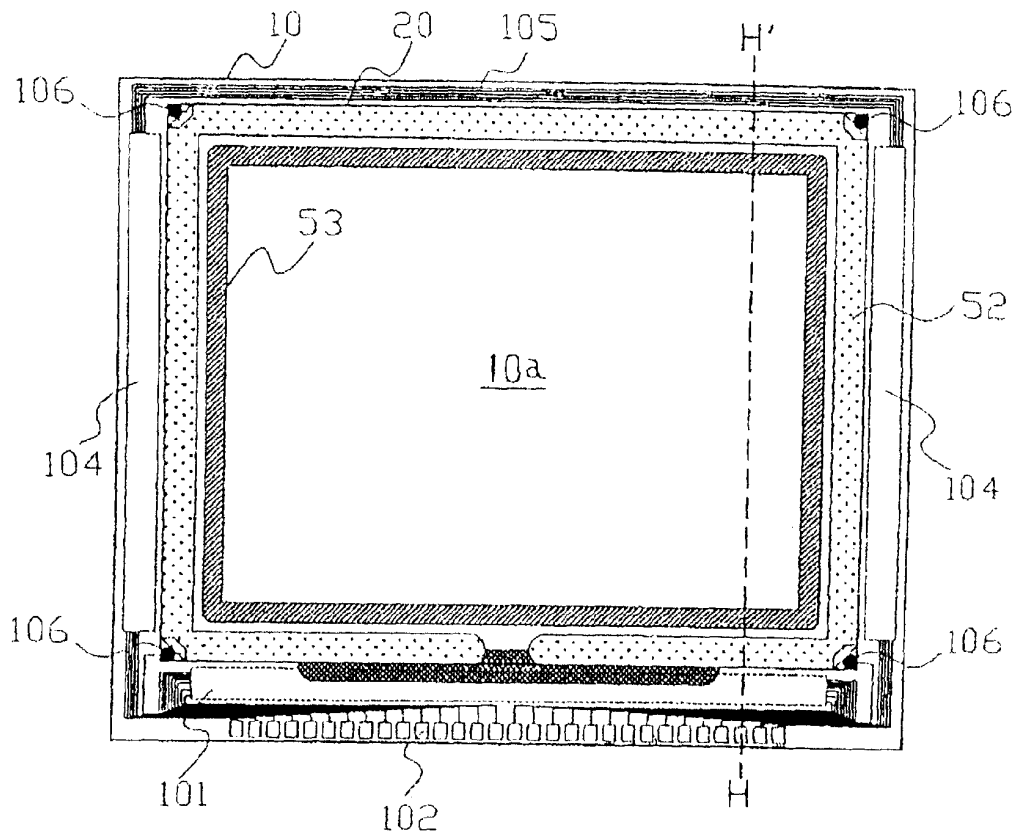


图 8

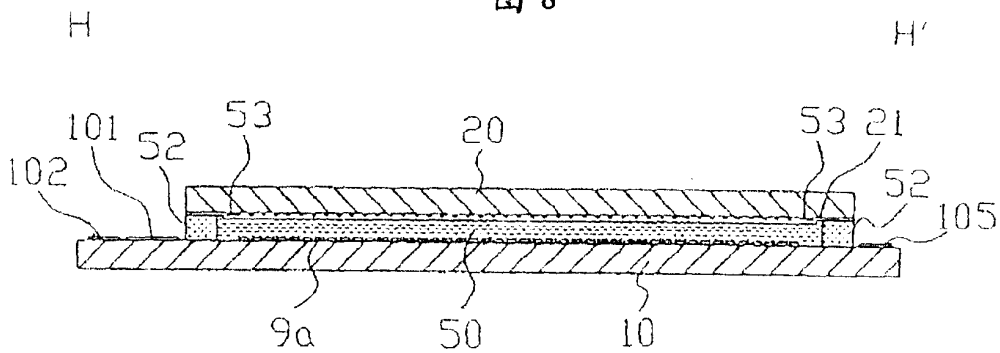


图 9

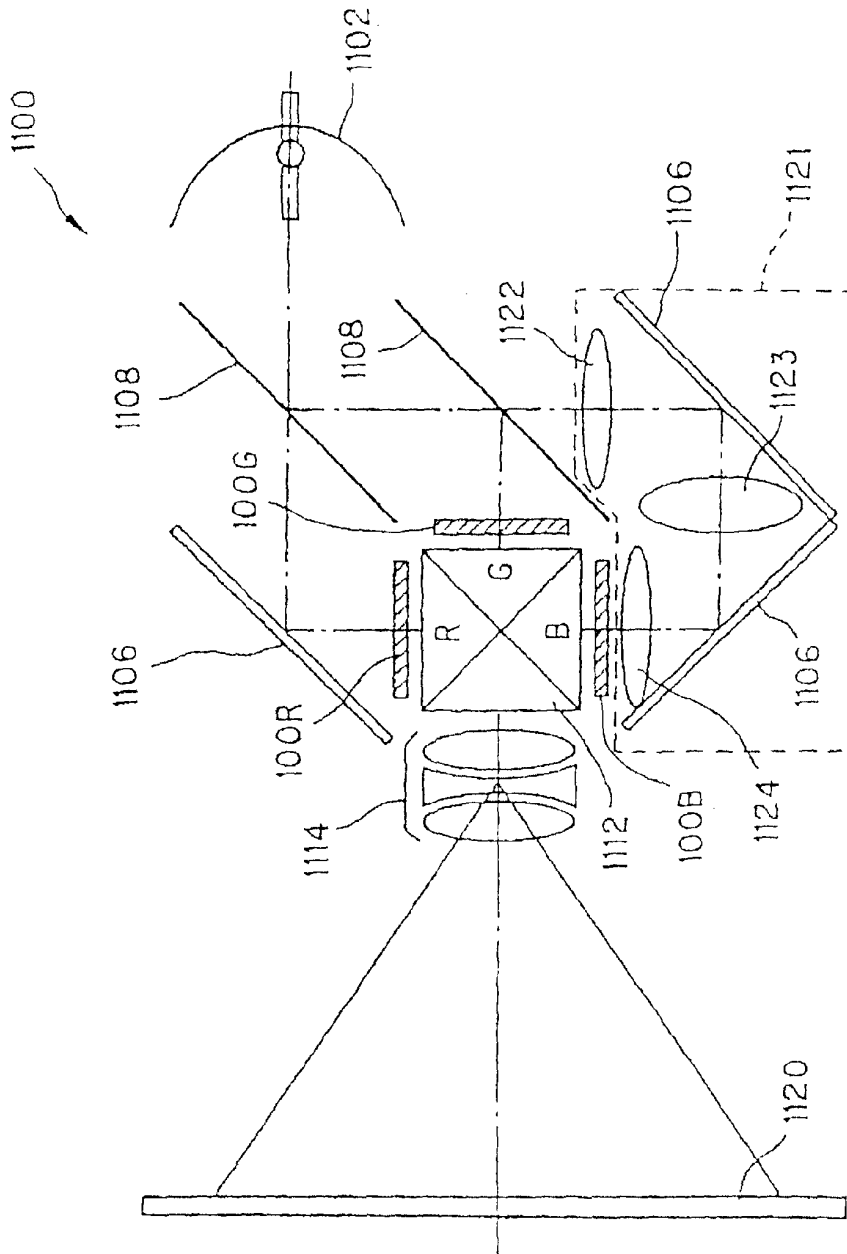


图 10



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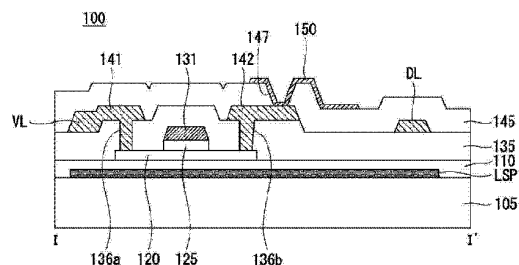
权利要求书2页 说明书8页 附图9页

(54) 发明名称

薄膜晶体管阵列基板及其制造方法

(57) 摘要

公开了一种薄膜晶体管阵列基板及其制造方法。薄膜晶体管阵列基板包括由基板上的栅极线与数据线和电源线的交叉结构所界定的多个像素单元。多个像素单元中的每个像素单元包括驱动单元以及发光单元,驱动单元包括存储信号的电容器和接收来自栅极线、数据线以及电源线的信号的开关薄膜晶体管和驱动薄膜晶体管;发光单元在像素电极上发光,像素电极接收来自驱动薄膜晶体管的驱动电流。多个屏蔽图案中的每个屏蔽图案设置在像素单元的开关薄膜晶体管和驱动薄膜晶体管的下方。



1. 一种薄膜晶体管阵列基板,包括:

多个像素单元,所述多个像素单元由基板上的栅极线与数据线和电源线的交叉结构所界定,所述多个像素单元中的每个像素单元包括:

驱动单元,所述驱动单元包括存储信号的电容器,和接收来自所述栅极线、所述数据线以及所述电源线的信号的开关薄膜晶体管和驱动薄膜晶体管;以及

发光单元,所述发光单元在像素电极上发光,所述像素电极接收来自所述驱动薄膜晶体管的驱动电流;以及

多个屏蔽图案,所述多个屏蔽图案中的每个屏蔽图案设置在每个像素单元的所述开关薄膜晶体管和所述驱动薄膜晶体管的下方。

2. 根据权利要求1所述的薄膜晶体管阵列基板,其中一个像素单元的所述屏蔽图案通过屏蔽线连接到与所述一个像素单元相邻的其它像素单元的屏蔽图案。

3. 根据权利要求2所述的薄膜晶体管阵列基板,其中所述屏蔽线与所述薄膜晶体管的有效区域周围的恒定电压驱动器连接。

4. 根据权利要求2所述的薄膜晶体管阵列基板,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个具有顶栅结构,并且所述屏蔽线设置成与所述数据线和所述电源线中的至少一者交叠。

5. 根据权利要求2所述的薄膜晶体管阵列基板,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个具有底栅结构,并且所述屏蔽线设置成与所述数据线和所述电源线中的至少一者交叠。

6. 根据权利要求5所述的薄膜晶体管阵列基板,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个包括蚀刻阻挡体。

7. 根据权利要求1所述的薄膜晶体管阵列基板,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个形成在设置于所述基板上的缓冲层上,并且所述屏蔽图案设置在所述基板与所述缓冲层之间。

8. 根据权利要求3所述的薄膜晶体管阵列基板,其中来自所述恒定电压驱动器的恒定电压通过所述屏蔽线施加至所述屏蔽图案。

9. 根据权利要求1所述的薄膜晶体管阵列基板,其中所述屏蔽图案具有单层或多层。

10. 根据权利要求1所述的薄膜晶体管阵列基板,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个包括有源层,所述有源层包含氧化物并且脱水去除了氢和/或氢氧离子。

11. 一种制造薄膜晶体管阵列基板的方法,包括:

在基板上形成屏蔽图案,在所述基板上将界定有多个像素单元,所述多个像素单元中的每个像素单元包括驱动单元和发光单元;

在上面形成有所述屏蔽图案的所述基板上形成栅极线、数据线、电源线、开关薄膜晶体管和驱动薄膜晶体管,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个包括有源层、栅极、源极和漏极;以及

形成与所述薄膜晶体管连接的像素电极,

其中所述屏蔽图案形成在所述开关薄膜晶体管和所述驱动薄膜晶体管的下方。

12. 根据权利要求11所述的方法,其中一个像素单元的所述屏蔽图案通过屏蔽线连接

到与所述一个像素单元相邻的其它像素单元的屏蔽图案。

13. 根据权利要求 12 所述的方法,其中所述屏蔽线与所述薄膜晶体管的有效区域周围的恒定电压驱动器连接。

14. 根据权利要求 11 所述的方法,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个具有顶栅结构,并且所述屏蔽线设置成与所述数据线和所述电源线中的至少一者交叠。

15. 根据权利要求 11 所述的方法,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个具有底栅结构,并且所述屏蔽线设置成与所述数据线和所述电源线中的至少一者交叠。

16. 根据权利要求 15 所述的方法,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个包括蚀刻阻挡体。

17. 根据权利要求 11 所述的方法,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个形成在设置于所述基板上的缓冲层上,并且所述屏蔽图案设置在所述基板与所述缓冲层之间。

18. 根据权利要求 13 所述的方法,其中来自所述恒定电压驱动器的恒定电压通过所述屏蔽线施加至所述屏蔽图案。

19. 根据权利要求 11 所述的方法,其中所述屏蔽图案具有单层或多层。

20. 根据权利要求 11 所述的方法,其中所述有源层包含氧化物并且在所述有源层形成之后,通过在大约 300℃至 800℃下执行热处理而使所述有源层脱水去除氢和 / 或氢氧离子。

薄膜晶体管阵列基板及其制造方法

技术领域

[0001] 本发明的实施方式涉及一种薄膜晶体管阵列基板及其制造方法。特别地,本发明的实施方式涉及一种通过将电压施加至屏蔽图案并且执行热处理而能够改善薄膜晶体管特性的薄膜晶体管阵列基板及其制造方法。

背景技术

[0002] 近来,平板显示器的重要性随着多媒体的发展而增大。因此,诸如液晶显示器(LCD)、等离子体显示面板(PDP)、场发射显示器(FED)以及有机发光二极管(OLED)显示器这样的各类平板显示器已经投入实际使用。在这些平板显示器中,OLED显示器具有出色的特性,包括1毫秒或更短的快速响应时间,低功耗、自发光结构等。因此,OLED显示器在视角方面不存在问题。由此,OLED显示器被视为下一代显示器。

[0003] 用于驱动显示装置的方法分为无源矩阵驱动方法和使用薄膜晶体管的有源矩阵驱动方法。在无源矩阵驱动方法中,阳极和阴极构造成彼此垂直,并且选定行,由此驱动显示装置。另一方面,在有源矩阵驱动方法中,薄膜晶体管分别与像素电极连接,并且显示装置由与薄膜晶体管的栅极连接的电容器的电容所保持的电压所驱动。

[0004] 除了薄膜晶体管的包括迁移率、漏电流等的基本特性以外,为保持长寿命所需要的耐用性和电气可靠性对薄膜晶体管来说也非常重要。薄膜晶体管的有源层通常由非晶硅或多晶硅形成。非晶硅具有通过简单的形成工序而减少有源层的生产成本的优点。然而,其难以确保电气可靠性。而且,由于高处理温度,所以很难将多晶硅应用于大面积装置,且无法确保基于结晶型的多晶硅的均匀性。

[0005] 当有源层由氧化物形成时,即使在低温中形成有源层,也可获得薄膜晶体管的出色的迁移率。并且,由于有源层的电阻的变化增大了对氧气量的依赖,所以非常容易获得薄膜晶体管的所希望的物理性能。因此,近来,对薄膜晶体管的应用的兴趣显著增大。特别地,在有源层中使用的氧化物的实例包括氧化锌(ZnO)、氧化铟锌(InZnO)以及氧化铟镓锌(InGaZnO₄)。

[0006] 然而,由于包括由氧化物形成的有源层的薄膜晶体管通过外部光源产生光电流,并且由此呈现不稳定的特性,所以降低了薄膜晶体管的可靠性。

发明内容

[0007] 本发明的实施方式提供了一种通过将电压施加至屏蔽图案并且执行热处理而能够改善薄膜晶体管特性的薄膜晶体管阵列基板及其制造方法。

[0008] 在一个方面,一种薄膜晶体管阵列基板,包括:多个像素单元,所述多个像素单元由基板上的栅极线与数据线和电源线的交叉结构所界定,所述多个像素单元中的每个像素单元包括:驱动单元,所述驱动单元包括存储信号的电容器,和接收来自所述栅极线、所述数据线以及所述电源线的信号的开关薄膜晶体管和驱动薄膜晶体管;以及发光单元,所述发光单元在像素电极上发光,所述像素电极接收来自所述驱动薄膜晶体管的驱动电流;以

及多个屏蔽图案,所述多个屏蔽图案中的每个屏蔽图案设置在每个像素单元的所述开关薄膜晶体管和所述驱动薄膜晶体管的下方。

[0009] 一个像素单元的所述屏蔽图案可通过屏蔽线连接到与所述一个像素单元相邻的其它像素单元的屏蔽图案。

[0010] 所述屏蔽线可与所述薄膜晶体管的有效区域周围的恒定电压驱动器连接。

[0011] 此外,所述开关薄膜晶体管和所述驱动薄膜晶体管每个可具有顶栅结构,并且所述屏蔽线设置成与所述数据线和所述电源线中的至少一者交叠。

[0012] 此外,所述开关薄膜晶体管和所述驱动薄膜晶体管每个可具有底栅结构,并且所述屏蔽线设置成与所述数据线和所述电源线中的至少一者交叠。

[0013] 此外,所述开关薄膜晶体管和所述驱动薄膜晶体管每个可包括蚀刻阻挡体。

[0014] 并且,所述开关薄膜晶体管和所述驱动薄膜晶体管每个可形成在设置于所述基板上的缓冲层上,并且所述屏蔽图案可设置在所述基板与所述缓冲层之间。

[0015] 并且,来自所述恒定电压驱动器的恒定电压可通过所述屏蔽线施加至所述屏蔽图案。

[0016] 此外,所述屏蔽图案可具有单层或多层。

[0017] 此外,所述开关薄膜晶体管和所述驱动薄膜晶体管每个可包括有源层,所述有源层包含氧化物并且脱水去除了氢和 / 或氢氧离子。

[0018] 另一方面,一种制造薄膜晶体管阵列基板的方法,包括:在基板上形成屏蔽图案,所述基板上将界定多个像素单元,所述多个像素单元中的每个像素单元包括驱动单元和发光单元;在上面形成有所述屏蔽图案的所述基板上形成栅极线、数据线、电源线、开关薄膜晶体管和驱动薄膜晶体管,其中所述开关薄膜晶体管和所述驱动薄膜晶体管每个包括有源层、栅极、源极和漏极;以及形成与所述薄膜晶体管连接的像素电极,其中所述屏蔽图案形成在所述开关薄膜晶体管和所述驱动薄膜晶体管的下方。

[0019] 此外,一个像素单元的所述屏蔽图案可通过屏蔽线连接到与所述一个像素单元相邻的其它像素单元的屏蔽图案。

[0020] 此外,所述屏蔽线可与所述薄膜晶体管的有效区域周围的恒定电压驱动器连接。

[0021] 此外,所述开关薄膜晶体管和所述驱动薄膜晶体管每个可具有顶栅结构,并且所述屏蔽线可设置成与所述数据线和所述电源线中的至少一者交叠。

[0022] 此外,所述开关薄膜晶体管和所述驱动薄膜晶体管每个可具有底栅结构,并且所述屏蔽线可设置成与所述数据线和所述电源线中的至少一者交叠。

[0023] 此外,所述开关薄膜晶体管和所述驱动薄膜晶体管每个可包括蚀刻阻挡体。

[0024] 并且,所述开关薄膜晶体管和所述驱动薄膜晶体管每个形成在设置于所述基板上的缓冲层上,并且所述屏蔽图案设置在所述基板与所述缓冲层之间。

[0025] 此外,来自所述恒定电压驱动器的恒定电压可通过所述屏蔽线施加至所述屏蔽图案。

[0026] 此外,所述屏蔽图案可具有单层或多层。

[0027] 此外,所述有源层可包含氧化物并且在所述有源层形成之后,可通过在大约 300℃ 至 800℃ 下执行热处理而使所述有源层脱水去除氢和 / 或氢氧离子。

附图说明

[0028] 被包括在内以给本发明提供进一步理解并结合在本申请中组成本说明书一部分的附图图解了本发明的实施方式,并与说明书一起用于解释本发明的原理。在附图中:

[0029] 图 1 是根据本发明实施方式的薄膜晶体管阵列基板的平面图,并且示出了多个像素中的一个像素的构造作为实例;

[0030] 图 2 是示出根据本发明实施方式的薄膜晶体管阵列基板中的屏蔽图案和屏蔽线的布置的平面图;

[0031] 图 3 是沿图 1 的线 I-I' 所取的剖面图;

[0032] 图 4A 至图 4E 是按顺序示出根据本发明实施方式的制造薄膜晶体管阵列基板的方法中的每个阶段的剖面图;

[0033] 图 5 示出了在有源层上执行热处理之前和之后屏蔽图案的位置偏移(position shift);

[0034] 图 6 是根据本发明另一实施方式的薄膜晶体管阵列基板的剖面图;

[0035] 图 7A 至图 7D 是按顺序示出根据本发明另一实施方式的制造薄膜晶体管阵列基板的方法中的每个阶段的剖面图;

[0036] 图 8 是根据本发明再一实施方式的薄膜晶体管阵列基板的剖面图;以及

[0037] 图 9A 至图 9E 是按顺序示出根据本发明再一实施方式的制造薄膜晶体管阵列基板的方法中的每个阶段的剖面图。

具体实施方式

[0038] 现在将详细描述本发明的实施方式,附图中图解了这些实施方式的一些实例。尽可能地在整个附图中使用相同的附图标记表示相同或相似的部件。应当注意的是,如果已知技术可能造成本发明的实施方式被误解,那么将省略对所述已知技术的详细描述。

[0039] 图 1 是根据本发明实施方式的薄膜晶体管阵列基板的平面图,并且图 1 示出了多个像素中的一个像素的构造作为实例。图 2 是示出在薄膜晶体管阵列基板中的屏蔽图案和屏蔽线的布置的平面图。图 3 是沿图 1 的线 I-I' 所取的剖面图。图 4A 至图 4E 是按顺序示出根据本发明实施方式的制造薄膜晶体管阵列基板的方法中的每个阶段的剖面图。

[0040] 如图 1 中所示,提供包括多个像素单元 SP 的基板(未示出)。像素单元 SP 由在一个方向上布置的栅极线 GL、与栅极线 GL 垂直布置的数据线 DL、以及与数据线 DL 平行布置的电源线 VL 界定。

[0041] 每个像素单元 SP 包括与栅极线 GL 和数据线 DL 连接的开关薄膜晶体管 STR、与开关薄膜晶体管 STR 和电源线 VL 连接的电容器 Cst、以及与电容器 Cst 和电源线 VL 连接的驱动薄膜晶体管 DTR。电容器 Cst 包括电容器下电极 133 和电容器上电极 144。栅极线 GL、数据线 DL、电源线 VL、开关薄膜晶体管 STR、电容器 Cst 以及驱动薄膜晶体管 DTR 的形成区域被定义为驱动单元 DP。

[0042] 发光二极管包括与驱动薄膜晶体管 DTR 电连接的像素电极 150、位于像素电极 150 上的发光层(未示出)、以及相对的电极(未示出)。在本发明的实施方式中,设置在像素电极 150 上且由发光层发光的部分被定义为发光单元 LEP。

[0043] 屏蔽图案 LSP 设置在每个像素单元 SP 中以便使每个像素单元 SP 的开关薄膜晶体

管 STR 和驱动薄膜晶体管 DTR 遮蔽光。为此,屏蔽图案 LSP 设置在开关薄膜晶体管 STR 和驱动薄膜晶体管 DTR 的形成区域。即,屏蔽图案 LSP 设置在从像素单元 SP 除去发光单元 LEI 的驱动单元 DP 中。一个像素单元 SP 的屏蔽图案 LSP 通过屏蔽线 LSL 连接到与所述一个像素单元 SP 相邻的其它像素单元 SP 的屏蔽图案 LSP。屏蔽线 LSL 设置成与电源线 VL 交叠,但是本发明的实施方式并不限于此。例如,屏蔽线 LSL 可设置成与栅极线 GL 和数据线 DL 中的至少一者交叠。

[0044] 更具体地,如图 2 中所示,根据本发明的实施方式的薄膜晶体管阵列包括有效区域 A/A,所述有效区域 A/A 包括多个像素(未示出)并显示图像。屏蔽图案 LSP 分别设置在多个像素上并且通过屏蔽线 LSL 彼此相连。用于连接屏蔽图案 LSP 的屏蔽线 LSL 具有网状结构(mesh structure)并且所述屏蔽线 LSL 形成在有效区域 A/A 中。

[0045] 恒定电压驱动器 CVD 设置在有效区域 A/A 周围并且将恒定电压施加至屏蔽线 LSL。每条屏蔽线 LSL 与有效区域 A/A 上侧上的恒定电压驱动器 CVD 连接并且接收来自恒定电压驱动器 CVD 的恒定电压。当通过屏蔽线 LSL 将恒定电压施加至屏蔽图案 LSP 时,屏蔽图案 LSP 与薄膜晶体管的栅极一起用作双栅极(double gate electrode),从而改善薄膜晶体管的初始特征色散(initial characteristic dispersion)。因此,可提高薄膜晶体管的可靠性。

[0046] 下面详细描述根据本发明的实施方式的薄膜晶体管阵列基板。

[0047] 如图 3 中所示,屏蔽图案 LSP 设置在基板 105 上,并且缓冲层 110 设置在屏蔽图案 LSP 上。包含氧化物的有源层 120 设置在缓冲层 110 上,栅极绝缘层 125 和栅极 131 设置在有源层 120 的一部分上。层间介电层 135 设置在上面具有栅极 131 的栅极绝缘层 125 上。源极 141 和漏极 142 设置在层间介电层 135 上并且通过暴露有源层 120 的两侧的接触孔 136a 和 136b 与有源层 120 连接。源极 141 与电源线 VL 连接,数据线 DL 设置在层间介电层 135 的一个区域上。从而,构造成包括有源层 120、栅极 131、源极 141 以及漏极 142 的驱动薄膜晶体管 DTR。

[0048] 钝化层 145 设置在驱动薄膜晶体管 DTR 上,像素电极 150 设置在钝化层 145 上并且通过暴露漏极 142 的过孔 147 与漏极 142 连接。从而,构造成根据本发明的实施方式的薄膜晶体管阵列基板 100。

[0049] 下面参照图 4A 至图 4E 详细描述根据本发明的实施方式的制造薄膜晶体管阵列基板的方法。

[0050] 如图 4A 中所示,在基板 105 上形成屏蔽图案 LSP。屏蔽图案 LSP 可由能够阻挡光的材料形成。根据本发明的实施方式的屏蔽图案 LSP 可具有单层或具有相似的热膨胀系数的多层。因为在一些情况中,如果屏蔽图案 LSP 具有由不同的材料形成的多层,这些多层则可能由于不同的热膨胀系数而在后续的热处理中损坏。优选地,考虑到屏蔽图案 LSP 由于在后续的有源层的热处理中高温所导致的收缩,所以根据本发明的实施方式的屏蔽图案 LSP 具有单层。例如,屏蔽图案 LSP 可由诸如铬(Cr)、钛(Ti)和钼(Mo)这样的金属材料形成。

[0051] 在上面形成有屏蔽图案 LSP 的基板 105 上形成缓冲层 110。形成缓冲层 110 以便保护将在后续工序中形成的薄膜晶体管免受杂质,例如来自基板 105 的碱离子。可使用二氧化硅(SiO_2)、硅氮化物(SiNx)等选择性地形成缓冲层 110。基板 105 可由玻璃、塑料或金

属形成。

[0052] 然后,可使用氧化镓(Ga_2O_3)、氧化铟(In_2O_3)和氧化锌(ZnO)的复合氧化物靶材通过溅射方法在缓冲层 110 上形成非晶锌氧化物基复合半导体,特别是 a-IGZO (非晶氧化铟镓锌) 半导体。可选择地,可使用化学汽相沉积(CVD)方法或者原子层沉积(ALD)方法。在本发明的实施方式中,可使用复合氧化物靶材沉积非晶锌氧化物基复合半导体,在所述复合氧化物靶材中,镓(Ga)、铟(In)和锌(Zn)的原子比例为大约 1:1:1 或 2:2:1 或 3:2:1 或 4:2:1。当复合氧化物靶材中所包含的镓(Ga)、铟(In)和锌(Zn)的原子比例为大约 2:2:1 时,镓(Ga)、铟(In)和锌(Zn)的当量比为大约 2.8:2.8:1。并且,可根据其它处理条件对根据本发明的实施方式的非晶锌氧化物基复合半导体进行不同地沉积。然而,非晶锌氧化物基复合半导体可在如下条件下沉积:在大约 1 埃/秒至 200 埃/秒的沉积速率下,注入的氧气流量与氧气流量和氩气流量的百分比(即氧气浓度)为大约 1% 至 40%。

[0053] 通过热处理对非晶锌氧化物基复合半导体进行构图从而形成有源层 120。热处理是一种用于去除有源层 120 中所包含的氢(H_2 和 H)或氢氧离子(OH)的脱水处理。热处理可使用应用高温惰性气体的快速热退火(RTA)处理。脱水处理去除了妨碍载流子在有源层 120 内移动的氢(H_2 和 H)或氢氧离子(OH),从而改善有源层 120 的特性。热处理可在大约 300°C 至 800°C 下执行,优选地在等于或高于大约 500°C 下执行。此外,热处理可执行大约 1 分钟至 30 分钟。例如,可在大约 650°C 下执行 RTA 处理大约 3 到 6 分钟。

[0054] 接下来,如图 4B 中所示,将硅氧化物(SiO_x)或硅氮化物(SiN_x)堆叠在有源层 120 上。然后,将选自以下物质构成的组中的一种堆叠在所述硅氧化物(SiO_x)或硅氮化物(SiN_x)上:铜(Cu)、钼(Mo)、铝(Al)、铬(Cr)、金(Au)、钛(Ti)、镍(Ni)、钕(Nd)、钽(Ta)以及钨(W)或上述物质的组合,并蚀刻形成栅极绝缘层 125 和栅极 131。

[0055] 栅极 131 形成在有源层 120 的一部分之上,在有源层 120 中将形成沟道区域。此外,栅极 131 可具有多层,在所述多层中,每层由选自以下物质构成的组中的一种形成:铜(Cu)、钼(Mo)、铝(Al)、铬(Cr)、金(Au)、钛(Ti)、镍(Ni)、钕(Nd)、钽(Ta)以及钨(W)或上述物质的组合。

[0056] 接下来,如图 4C 中所示,将硅氧化物(SiO_x)、硅氮化物(SiN_x)或它们二者堆叠在上面形成有栅极 131 的基板 105 之上,从而形成层间介电层 135。对层间介电层 135 的与有源层 120 的两侧相对应的部分进行蚀刻从而形成暴露有源层 120 的接触孔 136a 和 136b。

[0057] 接下来,如图 4D 中所示,在上面形成有层间介电层 135 的基板 105 之上形成源极 141、漏极 142 以及数据线 DL。尽管未示出,但同时形成电源线。源极 141、漏极 142 和数据线 DL 每个可具有单层或多层。当源极 141、漏极 142 和数据线 DL 每个都具有单层时,它们可由选自以下物质构成的组中的一种形成:钼(Mo)、铝(Al)、铬(Cr)、金(Au)、钛(Ti)、镍(Ni)、钕(Nd)以及铜(Cu)或上述物质的组合。当源极 141 和漏极 142 每个都具有多层时,它们可具有由 Mo/Al-Nd、Mo/Al 或 Ti/Al 形成的双层或者由 Mo/Al-Nd/Mo、Mo/Al/Mo 或 Ti/Al/Ti 形成的三层。由此,形成了包括有源层 120、栅极 131、源极 141 以及漏极 142 的薄膜晶体管。

[0058] 接下来,如图 4E 中所示,将硅氧化物(SiO_x)、硅氮化物(SiN_x)或它们二者堆叠在上面形成有源极 141 和漏极 142 的基板 105 之上,从而形成钝化层 145。将钝化层 145 的与漏极 142 相对应的部分进行蚀刻从而形成暴露漏极 142 的过孔 147。

[0059] 然后,在上面形成有钝化层 145 的基板 105 之上形成像素电极 150。像素电极 150 可由透明导电材料形成,例如,氧化铟锡(ITO)或氧化铟锌(IZO)。像素电极 150 通过过孔 147 与漏极 142 连接。从而,生产出了根据本发明的实施方式的薄膜晶体管阵列基板 100。

[0060] 图 5 示出了在有源层上执行热处理之前和之后屏蔽图案的位置偏移。如图 5 中所示,当在有源层上执行热处理时,玻璃基板可能会由于热处理的高温而收缩。在此情况下,形成在基板上的屏蔽图案 LSP 通过基板的收缩而发生偏移。即,形成在基板上的屏蔽图案 LSP 从初始形成位置‘A’向左右上下偏移了大约 15 微米,从而移动到最终位置‘B’。由于屏蔽图案 LSP 的偏移距离‘d’被包括在屏蔽图案 LSP 的偏移余量(shift margin)中,所以所述偏移并不要紧。

[0061] 与公开了顶栅结构,即栅极位于有源层上方的上述实施方式不同,根据本发明另一实施方式的薄膜晶体管阵列基板可包括具有底栅结构的薄膜晶体管,所述底栅结构是指栅极位于有源层下方。

[0062] 图 6 是根据本发明另一实施方式的薄膜晶体管阵列基板的剖面图。图 7A 至图 7D 是按顺序示出根据本发明另一实施方式的制造薄膜晶体管阵列基板的方法中的每个阶段的剖面图。

[0063] 如图 6 中所示,屏蔽图案 LSP 设置在基板 205 上,并且缓冲层 210 设置在屏蔽图案 LSP 上。栅极 231 设置在缓冲层 210 上,并且栅极绝缘层 225 设置在栅极 231 上。包含氧化物的有源层 220 设置在栅极绝缘层 225 上,并且蚀刻阻挡体 235 设置在有源层 220 的一部分上。源极 241 和漏极 242 设置在蚀刻阻挡体 235 的一部分上并且分别覆盖有源层 220 的两端。源极 241 与电源线 VI 连接,并且数据线 DI 设置在与漏极 242 隔开的区域中。因而,构造了包括有源层 220、栅极 231、源极 241 以及漏极 242 的薄膜晶体管。

[0064] 钝化层 245 设置在包括源极 241 和漏极 242 的基板 205 之上。像素电极 250 设置在钝化层 245 上并且通过过孔 247 与漏极 242 连接。由此,构造了根据本发明的实施方式的薄膜晶体管阵列基板 200。

[0065] 下面参照图 7A 至图 7D 详细描述制造图 6 中示出的薄膜晶体管阵列基板 200 的方法。在下文中,可简要描述或完全省略与图 4A 至图 4E 相同的制造方法。

[0066] 如图 7A 中所示,在基板 205 上形成屏蔽图案 LSP,并且在上面形成有屏蔽图案 LSP 的基板 205 上形成缓冲层 210。然后,在缓冲层 210 上形成栅极 231,在栅极 231 上形成栅极绝缘层 225。然后,将氧化锌(ZnO)、氧化铟锌(InZnO)、氧化铟锡(ZnSnO)和氧化铟镓锌(InGaZnO₄)中的一种堆叠在栅极绝缘层 225 上并且通过热处理进行构图,从而形成有源层 220。优选地,可用氧化铟镓锌(InGaZnO₄)形成有源层 220。

[0067] 接下来,如图 7B 中所示,将硅氧化物(SiO_x)或硅氮化物(SiN_x)堆叠在有源层 220 上并构图形成蚀刻阻挡体 235。蚀刻阻挡体 235 防止位于源极 241 和漏极 242 下方的有源层 220 在后续用于构图源极 241 和漏极 242 的工序中损坏。然后,将选自以下物质构成的组中的一种堆叠在包括蚀刻阻挡体 235 的基板 205 之上,从而形成金属层 240:钼(Mo)、铝(Al)、铬(Cr)、金(Au)、钛(Ti)、镍(Ni)、钕(Nd)以及铜(Cu)或上述物质的组合。

[0068] 接下来,如图 7C 中所示,对金属层 240 进行构图从而形成源极 241 和漏极 242,所述源极 241 和所述漏极 242 设置在蚀刻阻挡体 235 的一部分上并且与有源层 220 连接。从而,形成了包括栅极 231、有源层 220、源极 241 以及漏极 242 的薄膜晶体管。

[0069] 接下来,如图 7D 中所示,将钝化层 245 设置在上面形成有源极 241 和漏极 242 的基板 205 之上。对钝化层 245 的与漏极 242 相对应的部分进行蚀刻从而形成暴露漏极 242 的过孔 247。然后,在上面形成有钝化层 245 的基板 205 之上形成像素电极 250。从而,生产出了根据本发明的实施方式的薄膜晶体管阵列基板 200。

[0070] 与上述实施方式不同,根据本发明再一实施方式的薄膜晶体管阵列基板可包括具有背沟道(back channel)蚀刻结构的薄膜晶体管。图 8 是根据本发明再一实施方式的薄膜晶体管阵列基板的剖面图。图 9A 至图 9E 是按顺序示出根据本发明再一实施方式的制造薄膜晶体管阵列基板的方法中的每个阶段的剖面图。

[0071] 如图 8 中所示,屏蔽图案 LSP 设置在基板 305 上,并且缓冲层 310 设置在屏蔽图案 LSP 上。栅极 331 设置在缓冲层 310 上,并且栅极绝缘层 325 设置在栅极 331 上。包含氧化物的有源层 320 设置在栅极绝缘层 325 上,并且欧姆接触层 335 分别设置在有源层 320 的两侧上。源极 341 和漏极 342 分别设置在欧姆接触层 335 上并且覆盖有源层 320 的两端。源极 341 与电源线 VL 连接,并且数据线 DL 设置在与漏极 342 隔开的区域中。由此,构造了包括有源层 320、栅极 331、欧姆接触层 335、源极 341 以及漏极 342 的薄膜晶体管。

[0072] 钝化层 345 设置在包括源极 341 和漏极 342 的基板 305 之上。像素电极 350 设置在钝化层 345 上并且通过过孔 347 与漏极 342 连接。由此,构造了根据本发明的实施方式的薄膜晶体管阵列基板 300。

[0073] 下面参照图 9A 至图 9E 详细描述制造图 8 中示出的薄膜晶体管阵列基板 300 的方法。在下文中,可简要描述或完全省略与图 7A 至图 7D 相同的制造方法。

[0074] 如图 9A 中所示,在基板 305 上形成屏蔽图案 LSP,在上面形成有屏蔽图案 LSP 的基板 305 上形成缓冲层 310。然后,在缓冲层 310 上形成栅极 331,在栅极 331 上形成栅极绝缘层 325。然后,将氧化锌(ZnO)、氧化镓锌(InZnO)、氧化锌锡(ZnSnO)和氧化镓镓锌(InGaZnO₄)中的一种堆叠在栅极绝缘层 325 形成氧化物层 322。然后,将非晶硅堆叠在氧化物层 322 上形成非晶硅层 333。

[0075] 接下来,如图 9B 中所示,在上面形成有氧化物层 322 和非晶硅层 333 的基板 305 上执行热处理,从而对氧化物层 322 和非晶硅层 333 进行构图。由此,形成了有源层 320 和欧姆接触层 335。欧姆接触层 335 改善了有源层与将在稍后形成的源极和漏极之间的欧姆特性,并且提高了薄膜晶体管的电流导通(on-current)特性。

[0076] 接下来,如图 9C 中所示,将选自以下物质构成的组中的一种堆叠在包括有源层 320 和欧姆接触层 335 的基板 305 之上:钼(Mo)、铝(Al)、铬(Cr)、金(Au)、钛(Ti)、镍(Ni)、钕(Nd)、铜(Cu)或上述物质的组合,并构图形成通过欧姆接触层 335 与有源层 320 连接的源极 341 和漏极 342。

[0077] 接下来,如图 9D 中所示,将源极 341 和漏极 342 用作阻挡层通过背沟道蚀刻工艺对欧姆接触层 335 进行蚀刻,从而暴露了有源层 320 的与栅极 331 相对应的部分。由此,界定了有源层 320 的沟道,并且将欧姆接触层 335 划分并隔开。结果,形成了包括栅极 331、有源层 320、欧姆接触层 335、源极 341 以及漏极 342 的薄膜晶体管。

[0078] 接下来,如图 9E 中所示,将钝化层 345 设置在上面形成有源极 341 和漏极 342 的基板 305 之上。对钝化层 345 的与漏极 342 相对应的部分进行蚀刻从而形成暴露漏极 342 的过孔 347。然后,在上面形成有钝化层 345 的基板 305 之上形成像素电极 350。由此,生

产出了根据本发明的实施方式的薄膜晶体管阵列基板 300。

[0079] 如上所述,根据本发明的实施方式的薄膜晶体管阵列基板包括屏蔽图案,从而提高了外部光的可靠性。此外,根据本发明的实施方式的薄膜晶体管阵列基板将恒定电压施加至屏蔽图案,从而改善了薄膜晶体管的初始特征色散。

[0080] 此外,根据本发明的实施方式的薄膜晶体管阵列基板在包含氧化物的有源层上执行热处理,并去除了妨碍载流子在有源层内移动的氢(H_2 和 H) 或氢氧离子(OH),从而改善了有源层的特性。

[0081] 尽管已经参照一些示例性实施方式描述了本发明的实施方式,但应当理解的是:所属领域技术人员可以设计出落入本公开内容原理的范围内的大量其它修改和实施方式。更具体地,可以在说明书、附图和所附权利要求书的范围内对主题组合方案的组成部件和/或布置作出各种变化和修改。除了组成部件和/或布置的变化和修改之外,替代使用对于所属领域技术人员来说也将是显而易见的。

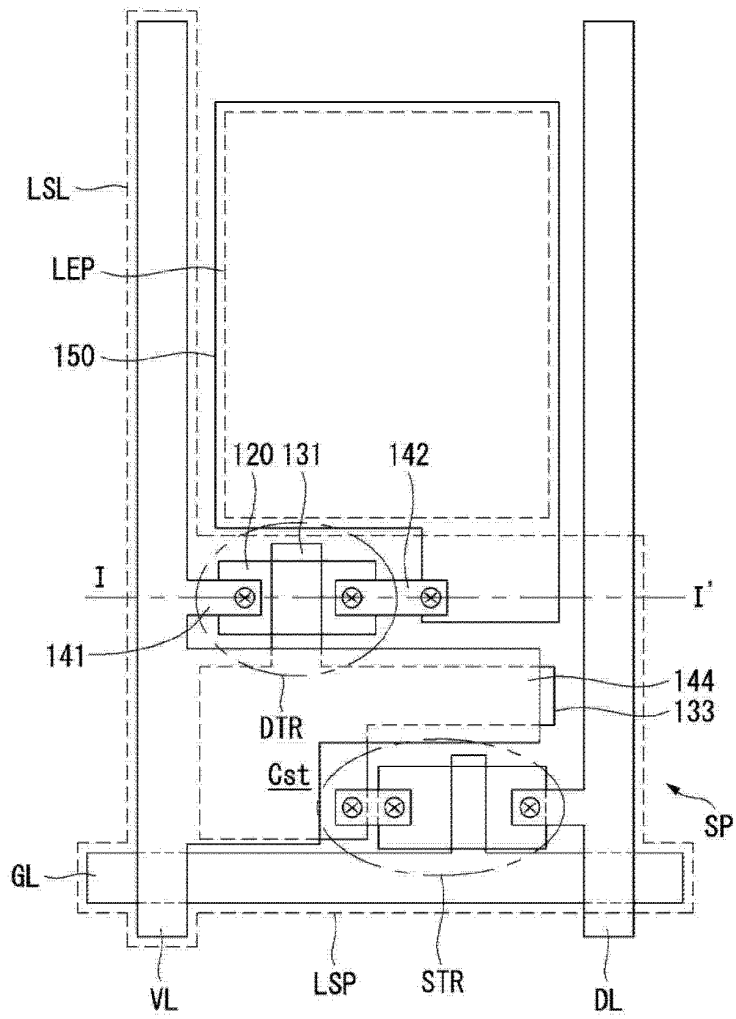


图 1

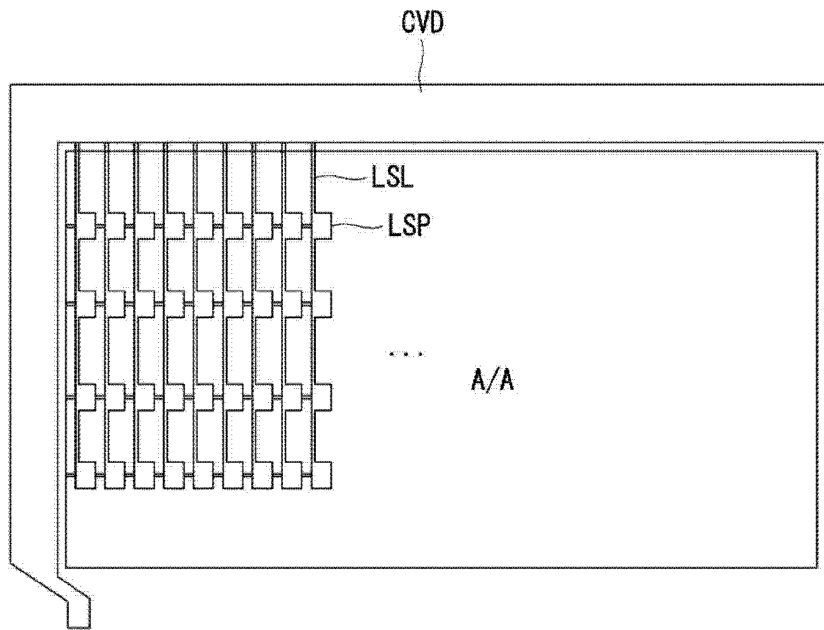


图 2

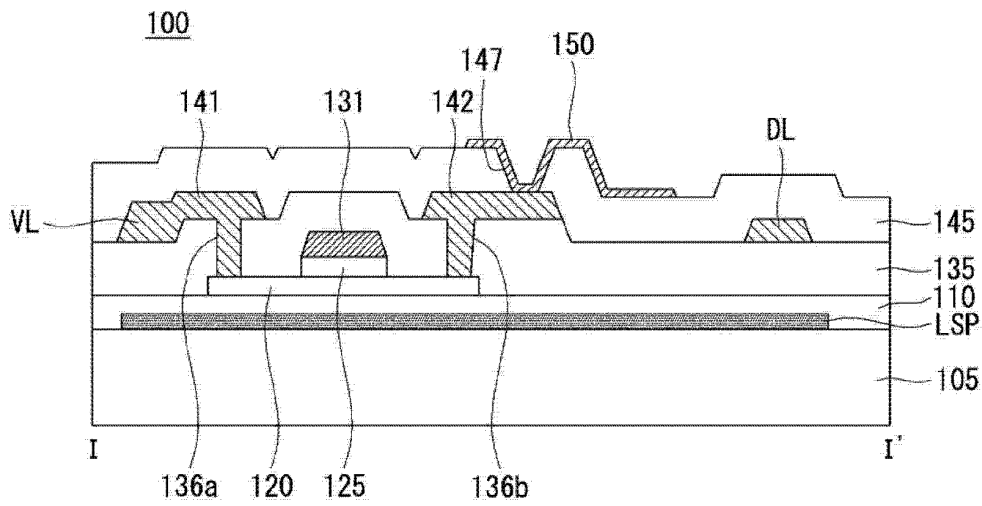


图 3

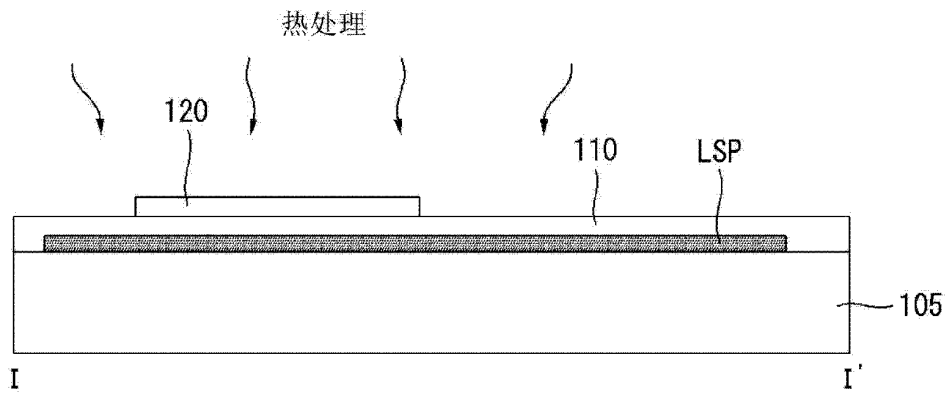


图 4A

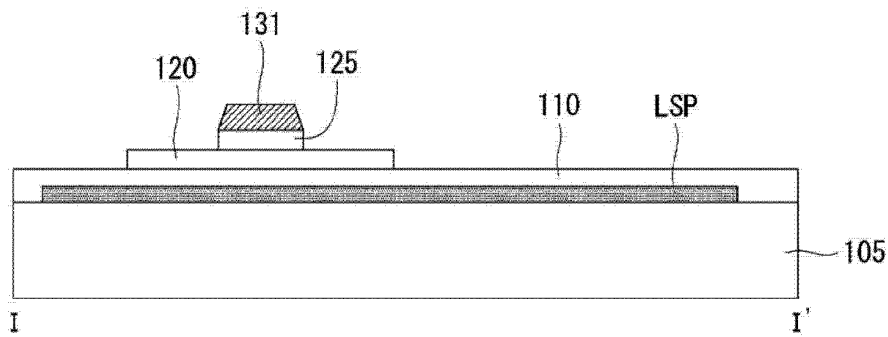


图 4B

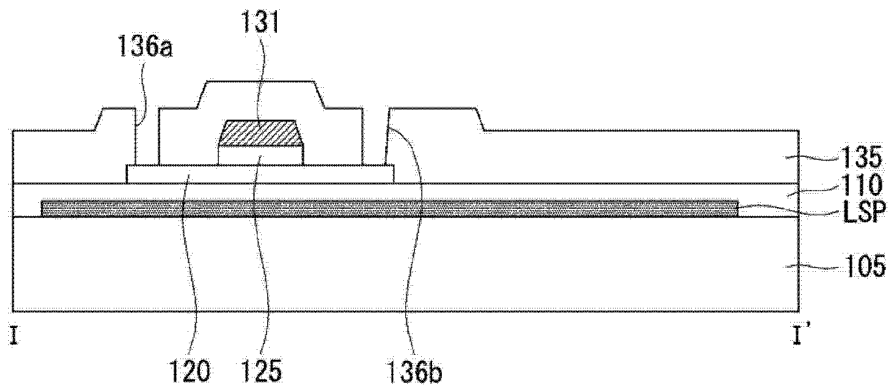


图 4C

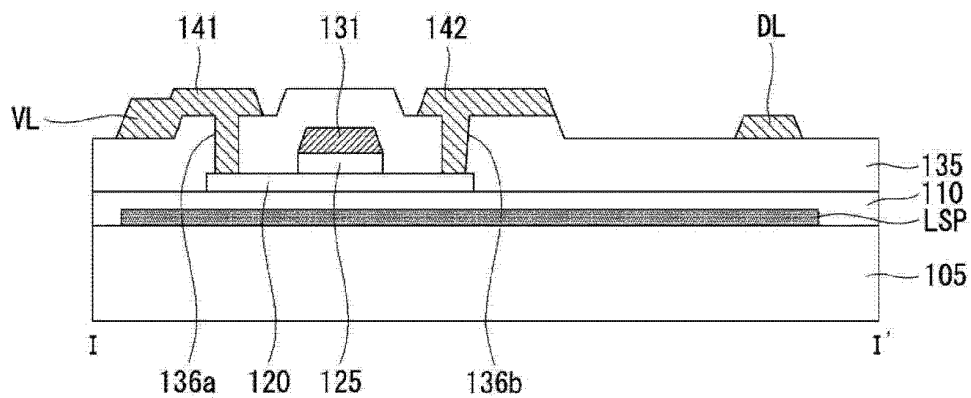


图 4D

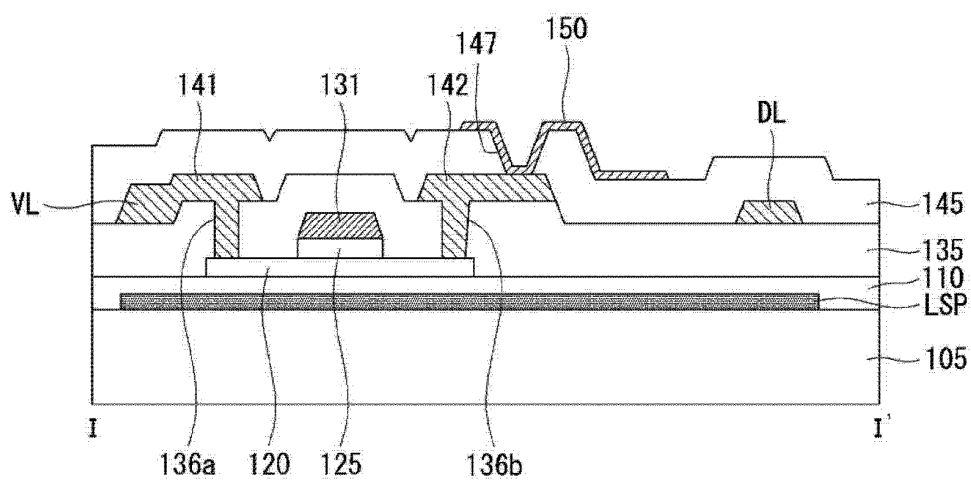


图 4E

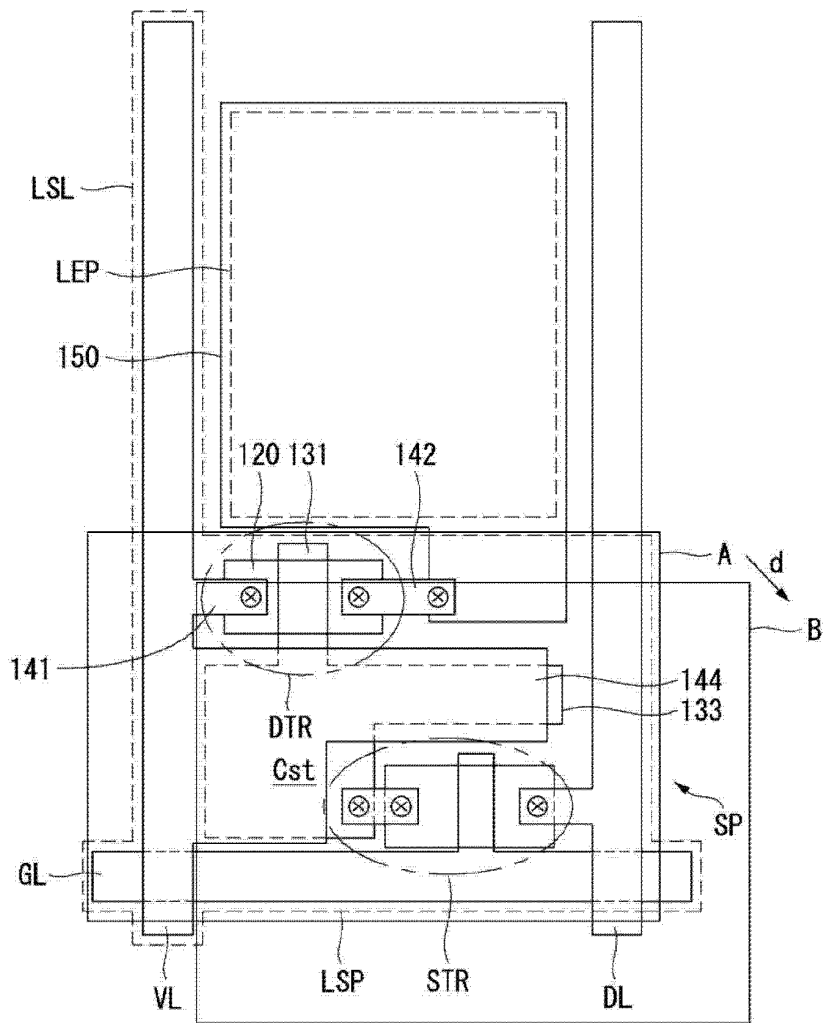


图 5

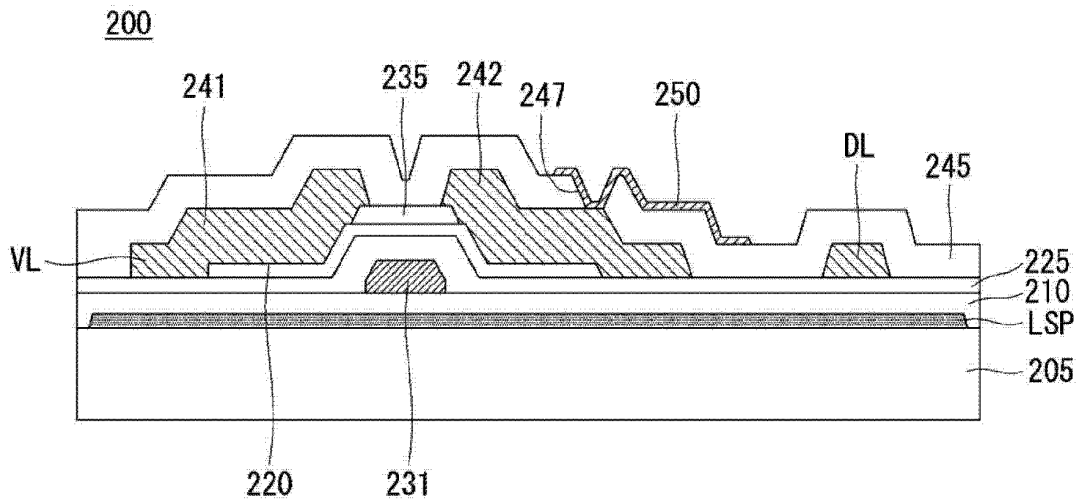


图 6

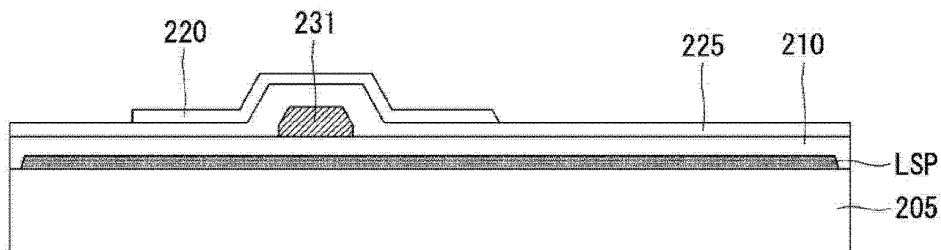


图 7A

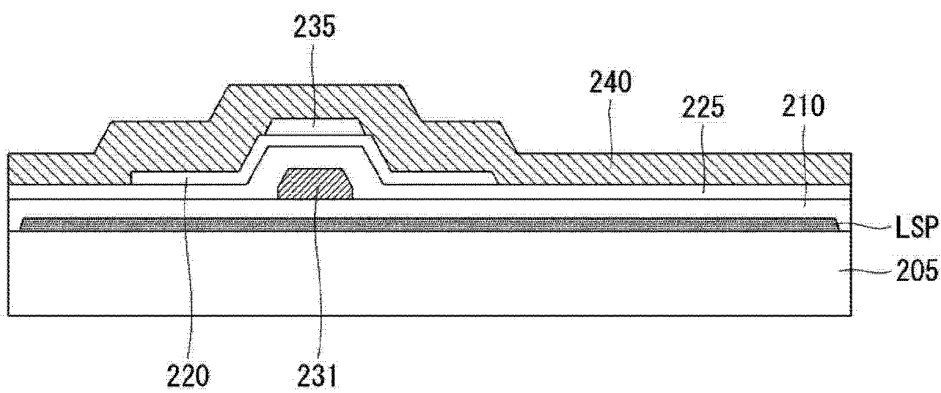


图 7B

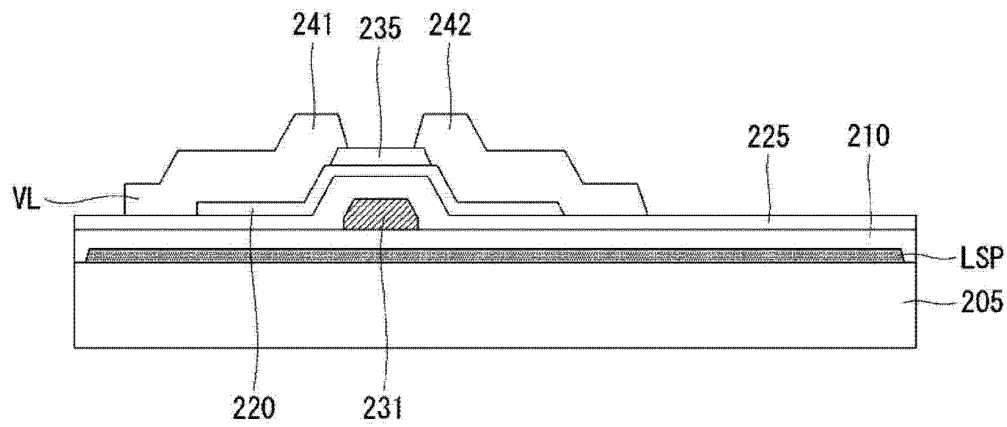


图 7C

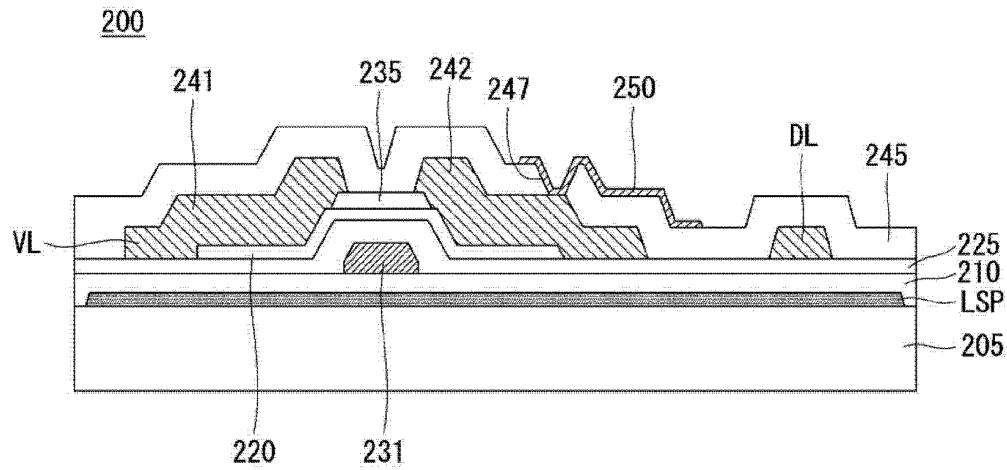


图 7D

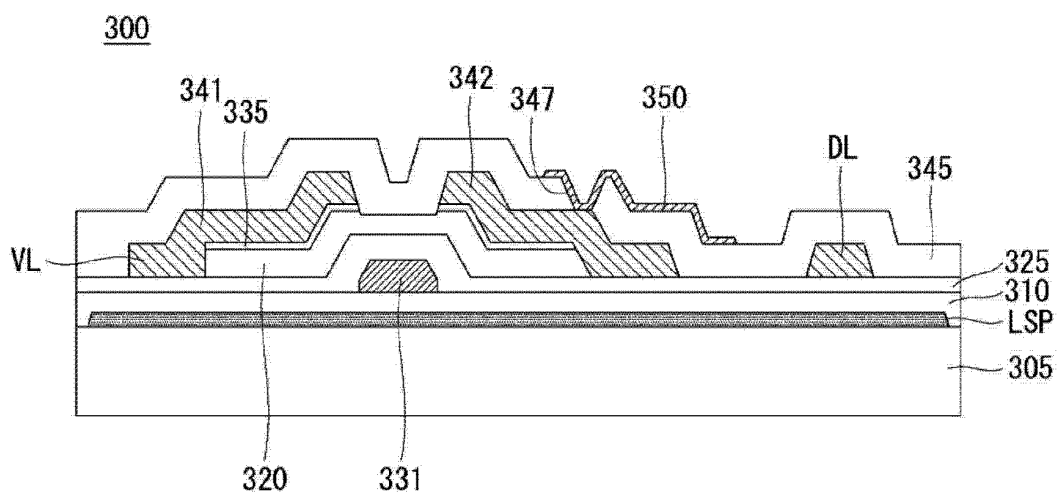


图 8

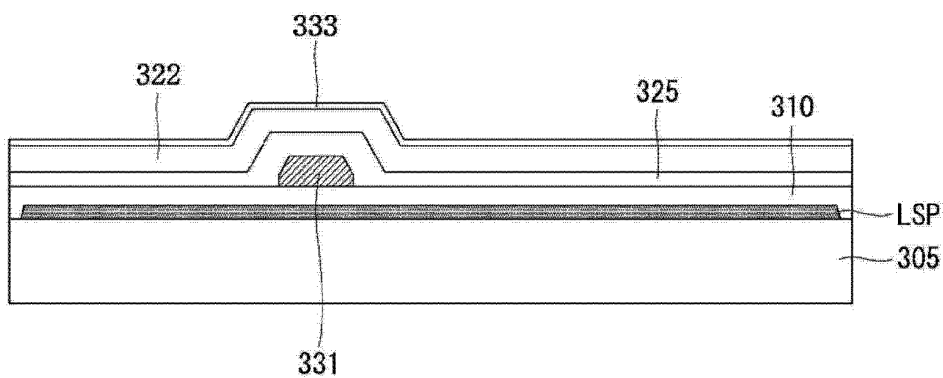


图 9A

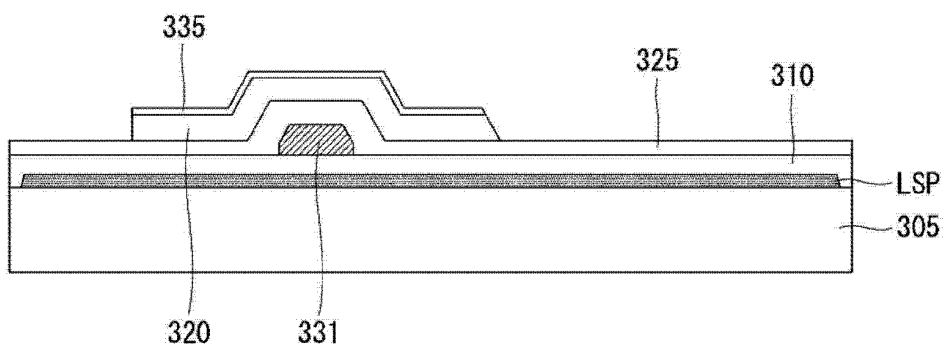


图 9B

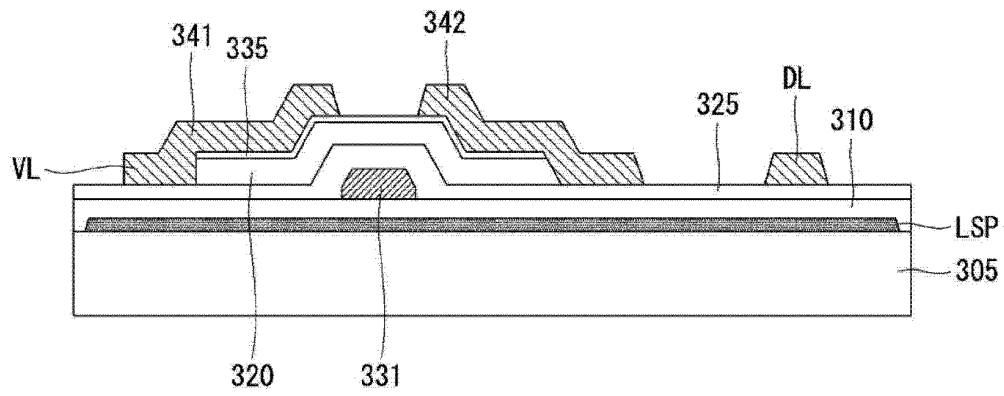


图 9C

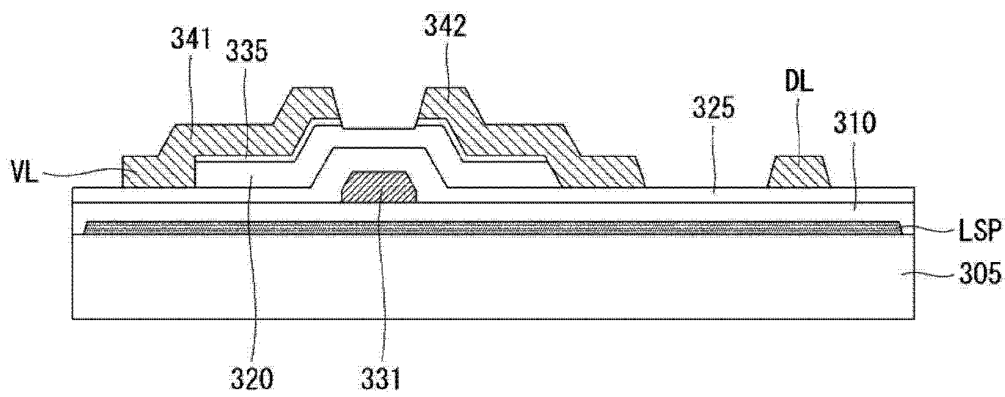


图 9D

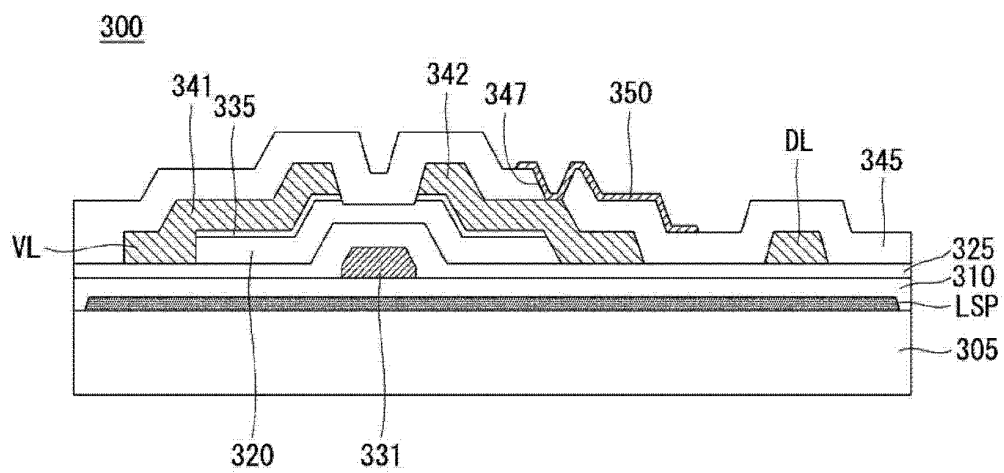


图 9E

Electronic Patent Application Fee Transmittal				
Application Number:		15838138		
Filing Date:		11-Dec-2017		
Title of Invention:		DISPLAY APPARATUS		
First Named Inventor/Applicant Name:		Yangwan Kim		
Filer:		Jun-Young E. Jeon/Yanira Vanegas		
Attorney Docket Number:		148454/411598-03044		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
Total in USD (\$)				240

Electronic Acknowledgement Receipt

EFS ID:	36603334
Application Number:	15838138
International Application Number:	
Confirmation Number:	4358
Title of Invention:	DISPLAY APPARATUS
First Named Inventor/Applicant Name:	Yangwan Kim
Customer Number:	23363
Filer:	Jun-Young E. Jeon/Yanira Vanegas
Filer Authorized By:	Jun-Young E. Jeon
Attorney Docket Number:	148454/411598-03044
Receipt Date:	16-JUL-2019
Filing Date:	11-DEC-2017
Time Stamp:	19:00:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$240
RAM confirmation Number	071719INTEFSW19015200
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		148454_IDS.pdf	36246	yes	3
			2c53b6dc26131a6668d26ee9b8f07a4d2b8ff6d		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Information Disclosure Statement (IDS) Form (SB08)		3	3	
	Transmittal Letter		1	2	
Warnings:					
Information:					
2	Foreign Reference	CN_1459656A_Abstract.pdf	2399354	no	28
			f9adbe272193be76c2967bb74b9b4722d9622e5f		
Warnings:					
Information:					
3	Foreign Reference	CN_1503041_A.pdf	5657513	no	47
			d7b1ec0db3ac2aea962440888ad61acc836851e		
Warnings:					
Information:					
4	Foreign Reference	CN_103681751_A.pdf	5200971	no	20
			02209c6745b0866a6cacee516bec8fe9397a6050		
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30585	no	2
			6e26c8fe2bb4bfa358e87b1d89e86e571575956e		
Warnings:					
Information:					

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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NOTICE OF ALLOWANCE AND FEE(S) DUE

23363 7590 05/28/2019
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2895	

DATE MAILED: 05/28/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/838,138	12/11/2017	Yangwan Kim	148454/411598-03044	4358

TITLE OF INVENTION: DISPLAY APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	08/28/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23363 7590 05/28/2019
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/838,138	12/11/2017	Yangwan Kim	148454/411598-03044	4358

TITLE OF INVENTION: DISPLAY APPARATUS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	08/28/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
COLEMAN, WILLIAM D	2895	257-071000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

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☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/838,138	12/11/2017	Yangwan Kim	148454/411598-03044	4358
23363	7590	05/28/2019	EXAMINER	
Lewis Roca Rothgerber Christie LLP			COLEMAN, WILLIAM D	
PO BOX 29001			ART UNIT	
Glendale, CA 91209-9001			PAPER NUMBER	
			2895	
DATE MAILED: 05/28/2019				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/838,138	Applicant(s) Kim et al.	
	Examiner WILLIAM D COLEMAN	Art Unit 2895	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to April 01, 2019.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2-34. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 14/660,813.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/William Coleman/ Primary Examiner, Art Unit 2895	
--	--

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 01, 2019 has been entered.

Allowable Subject Matter

1. Claims 2-34 allowed.
2. The following is an examiner's statement of reasons for allowance: the prior art does not anticipate nor render obviousness with respect to a display apparatus comprising amongst other limitations: a first signal line over the second electrode layer; and a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM D COLEMAN whose telephone number is (571)272-1856. The examiner can normally be reached on M-F Flex.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eliseo Ramos-Feliciano can be reached on 571-272-7925. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 15/838,138
Art Unit: 2895

Page 4

/William Coleman/
Primary Examiner, Art Unit 2895

<i>Search Notes</i> 	Application/Control No. 15/838,138	Applicant(s)/Patent Under Reexamination Kim et al.
	Examiner WILLIAM D COLEMAN	Art Unit 2895

CPC - Searched*		
Symbol	Date	Examiner
H01L27/3272,124,3262,3265,3276,3248	5/3/2018	SCS
G02F2001/136218,13629	5/3/2018	SCS
G02F1/136213	5/3/2018	SCS
H01L 27/3272	05/22/2019	/WDC/
H01L 27/3262	05/22/2019	/WDC/
H01L 27/3265	05/22/2019	/WDC/
H01L 27/124	05/22/2019	/WDC/
G02F 1/136213	05/22/2019	/WDC/

CPC Combination Sets - Searched*		
Symbol	Date	Examiner
G02F 2001/136218	05/22/2019	/WDC/

US Classification - Searched*			
Class	Subclass	Date	Examiner
East Text Search			

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
East Text Search of CPC H01L27/3272,124,3262,3265,3276,3248	5/3/2018	SCS
East Text Search of CPC G02F2001/136218,13629	5/3/2018	SCS
East Text Search of CPC G02F1/136213	5/3/2018	SCS
Updated East Text Search	12/14/2018	SCS

/William Coleman/ Primary Examiner, Art Unit 2895	
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<i>Search Notes</i> 	Application/Control No. 15/838,138	Applicant(s)/Patent Under Reexamination Kim et al.
	Examiner WILLIAM D COLEMAN	Art Unit 2895

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L	27/3272	05/22/2019	/WDC/

/William Coleman/ Primary Examiner, Art Unit 2895	
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Issue Classification 	Application/Control No. 15/838,138	Applicant(s)/Patent Under Reexamination Kim et al.
	Examiner WILLIAM D COLEMAN	Art Unit 2895

CPC						
Symbol					Type	Version
H01L	/	27	/	3272	F	2013-01-01
H01L	/	27	/	124	I	2013-01-01
H01L	/	27	/	3262	I	2013-01-01
H01L	/	27	/	3265	I	2013-01-01
H01L	/	27	/	3276	I	2013-01-01
G02F	/	2001	/	13629	A	2013-01-01
G02F	/	2001	/	136218	A	2013-01-01
G02F	/	1	/	136213	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	33	
/William Coleman/ Primary Examiner, Art Unit 2895	22 May 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Issue Classification 	Application/Control No. 15/838,138	Applicant(s)/Patent Under Reexamination Kim et al.
	Examiner WILLIAM D COLEMAN	Art Unit 2895

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L	/	27	/ 32
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	33	
/William Coleman/ Primary Examiner, Art Unit 2895	22 May 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Issue Classification 	Application/Control No. 15/838,138	Applicant(s)/Patent Under Reexamination Kim et al.
	Examiner WILLIAM D COLEMAN	Art Unit 2895

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	14	10	21	19	30	28								
1	2	6	11	22	20	31	29								
2	3	15	12	23	21	32	30								
3	4	16	13	24	22	8	31								
4	5	7	14	25	23	9	32								
5	6	17	15	26	24	10	33								
11	7	18	16	27	25	33	34								
12	8	19	17	28	26										
13	9	20	18	29	27										

NONE	Total Claims Allowed:	
(Assistant Examiner)	(Date)	33
/William Coleman/ Primary Examiner, Art Unit 2895	22 May 2019	O.G. Print Claim(s)
(Primary Examiner)	(Date)	1
		O.G. Print Figure
		8

CPC Classification - Application Number: 15838138**Examiner:** William Coleman **Date Created:** May 22, 2019 10:16**Family ID:** 53541555**US App. No. (2) & Documents (3):** 15/838138 (20180102401 A1), 14/660813 (20160043159 A1, 9842892 B2)**Foreign Documents (6):** CN105336295A, CN105336295B, EP2983205A1, KR20160017394A, KR101640192B1, TW201607004A**Allocations (8)**

No.	CPC	Type			Endorsed By	CPC Version	IPC
1	H01L 27/3272	F			US, EP	2013-01-01	H01L27/32
2	H01L 27/3262	I			US, EP	2013-01-01	H01L27/32
3	H01L 27/3265	I			US, EP	2013-01-01	H01L27/32
4	H01L 27/3276	I			US, EP	2013-01-01	H01L27/32
5	H01L 27/124	I			EP, US	2013-01-01	H01L27/12
6	G02F 1/136213	A			US	2013-01-01	G02F1/1362
7	G02F2001/13629	A			US	2013-01-01	G02F1/1362
8	G02F2001/136218	A			US	2013-01-01	G02F1/1362

Combination Sets (0)

No.	CPC	Type	Set	Rank	Endorsed By	CPC Version	IPC
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	("9842892").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/05/22 07:47
S2	19	("20030202267" "20040252088" "20050068310" "20070029644" "20070228389" "20090009441" "20100110050" "20110102693" "20120074423" "20120229438" "20130235020" "20140062990" "20140070184" "20140098078" "20140167009" "20150177578" "20150364500" "7046282" "8471973").PN. OR ("9842892").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/05/22 07:48
S3	0	(13/415378).APP.	USPAT; USOCR	OR	OFF	2019/05/22 07:52
S4	0	(10/387515).APP.	USPAT; USOCR	OR	OFF	2019/05/22 08:00
S5	607	(H01L27/3272).cpc.	USPAT; USOCR	OR	OFF	2019/05/22 09:11
S6	1	(H01L27/3272 and H01L27/3262 and H01L27/3265 and H01L27/124 and G02F1/136213 and G02F2001/136218).cpc.	USPAT; USOCR	OR	OFF	2019/05/22 09:39
S7	67010	(H01L27/3272 or H01L27/3262 or H01L27/3265 or H01L27/124 or G02F1/136213 or G02F2001/136218).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	OFF	2019/05/22 09:39
S8	10345	(overlapped near4 electrodes) or (overlapping adj electrodes)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	OFF	2019/05/22 09:40
S9	1267	S7 and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	OFF	2019/05/22 09:41
S10	436350	tft or thin adj film adj transistor	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2019/05/22 09:42

			EPO; JPO; DERWENT			
S11	1041	S9 and S10	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	OFF	2019/05/22 09:42
S12	55	(thin adj film adj transistor and (signal adj line or data adj line) and second adj electrode and (shield or shielding) and source and drain).clm.	US- PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	OFF	2019/05/22 12:33

5/ 22/ 2019 3:45:00 PM

C:\Users\wcoleman\Documents\EAST\Workspaces\FY2019\15838138.wsp

PATENT
RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2896

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on May 10, 2019 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Marti Carrillo/
Marti Carrillo

Appl No. : 15/838,138 Confirmation No. 4358
Inventor : Yangwan Kim, et al.
Filed : December 11, 2017
Title : DISPLAY APPARATUS

TC/A.U. : 2896
Examiner : Stephen C. Smith

Docket No. : 148454

Customer No. : 23363

SUPPLEMENTAL AMENDMENT

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
May 10, 2019

Commissioner:

This Supplemental Amendment supplements and replaces the April 1, 2019 Amendment submitted with Request for Continued Examination filed in response to the Office action of December 31, 2018. Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Electronic Patent Application Fee Transmittal				
Application Number:		15838138		
Filing Date:		11-Dec-2017		
Title of Invention:		DISPLAY APPARATUS		
First Named Inventor/Applicant Name:		Yangwan Kim		
Filer:		Kyle W. Kellar/Marti Carrillo		
Attorney Docket Number:		148454/411598-03044		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	4	100	400
INDEPENDENT CLAIMS IN EXCESS OF 3	1201	1	460	460
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				860

Electronic Acknowledgement Receipt

EFS ID:	35983814
Application Number:	15838138
International Application Number:	
Confirmation Number:	4358
Title of Invention:	DISPLAY APPARATUS
First Named Inventor/Applicant Name:	Yangwan Kim
Customer Number:	23363
Filer:	Kyle W. Kellar/Marti Carrillo
Filer Authorized By:	Kyle W. Kellar
Attorney Docket Number:	148454/411598-03044
Receipt Date:	10-MAY-2019
Filing Date:	11-DEC-2017
Time Stamp:	18:06:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$860
RAM confirmation Number	051319INTEFSW00004908031728
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		148454_Supplemental-Amendment.pdf	178346	yes	13
			4ebee0891da016547971fca87f2035907f100365		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Arguments/Remarks Made in an Amendment		10	13	
	Claims		2	9	
	Supplemental Response or Supplemental Amendment		1	1	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32053	no	2
			c5d141bfb287963991ca23b5edb1e7a9ccf7f807		
Warnings:					
Information:					
Total Files Size (in bytes):			210399		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Claim 2-34 are in the present application, and claims 2, 22, 26, and 34 are independent. Claim 1 is cancelled herein without prejudice, and claims 2-34 are added herein. Support for new claims 2-34 can be found throughout the application as filed, at least at FIGS. 2, 5, and 10-12 and corresponding text. No new matter has been introduced. Applicant respectfully requests consideration on the merits and allowance of claims 2-34.

Rejection of Claim 1 Under 35 U.S.C. § 102

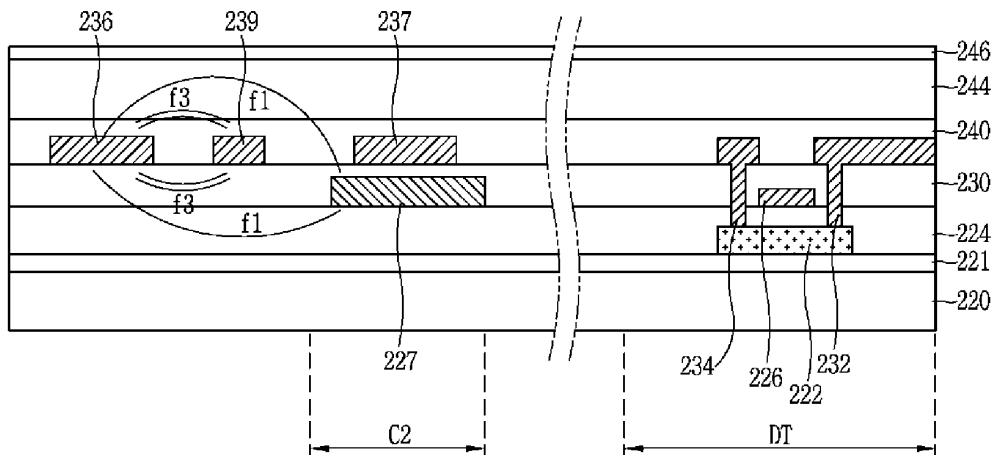
Claim 1 was rejected under 35 U.S.C. § 102(a)(2) as allegedly being anticipated by Lee et al. (U.S. Publication No. 2014/0167009).

Claim 1 has been cancelled herein without prejudice. Claim 2 has been added herein and recites:

A display apparatus comprising: a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area; a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor; a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer; a first signal line over the second electrode layer; and a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.

The cited Figure 8 of Lee (reproduced below) does not appear to disclose at least either “a first signal line over the second electrode layer” or “a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor” as recited in new claim 2.

FIG. 8



Claim 22 has been added herein and recites:

A display apparatus comprising: a first thin-film transistor comprising a first semiconductor; a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor; a first signal line over the first electrode layer; a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line; and a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

Figure 8 of Lee does not appear to disclose at least either “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line” or “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor” as recited in new claim 22.

Claim 26 has also been added herein and recites:

A display apparatus comprising: a first thin-film transistor comprising a first semiconductor; a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor; a first signal line over the first electrode layer; a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

Figure 8 of Lee does not appear to disclose at least either “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer” or “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor” as recited in new claim 26.

Claim 34 has also been added herein and recites:

A display apparatus comprising: a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area; a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor; a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer; a first signal line over the second electrode layer; and a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor, wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line, wherein the first signal line extends in a first direction, and wherein a length along the first direction of the overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction.

Lee does not appear to disclose the features of new claim 34.

Appln No. 15/838,138
Amdt date May 10, 2019
Reply to Office action of December 31, 2018

Accordingly, Applicant respectfully submits that Lee fails to disclose at least the above-discussed features of new claims 2, 22, 26, and 34. As such, Applicant respectfully submits that claims 2, 22, 26, and 34 are patentably distinguishable over Lee and respectfully requests that these claims be allowed.

Moreover, because claims 3-21 and 31-33 each depend, directly or indirectly, from claim 2, claims 23-25 each depend, directly or indirectly, from claim 22, and claims 27-30 each depend, directly or indirectly, from claim 26, these claims each incorporate all the terms and features of their respective base claim, in addition to other terms and features, which together further patentably distinguish these claims over the art of record. Therefore, Applicant respectfully requests that that these claims be allowed as well.

Concluding Remarks

In view of the foregoing amendments and remarks, Applicant earnestly solicits a timely issuance of a Notice of Allowance with claims 2-34. If there are any remaining issues that can be addressed over the telephone, the Examiner is cordially invited to call Applicant's attorney at the number listed below.

Respectfully submitted,
LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Kyle W. Kellar/
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/kwk

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)
2. (New) A display apparatus comprising:
 - a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;
 - a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;
 - a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;
 - a first signal line over the second electrode layer; and
 - a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.
3. (New) The display apparatus of claim 2, wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line.
4. (New) The display apparatus of claim 2, further comprising a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first signal line.

5. (New) The display apparatus of claim 2, further comprising a first voltage line in the same layer as the first signal line and connected to the second electrode layer.

6. (New) The display apparatus of claim 2, further comprising:
a third thin-film transistor comprising a third semiconductor, one end of the third semiconductor being connected to one end of the first semiconductor, and the other end of the third semiconductor being connected to the first electrode layer; and
a second shield layer in a layer between the first signal line and the third semiconductor and overlapping a part between a first channel area and a second channel area of the third semiconductor.

7. (New) The display apparatus of claim 6, wherein a gate electrode of the third thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the third semiconductor, and the second gate electrode overlapping the second channel area of the third semiconductor, and
wherein the gate electrode of the third thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

8. (New) The display apparatus of claim 6, further comprising a first voltage line in the same layer as the first signal line,
wherein the second shield layer is connected to the first voltage line.

9. (New) The display apparatus of claim 6, wherein the second shield layer is a part of the second electrode layer.

10. (New) The display apparatus of claim 6, further comprising a connecting line connecting the other end of the third semiconductor and the first electrode layer and being in the same layer as the first signal line .

11. (New) The display apparatus of claim 2, further comprising:
a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and
a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part of the fourth semiconductor.

12. (New) The display apparatus of claim 11, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer and overlapping the fourth semiconductor, and
wherein the third shield layer is a part of the second voltage line and overlaps a part of the fourth semiconductor between the first gate electrode and the second gate electrode.

13. (New) The display apparatus of claim 12, wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.

14. (New) The display apparatus of claim 2, further comprising:
a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and

a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part between a first channel area and a second channel area of the fourth semiconductor.

15. (New) The display apparatus of claim 14, wherein the third shield layer is a part of the second voltage line.

16. (New) The display apparatus of claim 14, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the fourth semiconductor, and the second gate electrode overlapping the second channel area of the fourth semiconductor, and

wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.

17. (New) The display apparatus of claim 14, further comprising a connecting line connecting the one end of the fourth semiconductor and the first electrode layer and being in the same layer as the first signal line .

18. (New) The display apparatus of claim 4, further comprising a fifth thin-film transistor comprising a fifth semiconductor, one end of the fifth semiconductor being connected to the one end of the first semiconductor and the one end of the second semiconductor, and the other end of the fifth semiconductor being connected to a first voltage line,

wherein the first voltage line in the same layer as the first signal line and connected to the second electrode layer.

19. (New) The display apparatus of claim 18, further comprising a fourth shield layer in a layer between the first signal line and the fifth semiconductor,

wherein the fourth shield layer overlaps a part of semiconductor between the channel area of the first semiconductor, the channel area of the second semiconductor, and the channel area of the fifth semiconductor.

20. (New) The display apparatus of claim 19, wherein the fourth shield layer is a part of the second electrode layer.

21. (New) The display apparatus of claim 20, further comprising a capacitor comprising a first capacitor plate and a second capacitor plate,

wherein the first capacitor plate is a part of the first electrode layer, and the second capacitor plate is a part of the second electrode layer.

22. (New) A display apparatus comprising:
a first thin-film transistor comprising a first semiconductor;
a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;
a first signal line over the first electrode layer;
a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line; and
a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

23. (New) The display apparatus of claim 22, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode

in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and

wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

24. (New) The display apparatus of claim 22, wherein the shield layer is a part of the voltage line.

25. (New) The display apparatus of claim 22, further comprising a connecting line connecting the one end of the second semiconductor and the first electrode layer and being in the same layer as the first signal line .

26. (New) A display apparatus comprising:
a first thin-film transistor comprising a first semiconductor;
a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;
a first signal line over the first electrode layer;
a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and
a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

27. (New) The display apparatus of claim 26, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode

in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and

wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

28. (New) The display apparatus of claim 26, further comprising a voltage line in the same layer as the first signal line,

wherein the shield layer is connected to the voltage line.

29. (New) The display apparatus of claim 26, further comprising a second electrode layer over the first electrode layer and overlapping the first electrode layer,

wherein the shield layer is a part of the second electrode layer.

30. (New) The display apparatus of claim 29, further comprising a voltage line in the same layer as the first signal line,

wherein the voltage line is connected to the second electrode layer.

31. (New) The display apparatus of claim 2, wherein the first signal line extends in a first direction, and

wherein a length along the first direction of the overlapping part of the first shield layer with the part of one of the source area and the drain area of the first semiconductor is larger than a length of the first electrode layer along the first direction.

32. (New) The display apparatus of claim 2, wherein the first shield layer fully overlaps the part of one of the source area and the drain area of the first semiconductor.

33. (New) The display apparatus of claim 2, wherein the first signal line extends in a first direction, and

wherein a length along the first direction of the overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction.

34. (New) A display apparatus comprising:

a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;

a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;

a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;

a first signal line over the second electrode layer; and

a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor,

wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line,

wherein the first signal line extends in a first direction, and

wherein a length along the first direction of the overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 15/838,138		Filing Date 12/11/2017		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
		(Column 1)			(Column 2)				
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		x \$80 =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		x \$420 =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED - PART II									
AMENDMENT		(Column 1)		(Column 2)	(Column 3)				
	05/10/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 33	Minus	** 29	= 4		x \$100 =	400	
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 3	= 1		x \$460 =	460	
	☐ Application Size Fee (37 CFR 1.16(s))								
AMENDMENT	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
							TOTAL ADD'L FEE	860	
		(Column 1)		(Column 2)	(Column 3)				
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=		x \$0 =		
AMENDMENT	Independent (37 CFR 1.16(h))	*	Minus	***	=		x \$0 =		
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
							TOTAL ADD'L FEE		
	* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE		
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/SUSAN A HAY/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**REQUEST FOR CONTINUED EXAMINATION (RCE)
TRANSMITTAL**

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on April 1, 2019 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Marti Carrillo/
Marti Carrillo

Application Number : 15/838,138	Confirmation No. 4358
Filing Date : December 11, 2017	
Inventor(s) : Yangwan Kim, et al.	
Title : DISPLAY APPARATUS	
Group Art Unit : 2896	
Examiner Name : Stephen C. Smith	
Docket No. : 148454	Date: April 1, 2019

MAIL TO: Mail Stop RCE

This is a Request for Continued Examination (RCE) under 37 CFR § 1.114 of the above-identified application.

This application is **not** an application of the kind specified in 37 CFR § 1.114(e).

1. THE STATUS OF THE APPLICATION IS AS FOLLOWS:

- a. ☒ Pending (no review proceedings active)
- (1) ☒ An Action was mailed by the Office on December 31, 2018, as to which no appeal under 37 CFR § 1.191 has been filed and
- ☐ a response under 37 CFR § 1.116 was filed on
- ☐ via Express Mail
- ☐ with certificate of electronic transmission under 37 CFR § 1.8
- ☒ that Action was a Final Rejection, the finality of which is to be withdrawn by this Request
- ☐ an appeal or civil action under 35 U.S.C. 141, 145 or 146 has been terminated
- (2) ☐ Allowed: the Notice of Allowance was mailed by the Office on
- ☐ the Issue Fee has not been paid
- ☐ the Issue Fee has been paid **and** a petition under 37 CFR § 1.313 was granted on
- b. ☐ Pending (with review proceeding active)
- An appeal under 37 CFR § 1.191 has been filed. **Applicant(s) hereby withdraw that appeal and request reopening of the prosecution of the application.**

2. SUBMISSION(S) REQUIRED (check at least one)

- a. Previously submitted
- ☐ Consider the amendments/reply under 37 CFR § 1.116 previously filed on
- ☐ Consider the arguments in the Appeal or Reply Brief previously filed on
- ☐ Other:

REQUEST FOR CONTINUED EXAMINATION (RCE)
TRANSMITTAL

Application No. 15/838,138

b. Enclosed

- ☒ Amendment/Reply
- ☐ Affidavit(s)/Declaration(s)
- ☐ Information Disclosure Statement
- ☐ Documents under 37 CFR § 1.48
- ☐ Petition for Extension of Time
- ☐ Other:

The Examiner is requested to telephone the undersigned promptly following receipt and initial review of the application in light of the Submissions(s) for the conduct of, or the scheduling of, a telephone interview in the application.

Please direct all correspondence to **CUSTOMER NUMBER 23363**. Direct telephone calls to 626/795-9900, **LEWIS ROCA ROTHGERBER CHRISTIE LLP, P.O. Box 29001, Glendale, CA 91209-9001**.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Kyle W. Kellar/

Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/mac

**REQUEST FOR CONTINUED EXAMINATION (RCE)
FEE CALCULATION SHEET**

Application No. 15/838,138

PART I -- BASIC FILING FEE							
				Large Entity Rate	Small Entity Rate	Micro Entity Rate	FEE
Basic Filing Fee				1,300.00	650.00	325.00	1,300.00
PART II -- ADDITIONAL CLAIMS (compared to application before RCE)							
	Claims Remaining After Amendment	Highest Number Paid For	Number Extra Claims	Large Entity Rate	Small Entity Rate	Micro Entity Rate	FEE
Total Claims	29 -	* 20	= 9	9 x 100.00	50.00	25.00	900.00
Independent Claims	3 -	** 3	= 0	x 460.00	230.00	115.00	0
First Presentation of Multiple Dependent Claims				820.00	410.00	205.00	0.00
TOTAL FILING FEE							\$2,200.00
LIST INDEPENDENT CLAIMS: 2, 22, 26							
* IF THE "HIGHEST NUMBER OF TOTAL CLAIMS PREVIOUSLY PAID FOR" IS 20 OR LESS, WRITE "20" IN THIS SPACE							
** IF HIGHEST NUMBER OF INDEPENDENT CLAIMS PREVIOUSLY PAID FOR IS 3 OR LESS, WRITE "3" IN THIS SPACE							

1. FEES (The RCE fee under 37 CFR § 1.17(e) is required by 37 CFR § 1.114 when the RCE is filed.)
- a. Amount (total from Fee Calculation Sheet)
- The fee of \$2,200.00 is submitted herewith.
- b. X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required for this transaction to Deposit Account No. 03-1728. Please show our docket number with any charge or credit to our Deposit Account.

MAC 107724107.2-*04/01/2019 12:27 PM

PATENT
RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2896

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on April 1, 2019 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Marti Carrillo/
Marti Carrillo

Appl No. : 15/838,138 Confirmation No. 4358
Inventor : Yangwan Kim, et al.
Filed : December 11, 2017
Title : DISPLAY APPARATUS

TC/A.U. : 2896
Examiner : Stephen C. Smith

Docket No. : 148454

Customer No. : 23363

AMENDMENT SUBMITTED WITH REQUEST FOR CONTINUED EXAMINATION

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
April 1, 2019

Commissioner:

In response to the Office action of December 31, 2018, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begin on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)
2. (New) A display apparatus comprising:
 - a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;
 - a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;
 - a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;
 - a first signal line over the second electrode layer; and
 - a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.
3. (New) The display apparatus of claim 2, wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line.
4. (New) The display apparatus of claim 2, further comprising a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first signal line.

5. (New) The display apparatus of claim 2, further comprising a first voltage line in the same layer as the first signal line and connected to the second electrode layer.

6. (New) The display apparatus of claim 2, further comprising:
a third thin-film transistor comprising a third semiconductor, one end of the third semiconductor being connected to one end of the first semiconductor, and the other end of the third semiconductor being connected to the first electrode layer; and
a second shield layer in a layer between the first signal line and the third semiconductor and overlapping a part between a first channel area and a second channel area of the third semiconductor.

7. (New) The display apparatus of claim 6, wherein a gate electrode of the third thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the third semiconductor, and the second gate electrode overlapping the second channel area of the third semiconductor, and
wherein the gate electrode of the third thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

8. (New) The display apparatus of claim 6, further comprising a first voltage line in the same layer as the first signal line,
wherein the second shield layer is connected to the first voltage line.

9. (New) The display apparatus of claim 6, wherein the second shield layer is a part of the second electrode layer.

10. (New) The display apparatus of claim 6, further comprising a connecting line connecting the one end of the third semiconductor and the first electrode layer and being in the same layer as the first signal line .

11. (New) The display apparatus of claim 2, further comprising:
a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and
a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part of the fourth semiconductor.

12. (New) The display apparatus of claim 11, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer and overlapping the fourth semiconductor, and
wherein the third shield layer is a part of the second voltage line and overlaps a part of the fourth semiconductor between the first gate electrode and the second gate electrode.

13. (New) The display apparatus of claim 12, wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.

14. (New) The display apparatus of claim 2, further comprising:
a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and

a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part between a first channel area and a second channel area of the fourth semiconductor.

15. (New) The display apparatus of claim 14, wherein the third shield layer is a part of the second voltage line.

16. (New) The display apparatus of claim 14, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the fourth semiconductor, and the second gate electrode overlapping the second channel area of the fourth semiconductor, and

wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.

17. (New) The display apparatus of claim 14, further comprising a connecting line connecting the one end of the fourth semiconductor and the first electrode layer and being in the same layer as the first signal line .

18. (New) The display apparatus of claim 4, further comprising a fifth thin-film transistor comprising a fifth semiconductor, one end of the fifth semiconductor being connected to the one end of the first semiconductor and the one end of the second semiconductor, and the other end of the fifth semiconductor being connected to a first voltage line,

wherein the first voltage line in the same layer as the first signal line and connected to the second electrode layer.

19. (New) The display apparatus of claim 18, further comprising a fourth shield layer in a layer between the first signal line and the fifth semiconductor,

wherein the fourth shield layer overlaps a part of semiconductor between the channel area of the first semiconductor, the channel area of the second semiconductor, and the channel area of the fifth semiconductor.

20. (New) The display apparatus of claim 19, wherein the fourth shield layer is a part of the second electrode layer.

21. (New) The display apparatus of claim 20, further comprising a capacitor comprising a first capacitor plate and a second capacitor plate,

wherein the first capacitor plate is a part of the first electrode layer, and the second capacitor plate is a part of the second electrode layer.

22. (New) A display apparatus comprising:
a first thin-film transistor comprising a first semiconductor;
a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;
a first signal line over the first electrode layer;
a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line; and
a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

23. (New) The display apparatus of claim 22, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode

in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and

wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

24. (New) The display apparatus of claim 22, wherein the shield layer is a part of the voltage line.

25. (New) The display apparatus of claim 22, further comprising a connecting line connecting the one end of the second semiconductor and the first electrode layer and being in the same layer as the first signal line .

26. (New) A display apparatus comprising:
a first thin-film transistor comprising a first semiconductor;
a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;
a first signal line over the first electrode layer;
a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and
a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

27. (New) The display apparatus of claim 26, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode

in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and

wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

28. (New) The display apparatus of claim 26, further comprising a voltage line in the same layer as the first signal line,

wherein the shield layer is connected to the voltage line.

29. (New) The display apparatus of claim 26, further comprising a second electrode layer over the first electrode layer and overlapping the first electrode layer,

wherein the shield layer is a part of the second electrode layer.

30. (New) The display apparatus of claim 29, further comprising a voltage line in the same layer as the first signal line,

wherein the voltage line is connected to the second electrode layer.

REMARKS/ARGUMENTS

Claim 2-30 are in the present application, and claims 2, 22, and 26 are independent. Claim 1 is cancelled herein without prejudice, and claims 2-30 are added herein. Support for new claims 2-30 can be found throughout the application as filed, at least at FIGS. 2, 5, and 10-12 and corresponding text. No new matter has been introduced. Applicant respectfully requests consideration on the merits and allowance of claims 2-30.

Rejection of Claim 1 Under 35 U.S.C. § 102

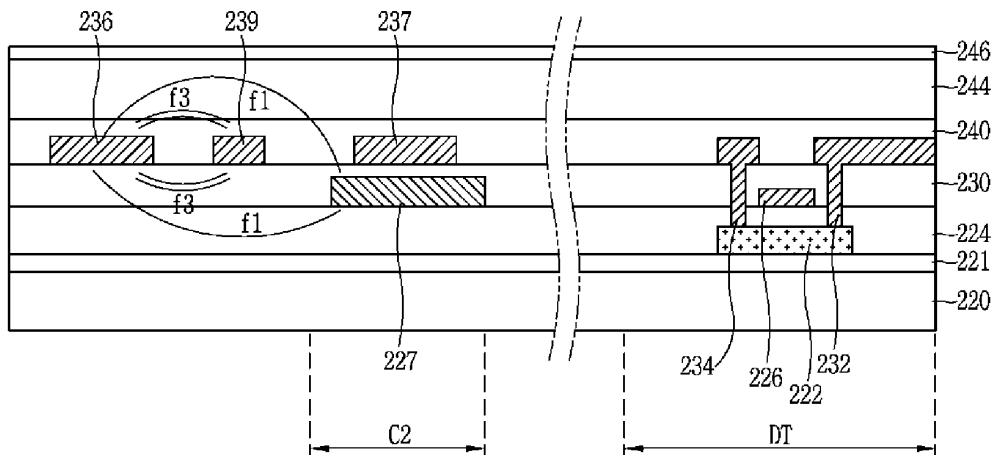
Claim 1 was rejected under 35 U.S.C. § 102(a)(2) as allegedly being anticipated by Lee et al. (U.S. Publication No. 2014/0167009).

Claim 1 has been cancelled herein without prejudice. Claim 2 has been added herein and recites:

A display apparatus comprising: a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area; a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor; a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer; a first signal line over the second electrode layer; and a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.

The cited Figure 8 of Lee (reproduced below) does not appear to disclose at least either “a first signal line over the second electrode layer” or “a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor” as recited in new claim 2.

FIG. 8



Claim 22 has been added herein and recites:

A display apparatus comprising: a first thin-film transistor comprising a first semiconductor; a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor; a first signal line over the first electrode layer; a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line; and a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

Figure 8 of Lee does not appear to disclose at least either “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line” or “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor” as recited in new claim 22.

Claim 26 has also been added herein and recites:

A display apparatus comprising: a first thin-film transistor comprising a first semiconductor; a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor; a first signal line over the first electrode layer; a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

Figure 8 of Lee does not appear to disclose at least either “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer” or “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor” as recited in new claim 26.

Accordingly, Applicant respectfully submits that Lee fails to disclose at least the above-discussed features of new claims 2, 22, and 26. As such, Applicant respectfully submits that claims 2, 22, and 26 are patentably distinguishable over Lee and respectfully requests that these claims be allowed.

Moreover, because claims 3-21 each depend, directly or indirectly, from claim 2, claims 23-25 each depend, directly or indirectly, from claim 22, and claims 27-30 each depend, directly or indirectly, from claim 26, these claims each incorporate all the terms and features of their respective base claim, in addition to other terms and features, which together further patentably distinguish these claims over the art of record. Therefore, Applicant respectfully requests that that these claims be allowed as well.

Appln No. 15/838,138
Amdt date April 1, 2019
Reply to Office action of December 31, 2018

Concluding Remarks

In view of the foregoing amendments and remarks, Applicant earnestly solicits a timely issuance of a Notice of Allowance with claims 2-30. If there are any remaining issues that can be addressed over the telephone, the Examiner is cordially invited to call Applicant's attorney at the number listed below.

Respectfully submitted,
LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Kyle W. Kellar/
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/kwk

Electronic Patent Application Fee Transmittal				
Application Number:		15838138		
Filing Date:		11-Dec-2017		
Title of Invention:		DISPLAY APPARATUS		
First Named Inventor/Applicant Name:		Yangwan Kim		
Filer:		Kyle W. Kellar/Marti Carrillo		
Attorney Docket Number:		148454/411598-03044		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	9	100	900
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
Total in USD (\$)				2200

Electronic Acknowledgement Receipt

EFS ID:	35590666
Application Number:	15838138
International Application Number:	
Confirmation Number:	4358
Title of Invention:	DISPLAY APPARATUS
First Named Inventor/Applicant Name:	Yangwan Kim
Customer Number:	23363
Filer:	Kyle W. Kellar/Marti Carrillo
Filer Authorized By:	Kyle W. Kellar
Attorney Docket Number:	148454/411598-03044
Receipt Date:	01-APR-2019
Filing Date:	11-DEC-2017
Time Stamp:	15:35:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$2200
RAM confirmation Number	040219INTEFSW15363600
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	148454_RCE.pdf	194943	no	3
			083f49734c3f055faa35206a35b5a8799287262c		
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
2		148454_Amendment.pdf	173377	yes	12
			e6f1fb4901404280861c406e954aaae8e6a865e8		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Claims		2	8	
	Applicant Arguments/Remarks Made in an Amendment		9	12	
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31978	no	2
			d997facd1ab24f79293f6977c88fe7dce11522f5		
Warnings:					
Information:					
Total Files Size (in bytes):			400298		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 15/838,138		Filing Date 12/11/2017		☐ To be Mailed					
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO													
APPLICATION AS FILED - PART I													
		(Column 1)	(Column 2)										
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)		FEE (\$)						
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A								
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A								
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A								
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 = *		x \$80 =									
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 = *		x \$420 =									
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL							
APPLICATION AS AMENDED - PART II													
		(Column 1)	(Column 2)		(Column 3)								
AMENDMENT	04/01/2019	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)				
	Total (37 CFR 1.16(i))	* 29	Minus	** 20	= 9		x \$100 =		900				
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x \$460 =		0				
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
								TOTAL ADD'L FEE		900			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)				
	Total (37 CFR 1.16(i))	*	Minus	**	=		x \$0 =						
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x \$0 =						
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
								TOTAL ADD'L FEE		LIE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.													
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".													
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".													
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.													

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 15/838,138		Filing Date 12/11/2017		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
		(Column 1)			(Column 2)				
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		x \$80 =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		x \$420 =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED - PART II									
AMENDMENT		(Column 1)		(Column 2)	(Column 3)				
	04/01/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 29	Minus	** 20	= 9		x \$100 =	900	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x \$460 =	0	
	☐ Application Size Fee (37 CFR 1.16(s))								
AMENDMENT	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
							TOTAL ADD'L FEE	900	
		(Column 1)		(Column 2)	(Column 3)				
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=		x \$0 =		
AMENDMENT	Independent (37 CFR 1.16(h))	*	Minus	***	=		x \$0 =		
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
							TOTAL ADD'L FEE		
	* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE		
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/JERMAINE D MINOR/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".									
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/838,138	12/11/2017	Yangwan Kim	148454/411598-03044	4358
23363	7590	12/31/2018		
Lewis Roca Rothgerber Christie LLP				
PO BOX 29001				
Glendale, CA 91209-9001				
EXAMINER				
SMITH, STEPHEN C				
ART UNIT		PAPER NUMBER		
2896				
NOTIFICATION DATE		DELIVERY MODE		
12/31/2018		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pair_cph@firsttofile.com

pto@lrrc.com

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This action is responsive to the amendments and arguments for U.S. Patent Application No. 15/838,138 filed on November 16, 2018. In this paper, claim 1 is amended.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on October 24, 2018 was filed and the submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claim 1 rejected under 35 U.S.C. 102(a)(2) as being anticipated by Lee et al. (US Patent Application Publication No. 2014/0167009).

In claim 1, Lee discloses (see Fig. 8) "a display apparatus comprising: a thin-film transistor (**DT**) comprising a first electrode (**232**), a second electrode (**234**), and a third electrode (**226**); a data line (**236**)

in a layer different from the first electrode (**232**), the second electrode (**234**), and the third electrode (**226**), wherein the data line (**236**) is configured to transmit a data signal; and a shield layer (**239**) between the data line (**236**) and a component of the thin-film transistor (**DT**).” Para. 0096-97.

Response to Arguments

Applicant's arguments filed for claim 1 have been fully considered but they are not persuasive.

Applicant argues that:

As can be seen at least in the cited Figure 8 of Lee (reproduced below), the data line 236 is not "in a layer different from" the alleged first and second electrodes 232/234. More specifically, Lee states that:

[0094]An interlayer insulation layer 230 is formed on an upper layer of the gate electrode 226, and a source electrode 232 and a drain electrode 234 of the driving thin-film transistor (DT) are formed on an upper layer of the 230. Furthermore, a data line 236 is formed in a second direction on the same layer.

Lee, paragraph [0094] (emphasis added).

Applicant's Remarks, pg. 3.

Examiner respectfully disagrees. Electrodes (**234, 232, 226**) are formed in the layers (**230, 224**) and connect to the wires in layer (**240**). The electrodes (**234, 232, 226**) are below the data line (**236**) and in different layers (**224, 230**) than the data line (**236**). The amended claim does not say wires that control the signals to the transistor. Besides electrodes (**234, 232**) are shown in Fig. 8 as being in the layer (**224**). Fig. 8.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The IDS submitted on October 24, 2018, includes a reference US Patent No. 9,953,572, which is a divisional Application 13/415,378, published as 2012/0229438, Fig. 5. and anticipates the claimed invention. Para. 0081.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN C SMITH whose telephone number is (313)446-4914. The examiner can normally be reached on 7:30-4:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer

Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. C. S./
Examiner, Art Unit 2896

/CHEUNG LEE/
Primary Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 15/838,138	Applicant(s)/Patent Under Reexamination Kim et al.	
	Examiner STEPHEN C SMITH	Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20120229438-A1	09-2012	FUJITA; Shin	G09G3/3233	345/211
	B					
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 15/838,138	Applicant(s)/Patent Under Reexamination Kim et al.
	Examiner STEPHEN C SMITH	Art Unit 2896

CPC - Searched*		
Symbol	Date	Examiner
H01L27/3272,124,3262,3265,3276,3248	5/3/2018	SCS
G02F2001/136218,13629	5/3/2018	SCS
G02F1/136213	5/3/2018	SCS

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
East Text Search			

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
East Text Search of CPC H01L27/3272,124,3262,3265,3276,3248	5/3/2018	SCS
East Text Search of CPC G02F2001/136218,13629	5/3/2018	SCS
East Text Search of CPC G02F1/136213	5/3/2018	SCS
Updated East Text Search	12/14/2018	SCS

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

	/STEPHEN C SMITH/ Examiner.Art Unit 2896
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4	"9953572"	USPAT	OR	OFF	2018/12/17 07:59
L2	1	"20170004767"	USPAT	OR	OFF	2018/12/17 08:02
L3	0	"20120229438"	USPAT	OR	OFF	2018/12/17 08:06
L4	0	"20120229438"	USPAT	OR	OFF	2018/12/17 08:08
L5	1	"20120229438"	US-PGPUB; USPAT	ADJ	OFF	2018/12/17 08:09
S1	10	Kim Yangwan.inv.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 14:19
S2	5	Kwak Wonkyu.inv.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 14:34
S3	1	Noh Jaedu.inv.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 14:37
S4	27	Lee Jaeyong.inv.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 14:37
S5	13026	Samsung Display	US-PGPUB; USPAT	ADJ	ON	2016/06/29 15:25
S6	1568	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer).clm.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 15:27
S7	42	S6 and S5	US-PGPUB; USPAT	ADJ	ON	2016/06/29 15:27
S8	11	("20110102693" "20120074423" "20090009441" "20140062990" "20120229438" "20140098078" "20140167009" "20130235020" "20050068310" "20100110050" "20140070184").PN.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 15:58
S9	12916	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 16:27
S10	1568	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode).clm.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 16:31
S11	147	S9 and S10	US-PGPUB;	ADJ	ON	2016/06/29 16:31

			USPAT			
S12	1	"20160043159"	US-PGPUB; USPAT	ADJ	ON	2016/06/30 07:05
S13	1607	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate)	US-PGPUB; USPAT	ADJ	ON	2016/06/30 08:24
S14	12971	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/06/30 08:25
S15	274	S14 and S13	US-PGPUB; USPAT	ADJ	ON	2016/06/30 08:25
S16	1607	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate)	US-PGPUB; USPAT	ADJ	ON	2016/06/30 14:13
S17	12971	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/06/30 14:13
S18	274	S17 and S16	US-PGPUB; USPAT	ADJ	ON	2016/06/30 14:13
S19	1212	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate) and capacitor	US-PGPUB; USPAT	ADJ	ON	2016/07/12 16:04
S20	13036	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/07/12 16:05
S21	225	S20 and S19	US-PGPUB; USPAT	ADJ	ON	2016/07/12 16:05
S22	13036	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/07/13 08:49
S23	56	(TFT or thin-film transistor or thin film transistor) and (data) and (shield electrode) and (two gate or second gate) and capacitor	US-PGPUB; USPAT	ADJ	ON	2016/07/14 11:17
S24	220	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate) and capacitor and (driving (TFT or thin-film transistor or thin film transistor))	US-PGPUB; USPAT	ADJ	ON	2016/07/14 15:46
S25	13064	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/07/14 15:46
S26	66	S25 and S24	US-PGPUB; USPAT	ADJ	ON	2016/07/14 15:46
S27	154	S24 not S26	US-PGPUB; USPAT	ADJ	ON	2016/07/14 16:13
S28	1	"20070228389"	US-	ADJ	ON	2016/07/18

			PGPUB; USPAT			11:13
S29	1283	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate) and capacitor	US- PGPUB; USPAT	ADJ	ON	2016/11/18 13:05
S30	14366	H01L27/3272,124,3262,3265,3276.cpc.	US- PGPUB; USPAT	ADJ	ON	2016/11/18 13:06
S31	259	S29 and S30	US- PGPUB; USPAT	ADJ	ON	2016/11/18 13:06
S32	14702	H01L27/3272,124,3262,3265,3276.cpc.	US- PGPUB; USPAT	ADJ	ON	2016/12/20 09:34
S33	1296	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate) and capacitor	US- PGPUB; USPAT	ADJ	ON	2016/12/20 09:35
S34	33345	(H01L27/3272,124,3262,3265,3276 or H01L23/5222,5223,5225 or H01L2225/06537or H01L2924/3025).cpc.	US- PGPUB; USPAT	ADJ	ON	2016/12/20 09:59
S35	314	S33 and S34	US- PGPUB; USPAT	ADJ	ON	2016/12/20 09:59
S36	33449	(H01L27/3272,124,3262,3265,3276 or H01L23/5222,5223,5225 or H01L2225/06537or H01L2924/3025).cpc.	US- PGPUB; USPAT	ADJ	ON	2016/12/29 08:25
S37	1515	S36 and ((electrical or electromagnetic or electro-magenetic or electric) adj2 (shield or protect\$3))	US- PGPUB; USPAT	ADJ	ON	2016/12/29 08:28
S38	102	S37 and (TFT or thin film transistor)	US- PGPUB; USPAT	ADJ	ON	2016/12/29 08:29
S39	35203	((electrical or electromagnetic or electro-magenetic or electric) adj2 (shield or protect\$3))	US- PGPUB; USPAT	ADJ	ON	2016/12/29 14:37
S40	1219	S39 and (TFT or thin film transistor)	US- PGPUB; USPAT	ADJ	ON	2016/12/29 14:38
S41	1219	S39 and (TFT or thin-film transistor or thin film transistor)	US- PGPUB; USPAT	ADJ	ON	2016/12/29 14:39
S42	886	S41 and (data or data line)	US- PGPUB; USPAT	ADJ	ON	2016/12/29 14:40
S43	613	S42 and capacitor	US- PGPUB; USPAT	ADJ	ON	2016/12/29 14:40
S44	30	S41 and (data or data line) near3 insulat\$3	US- PGPUB; USPAT	ADJ	ON	2016/12/29 14:41
S45	38	thin-film transistor and data line and source electrode and gate electrode and drain electrode and shield layer	US- PGPUB; USPAT	ADJ	ON	2016/12/29 15:08

S46	205	thin-film transistor and data line and source electrode and gate electrode and drain electrode and shield\$3 layer	US-PGPUB; USPAT	ADJ	ON	2016/12/29 15:19
S47	167	S46 not S45	US-PGPUB; USPAT	ADJ	ON	2016/12/29 15:29
S48	2	"20070029644"	US-PGPUB; USPAT	ADJ	ON	2017/03/21 13:25
S49	4	("5811846").PN. OR ("7358532").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/03/21 13:25
S50	1	thin-film transistor and data line and source electrode and gate electrode and drain electrode and (electromagnetic adj shield\$3 layer)	US-PGPUB; USPAT	ADJ	ON	2017/03/21 13:29
S51	1	thin-film transistor and data line and source and gate electrode and drain and (electromagnetic adj shield\$3 layer)	US-PGPUB; USPAT	ADJ	ON	2017/03/21 14:04
S52	2	thin-film transistor and data line and (electromagnetic adj shield\$3 layer)	US-PGPUB; USPAT	ADJ	ON	2017/03/21 14:04
S53	1679	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode).clm.	US-PGPUB; USPAT	ADJ	ON	2017/03/24 10:21
S54	4419	H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or G02F1/136213.cpc.	US-PGPUB; USPAT	ADJ	ON	2017/03/24 10:35
S55	102	S53 and S54	US-PGPUB; USPAT	ADJ	ON	2017/03/24 10:35
S56	13746	Electr\$3 with shield\$3 and TFT	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:01
S57	8946	Electr\$3 with shield\$3 and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:03
S58	16665	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:03
S59	16665	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:04
S60	8946	Electr\$3 with shield\$3 and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:05
S61	1350	S59 and S60	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:18
S62	4442	Electr\$3 near3 shield\$3 and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:18
S63	641	S59 and S62	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:19

S64	22540	(H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or G02F1/136213).cpc.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:01
S65	8966	Electr\$3 with shield\$3 and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:01
S66	2375	S64 and S65	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:02
S67	85311	Electr\$3 with (electrode or shield\$3) and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:03
S68	5	Electr\$3 with (shield) and TFT and (data or data line) same (directly adj overlap\$4)	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:05
S69	21	Electr\$3 with (shield) and TFT and (data or data line) and (directly adj overlap\$4)	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:06
S70	0	Samsung Display "Co.", ltd.as,aanm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:09
S71	0	Samsung Display, ltd.as,aanm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:10
S72	17788	Samsung Display CO ltd.as,aanm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:10
S81	22584	(H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or G02F1/136213).cpc.	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:19
S82	22358	S81 and (display or LCD)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:27
S83	17849	S82 and (TFT or thin\$film transistor)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:28
S84	12918	S83 and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:29
S85	46	S83 and (electric\$7 adj shield)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:34
S86	31	S84 and (electric\$7 adj shield)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:35
S87	15	S85 not S86	US-PGPUB; USPAT	ADJ	ON	2017/07/20 11:28
S88	2	"20140138651"	US-PGPUB; USPAT	ADJ	ON	2017/07/20 12:09
S89	2	"20130248933"	US-PGPUB; USPAT	ADJ	ON	2017/07/20 12:11
S90	1	"20030202267"	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:05

S91	1	"20050068310"	USPAT	OR	OFF	2018/05/03 09:08
S92	1	"20100110050"	USPAT	OR	OFF	2018/05/03 09:13
S93	1	"20120074423"	USPAT	OR	OFF	2018/05/03 09:14
S94	2	"20120074423"	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:14
S95	1	"20120229438"	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:16
S96	2	"20130235020"	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:22
S97	1	"20140062990"	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:24
S98	2	"20140070184"	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:25
S99	0	(thin\$film transistor or TFT) and source electrode and drain electrode and gate electrode and data line and shield layer.clm.	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:30
S100	25371	(H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or G02F1/136213).cpc.	US- PGPUB; USPAT	ADJ	ON	2018/05/03 09:38
S101	0	(thin\$film transistor or TFT) and source electrode and drain electrode and gate electrode and data line and shield layer	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:39
S102	56	(thin\$film transistor or TFT) and source electrode and drain electrode and gate electrode and data line and shield layer.clm.	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:39
S103	205	(thin\$film transistor or TFT) and source electrode and drain electrode and gate electrode and data line and shield layer	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 09:59
S104	93	S100 and S103	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 10:00
S105	112	S103 not S104	US- PGPUB; USPAT	ADJ	OFF	2018/05/03 10:47

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S73	14	(Electr\$3 with shield\$3) and (directly adj overlap) and (TFT or thin\$film) and (data or data line).clm.	US- PGPUB; USPAT	ADJ	ON	2017/07/19 12:59
S74	22540	(H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or G02F1/136213).cpc.	US- PGPUB; USPAT	ADJ	ON	2017/07/19 13:00
S75	17788	Samsung Display CO Ltd.as,aanm.	US- PGPUB; USPAT	ADJ	ON	2017/07/19 15:10
S76	0	S73 and S75	US-	ADJ	ON	2017/07/19

			PGPUB; USPAT			15:11
S77	1217	(Electr\$3 with shield\$3) and (TFT or thin\$film) and connect\$4 same layer same (data or data line).clm.	US- PGPUB; USPAT	ADJ	ON	2017/07/19 15:24
S78	92	(Electr\$3 with shield\$3) same second insulat\$3 and (TFT or thin\$film) and connect\$4 same layer same (data or data line).clm.	US- PGPUB; USPAT	ADJ	ON	2017/07/19 15:25
S79	56	S74 and S78	US- PGPUB; USPAT	ADJ	ON	2017/07/19 15:26
S80	5	(Electr\$3 with shield\$3) same second insulat\$3 and (TFT or thin\$film) and capacitor and (data or data line) near3 layer near3 source.clm.	US- PGPUB; USPAT	ADJ	ON	2017/07/19 16:02

12/ 17/ 2018 8:26:27 AM

C:\Users\ssmith4\Documents\EAST\Workspaces\15838138.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Attorney Docket Number	148454
	Application Number	15/838,138
	Filing Date	December 11, 2017
	Inventor(s)	Yangwan Kim, et al.
	Group Art Unit	2896
	Examiner Name	STEPHEN C. SMITH

U.S. PATENT DOCUMENTS				
EXAMINER INITIALS	Cite No. ¹	DOCUMENT NUMBER Number - Kind Code ² (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		9,953,572 B2	04-24-2018	Fujita

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
		CN 102682697 A	09-19-2012	Fujita	Corresponds to U.S. 9,953,572 B2, listed above

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EG 106360576.1-* -10/23/2018 3:19 PM

EXAMINER SIGNATURE	/STEPHEN C SMITH/	DATE CONSIDERED	12/17/2018
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³ Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.			

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on November 16, 2018 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Sheila R. Harter/
Sheila R. Harter

Appl No. : 15/838,138
Inventor : Yangwan Kim, et al.
Filed : December 11, 2017
Title : DISPLAY APPARATUS

Confirmation No. 4358

TC/A.U. : 2896
Examiner : Stephen C. Smith

Docket No. : 148454
Customer No. : 23363

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
November 16, 2018

Commissioner:

In response to the Office action of May 18, 2018, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
PETITION FOR EXTENSION OF TIME
FROM THE OFFICE ACTION**

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on November 16, 2018 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Sheila R. Harter/
Sheila R. Harter

Inventor(s) : Yangwan Kim, et al.
Application No. : 15/838,138
Filed : December 11, 2017
Title : DISPLAY APPARATUS

Confirmation No. 4358

Grp./Div. : 2896
Examiner : Stephen C. Smith

Docket No. : 148454

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
November 16, 2018

Commissioner:

Applicant petitions the Commissioner to extend the time for response to the Office action dated May 18, 2018 for three month(s) from August 18, 2018 to November 18, 2018.

The fee for extension of time required by 37 CFR § 1.17 is calculated below.

FEE CALCULATION			
LENGTH OF EXTENSION	LARGE ENTITY	SMALL ENTITY	FEE
WITHIN FIRST MONTH	\$200.00	\$100.00	
WITHIN SECOND MONTH	\$600.00	\$300.00	
WITHIN THIRD MONTH	\$1,400.00	\$700.00	\$1,400.00
WITHIN FOURTH MONTH	\$2,200.00	\$1,100.00	
WITHIN FIFTH MONTH	\$3,000.00	\$1,500.00	

Submitted herewith is the fee of \$1,400.00 to cover the cost of the extension.

Petition for Extension of Time
Application No. 15/838,138

The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper to Deposit Account No. 03-1728. Please show our docket number with any charge or credit to our Deposit Account.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Kyle W. Kellar/

Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/srh

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
AMENDMENT TRANSMITTAL LETTER

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on November 16, 2018 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Sheila R. Harter/
Sheila R. Harter

Inventor : Yangwan Kim, et al.
Application No. : 15/838,138
Filed : December 11, 2017
Title : DISPLAY APPARATUS

Confirmation No. 4358

Grp./Div. : 2896
Examiner : Stephen C. Smith

Docket No. : 148454

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
November 16, 2018

Commissioner:

Enclosed is an amendment to the above-identified application.

CLAIMS AS AMENDED							
	Claims Remaining After Amendment	Highest Number Previously Paid For	Number Extra Claims	Large Entity Rate	Small Entity Rate	Micro Entity Rate	FEE
Total Claims	1 -	* 20	= 0	0 x \$100.00	\$50.00	\$25.00	\$0.00
Independent Claims	1 -	** 3	= 0	0 x \$460.00	\$230.00	\$115.00	\$0.00
Multiple Dependent Claims***				\$820.00	\$410.00	\$205.00	\$0.00
Total Additional Fee							\$0.00
List Independent Claims: 1							
* If the "Highest Number of Total Claims Previously Paid For" is less than 20, enter "20" in this space							
** If the "Highest Number of Independent Claims Previously Paid For" is less than 3, enter "3" in this space							
*** Pay this fee only when "Multiple Dependent Claims" are added for the first time							

 X No additional fee is required.
 X A Petition for Extension of Time and the required fee are enclosed.
_____ Other enclosures: _____

Amendment Transmittal Letter
Application No. 15/838,138

The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by or to give effect to this paper to Deposit Account No. 03-1728. Please show our docket number with any charge or credit to our Deposit Account.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Kyle W. Kellar/

Kyle W. Kellar

Reg. No. 71,165

626/795-9900

KWK/srh

Electronic Patent Application Fee Transmittal				
Application Number:		15838138		
Filing Date:		11-Dec-2017		
Title of Invention:		DISPLAY APPARATUS		
First Named Inventor/Applicant Name:		Yangwan Kim		
Filer:		Kyle W. Kellar/sheila harter		
Attorney Docket Number:		148454/411598-03044		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 3 months with \$0 paid	1253	1	1400	1400
Miscellaneous:				
Total in USD (\$)				1400

Electronic Acknowledgement Receipt

EFS ID:	34339431
Application Number:	15838138
International Application Number:	
Confirmation Number:	4358
Title of Invention:	DISPLAY APPARATUS
First Named Inventor/Applicant Name:	Yangwan Kim
Customer Number:	23363
Filer:	Kyle W. Kellar/sheila harter
Filer Authorized By:	Kyle W. Kellar
Attorney Docket Number:	148454/411598-03044
Receipt Date:	16-NOV-2018
Filing Date:	11-DEC-2017
Time Stamp:	20:36:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1400
RAM confirmation Number	111918INTEFSW20375500
Deposit Account	031728
Authorized User	Kyle Kellar
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		148454Filing.pdf	64633	yes	8
			cfa4730a33eea2d183c9b30184d3aabbfcf72329		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Arguments/Remarks Made in an Amendment		7	8	
	Claims		6	6	
	Amendment/Req. Reconsideration-After Non-Final Reject		5	5	
	Extension of Time		3	4	
	Transmittal Letter		1	2	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30275	no	2
			44d2bd399ee99c8b19d057a75fe808d06538481b		
Warnings:					
Information:					
Total Files Size (in bytes):			94908		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS/ARGUMENTS

Claim 1 remains in the present application, and claim 1 is independent. Claim 1 is amended herein. No new matter has been introduced. Applicant respectfully requests reconsideration and allowance of claim 1.

Rejection of Claims 1, 3, 5, 7, and 9 Under 35 U.S.C. § 102

Claim 1 was rejected under 35 U.S.C. § 102(a)(2) as allegedly being anticipated by Lee et al. (U.S. Publication No. 2014/0167009).

Claim 1 is amended herein and now recites (emphasis added):

A display apparatus comprising: a thin-film transistor comprising a first electrode, a second electrode, and a third electrode; a data line in a layer different from the first electrode, the second electrode, and the third electrode, wherein the data line is configured to transmit a data signal; and a shield layer between the data line and a component of the thin-film transistor.

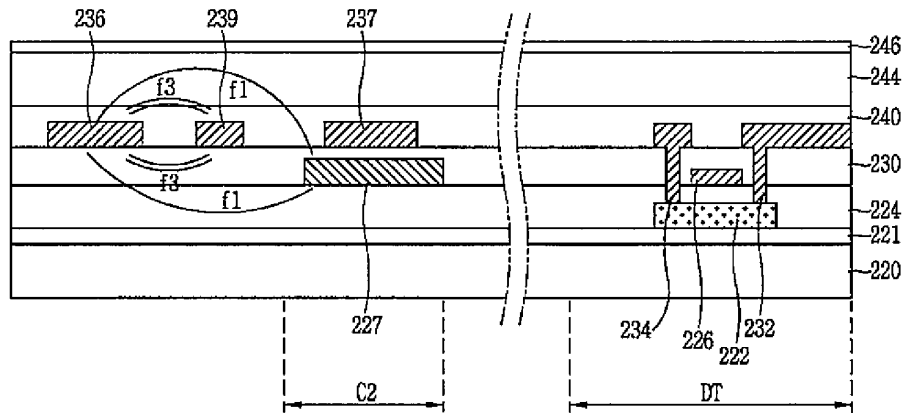
In rejecting claim 1, the Office action appears to equate the source electrode 232 of Lee with the now-recited first electrode, the second 234 of Lee with the now-recited second electrode, and the data line 236 of Lee with the recited data line. Office action, page 3.

As can be seen at least in the cited Figure 8 of Lee (reproduced below), the data line 236 is *not* "in a layer different from" the alleged first and second electrodes 232/234. More specifically, Lee states that:

[0094] An interlayer insulation layer 230 is formed on an upper layer of the gate electrode 226, and *a source electrode 232 and a drain electrode 234 of the driving thin-film transistor (DT) are formed on an upper layer of the 230. Furthermore, a data line 236 is formed in a second direction on the same layer.*

Lee, paragraph [0094] (*emphasis added*).

FIG. 8



Accordingly, Applicant respectfully submits that Lee fails to disclose at least the above-discussed features of amended claim 1. As such, Applicant respectfully submits that claim 1 is patentably distinguishable over Lee and respectfully requests that the rejection of claim 1 be withdrawn and that claim 1 be allowed.

Concluding Remarks

In view of the foregoing amendments and remarks, Applicant earnestly solicits a timely issuance of a Notice of Allowance with claim 1. If there are any remaining issues that can be addressed over the telephone, the Examiner is cordially invited to call Applicant's attorney at the number listed below.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Kyle W. Kellar/
Kyle W. Kellar
Reg. No. 71,165
626/795-9900

KWK/kwk

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A display apparatus comprising:
a thin-film transistor comprising a first source electrode, a second drain electrode, and a third gate electrode;
a data line in a layer different from the first source electrode, the second drain electrode, and the third gate electrode, wherein the data line is configured to transmit a data signal; and
a shield layer between the data line and a component of the thin-film transistor.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 15/838,138		Filing Date 12/11/2017		☐ To be Mailed		
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO										
APPLICATION AS FILED - PART I										
		(Column 1)			(Column 2)					
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		x \$80 =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		x \$420 =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL				
APPLICATION AS AMENDED - PART II										
AMENDMENT		(Column 1)		(Column 2)	(Column 3)					
	11/16/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	* 1	Minus	** 20	= 0	x \$100 =		0		
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x \$460 =		0		
	☐ Application Size Fee (37 CFR 1.16(s))									
AMENDMENT	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
							TOTAL ADD'L FEE		0	
		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =				
Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =					
☐ Application Size Fee (37 CFR 1.16(s))										
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
						TOTAL ADD'L FEE				
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						SLIE				
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/NICHELE D PETERSON/				
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".										
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Attorney Docket Number	148454
	Application Number	15/838,138
	Filing Date	December 11, 2017
	Inventor(s)	Yangwan Kim, et al.
	Group Art Unit	2896
	Examiner Name	STEPHEN C. SMITH

U.S. PATENT DOCUMENTS				
EXAMINER INITIALS	Cite No. ¹	DOCUMENT NUMBER Number - Kind Code ² (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		9,953,572 B2	04-24-2018	Fujita

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
		CN 102682697 A	09-19-2012	Fujita	Corresponds to U.S. 9,953,572 B2, listed above

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

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EXAMINER SIGNATURE	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³ Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.	

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Sheet 1 of 1

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on October 24, 2018 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.



Elizabeth Gomez

Inventor(s) : Yangwan Kim, et al.
Application No. : 15/838,138
Filed : December 11, 2017
Title : DISPLAY APPARATUS

Confirmation No. 4358

Grp./Div. : 2896
Examiner : STEPHEN C. SMITH

Docket No. : 148454

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT AND
CERTIFICATION UNDER § 1.97(e)(1)**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
October 24, 2018

Commissioner:

In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, and in accordance with the provisions in the Manual of Patent Examining Procedure §§ 609 and 707.05(b), enclosed is an information disclosure statement with a listing of references that are known to applicant. A copy of the listed Foreign Patent Documents reference is enclosed.

It is respectfully requested that these references be considered in the examination of this application and identified on the list of references cited on the patent issuing on this application. Applicant also requests that an initialed copy of the information disclosure statement be entered in the application file and returned to applicant with the next communication from the Office in accordance with MPEP § 609.

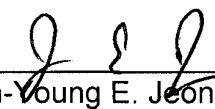
Application No. 15/838,138

Applicant's undersigned attorney hereby certifies, in accordance with 37 CFR § 1.97(e)(1), that each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement.

The Commissioner is hereby authorized to charge any fees which may be required by this paper to Deposit Account No. 03-1728. Please show our docket number with any Deposit Account transaction.

Respectfully submitted,

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By 
Jun-Young E. Jeon
Reg. No. 43,693
626/795-9900

JEJ/eg

Enclosures: Information Disclosure Statement w/references

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(51) Int. Cl.

G09G 3/32 (2006.01)

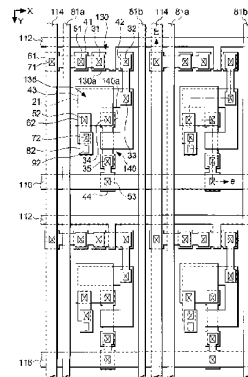
权利要求书 2 页 说明书 15 页 附图 20 页

(54) 发明名称

电光学装置以及电子设备

(57) 摘要

一种电光学装置,使不易受到起因于数据线(114)的电位变动的噪声的影响,而对流过发光元件(150)的电流进行控制。具有相互交叉的扫描线(112)以及数据线(114)、与上述交叉对应地设置的像素电路(110)以及屏蔽配线(81a、81b)。像素电路(110)具备:发光元件(150);对流过发光元件(150)的电流进行控制的晶体管(140);以及在晶体管(140)的栅极结点(g)和数据线(114)之间,根据供给至扫描线(112)的扫描信号被控制导通状态的晶体管(130),屏蔽配线(81a、81b)在俯视时设置于数据线(114)和晶体管(140)之间。



1. 一种电光学装置,包括:
扫描线;
数据线,所述数据线与所述扫描线相交;
配线,所述配线被施加恒定电位;
发光元件;
驱动晶体管,所述驱动晶体管控制流过所述发光元件的电流,所述驱动晶体管具有第一端和第二端,所述第一端连接至所述发光元件;
开关晶体管,所述开关晶体管连接在所述驱动晶体管的栅极和所述数据线之间,并且根据通过所述扫描线提供的扫描信号来控制所述开关晶体管的导通状态;以及
保持电容器,所述保持电容器具有连接至所述驱动晶体管的第一端的第一电极,
在俯视图中所述配线与所述保持电容器的第一电极的至少一部分重叠。
2. 根据权利要求1所述的电光学装置,
所述驱动晶体管是N沟道型晶体管。
3. 根据权利要求1所述的电光学装置,
所述保持电容器连接在所述驱动晶体管的第一端和所述驱动晶体管的栅极之间。
4. 根据权利要求1所述的电光学装置,在横截面图中所述配线被设置在所述驱动晶体管和所述数据线之间。
5. 根据权利要求1所述的电光学装置,
所述配线和所述数据线之间的距离短于所述配线和所述驱动晶体管之间的距离。
6. 根据权利要求1所述的电光学装置,还包括第一电源线和第二电源线,
所述发光元件和所述驱动晶体管在所述第一电源线和所述第二电源线之间的路径中彼此串联连接,以及
所述配线连接至所述第一电源线和所述第二电源线之一。
7. 根据权利要求6所述的电光学装置,
所述配线具有与所述第一电源线和所述第二电源线之一连接的部分。
8. 根据权利要求1所述的电光学装置,
所述配线与所述数据线平行。
9. 根据权利要求1所述的电光学装置,还包括另一配线以及与所述数据线紧邻的另一数据线,
在俯视图中,所述另一配线被设置在所述驱动晶体管和所述另一数据线之间,所述数据线和所述另一数据线被设置在所述驱动晶体管的相反两侧。
10. 根据权利要求1所述的电光学装置,
在俯视图中所述配线与所述驱动晶体管的第一端重叠。
11. 根据权利要求1所述的电光学装置,
所述配线含有屏蔽功能。
12. 根据权利要求1所述的电光学装置,
所述配线减少噪声对所述保持电容器的第一电极的电位的影响,所述噪声是由所述数据线的电位波动导致的。
13. 根据权利要求1所述的电光学装置,还包括连接至驱动晶体管的第一端和所述发

光元件的中继电极，

所述配线具有开口，

所述中继电极被设置在所述配线的开口之中。

14. 一种电光学装置，包括：

扫描线；

数据线，所述数据线与所述扫描线相交；

配线，所述配线被施加恒定电位；

发光元件；

驱动晶体管，所述驱动晶体管控制流过所述发光元件的电流，所述驱动晶体管具有第一端和第二端，所述第一端连接至所述发光元件；

开关晶体管，所述开关晶体管连接在所述驱动晶体管的栅极和所述数据线之间，并且根据通过所述扫描线提供的扫描信号来控制所述开关晶体管的导通状态；以及

在俯视图中所述配线与所述驱动晶体管的第一端重叠。

15. 一种电子设备，包括根据权利要求 1 所述的电光学装置。

16. 一种电子设备，包括根据权利要求 14 所述的电光学装置。

电光学装置以及电子设备

技术领域

[0001] 本发明涉及电光学装置以及电子设备。

背景技术

[0002] 近年来,提出了各种使用了有机发光二极管(Organic Light Emitting Diode,以下称为“OLED”)等发光元件的电光学装置。在这种电光学装置中,与扫描线和数据线的交叉相对应地设置像素电路。该像素电路一般构成为包含上述发光元件、开关晶体管和驱动晶体管(参照专利文献1)。这里,开关晶体管在数据线和驱动晶体管的栅极之间,在扫描线的选择期间导通,由此,在栅极保持向数据线供给的电位。而且,驱动晶体管构成为,使与该栅极的保持电位对应的电流流过发光元件。

[0003] 专利文献1:日本特开2007-310311号公报

[0004] 然而,在要求显示尺寸的小型化、显示的高精细化的用途中,被指出了以下问题。数据线和驱动晶体管相互接近,电容耦合的程度变高。因此,若数据线进行电位变动,则该电位变动作为一种噪声经由寄生电容向驱动晶体管的各部,特别向栅极传播,从而使该栅极的保持电位变动。因此,不能使目标电流流过发光元件,而使显示品质降低。

发明内容

[0005] 本发明是鉴于上述课题而完成的,其目的之一在于防止显示品质因起因于数据线的电位变动的噪声而降低。

[0006] 为了解决上述课题,本发明所涉及的电光学装置,其特征在于,具有相互交叉的扫描线以及数据线;与上述扫描线和上述数据线的交叉对应地设置的像素电路;屏蔽配线,上述像素电路具备发光元件;对流过上述发光元件的电流进行控制的驱动晶体管;开关晶体管,其连接于上述驱动晶体管的栅极和上述数据线之间,根据供给至上述扫描线的扫描信号,控制其导通状态,上述屏蔽配线俯视时设置于上述数据线和上述驱动晶体管之间。

[0007] 根据本发明,以数据线作为发生源的噪声在到达像素电路的驱动晶体管之前被屏蔽配线吸收。因此,驱动晶体管不易受噪声等的影响,因此能够防止显示品质的降低。

[0008] 在本发明中,优选上述屏蔽配线和上述数据线的距离比上述屏蔽配线和上述驱动晶体管的距离短的方式。根据该方式,能够更加可靠地抑制噪声等的影响。

[0009] 在本发明中,即便上述屏蔽配线处于未与任何部分电连接的高阻抗(悬浮)状态,例如若与时间上恒定电位的供电线电容耦合,则也能够吸收噪声,但优选与时间上恒定的电位直接连接的结构。在这种结构中,若为在上述像素电路中,在高位侧的电源线和低位侧的电源线之间的路径上,上述发光元件和上述驱动晶体管被串联连接,上述屏蔽配线与上述高位侧的电源线或者上述低位侧的电源线连接的方式,则与已经存在的电源线连接即可。

[0010] 并且,在这种方式中,若为在上述像素电路中,上述屏蔽配线具有与上述高位侧的电源线或者上述低位侧的电源线连接的部分的结构,则能够实现屏蔽配线的低阻抗化,因

此能够更加可靠地吸收噪声。

[0011] 另外,在本发明中,优选具有一端与上述驱动晶体管的栅极电连接的保持电容的结构。在该结构中,若上述屏蔽配线在俯视时覆盖上述保持电容,则基于保持电容的保持电压也能够不易受到噪声的影响。

[0012] 另外,上述目的通过下述结构也能达成,即,具有相互交叉的扫描线以及数据线;与上述扫描线和上述数据线的交叉对应地设置的像素电路;屏蔽配线,上述像素电路具备发光元件;对流过上述发光元件的电流进行控制的驱动晶体管;开关晶体管,其在驱动晶体管的栅极和上述数据线之间,根据供给至上述扫描线的扫描信号,控制其导通状态,上述屏蔽配线在剖视时设置于上述数据线和上述驱动晶体管之间,俯视时与上述数据线或者上述驱动晶体管的至少一部分重叠。

[0013] 此外,本发明所涉及的电光学装置能够适用于各种的电子设备。典型的是显示装置,作为电子设备列举个人计算机、手机等。特别是本申请发明,即便在不能充分确保保持电容时,来自数据线的噪声在到达像素电路的驱动晶体管之前也能被屏蔽配线吸收,由此能够防止显示品质的降低,例如适于像头置式显示器用、投影仪一样,形成缩小图像的显示装置。不过,本发明的电光学装置的用途不限于显示装置。例如,也能够适用于用于通过光线的照射使潜像形成于感光鼓等的图像载体的曝光装置(光学头)。

附图说明

[0014] 图 1 是表示第 1 实施方式所涉及的电光学装置的结构框图。

[0015] 图 2 是表示电光学装置的像素电路的等价电路的图。

[0016] 图 3 是表示电光学装置的显示动作的图。

[0017] 图 4 是表示像素电路的结构俯视图。

[0018] 图 5 是表示以图 4 中的 E-e 线切开的结构的局部剖视图。

[0019] 图 6 是表示像素电路中吸收来自数据线的噪声的图。

[0020] 图 7 是表示像素电路中的各种寄生电容的图。

[0021] 图 8 是将像素电路中的各种寄生电容模型化的图。

[0022] 图 9 是表示串扰的一个例子的图。

[0023] 图 10 是表示第 2 实施方式所涉及的电光学装置的像素电路的结构俯视图。

[0024] 图 11 是表示以图 10 中的 F-f 线切开的结构的局部剖视图。

[0025] 图 12 是表示第 3 实施方式所涉及的电光学装置的像素电路的结构俯视图。

[0026] 图 13 是表示以图 12 中的 H-h 线切开的结构的局部剖视图。

[0027] 图 14 是表示第 4 实施方式所涉及的电光学装置的像素电路的结构俯视图。

[0028] 图 15 是表示第 5 实施方式所涉及的电光学装置的像素电路的结构俯视图。

[0029] 图 16 是表示第 6 实施方式所涉及的电光学装置的像素电路的结构俯视图。

[0030] 图 17 是表示以图 16 中的 J-j 线切开的结构的局部剖视图。

[0031] 图 18 是表示第 7 实施方式所涉及的电光学装置的像素电路的结构俯视图。

[0032] 图 19 是表示其他例子所涉及的像素电路的等价电路的图。

[0033] 图 20 是表示适用了电光学装置的电子设备(其 1)的图。

[0034] 图 21 是表示适用了电光学装置的电子设备(其 2)的图。

[0035] 图 22 是表示适用了电光学装置的电子设备（其 3）的图。

具体实施方式

[0036] 第 1 实施方式

[0037] 图 1 是表示本发明的第 1 实施方式所涉及的电光学装置的结构框图。电光学装置 1 是利用多个像素电路 110 来显示图像的装置。

[0038] 如该图所示，电光学装置 1 为包含元件部 100、扫描线驱动电路 210 以及数据线驱动电路 220 的构成。

[0039] 其中，在元件部 100，沿图中行（X）方向设置有 m 行的扫描线 112，沿列（Y）方向且以与各扫描线 112 相互保持电绝缘的方式设置有 n 列的数据线 114。像素电路 110 分别与 m 行的扫描线 112 和 n 列的数据线 114 的各交叉对应地排列。因此，在本实施方式中，像素电路 110 以纵 m 行 $\times$ 横 n 列排列成矩阵状。其中， m 、 n 均为自然数。

[0040] 电源线 116 分别共同连接在各像素电路 110，向其供给元件电源的高位侧的电位 V_{el} 。此外，虽在图 1 中省略，但如后述，在各像素电路 110 设置有共用电极，来供给元件电源的低位侧的电位 V_{ct} 。这些电位 V_{el} 、 V_{ct} 由省略图示的电源电路生成。

[0041] 另外，为了便于区分扫描线 112 以及像素电路 110 的行，在图 1 中有时从上起按顺序称为 1 行、2 行、3 行、...、 $(m-1)$ 行、 m 行。同样，为了便于区分数据线 114 以及像素电路 110 的列，在图 1 中有时从左起按顺序称为 1 列、2 列、3 列、...、 $(n-1)$ 列、 n 列。

[0042] 在电光学装置 1 中，在像素电路 110 以矩阵状排列的区域的周边配置有扫描线驱动电路 210 以及数据线驱动电路 220。扫描线驱动电路 210 以及数据线驱动电路 220 的动作被省略图示的控制器控制。另外，从上述控制器向数据线驱动电路 220 供给指定在各像素电路 110 应显示的灰度（亮度）的灰度数据。

[0043] 扫描线驱动电路 210 在各帧中依次选择第 1 $\sim m$ 行。作为一个例子，扫描线驱动电路 210 是将扫描信号 $Gwr(1)$ 、 $Gwr(2)$ 、 $Gwr(3)$ 、...、 $Gwr(m-1)$ 、 $Gwr(m)$ 分别供给至第 1、2、3、...、 $(m-1)$ 、 m 行的扫描线 112 的电路，在帧中，使各扫描信号依次排他地成为 H 电平。此外，在本说明中，帧是指使 1 个镜头（画面）的量的图像显示在电光学装置 1 所需的期间，若垂直扫描频率为 60Hz，则指其 1 个周期的量的 16.67 毫秒的期间。

[0044] 数据线驱动电路 220 将与该像素电路 110 的灰度数据对应的电位的数据信号，经由数据线 114 供给至位于通过扫描线驱动电路 210 选择出的行的像素电路 110。为方便起见，将分别供给至第 1、2、3、...、 $(n-1)$ 、 n 列的数据线 114 的数据信号记为 $Vd(1)$ 、 $Vd(2)$ 、 $Vd(3)$ 、...、 $Vd(n-1)$ 、 $Vd(n)$ 。

[0045] 接下来，参照图 2，对像素电路 110 的等价电路进行说明。此外，图 2 示出与第 i 行以及相对该第 i 行在下侧相邻的第 $(i+1)$ 行的扫描线 112、和第 j 列以及相对该第 j 列在右侧相邻的第 $(j+1)$ 列的数据线 114 的交叉对应的 2×2 共计 4 个像素的量的像素电路 110。此处， i 、 $(i+1)$ 是一般表示像素电路 110 排列的行的符号，为 1 以上 m 以下的整数。同样， j 、 $(j+1)$ 是一般表示像素电路 110 排列的列的符号，为 1 以上 n 以下的整数。

[0046] 如图 2 所示，各像素电路 110 具有 N 沟道型的晶体管 130、140、保持电容 135 和发光元件 150。各像素电路 110 的结构彼此相同，因此以位于第 i 行 j 列的像素电路为代表进行说明。在第 i 行 j 列的像素电路 110 中，晶体管 130 作为开关晶体管发挥作用，其栅极结

点与第 i 行的扫描线 112 连接,而其漏极结点与第 j 列的数据线 114 连接,其源极结点分别与保持电容 135 的一端和晶体管 140 的栅极结点连接。

[0047] 保持电容 135 的另一端分别与晶体管 140 的源极结点以及发光元件 150 的阳极连接。另一方面,晶体管 140 的漏极结点与电源线 116 连接。

[0048] 为方便起见,在第 i 行 j 列的像素电路 110 中,将晶体管 130 的漏极结点记作大写的 D ,将晶体管 140 的栅极结点(晶体管 130 的源极结点以及保持电容 135 的一端)记作小写的 g 。特别是将第 i 行 j 列的晶体管 140 的栅极结点记作 $g(i, j)$ 。

[0049] 而且,将晶体管 140 的漏极结点(电源线 116)记作小写的 d ,将晶体管 140 的源极结点(发光元件 150 的阳极)记作小写的 s 。

[0050] 发光元件 150 的阴极在各像素电路 100 中与共用电极 118 连接。该共用电极 118 在各像素电路 110 的发光元件 150 中通用。发光元件 150 是在相互对置的阳极和阴极之间夹持由有机 EL 材料构成的发光层的 OLED,以与从阳极向阴极流动的电流对应的亮度发光。

[0051] 此外,在图 2 中, $Gwr(i)$ 、 $Gwr(i+1)$ 分别表示向第 i 、 $(i+1)$ 行的扫描线 112 供给的扫描信号。另外, $Vd(j)$ 、 $Vd(j+1)$ 分别表示向第 j 、 $(j+1)$ 列的数据线 114 供给的数据信号。

[0052] 另外,在本实施方式中,在数据线 114 的附近设置有屏蔽配线,后面叙述屏蔽配线的详细内容。

[0053] 接下来,参照图 3 对电光学装置 1 的显示动作进行简单说明。图 3 是表示扫描信号以及数据信号的波形的一个例子的图。

[0054] 如该图所示,扫描信号 $Gwr(1)$ 、 $Gwr(2)$ 、 $Gwr(3)$ 、 $\dots$ 、 $Gwr(m-1)$ 、 $Gwr(m)$ 通过扫描线驱动电路 210 在各帧中按每个水平扫描期间(H)依次排他地成为 H 电平。

[0055] 此处,第 i 行的扫描线 112 被选择从而扫描信号 $Gwr(i)$ 成为 H 电平时,通过数据线驱动电路 220 向第 j 列的数据线 114 供给与第 i 行 j 列的像素电路 110 的灰度数据对应的电位的的数据信号 $Vd(j)$ 。

[0056] 在第 i 行 j 列的像素电路 110 中,若扫描信号 $Gwr(i)$ 成为 H 电平,则晶体管 130 导通,因此,栅极结点 $g(i, j)$ 成为与第 j 列的数据线 114 电连接的状态。因此,栅极结点 $g(i, j)$ 的电位如图 3 中的向上箭头所示,成为数据信号 $Vd(j)$ 的电位。此时,晶体管 140 使与栅极结点 $g(i, j)$ 的电位对应的电流流过发光元件 150,保持电容 135 保持此时的晶体管 140 的栅极、源极间的电压。在第 i 行的扫描线 112 的选择结束而扫描信号 $Gwr(i)$ 变为 L 电平时,晶体管 130 截止。

[0057] 即便晶体管 130 从导通切换至截止,也通过保持电容 135 保持着该晶体管 130 导通时的、晶体管 140 的栅极、源极间的电压。因此,即便晶体管 130 截止,晶体管 140 也使与基于保持电容 135 的保持电压对应的电流持续流过发光元件 150,直至下次第 i 行的扫描线 112 再次被选择。因此,第 i 行 j 列的像素电路 110 中的发光元件 150 以对应于选择出第 i 行时的数据信号 $Vd(j)$ 的电位的亮度,即,以对应于第 i 行 j 列的灰度数据的亮度,在相当于 1 帧的期间持续发光。

[0058] 此外,在第 i 行中,即便为第 j 列以外的像素电路 110,也以与供给至对应的数据线 114 的数据信号的电位对应的亮度发光。另外,此处,对与第 i 行的扫描线 112 对应的像素电路 110 进行了说明,但扫描线 112 以第 1、2、3、 $\dots$ 、 $(m-1)$ 、 m 行的顺序被选择的结果,各像素电路 110 分别以与灰度数据对应的亮度发光。该动作按每帧反复进行。

[0059] 另外,在图 3 中,与扫描信号的电位比例 (scale) 相比,为方便起见使数据信号 $V_d(j)$ 、栅极结点 $g(i, j)$ 的电位比例放大。

[0060] 然而,数据信号为与位于所选择出的行的像素的灰度数据对应的电位,因此数据线 114 根据显示内容时时刻刻进行电位变动。例如向第 j 列的数据线 114 供给图 3 所示的数据信号 $V_d(j)$,因此在每个水平扫描期间 (H) 进行电位变动。

[0061] 若数据线 114 与像素电路 110 的各部电容耦合,则数据线 114 的电位变动会给像素电路 110 的各部的电位造成负面影响。特别是在要求显示尺寸的小型化和显示的高精细化的用途中,例如,在显示尺寸按对角不足 1 英寸且具有 1280×720 像素以上的分辨率的微显示器等中,与保持电容 135 比较,各部的寄生电容相对变大,因此其影响显著地显现。特别是,晶体管 140 的栅极结点 g 以及源极结点 s 的电位对流过发光元件 150 的电流进行规定,因此,该部分的电位变动引起显示乱码和后述的串扰等的产生,成为使显示品质大幅降低的重要因素。

[0062] 因此,在本实施方式中,使像素电路 110 以下述那样地构成,而不易受到起因于数据线的电位变动的噪声的影响。

[0063] 参照图 4 以及图 5 对该像素电路 110 的结构进行说明。

[0064] 图 4 是表示在纵、横方向彼此相邻的 4 个像素电路 110 的结构的俯视图,图 5 是沿图 4 中的 E-e 线切开的局部剖视图。

[0065] 此外,图 4 是表示从观察侧俯视顶部发光的像素电路 110 时的配线结构,但为了简单化,省略在发光元件 150 的像素电极(阳极)以后形成的结构体。在图 5 中,表示至发光元件 150 的像素电极,省略以后的结构体。另外,在以下各图中,为了使各层、各部件、各区域等成为能够识别的大小,使比例尺不同。

[0066] 首先,如图 5 所示,在作为基础的基板 2 上分别设置有将多晶硅膜岛状地图案成形的半导体层 130a、140a。半导体层 130a 构成晶体管 130,半导体层 140a 构成晶体管 140。此处,半导体层 130a 在俯视时如图 4 所示,形成为长边在沿后面形成的扫描线 112 的横向延伸的矩形。另一方面,半导体层 140a 在俯视时形成为长边在沿后面形成的数据线 114 的纵向延伸的矩形。

[0067] 如图 5 所示,以覆盖半导体层 130a、140b 的几乎整个面的方式设置有栅极绝缘膜 10。在栅极绝缘膜 10 的表面设置铝、钼等栅极配线层,并且,通过将该栅极配线层进行图案成形,而分别设置有扫描线 112 以及栅极电极层 21。

[0068] 扫描线 112 在图 4 中沿横向延伸,并且,在每个像素电路 110 上具有朝向下分支的部分,该分支部分在半导体层 130a 的中央部分重叠。半导体层 130a 中的与扫描线 112 的分支部分重叠的区域成为沟道区域 130c(参照图 5)。此外,在半导体层 130a 中,相对沟道区域 130c 在图 5 中左方向为漏极区域 130d,右方向为源极区域 130s。

[0069] 另一方面,栅极电极层 21 在俯视时如图 4 所示,呈在四角框中没有左边且上边、右边以及下边为一体的形状。其中,下边在半导体层 140a 的中央部分重叠。半导体层 140a 中的与栅极电极层 21 的下边重叠的区域为沟道区域 140c(参照图 5)。半导体层 140a 中,相对沟道区域 140c 区域在图 5 中左方向为源极区域 140s,右方向为漏极区域 140d。

[0070] 在图 5 中,以覆盖扫描线 112、栅极电极层 21 或者栅极绝缘膜 10 的方式形成有第 1 层间绝缘膜 11。在第 1 层间绝缘膜 11 的表面形成有导电性的配线层,并且,通过该配线

层的图案成形而分别形成有中继电极 41、42、43、44。

[0071] 其中,中继电极 41 经由分别对第 1 层间绝缘膜 11 以及栅极绝缘膜 10 进行开孔的接触孔(通孔)31 与漏极区域 130d 连接。

[0072] 此外,在图 4 中,在不同种类的配线层彼此重叠的部分,在“□”标记中标记有“×”标记的部分为接触孔。

[0073] 在图 5 中,中继电极 42 的一端经由分别对第 1 层间绝缘膜 11 以及栅极绝缘膜 10 进行开孔的接触孔 32 与源极区域 130s 连接,而中继电极 42 的另一端经由对第 1 层间绝缘膜 11 进行开孔的接触孔 33 与栅极电极层 21 连接。

[0074] 中继电极 43 经由分别对第 1 层间绝缘膜 11 以及栅极绝缘膜 10 进行开孔的接触孔 34 与源极区域 140s 连接。此处,中继电极 43 的俯视时的形状如图 4 所示,为覆盖栅极电极层 21 的上边那样的长方形。因此,保持电容 135 如图 5 所示,成为以栅极电极层 21 和中继电极 43 夹持第 1 层间绝缘膜 11 的构成。

[0075] 中继电极 44 经由分别对第 1 层间绝缘膜 11 以及栅极绝缘膜 10 进行开孔的接触孔 35 与漏极区域 140d 连接。

[0076] 以覆盖中继电极 41、42、43、44 或者第 1 层间绝缘膜 11 的方式形成有第 2 层间绝缘膜 12。在第 2 层间绝缘膜 12 的表面形成有导电性的配线层,并且,通过该配线层的图案成形而分别形成有中继电极 61、62 以及电源线 116。

[0077] 其中,中继电极 61 经由对第 2 层间绝缘膜 12 进行开孔的接触孔 51 与中继电极 41 连接。中继电极 62 也经由对第 2 层间绝缘膜 12 进行开孔的接触孔 52 与中继电极 43 连接。

[0078] 电源线 116 经由对第 2 层间绝缘膜 12 进行开孔的接触孔 53 与中继电极 44 连接。因此,电源线 116 经由中继电极 44 与漏极区域 140d 连接。电源线 116 在俯视时如图 4 所示沿着扫描线 112 延伸的横向形成。

[0079] 此外,也可以通过在接触孔 51、52、53 中填充由钨等高熔点金属构成的柱状的连接塞来分别连接中继电极 41 和 61 彼此、中继电极 43 和 62 彼此、以及中继电极 44 和电源线 116 彼此。

[0080] 以覆盖中继电极 61、62 或者第 2 层间绝缘膜 12 的方式形成有第 3 层间绝缘膜 13。在第 3 层间绝缘膜 13 的表面形成有导电性的配线层,并且,通过该配线层的图案成形而分别形成有数据线 114、屏蔽配线 81a、81b(在图 5 中省略)以及中继电极 82。

[0081] 其中,数据线 114 经由对第 3 层间绝缘膜 13 进行开孔的接触孔 71 与中继电极 61 连接。因此,数据线 114 按照中继电极 61、中继电极 41 这样的路径与漏极区域 130d 连接。此处,数据线 114 在俯视时如图 4 所示,沿与扫描线 112 的延伸方向正交的纵向形成。

[0082] 中继电极 82 经由对第 3 层间绝缘膜 13 进行开孔的接触孔 72 与中继电极 62 连接。

[0083] 此外,还可以通过在接触孔 71、72 中填充由高熔点金属构成的柱状的连接塞来分别连接中继电极 61 和数据线 114 彼此,以及中继电极 62、82 彼此。

[0084] 各屏蔽配线 81a、81b 在俯视时如图 4 所示,分别与各列对应地形成。

[0085] 具体地说,某列的屏蔽配线 81a 以位于该列的数据线 114 和该列的像素电路 110 中的晶体管 140 之间的方式在数据线 114 的右侧沿纵向形成。此时,在比较数据线 114 和晶体管 140 时,屏蔽配线 81a 设置在更靠近数据线 114 侧。即,屏蔽配线 81a 和数据线 114 之间的距离比屏蔽配线 81a 和晶体管 140 之间的距离短。因此,与晶体管 140 相比屏蔽配

线 81a 更容易与数据线 114 电容耦合。

[0086] 另一方面,某列的屏蔽配线 81b 以位于相对该列在右侧相邻的数据线 114 和该列的像素电路 110 中的晶体管 140 之间的方式,在数据线 114 的左侧沿纵向形成。此时,在比较数据线 114 合晶体管 140 时,屏蔽配线 81b 设置在更靠近数据线 114 侧。即,屏蔽配线 81b 和数据线 114 之间的距离比屏蔽配线 81b 和晶体管 140 之间的距离短。因此,与晶体管 140 相比,屏蔽配线 81b 更容易与数据线 114 电容耦合。

[0087] 俯视时若从晶体管 140 观察,则其被左侧的数据线 114 和右侧的数据线 114 夹持地配设,但在左侧的数据线 114 的跟前配设有屏蔽配线 81a,在右侧的数据线 114 的跟前配设有屏蔽配线 81b。

[0088] 此外,屏蔽配线 81a、81b 在图 4 中形成为纵向,并且,延伸至像素电路 110 排列的区域的外侧,被施加时间上恒定的电位,例如电位 V_{el} 。

[0089] 另外,屏蔽配线 81a、81b 也可以每隔 1 行或者几行在俯视时与电源线 116 交叉的部分经由接触孔连接。

[0090] 以覆盖数据线 114、屏蔽配线 81a、81b、中继电极 82 或者第 3 层间绝缘膜 13 的方式形成第 4 层间绝缘膜 14。在第 4 层间绝缘膜 14 的表面形成具有导电性以及反射性的配线层,并且,通过该配线层的图案成形而形成发光元件 150 的阳极。该阳极为按每个像素电路 110 单独的像素电极,经由对第 4 层间绝缘膜 14 进行开孔的接触孔 92 与中继电极 82 连接。因此阳极(像素电极)按照中继电极 82、中继电极 62、以及兼作保持电容 135 的另一个电极的中继电极 43 这样的路径与源极区域 140s 连接。

[0091] 此外,也可以在接触孔 92 中填充由高熔点金属构成的柱状的连接塞,来连接中继电极 82 以及像素电极彼此。

[0092] 图示省略了作为电光学装置 1 的以后的结构,但在阳极上按每个像素电路 110 层叠由有机 EL 材料构成的发光层,而且,在各像素电路 110 将共用的透明电极作为兼作阴极的共用电极 118 而设置。由此,发光元件 150 成为在相互对置的阳极和阴极之间夹持发光层的 OLED,以与从阳极朝向阴极流动的电流对应的亮度发光,被从与基板 2 相反方向观察(顶部发光结构)。除此以外,设置用于从大气隔离发光层的密封玻璃等,但省略说明。

[0093] 另外,在图 4 中,省略了作为发光元件 150 的阳极的像素电极的图示,因此接触孔 92 上只标注表示位置的“□”标记。

[0094] 接下来,参照图 6 对基于屏蔽配线 81a、81b 的屏蔽功能进行说明。图 6 是将图 4 所示的像素电路 110 的平面结构置换成电路表示的图。

[0095] 如上所述,各列的数据线 114 进行电位变动,因此起因于其电位变动的噪声传播至像素电路 110 的各部。

[0096] 在第 1 实施方式中,从第 j 列的数据线 114 观察,屏蔽配线 81a 位于与第 i 行 j 列的晶体管 140 的栅极结点 g、源极结点 s 相比靠跟前侧。因此,从第 j 列的数据线 114 产生的噪声被屏蔽配线 81a 和第 j 列的数据线 114 之间的耦合电容 C_a 吸收。

[0097] 另外,从第 (j+1) 列的数据线 114 观察,屏蔽配线 81b 也位于与第 i 行 j 列的晶体管 140 的栅极结点 g、源极结点 s 相比靠跟前侧。因此,从第 (j+1) 列的数据线 114 产生的噪声被屏蔽配线 81b 和该第 (j+1) 列的数据线 114 之间的耦合电容 C_b 吸收。

[0098] 因此,根据该电光学装置 1,晶体管 140 的栅极结点 g、源极结点 s 不易受到起因于

数据线 114 的电位变动的噪声的影响,因此,能够稳定的显示。

[0099] 另外,在第 1 实施方式中,屏蔽配线 81a、81b 是对与数据线 114、中继电极 82 相同的配线层进行图案成形而形成,因此无需在制造工序中追加工序。

[0100] 图 7 是将像素电路 110 的等价电路与各部的寄生电容一起表示的图。

[0101] 在该图中, C_{dg} 表示在晶体管 130 的漏极结点 D (数据线 114) 和晶体管 140 的栅极结点 g 之间产生的寄生电容, C_{ds} 表示在晶体管 130 的漏极结点 D 和晶体管 140 的源极结点 s 之间产生的寄生电容。

[0102] C_{hold} 表示保持电容 135 的电容。

[0103] C_{gd} 表示在晶体管 140 的栅极结点 g 和漏极结点 d (电源线 116) 之间产生的寄生电容, C_{ds} 表示在晶体管 140 的漏极结点 d 和源极结点 s 之间产生的寄生电容, C_{oled} 表示发光元件 150 的电容成分。

[0104] 在对应的扫描线为非选择期间时,像素电路 110 的晶体管 130 为截止状态。而且,电源线 116 以及共用电极 118 的电位恒定。

[0105] 因此,非选择期间的像素电路 110 能够简化为图 8 所示的模型。此外,在图中, V_{amp} 为非选择期间的数据线 114 的电位振幅。

[0106] 该模型中,保持电容 135 的保持电压 V_{gs} 所施加的变动量 ΔV_{gs} 能够如图 8 的式 (1) 那样表示。应予说明,式 (1) 中的系数 K_1 如式 (2) 那样表示,而系数 K_2 如式 (3) 那样表示。

[0107] 在本实施方式中,由于具有屏蔽配线 81a、81b,因此与没有屏蔽配线 81a、81b 的构成相比,寄生电容 C_{dg} 、 C_{ds} 分别变小。

[0108] 因此,由于式 (2) 中 (a) 项的成分变大,分母成分整体变大,因此,系数 K_1 变小。另一方面,由于式 (3) 中 (b) 项的成分变大,分母成分整体变大,因此,系数 K_2 也变小。

[0109] 因此,在本实施方式中,相对电位振幅 V_{amp} 的变动量 ΔV_{gs} 与没有屏蔽配线 81a、81b 的构成相比变小,因此,能够进行不易受到数据线 114 的电位变动和噪声等影响的稳定的显示。

[0110] 这里,栅极结点 g、源极结点 s 的电位因起因于数据线 114 的电位变动的噪声而变动时,具体而言,以下述的串扰这样的形式显著化,使显示品质降低。

[0111] 图 9 是表示在不具有本实施方式这样的屏蔽配线 81a、81b 的电光学装置中发生的串扰的一个例子的图。

[0112] 这里所说的串扰是指如图 9(A) 所示,例如在将灰色作为背景区域使黑色的矩形区域窗口显示时,实际上如图 9(B) 所示,相对于黑色的区域 (b2),上侧的区域 (a2) 以及下侧的区域 (c2) 以与其他灰色的区域 (a1、a3、b1、b3、c1、c3) 不同的较暗的灰度显示的现象。

[0113] 应予说明,在图 9 中,以斜线的密度表示区域的亮度。另外,该串扰在使区域 (b2) 为白色时也产生。不管哪一种,由于以不同的灰度显示的区域均出现在区域 (b2) 的上下方向,因此特别有时也称作纵串扰。

[0114] 可以认为该纵串扰是由于下述原因产生的。即,在某个帧中,跨区域 (a1、b1、c1) 的数据线 114 在从第 1 行至最终第 m 行的选择中维持与灰色的灰度数据对应的电位。因此,属于区域 (a1、b1、c1) 的像素电路 110 分别保持通过自身对应的扫描线的选择而在栅

极结点 g 保持的电位,而不受来自数据线的噪声的影响。跨区域 (a3、b3、c3) 的数据线 114 以及属于该区域 (a3、b3、c3) 的像素电路 110 也相同。因此,属于区域 (a1、a3、b1、b3、c1、c3) 的像素电路 110 分别在相当于 1 帧的期间的整个范围,以与栅极结点 g 的保持电位对应的亮度发光。

[0115] 与此相对,跨区域 (a2、b2、c2) 的数据线 114 在区域 (a2) 的选择中成为与灰色的灰度数据对应的电位,在区域 (b2) 的选择中下降至与黑色的灰度数据对应的电位,在区域 (c2) 的选择中再次成为与灰色的灰度数据对应的电位。

[0116] 因此,在属于区域 (a2) 的像素电路 110 中,即便通过与自身对应的扫描线的选择,栅极结点 g 保持与灰色相当的电位,也会因起因于选择区域 (b2) 时的数据线 114 的电位变动的噪声而变化。

[0117] 此外,选择区域 (c2) 时数据线 114 再次返回至与灰色相当的电位,因此,通过该返回,栅极结点 g 有可能恢复为或接近与灰色相当的电位。

[0118] 然而,即便栅极结点 g 恢复为与灰色相当的电位,属于区域 (a2) 的像素电路 110 分别在写入后,在相当于 1 帧的期间中,至少在选择区域 (b2) 时,以对应于从与灰色相当的电位降低的电位的亮度发光。

[0119] 区域 (c2) 也相同。即,在属于区域 (c2) 的像素电路 110 中,即便根据与自身对应的扫描线的选择,栅极结点 g 保持与灰色相当的电位,也在下一帧中,在选择区域 (b2) 时受到数据线 114 的电位变动而变化。

[0120] 因此,以相当于 1 帧的期间的平均值来看,属于区域 (a2、c2) 的像素电路 110 的每一个与属于其他的区域 (a1、a3、b1、b3、c1、c3) 的像素电路 110 的每一个不同,观察出较暗的灰度。可以认为其为纵串扰产生的机理。

[0121] 根据第 1 实施方式,为栅极结点 g 以及源极结点 s 的每一个因屏蔽配线 81a、82,不易受到起因于数据线 114 的电位变动的噪声的影响的结构,因此,能够抑制这样的纵串扰,进行高品质显示。

[0122] 此外,在第 1 实施方式中,使屏蔽配线 81a、81b 为与电源线 116 相同的电位 V_{el} ,但可以使保持其他的电位,例如电位 V_{ct} 。

[0123] 第 2 实施方式

[0124] 在第 1 实施方式中,对与数据线 114 相同的配线层进行图案成形而形成屏蔽配线 81a、81b,但也可以由与数据线 114 不同的配线层形成。因此,接下来,作为第 2 实施方式,以由与比数据线 114 靠下层侧的中继电极 61、62 以及电源线 116 相同的配线层形成屏蔽配线 81a、81b 的情况为例进行说明。

[0125] 图 10 是表示第 2 实施方式的电光学装置的像素电路 110 的结构的俯视图。图 11 是以图 10 中的 F-f 线切开的局部剖视图。

[0126] 在由与中继电极 61、62 以及电源线 116 相同的配线层形成屏蔽配线 81a、81b 的情况下,需要避免屏蔽配线 81a 和中继电极 61 的干扰(电接触)。具体而言,需要将接触孔 51 设置在俯视时与屏蔽配线 81a 相比靠外侧(在图 10、图 11 中为左侧)。

[0127] 因此,在第 2 实施方式中,如图 10 所示,使接触孔 51、71 配置为,俯视时在同一地点重叠,并使中继电极 41 延伸至该地点。当然,例如也可以将中继电极 61 延伸配置至其他地点等,使接触孔 51、71 配置成在俯视时为不同地点(省略图示)。

[0128] 即便在第 2 实施方式中,从第 j 列的数据线 114 观察,在俯视时屏蔽配线 81a 也位于第 i 行 j 列的晶体管 140 的各结点的跟前,因此从第 j 列的数据线 114 产生的噪声被屏蔽配线 81a 和第 j 列的数据线 114 之间的耦合电容吸收。

[0129] 另外,从第 $(j+1)$ 列的数据线 114 观察,俯视时屏蔽配线 81b 也位于第 i 行 j 列的晶体管 140 的各结点的跟前,因此从第 $(j+1)$ 列的数据线 114 产生的噪声被屏蔽配线 81b 和该第 $(j+1)$ 列的数据线 114 之间的耦合电容吸收。

[0130] 因此,即便在第 2 实施方式中,由于不易受到噪声等影响,因此,能够稳定地进行显示。

[0131] 另外,在第 2 实施方式中,屏蔽配线 81a、81b 是对与中继电极 61、62 以及电源线 116 相同的配线层进行图案成形而形成的,因此,与第 1 实施方式相同,无需在制造工序中追加工序。

[0132] 另外,在第 2 实施方式中,使用与数据线 114 不同的配线层形成屏蔽配线 81a、81b。所以,能够避免屏蔽配线 81a、81b 和数据线 114 的接触,因此,像素电路的窄间距化变得容易。即,在第 1 实施方式中,由与数据线 114 相同的配线层形成屏蔽配线 81a、81b,因此为了确保屏蔽功能,需要使屏蔽配线 81a、81b 与数据线 114 分离。与此相对,在第 2 实施方式中,没有这样的必要,即便俯视时屏蔽配线 81a、81b 与数据线 114 重叠,只要在中继电极 61 的部分分离,就能够确保电绝缘,因此,窄间距化变得容易。

[0133] 然而,若俯视时屏蔽配线形成为与晶体管 140 的各结点交叉,则能够期待更强的屏蔽功能。因此,在第 3 实施方式、第 5 实施方式中说明由与数据线相同的配线层形成屏蔽配线,而实现屏蔽功能的强化的例子。另外,在第 6 实施方式、第 7 实施方式中后述说明由与数据线不同的配线层形成屏蔽配线,而实现屏蔽功能的强化的例子。

[0134] 第 3 实施方式

[0135] 图 12 是表示第 3 实施方式的电光学装置的像素电路 110 的结构的俯视图,图 13 是表示以图 12 中的 H-h 线切开的局部剖视图。

[0136] 如图 12 所示,在第 3 实施方式中,屏蔽配线 81a 的一部分以朝向右侧延伸,且俯视时覆盖中继电极 43 的方式形成。保持电容 135 为俯视时中继电极 43 和栅极电极层 21 重叠的区域,中继电极 43 为保持电容 135 中的另一个电极,也是晶体管 140 的源极结点 s 。因此,在第 3 实施方式中,屏蔽功能与第 1 实施方式相比进一步强化。

[0137] 第 4 实施方式

[0138] 图 14 是表示第 4 实施方式的电光学装置的像素电路 110 的结构的俯视图。

[0139] 如该图所示,屏蔽配线 81a、81b 分别按每个像素电路 110,沿数据线 114 形成为长条状,并且,分别与电源线 116 连接。此外,在第 4 实施方式中,屏蔽配线 81a、81b 由与数据线 114 相同的配线层形成。因此,屏蔽配线 81a 经由对第 3 层间绝缘膜 13 进行开孔的接触孔 73 与电源线 116 连接,屏蔽配线 81b 也同样经由对第 3 层间绝缘膜 13 进行开孔的接触孔 74 与电源线 116 连接。此外,省略剖视图。

[0140] 如第 1 实施方式所示,在使屏蔽配线 81a、81b 沿数据线 114 分别形成为 1 根的情况下,若电阻率较大,或与固定电位的连接点相隔,则屏蔽配线 81a、81b 的阻抗变得较高,有时不能充分吸收噪声。与此相对,根据第 4 实施方式,按每个像素电路 110 设置屏蔽配线 81a、81b,并且与电源线 116 连接,因此,能够实现低阻抗化,提高噪声的吸收能力。

[0141] 第 5 实施方式

[0142] 图 15 是表示第 5 实施方式的电光学装置的像素电路 110 的结构的俯视图。该第 5 实施方式中是对第 3 实施方式和第 4 实施方式进行组合而成的结构,改变图 14 所示的屏蔽配线 81a 的形状,而形成俯视时覆盖中继电极 43。

[0143] 因此,根据第 5 实施方式,能够强化屏蔽功能,提高噪声的吸收能力。

[0144] 第 6 实施方式

[0145] 如第 2 实施方式所示,在由与数据线 114 不同的配线层形成屏蔽配线的情况下,也可以将屏蔽配线以不与数据线 114 左右相邻,而在俯视时与数据线 114 重叠的方式设置在数据线 114 的下层侧。

[0146] 另一方面,若将屏蔽配线按每个像素电路 110 与例如电源线 116 连接,则能够提高噪声的吸收能力这一点已经在第 4(第 5)实施方式中叙述。

[0147] 因此,接下来,说明对两者进行组合,将屏蔽配线由与数据线 114 不同的配线层形成,以俯视时与数据线 114 重叠的方式设置在数据线 114 的下层侧,并且与电源线 116 一体化的第 6 实施方式。

[0148] 图 16 是表示第 6 实施方式中的电光学装置的像素电路 110 的结构的俯视图,图 17 是以图 16 中的 J-j 线切开的局部剖视图。

[0149] 从第 1 实施方式至第 5 实施方式,每 1 列设置有屏蔽配线 81a、81b,但在第 6 实施方式中,统一成屏蔽配线 81,并且,兼作电源线 116。

[0150] 如图 17 所示,兼作电源线 116 的屏蔽配线 81 与中继电极 61、62 一起,是对形成在第 2 层间绝缘膜 12 上的配线层进行图案成形的配线。俯视屏蔽配线 81 时的形状如图 16 所示,为与纵向的数据线 114 重叠且比数据线 114 的宽度宽,并且与横向的电源线 116 为一体呈格子状。

[0151] 数据线 114 依次经由中继电极 61、41 与漏极区域 130d 连接,但屏蔽配线 81 由与中继电极 61 相同的配线层形成,因此需要避免干扰。因此,数据线 114 在图 16 中向右方分支,并且,延伸至未形成屏蔽配线 81 的部分。在该延伸部分形成有接触孔 51,使数据线 114 与中继电极 61 连接。由此,屏蔽配线 81 和中继电极 61 不相互干扰地电分离。

[0152] 此外,在该例中,使接触孔 51、71 配置为俯视时在相同地点重叠,但也可以配置为成为不同地点(省略图示)。

[0153] 另外,在第 6 实施方式中,由于使数据线 114 向右侧分支延伸,因此会有噪声从该延伸部分进入到晶体管 140 的栅极结点 g、源极结点 s 的可能性。因此,在第 6 实施方式中,在俯视时数据线 114 的分支部分和中继电极 43/ 栅极电极层 21 之间设置有使屏蔽配线 81 向右侧延伸的分支配线 81d。由此,来自向数据线 114 的右侧延伸的部分,即来自接触孔 71 附近的噪声在到达晶体管 140 的各结点前被分支配线 81d 吸收。

[0154] 根据第 6 实施方式,屏蔽配线 81 被设置为俯视时与数据线 114 重叠,并且,兼作电源线 116 而电位被固定化,因此,能够实现屏蔽功能的强化。

[0155] 第 7 实施方式

[0156] 图 18 是表示第 7 实施方式的电光学装置的像素电路 110 的结构的俯视图。

[0157] 如该图所示,第 7 实施方式中,使兼作电源线 116 的屏蔽配线 81 在俯视时覆盖保持电容 135(栅极电极层 21)以及晶体管 140。

[0158] 如上所述,屏蔽配线 81(电源线 116)对与中继电极 61、62 相同的配线层进行图案成形而形成,因此,需要避免与中继电极 61、62 的干扰。在该第 7 实施方式中,兼作电源线 116 的屏蔽配线 81 在中继电极 61、62 的附近区域呈开孔的形状。

[0159] 此外,第 7 实施方式的像素电路 110 中的主要部分剖视图是图 17 中,追加以虚线表示的部分的内容。

[0160] 根据第 7 实施方式,屏蔽配线 81 被设置为在俯视时与数据线 114 重叠,并且覆盖保持电容 135 以及晶体管 140,并且,通过兼作电源线 116 而电位被固定化,因此,实现屏蔽功能的进一步的强化。

[0161] 此外,在第 7 实施方式中,只要不与中继电极 61、62 干扰,可以使屏蔽配线 81 的开孔面积更窄。另外,在第 7 实施方式中,屏蔽配线 81 在俯视时覆盖保持电容 135 以及晶体管 140 的整个区域,但也可以仅覆盖一部分。

[0162] 应用例・变形例

[0163] 本发明不限于上述实施方式,可进行以下应用、变形。

[0164] 例如对于保持电容 135 的结构而言,以栅极电极层 21 和中继电极 43 夹持第 1 层间绝缘膜 11,但也可以例如以在俯视时与栅极电极层 21 重叠的方式设置半导体层,用该半导体层和栅极电极层 21 夹持栅极绝缘膜 10。作为半导体层,可以使用使源极区域 140s 延伸的结构,也可以使用另外图案成形的结构。除此之外,也可以为以由不同种类配线层构成的电极、配线彼此夹持层间绝缘膜、栅极绝缘膜的构成,还可以将多个并列连接的结构作为整体而作为保持电容 135 使用。

[0165] 另外,对于电插入保持电容 135 的位置而言,除了晶体管 140 的栅极结点 g 和源极结点 s 之间以外,例如如图 19 所示,还可以位于栅极结点 g 和共用电极 118 之间,虽未特别图示,还可以位于栅极结点 g 和被固定在其他电位的配线之间。

[0166] 对于像素电路 110 的驱动而言,不限于在晶体管 130 为导通状态的选择期间,仅使栅极结点 g 保持与灰度数据对应的电位的驱动信号的方法。例如,可以以如下方式驱动,在晶体管 130 为导通状态的选择期间,使数据线 114 为基准电位,并且,以第 1 电位和第 2 电位切换基于电源线 116 以及共用电极 118 的电源,使保持电容 135 保持与晶体管 140 的阈值电压相当的电压,之后,使数据线 114 成为与灰度数据对应的电位。另外,还可以在在选择期间使数据信号的电位变化,并且使选择期间结束时的数据信号的时间变化率为与灰度数据对应的值的方式驱动,还可以以经由电容元件按每行向源极结点 s 供给灯信号向晶体管 140 流入规定(set)电流的方式驱动。

[0167] 无论哪种驱动,均能够通过将各实施方式的屏蔽配线设置于像素电路 110,抑制使电流流过发光元件 150 的晶体管 140 的各结点的电位因来自数据线 114 的噪声而变动。

[0168] 对于屏蔽配线而言,可以使用对不同的两层以上的配线层进行图案成形的配线。例如在第 6(第 7)实施方式中,也可以对与数据线 114 以及中继电极 82 相同的配线层进行图案成形,成为屏蔽配线 81(电源线 116)和另形成的屏蔽配线的二重构造。此外,对于另形成的屏蔽配线而言,只要能够避免数据线 114 以及中继电极 82 的干扰即可。

[0169] 作为发光元件 150,除 OLED 外,能够适用无机 EL 元件、LED(Light Emitting Diode)元件等以对应于电流的亮度发光的元件。

[0170] 电子设备

[0171] 接下来,对适用了本发明所涉及的电光学装置的几个电子设备进行说明。

[0172] 图 20 是表示将上述的实施方式所涉及的电光学装置 1 作为显示装置而采用的个人计算机的外观的图。个人计算机 2000 具备作为显示装置的电光学装置 1 和主体部 2010。主体部 2010 设置有电源开关 2001 以及键盘 2002。

[0173] 在电光学装置 1 中,作为发光元件 150 使用 OLED 的情况下,能够实现视角广阔,容易观察的画面显示。

[0174] 图 21 是表示将实施方式所涉及的电光学装置 1 作为显示装置而采用的手机的外观的图。手机 3000 除了多个操作按钮 3001、方向键 3002 等外,还具备耳承 (ear piece) 3003、送话口 (mouthpiece) 3004、上述的电光学装置 1。通过操作方向键 3002,显示在电光学装置 1 的画面滚动。

[0175] 图 22 是表示将实施方式所涉及的电光学装置 1 作为显示装置而采用的移动信息终端 (PDA:Personal Digital Assistants) 的外观的图。移动信息终端 4000 除了多个操作按钮 4001、方向键 4002 等外,还具备上述的电光学装置 1。在移动信息终端 4000 中,通过规定的操作使通信簿、日程表等各种的信息显示于电光学装置 1,并且,显示的信息通过方向键 4002 的操作被滚动。

[0176] 此外,作为适用了本发明所涉及的电光学装置的电子设备,除了图 20 至图 22 表示的例子外,还能够列举电视机、车辆导航装置、呼叫器、电子记事本、电子书,计算机、文字处理器、工作站,可视电话,POS 终端、打印机、扫描仪、复印机、视频播放器、具备触摸面板的设备等。特别是作为微显示器,能够列举头戴式可视设备、数码照相机或者摄像机的电子取景器等。

[0177] 本发明也覆盖如下进一步的方面“A”:

[0178] A1. 一种电光学装置,包括:

[0179] 扫描线;

[0180] 数据线,所述数据线与所述扫描线相交;

[0181] 像素电路,所述像素电路被设置为对应于所述扫描线和所述数据线的交叉点;以及

[0182] 配线,所述配线被施加恒定电位,

[0183] 所述像素电路包含:

[0184] 发光元件;

[0185] 驱动晶体管,所述驱动晶体管控制流向所述发光元件的电流,所述驱动晶体管包含栅极,所述配线被设置在所述驱动晶体管和所述数据线之间;以及

[0186] 开关晶体管,所述开关晶体管连接在所述驱动晶体管的栅极和所述数据线之间,并且根据提供给所述扫描线的扫描信号来控制所述开关晶体管的导通状态。

[0187] A2. 根据技术方案 A1 所述的电光学装置,在所述像素电路中,在俯视图中所述配线被设置在所述驱动晶体管和所述数据线之间。

[0188] A3. 根据技术方案 A1 所述的电光学装置,在所述像素电路中,在横截面图中所述配线被设置在所述驱动晶体管和所述数据线之间,在俯视图中所述配线与所述数据线或与所述驱动晶体管的至少一部分重叠。

[0189] A4. 根据技术方案 A2 所述的电光学装置,

- [0190] 所述配线和所述数据线之间的距离短于所述配线和所述驱动晶体管之间的距离。
- [0191] A5. 根据技术方案 A1 所述的电光学装置,还包括第一电源线和第二电源线,
- [0192] 在所述像素电路中,所述发光元件和所述驱动晶体管在所述第一电源线和所述第二电源线之间的路径中彼此串联连接,以及
- [0193] 所述配线连接至所述第一电源线和所述第二电源线之一。
- [0194] A6. 根据技术方案 A5 所述的电光学装置,
- [0195] 在所述像素电路中,所述配线具有与所述第一电源线和所述第二电源线之一连接的部分。
- [0196] A7. 根据技术方案 A1 所述的电光学装置,
- [0197] 所述像素电路还包括:
- [0198] 保持电容器,所述保持电容器的一端电连接至所述驱动晶体管的栅极。
- [0199] A8. 根据技术方案 A7 所述的电光学装置,
- [0200] 在所述像素电路中,当在俯视图中观看时所述配线覆盖所述保持电容器。
- [0201] A9. 根据技术方案 A1 所述的电光学装置,所述配线与所述数据线平行。
- [0202] A10. 根据技术方案 A1 所述的电光学装置,还包括另一配线以及与所述数据线紧邻的另一数据线,
- [0203] 在俯视图中,所述另一配线被设置在所述驱动晶体管和所述另一数据线之间,所述数据线和所述另一数据线被设置在所述驱动晶体管的相反两侧。
- [0204] A11. 一种电光学装置,包括:
- [0205] 扫描线;
- [0206] 数据线,所述数据线与所述扫描线相交;
- [0207] 像素电路,所述像素电路被设置为对应于所述扫描线和所述数据线的交叉点;以及
- [0208] 配线,所述配线被施加恒定电位,
- [0209] 所述像素电路包含:
- [0210] 发光元件;
- [0211] 驱动晶体管,所述驱动晶体管控制流向所述发光元件的电流,所述驱动晶体管包含栅极,在俯视图中所述配线被设置在所述驱动晶体管和所述数据线之间;以及
- [0212] 开关晶体管,所述开关晶体管连接在所述驱动晶体管的栅极和所述数据线之间,并且根据提供给所述扫描线的扫描信号来控制所述开关晶体管的导通状态。
- [0213] A12. 一种电光学装置,包括:
- [0214] 扫描线;
- [0215] 数据线,所述数据线与所述扫描线相交;
- [0216] 像素电路,所述像素电路被设置为对应于所述扫描线和所述数据线的交叉点;以及
- [0217] 配线,所述配线被施加恒定电位,
- [0218] 所述像素电路包含:
- [0219] 发光元件;
- [0220] 驱动晶体管,所述驱动晶体管控制流向所述发光元件的电流,所述驱动晶体管包

含栅极,当在横截面图中观看时所述配线被设置在所述驱动晶体管和所述数据线之间,而当在俯视图中观看时所述配线与所述数据线或与所述驱动晶体管的至少一部分重叠;以及

[0221] 开关晶体管,所述开关晶体管连接在所述驱动晶体管的栅极和所述数据线之间,并且根据提供给所述扫描线的扫描信号来控制所述开关晶体管的导通状态。

[0222] A13. 一种电子设备,包括根据技术方案 A1 所述的电光学装置。

[0223] 符号说明

[0224] 1... 电光学装置,81、81a、81b... 屏蔽配线,110... 像素电路,112... 扫描线,114... 数据线,116... 电源线,118... 共用电极,130... 晶体管,135... 保持电容,140... 晶体管,150... 发光元件,210... 扫描线驱动电路,220... 数据线驱动电路,2000... 个人计算机,3000... 手机,4000... 移动信息终端。

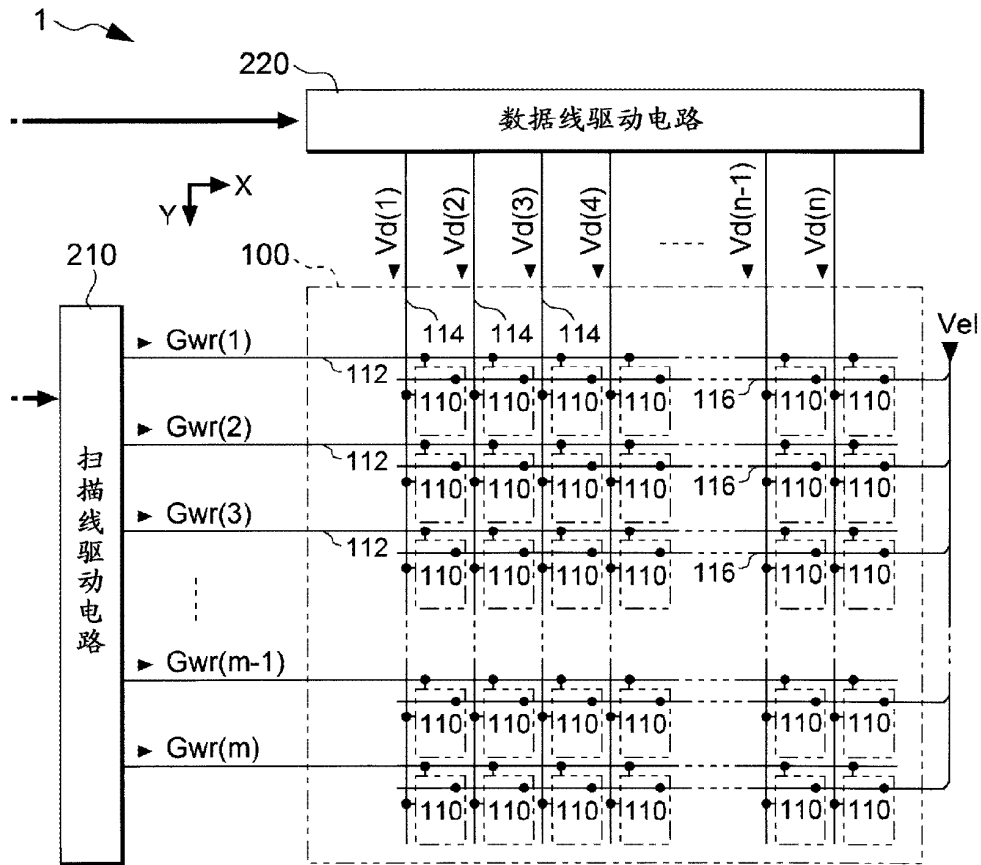


图 1

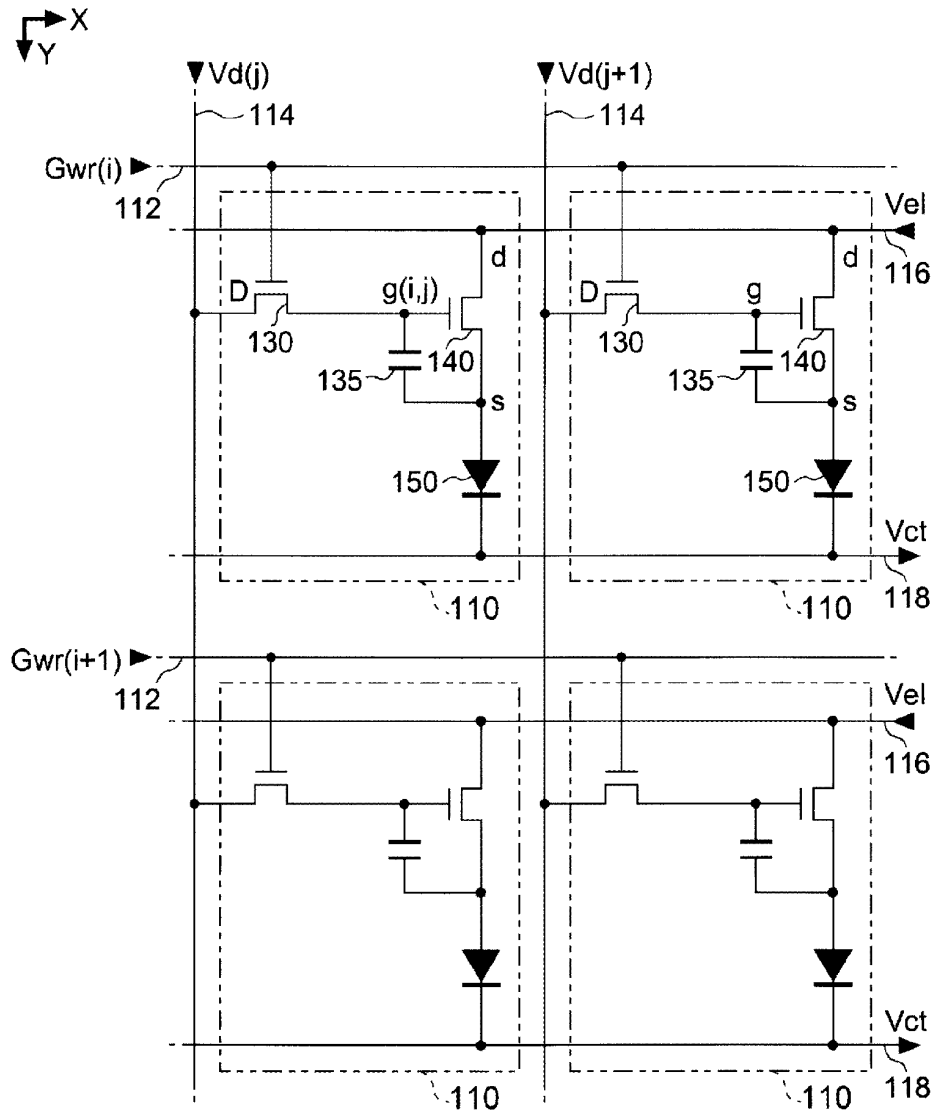


图 2

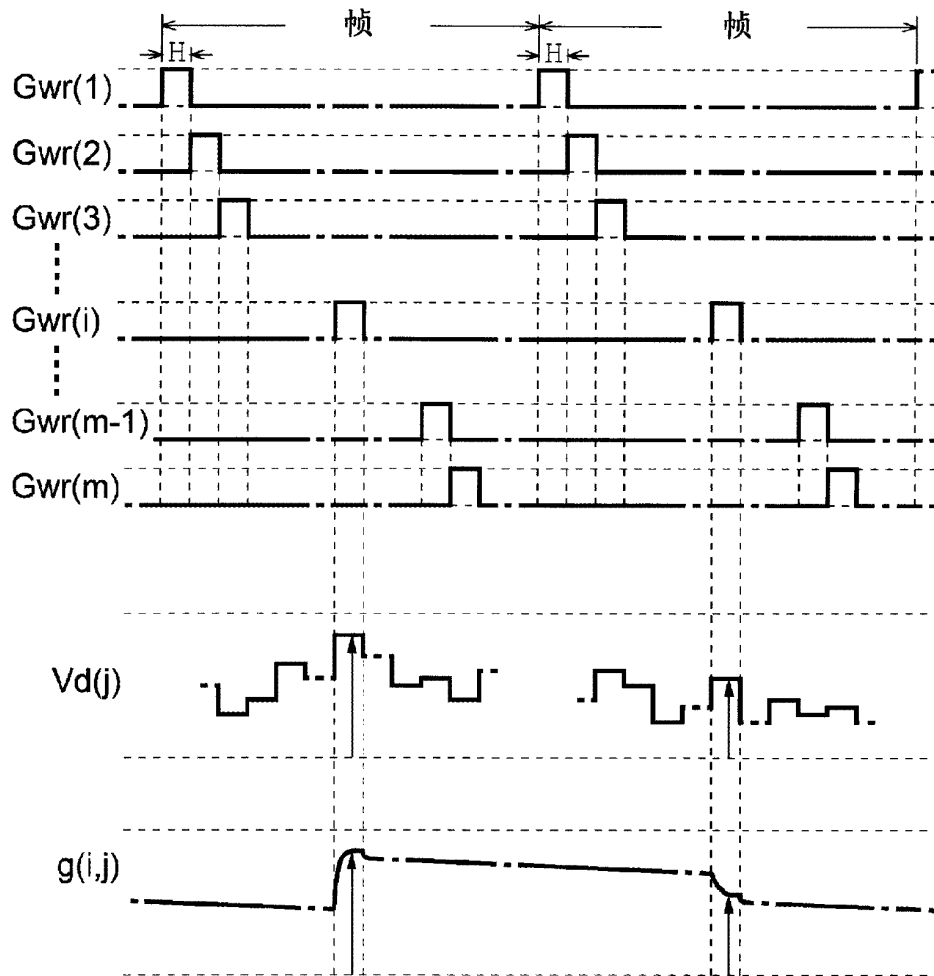


图 3

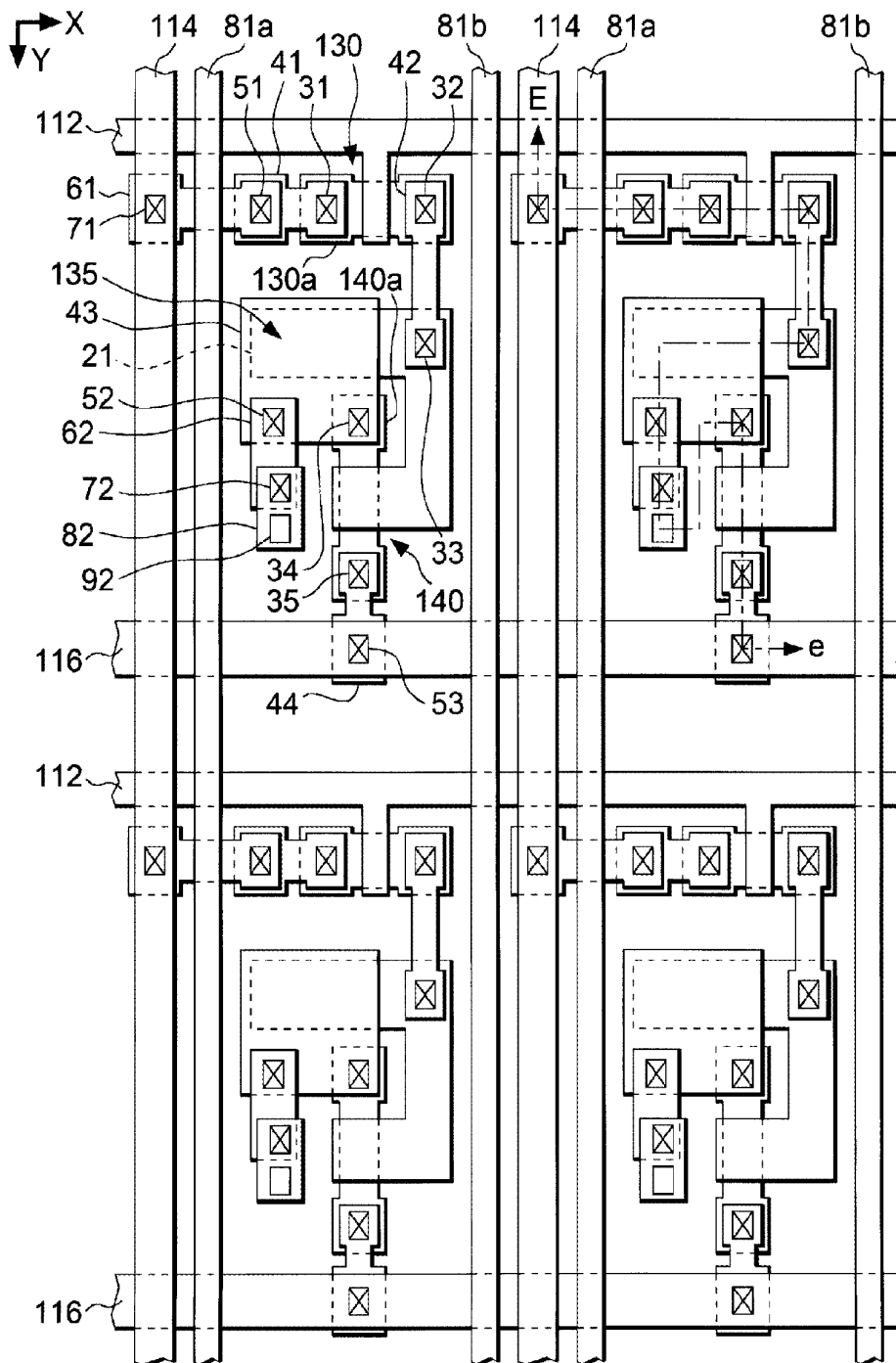


图 4

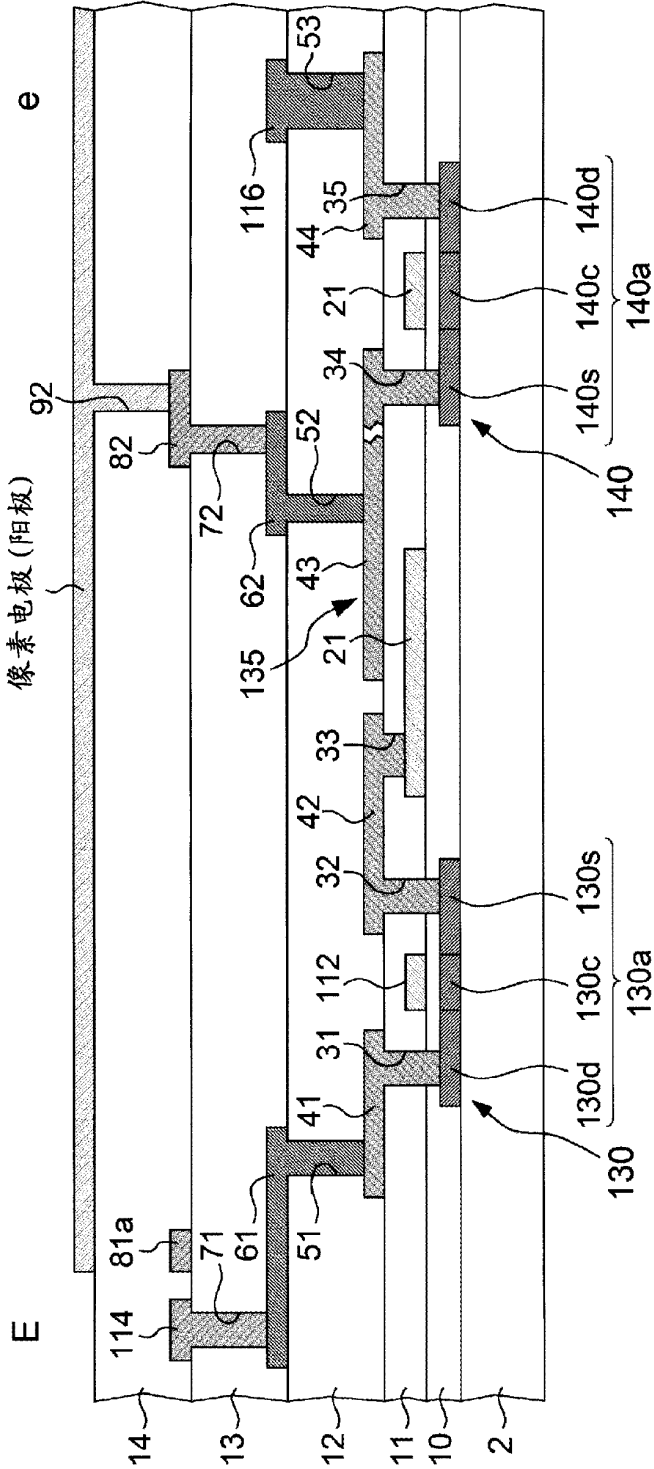


图 5

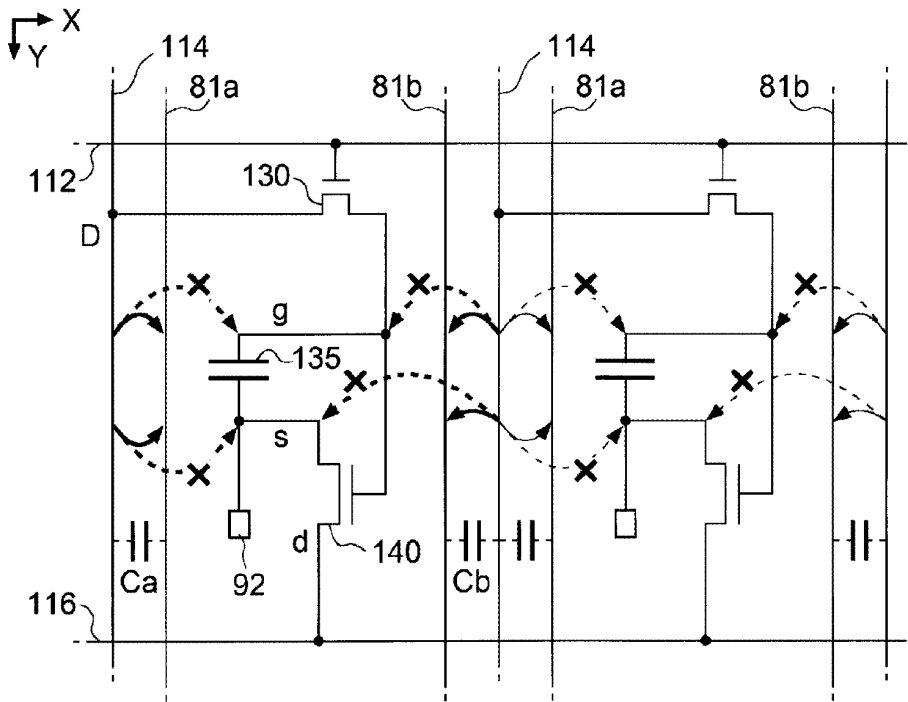


图 6

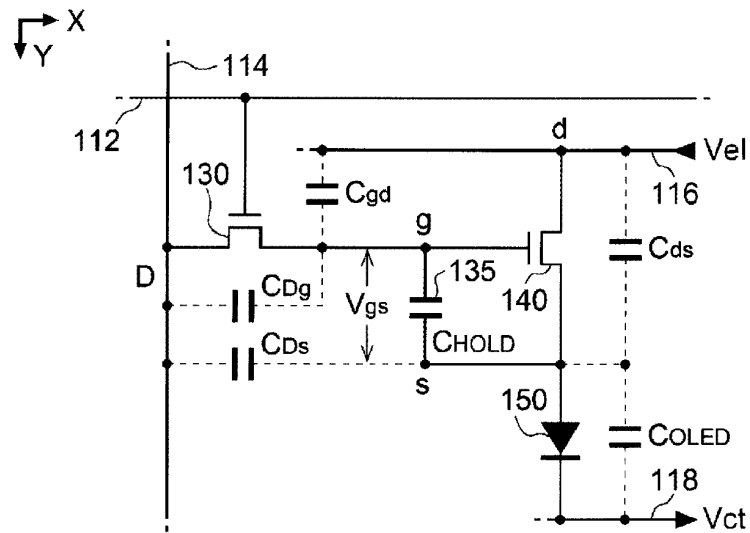
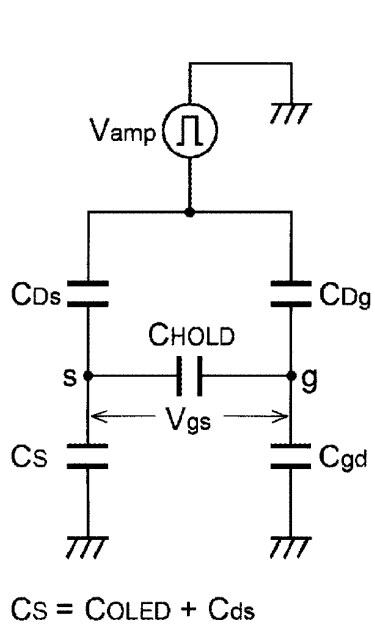


图 7

$$\Delta V_{gs} = V_{amp} \left\{ K_1 \left(1 - \frac{C_{HOLD}}{C_{HOLD} + C_s} \right) + K_2 \left(\frac{C_{HOLD}}{C_{HOLD} + C_{gd}} - 1 \right) \right\} \quad \cdots(1)$$



$$K_1 = \frac{\frac{1}{C_{gd} + \frac{C_{HOLD} \cdot C_s}{C_{HOLD} + C_s}}}{\underbrace{\frac{1}{C_{Dg}}}_{(a)} + \frac{1}{C_{gd} + \frac{C_{HOLD} \cdot C_s}{C_{HOLD} + C_s}}} \quad \cdots(2)$$

$$K_2 = \frac{\frac{1}{C_s + \frac{C_{HOLD} \cdot C_{gd}}{C_{HOLD} + C_{gd}}}}{\underbrace{\frac{1}{C_{Ds}}}_{(b)} + \frac{1}{C_s + \frac{C_{HOLD} \cdot C_{gd}}{C_{HOLD} + C_{gd}}}} \quad \cdots(3)$$

图 8

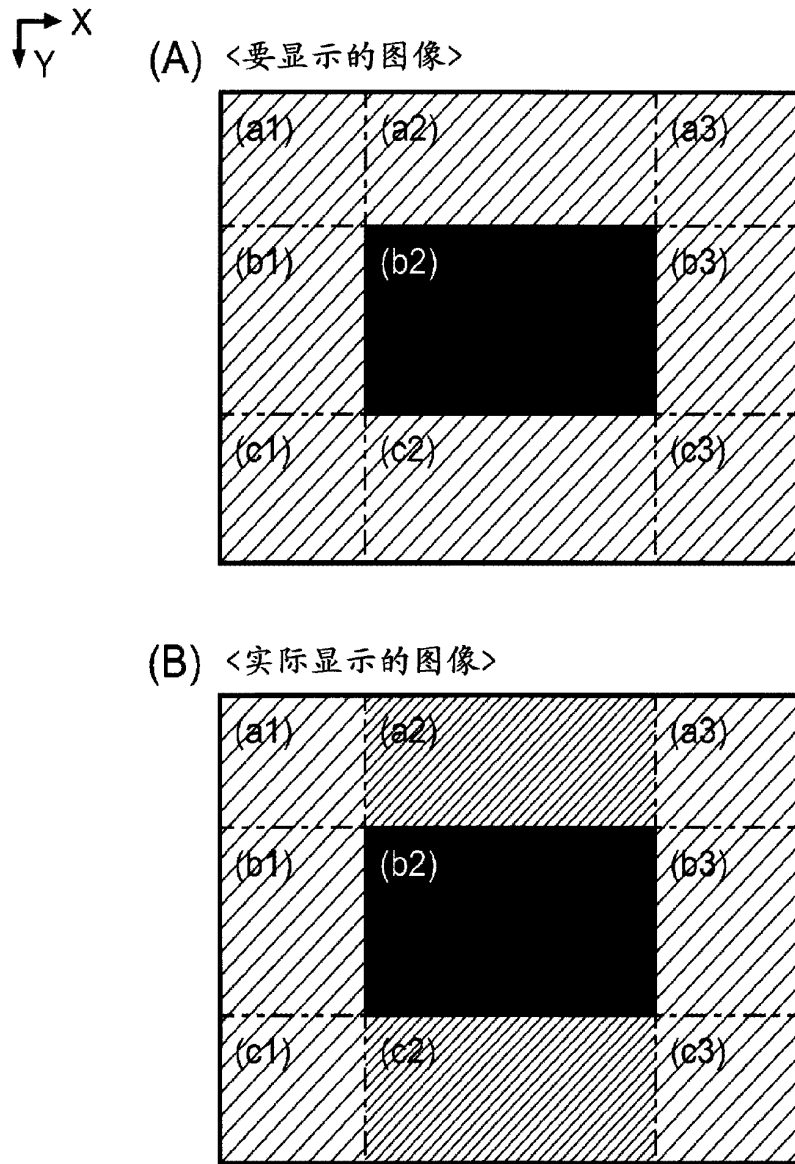


图 9

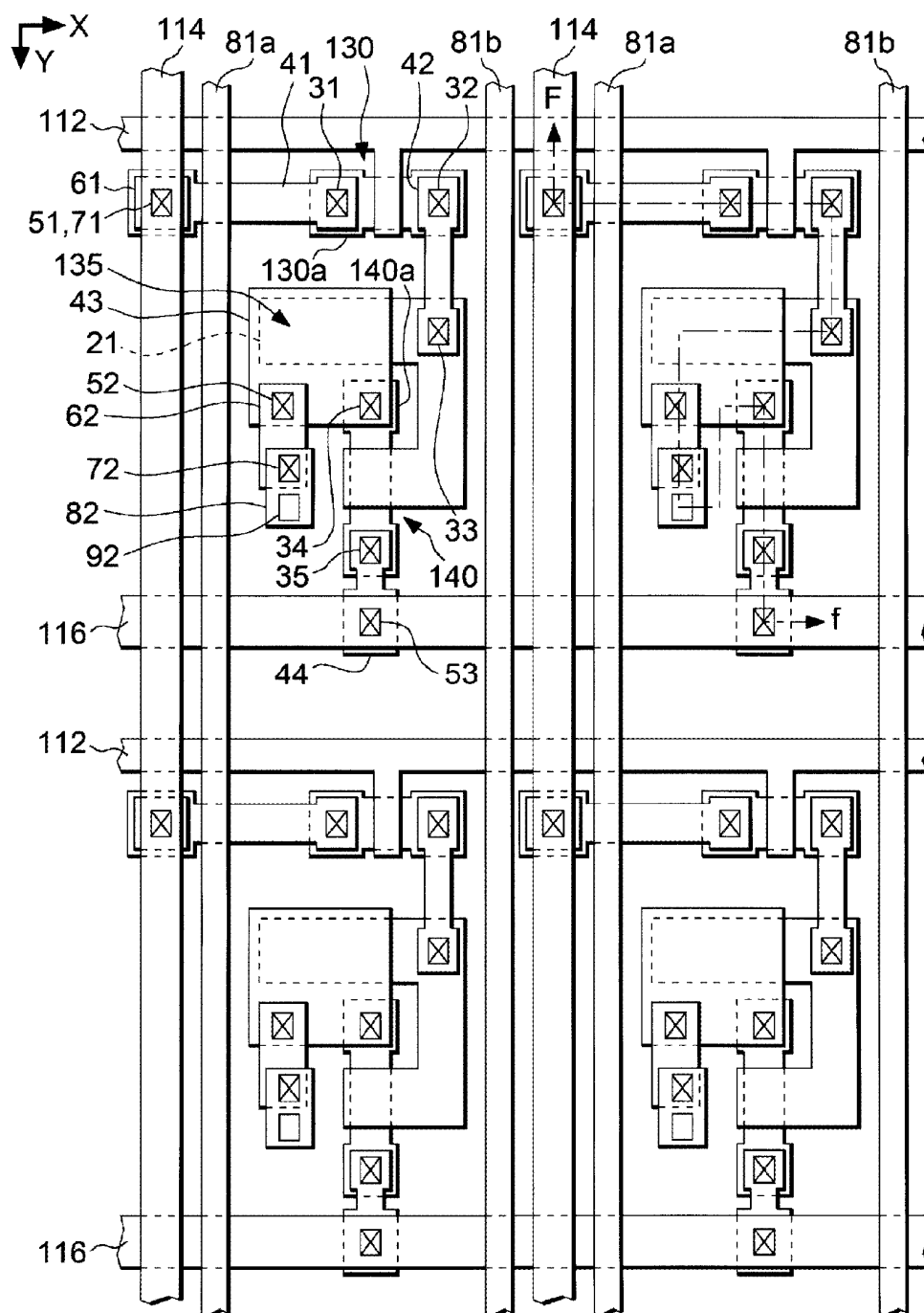


图 10

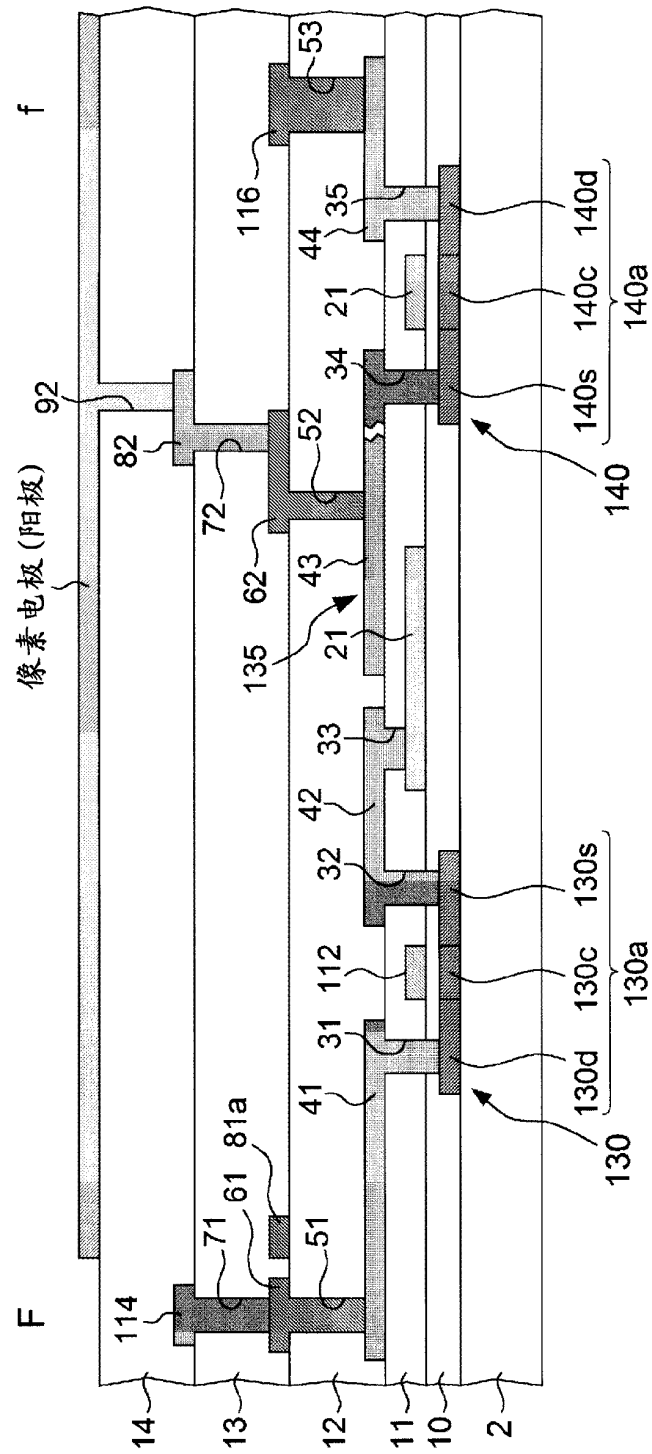


图 11

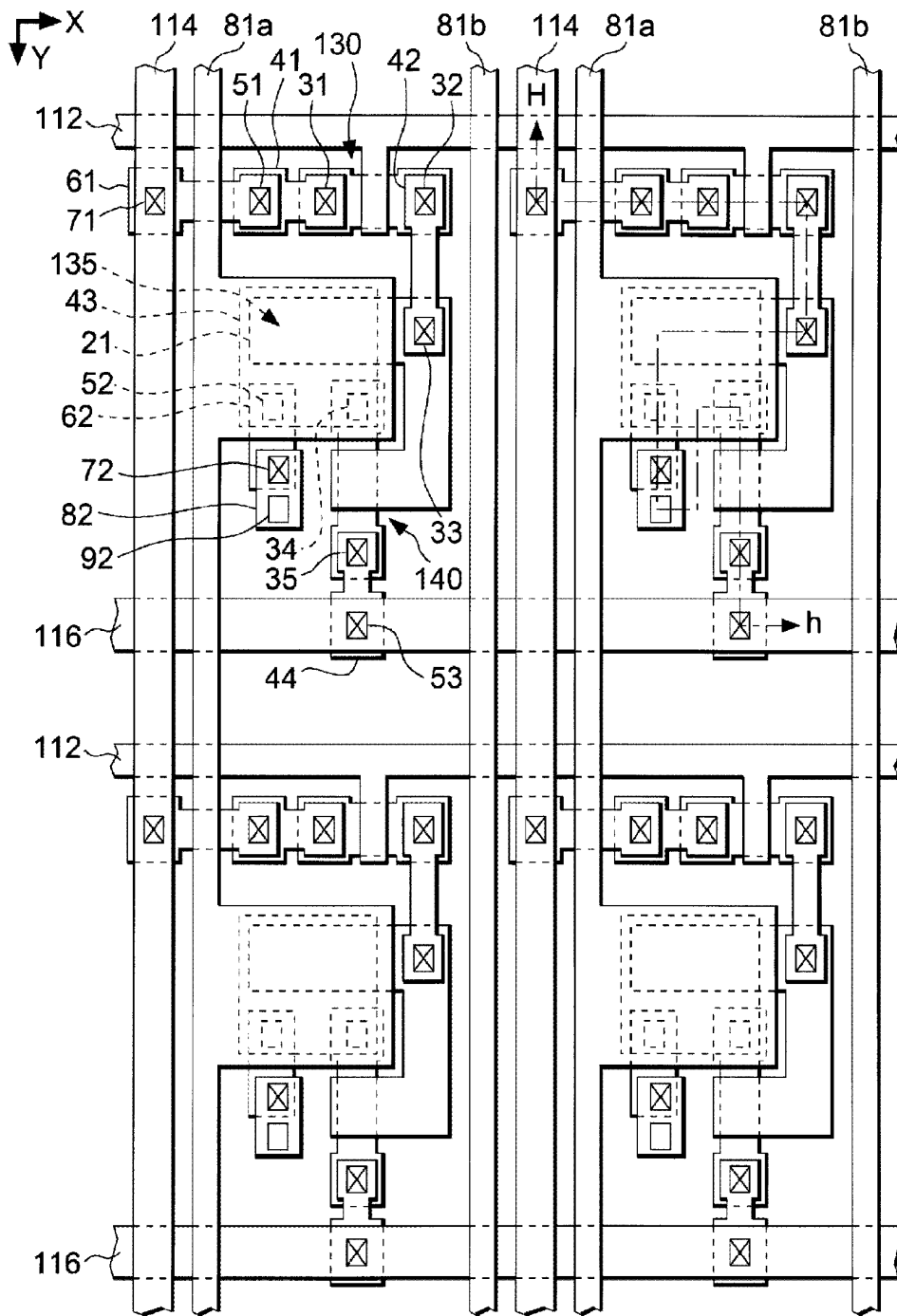


图 12

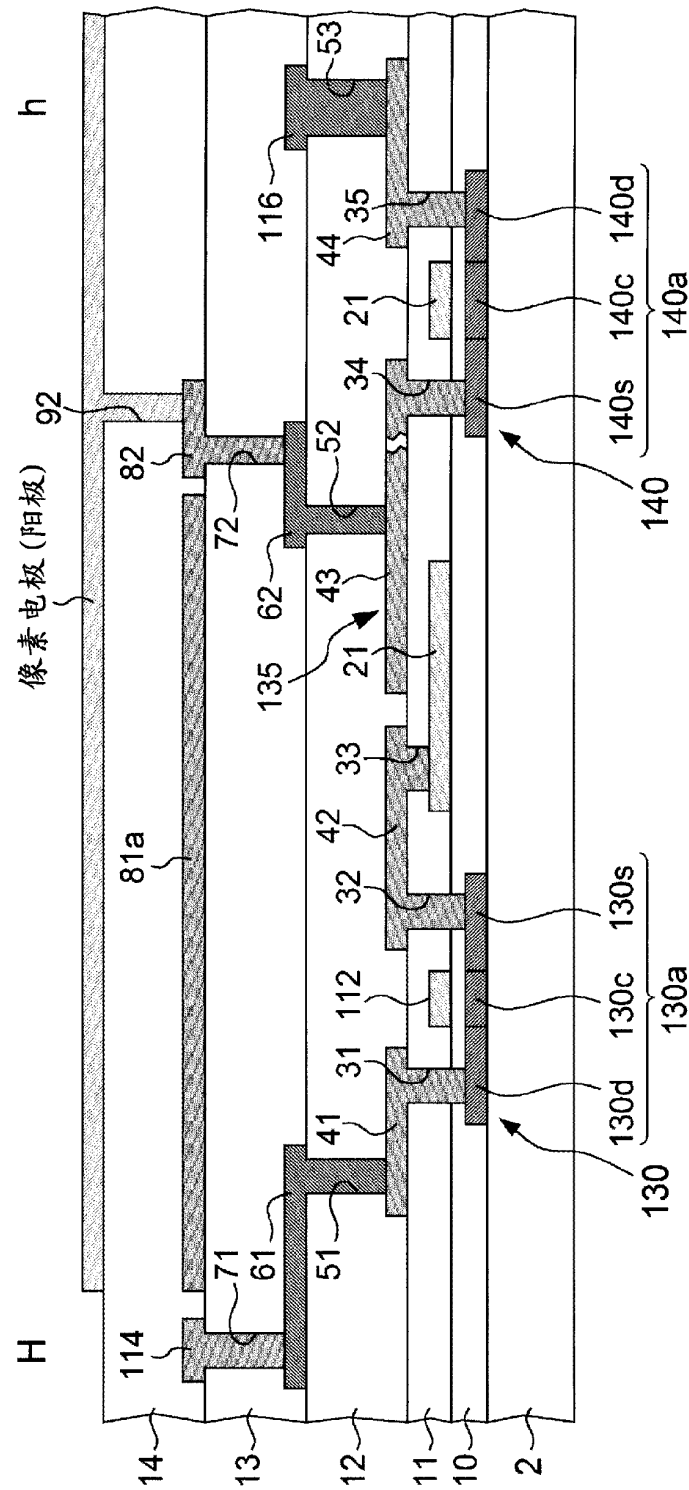


图 13

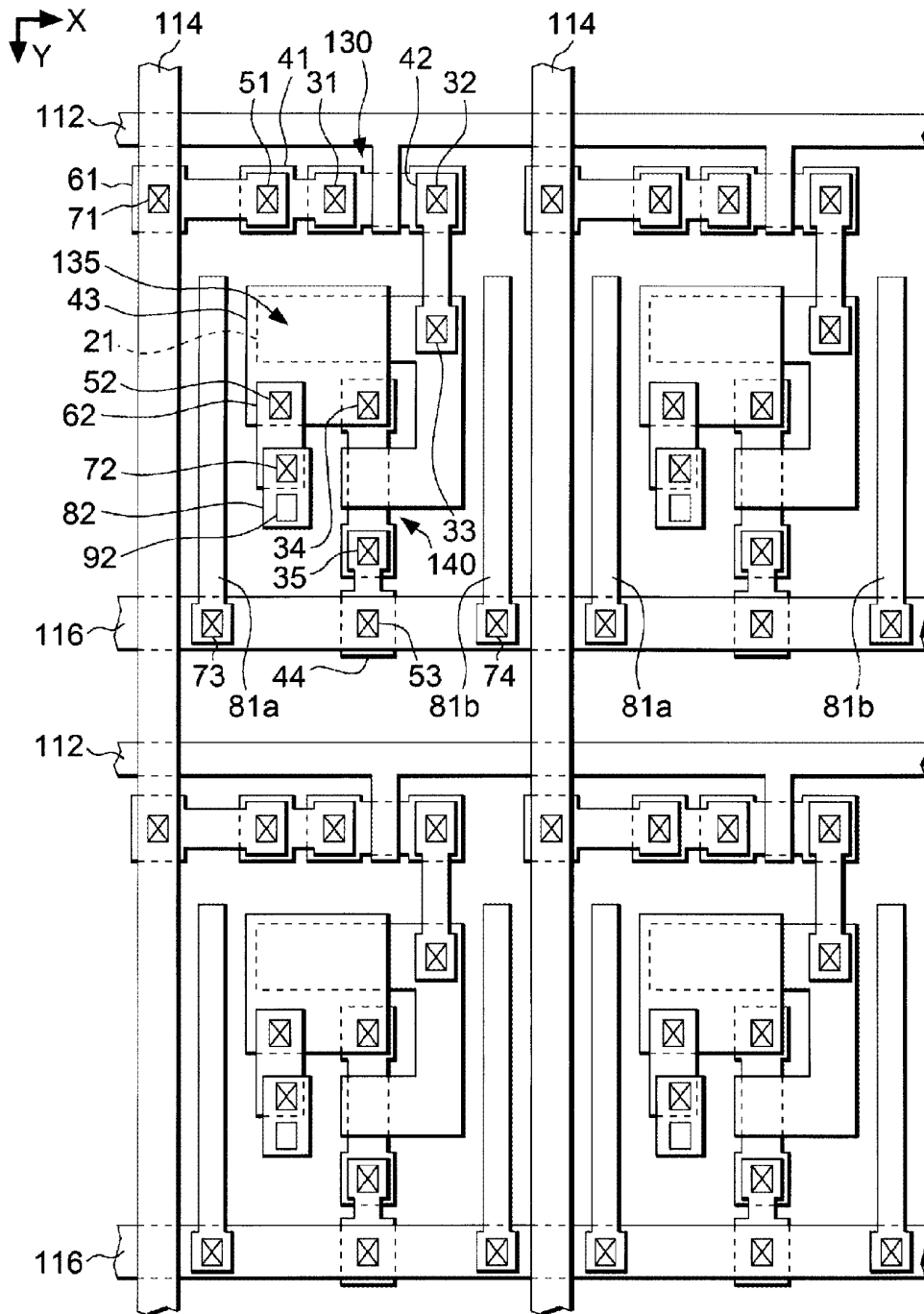


图 14

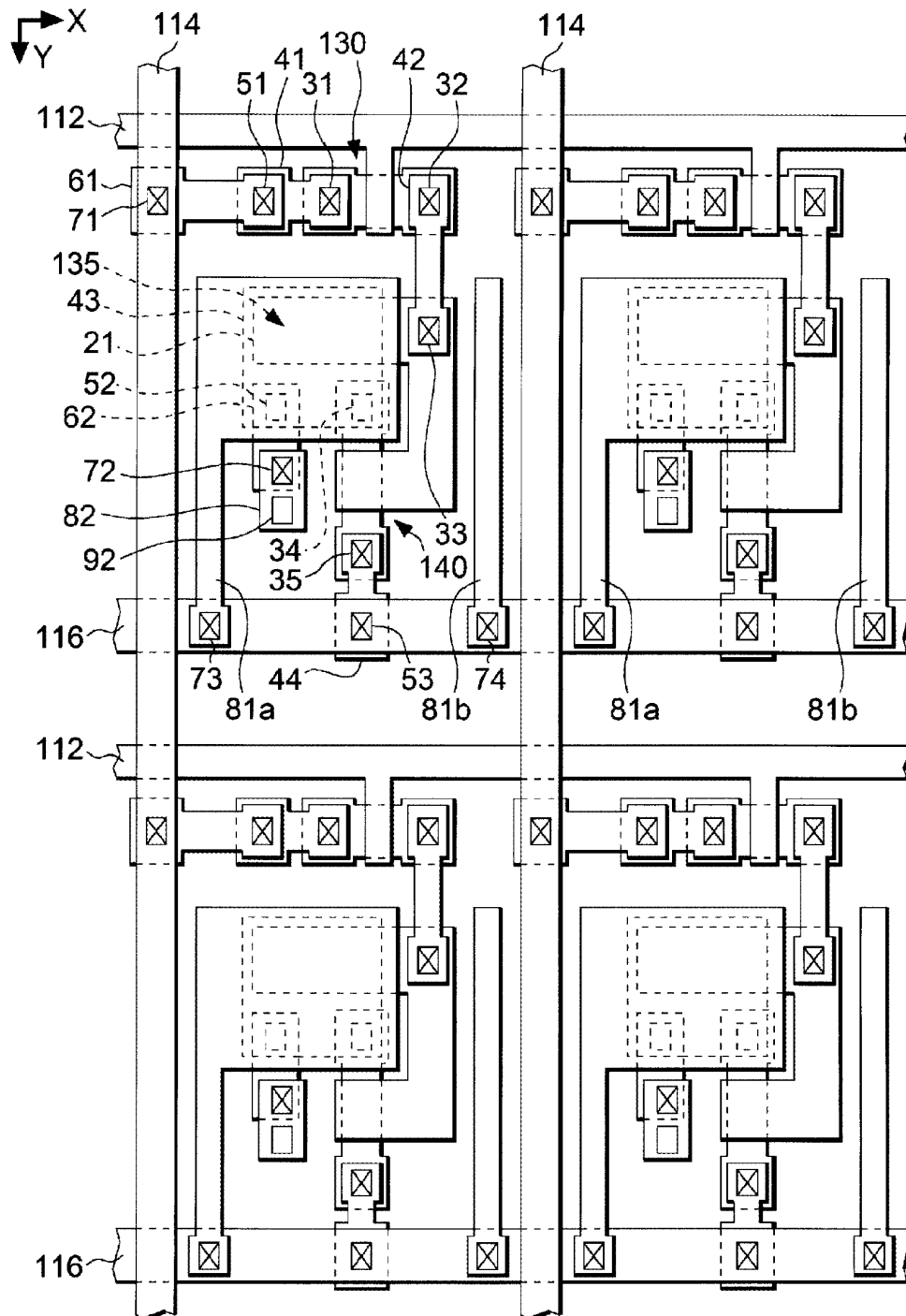


图 15

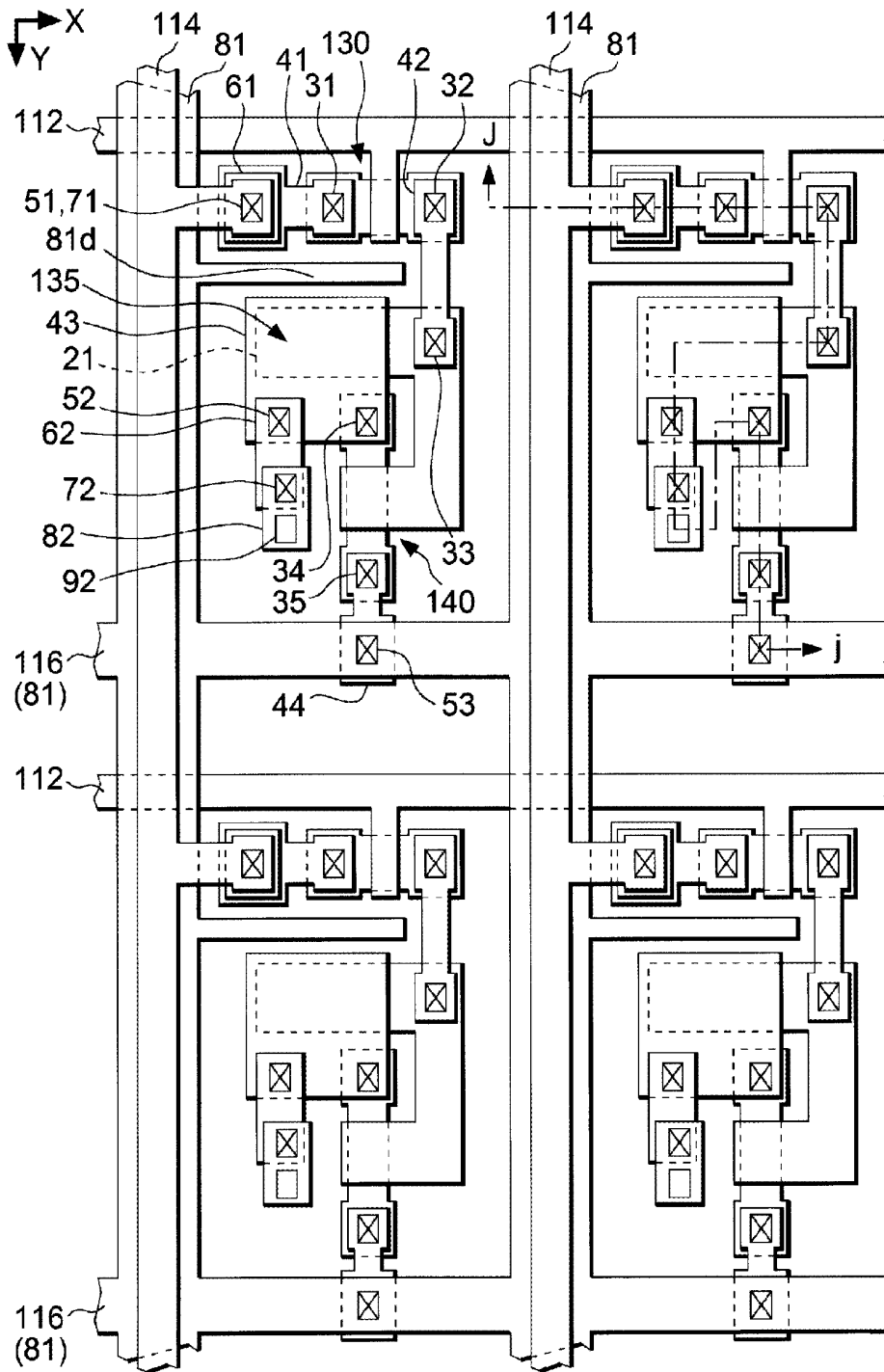


图 16

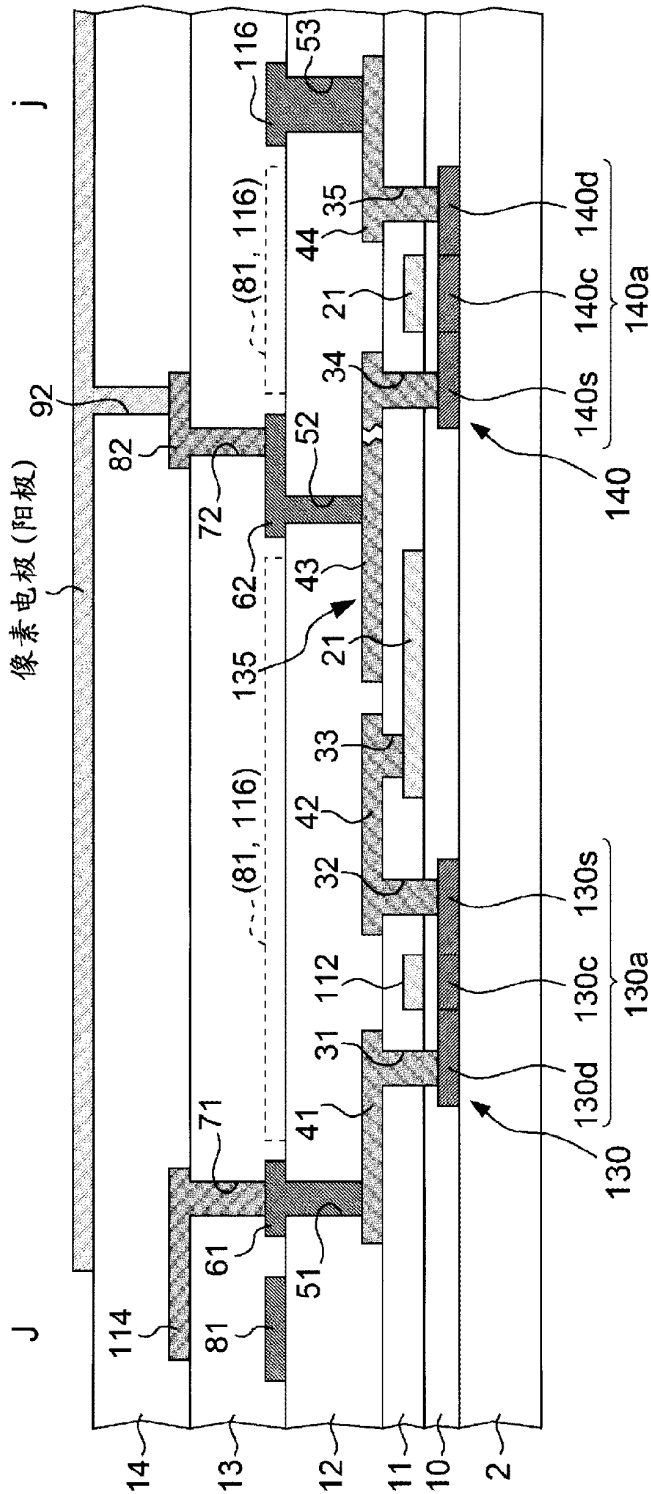


图 17

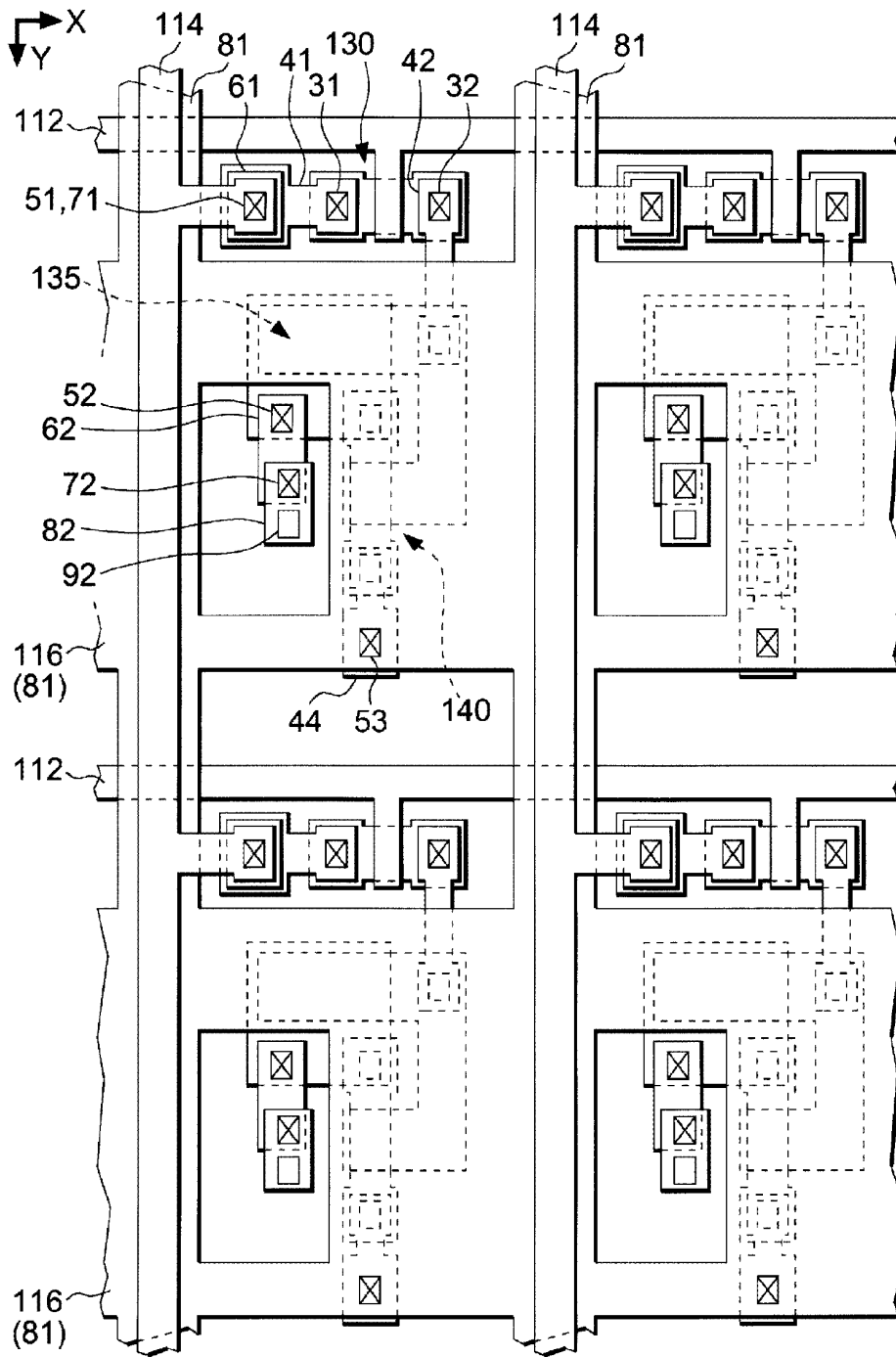


图 18

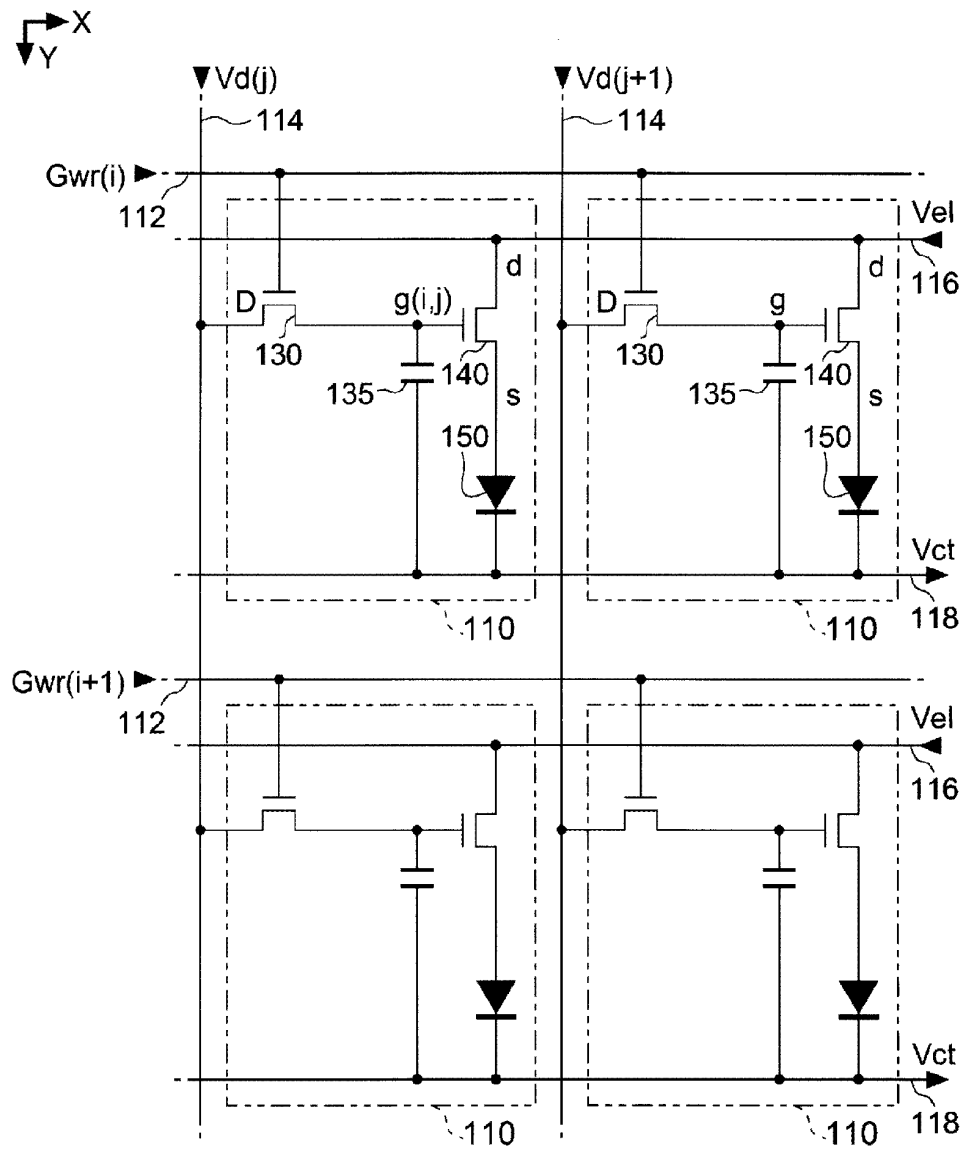


图 19

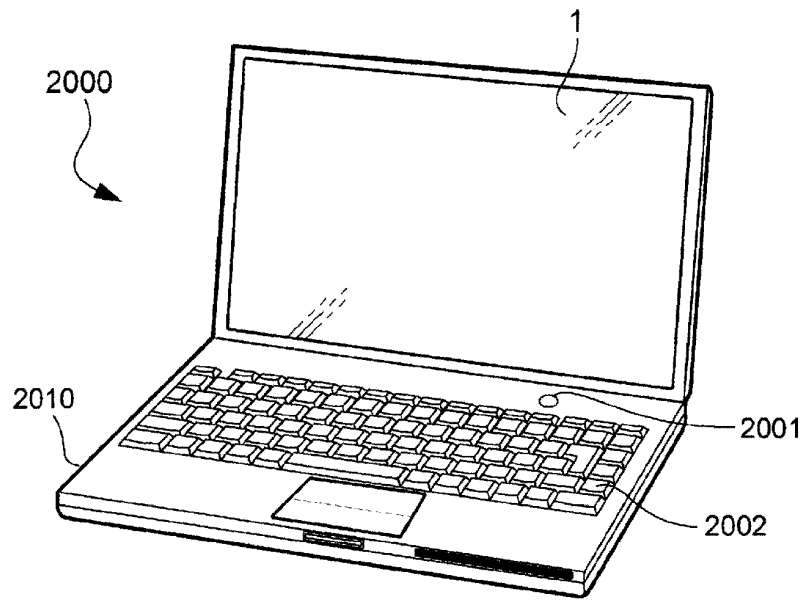


图 20

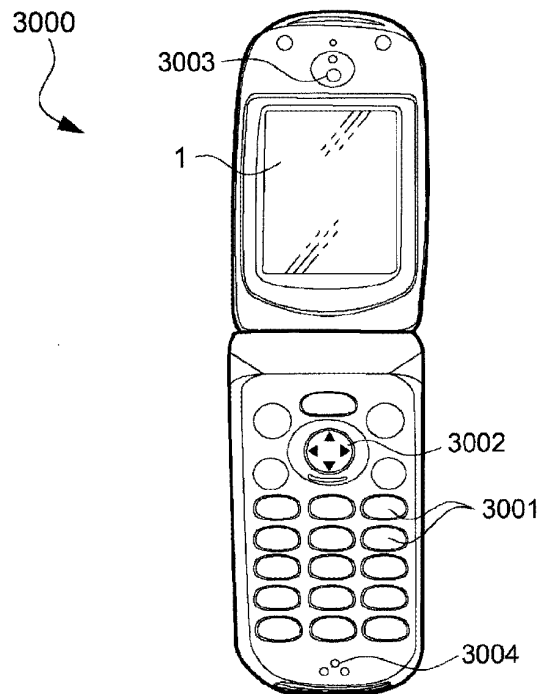


图 21

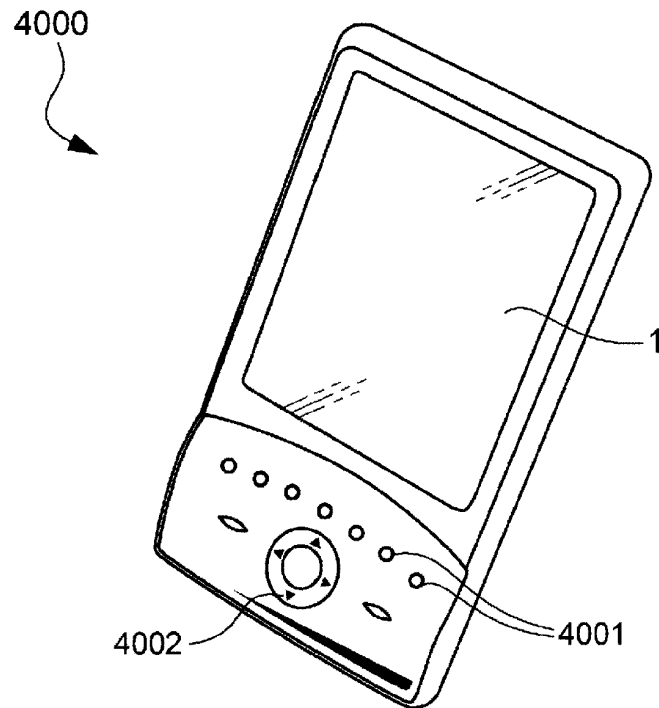


图 22

Electronic Acknowledgement Receipt

EFS ID:	34103859
Application Number:	15838138
International Application Number:	
Confirmation Number:	4358
Title of Invention:	DISPLAY APPARATUS
First Named Inventor/Applicant Name:	Yangwan Kim
Customer Number:	23363
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Filer Authorized By:	Jun-Young E. Jeon
Attorney Docket Number:	148454/411598-03044
Receipt Date:	24-OCT-2018
Filing Date:	11-DEC-2017
Time Stamp:	15:50:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		148454_IDS.PDF	107297	yes	3
			ea3267970da67e4401e97af5900fd8924b344d4f		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Information Disclosure Statement (IDS) Form (SB08)	3	3
	Transmittal Letter	1	2

Warnings:

Information:

2	Foreign Reference	CN_102682697.pdf	7672328	no	38
			5937d3086649b0d67691e7b51ae02d8a0701651e		

Warnings:

Information:

Total Files Size (in bytes):	7779625
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/838,138	12/11/2017	Yangwan Kim	148454/411598-03044	4358
23363 7590 05/18/2018 Lewis Roca Rothgerber Christie LLP PO BOX 29001 Glendale, CA 91209-9001 UNITED STATES OF AMERICA			EXAMINER SMITH, STEPHEN C	
			ART UNIT 2896	PAPER NUMBER
			NOTIFICATION DATE 05/18/2018	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pto@lrrc.com
pair_cph@firsttofile.com

Office Action Summary	Application No. 15/838,138	Applicant(s) KIM ET AL.	
	Examiner STEPHEN C. SMITH	Art Unit 2896	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 12/11/2017.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☒ Claim(s) 1 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☒ Claim(s) 1 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☒ The drawing(s) filed on 12/11/2017 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☒ All b) ☐ Some** c) ☐ None of the:

1. ☒ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

4) ☐ Other: _____.

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

This action is responsive to the claim for U.S. Patent Application No. 15/838,138 filed on December 11, 2017.

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119 (a)-(d). The certified copy has been filed.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on December 11, 2017 was filed and the submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

The drawings submitted on December 11, 2017 are accepted.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

Claim 1 rejected under 35 U.S.C. 102(a)(2) as being anticipated by Lee et al. (US Patent Application Publication No. 2014/0167009).

In claim 1, Lee discloses (see Fig. 8) "a display apparatus comprising: a thin-film transistor (**DT**) comprising a source electrode (**232**), a drain electrode (**234**), and a gate electrode (**226**); a data line (**236**) in a layer different from the source electrode (**232**), the drain electrode (**234**), and the gate electrode (**226**), wherein the data line (**236**) is configured to transmit a data signal; and a shield layer (**239**) between the data line (**236**) and a component of the thin-film transistor (**DT**).” Para. 0096-97.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN C. SMITH whose telephone number is 313-446-4914. The examiner can normally be reached on Monday - Friday 7:30-4:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Art Unit: 2896

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. C. S./

Examiner, Art Unit 2896

/CHEUNG LEE/

Primary Examiner, Art Unit 2896

Notice of References Cited	Application/Control No. 15/838,138		Applicant(s)/Patent Under Reexamination KIM ET AL.	
	Examiner STEPHEN C. SMITH		Art Unit 2896	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2014/0167009 A1	06-2014	Lee; JungHyun	H01L27/3272	257/40
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	1	"20030202267"	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:05
L13	1	"20050068310"	USPAT	OR	OFF	2018/05/03 09:08
L14	1	"20100110050"	USPAT	OR	OFF	2018/05/03 09:13
L15	1	"20120074423"	USPAT	OR	OFF	2018/05/03 09:14
L16	2	"20120074423"	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:14
L17	1	"20120229438"	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:16
L18	2	"20130235020"	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:22
L19	1	"20140062990"	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:24
L20	2	"20140070184"	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:25
L21	0	(thin\$film transistor or TFT) and source electrode and drain electrode and gate electrode and data line and shield layer.clm.	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:30
L22	25371	(H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or G02F1/136213).cpc.	US-PGPUB; USPAT	ADJ	ON	2018/05/03 09:38
L23	0	(thin\$film transistor or TFT) and source electrode and drain electrode and gate electrode and data line and shield layer	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:39
L24	56	(thin\$film transistor or TFT) and source electrode and drain electrode and gate electrode and data line and shield layer.clm.	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:39
L25	205	(thin\$film transistor or TFT) and source electrode and drain electrode and gate electrode and data line and shield layer	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 09:59
L26	93	I22 and I25	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 10:00
L27	112	I25 not I26	US-PGPUB; USPAT	ADJ	OFF	2018/05/03 10:47
S1	10	Kim Yangwan.inv.	US-PGPUB;	ADJ	ON	2016/06/29 14:19

			USPAT			
S2	5	Kwak Wonkyu.inv.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 14:34
S3	1	Noh Jaedu.inv.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 14:37
S4	27	Lee Jaeyong.inv.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 14:37
S5	13026	Samsung Display	US-PGPUB; USPAT	ADJ	ON	2016/06/29 15:25
S6	1568	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer).clm.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 15:27
S7	42	S6 and S5	US-PGPUB; USPAT	ADJ	ON	2016/06/29 15:27
S8	11	("20110102693" "20120074423" "20090009441" "20140062990" "20120229438" "20140098078" "20140167009" "20130235020" "20050068310" "20100110050" "20140070184").PN.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 15:58
S9	12916	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 16:27
S10	1568	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode).clm.	US-PGPUB; USPAT	ADJ	ON	2016/06/29 16:31
S11	147	S9 and S10	US-PGPUB; USPAT	ADJ	ON	2016/06/29 16:31
S12	1	"20160043159"	US-PGPUB; USPAT	ADJ	ON	2016/06/30 07:05
S13	1607	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate)	US-PGPUB; USPAT	ADJ	ON	2016/06/30 08:24
S14	12971	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/06/30 08:25
S15	274	S14 and S13	US-PGPUB; USPAT	ADJ	ON	2016/06/30 08:25
S16	1607	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate)	US-PGPUB; USPAT	ADJ	ON	2016/06/30 14:13
S17	12971	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/06/30 14:13
S18	274	S17 and S16	US-PGPUB; USPAT	ADJ	ON	2016/06/30 14:13

S19	1212	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate) and capacitor	US-PGPUB; USPAT	ADJ	ON	2016/07/12 16:04
S20	13036	H01L27/3272, 124, 3262, 3265, 3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/07/12 16:05
S21	225	S20 and S19	US-PGPUB; USPAT	ADJ	ON	2016/07/12 16:05
S22	13036	H01L27/3272, 124, 3262, 3265, 3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/07/13 08:49
S23	56	(TFT or thin-film transistor or thin film transistor) and (data) and (shield electrode) and (two gate or second gate) and capacitor	US-PGPUB; USPAT	ADJ	ON	2016/07/14 11:17
S24	220	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate) and capacitor and (driving (TFT or thin-film transistor or thin film transistor))	US-PGPUB; USPAT	ADJ	ON	2016/07/14 15:46
S25	13064	H01L27/3272, 124, 3262, 3265, 3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/07/14 15:46
S26	66	S25 and S24	US-PGPUB; USPAT	ADJ	ON	2016/07/14 15:46
S27	154	S24 not S26	US-PGPUB; USPAT	ADJ	ON	2016/07/14 16:13
S28	1	"20070228389"	US-PGPUB; USPAT	ADJ	ON	2016/07/18 11:13
S29	1283	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate) and capacitor	US-PGPUB; USPAT	ADJ	ON	2016/11/18 13:05
S30	14366	H01L27/3272, 124, 3262, 3265, 3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/11/18 13:06
S31	259	S29 and S30	US-PGPUB; USPAT	ADJ	ON	2016/11/18 13:06
S32	14702	H01L27/3272, 124, 3262, 3265, 3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2016/12/20 09:34
S33	1296	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode) and (two gate or second gate) and capacitor	US-PGPUB; USPAT	ADJ	ON	2016/12/20 09:35
S34	33345	(H01L27/3272, 124, 3262, 3265, 3276 or H01L23/5222, 5223, 5225 or H01L2225/06537 or H01L2924/3025).cpc.	US-PGPUB; USPAT	ADJ	ON	2016/12/20 09:59
S35	314	S33 and S34	US-PGPUB; USPAT	ADJ	ON	2016/12/20 09:59
S36	33449	(H01L27/3272, 124, 3262, 3265, 3276 or	US-	ADJ	ON	2016/12/29

		H01L23/5222,5223,5225 or H01L2225/06537 or H01L2924/3025).cpc.	PGPUB; USPAT			08:25
S37	1515	S36 and ((electrical or electromagnetic or electro-magenetic or electric) adj2 (shield or protect\$3))	US-PGPUB; USPAT	ADJ	ON	2016/12/29 08:28
S38	102	S37 and (TFT or thin film transistor)	US-PGPUB; USPAT	ADJ	ON	2016/12/29 08:29
S39	35203	((electrical or electromagnetic or electro-magenetic or electric) adj2 (shield or protect\$3))	US-PGPUB; USPAT	ADJ	ON	2016/12/29 14:37
S40	1219	S39 and (TFT or thin film transistor)	US-PGPUB; USPAT	ADJ	ON	2016/12/29 14:38
S41	1219	S39 and (TFT or thin-film transistor or thin film transistor)	US-PGPUB; USPAT	ADJ	ON	2016/12/29 14:39
S42	886	S41 and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2016/12/29 14:40
S43	613	S42 and capacitor	US-PGPUB; USPAT	ADJ	ON	2016/12/29 14:40
S44	30	S41 and (data or data line) near3 insulat\$3	US-PGPUB; USPAT	ADJ	ON	2016/12/29 14:41
S45	38	thin-film transistor and data line and source electrode and gate electrode and drain electrode and shield layer	US-PGPUB; USPAT	ADJ	ON	2016/12/29 15:08
S46	205	thin-film transistor and data line and source electrode and gate electrode and drain electrode and shield\$3 layer	US-PGPUB; USPAT	ADJ	ON	2016/12/29 15:19
S47	167	S46 not S45	US-PGPUB; USPAT	ADJ	ON	2016/12/29 15:29
S48	2	"20070029644"	US-PGPUB; USPAT	ADJ	ON	2017/03/21 13:25
S49	4	("5811846").PN. OR ("7358532").URPN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2017/03/21 13:25
S50	1	thin-film transistor and data line and source electrode and gate electrode and drain electrode and (electromagnetic adj shield\$3 layer)	US-PGPUB; USPAT	ADJ	ON	2017/03/21 13:29
S51	1	thin-film transistor and data line and source and gate electrode and drain and (electromagnetic adj shield\$3 layer)	US-PGPUB; USPAT	ADJ	ON	2017/03/21 14:04
S52	2	thin-film transistor and data line and (electromagnetic adj shield\$3 layer)	US-PGPUB; USPAT	ADJ	ON	2017/03/21 14:04
S53	1679	(TFT or thin-film transistor or thin film transistor) and (data or data line) and (shield or shield layer or shield electrode).clm.	US-PGPUB; USPAT	ADJ	ON	2017/03/24 10:21
S54	4419	H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or	US-PGPUB;	ADJ	ON	2017/03/24 10:35

		G02F1/136213.cpc.	USPAT			
S55	102	S53 and S54	US-PGPUB; USPAT	ADJ	ON	2017/03/24 10:35
S56	13746	Electr\$3 with shield\$3 and TFT	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:01
S57	8946	Electr\$3 with shield\$3 and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:03
S58	16665	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:03
S59	16665	H01L27/3272,124,3262,3265,3276.cpc.	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:04
S60	8946	Electr\$3 with shield\$3 and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:05
S61	1350	S59 and S60	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:18
S62	4442	Electr\$3 near3 shield\$3 and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:18
S63	641	S59 and S62	US-PGPUB; USPAT	ADJ	ON	2017/07/07 14:19
S64	22540	(H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or G02F1/136213).cpc.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:01
S65	8966	Electr\$3 with shield\$3 and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:01
S66	2375	S64 and S65	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:02
S67	85311	Electr\$3 with (electrode or shield\$3) and TFT and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:03
S68	5	Electr\$3 with (shield) and TFT and (data or data line) same (directly adj overlap\$4)	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:05
S69	21	Electr\$3 with (shield) and TFT and (data or data line) and (directly adj overlap\$4)	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:06
S70	0	Samsung Display "Co.", ltd.as,aanm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:09
S71	0	Samsung Display, ltd.as,aanm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:10
S72	17788	Samsung Display CO ltd.as,aanm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:10
S81	22584	(H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or	US-PGPUB;	ADJ	ON	2017/07/20 09:19

		G02F1/136213).cpc.	USPAT			
S82	22358	S81 and (display or LCD)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:27
S83	17849	S82 and (TFT or thin\$film transistor)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:28
S84	12918	S83 and (data or data line)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:29
S85	46	S83 and (electric\$7 adj shield)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:34
S86	31	S84 and (electric\$7 adj shield)	US-PGPUB; USPAT	ADJ	ON	2017/07/20 09:35
S87	15	S85 not S86	US-PGPUB; USPAT	ADJ	ON	2017/07/20 11:28
S88	2	"20140138651"	US-PGPUB; USPAT	ADJ	ON	2017/07/20 12:09
S89	2	"20130248933"	US-PGPUB; USPAT	ADJ	ON	2017/07/20 12:11

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S73	14	(Electr\$3 with shield\$3) and (directly adj overlap) and (TFT or thin\$film) and (data or data line).clm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 12:59
S74	22540	(H01L27/3272,124,3262,3265,3276,3248 or G02F2001/136218,13629 or G02F1/136213).cpc.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 13:00
S75	17788	Samsung Display CO Ltd.as,aanm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:10
S76	0	S73 and S75	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:11
S77	1217	(Electr\$3 with shield\$3) and (TFT or thin\$film) and connect\$4 same layer same (data or data line).clm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:24
S78	92	(Electr\$3 with shield\$3) same second insulat\$3 and (TFT or thin\$film) and connect\$4 same layer same (data or data line).clm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:25
S79	56	S74 and S78	US-PGPUB; USPAT	ADJ	ON	2017/07/19 15:26
S80	5	(Electr\$3 with shield\$3) same second insulat\$3 and (TFT or thin\$film) and capacitor and (data or data line) near3 layer near3 source.clm.	US-PGPUB; USPAT	ADJ	ON	2017/07/19 16:02

5/ 3/ 2018 12:53:37 PM

C:\ Users\ ssmith4\ Documents\ EAST\ Workspaces\ 15838138.wsp

Search Notes 	Application/Control No. 15838138	Applicant(s)/Patent Under Reexamination KIM ET AL.
	Examiner STEPHEN C SMITH	Art Unit 2896

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/3272,124,3262,3265,3276,3248	5/3/2018	SCS
G02F2001/136218,13629	5/3/2018	SCS
G02F1/136213	5/3/2018	SCS

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
East Text Search			

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
East Text Search of CPC H01L27/3272,124,3262,3265,3276,3248	5/3/2018	SCS
East Text Search of CPC G02F2001/136218,13629	5/3/2018	SCS
East Text Search of CPC G02F1/136213	5/3/2018	SCS

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

/STEPHEN C SMITH/ Examiner.Art Unit 2896	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Attorney Docket Number	148454
	Application Number	To Be Determined
	Filing Date	December 11, 2017
	Inventor(s)	Yangwan Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

U.S. PATENT DOCUMENTS				
EXAMINER INITIALS	Cite No. ¹	DOCUMENT NUMBER Number - Kind Code ² (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
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EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
		EP 1 365 277 A2	11-26-2003	Murade	

EXAMINER SIGNATURE	/STEPHEN C SMITH/	DATE CONSIDERED	05/03/2018
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English Language Translation is attached.

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Sheet 1 of 2

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.C.S/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Attorney Docket Number	148454
	Application Number	To Be Determined
	Filing Date	December 11, 2017
	Inventor(s)	Yangwan Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
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OTHER DOCUMENTS

EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
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SMV 103016275.1-*-12/11/2017 11:03 AM

EXAMINER SIGNATURE	/STEPHEN C SMITH/	DATE CONSIDERED	05/07/2018
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³ Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.			

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Sheet 2 of 2

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별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto
is a true copy from the records of the Korean Intellectual
Property Office.

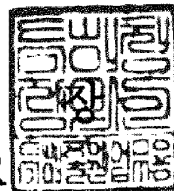
출 원 번 호 : 10-2014-0100700
Application Number

출 원 년 월 일 : 2014년 08월 05일
Filing Date 8월 . 05, 2014

출 원 인 : 삼성디스플레이 주식회사
Applicant(s) Samsung Display Co., Ltd.

2018년 04월 16일

특 허 청
COMMISSIONER



【서지사항】

【서류명】 특허출원서

【참조번호】 15

【출원구분】 특허출원

【출원인】

【명칭】 삼성디스플레이 주식회사

【특허고객번호】 1-2012-016455-2

【대리인】

【명칭】 리앤목 특허법인

【대리인번호】 9-2005-100002-8

【지정된변리사】 이영필, 이해영, 하수영, 박이주, 박기원

【포괄위임등록번호】 2012-055549-3

【발명의 국문명칭】 디스플레이 장치

【발명의 영문명칭】 Display apparatus

【발명자】

【성명】 김양완

【성명의 영문표기】 KIM, Yang Wan

【주민등록번호】 750710-1XXXXXX

【우편번호】 446-711

【주소】 경기도 용인시 기흥구 삼성2로 95 (농서동)

【국적】 KR

【발명자】

【성명】 곽원규

【성명의 영문표기】 KWAK, Won Kyu

【주민등록번호】 721108-1XXXXXX

【우편번호】 446-711

제출 일자 : 2014-08-05

【주소】 경기도 용인시 기흥구 삼성2로 95 (농서동)
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【발명자】
【성명】 노재두
【성명의 영문표기】 NOH, Jae Du
【주민등록번호】 861214-1XXXXXX
【우편번호】 446-711
【주소】 경기도 용인시 기흥구 삼성2로 95 (농서동)
【국적】 KR
【발명자】
【성명】 이재용
【성명의 영문표기】 LEE, Jae Yong
【주민등록번호】 780721-1XXXXXX
【우편번호】 446-711
【주소】 경기도 용인시 기흥구 삼성2로 95 (농서동)
【국적】 KR
【심사청구】 청구
【취지】 위와 같이 특허청장에게 제출합니다.

대리인 리앤목 특허법인 (서명 또는 인)

【수수료】
【출원료】 0 면 46,000 원
【가산출원료】 51 면 0 원
【우선권주장료】 0 건 0 원
【심사청구료】 12 항 671,000 원

55-2

제출 일자 : 2014-08-05

【합계】 717,000 원

【발명의 설명】

【발명의 명칭】

디스플레이 장치{Display apparatus}

【기술분야】

<1> 본 발명의 실시예들은 디스플레이 장치에 관한 것으로서, 더 상세하게는 디스플레이되는 이미지의 품질 저하를 방지할 수 있는 디스플레이 장치에 관한 것이다.

【배경기술】

<2> 일반적으로 유기발광 디스플레이 장치 등은 각 (부)화소의 휘도 등을 제어하기 위해 박막트랜지스터들이 각 (부)화소에 배치된다. 이러한 박막트랜지스터들은 전달된 데이터신호 등에 따라 대응하는 (부)화소의 휘도 등을 제어한다.

<3> 그러나 종래의 디스플레이 장치에는 (부)화소에서 구현되는 휘도 등이 전달된 데이터신호에 따른 휘도 등이 아닌 상이한 휘도 등일 수도 있다는 문제점이 있었다. 이 경우 디스플레이 장치에서 디스플레이되는 이미지는 당초 디스플레이될 이미지와는 상이한 이미지, 즉 품질이 저하된 이미지가 될 수밖에 없다.

【발명의 내용】

【해결하려는 과제】

<4> 본 발명은 상기와 같은 문제점을 포함하여 여러 문제점들을 해결하기 위한 것으로서, 디스플레이되는 이미지의 품질 저하를 방지할 수 있는 디스플레이 장치

를 제공하는 것을 목적으로 한다. 그러나 이러한 과제는 예시적인 것으로, 이에 의해 본 발명의 범위가 한정되는 것은 아니다.

【과제의 해결 수단】

<5> 본 발명의 일 관점에 따르면, 소스전극과 드레인전극과 게이트전극을 포함하는 박막트랜지스터와, 상기 소스전극과 상기 드레인전극과 상기 게이트전극과 상이한 층에 위치하며 데이터신호를 전달하는 데이터선과, 상기 박막트랜지스터의 적어도 일부분과 상기 데이터선 사이에 위치하는 실드층을 구비하는, 디스플레이 장치가 제공된다.

<6> 상기 실드층은 상기 소스전극과 상기 데이터선 사이와, 상기 드레인전극과 상기 데이터선 사이와, 상기 게이트전극과 상기 데이터선 사이 중 적어도 어느 한 곳에 위치할 수 있다.

<7> 제1스토리지 축전판과, 상기 제1스토리지 축전판과 중첩되며 상기 제1스토리지 축전판 상부에 위치한 제2스토리지 축전판을 포함하는 스토리지 캐패시터를 더 구비하고, 상기 데이터선은 상기 제2스토리지 축전판보다 상부층에 위치하며, 상기 실드층은 상기 제2스토리지 축전판의 일부분으로서, 상기 게이트전극과 상기 데이터선 사이로 연장된 부분 또는 상기 데이터선 하부로 연장된 부분일 수 있다.

<8> 이때, 상기 제1스토리지 축전판은 상기 게이트전극과 전기적으로 연결될 수 있다. 나아가, 상기 제1스토리지 축전판과 상기 게이트전극은 일체(一體)일 수 있다.

<9> 한편, 상기 게이트전극은 제1게이트전극과 제2게이트전극을 포함하고, 상기 실드층은 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부와 상기 데이터선 사이에 위치할 수 있다.

<10> 이때, 제1스토리지 축전판과, 상기 제1스토리지 축전판과 중첩되며 상기 제1스토리지 축전판 상부에 위치한 제2스토리지 축전판을 포함하는 스토리지 캐패시터를 더 구비하고, 상기 데이터선은 상기 제2스토리지 축전판보다 상부층에 위치하며, 상기 실드층은 상기 제2스토리지 축전판의 일부분으로서, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부와 상기 데이터선 사이로 연장된 부분, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부 상부로 연장된 부분 또는 상기 데이터선 하부로 연장된 부분일 수 있다.

<11> 나아가, 상기 제1스토리지 축전판과 전기적으로 연결된 구동 게이트전극과, 상기 소스전극과 전기적으로 연결된 구동 드레인전극을 포함하는 구동 박막트랜지스터를 더 구비하고, 상기 제1스토리지 축전판은 상기 드레인전극과 전기적으로 연결될 수 있다.

<12> 또는, 제1스토리지 축전판과, 상기 제1스토리지 축전판과 중첩되며 상기 제1스토리지 축전판 상부에 위치한 제2스토리지 축전판을 포함하는 스토리지 캐패시터와, 구동 박막트랜지스터의 상기 제1스토리지 축전판과 전기적으로 연결되는 구동 게이트전극에 전달할 초기화전압을 전달하며 상기 제2스토리지 축전판과 동일층에 위치하는 초기화전압선을 더 구비하고, 상기 드레인전극은 상기 제1스토리지 축전

판에 전기적으로 연결되고, 상기 소스전극은 상기 초기화전압선에 전기적으로 연결되며, 상기 데이터선은 상기 제2스토리지 축전판보다 상부층에 위치하고, 상기 실드층은 상기 초기화전압선의 일부분으로서, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부와 상기 데이터선 사이로 연장된 부분, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부 상부로 연장된 부분 또는 상기 데이터선 하부로 연장된 부분일 수 있다.

<13> 본 발명의 다른 일 관점에 따르면, (i) 소스전극과 드레인전극과 게이트전극을 포함하는 박막트랜지스터와, (ii) 상기 소스전극, 상기 드레인전극 및 상기 게이트전극과 상이한 층에 위치하며 데이터신호를 전달하는 데이터선과, (iii) 상기 드레인전극과 전기적으로 연결되는 제1스토리지 축전판과, 상기 제1스토리지 축전판과 중첩되도록 상기 제1스토리지 축전판이 위치한 층과 상이한 층에 위치한 제2스토리지 축전판을 포함하는 스토리지 캐패시터와, (iv) 구동 박막트랜지스터의 상기 제1스토리지 축전판과 전기적으로 연결되는 구동 게이트전극에 전달할 초기화전압을 전달하며, 상기 소스전극과 전기적으로 연결되는, 초기화전압선을 구비하고, 상기 게이트전극은 제1게이트전극과 제2게이트전극을 포함하고, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분과 상기 데이터선 사이에 상기 제1게이트전극과 상기 제2게이트전극 중 어느 하나가 적어도 부분적으로 위치하도록 할 수 있다.

<14> 이때, 상기 제1게이트전극과 상기 제2게이트전극 중 상기 박막트랜지스터의

상기 제1게이트전극과 상기 제2게이트전극 사이의 부분과 상기 데이터선 사이에 위치하는 것은, 상기 데이터선의 하부 또는 상부까지 연장되도록 할 수 있다.

<15> 본 발명의 또 다른 일 관점에 따르면, 소스전극과 드레인전극과 게이트전극을 포함하는 박막트랜지스터와, 상기 소스전극과 상기 드레인전극과 상기 게이트전극과 상이한 층에 위치하며 제어신호를 전달하는 제어신호선과, 상기 박막트랜지스터의 적어도 일부분과 상기 제어신호선 사이에 위치하는 실드층을 구비하는, 디스플레이 장치가 제공된다.

<16> 전술한 것 외의 다른 측면, 특징, 이점은 이하의 발명을 실시하기 위한 구체적인 내용, 특허청구범위 및 도면으로부터 명확해질 것이다.

【발명의 효과】

<17> 상기한 바와 같이 이루어진 본 발명의 일 실시예에 따르면, 디스플레이되는 이미지의 품질 저하를 방지할 수 있는 디스플레이 장치를 구현할 수 있다. 물론 이러한 효과에 의해 본 발명의 범위가 한정되는 것은 아니다.

【도면의 간단한 설명】

<18> 도 1은 본 발명의 일 실시예에 따른 유기발광 디스플레이 장치의 하나의 (부)화소의 등가 회로도이다.

도 2는 도 1의 (부)화소에 있어서의 복수개의 박막트랜지스터들 및 캐패시터 등의 위치를 개략적으로 도시하는 배치도이다.

도 3 내지 도 6은 도 2의 복수개의 박막트랜지스터들 및 캐패시터 등의 구성

요소들을 층별로 개략적으로 도시하는 배치도들이다.

도 7은 도 2의 VII-VII선을 따라 취한 단면도이다.

도 8은 다른 일 실시예에 따른 유기발광 디스플레이 장치의 단면도이다.

도 9는 도 2의 IX-IX선을 따라 취한 단면도이다.

도 10은 도 2의 X-X선을 따라 취한 단면도이다.

도 11은 본 발명의 또 다른 일 실시예에 따른 유기발광 디스플레이 장치의 일 (부)화소에 있어서의 복수개의 박막트랜지스터들 및 캐패시터 등의 위치를 개략적으로 도시하는 배치도이다.

도 12는 도 11의 XII-XII선을 따라 취한 단면도이다.

【발명을 실시하기 위한 구체적인 내용】

<19> 본 발명은 다양한 변환을 가할 수 있고 여러 가지 실시예를 가질 수 있는 바, 특정 실시예들을 도면에 예시하고 상세한 설명에 상세하게 설명하고자 한다. 본 발명의 효과 및 특징, 그리고 그것들을 달성하는 방법은 도면과 함께 상세하게 후술되어 있는 실시예들을 참조하면 명확해질 것이다. 그러나 본 발명은 이하에서 개시되는 실시예들에 한정되는 것이 아니라 다양한 형태로 구현될 수 있다.

<20> 이하, 첨부된 도면을 참조하여 본 발명의 실시예들을 상세히 설명하기로 하며, 도면을 참조하여 설명할 때 동일하거나 대응하는 구성 요소는 동일한 도면부호를 부여하고 이에 대한 중복되는 설명은 생략하기로 한다.

<21> 이하의 실시예에서 층, 막, 영역, 판 등의 각종 구성요소가 다른 구성요소

"상에" 있다고 할 때, 이는 다른 구성요소 "바로 상에" 있는 경우뿐 아니라 그 사이에 다른 구성요소가 개재된 경우도 포함한다. 또한 설명의 편의를 위하여 도면에서는 구성 요소들이 그 크기가 과장 또는 축소될 수 있다. 예컨대, 도면에서 나타난 각 구성의 크기 및 두께는 설명의 편의를 위해 임의로 나타내었으므로, 본 발명이 반드시 도시된 바에 한정되지 않는다.

<22> 이하의 실시예에서, x축, y축 및 z축은 직교 좌표계 상의 세 축으로 한정되지 않고, 이를 포함하는 넓은 의미로 해석될 수 있다. 예를 들어, x축, y축 및 z축은 서로 직교할 수도 있지만, 서로 직교하지 않는 서로 다른 방향을 지칭할 수도 있다.

<23> 도 1은 본 발명의 일 실시예에 따른 유기발광 디스플레이 장치의 하나의 (부)화소의 등가 회로도이다.

<24> 도 1에 도시한 바와 같이, 본 발명의 일 실시예에 따른 유기발광 디스플레이 장치의 하나의 (부)화소는 복수개의 신호선들(121, 122, 123, 124, 171, 172), 복수개의 신호선들에 연결되어 있는 복수개의 박막트랜지스터들(T1, T2, T3, T4, T5, T6), 스토리지 캐패시터(storage capacitor, Cst) 및 유기발광소자(organic light-emitting device, OLED)를 포함한다. 물론 복수개의 신호선들(121, 122, 123, 124, 171, 172)은 복수개의 (부)화소들에 있어서 공유될 수 있다.

<25> 박막트랜지스터는 구동 박막트랜지스터(driving TFT, T1), 스위칭 박막트랜지스터(switching TFT, T2), 보상 박막트랜지스터(T3), 초기화 박막트랜지스터(T4), 동작제어 박막트랜지스터(T5) 및 발광제어 박막트랜지스터(T6)를 포함한다.

<26> 신호선은 스캔신호(Sn)를 전달하는 스캔선(121), 초기화 박막트랜지스터(T4)에 이전 스캔신호(Sn-1)를 전달하는 이전 스캔선(122), 동작제어 박막트랜지스터(T5) 및 발광제어 박막트랜지스터(T6)에 발광제어신호(En)를 전달하는 발광제어선(123), 스캔선(121)과 교차하며 데이터신호(Dm)를 전달하는 데이터선(171), 구동전압(ELVDD)을 전달하며 데이터선(171)과 거의 평행하게 형성되어 있는 구동전압선(172), 구동 박막트랜지스터(T1)를 초기화하는 초기화전압(Vint)을 전달하는 초기화전압선(124)을 포함한다.

<27> 구동 박막트랜지스터(T1)의 게이트전극(G1)은 스토리지 캐패시터(Cst)의 제1 스토리지 축전판(Cst1)에 연결되어 있고, 구동 박막트랜지스터(T1)의 소스전극(S1)은 동작제어 박막트랜지스터(T5)를 경유하여 구동전압선(172)에 연결되어 있으며, 구동 박막트랜지스터(T1)의 드레인전극(D1)은 발광제어 박막트랜지스터(T6)를 경유하여 유기발광소자(OLED)의 화소전극과 전기적으로 연결되어 있다. 구동 박막트랜지스터(T1)는 스위칭 박막트랜지스터(T2)의 스위칭 동작에 따라 데이터신호(Dm)를 전달받아 유기발광소자(OLED)에 구동전류(I_{OLED})를 공급한다.

<28> 스위칭 박막트랜지스터(T2)의 게이트전극(G2)은 스캔선(121)에 연결되어 있고, 스위칭 박막트랜지스터(T2)의 소스전극(S2)은 데이터선(171)에 연결되어 있으며, 스위칭 박막트랜지스터(T2)의 드레인전극(D2)은 구동 박막트랜지스터(T1)의 소스전극(S1)에 연결되어 있으면서 동작제어 박막트랜지스터(T5)를 경유하여 구동전압선(172)에 연결되어 있다. 이러한 스위칭 박막트랜지스터(T2)는 스캔선(121)을

통해 전달받은 스캔신호(Sn)에 따라 턴-온되어 데이터선(171)으로 전달된 데이터 신호(Dm)를 구동 박막트랜지스터(T1)의 소스전극으로 전달하는 스위칭 동작을 수행한다.

<29> 보상 박막트랜지스터(T3)의 게이트전극(G3)은 스캔선(121)에 연결되어 있고, 보상 박막트랜지스터(T3)의 소스전극(S3)은 구동 박막트랜지스터(T1)의 드레인전극(D1)에 연결되어 있으면서 발광제어 박막트랜지스터(T6)를 경유하여 유기발광소자(OLED)의 화소전극과 연결되어 있고, 보상 박막트랜지스터(T3)의 드레인전극(D3)은 스토리지 캐패시터(Cst)의 제1스토리지 축전판(Cst1), 초기화 박막트랜지스터(T4)의 드레인전극(D4) 및 구동 박막트랜지스터(T1)의 게이트전극(G1)에 연결되어 있다. 이러한 보상 박막트랜지스터(T3)는 스캔선(121)을 통해 전달받은 스캔신호(Sn)에 따라 턴-온되어 구동 박막트랜지스터(T1)의 게이트전극(G1)과 드레인전극(D1)을 전기적으로 연결하여 구동 박막트랜지스터(T1)를 다이오드 연결시킨다.

<30> 초기화 박막트랜지스터(T4)의 게이트전극(G4)은 이전 스캔선(122)에 연결되어 있고, 초기화 박막트랜지스터(T4)의 소스전극(S4)은 초기화전압선(124)에 연결되어 있으며, 초기화 박막트랜지스터(T4)의 드레인전극(D4)은 스토리지 캐패시터(Cst)의 제1스토리지 축전판(Cst1), 보상 박막트랜지스터(T3)의 드레인전극(D3) 및 구동 박막트랜지스터(T1)의 게이트전극(G1)에 연결되어 있다. 이러한 초기화 박막트랜지스터(T4)는 이전 스캔선(122)을 통해 전달받은 이전 스캔신호(Sn-1)에 따라 턴-온되어 초기화전압(Vint)을 구동 박막트랜지스터(T1)의 게이트전극(G1)에 전달하여 구동 박막트랜지스터(T1)의 게이트전극(G1)의 전압을 초기화시키는 초기화동

작을 수행한다.

<31> 동작제어 박막트랜지스터(T5)의 게이트전극(G5)은 발광제어선(123)에 연결되어 있으며, 동작제어 박막트랜지스터(T5)의 소스전극(S5)은 구동전압선(172)과 연결되어 있고, 동작제어 박막트랜지스터(T5)의 드레인전극(D5)은 구동 박막트랜지스터(T1)의 소스전극(S1) 및 스위칭 박막트랜지스터(T2)의 드레인전극(D2)과 연결되어 있다.

<32> 발광제어 박막트랜지스터(T6)의 게이트전극(G6)은 발광제어선(123)에 연결되어 있고, 발광제어 박막트랜지스터(T6)의 소스전극(S6)은 구동 박막트랜지스터(T1)의 드레인전극(D1) 및 보상 박막트랜지스터(T3)의 소스전극(S3)에 연결되어 있으며, 발광제어 박막트랜지스터(T6)의 드레인전극(D6)은 유기발광소자(OLED)의 화소전극에 전기적으로 연결되어 있다. 이러한 동작제어 박막트랜지스터(T5) 및 발광제어 박막트랜지스터(T6)는 발광제어선(123)을 통해 전달받은 발광제어신호(En)에 따라 동시에 턴-온되어, 구동전압(ELVDD)이 유기발광소자(OLED)에 전달되어 유기발광소자(OLED)에 구동전류(I_{OLED})가 흐르도록 한다.

<33> 스토리지 캐패시터(Cst)의 제2스토리지 축전판(Cst2)은 구동전압선(172)에 연결되어 있으며, 유기발광소자(OLED)의 대향전극은 공통전압(ELVSS)에 연결되어 있다. 이에 따라, 유기발광소자(OLED)는 구동 박막트랜지스터(T1)로부터 구동전류(I_{OLED})를 전달받아 발광함으로써 화상을 표시할 수 있다.

<34> 이하에서 이러한 유기발광 디스플레이 장치의 한 화소의 구체적인 동작을 개

략적으로 설명한다.

<35> 먼저, 초기화 기간 동안 이전 스캔선(122)을 통해 로우레벨(low level)의 이전 스캔신호(Sn-1)가 공급된다. 그러면, 로우레벨의 이전 스캔신호(Sn-1)에 대응하여 초기화 박막트랜지스터(T4)가 턴-온(Turn on)되어, 초기화 박막트랜지스터(T4)를 통해 초기화전압선(124)으로부터의 초기화전압(Vint)이 구동 박막트랜지스터(T1)의 게이트전극에 전달되고, 이에 따라 초기화전압(Vint)에 의해 구동 박막트랜지스터(T1)가 초기화된다.

<36> 이 후, 데이터 프로그래밍 기간 중 스캔선(121)을 통해 로우레벨의 스캔신호(Sn)가 공급된다. 그러면, 로우레벨의 스캔신호(Sn)에 대응하여 스위칭 박막트랜지스터(T2) 및 보상 박막트랜지스터(T3)가 턴-온된다. 이에 따라 구동 박막트랜지스터(T1)는 턴-온된 보상 박막트랜지스터(T3)에 의해 다이오드 연결되고, 순방향으로 바이어스 된다. 그러면, 데이터선(171)으로부터 공급된 데이터신호(Dm)에서 구동 박막트랜지스터(T1)의 문턱전압(Threshold voltage, V_{th})만큼 감소한 보상전압($Dm+V_{th}$, V_{th} 는 (-)의 값)이 구동 박막트랜지스터(T1)의 게이트전극(G1)에 인가된다. 그리고 스토리지 커패시터(Cst)의 양단에는 구동전압(ELVDD)과 보상전압($Dm+V_{th}$)이 인가되어, 스토리지 커패시터(Cst)에는 양단 전압차에 대응하는 전하가 저장된다.

<37> 이 후, 발광기간 동안 발광제어선(123)으로부터 공급되는 발광제어신호(En)가 하이레벨에서 로우레벨로 변경된다. 그러면, 발광기간 동안 로우레벨의 발광제어신호(En)에 의해 동작제어 박막트랜지스터(T5) 및 발광제어 박막트랜지스터(T6)

가 턴-온된다. 그러면, 구동 박막트랜지스터(T1)의 게이트전극의 전압과 구동전압(ELVDD) 간의 전압차에 따라 결정되는 구동전류(I_{OLED})가 발생하고, 발광제어 박막트랜지스터(T6)를 통해 구동전류(I_{OLED})가 유기발광소자(OLED)에 공급된다. 발광기간동안 스토리지 캐패시터(Cst)에 의해 구동 박막트랜지스터(T1)의 게이트-소스 전압(V_{GS})은 ' $(Dm+V_{th})-ELVDD$ '으로 유지되며, 구동 박막트랜지스터(T1)의 전류-전압 관계에 따르면 구동전류(I_{OLED})는 게이트-소스 전압(V_{GS})에서 문턱전압(V_{th})을 차감한 값의 제곱인 ' $(Dm-ELVDD)^2$ '에 비례하기에, 구동전류(I_{OLED})는 구동 박막트랜지스터(T1)의 문턱전압(V_{th})에 관계없이 결정된다.

<38> 이하에서는 도 1에 도시된 유기발광 디스플레이 장치의 일 (부)화소의 상세 구조에 대해 도 2 내지 도 10을 참조하여 설명한다.

<39> 도 2는 도 1의 (부)화소에 있어서의 복수개의 박막트랜지스터들 및 캐패시터 등의 위치를 개략적으로 도시하는 배치도이다. 도 3 내지 도 6은 도 2의 복수개의 박막트랜지스터들 및 캐패시터 등의 구성요소들을 층별로 개략적으로 도시하는 배치도들이다. 즉, 도 3 내지 도 6 각각은 동일층에 위치하는 배선이나 반도체층 등의 배치를 도시한 것으로서, 도 3 내지 도 6에 도시된 층상 구조들 사이에는 절연층 등이 개재될 수 있다. 예컨대 도 3에 도시된 층과 도 4에 도시된 층 사이에는 제1절연층(141, 도 7 참조)이 개재되고, 도 4에 도시된 층과 도 5에 도시된 층 사이에는 제2절연층(142, 도 7 참조)이 개재되며, 도 5에 도시된 층과 도 6에 도시된

층 사이에는 중간절연층(160, 도 7 참조)이 게재될 수 있다. 물론 그러한 절연층들에는 콘택홀 등이 형성되어, 도 3 내지 도 6에 도시된 층상 구조들이 상하로 서로 전기적으로 연결될 수도 있다.

<40> 본 실시예에 따른 유기발광 디스플레이 장치의 (부)화소는 스캔신호(Sn), 이전 스캔신호(Sn-1), 발광제어신호(En) 및 초기화전압(Vint)을 각각 인가하며 행 방향을 따라 형성되어 있는 스캔선(121), 이전 스캔선(122), 발광제어선(123) 및 초기화전압선(124)을 포함한다. 그리고 본 실시예에 따른 유기발광 디스플레이 장치의 (부)화소는 스캔선(121), 이전 스캔선(122), 발광제어선(123) 및 초기화전압선(124)과 교차하며 (부)화소에 데이터신호(Dm) 및 구동전압(ELVDD)을 각각 인가하는 데이터선(171)과 구동전압선(172)을 포함할 수 있다.

<41> 또한, (부)화소는 구동 박막트랜지스터(T1), 스위칭 박막트랜지스터(T2), 보상 박막트랜지스터(T3), 초기화 박막트랜지스터(T4), 동작제어 박막트랜지스터(T5), 발광제어 박막트랜지스터(T6), 스토리지 캐패시터(Cst) 및 유기발광소자(미도시)를 포함할 수 있다.

<42> 구동 박막트랜지스터(T1), 스위칭 박막트랜지스터(T2), 보상 박막트랜지스터(T3), 초기화 박막트랜지스터(T4), 동작제어 박막트랜지스터(T5) 및 발광제어 박막트랜지스터(T6)는 도 3에 도시된 것과 같은 반도체층을 따라 형성되어 있는데, 반도체층은 다양한 형상으로 굴곡진 형상을 가질 수 있다. 반도체층은 구동 박막트랜지스터(T1)에 대응하는 구동 반도체층(131a), 스위칭 박막트랜지스터(T2)에 대응하는 스위칭 반도체층(131b), 보상 박막트랜지스터(T3)에 대응하는 보상 반도체층

(131c1, 131c2, 131c3), 초기화 박막트랜지스터(T4)에 대응하는 초기화 반도체층(131d1, 131d2, 131d3), 동작제어 박막트랜지스터(T5)에 대응하는 동작제어 반도체층(131e) 및 발광제어 박막트랜지스터(T6)에 대응하는 발광제어 반도체층(131f)을 포함할 수 있다. 즉, 구동 반도체층(131a), 스위칭 반도체층(131b), 보상 반도체층(131c1, 131c2, 131c3), 초기화 반도체층(131d1, 131d2, 131d3), 동작제어 반도체층(131e) 및 발광제어 반도체층(131f)은 도 3에 도시된 것과 같은 반도체층의 일부 영역들인 것으로 이해될 수 있다.

<43> 이러한 반도체층은 폴리실리콘을 포함할 수 있다. 그리고 반도체층은 예컨대 불순물이 도핑되지 않은 채널영역과, 채널영역의 양옆의 불순물이 도핑되어 형성된 소스영역과 드레인영역을 포함할 수 있다. 여기서, 불순물은 박막트랜지스터의 종류에 따라 달라지며, N형 불순물 또는 P형 불순물을 사용될 수 있다. 그리고 도핑되어 형성된 소스영역이나 드레인영역은 박막트랜지스터의 소스전극이나 드레인전극으로 해석될 수 있다. 즉, 예컨대 구동 소스전극(176a)은 도 3에 도시된 반도체층에 있어서 구동 반도체층(131a) 근방에서 불순물이 도핑된 구동 소스영역(176a)에 해당하고, 구동 드레인전극(177a)은 도 3에 도시된 반도체층에 있어서 구동 반도체층(131a) 근방에서 불순물이 도핑된 구동 드레인영역(177a)에 해당할 수 있다. 또한, 도 3에 도시된 반도체층에 있어서 박막트랜지스터들 사이에 대응하는 반도체층의 부분들도 불순물로 도핑되어, 박막트랜지스터들을 전기적으로 연결하는 역할을 하는 배선으로 해석될 수 있다.

<44> 한편, 스토리지 캐패시터(Cst)가 배치될 수 있다. 스토리지 캐패시터(Cst)는

제2절연층(142)을 사이에 두고 배치되는 제1스토리지 축전판(125a)과 제2스토리지 축전판(127)을 포함할 수 있다. 이때, 제1스토리지 축전판(125a)은 구동 박막트랜지스터(T1)의 구동 게이트전극의 역할도 동시에 할 수 있다. 즉, 구동 게이트전극과 제1스토리지 축전판(125a)은 일체(一體)인 것으로 이해될 수 있다. 이하에서는 구동 게이트전극을 언급할 시에 편의상 제1스토리지 축전판(125a)과 동일한 참조번호를 사용한다.

<45> 제1스토리지 축전판(125a)은 도 4에 도시된 것과 같이 인접한 (부)화소와 분리된 사각형 형상을 가질 수 있다. 이러한 제1스토리지 축전판(125a)은 도 4에 도시된 것과 같이 스캔선(121), 이전 스캔선(122) 및 발광제어선(123)과 동일층에 동일 물질로 형성될 수 있다.

<46> 참고로 스위칭 게이트전극(125b)과 보상 게이트전극(125c1, 125c2)은 반도체층과 교차하는 스캔선(121)의 부분들이거나 스캔선(121)으로부터 돌출된 부분들이고, 초기화 게이트전극(125d1, 125d2)은 반도체층과 교차하는 이전 스캔선(122)의 부분들이거나 이전 스캔선(122)으로부터 돌출된 부분들이며, 동작제어 게이트전극(125e)과 발광제어 게이트전극(125f)은 반도체층과 교차하는 발광제어선(123)의 부분들이거나 발광제어선(123)으로부터 돌출된 부분들이므로 이해될 수 있다.

<47> 제2스토리지 축전판(127)은 인접한 (부)화소들에 있어서 서로 연결되어 있을 수 있으며, 도 5에 도시된 것과 같이 초기화전압선(124)과 동일층에 동일 물질로 형성될 수 있다. 제2스토리지 축전판(127)에는 스토리지 개구부(27)가 형성될 수 있는데, 이를 통해 후술하는 것과 같은 연결부재(174)로 제1스토리지 축전판(125

a)과 보상 박막트랜지스터(T3)의 드레인전극(177c)이 전기적으로 연결되도록 할 수 있다. 제2스토리지 축전판(127)은 층간절연층(160)에 형성된 콘택홀(168)을 통해 구동전압선(172)에 연결될 수 있다.

<48> 구동 박막트랜지스터(T1)는 구동 반도체층(131a), 구동 게이트전극(125a), 구동 소스전극(176a) 및 구동 드레인전극(177a)을 포함한다. 구동 게이트전극(125a)은 전술한 것과 같이 제1스토리지 축전판(125a)의 역할을 겸할 수 있다. 구동 소스전극(176a)은 구동 게이트전극(125a) 외측(도 3 등에서는 -x 방향) 부분이 고, 구동 드레인전극(177a)은 구동 게이트전극(125a) 외측(도 3 등에서는 +x 방향) 부분으로서 구동 게이트전극(125a)을 중심으로 구동 소스전극(176a)의 반대쪽에 위치한다.

<49> 스위칭 박막트랜지스터(T2)는 스위칭 반도체층(131b), 스위칭 게이트전극(125b), 스위칭 소스전극(176b) 및 스위칭 드레인전극(177b)을 포함한다. 스위칭 소스전극(176b)은 제1절연층(141), 제2절연층(142) 및 층간절연층(160)에 형성된 콘택홀(164)을 통해 데이터선(171)과 전기적으로 연결될 수 있다. 이때, 필요에 따라 데이터선(171)의 콘택홀(164) 근방의 부분을 스위칭 박막트랜지스터(T2)의 소스전극으로 이해할 수도 있다. 스위칭 드레인전극(177b)은 스위칭 반도체층(131b) 근방에서 불순물이 도핑된 스위칭 드레인영역(177b)에 해당한다.

<50> 보상 박막트랜지스터(T3)는 보상 반도체층(131c1, 131c2, 131c3), 보상 게이트전극(125c1, 125c2), 보상 소스전극(176c) 및 보상 드레인전극(177c)을 포함한다. 보상 소스전극(176c)은 보상 반도체층(131c1, 131c2, 131c3) 근방에서

불순물이 도핑된 보상 소스영역(176c)에 해당하고, 보상 드레인전극(177c)은 보상 반도체층(131c1, 131c2, 131c3) 근방에서 불순물이 도핑된 보상 드레인영역(177c)에 해당한다. 보상 게이트전극(125c1, 125c2)은 제1게이트전극(125c1)과 제2게이트전극(125c2)을 포함하는 듀얼 게이트전극으로서, 누설 전류(leakage current)의 발생을 방지하거나 줄이는 역할을 할 수 있다. 보상 박막트랜지스터(T3)의 보상 드레인전극(177c)은 연결부재(174)를 통해 제1스토리지 축전판(125a)에 연결될 수 있다. 보상 반도체층(131c1, 131c2, 131c3)은 제1게이트전극(125c1)에 대응하는 부분(131c1), 제2게이트전극(125c2)에 대응하는 부분(131c3), 그리고 그 두 부분들(131c1, 131c3) 사이의 부분(131c2)을 포함할 수 있다.

<51> 연결부재(174)는 도 6에 도시된 것과 같이 데이터선(171) 등과 동일 물질로 동일층에 형성될 수 있다. 연결부재(174)의 일단은 제1절연층(141), 제2절연층(142) 및 층간절연층(160)에 형성된 컨택홀(166)을 통해 보상 드레인전극(177c) 및 초기화 드레인전극(177d)에 연결되며, 연결부재(174)의 타단은 제2절연층(142) 및 층간절연층(160)에 형성된 컨택홀(167)을 통해 제1스토리지 축전판(125a)에 연결된다. 이때, 연결부재(174)의 타단은 제2스토리지 축전판(127)에 형성된 스토리지 게구부(27)를 통해 제1스토리지 축전판(125a)에 연결된다.

<52> 초기화 박막트랜지스터(T4)는 초기화 반도체층(131d), 초기화 게이트전극(125d), 초기화 소스전극(176d) 및 초기화 드레인전극(177d)을 포함한다. 초기화 드레인전극(177d)은 초기화 반도체층(131d) 근방에서 불순물이 도핑된 초기화 드레인영역(177d)에 해당한다.

<53> 초기화 소스전극(176d)은 초기화연결선(78)을 통해 초기화전압선(124)과 연결되어 있다. 초기화연결선(78)의 일단은 제2절연층(142) 및 층간절연층(160)에 형성된 콘택홀(161)을 통해 초기화전압선(124)과 연결되고, 초기화연결선(78)의 타단은 제1절연층(141), 제2절연층(142) 및 층간절연층(160)에 형성된 콘택홀(162)을 통해 초기화 소스전극(176d)과 연결될 수 있다.

<54> 동작제어 박막트랜지스터(T5)는 동작제어 반도체층(131e), 동작제어 게이트전극(125e), 동작제어 소스전극(176e) 및 동작제어 드레인전극(177e)을 포함한다. 동작제어 소스전극(176e)은 제1절연층(141), 제2절연층(142) 및 층간절연층(160)에 형성된 콘택홀(165)을 통해 구동전압선(172)에 전기적으로 연결될 수 있다. 이때, 필요에 따라 구동전압선(172)의 콘택홀(165) 근방의 부분을 동작제어 박막트랜지스터(T5)의 소스전극으로 이해할 수도 있다. 동작제어 드레인전극(177e)은 동작제어 반도체층(131e) 근방에서 불순물이 도핑된 동작제어 드레인영역(177e)에 해당한다.

<55> 발광제어 박막트랜지스터(T6)는 발광제어 반도체층(131f), 발광제어 게이트전극(125f), 발광제어 소스전극(176f) 및 발광제어 드레인전극(177f)을 포함한다. 발광제어 소스전극(176f)은 발광제어 반도체층(131f) 근방에서 불순물이 도핑된 발광제어 소스영역(176f)에 해당한다. 발광제어 드레인전극(177f)은 도 6에 도시된 것과 같이 데이터선(171)이나 구동전압선(172) 등과 함께 층간절연층(160) 상에 형성된 부분으로 이해될 수 있다. 이 발광제어 드레인전극(177f)은 제1절연층(141), 제2절연층(142) 및 층간절연층(160)에 형성된 콘택홀(163)을 통해 하부의 반도체층에 연결될 수 있다. 또는, 하부의 반도체층의 일부분이 발광제어 드레인전극이고,

참조번호 177f는 발광제어 드레인전극과 유기발광소자(OLED)의 화소전극을 연결하기 위한 중간연결층인 것으로 이해될 수도 있다.

<56> 구동 박막트랜지스터(T1)의 구동 반도체층(131a)의 일단은 스위칭 반도체층(131b) 및 보상 반도체층(131c1, 131c2, 131c3)에 연결되어 있으며, 구동 반도체층(131a)의 타단은 동작제어 반도체층(131e) 및 발광제어 반도체층(131f)에 연결되어 있다. 따라서, 구동 소스전극(176a)은 스위칭 드레인전극(177b) 및 동작제어 드레인전극(177e)에 연결되고, 구동 드레인전극(177a)은 보상 소스전극(176c) 및 발광제어 소스전극(176f)에 연결된다.

<57> 한편, 스위칭 박막트랜지스터(T2)는 발광시키하고자 하는 (부)화소를 선택하는 스위칭 소자로 사용된다. 스위칭 게이트전극(125b)은 스캔선(121)에 연결되어 있고, 스위칭 소스전극(176b)은 데이터선(171)에 연결되어 있으며, 스위칭 드레인전극(177b)은 구동 박막트랜지스터(T1) 및 동작제어 박막트랜지스터(T5)에 연결되어 있다.

<58> 그리고, 발광제어 박막트랜지스터(T6)의 발광제어 드레인전극(177f)은 도 6에 도시된 것과 같이 동일층에 형성된 데이터선(171)이나 구동전압선(172) 등을 덮는 보호막 또는 평탄화막(미도시)에 형성된 콘택홀(181)을 통해 유기발광소자(OLED)의 화소전극에 연결된다.

<59> 도 7은 도 2의 VII-VII선을 따라 취한 단면도이다. 도 7에 도시된 것과 같이, 지금까지 설명한 다양한 구성요소들은 기판(110) 상에 위치할 수 있다. 기판(110)은 글라스재, 금속재 또는 플라스틱재 등과 같은 다양한 재료로 형성된 것일

수 있다. 이러한 기판(110)에는 필요에 따라 버퍼층(111)이 위치할 수 있다. 버퍼층(111)은 기판(110)의 면을 평탄화하거나, 그 상부의 반도체층으로 불순물 등이 침투하는 것을 방지하는 역할을 할 수 있다. 그러한 버퍼층(111)은 실리콘옥사이드, 실리콘나이트라이드 또는 실리콘옥시나이트라이드 등으로 형성된 단일층/다층 구조를 가질 수 있다.

<60> 버퍼층(111) 상에는 도 3에 도시된 것과 같은 구동 반도체층(131a), 스위칭 반도체층(131b), 보상 반도체층(131c1, 131c2, 131c3) 등이 위치할 수 있다. 이러한 구동 반도체층(131a), 스위칭 반도체층(131b), 보상 반도체층(131c1, 131c2, 131c3) 등의 상부에는 실리콘나이트라이드, 실리콘옥사이드 또는 실리콘옥시나이트라이드 등으로 형성된 제1절연층(141)이 위치할 수 있다.

<61> 제1절연층(141) 상에는 도 4에 도시된 것과 같은 구동 게이트전극(125a)과, 스위칭 게이트전극(125b)과 보상 게이트전극(125c)을 포함하는 스캔선(121)과, 초기화 게이트전극(125d)을 포함하는 이전 스캔선(122), 동작제어 게이트전극(125e) 및 발광제어 게이트전극(125f)을 포함하는 발광제어선(123)을 포함하는 배선이 위치할 수 있다. 이러한 구동 게이트전극(125a), 스캔선(121), 이전 스캔선(122) 및 발광제어선(123)을 통칭하여 제1게이트배선이라고 할 수 있다.

<62> 제2절연층(142)은 제1게이트배선을 덮을 수 있다. 이러한 제2절연층(142)은 실리콘나이트라이드, 실리콘옥사이드 또는 실리콘옥시나이트라이드 등으로 형성될 수 있다. 이러한 제2절연층(142) 상에는 도 5에 도시된 것과 같은 제2스토리지 축전판(127) 및 초기화전압선(124)이 위치할 수 있다. 제2스토리지 축전판(127)과 초

기화전압선(124)을 통칭하여 제2게이트배선이라 할 수 있다.

<63> 제2게이트배선 상에는 층간절연층(160)이 위치한다. 층간절연층(160)은 실리콘나이트라이드, 실리콘옥사이드 또는 실리콘옥시나이트라이드 등으로 형성될 수 있다.

<64> 층간절연층(160) 상에는 도 6에 도시된 것과 같은 데이터선(171), 구동전압선(172), 연결부재(174), 초기화연결선(78) 및 발광제어 드레인전극(177f)이 배치될 수 있다. 데이터선(171), 구동전압선(172), 연결부재(174), 초기화연결선(78), 발광제어 드레인전극(177f)을 통칭하여 데이터배선이라 할 수 있다. 이러한 데이터선(171), 구동전압선(172), 연결부재(174), 초기화연결선(78), 발광제어 드레인전극(177f) 등은 전술한 것과 같이 제1절연층(141), 제2절연층(142) 및 층간절연층(160)의 적어도 일부에 형성된 컨택홀들(161, 162, 163, 164, 165, 166, 167, 168)을 통해 하부의 반도체층이나 전극 등에 전기적으로 연결될 수 있다.

<65> 데이터배선 상에는 보호막 또는 평탄화막(미도시) 등이 배치되고, 이 보호막 또는 평탄화막 상에 유기발광소자의 화소전극(미도시)이 위치할 수 있다. 이 화소전극은 보호막 또는 평탄화막에 형성된 컨택홀(181)을 통해 발광제어 드레인전극(177f)에 연결될 수 있다.

<66> 한편, 제2스토리지 축전판(127)은 도 2, 도 5 및 도 7에 도시된 것과 같이 일측에 제1실드층(SD1)을 가질 수 있다. 이 제1실드층(SD1)은 도 2 및 도 5에 도시된 것과 같이 제2스토리지 축전판(127)으로부터 돌출 부분일 수 있다. 이 제1실드층(SD1)은 제2스토리지 축전판(127)의, 보상 박막트랜지스터(T3)의 제1게이트전극

(125c1)과 제2게이트전극(125c2) 사이의 부분의 적어도 일부와 데이터선(171) 사이로 연장된 부분으로 이해될 수 있다.

<67> 참고로 도 2에 도시된 것과 같은 배치도는 일 (부)화소의 배치도로서 그 상하좌우로 동일/유사한 구성이 배치될 수 있으며, 도 7에서는 도 2에 대응하는 부분을 (부)화소(P1)로 표시하고, 도 2에 도시되지 않았으나 (+x 방향으로의) 그 옆에 위치한 (부)화소(P2)의 일부를 함께 도시하였다. (부)화소(P2) 역시 데이터선(171)을 가질 수 있으며, 이에 따라 (부)화소(P1)의 제1실드층(SD1)은 제2스토리지 축전판(127)의, 보상 박막트랜지스터(T3)의 제1게이트전극(125c1)과 제2게이트전극(125c2) 사이의 부분의 적어도 일부와 (부)화소(P2)의 데이터선(171) 사이로 연장된 부분으로 이해될 수 있다.

<68> 만일 제1실드층(SD1)이 존재하지 않는다면 보상 박막트랜지스터(T3)의 제1게이트전극(125c1)과 제2게이트전극(125c2) 사이의 부분, 구체적으로 보상 반도체층의 부분(131c2)은 데이터선(171)에 의해 영향을 받게 된다.

<69> 데이터선(171)은 (부)화소(P1)의 +x 방향 근방에 위치한 (부)화소(P2)에 데이터신호를 전달하는 것 외에, (부)화소(P2)의 +y 방향과 -y 방향에 위치한 복수개의 (부)화소들에도 데이터신호를 전달한다. 이때 전달하는 데이터신호는 (부)화소(P2)의 +y 방향과 -y 방향에 위치한 복수개의 (부)화소들에서 구현될 휘도에 따라 모두 달라질 수 있으며, 이에 따라 (부)화소(P1)가 발광하고 있는 동안 시간의 흐름에 따라 (부)화소(P1)의 보상 반도체층의 부분(131c2) 근방의 데이터선(171)은 상이한 전기적 신호를 전달하게 된다.

<70> 만일 제1실드층(SD1)이 존재하지 않는다면 (부)화소(P1)의 보상 박막트랜지스터(T3)의 부분(131c2)과 (부)화소(P2)의 데이터선(171) 사이에는 기생 커패시턴스가 존재하게 되며, 이에 따라 (부)화소(P1)가 발광하고 있는 동안 시간의 흐름에 따라 (부)화소(P1)의 보상 박막트랜지스터(T3)의 부분(131c2)의 전위가 (부)화소(P2)의 데이터선(171)이 전달하는 상이한 전기적 신호들에 의해 영향을 받게 된다. 보상 박막트랜지스터(T3)는 구동 박막트랜지스터(T1)와 전기적으로 연결되는바, (부)화소(P1)의 보상 박막트랜지스터(T3)의 부분(131c2)의 전위가 (부)화소(P2)의 데이터선(171)이 전달하는 상이한 전기적 신호들에 의해 영향을 받게 되면 결국 구동 박막트랜지스터(T1)에 의해 휘도가 결정되는 유기발광소자(OLED)의 휘도가 최초 의도한 것과 다르게 달라질 수 있으며, 이는 결국 유기발광 디스플레이 장치가 디스플레이하는 이미지의 품질 저하를 야기하게 된다.

<71> 그러나 본 실시예에 따른 유기발광 디스플레이 장치의 경우 제1실드층(SD1)이 (부)화소(P1)의 보상 박막트랜지스터(T3)의 부분(131c2)과 (부)화소(P2)의 데이터선(171) 사이에 존재하는바, 따라서 (부)화소(P1)의 보상 박막트랜지스터(T3)의 부분(131c2)이 (부)화소(P2)의 데이터선(171)에 의해 영향을 받는 것을 방지하거나 최소화함으로써, 고품질의 유기발광 디스플레이 장치가 정확한 휘도의 고품질의 이미지를 디스플레이하도록 할 수 있다. 특히 제1실드층(SD1)이 제2스토리지 축전판(127)의 일부분일 경우, 제2스토리지 축전판(127)이 컨택홀(168)을 통해 언제나 일정한 전위의 구동전압선(172)에 연결되어 있으므로 제1실드층(SD1) 역시 언제나 일정한 전위를 갖게 된다. 그 결과 보상 박막트랜지스터(T3)의 부분(131c2)이 주위의

다른 전기적 신호에 의해 영향을 받는 것을 최소화할 수 있다.

<72> 물론 제1실드층(SD1)은 도 7에 도시된 것에 그치지 않고, 본 발명의 다른 일 실시예에 따른 유기발광 디스플레이 장치의 단면도인 도 8에 도시된 것과 같이 (부)화소(P2)의 데이터선(171) 하부까지 제1실드층(SD1)이 연장되도록 할 수도 있다. 이를 통해 보상 박막트랜지스터(T3)의 부분(131c2)의 실드가 더욱 확실하게 이루어지도록 할 수 있다. 물론 제1실드층(SD1)이 보상 박막트랜지스터(T3)의 제1게이트전극(125c1)과 제2게이트전극(125c2) 사이의 부분(131c2)의 적어도 일부 상부로 연장되도록 하는 것만으로도 큰 효과를 볼 수 있다.

<73> 도 9는 도 2의 IX-IX선을 따라 취한 단면도이다. 도 2, 도 5 및 도 9에 도시된 것과 같이, 초기화전압선(124)은 제2실드층(SD2)을 가질 수 있다.

<74> 이 제2실드층(SD2)은 도 2 및 도 5에 도시된 것과 같이 x축을 따라 연장된 초기화전압선(124)의 일부분일 수 있다. 이 제2실드층(SD2)은 초기화전압선(124)의, 초기화 박막트랜지스터(T4)의 제1게이트전극(125d1)과 제2게이트전극(125d2) 사이의 부분의 적어도 일부와 데이터선(171) 사이로 연장된 부분으로 이해될 수 있다.

<75> 도 2 및 도 5 등에서는 초기화전압선(124)이 마침 초기화 박막트랜지스터(T4)의 제1게이트전극(125d1)과 제2게이트전극(125d2) 사이의 부분의 상부를 지나도록 연장된 것으로 도시되어 있으나, 본 발명이 이에 한정되는 것은 아니다. 만일 초기화전압선(124)의 위치가 이와 달리 +y 방향이나 -y 방향 또는 그 외의 방향으로 이동되거나 절곡되는 등의 다른 형상을 가질 경우, 초기화전압선(124)은 돌출부

를 갖고 이 돌출부가 초기화 박막트랜지스터(T4)의 제1게이트전극(125d1)과 제2게이트전극(125d2) 사이의 부분의 적어도 일부와 데이터선(171) 사이로 연장되도록 하여 제2실드층(SD2)의 역할을 하도록 할 수 있다. 즉, 도 2 및 도 5 등에서는, 초기화전압선(124)이 x축 방향을 따라 연장되며 초기화 박막트랜지스터(T4)의 제1게이트전극(125d1)과 제2게이트전극(125d2) 사이의 부분의 적어도 일부와 데이터선(171) 사이를 지나도록 하여, 초기화전압선(124)이 그러한 돌출부를 갖지 않아도 되도록 초기화전압선(124)의 위치가 특정된 것으로 이해될 수 있다.

<76> 만일 제2실드층(SD2)이 존재하지 않는다면 초기화 박막트랜지스터(T4)의 제1게이트전극(125d1)과 제2게이트전극(125d2) 사이의 부분, 구체적으로 초기화 반도체층의 부분(131d2)은 데이터선(171)에 의해 영향을 받게 된다.

<77> 데이터선(171)은 도 2에 도시된 (부)화소에 데이터신호를 전달하는 것 외에, 그 (부)화소의 +y 방향과 -y 방향에 위치한 복수개의 (부)화소들에도 데이터신호를 전달한다. 이때 전달하는 데이터신호는 도 2에 도시된 (부)화소의 +y 방향과 -y 방향에 위치한 복수개의 (부)화소들에서 구현될 휘도에 따라 모두 달라질 수 있으며, 이에 따라 도 2에 도시된 (부)화소가 발광하는 동안, 시간의 흐름에 따라 도 2에 도시된 (부)화소의 초기화 반도체층의 부분(131d2) 근방의 데이터선(171)은 상이한 전기적 신호를 전달하게 된다.

<78> 만일 제2실드층(SD2)이 존재하지 않는다면 초기화 박막트랜지스터(T4)의 부분(131d2)과 데이터선(171) 사이에는 기생 커패시턴스가 존재하게 되며, 이에 따라 도 2에 도시된 (부)화소가 발광하는 동안 시간의 흐름에 따라 초기화 박막트랜지스

터(T4)의 부분(131d2)의 전위가 데이터선(171)이 전달하는 상이한 전기적 신호들에 의해 영향을 받게 된다. 초기화 박막트랜지스터(T4)는 구동 박막트랜지스터(T1)와 전기적으로 연결되는바, 초기화 박막트랜지스터(T4)의 부분(131d2)의 전위가 데이터선(171)이 전달하는 상이한 전기적 신호들에 의해 영향을 받게 되면 결국 구동 박막트랜지스터(T1)에 의해 휘도가 결정되는 유기발광소자(OLED)의 휘도가 최초 의도한 것과 다르게 달라질 수 있으며, 이는 결국 유기발광 디스플레이 장치가 디스플레이하는 이미지의 품질 저하를 야기하게 된다.

<79> 그러나 본 실시예에 따른 유기발광 디스플레이 장치의 경우 제2실드층(SD2)이 초기화 박막트랜지스터(T4)의 부분(131d2)과 데이터선(171) 사이에 존재하는바, 따라서 초기화 박막트랜지스터(T4)의 부분(131d2)이 데이터선(171)에 의해 영향을 받는 것을 방지하거나 최소화함으로써, 고품질의 유기발광 디스플레이 장치가 정확한 휘도의 고품질의 이미지를 디스플레이하도록 할 수 있다. 특히 제2실드층(SD2)이 초기화전압선(124)의 일부분일 경우, 언제나 일정한 전위의 초기화전압선(124)에 의해 제2실드층(SD2) 역시 언제나 일정한 전위를 갖게 된다. 그 결과 초기화 박막트랜지스터(T4)의 부분(131d2)이 주위의 다른 전기적 신호에 의해 영향을 받는 것을 최소화할 수 있다.

<80> 물론 각종 배선이나 반도체층 등의 레이아웃이 도 2 등에 도시된 것과 달라질 경우, 제2실드층(SD2)은 초기화 박막트랜지스터(T4)의 제1게이트전극(125d1)과 제2게이트전극(125d2) 사이의 부분(131d2)의 적어도 일부 상부로 연장된 부분이거나, 데이터선(171) 하부로 연장된 부분일 수 있다.

<81> 도 10은 도 2의 X-X선을 따라 취한 단면도이다. 도 2, 도 5 및 도 10에 도시된 것과 같이, 제2스토리지 축전판(127)은 제3실드층(SD3)을 가질 수 있다.

<82> 제3실드층(SD3)은 도 2 및 도 5에 도시된 것과 같이 제2스토리지 축전판(127)의 일부분일 수 있다. 이 제3실드층(SD3)은 제2스토리지 축전판(127)의, 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)과 데이터선(171) 사이로 연장된 부분으로 이해될 수 있다. 예컨대 제2스토리지 축전판(127) 자체는 그 -x 방향의 (가상의) 끝단이 하부의 제1스토리지 축전판(125a)의 -x 방향 끝단과 대략 일치하고, 그 (가상의) 끝단에서 -x 방향으로의 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)과 데이터선(171) 사이에 개재되는 제3실드층(SD3)이 존재하며, 그러한 제3실드층(SD3)이 제2스토리지 축전판(127)과 일체(一體)인 것으로 이해될 수도 있다.

<83> 도 2 및 도 5 등에 도시된 것과 달리 제3실드층(SD3)이 존재하지 않아 제2스토리지 축전판(127)이 데이터선(171)이 위치한 -x 방향으로 연장되지 않고, 제2스토리지 축전판(127)의 -x 방향의 끝단이 제1스토리지 축전판(125a)의 -x 방향 끝단과 대략 일치하게 하는 것을 고려할 수도 있다. 그러한 경우 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)은 데이터선(171)에 의해 영향을 받게 된다.

<84> 데이터선(171)은 도 2에 도시된 (부)화소에 데이터신호를 전달하는 것 외에, 그 (부)화소의 +y 방향과 -y 방향에 위치한 복수개의 (부)화소들에도 데이터신호를 전달한다. 이때 전달하는 데이터신호는 도 2에 도시된 (부)화소의 +y 방향과 -y 방향에 위치한 복수개의 (부)화소들에서 구현될 휘도에 따라 모두 달라질 수 있으며, 이에 따라 도 2에 도시된 (부)화소가 발광하는 동안 시간의 흐름에 따라 도 2에 도

시된 (부)화소의 초기화 반도체층의 부분(131d2) 근방의 데이터선(171)은 상이한 전기적 신호를 전달하게 된다.

<85> 만일 제3실드층(SD3)이 존재하지 않아 제2스토리지 축전판(127)이 데이터선(171)이 위치한 -x 방향으로 연장되지 않고 제2스토리지 축전판(127)의 -x 방향의 끝단이 제1스토리지 축전판(125a)의 -x 방향 끝단과 대략 일치하게 되면, 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)과 데이터선(171) 사이에는 기생 커패시턴스가 존재하게 되며, 이에 따라 도 2에 도시된 (부)화소가 발광하는 동안 시간의 흐름에 따라 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)의 전위가 데이터선(171)이 전달하는 상이한 전기적 신호들에 의해 영향을 받게 된다. 이는 결국 구동 박막트랜지스터(T1)에 의해 휘도가 결정되는 유기발광소자(OLED)의 휘도가 최초 의도한 것과 다르게 달라질 수 있으며, 이에 따라 유기발광 디스플레이 장치가 디스플레이하는 이미지의 품질 저하가 야기될 수 있다.

<86> 그러나 본 실시예에 따른 유기발광 디스플레이 장치의 경우 제3실드층(SD3)이 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)과 데이터선(171) 사이에 존재하는바, 따라서 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)이 데이터선(171)에 의해 영향을 받는 것을 방지하거나 최소화함으로써, 고품질의 유기발광 디스플레이 장치가 정확한 휘도의 고품질의 이미지를 디스플레이하도록 할 수 있다. 특히 제3실드층(SD3)이 제2스토리지 축전판(127)의 일부분일 경우, 제2스토리지 축전판(127)이 컨택홀(168)을 통해 언제나 일정한 전위의 구동전압선(172)에 연결되어 있으므로 제3실드층(SD3) 역시 언제나 일정한 전위를 갖게 된다. 그 결과 구동

박막트랜지스터(T1)의 구동 게이트전극(125a)이 주위의 다른 전기적 신호에 의해 영향을 받는 것을 최소화할 수 있다.

<87> 물론 제3실드층(SD3)은 구동 게이트전극(125a)과 데이터선(171) 사이에 개재되는 것에 그치지 않고, 도 10에 도시된 것과 같이 데이터선(171) 하부까지 제3실드층(SD3)이 연장되도록 할 수도 있다. 이를 통해 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)의 실드가 더욱 확실하게 이루어지도록 할 수 있다.

<88> 지금까지 유기발광 디스플레이 장치가 제1실드층(SD1), 제2실드층(SD2) 및 제3실드층(SD3)을 모두 갖는 경우에 대해 설명하였다. 그러나 본 발명이 이에 한정되는 것은 아니며, 유기발광 디스플레이 장치는 제1실드층(SD1), 제2실드층(SD2) 및 제3실드층(SD3) 중 일부만 가질 수도 있다. 즉, 제1실드층(SD1), 제2실드층(SD2) 및 제3실드층(SD3) 중 적어도 어느 하나를 구비하는 유기발광 디스플레이 장치라면 본 발명의 범위에 속한다고 할 것이다.

<89> 상술한 실시예에 있어서, 보상 박막트랜지스터(T3)와 초기화 박막트랜지스터(T4)가 듀얼 게이트전극을 갖는 경우에 대해 설명하였다. 그러나 본 발명이 이에 한정되는 것은 아니며, 보상 박막트랜지스터(T3)와 초기화 박막트랜지스터(T4)가 싱글 게이트전극을 갖는 경우라 하더라도, 보상 박막트랜지스터(T3) 및/또는 초기화 박막트랜지스터(T4)의 일부분과 데이터선(171) 사이에 개재되는 제1실드층(SD1)이나 제2실드층(SD2)을 가질 수도 있음은 물론이다.

<90> 한편, 지금까지는 제1실드층(SD1), 제2실드층(SD2) 및 제3실드층(SD3) 모두가 도 2 및 도 5에 도시된 것과 같이 제2게이트배선에 포함되는 것으로 설명하였으

나, 본 발명이 이에 한정되는 것은 아니다. 즉, 제1실드층(SD1), 제2실드층(SD2) 및 제3실드층(SD3)은 도 2 및 도 5에 도시된 것과 같이 제2스토리지 축전판(127)의 일부이거나 초기화전압선(124)의 일부일 수도 있으나, 본 발명이 이에 한정되는 것은 아니다.

<91> 도 11은 본 발명의 또 다른 일 실시예에 따른 유기발광 디스플레이 장치의 일 (부)화소에 있어서의 복수개의 박막트랜지스터들 및 캐패시터 등의 위치를 개략적으로 도시하는 배치도이고, 도 12는 도 11의 XII-XII선을 따라 취한 단면도이다. 도 2 등을 전술하여 설명한 유기발광 디스플레이 장치와 동일/유사한 부분의 설명은 생략하고 상이한 부분만 설명하면, 이전 스캔선(122), 초기화전압선(124, 도 11 및 도 12에서는 미도시) 및 초기화 박막트랜지스터(T4)의 형상이 상이하다.

<92> 도 11 및 도 12를 참조하면, 초기화전압선(미도시)은 제2스토리지 축전판(127)과 동일층에 위치할 수도 있고, 이와 달리 화소전극(미도시)과 동일층에 위치할 수도 있다. 어떤 경우이든 초기화전압선은 콘택홀(162)을 통해 초기화 박막트랜지스터(T4)의 소스전극(176d)에 연결될 수 있다. 초기화 박막트랜지스터(T4)의 드레인전극(177d)은 도 2 등을 참조하여 전술한 것과 같이 보상 박막트랜지스터(T3)의 보상 드레인전극(177c) 및 구동 박막트랜지스터(T1)의 구동 게이트전극(125a)에 전기적으로 연결된다.

<93> 구동 게이트전극(125a), 스캔선(121) 및 발광제어선(123)과 동일층에 위치할 수 있는 이전 스캔선(122)은 초기화 박막트랜지스터(T4)의 위치에 대응하는 두 개의 돌출부들을 가질 수 있는데, 이 두 개의 돌출부들은 초기화 박막트랜지스터(T

4)의 제1게이트전극(125d1)과 제2게이트전극(125d2)일 수 있다. 이 중 제2게이트전극(125d2)의 적어도 일부는 제2실드층(SD2)인 것으로 이해될 수 있다.

<94> 듀얼 게이트전극은 반도체층과 중첩되는 2개의 부분들을 가지면 된다. 예컨대 도 11에 도시된 것과 같은 배치도의 경우, 초기화 박막트랜지스터(T4)의 제2게이트전극(125d2)은 이전 스캔선(122)으로부터 돌출될 필요 없이, x축을 따라 연장된 이전 스캔선(122)의 부분으로서, 제1게이트전극(125d1)의 -x 방향 위치에서 초기화 소스전극(176d) 근방에서 반도체층과 교차하는 부분(125d2')이, 제2게이트전극의 역할을 하도록 할 수도 있다. 그러나 이 경우 참조번호 125d2'에 대응하는 반도체층의 부분과 제1게이트전극(125d1)에 대응하는 반도체층의 부분 사이의 부분이 데이터선(171)에 인접하여 위치하며 실드되지 않기에, 그 부분이 데이터선(171)에 의해 영향을 받게 된다.

<95> 그러나 본 실시예에 따른 유기발광 디스플레이 장치의 경우 이전 스캔선(122)이 2개의 돌출부들을 가지며 그 중 하나의 돌출부는 제1게이트전극(125d1)의 역할을 하고 다른 하나의 돌출부는 이전 스캔선(122)의 참조번호 125d2'에 해당하는 위치로부터 돌출되어 제2게이트전극(125d2)의 역할을 한다. 이때 돌출된 제2게이트전극(125d2)은 참조번호 125d2'에 대응하는 반도체층의 부분과 제1게이트전극(125d1)에 대응하는 반도체층의 부분 사이의 부분을 데이터선(171)으로부터 실드하여, 초기화 박막트랜지스터(T4)가 데이터선(171)으로부터 의도되지 않은 영향을 받는 것을 효과적으로 방지하거나 줄일 수 있다.

<96> 이러한 초기화 박막트랜지스터(T4)의 구조는 결과적으로, 초기화 박막트랜지

스터(T4)가 제1게이트전극(125d1)과 제2게이트전극(125d2)을 가지며, 초기화 박막 트랜지스터(T4)의 제1게이트전극(125d1)과 제2게이트전극(125d2) 사이의 부분인 반도체층(131d2)과 데이터선(171) 사이에 제1게이트전극(125d1)과 제2게이트전극(125d2) 중 어느 하나가 적어도 부분적으로 위치하는 것으로 이해될 수 있다. 도 11 및 도 12에서는 초기화 박막트랜지스터(T4)의 제1게이트전극(125d1)과 제2게이트전극(125d2) 사이의 부분인 반도체층(131d2)과 데이터선(171) 사이에 제2게이트전극(125d2)이 적어도 부분적으로 위치하여, 반도체층(131d2)을 데이터선(171)으로부터 실드하는 것으로 도시하고 있다. 즉, 제2게이트전극(125d2)이 제2실드층(SD2)인 것으로 도시하고 있다. 물론 도 11 및 도 12에 도시된 것과 같이 제2게이트전극(125d2)이 반도체층(131d2)과 데이터선(171) 사이에 개재되는 것에 그치지 않고, 제2게이트전극(125d2)이 데이터선(171)의 하부까지 (-x 방향으로) 연장되도록 할 수도 있음은 물론이다. 도 12에서는 데이터선(171)이 제2게이트전극(125d2)의 상부에 위치하는 것으로 도시하고 있으나, 만일 데이터선(171)이 반도체층(131d2)의 하부에 위치하고 제2게이트전극(125d2)이 데이터선(171)과 반도체층(131d2) 사이에 위치한다면, 제2게이트전극(125d2)은 물론 데이터선(171)의 상부까지 연장될 수 있다.

<97> 이처럼, 제2실드층(SD2)은 도 2, 도 5 및 도 9를 참조하여 전술한 것과 같이 제2게이트배선으로 형성될 수도 있지만, 도 11 및 도 12를 참조하여 설명한 것과 같이 제1게이트배선으로 형성될 수도 있다. 제2실드층(SD2) 외의 제1실드층(SD1)이나 제3실드층(SD3) 역시 필요하다면 제1게이트배선으로 형성될 수도 있다. 이 경우

제1실드층(SD1)이나 제3실드층(SD3)은 제2스토리지 축전판(127)과 전기적으로 연결되지 않고 아일랜드 형상으로서 전기적으로 플로팅된 것일 수도 있다.

<98> 지금까지 구동 박막트랜지스터(T1), 보상 박막트랜지스터(T3) 및 초기화 박막트랜지스터(T4) 등의 일부분을 데이터선(171)으로부터 실드하는 것으로 설명하였으나, 본 발명이 이에 한정되는 것은 아니다. 즉, 유기발광 디스플레이 장치가 구비하는 (부)화소의 박막트랜지스터가 데이터선(171) 근방에 위치할 경우, 그러한 박막트랜지스터의 적어도 일부분과 데이터선(171) 사이에 실드층이 위치하도록 함으로써, 고품질의 이미지를 디스플레이하는 유기발광 디스플레이 장치를 구현할 수 있다. 그러한 실드층은 예컨대 박막트랜지스터의 소스전극과 데이터선 사이와, 드레인전극과 데이터선 사이와, 게이트전극과 데이터선 사이 중 적어도 어느 한 곳에 위치할 수 있다.

<99> 한편, 지금까지는 박막트랜지스터의 일부분과 데이터선 사이에 실드층이 위치하도록 하는 것으로 설명하였으나, 본 발명이 이에 한정되는 것은 아니다. 예컨대 소스전극과 드레인전극과 게이트전극을 포함하는 박막트랜지스터와, 상기 소스전극과 상기 드레인전극과 상기 게이트전극과 상이한 층에 위치하며 제어신호를 전달하는 제어신호선과, 상기 박막트랜지스터의 적어도 일부분과 상기 제어신호선 사이에 위치하는 실드층을 구비하는, 유기발광 디스플레이 장치 역시 본 발명의 범위에 속한다. 여기서 제어신호선은 전술한 복수개의 신호선들(121, 122, 123, 124, 171, 172) 중 적어도 어느 하나가 될 수 있다. 즉, 제어신호선은 스캔선(121), 이 전 스캔선(122), 발광제어선(123), 데이터선(171), 구동전압선(172) 또는 초기화전

압선(124)일 수 있다. 실드층은 박막트랜지스터의 적어도 일부분을 이러한 제어 신호선으로부터 차폐하여, 박막트랜지스터가 제어 신호선이 전달하는 제어 신호에 의해 영향을 받는 것을 방지하거나 최소화할 수 있다.

<100> 물론 본 발명이 유기발광 디스플레이 장치에 국한되는 것은 아니다. 유기발광 디스플레이 장치가 아니더라도 (부)화소에 박막트랜지스터를 가지며 데이터선을 갖는 디스플레이 장치라면, 상술한 것과 동일/유사하게 실드층을 가짐으로써 고품질의 이미지를 디스플레이할 수 있도록 고려할 수 있다.

<101> 이와 같이 본 발명은 도면에 도시된 실시예를 참고로 설명되었으나 이는 예시적인 것에 불과하며, 당해 기술분야에서 통상의 지식을 가진 자라면 이로부터 다양한 변형 및 균등한 다른 실시예가 가능하다는 점을 이해할 것이다. 따라서 본 발명의 진정한 기술적 보호 범위는 첨부된 특허청구범위의 기술적 사상에 의하여 정해져야 할 것이다.

【부호의 설명】

<102>	T1: 구동 박막트랜지스터	T2: 스위칭 박막트랜지스터
	T3: 보상 박막트랜지스터	T4: 초기화 박막트랜지스터
	T5: 구동제어 박막트랜지스터	T6: 발광제어 박막트랜지스터
	Cst: 스토리지 캐패시터	S1S6: 소스전극
	DID6: 드레인전극	G1G6: 게이트전극
	125a, 125b, 125c, 125d, 125e, 125f: 게이트전극	

131a, 131b, 131c, 131d, 131e, 131f: 반도체층

176a, 176b, 176c, 176d, 176e, 176f: 소스전극

177a, 177b, 177c, 177d, 177e, 177f: 드레인전극

Cst1, 125a: 제1스토리지 축전판 Cst2, 127: 제2스토리지 축전판

27: 스토리지 개구부

121: 스캔선

122: 이전 스캔선

123: 발광제어선

124: 초기화전압선

171: 데이터선

172: 구동전압선

78: 초기화연결선

174: 연결부재

SD1: 제1실드층

SD2: 제2실드층

SD3: 제3실드층

110: 기판

111: 버퍼층

141: 제1절연층

142: 제2절연층

160: 층간절연층

161-168, 181: 콘택홀

【특허청구범위】

【청구항 1】

소스전극, 드레인전극 및 게이트전극을 포함하는 박막트랜지스터;

상기 소스전극, 상기 드레인전극 및 상기 게이트전극과 상이한 층에 위치하며, 데이터신호를 전달하는, 데이터선; 및

상기 박막트랜지스터의 적어도 일부분과 상기 데이터선 사이에 위치하는 실드층;

을 구비하는, 디스플레이 장치.

【청구항 2】

제1항에 있어서,

상기 실드층은 상기 소스전극과 상기 데이터선 사이와, 상기 드레인전극과 상기 데이터선 사이와, 상기 게이트전극과 상기 데이터선 사이 중 적어도 어느 한 곳에 위치하는, 디스플레이 장치.

【청구항 3】

제1항에 있어서,

제1스토리지 축전판과, 상기 제1스토리지 축전판과 중첩되며 상기 제1스토리지 축전판 상부에 위치한 제2스토리지 축전판을 포함하는 스토리지 캐패시터를 더 구비하고,

상기 데이터선은 상기 제2스토리지 축전판보다 상부층에 위치하며,

상기 실드층은 상기 제2스토리지 축전판의 일부분으로서, 상기 게이트전극과 상기 데이터선 사이로 연장된 부분 또는 상기 데이터선 하부로 연장된 부분인, 디스플레이 장치.

【청구항 4】

제3항에 있어서,

상기 제1스토리지 축전판은 상기 게이트전극과 전기적으로 연결된, 디스플레이 장치.

【청구항 5】

제4항에 있어서,

상기 제1스토리지 축전판과 상기 게이트전극은 일체(一體)인, 디스플레이 장치.

【청구항 6】

제1항에 있어서,

상기 게이트전극은 제1게이트전극과 제2게이트전극을 포함하고,

상기 실드층은 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부와 상기 데이터선 사이에 위치하는, 디스플레이 장치.

【청구항 7】

제6항에 있어서,

제1스토리지 축전판과, 상기 제1스토리지 축전판과 중첩되며 상기 제1스토리지 축전판 상부에 위치한 제2스토리지 축전판을 포함하는 스토리지 캐패시터를 더 구비하고,

상기 데이터선은 상기 제2스토리지 축전판보다 상부층에 위치하며,

상기 실드층은 상기 제2스토리지 축전판의 일부분으로서, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부와 상기 데이터선 사이로 연장된 부분, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부 상부로 연장된 부분 또는 상기 데이터선 하부로 연장된 부분인, 디스플레이 장치.

【청구항 8】

제7항에 있어서,

상기 제1스토리지 축전판과 전기적으로 연결된 구동 게이트전극과, 상기 소스전극과 전기적으로 연결된 구동 드레인전극을 포함하는 구동 박막트랜지스터를 더 구비하고,

상기 제1스토리지 축전판은 상기 드레인전극과 전기적으로 연결된, 디스플레이 장치.

【청구항 9】

제6항에 있어서,

제1스토리지 축전판과, 상기 제1스토리지 축전판과 중첩되며 상기 제1스토리

지 축전판 상부에 위치한 제2스토리지 축전판을 포함하는 스토리지 캐패시터; 및

구동 박막트랜지스터의 상기 제1스토리지 축전판과 전기적으로 연결되는 구동 게이트전극에 전달할 초기화전압을 전달하며, 상기 제2스토리지 축전판과 동일층에 위치하는, 초기화전압선;

을 더 구비하고,

상기 드레인전극은 상기 제1스토리지 축전판에 전기적으로 연결되고, 상기 소스전극은 상기 초기화전압선에 전기적으로 연결되며,

상기 데이터선은 상기 제2스토리지 축전판보다 상부층에 위치하고,

상기 실드층은 상기 초기화전압선의 일부분으로서, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부와 상기 데이터선 사이로 연장된 부분, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분의 적어도 일부 상부로 연장된 부분 또는 상기 데이터선 하부로 연장된 부분인, 디스플레이 장치.

【청구항 10】

소스전극, 드레인전극 및 게이트전극을 포함하는 박막트랜지스터;

상기 소스전극, 상기 드레인전극 및 상기 게이트전극과 상이한 층에 위치하며, 데이터신호를 전달하는, 데이터선;

상기 드레인전극과 전기적으로 연결되는 제1스토리지 축전판과, 상기 제1스토리지 축전판과 중첩되도록 상기 제1스토리지 축전판이 위치한 층과 상이한 층에

위치한 제2스토리지 축전판을 포함하는 스토리지 캐패시터; 및

구동 박막트랜지스터의 상기 제1스토리지 축전판과 전기적으로 연결되는 구동 게이트전극에 전달할 초기화전압을 전달하며, 상기 소스전극과 전기적으로 연결되는, 초기화전압선;

을 구비하고,

상기 게이트전극은 제1게이트전극과 제2게이트전극을 포함하고, 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분과 상기 데이터선 사이에 상기 제1게이트전극과 상기 제2게이트전극 중 어느 하나가 적어도 부분적으로 위치하는, 디스플레이 장치.

【청구항 11】

제10항에 있어서,

상기 제1게이트전극과 상기 제2게이트전극 중 상기 박막트랜지스터의 상기 제1게이트전극과 상기 제2게이트전극 사이의 부분과 상기 데이터선 사이에 위치하는 것은, 상기 데이터선의 하부 또는 상부까지 연장된, 디스플레이 장치.

【청구항 12】

소스전극, 드레인전극 및 게이트전극을 포함하는 박막트랜지스터;

상기 소스전극, 상기 드레인전극 및 상기 게이트전극과 상이한 층에 위치하며, 제어신호를 전달하는, 제어신호선; 및

상기 박막트랜지스터의 적어도 일부분과 상기 제어신호선 사이에 위치하는

제출 일자 : 2014-08-05

실드층;

을 구비하는, 디스플레이 장치.

【요약서】

【요약】

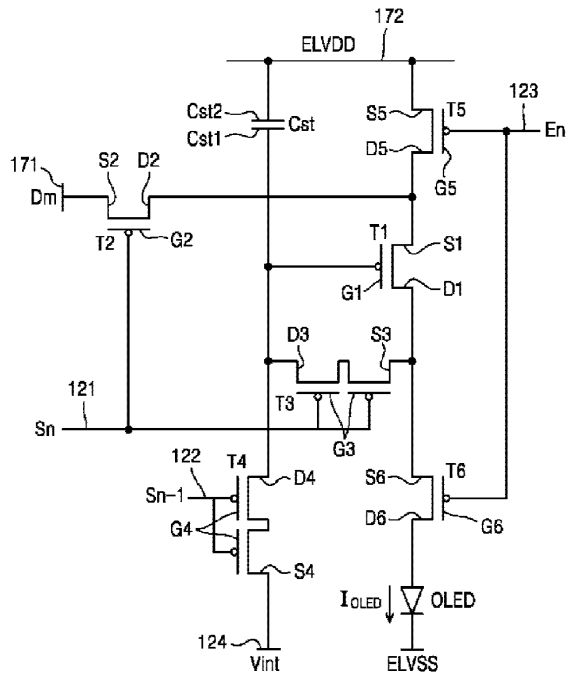
본 발명은 디스플레이되는 이미지의 품질 저하를 방지할 수 있는 디스플레이 장치를 위하여, 소스전극과 드레인전극과 게이트전극을 포함하는 박막트랜지스터와, 상기 소스전극과 상기 드레인전극과 상기 게이트전극과 상이한 층에 위치하며 데이터신호를 전달하는 데이터선과, 상기 박막트랜지스터의 적어도 일부분과 상기 데이터선 사이에 위치하는 실드층을 구비하는, 디스플레이 장치를 제공한다.

【대표도】

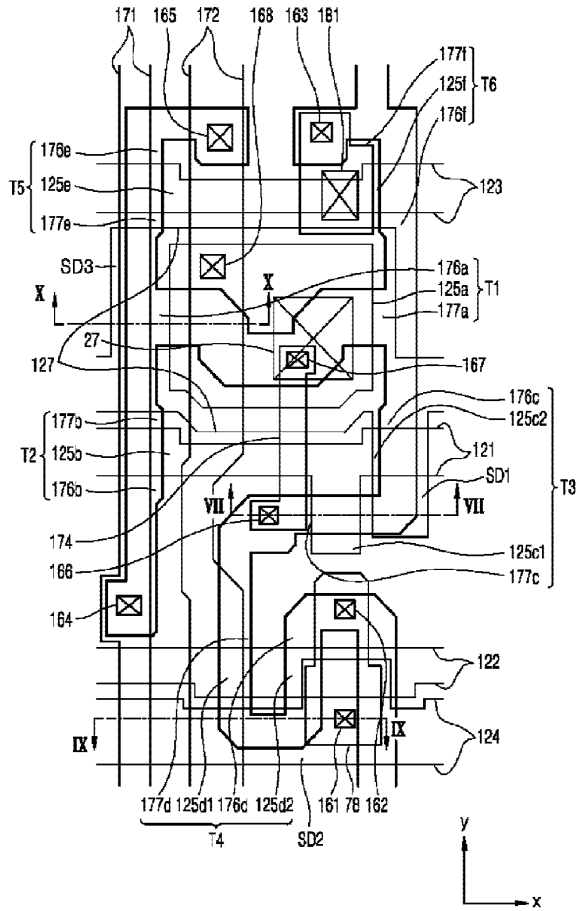
도 2

【도면】

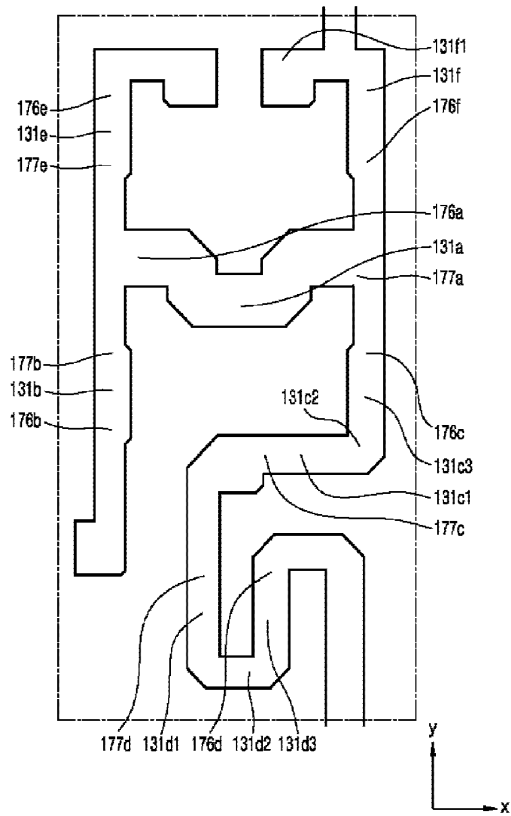
【도 1】



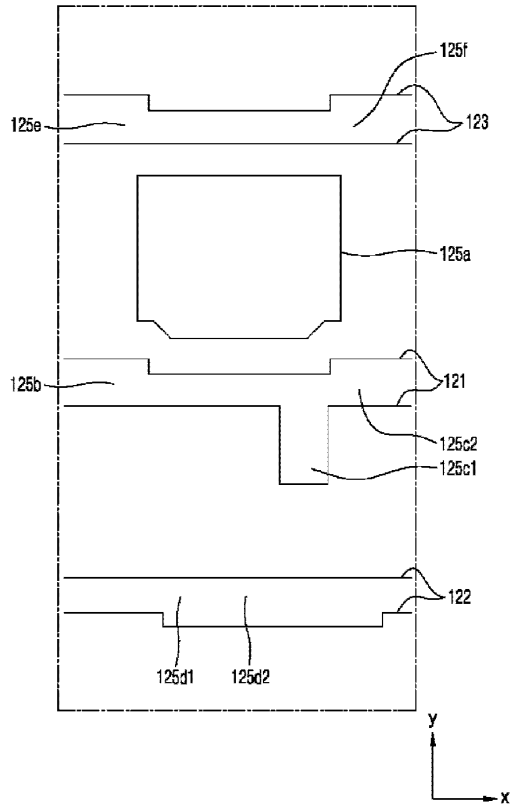
【도 2】



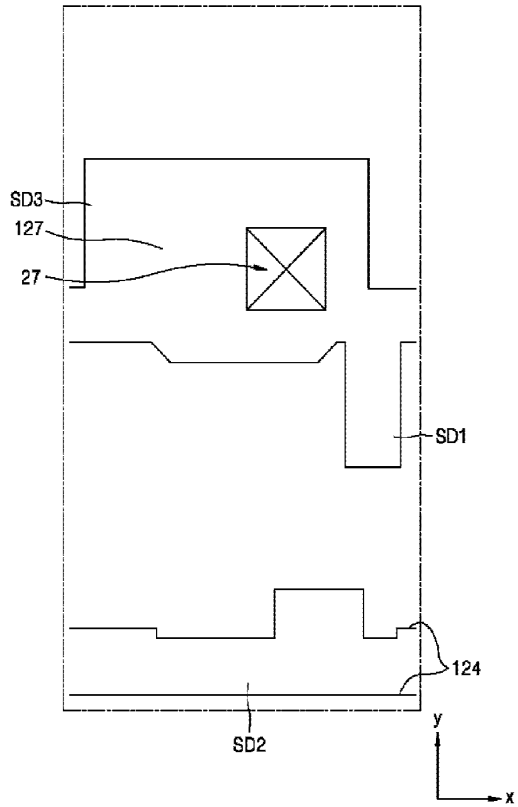
【도 3】



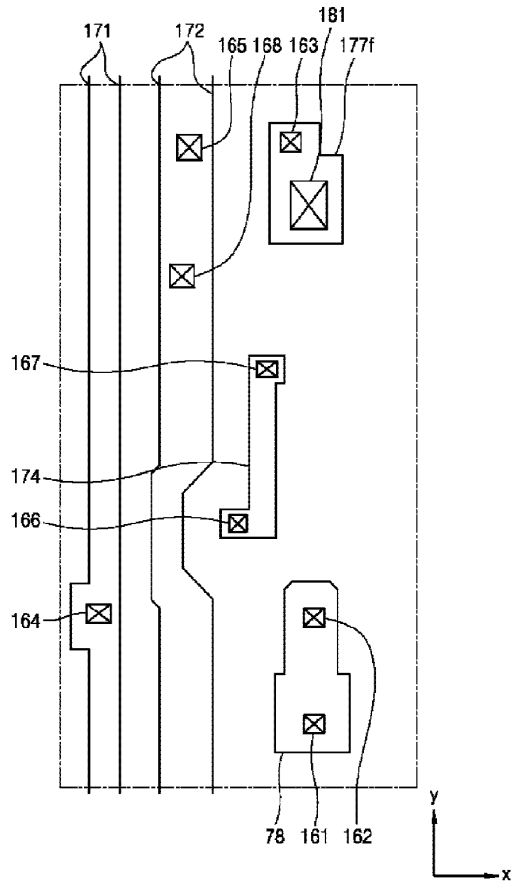
【도 4】



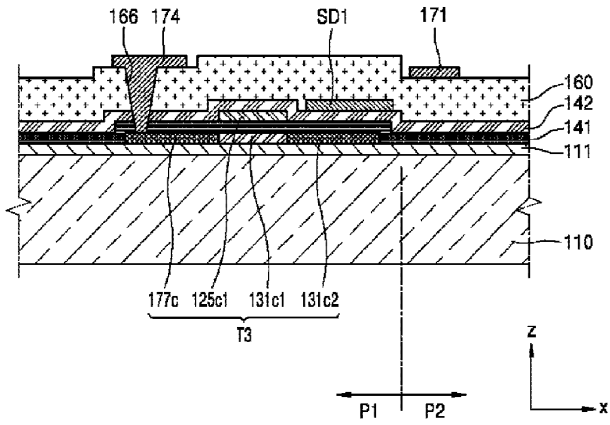
【도 5】



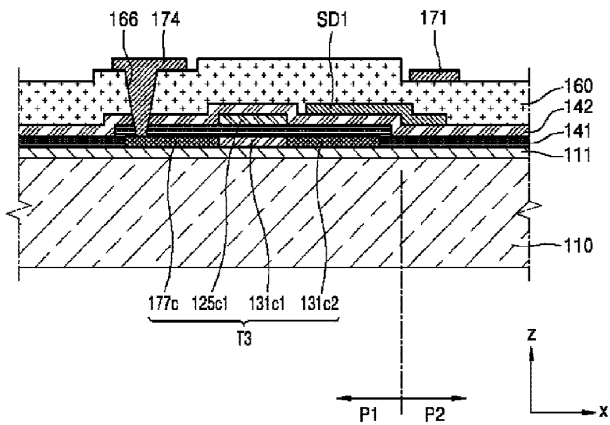
【도 6】



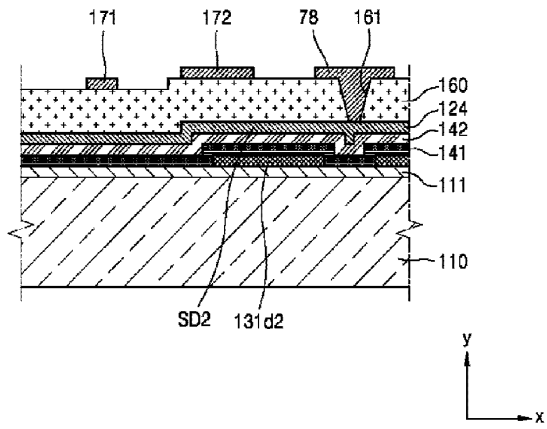
【도 7】



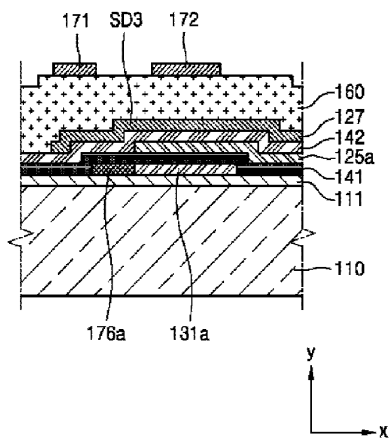
【도 8】



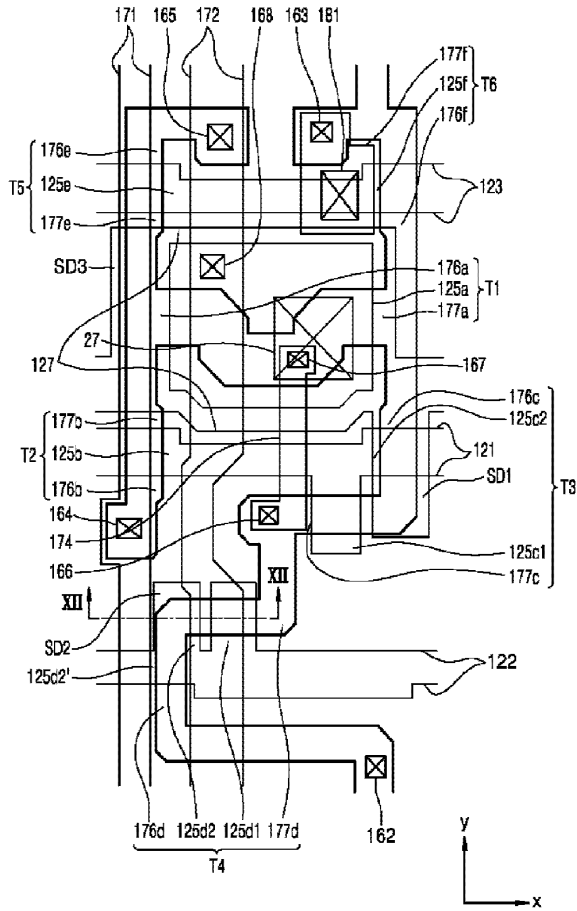
【도 9】



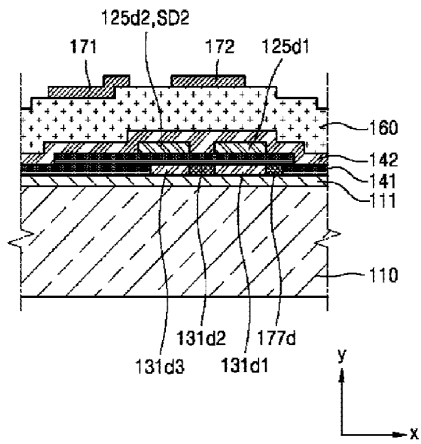
【도 10】



【도 11】



【도 12】





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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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United States Patent and Trademark Office
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www.uspto.gov

PRIORITY DOCUMENT EXCHANGE

FAILURE STATUS REPORT

An attempt by the Office to electronically retrieve, under the Priority Document Exchange programs (PDX and DAS), 10-2014-0100700 to which priority is claimed has FAILED on 03/13/2018.

For further questions or assistance, please contact our EBC Customer Support Center at

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pdx@uspto.gov (email)

Priority Document Exchange Website: http://www.uspto.gov/patents/process/file/pdx/pdx_index.jsp

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 15/838,138	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	1	minus 20 = *			OR	x 80 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =
	Application Size Fee (37 CFR 1.16(s))					OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR	
				TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =	OR	x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =	OR	x =
	Application Size Fee (37 CFR 1.16(s))					OR	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					OR	
				TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
15/838,138	12/11/2017	2811	1600	148454/411598-03044	1	1

CONFIRMATION NO. 4358

23363

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

FILING RECEIPT



CC00000098398942

Date Mailed: 01/04/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Yangwan Kim, Yongin-si, KOREA, REPUBLIC OF;
Wonkyu Kwak, Yongin-si, KOREA, REPUBLIC OF;
Jaedu Noh, Yongin-si, KOREA, REPUBLIC OF;
Jaeyong Lee, Yongin-si, KOREA, REPUBLIC OF;

Applicant(s)

Samsung Display Co., Ltd., Yongin-si, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 23363

Domestic Priority data as claimed by applicant

This application is a CON of 14/660,813 03/17/2015 PAT 9842892

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

REPUBLIC OF KOREA 10-2014-0100700 08/05/2014

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 01/02/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/838,138**

Projected Publication Date: 04/12/2018

Non-Publication Request: No

Early Publication Request: No
Title

DISPLAY APPARATUS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Attorney Docket Number	148454
	Application Number	To Be Determined
	Filing Date	December 11, 2017
	Inventor(s)	Yangwan Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

U.S. PATENT DOCUMENTS				
EXAMINER INITIALS	Cite No. ¹	DOCUMENT NUMBER Number - Kind Code ² (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		7,046,282 B1	05-16-2006	Zhang et al.
		8,471,973 B2	06-25-2013	Lin et al.
		2003/0202267 A1	10-30-2003	Yamasaki et al.
		2004/0252088 A1	12-16-2004	Kawachi et al.
		2005/0068310 A1	03-31-2005	Ishii
		2007/0029644 A1	02-08-2007	Nakagawa
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		2009/0009441 A1	01-08-2009	Yamamoto et al.
		2010/0110050 A1	05-06-2010	Park et al.
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		2013/0235020 A1	09-12-2013	Kim et al.
		2014/0062990 A1	03-06-2014	Zhang
		2014/0070184 A1	03-13-2014	Shin
		2014/0098078 A1	04-10-2014	Jeon et al.
		2014/0167009 A1	06-19-2014	Lee et al.
		2015/0177578 A1	06-25-2015	Uramoto
		2015/0364500 A1	12-17-2015	Cheng et al.

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
		EP 1 365 277 A2	11-26-2003	Murade	

EXAMINER SIGNATURE	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³ Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)	Attorney Docket Number	148454
	Application Number	To Be Determined
	Filing Date	December 11, 2017
	Inventor(s)	Yangwan Kim, et al.
	Group Art Unit	To Be Determined
	Examiner Name	To Be Determined

FOREIGN PATENT DOCUMENTS					
EXAMINER INITIALS	Cite No. ¹	Foreign Patent Document Country Code ³ - Number ⁴ - Kind Code ⁵ (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T ⁶ (✓)
		EP 2 693 481 A2	02-05-2014	Kim et al.	
		KR 10-2005-0021887	03-07-2005	Ishii	Corresponds to U.S. Pub. No. 2005/0068310 A1 listed above
		KR 10-2010-0049901	05-13-2010	Park et al.	Corresponds to U.S. Pub. No. 2010/0110050 A1 listed above
		KR 10-2012-0048531	05-15-2012	Kanegae	Corresponds to U.S. Pub. No. 2012/0074423 A1 listed above
		KR 10-2012-0103463	09-19-2012	Fujita	Corresponds to U.S. Pub. No. 2012/0229438 A1 listed above
		KR 10-2014-0035156	03-21-2014	Shin	Corresponds to U.S. Pub. No. 2014/0070184 A1 listed above

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		EPO Search Report dated December 11, 2015, for corresponding European Patent application 15176212.7, (9 pages)
		KIPO Office action dated October 1, 2015, for Korean priority Patent application 10-2014-0100700, (4 pages)
		KIPO Notice of Allowance dated April 11, 2016, for Korean priority Patent application 10-2014-0100700, (6 pages)

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EXAMINER SIGNATURE	DATE CONSIDERED
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³ Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.	

PCH/smv

Sheet 2 of 2

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		DISPLAY APPARATUS		
First Named Inventor/Applicant Name:		Yangwan Kim		
Filer:		Peter C. Hsueh/Si Vuong		
Attorney Docket Number:		148454/411598-03044		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt

EFS ID:	31193291
Application Number:	15838138
International Application Number:	
Confirmation Number:	4358
Title of Invention:	DISPLAY APPARATUS
First Named Inventor/Applicant Name:	Yangwan Kim
Customer Number:	23363
Filer:	Peter C. Hsueh/Si Vuong
Filer Authorized By:	Peter C. Hsueh
Attorney Docket Number:	148454/411598-03044
Receipt Date:	11-DEC-2017
Filing Date:	
Time Stamp:	19:14:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	121217INTEFSW19153000
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	148454_CONApplicationTransmittal.pdf	357045	no	3
			e911bdfb0f144c1655273d18d960fea1c3e4664b		
Warnings:					
Information:					
2	Power of Attorney	148454_POA.pdf	223385	no	2
			804f1d59bec0c27f109801dd918c03f4fa6d3bab		
Warnings:					
Information:					
3	Oath or Declaration filed	148454_ParentDec_030315.pdf	146412	no	3
			edf0f8b3a7ef785a68e3e102d09b1b8ef846585f		
Warnings:					
Information:					
4	Application Data Sheet	148454_ADS.pdf	1828889	no	9
			799bb19e4d1daea84db44cce77639ecd976ecf94		
Warnings:					
Information:					
5		148454_CONApplicationAsFiled.pdf	183619	yes	31
			67209f7efd80cbfa5985dcfb0e67b857a87af02c		
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Specification	1	29		
	Claims	30	30		
	Abstract	31	31		

Warnings:					
Information:					
6	Drawings-only black and white line drawings	148454_CONDrawingsAsFiled.pdf	328054 612745e2edc3ebbb0eed590966f4c4100a490688	no	12
Warnings:					
Information:					
7		148454_IDS_121117.pdf	314705 70c2e95410317e2b51df9d4ee3321995e0c03eab	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	3	
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	35127 aafd8938b687657907ceabed52dfb5281dd52748	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			3417236		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

UTILITY PATENT APPLICATION TRANSMITTAL
(Only for new nonprovisional applications under 37 CFR 1.53(b))

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on December 11, 2017 at or before 11:59 p.m. Eastern Standard Time under the Rules of 37 CFR § 1.10.



Si Vuong

Docket No. : 148454
Inventor(s) : Yangwan Kim, et al.
Title : DISPLAY APPARATUS

ADDRESS TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 11, 2017

1. ☒ **FEE TRANSMITTAL FORM**

2. **IF A CONTINUING APPLICATION**

☒ This application is a continuation of patent application No. 14/660,813.

Prior application information: Examiner Stephen C. Smith; Group Art Unit: 2896.

_____ This application claims the benefit of Provisional Application No. _____ pursuant to 35 U.S.C. §119(e) and 37 CFR §1.78(a)(4).

3. **APPLICATION COMPRISED OF**

Specification

31 Specification, claims and Abstract (total pages)

Drawings

12 Sheets of formal drawing(s) (FIGS. 1 to 12)

Inventor's Declaration(s)

_____ Executed Declaration (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional)

☒ Executed Declaration/Assignment (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional)

Power of Attorney by Applicant(s)

☒ Executed (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional) with transmittal

Application Data Sheet

☒ Newly executed ADS

_____ Unexecuted ADS

4. _____ **Microfiche Computer Program** (Appendix)

UTILITY PATENT APPLICATION TRANSMITTAL
(Only for new nonprovisional applications under 37 CFR 1.53(b))

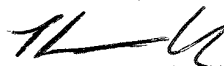
Docket No.: 148454

5. ☐ **Nucleotide and/or Amino Acid Sequence Submission** (if applicable, all necessary)
☐ Computer Readable Copy
☐ Paper Copy (identical to computer copy)
☐ Statement verifying identity of above copies
6. **APPLICANT(S) STATUS UNDER 37 CFR § 1.27 or 1.29**
☐ Applicant(s) and any others associated with it/them under § 1.27(a) are a SMALL ENTITY
☐ Applicant(s) and any others associated with it/them under § 1.29(a) are a MICRO ENTITY
☐ Certification of Micro Entity Status (Gross Income Basis)
7. **ALSO ENCLOSED ARE**
☐ Request and Certificate under 35 U.S.C. §122(b)(2)(B)(i) (**Request for Non-Publication**)
☐ Preliminary Amendment
☐ Includes "Cross-Reference to Related Applications"
☐ A Petition for Extension of Time for the parent application and the required fee are being filed concurrently herewith.
☐ This application is owned by ☐ pursuant to an Assignment recorded at Reel ☐ Frame ☐
☒ Information Disclosure Statement (IDS)
☐ Copies of IDS Citations
☐ Certified copy of Priority Document(s) (paper filing only, if foreign priority is claimed)
☐ English Translation Document (if applicable)
☐ Return Receipt Postcard (MPEP 503) (should be specifically itemized).
☐ Other: ☐
8. **DIRECT ALL CORRESPONDENCE TO: CUSTOMER NUMBER 23363**

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By



Peter C. Hsueh
Reg. No. 45,574
626/795-9900

LEWIS ROCA ROTHGERBER CHRISTIE LLP, P.O. BOX 29001, GLENDALE, CA 91209-9001

DATE: December 11, 2017

Duplicate

CLAIMS AS FILED							
	Number Filed	Number Extra	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee	
Total Claims	1 – 20	= 0	0 x \$80.00	\$40.00	\$20.00	\$0.00	
Independent Claims	1 – 3	= 0	0 x \$420.00	\$210.00	\$105.00	\$0.00	
Multiple-Dependent Claims Fee			\$780.00	\$390.00	\$195.00	\$0.00	
BASIC FILING, SEARCH, AND EXAMINATION FEES							
			Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee	
Basic Filing Fee			\$280.00	\$70.00	\$70.00	\$280.00	
Search Fee			\$600.00	\$300.00	\$150.00	\$600.00	
Examination Fee			\$720.00	\$360.00	\$180.00	\$720.00	
APPLICATION SIZE FEE							
EFS Paper Size Equivalent	Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof (round up to whole number)	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
43 * 75	= 33 – 100	= 0/50	= 0	0 x \$400.00	\$200.00	\$100.00	\$0.00
OTHER							
				Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Late Submission of Oath/Declaration Fee				\$140.00	\$70.00	\$35.00	\$0.00
Non-Electronic Filing Fee				\$400.00	\$200.00	\$200.00	\$0.00
TOTAL AMOUNT OF FEES						\$1,600.00	
List Independent Claims: 1							

 X Submitted herewith is the fee of \$1,600.00.

 X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required during the **entire pendency** of the application to Deposit Account No. 03-1728. Please show our docket number with any charge or credit to our Deposit Account.

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By

PCH/smv

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on December 11, 2017 at or before 11:59 p.m. Eastern Standard Time under the Rules of 37 CFR § 1.10.

Si Vuong



Inventor : Yangwan Kim, et al.
Application No. : To Be Determined
Filed : December 11, 2017
Title : DISPLAY APPARATUS

Grp./Div. : To Be Determined
Examiner : To Be Determined

Docket No. : 148454

**TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS
IN ACCORDANCE WITH 37 CFR 1.5**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
December 11, 2017

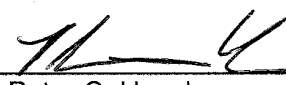
Commissioner:

Attached herewith is a General Power of Attorney for the above-identified patent application.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By



Peter C. Hsueh
Reg. No. 45,574
626/795-9900

PCH/smv

SMV 103016426.1-*-12/11/2017 11:10 AM

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number

Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)



I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

23363

OR



I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:



The address associated with the above-mentioned Customer Number

OR



The address associated with Customer Number:

OR

Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

SAMSUNG DISPLAY CO., LTD.



Inventor or Joint Inventor (title not required below)



Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)



Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)



Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Dong-Ho Lee

Title

Group Leader, IP Prosecution Group

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.



Total of

forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**INVENTOR'S DECLARATION AND ASSIGNMENT
FOR PATENT APPLICATION**

PATENT

Title of Invention: **DISPLAY APPARATUS**
Docket No.: **75955/S1437**

INVENTOR'S DECLARATION

As a below named inventor, I hereby declare that:

This declaration is directed to the attached application unless the following is checked:

☐ United States Application or PCT International Application Number _____
filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the above-identified application.

I have reviewed and understand the contents of the above-identified application, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, the undersigned,

(1) Yangwan Kim, Wonkyu Kwak, Jaedu Noh, and Jaeyong Lee

HEREBY SELL(S), ASSIGN(S) AND TRANSFER(S) TO

(2) SAMSUNG DISPLAY CO., LTD.

having a place of business at

(3) 95, Samsung 2 Ro, Giheung-Gu, Yongin-City, Gyeonggi-Do, Korea

(hereinafter called "ASSIGNEE") the entire right, title and interest in and to any and all improvements which are disclosed in the application for United States Letters Patent entitled

(4) DISPLAY APPARATUS

**INVENTOR'S DECLARATION AND ASSIGNMENT
FOR PATENT APPLICATION**

Docket No.: 75955/S1437

which application executed on even date
herewith or was

(a) executed on (5a): _____;

(b) filed on (5b): _____;

Application No.: _____;

(CHRISTIE PARKER & HALE, LLP, P.O. Box
29001, Glendale, CA 91209-9001) is hereby
authorized to insert in (b) the specified data,
when known.

including any and all United States Patents which may be granted on said application, and any and all extensions, divisions, reissues, substitutes, renewals or continuations of said application and patents, and the right to all benefits under all international conventions for the protection of industrial property and applications for said improvements.

It is hereby authorized and requested that the Commissioner of Patents issue any and all of said Letters Patent, when granted, to said ASSIGNEE, its assigns or its successors in interest or its designee.

Upon said consideration, it is further agreed that, when requested, without charge to but at the expense of said ASSIGNEE, the undersigned will execute all divisional, continuing, substitute, renewal, and reissue patent applications; execute all rightful other papers; and generally do everything possible which said ASSIGNEE shall consider desirable for aiding in securing and maintaining patent protection as provided herein.

Yangwan Kim
Legal Name of Inventor

2015. 3. 3
Date

Yang wan Kim
Signature

Wonkyu Kwak
Legal Name of Inventor

2015. 3. 3
Date

Won Kyu Kwak
Signature

**INVENTOR'S DECLARATION AND ASSIGNMENT
FOR PATENT APPLICATION**

Docket No.: 75955/S1437

Jaedu Noh
Legal Name of Inventor

2015. 3. 3
Date

Jaedu Noh
Signature

Jaeyong Lee
Legal Name of Inventor

2015. 3. 3
Date

Jaeyong Lee
Signature

WITNESSES:

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	148454/411598-03044
		Application Number	
Title of Invention	DISPLAY APPARATUS		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2:

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor	1				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Yangwan		Kim		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Yongin-si	Country of Residence ⁱ	KR		

Mailing Address of Inventor:

Address 1	c/o Samsung Display Co., Ltd.				
Address 2	1, Samsung-ro, Giheung-gu				
City	Yongin-si, Gyeonggi-do	State/Province			
Postal Code	17113	Country ⁱ	KR		

Inventor	2				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Wonkyu		Kwak		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Yongin-si	Country of Residence ⁱ	KR		

Mailing Address of Inventor:					
Address 1	c/o Samsung Display Co., Ltd.				
Address 2	1, Samsung-ro, Giheung-gu				
City	Yongin-si, Gyeonggi-do	State/Province			
Postal Code	17113	Country ⁱ	KR		

Inventor	3				Remove
Legal Name					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	148454/411598-03044
		Application Number	
Title of Invention	DISPLAY APPARATUS		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jaedu		Noh	
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service				
City	Yongin-si	Country of Residence ⁱ	KR	

Mailing Address of Inventor:

Address 1	c/o Samsung Display Co., Ltd.			
Address 2	1, Samsung-ro, Giheung-gu			
City	Yongin-si, Gyeonggi-do	State/Province		
Postal Code	17113	Country ⁱ	KR	
Inventor	4			<input type="button" value="Remove"/>
Legal Name				

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jaeyong		Lee	
Residence Information (Select One) US Residency ☒ Non US Residency Active US Military Service				
City	Yongin-si	Country of Residence ⁱ	KR	

Mailing Address of Inventor:

Address 1	c/o Samsung Display Co., Ltd.			
Address 2	1, Samsung-ro, Giheung-gu			
City	Yongin-si, Gyeonggi-do	State/Province		
Postal Code	17113	Country ⁱ	KR	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. <input type="button" value="Add"/>				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	23363		
Email Address	pto@lrrc.com	<input type="button" value="Add Email"/>	<input type="button" value="Remove Email"/>

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	148454/411598-03044
		Application Number	
Title of Invention	DISPLAY APPARATUS		

Application Information:

Title of the Invention	DISPLAY APPARATUS		
Attorney Docket Number	148454/411598-03044	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	12	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

<p>Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.</p>											
<table border="1"> <tr> <td>Please Select One:</td> <td>☒ Customer Number</td> <td>US Patent Practitioner</td> <td>☐ Limited Recognition (37 CFR 11.9)</td> </tr> <tr> <td>Customer Number</td> <td colspan="3">23363</td> </tr> </table>				Please Select One:	☒ Customer Number	US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)	Customer Number	23363		
Please Select One:	☒ Customer Number	US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)								
Customer Number	23363										

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	148454/411598-03044
		Application Number	
Title of Invention	DISPLAY APPARATUS		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	14/660813	2015-03-17
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Remove
10-2014-0100700	KR	2014-08-05	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	148454/411598-03044
		Application Number	
Title of Invention	DISPLAY APPARATUS		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	148454/411598-03044
		Application Number	
Title of Invention	DISPLAY APPARATUS		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant	1		<input type="button" value="Remove"/>
<p>If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.</p>			
		<input type="button" value="Clear"/>	
☒ Assignee	Legal Representative under 35 U.S.C. 117		Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
<div style="border: 1px solid black; height: 20px; width: 100%;"></div>			
Name of the Deceased or Legally Incapacitated Inventor: <div style="border: 1px solid black; height: 20px; width: 100%;"></div>			
If the Applicant is an Organization check here. ☒			
Organization Name	Samsung Display Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	1, Samsung-ro, Giheung-gu		
Address 2			
City	Yongin-si, Gyeonggi-do	State/Province	
Country	KR	Postal Code	17113
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			<input type="button" value="Add"/>

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	148454/411598-03044
		Application Number	
Title of Invention	DISPLAY APPARATUS		

Assignee	1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
<input type="button" value="Remove"/>				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>	<input type="text"/>
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1		<input type="text"/>		
Address 2		<input type="text"/>		
City	<input type="text"/>	State/Province	<input type="text"/>	
Country ⁱ	<input type="text"/>	Postal Code	<input type="text"/>	
Phone Number	<input type="text"/>	Fax Number	<input type="text"/>	
Email Address	<input type="text"/>			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. <input type="button" value="Add"/>				

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Peter C. Hsueh/		Date (YYYY-MM-DD)	2017-12-11
First Name	Peter C.	Last Name	Hsueh	Registration Number
				45574
Additional Signature may be generated within this form by selecting the Add button. <input type="button" value="Add"/>				

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	148454/411598-03044
		Application Number	
Title of Invention	DISPLAY APPARATUS		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DISPLAY APPARATUS

5 CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation of U.S. Patent Application No. 14/660,813, filed March 17, 2015, which claims priority to and the benefit of Korean Patent Application No. 10-2014-0100700, filed August 5, 2014, the entire content of both of which is incorporated herein by reference.

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BACKGROUND

1. Field

[0002] Embodiments of the present invention relate to a display apparatus.

15 2. Description of the Related Art

[0003] In an organic light-emitting display apparatus, thin-film transistors (TFTs) may be located in each (sub) pixel to control the luminance of each (sub) pixel. Such TFTs control the luminance of the sub (pixel) according to a received data signal.

20 [0004] However, luminance realized in a (sub) pixel of a general display apparatus may be different from that depending on a received data signal. Accordingly, an image displayed on the general display apparatus may have deteriorated quality.

SUMMARY

25 [0005] One or more embodiments of the present invention include a display apparatus for preventing quality deterioration of a displayed image.

[0006] Additional aspects will be set forth in part in the description which follows and, in part, will be apparent from the description, or may be learned by practice of the presented embodiments.

5 [0007] According to some embodiments of the present invention, a display apparatus includes: a thin-film transistor including a source electrode, a drain electrode, and a gate electrode; a data line in a layer different from the source electrode, the drain electrode, and the gate electrode, wherein the data line is configured to transmit a data signal; and a shield layer between the data line and a component of the thin-film transistor.

10 [0008] The shield layer may be between at least one of the source electrode and the data line, the drain electrode and the data line, or the gate electrode and the data line.

15 [0009] The display apparatus may further include a storage capacitor including a first storage capacitor plate and a second storage capacitor plate, the second storage capacitor plate overlapping the first storage capacitor plate and being above the first storage capacitor plate, the data line may be in a layer above the second storage capacitor plate, the second storage capacitor plate may include the shield layer, and the shield layer may extend between the gate electrode and the data line or extends below the data line.

20 [0010] The first storage capacitor plate may be electrically coupled to the gate electrode.

[0011] The first storage capacitor plate and the gate electrode may be integrally formed.

25 [0012] The gate electrode may include a first gate electrode and a second gate electrode, the shield layer may be between the data line and the component, and the component may be between the first gate electrode and the second gate electrode of the thin-film transistor.

[0013] The display apparatus may further include a storage capacitor including a first storage capacitor plate and a second storage capacitor plate, the second storage capacitor plate overlapping the first storage capacitor plate and being above the first

storage capacitor plate, the data line may be in a layer above the second storage capacitor plate, and the second storage capacitor plate may include the shield layer and extend at least one of between the data line and the component, between the first gate electrode and the second gate electrode of the thin-film transistor, or below the data line.

[0014] The display apparatus may further include a driving thin-film transistor including a driving gate electrode electrically coupled to the first storage capacitor plate and a driving drain electrode electrically coupled to the source electrode, and the first storage capacitor plate may be electrically coupled to the drain electrode.

[0015] The display apparatus may further include: a storage capacitor including a first storage capacitor plate and a second storage capacitor plate, the second capacitor plate overlapping the first storage capacitor plate and being above the first storage capacitor plate; and an initialization voltage line configured to transmit an initialization voltage to a driving gate electrode electrically coupled to the first storage capacitor plate of a driving thin-film transistor, the initialization voltage line may be in a same layer as the second storage capacitor plate, the drain electrode may be electrically coupled to the first storage capacitor plate and the source electrode may be electrically coupled to the initialization voltage line, the data line may be in a layer above the second storage capacitor plate, and the shield layer may be integrated with the initialization voltage line and may extend at least one of between the data line and the component, above the component between the first gate electrode and the second gate electrode of the thin-film transistor, or below the data line.

[0016] According to some embodiments of the present invention, a display apparatus includes: a thin-film transistor including a source electrode, a drain electrode, and a gate electrode; a data line in a layer different from the source electrode, the drain electrode, and the gate electrode, wherein the data line is configured to transmit a data signal; a storage capacitor including: a first storage

capacitor plate electrically coupled to the drain electrode; and a second storage capacitor plate in a layer different from the first storage capacitor plate, wherein the second storage capacitor plate overlaps the first storage capacitor plate; and an initialization voltage line configured to transmit an initialization voltage to a driving gate electrode electrically coupled to the first storage capacitor plate of a driving thin-film transistor and is electrically coupled to the source electrode, wherein the gate electrode includes a first gate electrode and a second gate electrode, and one of the first gate electrode and the second gate electrode is at least partially between the data line and a component between the first gate electrode and the second gate electrode of the thin-film transistor.

[0017] The one of the first gate electrode and the second gate electrode may extend below or above the data line.

[0018] According to some embodiments of the present invention, a display apparatus includes: a thin-film transistor including a source electrode, a drain electrode, and a gate electrode; a control signal line in a layer different from the source electrode, the drain electrode, and the gate electrode, and wherein the control signal line is configured to transmit a control signal; and a shield layer between the control signal line and a component of the thin-film transistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] These and/or other aspects will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings in which:

[0020] FIG. 1 is a circuit diagram of a (sub) pixel of an organic light-emitting display apparatus, according to an embodiment of the present invention;

[0021] FIG. 2 is a schematic diagram showing locations of a plurality of thin-film transistors (TFTs) and a capacitor in the (sub) pixel of FIG. 1, according to an embodiment of the present invention;

[0022] FIGS. 3 through 6 are schematic diagrams showing components of the plurality of TFTs and the capacitor of FIG. 2 by each layer;

[0023] FIG. 7 is a cross-sectional view taken along the line VII-VII of FIG. 2;

[0024] FIG. 8 is a cross-sectional view of an organic light-emitting display apparatus according to some embodiments of the present invention;

[0025] FIG. 9 is a cross-sectional view taken along the line IX-IX of FIG. 2;

[0026] FIG. 10 is a cross-sectional view taken along the line X-X of FIG. 2;

[0027] FIG. 11 is a schematic diagram showing locations of a plurality of TFTs and a capacitor in a (sub) pixel of an organic light-emitting display apparatus, according to another embodiment of the present invention; and

[0028] FIG. 12 is a cross-sectional view taken along the line XII-XII of FIG. 11.

DETAILED DESCRIPTION

[0029] Aspects and features of one or more embodiments of the present invention and methods of accomplishing the same may be understood more readily by reference to the following detailed description of the embodiments and the accompanying drawings. In this regard, the present embodiments may have different forms and should not be construed as being limited to the descriptions set forth herein. Rather, these embodiments are provided so that this disclosure will be more thorough and complete and will more fully convey the concepts of the present embodiments to one of ordinary skill in the art, and the present invention will only be defined by the appended claims and their equivalents.

[0030] Hereinafter, one or more embodiments of the present invention will be described below in more detail with reference to the accompanying drawings. Those

components that are the same or are in correspondence are rendered the same reference numeral regardless of the figure number, and redundant explanations are omitted.

[0031] It will be understood that when a layer, region, or component is referred to as being "formed on," another layer, region, or component, it can be directly or indirectly formed on the other layer, region, or component. That is, for example, intervening layers, regions, or components may be present. Sizes of elements in the drawings may be exaggerated for convenience of explanation. In other words, since sizes and thicknesses of components in the drawings are arbitrarily illustrated for convenience of explanation, the following embodiments are not limited thereto.

[0032] In the following examples, the x-axis, the y-axis and the z-axis are not limited to three axes of the rectangular coordinate system, and may be interpreted in a broader sense. For example, the x-axis, the y-axis, and the z-axis may be perpendicular to one another, or may represent different directions that are not perpendicular to one another.

[0033] As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0034] FIG. 1 is an equivalent circuit diagram of a (sub) pixel of an organic light-emitting display apparatus, according to some embodiments of the present invention.

[0035] As shown in FIG. 1, the (sub) pixel of the organic light-emitting display apparatus according to an embodiment includes a plurality of signal lines, a plurality of thin-film transistors (TFTs) coupled to the plurality of signal lines, a storage capacitor Cst, and an organic light-emitting device OLED. Here, the plurality of signal lines may be shared by a plurality of (sub) pixels.

[0036] The plurality of TFTs include a driving TFT T1, a switching TFT T2, a compensating TFT T3, an initialization TFT T4, an operation control TFT T5, and an emission control TFT T6.

[0037] The plurality of signal lines include a scan line 121 transmitting a scan signal S_n , a previous scan line 122 transmitting a previous scan line S_{n-1} to the initialization TFT T4, an emission control line 123 transmitting an emission control signal E_n to the operation control TFT T5 and the emission control TFT T6, a data line 171 crossing the scan line 121 and transmitting a data signal D_m , a driving voltage line 172 transmitting a driving voltage ELVDD and disposed almost in parallel to the data line 171, and an initialization voltage line 124 transmitting an initialization voltage V_{int} for initializing the driving TFT T1.

[0038] A gate electrode G1 of the driving TFT T1 is coupled to a first storage capacitor plate Cst1 of the storage capacitor Cst, a source electrode S1 of the driving TFT T1 is coupled to the driving voltage line 172 through the operation control TFT T5, and a drain electrode D1 of the driving TFT T1 is electrically coupled to a pixel electrode of the organic light-emitting device OLED through the emission control TFT T6. According to a switching operation of the switching TFT T2, the driving TFT T1 receives the data signal D_m and supplies a driving current I_{OLED} to the organic light-emitting device OLED.

[0039] A gate electrode G2 of the switching TFT T2 is coupled to the scan line 121, a source electrode S2 of the switching TFT T2 is coupled to the data line 171, and a drain electrode D2 of the switching TFT T2 is coupled to the source electrode S1 of the driving TFT T1 and coupled to the driving voltage line 172 through the operation control TFT T5. Such a switching TFT T2 is turned on according to the scan signal S_n received through the scan line 121, and performs a switching operation by transmitting the data signal D_m from the data line 171 to the source electrode S1 of the driving TFT T1.

[0040] A gate electrode G3 of the compensation TFT T3 is coupled to the scan line 121, a source electrode S3 of the compensating TFT T3 is coupled to the drain electrode D1 of the driving TFT T1 while being coupled to the pixel electrode of the

organic light-emitting device OLED through the emission control TFT T6, and a drain electrode D3 of the compensating TFT T3 is coupled to the first storage capacitor plate Cst1 of the storage capacitor Cst, a drain electrode D4 of the initialization TFT T4, and the gate electrode G1 of the driving TFT T1. Such a compensating TFT T3 is turned on according to the scan signal Sn received through the scan line 121, and diode-connects the driving TFT T1 by electrically coupling the gate electrode G1 and the drain electrode D1 of the driving TFT T1.

10 **[0041]** A gate electrode G4 of the initialization TFT T4 is coupled to the previous scan line 122, a source electrode S4 of the initialization TFT T4 is coupled to the initialization voltage line 124, and the drain electrode D4 of the initialization TFT T4 is coupled to the first storage capacitor plate Cst1 of the storage capacitor Cst, the drain electrode D3 of the compensating TFT T3, and the gate electrode G1 of the driving TFT T1. The initialization TFT T4 is turned on according to the previous scan signal Sn-1 received through the previous scan line 122, and performs an initialization operation by initializing a voltage of the gate electrode G1 of the driving TFT T1 by transmitting the initialization voltage Vint to the gate electrode G1 of the driving TFT T1.

20 **[0042]** A gate electrode G5 of the operation control TFT T5 is coupled to the emission control line 123, a source electrode S5 of the operation control TFT T5 is coupled to the driving voltage line 172, and a drain electrode D5 of the operation control TFT T5 is coupled to the source electrode S1 of the driving TFT T1 and the drain electrode D2 of the switching TFT T2.

25 **[0043]** A gate electrode G6 of the emission control TFT T6 is coupled to the emission control line 123, a source electrode S6 of the emission control TFT T6 is coupled to the drain electrode D1 of the driving TFT T1 and the source electrode S3 of the compensating TFT T3, and a drain electrode D6 of the emission control TFT T6 is electrically coupled to the pixel electrode of the organic light-emitting device OLED.

The operation control TFT T5 and an emission control TFT T6 are concurrently (e.g., simultaneously) turned on according to the emission control signal En received through the emission control line 123, and transmit the driving voltage ELVDD to the organic light-emitting device OLED such that the driving current I_{OLED} flows through the organic light-emitting device OLED.

[0044] A second storage capacitor plate Cst2 of the storage capacitor Cst is coupled to the driving voltage line 172, and a counter electrode of the organic light-emitting device OLED is coupled to a common voltage ELVSS. Accordingly, the organic light-emitting device OLED emits light by receiving the driving current I_{OLED} from the driving TFT T1, thereby displaying an image.

[0045] Detailed operations of a pixel in such an organic light-emitting display apparatus will now be briefly described.

[0046] First, the previous scan signal Sn-1 in a low level is supplied through the previous scan line 122 during an initialization period. Then, the initialization TFT T4 is turned on in response to the previous scan signal Sn-1 in the low level, and thus the initialization voltage Vint is transmitted to the gate electrode G1 of the driving TFT T1 from the initialization voltage line 124 through the initialization TFT T4, and the driving TFT T1 is initialized by the initialization voltage Vint.

[0047] Then, the scan signal Sn in a low level is supplied through the scan line 121 during a data programming period. Accordingly, the switching TFT T1 and the compensating TFT T3 are turned on in response to the scan signal Sn in the low level. Thus, the driving TFT T1 is diode-coupled by the turned on compensating TFT T3 and is biased in a forward direction. Then, a compensating voltage ($Dm + V_{th}$, wherein V_{th} has a negative value) obtained by subtracting a threshold voltage V_{th} of the driving TFT T1 from the data signal Dm supplied from the data line 171 is applied to the gate electrode G1. Next, the driving voltage ELVDD and the compensating voltage are

applied to two ends of the storage capacitor Cst, and thus a charge corresponding to a voltage difference between the two ends is stored in the storage capacitor Cst.

5 **[0048]** Then, the emission control signal En supplied from the emission control line 123 during an emission period is changed from a high level to a low level. Accordingly, the operation control TFT T5 and the emission control TFT T6 are turned on according to the emission control signal En in the low level during the emission period. Then, the driving current I_{OLED} determined based on a voltage difference between a voltage of the gate electrode G1 of the driving TFT T1 and the driving voltage ELVDD is generated, and the driving current I_{OLED} is supplied to the organic light-emitting device OLED through the emission control TFT T6. A gate-source voltage V_{GS} of the driving TFT T1 maintains '(Dm+Vth)-ELVDD' by the storage capacitor Cst during the emission period, and because the driving current I_{OLED} is proportional to '(Dm-ELVDD)²' (i.e., a square of a value obtained by subtracting the threshold voltage Vth from the gate-source voltage V_{GS} , according to a current-voltage relationship of the driving TFT T1), the driving current I_{OLED} may be determined regardless of the threshold voltage Vth of the driving TFT T1.

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[0049] A more detailed structure of the (sub) pixel of the organic light-emitting display apparatus of FIG. 1 will now be described with reference to FIGS. 2 through 10.

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[0050] FIG. 2 is a schematic diagram showing locations of the plurality of TFTs and the capacitor in the (sub) pixel of FIG. 1, according to an embodiment of the present invention. FIGS. 3 through 6 are schematic diagrams showing components of the plurality of TFTs and the capacitor of FIG. 2 by each layer. In other words, each of FIGS. 3 through 6 illustrates an arrangement of a wire or a semiconductor layer disposed in the same layer, and an insulating layer may be located between layers shown in FIGS. 3 through 6. For example, a first insulating layer 141 of FIG. 7 may be located between the layer of FIG. 3 and the layer of FIG. 4, a second insulating layer 142 of FIG. 7 may be located between the layer of FIG. 4 and the layer of FIG. 5, and

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an interlayer insulating layer 160 of FIG. 7 may be located between the layer of FIG. 5 and the layer of FIG. 6. Here, contact holes etc. may be formed on such insulating layers so that the layers of FIGS. 3 through 6 are electrically coupled to each other.

[0051] The (sub) pixel of the organic light-emitting display apparatus, according to the current embodiment, includes the scan line 121, the previous scan line 122, the emission control line 123, and the initialization voltage line 124, which respectively apply the scan signal S_n , the previous scan signal S_{n-1} , the emission control signal E_n , and the initialization voltage V_{int} and are formed along a row direction. Also, the (sub) pixel of the organic light-emitting display apparatus, according to the current embodiment, may include the data line 171 and the driving voltage line 172, which cross the scan line 121, the previous scan line 122, the emission control line 123, and the initialization voltage line 124, and respectively apply the data signal D_m and the driving voltage ELVDD to the (sub) pixel.

[0052] Also, the (sub) pixel may include the driving TFT T1, the switching TFT T2, the compensating TFT T3, the initialization TFT T4, the operation control TFT T5, the emission control TFT T6, the storage capacitor C_{st} , and an organic light-emitting device.

[0053] The driving TFT T1, the switching TFT T2, the compensating TFT T3, the initialization TFT T4, the operation control TFT T5, and the emission control TFT T6 are formed on a semiconductor layer as shown in FIG. 3, wherein the semiconductor layer may have a shape curving or contouring in any shape. The semiconductor layer may include a driving semiconductor layer 131a corresponding to the driving TFT T1, a switching semiconductor layer 131b corresponding to the switching TFT T2, a compensating semiconductor layer 131c1, 131c2, and 131c3 corresponding to the compensating TFT T3, initialization semiconductor layer 131d1, 131d2, and 131d3 corresponding to the initialization TFT T4, an operation control semiconductor layer 131e corresponding to the operation control TFT T5, and an emission control

semiconductor layer 131f corresponding to the emission control TFT T6. In other words, the driving semiconductor layer 131a, the switching semiconductor layer 131b, the compensating semiconductor layer 131c1, 131c2, and 131c3, the initialization semiconductor layer 131d1 through 131d3, the operation control semiconductor layer 131e, and the emission control semiconductor layer 131f may be understood to constitute partial regions of the semiconductor layer of FIG. 3.

[0054] The semiconductor layer may include polysilicon. Also, the semiconductor layer may include, for example, a channel region that is not doped with an impurity, and source and drain regions that are formed as impurities are doped on two sides of the channel region. Here, the impurities may vary according to a type of a TFT, and may be N-type impurities or P-type impurities. Also, the source or drain region may be interpreted as a source or drain electrode of a TFT. In other words, for example, a driving source electrode 176a may correspond to a driving drain region doped with an impurity near the driving semiconductor layer 131a of the semiconductor layer of FIG. 3, and a driving drain electrode 177a may correspond to a driving drain region doped with an impurity near the driving semiconductor layer 131a of the semiconductor layer of FIG. 3. Also, a region of the semiconductor layer of FIG. 3 between TFTs may be doped with an impurity to operate as a wire electrically coupling the TFTs.

[0055] Meanwhile, the storage capacitor Cst may be formed. The storage capacitor Cst may include a first storage capacitor plate 125a and a second storage capacitor plate 127, wherein the second insulating layer 142 is located therebetween. Here, the first storage capacitor plate 125a may also operate as a driving gate electrode of the driving TFT T1. In other words, the driving gate electrode and the first storage capacitor plate 125a may be integrally formed. Hereinafter, for convenience, the same reference numeral as the first storage capacitor plate 125a may be used for the driving gate electrode.

[0056] The first storage capacitor plate 125a may have a rectangular shape isolated from an adjacent (sub) pixel as shown in FIG. 4. Such a first storage capacitor plate
5 125a may be formed in the same layer and of the same material as the scan line 121, the previous scan line 122, and the emission control line 123 as shown in FIG. 4.

[0057] For reference, a switching gate electrode 125b and a compensating gate electrode 125c1 and 125c2 may be a part of the scan line 121 crossing the semiconductor layer or a part protruding from the scan line 121, an initialization gate
10 electrode 125d1 and 125d2 may be parts of the previous scan line 122 crossing the semiconductor layer or parts protruding from the previous scan line 122, and an operation control gate electrode 125e and an emission control gate electrode 125f may be parts of the emission control line 123 crossing the semiconductor layer or parts protruding from the emission control line 123.

[0058] The second storage capacitor plates 127 of adjacent (sub) pixels may be coupled to each other, and as shown in FIG. 5, may be formed in the same layer and of the same material as the initialization voltage line 124. A storage opening 27 may be formed on the second storage capacitor plate 127 and may enable the first storage capacitor plate 125a and a compensating drain electrode 177c of the compensating
15 TFT T3 to be electrically coupled to each other through a connecting unit 174 described in more detail later. The second storage capacitor plate 127 may be coupled to the driving voltage line 172 through a contact hole 168 formed on the interlayer insulating layer 160.

[0059] The driving TFT T1 includes the driving semiconductor layer 131a, the driving gate electrode 125a, the driving source electrode 176a, and the driving drain electrode 177a. As described above, the driving gate electrode 125a may also operate as the first storage capacitor plate 125a. The driving source electrode 176a is an external region (in -x direction in FIG. 3) of the driving gate electrode 125a, and the driving drain electrode 177a is an external region (in +x direction in FIG. 3) of the
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driving gate electrode 125a and is arranged opposite to the driving source electrode 176a based on the driving gate electrode 125a.

5 **[0060]** The switching TFT T2 includes the switching semiconductor layer 131b, the switching gate electrode 125b, a switching source electrode 176b, and a switching drain electrode 177b. The switching source electrode 176b may be electrically coupled to the data line 171 through a contact hole 164 formed through the first insulating layer 141, the second insulating layer 142, and the interlayer insulating layer 160. Here, if
10 required, a part near the contact hole 164 of the data line 171 may be understood to be the source electrode S2 of the switching TFT T2. The switching drain electrode 177b corresponds to a switching drain region doped with an impurity near the switching semiconductor layer 131b.

[0061] The compensating TFT T3 includes the compensating semiconductor layer 15 131c1, 131c2, and 131c3, the compensating gate electrode 125c1 and 125c2, a compensating source electrode 176c, and the compensating drain electrode 177c. The compensating source electrode 176c corresponds to a compensating source region doped with an impurity near the compensating semiconductor layer, and the compensating drain electrode 177c corresponds to a compensating drain region doped
20 with an impurity near the compensating semiconductor layer. The compensating gate electrode 125c1 and 125c2 is a dual gate electrode including a first gate electrode 125c1 and a second gate electrode 125c2, and may prevent or reduce generation of a leakage current. The compensating drain electrode 177c of the compensating TFT T3 may be coupled to the first storage capacitor plate 125a through the connecting unit
25 174. The compensating semiconductor layer may include a part or component 131c1 corresponding to the first gate electrode 125c1, a part or component 131c3 corresponding to the second gate electrode 125c2, and a part or component 131c2 between the parts 131c1 and 131c3.

[0062] As shown in FIG. 6, the connecting unit 174 may be formed of the same material and in the same layer as the data line 171. One end of the connecting unit 174 is coupled to the compensating drain electrode 177c and an initialization drain electrode 177d through a contact hole 166 formed through the first insulating layer 141, the second insulating layer 142, and the interlayer insulating layer 160, and the other end of the connecting unit 174 is coupled to the first storage capacitor plate 125a through a contact hole 167 formed through the second insulating layer 142 and the interlayer insulating layer 160. Here, the other end of the connecting unit 174 is coupled to the first storage capacitor plate 125a through the storage opening 27 formed on the second storage capacitor plate 127.

[0063] The initialization TFT T4 includes an initialization semiconductor layer 131d1, 131d2, and 131d3, an initialization gate electrode 125d1 and 125d2, an initialization source electrode 176d, and the initialization drain electrode 177d. The initialization drain electrode 177d corresponds to an initialization drain region doped with an impurity near the initialization semiconductor layer 131d1, 131d2, and 131d3.

[0064] The initialization source electrode 176d is coupled to the initialization voltage line 124 through an initialization connecting line 78. One end of the initialization connecting line 78 may be coupled to the initialization voltage line 124 through a contact hole 161 formed through the second insulating layer 142 and the interlayer insulating layer 160, and the other end of the initialization connecting line 78 may be coupled to the initialization source electrode 176d through a contact hole 162 formed through the first insulating layer 141, the second insulating layer 142, and the interlayer insulating layer 160.

[0065] The operation control TFT T5 includes the operation control semiconductor layer 131e, the operation control gate electrode 125e, an operation control source electrode 176e, and an operation control drain electrode 177e. The operation control source electrode 176e may be electrically coupled to the driving voltage line 172

through a contact hole 165 formed through the first insulating layer 141, the second insulating layer 142, and the interlayer insulating layer 160. Here, if required, a part near the contact hole 165 of the driving voltage line 172 may be understood to be the source electrode S5 of the operation control TFT T5. The operation control drain electrode 177e corresponds to an operation control drain region doped with an impurity near the operation control semiconductor layer 131e.

[0066] The emission control TFT T6 includes the emission control semiconductor layer 131f, the emission control gate electrode 125f, an emission control source electrode 176f, and an emission control drain electrode 177f. The emission control source electrode 176f corresponds to an emission control source region doped with an impurity near the emission control semiconductor layer 131f. As shown in FIG. 6, the emission control drain electrode 177f may be understood to be a part formed on the interlayer insulating layer 160 together with the data line 171 or the driving voltage line 172. The emission control drain electrode 177f may be coupled to a lower semiconductor layer through a contact hole 163 formed through the first insulating layer 141, the second insulating layer 142, and the interlayer insulating layer 160. Alternatively, it may be understood that a part of the lower semiconductor layer is a emission control drain electrode, and the reference numeral 177f denote an intermediate connection layer for coupling the emission control drain electrode and the pixel electrode of the organic light-emitting device OLED.

[0067] One end of the driving semiconductor layer 131a of the driving TFT T1 is coupled to the switching semiconductor layer 131b and the compensating semiconductor layer, and the other end of the driving semiconductor layer 131a is coupled to the operation control semiconductor layer 131e and the emission control semiconductor layer 131f. Accordingly, the driving source electrode 176a is coupled to the switching drain electrode 177b and the operation control drain electrode 177e, and

the driving drain electrode 177a is coupled to the compensating source electrode 176c and the emission control source electrode 176f.

5 **[0068]** Meanwhile, the switching TFT T2 is used as a switching device for selecting a (sub) pixel to emit light. The switching gate electrode 125b is coupled to the scan line 121, the switching source electrode 176b is coupled to the data line 171, and the switching drain electrode 177b is coupled to the driving TFT T1 and the operation control TFT T5.

10 **[0069]** Also, as shown in FIG. 6, the emission control drain electrode 177f of the emission control TFT T6 is coupled to the pixel electrode of the organic light-emitting device OLED through a contact hole 181 formed on a passivation film or planarization film covering the data line 171 or the driving voltage line 172 formed in the same layer.

[0070] FIG. 7 is a cross-sectional view taken along the line VII-VII of FIG. 2. As shown in FIG. 7, various components described above may be arranged on a substrate 110. The substrate 110 may be formed of any one of various suitable substrate materials, such as glass, a metal, and plastic. A buffer layer 111 may be disposed on the substrate 110 as occasion demands. The buffer layer 111 may flatten a surface of the substrate 110 or prevent impurities from penetrating into a semiconductor layer on the substrate 110. Such a buffer layer 111 may be a single layer or multilayer structure formed of silicon oxide, silicon nitride, or silicon oxynitride.

20 **[0071]** The driving semiconductor layer 131a, the switching semiconductor layer 131b, and the compensating semiconductor layer described above with reference to FIG. 3 may be arranged on the buffer layer 111. The first insulating layer 141 formed of silicon nitride, silicon oxide, or silicon oxynitride may be arranged on the driving semiconductor layer 131a, the switching semiconductor layer 131b, and the compensating semiconductor layer.

[0072] Wires including the driving gate electrode 125a, the scan line 121 including the switching gate electrode 125b and the compensating gate electrode 125c1 and

125c2, the previous scan line 122 including the initialization gate electrode 125d1 and 125d2, the emission control line 123 including the operation control gate electrode 125e and the emission control gate electrode 125f, which have been described above with reference to FIG. 4, may be arranged on the first insulating layer 141. The driving gate electrode 125a, the scan line 121, the previous scan line 122, and the emission control line 123 may be collectively referred to as a first gate wire.

[0073] The second insulating layer 142 may cover the first gate wire. The second insulating layer 142 may be formed of silicon nitride, silicon oxide, or silicon oxynitride. The second storage capacitor plate 127 and the initialization voltage line 124 described above with reference to FIG. 5 may be arranged on the second insulating layer 142. The second storage capacitor plate 127 and the initialization voltage line 124 may be collectively referred to as a second gate wire.

[0074] The interlayer insulating layer 160 is disposed on the second gate wire. The interlayer insulating layer 160 may be formed of silicon nitride, silicon oxide, or silicon oxynitride.

[0075] The data line 171, the driving voltage line 172, the connecting unit 174, the initialization connecting line 78, and the emission control drain electrode 177f, which have been described above with reference to FIG. 6, may be arranged on the interlayer insulating layer 160. The data line 171, the driving voltage line 172, the connecting unit 174, the initialization connecting line 78, and the emission control drain electrode 177f may be collectively referred to as a data wire. As described above, the data line 171, the driving voltage line 172, the connecting unit 174, the initialization connecting line 78, and the emission control drain electrode 177f may be electrically coupled to a lower semiconductor layer or an electrode through the contact holes 161 through 168 formed on at least a part of the first insulating layer 141, the second insulating layer 142, and the interlayer insulating layer 160.

[0076] A passivation film or planarization film is disposed on the data wire, and a pixel electrode of an organic light-emitting device may be arranged on the passivation film or planarization film. The pixel electrode may be coupled to the emission control drain electrode 177f through the contact hole 181 formed on the passivation film or planarization film.

[0077] Meanwhile, as shown in FIGS. 2, 5, and 7, the second storage capacitor plate 127 may include a first shield layer SD1 at one side. As shown in FIGS. 2 and 5, the first shield layer SD1 may be a part protruding from the second storage capacitor plate 127. The first shield layer SD1 may be understood as a part of the second storage capacitor plate 127, which extends between the data line 171 and at least a part between the first gate electrode 125c1 and the second gate electrode 125c2 of the compensating TFT T3.

[0078] For reference, FIG. 2 is a diagram of one (sub) pixel, and a (sub) pixel having the same or similar structure may be disposed top, bottom, left, and right of the (sub) pixel. In FIG. 7, a (sub) pixel P1 corresponds to the (sub) pixel of FIG. 2, and a part of a (sub) pixel P2 disposed next to the (sub) pixel P1 in the +x direction of FIG. 2 are illustrated. The (sub) pixel P2 may also include the data line 171, and accordingly, the first shield layer SD1 of the (sub) pixel P1 may be understood to be a part of the second storage capacitor plate 127, which extends between the data line 171 of the (sub) pixel P2 and at least a part between the first and second gate electrodes 125c1 and 125c2 of the compensating TFT T3.

[0079] If the first shield layer SD1 does not exist, the components between the first and second gate electrodes 125c1 and 125c2 of the compensating TFT T3, for example, the part 131c2 of the compensating semiconductor layer, may be affected by the data line 171.

[0080] The data line 171 transmits a data signal to the (sub) pixel P2 disposed near the (sub) pixel P1 in the +x direction, and also transmits a data signal to a plurality of

(sub) pixels disposed near the (sub) pixel P2 in +y and -y directions. Here, a data signal being transmitted may vary according to luminance to be realized in the plurality of (sub) pixels disposed near the (sub) pixel P2 in the +y and -y directions, and accordingly, the data line 171 near the part 131c2 of the compensating semiconductor layer of the (sub) pixel P1 may transmit different electric signals according to time while the (sub) pixel P1 emits light.

[0081] If the first shield layer SD1 does not exist, parasitic capacitance may occur between the data line 171 of the (sub) pixel P2 and the part 131c2 of the compensating TFT T3 of the (sub) pixel P1, and accordingly, the electric potential of the part 131c2 of the compensating TFT T3 of the (sub) pixel P1 may be affected by different electric signals transmitted by the data line 171 of the (sub) pixel P2 according to time while the (sub) pixel P1 emits light. Because the compensating TFT T3 is electrically coupled to the driving TFT T1, if the electric potential of the part 131c2 of the compensating TFT T3 of the (sub) pixel P1 is affected by the different electric signals transmitted by the data line 171 of the (sub) pixel P2, the luminance of the organic light-emitting device OLED determined by the driving TFT T1 may become different from an initial intension, and thus quality of an image displayed by the organic light-emitting display apparatus may deteriorate.

[0082] However, according to the organic light-emitting display apparatus of some embodiments, because the first shield layer SD1 is disposed between the data line 171 of the (sub) pixel P2 and the part 131c2 of the compensating TFT T3 of the (sub) pixel P1, the part 131c2 of the compensating TFT T3 of the (sub) pixel P1 may not be affected or may be less affected by the data line 171 of the (sub) pixel P2, and thus the organic light-emitting display apparatus may be able to display an image having a more accurate luminance and a relatively higher quality. For example, if the first shield layer SD1 is a part of the second storage capacitor plate 127, the second storage capacitor plate 127 is connected to the driving voltage line 172 always having uniform electric

potential, through the contact hole 168, and thus the first shield layer SD1 may also always have a uniform electric potential. Accordingly, an effect of an adjacent electric
5 signal on the part 131c2 of the compensating TFT T3 may be reduced.

[0083] Alternatively, the first shield layer SD1 may extend below the data line 171 of the (sub) pixel P2 as shown in FIG. 8 that is a cross-sectional view of an organic light-emitting display apparatus according to some embodiments of the present invention. Accordingly, the part 131c2 of the compensating TFT T3 may be further shielded.

10 Here, the part 131c2 of the compensating TFT T3 may also be further shielded by extending the first shield layer SD1 above at least a part of the part 131c2 between the first and second gate electrodes 125c1 and 125c2 of the compensating TFT T3.

[0084] FIG. 9 is a cross-sectional view taken along the line IX-IX of FIG. 2. As shown in FIGS. 2, 5, and 9, the initialization voltage line 124 may include a second
15 shield layer SD2.

[0085] As shown in FIGS. 2 and 5, the second shield layer SD2 may be a part of the initialization voltage line 124, which extends along an x-axis. The second shield layer SD2 may be understood to be a part of the initialization voltage line 124, which extends between the data line 171 and at least a part between first gate electrode 125d1 and a
20 second gate electrode 125d2 of the initialization gate electrode 125d1 and 125d2 of the initialization TFT T4.

[0086] In FIGS. 2 and 5, the initialization voltage line 124 extends above the part between the first and second gate electrodes 125d1 and 125d2 of the initialization TFT T4, but an embodiment is not limited thereto. If the initialization voltage line 124 has
25 another location or another shape, for example, is moved in a +y direction, a -y direction, or another direction, or is curved, the initialization voltage line 124 may have a protrusion and the protrusion may extend between the data line 171 and at least a part between the first and second gate electrodes 125d1 and 125d2 of the initialization TFT T4 to operate as the second shield layer SD2. In other words, in FIGS. 2 and 5,

the initialization voltage line 124 may extend along an x-axis direction while passing between the data line 171 and at least the part between the first and second gate electrodes 125d1 and 125d2 of the initialization TFT T4, such that a location of the initialization voltage line 124 is specified without having to include the protrusion.

[0087] If the second shield layer SD2 does not exist, the components between the first and second gate electrodes 125d1 and 125d2 of the initialization TFT T4, for example, a part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 may be affected by the data line 171.

[0088] The data line 171 transmits a data signal to the (sub) pixel of FIG. 2, and also transmits a data signal to a plurality of (sub) pixels disposed near the (sub) pixel of FIG. 2 in +y and -y directions. Here, a data signal being transmitted may vary according to luminance to be realized by the plurality of (sub) pixels disposed near the (sub) pixel of FIG. 2 in the +y and -y directions, and accordingly, the data line 171 near the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 of the (sub) pixel of FIG. 2 transmits different electric signals according to time while the (sub) pixel of FIG. 2 emits light.

[0089] If the second shield layer SD2 does not exist, parasitic capacitance may occur between the data line 171 and the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 of the initialization TFT T4, and thus electric potential of the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 of the initialization TFT T4 may be affected by the different electric signals transmitted by the data line 171, according to time while the (sub) pixel of FIG. 2 emits light. Because the initialization TFT T4 is electrically coupled to the driving TFT T1, if the electric potential of the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 of the initialization TFT 4 is affected by the different electric signals transmitted by the data line 171, the luminance of the organic light-emitting device OLED determined by the driving TFT T1 may become different from an initial intention, and

thus quality of an image displayed by the organic light-emitting display apparatus may deteriorate.

[0090] However, according to the organic light-emitting display apparatus of some embodiments, because the second shield layer SD2 is arranged between the data line 171 and the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 of the initialization TFT T4, the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 of the initialization TFT T4 may not be affected or may be less affected by the data line 171, and thus the organic light-emitting display apparatus may be able to display an image having a more accurate luminance and a relatively higher quality. For example, if the second shield layer SD2 is a part of the initialization voltage line 124, the second shield layer SD2 may always have a uniform electric potential by the initialization voltage line 124 that always has uniform electric potential. Accordingly, an effect of an adjacent electric signal on the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 of the initialization TFT T4 may be reduced.

[0091] Here, if a layout of various wires or a semiconductor layer differs from that shown in FIG. 2, the second shield layer SD2 may be a part extending at least above the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 between the first and second gate electrodes 125d1 and 125d2 of the initialization TFT T4, or a part extending below the data line 171.

[0092] FIG. 10 is a cross-sectional view taken along the line X-X of FIG. 2. As shown in FIGS. 2, 5, and 10, the second storage capacitor plate 127 may include a third shield layer SD3.

[0093] As shown in FIGS. 2 and 5, the third shield layer SD3 may be a part of the second storage capacitor plate 127. The third shield layer SD3 may be understood to be a part of the second storage capacitor plate 127, which extends between the data line 171 and the driving gate electrode 125a of the driving TFT T1. For example, the

second storage capacitor plate 127 may have a (virtual) end in the -x direction, which approximately match an end of the first storage capacitor plate 125a in the -x direction below the second storage capacitor plate 127, and the third shield layer SD3 may exist between the data line 171 and the driving gate electrode 125a of the driving TFT T1 in the -x direction from the (virtual) end, wherein the third shield layer SD3 may be understood to be integrally formed with the second storage capacitor plate 127.

[0094] Alternatively, unlike shown in FIGS. 2 and 5, the second storage capacitor plate 127 may not extend in the -x direction where the data line 171 is located due to nonexistence of the third shield layer SD3, and the end of the second storage capacitor plate 127 in the -x direction may approximately match the end of the first storage capacitor plate 125a in the -x direction. In this case, the driving gate electrode 125a of the driving TFT T1 is affected by the data line 171.

[0095] The data line 171 transmits a data signal to the (sub) pixel of FIG. 2, and also transmits a data signal to the plurality of (sub) pixels disposed in the +y and -y directions of the (sub) pixel. Here, the data signal being transmitted may vary according to the luminance to be realized by the plurality of (sub) pixels disposed in the +y and -y directions of the (sub) pixel of FIG. 2, and accordingly, the data line 171 near the part 131d2 of the initialization semiconductor layer 131d1, 131d2, and 131d3 of the (sub) pixel of FIG. 2 may transmit different electric signals according to time while the (sub) pixel of FIG. 2 emits light.

[0096] If the third shield layer SD3 does not exist and thus the second storage capacitor plate 127 does not extend in the -x direction where the data line 171 is disposed and the end of the second storage capacitor plate 127 in the -x direction approximately matches the end of the first storage capacitor plate 125a in the -x direction, parasitic capacitance exists between the data line 171 and the driving gate electrode 125a of the driving TFT T1, and accordingly, electric potential of the driving gate electrode 125a of the driving TFT T1 is affected by the different electric signals

transmitted by the data line 171 according to time while the (sub) pixel of FIG. 2 emits light. As a result, the luminance of the organic light-emitting device OLED determined
5 by the driving TFT T1 may become different from an initial intension, and thus quality of an image displayed by the organic light-emitting display apparatus may deteriorate.

[0097] However, according to the organic light-emitting display apparatus of the current embodiment, because the third shield layer SD3 exists between the data line 171 and the driving gate electrode 125a of the driving TFT T1, the driving gate
10 electrode 125a of the driving TFT T1 may not be affected or may be less affected by the data line 171, and thus the organic light-emitting display apparatus may be able to display an image having a more accurate luminance and a relatively higher quality. For example, if the third shield layer SD3 is a part of the second storage capacitor plate 127, the second storage capacitor plate 127 is coupled to the driving voltage line 172
15 always having uniform electric potential, through the contact hole 168, and thus the third shield layer SD3 may also always have a uniform electric potential. Accordingly, an effect of an adjacent electric signal on the driving gate electrode 125a of the driving TFT T1 may be reduced.

[0098] Of course, the third shield layer SD3 may not only be disposed between the
20 data line 171 and the driving gate electrode 125a, and may also extend below the data line 171 as shown in FIG. 10. Accordingly, the driving gate electrode 125a of the driving TFT T1 may be further shielded.

[0099] Hereinabove, the organic light-emitting display apparatus may include the first shield layer SD1, the second shield layer SD2, and the third shield layer SD3, but
25 alternatively, the organic light-emitting display apparatus may include only some of the first through third shield layers SD1 through SD3. In other words, the organic light-emitting display apparatus may include at least any one of the first through third shield layers SD1 through SD3.

[00100] In the above embodiments, the compensating TFT T3 and the initialization TFT T4 include a dual gate electrode. However, an embodiment is not limited thereto and the organic light-emitting display apparatus may include the first or second shield layer SD1 or SD2 disposed between the data line 171 and a part of the compensating TFT T3 and/or the initialization TFT T4, even if the compensating TFT T3 and the initialization TFT T4 include a single gate electrode.

[00101] Meanwhile, all of the first through third shield layers SD1 through SD3 are included in the second gate wire as shown in FIGS. 2 and 5, but an embodiment is not limited thereto. In other words, the first through third shield layers SD1 through SD3 may be a part of the second storage capacitor plate 127 or a part of the initialization voltage line 124.

[00102] FIG. 11 is a schematic diagram showing locations of a plurality of TFTs and a capacitor in a (sub) pixel of an organic light-emitting display apparatus, according to another embodiment of the present invention, and FIG. 12 is a cross-sectional view taken along the line XII-XII of FIG. 11. Differences between the organic light-emitting display apparatuses of FIGS. 2 and 11 are shapes of the previous scan lines 122, the initialization voltage lines 124, and the initialization TFTs T4.

[00103] Referring to FIGS. 11 and 12, the initialization voltage line may be arranged in the same layer as the second storage capacitor plate 127, or in the same layer as a pixel electrode. The initialization voltage line may be coupled to the initialization source electrode 176d of the initialization TFT T4 through the contact hole 162. As described above with reference to FIG. 2, the initialization drain electrode 177d of the initialization TFT T4 is electrically coupled to the compensating drain electrode 177c of the compensating TFT T3 and the driving gate electrode 125a of the driving TFT T1.

[00104] The previous scan line 122 that may be arranged in the same layer as the driving gate electrode 125a, the scan line 121, and the emission control line 123 may include two protrusions corresponding to a location of the initialization TFT T4. Here,

the two protrusions may be the first and second gate electrodes 125d1 and 125d2 of the initialization TFT T4. At least a part of the second gate electrode 125d2 may be the second shield layer SD2.

[00105] A dual gate electrode may have two parts overlapping a semiconductor layer. For example, referring to FIG. 11, the second gate electrode 125d2 of the initialization TFT T4 may be a part of the previous scan line 122 extending along an x-axis without having to protrude from the previous scan line 122, and a part 125d2' of the first gate electrode 125d1 in the -x direction, which crosses a semiconductor layer near the initialization source electrode 176d, may operate as a second gate electrode. However, in this case, a part between a part of the semiconductor layer corresponding to the part 125d2' and a part of the semiconductor layer corresponding to the first gate electrode 125d1 is arranged adjacent to the data line 171 and is not shielded, and thus may be affected by the data line 171.

[00106] However, according to the organic light-emitting display apparatus of the some embodiments, the previous scan line 122 includes the two protrusions, wherein one of the protrusions operates as the first gate electrode 125d1 and the other one of the protrusions protrudes from the part 125d2' of the previous scan line 122 and operates as the second gate electrode 125d2. Here, the second gate electrode 125d2 shields the part between the part of the semiconductor layer corresponding to the part 125d2' and the part of the semiconductor layer corresponding to the first gate electrode 125d1 from the data line 171, and thus an unintended effect on the initialization TFT T4 from the data line 171 may be effectively blocked or reduced.

[00107] According to the initialization TFT T4 having such a structure, the initialization TFT T4 includes the first and second gate electrodes 125d1 and 125d2, and one of the first and second gate electrodes 125d1 and 125d2 is at least partially disposed between the data line 171 and the semiconductor layer 131d2 that is a part between the source electrode 176d and the other of the first and second gate

electrodes 125d1 and 125d2 of the initialization TFT T4. In FIGS. 11 and 12, the second gate electrode 125d2 is at least partially disposed between the data line 171 and the semiconductor layer 131d2 that is the part between the source electrode 176d and the first gate electrode 125d1 of the initialization TFT T4, and thus the semiconductor layer 131d2 is shielded from the data line 171. In other words, the second gate electrode 125d2 is shown to be the second shield layer SD2. Here, the second gate electrode 125d2 may not only be arranged between the data line 171 and the semiconductor layer 131d2 as shown in FIGS. 11 and 12, but may also extend below the data line 171 in the -x direction. In FIG. 12, the data line 171 is arranged above the second gate electrode 125d2, but if the data line 171 is arranged below the semiconductor layer 131d2 and the second gate electrode 125d2 is arranged between the data line 171 and the semiconductor layer 131d2, the second gate electrode 125d2 may extend above the data line 171.

[00108] As such, the second shield layer SD2 may be formed as the second gate wire as described above with reference to FIGS. 2, 5, and 9, but may alternatively be formed as the first gate wire as described with reference to FIGS. 11 and 12. If the first or third shield layer SD1 or SD3 is included as well as the second shield layer SD2, the first or third shield layer SD1 or SD3 may be formed as the first gate wire. In this case, the first or third shield layer SD1 or SD3 may not be electrically coupled to the second storage capacitor plate 127, but may have an island shape and electrically float.

[00109] Hereinabove, it is described that the parts of the driving TFT T1, the compensating TFT T3, and the initialization TFT T4 are shielded from the data line 171, but an embodiment is not limited thereto. In other words, if a TFT of a (sub) pixel of an organic light-emitting display apparatus is near the data line 171, a shield layer may be disposed between the data line 171 and at least a part of the TFT such that the organic light-emitting display apparatus displays an image having high quality. The shield layer may be arranged at least one of between the data line 171 and a source

electrode of the TFT, between the data line 171 and a drain electrode of the TFT, and between the data line 171 and a gate electrode of the TFT.

5 **[00110]** Meanwhile, hereinabove, it is described that a shield layer is arranged between a data line and a part of a TFT, but an embodiment is not limited thereto. For example, an organic light-emitting display apparatus may include a TFT that includes a source electrode, a drain electrode, and a gate electrode, a control signal line that is arranged in a layer different from the source electrode, the drain electrode, and the gate electrode and transmits a control signal, and a shield layer that is arranged
10 between the control signal line and at least a part of the TFT. Here, the control signal line may be at least any one of the plurality of signal lines described above. In other words, the control signal line may be the scan line 121, the previous scan line 122, the emission control line 123, the data line 171, the driving voltage line 172, or the
15 initialization voltage line 124. The shield layer may shield the at least the part of the TFT from the control signal line so as to block or reduce an effect of a control signal transmitted from the control signal line on the TFT.

[00111] An embodiment of the present is not limited to an organic light-emitting display apparatus. An image having high quality may be displayed as long as a display
20 apparatus including a TFT and a data line in a (sub) pixel has a shield layer in the same or similar manner described above.

[00112] As described above, according to one or more embodiments of the present invention, a display apparatus capable of preventing quality deterioration of a displayed image may be realized.

25 **[00113]** While one or more embodiments of the present invention have been described with reference to the figures, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims, and their equivalents.

WHAT IS CLAIMED IS:

- 5 1. A display apparatus comprising:
a thin-film transistor comprising a source electrode, a drain electrode, and a
gate electrode;
a data line in a layer different from the source electrode, the drain electrode, and
the gate electrode, wherein the data line is configured to transmit a data signal; and
10 a shield layer between the data line and a component of the thin-film transistor.

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ABSTRACT

5 A display apparatus includes: a thin-film transistor including a source electrode,
a drain electrode, and a gate electrode; a data line in a layer different from the source
electrode, the drain electrode, and the gate electrode, wherein the data line is
configured to transmit a data signal; and a shield layer between the data line and a
10 component of the thin-film transistor.

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FIG. 1

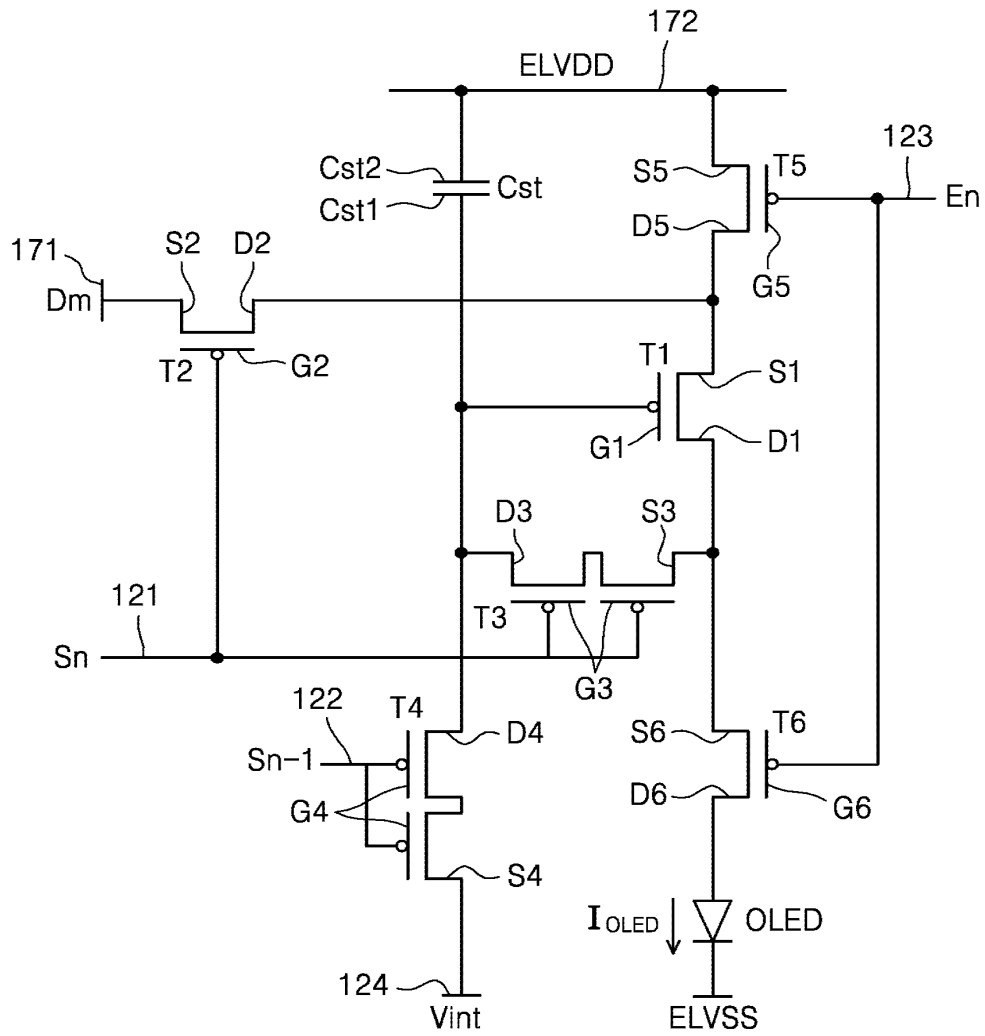


FIG. 2

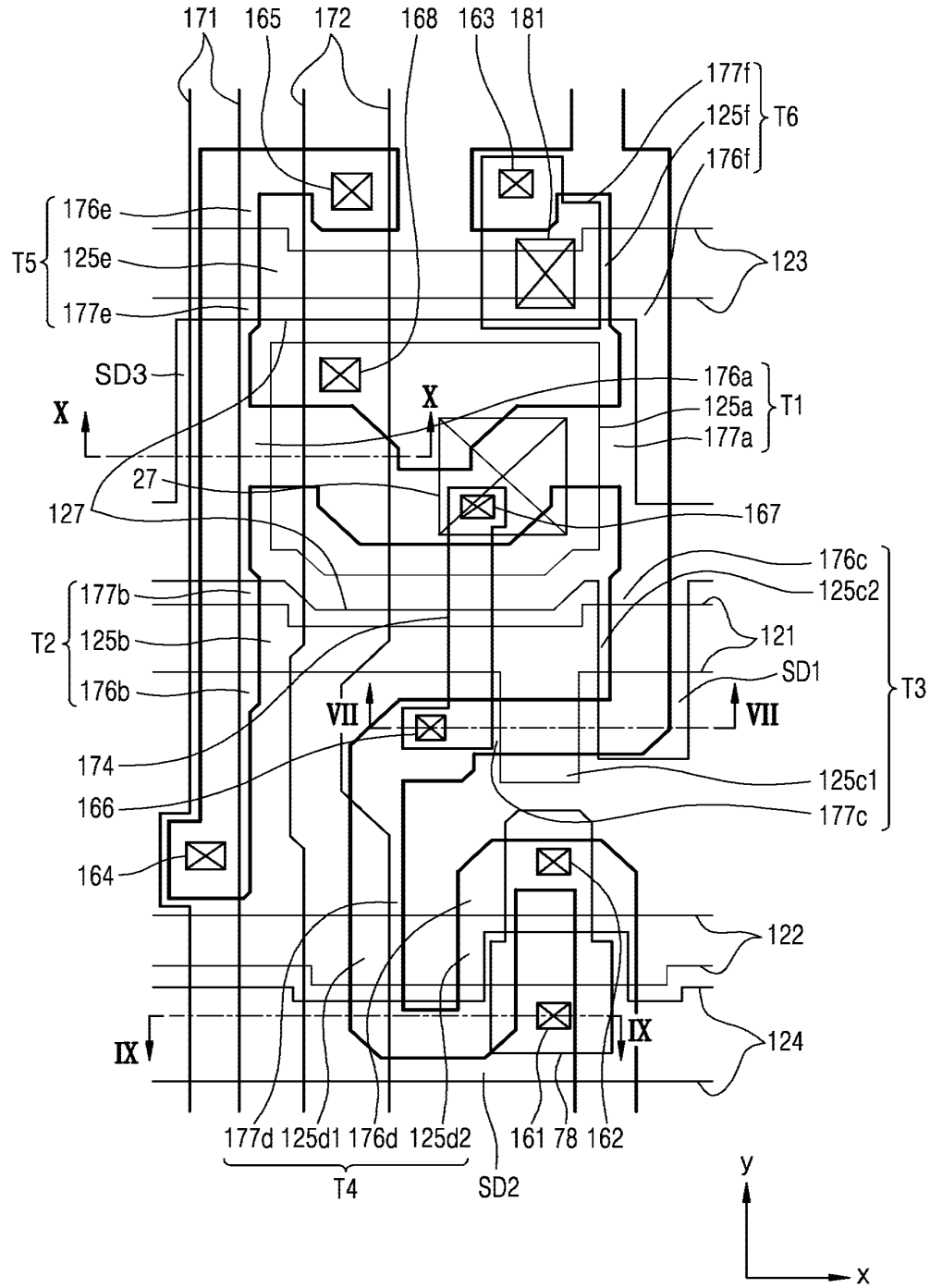


FIG. 3

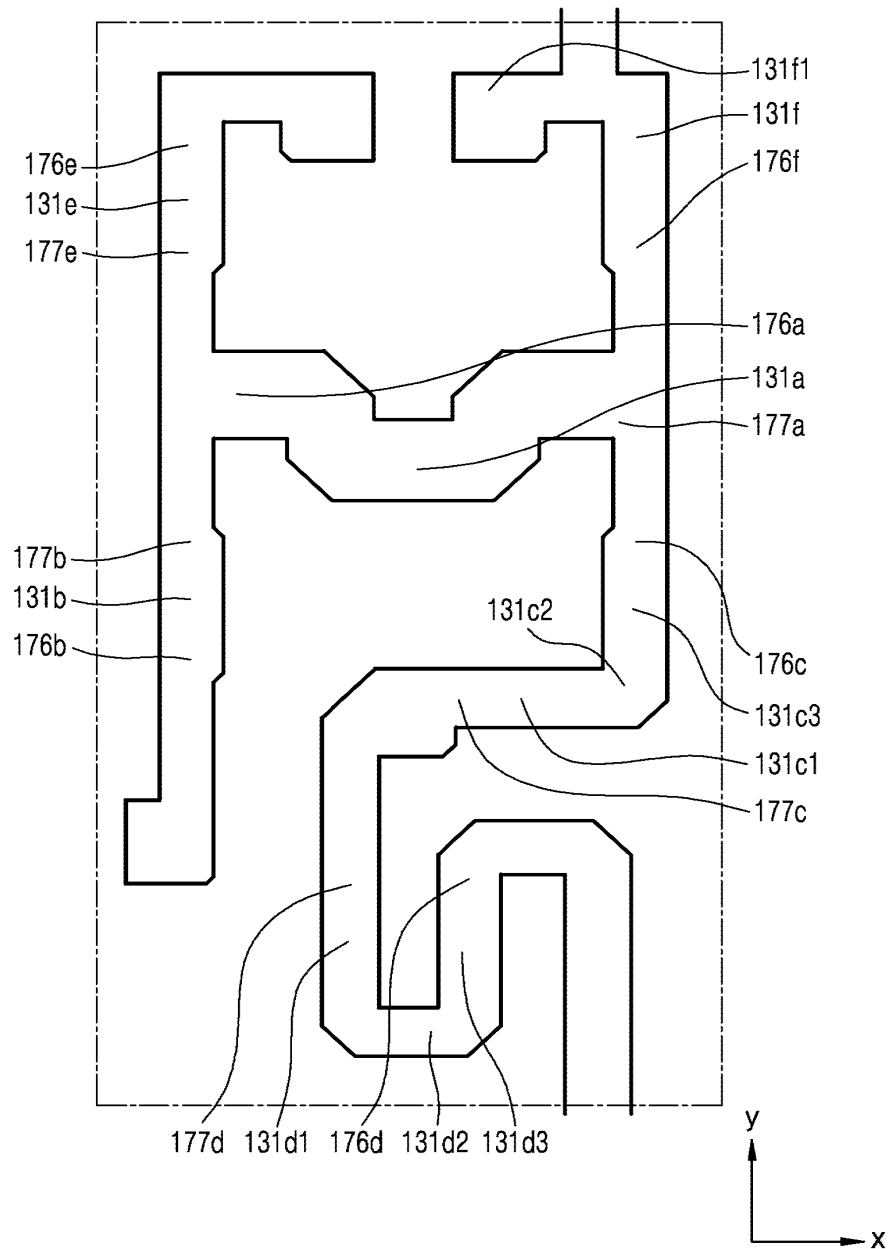


FIG. 4

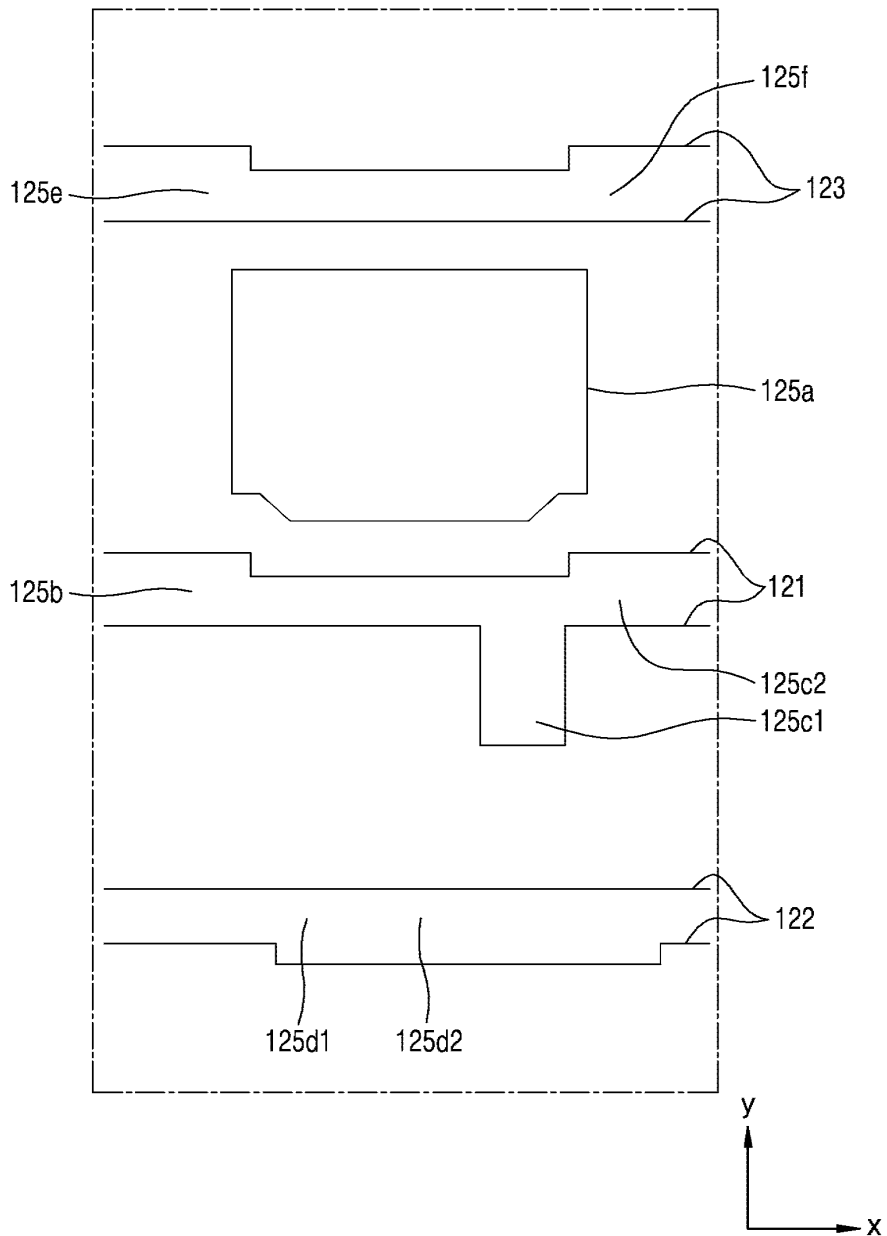


FIG. 5

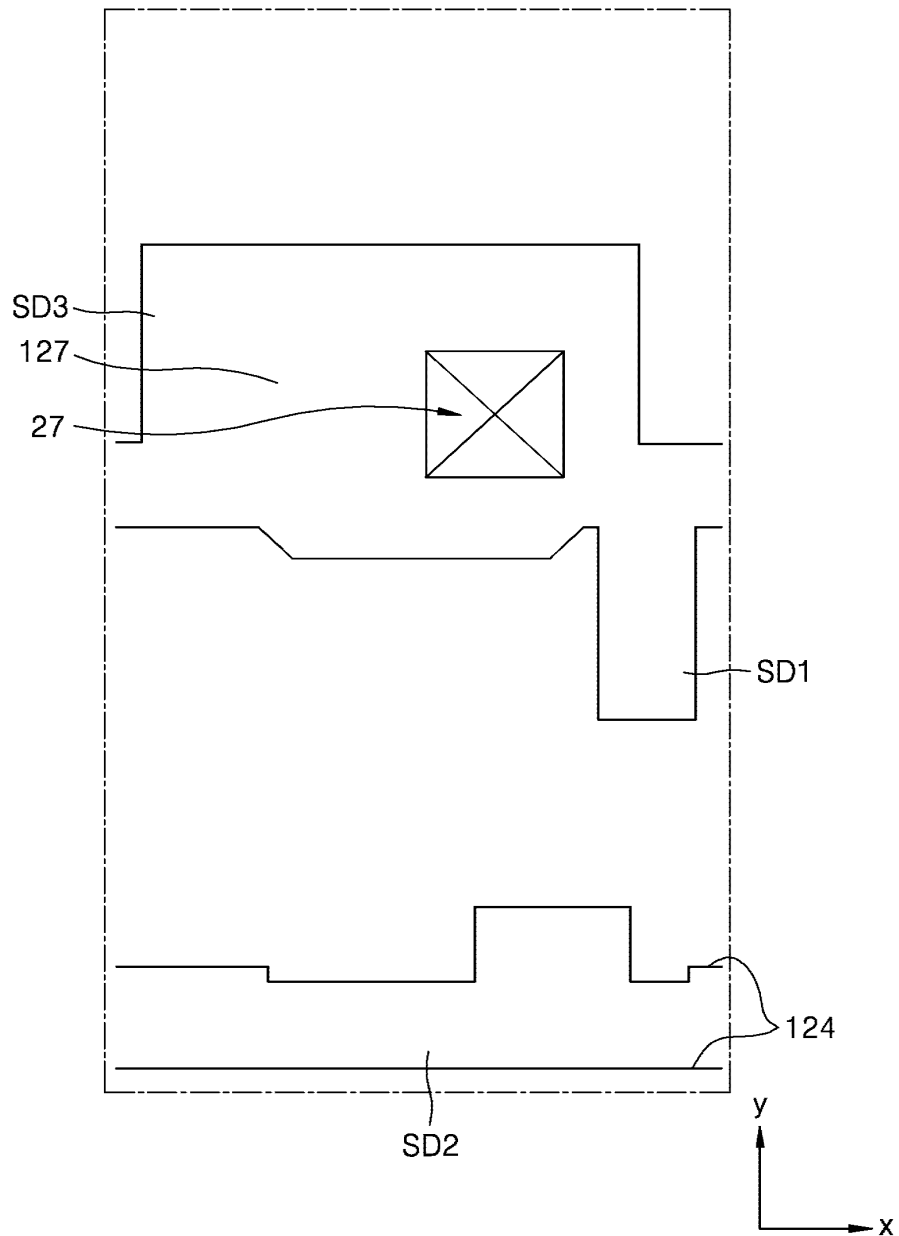


FIG. 6

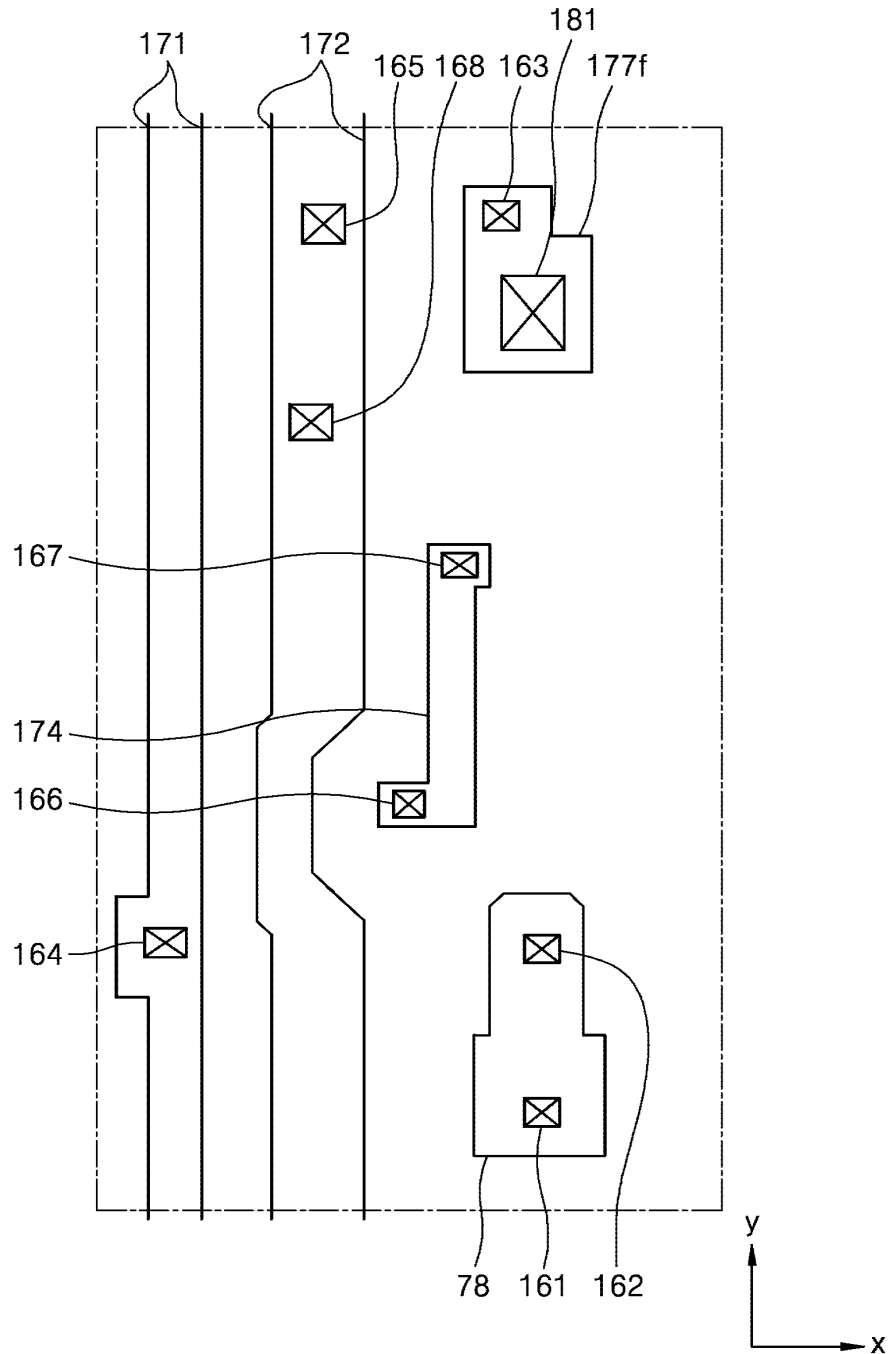


FIG. 9

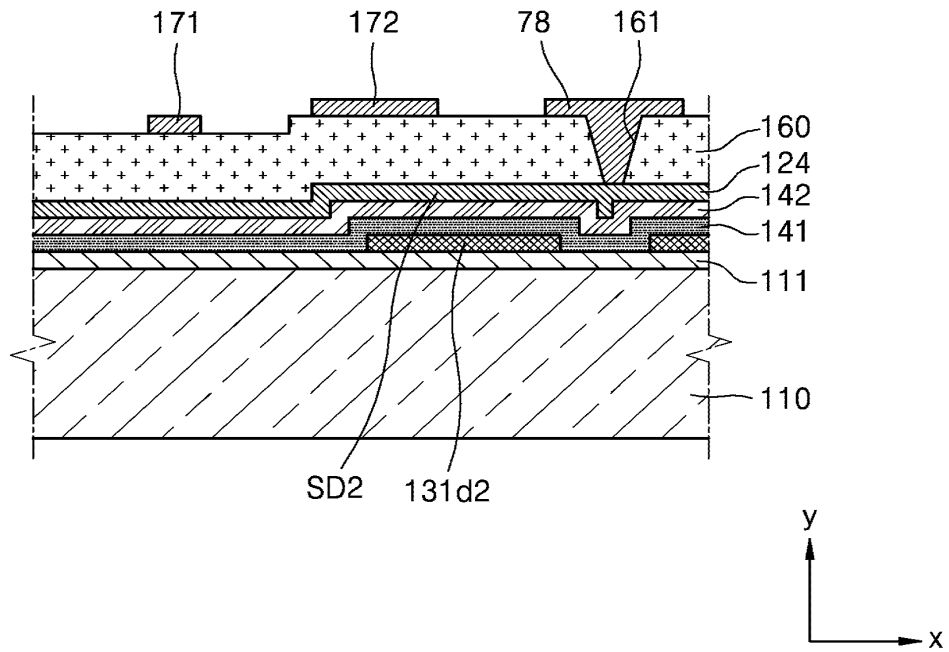


FIG. 10

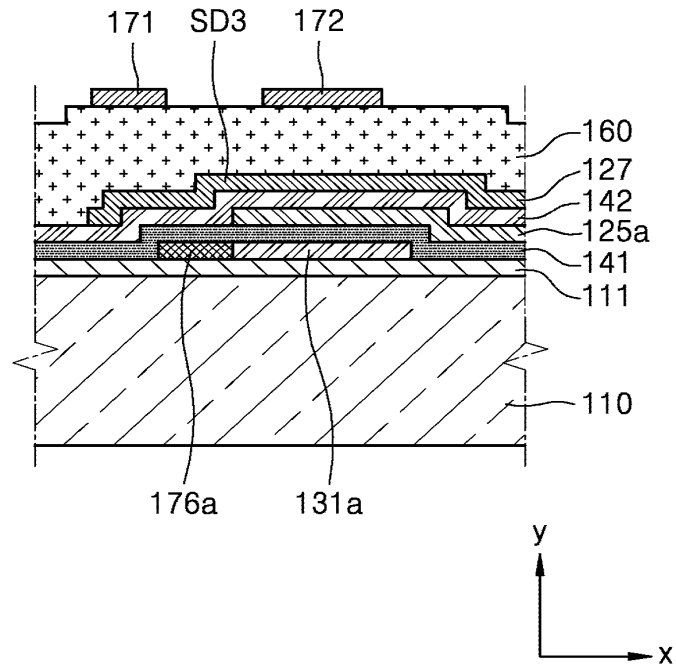


FIG. 11

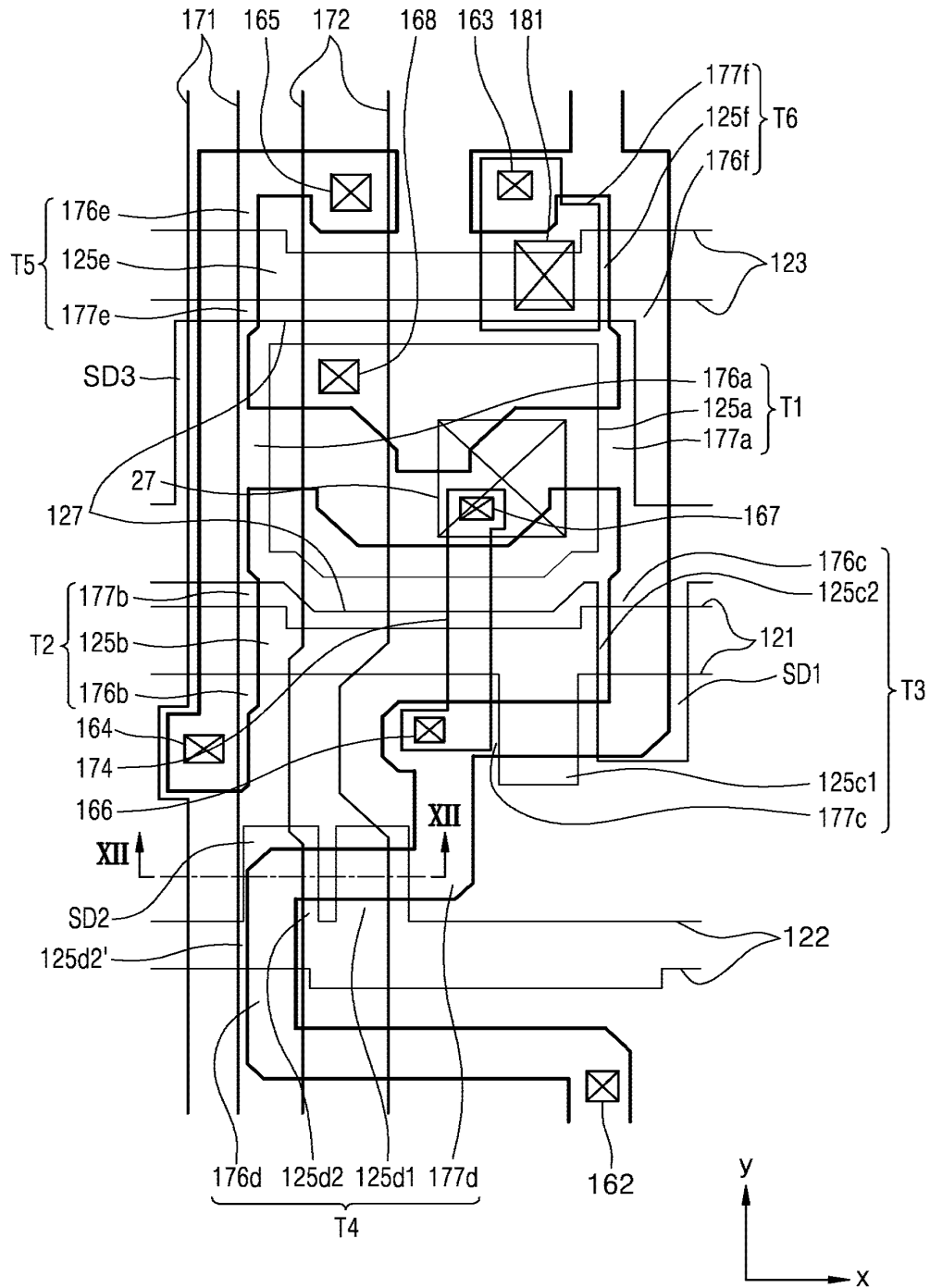
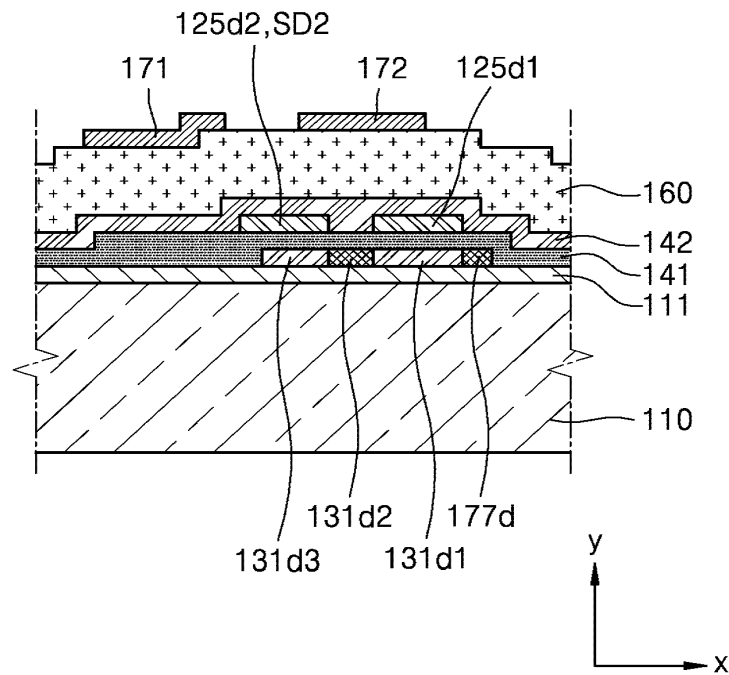


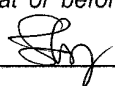
FIG. 12



PATENT

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Si Vuong

Inventor(s) : Yangwan Kim, et al.
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Filed : December 11, 2017
Title : DISPLAY APPARATUS
Grp./Div. : To Be Determined
Examiner : To Be Determined
Docket No. : 148454

**INFORMATION DISCLOSURE STATEMENT
FOR A CONTINUING NON-CPA APPLICATION**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
December 11, 2017

Commissioner:

In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, enclosed is an information disclosure statement. The references listed thereon are not enclosed because they were of record in the parent application, Application No. 14/660,813, filed March 17, 2015.

It is respectfully requested that these references be considered in the examination of this application, and identified in the list of references cited on the patent issuing on this application. Applicant also requests that an initialed copy of the information disclosure statement be entered in the application file and returned to applicant with the next communication from the Office in accordance with MPEP § 609.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By 

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626/795-9900

PCH/smv
Information Disclosure Statement

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