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(71) Applicant Yungu (Gu'an) Technology Co., Ltd.

Address: 065500 Emerging Industry Demonstration Zone, Gu'an County, Langfang
City, Hebei Province

(72) Inventors: Tian Miaomiao, Ma Zhili, Zhao Hong, Pang Yugan

Zhu Zhengyong

(74) Patent Agency Beijing Yuanzhahui Intellectual Property Agency

Co., Ltd. 11659

Agent Fan Kunkun

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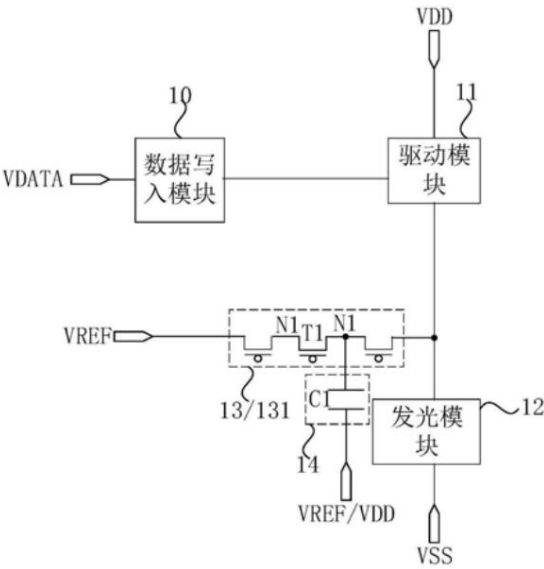
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(54) Invention Name:

Pixel Circuit and Display Panel (57)

Abstract: The

present invention discloses a pixel circuit and a display panel, wherein the pixel circuit includes a data writing module, a driving module, a light-emitting module, a first initialization module, and a first shielding module. The first end of the first initialization module is connected to the initialization signal line, the second end of the first initialization module is connected to the first end of the light-emitting module, the first initialization module includes a first multi-gate transistor, the first multi-gate transistor includes at least two first sub-transistors connected in series, and adjacent first sub-transistors are electrically connected through a first intermediate node between the two. The first shielding module includes at least one first shielding capacitor, and the first end of the first shielding capacitor is connected to the first intermediate node. The more the number of first sub-transistors, the smaller the leakage current of the first initialization module, thereby reducing the potential change of the first end of the light-emitting module. The first shielding capacitor can stabilize the potential of the first intermediate node, thereby reducing the leakage current of the first multi-gate transistor, which is beneficial to display uniformity.



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1. A pixel circuit, comprising: a data writing module, a driving module, a light emitting module, a first initialization module, and a first shielding module;

The data writing module is used to write data signals to the control end of the driving module under the control of the signal received by its own control end; the driving module and the light emitting module are connected between

the first power line and the second power line, and the driving module is used to write data signals to the control end of the driving module under the control of the signal received by its own control end; outputting a driving signal according to the data signal to drive the light-emitting module to emit light;

A first end of the first initialization module is connected to an initialization signal line, and a second end of the first initialization module is connected to a first end of the light-emitting module. The first initialization module is configured to write an initialization voltage to the first end of the light-emitting module under control of a signal connected to its control end. The first initialization module includes a first multi-gate transistor, which includes at least two first sub-transistors connected in series, with adjacent first sub-transistors electrically connected via a first intermediate node therebetween.

The first shielding module includes at least one first shielding capacitor, a first end of the first shielding capacitor is connected to at least one first intermediate node, and a second end of the first shielding capacitor is connected to a fixed voltage.

The first shielding capacitor is electrically connected to the initialization signal line, or the second end of the first shielding capacitor is electrically connected to the first power line.

3. The pixel circuit according to claim 1, characterized in that the line width of the active layer of the first multi-gate transistor is less than a first set threshold value; preferably, the driving module includes

a driving transistor, and the first set threshold value is equal to the line width of the active layer of the driving transistor. 4. The pixel circuit according to claim 1, characterized in that it

also includes a second initialization module and a second shielding module; the first end of the second initialization module is connected to the initialization signal line, the

second end of the second initialization module is connected to the control end of the driving module, and the second initialization module is used to write the initialization voltage to the control end of the driving module under the control of the signal connected to its own control end; the second initialization module includes a second multi-gate transistor, the second multi-gate transistor includes at least two second sub-transistors connected in series, and adjacent second sub-transistors are electrically connected through a second intermediate node therebetween; the second shielding module includes at least one second shielding capacitor, the first end of the second shielding capacitor is connected to at least one second intermediate node, and the

second end of the second shielding capacitor is connected to a fixed voltage; preferably, the second end of the second shielding capacitor is electrically connected to the initialization signal line, or the second shielding

The second end of the capacitor is electrically connected to the first power line;

preferably, the line width of the active layer of the second multi-gate transistor is less than the second set threshold; and/or, the pixel circuit further includes a compensation module and a third shielding module, the compensation module is used to control the pixel circuit to Compensating the threshold voltage of the driving transistor included in the driving module under the control of the signal connected to the terminal;

The compensation module includes a third multi-gate transistor, the third multi-gate transistor includes at least two third sub-transistors connected in series, and adjacent third sub-transistors are electrically connected via a third intermediate node therebetween; the third shielding module includes at least

one third shielding capacitor, a first end of the third shielding capacitor is connected to at least one third intermediate node, and a second end of the third shielding capacitor is connected to a fixed voltage; preferably, the second end of the third shielding capacitor is electrically connected to the

initialization signal line, or the third shielding module is electrically connected to the initialization signal line.

The second end of the capacitor is electrically connected to the first power line.

5. A display panel, characterized in that it includes the pixel circuit according to any one of claims 1-4, and further includes a first power line, a data line, an initialization signal line, a first scan line and a second scan line, the first power line and the data line extend along a first direction, the initialization signal line, the first scan line and the second scan line extend along a second direction, and the first direction and the second direction intersect; Preferably, the pixel circuits are arranged in

an array, the first direction is the column direction of the pixel circuits, the second direction is the row direction of the pixel circuits, the control end of the first initialization module in each row of the pixel circuits is connected to the same first scan line, the first end of the first initialization module of each row of the pixel circuits is connected to the same initialization signal line, the control end of the data write module of each row of the pixel circuits is connected to the same second scan line, the first end of the data write module of each column of the pixel circuits is connected to the same data line, and the pixel circuits in each column are connected to the same first power line; the first scan line connected to the pixel circuits in the same row is located between the initialization signal line and the second scan line.

6. The display panel according to claim 5, wherein at least one of the first intermediate nodes of the first multi-gate transistor overlaps with the first fixed potential structure to form at least one first shielding capacitor, and the first intermediate node of the first multi-gate transistor comprises a first active portion in the active layer of the first multi-gate transistor that connects to an adjacent first sub-transistor;

Preferably, the first active portion includes the first scan line and the first active portion electrically connected to the same pixel circuit.
a first sub-active portion between the second scan lines;

The first fixed potential structure includes the first scanning line electrically connected to the same pixel circuit,
a first fixed potential portion between the second scan lines, the first fixed potential portion being electrically connected to the first power line;

The first fixed potential portion overlaps with the first sub-active portion to form a first shielding capacitor. 7. The display panel according to claim 6, wherein the data line and the first power line are arranged along the second direction, and the first multi-gate transistor is located on a side of the first power line connected to the pixel circuit to which the first multi-gate transistor belongs, away from the data line;

The first fixed potential structure further includes a first connecting portion connecting the first power line and the first fixed potential portion, the first connecting portion extending along the second direction, and in the same pixel circuit, the first sub-active portion is located on a side of the first connecting portion closer to the first scan line to which the pixel circuit is connected. 8. The display panel according

to claim 6, wherein the first multi-gate transistor includes at least three first sub-transistors connected in series, the first active portion includes a second sub-active portion located on a side of the first scan line away from the second scan line; the second sub-active portion overlaps with the initialization signal line to form a

first shielding capacitor; preferably, the pixel circuit includes a second connecting portion, the second connecting portion extending along the first direction, one end of the second connecting portion connected to the initialization signal line and the other end connected to the first electrode of the first multi-gate transistor, and the second electrode of the first multi-gate transistor connected to the first end of the light-emitting module.

9. The display panel according to claim 7, wherein the pixel circuit further comprises a compensation module and a third shielding module, the compensation module comprising a third multi-gate transistor, the third multi-gate transistor comprising at least two third sub-transistors connected in series, at least one third intermediate node of the third multi-gate transistor overlapping with a third fixed potential structure to form at least one third shielding capacitor, and the third intermediate node of the third multi-gate transistor comprising a third active portion in an active layer of the third multi-gate transistor connecting adjacent third sub-transistors;

Preferably, the third active portion includes at least one third sub-active portion between the first scan line and the second scan line connected to the same pixel circuit, and the third fixed potential structure includes at least one third fixed potential

part, the third fixed potential part is connected to the first connecting part, and in the same pixel circuit, the third sub-active part and the third fixed potential part are located on the side of the first connecting part close to the second scanning line connected to the pixel circuit, and the third sub-active part overlaps with the corresponding third fixed potential part to form the third shielding capacitor.

10. The display panel according to claim 5 or 6, characterized in that the pixel circuit further comprises a second initialization module and a second shielding module; the second initialization module comprises a second multi-gate transistor, the second multi-gate transistor comprises at least two second sub-transistors connected in series, at least one second intermediate node of the second multi-gate transistor overlaps with the second fixed potential structure to form at least one second shielding capacitor, and the second intermediate node of the second multi-gate transistor comprises a second active portion in the active layer of the second multi-gate transistor connecting adjacent second sub-transistors;

preferably, the second active portion comprises a portion located away from the first scan line connected to the same pixel circuit at least one fourth sub-active portion on one side of the second scan line; the

fourth sub-active portion overlaps with the initialization signal line to form a second shielding capacitor; preferably, the pixel circuit includes a third connection portion and a fourth connection portion, the third connection portion and the fourth connection portion both extending along the first direction, one end of the third connection portion connected to the initialization signal line, and the other end connected to the first electrode of the second multi-gate transistor, one end of the fourth connection portion connected to the second electrode of the second multi-gate transistor, and the other end connected to the control end of the driving module; preferably,

the third connection portion and the second connection portion have the same structure;

preferably, the second multi-gate transistor includes at least three second sub-transistors connected in series, and the second active portion includes a fifth sub-active portion located between the first scan line and the second scan line electrically connected to the same pixel circuit; the second fixed potential structure includes

a fifth sub-active portion located between the first scan line, the first scan line and the second scan line electrically connected to the same pixel circuit. A second fixed potential portion is provided between the second scan lines, and is electrically connected to the first power line. The second fixed potential portion overlaps with the fifth sub-active portion to form a second shielding capacitor.

Pixel circuit and display panel

Technical Field

[0001] The embodiments of the present invention relate to the field of display technology, and in particular to a pixel circuit and a display panel.

BACKGROUND

[0002] With the development of display products and the increasing demand for high refresh rates, low grayscale display performance has become increasingly important in display products. [0003] Current display panels typically include multiple pixel circuits. When displaying at low grayscale, existing display panels are prone to uneven light emission, which affects the display quality.

SUMMARY OF

THE INVENTION [0004] The present invention provides a pixel circuit and a display panel to reduce leakage of a first initialization module, improve display uniformity, and enhance display quality. [0005] In

a first aspect, an embodiment of the present invention provides a pixel circuit, comprising: a data writing module, a driving module, a light-emitting module, a first initialization module and a first shielding module; [0006] the data writing module is used to write a data signal to the control end of the driving module under the control of a signal connected to its own control end; [0007] the driving module and the

light-emitting module are connected between a first power line and a second power line, and the driving module is used to output a driving signal according to the data signal to drive the light-emitting module to emit light; [0008] the first

end of the first initialization module is connected to the initialization signal line, the second end of the first initialization module is connected to the first end of the light-emitting module, and the first initialization module is used to write an initialization voltage to the first end of the light-emitting module under the control of a signal connected to its own control end; the first initialization module includes a first multi-gate transistor, the first multi-gate transistor includes at least two first sub-transistors connected in series, and adjacent first sub-transistors are electrically connected via a first intermediate node therebetween; [0009] the first shielding module includes at least one first shielding capacitor, the first end of the first shielding capacitor is connected to at least one intermediate node, and the second end of the first shielding capacitor is connected to a fixed voltage. [0010]

Optionally, the second end of the first shielding capacitor is electrically connected to the initialization signal line, or the second end of the first shielding capacitor is electrically connected to the first power line.

[0011] Optionally, the line width of the active layer of the first multi-gate transistor is less than the first set threshold; [0012]

Optionally, the driving module includes a driving transistor, and the first set threshold is equal to the line width of the active layer of the driving transistor. [0013]

Optionally, the pixel circuit also includes a second initialization module and a second shielding module; [0014] The first

end of the second initialization module is connected to the initialization signal line, and the second end of the second initialization module is connected to the control end of the driving module, and the second initialization module is used to write an initialization voltage to the control end of the driving module under the control of the signal connected to its own control end; the second initialization module includes a second multi-gate transistor, and the second multi-gate transistor includes at least two second sub-transistors connected in series, and adjacent second sub-transistors are electrically connected through a second intermediate node therebetween; [0015] The second shielding module includes at least one second shielding capacitor, the first end of the second shielding capacitor is connected to at least one second intermediate node, and the second end of the second shielding capacitor is connected to a fixed voltage;

[0016] Optionally, the second end of the second shielding capacitor is electrically connected to the initialization signal line, or the second end of the second shielding capacitor is electrically connected to the first power line;

[0017] Optionally, the line width of the active layer of the second multi-gate transistor is less than the second set threshold; [0018] And/or, the pixel circuit also includes a compensation module and a third shielding module, the compensation module is used to compensate for the threshold voltage of the driving transistor included in the driving module under the control of the signal connected to its own control end; [0019] The compensation module includes a third multi-gate transistor, the third multi-gate transistor includes at least two third sub-transistors connected in series, and adjacent third sub-transistors are electrically connected through a third intermediate node therebetween; [0020] The third shielding module includes at least one third shielding capacitor, the first end of the third shielding capacitor is connected to at least one third intermediate node, and the second end of the third shielding capacitor is connected to a fixed voltage; [0021] Optionally, the second end of the third shielding capacitor is electrically connected to the initialization signal line, or the second end of the third shielding capacitor is electrically connected to the first power line. [0022] In a second aspect, an embodiment of the present invention further provides a display panel, which includes the pixel circuit of any one of the first aspects, and also includes a first power line, a data line, an initialization signal line, a first scan line and a second scan line, the first power line and the data line extend along a first direction, the initialization signal line, the first scan line and the second scan line extend along a second direction, and the first direction and the second direction intersect; [0023] Optionally, the pixel circuits are arranged in an array, the first direction is the column direction of the pixel circuit arrangement, the second direction is the row direction of the pixel circuit arrangement, the control end of the first initialization module in each row of pixel circuits is connected to the same first scan line, the first end of the first initialization module of each row of pixel circuits is connected to the same initialization signal line, the control end of the data write module of each row of pixel circuits is connected to the same second scan line, the first end of the data write module of each column of pixel circuits is connected to the same data line, and each column of pixel circuits is connected to the same first power line; the first scan line connected to the pixel circuits in the same row is located between the initialization signal line and the second scan line. [0024] Optionally, at least one first intermediate node of the first multi-gate transistor overlaps with the first fixed potential structure to form at least one first shielding capacitor, and the first intermediate node of the first multi-gate transistor includes a first active portion in the active layer of the first multi-gate transistor connecting the adjacent first sub-transistors; [0025] Optionally, the first active portion includes a first sub-active portion located between a first scan line and a second scan line electrically connected to the same pixel circuit; [0026] The first fixed potential structure includes a first fixed potential portion located between a first scan line and a second scan line electrically connected to the same pixel circuit, and the first fixed potential portion is electrically connected to the first power line; [0027] The first fixed potential portion overlaps with the first sub-active portion to form a first shielding capacitor. [0028] Optionally, the data line and the first power line are arranged along the second direction, and the first multi-gate transistor is located on a side of the first power line connected to the pixel circuit to which the first multi-gate transistor belongs, away from the data line; [0029] The first fixed potential structure also includes a first connecting portion connecting the first power line and the first fixed potential portion, the first connecting portion extending along the second direction, and in the same pixel circuit, the first sub-active portion is located on a side of the first connecting portion close to the first scan line connected to the pixel circuit. [0030] Optionally, the first multi-gate transistor includes at least three first sub-transistors connected in series, the first active portion includes a second sub-active portion located on a side of the first scan line away from the second scan line; [0031] The second sub-active portion overlaps with the initialization signal line to form a first shielding capacitor; [0032] Optionally, the pixel circuit includes a second connecting portion, the second connecting portion extending along the first direction, one end of the second connecting portion connected to the initialization signal line, the other end connected to the first electrode of the first multi-gate transistor, and the second electrode of the first multi-gate transistor connected to the first electrode of the first multi-gate transistor.

[0033] Optionally, the pixel circuit

further includes a compensation module and a third shielding module, the compensation module including a third multi-gate transistor, the third multi-gate transistor including at least two third sub-transistors connected in series, at least one third intermediate node of the third multi-gate transistor overlapping with the third fixed potential structure to form at least one third shielding capacitor, the third intermediate node of the third multi-gate transistor including a third active portion in the active layer of the third multi-gate transistor connecting adjacent third sub-transistors; [0034] Optionally, the third active portion includes at least one third sub-active portion between a first scan line and a second scan line connected to the same pixel circuit, the third fixed potential structure including at least one third fixed potential portion, the third fixed potential portion connected to the first connecting portion, in the same pixel circuit, the third sub-active portion and the third fixed potential portion are located on a side of the first connecting portion close to the second scan line connected to the pixel circuit, and the third sub-active portion overlaps with the corresponding third fixed potential portion to form a third shielding capacitor. [0035] Optionally, the pixel circuit further includes

a second initialization module and a second shielding module; the second initialization module includes a second multi-gate transistor, the second multi-gate transistor includes at least two second sub-transistors connected in series, at least one second intermediate node of the second multi-gate transistor overlaps with the second fixed potential structure to form at least one second shielding capacitor, and the second intermediate node of the second multi-gate transistor includes a second active portion in the active layer of the second multi-gate transistor that connects adjacent second sub-transistors; [0036] Optionally, the

second active portion includes at least one fourth sub-active portion located on a side of the first scan line connected to the same pixel circuit away from the second scan line; [0037] the fourth sub-active portion

overlaps with the initialization signal line to form a second shielding capacitor; [0038] Optionally, the pixel circuit

includes a third connection portion and a fourth connection portion, the third connection portion and the fourth connection portion both extending along the first direction, one end of the third connection portion connected to the initialization signal line, and the other end connected to the first electrode of the second multi-gate transistor, one end of the fourth connection portion connected to the second electrode of the second multi-gate transistor, and the other end connected to the control end of the driving module; [0039] Optionally, the third connection portion

and the second connection portion have the same structure. [0040] Optionally, the second multi-gate transistor includes at least three second sub-transistors connected in series, and the second active portion includes a fifth sub-active portion located between a first scan line and a second

scan line electrically connected to the same pixel circuit; [0041] The second fixed potential structure includes a second fixed potential portion located between a first scan line and a second scan line electrically connected to the same pixel circuit, the second fixed

potential portion being electrically connected to the first power line; [0042] The second fixed potential portion and the fifth

sub-active portion overlap to form a second shielding capacitor. [0043] An embodiment of the present invention provides a pixel circuit and a display panel, the pixel circuit including a data writing module, a driving module, a light-emitting module, a first initialization module, and a first shielding module. The first initialization module is configured to write an initialization voltage to a first terminal of the light-emitting module under control of a signal connected to its control terminal. The first initialization module includes a first multi-gate transistor, the first multi-gate transistor including at least two first sub-transistors connected in series. Adjacent first sub-transistors are electrically connected via a first intermediate node therebetween. The first shielding module includes at least one first shielding capacitor, a first terminal of the first shielding capacitor being connected to the at least one first intermediate node, and a second terminal of the first shielding capacitor being connected to a fixed voltage. The first multi-gate transistor of the first initialization module includes at least two first sub-transistors connected in series, which reduces leakage current in the first initialization module and, in turn, minimizes potential variations at the first terminal of the light-emitting module.

Furthermore, at least one first shielding capacitor stabilizes the potential of the first intermediate node of the first multi-gate transistor, reducing the impact of potential variations at the control terminal of the first multi-gate transistor on the potential of the first intermediate node. This further reduces leakage current in the first initialization module, maintains a stable potential at the first terminal of the light-emitting module, and improves display uniformity.

BRIEF

DESCRIPTION OF THE DRAWINGS [0044] FIG. 1 is a schematic diagram of the structure of a pixel circuit provided in an embodiment of the present invention; [0045] FIG. 2 is a schematic diagram of the structure of another pixel circuit provided in an embodiment of the present invention; [0046] FIG. 3 is a schematic diagram of the structure of another pixel circuit provided in an embodiment of the present invention; [0047] FIG. 4 is a schematic diagram of the structure of another pixel circuit provided in an embodiment of the present invention; [0048] FIG. 5 is a schematic diagram of the structure of another pixel circuit provided in an embodiment of the present invention; [0049] FIG. 6 is a timing diagram of a pixel circuit provided in an embodiment of the present invention; [0050] FIG. 7 is a schematic diagram of the structure of a display panel provided in an embodiment of the present invention; [0051] FIG. 8 is a partial enlarged view of a display panel provided in an embodiment of the present invention; [0052] FIG. 9 is a schematic diagram of the structure of an active layer and a first metal layer in a display panel provided in an embodiment of the present invention; [0053] FIG. 10 is a schematic diagram of the structure of an active layer, a first metal layer and a second metal layer in a display panel provided in an embodiment of the present invention; [0054] FIG. 11 is a schematic diagram of the structure of another display panel provided in an embodiment of the present invention; [0055] Figure 12 is a partial large-scale image of another display panel provided by an embodiment of the present invention; [0056] Figure 13 is a structural schematic diagram of an active layer and a first metal layer in another display panel provided by an embodiment of the present invention; [0057] Figure 14 is a structural schematic diagram of an active layer, a first metal layer and a second metal layer in another display panel provided by an embodiment of the present invention; [0058] Figure 15 is a structural schematic diagram of another display panel provided by an embodiment of the present invention; [0059] Figure 16 is a structural schematic diagram of an active layer and a first metal layer in another display panel provided by an embodiment of the present invention; [0060] Figure 17 is a partial large-scale image of another display panel provided by an embodiment of the present invention; [0061] Figure 18 is a structural schematic diagram of another display panel provided by an embodiment of the present invention.

Specific embodiments

[0062] The present invention will be further described in detail below with reference to the accompanying drawings and embodiments. It will be understood that the specific embodiments described herein are only used to explain the present invention and are not intended to limit the present invention. It should also be noted that, for ease of description, only parts of the present invention, not all structures, are shown in the accompanying drawings. [0063] As described in the background art, the existing display panel has a problem of poor display uniformity when displaying, which affects the display effect. The inventors have found that the reason for the above problem is that the transistor for initializing the light-emitting module, which is connected to the first end of the light-emitting module in the existing pixel circuit, has a relatively serious leakage current, resulting in poor uniformity of light emission from the light-emitting module at low grayscale. Most transistors for initializing the light-emitting module are single-gate structures. When the voltage at the control end of a single-gate structure transistor changes, the voltages at the first and second electrodes of the transistor will change significantly due to the change in the voltage at the control end, resulting in unequal voltages at the first and second electrodes, generating a large leakage current, thereby causing the voltage at the first end of the light-emitting module to change, reducing display uniformity. [0064] Based on the above reasons, an embodiment of the present invention provides a pixel circuit. FIG1 is a schematic diagram of the structure of a pixel circuit provided by an embodiment of the present invention. Referring to FIG1, the pixel circuit includes a data writing module 10, a driving module 11, a light emitting module 12, a first initialization module 13, and a first shielding module 14. The data writing module 10 is used to write data to the control terminal of the driving module 11 under the control of the signal received by its own control terminal.

Write data signal; [0066]

The driving module 11 and the light-emitting module 12 are connected between the first power line VDD and the second power line VSS, and the driving module 11 is used to output a driving signal according to the data signal to drive the

light-emitting module 12 to emit light; [0067] The first end of the first initialization module 13 is connected to the initialization signal line VREF, and the second end of the first initialization module 13 is connected to the first end of the light-emitting module 12. The first initialization module 13 is used to write an initialization voltage to the first end of the light-emitting module 12 under the control of the signal connected to its own control end; the first initialization module 13 includes a first multi-gate transistor 131, and the first multi-gate transistor 131 includes at least two first sub-transistors T1 connected in series, and adjacent

first sub-transistors T1 are electrically connected through a first intermediate node N1 therebetween; [0068] The first shielding module 14 includes at least one first shielding capacitor C1, the first end of the first shielding capacitor C1 is connected to at least one

first intermediate node N1, and the second end of the first shielding capacitor C1 is connected to a fixed voltage. [0069] Wherein, the light emitting module 11 may be an organic light emitting diode (OLED), the first end of the light emitting module 11 being the anode of the OLED, the driving signal being the driving current, and the OLED emitting light under the driving current. When the first multi-gate transistor 131 includes two first sub-transistors T1 connected in series, the first multi-gate transistor 131 is a double-gate transistor, when the first multi-gate transistor 131 includes three first sub-transistors T1 connected in series, the first multi-gate transistor 131 is a triple-gate transistor, and so on. There is a problem with multi-gate transistors, that is, when the multi-gate transistor is turned off, the middle node of the multi-gate transistor floats, making the potential of the middle node easily affected by other signals in the display panel, causing the potential of the middle node of the multi-gate transistor to be unstable, and the leakage current may still be large, resulting in poor luminous uniformity of the display panel, affecting the display quality. Therefore, in this embodiment, a first shielding capacitor C1 is connected at the first middle node N1 to stabilize the potential of the first middle node. The data writing module 10 is also connected to the data line VDATA, which is used to provide a data signal. Optionally, the second end of the first shielding capacitor C1 is electrically connected to the initialization signal line VREF, or the second

end of the first shielding capacitor C1 is electrically connected to the first power line VDD. [0070] In this embodiment, an exemplary embodiment includes three first sub-transistors T1 connected in series and a first shielding capacitor C1, wherein the first electrode of the first first sub-transistor T1 is connected to the initialization signal line VREF, the second electrode is connected to the first electrode of the adjacent second first sub-transistor T1, the second electrode of the second first sub-transistor T1 is connected to the first electrode of the adjacent third first sub-transistor T1, and the second electrode of the third first sub-transistor T1 is connected to the first end of the light-emitting module 12. The gates of the three first sub-transistors T1 serve as control terminals of the first initialization module 13. The first electrodes of the three first sub-transistors T1 are all sources, and the second electrodes are all drains. The first sub-transistors T1 can be either N-type transistors or P-type transistors. In this embodiment, the first sub-transistor T1 is exemplarily shown as a P-type transistor. In this embodiment, when the first multi-gate transistor 131 includes three first sub-transistors T1, there are two first intermediate nodes N1. In other embodiments, when the first multi-gate transistor 131 includes two first sub-transistors T1, there is one first intermediate node N1; when the first multi-gate transistor 131 includes four first sub-transistors T1, there are three first intermediate nodes N1, and so on. Each first intermediate node N1 can be connected to a first shielding capacitor C1. The user can set the number of first shielding capacitors C1 as needed. The first shielding capacitor C1 can stabilize the potential of the first intermediate node N1 of the first multi-gate transistor 131 when the first multi-gate transistor 131 is turned off, thereby reducing leakage of the first multi-gate transistor 131, thereby ensuring the stability of the potential of the first end of the light-emitting module 12, which is conducive to improving the uniformity of the display. [0071] The operation process of the pixel circuit can include an initialization phase, a data writing phase, and a light-emitting phase. In the initialization phase, the multiple first sub-transistors T1 connected in series are turned on under the control of the signal connected to their gates, and the initialization voltage provided by the initialization signal line VREF is written to the first end of the light-emitting module 12 to initialize the light-emitting module 12. In the data writing phase, the data writing module 10 is turned on under the control of the signal connected to its control end, and then writes the data signal to the control end of the driving module 11.

The voltage and the first power supply voltage provided by the first power line VDD generate a driving current to drive the light-emitting module 12 to emit light. During the light-emitting phase, the first multi-gate transistor 131 is in the off state. The first shielding capacitor C1 can stabilize the potential of the first intermediate node N1 of the first multi-gate transistor 131, thereby reducing the leakage of the first multi-gate transistor 131, ensuring the stability of the potential of the first terminal of the light-emitting module 12, and facilitating improved display

uniformity. [0072] The first multi-gate transistor of the first initialization module of the pixel circuit provided in this embodiment includes at least two first sub-transistors connected in series, so that the leakage current of the first initialization module is small, thereby reducing the potential variation of the first terminal of the light-emitting module. At the same time, at least one first shielding capacitor can stabilize the potential of the first intermediate node of the first multi-gate transistor, reducing the impact of the potential variation of the control terminal of the first multi-gate transistor on the potential of the first intermediate node, thereby further reducing the leakage of the first initialization module, maintaining the stability of the potential of the first terminal of the light-emitting module, thereby reducing the variation of the driving current and improving display

uniformity. [0073] Based on the above technical solution, optionally, the line width of the active layer of the first multi-gate transistor is less than the first set threshold.

[0074] The

line width of the active layer is the width of the active layer in a direction perpendicular to the direction of current flow. The line width of the active layer of the first multi-gate transistor is less than the first set threshold value, which can realize the setting of the multi-gate structure within a limited area, which is conducive to ensuring a high pixel density of the display panel. The first set threshold value can be set according to demand. [0075]

Figure 2 is a structural schematic diagram of another pixel circuit provided by an embodiment of the present invention. Referring to Figure 2, optionally, the driving module 11 includes a driving transistor T0, and the first set threshold value is equal to the line width of the active layer of the driving transistor

T0. [0076] The gate of the driving transistor T0 serves as the control terminal of the driving module 11. The line width of the active layer of the first multi-gate transistor 131 is less than the line width of the active layer of the driving transistor T0, which can realize the setting of the multi-gate structure within a limited area. Optionally, the driving transistor T0 is a single-gate transistor. [0077]

FIG3 is a schematic structural diagram of another pixel circuit provided in an embodiment of the present invention. Referring to FIG3, the pixel circuit optionally further includes a second initialization module 15 and a second shielding module 16. [0078] A

first end of the second initialization module 15 is connected to the initialization signal line VREF, and a second end of the second initialization module 15 is connected to the control end of the driving module 11. The second initialization module 15 is configured to write an initialization voltage to the control end of the driving module 11 under the control of a signal input to its own control end. The second initialization module 15 includes a second multi-gate transistor 151, and the second multi-gate transistor 151 includes at least two second sub-transistors T2 connected in series, with adjacent second sub-transistors T2 electrically connected via a second intermediate node N2 therebetween.

[0079] The second shielding module 16 includes at least one second shielding capacitor C2, a first end of the second shielding capacitor C2 is connected to the at least one second intermediate node N2, and a second end of the second shielding capacitor C2 is connected to a fixed

voltage. [0080] Optionally, the second end of the second shielding capacitor C2 is electrically connected to the initialization signal line VREF, or the second end of the second shielding capacitor C2 is electrically connected to the first power

line VDD. In this embodiment, the second multi-gate transistor 151 includes four second sub-transistors T2 connected in series and a second shielding capacitor C2, wherein the first electrode of the first second sub-transistor T2 is connected to the initialization signal line VREF, the second electrode of the first second sub-transistor

T2 is connected to the first electrode of the second second sub-transistor T2, and the second second sub-transistor T2 is connected to the first electrode of the second second sub-transistor T2

The second electrode of T2 is connected to the first electrode of the third second sub-transistor T2, the second electrode of the third second sub-transistor T2 is

connected to the first electrode of the fourth second sub-transistor T2, the second electrode of the fourth second sub-transistor T2 is connected to the control terminal

of the driving module 11, and the gates of the four second sub-transistors T2 serve as the control terminal of the second initialization module 15. Among them, the first

electrodes of the four second sub-transistors T2 are all sources, and the second electrodes are all drains. The second sub-transistor T2 can be an N-type transistor or

a P-type transistor. In this embodiment, the second sub-transistor T2 is exemplarily shown as a P-type transistor. In this embodiment, the second multi-gate transistor T2 is a

When the body transistor 151 includes four second sub-transistors T2, the second multi-gate transistor 151 includes three second intermediate nodes N2. In other embodiments, when the second multi-gate transistor 151 includes three second sub-transistors T2, the second multi-gate transistor 151 includes two second intermediate nodes N2. When the second multi-gate transistor 151 includes five second sub-transistors T2, the second multi-gate transistor 151 includes four second intermediate nodes N2, and so on. Each second intermediate node N2 can be connected to a second shielding capacitor C2, and the user can set the number of second shielding capacitors C2 as needed. The second shielding capacitor C2 can stabilize the potential of the second intermediate node N2 of the second multi-gate transistor 151. When the second multi-gate transistor 151 is turned off, the presence of the second shielding capacitor C2 can reduce the leakage of the second multi-gate transistor 151, thereby ensuring the stability of the potential of the control terminal of the driving module 11, thereby ensuring the stability of the driving current, which is conducive to improving display uniformity. [0082]

Based on the above technical solution, with continued reference to FIG3, optionally, the line width of the active layer of the second multi-gate transistor 151 is smaller than the second set threshold.

[0083] The line width of the active layer of the second multi-gate transistor 151 is smaller than the second set threshold, which allows the multi-gate structure to be configured within a limited area. The second set threshold can be set as required, and the second set threshold can be equal to the first set threshold.

Optionally, when the driving module 11 includes a driving transistor, the second set threshold is equal to the line width of the active layer of the driving transistor. The line width of the active layer of the second multi-gate transistor 151 is smaller than the line width of the active layer of the driving transistor, which allows the multi-gate structure to be configured within a limited area, which is beneficial for ensuring a higher pixel density of the

display panel. [0084] FIG4 is a schematic structural diagram of another pixel circuit provided in an embodiment of the present invention. Referring to FIG4, the pixel circuit optionally further includes a compensation module 17 and a third shielding module 18. The compensation module 17 is configured to compensate for the threshold voltage of the driving transistor T0 included in the driving module 11 under the control of a signal

input to its control terminal. [0085] The compensation module 17 includes a third multi-gate transistor 171. The third multi-gate transistor 171 includes at least two third sub-transistors T3 connected in series. Adjacent third sub-transistors T3 are electrically connected via a third intermediate node N3

therebetween. [0086] The third shielding module 18 includes at least one third shielding capacitor C3. A first end of the third shielding capacitor C3 is connected to the at least one third intermediate node N3, and a second end of the third shielding capacitor C3 is connected to a

fixed voltage. [0087] Optionally, a second end of the third shielding capacitor C3 is electrically connected to the initialization signal line VREF, or a second end of the third shielding capacitor C3 is electrically connected to the first

power supply line VDD. [0088] Optionally, the pixel circuit further includes a light emitting control module 20. The light emitting control module 20, the driving module 11, and the light emitting module 12 are connected between the first power line VDD and the second power line VSS. The light emitting control module 20 is configured to control the light emitting module 12 to emit light according to the driving signal output by the driving

module 11 under the control of a signal at its control end. [0089] In this embodiment, the third multi-gate transistor 171 exemplarily includes two third sub-transistors T3 connected in series and a third shielding capacitor C3. The first electrode of the first third sub-transistor T3 is connected to the second electrode of the driving transistor T0, the second electrode is connected to the first electrode of the second third sub-transistor T3, and the second electrode of the second third sub-transistor T3 is connected to the first electrode of the driving transistor T0. The gate of the third sub-transistor T3 is connected to the control terminal of the compensation module 13.

The first electrodes of T3 are all sources, and the second electrodes are all drains. The third sub-transistor T3 can be an N-type transistor or a P-type transistor.

In this embodiment, the third sub-transistor T3 is exemplarily shown to be a P-type transistor. In this embodiment, when the third multi-gate transistor 171 includes two third sub-transistors T3, the third multi-gate transistor 171 includes a third intermediate node N3. In other embodiments, when the third multi-gate transistor 171 includes three third sub-transistors T3, the third multi-gate transistor 171 includes two third intermediate nodes N3, and so on. A third shielding capacitor C3 can be connected to each third intermediate node N3, and the user can set the number of third shielding capacitors C3 according to needs. [0090] In the data writing stage, the data voltage is written to the gate of the driving

transistor T0 through the data writing module 10 and the compensation module 17. At the same time, the compensation module 17 can compensate the threshold of the driving transistor T0, so that the driving transistor T0 can be driven.

The gate voltage includes a voltage associated with the data voltage and the threshold voltage, thereby realizing the writing of the data voltage and threshold compensation of the driving transistor T0. The third shielding capacitor C3 can stabilize the potential of the third intermediate node N3 of the third multi-gate transistor 171. When the third multi-gate transistor 171 is turned off, due to the presence of the third shielding capacitor C3, the leakage of the third multi-gate transistor 171 can be reduced, thereby ensuring the stability of the potential of the control terminal of the driving module 11, so that the stability of the driving current is improved, which is conducive to improving display uniformity. [0091]

Figure 5 is a structural schematic diagram of another pixel circuit provided by an embodiment of the present invention. Referring to Figure 5, the pixel circuit optionally further includes a storage module 19, which is connected to the control terminal of the driving module 11 and is used to store the voltage of the control terminal of the driving module 11. Optionally, the storage module 19 includes a storage capacitor C0, one end of the storage capacitor C0 is connected to the first power line VDD, and the other end of the storage capacitor C0 is connected to the control terminal of the driving

module 11. [0092] Optionally, the light control module 20 includes a fourth transistor T4 and a fifth transistor T5, wherein a first electrode of the fourth transistor T4 is connected to the first power line VDD, a second electrode of the fourth transistor T4 is connected to the first end of the driving module 11, a first electrode of the fifth transistor T5 is connected to the second end of the driving module 11, a second electrode of the fifth transistor T5 is connected to the first end of the light emitting module 12, and gate electrodes of the fourth transistor T4 and the fifth transistor T5 are connected to the light

control signal line EM. [0093] The data writing module 10 includes a sixth transistor T6, wherein a first electrode of the sixth transistor T6 is connected to the data line VDATA, a second electrode of the sixth transistor T6 is connected to the first end of the driving module 11, and a gate electrode of the sixth transistor T6 is

connected to the second scan line S2. [0094] Optionally, the first multi-gate transistor 131 includes a first sub-transistor T1, whose gate electrode is connected to the first scan line S1, and a first shielding capacitor C1 is connected to the first power line VDD. The second multi-gate transistor 151 includes a second sub-transistor T2, whose gate electrode is connected to the first scan line S1, and a second shielding capacitor C2 is connected to the first power line VDD. The third multi-gate transistor 171 includes a third sub-

transistor T3, whose gate electrode is connected to the second scan line, and the third shielding capacitor C3 is connected to the first power supply line VDD. In other optional embodiments of the present invention, the first shielding capacitor C1, the second shielding capacitor C2, and the third shielding capacitor C3 can all be connected to the

initialization signal line VREF. [0095] Figure 6 is a timing diagram of a pixel circuit provided in an embodiment of the present invention. The timing diagram shown in Figure 6 is applicable to the pixel circuit shown in Figure 5. Among them, the transistors included in the pixel circuit shown in Figure 5 are all P-type transistors.

Referring to Figures 5 and 6, the working process of the pixel circuit includes an initialization stage t1, a data writing and threshold compensation stage t2, and a light-emitting stage t3. The working process

of the pixel circuit is as follows: [0096] In the initialization stage t1, the signal on the first scan line S1 is low, and the signals on the second scan line S2 and the light-emitting control signal line EM are both high. The first sub-transistor T1 included in the first multi-gate transistor 131 and the second sub-transistor T2 included in the second multi-gate transistor 151 are turned on, and the third sub-transistor T3 and the fourth transistor T3 included in the third multi-gate transistor 171 are turned on.

In the data writing and threshold compensation phase t2, the signal on the second scan line S2 is at a low level, the signal on the first scan line S1 and the signal on the light emitting control signal line EM are at a high level, the third sub-transistor T3, the sixth transistor T6, and the driving transistor T0 included in the third multi-gate transistor 171 are turned on, and the first sub-transistor T1 included in the first multi-gate transistor 131,

the second sub-transistor T2 included in the second multi-gate transistor 151, the fourth transistor T4, and the fifth transistor T5 are turned off. The data voltage transmitted by the data line VDATA is written to the gate of the driving transistor T0 via the sixth transistor T6, the driving transistor T0, and the third sub-transistor T3 included in the third multi-gate transistor 171, thereby writing the data voltage to the gate of the driving transistor T0 and compensating the threshold voltage of the driving transistor T0. In the light-emitting stage t3, the signal on the light-emitting control signal line EM is at a low level, the signals on the first scan line S1 and the second scan line S2 are at a high level, the driving transistor T0, the fourth transistor T4 and the fifth transistor T5 are turned on, and the first multi-gate transistor

The first sub-transistor T1 included in 131, the second sub-transistor T2 included in the second multi-gate transistor 151, the third sub-transistor T3 included in the third multi-gate transistor 171, and the sixth transistor T6 are turned off. The first power supply voltage on the first power line VDD is transmitted to the first electrode of the driving transistor T0 through the fourth transistor T4. The driving transistor T0 drives the light-emitting module 12 to emit light according to the voltage of its gate and the voltage of the first electrode. Due to the presence of the second shielding capacitor C2, the potential of the second intermediate node N2 of the second multi-gate transistor 151 can be stabilized, thereby reducing the leakage of the second multi-gate transistor 151 and maintaining the stability of the gate potential of the driving transistor T0, thereby ensuring the stability of the driving current and improving display uniformity. The third shielding capacitor C3 can stabilize the potential of the third intermediate node N3 of the third multi-gate transistor 171, thereby reducing the leakage of the third multi-gate transistor 171 and maintaining the stability of the gate potential of the driving transistor T0. The gate potential of T0 is stabilized, ensuring the stability of the driving current and improving the display uniformity. At the same time, the first shielding capacitor C1 can stabilize the potential of the first intermediate node N1 of the first multi-gate transistor 131, thereby reducing the leakage of the first multi-gate transistor 131, maintaining the stability of the potential of the first end of the light-emitting module 12, and further improving the display uniformity.

[0099] An embodiment of the present invention further provides a display panel, including the pixel circuit of any of the above embodiments. FIG7 is a schematic structural diagram of a display panel provided by an embodiment of the present invention. Referring to FIG7 and FIG1, the display panel further includes a first power line VDD, a data line VDATA, an initialization signal line VREF, a first scan line S1 and a second scan line S2. The first power line VDD and the data line VDATA extend along a first direction Y, and the initialization signal line VREF, the first scan line S1 and the second scan line S2 extend along a second direction X. The first direction Y and the second direction X intersect. [0100] Optionally, the pixel circuits 01 are arranged in an array, with the first direction Y being the column direction of the pixel circuits 01, and the second direction X being the row direction of the pixel circuits 01. The control end of the first initialization module 13 in each row of pixel circuits 01 is connected to the same first scan line S1, the first end of the first initialization module 13 in each row of pixel circuits 01 is connected to the same initialization signal line VREF, the control end of the data writing module 10 in each row of pixel circuits 01 is connected to the same second scan line S2, the first end of the data writing module 10 in each column of pixel circuits 01 is connected to the same data line VDATA, and the pixel circuits 01 in each column are connected to the same first power line VDD; the first scan line S1 connected to the pixel circuits 01 in the same row is located between the initialization signal line VREF and the second scan line S2. [0101] In this embodiment, two complete pixel circuits 01 are exemplarily shown. It is worth noting that, during the initialization phase, the first

initialization module 13 in the pixel circuits 01 in the nth row initializes the first end of the light-emitting module 12 of the pixel circuits 01 in the n-1th row in the same column. Wherein, $n \geq 2$. [0102] FIG8 is a partial enlarged view of a display panel, FIG8 is a partial enlarged view of the dotted area 001 shown in FIG7, FIG9 is a schematic structural diagram of an active layer and a first metal layer

in a display panel provided in an embodiment of the present invention, and FIG10 is a schematic structural diagram of an active layer, a first metal layer, and a second metal layer in a display panel provided in an embodiment of the present invention. Referring to FIG7-FIG10, optionally, the display panel includes an active layer 100, a first metal layer 200, and a second metal layer 300 stacked, wherein the first scan line S1 and the second scan line S2 are located in the first metal layer 200, and the initialization signal line VREF is located in the second metal layer 300; the display panel also includes a third metal layer, and the first power line VDD and the data line VDATA in the display panel are located in the third metal layer. [0103] Continuing with reference to Figures 1, 7-10, optionally, at least one first intermediate node N1 of the first multi-gate transistor 131 overlaps with the first fixed potential structure to form at least one first shielding capacitor C1. The first intermediate node N1 of the first multi-gate transistor 131 includes a first active portion in the active layer of the first multi-gate transistor 131 that connects adjacent first sub-transistors T1. [0104] The active layer of the first multi-gate transistor 131 overlaps with the first scan line S1 to form at least two first sub-transistors T1 connected in series. [0105] Optionally, the first active portion includes a first sub-active portion 111 located between the first scan line S1 and the second scan line S2 that are electrically connected to the same pixel circuit 01.

[0106] The first fixed potential structure includes a first fixed potential portion 311 located between a first scan line S1 and a second scan line S2 electrically connected to the same pixel circuit O1. The first fixed potential portion 311 is electrically connected to the first power supply line VDD.

[0107] The first fixed potential portion 311 overlaps with the first sub-active portion 111 to form a first shielding capacitor C1. [0108] In this embodiment, the first multi-gate transistor 131 exemplarily includes three first sub-transistors T1. The first first sub-transistor T1, the second first sub-transistor T1, and the third first sub-transistor T1 are arranged from left to right along the second direction X. The active layer connecting the second first sub-transistor T1 and the third first sub-transistor T1 serves as the first sub-active portion 111. In this embodiment, the first fixed potential portion 311 is electrically connected to the first power line VDD. The first fixed potential portion 311 overlaps with the first sub-active portion 111 to form a first shielding capacitor C1. Specifically, the first sub-active portion 111 serves as one plate of the first shielding capacitor C1, and the first fixed potential portion 311 serves as the other plate of the first shielding capacitor C1. This allows the potential of the first intermediate node N1 to remain stable when the first multi-gate transistor 131 is turned off, thereby reducing leakage of the first multi-gate transistor 131, ensuring the stability of the potential at the first end of the light-emitting module 12, and improving display uniformity. Optionally, the first fixed potential structure is located in the second metal layer 300 and is disposed on the same layer as the initialization signal line VREF. This eliminates the need for additional metal layers in the display panel to form the first fixed potential structure, thus minimizing the number of film layers in the display panel and facilitating a thinner and lighter display panel. [0109] Continuing to refer to Figures 1, 7, and 10, optionally, the data line VDATA and the first

power line VDD are arranged along the second direction X, and the first multi-gate transistor 131 is located on a side of the first power line VDD connected to the pixel circuit O1 to which the first multi-gate transistor 131 belongs, away from the data line VDATA. [0110] The first fixed potential structure also includes a first connecting portion 312 connecting

the first power line VDD and the first fixed potential portion 311. The first connecting portion 312 extends along the second direction X. In the same pixel circuit O1, the first sub-active portion 111 is located on a side of the first connecting portion 312 close to the first scan line S1 connected to the pixel circuit O1.

[0111] The first connecting portion 312 extends along the second direction X, and the first connecting portion 312 simultaneously connects the first fixed potential portion 311 and the first power line VDD, so that the potential of the first fixed potential portion 311 is equal to the first power supply voltage transmitted by the first power line VDD. Continuing to refer to Figures 1, 7, and 10, optionally, the first multi-gate transistor includes at least three first sub-transistors connected in series.

The first active portion T1 includes a second sub-active portion 112 located on a side of the first scan line S1 away from the second scan line S2.

[0112] The second sub-active portion 112 overlaps with the initialization signal line VREF to form a first shielding capacitor C1. [0113] In this embodiment, the active layer connecting the first first sub-transistor T1 and the second first sub-transistor T1 is the second sub-active portion 112. The second sub-active portion 112 overlaps with the initialization signal line VREF to form a first shielding capacitor C1. That is, the second sub-active portion 112 serves as one plate of the first shielding capacitor C1, and the initialization signal line VREF serves as the other plate of the first shielding capacitor C1. This ensures that when the first multi-gate transistor 131 is turned off, the potential at the second sub-active portion 112 remains stable, thereby reducing leakage of the first multi-gate transistor 131 and maintaining a stable potential at the first end of the light-emitting module 12, which is beneficial for improving display uniformity. At the same time, the initialization signal line VREF serves as a plate of the first shielding capacitor C1, thereby eliminating the need to provide an additional metal layer or the like in the display panel to form a capacitor structure, thereby preventing an increase in the number of film layers of the display panel and a thickness of the display panel, which is conducive to achieving a thinner and lighter display panel. [0114]

Continuing to refer to Figures 1 and 7-10, the pixel circuit O1 optionally includes a second connection portion 313, the second connection portion 313 extending along the first direction Y, one end of the second connection portion 313 connected to the initialization signal line VREF, and the other end connected to the first electrode T1-1 of the first multi-gate transistor 131, and the second electrode T1-2 of the first multi-gate transistor 131 connected to the first end of the light-emitting module 12. [0115] Optionally, the second connection portion 313 is located in the third metal layer, and the second connection portion 313 is located in the same layer as the data line VDATA and the first power line VDD. The initialization signal line VREF located in the second metal layer 300 is connected to the third metal layer through the via 002, and the third metal layer is connected to the first electrode T1-1 of the first multi-gate transistor through the via 002, thereby realizing the initialization s

The signal line VREF is connected to the first electrode T1-1 of the first multi-gate transistor 131. In the initialization stage, the initialization voltage provided by the initialization signal line VREF is written into the first end of the light-emitting module 12 via the first multi-gate transistor 131 to realize the initialization of the light-emitting module 12. There are vias between the second metal layer 300 and the third metal layer for connection, and there are also vias between the third metal layer and the active layer 100 for connection. When the active layer 100 is connected to the initialization signal line VREF, no additional separate mask step is required for drilling, which simplifies the process and makes the display panel easier to manufacture. [0116] Referring to Figures 4 and 7-10, optionally, the pixel circuit further includes a compensation module 17 and a third shielding module 18. The compensation module 17 includes a third multi-gate transistor 171. The third multi-gate transistor 171 includes at least two third sub-transistors connected in series. T3, at least one third intermediate node N3 of the third multi-gate transistor 171 overlaps with the third fixed potential structure to form at least one third shielding capacitor C3, and the third intermediate node N3 of the third multi-gate transistor 171 includes a third active portion in the active layer of the third multi-gate transistor 171 that connects the adjacent third sub-transistor T3;

[0117] Referring to Figures 4 and 7-10, optionally, the third active portion includes at least one third sub-active portion 113 between the first scan line S1 and the second scan line S2 connected to the same pixel circuit 01, and the third fixed potential structure includes at least one third fixed potential portion 331, and the third fixed potential portion 331 is connected to the first connecting portion 312. In the same pixel circuit 01, the third sub-active portion 113 and the third fixed potential portion 331 are located on a side of the first connecting portion 312 close to the second scan line S2 connected to the pixel circuit 01, and the third sub-active portion 113 overlaps with the corresponding third fixed potential portion 331 to form a third shielding capacitor C3. In this embodiment, the third multi-gate transistor 171 includes two third sub-transistors T3, and the active layer connected to the two third sub-transistors T3 serves as the third sub-active portion 113. The third fixed potential portion 331 is located in the second metal layer 300. This eliminates the need for additional metal layers in the display panel to form a first fixed potential structure, thereby minimizing the number of film layers in the display panel and facilitating a thinner and lighter display panel. The third fixed potential portion 331 is connected to the first power line VDD via the first connecting portion 312, such that the potential of the third fixed potential portion 331 is equal to the first power supply voltage. The third sub-active portion 113 overlaps with the corresponding third fixed potential portion 331 to form a third shielding capacitor C3. Specifically, the third sub-active portion 113 serves as one plate of the third shielding capacitor C3, and the third fixed potential portion 331 serves as the other plate of the third shielding capacitor C3. The third shielding capacitor C3 ensures that the third intermediate node N3 of the third multi-gate transistor 171 remains stable when the third multi-gate transistor 171 is turned off, thereby reducing leakage of the third multi-gate transistor 171 and maintaining the stability of the control terminal of the driving module 11, thereby ensuring the stability of the driving current and improving display

uniformity. [0119] In the prior art, the third fixed potential portion 331 of the pixel circuit 01 located in the jth column is connected to the first power line VDD connected to the pixel circuit 01 in the j+1th column of the same row, thereby forming one plate of the third shielding capacitor C3 to stabilize the potential of the third intermediate node N3 of the third multi-gate transistor 171. However, when the third fixed potential portion 331 is connected to the first power line VDD connected to the pixel circuit 01 in the adjacent column, it needs to jump across the data line VDATA, thereby forming a parasitic capacitance, which in turn affects the potential of the third intermediate node N3 of the third multi-gate transistor 171. Wherein, j, j+1. In this embodiment, the third fixed potential portion 331 is connected to the first connection portion 312, and the first connection portion 312 is connected to the first power line VDD connected to the pixel circuit. There is no need to jumper the data line VDATA, thereby avoiding the influence of the parasitic capacitance formed by the data line VDATA and the first connection portion 312 on the third intermediate node N3 of the third multi-gate transistor, and the layout of the third shielding capacitor C3 is simpler and easier to implement. [0120] Referring to Figures 5, 7 and 8, the pixel circuit also includes a second initialization module 15 and a light control module 20. The second initialization module includes a second multi-gate transistor 151, and the second multi-gate transistor 151 includes at least two second sub-transistors T2 connected in series. The light control module 20 includes a fourth transistor T4 and a fifth transistor T5. The data

writing module 10 includes a sixth transistor T6. [0121] Figure 11 is a structural schematic diagram of another display panel provided in an embodiment of the present invention. Figure 12 is a partial enlarged view of another display panel provided in an embodiment of the present invention. Figure 12 is a partial enlarged view of the dotted

FIG14 is a schematic diagram of the structure of the active layer and the first metal layer of another display panel provided by an embodiment of the present invention.

FIG15 is a schematic diagram of the structure of the active layer, the first metal layer and the second metal layer of another display panel provided by an embodiment of the present invention. Referring to FIG3 and FIG11-FIG14, optionally, the pixel circuit further includes a second initialization module 15 and a second shielding module; the second initialization module 15 includes a second multi-gate transistor 151, and the second multi-gate transistor 151 includes at least two second sub-transistors connected in series.

T2, at least one second intermediate node N2 of the second multi-gate transistor 151 overlaps with the second fixed potential structure to form at least one second shielding capacitor C2, and the second intermediate node N2 of the second multi-gate transistor 151 includes a second active portion in the active layer of the second multi-gate transistor 151 that connects to the adjacent second sub-transistor T2. [0122] Referring

to Figures 3, 11-14, optionally, the second active portion includes at least one fourth sub-active portion 114 located on a side of the first scan line S1 connected to the same pixel circuit O1 away from the second scan line S2. [0123] The fourth sub-active portion 114 overlaps with the

initialization signal line VREF to form a second shielding capacitor C2. [0124] The fourth sub-active portion 114 serves as one plate of the second

shielding capacitor C2, and the initialization signal line VREF serves as the other plate of the shielding capacitor. The initialization signal line VREF serving as the other plate of the second shielding capacitor eliminates the need to provide an additional metal layer or the like in the display panel to form a capacitor structure, thereby reducing the number of film layers of the display panel and facilitating a thinner and lighter display panel. The second shielding capacitor C2 can ensure that when the second multi-

gate transistor 151 is turned off, the potential of the second intermediate node N2 of the second multi-gate transistor 151 remains stable, thereby reducing the leakage of the second multi-gate transistor 151, maintaining the stability of the potential of the control terminal of the driving module 11, and thus maintaining the stability of the driving current, thereby improving display uniformity. [0125] Continuing to refer to Figures 3 and 11-14, optionally, the pixel circuit 01 includes a third

connecting portion 314 and a fourth connecting portion 315, and the third connecting portion 314 and the fourth connecting portion 315 both extend along the first direction

Y. One end of the third connecting portion 314 is connected to the initialization signal line VREF, and the other end is connected to the first electrode T2-1 of the second multi-gate transistor 151. One end of the fourth connecting portion 315 is connected to the second electrode T2-2 of the second multi-gate transistor, and the other end is connected to the control terminal of the driving module 10. The third connection portion 314 and the fourth connection

portion 315 are both located in the third metal layer. The third connection portion 314 is connected to the initialization signal line VREF through the via 002. At the same time, the third connection portion 314 is connected to the first electrode T2-1 of the second multi-gate transistor 151, thereby connecting the first electrode T2-1 of the

second multi-gate transistor 151 to the initialization signal line VREF. One end of the fourth connection portion 315 is connected to the second electrode T2-2 of the second multi-gate transistor 151, and the other end is connected to the control terminal of the driving module 11, thereby connecting the second electrode T2-2 of the second multi-

gate transistor 151 to the control terminal of the driving module 11. Therefore, during the initialization phase, the second multi-gate transistor 151 writes the initialization voltage to the control terminal of the driving module 11, thereby initializing the driving module 11. There are vias between the second metal layer 300 and the third metal layer for connection, and there are also vias between the third metal layer and the active layer 100 for connection. Therefore, when connecting the active layer 100 to the initialization signal line VREF, no additional masking step is required for drilling holes, which simplifies the process and makes the display panel easier to manufacture.

[0127] Optionally, the third connection portion 314 and the second connection portion 313 have the

same structure. [0128] The third connection portion 314 and the second connection portion 313 have the same

structure, which can avoid the need for an additional third connection portion 314, thereby simplifying the layout of the display panel and saving the area of the display panel. [0129] Referring to Figures 5 and 11-14, the pixel circuit also includes a second initialization

module 15 and a light control module 20. The second initialization module 15 includes a second multi-gate transistor 151, which includes at least two second sub-transistors T2 connected in series. The light control module includes a fourth transistor T4 and a fifth transistor T5. The data writing module includes a sixth transistor T6. [0130]

Optionally, the first multi-gate transistor includes an odd number of first sub-transistors, and the second multi-gate transistor includes an even number of second sub-transistors

(for example, the display panel structure shown in FIG7). [0131] FIG15 is a schematic diagram of the structure of another display panel provided in an embodiment of the present invention, and FIG16 is a schematic diagram of the structure of an

embodiment of the present invention.

A schematic structural diagram of the active layer and the first metal layer of another display panel is provided. FIG17 is a partial enlarged view of another display panel provided in an embodiment of the present invention. FIG17 is a partial enlarged view of the dotted line 004 area shown in FIG16. Referring to FIG15-FIG17, optionally, the first multi-gate transistor 131 includes an even number of first sub-transistors T1, and the second multi-gate transistor 151 includes an odd number of second sub-transistors T2.

[0132] Referring to FIG15-FIG17, the pixel circuit also includes a second initialization module and a light emitting control module. The second initialization module includes a second multi-gate transistor 151. The second multi-gate transistor 151 includes at least two second sub-transistors T2 connected in series. The light emitting control module includes a fourth transistor T4 and a fifth transistor T5. The data writing module includes a sixth transistor T6. The driving module includes a driving transistor T0. [0133] Continuing

to refer to FIG5 and FIG11-FIG17, the second multi-gate transistor 151 includes at least three second sub-transistors connected in series.

T2, the second active portion includes a fifth sub-active portion 115 located between the first scan line S1 and the second scan line S2 electrically connected to the same pixel circuit 01; [0134]

the second fixed potential structure includes a second fixed potential portion 321 located between the first scan line S1 and the second scan line S2 electrically connected to the same pixel circuit 01, the second fixed potential portion 321 being electrically connected to the first power supply line VDD;

[0135] the second fixed potential portion 321 overlaps with the fifth sub-active portion 115 to form a second shielding capacitor C2. [0136]

In this embodiment, four second sub-transistors T2 are exemplarily shown, including, from left to right along the second direction X, the first second sub-transistor T2, the second second sub-transistor T2, the third second sub-transistor T2, and the fourth second sub-transistor T2. The active layer connected to the second second sub-transistor T2 and the third second sub-transistor T2 is the fifth sub-active portion 115. The second fixed potential portion 321 is located in the second metal layer and is electrically connected to the first power line VDD, so that the second fixed potential portion 321 constitutes one plate of the second shielding capacitor C2, and the fifth sub-active portion 115 constitutes the other plate of the second shielding capacitor C2. When the second multi-gate transistor 151 is turned off, the second shielding capacitor C2 can stabilize the potential of the second intermediate node N2 of the second multi-gate transistor 151, thereby reducing the leakage of the second multi-gate transistor 151, maintaining the stability of the control terminal potential of the driving module 11, and thus displaying uniformity. [0137] Figure 18 is a

schematic structural diagram of another display panel provided by an embodiment of the present invention. Referring to Figure 18, optionally, the pixel circuit 01 of the display panel in this embodiment includes a driving transistor T0, a first sub-transistor T1, a second sub-transistor T2, a third transistor T3, a fourth transistor T4, a fifth transistor T5, and a sixth transistor T6. The pixel circuit 01 includes a second connection portion 313, which extends along a first direction Y. One end of the second connection portion 313 is connected to the initialization signal line VREF, and the other end is connected to the first electrode T1-1 of the first multi-gate transistor. The pixel circuit may also include a fifth connection portion 316, which extends along a second direction X. One end of the fifth connection portion 316 is connected to the second connection portion 313, and the other end of the fifth connection portion 316 overlaps with the first sub-active portion to form a first shielding capacitor C1. [0138] The fifth connection portion 316 is connected to

the second connection portion 313, and the second connection portion 313 is connected to the initialization signal line VREF. Therefore, the potential on the fifth connection portion 316 is equal to the initialization voltage. That is, the potential on the first shielding capacitor C1 formed by the overlap of the fifth connection portion 316 and the first sub-active portion can be the initialization voltage. The second connection portion 313 and the fifth connection portion 316 are provided in the same layer as the first power line VDD, thereby making it unnecessary to provide an additional metal layer in the display panel when forming the first shielding capacitor C1, so that the number of film layers of the display panel does not increase, which is conducive to achieving a lighter

and thinner display panel. [0139] Note that the above are only preferred embodiments of the present invention and the technical principles used. Those skilled in the art will understand that the present invention is not limited to the specific embodiments described herein, and that various obvious changes, readjustments, and substitutions can be made by those skilled in the art without departing from the scope of protection of the present invention. Therefore, although the present invention has been described in detail through the above embodiments, the present invention is not limited to the above embodiments, and may include more other equivalent embodiments without departing from the concept of the present invention, and the scope of the present invention is determined by the scope of the appended claims.

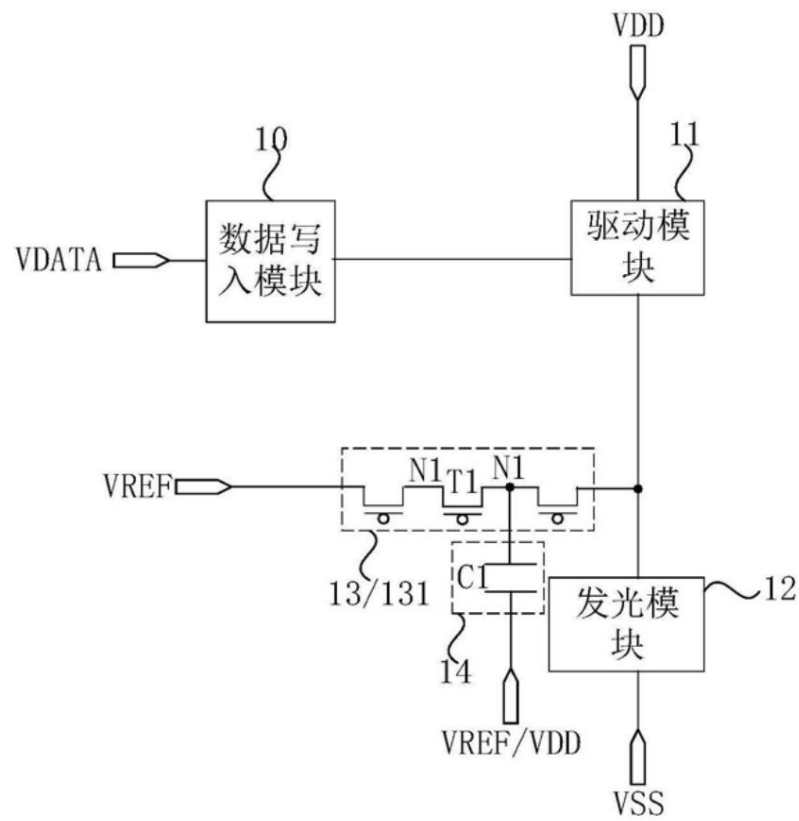


Figure 1

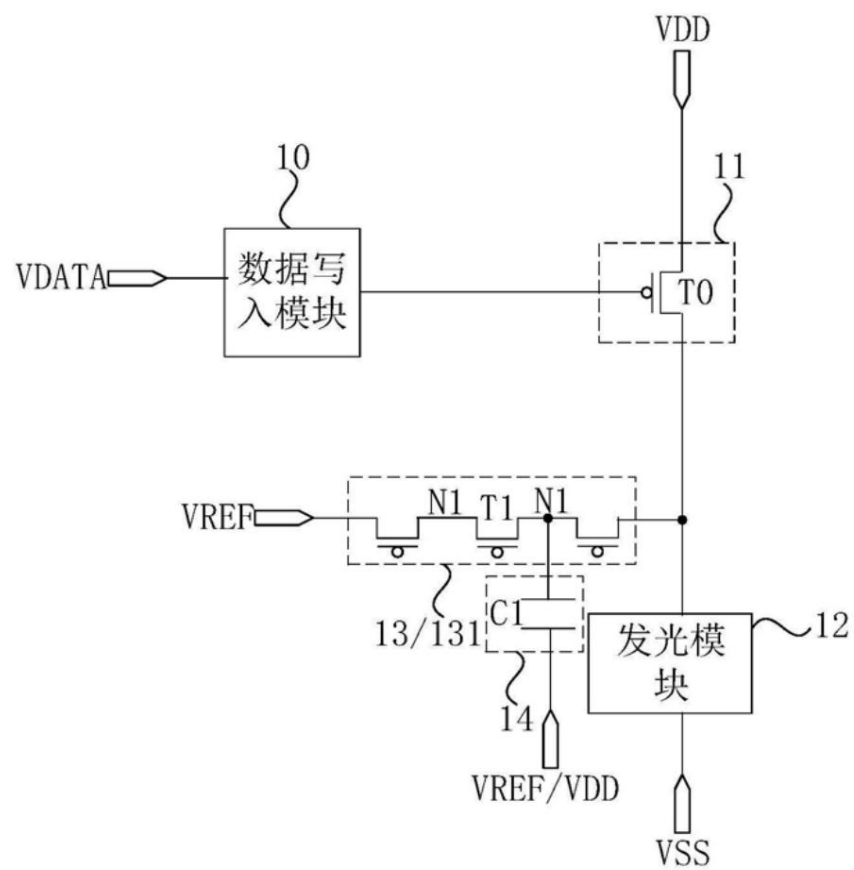


Figure 2

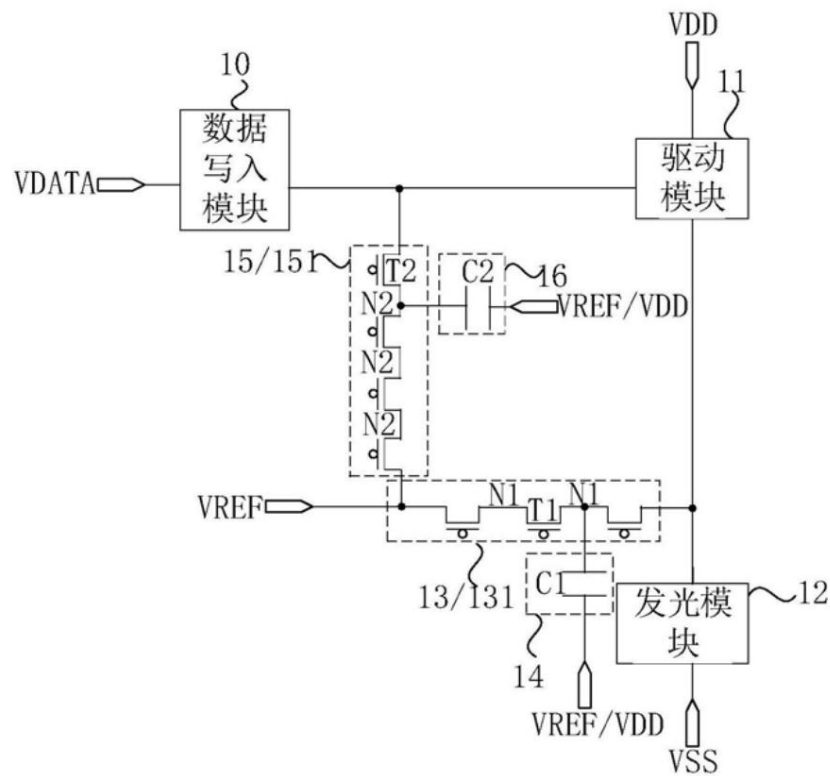


Figure 3

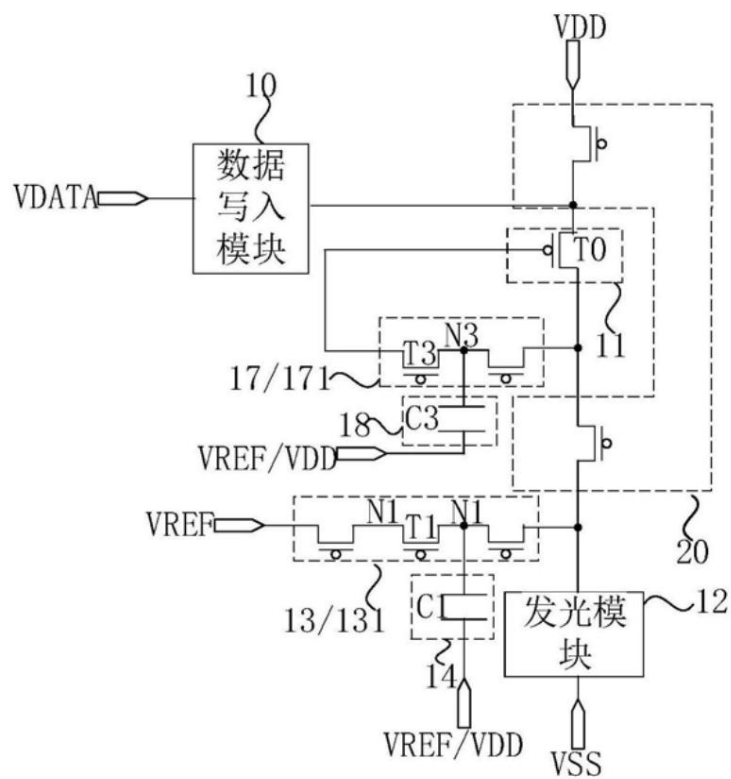


Figure 4



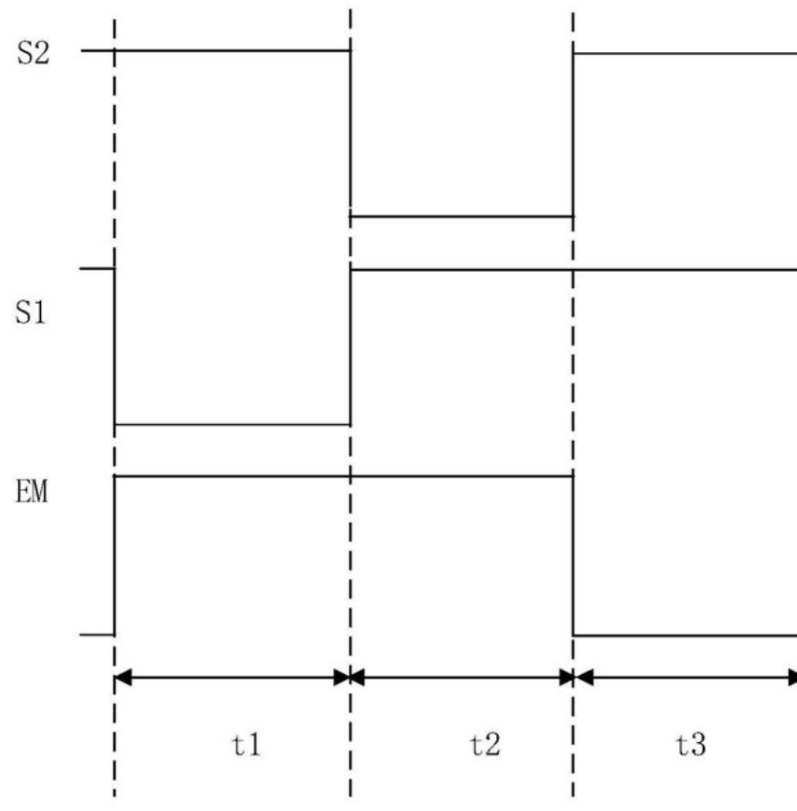


Figure 6

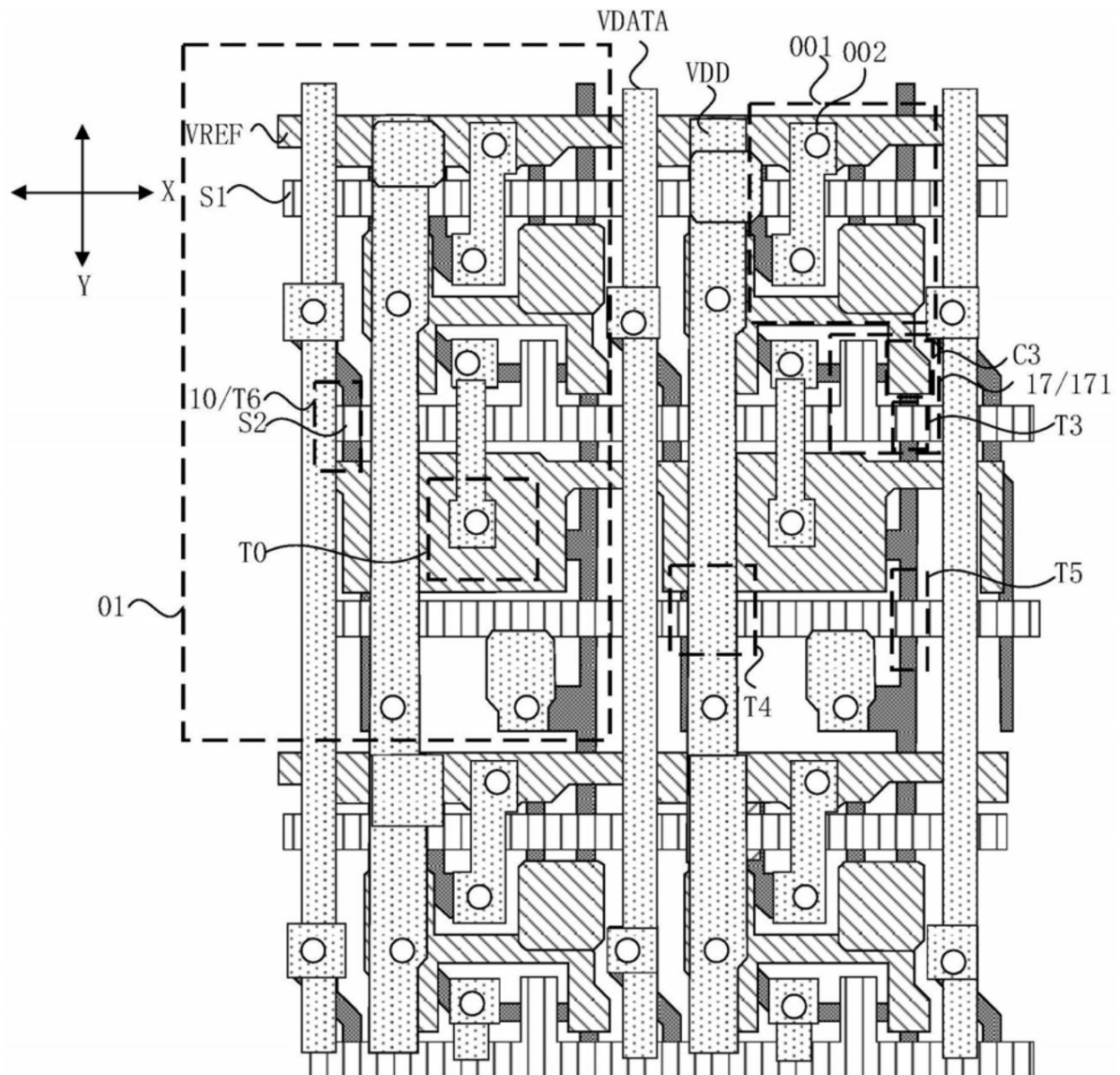


Figure 7

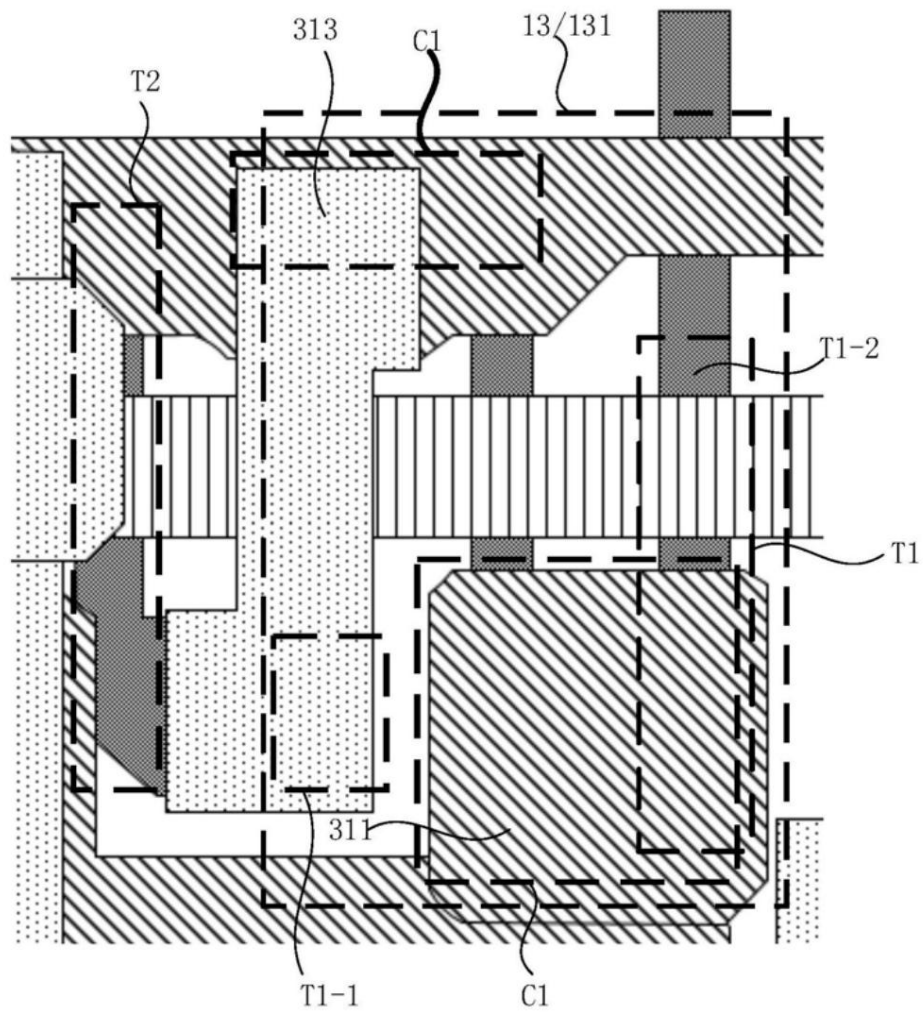


Figure 8

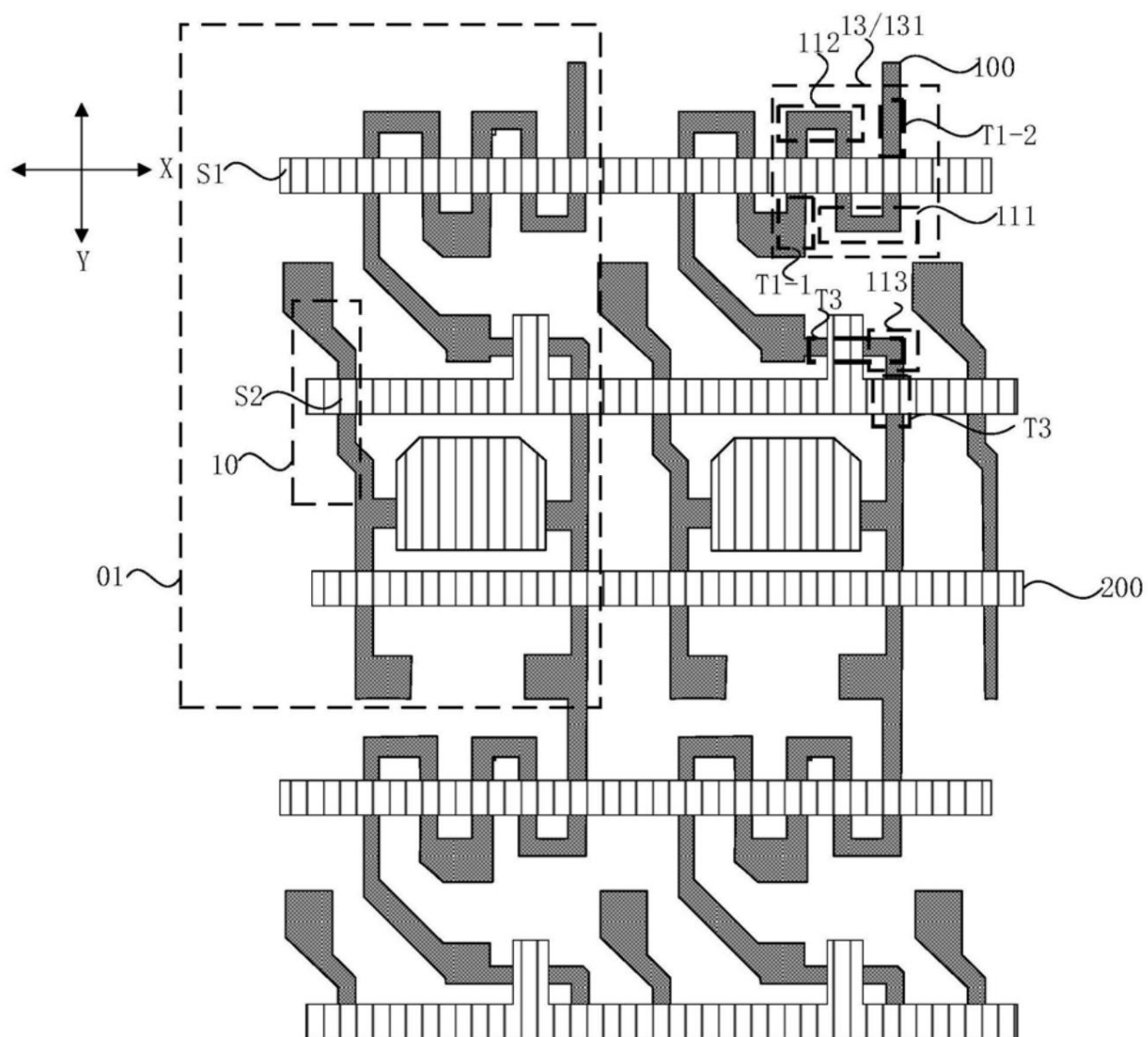


Figure 9

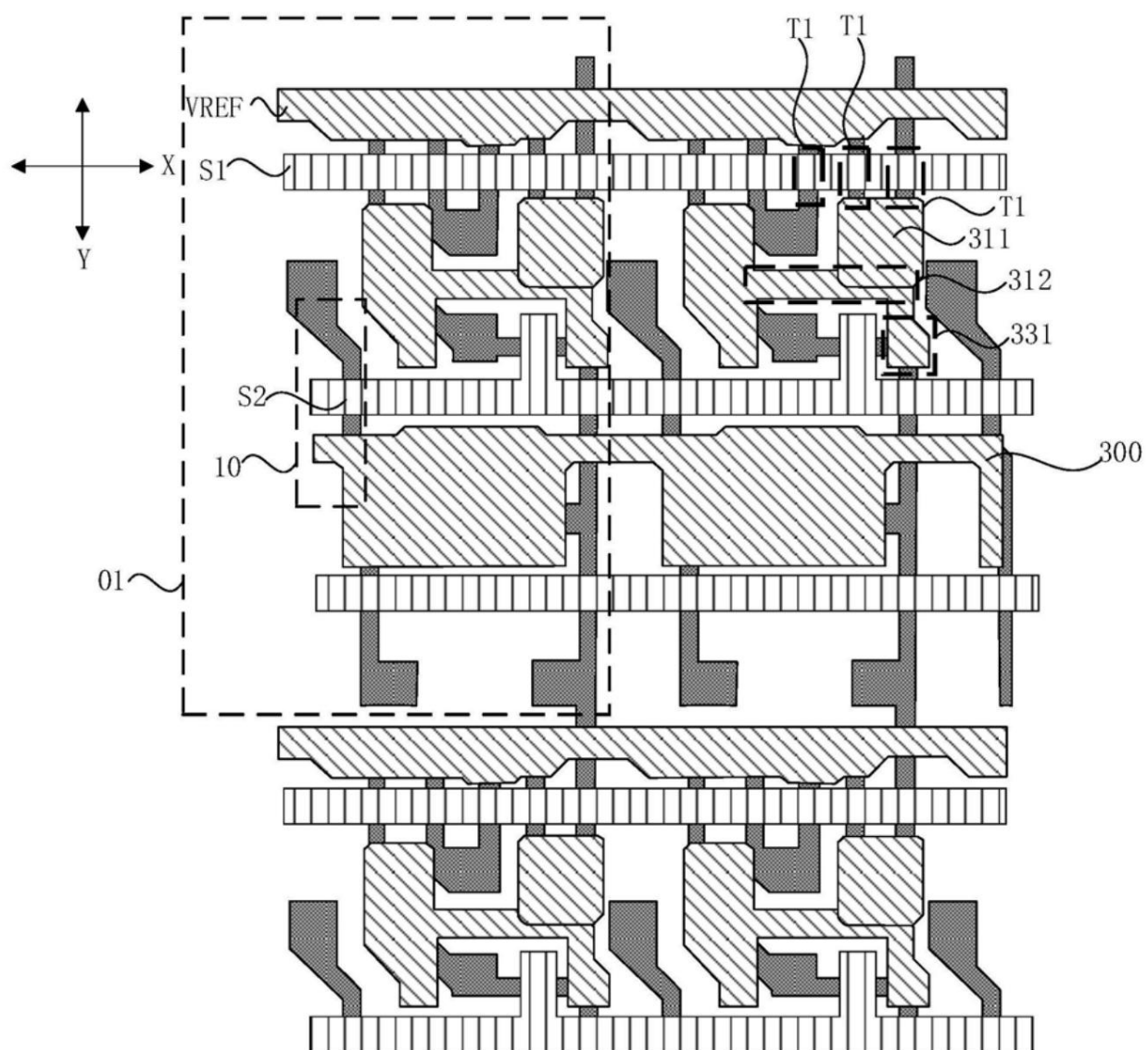


Figure 10

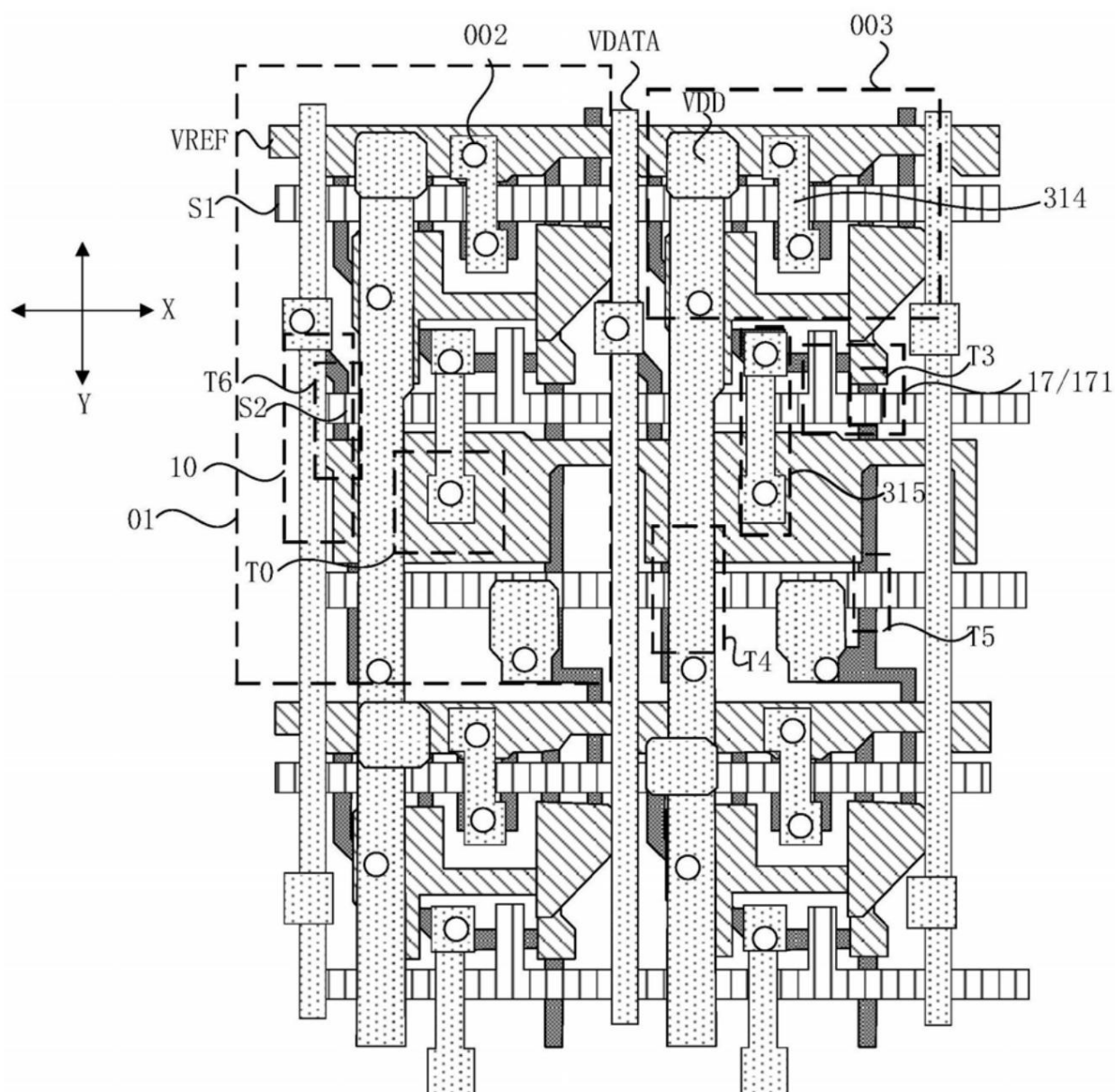


Figure 11

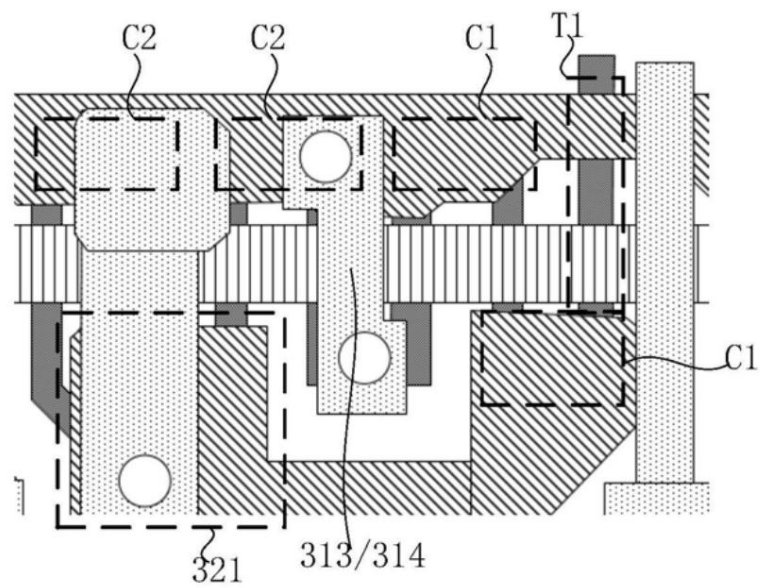


Figure 12

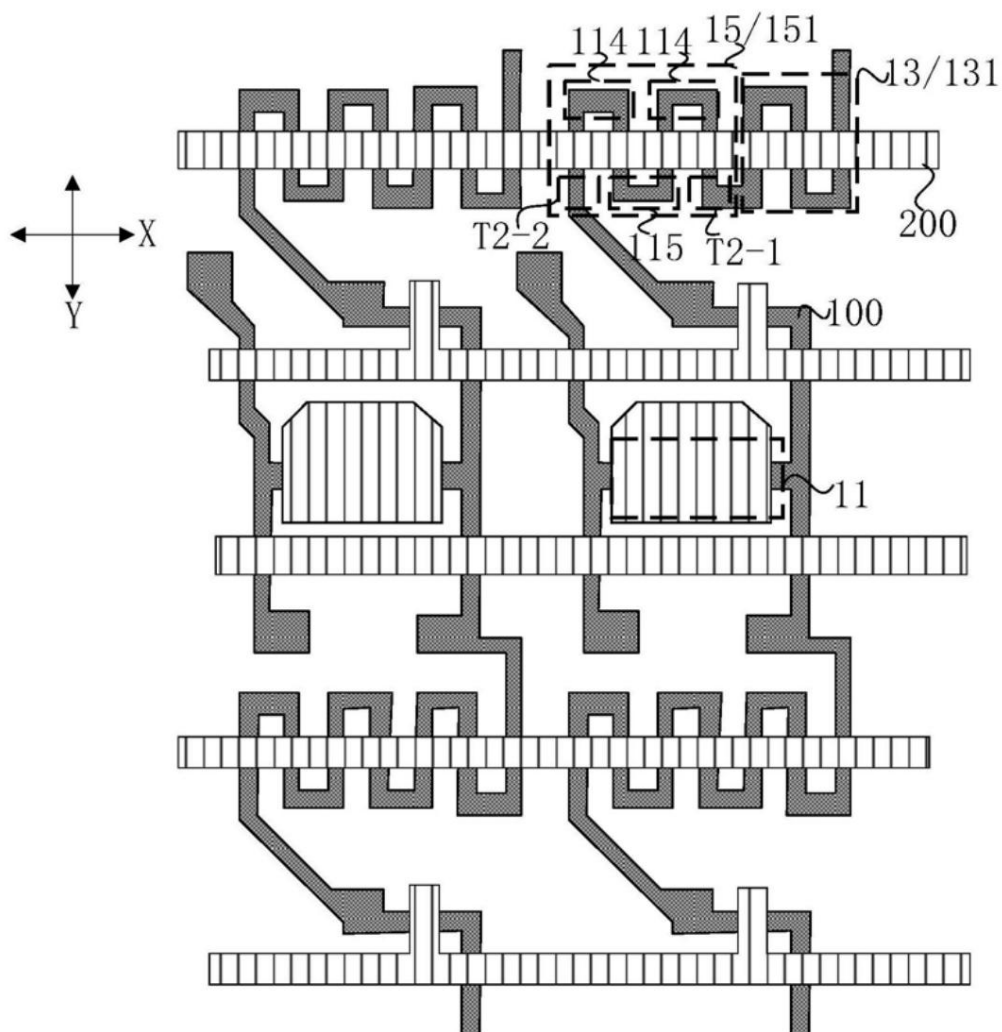


Figure 13

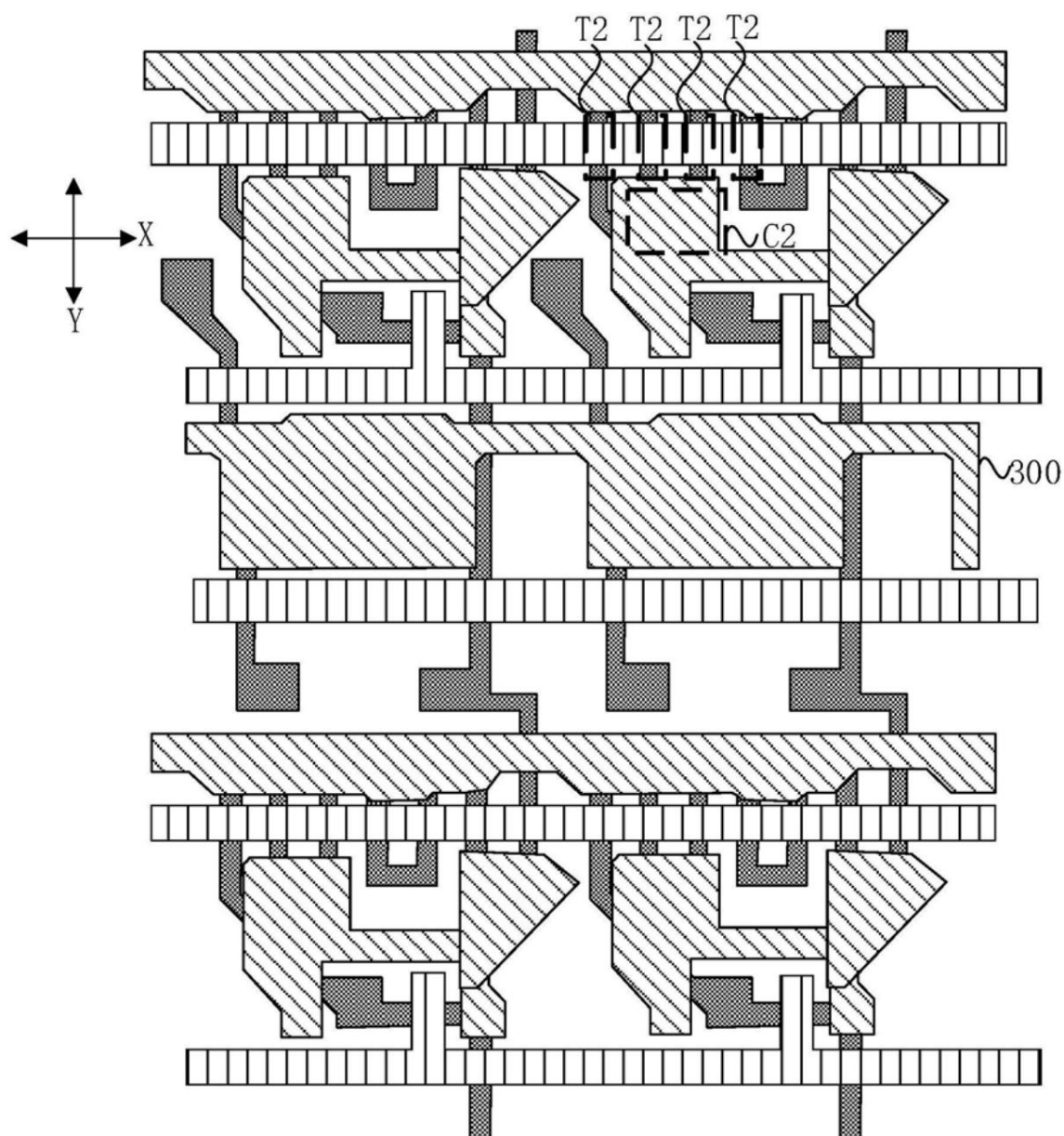


Figure 14

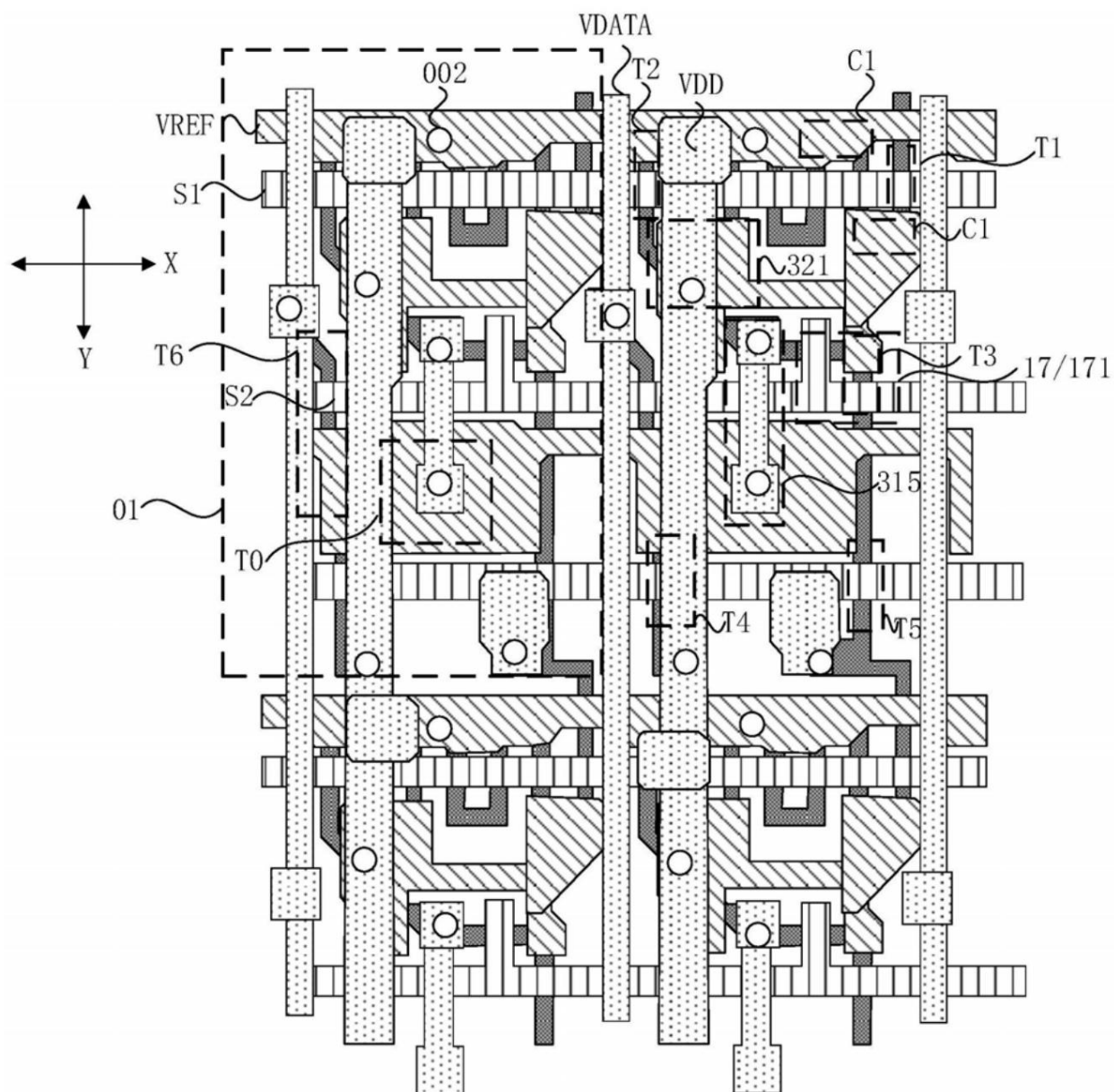


Figure 15

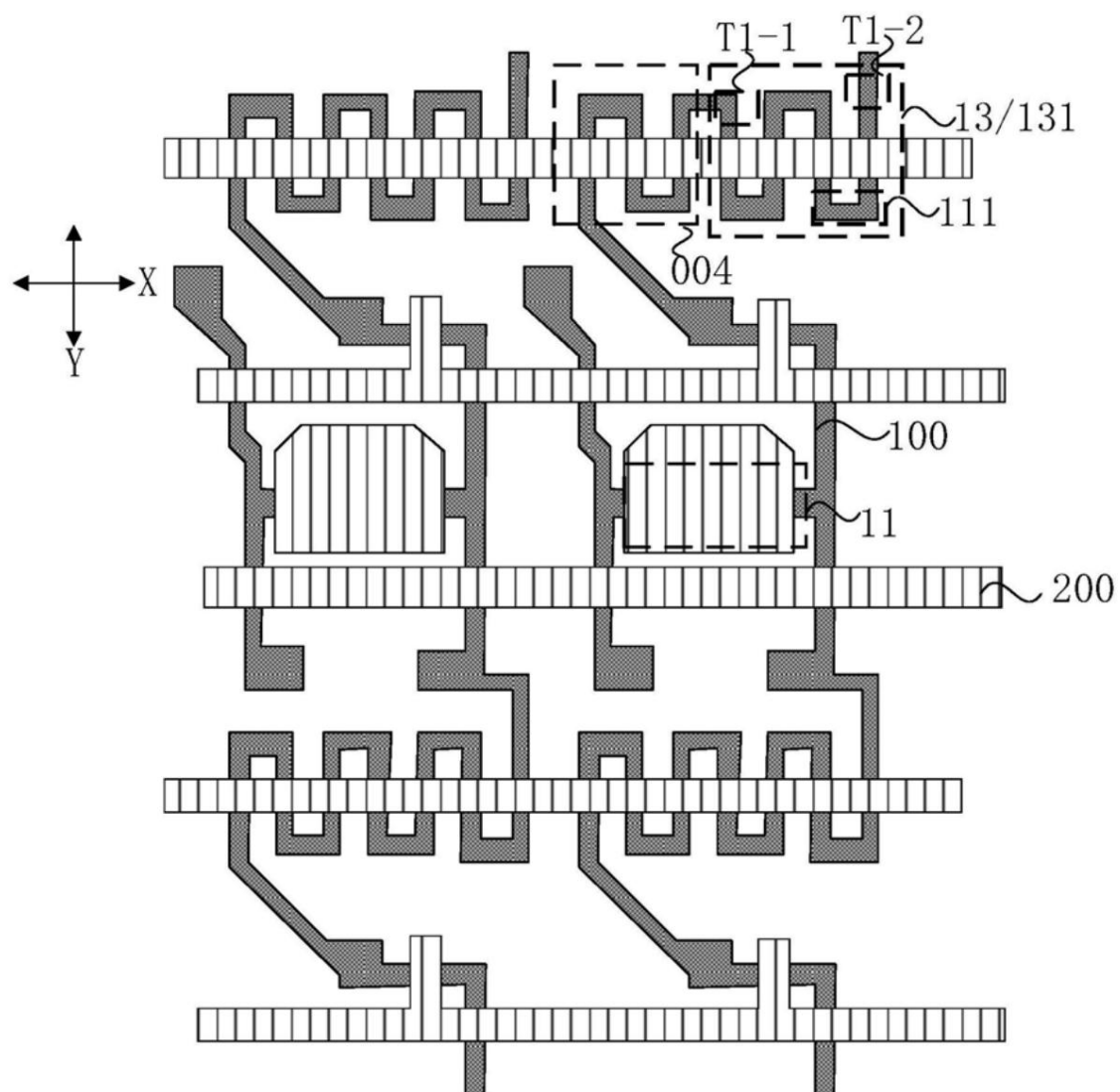


Figure 16

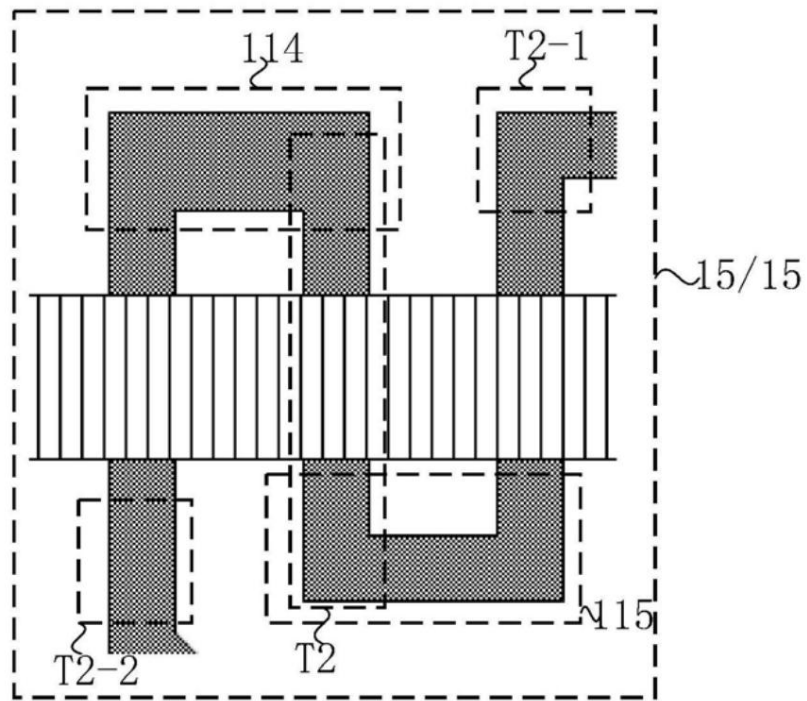


Figure 17

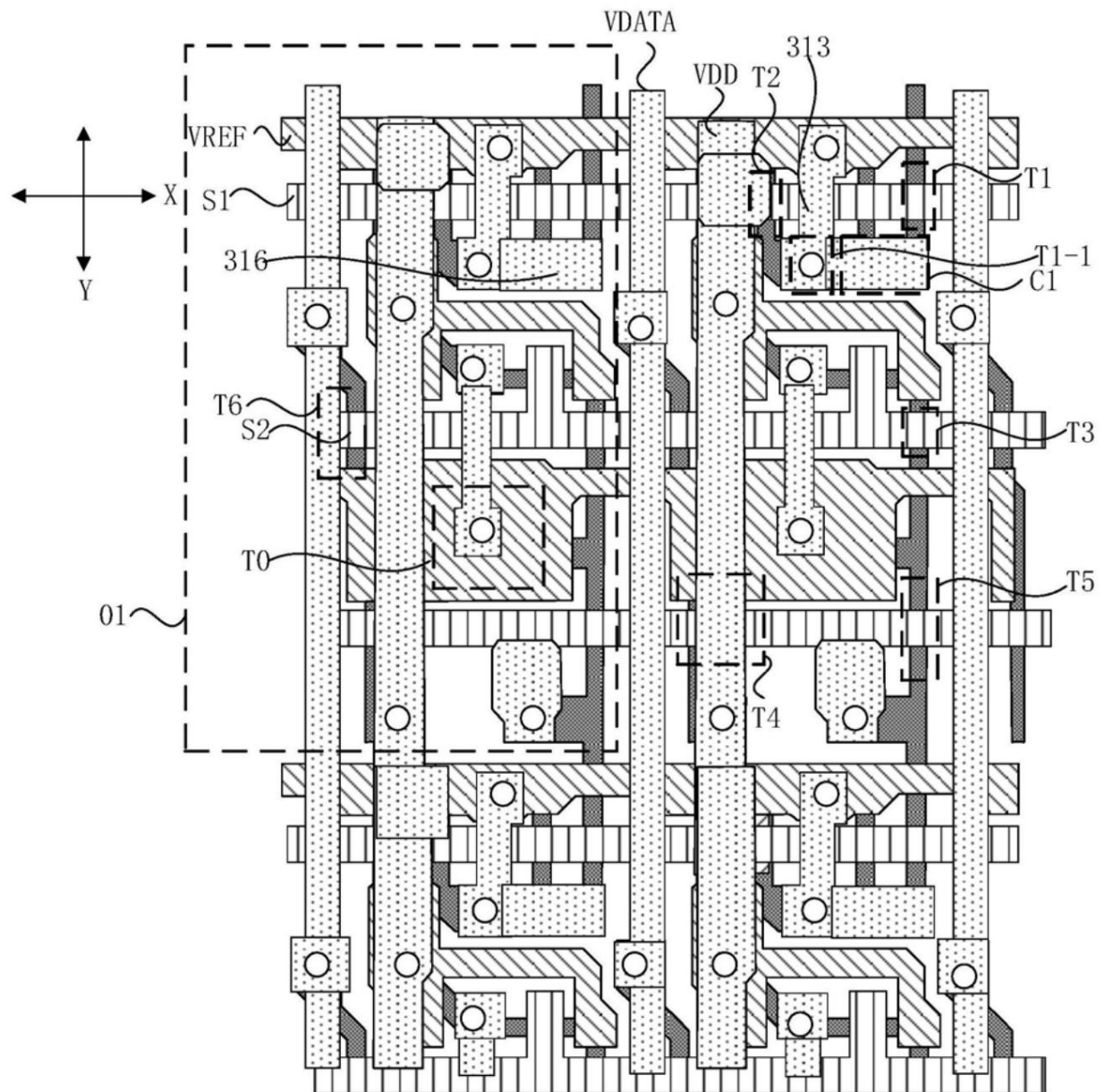


Figure 18



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(71) 申请人 云谷(固安)科技有限公司

地址 065500 河北省廊坊市固安县新兴产业示范区

(72) 发明人 田苗苗 马志丽 赵虹 庞玉乾
朱正勇

(74) 专利代理机构 北京远智汇知识产权代理有限公司 11659

代理人 范坤坤

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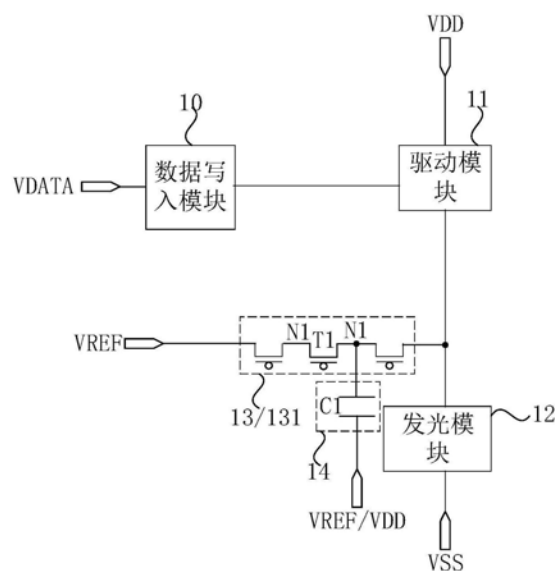
权利要求书3页 说明书13页 附图17页

(54) 发明名称

像素电路及显示面板

(57) 摘要

本发明公开了一种像素电路及显示面板,像素电路包括数据写入模块、驱动模块、发光模块、第一初始化模块和第一屏蔽模块。第一初始化模块的第一端连接初始化信号线,第一初始化模块的第二端连接发光模块的第一端,第一初始化模块包括第一多栅晶体管,第一多栅晶体管包括至少两个串联的第一子晶体管,相邻第一子晶体管通过二者之间的第一中间节点电连接,第一屏蔽模块包括至少一个第一屏蔽电容,第一屏蔽电容的第一端与第一中间节点连接。第一子晶体管的数量越多,第一初始化模块的漏电流越小,进而可以降低发光模块的第一端的电位变化。第一屏蔽电容可以稳定第一中间节点的电位,进而降低第一多栅晶体管的漏电,有利于显示均一性。



1. 一种像素电路,其特征在于,包括:数据写入模块、驱动模块、发光模块、第一初始化模块和第一屏蔽模块;

所述数据写入模块用于在自身控制端所接入信号的控制下向所述驱动模块的控制端写入数据信号;

所述驱动模块和所述发光模块连接于第一电源线和第二电源线之间,所述驱动模块用于根据所述数据信号输出驱动信号驱动所述发光模块发光;

所述第一初始化模块的第一端连接初始化信号线,所述第一初始化模块的第二端连接所述发光模块的第一端,所述第一初始化模块用于在自身控制端所接入信号的控制下向所述发光模块的第一端写入初始化电压;所述第一初始化模块包括第一多栅晶体管,所述第一多栅晶体管包括至少两个串联的第一子晶体管,相邻所述第一子晶体管通过二者之间的第一中间节点电连接;

所述第一屏蔽模块包括至少一个第一屏蔽电容,所述第一屏蔽电容的第一端与至少一个所述第一中间节点连接,所述第一屏蔽电容的第二端接入固定电压。

2. 根据权利要求1所述的像素电路,其特征在于,所述第一屏蔽电容的第二端与所述初始化信号线电连接,或者所述第一屏蔽电容的第二端与所述第一电源线电连接。

3. 根据权利要求1所述的像素电路,其特征在于,所述第一多栅晶体管的有源层的线宽小于第一设定阈值;

优选的,所述驱动模块包括驱动晶体管,所述第一设定阈值等于所述驱动晶体管的有源层的线宽。

4. 根据权利要求1所述的像素电路,其特征在于,还包括第二初始化模块和第二屏蔽模块;

所述第二初始化模块的第一端连接所述初始化信号线,所述第二初始化模块的第二端连接所述驱动模块的控制端,所述第二初始化模块用于在自身控制端所接入信号的控制下向所述驱动模块的控制端写入所述初始化电压;所述第二初始化模块包括第二多栅晶体管,所述第二多栅晶体管包括至少两个串联的第二子晶体管,相邻所述第二子晶体管通过二者之间的第二中间节点电连接;

所述第二屏蔽模块包括至少一个第二屏蔽电容,所述第二屏蔽电容的第一端与至少一个所述第二中间节点连接,所述第二屏蔽电容的第二端接入固定电压;

优选的,所述第二屏蔽电容的第二端与所述初始化信号线电连接,或者所述第二屏蔽电容的第二端与所述第一电源线电连接;

优选的,所述第二多栅晶体管的有源层的线宽小于第二设定阈值;

和/或,所述像素电路还包括补偿模块和第三屏蔽模块,所述补偿模块用于在自身控制端所接入信号的控制下对所述驱动模块包括的驱动晶体管的阈值电压进行补偿;

所述补偿模块包括第三多栅晶体管,所述第三多栅晶体管包括至少两个串联的第三子晶体管,相邻所述第三子晶体管通过二者之间的第三中间节点电连接;

所述第三屏蔽模块包括至少一个第三屏蔽电容,所述第三屏蔽电容的第一端与至少一个所述第三中间节点连接,所述第三屏蔽电容的第二端接入固定电压;

优选的,所述第三屏蔽电容的第二端与所述初始化信号线电连接,或者所述第三屏蔽电容的第二端与所述第一电源线电连接。

5. 一种显示面板, 其特征在于, 包括权利要求1-4任一项所述的像素电路, 还包括第一电源线、数据线、初始化信号线、第一扫描线 and 第二扫描线, 所述第一电源线、所述数据线沿第一方向延伸, 所述初始化信号线、所述第一扫描线和所述第二扫描线沿第二方向延伸, 所述第一方向和所述第二方向相交;

优选的, 所述像素电路阵列排布, 所述第一方向为所述像素电路排布的列方向, 所述第二方向为所述像素电路排布的行方向, 每行所述像素电路中所述第一初始化模块的控制端连接同一条所述第一扫描线, 每行像素电路的第一初始化模块的第一端连接同一条所述初始化信号线, 每行所述像素电路的数据写入模块的控制端连接同一条所述第二扫描线, 每列所述像素电路的数据写入模块的第一端连接同一条所述数据线, 每列所述像素电路连接同一条第一电源线; 同一行所述像素电路连接的所述第一扫描线位于所述初始化信号线和所述第二扫描线之间。

6. 根据权利要求5所述的显示面板, 其特征在于, 所述第一多栅晶体管的至少一个所述第一中间节点与第一固定电位结构交叠形成至少一个第一屏蔽电容, 所述第一多栅晶体管的所述第一中间节点包括第一多栅晶体管的有源层中连接相邻第一子晶体管的所述第一有源部;

优选的, 所述第一有源部包括位于与同一所述像素电路电连接的所述第一扫描线和所述第二扫描线之间的第一子有源部;

所述第一固定电位结构包括位于与同一所述像素电路电连接的所述第一扫描线、所述第二扫描线之间的第一固定电位部, 所述第一固定电位部与所述第一电源线电连接;

所述第一固定电位部与所述第一子有源部交叠形成一所述第一屏蔽电容。

7. 根据权利要求6所述的显示面板, 其特征在于, 所述数据线和所述第一电源线沿所述第二方向排布, 所述第一多栅晶体管位于所述第一多栅晶体管所属像素电路所连接的所述第一电源线远离所述数据线的一侧;

所述第一固定电位结构还包括连接所述第一电源线和所述第一固定电位部的第一连接部, 所述第一连接部沿所述第二方向延伸, 同一所述像素电路中, 所述第一子有源部位于所述第一连接部靠近所述像素电路所连接的所述第一扫描线的一侧。

8. 根据权利要求6所述的显示面板, 其特征在于, 所述第一多栅晶体管包括至少三个串联的所述第一子晶体管, 所述第一有源部包括位于所述第一扫描线远离所述第二扫描线一侧的第二子有源部;

所述第二子有源部与所述初始化信号线交叠形成一所述第一屏蔽电容;

优选的, 所述像素电路包括第二连接部, 所述第二连接部沿所述第一方向延伸, 所述第二连接部的一端连接所述初始化信号线, 另一端连接所述第一多栅晶体管的第一极, 所述第一多栅晶体管的第二极连接所述发光模块的第一端。

9. 根据权利要求7所述的显示面板, 其特征在于, 所述像素电路还包括补偿模块和第三屏蔽模块, 所述补偿模块包括第三多栅晶体管, 所述第三多栅晶体管包括至少两个串联的第三子晶体管, 所述第三多栅晶体管的至少一个第三中间节点与第三固定电位结构交叠形成至少一个第三屏蔽电容, 所述第三多栅晶体管的第三中间节点包括第三多栅晶体管的有源层中连接相邻第三子晶体管的第三有源部;

优选的, 所述第三有源部包括与同一所述像素电路连接的所述第一扫描线和所述第二扫描线之间的至少一个第三子有源部, 所述第三固定电位结构包括至少一个第三固定电位

部,所述第三固定电位部与所述第一连接部连接,同一所述像素电路中,所述第三子有源部和所述第三固定电位部位于所述第一连接部靠近所述像素电路连接的所述第二扫描线的一侧,所述第三子有源部与对应的所述第三固定电位部交叠形成所述第三屏蔽电容。

10. 根据权利要求5或6所述的显示面板,其特征在于,所述像素电路还包括第二初始化模块和第二屏蔽模块;所述第二初始化模块包括第二多栅晶体管,所述第二多栅晶体管包括至少两个串联的第二子晶体管,所述第二多栅晶体管的至少一个第二中间节点与第二固定电位结构交叠形成至少一个第二屏蔽电容,所述第二多栅晶体管的第二中间节点包括第二多栅晶体管的有源层中连接相邻第二子晶体管的第二有源部;

优选的,所述第二有源部包括位于与同一所述像素电路连接的所述第一扫描线远离所述第二扫描线一侧的至少一个第四子有源部;

所述第四子有源部与所述初始化信号线交叠形成一所述第二屏蔽电容;

优选的,所述像素电路包括第三连接部和第四连接部,所述第三连接部和所述第四连接部均沿所述第一方向延伸,所述第三连接部的一端连接所述初始化信号线,另一端连接所述第二多栅晶体管的第一极,所述第四连接部的一端连接所述第二多栅晶体管的第二极,另一端连接所述驱动模块的控制端;

优选的,所述第三连接部与第二连接部为同一结构;

优选的,所述第二多栅晶体管包括至少三个串联的所述第二子晶体管,所述第二有源部包括位于与同一所述像素电路电连接的所述第一扫描线和所述第二扫描线之间的第五子有源部;

所述第二固定电位结构包括位于与同一所述像素电路电连接的所述第一扫描线、所述第二扫描线之间的第二固定电位部,所述第二固定电位部与所述第一电源线电连接;

所述第二固定电位部与所述第五子有源部交叠形成一所述第二屏蔽电容。

像素电路及显示面板

技术领域

[0001] 本发明实施例涉及显示技术领域,尤其涉及一种像素电路及显示面板。

背景技术

[0002] 随着显示产品的发展,伴随着对显示产品高刷新频率的需求日益增大,低灰阶显示性能在显示产品中日益重要。

[0003] 目前的显示面板通常包括多个像素电路,现有显示面板在低灰阶下进行显示时,容易出现发光不均的问题,影响显示的质量。

发明内容

[0004] 本发明提供一种像素电路及显示面板,以实现降低第一初始化模块的漏电,提高显示均一性,提升显示画质。

[0005] 第一方面,本发明实施例提供了一种像素电路,包括:数据写入模块、驱动模块、发光模块、第一初始化模块和第一屏蔽模块;

[0006] 数据写入模块用于在自身控制端所接入信号的控制下向驱动模块的控制端写入数据信号;

[0007] 驱动模块和发光模块连接于第一电源线和第二电源线之间,驱动模块用于根据数据信号输出驱动信号驱动发光模块发光;

[0008] 第一初始化模块的第一端连接初始化信号线,第一初始化模块的第二端连接发光模块的第一端,第一初始化模块用于在自身控制端所接入信号的控制下向发光模块的第一端写入初始化电压;第一初始化模块包括第一多栅晶体管,第一多栅晶体管包括至少两个串联的第一子晶体管,相邻第一子晶体管通过二者之间的第一中间节点电连接;

[0009] 第一屏蔽模块包括至少一个第一屏蔽电容,第一屏蔽电容的第一端与至少一个中间节点连接,第一屏蔽电容的第二端接入固定电压。

[0010] 可选的,第一屏蔽电容的第二端与初始化信号线电连接,或者第一屏蔽电容的第二端与第一电源线电连接。

[0011] 可选的,第一多栅晶体管的有源层的线宽小于第一设定阈值;

[0012] 可选的,驱动模块包括驱动晶体管,第一设定阈值等于驱动晶体管的有源层的线宽。

[0013] 可选的,像素电路还包括第二初始化模块和第二屏蔽模块;

[0014] 第二初始化模块的第一端连接初始化信号线,第二初始化模块的第二端连接驱动模块的控制端,第二初始化模块用于在自身控制端所接入信号的控制下向驱动模块的控制端写入初始化电压;第二初始化模块包括第二多栅晶体管,第二多栅晶体管包括至少两个串联的第二子晶体管,相邻第二子晶体管通过二者之间的第二中间节点电连接;

[0015] 第二屏蔽模块包括至少一个第二屏蔽电容,第二屏蔽电容的第一端与至少一个第二中间节点连接,第二屏蔽电容的第二端接入固定电压;

[0016] 可选的,第二屏蔽电容的第二端与初始化信号线电连接,或者第二屏蔽电容的第二端与第一电源线电连接;

[0017] 可选的,第二多栅晶体管的有源层的线宽小于第二设定阈值;

[0018] 和/或,像素电路还包括补偿模块和第三屏蔽模块,补偿模块用于在自身控制端所接入信号的控制下对驱动模块包括的驱动晶体管的阈值电压进行补偿;

[0019] 补偿模块包括第三多栅晶体管,第三多栅晶体管包括至少两个串联的第三子晶体管,相邻第三子晶体管通过二者之间的第三中间节点电连接;

[0020] 第三屏蔽模块包括至少一个第三屏蔽电容,第三屏蔽电容的第一端与至少一个第三中间节点连接,第三屏蔽电容的第二端接入固定电压;

[0021] 可选的,第三屏蔽电容的第二端与初始化信号线电连接,或者第三屏蔽电容的第二端与第一电源线电连接。

[0022] 第二方面,本发明实施例还提供了一种显示面板,该显示面板包括第一方面任一项的像素电路,还包括第一电源线、数据线、初始化信号线、第一扫描线 and 第二扫描线,第一电源线、数据线沿第一方向延伸,初始化信号线、第一扫描线 and 第二扫描线沿第二方向延伸,第一方向 and 第二方向相交;

[0023] 可选的,像素电路阵列排布,第一方向为像素电路排布的列方向,第二方向为像素电路排布的行方向,每行像素电路中第一初始化模块的控制端连接同一条第一扫描线,每行像素电路的第一初始化模块的第一端连接同一条初始化信号线,每行像素电路的数据写入模块的控制端连接同一条第二扫描线,每列像素电路的数据写入模块的第一端连接同一条数据线,每列像素电路连接同一条第一电源线;同一行像素电路连接的第一扫描线位于初始化信号线 and 第二扫描线之间。

[0024] 可选的,第一多栅晶体管的至少一个第一中间节点与第一固定电位结构交叠形成至少一个第一屏蔽电容,第一多栅晶体管的第一中间节点包括第一多栅晶体管的有源层中连接相邻第一子晶体管的第一有源部;

[0025] 可选的,第一有源部包括位于与同一像素电路电连接的第一扫描线 and 第二扫描线之间的第一子有源部;

[0026] 第一固定电位结构包括位于与同一像素电路电连接的第一扫描线、第二扫描线之间的第一固定电位部,第一固定电位部与第一电源线电连接;

[0027] 第一固定电位部与第一子有源部交叠形成一第一屏蔽电容。

[0028] 可选的,数据线和第一电源线沿第二方向排布,第一多栅晶体管位于第一多栅晶体管所属像素电路所连接的第一电源线远离数据线的一侧;

[0029] 第一固定电位结构还包括连接第一电源线和第一固定电位部的第一连接部,第一连接部沿第二方向延伸,同一像素电路中,第一子有源部位于第一连接部靠近像素电路所连接的第一扫描线的一侧。

[0030] 可选的,第一多栅晶体管包括至少三个串联的第一子晶体管,第一有源部包括位于第一扫描线远离第二扫描线一侧的第二子有源部;

[0031] 第二子有源部与初始化信号线交叠形成一第一屏蔽电容;

[0032] 可选的,像素电路包括第二连接部,第二连接部沿第一方向延伸,第二连接部的一端连接初始化信号线,另一端连接第一多栅晶体管的第一极,第一多栅晶体管的第二极连

接发光模块的第一端。

[0033] 可选的,像素电路还包括补偿模块和第三屏蔽模块,补偿模块包括第三多栅晶体管,第三多栅晶体管包括至少两个串联的第三子晶体管,第三多栅晶体管的至少一个第三中间节点与第三固定电位结构交叠形成至少一个第三屏蔽电容,第三多栅晶体管的第三中间节点包括第三多栅晶体管的有源层中连接相邻第三子晶体管的第三有源部;

[0034] 可选的,第三有源部包括与同一像素电路连接的第一扫描线和第二扫描线之间的至少一个第三子有源部,第三固定电位结构包括至少一个第三固定电位部,第三固定电位部与第一连接部连接,同一像素电路中,第三子有源部和第三固定电位部位于第一连接部靠近像素电路连接的第二扫描线的一侧,第三子有源部与对应的第三固定电位部交叠形成第三屏蔽电容。

[0035] 可选的,像素电路还包括第二初始化模块和第二屏蔽模块;第二初始化模块包括第二多栅晶体管,第二多栅晶体管包括至少两个串联的第二子晶体管,第二多栅晶体管的至少一个第二中间节点与第二固定电位结构交叠形成至少一个第二屏蔽电容,第二多栅晶体管的第二中间节点包括第二多栅晶体管的有源层中连接相邻第二子晶体管的第二有源部;

[0036] 可选的,第二有源部包括位于与同一像素电路连接的第一扫描线远离第二扫描线一侧的至少一个第四子有源部;

[0037] 第四子有源部与初始化信号线交叠形成一第二屏蔽电容;

[0038] 可选的,像素电路包括第三连接部和第四连接部,第三连接部和第四连接部均沿第一方向延伸,第三连接部的一端连接初始化信号线,另一端连接第二多栅晶体管的第一极,第四连接部的一端连接第二多栅晶体管的第二极,另一端连接驱动模块的控制端;

[0039] 可选的,第三连接部与第二连接部为同一结构。

[0040] 可选的,第二多栅晶体管包括至少三个串联的第二子晶体管,第二有源部包括位于与同一像素电路电连接的第一扫描线和第二扫描线之间的第五子有源部;

[0041] 第二固定电位结构包括位于与同一像素电路电连接的第一扫描线、第二扫描线之间的第二固定电位部,第二固定电位部与第一电源线电连接;

[0042] 第二固定电位部与第五子有源部交叠形成一第二屏蔽电容。

[0043] 本发明实施例提供了一种像素电路和显示面板,像素电路包括数据写入模块、驱动模块、发光模块、第一初始化模块和第一屏蔽模块。第一初始化模块用于在自身控制端所接入信号的控制下向发光模块的第一端写入初始化电压,第一初始化模块包括第一多栅晶体管,第一多栅晶体管包括至少两个串联的第一子晶体管。相邻第一子晶体管通过二者之间的第一中间节点电连接,第一屏蔽模块包括至少一个第一屏蔽电容,第一屏蔽电容的第一端与至少一个第一中间节点连接,第一屏蔽电容的第二端接入固定电压。第一初始化模块的第一多栅晶体管包括至少两个串联的第一子晶体管,使得第一初始化模块的漏电流较小,进而可以减小发光模块的第一端的电位变化。同时,至少一个第一屏蔽电容可以稳定第一多栅晶体管的第一中间节点的电位,降低第一多栅晶体管的控制端的电位变化对第一中间节点电位的影响,进而进一步降低第一初始化模块的漏电,维持发光模块的第一端的电位的稳定,提高显示均一性。

附图说明

- [0044] 图1是本发明实施例提供的一种像素电路的结构示意图；
- [0045] 图2是本发明实施例提供的另一种像素电路的结构示意图；
- [0046] 图3是本发明实施例提供的另一种像素电路的结构示意图；
- [0047] 图4是本发明实施例提供的另一种像素电路的结构示意图；
- [0048] 图5是本发明实施例提供的另一种像素电路的结构示意图；
- [0049] 图6是本发明实施例提供的一种像素电路的时序图；
- [0050] 图7是本发明实施例提供的一种显示面板的结构示意图；
- [0051] 图8是本发明实施例提供的一种显示面板的局部放大图；
- [0052] 图9是本发明实施例提供的一种显示面板中有源层和第一金属层的结构示意图；
- [0053] 图10是本发明实施例提供的一种显示面板中有源层、第一金属层和第二金属层的结构示意图；
- [0054] 图11是本发明实施例提供的另一种显示面板的结构示意图；
- [0055] 图12是本发明实施例提供的另一种显示面板的局部放大图；
- [0056] 图13是本发明实施例提供的一种显示面板中有源层和第一金属层的结构示意图；
- [0057] 图14是本发明实施例提供的另一种显示面板中有源层、第一金属层和第二金属层的结构示意图；
- [0058] 图15是本发明实施例提供的另一种显示面板的结构示意图；
- [0059] 图16是本发明实施例提供的一种显示面板中有源层和第一金属层的结构示意图；
- [0060] 图17是本发明实施例提供的另一种显示面板的局部放大图；
- [0061] 图18是本发明实施例提供的另一种显示面板的结构示意图。

具体实施方式

[0062] 下面结合附图和实施例对本发明作进一步的详细说明。可以理解的是,此处所描述的具体实施例仅仅用于解释本发明,而非对本发明的限定。另外还需要说明的是,为了便于描述,附图中仅示出了与本发明相关的部分而非全部结构。

[0063] 正如背景技术中所述,现有显示面板在进行显示时,存在显示均一性差的问题,影响显示效果。经发明人研究发现,出现上述问题的原因在于,现有像素电路与发光模块的第一端连接的用于初始化发光模块的晶体管,漏电较为严重,导致在低灰阶下,发光模块发光的均一性较差。初始化发光模块的晶体管大多为单栅结构,单栅结构的晶体管,在其控制端的电压发生变化时,晶体管第一极和第二极的电压会因控制端电压的变化而产生较大变化,使得第一极和第二极的电压不等,产生较大的漏电流,从而使得发光模块的第一端的电压变化,降低显示均一性。

[0064] 基于上述原因,本发明实施例提供了一种像素电路。图1为本发明实施例提供的一种像素电路的结构示意图,参考图1,像素电路包括数据写入模块10、驱动模块11、发光模块12、第一初始化模块13和第一屏蔽模块14;

[0065] 数据写入模块10用于在自身控制端所接入信号的控制下向驱动模块11的控制端

写入数据信号;

[0066] 驱动模块11和发光模块12连接于第一电源线VDD和第二电源线VSS之间,驱动模块11用于根据数据信号输出驱动信号驱动发光模块12发光;

[0067] 第一初始化模块13的第一端连接初始化信号线VREF,第一初始化模块13的第二端连接发光模块12的第一端,第一初始化模块13用于在自身控制端所接入信号的控制下向发光模块12的第一端写入初始化电压;第一初始化模块13包括第一多栅晶体管131,第一多栅晶体管131包括至少两个串联的第一子晶体管T1,相邻第一子晶体管T1通过二者之间的第一中间节点N1电连接;

[0068] 第一屏蔽模块14包括至少一个第一屏蔽电容C1,第一屏蔽电容C1的第一端与至少一个第一中间节点N1连接,第一屏蔽电容C1的第二端接入固定电压。

[0069] 其中,发光模块11可以为有机发光二极管(Organic Light Emitting Diode, OLED),发光模块11的第一端为OLED的阳极,驱动信号可以为驱动电流,OLED在驱动电流的驱动下发光。当第一多栅晶体管131包括两个串联的第一子晶体管T1时,第一多栅晶体管131为双栅晶体管,当第一多栅晶体管131包括三个串联的第一子晶体管T1时,第一多栅晶体管131为三栅晶体管,依次类推。多栅晶体管存在一个问题,即在多栅晶体管关断时,多栅晶体管的中间节点浮置,使得该中间节点电位容易受到显示面板中其他信号的影响,造成多栅晶体管中间节点的电位不稳定,漏电流仍可能会较大,导致显示面板的发光均一性较差,影响显示画质。因此,本实施例中,通过在第一中间节点N1处连接第一屏蔽电容C1,以稳定第一中间节点的电位。数据写入模块10还与数据线VDATA连接,数据线VDATA用于提供数据信号。可选的,第一屏蔽电容C1的第二端与初始化信号线VREF电连接,或者第一屏蔽电容C1的第二端与第一电源线VDD电连接。

[0070] 本实施例中示例性示出包括三个串联的第一子晶体管T1和一个第一屏蔽电容C1,其中第一个第一子晶体管T1的第一极与初始化信号线VREF连接,第二极与相邻的第二个第一子晶体管T1的第一极连接,第二个第一子晶体管T1的第二极连接相邻的第三个第一子晶体管T1的第一极,第三个第一子晶体管T1的第二极连接发光模块12的第一端,三个第一子晶体管T1的栅极作为第一初始化模块13的控制端。其中,三个第一子晶体管T1的第一极均为源极,第二极均为漏极。第一子晶体管T1可以为N型晶体管,也可以为P型晶体管,本实施例中示例性示出第一子晶体管T1为P型晶体管。本实施例中第一多栅晶体管131包括三个第一子晶体管T1时,存在两个第一中间节点N1。在其他实施例中,第一多栅晶体管131包括两个第一子晶体管T1时,存在一个第一中间节点N1,第一多栅晶体管131包括四个第一子晶体管T1时,存在三个第一中间节点N1,以此类推。每一第一中间节点N1处均可连接一个第一屏蔽电容C1。用户可根据需求设定第一屏蔽电容C1的数量。第一屏蔽电容C1在第一多栅晶体管131关断时可以稳定第一多栅晶体管131的第一中间节点N1的电位,从而降低第一多栅晶体管131的漏电,进而保证发光模块12的第一端的电位的稳定,有利于提高显示的均一性。

[0071] 像素电路的工作过程可以包括初始化阶段、数据写入阶段和发光阶段。在初始化阶段,串联连接的多个第一子晶体管T1在其栅极连接的信号的控制下导通,将初始化信号线VREF提供的初始化电压写入发光模块12的第一端,实现对发光模块12的初始化。在数据写入阶段,数据写入模块10在自身控制端所接入信号的控制下导通,进而向驱动模块11的控制端写入数据信号,其中数据信号为数据电压。在发光阶段,驱动模块11根据其控制端的

电压和第一电源线VDD提供的第一电源电压产生驱动电流,驱动发光模块12发光。在发光阶段,第一多栅晶体管131处于关断状态,第一屏蔽电容C1可以稳定第一多栅晶体管131的第一中间节点N1的电位,进而降低第一多栅晶体管131的漏电,保证发光模块12的第一端的电位的稳定,有利于提高显示均一性。

[0072] 本实施例提供的像素电路的第一初始化模块的第一多栅晶体管包括至少两个串联的第一子晶体管,使得第一初始化模块的漏电流较小,进而可以减小发光模块的第一端的电位变化。同时,至少一个第一屏蔽电容可以稳定第一多栅晶体管的第一中间节点的电位,降低第一多栅晶体管的控制端的电位变化对第一中间节点电位的影响,进而进一步降低第一初始化模块的漏电,维持发光模块的第一端的电位的稳定,进而减小驱动电流的变化,提高显示均一性。

[0073] 在上述技术方案的基础上,可选的,第一多栅晶体管的有源层的线宽小于第一设定阈值。

[0074] 有源层的线宽为与电流流经方向垂直方向的有源层的宽度,第一多栅晶体管的有源层的线宽小于第一设定阈值,可以在有限的面积内实现多栅结构的设置,有利于保证显示面板较高的像素密度,第一设定阈值可根据需求进行设定。

[0075] 图2为本发明实施例提供的另一种像素电路的结构示意图,参考图2,可选的,驱动模块11包括驱动晶体管T0,第一设定阈值等于驱动晶体管T0的有源层的线宽。

[0076] 驱动晶体管T0的栅极作为驱动模块11的控制端。第一多栅晶体管131的有源层的线宽小于驱动晶体管T0的有源层的线宽,可以在有限的面积内实现多栅结构的设置。可选的,驱动晶体管T0为单栅晶体管。

[0077] 图3为本发明实施例提供的另一种像素电路的结构示意图,参考图3,可选的,像素电路还包括第二初始化模块15、第二屏蔽模块16;

[0078] 第二初始化模块15的第一端连接初始化信号线VREF,第二初始化模块15的第二端连接驱动模块11的控制端,第二初始化模块15用于在自身控制端所接入信号的控制下向驱动模块11的控制端写入初始化电压;第二初始化模块15包括第二多栅晶体管151,第二多栅晶体管151包括至少两个串联的第二子晶体管T2,相邻第二子晶体管T2通过二者之间的第二中间节点N2电连接;

[0079] 第二屏蔽模块16包括至少一个第二屏蔽电容C2,第二屏蔽电容C2的第一端与至少一个第二中间节点N2连接,第二屏蔽电容C2的第二端接入固定电压;

[0080] 可选的,第二屏蔽电容C2的第二端与初始化信号线VREF电连接,或者第二屏蔽电容C2的第二端与第一电源线VDD电连接;

[0081] 本实施例中示例性示出第二多栅晶体管151包括四个串联的第二子晶体管T2和一个第二屏蔽电容C2,其中第一个第二子晶体管T2的第一极与初始化信号线VREF连接,第一个第二子晶体管T2的第二极与第二个第二子晶体管T2的第一极连接,第二个第二子晶体管T2的第二极与第三个第二子晶体管T2的第一极连接,第三个第二子晶体管T2的第二极与第四个第二子晶体管T2的第一极连接,第四个第二子晶体管T2的第二极与驱动模块11的控制端连接,四个第二子晶体管T2的栅极作为第二初始化模块15的控制端。其中,四个第二子晶体管T2的第一极均为源极,第二极均为漏极。第二子晶体管T2可以为N型晶体管,也可以为P型晶体管,本实施例中示例性示出第二子晶体管T2为P型晶体管。本实施例中,第二多栅晶

体管151包括四个第二子晶体管T2时,第二多栅晶体管151包括三个第二中间节点N2。在其他实施例中,第二多栅晶体管151包括三个第二子晶体管T2时,第二多栅晶体管151包括两个第二中间节点N2,第二多栅晶体管151包括五个第二子晶体管T2时,第二多栅晶体管151包括四个第二中间节点N2,以此类推。每一第二中间节点N2处均可连接一个第二屏蔽电容C2,用户可根据需求设定第二屏蔽电容C2的数量。第二屏蔽电容C2可以稳定第二多栅晶体管151的第二中间节点N2的电位,当第二多栅晶体管151关断时,由于第二屏蔽电容C2的存在,可以降低第二多栅晶体管151的漏电,进而保证驱动模块11的控制端的电位的稳定,进而保证驱动电流的稳定,有利于提高显示均一性。

[0082] 在上述技术方案的基础上,继续参考图3,可选的,第二多栅晶体管151的有源层的线宽小于第二设定阈值。

[0083] 第二多栅晶体管151的有源层的线宽小于第二设定阈值,可以在有限的面积内实现多栅结构的设置。第二设定阈值可根据需求进行设定,第二设定阈值可以等于第一设定阈值。可选的,当驱动模块11包括驱动晶体管时,第二设定阈值等于驱动晶体管的有源层的线宽。第二多栅晶体管151的有源层的线宽小于驱动晶体管的有源层的线宽,可以在有限的面积内实现多栅结构的设置,有利于保证显示面板较高的像素密度。

[0084] 图4为本发明实施例提供的另一种像素电路的结构示意图,参考图4,可选的,像素电路还包括补偿模块17和第三屏蔽模块18,补偿模块17用于在自身控制端所接入信号的控制下对驱动模块11包括的驱动晶体管T0的阈值电压进行补偿;

[0085] 补偿模块17包括第三多栅晶体管171,第三多栅晶体管171包括至少两个串联的第三子晶体管T3,相邻第三子晶体管T3通过二者之间的第三中间节点N3电连接;

[0086] 第三屏蔽模块18包括至少一个第三屏蔽电容C3,第三屏蔽电容C3的第一端与至少一个第三中间节点N3连接,第三屏蔽电容C3的第二端接入固定电压;

[0087] 可选的,第三屏蔽电容C3的第二端与初始化信号线VREF电连接,或者第三屏蔽电容C3的第二端与第一电源线VDD电连接。

[0088] 可选的,像素电路还包括发光控制模块20,发光控制模块20、驱动模块11、发光模块12连接于第一电源线VDD和第二电源线VSS之间,发光控制模块20用于在自身控制端的信号的控制下,控制发光模块12根据驱动模块11输出的驱动信号发光。

[0089] 本实施例中示例性示出第三多栅晶体管171包括两个串联的第三子晶体管T3和一个第三屏蔽电容C3,第一个第三子晶体管T3的第一极与驱动晶体管T0的第二极连接,第二极与第二个第三子晶体管T3的第一极连接,第二个第三子晶体管T3的第二极与驱动晶体管T0的栅极连接。第三子晶体管T3的栅极作为补偿模块13的控制端。其中,两个第三子晶体管T3的第一极均为源极,第二极均为漏极。第三子晶体管T3可以为N型晶体管,也可以为P型晶体管,本实施例中示例性示出第三子晶体管T3为P型晶体管。本实施例中,第三多栅晶体管171包括两个第三子晶体管T3时,第三多栅晶体管171包括一个第三中间节点N3。在其他实施例中,第三多栅晶体管171包括三个第三子晶体管T3时,第三多栅晶体管171包括两个第三中间节点N3,以此类推。每一第三中间节点N3处均可连接一个第三屏蔽电容C3,用户可根据需求设定第三屏蔽电容C3的数量。

[0090] 在数据写入阶段,数据电压经数据写入模块10和补偿模块17写入驱动晶体管T0的栅极,同时,补偿模块17可以对驱动晶体管T0的阈值进行补偿,从而可以使得驱动晶体管T0

的栅极的电压包括与数据电压和阈值电压关联的电压,实现了驱动晶体管T0的数据电压的写入和阈值补偿。且第三屏蔽电容C3可以稳定第三多栅晶体管171的第三中间节点N3的电位,当第三多栅晶体管171关断时,由于第三屏蔽电容C3的存在,可以降低第三多栅晶体管171的漏电,进而保证驱动模块11的控制端的电位的稳定,使得驱动电流的稳定性提高,进而有利于提高显示均一性。

[0091] 图5为本发明实施例提供的另一种像素电路的结构示意图,参考图5,可选的,像素电路还包括存储模块19,存储模块19与驱动模块11的控制端连接,用于存储驱动模块11的控制端的电压。可选的,存储模块19包括存储电容C0,存储电容C0的一端连接第一电源线VDD,存储电容C0的另一端连接驱动模块11的控制端。

[0092] 可选的,发光控制模块20包括第四晶体管T4和第五晶体管T5,第四晶体管T4的第一极连接第一电源线VDD,第四晶体管T4的第二极连接驱动模块11的第一端,第五晶体管T5的第一极连接驱动模块11的第二端,第五晶体管T5的第二极连接发光模块12的第一端,第四晶体管T4和第五晶体管T5的栅极连接发光控制信号线EM。

[0093] 数据写入模块10包括第六晶体管T6,第六晶体管T6的第一极连接数据线VDATA,第六晶体管T6的第二极连接驱动模块11的第一端,第六晶体管T6的栅极连接第二扫描线S2。

[0094] 可选的,第一多栅晶体管131包括的第一子晶体管T1的栅极连接第一扫描线S1,第一屏蔽电容C1连接第一电源线VDD,第二多栅晶体管151的第二子晶体管T2的栅极连接第一扫描线S1,第二屏蔽电容C2连接第一电源线VDD,第三多栅晶体管171包括的第三子晶体管T3的栅极连接第二扫描线,第三屏蔽电容C3连接第一电源线VDD。在本发明其他可选实施例中,第一屏蔽电容C1、第二屏蔽电容C2、第三屏蔽电容C3均可以连接初始化信号线VREF。

[0095] 图6为本发明实施例提供的一种像素电路的时序图,图6所示的时序图适用于图5所示的像素电路。其中,图5所示的像素电路中包括的晶体管均为P型晶体管。参考图5和图6,像素电路的工作过程包括初始化阶段t1、数据写入和阈值补偿阶段t2、发光阶段t3,像素电路的工作过程如下:

[0096] 初始化阶段t1,第一扫描线S1上的信号为低电平、第二扫描线S2和发光控制信号线EM上的信号均为高电平,第一多栅晶体管131包括的第一子晶体管T1和第二多栅晶体管151包括的第二子晶体管T2导通,第三多栅晶体管171包括的第三子晶体管T3、第四晶体管T4、第五晶体管T5和第六晶体管T6关断。初始化信号线VREF上的初始化电压经第一子晶体管T1写入发光模块12的第一端,同时还经第二子晶体管T2写入驱动晶体管T0的栅极,初始化阶段t1,实现对发光模块12和驱动晶体管T0的初始化。

[0097] 数据写入和阈值补偿阶段t2,第二扫描线S2上的信号为低电平,第一扫描线S1、发光控制信号线EM上的信号为高电平,第三多栅晶体管171包括的第三子晶体管T3、第六晶体管T6、驱动晶体管T0导通,第一多栅晶体管131包括的第一子晶体管T1、第二多栅晶体管151包括的第二子晶体管T2、第四晶体管T4和第五晶体管T5关断。数据线VDATA传输的数据电压经第六晶体管T6、驱动晶体管T0、第三多栅晶体管171包括的第三子晶体管T3写入驱动晶体管T0的栅极,实现驱动晶体管T0栅极的数据电压的写入以及驱动晶体管T0阈值电压的补偿。

[0098] 发光阶段t3,发光控制信号线EM上的信号为低电平,第一扫描线S1和第二扫描线S2上的信号为高电平,驱动晶体管T0、第四晶体管T4和第五晶体管T5导通,第一多栅晶体管

131包括的第一子晶体管T1、第二多栅晶体管151包括的第二子晶体管T2、第三多栅晶体管171包括的第三子晶体管T3和第六晶体管T6关断,第一电源线VDD上的第一电源电压通过第四晶体管T4传输至驱动晶体管T0的第一极,驱动晶体管T0根据其栅极的电压和第一极的电压驱动发光模块12发光。由于第二屏蔽电容C2的存在,可以稳定第二多栅晶体管151的第二中间节点N2的电位,进而降低第二多栅晶体管151的漏电,维持驱动晶体管T0的栅极电位的稳定,从而保证驱动电流的稳定,提高显示均一性。第三屏蔽电容C3,可以稳定第三多栅晶体管171的第三中间节点N3的电位,进而降低第三多栅晶体管171的漏电,维持驱动晶体管T0的栅极电位的稳定,保证驱动电流的稳定,提高显示均一性。同时,第一屏蔽电容C1,可以稳定第一多栅晶体管131的第一中间节点N1的电位,进而降低第一多栅晶体管131的漏电,维持发光模块12的第一端的电位的稳定,进一步提高显示均一性。

[0099] 本发明实施例还提供了一种显示面板,包括上述任一实施例中的像素电路,图7为本发明实施例提供的一种显示面板的结构示意图,参考图7和图1,显示面板还包括第一电源线VDD、数据线VDATA、初始化信号线VREF、第一扫描线S1和第二扫描线S2,第一电源线VDD、数据线VDATA沿第一方向Y延伸,初始化信号线VREF、第一扫描线S1和第二扫描线S2沿第二方向X延伸,第一方向Y和第二方向X相交。

[0100] 可选的,像素电路01阵列排布,第一方向Y为像素电路01排布的列方向,第二方向X为像素电路01排布的行方向,每行像素电路01中第一初始化模块13的控制端连接同一条第一扫描线S1,每行像素电路01的第一初始化模块13的第一端连接同一条初始化信号线VREF,每行像素电路01的数据写入模块10的控制端连接同一条第二扫描线S2,每列像素电路01的数据写入模块10的第一端连接同一条数据线VDATA,每列像素电路01连接同一条第一电源线VDD;与同一行像素电路01连接的第一扫描线S1位于初始化信号线VREF和第二扫描线S2之间。

[0101] 本实施例中示例性示出包括两个完整的像素电路01,值得注意的是,在初始化阶段,第n行像素电路01中的第一初始化模块13为同一列中,第n-1行像素电路01的发光模块12的第一端初始化。其中, $n \geq 2$ 。

[0102] 图8是一种显示面板的局部放大图,图8是对图7所示虚线区域001的局部放大,图9是本发明实施例提供的一种显示面板中有源层和第一金属层的结构示意图,图10是本发明实施例提供的一种显示面板中有源层、第一金属层和第二金属层的结构示意图,参考图7-图10,可选的,显示面板包括层叠设置的有源层100、第一金属层200和第二金属层300,其中,第一扫描线S1、第二扫描线S2位于第一金属层200,初始化信号线VREF位于第二金属层300;显示面板还包括第三金属层,显示面板中的第一电源线VDD、数据线VDATA位于第三金属层。

[0103] 继续参考图1、图7-图10,可选的,第一多栅晶体管131的至少一个第一中间节点N1与第一固定电位结构交叠形成至少一个第一屏蔽电容C1,第一多栅晶体管131的第一中间节点N1包括第一多栅晶体管131的有源层中连接相邻第一子晶体管T1的第一有源部;

[0104] 第一多栅晶体管131的有源层与第一扫描线S1交叠形成串联的至少两个第一子晶体管T1;

[0105] 可选的,第一有源部包括位于与同一像素电路01电连接的第一扫描线S1和第二扫描线S2之间的第一子有源部111;

[0106] 第一固定电位结构包括位于与同一像素电路01电连接的第一扫描线S1、第二扫描线S2之间的第一固定电位部311,第一固定电位部311与第一电源线VDD电连接;

[0107] 第一固定电位部311与第一子有源部111交叠形成一第一屏蔽电容C1。

[0108] 本实施例中示例性示出第一多栅晶体管131包括三个第一子晶体管T1,第一个第一子晶体管T1、第二个第一子晶体管T1和第三个第一子晶体管T1沿第二方向X从左至右排列,连接第二个第一子晶体管T1和第三个第一子晶体管T1的有源层作为第一子有源部111。本实施例中示例性示出第一固定电位部311与第一电源线VDD电连接,第一固定电位部311与第一子有源部111交叠形成一第一屏蔽电容C1,即第一子有源部111作为第一屏蔽电容C1的一个极板,第一固定电位部311作为第一屏蔽电容C1的另一个极板,使得在第一多栅晶体管131关断时,第一中间节点N1的电位可以保持稳定,进而降低第一多栅晶体管131的漏电,保证发光模块12的第一端的电位的稳定,提高显示均一性。可选的,第一固定电位结构位于第二金属层300,第一固定电位结构与初始化信号线VREF同层设置,进而使得无需在显示面板中额外设置金属层等形成第一固定电位结构,使得显示面板的膜层数量不会增加,有利于实现显示面板的轻薄化。

[0109] 继续参考图1、图7-图10,可选的,数据线VDATA和第一电源线VDD沿第二方向X排布,第一多栅晶体管131位于第一多栅晶体管131所属像素电路01所连接的第一电源线VDD远离数据线VDATA的一侧;

[0110] 第一固定电位结构还包括连接第一电源线VDD和第一固定电位部311的第一连接部312,第一连接部312沿第二方向X延伸,同一像素电路01中,第一子有源部111位于第一连接部312靠近像素电路01所连接的第一扫描线S1的一侧。

[0111] 第一连接部312沿第二方向延伸X,且第一连接部312同时连接第一固定电位部311和第一电源线VDD,使得第一固定电位部311的电位等于第一电源线VDD传输的第一电源电压。继续参考图1、图7-图10,可选的,第一多栅晶体管包括至少三个串联的第一子晶体管T1,第一有源部包括位于第一扫描线S1远离第二扫描线S2一侧的第二子有源部112;

[0112] 第二子有源部112与初始化信号线VREF交叠形成一第一屏蔽电容C1。

[0113] 本实施例中,连接第一个第一子晶体管T1和第二个第一子晶体管T1的有源层为第二子有源部112。第二子有源部112与初始化信号线VREF交叠形成一第一屏蔽电容C1,即第二子有源部112作为第一屏蔽电容C1的一个极板,初始化信号线VREF作为第一屏蔽电容C1的另一个极板,使得在第一多栅晶体管131关断时,第二子有源部112处的电位保持稳定,进而降低第一多栅晶体管131的漏电,维持发光模块12第一端的电位的稳定,有利于提高显示均一性。同时,初始化信号线VREF作为第一屏蔽电容C1的一个极板,进而使得无需在显示面板中额外设置金属层等形成电容结构,使得显示面板的膜层数量不会增加,显示面板的厚度不会增加,有利于实现显示面板的轻薄化。

[0114] 继续参考图1、图7-图10,可选的,像素电路01包括第二连接部313,第二连接部313沿第一方向Y延伸,第二连接部313的一端连接初始化信号线VREF,另一端连接第一多栅晶体管131的第一极T1-1,第一多栅晶体管131的第二极T1-2连接发光模块12的第一端。

[0115] 可选的,第二连接部313位于第三金属层,第二连接部313与数据线VDATA和第一电源线VDD位于同一层。位于第二金属层300的初始化信号线VREF经过过孔002与第三金属层连接,第三金属层又经过过孔002与第一多栅晶体管的第一极T1-1连接,进而实现初始化信

号线VREF与第一多栅晶体管131的第一极T1-1连接,在初始化阶段,初始化信号线VREF提供的初始化电压经第一多栅晶体管131写入发光模块12的第一端,实现对发光模块12的初始化。且第二金属层300和第三金属层之间本身存在过孔以进行连接,第三金属层和有源层100之间也存在过孔以进行连接,进而实现有源层100与初始化信号线VREF连接时,无需额外单独掩膜步骤进行打孔,简化工艺,使得显示面板更易于制作。

[0116] 参考图4和图7-图10,可选的,像素电路还包括补偿模块17和第三屏蔽模块18,补偿模块17包括第三多栅晶体管171,第三多栅晶体管171包括至少两个串联的第三子晶体管T3,第三多栅晶体管171的至少一个第三中间节点N3与第三固定电位结构交叠形成至少一个第三屏蔽电容C3,第三多栅晶体管171的第三中间节点N3包括第三多栅晶体管171的有源层中连接相邻第三子晶体管T3的第三有源部;

[0117] 参考图4和图7-图10,可选的,第三有源部包括与同一像素电路01连接的第一扫描线S1和第二扫描线S2之间的至少一个第三子有源部113,第三固定电位结构包括至少一个第三固定电位部331,第三固定电位部331与第一连接部312连接,同一像素电路01中,第三子有源部113和第三固定电位部331位于第一连接部312靠近像素电路01连接的第二扫描线S2的一侧,第三子有源部113与对应的第三固定电位部331交叠形成第三屏蔽电容C3。

[0118] 本实施例中,示例性示出第三多栅晶体管171包括两个第三子晶体管T3,两个第三子晶体管T3连接的有源层作为第三子有源部113。第三固定电位部331位于第二金属层300,进而使得无需在显示面板中额外设置金属层等形成第一固定电位结构,使得显示面板的膜层数量不会增加,有利于实现显示面板的轻薄化。第三固定电位部331经第一连接部312与第一电源线VDD连接,使得第三固定电位部331的电位等于第一电源电压。第三子有源部113与对应的第三固定电位部331交叠形成第三屏蔽电容C3,即第三子有源部113作为第三屏蔽电容C3的一个极板,第三固定电位部331作为第三屏蔽电容C3的另一个极板。第三屏蔽电容C3使得第三多栅晶体管171管关断时,第三多栅晶体管171的第三中间节点N3保持稳定,降低第三多栅晶体管171的漏电,维持驱动模块11的控制端的稳定,进而保证驱动电流的稳定,提高显示均一性。

[0119] 现有技术中,位于第j列的像素电路01的第三固定电位部331连接同行的第j+1列像素电路01所连接的第一电源线VDD,进而构成第三屏蔽电容C3的一个极板以稳定第三多栅晶体管171的第三中间节点N3的电位,但是第三固定电位部331连接相邻列像素电路01所连接的第一电源线VDD时,需跨接数据线VDATA,由此可能形成寄生电容,进而影响第三多栅晶体管171的第三中间节点N3的电位。其中, $j \geq 1$ 。而本实施例中,第三固定电位部331与第一连接部312连接,第一连接部312与本像素电路所连接的第一电源线VDD连接,无需跨接数据线VDATA,避免数据线VDATA与第一连接部312形成寄生电容对第三多栅晶体管的第三中间节点N3的影响,且形成第三屏蔽电容C3的布局更为简单,更易实现。

[0120] 参考图5、图7和图8,像素电路还包括第二初始化模块15、发光控制模块20,第二初始化模块包括第二多栅晶体管151,第二多栅晶体管151包括至少两个串联的第二子晶体管T2,发光控制模块20包括第四晶体管T4和第五晶体管T5,数据写入模块10包括第六晶体管T6。

[0121] 图11是本发明实施例提供的另一种显示面板的结构示意图,图12是本发明实施例提供的另一种显示面板的局部放大图,图12是对图11所示虚线区域003的局部放大图,图13

是本发明实施例提供的另一种显示面板中有源层、第一金属层的结构示意图,图14是本发明实施例提供的另一种显示面板中有源层、第一金属层和第二金属层的结构示意图,参考图3、图11-图14,可选的,像素电路还包括第二初始化模块15和第二屏蔽模块;第二初始化模块15包括第二多栅晶体管151,第二多栅晶体管151包括至少两个串联的第二子晶体管T2,第二多栅晶体管151的至少一个第二中间节点N2与第二固定电位结构交叠形成至少一个第二屏蔽电容C2,第二多栅晶体管151的第二中间节点N2包括第二多栅晶体管151的有源层中连接相邻第二子晶体管T2的第二有源部;

[0122] 参考图3、图11-图14,可选的,第二有源部包括位于与同一像素电路01连接的第一扫描线S1远离第二扫描线S2一侧的至少一个第四子有源部114;

[0123] 第四子有源部114与初始化信号线VREF交叠形成一第二屏蔽电容C2。

[0124] 第四子有源部114作为第二屏蔽电容C2的一个极板,初始化信号线VREF作为屏蔽电容的另一个极板。初始化信号线VREF作为第二屏蔽电容的另一个极板进而使得无需在显示面板中额外设置金属层等形成电容结构,使得显示面板的膜层数量不会增加,有利于实现显示面板的轻薄化。第二屏蔽电容C2可以使得第二多栅晶体管151关断时,第二多栅晶体管151的第二中间节点N2的电位维持稳定,进而降低第二多栅晶体管151的漏电,维持驱动模块11的控制端的电位的稳定,进而维持驱动电流的稳定,提高显示均匀性。

[0125] 继续参考图3、图11-图14,可选的,像素电路01包括第三连接部314和第四连接部315,第三连接部314和第四连接部315均沿第一方向延伸Y,第三连接部314的一端连接初始化信号线VREF,另一端连接第二多栅晶体管151的第一极T2-1,第四连接部315的一端连接第二多栅晶体管的第二极T2-2,另一端连接驱动模块10的控制端。

[0126] 第三连接部314和第四连接部315均位于第三金属层,第三连接部314通过过孔002与初始化信号线VREF连接,同时第三连接部314又与第二多栅晶体管151的第一极T2-1连接,进而实现第二多栅晶体管151的第一极T2-1与初始化信号线VREF连接。第四连接部315一端连接第二多栅晶体管151的第二极T2-2,另一端连接驱动模块11的控制端,进而实现第二多栅晶体管151的第二极T2-2与驱动模块11的控制端的连接,从而使得在初始化阶段,第二多栅晶体管151将初始化电压写入驱动模块11的控制端,实现对驱动模块11的初始化。第二金属层300和第三金属层之间本身存在过孔以进行连接,第三金属层和有源层100之间也存在过孔以进行连接,进而实现有源层100与初始化信号线VREF连接时,无需额外单独掩膜步骤进行打孔,简化工艺,使得显示面板更易于制作。

[0127] 可选的,第三连接部314与第二连接部313为同一结构。

[0128] 第三连接部314与第二连接部313为同一结构,可以避免设置额外的第三连接部314,进而简化显示面板的布局,节省显示面板的面积。

[0129] 参考图5和图11-图14,像素电路还包括第二初始化模块15、发光控制模块20,第二初始化模块15包括第二多栅晶体管151,第二多栅晶体管151包括至少两个串联的第二子晶体管T2,发光控制模块包括第四晶体管T4和第五晶体管T5,数据写入模块包括第六晶体管T6。

[0130] 可选的,第一多栅晶体管包括奇数个第一子晶体管,第二多栅晶体管包括偶数个第二子晶体管(例如如图7所示显示面板结构)。

[0131] 图15为本发明实施例提供的另一种显示面板的结构示意图,图16为本发明实施例

提供的另一种显示面板的有源层和第一金属层的结构示意图,图17为本发明实施例提供的另一种显示面板的局部放大图,图17为图16所示虚线004区域的局部放大图。参考图15-图17,可选的,第一多栅晶体管131包括偶数个第一子晶体管T1,第二多栅晶体管151包括奇数个第二子晶体管T2。

[0132] 参考图15-图17,像素电路还包括第二初始化模块、发光控制模块,第二初始化模块包括第二多栅晶体管151,第二多栅晶体管151包括至少两个串联的第二子晶体管T2,发光控制模块包括第四晶体管T4和第五晶体管T5,数据写入模块包括第六晶体管T6,驱动模块包括驱动晶体管T0。

[0133] 继续参考图5、图11-图17,第二多栅晶体管151包括至少三个串联的第二子晶体管T2,第二有源部包括位于与同一像素电路01电连接的第一扫描线S1和第二扫描线S2之间的第五子有源部115;

[0134] 第二固定电位结构包括位于与同一像素电路01电连接的第一扫描线S1、第二扫描线S2之间的第二固定电位部321,第二固定电位部321与第一电源线VDD电连接;

[0135] 第二固定电位部321与第五子有源部115交叠形成一第二屏蔽电容C2。

[0136] 本实施例中示例性示出包括四个第二子晶体管T2,沿第二方向X,从左至右依次为第一个第二子晶体管T2、第二个第二子晶体管T2、第三个第二子晶体管T2、第四个第二子晶体管T2,第二个第二子晶体管T2、第三个第二子晶体管T2连接的有源层为第五子有源部115。第二固定电位部321位于第二金属层,与第一电源线VDD电连接,使得第二固定电位部321构成第二屏蔽电容C2的一个极板,第五子有源部115构成第二屏蔽电容C2的另一个极板。在第二多栅晶体管151关断时,第二屏蔽电容C2可以稳定第二多栅晶体管151的第二中间节点N2的电位,进而降低第二多栅晶体管151的漏电,维持驱动模块11控制端电位的稳定,进而显示均一性。

[0137] 图18为本发明实施例提供的另一种显示面板的结构示意图,参考图18,可选的,本实施例中显示面板的像素电路01包括驱动晶体管T0、第一子晶体管T1、第二子晶体管T2、第三晶体管T3、第四晶体管T4、第五晶体管T5、第六晶体管T6。像素电路01包括第二连接部313,第二连接部313沿第一方向Y延伸,第二连接部313的一端连接初始化信号线VREF,另一端连接第一多栅晶体管的第一极T1-1。像素电路还可以包括第五连接部316,第五连接部316沿第二方向X延伸,第五连接部316的一端连接第二连接部313,第五连接部316的另一端与第一子有源部交叠形成一第一屏蔽电容C1。

[0138] 第五连接部316与第二连接部313连接,而第二连接部313又与初始化信号线VREF连接,因此,第五连接部316上的电位等于初始化电压。即第五连接部316与第一子有源部交叠形成的第一屏蔽电容C1上的电位可以为初始化电压。第二连接部313和第五连接部316与第一电源线VDD同层设置,进而使得在形成第一屏蔽电容C1时,无需在显示面板中额外设置金属层,使得显示面板的膜层数量不会增加,有利于实现显示面板的轻薄化。

[0139] 注意,上述仅为本发明的较佳实施例及所运用技术原理。本领域技术人员会理解,本发明不限于这里所述的特定实施例,对本领域技术人员来说能够进行各种明显的变化、重新调整和替代而不会脱离本发明的保护范围。因此,虽然通过以上实施例对本发明进行了较为详细的说明,但是本发明不仅仅限于以上实施例,在不脱离本发明构思的情况下,还可以包括更多其他等效实施例,而本发明的范围由所附的权利要求范围决定。

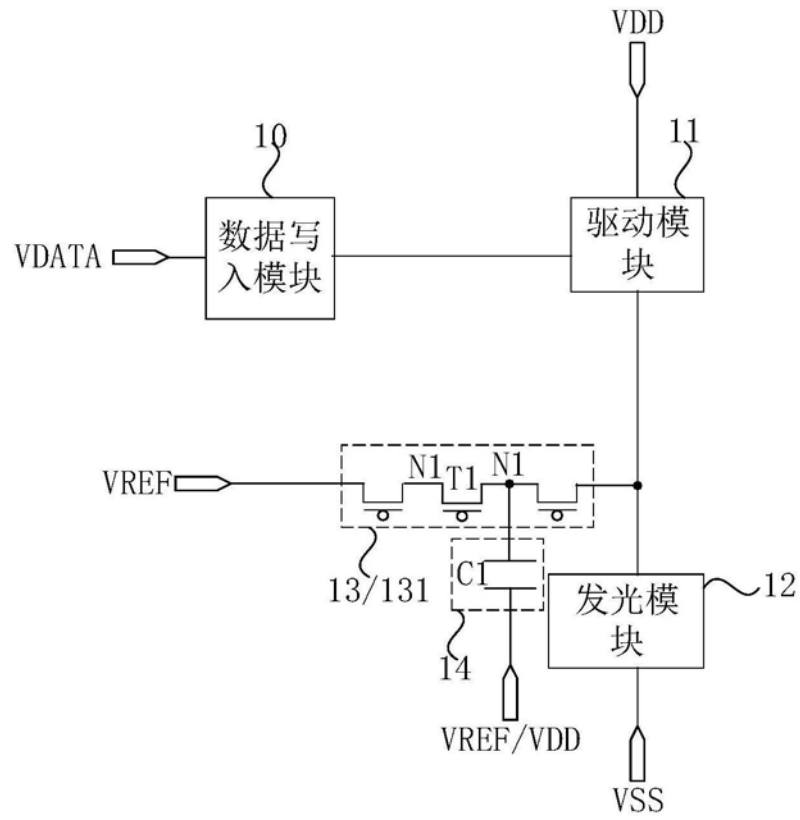


图1

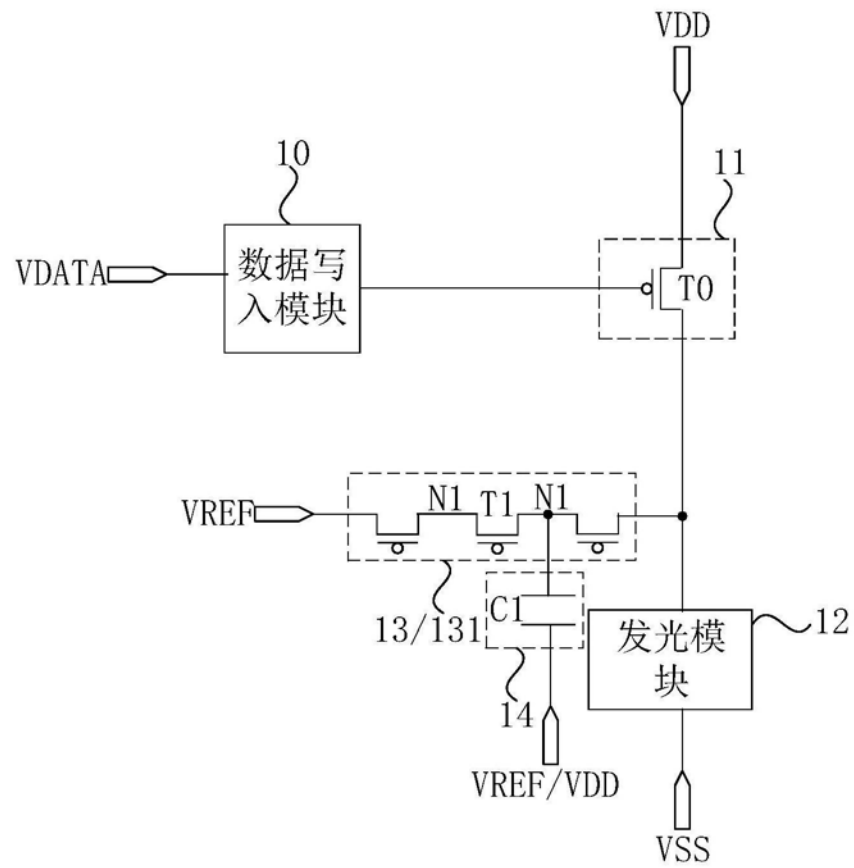


图2

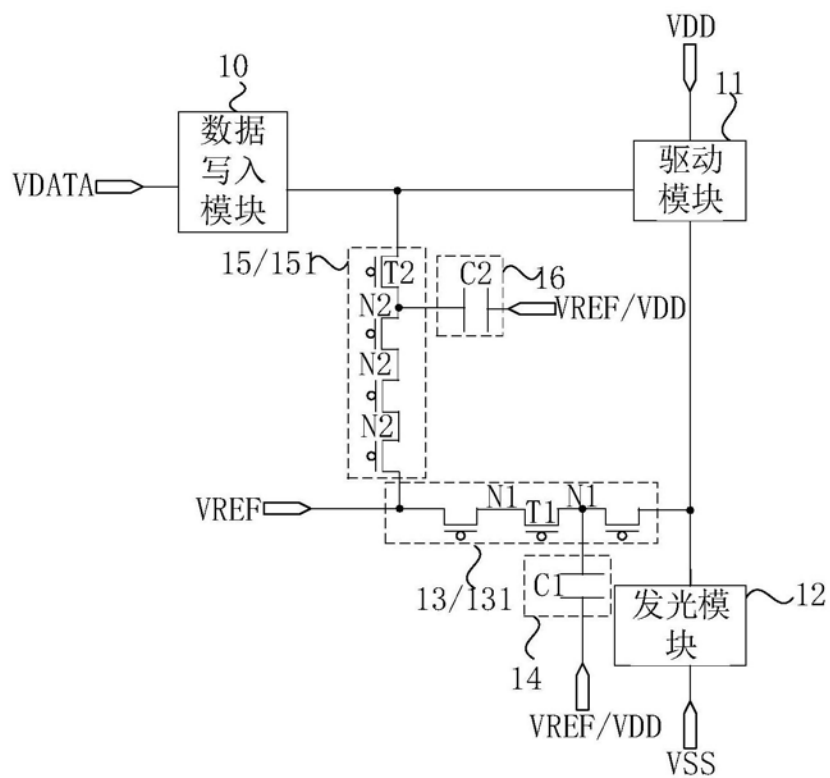


图3

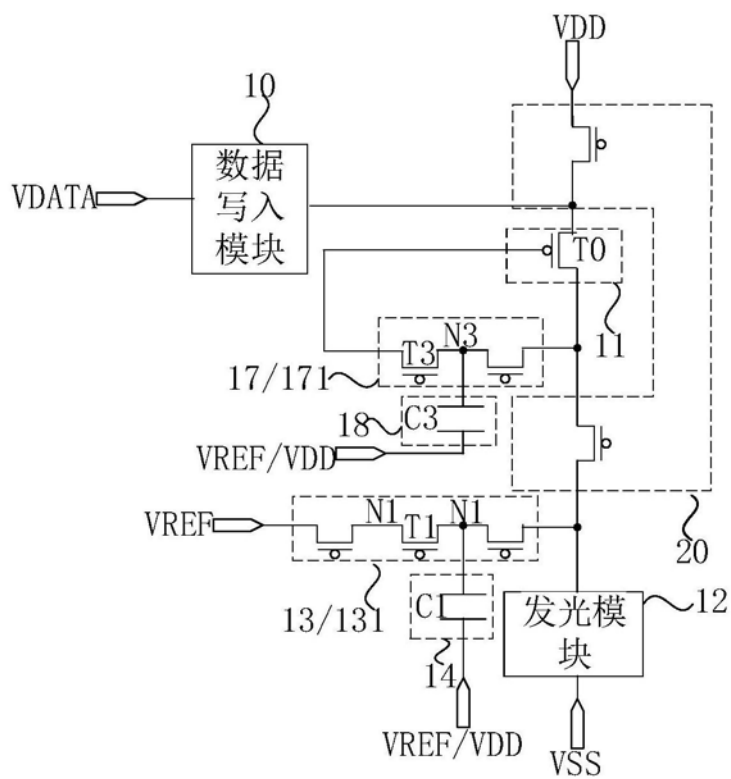


图4

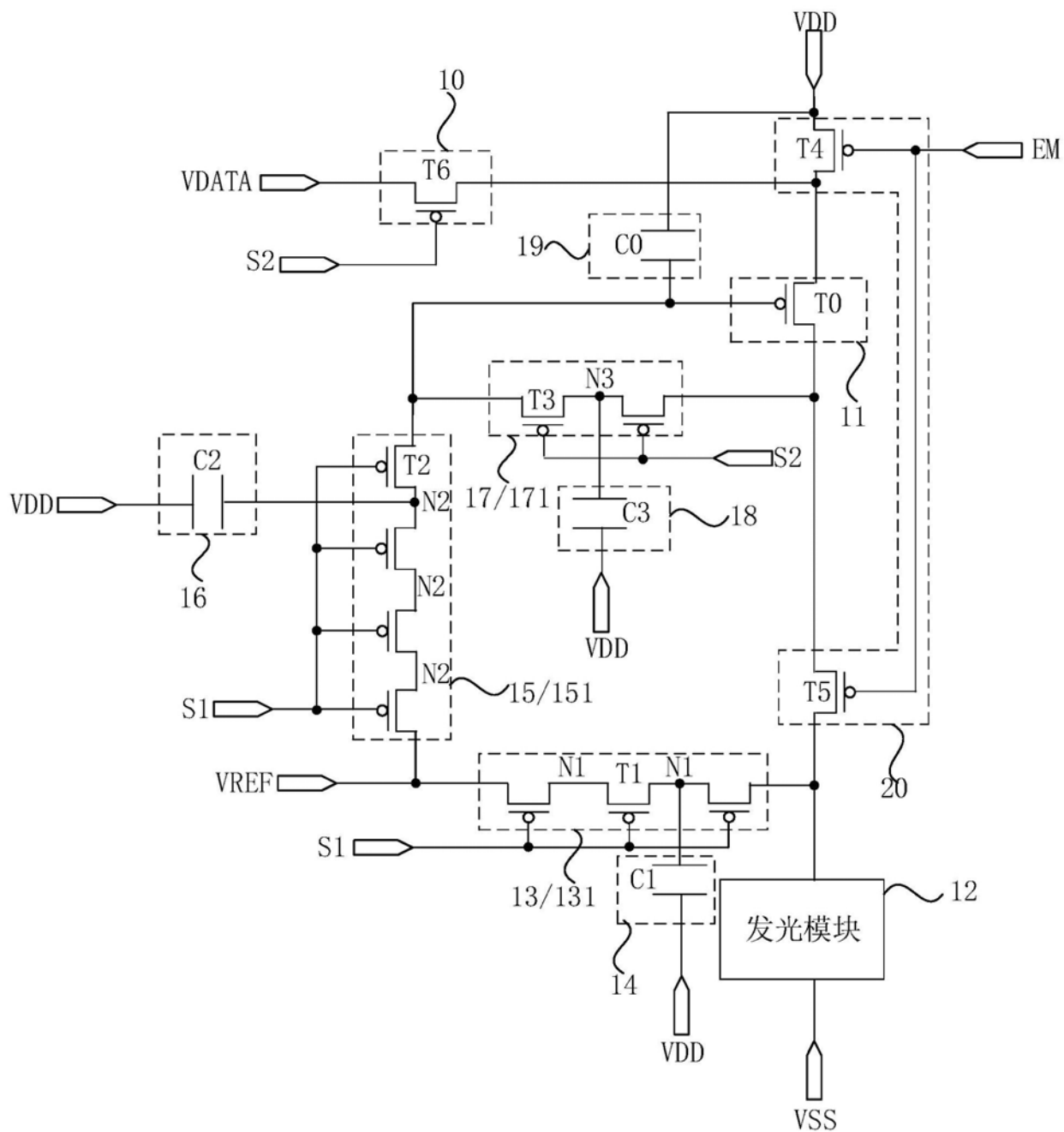


图5

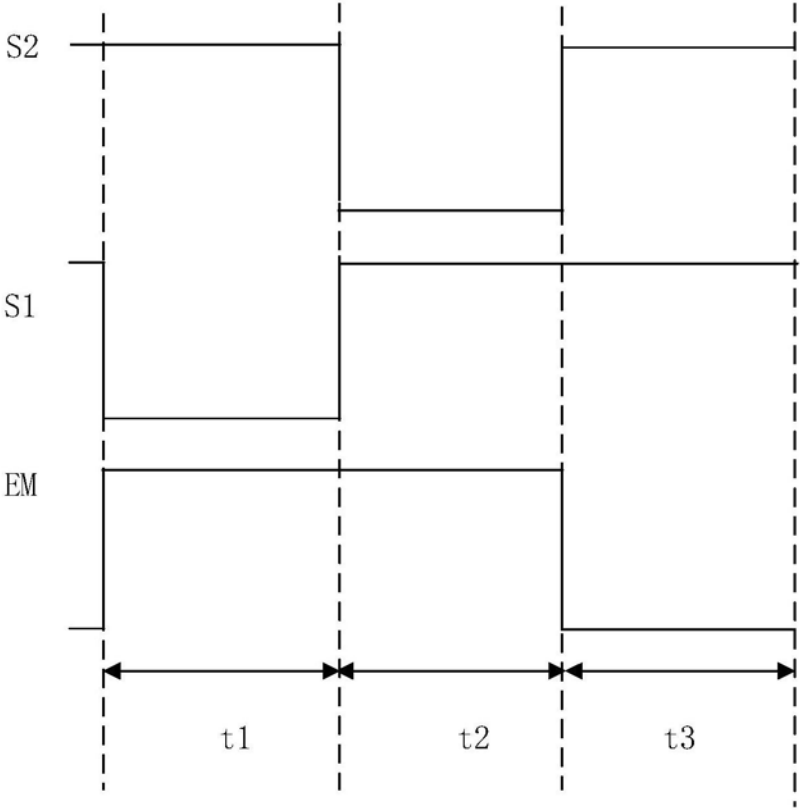


图6

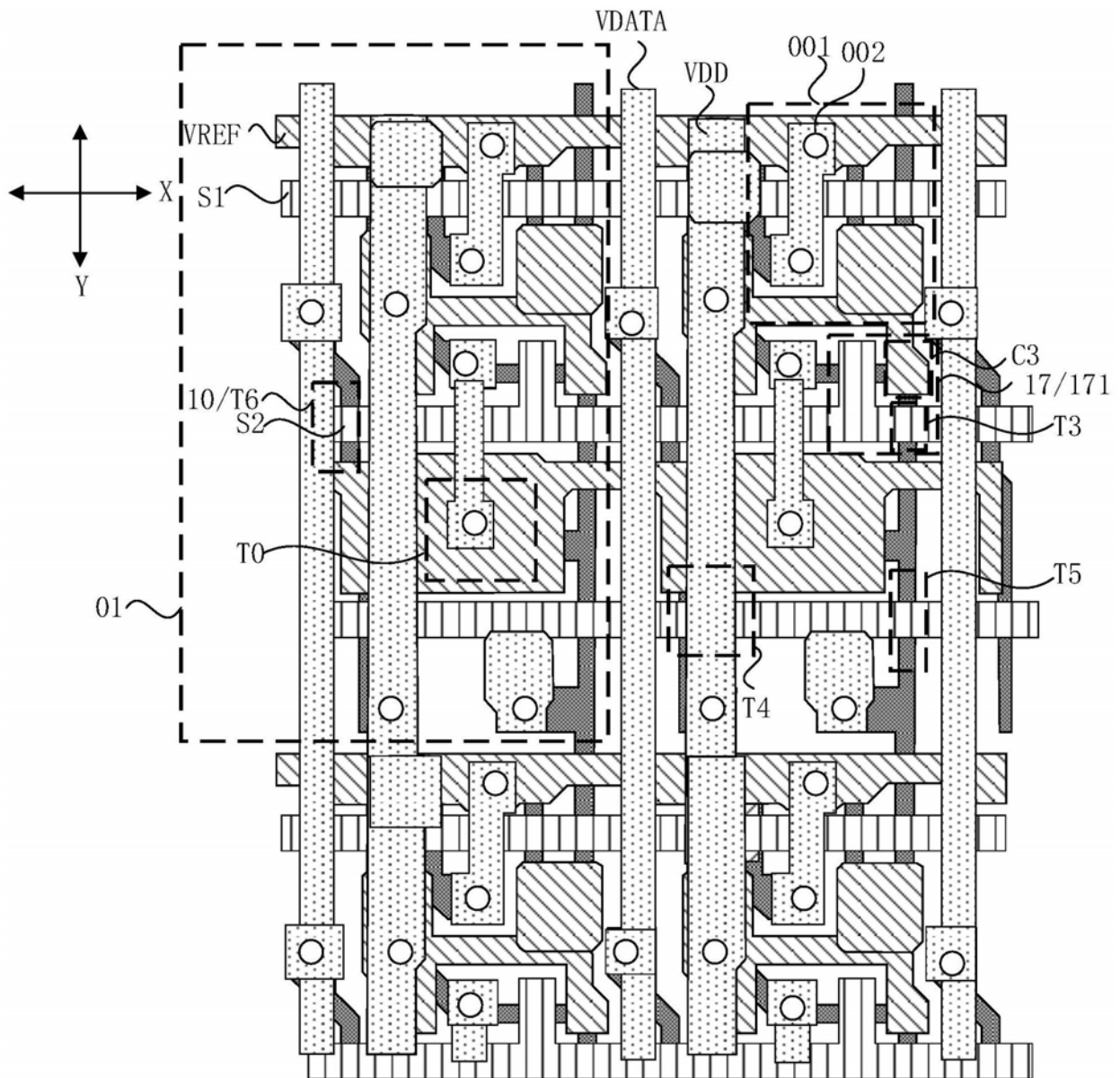


图7

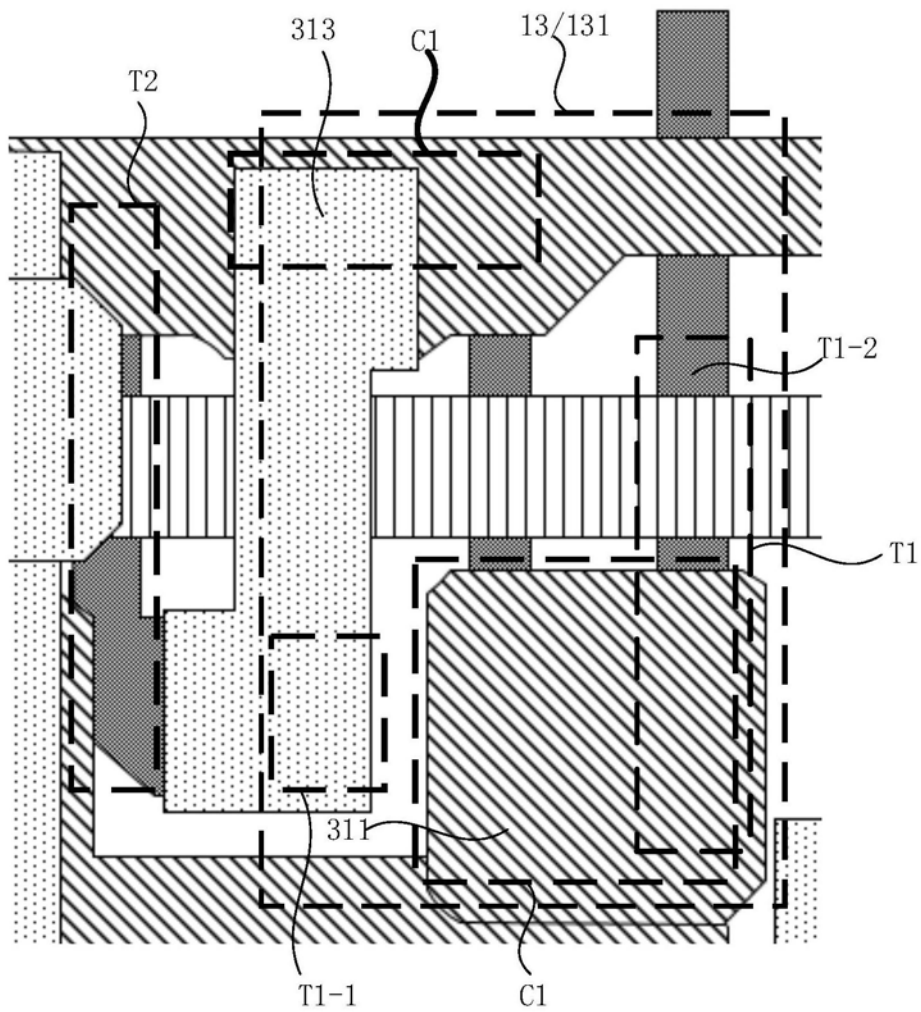


图8

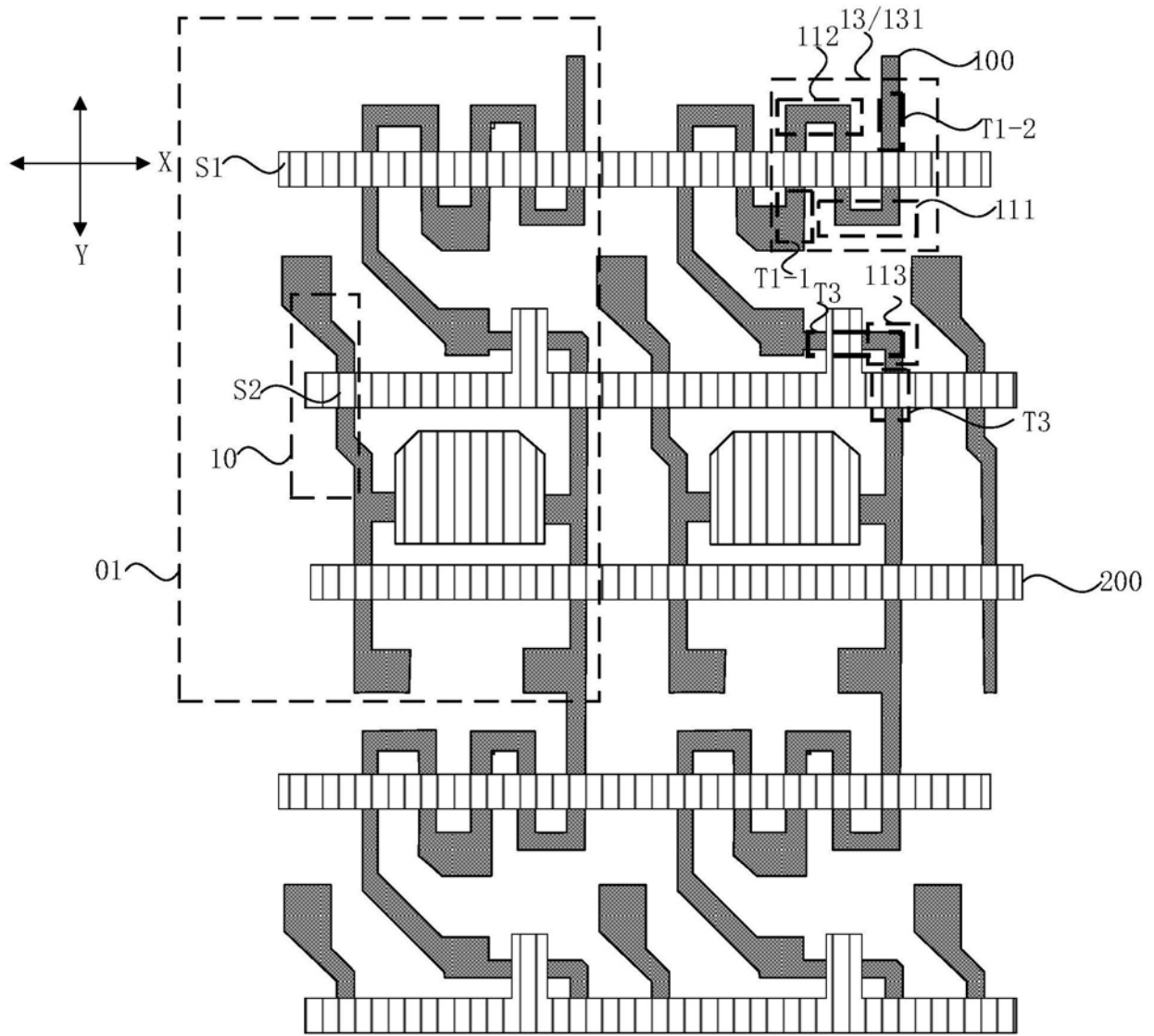


图9

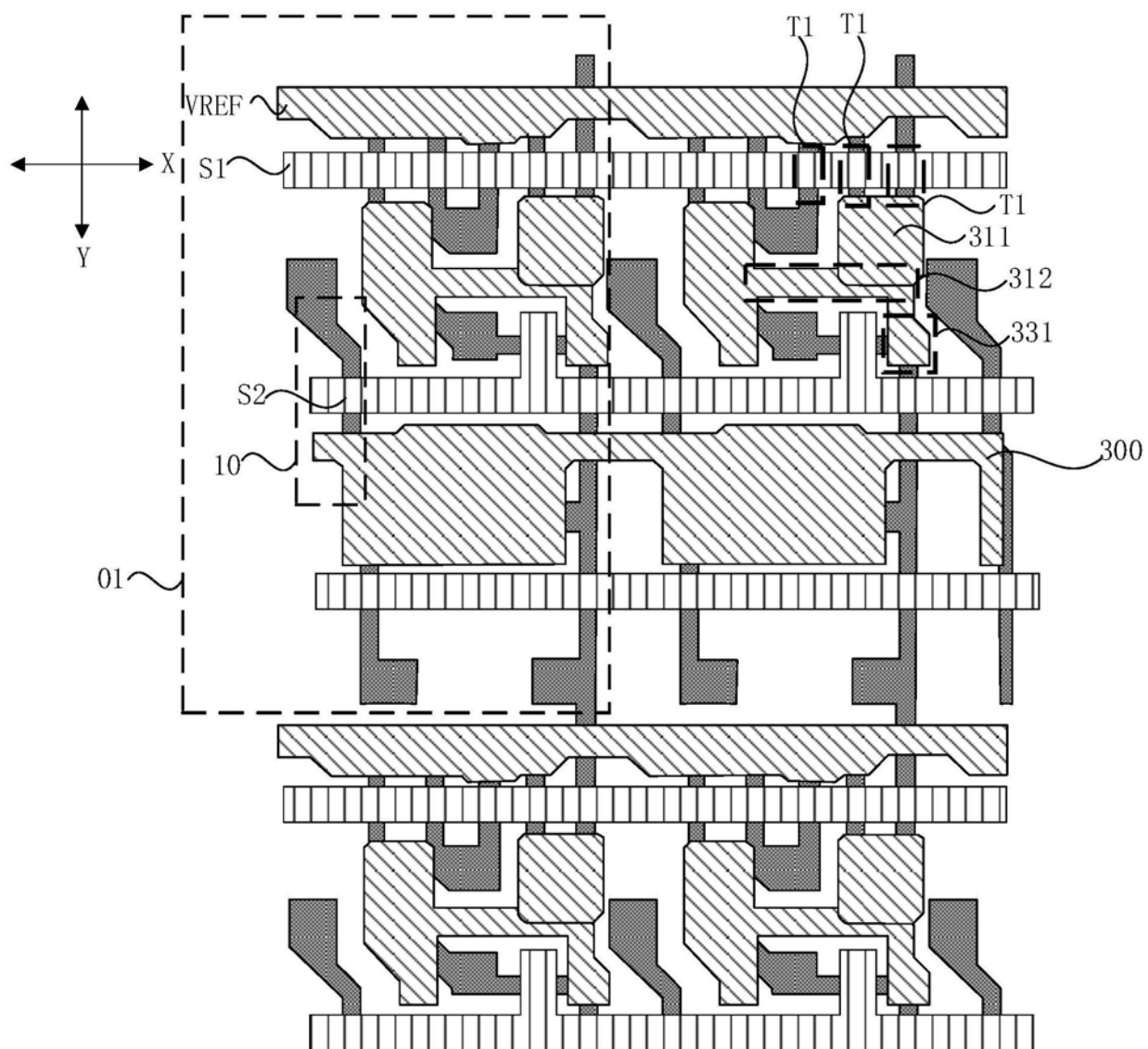


图10

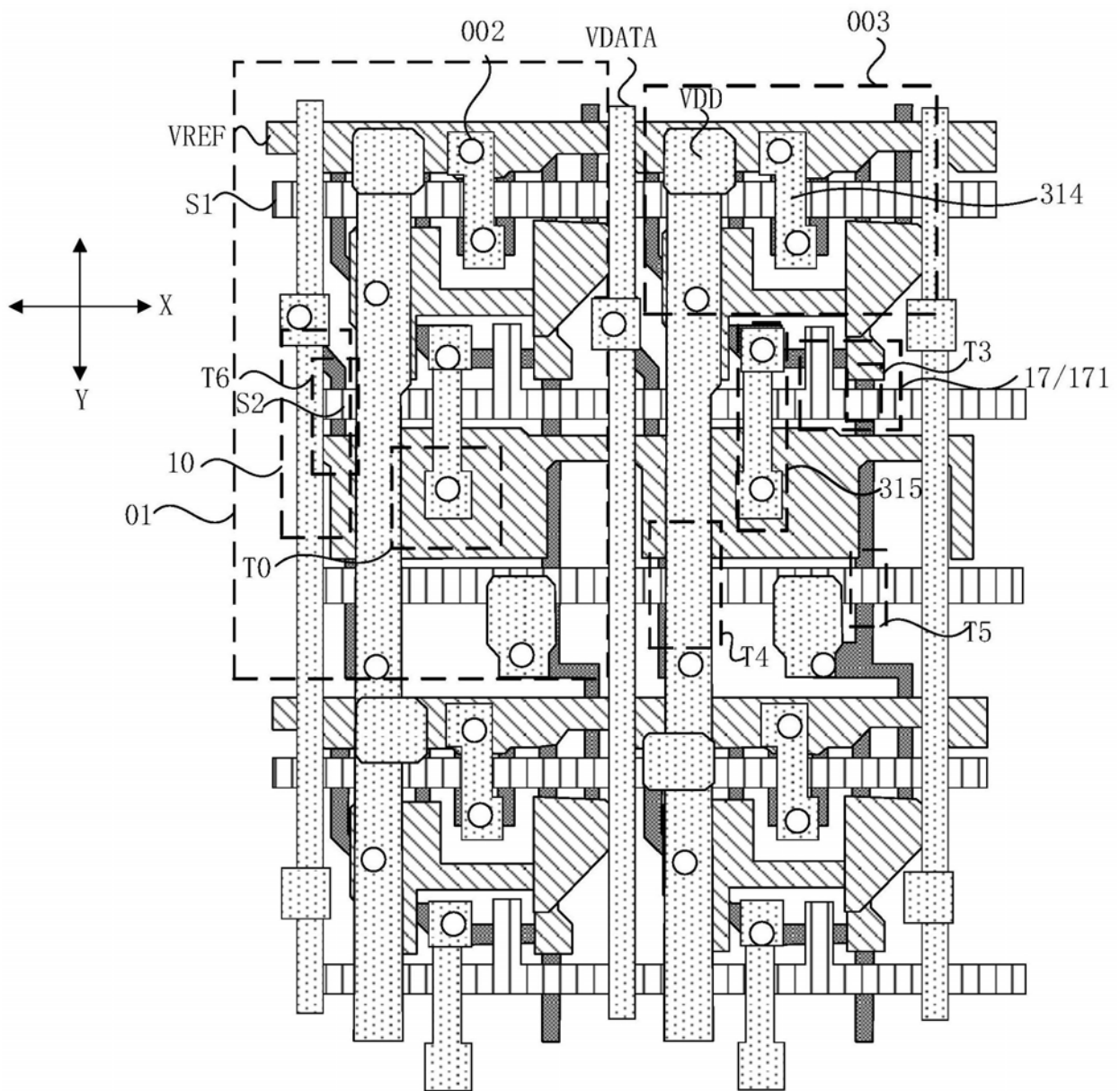


图11

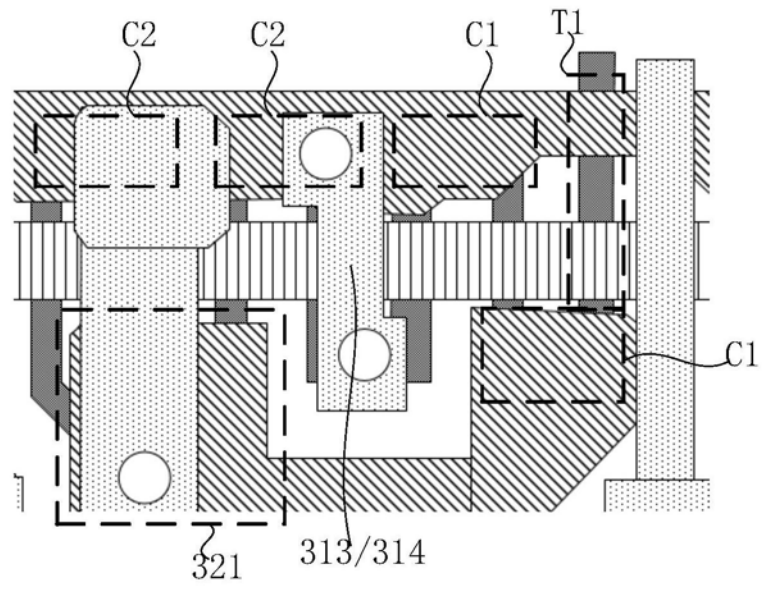


图12

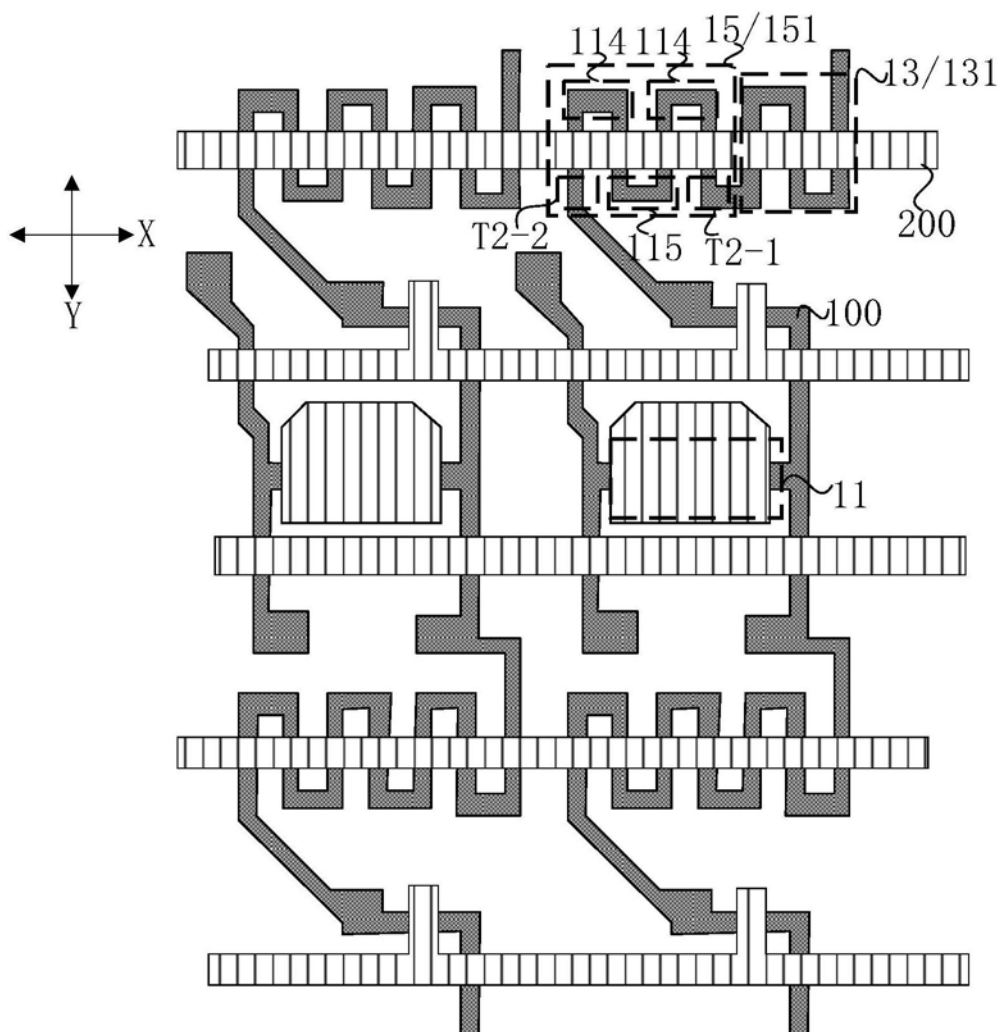


图13

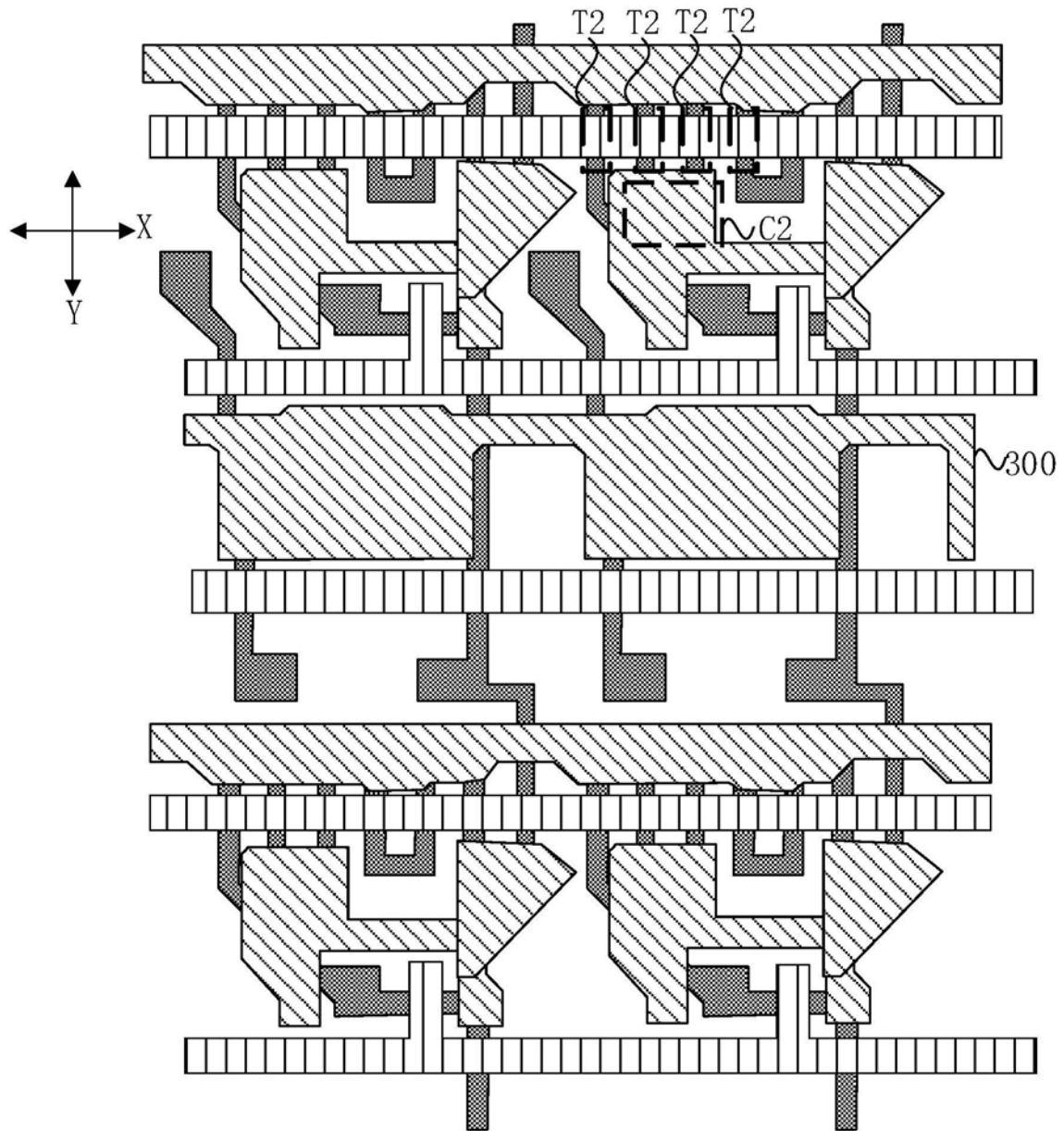


图14

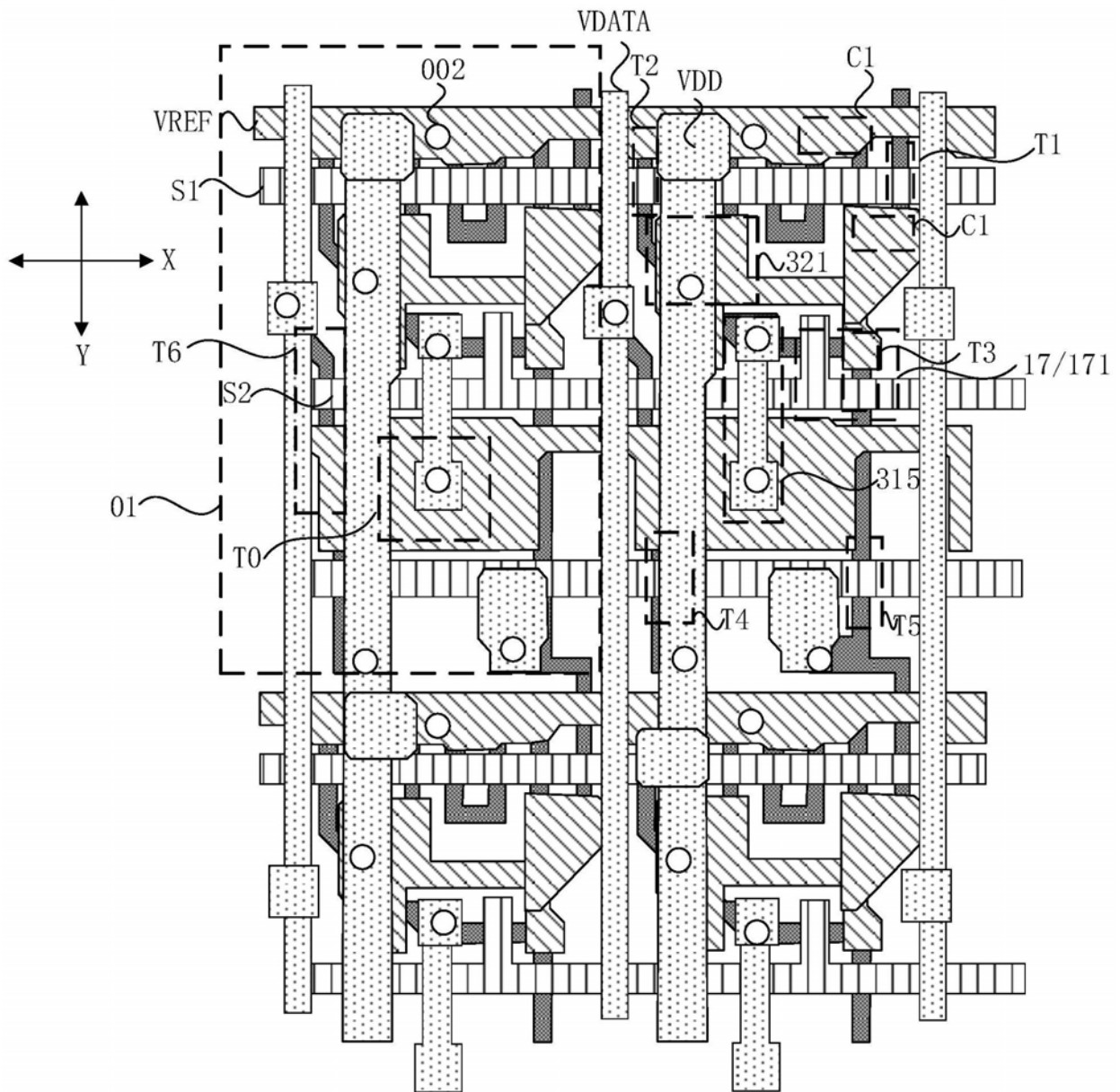


图15

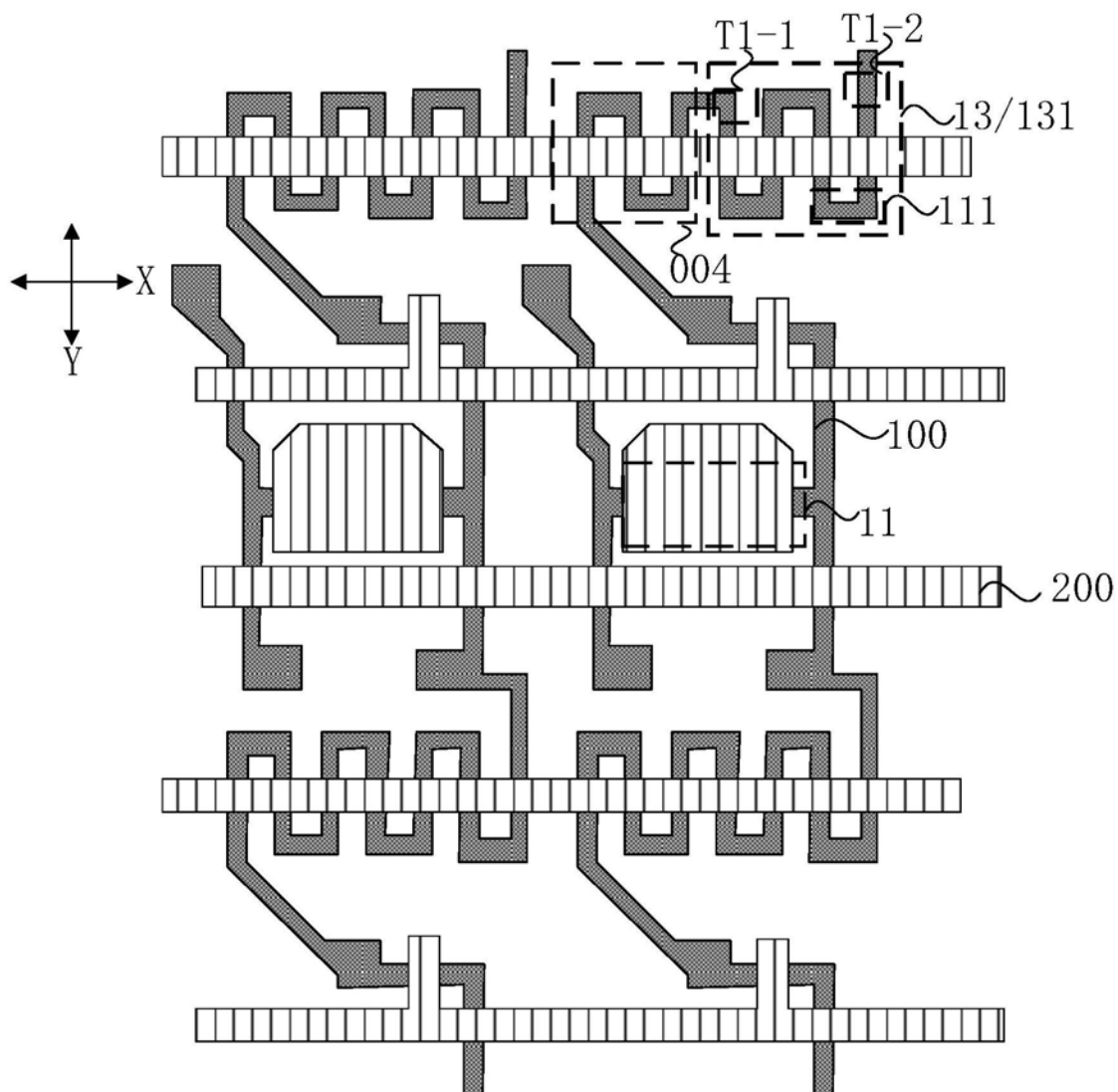


图16

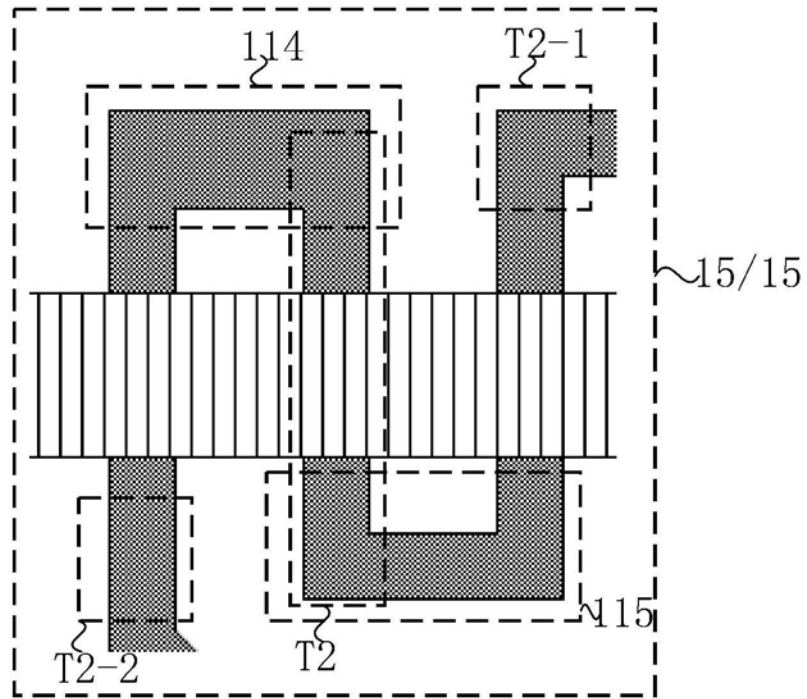


图17

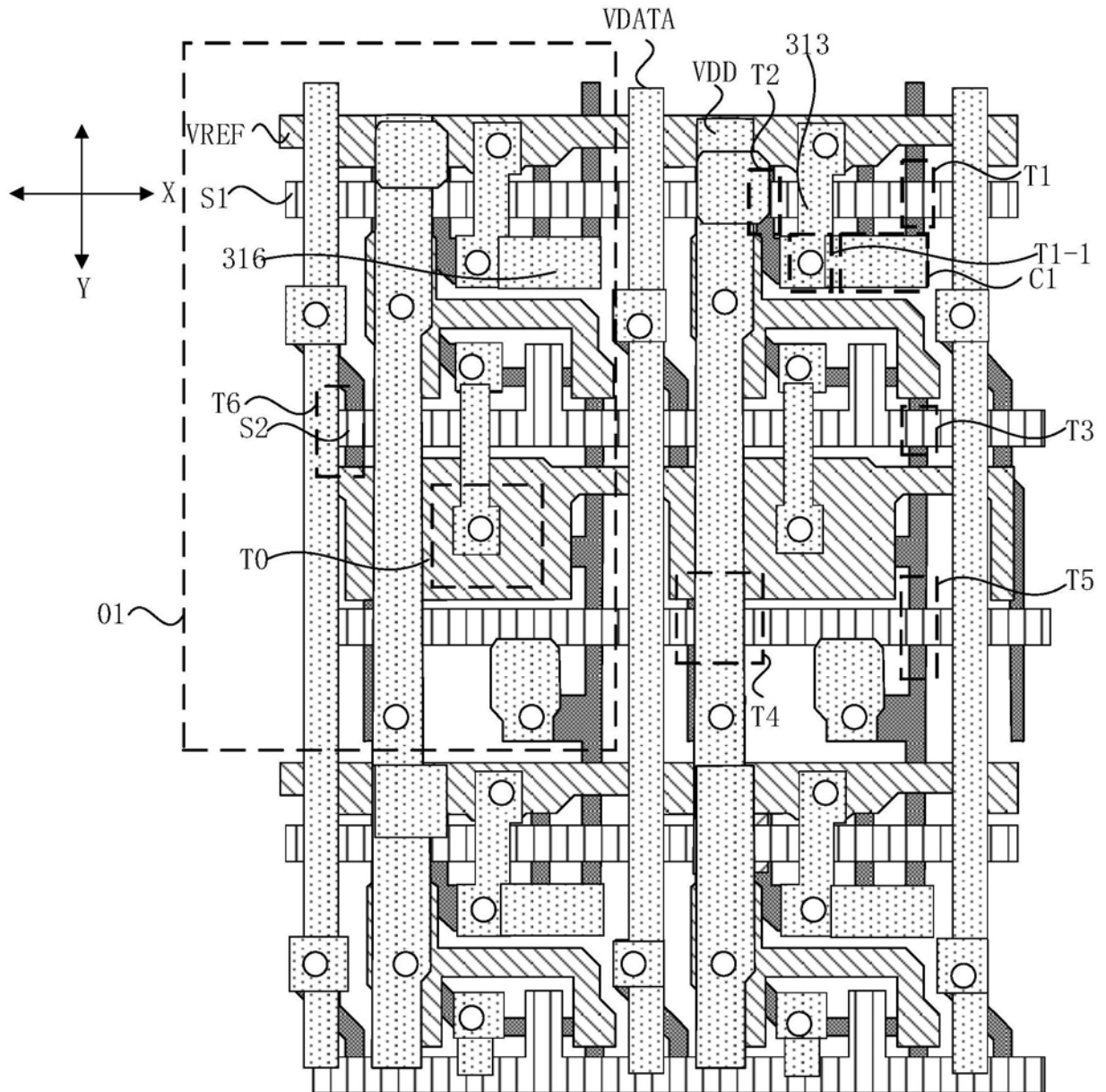


图18