

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,

Petitioner

v.

SAMSUNG DISPLAY CO., LTD.,

Patent Owner.

IPR2025-01480

U.S. Patent No. 10,439,015

**DECLARATION OF RONALD S. COK IN SUPPORT OF PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT NO. 10,439,015**

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EXHIBIT LIST

No.	Exhibit
1001	U.S. Patent No. 10,439,015 (“’015 Patent” or “’015 Pat.”)
1002	File History of the ’015 Patent (“’015FH”)
1003	Declaration of Ronald S. Cok (“Cok”)
1004	U.S. Patent Publication No. 2014/0132584 A1 (“Kim-584”)
1005	U.S. Patent Publication No. 2012/0019504 A1 (“Han”)
1006	U.S. Patent Publication No. 2014/0034923 A1 (“Kim-923”)
1007	U.S. Patent Publication No. 2014/0042405 A1 (“Moon”)
1008	U.S. Patent Publication No. 2014/0098078 A1 (“Jeon-078”)
1009	RESERVED
1010	Japanese Pat. No. 3,858,572 (“Masao”)
1011	U.S. Patent No. 6,225,966 B1 (“Ohtani”)
1012	N. H. E. Weste et al., <i>CMOS VLSI Design: A Circuits and Systems Perspective</i> , Fourth Edition, Addison-Wesley, 2011 (“Weste”)
1013	U.S. Patent No. 5,136,358 (“Sakai”)
1014	U.S. Patent No. 5,285,017 (“Gardner”)
1015	U.S. Patent No. 6,510,545 (“Yee”)
1016	U.S. Patent No. 8,692,297 (“Ho”)
1017	U.S. Patent No. 6,622,294 (“Saxena”)
1018	U.S. Patent No. 8,670,099 (“Xie”)
1019	U.S. Patent No. 8,988,852 (“Signoff”)

No.	Exhibit
1020	Chinese Patent Publication No. 113936600 (“Tian”)
1021	U.S. Patent Publication No. 2014/0320544 (“Kim-544”)
1022	U.S. Patent Publication No. 2014/0070184 (“Shin”)
1023	U.S. Patent Publication No. 2007/0007535 (“Tang”)
1024	RESERVED
1025	Korean Patent Publication No. 20050052033 (“Kim-033”)
1026	U.S. Patent Publication No. 2011/0025585 (“Kim-585”)
1027	Korean Patent Publication No. 870000854 (“Hong”)
1028	U.S. Patent No. 8,487,311 (“Liu”)
1029	U.S. Patent No. 8,514,155 (“Kobayashi”)
1030	U.S. Patent No. 8,269,696 (“Tomida”)
1031	U.S. Patent No. 7,855,507 (“Kim-507”)
1032	U.S. Patent No. 8,653,521 (“Hwang”)
1033	U.S. Patent No. 8,701,068 (“McElvain”)

LISTING OF CHALLENGED CLAIMS

10,439,015
Claim 1
1[pre] A display apparatus comprising:
1[a] a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;
1[b] a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;
1[c] a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;
1[d] a first signal line over the second electrode layer; and
1[e] a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.
Claim 2
2. The display apparatus of claim 1, wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line.
Claim 3
3. The display apparatus of claim 1, further comprising a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first signal line.
Claim 4

4. The display apparatus of claim 1, further comprising a first voltage line in the same layer as the first signal line and connected to the second electrode layer.

Claim 5

5[pre] The display apparatus of claim 1, further comprising:

5[a] a third thin-film transistor comprising a third semiconductor, one end of the third semiconductor being connected to one end of the first semiconductor, and the other end of the third semiconductor being connected to the first electrode layer; and

5[b] a second shield layer in a layer between the first signal line and the third semiconductor and overlapping a part between a first channel area and a second channel area of the third semiconductor.

Claim 6

6[pre] The display apparatus of claim 1, further comprising:

6[a] a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and

6[b] a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part of the fourth semiconductor.

Claim 7

7[pre] The display apparatus of claim 1, further comprising:

7[a] a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and

7[b] a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part between a first channel area and a second channel area of the fourth semiconductor.

Claim 8

8[pre] The display apparatus of claim 1, wherein the first signal line extends in a first direction, and

8[a] wherein a length along the first direction of the overlapping part of the first shield layer with the part of one of the source area and the drain area of the first semiconductor is larger than a length of the first electrode layer along the first direction.

Claim 9

9. The display apparatus of claim 1, wherein the first shield layer fully overlaps the part of one of the source area and the drain area of the first semiconductor.

Claim 10

10[a] The display apparatus of claim 1, wherein the first signal line extends in a first direction, and

10[b] wherein a length along the first direction of ~~[[the]]~~ an overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction.

Claim 11

11[a] The display apparatus of claim 5, wherein a gate electrode of the third thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the third semiconductor, and the second gate electrode overlapping the second channel area of the third semiconductor, and

11[b] wherein the gate electrode of the third thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

Claim 12
12. The display apparatus of claim 5, further comprising a first voltage line in the same layer as the first signal line, wherein the second shield layer is connected to the first voltage line.
Claim 13
13. The display apparatus of claim 5, wherein the second shield layer is a part of the second electrode layer.
Claim 14
14. The display apparatus of claim 5, further comprising a connecting line connecting the other end of the third semiconductor and the first electrode layer and being in the same layer as the first signal line.
Claim 15
15[a] The display apparatus of claim 6, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer and overlapping the fourth semiconductor, and
15[b] wherein the third shield layer is a part of the second voltage line and overlaps a part of the fourth semiconductor between the first gate electrode and the second gate electrode.
Claim 16
16. The display apparatus of claim 15, wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.
Claim 17
17. The display apparatus of claim 7, wherein the third shield layer is a part of the second voltage line.

Claim 18
18[a] The display apparatus of claim 7, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the fourth semiconductor, and the second gate electrode overlapping the second channel area of the fourth semiconductor, and
18[b] wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.
Claim 19
19. The display apparatus of claim 7, further comprising a connecting line connecting the one end of the fourth semiconductor and the first electrode layer and being in the same layer as the first signal line.
Claim 20
20[a] The display apparatus of claim 3, further comprising a fifth thin-film transistor comprising a fifth semiconductor, one end of the fifth semiconductor being connected to the one end of the first semiconductor and the one end of the second semiconductor, and the other end of the fifth semiconductor being connected to a first voltage line,
20[b] wherein the first voltage line in the same layer as the first signal line and connected to the second electrode layer.
Claim 21
21[a] The display apparatus of claim 20, further comprising a fourth shield layer in a layer between the first signal line and the fifth semiconductor,
21[b] wherein the fourth shield layer overlaps a part of semiconductor between the channel area of the first semiconductor, the channel area of the second semiconductor, and the channel area of the fifth semiconductor.

Claim 22
22. The display apparatus of claim 21, wherein the fourth shield layer is a part of the second electrode layer.
Claim 23
23[a] The display apparatus of claim 22, further comprising a capacitor comprising a first capacitor plate and a second capacitor plate,
23[b] wherein the first capacitor plate is a part of the first electrode layer, and the second capacitor plate is a part of the second electrode layer.
Claim 24
24[pre] A display apparatus comprising:
24[a] a first thin-film transistor comprising a first semiconductor;
24[b] a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;
24[c] a first signal line over the first electrode layer;
24[d] a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line; and
24[e] a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.
Claim 25
25[a] The display apparatus of claim 24, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and

25[b] wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

Claim 26

26. The display apparatus of claim 24, wherein the shield layer is a part of the voltage line.

Claim 27

27. The display apparatus of claim 24, further comprising a connecting line connecting the one end of the second semiconductor and the first electrode layer and being in the same layer as the first signal line.

Claim 28

28[pre] A display apparatus comprising:

28[a] a first thin-film transistor comprising a first semiconductor;

28[b] a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;

28[c] a first signal line over the first electrode layer;

28[d] a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and

28[e] a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

Claim 29

29[a] The display apparatus of claim 28, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the

second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and
29[b] wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.
Claim 30
30. The display apparatus of claim 28, further comprising a voltage line in the same layer as the first signal line, wherein the shield layer is connected to the voltage line.
Claim 31
31. The display apparatus of claim 28, further comprising a second electrode layer over the first electrode layer and overlapping the first electrode layer, wherein the shield layer is a part of the second electrode layer.
Claim 32
32. The display apparatus of claim 31, further comprising a voltage line in the same layer as the first signal line, wherein the voltage line is connected to the second electrode layer.
Claim 33
33[pre] A display apparatus comprising:
33[a] a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;
33[b] a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;
33[c] a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;

33[d] a first signal line over the second electrode layer; and
33[e] a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor,
33[f] wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line,
33[g] wherein the first signal line extends in a first direction, and
33[h] wherein a length along the first direction of the overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction.

I, Ronald S. Cok, do hereby declare as follows:

I. INTRODUCTION

1. My name is Ronald S. Cok, and I have been retained by counsel for Petitioner (“Petitioner” or “BOE”) as a consultant to provide my opinion regarding certain prior-art references and U.S. Patent No. 10,439,015 (the “’015 Patent”).

2. I make this Declaration based upon my own personal knowledge and, if called upon to testify, will testify competently to the matters stated herein.

3. I have been asked to provide my expert opinion in connection with the Inter Partes Review (IPR) of the ’015 Patent to Kim *et al.* concerning whether it is unpatentable over certain prior art. This Declaration is a statement of my opinions on issues relating to the patentability of claims 1-33 (the “Challenged Claims”) of the ’015 Patent. As I explain more fully below, it is my opinion that all of the Challenged Claims would have been obvious to a person of ordinary skill in the art (“POSITA”) at the time of the alleged invention.

4. I am being compensated for my work in this matter at my standard hourly rate. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation. My compensation is not contingent on the outcome of this matter or the specifics of my testimony. I have reviewed and considered the following documents in connection with my analysis of the ’015 Patent:

- EX1001: U.S. Pat. No. 10,439,015 (“’015 Patent” or “’015 Pat.”)
- EX1002: File History of the ’015 Patent (“’015FH”)
- EX1004: U.S. Pat. Pub. No. 2014/0132584 A1 (“Kim-584”)
- EX1005: U.S. Pat. Pub. No. 2012/0019504 A1 (“Han”)
- EX1006: U.S. Pat. Pub. No. 2014/0034923 A1 (“Kim-923”)
- EX1007: U.S. Pat. Pub. No. 2014/0042405 A1 (“Moon”)
- EX1008: U.S. Pat. Pub. No. 2014/0098078 A1 (“Jeon-078”)
- EX1009: RESERVED
- EX1010: Japanese Pat. No. 3,858,572 (“Masao”)
- EX1011: U.S. Pat. No. 6,225,966 B1 (“Ohtani”)
- EX1012: N. H. E. Weste et al., CMOS VLSI Design: A Circuits and Systems Perspective, Fourth Edition, Addison-Wesley, 2011 (“Weste”)
- EX1013: U.S. Pat. No. 5,136,358 (“Sakai”)
- EX1014: U.S. Pat. No. 5,285,017 (“Gardner”)
- EX1015: U.S. Pat. No. 6,510,545 (“Yee”)
- EX1016: U.S. Pat. No. 8,692,297 (“Ho”)
- EX1017: U.S. Pat. No. 6,622,294 (“Saxena”)
- EX1018: U.S. Pat. No. 8,670,099 (“Xie”)
- EX1019: U.S. Pat. No. 8,988,852 (“Signoff”)

- EX1020: Chinese Pat. Pub. No. 113936600 (“Tian”)
 - EX1021: U.S. Pat. Pub. No. 2014/0320544 (“Kim-544”)
 - EX1022: U.S. Pat. Pub. No. 2014/0070184 (“Shin”)
 - EX1023: U.S. Pat. Pub. No. 2007/0007535 (“Tang”)
 - EX1024: RESERVED
 - EX1025: Korean Patent Pub. No. 20050052033 (“Kim-033”)
 - EX1026: U.S. Pat. Pub. No. 2011/0025585 (“Kim-585”)
 - EX1027: Korean Pat. Pub. No. 19840006800 (“Hong”)
 - EX1028: U.S. Pat. No. 8,487,311 (“Liu”)
 - EX1029: U.S. Pat. No. 8,514,155 (“Kobayashi”)
 - EX1030: U.S. Pat. No. 8,269,696 (“Tomida”)
 - EX1031: U.S. Pat. No. 7,855,507 (“Kim-507”)
 - EX1032: U.S. Pat. No. 8,653,521 (“Hwang”)
 - EX1033: U.S. Pat. No. 8,701,068 (“McElvain”)
5. In forming the opinions expressed below, I have considered:
- the documents listed above;
 - the relevant legal standards as explained to me by the Petitioner’s counsel, including the standard for obviousness, and any additional authoritative documents as cited in the body of this Declaration;

- my own knowledge and experience based upon my work in the field of flat-panel displays as described below; and
- any other documents not listed above but cited below.

6. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Samsung Display Co. (“Patent Owner” or “SDC”). Further, I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

7. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This Declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

8. Unless otherwise noted, all emphasis in any quoted material has been added.

II. TECHNICAL QUALIFICATIONS AND EXPERIENCE

9. I am an expert in the field of displays, and in particular for organic and inorganic light-emitting-diode flat-panel displays (FPDs). I have studied, researched, and practiced in this field for over 26 years. The following is a brief summary of my relevant qualifications and professional experience.

10. I earned my Bachelor of Arts in Science degrees in Physics (with Honors) and in Mathematics at Calvin College (now Calvin University) in Grand Rapids, Michigan, in 1980 and a Master of Science degree in Electrical Science from the University of Michigan in 1981. I have extensive technical experience in Physics, Mathematics, Electrical Engineering, and Computer Science.

11. Following my graduation from the University of Michigan, I worked in the Eastman Kodak Research Laboratories for 34 years, first as a research scientist working in electronic image processing, then as a senior research scientist, project manager, and digital commercialization manager working in supercomputers for image processing, digital cinema, imaging kiosks, and on-line image fulfillment, including a stint in the United Kingdom managing the digital imaging activities of three European research laboratories. I then transitioned to a Senior laboratory head and research fellow role for distributed wireless (IEEE 802.11) and OLED systems in late 1999. I worked extensively in OLED display systems for over ten years. My activities included technology development, publication, and extensive patent activities for core elements of OLED display technology, systems, and applications. OLED projects were related to quantum dots, wide-format curved displays, touch screens, alternative backplanes, RGBW designs, electronic compensation and light output enhancement, and single-use masking. We constructed the world's first

passive- and active-matrix OLED displays. I also served as Company liaison for universities and external start-ups for technology development.

12. Since 2015, I have worked with X-Celeprint, Inc. as a Director and with X Display Company on micro-assembly, including inorganic LED displays and systems. We demonstrated and patented the world's first full-color active- and passive-matrix micro-inorganic LED displays. These activities included system design for optical and electronic performance, touching on human factors, optical and signal transmission, control methods, and circuit designs.

13. I have managed and contributed to the development and commercialization of thirteen digital imaging products. My work in digital cinema technology earned a Technical Achievement Award from the Academy of Motion Picture Arts and Sciences (an Oscar). I have approximately 650 patents, most in the field of LED displays, as well as over 60 papers in professional or scientific journals. Projects and proposals included work for the U.S. Treasury, U.S. Postal Service, and DARPA. A more detailed account of my professional experience is provided in my CV, which is attached as Appendix A.

14. I taught as an Adjunct Professor in the graduate school of computer engineering at the Rochester Institute of Technology for three years, authored a textbook on parallel computing (Prentice Hall, 1991), served as an Associate Editor

for a professional journal (Wiley), and am certified in Black Belt Management. I have been recognized as a USA top inventor for 2003-2005 and won an IR&D 100 Innovation and Excellence award. I have been a member of the Society of Information Display for over ten years.

15. Considering the foregoing, I consider myself to be an expert in the field of flat panel displays and integrated circuits manufacturing, including OLED displays, and including thin film deposition techniques, etching chemistry, chemical-mechanical polishing, devices and circuits processing and photolithographic steps, and the designs used in the fabrication of devices and circuits, with the feature sizes ranging from micron to submicron for various industrial applications including FPDs. Therefore, I believe that I am qualified to provide an opinion as to what a person of ordinary skill in the art (“POSITA”) at the time of the invention around 2014 would have understood, known, or concluded regarding the subject matter of the patents involved in this case.

III. LEVEL OF ORDINARY SKILL IN THE ART

16. My analysis reflects the views of a person of ordinary skill in the art (POSITA) in the field of the '015 Patent as of August 5, 2014, which I understand is the alleged time of invention.

17. I have been advised by the Petitioner’s counsel and understand there are multiple factors relevant to determining the level of ordinary skill in the pertinent

art, including (1) the levels of education and experience of persons working in the field at the time of the invention; (2) the sophistication of the technology; (3) the types of problems encountered in the field; and (4) the prior-art solutions to those problems. I understand that a POSITA is not a specific real individual but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from teachings of the prior art, including the art cited below.

18. Taking these factors into consideration, in my opinion, on or before August 5, 2014, a POSITA would have been someone knowledgeable and familiar with design or development of thin-film transistor (TFT) display circuits and systems that are pertinent to the '015 Patent. That person would have a bachelor's degree in electrical engineering, physics, materials science or engineering, or a related field and at least four years of practical experience with design or development of flat-panel displays, including pixel layout, or the equivalent. In my opinion, a lack of work experience can be remedied by additional education, and vice versa.

19. As of August 5, 2014, I met, and in fact exceeded, the qualifications of a person of ordinary skill in the art.

20. For purposes of this Declaration, in general, and unless otherwise noted, my statements and opinions, such as those regarding my experience and the understanding of a POSITA generally (and specifically related to the references I consulted herein), reflect the knowledge that existed in the field as of the earliest possible priority date of the '015 Patent (i.e., August 5, 2014). Unless otherwise stated, when I provide my understanding and analysis below, it is consistent with the level of a POSITA prior to the earliest alleged priority date of the '015 Patent.

IV. RELEVANT LEGAL STANDARDS

21. I am not an attorney. Petitioner's counsel has explained certain legal principles, which have assisted me in the preparation of this Declaration, considering the subject matter of the '015 Patent.

22. I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious in view of what was known before the invention was made.

23. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

24. I understand that in this proceeding Petitioner has the burden of proving that the claims of the '015 Patent are anticipated by or obvious in view of the prior

art by a preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not.

25. I understand that prior art to the '015 Patent in this proceeding includes patents and printed publications in the relevant art that predate the proper priority date of the alleged invention recited in the '015 Patent.

26. I understand that terms appearing in the patent claims are to be interpreted according to their “ordinary and customary meaning” in an IPR proceeding. In determining the ordinary and customary meaning, the words of a claim are first given their plain meaning as they would have been understood by a POSITA at the time of the alleged invention, in light of the specification and file history. I understand that treatises and dictionaries may be consulted, albeit under limited circumstances, to determine the meaning attributed by a POSITA at the time of the alleged invention. I have followed this approach in my analysis and have applied the ordinary and customary meaning of those terms throughout my analysis in this Declaration.

27. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to “anticipate” the claim. Second, the prior art can be shown to have made the claim “obvious” to a person of

ordinary skill in the art. In this Declaration I focus on “obviousness.” My understanding of the legal standard for “obviousness” is set forth below.

28. I have been informed that a claimed invention is unpatentable as obvious if the differences between the invention and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. I have also been informed by counsel that the obviousness analysis takes into account factual inquiries including the level of ordinary skill in the art, the scope and content of the prior art, and the differences between the prior art and the claimed subject matter.

29. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

30. I have been informed by counsel that the Supreme Court has recognized several rationales for combining references or modifying a reference to show

obviousness of claimed subject matter. Some of these rationales include the following: (a) combining prior-art elements according to known methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention. I also understand that, at least in IPR proceedings, admissions in the patent or in the prosecution file history of the patent (referred to as Applicant Admitted Prior Art or “AAPA”) can be used to, among other things, establish background knowledge possessed by a POSITA.

31. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the

alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

32. I am not aware of any allegations that any secondary considerations are relevant to the obviousness analysis of any Challenged Claim of the '015 Patent.

33. I understand that for a claim to be valid, its scope must be definite, and that improperly introducing a term can lead to an unascertainable scope of a term, rendering it indefinite. I understand that any claim element first addressed in the claims by the antecedent basis, “a” may then be identified later in the claims by the antecedent basis, “the.” I understand that failing to follow this convention may lead to ambiguity in the identification of the particular claim element in question, leading to an indefinite scope of the claim’s term. For purposes of this proceeding, I identified and provided my best understanding of any such terms despite such ascertainable scope.

V. SUMMARY OF THE '015 PATENT

A. Specification

34. The '015 Patent describes a display apparatus that includes a thin-film transistor (TFT) having source, drain and gate electrodes, and a data (signal) line in a layer different from the source, drain, and gate electrodes. '015 Pat., Abstract. The data line is configured to transmit a data signal, and a shield layer is located between the data line and a component of the thin-film transistor. *Id.*

35. While the figures of the '015 Patent, “according to some embodiments,” show a circuit and TFT layouts associated with a pixel of an organic light-emitting diode (OLED) display (*id.*, 3:10-34, 4:6-9), the specification of the '015 Patent makes it clear that its embodiments are “**not limited to an organic light-emitting display apparatus**. An image having high quality may be displayed as long as a display apparatus including a TFT and a data line in a (sub) pixel has a shield layer in the same or similar manner described above.” *Id.*, 16:63-67. The '015 Patent’s intention to expand its alleged invention to non-OLED display devices is also evident from the “Abstract,” the “Field” subsection (*id.*, 1:15-17), referencing “a display apparatus,” and its 33 claims (*id.*, 17:12-20-57), none of which describe or require an OLED or OLED display.

36. Fig. 1 of the '015 Patent (annotated below) shows a circuit that includes a plurality of signal lines (121-124 and 171-172), a plurality of TFTs (T1-T6), a

storage capacitor (Cst), and an OLED coupled to the plurality of signal lines, and in particular coupled at one end to emission control TFT T6. When TFT T2 is in a switched-on state, driving TFT T1 receives data signal Dm and supplies a driving current IOLED to the OLED. *Id.*, 4:39-42.

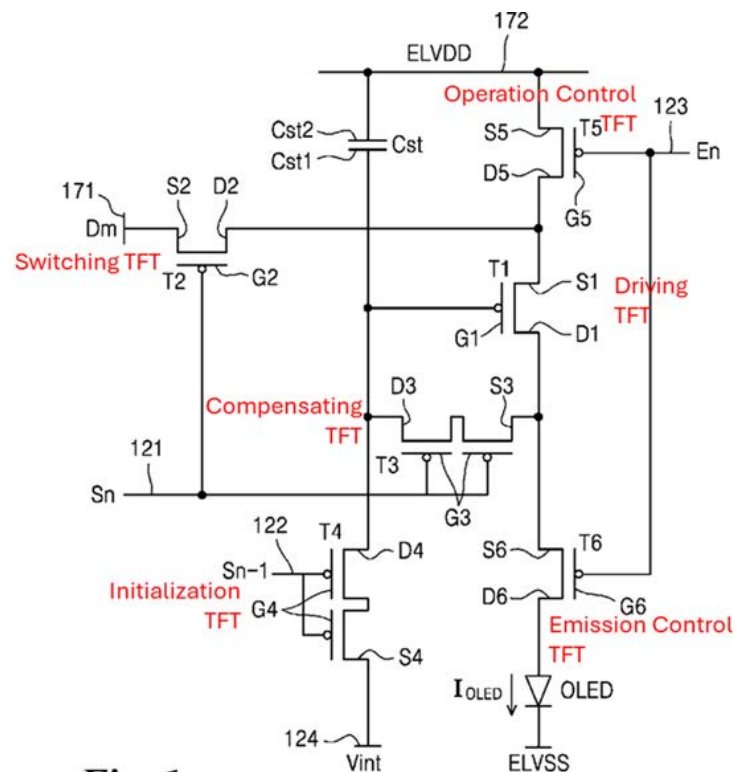


Fig. 1

37. The six TFTs T1-T6 are formed in a semiconductor region, and each TFT includes a source region, a drain region, and a channel region. *Id.*, 7:18-24 The '015 Patent describes TFTs T3 and T4, in some cases, may be “dual gate electrode” TFTs that “may prevent or reduce generation of a leakage current.” *Id.*, 8:42-47, 14:62-65; 15:36-45.

38. To prevent quality deterioration of a displayed image, one or more shield layers are disposed between a layer containing a signal line and a layer containing the TFTs. *Id.*, 1:34-36, 46-48.

39. The use of shield layers is shown in the example of Fig. 5 (below for SD1, SD2, SD3). The shield layers are not necessarily independent layers, wires, or conductive areas in a circuit but rather can be extensions of other components within an OLED pixel element, or a component within the pixel element can perform dual functions, one of which is to act as a shield. *See, e.g., id.*, 15:3-5. For example, first shield layer SD1 can be part of a second storage capacitor plate. *Id.*, 11:11-13. SD1 helps to prevent compensating TFT T3 from being affected by data line 171. *Id.*, 11:29-33. SD2 is part of initialization voltage line 124 and shields T4 from data line 171. *Id.*, 12:28-30, 52-56. SD3 is part of the second storage capacitor plate and shields TFT T1. *Id.*, 13:47-48, 14:16-26.

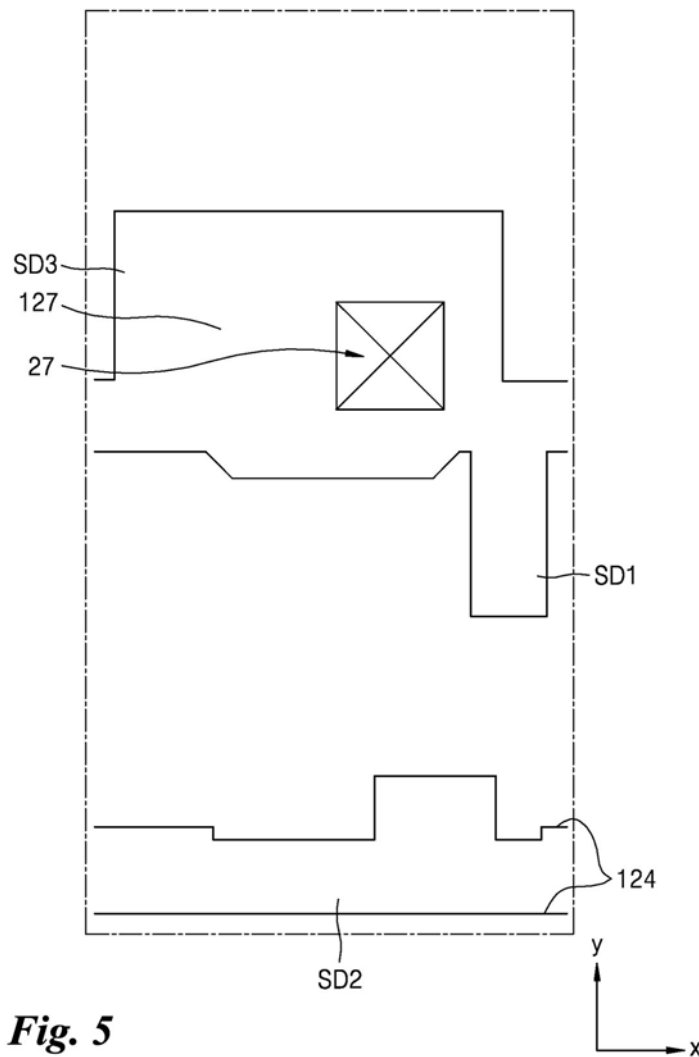


Fig. 5

B. Prosecution History

40. I understand that the '015 Patent issued from U.S. Patent Application No. 15/838,138, filed on December 11, 2017. The '015 Patent claims priority to Korean Patent Application No. 10-2014-0100700, filed August 5, 2014.¹

¹ August 5, 2014, is assumed to be the priority date for purposes of this Petition only.

41. The application was originally filed with a single claim, which was canceled after two Office Actions that rejected the sole claim as being anticipated by Lee et al. (U.S. Pat. Pub. No. 2014/0167009). EX1002, pp. 170-175, 243-247, 375. The Applicant then canceled the pending claim and filed new claims, which were allowed without an Office Action. *Id.*, pp. 113-120, 152-158. The Notice of Allowance did not indicate the closest prior art, but stated that the prior art does not anticipate nor render obviousness with respect to a display apparatus comprising amongst other limitations: a first signal line over the second electrode layer; and a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor. *Id.*, p. 118.

42. By my review, Jeon-078 was cited in an Information Disclosure Statement (IDS) filed by the Applicant on December 11, 2017. *Id.*, p. 322. However, Jeon-078 was not relied upon during the prosecution, and the use of Joen-078 in this Petition is not cumulative. *See* §VIII.F.

VI. TECHNOLOGY BACKGROUND

A. Introduction to Flat-Panel Displays and TFTs

43. Flat-panel displays have displaced the 127-year-old cathode ray tube technology because the flat panels can have a much superior (thinner) form factor with a larger viewing area, greater resolution, reduced power, and a much smaller

volume and weight. Most flat-panel displays are formed on a glass substrate coated with a thin film of silicon. (There are micro-displays formed on silicon substrates, but they are not at issue here.) The coated silicon is typically amorphous or polycrystalline and has a much lower performance than mono-crystalline silicon found in most integrated-circuit chips. Thus, pixel control circuits formed on display substrates are generally larger and slower than those in conventional integrated-circuit chips. Despite this performance difference, the fundamental nature of TFT circuits is the same as in integrated circuits. Issues including circuit area/density, performance, signal integrity, number of connection layers, and such are very similar or identical.

44. Flat-panel displays generally include a display substrate on which is deposited a single thin film of silicon. Circuits are formed in the thin film using photolithographic processes that are very similar to or the same as those of the integrated-circuit (chip) industry. The thin-film silicon is doped to control its behavior and patterned to form transistors (thin-film transistors or TFTs). A typical transistor has a source (for providing current), a gate for switching the transistor on or off, and a drain (from which switched current can be used). Each of these transistor elements is connected to an electrode for supplying the appropriate signal to the element. A portion of the semiconductor beneath the gate is called a channel

and the source and drain semiconductor portions are often doped with additional material to enhance their performance characteristics (as the channel can), depending on the type of transistor. No transistor is perfect and TFTs can suffer from current leakage, unwanted current flow that occurs even when the transistor is off. Circuits are often designed to reduce this leakage, as it can result in a pixel emitting light when it is not supposed to, impacting the display black level, an advantage of OLED displays.

45. Layers of conductive metal wires separated by insulating layers (inter-layer dielectric or ILDs) are formed over the thin-film silicon layer and connected to the transistors as electrodes directly or through vias formed in the ILD to form a control circuit connected to each display picture element (pixel) forming an image on the flat-panel display.

B. TFT-Based Control Circuits for Flat-Panel Displays

46. Thin-film circuits can control a variety of light controllers or light emitters in a corresponding variety of displays. Liquid crystal displays (LCDs) were the first widely adopted flat-panel-display technology. More recently, organic light-emitting-diode (OLED) displays entered the marketplace in 1997, initially in small displays (for cell phones, smart watches, and the like) and more recently in laptops and televisions. In any case, the thin-film circuits are designed to effectively control each pixel and adapted to the needs of the light-emitting or light-controlling

technology of each display. The chosen circuit should effectively and uniformly control a pixel in the presence of manufacturing variability, including variability in the deposited silicon (the epitaxial layer or epi), the circuit patterning and construction, and the light emitter.

47. Electronic circuits (such as those in TFT pixel-control circuits) are generally optimized to the extent possible to ensure good performance and small size. Such optimization inevitably requires tradeoffs and compromises in the display. Modelling and layout software are frequently used to assist with such optimization and circuit layout. In particular, TFT circuits (in common with all electronic circuits) produce and are susceptible to electromagnetic radiation that interferes with the performance of the circuit (often known as electromagnetic interference or EMI) as well as unwanted, parasitic electronic behavior, such as unwanted capacitance, resistance, and inductance in the circuit. EMI radiation is produced by the acceleration of electrons (inherent in any transistor circuit), and parasitic capacitance, resistance, and inductance are produced by circuit elements that are not perfectly conductive, are not perfectly straight, or have adjacent elements – that is, all practical and physical circuits suffer from these issues. In particular, EMI emitted by one portion of a circuit can be absorbed by another portion of the circuit, since wires in one portion of a circuit act as antennae that can absorb electro-magnetic radiation

from another different portion of the circuit. The absorbed radiation (electronic noise) can affect or overwhelm the signals transmitted in the wires that receive the radiation and cause a circuit to fail or behave in unwanted ways. These design and layout issues have been understood and addressed for many decades in integrated-circuit design and are likewise present in thin-film circuits and the circuits can likewise be designed to compensate for such issues.

C. Design and Layout Considerations for TFT-Based Control Circuits

48. Unwanted electrical effects (e.g., parasitic phenomenon, transient behaviors, charge trapping instabilities, etc.) are typically addressed by carefully laying out the TFT circuit to minimize the problems, as well as conforming to circuit performance requirements and spatial considerations in each pixel in a flat-panel display. A variety of layout options are available to a circuit designer, and these can be tested using modeling tools and layout software that can assist the designer. Typically, different layouts are attempted and the best one meeting the overall needs of the system is chosen.

49. A particular circuit can be laid out in many ways on a substrate. Often, however, there are useful conventions that a POSITA or a designer can follow to simplify the task. For example, signal lines in a circuit connected to an external signal source are often (but not necessarily) routed on a top layer of a multi-layer

circuit (e.g., having multiple wire layers known as metal layers). This convention is useful for electrically connecting to connectors that would otherwise require additional connections to the lower layers, and for enabling testing as the signals can be readily contacted when on a top layer. The signals can then be routed through vias to other layers for use, connection, or processing, e.g., by thin-film transistors.

50. The use of multiple metal layers connected by vias in integrated circuit design (such as TFT circuits) is a typical and well-known method for routing wires in a circuit. The specific layout of the wires is usually chosen to optimize desirable circuit characteristics, such as electrical efficiency, electrical noise suppression, minimum number of metal layers (to reduce cost), spatial area, or fit to a desired form factor. Most often, some combination of these is chosen and can be implemented (laid out) in a variety of configurations. The circuit design and layout skillset possessed by a POSITA is evidenced, for example, by Kobayashi (EX1029) disclosing an OLED display with voltage and ground connections together with select and data signals controlling an amorphous silicon thin-film transistor circuit disposed, connected, and routed on a glass substrate; Tomida (EX1030) teaching circuit and physical layouts for an electroluminescent display panel including a pixel circuit; and Kim-507 (EX1031) teaching circuit diagrams and physical layouts for an OLED device.

51. The understanding possessed by a POSITA in this area is further demonstrated, for instance, by textbooks such as *CMOS VLSI Design: A Circuits and Systems Perspective* (by N. Weste and D. Harris, 2011) (EX1012). This reference addresses, among other topics, layout design rules that “describe how small features can be and how closely they can be reliably packed in a particular manufacturing process,” Weste, Chapter 1.5.3. It also explains that “[t]he rules are defined in terms of feature sizes (widths), separations, and overlaps, [and wherein] [t]he main objective of the layout rules is to build reliably functional circuits in as small an area as possible.” Weste, Chapter 3.3; *see generally* Weste, Chapters 1 and 3. Certain design rules related to using electronic “shields” and TFTs with two or more gate electrodes, which were well-known in both industry and academia by 2014, are discussed next.

D. Electronic Shielding in TFT-Based Control Circuits

52. One method to reduce EMI noise in a circuit is to construct electronic “shields”. These shields are typically electrically conductive wires or areas (such as capacitor plates) placed between or adjacent to signal wires. The variation in the signal in the wires produces radiation (EMI) that is absorbed by the shields rather than by another signal wire, thereby preventing or reducing any electronic noise that might otherwise be absorbed by the other signal wire. The shields are typically electrically connected to a fixed voltage (usually a ground or power supply voltage)

that is difficult to change or of sufficient quality that any absorbed radiation in the ground or power supply voltage has no or limited effect on the circuit performance. Thus, the use of shields improves the circuit performance by reducing electronic noise.

53. I also note that such shielding methods have been known and in use for many years, for example Sakai (EX1013) in 1991 disclosed a multi-layered wiring structure including thin-film transistors and shield lines for absorbing electrical effects. Other designs include (i) shield areas (such as ground or power planes in printed circuit boards, as disclosed in Gardner (EX1014)), (ii) multiple interdigitated signal and shield wires in a plane or in an adjacent plane, and (iii) the use of capacitor plates to act as shields.

54. Using wires as shields typically involves using a “shield wire” with a constant (or reference) potential that can be placed adjacent to a signal-carrying wire or trace, and which absorbs or redirects electromagnetic fields that would otherwise couple into the adjacent signal lines. In an example, Yee (EX1015) teaches adding VDD and VSS shields between wires for reducing charge loss due to capacitive coupling, as illustrated in Fig. 4 below. Yee, 2:5-9, Fig. 4.

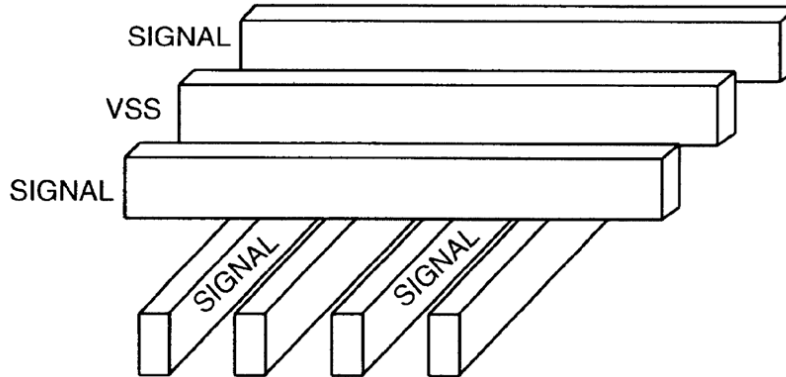


FIG. 4

55. Shield wires are ubiquitous in the integrated circuit art and are disclosed, for example, in Yee, Abstract (“shielding integrated circuits... by inserting VDD and VSS wire proximate to signal wires on the same metal layer”); Saxena (EX1017), 2:36-37 (“minimize switching cross-capacitance by shielding sensitive signal nets using power supply (Vcc) and ground (Vss) lines”); Ho (EX1016), Abstract (“routing of a shield mesh of both power and ground lines to remove noise created by capacitive and inductive coupling”), Hwang (EX1032), 4:11-13 (“a shield line 136 overlapping the data line 107 [that] prevents an unnecessary electric field from being formed”); and McElvain (EX1033), 9:47-50 (“a shielding mesh of at least two reference voltages (e.g., power and ground) is used to reduce both capacitive coupling and inductive coupling in signal wires”).

56. As noted above, capacitor plates can also be used to act as shields against EMI, as disclosed in Saxena, 1:32-39 (“area used by the shields”); Xie

(EX1018), 8:46-55 (“the first pixel electrode and the first shield line constitute storage capacitor, so the first shield line of the present embodiment also acts as a storage electrode”); Kim-585 (EX1026), ¶83 (“the other electrode (second electrode) of the storage capacitor Cst... coupled to... the constant voltage source,... the effects of the voltage fluctuation of the data line... are blocked”); Signoff (EX1019), 3:39-41 (“couples ground shield capacitor 300 to a first reference voltage, such as a supply voltage”); and Tian (EX1020), ¶¶9, 43 (“first shielding module comprises at least one first shielding capacitor, the first end of the first shielding capacitor is connected with the first intermediate node... so as to reduce the electric potential change of the first end of the light emitting module. The first shielding capacitor can stabilize the potential of the first intermediate node, so as to reduce the leakage of the first multi-gate transistor, which is good for displaying uniformity.”)

E. Multi-Gated Transistors in TFT-Based Control Circuits

57. Multi-gated TFTs are frequently used in pixel driving circuits for flat-panel displays, such as active-matrix liquid crystal displays (AMLCDs) and organic light-emitting diode (AMOLED) panels, due to their ability to enhance device performance and display quality. In conventional single-gate TFTs, issues such as leakage current, poor subthreshold characteristics, and limited control over the channel can degrade the performance of the pixel circuit, leading to image retention, reduced contrast, and higher power consumption. By incorporating multiple gates,

designers can achieve better electrostatic control over the channel, which significantly reduces leakage currents and improves the switching characteristics of the TFTs. The use of multi-gated TFTs also enables more precise control of the threshold voltage and enhances the uniformity of the electrical characteristics across the display panel. For example, multi-gated TFTs can be used in compensation circuits to correct for threshold voltage shifts and mobility variations, ensuring consistent brightness and color accuracy across the screen.

58. I note here that multi-gated TFTs have been known and used for many years before the 2014 priority date of the '015 Patent. For example, Kim-544 (EX1021) provides a “dual compensation gate electrode” that can “reduce an off-leakage current” in an OLED device. Kim-544, Abstract, ¶¶107, 111. Shin (EX1022) teaches a dual-gate transistor that includes “a first compensation gate electrode and a second compensation gate electrode” for reducing a leakage current. Shin, Abstract, ¶43. Tang (EX1023) teaches using a dual-gate transistor structure to reduce leakage current in a pixel circuit for a light-emitting display. Tang, ¶¶3,19-20, Fig. 3B. Kim-033 (EX1025) describes using dual-gate switching (T32) and threshold compensation transistors (T33) to decrease off current when turned off, thereby reducing leakage current. Kim-033, ¶46. Hong (EX1027) teaches that the pair-gate structure employed in the disclosed thin-film transistor therein prevents an increase

in leakage when the gate voltage V_{gs} is negatively biased. Hong, p. 2:16-17. In addition, Kim-584 (EX1004), Han (EX1005), Kim-923 (EX1006), Moon (EX1007), Jeon-078 (EX1008) and Ohtani (EX1011) used in the invalidity grounds all describe multi-gated TFTs.

VII. CLAIM CONSTRUCTION

59. It is my understanding that in order to properly evaluate the Challenged Patent, the terms of the claims must first be interpreted. It is my understanding that for the purposes of this inter partes review, the claims are to be construed under the so-called *Phillips* standard, under which claim terms are given their ordinary and customary meaning as would have been understood by one of ordinary skill in the art in light of the specification and prosecution history, unless the inventor has set forth a special meaning for a term. For the purposes of this Declaration, I have given all the claim terms of the Challenged Claims their plain and ordinary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I assume is August 5, 2014, for all claims.

VIII. CLAIMS 1-33 ARE UNPATENTABLE

60. The discussion below provides a detailed analysis of my opinion as to how a POSITA would have found the Challenged Claims obvious in view of the prior-art references based on the Grounds identified in the table below.

Ground	Prior Art	Claims
1A	Kim-584	1-4, 8-10, 20-23, 33
1B	Kim-584 + Han	5, 11-14, 28-32
2A	Kim-923	1-4, 8-10, 20-23, 33
2B	Kim-923 + Moon	6-7, 15-19, 24-27
2C	Kim-923 + Han	5, 11-14, 28-32
3	Moon + Jeon-078	24-27
4A	Masao	1-2, 8-10, 33
4B	Masao + Ohtani	5, 11, 13, 28-29, 31

A. Ground 1A: Kim-584 Renders Obvious Claims 1-4, 8-10, 20-23, and 33

1. Summary of Kim-584

61. Kim-584 describes an organic light-emitting display (OLED) device that utilizes a mesh structure for wires that supply a power supply voltage in order to prevent dropoff of the voltage and minimize leakage current. Kim-584, ¶8. The OLED devices described in Kim-584 are active-matrix OLED devices that utilize a six-transistor-one-capacitor (6T1C) structure. *Id.*, ¶95. Some embodiments of Kim-584 seek to minimize parasitic capacitance in order to prevent increasing black luminance. *Id.*, ¶93.

2. Claim 1

a. 1[pre]: “A display apparatus comprising:”

62. In my opinion, Kim-584 teaches or suggests limitation 1[pre].

63. Kim-584 describes a “[a]n organic light-emitting **display device.**” Kim-584, Abstract. Fig. 1 of Kim-584 illustrates a “display device 100” that “includes a display unit 10 including a plurality of pixels, a scan driver 20, a data driver 30, and a controller 40.” Kim-584, ¶31. This describes a well-known standard matrix-controlled array of pixels with a scan driver (row-select) circuit to select rows of pixels and a data driver (column-data) circuit providing data to each pixel in a selected row of pixels.

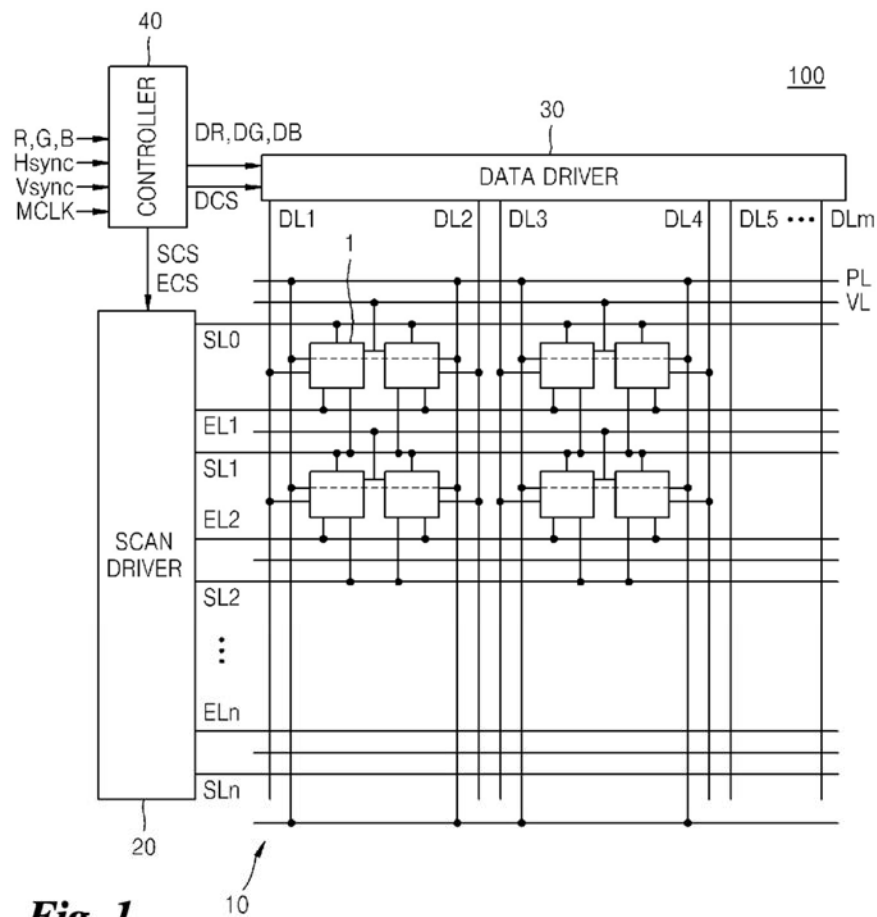


Fig. 1

- b. 1[a]: “a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;”

64. In my opinion, Kim-584 teaches or suggests limitation 1[a].

65. Kim-584 discloses “a first thin-film transistor” as TFT T1 that is illustrated in its Fig. 3 (annotated below; ¶44, “driving TFT T1”).

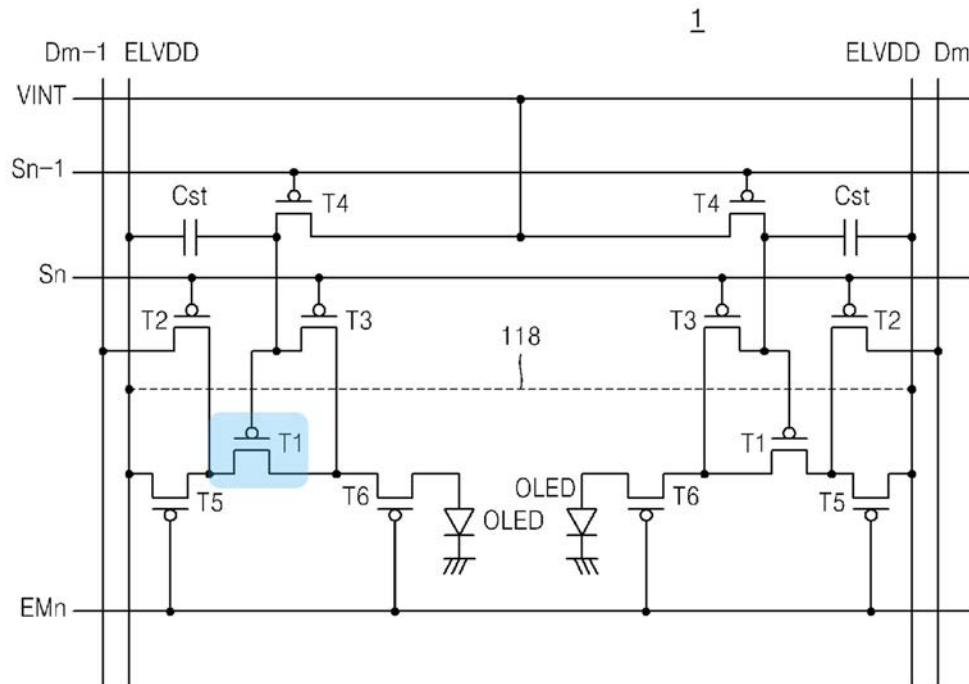


Fig. 3

66. Kim-584 discloses “the first semiconductor comprising a source area, a drain area, and a channel area” because Kim-584 explains that its driving TFT T1 has an active layer A1 (“first semiconductor”), and “[a]n active layer of each TFT includes a **channel area** which is not doped with impurities, and **source and drain**

areas which are formed by doping **both sides of the channel area** with impurities.”

Kim-584, ¶63, Figs. 5 and 6. Kim-584 also teaches that the active layers are made of a semiconductor: “[t]he first and second active layers 112-1 and 112-2 may be formed as amorphous silicon layers, polycrystalline silicon layers, or **oxide semiconductor layers** such as G-I-Z layers [(In₂O₃)_a(Ga₂O₃)_b(ZnO)_c layer] (wherein a, b, and c are real numbers satisfying a condition of $a \geq 0$, $b \geq 0$, and $c > 0$).”

Kim-584, ¶62.

67. I note that Fig. 5 of Kim-584 further illustrates the active layers of two adjacent pixels, where “TFTs of a pixel circuit are formed along the first and second active layers 112-1 and 112-2. **Active layers A1, A2, A3, A4, A5, and A6 of a driving TFT T1**, a switching TFT T2, a compensation TFT T3, an initialization TFT T4, a first emission control TFT T5, and a second emission control TFT T6 are formed on each of the first and second active layers 112-1 and 112-2.” Kim-584, ¶63, FIG. 5. As explained in §VIII.A.2.b for limitation 1[a], the ’015 Patent describes a conventional thin-film transistor (TFT) as shown in Figs. 5 and 6 and described in Kim-584.

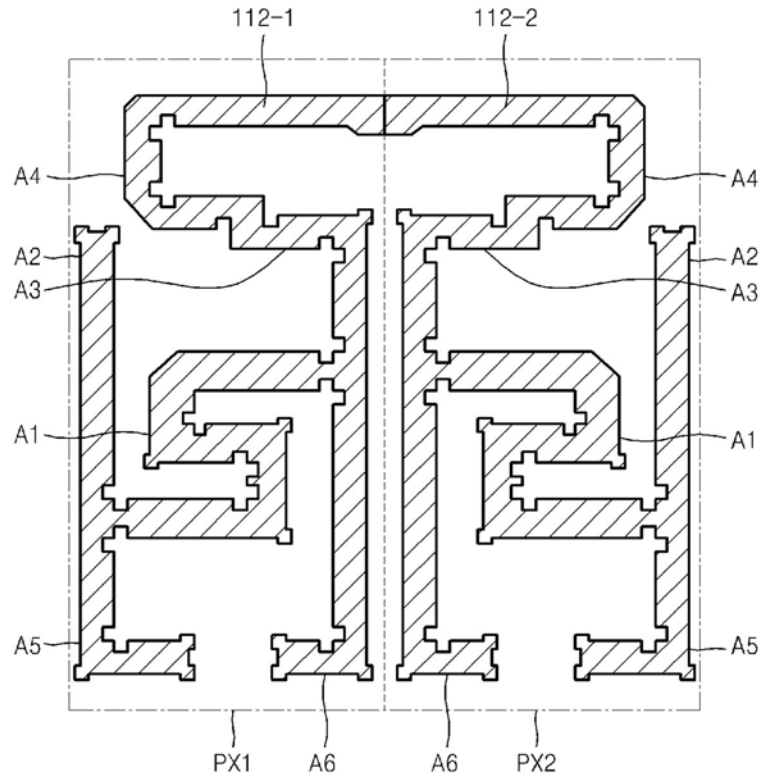


Fig. 5

68. Accordingly, limitation 1[a] is disclosed by Kim-584.

c. **1[b]: “a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;”**

69. In my opinion, Kim-584 teaches or suggests limitation 1[b].

70. As a preliminary matter, I note that in order to function, a TFT requires an “electrode layer” that includes electrodes (electrically conductive lines or wires) disposed in electrical contact with the source and drain (to provide or receive electrical current) and over and insulated from the channel between the source and

drain as a gate to control the current flow. This is a necessary and standard TFT design requirement and is taught in Kim-584.

71. Kim-584 discloses “a first electrode layer over the first semiconductor” as the electrode layer that includes first capacitor electrode 114-1 (which also operates as the gate of TFT T1). In particular, Kim-584 explains that “first gate lines are formed on the first gate insulating layer 102. The first gate lines may include a first scan line S_L_n, a second scan line S_L_n-1, an emission control line E_L_n, and **first capacitor electrodes 114-1 and 114-2.**” Kim-584, ¶66. Kim-584 further explains that “[t]he **first capacitor electrodes 114-1 and 114-2 operate as gate electrodes G1 of the driving TFTs T1 . . .** and overlap with the channel areas of the active areas A1 of the TFTs T1 in floating electrode shapes.” *Id.*, ¶67.

72. Kim-584 describes the layout of two adjacent pixels PX1 and PX2 in its various figures, including Figures 5 through 9. Kim-584, ¶58. In my analysis, I have focused on the features (active layer, voltage and data lines, transistors, and capacitor electrodes) of one of the pixels, namely PX1.

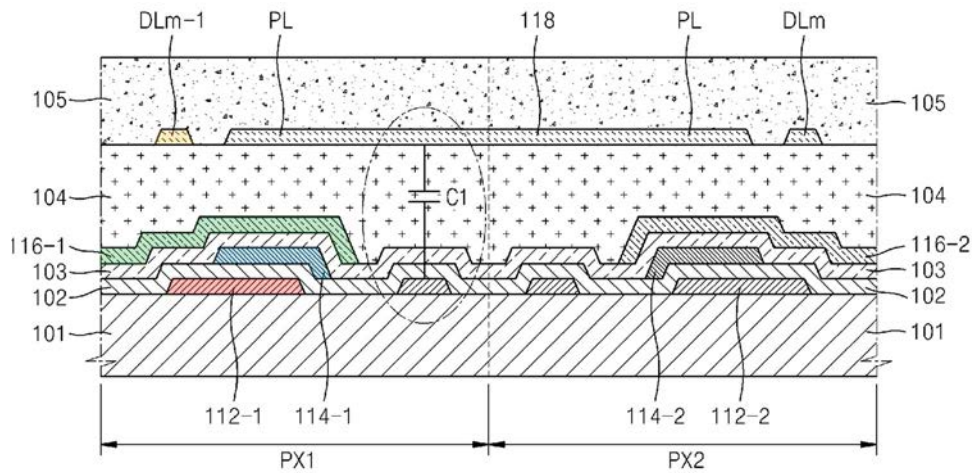


Fig. 9

73. The positioning of first capacitor electrode 114-1 is also shown in Fig. 9 of Kim-584 (annotated above), which is a cross-sectional view of Fig. 8 along the cut line A-A that passes through transistor T1. *Id.*, ¶60. As illustrated in Fig. 9, first capacitor electrode 114-1 (gate of T1) (shown in blue) overlaps first active layer 112-1 (shown in red).

74. The position of the first capacitor electrode in the first electrode layer is also shown in plan-view diagram of Kim-584's Fig. 6 (annotated below), where gate G1 of TFT T1 is formed by first capacitor electrode 114-1 (blue) and overlaps a portion of active layer A1 (red) of TFT T1, which includes the channel area of TFT T1. Kim-584, ¶67, Fig. 6.

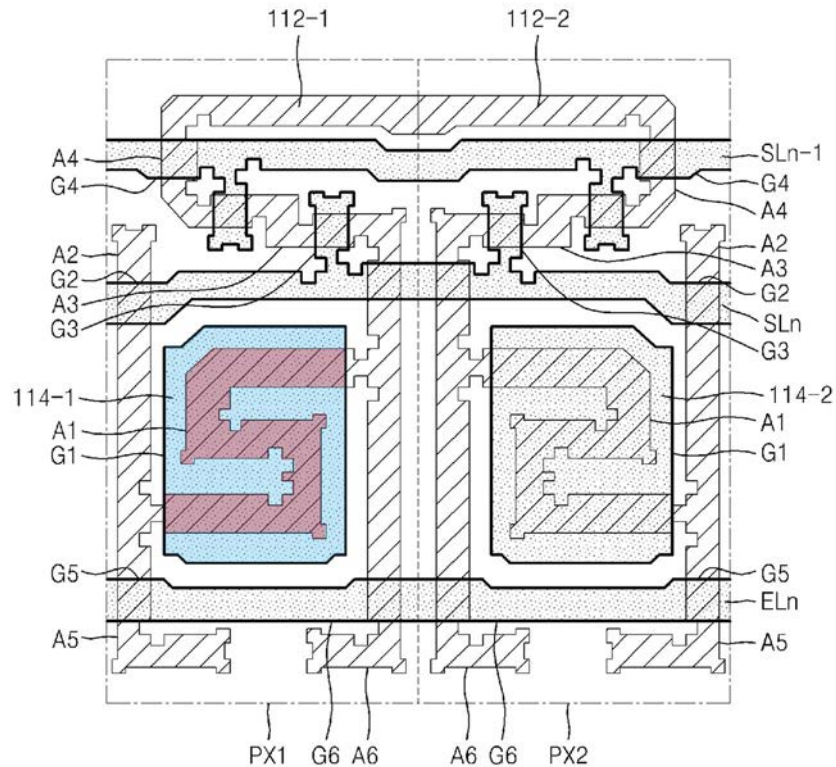


Fig. 6

75. Accordingly, limitation 1[b] is disclosed by Kim-584.

d. 1[c]: “a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;”

76. In my opinion, Kim-584 teaches or suggests limitation 1[c].

77. Kim-584 teaches “a second electrode layer” over the first electrode layer as the layer that includes second capacitor electrode 116-1. Kim-584 explains, “The **second capacitor electrodes 116-1 and 116-2 overlap with the first capacitor electrodes 114-1 and 114-2** to form the storage capacitor Cst.” Kim-584, ¶70.

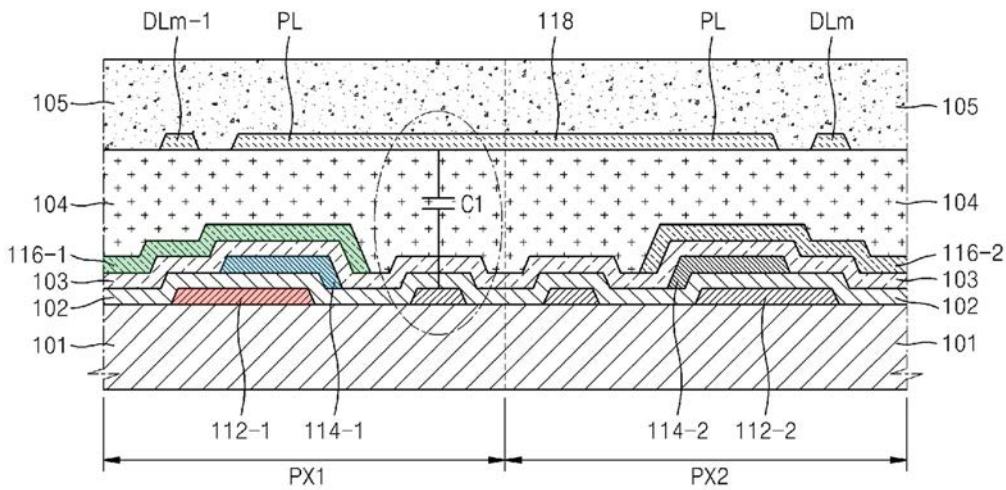


Fig. 9

78. Fig. 9 (shown above) and Fig. 8 (shown below) illustrate a part of second capacitor electrode 116-1 (annotated in green) (“a part of the second electrode layer”) overlaps first capacitor electrode 114-1 (annotated in blue), which is in “the first electrode layer”. *Id.*, Fig. 9.

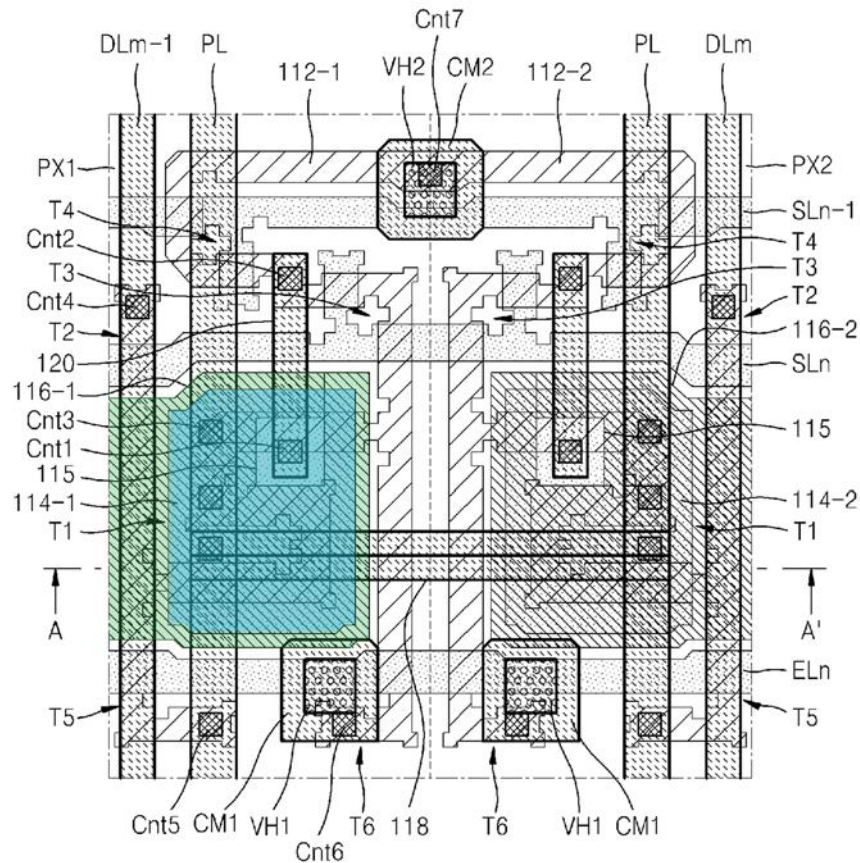


Fig. 8

79. Accordingly, limitation 1[c] is disclosed by Kim-584.

e. 1[d]: “a first signal line over the second electrode layer; and”

80. In my opinion, Kim-584 teaches or suggests limitation 1[d].

81. Kim-584 discloses “a first signal line” in the form of data signal line DLm-1 that is over second electrode layer 116-1, as shown in Fig. 9 (marked in orange and circled in red as annotated below).

82. Kim-584 explains, “A protective layer 105 is formed on the substrate 101 on which **data signal lines DLm-1** and DLm, driving voltage lines PL including

connection line 118, connection line 120, the first contact metals CM1, and the second contact metals CM2 are formed.” Kim-584, ¶78, Fig. 9. As Fig. 9 illustrates, Kim-584’s DLm-1 (“first signal line”) annotated in yellow is over second capacitor plate 116-1 (green), which is in the “second electrode layer.”

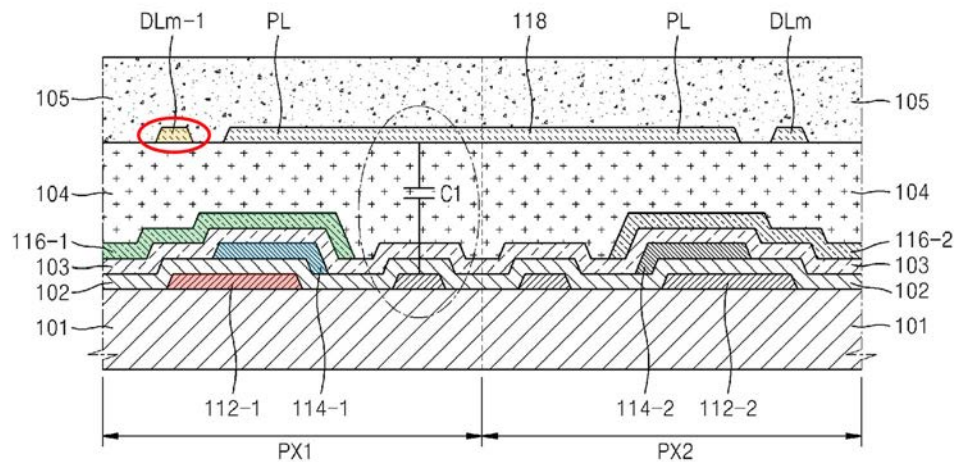


Fig. 9

83. Pixels in a display must be externally connected with signal lines to receive control and data signals in order to operate. The typical signals are scan (row-select) and data (column-data) signals, as shown in Figs. 1-3 of Kim-584 as SLn (or SLn-1) and DLm (or DLm-1), respectively. The location of the signal lines can be in any metal (electrode) layer but are often and conveniently located on the top metal layer, to simplify connection to external controllers without using vias, which reduce performance and yields.

84. Accordingly, limitation 1[d] is disclosed by Kim-584.

- f. **1[e]: “a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.”**

85. In my opinion, Kim-584 teaches or suggests limitation 1[e].

86. Kim-584 teaches or suggests “a first shield layer” in the form of second capacitor electrode 116-1, or a part thereof, which overlaps T1, and is situated in a layer between first signal line (DLm-1) and the first semiconductor (active layer 112-1 associated with T1). Kim-584, ¶¶69-70, Fig. 9. It has been very well known for decades that changing electrical current flow (e.g., accelerating electrons) in a first electrical conductor produces electro-magnetic radiation that can be absorbed by neighboring second electrical conductors (wires), thereby producing unwanted electrical activity in the second wires, which is referred to as electro-magnetic interference (EMI). As illustrated in annotated Fig. 9 above, second capacitor electrode 116-1 (marked in green) is in the second electrode layer positioned between data line DLm-1 and active layer 112-1 of transistor T1 and thus shields the active region of T1 from high frequency interference of the data lines. As I have previously discussed in §VI.D, well-known circuit layout techniques reduce this interference (EMI) by using shield wires or other electrically conductive structures (typically connected to a fixed voltage such as power or ground) that absorb the EMI,

reducing circuit electrical noise and improving circuit performance. Capacitor electrodes, typically having a relatively large spatial area, are ideal for this purpose.

87. In my opinion, it would have been obvious to a POSITA that second capacitor electrode 116-1 acts as a shield layer because it is positioned between the potential source of electromagnetic interference (i.e., DLm-1) and the semiconductor of TFT T1, and is connected to a constant voltage line, PL (also referred to as ELVDD). Kim-584, ¶¶35, 52, Fig. 3. I note that this interpretation of the capacitor plate as a shield layer is consistent with the '015 Patent, which explains that a capacitor plate can operate as and can be considered a shield layer: “the third shield layer SD3 *may be part of the second storage capacitor plate 127.*” '015 Patent, 13:47-48; *see also id.*, Fig. 10 (below), annotated to show top capacitor plate 127, bottom capacitor plate/gate 125a, showing a similar “shield layer” as Kim-584’s second capacitor electrode configuration shielding signal line 171 from 125a. *See also id.*, 9:57-62, explaining that a shield can be effectuated by existing circuit components. Furthermore, as previously discussed in §VI.D, using a capacitor plate as a shield layer was well known in 2014. *See generally* Saxena, Xie, and Kim-585.

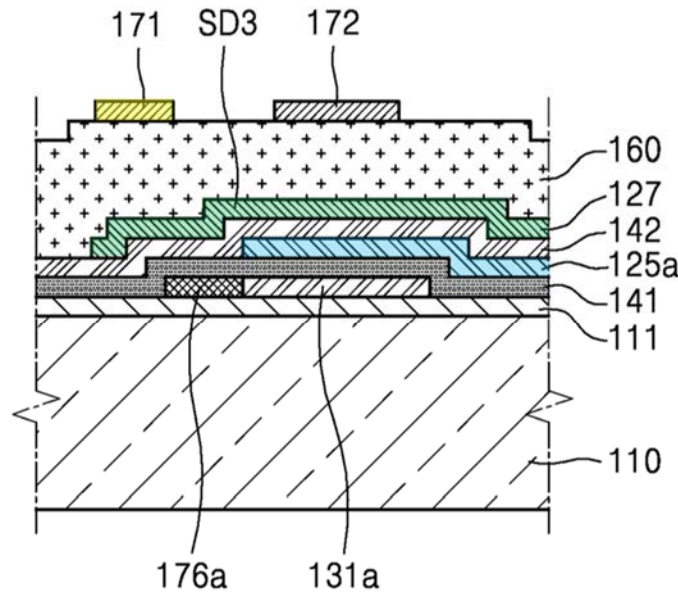


Fig. 10

88. Kim-584's second capacitor electrode 116-1 has a large enough area so that a portion of the second capacitor electrode overlaps "a part of one of the source area and the drain area of the first semiconductor." I have shown this in the annotated plan-view diagram of Fig. 7 (below), where only a portion of the overlapped source region is shown in purple. The annotated (purple) portions in Fig. 7 are sufficient to satisfy and render obvious the limitation in 1[e]. However, a larger position of the overlapped source region can also be used to satisfy limitations in 1[e]. I will discuss this further in Claim 8.

89. Ideally, the shield will overlap or be closely adjacent to any conductor that has fast-changing signals, such as gate electrodes controlling pixels, or transistor sources and drains whose current changes often in response to the gate electrodes,

as in Kim-584. From an electrical point of view, a larger shield is generally better, as would be understood by a POSITA.

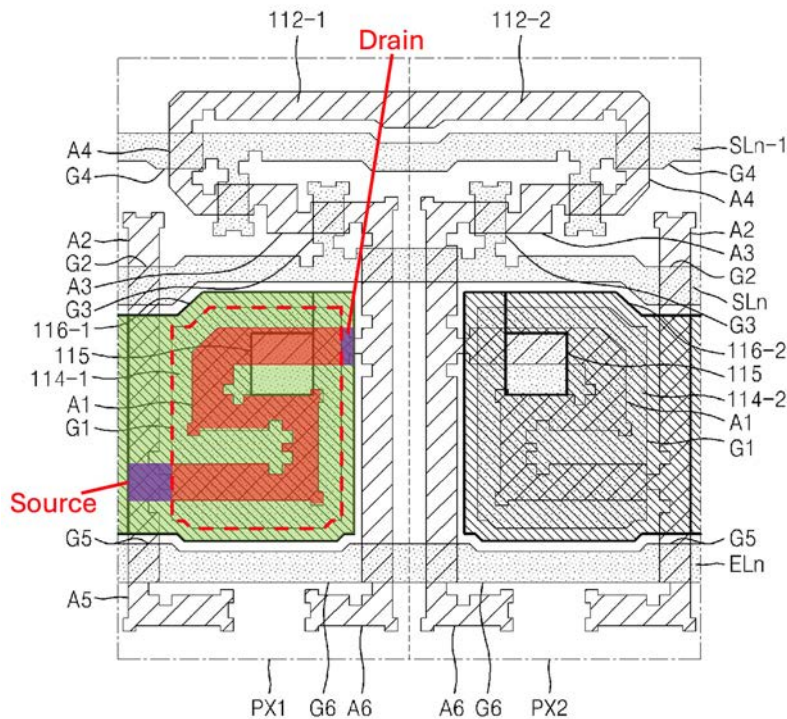


Fig. 7

90. In the annotated figure, the green area is the second capacitor electrode, and the dashed red rectangle is the bottom capacitor electrode (which is also gate electrode G1 of TFT T1). In my opinion, a POSITA would have understood and found it obvious that the section of the active layer under gate electrode G1 corresponds to the channel region of T1, and the active layer areas (annotated in purple) that are not under gate electrode G1 correspond to a part of the source area and drain area T1. *Id.*; see also Kim-584, ¶63: “[a]n active layer of each TFT includes a channel area which is not doped with impurities, and **source and drain**

areas which are formed by doping **both sides of the channel area** with impurities.”

A shield that also covers the source and drains of an electrode would be a natural and preferred design option as it will further reduce EMI. A large gate/channel enables greater current flow control.

91. It is my opinion that the designation of “source” and “drain” in Fig. 7 of Kim-584 would have been readily understood by a POSITA based on the transistor connectivity shown in Fig. 3 and labels A3 and A5 in Fig. 7 of Kim-584. In particular, I note that Kim-584 explains that the source of T1 is connected to drain of T5, and the drain of T1 is connected to drain of T3 (see Kim-584, FIG. 3), and Fig. 7 includes labels A3 and A5 as portions along the active layer 112-1 that forms two adjacent TFTs to T1. *Id.*, ¶63, Fig. 7, *see also* Fig. 5. The design, connectivity, and layout of TFTs in a given circuit are a well-known task for conventional circuit designs, as I have previously discussed in §VI.C.

92. Accordingly, limitation 1[e] is disclosed by Kim-584.

3. Claim 2: "... wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line."

93. In my opinion, Kim-584 teaches or suggests Claim 2.

94. As discussed above with respect to limitation 1[e], Kim-584 discloses “the first shield layer” as second capacitor electrode 116-1, or a part thereof. The second capacitor electrode is part of a “second electrode layer” that also includes

gate lines formed on top of insulating layer 103: “[s]econd gate lines are formed on the second gate insulating layer 103. The second gate lines include second capacitor electrodes 116-1 and 116-2.” Kim-584, ¶69, Fig. 9. Locating a shield in a common layer with other electrical structures would be a natural design choice well understood by a POSITA to optimize those circuit layout attributes, and given that the shield layer is part of an existing capacitor electrode.

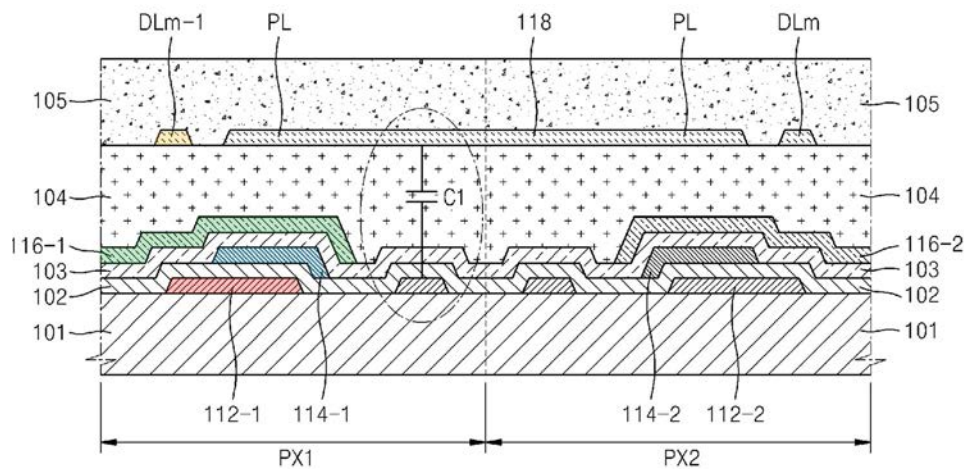


Fig. 9

95. Second capacitor electrode 116-1 (marked in green) overlaps a part of data signal line DLm-1 (“the first signal line” marked in yellow), as shown in the annotated plan-view diagram of Kim-584’s Fig. 8 (below).

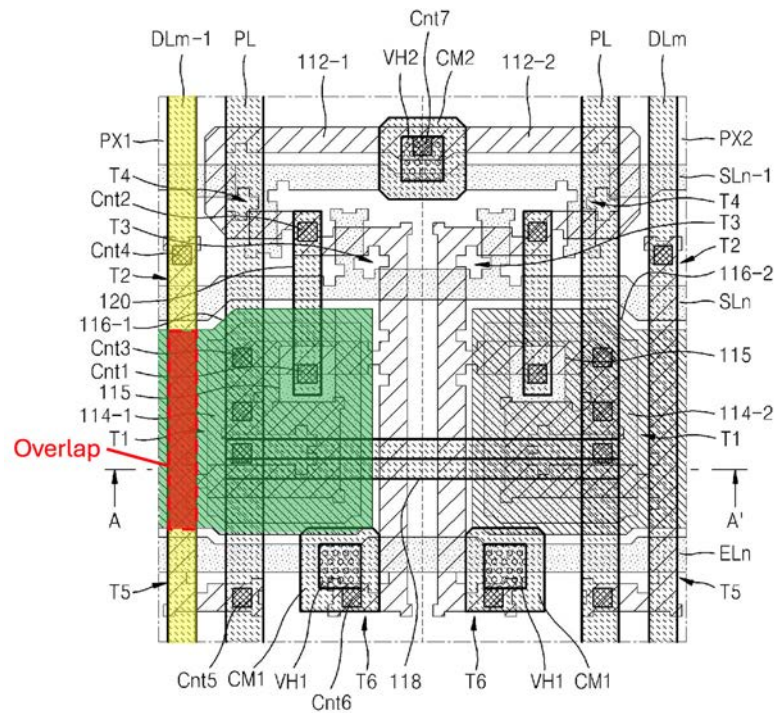


Fig. 8

96. In my opinion, the interpretation of a component (second capacitor plate) in a lower layer “overlapping” part of another component (part of the first signal line) in a higher layer is consistent with the ’015 Patent, which does not limit “overlapping” to mean “above” and treats these concepts separately. For example, Kim-584 explains: “the second storage capacitor plate overlapping the first storage capacitor plate and being above the first storage capacitor plate,” indicating that “overlapping” does not necessarily include “being above.” ’015 Pat., 1:54-56. Additionally, similar to the above description of Kim-584, the ’015 Patent illustrates various shield layers (SD1, SD2, SD3) that are positioned below the signal line 171. This is shown in Fig. 10, partially reproduced and annotated below, where data line

171 is in a layer above the shield layer SD3, but the '015 Patent characterizes this as a shield layer overlapping the signal line. *Id.*, 17:27-29, Figs. 5-7, 10, 12.

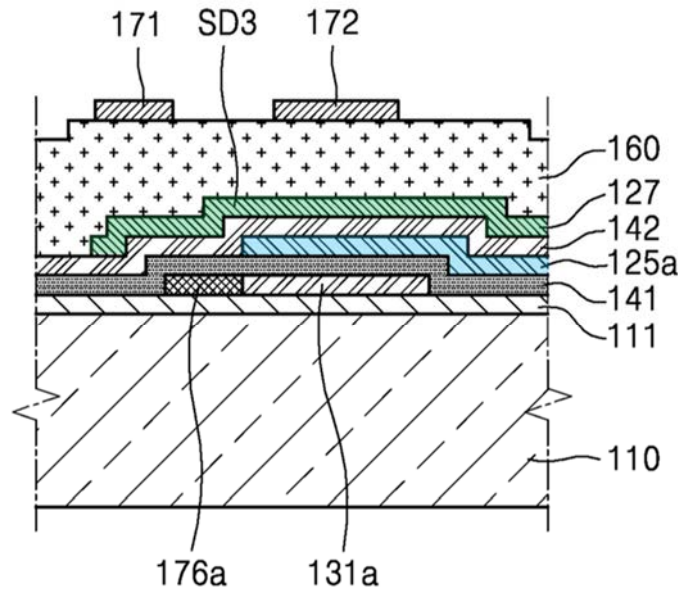


Fig. 10

97. Moreover, it is my opinion that a POSITA would readily understand that overlapping refers to plan view, without regard to the specific vertical ordering of elements. ‘Over’ and ‘under’ are typically arbitrary and relative designations with respect to a structure such as a TFT circuit on a substrate. Conventionally, but arbitrarily, the substrate is located at the bottom of a circuit cross section so other layers are ‘above’ the substrate, but the structure can be flipped over and the relative terms exchanged. Moreover, the term ‘overlap’ does not necessarily imply a specific location over or under, or above or below a first structure with respect to a second

structure but simply means that an orthogonal projection from the substrate through the first structure will intersect with the overlapping second structure.

98. Accordingly, Claim 2 is disclosed by Kim-584.

4. **Claim 3: "... further comprising a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first signal line."**

99. In my opinion, Kim-584 teaches or suggests Claim 3.

100. Kim-584 discloses a second TFT as thin-film transistor T2. Fig. 3 of Kim-584, which has been annotated below, shows transistor T2 is connected at one end (source) to the first signal line (DLm-1) (green line), and the other end (drain of T2) is connected to the first transistor T1 (i.e., to source of T1) (red line). Kim-584, Fig. 3, *see also id.*, Fig. 2 and ¶47 describing circuit connectivity: "A source electrode S2 of the switching TFT T2 is connected to the data signal line DLm. A drain electrode D2 of the switching TFT T2 is connected to the source electrode S1 of the driving TFT T1."

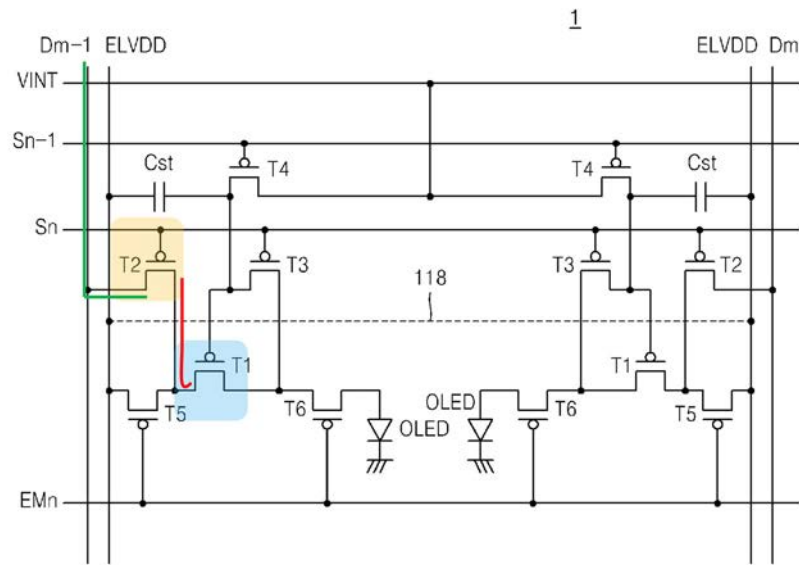


Fig. 3

101. As explained in limitation 1[a], Kim-584 discloses a semiconductor for each transistor as part of active layer 112-1, including an active layer A2 (“second semiconductor”) for TFT T2 (“second thin-film transistor”): “TFTs of a pixel circuit are formed along the first and second active layers 112-1 and 112-2. **Active layers A1, A2, A3, A4, A5, and A6** of a driving TFT T1, **a switching TFT T2**, a compensation TFT T3, an initialization TFT T4, a first emission control TFT T5, and a second emission control TFT T6 are formed on each of the first and second active layers 112-1 and 112-2.” Kim-584, ¶63, Figs. 5 and 6 (annotated below). Active-matrix OLED drive circuits typically use a switching transistor (T2) to control access to a pixel and a drive transistor (T1) that directly controls current passing through the OLED. The active layers are semiconductor layers. Kim-584, ¶62.

102. Kim-584 does not precisely define the extent of active layer A2. However, it is my opinion that it would be obvious to a POSITA that active layer A2 extends to both sides of a channel region of TFT T2, and the location of the channel region is obvious from the location of gate electrode G2. This is because an active layer must extend to the extent of the overlapping gate and connect to the drain and source regions to function as intended.

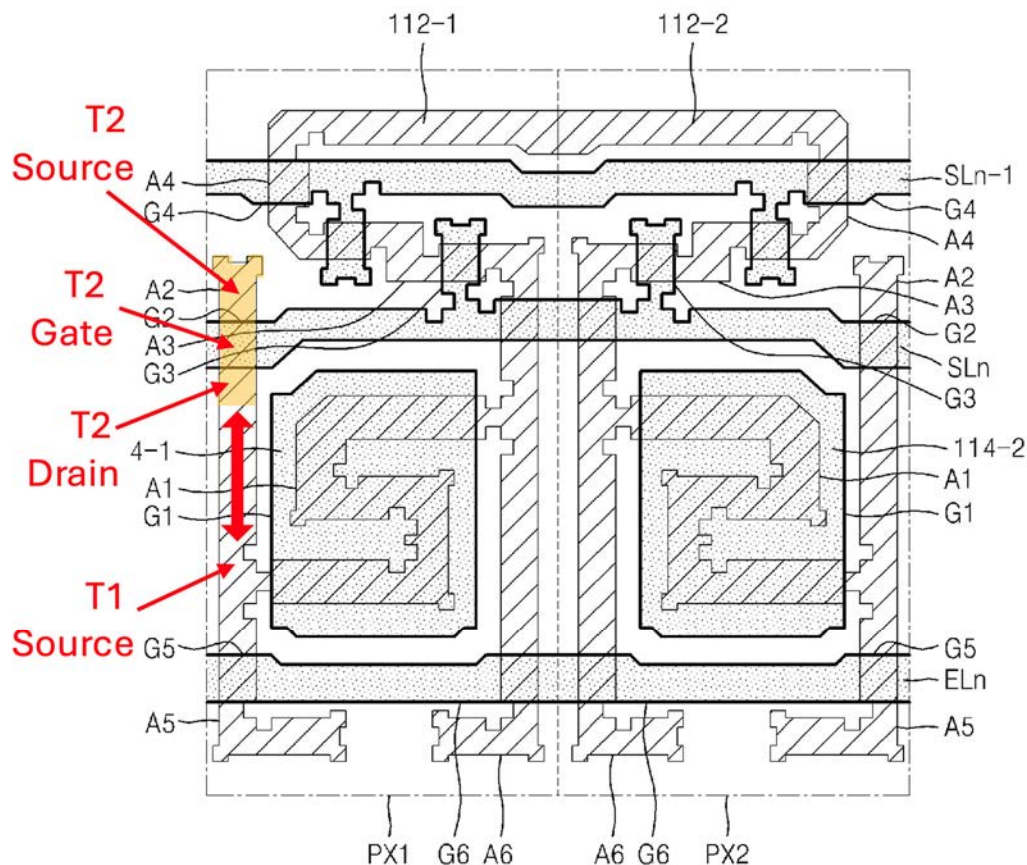


Fig. 6

103. The connectivity of T2's semiconductor ends are also evident from Fig. 6 (annotated above), showing “one end of second semiconductor” (T2's drain)

connected to “one end first semiconductor” (T1’s source); Fig. 8 (annotated below) shows connection of “other end of second semiconductor” (T2’s source) to DLm-1 (“first signal line”) through connection hole Cnt4. Kim-584, ¶74: “data signal lines DLm-1...[is] connected to the switching TFTs T2 through the fourth contact holes Cnt4.”

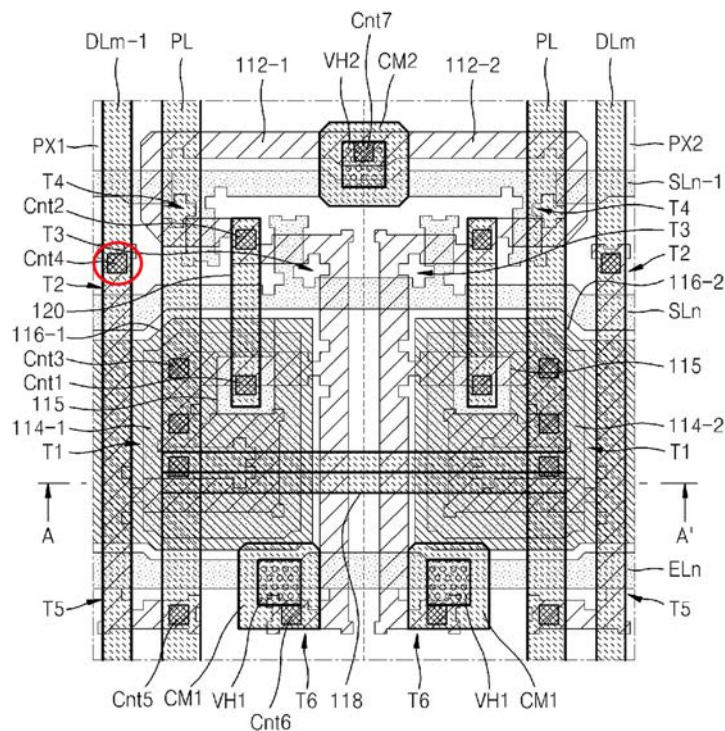


Fig. 8

104. Accordingly, Claim 3 is disclosed by Kim-584.

5. **Claim 4: "... further comprising a first voltage line in the same layer as the first signal line and connected to the second electrode layer."**

105. In my opinion, Kim-584 teaches or suggests Claim 4.

106. Kim-584 discloses “a first voltage line” as voltage line PL that is in the same layer as data signal line DLm-1 (“the first signal line”) and is connected to second capacitor electrode 116-1 in “the second electrode layer.” Kim-584 uses the notation ELVDD to indicate the power supply voltage that is provided to power line PL: “[t]he driving voltage line PL transmits a first power supply voltage ELVDD.” Kim-523 ¶45; *see also id.*, ¶35. Therefore, in my opinion, the terms PL and ELVDD are used interchangeably.

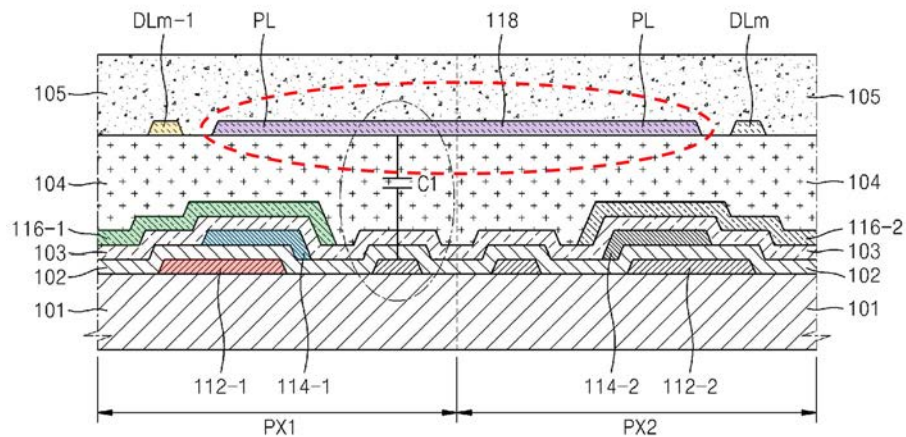


Fig. 9

107. Fig. 9 of Kim-584 (annotated above) shows voltage line PL (“a first voltage line,” shown in purple in the red-dashed ellipse) that is in the same layer as data signal line DLm-1 (“the first signal line,” shown in orange). This is also explicitly described in Kim-584: “[t]he **data signal lines DLm-1 and DLm, the driving voltage lines PL** including the connection line 118, the connection line 120,

the first contact metals CM1, and the second contact metals CM2 **may be formed of the same material on the same layer.**” Kim-584, ¶77.

108. Additionally, Fig. 3 of Kim shows a voltage line, labeled PL or ELVDD (Kim-523 ¶45), connected to second capacitor electrode Cst2, corresponding to second capacitor electrode 116-1, annotated in Fig. 3 below with a red line. *Id.*; Fig. 2; *see also id.*, ¶52: “A second electrode Cst2 of the storage capacitor Cst is connected to the driving voltage line PL.” *See also id.*, ¶¶72, 75, describing connections of PL to the second capacitor electrode. Fig. 3 shows first power supply voltage ELVDD, which is transmitted via driving voltage line PL. Kim-584 states that “[t]he driving voltage line PL transmits a first power supply voltage ELVDD.” Kim-523 ¶45; *see also id.*, ¶35.

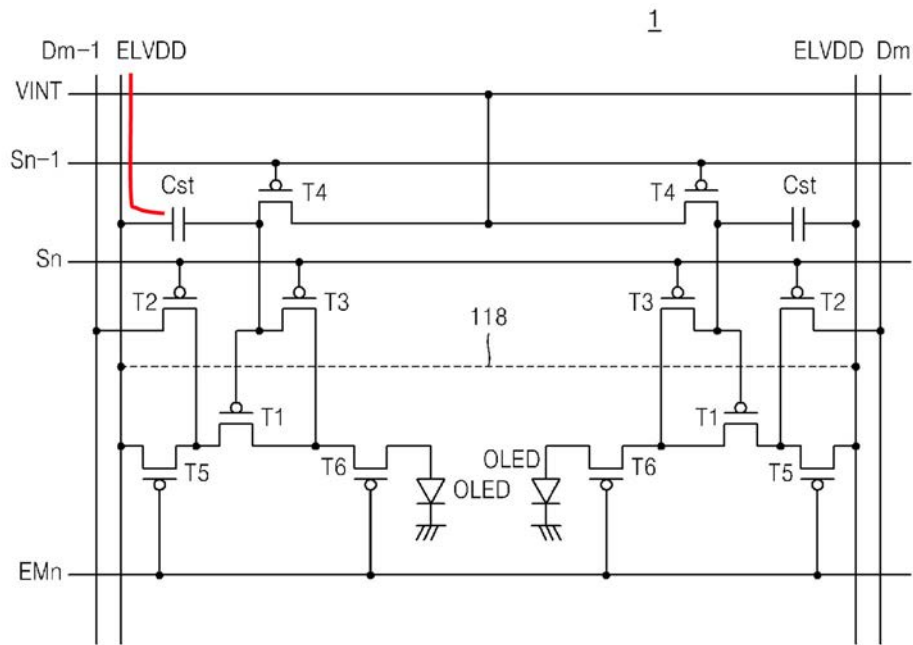


Fig. 3

109. Kim-584 further discloses that “[t]he driving voltage lines PL are connected to the second capacitor electrodes 116-1 and 116-2 through the third contact holes Cnt3.” *Id.*, ¶¶72, 75, describing connections of PL to the second capacitor electrode. Here, I note that power lines (PL) are needed to supply power to a circuit and, in a multi-metal-level structure, require vias to contact appropriate wires and/or signals. Such structures are well-known in the integrated circuit (IC) and TFT art.

110. Accordingly, Claim 4 is disclosed by Kim-584.

6. Claim 8

a. 8[pre] “... wherein the first signal line extends in a first direction, and”

111. In my opinion, Kim-584 teaches or suggests limitation 8[pre].

112. As shown in Fig. 8, annotated below, data line DLm-1 (“first signal line” shown highlighted in yellow) extends in a first direction (indicated with a red arrow). The green highlighted area shows capacitor electrode (or shield) 116-1. For simplicity, Fig. 7 is used for further analysis.

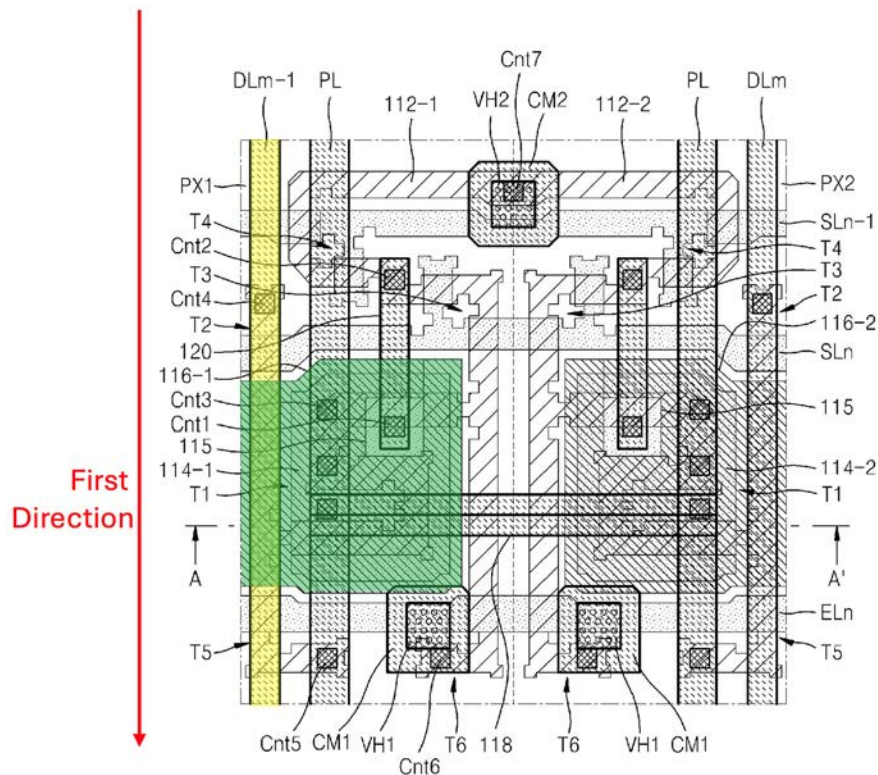


Fig. 8

- b. 8[a]: “wherein a length along the first direction of the overlapping part of the first shield layer with the part of one of the source area and the drain area of the first semiconductor is larger than a length of the first electrode layer along the first direction.”**

113. In my opinion, Kim-584 teaches or suggests limitation 8[a].

114. As shown in annotated partial Fig. 7 below, second capacitor electrode 116-1 (“first shield layer” – green) overlaps the source area of TFT T1 (purple portion on left side of figure) along a length L_A , and second storage capacitor overlaps the drain area of TFT T1 (purple portion on right side of figure) along length L_C . As I mentioned earlier, annotated Fig. 7 in limitation 1[e] only showed a smaller portion of the overlapped source area of T1 (purple annotation), which met the requirements of that element. However, the interpretation of an extended overlapped source area also satisfies the limitation in 1[e], because it also represents “a” part of the source of the first semiconductor (i.e., a part of source area of T1).

115. As also shown in partial annotated Fig. 7, L_A is larger than L_B , which is the length of one side of first capacitor electrode 114-1 (“a length of the first electrode layer” – blue) along the first direction. In the discussion of Ground 1A, Claim 1, limitation 1[b], I have explained that Kim-584 discloses “a first electrode layer” as the electrode layer that includes first capacitor electrode 114-1, and thus, “a length of the first electrode layer” corresponds to the length of one side of first

capacitor electrode 114-1, L_B that is shorter than L_A , as shown in partial annotated Fig. 7.

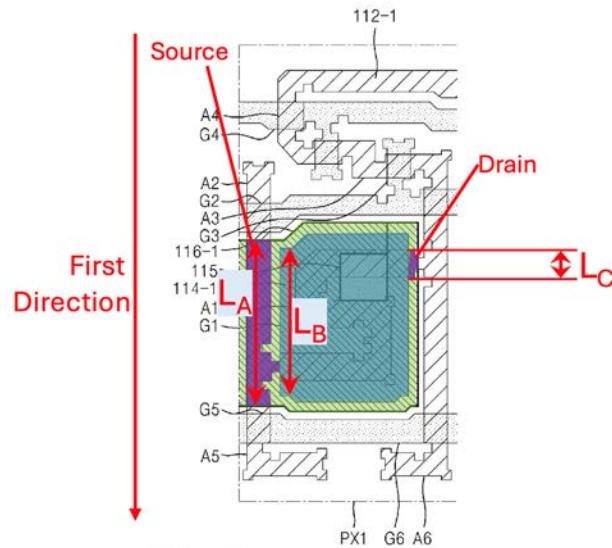
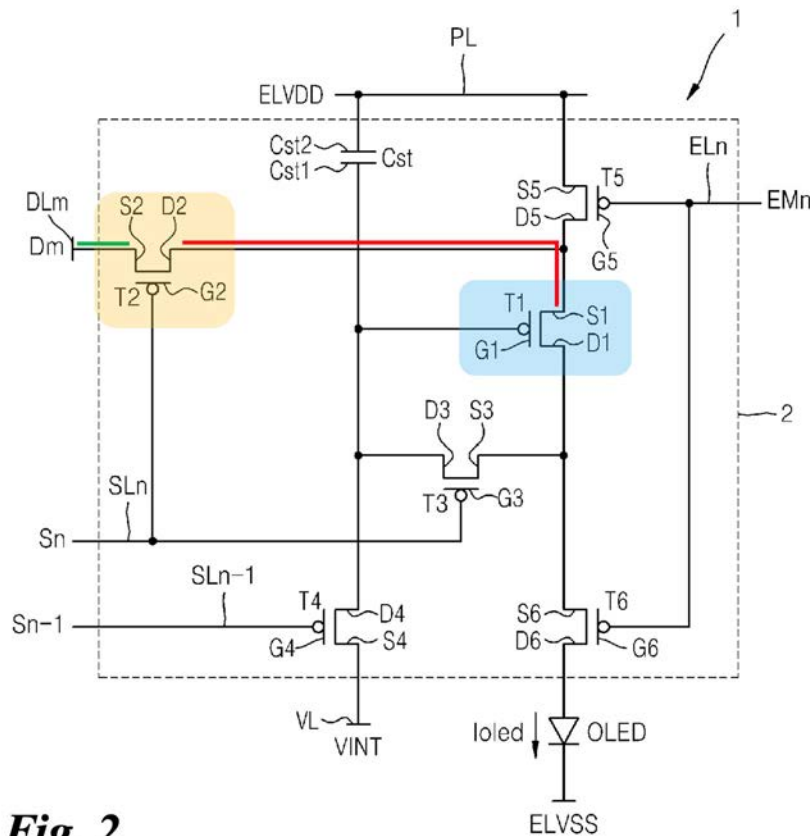


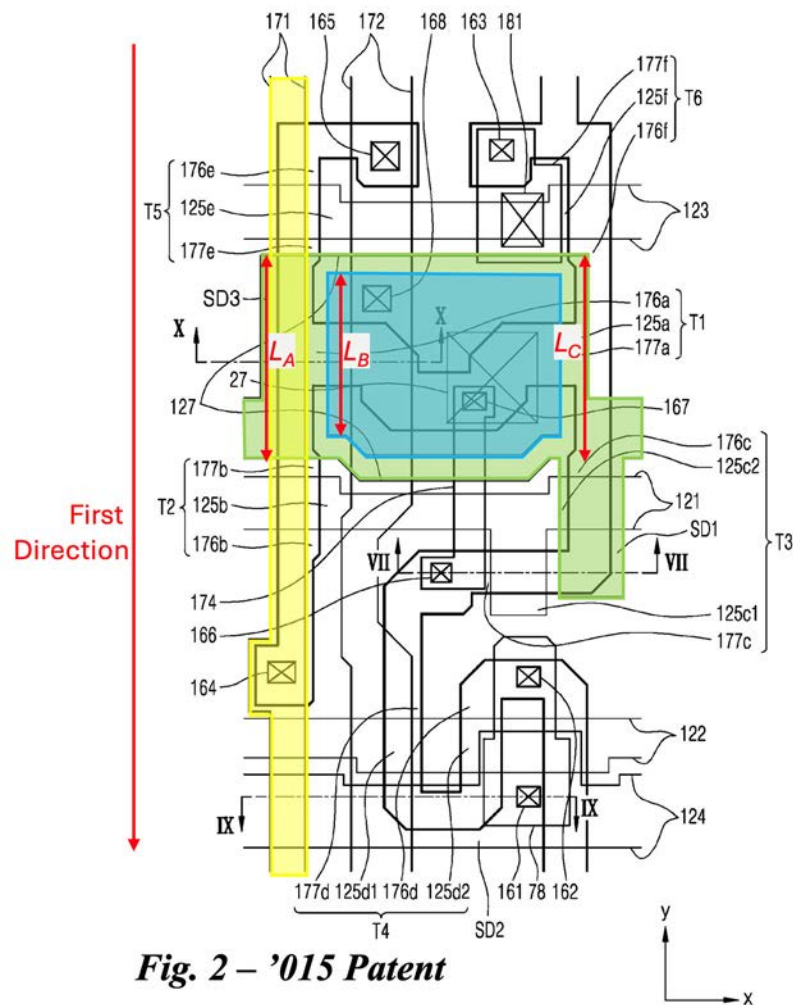
Fig. 7

116. In my opinion, it would have been obvious to a POSITA that the source and drain areas comprise doped semiconductor regions (i.e., regions other than channel regions) that extend along the first direction. I note that the source area of T1 has a length, L_A , that extends to and merges with the semiconductor regions associated with drain of T2 (D2) and drain of T5 (D5). Accordingly, a POSITA would have readily recognized this because of direct connections between S1, D2 and D5 shown in Kim-584's Figs. 7 and 8 (above) and Fig. 2 (annotated below), which indicate the associated doped semiconductor regions would be at the same voltage level, and thus would be considered a source area of T1.



117. Kim-584 explains, “An active layer of each TFT includes a channel area which is not doped with impurities, and source and drain areas which are formed by doping both sides of the channel area with impurities. Kim-584, ¶63. Accordingly, it is my opinion that the areas of the semiconductor outside of the undoped channel region associated with S1, D2 and D5 all have the same material and the same doping in order to maintain the same voltage. I note here that connected sources and drains of TFTs can be similarly doped and are not necessarily distinguished as they are one conductive structure (line). The relative sizes and extents of the elements are a matter of design choice subject to the priorities of the layout design.

118. Such an interpretation is not only consistent with the '015 Patent, but support for Claim 8 can only be found in the '015 Patent by adopting such an interpretation. Fig. 2 of the '015 Patent is annotated below. '015 Pat., Fig. 2. In order for the length of the overlapping part of the shield layer (SD3) with the source area (176a) and drain area (177a) (L_A) to be greater than the length of the first electrode layer (125a) along the first direction (L_B), the same interpretation of an extended source region of T1 must be adopted.



119. Accordingly, limitation 8[a] is disclosed by Kim-584.

7. Claim 9: "... wherein the first shield layer fully overlaps the part of one of the source area and the drain area of the first semiconductor."

120. In my opinion, Kim-584 teaches or suggests Claim 9.

121. As a preliminary matter, I note that the limitation of "[t]he part of one of the source area and the drain area of the first semiconductor" finds antecedent basis in Claim 1. This is shown with purple annotations in Fig. 7 below.

122. As I have explained in 1[e], Kim-584 discloses second capacitor electrode 116-1 ("the first shield layer") overlaps a part of one of the source area and the drain area of the first semiconductor. *See* Section IV(A)(1)(f), *supra*.

123. As shown in Fig. 7, annotated below, the overlap of second capacitor electrode 116-1 (highlighted in green) over the part of the source and drain of the first semiconductor (over the purple area) does not include gaps or holes over the claimed area. Therefore, it is my opinion that the part of the source and drain of the first semiconductor is/are fully covered by second capacitor electrode 116-1. Kim-584, Fig. 7. Furthermore, it is preferable that the shield structure (116-1) cover as large an area of signals as possible to reduce EMI. Here, I note that a natural choice is to cover as much as possible of the gates, sources, and drains of the TFT.

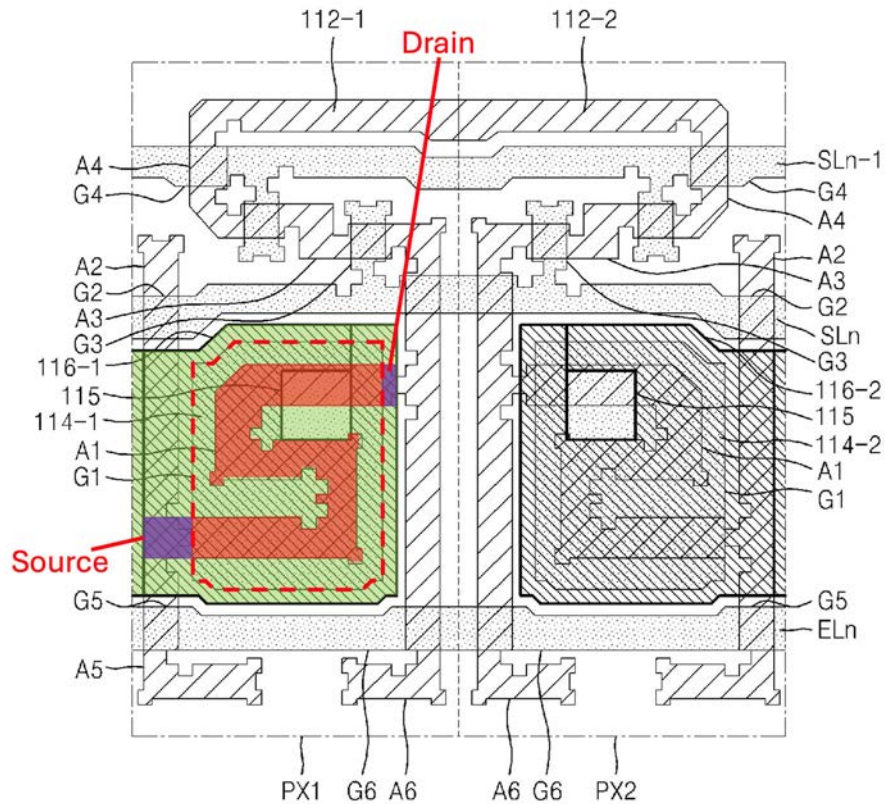


Fig. 7

124. Accordingly, Claim 9 is disclosed by Kim-584.

8. Claim 10

- a. **10[a]: "The display apparatus of claim 1, wherein the first signal line extends in a first direction, and"**

125. In my opinion, Kim-584 teaches or suggests limitation 10[a].

126. As shown in annotated Fig. 8 below, data line DLm-1 (highlighted in yellow) extends along the first direction indicated by the red arrow.

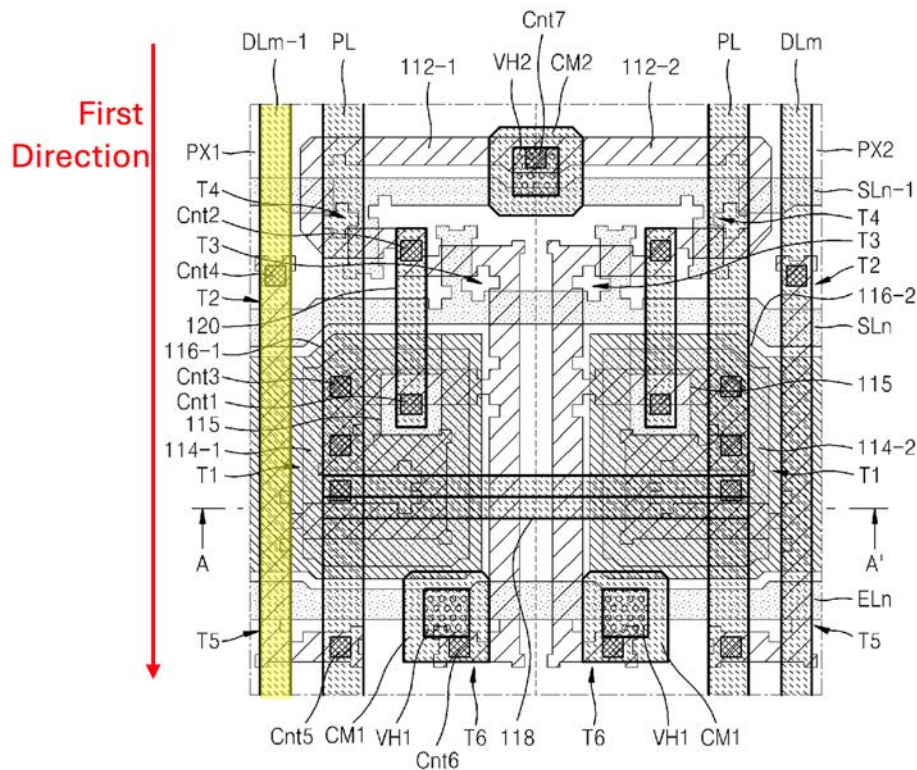


Fig. 8

127. Accordingly, limitation 10[a] is disclosed by Kim-584.

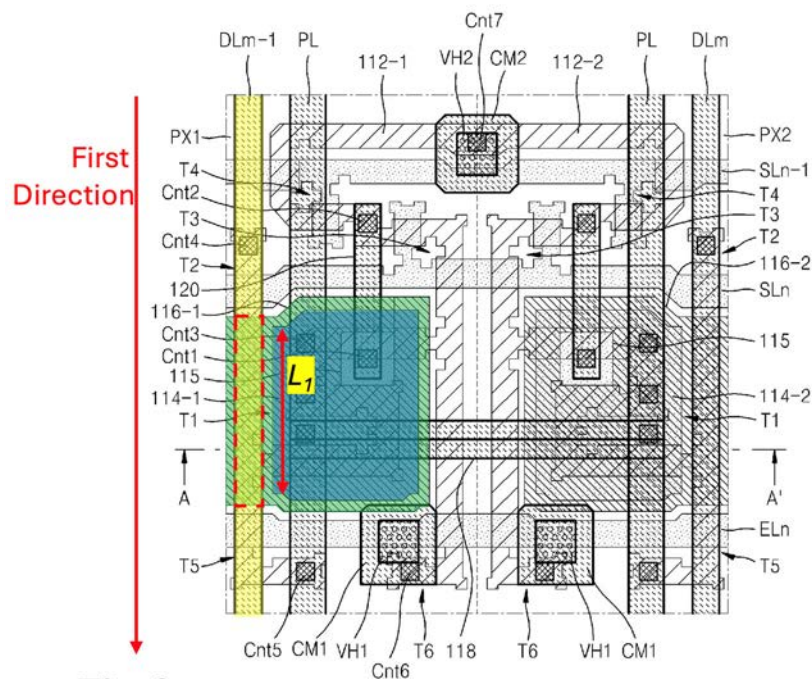
- b. 10[b]: "wherein a length along the first direction of an [[the]] overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction."**

128. In my opinion, Kim-584 teaches or suggests limitation 10[b].

129. As a preliminary matter, I note that in Claim 10, "the overlapping part" lacks proper antecedent basis, and is assumed to recite "an overlapping part."

130. I have annotated Fig. 8 below to illustrate an overlapping part (red box) of second capacitor electrode 116-1 ("the first shield layer") with data signal line DLm-1 ("the first signal line"). I have further annotated Fig. 8 to illustrate "a length

of the first electrode layer along the first direction” (shown with the red arrow and labeled L_1). Length, L_1 , corresponds to a length of the side of the first capacitor plate, which is part of the first electrode layer. See limitation 1[b]. I note that Claim 10 recites “a” length, and the length indicated by the red arrow labeled L_1 is “a” length of the first electrode layer that is shorter than the length of the overlapping part of the first shield layer with the first signal line (indicated by the dashed red box), thus meeting the claim limitation. Furthermore, ensuring that the shield overlaps more than the first electrode layer is a natural design feature that helps to mitigate EMI.



131. Accordingly, limitation 10[b] is disclosed by Kim-584.

9. Claim 20

- a. 20[a]: "The display apparatus of claim 3, further comprising a fifth thin-film transistor comprising a fifth semiconductor, one end of the fifth semiconductor being connected to the one end of the first semiconductor and the one end of the second semiconductor, and the other end of the fifth semiconductor being connected to a first voltage line,"

132. In my opinion, Kim-584 teaches or suggests limitation 20[a].

133. As a preliminary matter, I note that Claim 3 recites a "second" TFT and depends from Claim 1, which recites a "first" TFT. Herein, I am interpreting Claim 20's "fifth" TFT to be another TFT different from the first and the second TFTs recited in base claims 1 and 3.

134. Kim-584 discloses "a fifth thin-film transistor" as TFT T5, as shown in Fig. 3. Kim-584, Fig. 3. As discussed in limitation 1[a] and Claim 3, Kim-584 discloses a semiconductor for each of its transistors as part of active layer 112, which thus includes an active layer ("fifth semiconductor") for TFT T5 ("fifth thin film transistor"): "TFTs of a pixel circuit are formed along the first and second active layers 112-1 and 112-2. **Active layers** A1, A2, A3, A4, **A5**, and A6 of a driving TFT T1, a switching TFT T2, a compensation TFT T3, an initialization TFT T4, **a first emission control TFT T5**, and a second emission control TFT T6 are formed on each of first and second active layers 112-1 and 112-2." Kim-584, ¶63, Fig. 5. The active layers are semiconductor layers. Kim-584, ¶62.

135. Kim-584 also discloses that the drain of T5 (“one end of the fifth thin film transistor”) is connected to the source of T1: “[a] **drain electrode D5 of the first emission control TFT T5 is connected to the source electrode S1 of the driving TFT T1 and the drain electrode D2 of the switching TFT T2.**” Kim-584, ¶50; *see also* Fig. 3 (annotated below with the red line showing the connection between T5 and T1 and blue line showing the connection between T5 and T2). Kim-584 further explains that the source of T5 (“other end of the fifth semiconductor”) is connected to power line PL or ELVDD (“a first voltage line”). Kim-584; Fig. 3 (annotated below with green line). In particular, Kim-584 explains: “[a] **source electrode S5 of the first emission control TFT T5 is connected to the driving voltage line PL.**”² *Id.*, ¶50.

² As noted in connection with 1[e], PL and ELVDD both represent the same voltage line.

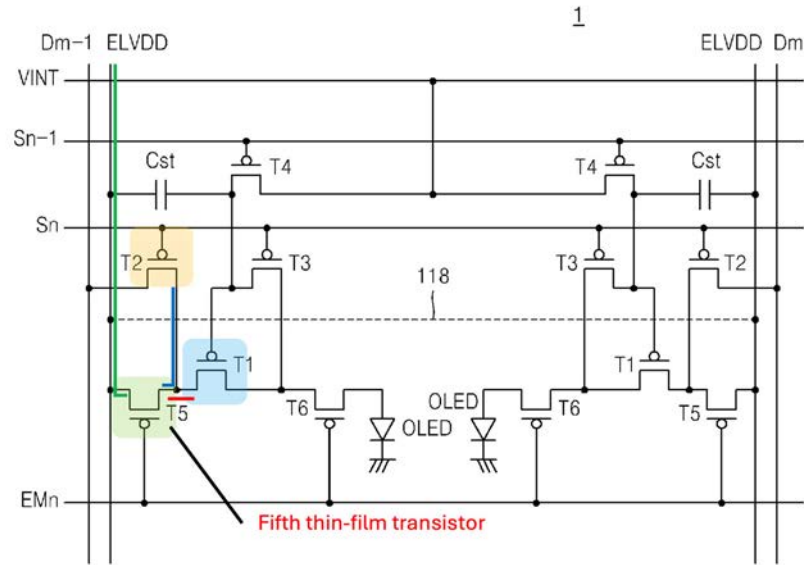


Fig. 3

136. The connectivity of T5's semiconductor ends are also evident from Fig. 6 (annotated below), showing T5's drain ("one end of the fifth semiconductor") is connected to T1's source ("one end of first semiconductor") and to T2's drain ("one end of the second semiconductor"), all being parts of the same contiguous semiconductor.

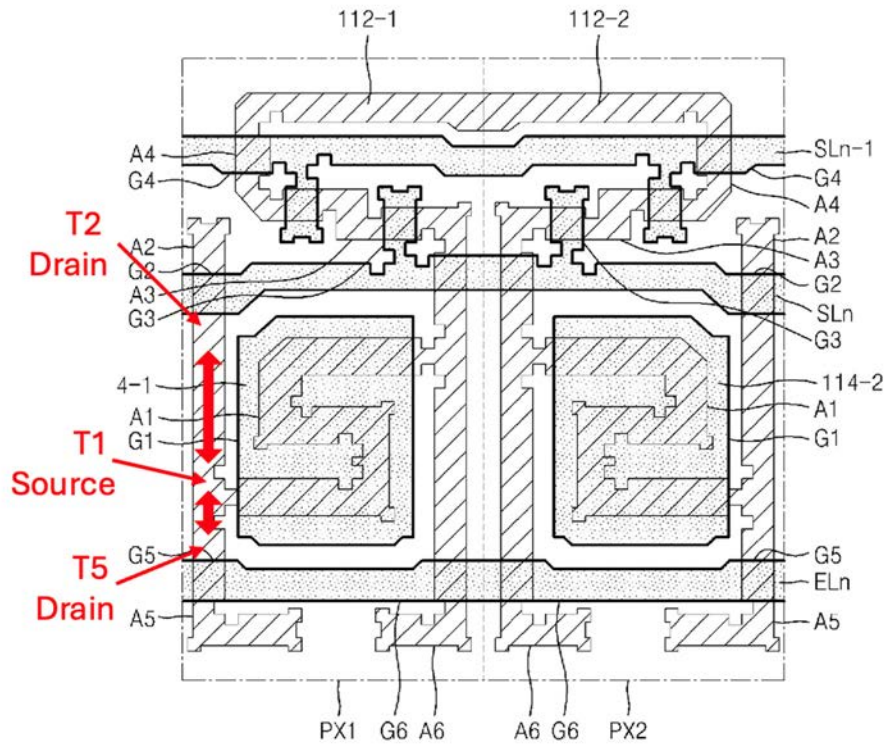


Fig. 6

137. Furthermore, annotated Fig. 8 (below) shows a connection from T5's source ("other end of the fifth semiconductor") to power line PL/ELVDD ("first voltage line") through contact hole cnt5. Kim-584, ¶72.

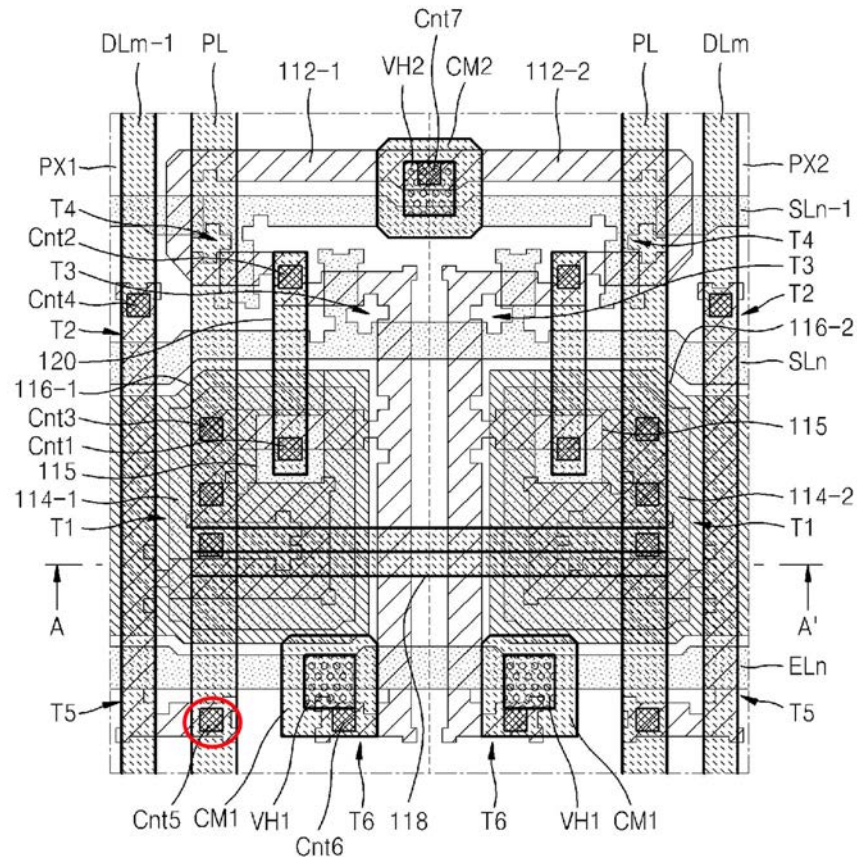


Fig. 8

138. In the context of limitation 20[a], I note that multi-TFT circuits for driving OLEDs are widely known. Therein, at least one of the TFTs must be connected to a signal line (e.g., S1) and another to a power line (e.g., ELVDD), else the circuit cannot function. Moreover, the transistor must be connected directly or through another circuit element. Such circuits are typical in the art.

139. Accordingly, limitation 20[a] is disclosed by Kim-584.

b. 20[b]: "wherein the first voltage line in the same layer as the first signal line and connected to the second electrode layer."

140. In my opinion, Kim-584 teaches or suggests limitation 20[b].

141. Annotated Fig. 9 (below) shows that voltage line PL ("first voltage line") is in the same layer as data signal line DLm-1 ("the first signal line"). This is also explicitly described in Kim-584: "[t]he data signal lines **DLm-1** and **DLm**, the driving voltage lines **PL** including the connection line 118, the connection line 120, the first contact metals **CM1**, and the second contact metals **CM2** may be formed of the same material on the same layer." Kim-584, ¶77.

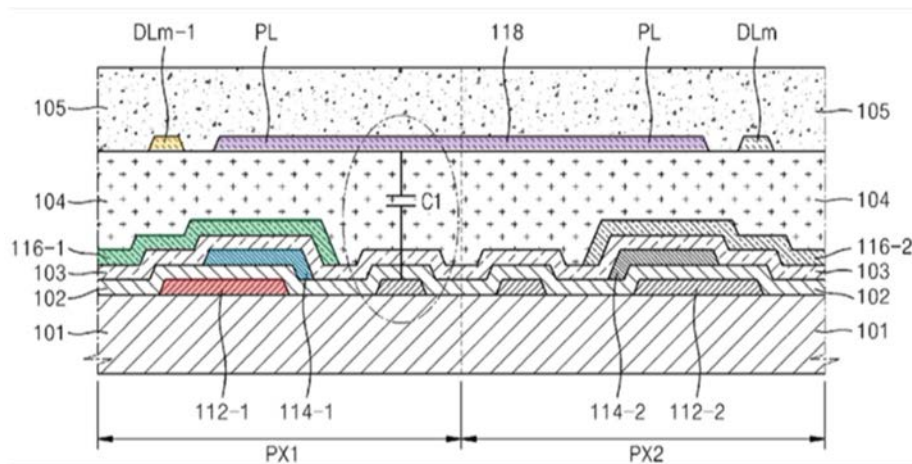


Fig. 9

142. Kim-584 describes that voltage line PL ("the first voltage line") is connected to second capacitor electrode 116-1, which is part of "the second electrode layer." Kim-584, ¶75: "The driving voltage lines **PL** are connected to the second capacitor electrodes **116-1** and **116-2** through the third contact holes **Cnt3**." Here,

I note that a POSITA will naturally place lines in a common layer where possible to reduce the number of layers necessary for a circuit, thereby saving costs. Furthermore, externally connected power and signal lines are typically on the top layer as that makes them easier to connect with a busbar connector (plug) and test.

143. Accordingly, limitation 20[b] is disclosed by Kim-584.

10. Claim 21

- a. 21[a]: “The display apparatus of claim 20, further comprising a fourth shield layer in a layer between the first signal line and the fifth semiconductor,”**

144. In my opinion, Kim-584 teaches or suggests limitation 21[a].

145. Kim-584 teaches a “fourth” shield layer in a layer between the first signal line and the fifth semiconductor. Specifically, the “fourth” shield layer is a portion of second capacitor electrode 116-1. The red rectangle outlined in annotated Fig. 8 below, or a portion thereof, is the fourth shield layer.

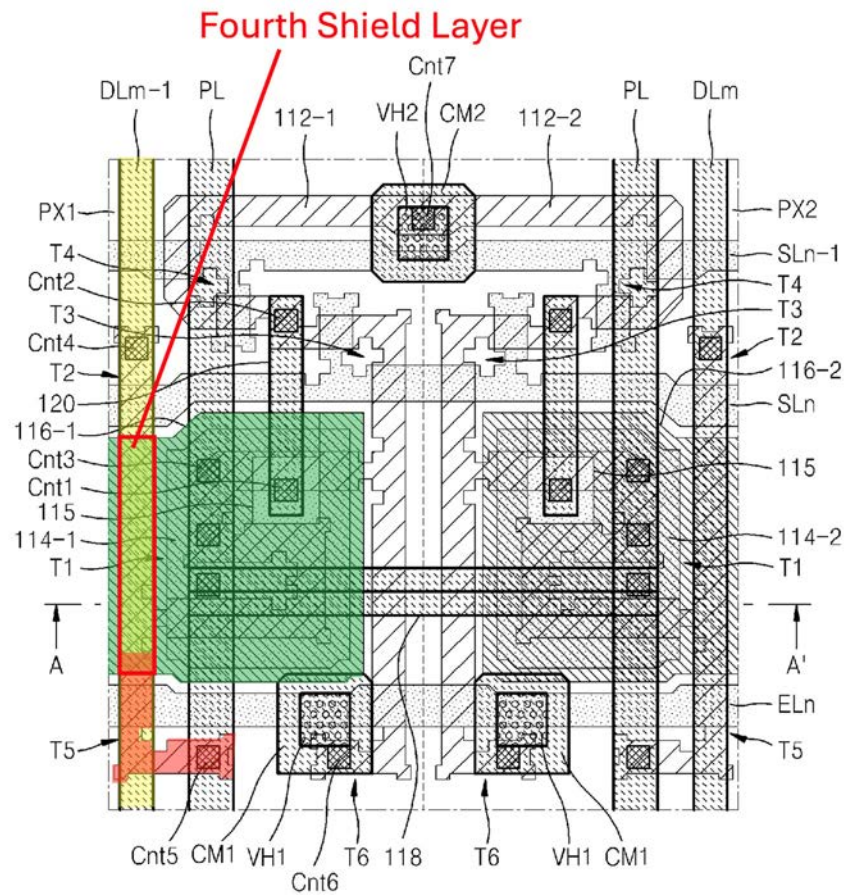
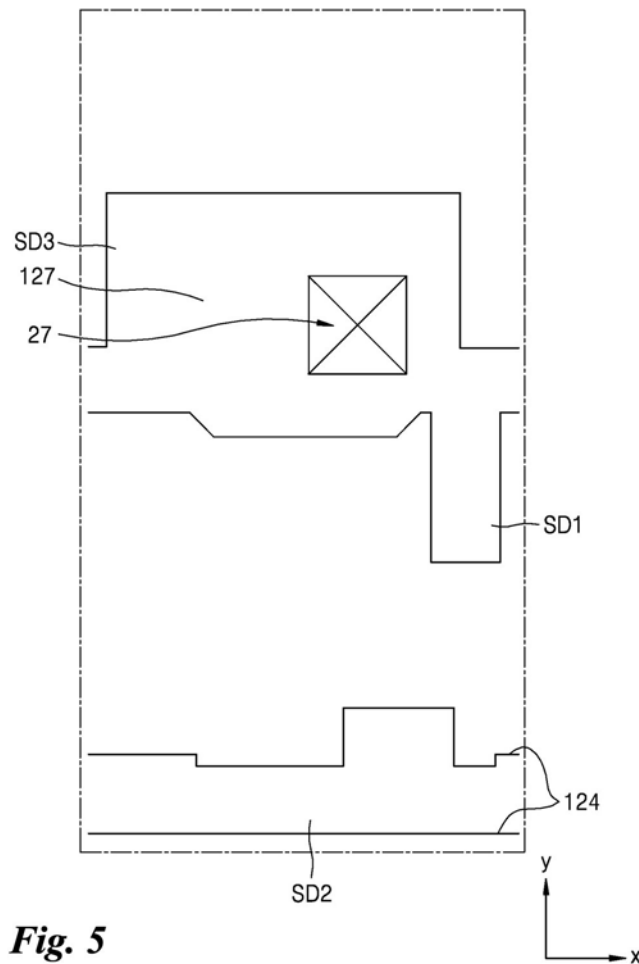


Fig. 8

146. In my opinion, the interpretation that the first and the fourth shield layer can be part of the same component is consistent with the '015 Patent, in which SD1 and SD3 are part of the same component, as shown below in '015 Patent's Fig. 5.



147. Annotated Fig. 9 (below) shows second capacitor electrode 116-1 (green), and therefore, its portion that forms the “fourth shield layer,” is in a layer between DLm-1 (“first signal line,” yellow) and semiconductor layer 112-1 (red). As explained in limitation 1[a] and Claim 3, Kim-584’s semiconductor layer 112-1 includes a portion that corresponds to each transistor, including TFT T5 (“fifth” TFT). Kim-584, ¶¶62, 63.

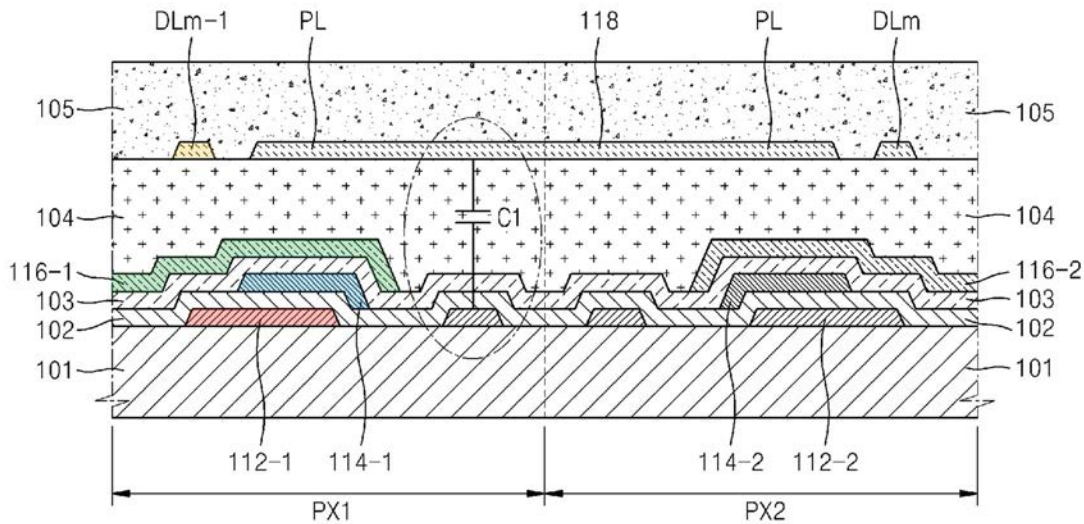


Fig. 9

148. Accordingly, limitation 21[a] is disclosed by Kim-584.

- b. 21[b]: “wherein the fourth shield layer overlaps a part of semiconductor between the channel area of the first semiconductor, the channel area of the second semiconductor, and the channel area of the fifth semiconductor.”**

149. In my opinion, Kim-584 teaches or suggests limitation 21[b].

150. Annotated and cropped Fig. 4 of Kim-584 (below left) shows a part of the semiconductor, which is between the channel area of T1 (“first” TFT), the channel area of T2 (“second” TFT), and the channel area of T5 (“fifth” TFT), that satisfies limitation 21[b]. The figure on the right shows that the part of the semiconductor is in between gate electrodes G1, G2, and G5 (indicated by the yellow outlines) of transistors T1, T2, and T5, respectively. Since the channel area of a

transistor is beneath its gate electrode, the part of the semiconductor is consequently in between the channel areas of T1, T2, and T5.

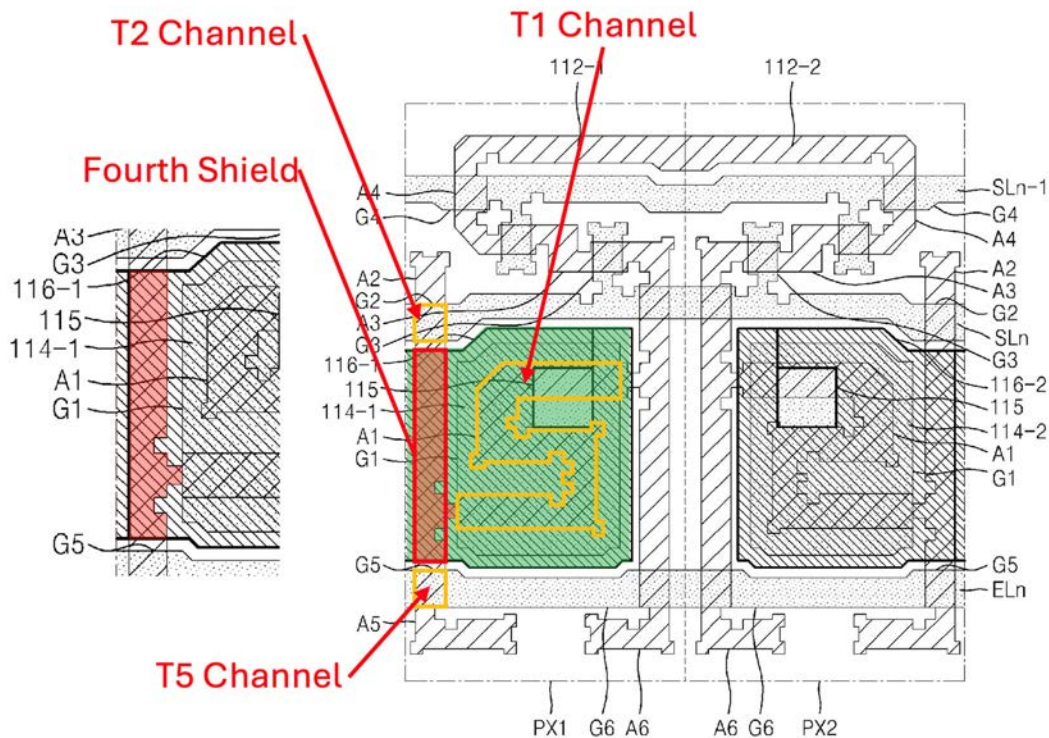


Fig. 7

151. As I have explained above in limitation 21[a], all or only a portion of the red rectangle can be construed as the “fourth” shield layer. The figure on the right shows the second capacitor electrode (highlighted in green) and the portion of the second capacitor electrode that is the fourth shield layer (indicated by the red outline), which overlaps that part of the semiconductor shown on the left of the figure below. Here, the claim recites “a” part of the semiconductor between the channel areas of the three TFTs can be construed to encompass a smaller portion of the active

layer than the full region annotated in red (on the left). Therefore, a smaller section of the red rectangle can also be interpreted to form the “fourth” shield layer, and it is not necessarily required for the full red rectangle to form to “fourth” shield layer.

152. Accordingly, limitation 21[b] is disclosed by Kim-584.

11. Claim 22: “The display apparatus of claim 21, wherein the fourth shield layer is a part of the second electrode layer.”

153. In my opinion, Kim-584 teaches or suggests Claim 22.

154. As I have explained above with respect to limitation 21[a], the fourth shield layer is part of second capacitor electrode 116-1, which is in the second electrode layer as described above with respect to Claim 2. Thus, the fourth shield layer is part of the second electrode layer.

155. Accordingly, Claim 22 is disclosed by Kim-584.

12. Claim 23

156. In my opinion, Kim-584 teaches or suggests Claim 23.

a. 23[a]: “The display apparatus of claim 22, further comprising a capacitor comprising a first capacitor plate and a second capacitor plate,”

157. See the discussions of Ground 1A, Claim 1, limitations 1[a] and 1[b] above, which describe a first capacitor electrode 114-1 and a second capacitor electrode 116-1. The electrodes have plate-like structures, as shown in annotated Fig. 8 below and Fig. 9 above.

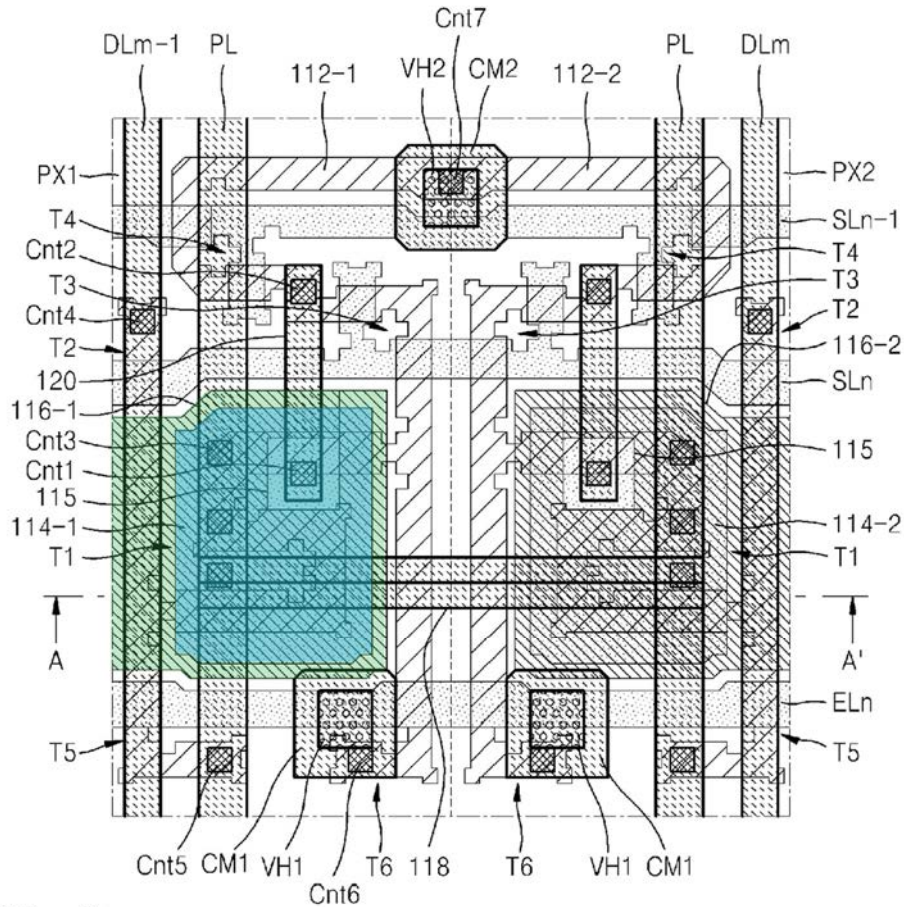


Fig. 8

158. Accordingly, limitation 23[a] is disclosed by Kim-584.

b. 23[b]: “wherein the first capacitor plate is a part of the first electrode layer, and the second capacitor plate is a part of the second electrode layer.”

159. See the discussions of Ground 1A, Claim 1, limitations 1[b] and 1[c] above, which discuss that the first capacitor plate is in the first electrode layer and the second capacitor plate is in the second electrode layer.

160. Accordingly, limitation 23[b] is disclosed by Kim-584.

13. Claim 33

161. In my opinion, Kim-584 teaches or suggests Claim 33. I have explained this below with reference to the discussions of claims 1, 2, and 10. In the context of Claims 1 and 33, I note that a shield layer is typically configured to be part of an existing layer, whenever possible, so as to reduce the number of metal layers in the design and should extend over as many signal lines as possible to reduce EMI given circuit design constraints.

a. 33[pre]: "A display apparatus comprising:"

162. See the discussion of Ground 1A, Claim 1, limitation 1[pre] above. Kim-584 relates to a display apparatus.

b. 33[a]: "a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;"

163. See the discussion of Ground 1A, Claim 1, limitation 1[a] above. Kim-584 includes a first thin-film transistor comprising a first semiconductor and having a source area, drain area, and channel area between the source area and the drain area.

c. 33[b]: "a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;"

164. See the discussion of Ground 1A, Claim 1, limitation 1[b] above.

- d. **33[c]: "a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;"**

165. See the discussion of Ground 1A, Claim 1, limitation 1[c] above.

- e. **33[d]: "a first signal line over the second electrode layer; and"**

166. See the discussion of Ground 1A, Claim 1, limitation 1[d] above.

- f. **33[e]: "a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor,"**

167. See the discussion of Ground 1A, Claim 1, limitation 1[e] above.

- g. **33[f]: "wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line,"**

168. See the discussion of Ground 1A, Claim 2 above.

- h. **33[g]: "wherein the first signal line extends in a first direction, and**

169. See the discussion of Ground 1A, Claim 10, limitation 10[a] above.

- i. **33[h]: "wherein a length along the first direction of the overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction."**

170. See the discussion of Ground 1A, Claim 10, limitation 10[b] above.

171. Accordingly, Claim 33 is disclosed by Kim-584.

B. Ground 1B: The combination of Kim-584 and Han renders Claims 5, 11-14, and 28-32 obvious.

1. Summary of Han

172. Han relates to OLED displays and specifically describes an OLED driving circuit that includes 6 transistors and 2 capacitors that are connected to voltage lines and data lines, as illustrated in Fig. 2. Han, ¶¶3, 38-41, Fig. 2. Han's invention aims to provide a pixel that can display an image having a desired luminance by minimizing or reducing a leakage current. *Id.*, ¶9. To this end, Han's driving circuit, in addition to the standard storage capacitor, C1, also includes a second capacitor, C2, as shown in Fig. 2 below, which can have the same (or similar) voltage as C1, thus maintaining the same voltage at nodes N1, N2 and N3, thereby minimizing or reducing the leakage currents. *Id.*, ¶¶48-49, 58, Fig. 2.

173. I further note that although Han's Fig. 2 shows three gate-connected TFTs at M3 and M4, it explains that the circuit can be implemented with two or more transistors in series. *Id.*, ¶¶44-45.

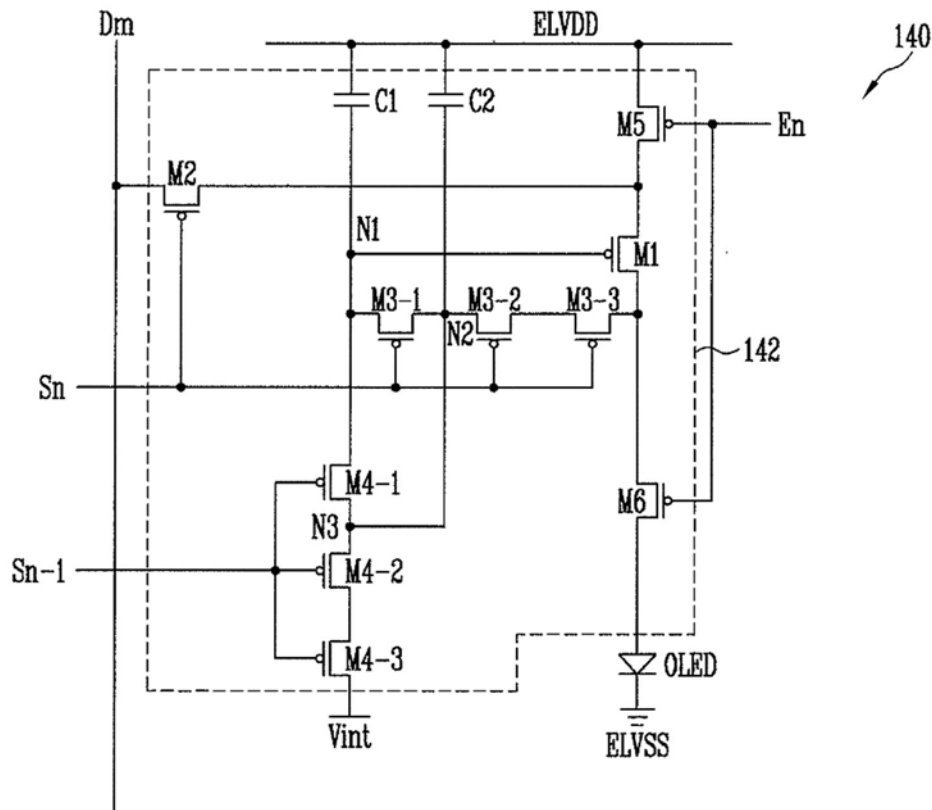


Fig. 2

2. Motivation to combine Kim-584 and Han

174. In my opinion, there are several reasons that motivate combining the teachings of Kim-584 and Han.

175. As an initial matter both references were in the same technical field because both described OLED display devices that utilized TFTs, and particularly, six TFTs arranged in a typical OLED driving configuration. Kim-584, ¶¶44, 95, Figs. 2,3; Han, ¶¶38-41, Fig. 2. And one objective in both references was to reduce leakage currents. Kim-584, ¶8; Han, ¶¶9, 58. Therefore, in my opinion, a POSITA would have had good reason to look at Han's teachings.

176. More specifically, it is my opinion that in the proposed Kim-584–Han combination, a POSITA would have found it obvious that the leakage current in the display device of Kim-584 can be further improved, based on the teachings of Han, by adding a second capacitor, C2, as described in Han. This modification is motivated based on Han’s express teachings that adding capacitor C2 in the designated location between voltage line ELVDD and TFT M3 would have “minimize[ed] or reduc[ed] the leakage currents.” Han, ¶58, Fig. 2, Fig. 4. As Han observes, prior-art designs have “a disadvantage in that even though at least four transistors are coupled at the leakage paths,... more than a fixed level of leakage current is generated.” *Id.*, ¶29. By adding a second capacitor C2 with a same voltage as C1, a voltage across M3-1 is ideally held at zero, reducing or eliminating any leakage current flow through the transistors as there is no voltage difference across the M3-1 transistor to induce an undesirable current. *Id.*, ¶¶56, 58. Therefore, reducing the leakage current that was effectuated in Han was a complementary mechanism for reducing leakage current, in addition to its series-connected TFTs.

177. In my opinion, a POSITA would have been skilled enough to use a second capacitor, as described in Han, to Kim-584’s OLED pixel to achieve the known and predictable result of reducing leakage current.

178. I will provide further comments about the combination of Kim-584 and Han in my analysis below.

3. Claim 5

a. 5[pre]: “The display apparatus of claim 1, further comprising:”

179. As described above in Ground 1A, Kim-584 teaches or suggests the limitations of base Claim 1. *See* §VIII.A.2, *supra*.

b. 5[a]: “a third thin-film transistor comprising a third semiconductor, one end of the third semiconductor being connected to one end of the first semiconductor, and the other end of the third semiconductor being connected to the first electrode layer; and”

180. In my opinion, Kim-584 teaches or suggests limitation 5[a].

181. Kim-584 teaches “a third” thin-film transistor, namely TFT T3. As shown in annotated Fig. 3 of Kim-584, below, source S3 of TFT T3 (“one end” of T3) is connected to the drain of first TFT T1 (labeled A) (“one end of first semiconductor”), and drain D3 of TFT T3 (“the other end” of T3) is connected to the first electrode layer, specifically the layer that includes storage capacitor plate Cst1 which also operates as gate electrode G1 of TFT T1 (labeled B). *See* §IV.A.1.c.

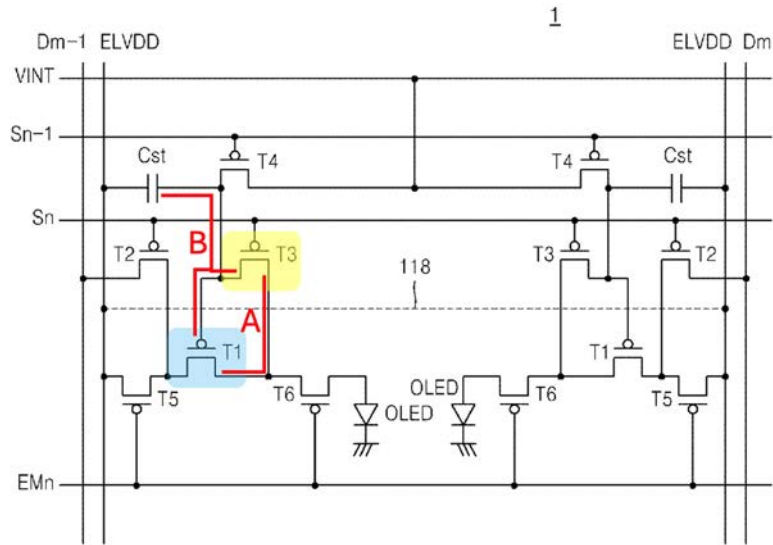


Fig. 3

182. The connectivity of T3's semiconductor ends are also evident from Fig. 6 (annotated below), showing T3's source ("one end of third semiconductor") connected to T1's drain ("one end of first semiconductor").

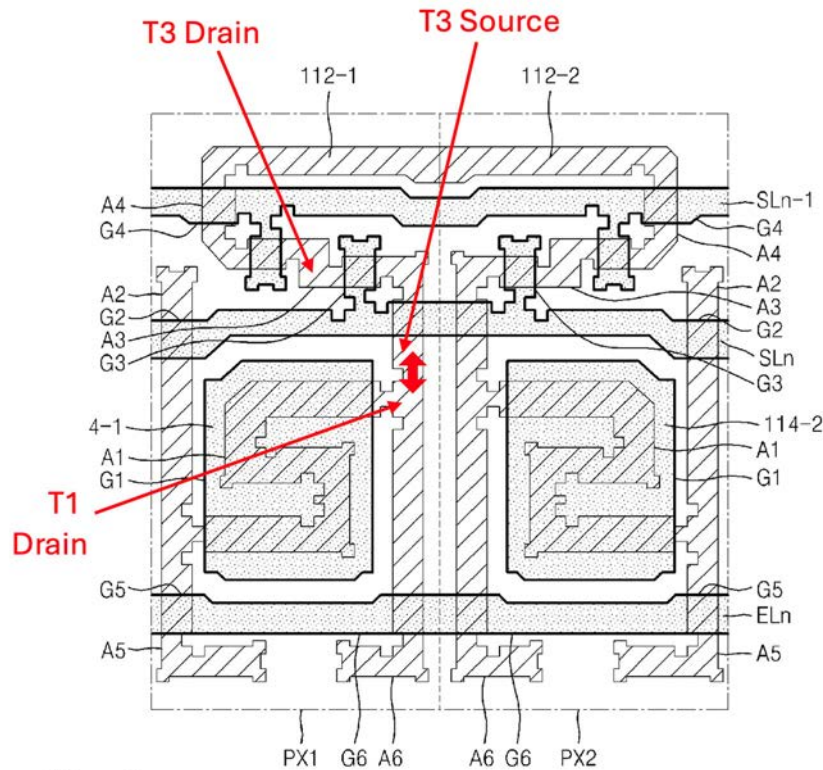


Fig. 6

183. Furthermore, Fig. 8 (annotated below) shows a connection from T3's drain ("other end third semiconductor") to first electrode Cst1 of storage capacitor through contact holes cnt1, cnt2 and connection line 120. Kim-584, ¶¶73, 76.

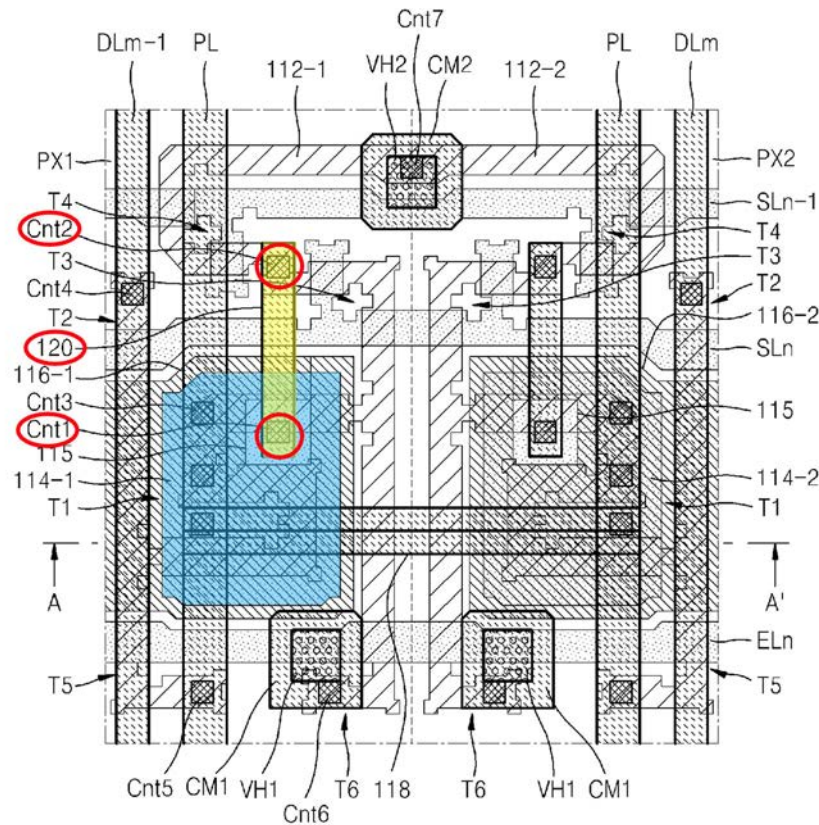


Fig. 8

184. Kim-584 also explains that “[a] source electrode S3 of the compensation TFT T3 is connected to the drain electrode D1 of the driving TFT T1 and is connected to the anode electrode of the OLED through the second emission control TFT T6. Drain electrode D3 of compensation TFT T3 is connected to first electrode Cst1 of storage capacitor Cst, drain electrode D4 of initialization TFT T4, and gate electrode G1 of driving TFT T1.” Kim-584, ¶48.

185. Accordingly, limitation 5[a] is disclosed by Kim-584.

- c. **5[b]: “a second shield layer in a layer between the first signal line and the third semiconductor and overlapping a part between a first channel area and a second channel area of the third semiconductor.”**

186. In my opinion, Kim-584 in combination with Han teaches or suggests limitation 5[b].

187. Kim-584’s Fig. 7 illustrates that T3 is a double-gated transistor because it includes two gate electrodes (shown as red circles labeled A and B in annotated partial Fig. 7 below), formed at locations where the scan line (blue) overlaps semiconductor A3 of T3. Kim-584, ¶¶45, 48, 68-70. An area C of semiconductor A3 is shown between the two gates of T3. In my opinion, a POSITA would have readily recognized that the semiconductor region under one gate electrode of T3 constitutes the “first channel area” and the semiconductor region under the other gate electrode of T3 constitutes the “second channel area.” *Id.* See also Kim-584, ¶63.

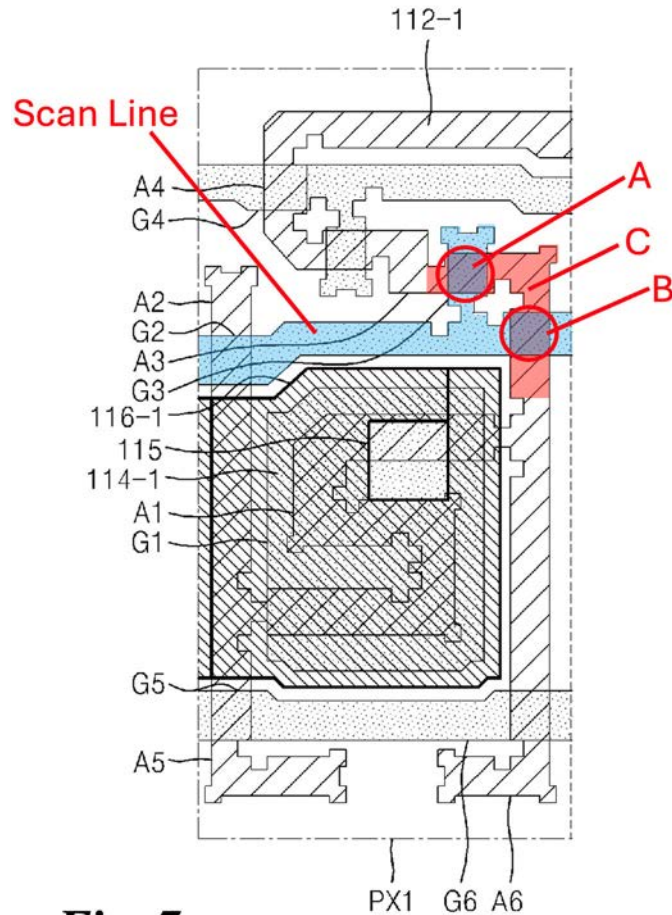


Fig. 7

188. Kim-584 does not explicitly recite a second shield layer. However, it is my opinion that this limitation would have been obvious based on the teachings of Han in the Kim-584–Han combination. Han teaches a similar 6-TFT circuit as Kim-584 that includes multiple serially connected TFTs with common gates (Han, ¶¶28, 44, Fig. 2, similar to a multi-gate TFT) and a storage capacitor (C1 in Han, and Cst in Kim-584, Fig. 2) but additionally includes a second capacitor, C2, to further reduce the leakage current. *Id.*, ¶¶41, 49, 56. Accordingly, there is a motivation to

combine Kim-584 with Han to achieve the desirable effects of Han in reducing the leakage current.

189. I note that Han does not provide a plan-view diagram of the pixel layout but shows, in its Fig. 2, and describes, in its detailed description, that second capacitor C2 is “coupled to the first power supply (ELVDD), and a first terminal ... is coupled to both a second node N2 and a third node N3.” Han, ¶49, Fig. 2.

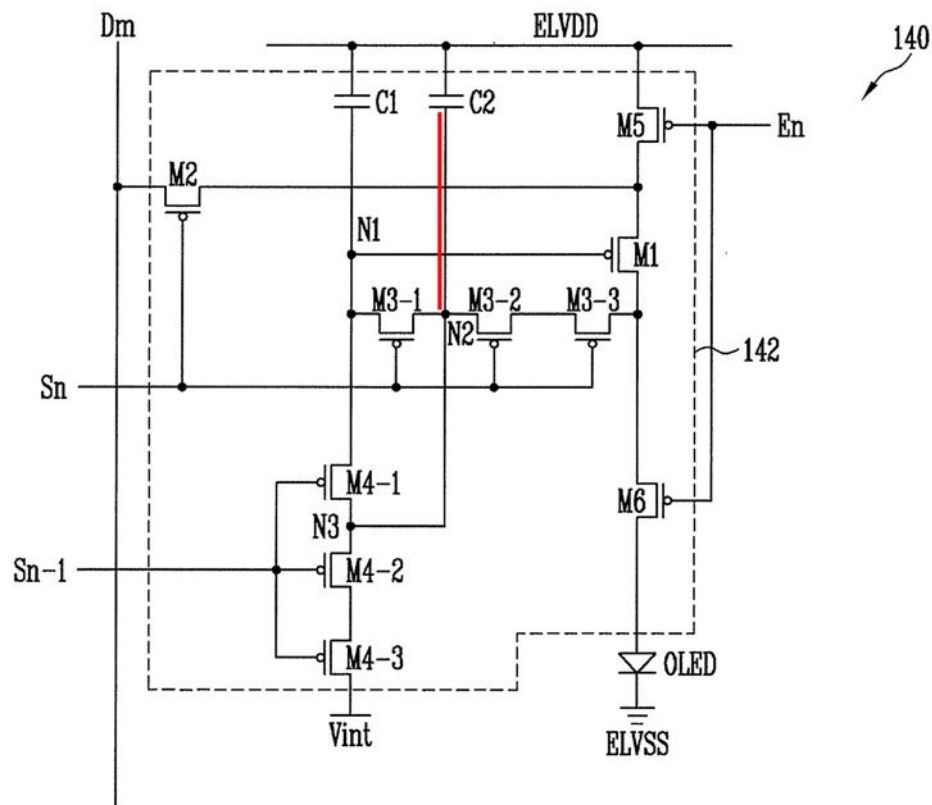


Fig. 2

190. Based on the explicit connections shown in Fig. 2 of Han, it is my opinion that a POSITA would have known that the lower plate of capacitor C2 must

be connected to the drain-source junction between the two series transistors (i.e., at N2). In the combination with Kim-584, this junction would be the semiconductor area between the two gates of T3, as annotated in Fig. 7 of Kim-584 (below). Therefore, an obvious location for placing the plates of capacitor C2 would be at or above this designated junction.

191. When Kim-584 is modified based on the teachings of Han, the lower plate of capacitor C2 would be connected to, the junction connecting the channels of the two gates of T3, and a POSITA would have the necessary skills and knowledge to carry out this task. For example, in one option, the portion of the semiconductor layer connecting the channels of the dual gates forms the lower plate of capacitor C2. Kim-584 explains that the semiconductor layer can be doped and made into a conductor outside the channel areas (e.g., in the source and drain semiconductor areas). Kim-584, ¶¶62, 63. In a known technique for OLED TFT circuit layout design for implementing a capacitor plate, the conductive doped semiconductor material can act as a capacitor plate, for example as described in Moon (EX1007) ¶76 ("the lower layer Cst1 of the storage capacitor made of semiconductor") and Kim-585 (EX1026) (Fig. 5, element 110) showing that a portion of the semiconductor layer can be a capacitor plate.

192. Alternatively, a POSITA would have understood that another obvious way to implement C2's lower plate would be to place C2's lower plate in the same layer as the gates, above the doped and conductive channel junction between the gates of T3 and above the gate insulating layer, and to connect the lower plate to the doped semiconductor junction using a "via." This alternative would have been obvious because, in this way, the lower plates of both capacitors C1 and C2 would be in the same layer (Kim-584, ¶67, Fig. 9, 114-1, 114-2). The lower plate of C2 would still be very close to the semiconductor junction, and would be easily connected to the junction by the "via" passing through the insulating layer. This alternative requires more process deposition and patterning steps but provides a more conductive lower capacitor plate closer to the upper capacitor plate of capacitor C2.

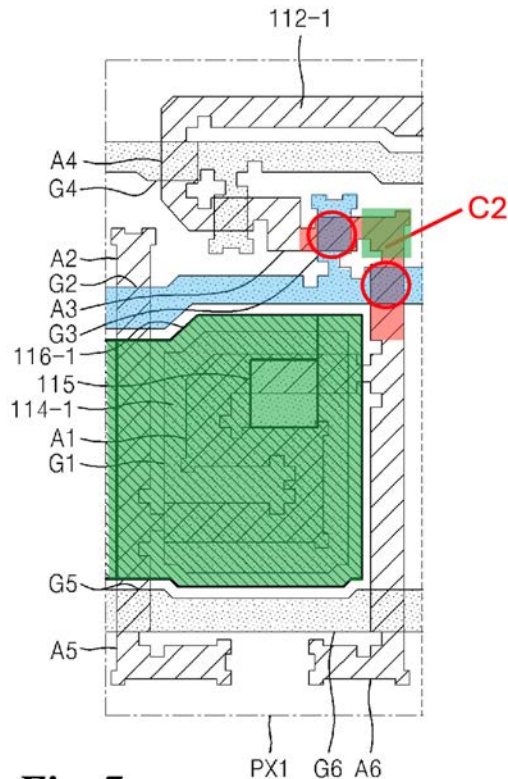


Fig. 7

193. The upper capacitor plate of C2 would be connected to voltage line ELVDD (line 172), as required by Han's circuit diagram of Fig. 2. Han, ¶49, Fig. 2. In my opinion, a POSITA would have found it obvious (and a matter of routine layout design) to implement that connection. For example, the upper capacitor plate of C2 would be connected to the upper capacitor plate (116-1) of storage capacitor, Cst, using a connection line, as shown in the annotated figure below. A POSITA would have found implementing such a connection obvious and advantageous because it minimized the length of the connection line due to the proximity of the upper plate of C1 (i.e., element 116-1 in Kim-584) to the upper plate of C2, and C1's

upper plate was already connected to ELVDD, thus providing a convenient way to connect C2's upper plate to the requisite voltage line. *Id.*, see also Kim-584, Fig. 3, showing connection of Cst to ELVDD, and Han, Fig. 2, showing connection of C1 to ELVDD. This meant the upper plates of both capacitors would be in the same layer, would be connected together and connected to ELVDD.

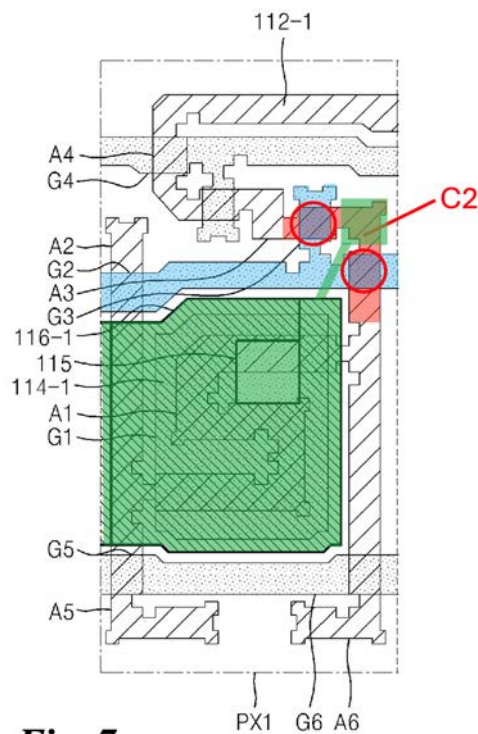


Fig. 7

194. In the combination, the upper capacitor plate of C2, being connected to a constant voltage source (ELVDD), would be the “second shield layer” because it was connected to a constant voltage line, and would also be overlapping the semiconductor region between the two gates of T3 (see the annotated figure above), similar to the reasons I explained in §IV.A.1.f. Consequently, the upper capacitor

plate of C2 would overlap “a part between a first channel area and a second channel area of the third semiconductor.” Furthermore, the “second shield layer” would be in “a layer between the first signal line and the third semiconductor” because the upper capacitor plate of C2 would reside in the same layer as storage capacitor’s upper plate (element 116-1, annotated in green in Fig. 7 above and Fig. 9 below), which as illustrated below (and explained in §83), is between the semiconductor layer (active layer 112-1) and the first signal line DLm-1. *Id.*

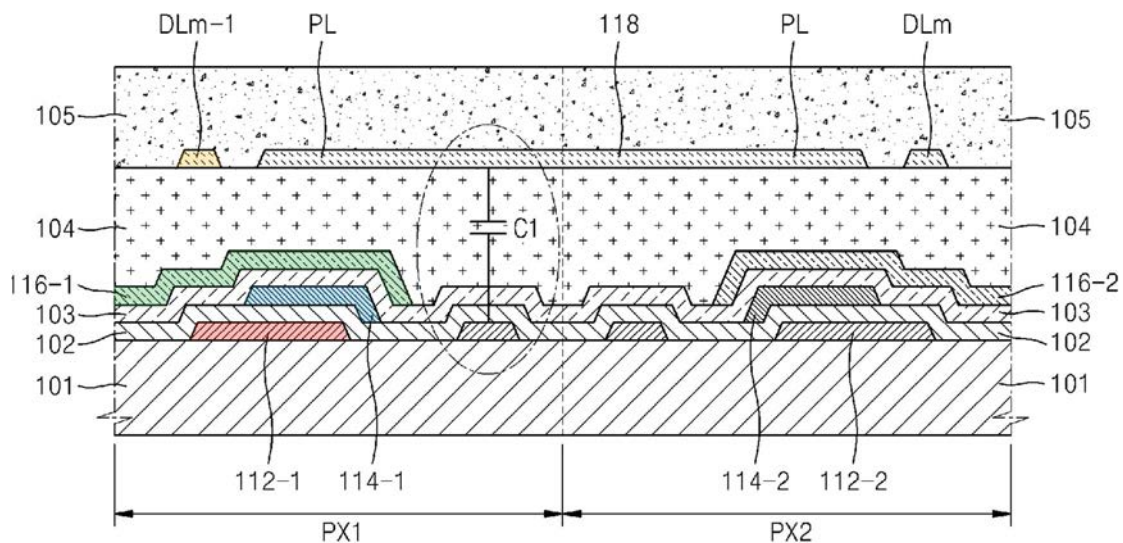


Fig. 9

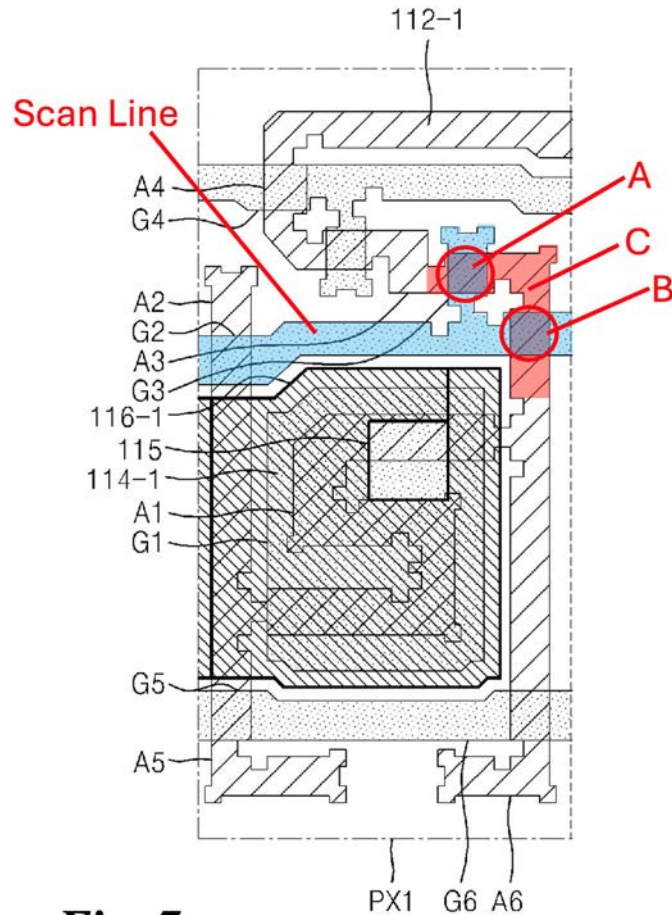
195. Accordingly, limitation 5[b] is disclosed by Kim-584 in combination with Han.

4. Claim 11

- a. 11[a]: “The display apparatus of claim 5, wherein a gate electrode of the third thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the third semiconductor, and the second gate electrode overlapping the second channel area of the third semiconductor, and”**

196. In my opinion, Kim-584 teaches or suggests limitation 11[a].

197. As discussed above with respect to Ground 1B, Claim 5, Kim-584 teaches that TFT T3 is double gated, and the combination includes at least two gate electrodes, as shown with red circles in partial annotated Fig. 7, where the gates are formed at locations where the scan line (blue) overlaps the active layer A3 (red color) of T3. Kim-584, ¶¶45, 48, 63. Therefore, in my opinion, a POSITA would have understood that one gate electrode of T3 overlaps the first channel area under that gate electrode, and the other gate electrode overlaps the second channel area under it. I note here that the two gate electrodes are in the same layer because they are both part of the scan line.



198. Accordingly, limitation 11[a] is disclosed by Kim-584.

- b. **11[b]: “wherein the gate electrode of the third thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.”**

199. In my opinion, Kim-584 teaches or suggests limitation 11[b].

200. The gate electrode for the third TFT is formed as part of scan line SL_n (“second signal line”). Kim-584, ¶48: “A gate electrode G3 of the compensation TFT T3 is connected to the first scan line SL_n.” Kim-584 further describes that “[t]he

data signal line DL_m intersects with the first scan line SL_n and transmits a data signal D_m.” Kim-584, ¶45; see also *id.*, Fig. 8, showing SL_n crossing DL_m and DL_m-1. As explained in connection with Claim 1 in Ground 1A, data line DL_m-1 is construed as the “first signal line.” See §VIII.A.2.e.

201. Kim-584 discusses that the scan line is in the same layer as first capacitor electrode 114-1 (“first electrode layer;” see §75): “A **first gate lines are formed on the first gate insulating layer 102. The first gate lines may include a first scan line SL_n**, a second scan line SL_n-1, an emission control line EL_n, **and first capacitor electrodes 114-1 and 114-2.**” Kim-584, ¶66.

202. Accordingly, limitation 11[b] is disclosed by Kim-584.

5. Claim 12: “The display apparatus of claim 5, further comprising a first voltage line in the same layer as the first signal line, wherein the second shield layer is connected to the first voltage line.”

203. In my opinion, Kim-584 teaches or suggests Claim 12.

204. Kim-584 teaches that voltage line PL (“first voltage line”) is in the same layer as data line DL_m-1 (“first signal line”), as shown in annotated Fig. 9 below marked in yellow. Kim-584 explains that “driving voltage line PL transmits a first power supply voltage ELVDD and is substantially parallel with the data signal line DL_m.” Kim-584, ¶45. As explained in connection with Claim 5, in the combination,

the top electrode of capacitor C2 (“second shield layer”) is connected to ELVDD (“first voltage line”). See §VIII.B.3.c.

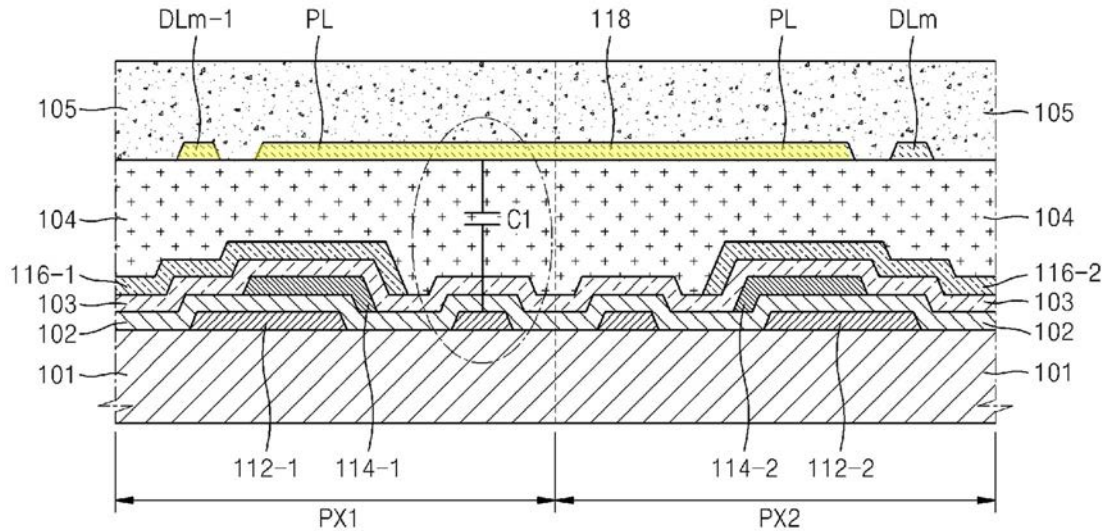


Fig. 9

205. Accordingly, Claim 12 is disclosed by Kim-584.

6. Claim 13: “The display apparatus of claim 5, wherein the second shield layer is a part of the second electrode layer.”

206. As explained in connection with Claim 5 (see §VIII.B.3.c), it is my opinion that it would have been obvious to a POSITA that the top electrode of second capacitor C2 would be in the same layer. As explained in connection with Claim 2 in Ground 1A, the top plate of the storage capacitor is part of the second electrode layer (see §VIII.A.3), and therefore, in the combination, the top plate of capacitor C2 (“second shield layer”) would also be in the second electrode layer.

207. Accordingly, Claim 13 is disclosed by Kim-584.

7. Claim 14: “The display apparatus of claim 5, further comprising a connecting line connecting the other end of the third semiconductor and the first electrode layer and being in the same layer as the first signal line.”

208. In my opinion, Kim-584 teaches or suggests Claim 14.

209. Kim-584 shows that the drain of T3 (“other end of the third semiconductor”) is connected to the storage capacitor’s first electrode (lower plate) of Cst1 and to gate electrode G1 of TFT T1 (“the first electrode layer”), as shown in annotated Fig. 3 below with line B.

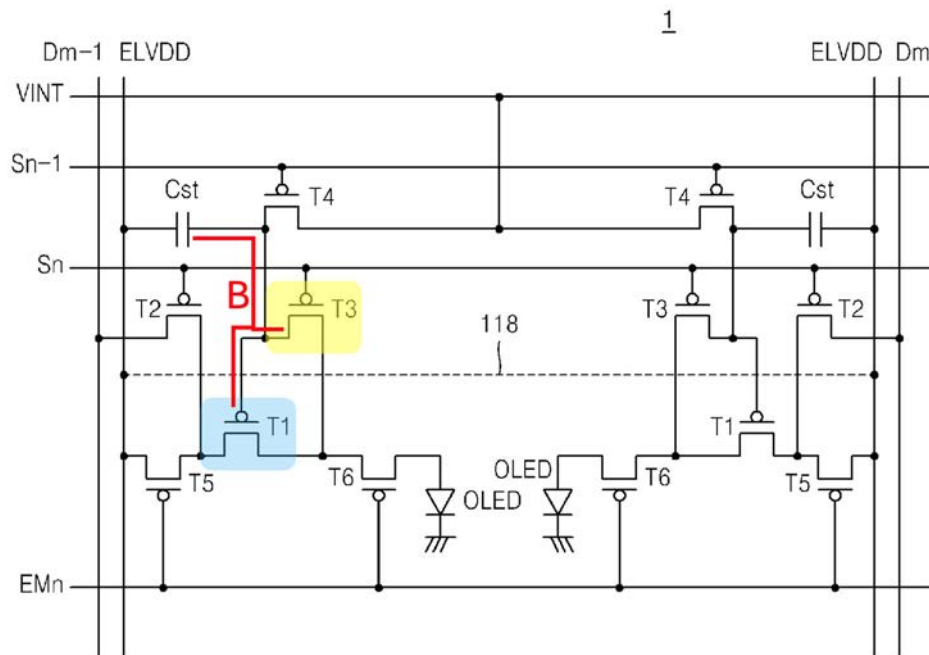


Fig. 3

210. As shown in annotated Fig. 8 (below) and explained in Kim-584, the drain of T3 is connected to first capacitor electrode 114-1 (blue) via connection line 120 (yellow) which is in the same layer as data line DLM-1 (“first signal line”).

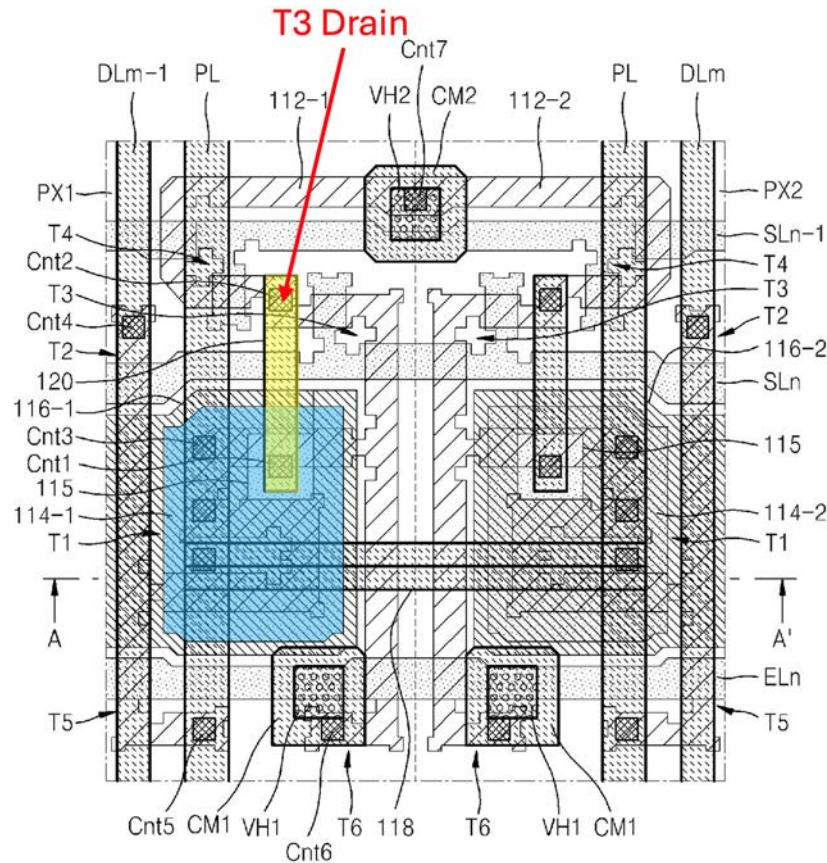


Fig. 8

211. Kim-584 explains that “[t]he **connection line 120 connects the first capacitor electrodes 114-1 and 114-2, the compensation TFTs T3, and the initialization TFTs T4.**” Kim-594, ¶76. Kim-584 further explains that “[t]he **data signal lines DLM-1 and DLM, the driving voltage lines PL including the connection line 118, the connection line 120, the first contact metals CM1, and the second contact metals CM2 may be formed of the same material on the same layer.** *Id.*, ¶77.

212. Accordingly, Claim 14 is disclosed by Kim-584.

8. Claim 28

a. 28[pre]: “A display apparatus comprising:”

213. In my opinion, each of Kim-584 and Han both describe the preamble because both describe displays, and in particular to OLED displays. See, e.g., Kim-584, Abstract and Han, Abstract.

b. 28[a]: “a first thin-film transistor comprising a first semiconductor;”

214. In my opinion, Kim-584 teaches this limitation as driving thin film transistor T1. See §VIII.A.2.b.

c. 28[b]: “a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;”

215. In my opinion, Kim-584 discloses this limitation. See §68.

d. 28[c]: “a first signal line over the first electrode layer;”

216. In my opinion, Kim-584 discloses this feature as data line DLm-1 (“first signal line”). See §VIII.A.2.e. Fig. 9 of Kim-584 (annotated below) shows DLm-1 (yellow) being over the lower capacitor electrode (114-1), which is part of the “first electrode layer.”

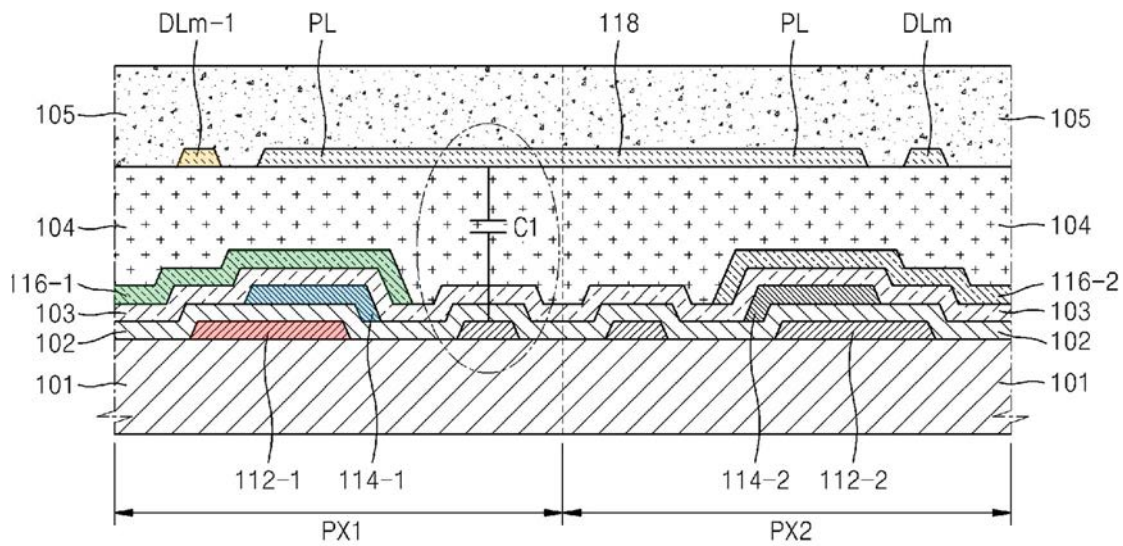


Fig. 9

- e. **28[d]: “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and”**

217. In my opinion, Kim-584 discloses this limitation because it discloses TFT T3 having its source (“one end of second semiconductor”) connected to the drain of TFT T1 (“one end of first semiconductor”), and its drain (“the other end of second semiconductor”) connected to gate electrode G1 of TFT T1 and to storage capacitor plate Cst1, as shown in annotated Fig. 3 below, and as described in connection with limitation 5[a]. While Claim 5 recites a “third” TFT (as opposed to a “second” TFT in Claim 28), TFT T3 of Kim-584 is mapped to the “second” TFT in Claim 28.

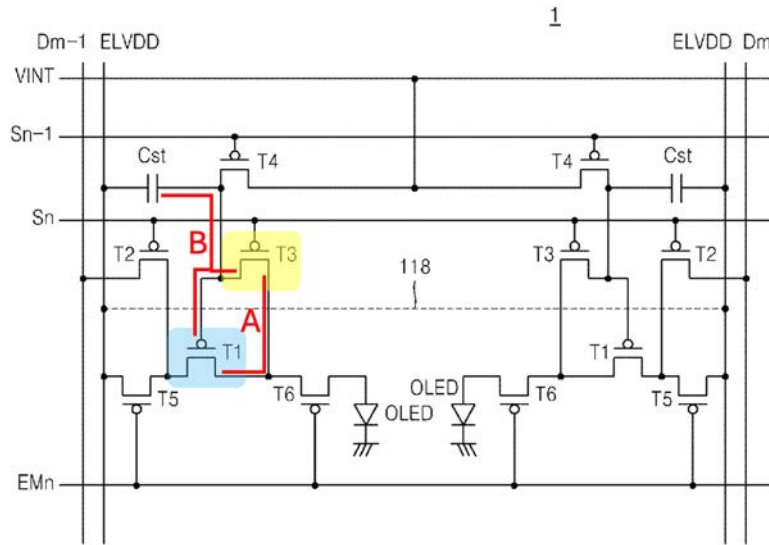


Fig. 3

- f. **28[e]: “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.”**

218. In my opinion, Kim-584 in combination with Han teaches or suggests limitation 28[e], as explained in connection with limitation 5[b]. In Claim 28 (similar to Claim 5), the top capacitor plate of capacitor C2 constitutes “a shield layer.”

9. Claim 29

- a. **29[a]: “The display apparatus of claim 28, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and”**

219. See Claim 11, limitation 11[a]. In Claim 29, TFT T3 is construed as the “second” TFT.

- b. **29[b]: “wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.”**

220. See Claim 11, limitation 11[b].

10. Claim 30: “The display apparatus of claim 28, further comprising a voltage line in the same layer as the first signal line, wherein the shield layer is connected to the voltage line.”

221. See Claim 12, which recites this limitation while noting that Claim 12 recites a “first voltage line” rather than “a voltage line” (both of which are mapped to voltage line PL or ELVDD of Kim-584) and “the second shield layer” rather than “the shield layer” (both of which are mapped to top capacitor plate of capacitor C2 in the Kim-584–Han combination).

11. Claim 31: “The display apparatus of claim 28, further comprising a second electrode layer over the first electrode layer and overlapping the first electrode layer, wherein the shield layer is a part of the second electrode layer.”

222. This claim is rendered obvious by Kim-584, as described in Ground 1A, Claim 1, limitation 1[c], and in Ground 1B, Claim 13, related to a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer, and the shield layer being part of the second electrode layer. In Claim 28, the second shield layer corresponds to the top plate of the capacitor C2, which as explained in connection with Claim 13, is part of the second electrode layer.

12. Claim 32: “The display apparatus of claim 31, further comprising a voltage line in the same layer as the first signal line, wherein the voltage line is connected to the second electrode layer.”

223. See Claim 4 in Ground 1A. §103.

C. Ground 2A: Kim-923 Renders Obvious Claims 1-4, 9-10, 20-23 and 33

1. Summary of Kim-923

224. Kim-923 relates to an organic light emitting diode (OLED) display. Kim-923, ¶3. The OLED display disclosed in Kim-923 includes circuitry to control the operation of each OLED in the OLED display. *Id.*, ¶¶ 6,60. Kim-923 addresses the problem of prior s OLED displays which have a narrow driving range for a gate voltage applied to a driving thin-film transistor, which limits the number of gray

levels that can be displayed by any given pixel of the OLED display. *Id.*, ¶¶ 7, 9, 40-41.

2. Claim 1

a. 1[pre]: “A display apparatus comprising:”

225. In my opinion, Kim-923 teaches or suggests limitation 1[pre].

226. Kim-923 describes a display apparatus, e.g., “The described technology relates generally to an organic light emitting diode display.” Kim-923 ¶3.

b. 1[a]: “a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;”

227. In my opinion, Kim-923 teaches or suggests limitation 1[a].

228. Kim-923 discloses “a first thin-film transistor” as TFT T1, which is illustrated in its Fig. 1 (annotated below).

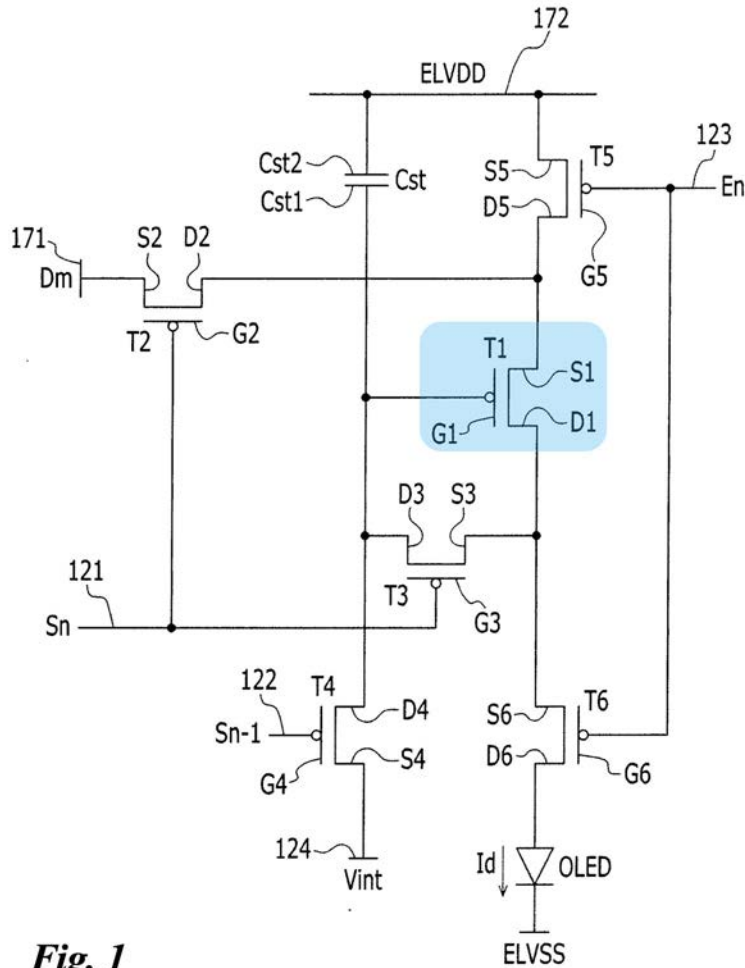


Fig. 1

229. Kim-923 discloses that first thin-film transistor T1 comprises “a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area.” Kim-923 explains that its driving TFT T1 is formed along a semiconductor layer (“first semiconductor”): “The **driving thin film transistor T1**, the switching thin film transistor T2, the compensation thin film transistor T3, the initialization thin film transistor T4, the operation control thin film transistor T5, and the light emission control thin film transistor T6 are **formed along**

the semiconductor layer 131, and the semiconductor layer 131 is bent to have various shapes.” Kim-923, ¶79. Kim-923 further explains, “**The semiconductor layer 131** may be formed of polysilicon, and **includes a channel region**, which is not doped with an impurity, **and a source region and a drain region formed at respective sides of the channel region** to be doped with the impurity.” *Id.* I note that transistors T1 through T6 in Kim-923 describe a conventional TFT architecture. *Id.*, ¶85.

[0085] The driving source electrode **176a** corresponds to the driving source region **176a** doped with the impurity in the driving semiconductor layer **131a**, and the driving drain electrode **177a** corresponds to the driving drain region **177a** doped with the impurity in the driving semiconductor layer **131a**. The storage capacitor Cst is formed thereon to overlap the driving gate electrode **125a**.

230. Accordingly, limitation 1[a] is disclosed by Kim-923.

c. **1[b]: “a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;”**

231. In my opinion, Kim-923 teaches or suggests limitation 1[b].

232. Kim-923 discloses this limitation because it describes an electrode layer that includes a driving gate electrode 125a and overlaps the channel region of the first TFT T1. Kim-923 states, “The **driving gate electrode 125a** is separated from the scan line 121 and the floating gate electrode 25 **overlaps the driving channel region 131a1 of the driving semiconductor layer 131a**.” Kim-923, ¶106.

I note that the quoted portion of Kim-923 erroneously mentions “floating gate electrode 25,” and that in my opinion, a POSITA would readily appreciate, from the description and accompanying drawings of Kim-923, that the floating gate electrode was not intended to be included in the quoted text.

233. Regardless, Figs. 3 and 5 of Kim-923, annotated below, show that driving gate electrode 125a (blue) overlays channel region 131a1 (red) of the first TFT.

electrode 125a) is in a layer above the first semiconductor, indicated by driving channel region 131a1.

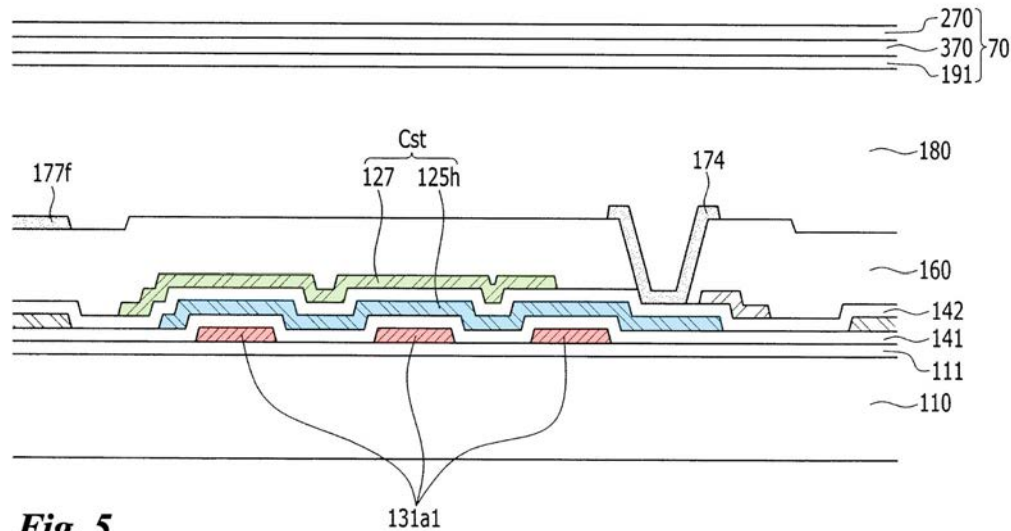


Fig. 5

235. Therefore, Kim-923 teaches or suggests an electrode layer that includes driving gate electrode 125a/h (“first electrode layer”) positioned over semiconductor 131a (“first semiconductor”) and overlaps driving channel region 131a1 (“the channel area of the first semiconductor”).

236. Accordingly, limitation 1[b] is disclosed by Kim-923.

d. 1[c]: “a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;”

237. In my opinion, Kim-923 teaches or suggests limitation 1[c].

238. Kim-923 discloses “a second electrode layer” as a layer that includes second storage capacitor plate 127 that is over the electrode layer that includes

driving gate electrode 125a/h (“first electrode layer”). As shown in annotated Fig. 5 above, second storage capacitor plate 127 (green), is in a layer over first storage capacitor plate 125h (“first electrode layer” shown in blue) and at least partially overlaps it. Annotated Fig. 3 below shows the relative positioning in plan-view of driving gate electrode/first capacitor plate 125a/125h (blue) and second storage capacitor plate 127 (green), showing that the second storage capacitor plate overlaps the first storage capacitor plate.

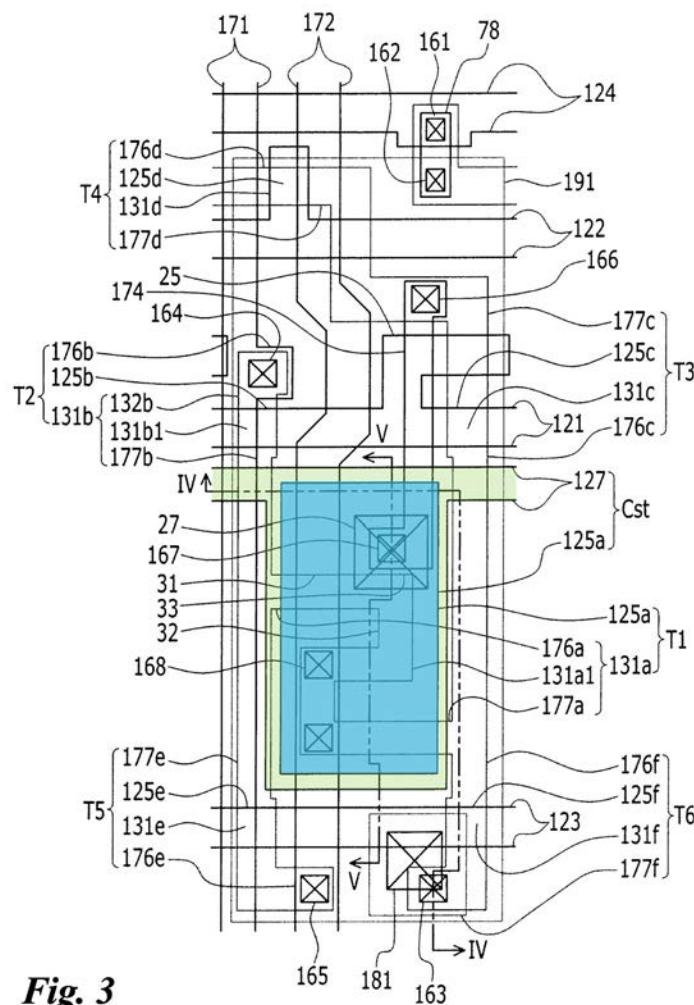


Fig. 3

239. Kim-923 explains that "[t]he **second storage capacitor plate 127 overlaps the first storage capacitor plate 125h** to form the storage capacitor Cst, and the first storage capacitor plate 125h overlaps the driving semiconductor layer 125a." Kim-923, ¶109; *see also id.*, Fig. 8, element 127. Thus, Kim-923 teaches that "a second electrode layer" overlaps the "first electrode layer."

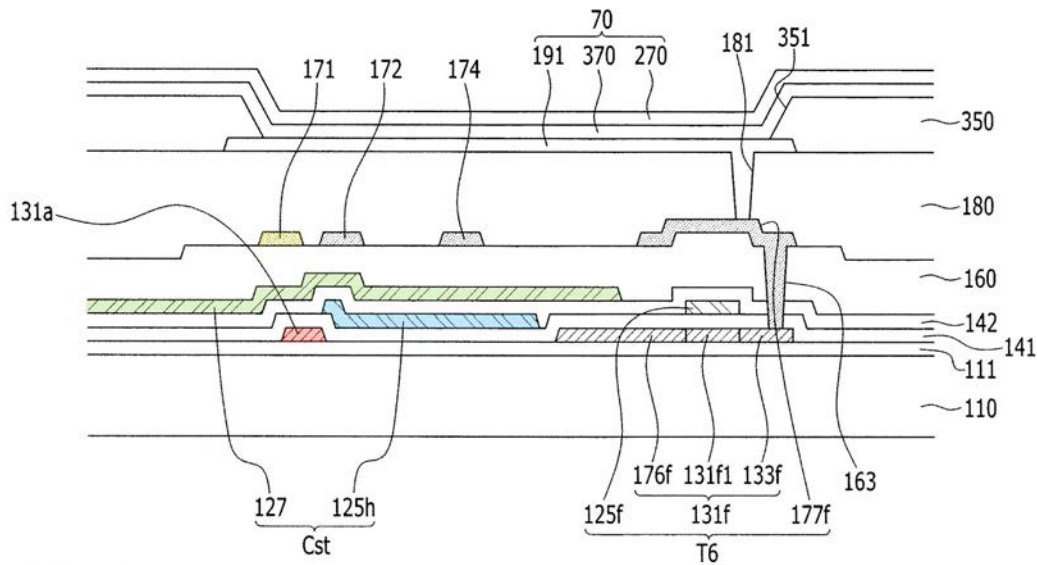
240. Accordingly, limitation 1[c] is disclosed by Kim-923.

e. 1[d]: "a first signal line over the second electrode layer; and"

241. In my opinion, Kim-923 teaches or suggests limitation 1[d].

242. Kim-923 discloses data line 171 ("first signal line") over the second storage capacitor plate 127, which is in the second electrode layer. Kim-923 explains that "one pixel of the organic light emitting diode display ... includes a plurality of **signal lines** 121, 122, 123, 124, **171**, and 172." Kim-923, ¶60. Accordingly, signal line 171, also referred to as data line 171, is the "first signal line" and is used for transferring a data signal Dm. Kim-923, ¶62.

243. Fig. 4 of Kim-923, annotated below, shows data line 171 (shown in yellow) in the same layer above the second electrode layer (i.e., the electrode layer that contains second storage capacitor plate 127, shown in green). Therefore, data line 171 is a signal line "over the second electrode layer."



244. Accordingly, limitation 1[d] is disclosed by Kim-923.

- f. **1[e]: “a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.”**

245. In my opinion, Kim-923 teaches or suggests limitation 1[e].

246. Kim-923 teaches or suggests “a first shield layer” as the second storage capacitor plate 127, or a part thereof, situated in a layer between data line 171 (“first signal line”) and “the first semiconductor” 131a. *See* annotated Fig. 4 above.

247. Fig. 3 has been annotated below to show “a part of one of the source area and the drain area of the first semiconductor” in dark purple, which is overlapped by second storage capacitor plate 127 (“first shield layer”). Other annotations in Fig. 3 include the shield layer in green and the channel in light red. In

my opinion, similar to the explanation provided in connection with 1[e] in Ground 1A, a POSITA would readily understand that the semiconductor area under gate electrode 125a (outlined with a dashed-red line) is channel region (131a) of TFT T1 and the semiconductor area that is not overlapping with gate electrode 125a comprises the source on one end and the drain on the other end of TFT T1. See §VIII.A.2.b. Furthermore, designations for “the driving source electrode 176a, and the driving drain electrode 177a” are provided in Kim-923’s specification. Kim-923, ¶80. Similar to my explanation in connection with Ground 1A, the purple annotated source region in Fig. 3 below shows “a” part of the source area that is overlapped by the shield layer that renders the limitations in 1[e] obvious. But, as I explain in connection with Claim 8, a larger area of the source region also renders limitations in 1[e] obvious.

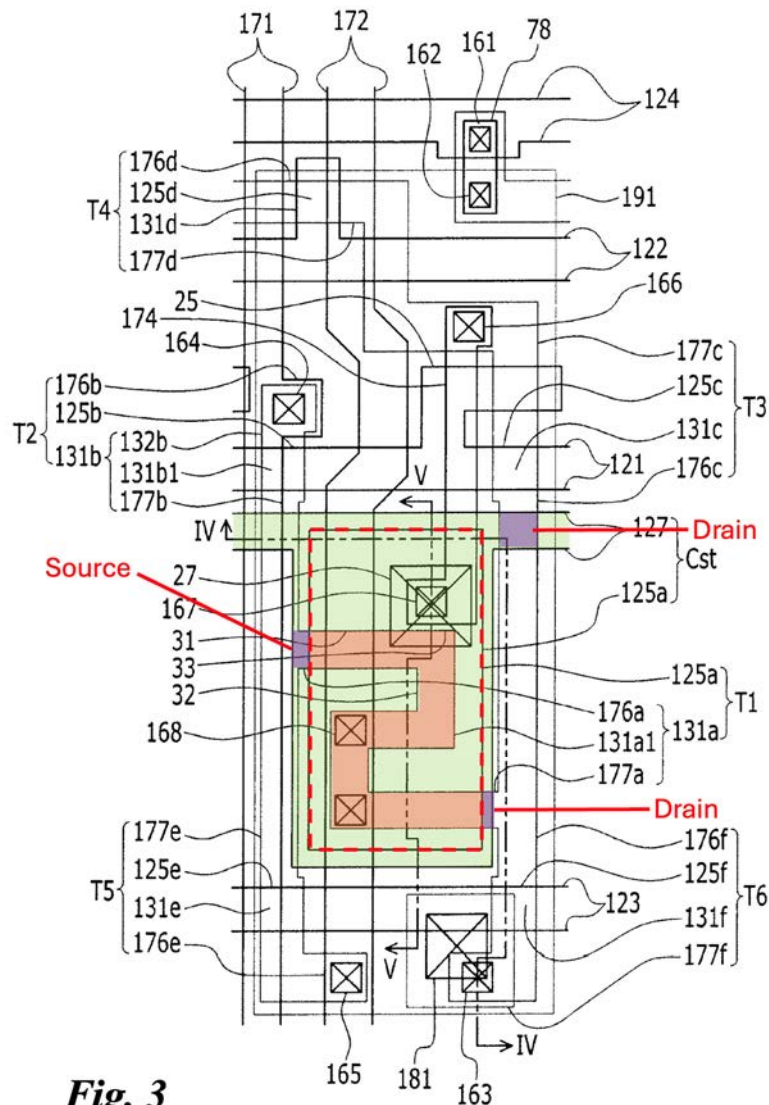


Fig. 3

248. As explained in 1[e] in Ground 1A, the interpretation of second storage capacitor plate 127 as the first shield layer is consistent with the '015 Patent. §VIII.A.2.f.

249. In my opinion, a POSITA would have understood and found it obvious that top capacitor plate 127 of Kim-923 (or a part thereof) is a conductor that is

disposed in a layer above T1 (above driving semiconductor layer 131a and driving gate electrode 125a/first storage capacitor plate 125h), is connected to a constant voltage source, ELVDD, (see Figs. 1 and 2, and voltage line 172 therein) and would shield T1 from the electromagnetic interference and noise produce by the signal lines (e.g., 171) disposed in upper layers. This is because a capacitor requires pairs of conductors, and when positioned over a signal line will naturally shield that signal line from EMI.

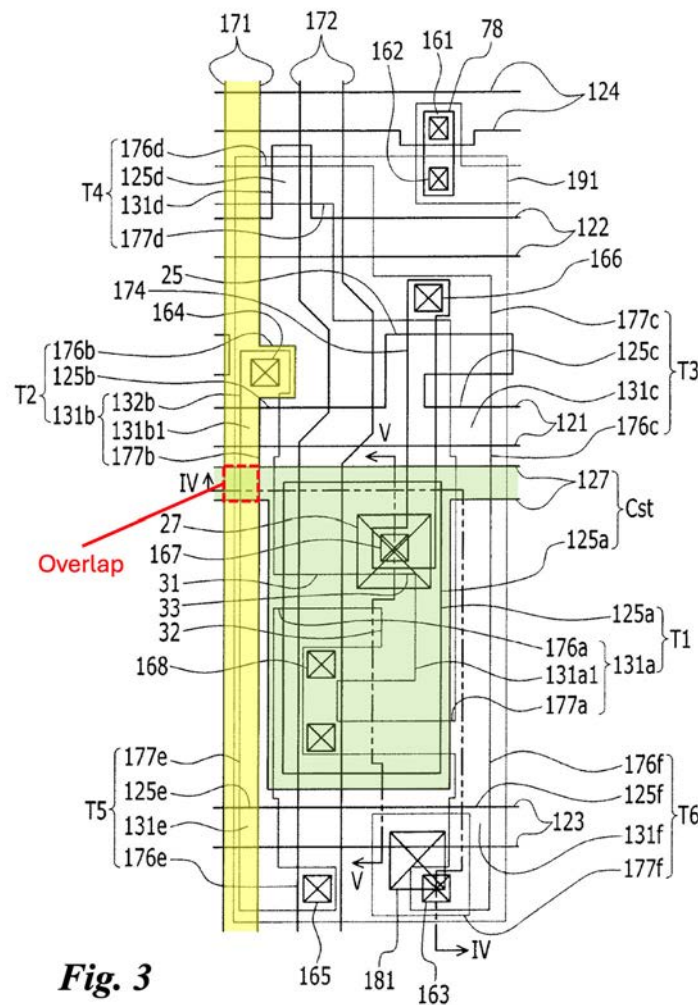
250. Accordingly, limitation 1[e] is disclosed by Kim-923.

3. Claim 2: "... wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line."

251. In my opinion, Kim-923 teaches or suggests this limitation.

252. As discussed in 1[e] above and illustrated in annotated Fig. 3 (below), Kim-923 discloses "the first shield layer" as the second capacitor plate 127 (or a part thereof). The second capacitor plate is part of a "second electrode layer" because it is in a layer distinct from the first capacitor plate 125a, and also includes other metal components (voltage lines): **"[t]he second storage capacitor plate 127 is coupled to the adjacent pixel, and is formed of the same material as the initialization voltage line 124, and is formed on the same layer as the initialization voltage line 124."** Kim-923, ¶88.

253. Second storage capacitor plate 127 overlaps part of signal line 171 (“first signal line”), as shown in Fig. 3 as annotated below and in Fig. 4 as annotated above in Ground 2A, Claim 1, limitation 1[d]. *See also* §VIII.A.3.



254. Accordingly, Claim 2 is disclosed by Kim-923.

4. Claim 3: "... further comprising a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first signal line."

255. In my opinion, Kim-923 teaches or suggests Claim 3.

256. Kim-923 discloses "a second thin-film transistor comprising a second semiconductor" as TFT T2. "As shown in Fig. 1 annotated below, one pixel of the organic light emitting diode display according to the first exemplary embodiment includes a plurality of signal lines 121, 122, 123, 124, 171, and 172, a plurality of **thin film transistors** T1, T2, T3, T4, T5, and T6, a storage capacitor Cst, and an OLED coupled to the plurality of signal lines." Kim-923, ¶60.

257. Kim-923 discloses that TFT T2 comprises a second semiconductor. Kim-923, ¶¶79, 90.

[0090] The switching thin film transistor T2 includes the switching semiconductor layer 131b, the switching gate electrode 125b, the switching source electrode 176b, and the switching drain electrode 177b. The switching source electrode 176b is a portion protruding from the data line 171, and the switching drain electrode 177b corresponds to a switching drain region 177b doped with an impurity in the switching semiconductor layer 131b.

258. Kim-923 discloses that the second semiconductor has "one end" (D2) that is "connected to one end of the first semiconductor" (S1) (red line in annotated Fig. 1 below) and T2's "other end" is "connected to the first signal line (Dm, signal

line 171)³, (green line in annotated Fig. 1). These connections are also explicitly described in Kim-923. See Kim-923, ¶64.

[0064] A gate electrode G2 of the switching thin film transistor T2 is coupled to the scan line 121, a source electrode S2 of the switching thin film transistor T2 is coupled to the data line 171, a drain electrode D2 of the switching thin film transistor T2 is coupled via the operation control thin film transistor T5 to the driving voltage line 172 while being coupled to the source electrode S1 of the driving thin film transistor T1. The switching thin film transistor T2 is turned on according to the scan signal Sn transferred through the scan line 121 to perform a switching operation for transferring the data signal Dm transferred to the data line 171 to the source electrode of the driving thin film transistor T1.

Kim-923, ¶64.

³ For Claim 3, the “first signal line” is mapped only to Kim-923’s data line 171.

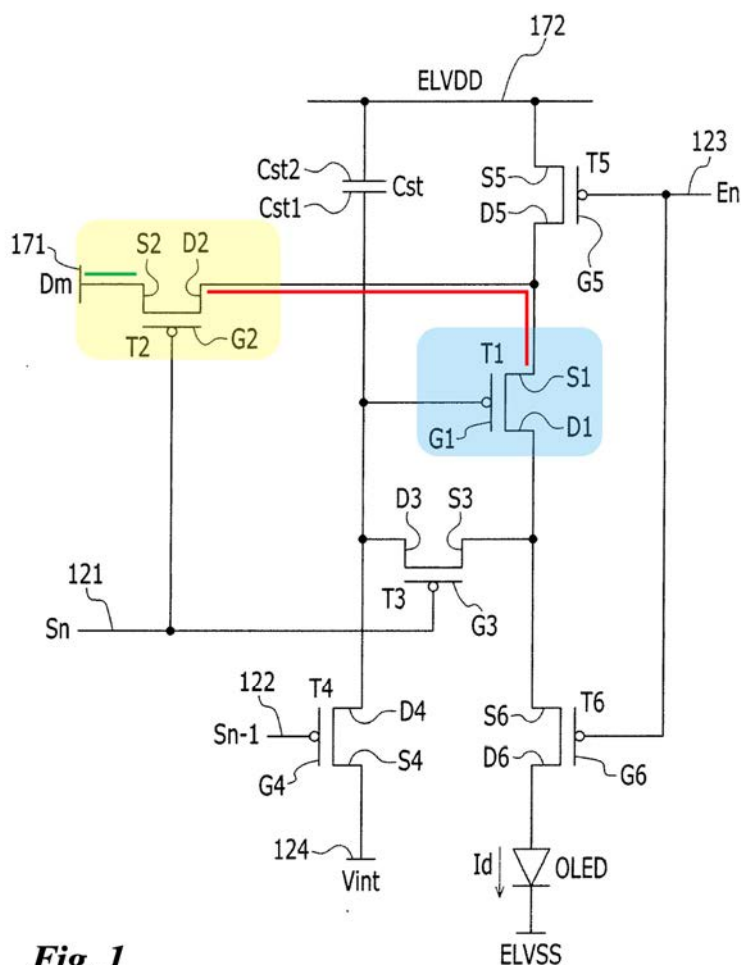


Fig. 3.

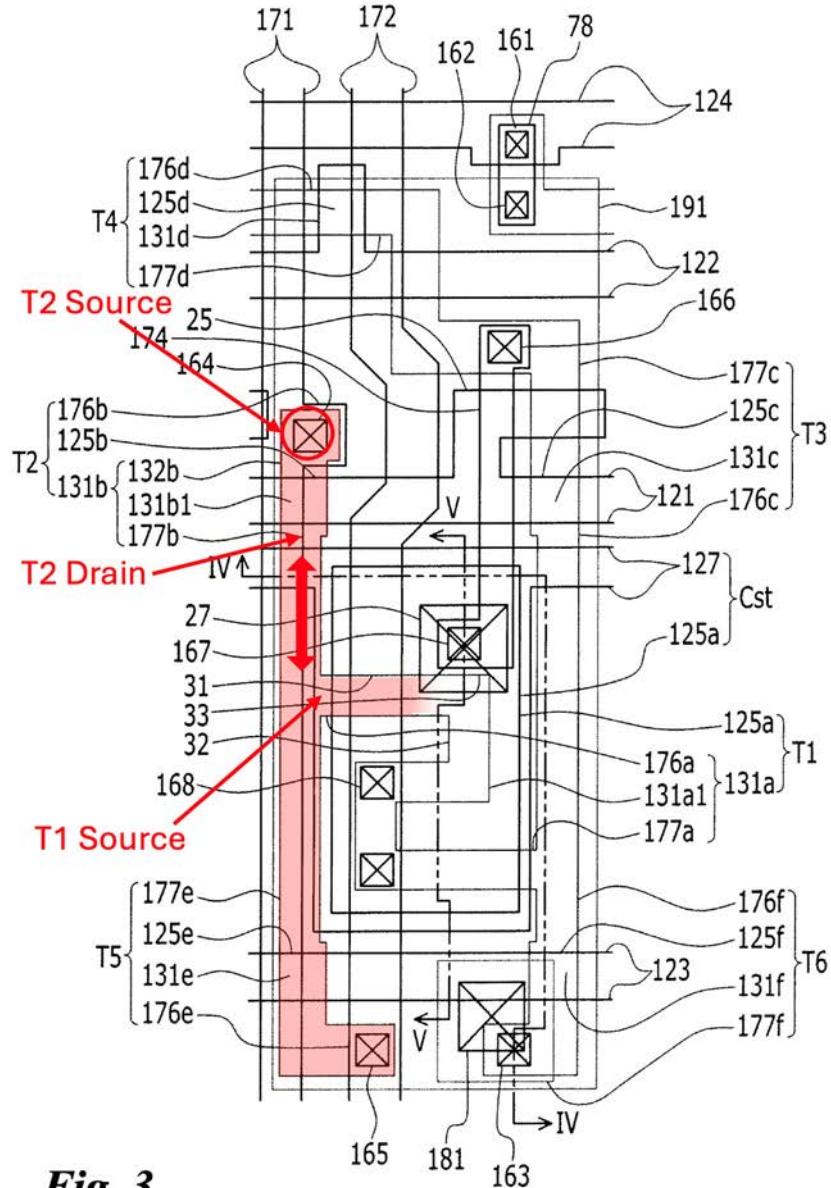


Fig. 3

260. Accordingly, Claim 3 is disclosed by Kim-923.

5. Claim 4: "... further comprising a first voltage line in the same layer as the first signal line and connected to the second electrode layer."

261. In my opinion, Kim-923 teaches or suggests Claim 4.

262. Kim-923 discloses “a first voltage line” as voltage line 172 that is in the same layer as data line 171.

263. Kim-923 further discloses that voltage line 172 (“first voltage line”) is connected to the second capacitor plate (“second electrode layer”): “[a]nother end **Cst2 of the storage capacitor Cst is coupled to the driving voltage line 172.**” Kim-923, ¶69. “The storage capacitor Cst includes a first storage capacitor plate 125h and a second storage capacitor plate 127, with the second gate insulating layer 142 interposed therebetween.” Kim-923, ¶86. I note that Fig. 4 (below) further illustrates the positioning of lines 171 and 172 in the same layer.

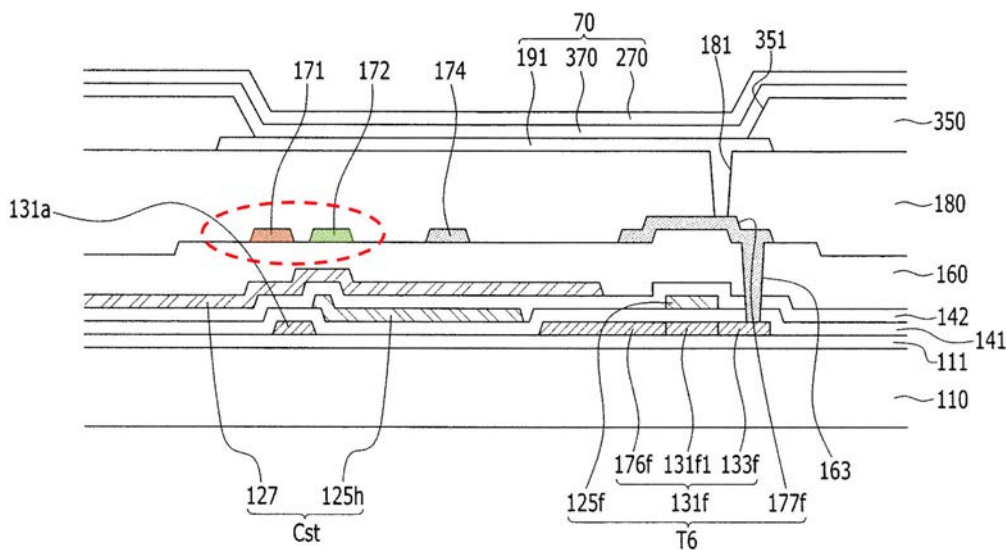


Fig. 4

264. Accordingly, Claim 4 is disclosed by Kim-923.

6. Claim 8

a. 8[pre] “... wherein the first signal line extends in a first direction, and”

265. In my opinion, Kim-923 teaches or suggests limitation 8[pre].

266. As shown in Fig. 3, annotated below, data line 171 (“first signal line”) extends in a first direction.

Specifically, the larger top capacitor plate 127 is larger. In the Fig. 8 embodiment, data line 171 also extends in a first direction, as shown below. The analysis for the embodiment of Fig. 8 is substantially the same as for the embodiment of Fig. 3, showing L_A is longer than L_B . Claim 8 is rendered obvious under either embodiment. In my opinion, it would have been obvious to a POSITA to use the larger capacitor plate in embodiment of FIG. 8 because it would have provided one of a few alternative shapes for the capacitor plate, provided increased shielding, and was already described in Kim-923.

270. As shown in annotated Figs. 3 and 8 above, second storage capacitor plate 127 (“first shield layer” – green) overlaps the source area of TFT T1 (purple) along a length L_A , and second storage capacitor overlaps the drain area of TFT T1 along length L_{C1} and L_{C2} . As also shown above, L_A is larger than L_B (blue), which is the length of one side of the bottom capacitor plate (“a length of the first electrode layer”) along the first direction.

271. In my opinion, it would have been obvious to a POSITA that the source and drain areas comprise doped semiconductor regions (i.e., regions other than channel regions) that extend along the first direction (annotated in orange). In particular, I note that the source area of T1 has a length, L_A , that extends to and merges with the semiconductor regions associated with drain of T5 (D5) and drain of T2 (D2) because of direct connections between S1, D2 and D5. These direct connections are shown in annotated Figs. 3 and 8 (above) and Fig. 1 of Kim-923 (annotated below), which indicates the associated doped semiconductor regions would be at the same voltage level, and thus would be considered to be a source area of T1.



272. Kim-923 explains that the undoped regions of the semiconductor are the channel regions, whereas the drain and source electrodes are formed by doping the regions of the semiconductor. Kim-923, ¶¶79, 85, 94. Accordingly, it is my opinion that the areas of the semiconductor outside of the undoped channel region associated with S1, D2 and D5 all have the same material and the same doping in order to maintain the same voltage.

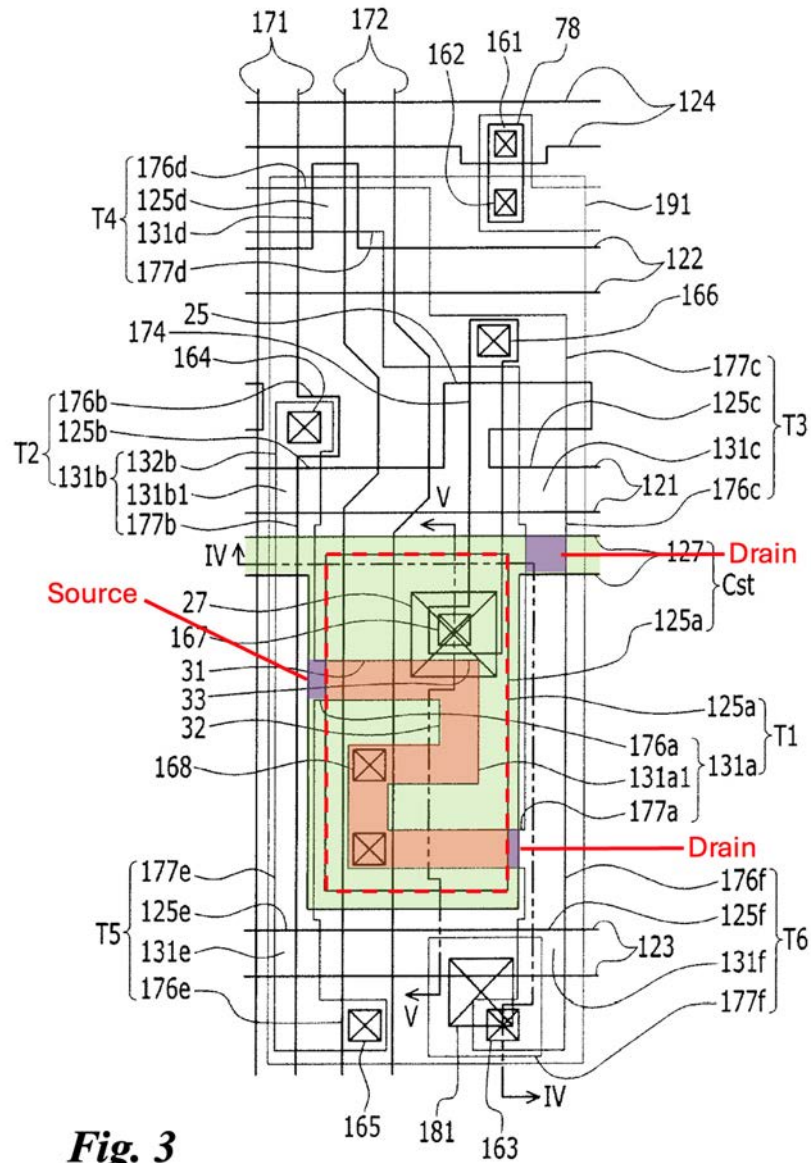
273. Such an interpretation is not only consistent with the '015 Patent, but support for claim limitation 8[a] can only be found in the '015 Patent by adopting such an interpretation. See §VIII.A.6.b.

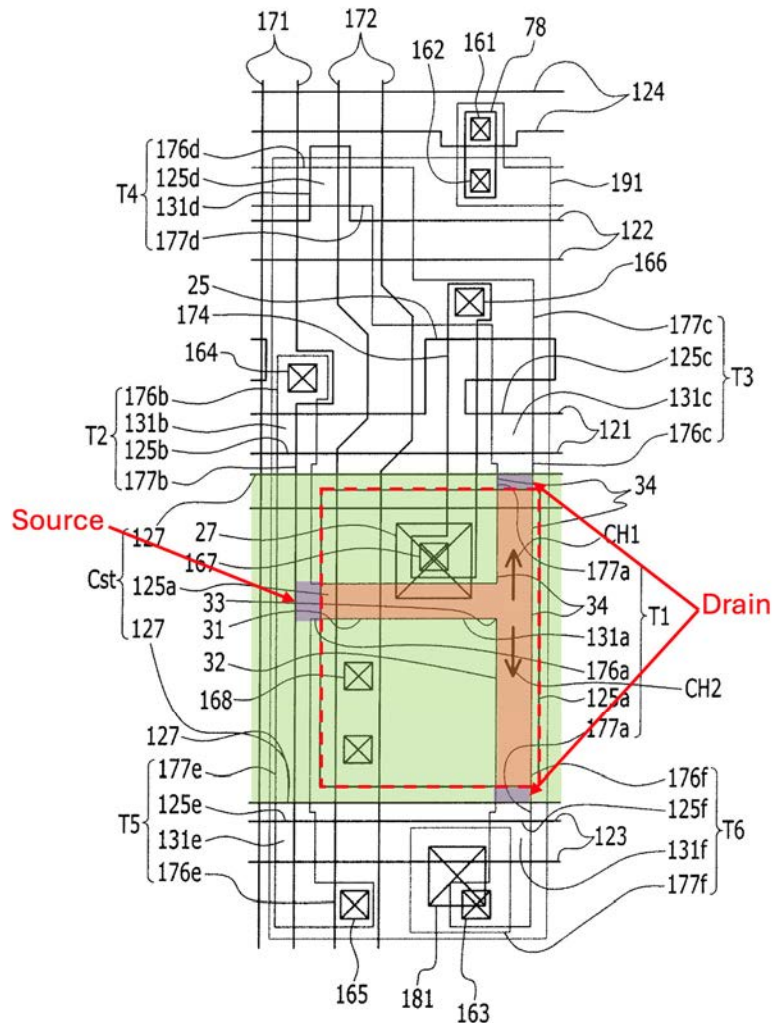
274. Accordingly, limitation 8[a] is disclosed by Kim-923.

7. Claim 9: "... wherein the first shield layer fully overlaps the part of one of the source area and the drain area of the first semiconductor."

275. In my opinion, Kim-923 teaches or suggests Claim 9.

276. Kim-923 discloses this limitation, as evident from Figs. 3 and 8, shown in annotated form below, where second storage capacitor plate 127 (green) ("first shield layer") extends beyond the boundaries of gate electrode 125a, and fully overlaps "the part of one of the source area and the drain area of the first semiconductor" (i.e., the purple-colored areas, and where the channel is the orange-colored area). See 1[e], above.





277. Accordingly, Claim 9 is disclosed by Kim-923.

8. Claim 10

- a. 10[a]: "The display apparatus of claim 1, wherein the first signal line extends in a first direction, and"**

278. In my opinion, Kim-923 teaches or suggests limitation 10[a].

279. Kim-923 discloses that data line 171 (“first signal line”) extends in a first direction as indicated by the red arrow in annotated Fig. 8 below. Kim-923, Fig. 8.

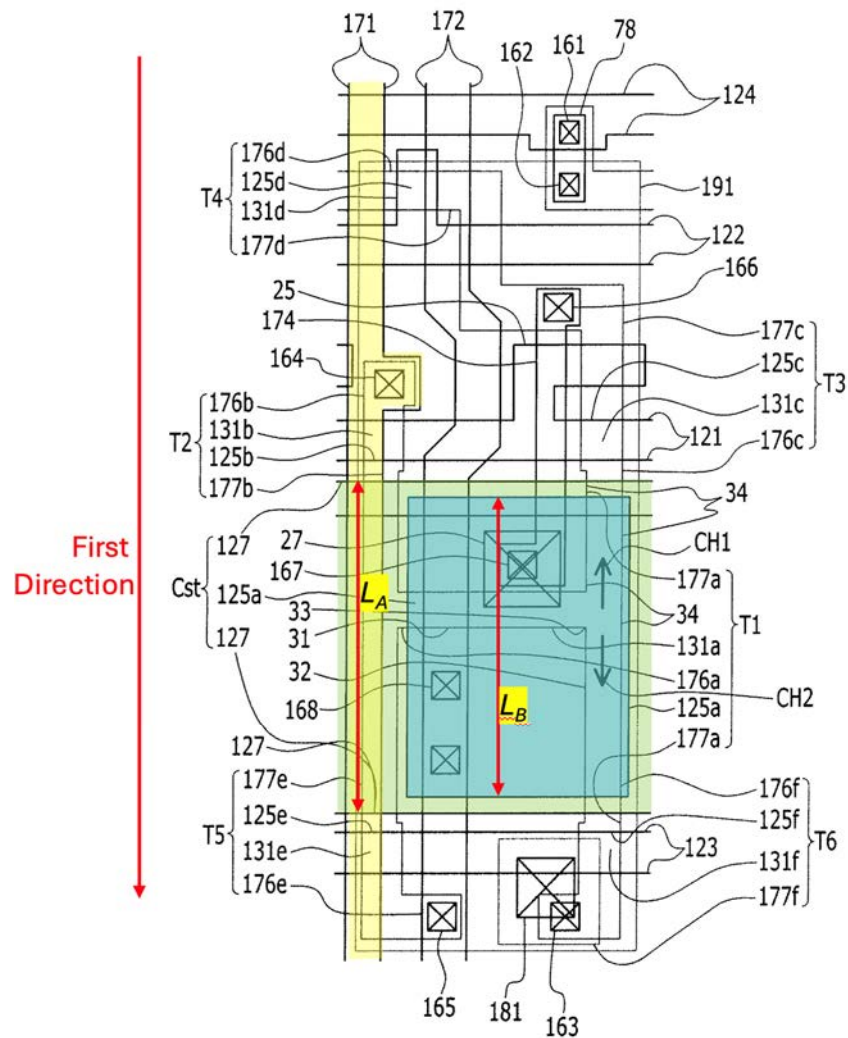


Fig. 8

280. Accordingly, limitation 10[a] is disclosed by Kim-923.

- b. 10[b]: "wherein a length along the first direction of an [[the]] overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction."**

281. In my opinion, Kim-923 teaches or suggests limitation 10[b].

282. Kim-923 discloses that "a length along the first direction of an [[the]] overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction."

283. As shown in annotated Fig. 8 of Kim-923 above, a length of the overlapped area of second storage capacitor plate 127 ("first shield layer" shown in green) with data line 171 ("first signal line" shown in blue), denoted by L_A , is longer along the first direction than the length of driving gate electrode 125a ("first electrode layer" shown in blue), denoted by L_B .

284. Accordingly, limitation 10[b] is disclosed by Kim-923.

9. Claim 20

- a. 20[a]: "The display apparatus of claim 3, further comprising a fifth thin-film transistor comprising a fifth semiconductor, one end of the fifth semiconductor being connected to the one end of the first semiconductor and the one end of the second semiconductor, and the other end of the fifth semiconductor being connected to a first voltage line,"**

285. In my opinion, Kim-923 teaches or suggests limitation 20[a].

286. Kim-923 discloses “a fifth thin-film transistor” as TFT T5 shown in annotated Fig. 1 below. Kim-923, Fig. 1. As discussed in limitation 1[a] and Claim 3, Kim-923 discloses a semiconductor for each of its transistors, including T5.

287. Kim-923 also discloses that the drain of T5 (“one end of the fifth semiconductor”) is connected to the source of T1 (“the one end of the first semiconductor”), as shown in annotated Fig. 1 below, labeled “A.”

288. Kim-923 also discloses that the drain of T5 (“one end of the fifth semiconductor”) is connected to the drain of T2 (“the one end of the second semiconductor”), as shown in annotated Fig. 1 below, labeled “B.”

289. Kim-923 also discloses that the source of T5 (“the other end of the fifth semiconductor”) is connected to driving voltage line 172 (“first voltage line”)⁴, as shown in annotated Fig. 1 below, labeled “C.”

⁴ For Claim 20, the “first signal line” is mapped to only data line 171 of Kim-923.

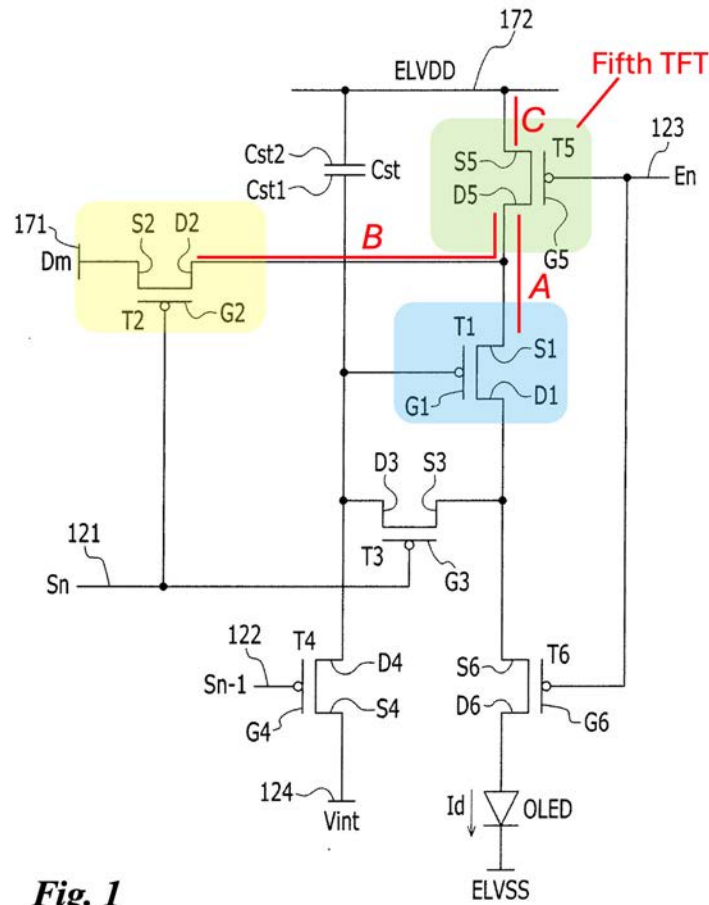


Fig. 1

290. I have illustrated the connectivity through the semiconductor layer in Fig. 3, which has been annotated below. As shown therein, T5's drain (177e) is connected to T1's source and to T2's drain (177b), and T5's source (176e) is connected to voltage line 172 through connector 165. Id., ¶93.

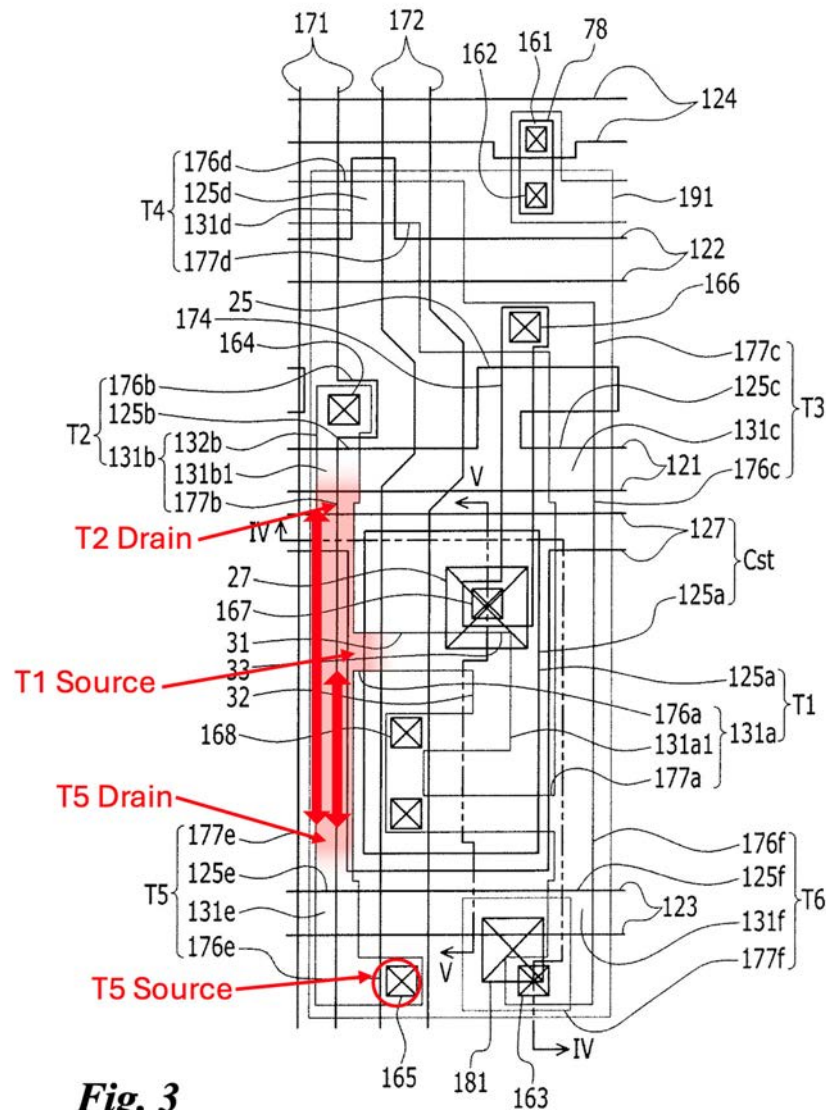


Fig. 3

291. Furthermore, Kim-923 also explicitly explains the connections: “A gate electrode G5 of the operation control thin film transistor T5 is coupled to the light emission control line 123, a **source electrode S5 of the operation control thin film transistor T5 is coupled to the driving voltage line 172**, and a **drain electrode D5 of the operation control thin film transistor T5 is coupled to the source electrode**

S1 of the driving thin film transistor T1 and the drain electrode S2 of the switching thin film transistor T2.” Kim-923. ¶67.

292. Accordingly, limitation 20[a] is disclosed by Kim-923.

b. 20[b]: "wherein the first voltage line in the same layer as the first signal line and connected to the second electrode layer."

293. In my opinion, Kim-923 teaches or suggests limitation 20[b].

294. Kim-923 discloses that driving voltage line 172 (“first voltage line” shown in green) is “in the same layer as the first signal line” (data line 171, shown in red). Annotated Fig. 4 shows that driving voltage line 172 and data line 171 are in the same layer. Kim-923, ¶1111, Fig. 4.

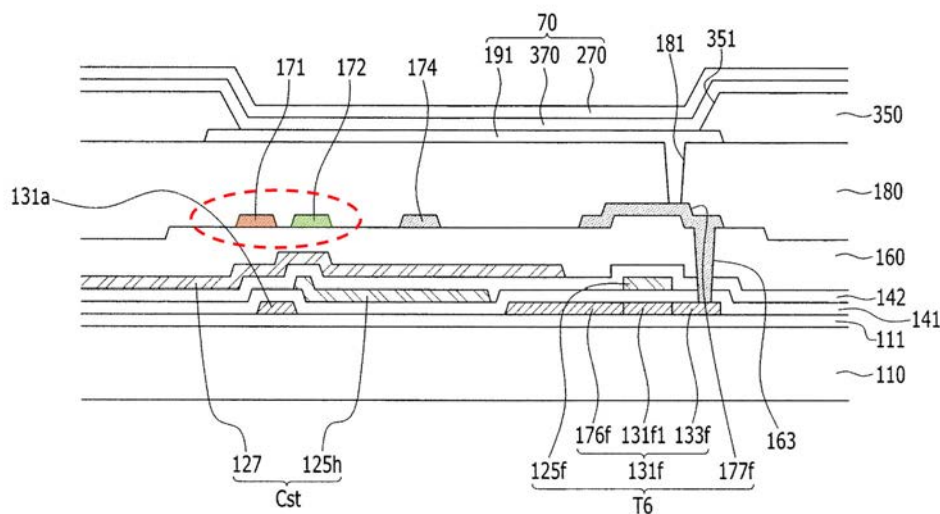


Fig. 4

295. Kim-923 discloses that driving voltage line 172 (“first voltage line”) is “connected to the second electrode layer” because driving voltage line 172 is

connected to second storage capacitor plate 127, labeled Cst2 in annotated Fig. 1 below. In my opinion, Kim-923 makes clear that Cst2 is the same as second storage capacitor plate 127: “The storage capacitor Cst includes a first storage capacitor plate 125h and a second storage capacitor plate 127.” Kim-923, ¶86.

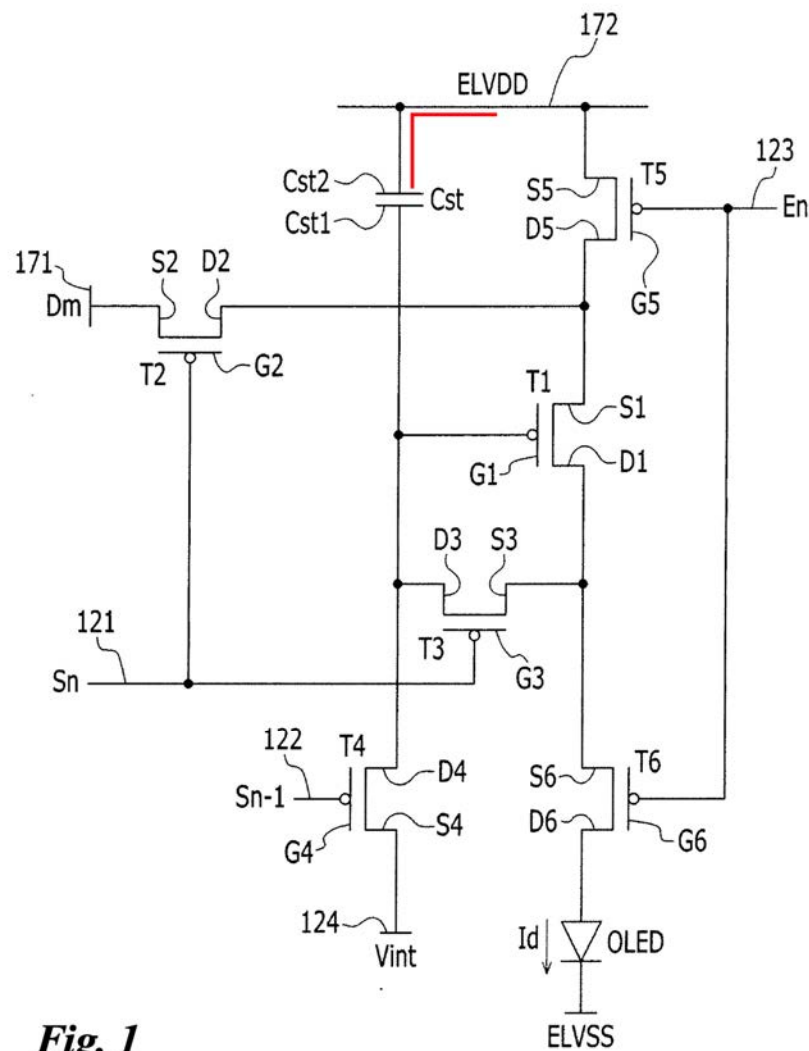


Fig. 1

296. Accordingly, limitation 20[b] is disclosed by Kim-923.

10. Claim 21

- a. 21[a]: “The display apparatus of claim 20, further comprising a fourth shield layer in a layer between the first signal line and the fifth semiconductor,”**

297. In my opinion, Kim-923 teaches or suggests limitation 21[a].

298. Kim-923 teaches a “fourth” shield layer in a layer between the first signal line and the fifth semiconductor. Specifically, I note that the “fourth” shield layer is a portion of the second storage capacitor plate 127, as I have shown below in annotated Fig. 3, in which the fourth shield layer is outlined by the red rectangle (or a portion thereof). Kim-923, Fig. 3. As I also explained in Ground 1A, the “fourth” shield layer can also be construed as only a portion of the red rectangle that is shown in Fig. 3 (and Fig. 8). Furthermore, it is my opinion that the “fourth” shield line is in a layer between line 171 (“first signal line”) and T5’s semiconductor because it is part of second capacitor plate 127 with the same positioning. §VIII.C.2.f.

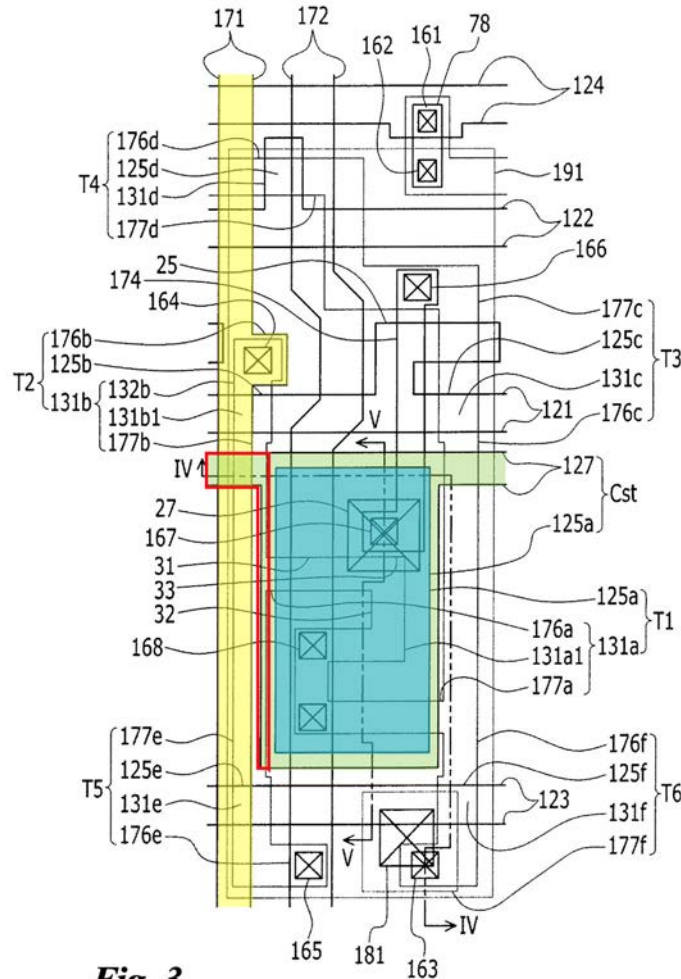


Fig. 3

299. Kim-923 includes another embodiment, shown in Fig. 8, that has a larger top capacitor plate 127 compared to the Fig. 3 embodiment, and also includes a fourth shield layer (again, indicated by a red rectangle, or a portion thereof) defined as part of second storage capacitor plate 127. It is my opinion that while this embodiment is not identical to the embodiment shown in Fig. 3, the same analysis with respect to Claims 21-23 applies to the Fig. 8 embodiment, and a POSITA would have found the use of a larger capacitor plate obvious. See Claim 8 discussion.

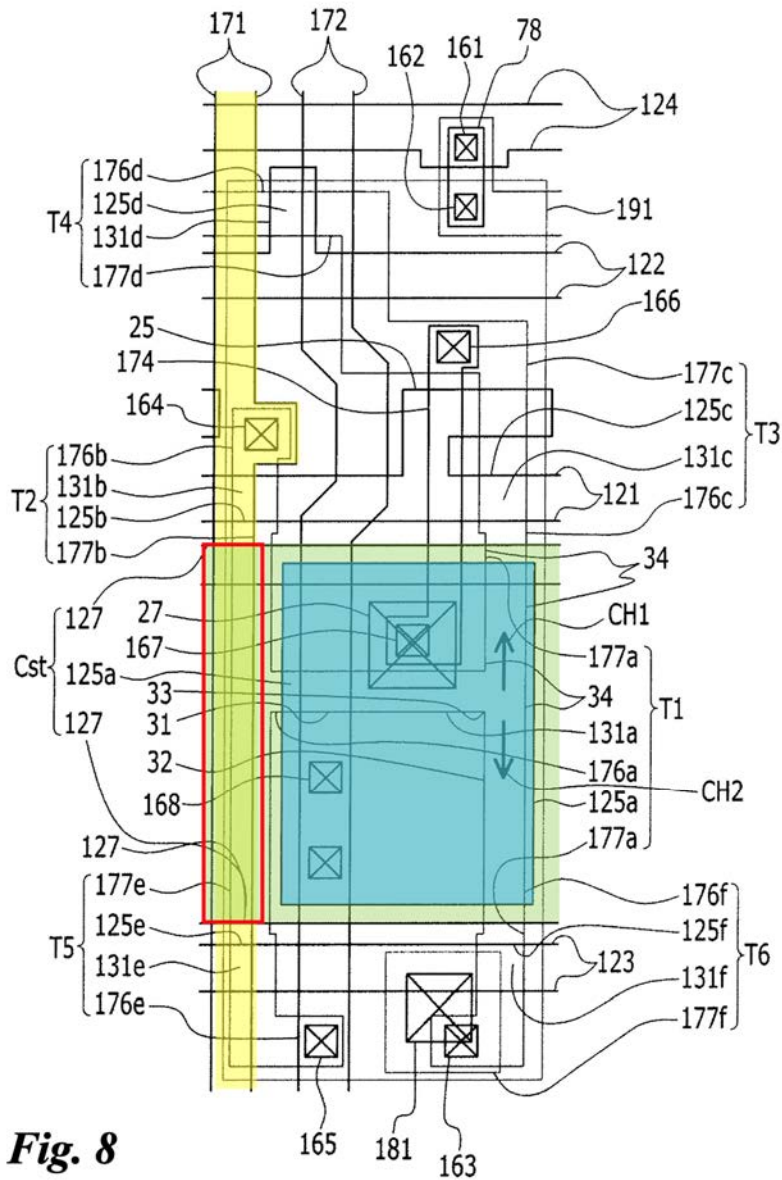


Fig. 8

300. As discussed above with respect to Ground 1A, Claim 21, limitation 21[a], identifying a portion of a metal component as the shield layer is consistent with the '015 Patent. *See* §VIII.A.10.a.

301. Accordingly, Kim-923 discloses limitation 21[a].

- b. 21[b]: “wherein the fourth shield layer overlaps a part of semiconductor between the channel area of the first semiconductor, the channel area of the second semiconductor, and the channel area of the fifth semiconductor.”**

302. In my opinion, Kim-923 teaches or suggests limitation 21[b].

303. With reference to annotated Figs. 3 and 8 above, and annotated portions of those figures below, it is my opinion that the fourth shield layer overlaps a portion between the channel area of the first semiconductor, the channel area of the second semiconductor, and the channel area of the fifth semiconductor. The channel area of a TFT corresponds to semiconductor region under the TFT’s gate electrode. As shown above in annotated Figs. 3 and 8, the fourth shield (red rectangle, or a portion thereof) overlaps the semiconductor region between the gate electrode of T1 (channel area of first semiconductor), gate electrode of T2 (channel area of second semiconductor) and gate electrode of T5 (channel area of fifth semiconductor). The overlapped semiconductor region is also illustrated below in red in partial Figs. 3 and 8.

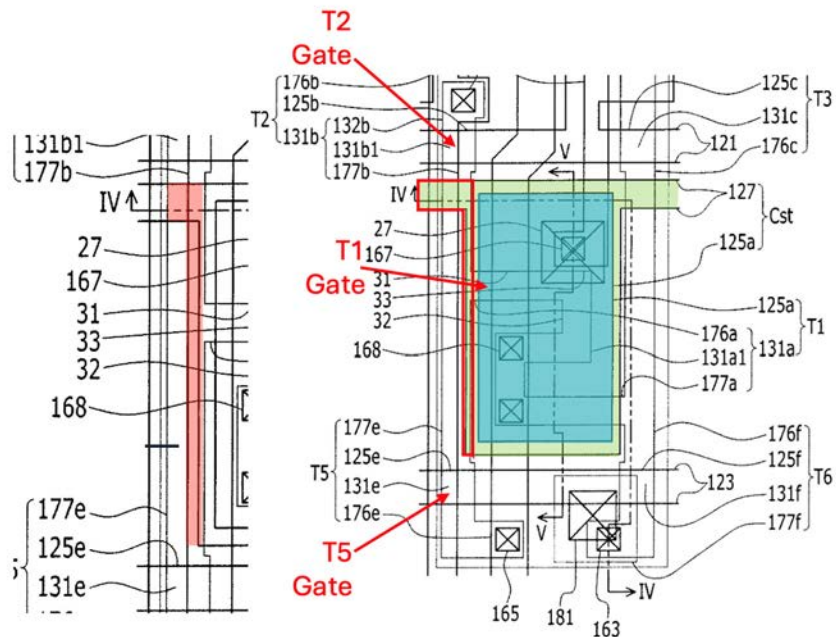


Fig. 3 (Annotated, Partial)

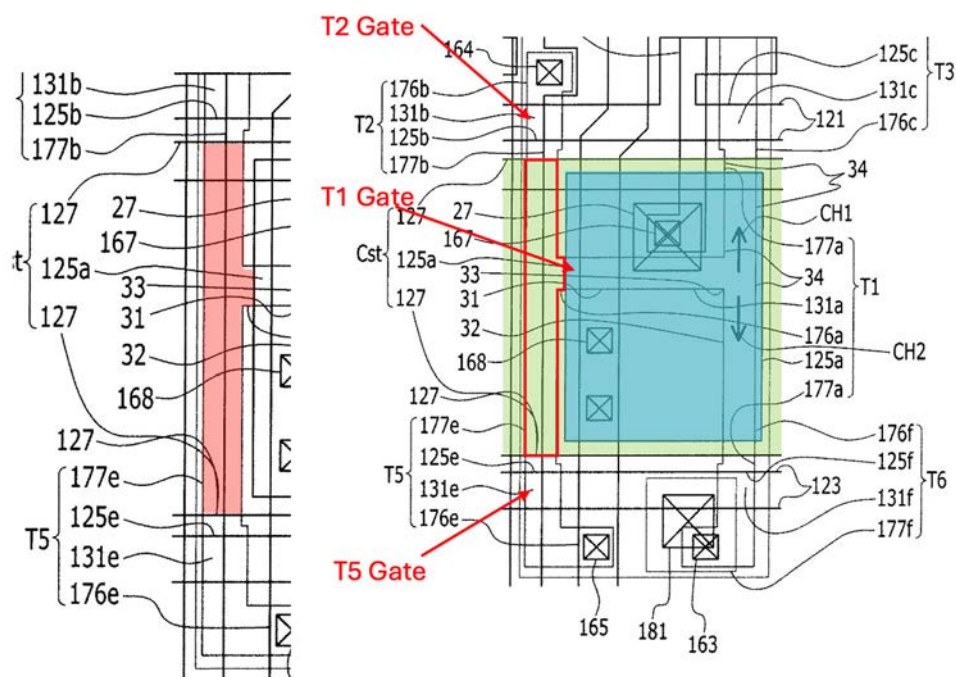


Fig. 8 (Annotated, Partial)

304. Accordingly, limitation 21[b] is disclosed by Kim-923.

11. Claim 22: “The display apparatus of claim 21, wherein the fourth shield layer is a part of the second electrode layer.”

305. In my opinion, Kim-923 teaches or suggests Claim 22.

306. As I have explained above with respect to limitation 21[a], the fourth shield layer is part of the second storage capacitor plate 127, which is in the second electrode layer as described above with respect to Claim 2. Thus, the fourth shield layer is part of the second electrode layer.

307. Accordingly, Claim 22 is disclosed by Kim-923.

12. Claim 23

308. In my opinion, Kim-923 teaches or suggests Claim 23.

a. 23[a]: “The display apparatus of claim 22, further comprising a capacitor comprising a first capacitor plate and a second capacitor plate,”

309. See the discussions of Ground 2A, Claim 1, limitations 1[b] and 1[c] above, which describe a first storage capacitor plate 125h/gate electrode 125a, and a second storage capacitor plate 127, which together form the storage capacitor. Kim-923, ¶86. See §§VIII.A.2.c, VIII.A.2.d.

b. 23[b]: “wherein the first capacitor plate is a part of the first electrode layer, and the second capacitor plate is a part of the second electrode layer.”

310. See the discussions of Ground 2A, Claim 1, limitations 1[b] and 1[c] above, which describe that the first capacitor plate is in the first electrode layer and

the second capacitor plate is in the second electrode layer, as shown in Fig. 4 of Kim-923. See §§VIII.A.2.c, VIII.A.2.d.

311. Accordingly, Claim 23 is disclosed by Kim-923.

13. Claim 33

312. In my opinion, Kim-923 teaches or suggests Claim 33.

a. 33[pre]: "A display apparatus comprising:"

313. See the discussion of Ground 2A, Claim 1, limitation 1[pre] above.

b. 33[a]: "a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;"

314. See the discussion of Ground 2A, Claim 1, limitation 1[a] above.

c. 33[b]: "a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;"

315. See the discussion of Ground 2A, Claim 1, limitation 1[b] above.

d. 33[c]: "a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;"

316. See the discussion of Ground 2A, Claim 1, limitation 1[c] above.

e. 33[d]: "a first signal line over the second electrode layer; and"

317. See the discussion of Ground 2A, Claim 1, limitation 1[d] above.

- f. 33[e]: "a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor,"**

318. See the discussion of Ground 2A, Claim 1, limitation 1[e] above. Here, element 127 in Kim-923's Fig. 8 embodiment forms the "first shield layer."

319. Accordingly, limitation 33[e] is disclosed by Kim-923.

- g. 33[f]: "wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line,"**

320. See the discussion of Ground 2A, Claim 2 above.

- h. 33[g]: "wherein the first signal line extends in a first direction, and**

321. See the discussion of Ground 2A, Claim 1, limitation 10[a] above.

- i. 33[h]: "wherein a length along the first direction of the overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction."**

322. See the discussion of Ground 2A, Claim 1, limitation 10[b] above.

323. Accordingly, Claim 33 is disclosed by Kim-923.

D. Ground 2B: The combination of Kim-923 and Moon renders Claims 6-7, 15-19 and 24-27 obvious.

1. Summary of Moon

324. Moon relates to thin-film transistors and OLED displays. Moon, ¶3. More particularly, Moon addresses the problem of "pixels may have a problem in

that light at lower luminance than desired is generated” and a pixel “fails to represent the image with desired luminance.” *Id.*, ¶26. Each pixel in Moon’s OLED display includes a driving circuit that includes 6 transistors 2 capacitors (6T2C) that are connected to voltage lines and data lines, as illustrated in Fig. 3. *Id.*, ¶42, Fig. 3. Driving transistor T1 is designed to have two current channels with different lengths to provide different current levels to storage capacitor Cst and to the OLED. *Id.*, ¶¶61-63.

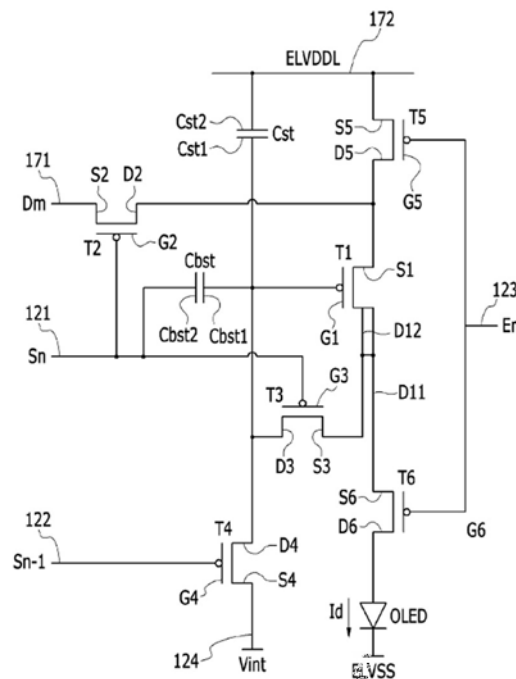


Fig. 3

325. Moon illustrates the locations of the transistors, capacitors, and voltage and signal lines in the layout view of Fig. 4. *Id.*, ¶¶25, 68-84, Fig. 4. For example, Fig. 4 (annotated below) illustrates T4 (the initialization TFT – red oval), identifying

its two gates (G4), source (S4) and drain (D4), and voltage line 124 (the initialization power line – green color) that overlaps T4. *Id.*, ¶¶48, 54, 79, 90, Fig. 4.

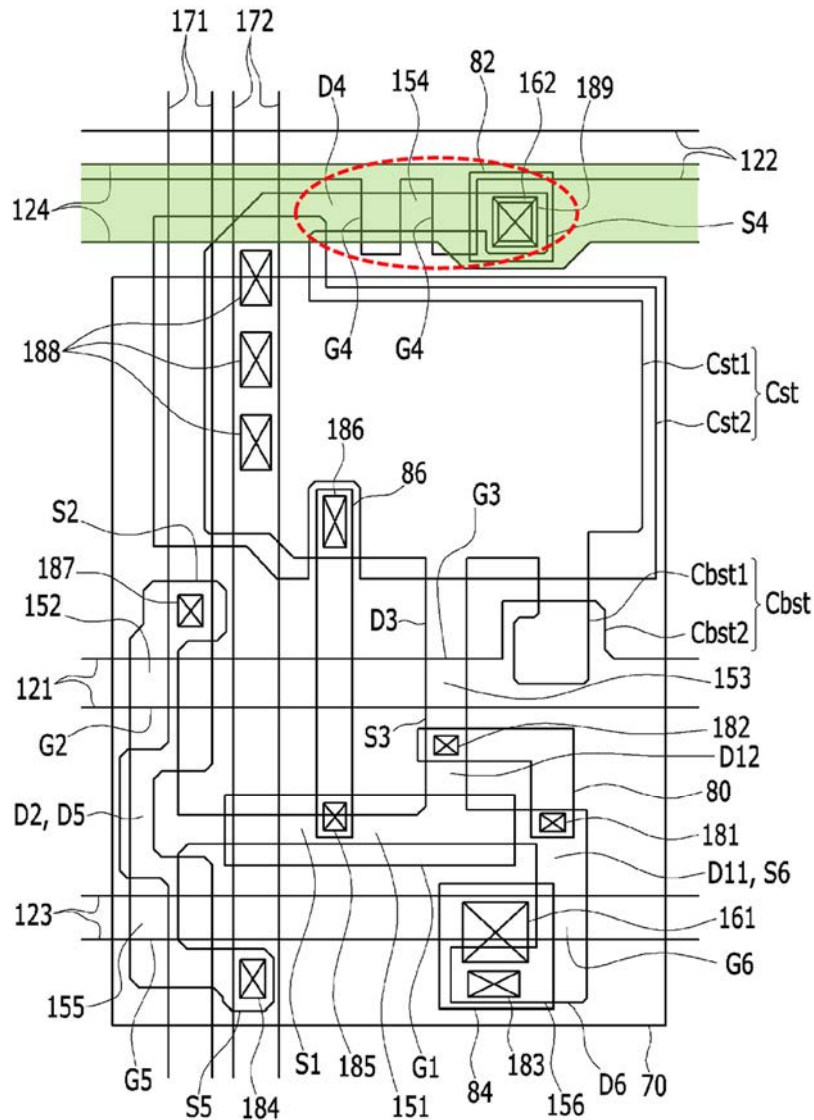


Fig. 4

2. Motivation to Combine Kim-923 and Moon

326. In my opinion, there are several reasons that motivate combining the teachings of Kim-923 and Moon.

327. Both references relate to OLED display devices that utilized TFTs, and particularly, six TFTs arranged in a typical OLED driving configuration (Kim-923, ¶¶3, 60, Fig. 1; Moon, ¶¶3, 42, Fig. 3) and strived to improve the operations of OLED displays. Kim-923, ¶9; Moon, ¶26. In my opinion, due to at least the two references being in the same specific technical area, a POSITA would have recognized that the teachings of Han can be used to complement the Kim-923 circuit configuration.

328. It is my opinion that a POSITA would have been motivated to apply the implementation of a multi-gated TFT and the relocation of a voltage line in the pixel layout to Kim-923's OLED pixel to yield the predictable results of reducing leakage current, simplifying design, and having a smaller footprint. Furthermore, there would have been a reasonable expectation of success, because using multi-gated TFTs in display circuits was well-known by 2014, as evidenced by the teachings of Moon and other known prior-art references such as Kim-544, Shin, Tang, Kim-033, and Hong (EX1021-EX1023, EX1025, EX1027).

329. I will provide additional explanations regarding the Kim-923–Moon combination in connection with claim limitations below.

3. Claim 24

330. In my opinion, Kim-923 in combination with Moon teaches or suggests Claim 24.

a. 24[pre]: “A display apparatus comprising:”

331. See the discussion of Ground 2A, Claim 1, limitation 1[pre] above.

Kim-923 relates to a display apparatus.

b. 24[a]: “a first thin-film transistor comprising a first semiconductor;”

332. See the discussion of Ground 2A, Claim 1, limitation 1[a] above. Kim-923 discloses a first TFT comprising a first semiconductor.

c. 24[b]: “a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;”

333. See the discussion of Ground 2A, Claim 1, limitation 1[b] above.

d. 24[c]: “a first signal line over the first electrode layer;”

334. In my opinion, Kim-923 teaches or suggests limitation 24[c].

335. As I have explained in the discussion of Ground 2A, Claim 1, limitation 1[d], Kim-923 describes the first signal line over the second electrode layer. See §VIII.C.2.e. Claim 24 recites the first signal over the first electrode layer as opposed to the second electrode layer. However, Kim-923 describes line 171 (“first signal line” shown in yellow) over both the first electrode layer (125h shown in blue) and second electrode layer (127 shown in green), as shown in annotated Fig. 4 below. Kim-923, Fig. 4.

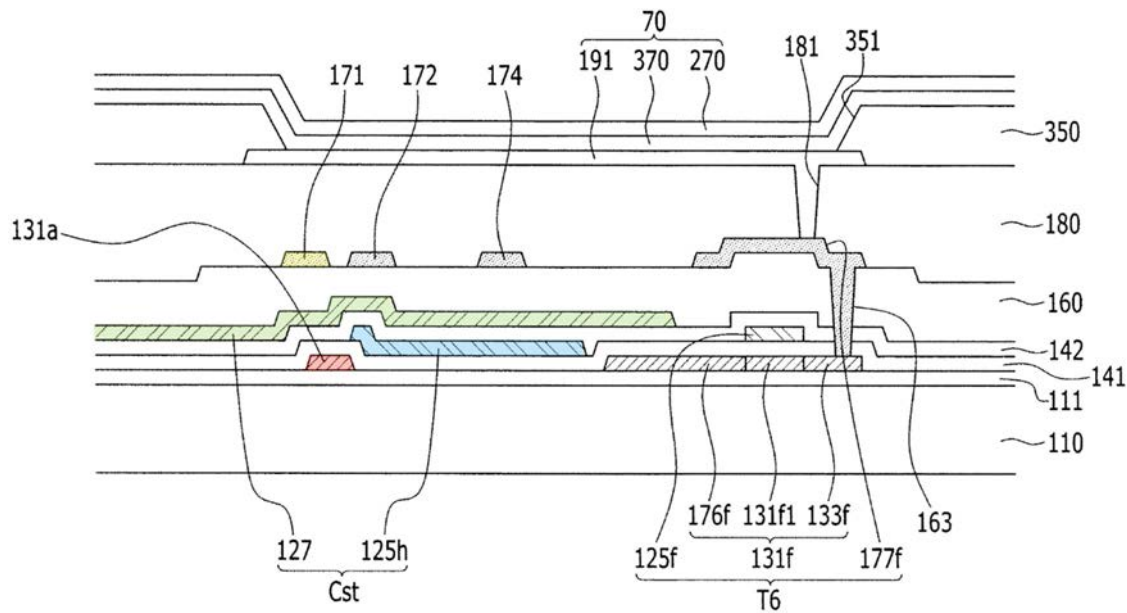


Fig. 4

336. Accordingly, limitation 24[c] is disclosed by Kim-923.

- e. **24[d]: “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line; and”**

337. In my opinion, Kim-923 teaches or suggests limitation 24[d].

338. Kim-923 discloses a second TFT, initialization transistor T4 formed along a semiconductor layer (“second semiconductor”): “The driving thin film transistor T1, the switching thin film transistor T2, the compensation thin film transistor T3, **the initialization thin film transistor T4**, the operation control thin film transistor T5, and the light emission control thin film transistor T6 are **formed**

along the semiconductor layer 131, and the semiconductor layer 131 is bent to have various shapes.” Kim-923, ¶¶79, 92.

[0092] The initialization thin film transistor T4 includes the initialization semiconductor layer 131d, the initialization gate electrode 125d, the initialization source electrode 176d, and the initialization drain electrode 177d. The initialization drain electrode 177d corresponds to the initialization drain region 177d doped with the impurity in the initialization semiconductor layer 131d. The initialization source electrode 176d is coupled through an initialization connection line 78 to the initialization voltage line 124. An end of the initialization connection line 78 is coupled through a contact hole 161 formed in the second gate insulating layer 142 and an inter-layer insulating layer 160 to the initialization voltage line 124, and another end of the initialization connection line 78 is coupled through the contact hole 162 formed in the gate insulating layer 141, the second gate insulating layer 142, and the interlayer insulating layer 160 to the initialization source electrode 176d.

339. Kim-923 further explains the connections of T4: “**A gate electrode G4 of the initialization thin film transistor T4 is coupled to the prior scan line 122, a source electrode S4 of the initialization thin film transistor T4 is coupled to the initialization voltage line 124, and a drain electrode D4 of the initialization thin film transistor T4 is coupled to the end Cst1 of the storage capacitor Cst, the drain electrode D3 of the compensation thin film transistor T3, and the gate electrode G1 of the driving thin film transistor T1.**” Kim-923, ¶66. As discussed in VIII.C.2.c., gate electrode G1 of TFT T1 is in the first electrode layer. *See also*

annotated Fig. 1, below, showing connections of the drain of T4 (“one end of the second semiconductor” D4) to the gate of T1 (G1) and storage capacitor plate Cst1 (red line labeled A) (“first electrode layer”), and connection of the source of T4 (“the other end of the second semiconductor”) to initialization voltage line 124 Vint (red line labeled B) (“a voltage line”).

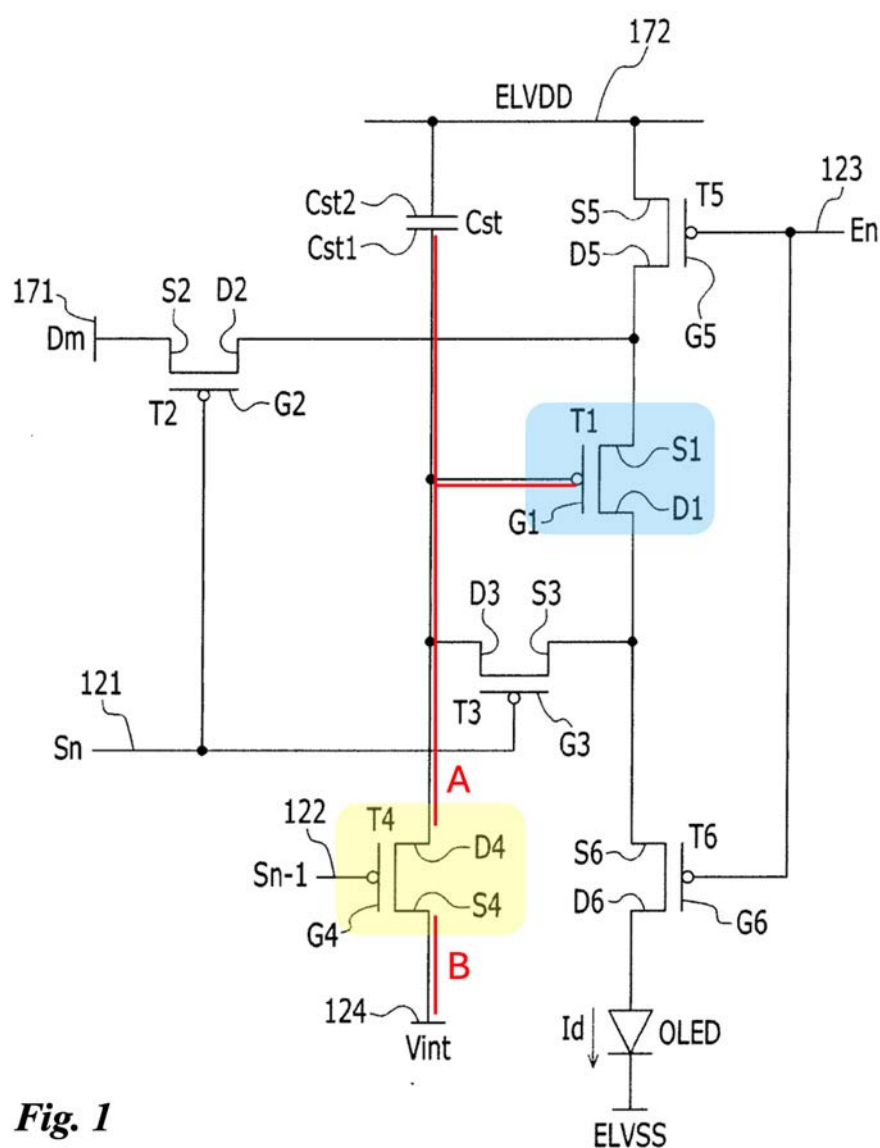


Fig. 1

340. Kim-923 explains that T4 is formed along a portion of semiconductor 131 (portion 131d for T4) and includes source/drain electrodes formed as doped regions of the semiconductor. Kim-923 ¶¶79, 85, 92. Therefore, the Fig. 1 connections of T4's source/drain are through the doped region of semiconductor 131 that forms the drain/source electrodes. *Id.*, see also Figs. 2 and 3 (annotated below), showing T4's drain (177d) connecting to T1's gate/lower storage capacitor plate Cst1 (125a) through contact holes 166, 167 and connection line 164 (*id.*, ¶112), and connection of T4's source (176d) to initialization voltage line 124 through contact holes 161, 162 and connection line 78. *Id.*, ¶92. Kim-923's Fig. 2 shows three adjacent OLED pixels, illustrating line 124 (Vint) connecting to T4's source in adjacent pixel.

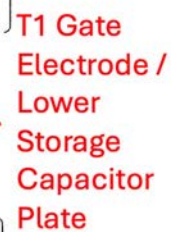


Fig. 3

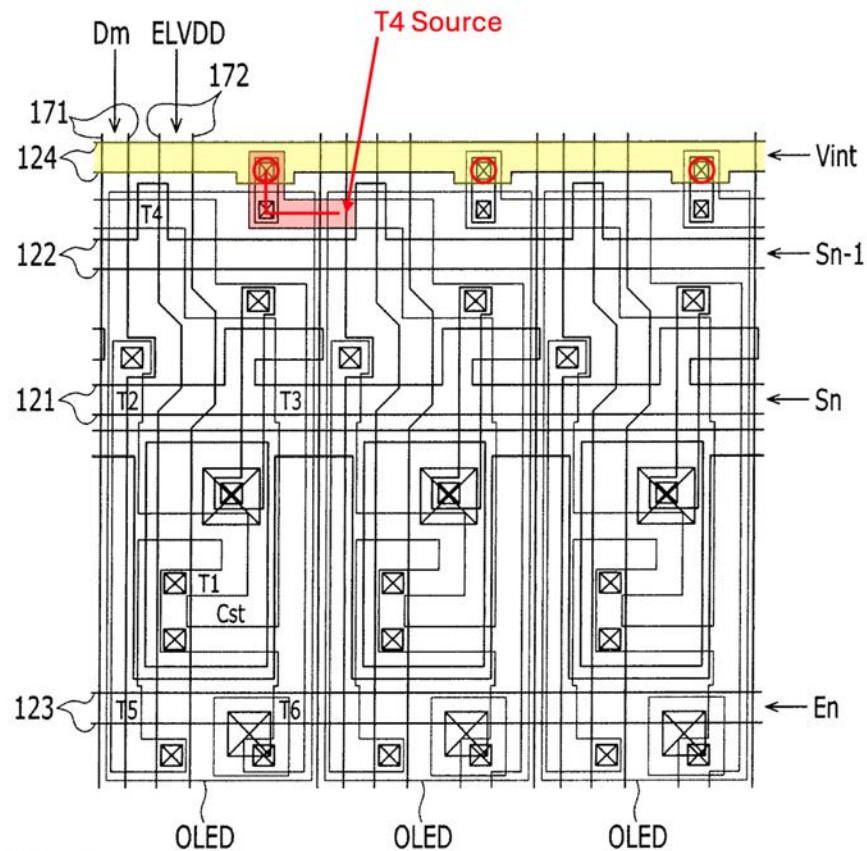


Fig. 2

341. Accordingly, limitation 24[d] is disclosed by Kim-923.

- f. **24[e]: “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.”**

342. In my opinion, Kim-923 in combination with Moon teaches or suggests limitation 24[e].

343. Kim-923 teaches that its data line 171 is in a layer above initialization power line 124. In my opinion, a POSITA would have known this because Kim-923's Fig. 4, annotated below, shows that second storage capacitor plate 127 (green)

is in a layer above semiconductor layer 131 (red) and below data line 171 (yellow). As Kim-923 explains, “**The second storage capacitor plate 127 ... is formed on the same layer as the initialization voltage line 124.**” Kim-923, ¶88. Therefore, line 124 is also above semiconductor layer of T4 (“second semiconductor”) and below signal line 171 (“first signal line.”)

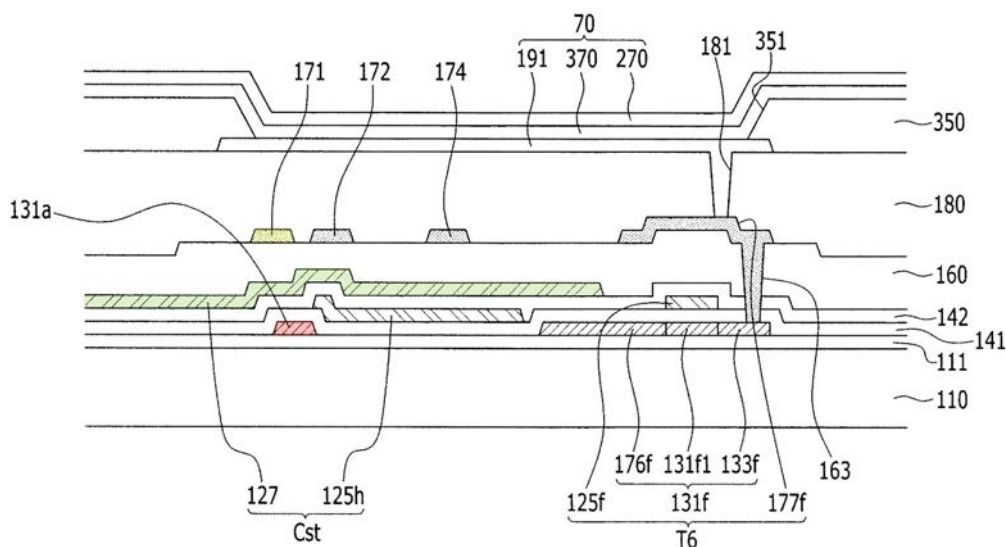


Fig. 4

344. Kim-923 does not show a shield layer between data line 171 (“first signal line”) and the second semiconductor. Fig. 3 of Kim-923 shows the previous scan line 122 overlapping the semiconductor at two locations but Kim-923 does not explicitly identify TFT T4 as a dual-gate TFT. However, Moon clearly discloses these limitations.

345. Moon discloses an initialization power line 124, as shown in annotated Fig. 4 below (green), that overlaps Moon’s double-gated T4 transistor (red dashed

circles). Moon, ¶¶43, 48. Fig. 4 shows that initialization power line 124 overlaps the entire T4, including a part between the first channel area and second channel area of the semiconductor portion of T4. *Id.*, Fig. 4. Specifically, I have annotated Fig. 4 below to illustrate T4's two gate electrode locations, both labeled G4 by Moon (annotated with red dashed circles), that are formed at locations where the previous scan line 122 (blue) overlaps the semiconductor layer. *Id.*, ¶73: "...the previous scan line 122 has the gate electrode G4 overlapping the semiconductor 154 of the initialization transistor T4."

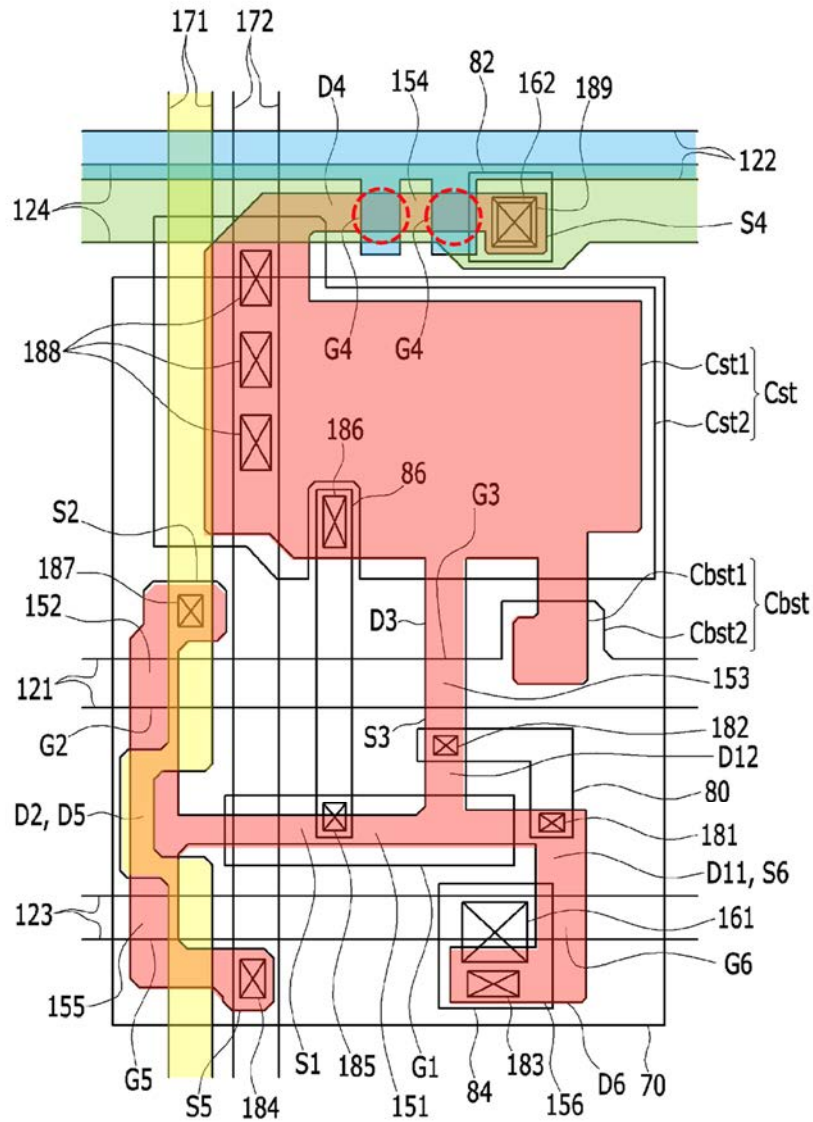


Fig. 4

346. In the Kim-923–Moon combination, Kim-923’s TFT T4 would have a multi-gated TFT structure as confirmed by Moon, and the initialization voltage line 124 of Kim-923 would also be moved to overlap TFT T4, as also taught by Moon. A rudimentary sketch of the proposed modification to Kim-923 is shown in the

figure below. Here, I note that making such modifications was well within the skills and capabilities of a POSITA given that a typical design of physical layout configurations involve rearranging the location or size of parts. If an improved attribute recognized in the art is desired for a design, the parts providing the improvement can be relocated to provide that improvement simply by re-laying out the TFT circuit as a routine part of such a design process.

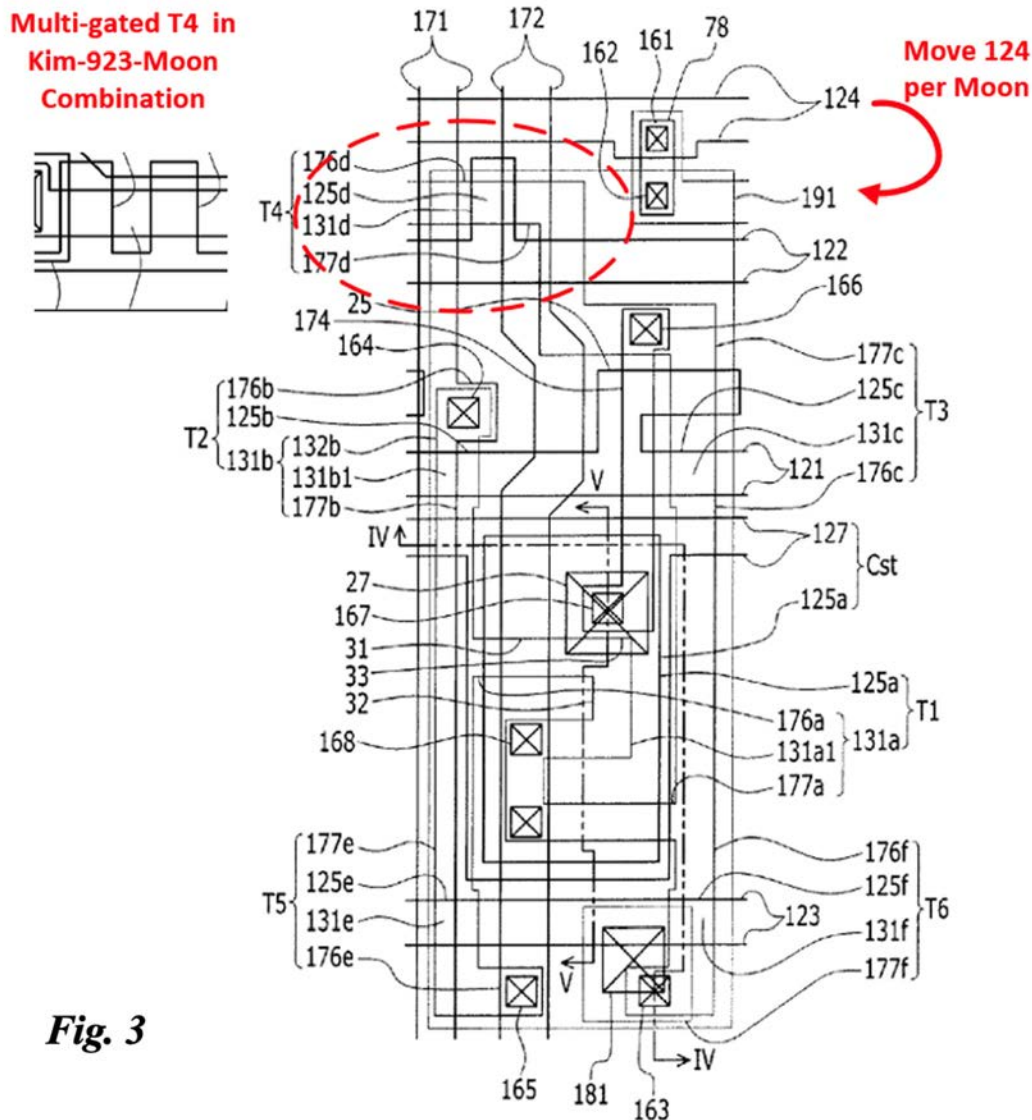


Fig. 3

347. In my opinion, a POSITA would have been motivated to combine Kim-923 with Moon because, in addition to the reasons articulated in §VIII.D.2, the modifications would have improved the operation of Kim-923's display device. Specifically, I note that having a multi-gated TFT structure would have reduced leakage current, which was well-known in the art, was routinely done in OLED drive

circuits (*see generally* Kim-544, Shin, Tang, Kim-033 – EX1021-EX1023, EX1025), and also acknowledged by Kim-923 in connection with TFT T3. Kim-923, ¶91 (“[t]he compensation gate electrode 125c prevents a leakage current by forming a separate dual-gate electrode 25”); §VI.E.

348. Furthermore, it is my opinion that it would have been advantageous to move Kim-923’s initialization voltage line 124 down to overlap T4 because rearrangement of the initialization voltage line would have freed up the top section of the OLED pixel layout that only contained voltage line 124, and would have thus enabled the OLED pixel area to be made more compact (since compact circuit layouts are generally desirable to improve display resolution and circuit performance). The rearrangement of voltage line 124 (Vint) would have also made the circuit layout of Kim-923 simpler because the connection from Vint to the source of T4 would have been made by a simple “via” given that Vint would be overlapping T4. *Id.* This connection in Kim-923 (prior to modification) requires a connection line 78 and two contact holes 161, 162. Kim-923, ¶92. A reduction in the number of vias (or contact holes) will improve manufacturing yields by reducing the number of structures needed.

349. In my opinion, a POSITA would have had reasonable expectation of success because the initialization TFT T4 and initialization voltage line 124 of both

references performed similar operations in the OLED drive circuit (Kim-923, ¶¶71, 79; Moon, ¶48), the modifications were already described in Moon, and the changes to the circuit layout were routine tasks well within the capabilities of a POSITA. Here, I note that relocating components, positioning wires (lines), and the use of vias are standard tasks in a TFT circuit layout.

350. The combination renders limitation 24[e] obvious because, as explained above, initialization voltage line 124 of Kim-923 is at the same layer as top capacitor plate 127 (green layer annotated in Fig. 4 below), and thus would have been between data line 171 (yellow) and the semiconductor associated with T4 (red), i.e., portion 131d of semiconductor layer 131 that also includes 131a. The initialization voltage line would overlap “a part between a first channel area and a second channel area of the second semiconductor” because it would overlap T4 as shown in Moon and described above.

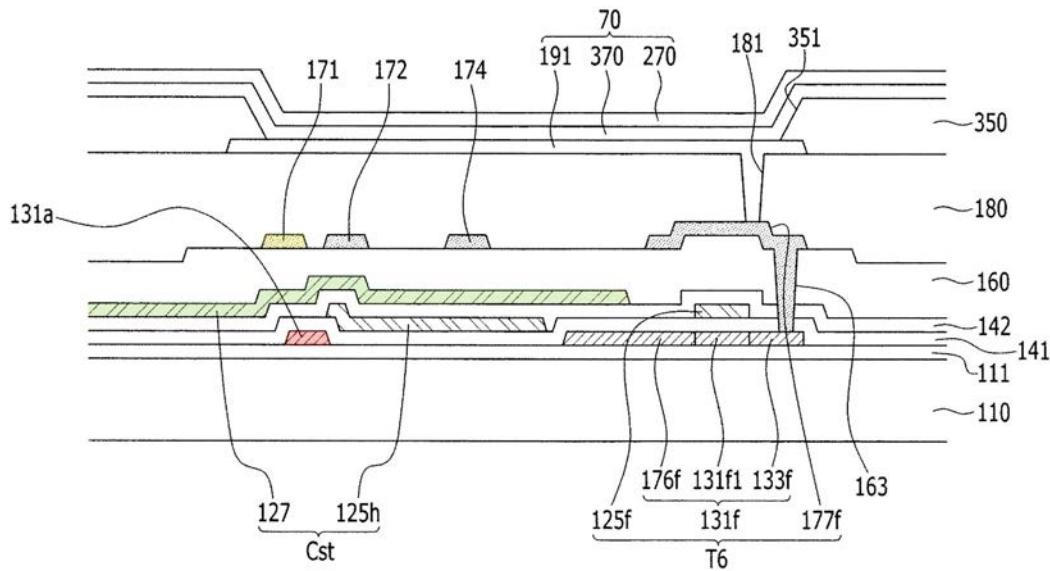


Fig. 4

351. Specifically, I note that initialization voltage line 124 would be a “shield layer” because it is connected to a constant voltage line (Vint) (Kim-923, ¶62) and forms a layer shielding the semiconductor of T4 from electrical noise associated with data line 171. In my opinion, this interpretation of a voltage line as a shield layer is consistent with the ’015 Patent, which explains that “*the second shield layer SD2 may be a part of the initialization voltage line 124.*” ’015 Pat., 13:47-48. Shields are generally connected to either a power line or ground line, i.e., a line that desirably has an unchanging voltage and is therefore suitable for shielding. Furthermore, and as I have discussed above, the use of voltage lines for shielding data lines was well known and obvious. See §VI.D.

352. Accordingly, limitation 24[e] is disclosed by Kim-923.

4. Claim 25

- a. 25[a] The display apparatus of claim 24, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and**

353. In my opinion, Kim-923 in combination with Moon teaches or suggests limitation 25[a].

354. As shown in annotated Fig. 4 of Moon above, Moon's T4 (second TFT) comprises a first gate electrode and a second gate electrode in the same layer, the first gate electrode overlaps the first channel area, and the second gate electrode overlaps the second channel area of the second semiconductor. Specifically, I note that Fig. 4 shows two gate electrodes—both labeled G4—formed at locations where previous scan line 122 overlaps the semiconductor. Moon, ¶73: “the previous scan line 122 has the gate electrode G4 overlapping the semiconductor 154 of the initialization transistor T4.”

355. In the Kim-923–Moon combination, T4 of Kim-923 would be modified and would include a similar configuration of Moon's T4 with two gates formed at locations where prior scan line 122 overlapped the semiconductor of T4, and each gate would overlap one section of the semiconductor associated with T4, as

explained in Claim 24. As I have previously discussed, dual-gate TFTs were well-known in the thin-film circuit art. *See* §VI.E.

356. Accordingly, limitation 25[a] is disclosed by Kim-923 in combination with Moon.

- b. 25[b] wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.**

357. In my opinion, Kim-923 in combination with Moon teaches or suggests limitation 25[b].

358. Kim-923 shows that prior scan line 122 (“second signal line”) crosses signal line 171 (“first signal line”), as shown in Kim-923’s Fig. 6 annotated below. In the Kim-923–Moon combination, prior scan line 122 would remain in the same location and form two gate electrodes (as shown in the rudimentary sketch in §VIII.D.3.f) based on the teachings of Moon, as discussed above in Claim 24 and 25[a]. Prior scan line 122 is in the same layer as the first electrode layer, i.e., the layer that includes the lower capacitor plate/gate electrode of T1. Kim-923 ¶105: **“...the prior scan line 122, which includes the initialization gate electrode 125d ... are formed on the first gate insulating layer 141.”** See also §VIII.C.2.c.

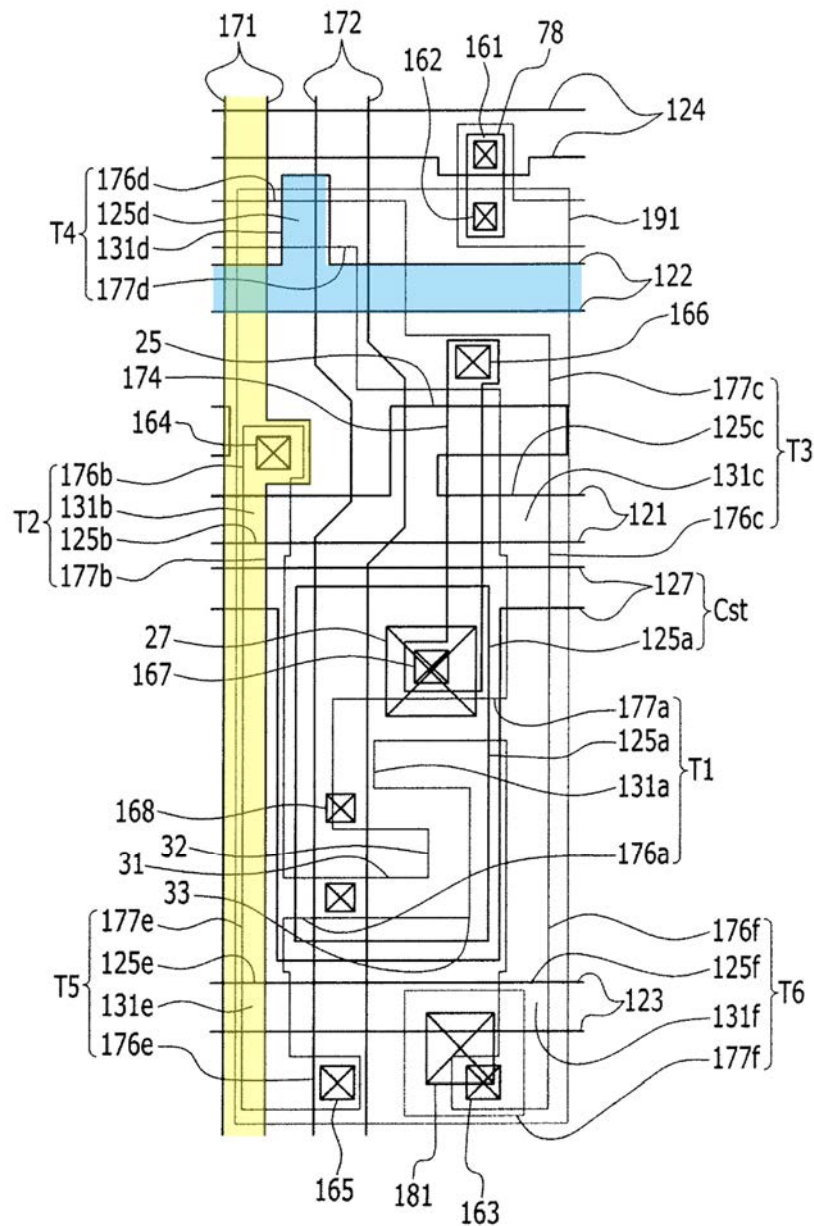


Fig. 6

359. Accordingly, limitation 25[b] is disclosed by Kim-923 in combination with Moon.

5. Claim 26: “The display apparatus of claim 24, wherein the shield layer is a part of the voltage line.”

360. See the discussion of Ground 2B, Claim 24, limitation 24[e] above. Kim-923 in combination with Moon teaches or suggests the shield layer is part of initialization voltage line 124 (“the voltage line”). See §VIII.D.3.f. As discussed above, power and ground lines naturally provide shielding if they are in suitable locations.

361. Accordingly, Kim-923 in combination with Moon discloses Claim 26.

6. Claim 27: “The display apparatus of claim 24, further comprising a connecting line connecting the one end of the second semiconductor and the first electrode layer and being in the same layer as the first signal line.”

362. In my opinion, Kim-923 in combination with Moon teaches or suggests Claim 27.

363. Kim-923 shows that one end of second semiconductor T4 is connected to the first electrode layer (e.g., the gate of T1 and capacitor plate Cst1), labeled A in annotated Fig. 1 of Kim-923 below.



364. Kim-923 describes using a connection member 174, which is in the same layer as data line 171, for implementing this connection: “[t]he first storage capacitor plate 125h of the storage capacitor Cst is coupled through the connection member 174 to the compensation drain electrode 177c and to the initialization drain electrode 177d.” Kim-923, ¶96. I note here that a connecting

line can simply be a metallic wire, via, or a doped portion of semiconductor that connects two active components or to an external signal.

365. As I have shown in annotated Fig. 3 of Kim-923 below, connection member 174 (yellow) connects the drain of T4, 177d, (“one end of the second semiconductor”) with capacitor plate/gate electrode 125a/125h (blue) (“first electrode layer”). Fig. 4 of Kim-923, also annotated below, shows that connection member 174 is in the same layer as data line 171 (“first signal line”).

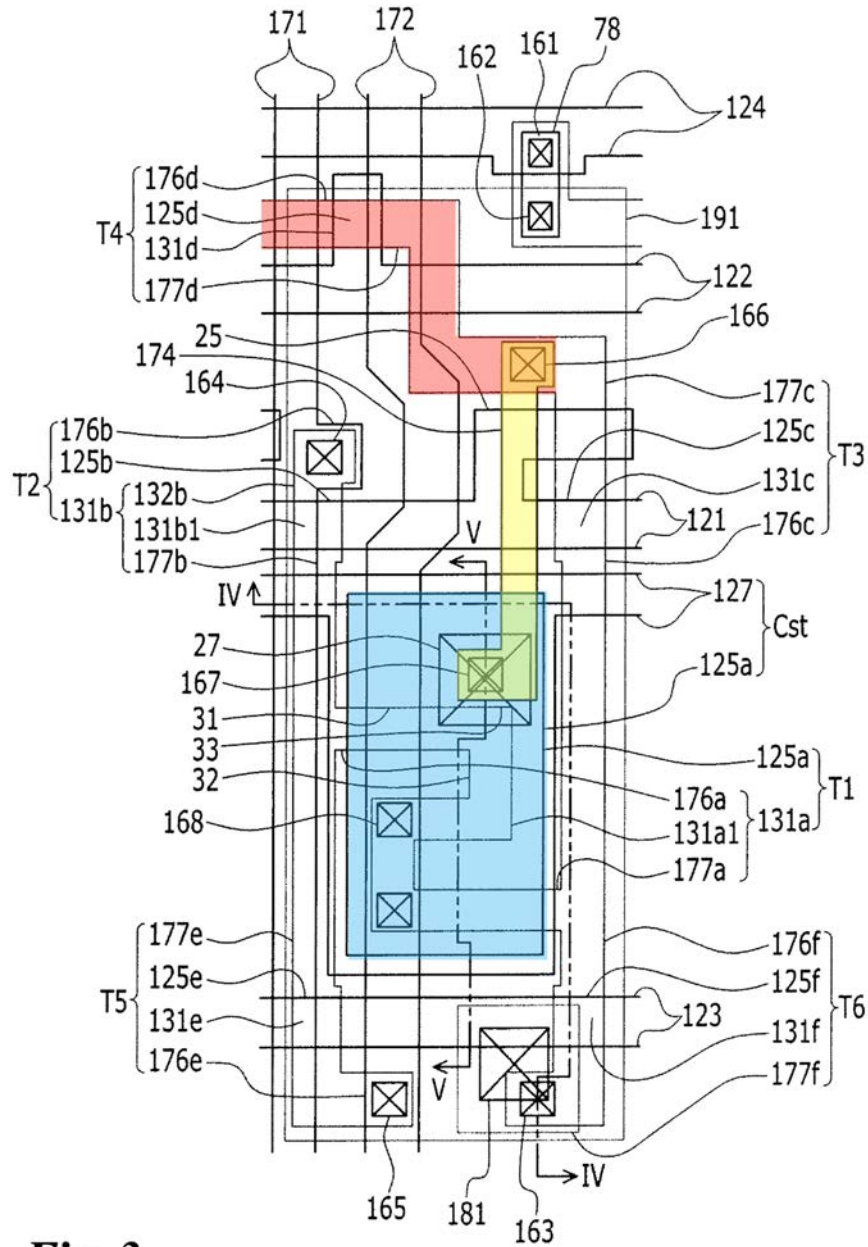
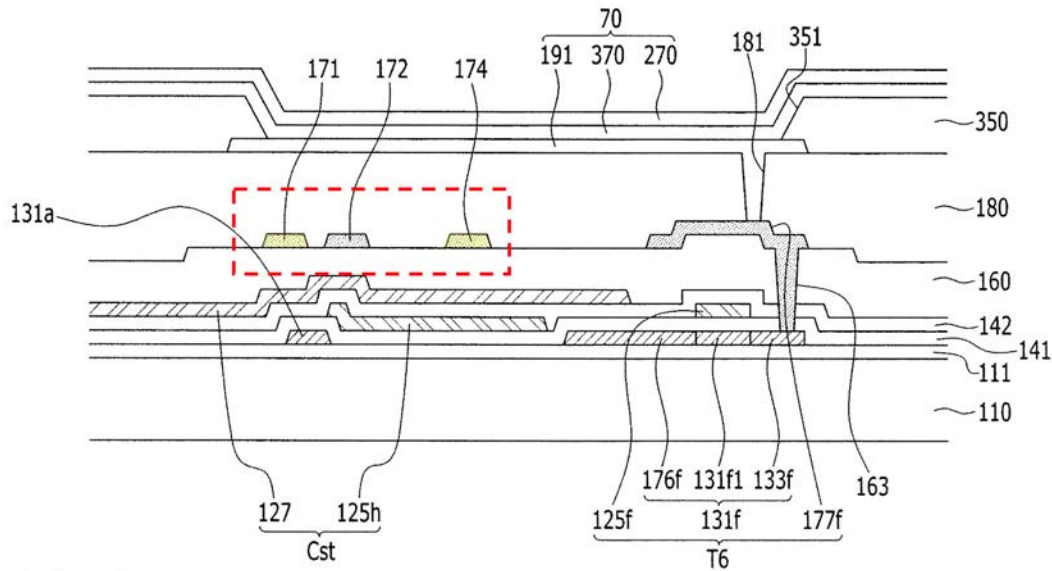


Fig. 3



366. Accordingly, Claim 27 is disclosed by Kim-923 in combination with Moon.

7. Claim 6

- a. 6[pre]: “The display apparatus of claim 1, further comprising:”**

367. As described above in Ground 2A, Kim-923 teaches or suggests the limitations of base Claim 1. See §VIII.C.2, *supra*.

- b. 6[a]: “a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and”**

368. See the discussion of Ground 2B, Claim 24, limitation 24[d] above. Kim-923 in combination with Moon teaches or suggests this limitation because the

“fourth semiconductor” is treated as a semiconductor in addition to the first semiconductor of Claim 1, and particularly as TFT T4 of Kim-923.

369. Claim 6 recites a “second voltage line,” which is equivalent to the “voltage line” recited in limitation 24[d], and is described in the combination to the initialization voltage line 124.

370. Accordingly, limitation 6[a] is disclosed by Kim-923 in combination with Moon.

- c. **6[b] “a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part of the fourth semiconductor.”**

371. See the discussion of Ground 2B, Claim 24, limitation 24[e] above. Kim-923 in combination with Moon teaches or suggests this limitation because the “third shield layer” over Claim 6 is equivalent to the “shield layer” recited in Claim 24 and is mapped to initialization voltage line 124 Vint in the Kim-923–Moon combination. Unlike limitation 24[e], this limitation merely requires the third shield layer overlap “a part” of the fourth semiconductor and does not recite a first and second channel area or specify a placement of the third shield layer with respect to a part between the first and second channel areas. In my discussion of limitation 24[e], I have explained that limitation of overlapping a part of the semiconductor is satisfied, and I reiterate that the fourth semiconductor can be any part of transistor T4 including the channel source and gate portions.

372. Accordingly, limitation 6[b] is disclosed by Kim-923 in combination with Moon.

8. Claim 7

- a. 7[pre]: “The display apparatus of claim 1, further comprising:”**

373. As described above in Ground 2A, Kim-923 teaches or suggests the limitations of base Claim 1. *See* §VIII.C.2, *supra*.

- b. 7[a]: “a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and”**

374. See the discussion of Ground 2B, Claim 6, limitation 6[a] above. Here, the fourth TFT and fourth semiconductor are mapped to TFT T4 and its corresponding semiconductor in the Kim-923-Moon combination. *See* §VIII.D.7.b.

- c. 7[b]: “a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part between a first channel area and a second channel area of the fourth semiconductor.”**

375. See the discussion of Ground 2B, Claim 24, limitation 24[e] above. Here, the third shield layer is equivalent to the “shield layer” recited in Claim 24 and is mapped to the initialization voltage line 124 in the Kim-923-Moon combination. *See* §VIII.D.3.f. As previously discussed, any of various different elements, if connected to a power or ground line, can serve as shields. *See* §VI.D.

376. Accordingly, Claim 7 is disclosed by Kim-923 in combination with Moon.

9. Claim 15

- a. 15[a]: “The display apparatus of claim 6, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer and overlapping the fourth semiconductor, and”**

377. See the discussion of Ground 2B, Claim 25, limitation 25[a] above. In the context of Claim 15, the fourth thin-film transistor is treated similar to the second TFT of Claim 25 and is mapped to TFT T4 in the Kim-923–Moon combination, and the fourth semiconductor is treated similar to the second semiconductor of Claim 25 and is mapped to the semiconductor associated with T4 in the combination.

378. Accordingly, limitation 15[a] is disclosed by Kim-923 in combination with Moon.

- b. 15[b]: “wherein the third shield layer is a part of the second voltage line and overlaps a part of the fourth semiconductor between the first gate electrode and the second gate electrode.”**

379. See the discussion of Ground 2B, Claim 24, and Claim 26 above. Herein, the third shield layer is treated similar to the shield layer of Claims 24 and 26, and the second voltage line is treated similar to the voltage line of Claims 24 and 26.

380. Accordingly, limitation 15[b] is disclosed by Kim-923 in combination with Moon.

10. Claim 16: “The display apparatus of claim 15, wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.”

381. See the discussion of Ground 2B, Claim 25, limitation 25[b] above. Herein, the third signal line of Claim 16 is treated similar to the second signal line of Claim 25 (mapped to the prior scan line 122 Sn-1 of Kim-923).

382. Accordingly, Claim 16 is disclosed by Kim-923 in combination with Moon.

11. Claim 17: “The display apparatus of claim 7, wherein the third shield layer is a part of the second voltage line.”

383. See the discussion of Ground 2B, Claim 26 above. Herein, the third shield layer is treated similar to second shield layer of Claim 26 and mapped to the initialization voltage line 124 Vint in the combination.

384. Accordingly, Claim 17 is disclosed by Kim-923 in combination with Moon.

12. Claim 18

- a. 18[a]: “The display apparatus of claim 7, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the fourth semiconductor, and the second gate electrode overlapping the second channel area of the fourth semiconductor, and”**

385. See the discussion of Ground 2B, Claim 25, limitation 25[a] above.

Herein, the “fourth” TFT is mapped to TFT T4 in the Kim-923–Moon combination.

In my opinion, the structure reflects the well-known use of a dual-gate TFT.

386. Accordingly, limitation 18[a] is disclosed by Kim-923 in combination with Moon.

- b. 18[b]: “wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.”**

387. See the discussion of Ground 2B, Claim 25, limitation 25[b] above.

Here, the third signal line of Claim 18 is treated similar to the second signal line of Claim 25 (mapped to the prior scan line 122 Sn-1 of Kim-923).

388. Accordingly, limitation 18[b] is disclosed by Kim-923 in combination with Moon.

13. Claim 19: “The display apparatus of claim 7, further comprising a connecting line connecting the one end of the fourth semiconductor and the first electrode layer and being in the same layer as the first signal line.”

389. See the discussion of Ground 2B, Claim 27 above.

E. Ground 2C: The combination of Kim-923 and Han renders Claims 5, 11-14, and 28-32 obvious.

1. Motivation to Combine Kim-923 and Han

390. In my opinion, there are several reasons that motivate combining the teachings of Kim-923 and Han.

391. Both references describe related technical aspects of OLED display devices that utilize TFTs, and particularly, six TFTs arranged in a typical OLED driving configuration. Kim-923, ¶¶3, 60, Fig. 1; Han, ¶¶38-41, Fig. 2. Han uses two triple-switched TFT structures for two of the TFTs that act in concert because they have a common gate control (similar to a double- or triple-gate TFT); Han; Figs. 2, 4. Further, both Kim-923 and Han advocated for reducing the leakage currents. Kim-923, ¶¶9, 91; Han, ¶¶9, 58.

392. Therefore, in my opinion, a POSITA would have clearly recognized common goals of the two references and would have understood that the device of Kim-923 can be improved based on the teachings of Han. While Han shows the use of triple-TFT structures to reduce leakage, Han also recognized that its invention

was not limited to triple-TFTs but can be implemented using two TFTs. Han, ¶¶44-45.

393. Specifically, it would have been obvious to further reduce the leakage current in the display device of Kim-923, based on the teachings of Han, by adding a second capacitor, C2, to the driving circuit of Kim-923, as described in Han. Further, there is motivation to make this modification based on Han's express teachings that adding capacitor C2 in the designated location between the voltage line ELVDD and TFT M3 would have "minimize[ed] or reduc[ed] the leakage currents." *Id.*, ¶58, Fig. 2. This is because leakage currents are a significant problem in integrated circuits, and especially thin-film circuits.

394. Thus, in my opinion, a POSITA would have been motivated to use a second capacitor, as described in Han, to Kim-923's OLED pixel to yield the predictable result of reducing leakage current. There would have been a reasonable expectation of success because adding a second capacitor to the OLED driving circuit was a routine design task, was taught by Han, and such modifications were well within the skillset of a POSITA.

395. I will provide additional explanations regarding the Kim-923–Han combination in connection with specific claim limitations below.

2. **Claim 5**

a. **5[pre]: “The display apparatus of claim 1, further comprising:”**

396. As described above in Ground 2A, Kim-923 teaches or suggests the limitations of base Claim 1. *See* §VIII.C.2, *supra*.

b. **5[a]: “a third thin-film transistor comprising a third semiconductor, one end of the third semiconductor being connected to one end of the first semiconductor, and the other end of the third semiconductor being connected to the first electrode layer; and”**

397. In my opinion, Kim-923 in combination with Han teaches or suggests limitation 5[a].

398. Kim-923 teaches “a third” thin-film transistor, namely TFT T3 formed along a semiconductor layer (“third semiconductor”). Kim-923 explains that T3 is formed along a portion of semiconductor 131 (i.e., 131c, “third semiconductor”) and includes source and drain electrodes formed as doped regions of the semiconductor. Kim-923 ¶¶79, 85, 91. Therefore, the Fig. 1 connection of source/drain of T4 is through the doped region of semiconductor 131 that forms the drain/source electrode of T4, as also evident from Fig. 3. *Id.*, Fig. 3.

[0079] The driving thin film transistor T1, the switching thin film transistor T2, the compensation thin film transistor T3, the initialization thin film transistor T4, the operation control thin film transistor T5, and the light emission control thin film transistor T6 are formed along the semiconductor layer 131, and the semiconductor layer 131 is bent to have various shapes. The semiconductor layer 131 may be formed of polysilicon, and includes a channel region, which is not doped with an impurity, and a source region and a drain region formed at respective sides of the channel region to be doped with the impurity. The type of impurity corresponds to the (partial reproduction)

[0085] The driving source electrode 176a corresponds to the driving source region 176a doped with the impurity in the driving semiconductor layer 131a, and the driving drain electrode 177a corresponds to the driving drain region 177a doped with the impurity in the driving semiconductor layer 131a. The storage capacitor Cst is formed thereon to overlap the driving gate electrode 125a.

Kim-923, ¶¶79 (partial), 85.

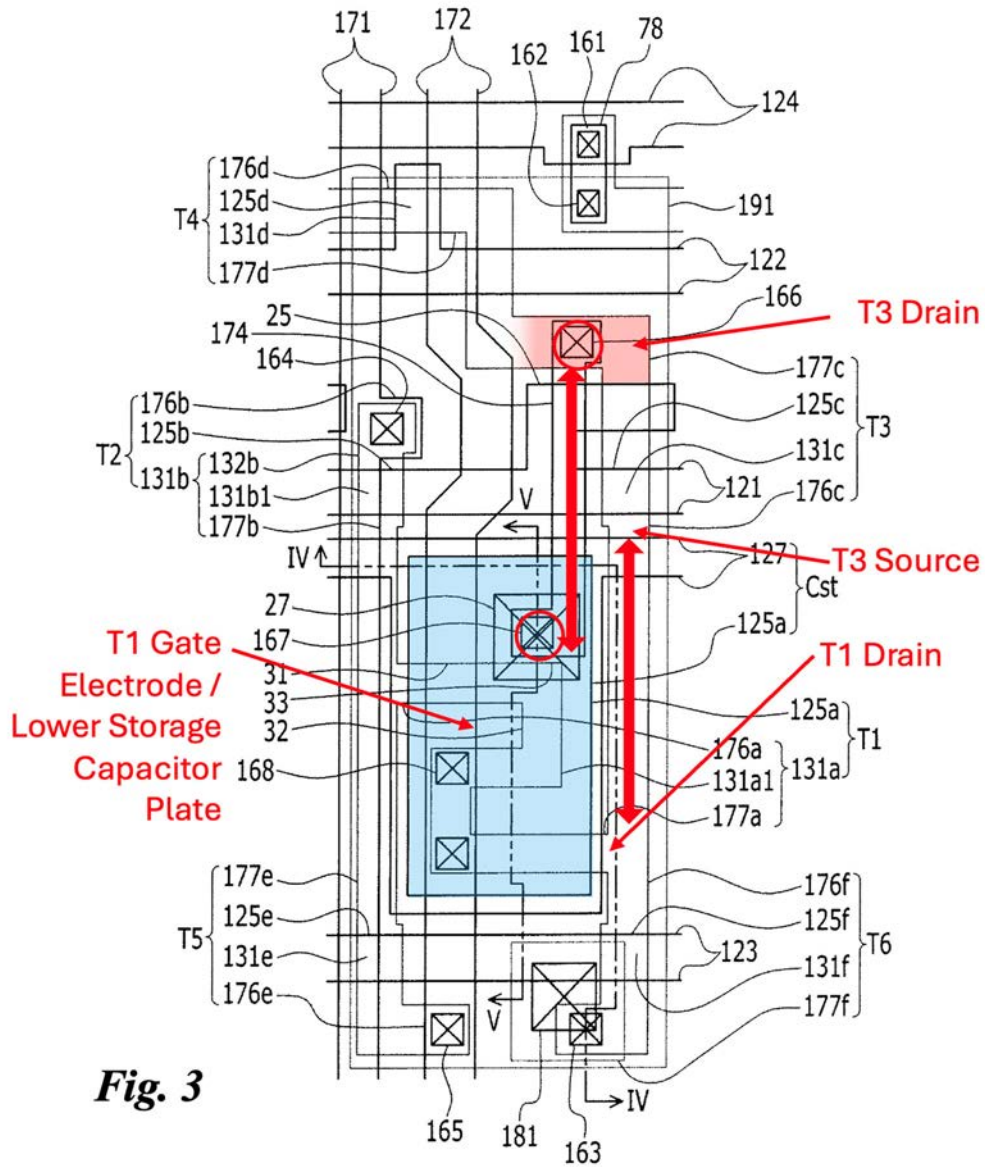
399. As shown in annotated Fig. 1 of Kim-923, below, source S3 of TFT T3 (“one end of third semiconductor” shown in yellow) is connected (labeled A) to drain D1 of first TFT T1 (“one end of the first semiconductor” shown in blue), and drain D3 of TFT T3 (“the other end of third semiconductor”) is connected (labeled B) to lower storage capacitor plate Cst1, which is gate electrode G1 of TFT T1 (“the first electrode layer”). Kim-923, ¶¶65.

[0065] A gate electrode G3 of the compensation thin film transistor T3 is coupled to the scan line 121, a source electrode S3 of the compensation thin film transistor T3 is coupled via the light emission control thin film transistor T6 to the anode of the OLED while being coupled to the drain electrode D1 of the driving thin film transistor T1, and a drain electrode D3 of the compensation thin film transistor T3 is coupled to an end Cst1 of the storage capacitor Cst, a drain electrode D4 of the initialization thin film transistor T4, and the gate electrode G1 of the driving thin film transistor T1 together. The compensation thin film transistor T3 is turned on according to the scan signal Sn transferred through the scan line 121 to couple the gate electrode G1 and the drain electrode D1 of the driving thin film transistor T1 to each other, thus performing diode-connection of the driving thin film transistor T1.

Kim-923, ¶65.



400. The semiconductor (131c) connectivity is also shown in Fig. 3 (annotated below): T3's source (176c) is connected to T1's drain (177a), and T3's drain (177c) is connected to lower storage capacitor plate/T1's gate electrode (125a) through holes 166, 167 and connection line 174. Kim-923, ¶96.



401. Accordingly, limitation 5[a] is disclosed by Kim-923 in combination with Han.

- c. **5[b]: “a second shield layer in a layer between the first signal line and the third semiconductor and overlapping a part between a first channel area and a second channel area of the third semiconductor.”**

402. In my opinion, Kim-923 in combination with Han teaches or suggests limitation 5[b].

403. Kim-923 teaches that T3 can be double-gated and shows the two gates of T3 in Fig. 3 (annotated below with red circles) formed at locations where scan line 121 (shown in blue) overlaps semiconductor 131c (red color) of T3. Kim-923, ¶¶79, 91, 105, Fig. 2. Therefore, in my opinion, a POSITA would have understood that the semiconductor region under one gate electrode of T3 constitutes the “first channel area” and the semiconductor region under the other gate electrode of T3 constitutes the “second channel area.” *Id.*

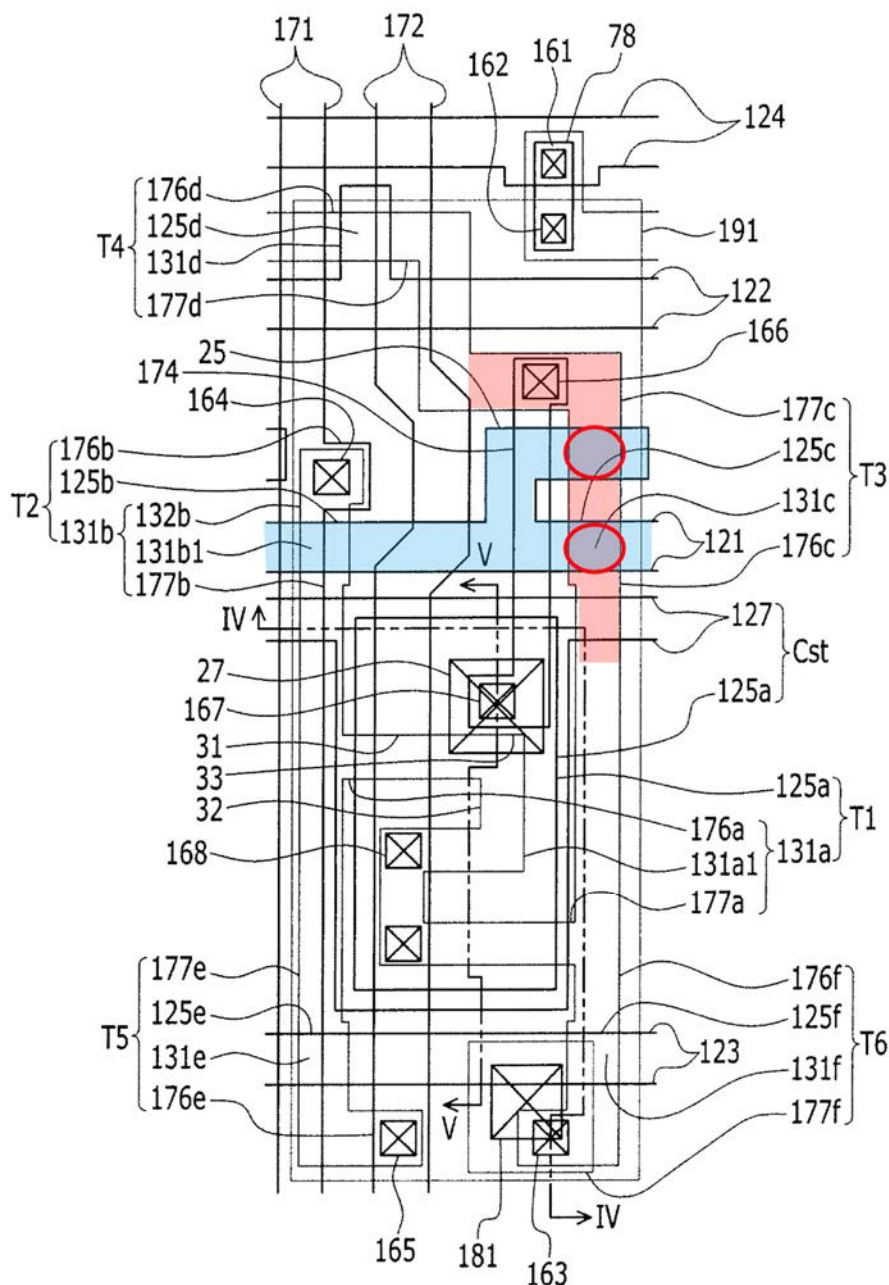


Fig. 3

404. I note that Kim-923 does not explicitly recite the second shield layer. However, in my opinion, this limitation would have been obvious based on the teachings of Han in the Kim-923–Han combination. Han teaches a similar 6-TFT

circuit as Kim-923 that includes multi-gated transistors (Han, ¶¶28, 44, Fig. 2, Fig. 4) and a storage capacitor (C1 in Han, and Cst in Kim-923) but additionally includes a second capacitor, C2, to further reduce the leakage current. *Id.*, ¶¶28, 41, 58. As I have explained in §VIII.E.1, a POSITA would have found it obvious to combine Kim-923 with Han to achieve the desirable effects of Han in reducing the leakage current.

405. Han does not provide a plan-view diagram of the pixel layout but shows, in its Fig. 2, and describes in its detailed description, that second capacitor C2 is “coupled to the first power supply (ELVDD), and a first terminal ... is coupled to both a second node N2 and a third node N3.” Han, ¶49, Fig. 2. As Fig. 2 illustrates, N2 is between M3-1 and M3-2 (first dual-gate TFTs). While Fig. 2 illustrates three series-connected TFTs for M3 and M4, Han also explains that each of M3 and M4 can include two series-connected TFTs. *Id.*, ¶¶44-45.

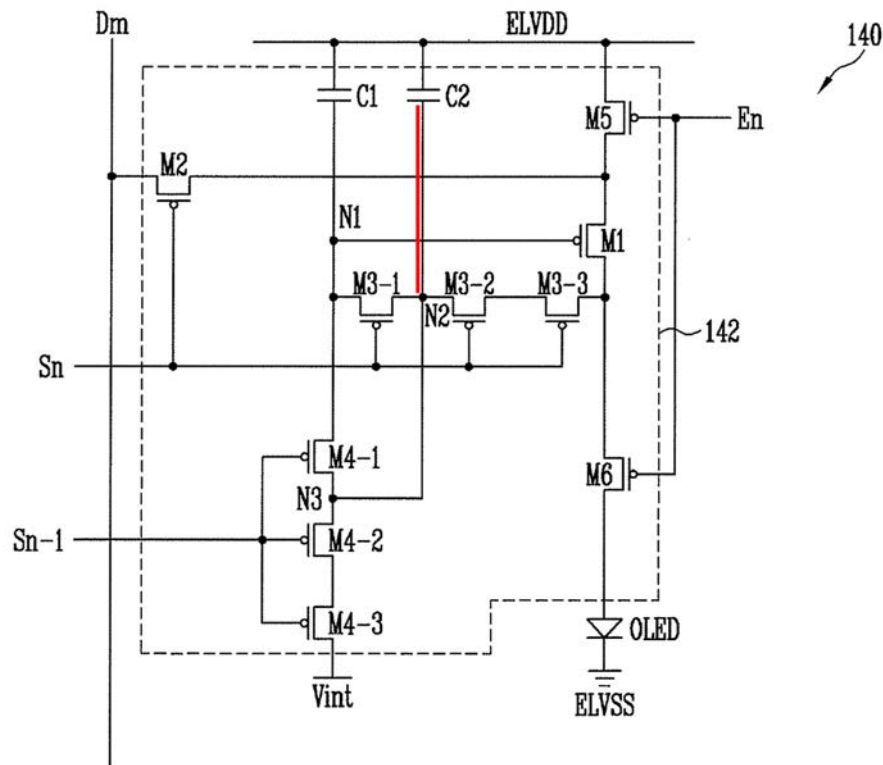


Fig. 2

406. Based on the explicit connections shown in Fig. 2 of Han, it is my opinion that a POSITA would have known that the lower plate of capacitor C2 must be connected to the drain-source junction between the two series transistors (i.e., at N2), as shown by the red line in annotated Fig. 2 above. In the combination with Kim-923, this junction would be a doped (and conductive) semiconductor area between the two gates of T3, as annotated in Fig. 3 of Kim-923 (below). As Kim-923 explains, source and drain regions outside of the channel area can be doped and made conductive. Kim-923, ¶79. A POSITA would have understood that an obvious location for placing the plates of parallel-plate capacitor C2 would be at or above the

designated junction. A POSITA would have found such a placement obvious and advantageous because it was at or close to the semiconductor region of interest (node N2), and it would have allowed easy and direct connection to that junction. Generally, circuit lines should be as short as possible to reduce parasitic elements and EMI. Therefore, as noted above, a preferred connection for C2 is directly between the gates, as shown in green in Fig. 3 annotated below. As I explained in Ground 1B, a POSITA would have found it obvious to implement the lower plate of C2 as part of the semiconductor layer, or place it over an insulating layer directly above the doped semiconductor layer with a “via” connecting the lower capacitor plate to the junction. The reasons for these obvious choices are similar to those that I explained in Ground 1B, element 5[b], and I refrain from repeating them here.

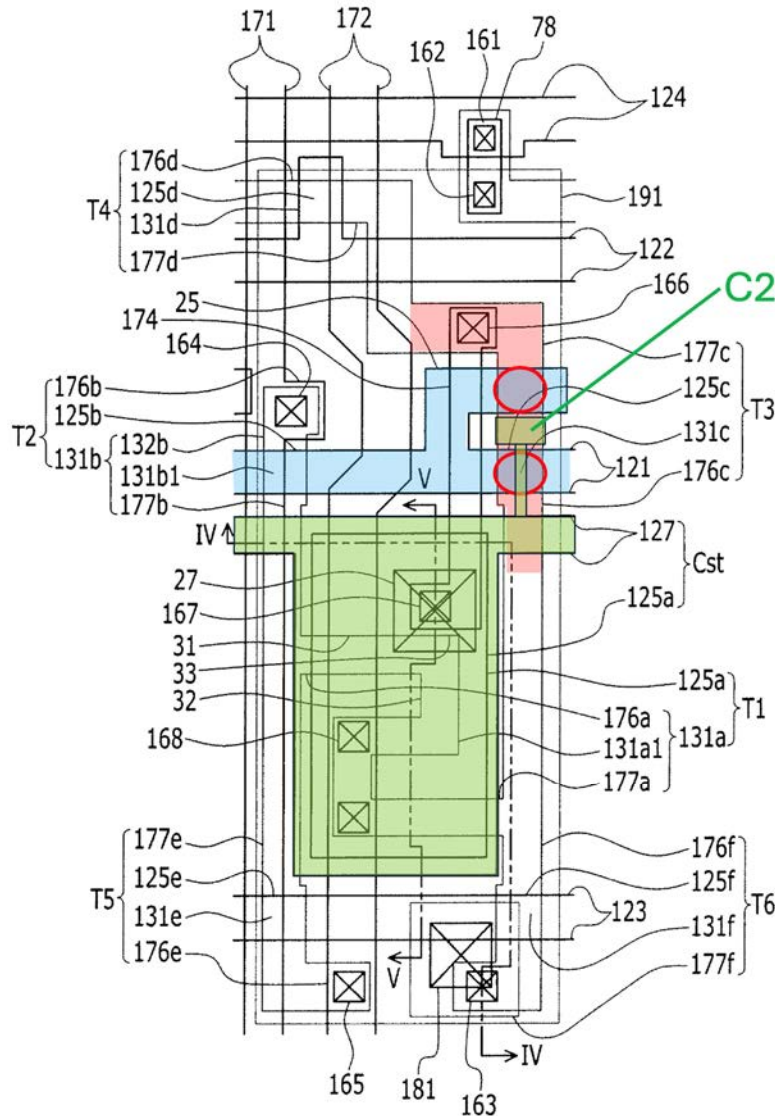


Fig. 3

407. The upper capacitor plate of C2 would be connected to voltage line, ELVDD (line 172), as required by Han's circuit diagram of Fig. 2. Han, ¶49, Fig. 2. In my opinion, it would have been obvious (and a matter of routine layout design) to implement that connection. Capacitor plates in a thin-film structure typically directly overlap in the vertical direction to maximize their capacitance and the upper

plate of C2 is connected to ELVDD (as shown in Han) and a short connection to C1 with reduced length and parasitic elements. For example, a POSITA would have connected the upper capacitor plate of C2 to upper plate 127 of storage capacitor Cst using a connection line, as shown in the annotated figure below. Such a connection would have been obvious, routine, and advantageous because the upper plate of C1 (i.e., element 127 in Kim-923) was nearby and was already connected to ELVDD. See also Kim-923, ¶97, Fig. 1, showing connection of Cst2 to ELVDD, and Han, Fig. 2, showing connection of C1 to ELVDD. Accordingly, the upper plates of both capacitors would be in the same layer, connected together and connected to ELVDD.

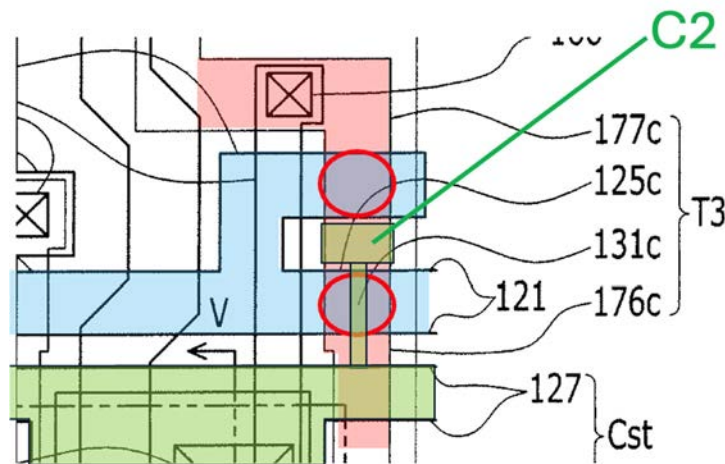


Fig. 3

408. Furthermore, the capacitance of a parallel-plate capacitor is proportional to area over thickness. See Weste (EX1012), Chapter 2.2, equation 2.2. In an example, for a capacitor with capacitor plates having dimensions $W \times L$ (width

by length) that are separated by a dielectric layer with thickness t and permittivity ε , the capacitance of the capacitor is given by:

$$C = \varepsilon \times \frac{W \times L}{t}.$$

409. Accordingly, the capacitance (in farads) of the capacitor can be configured to be a specific value by, for example, selecting a dielectric layer with a specific permittivity or varying the thickness of the dielectric layer. This standard equation would have been known to a POSITA and would have allowed a POSITA to design a capacitor layout and configuration in an OLED or LCD device.

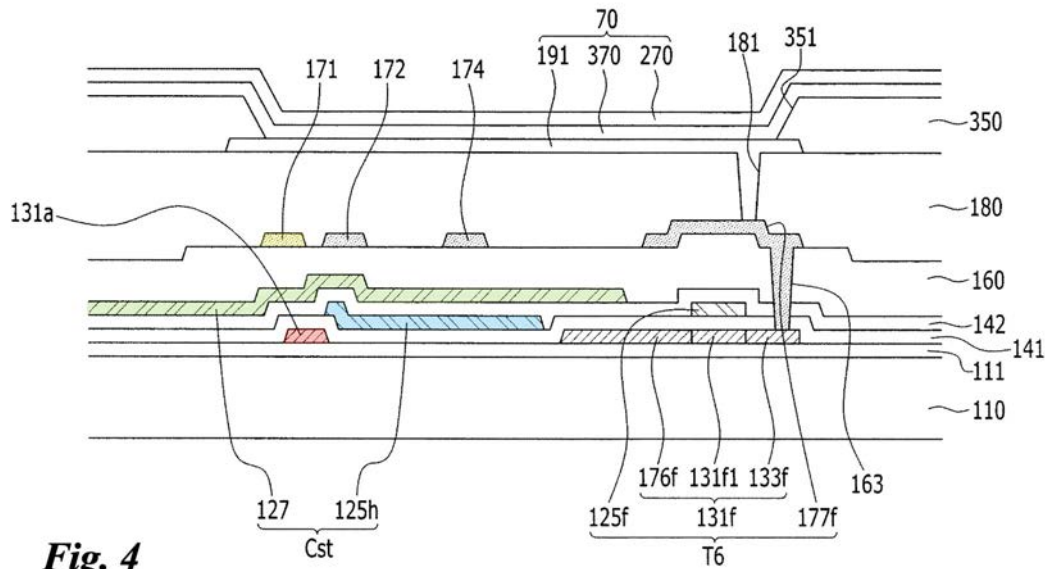
410. This knowledge is further evidenced by, for example, the disclosure in Liu (EX1028) that explicitly teaches “[t]he storage capacitance of the capacitor CS may be adjusted by selecting a specific capacitor dielectric material or adjusting a thickness of the capacitor dielectric layer.” Liu, 8:22-29. As noted above, the capacitance is directly proportional to the area of the capacitor plate and the permittivity of the dielectric layer, and inversely proportional to the thickness of the dielectric layer. It is my opinion that the trade-off between the area of the capacitor plate, a choice of dielectric, and a thickness of the dielectric layer would be a matter of routine design for a POSITA. Again, Liu provides an explicit example that teaches “when a thinner capacitor dielectric layer is formed, an area occupied by the

capacitor CS can be reduced on the premise that a predetermined capacitance is maintained, such that the display may have high resolution.” *Id.*⁵

411. In the Kim-923–Han combination, the upper capacitor plate of C2, being connected to a constant voltage source (ELVDD), would operate as, and would be, the “second shield layer” for the same reasons discussed in §IV.A.1.f. The upper capacitor plate of C2 would also be overlapping the semiconductor region between the two gates of T3 (see the upper green rectangle denoted C2 in the annotated figure above) and would thus overlap “a part between a first channel area and a second channel area of the third semiconductor.” Furthermore, the “second shield layer” would be in “a layer between the first signal line and the third semiconductor” because the upper capacitor plate of C2 would reside in the same layer as the storage capacitor’s upper plate (element 127, annotated in green in Fig. 4 below), which as illustrated below (and explained in §VIII.C.2.f), is between the semiconductor layer (131a/131f in annotated Fig. 4 below) and the first signal line (data line 171). I note that Fig. 4 of Kim-923 shows semiconductor 131a (T1) and 131f (T6). But Kim-923 explains that 131a, 131f and 131c (the semiconductor of T3, “third semiconductor”) are part of the same contiguous semiconductor layer 131. Kim-923, ¶79. Therefore,

⁵ This analysis also applies to Ground 1B’s combination.

the above noted relative positioning described using Fig. 4's 131a also applies to the "third" semiconductor 131c.



412. Accordingly, limitation 5[b] is disclosed by Kim-923 in combination with Han.

3. Claim 11

- a. 11[a]: "The display apparatus of claim 5, wherein a gate electrode of the third thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the third semiconductor, and the second gate electrode overlapping the second channel area of the third semiconductor, and"

413. As I have explained in the discussion of Ground 2C, Claim 5, Kim-923 teaches that TFT T3 is double gated, and the combination includes at least two gate electrodes in a same layer, as shown with red circles in annotated Fig. 3, where the

gates are formed at locations where scan line 121 (blue) overlaps semiconductor 131c (red color) of T3. Kim-923, ¶¶79, 91, 105, Fig. 2. Therefore, it is my opinion that a POSITA would have understood that one gate electrode of T3 overlaps the first channel area under that gate electrode, and the other gate electrode overlaps the second channel area under it. The two gate electrodes are in the same layer because they are both part of scan line 121.

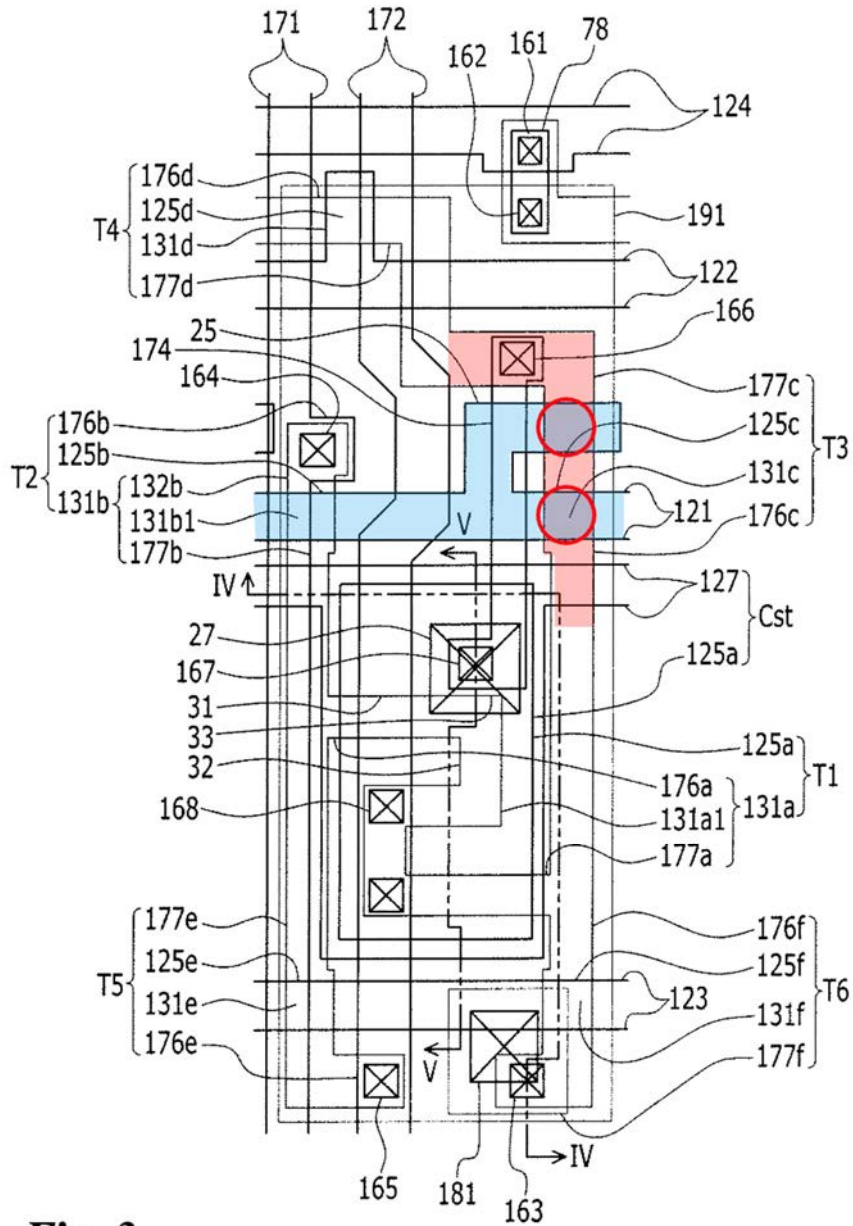


Fig. 3

414. Accordingly, limitation 11[a] is disclosed by Kim-923 in combination with Han.

- b. **11[b]: “wherein the gate electrode of the third thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.”**

415. In my opinion, Kim-923 in combination with Han teaches or suggests limitation 11[b].

416. The gate electrode for the third TFT is formed as part of scan line 121 (“second signal line”). Kim-923, ¶105: “The first gate wires including the scan line 121, which includes ... the compensation gate electrode 125c.” Kim-923 further teaches that “a plurality of signal lines” including “a data line 171 crossing the scan line 121.” Kim-923, ¶62. As explained above, data line 171 is construed as the “first signal line.” *See* §VIII.C.2.e.

417. Kim-923 shows that scan line 121 is in the same layer as the first storage capacitor plate/gate of T1 (“first electrode layer;” *see* §VIII.C.2.c): **“The first storage capacitor plate 125h** is separated from the adjacent pixel to form a rectangle, and **is formed of the same material as the scan line 121**, the prior scan line 122, the light emission control line 123, the switching gate electrode 125b, the compensation gate electrode 125 c, the operation control gate electrode 125e, and the light emission control gate electrode 125f, **which are on the same layer first storage capacitor plate 125h.**” Kim-923, ¶87.

418. Accordingly, limitation 11[b] is disclosed by Kim-923 in combination with Han.

4. Claim 12: “The display apparatus of claim 5, further comprising a first voltage line in the same layer as the first signal line, wherein the second shield layer is connected to the first voltage line.”

419. In my opinion, Kim-923 in combination with Han teaches or suggests Claim 12.

420. Kim-923 teaches that voltage line 172 (“first voltage line;” see §VIII.C.5) is in the same layer as data line 171 (“first signal line”), as shown in annotated Fig. 4 below in green and red, respectively. Kim-923 explains that voltage line 172 is a “driving voltage line ... for transferring a driving voltage ELVDD.” Kim-923, ¶62. As I have explained in the discussion of Claim 5, in the Kim923–Han combination, the top electrode of capacitor C2 (“second shield layer”) is connected to ELVDD. See §VIII.E.2.

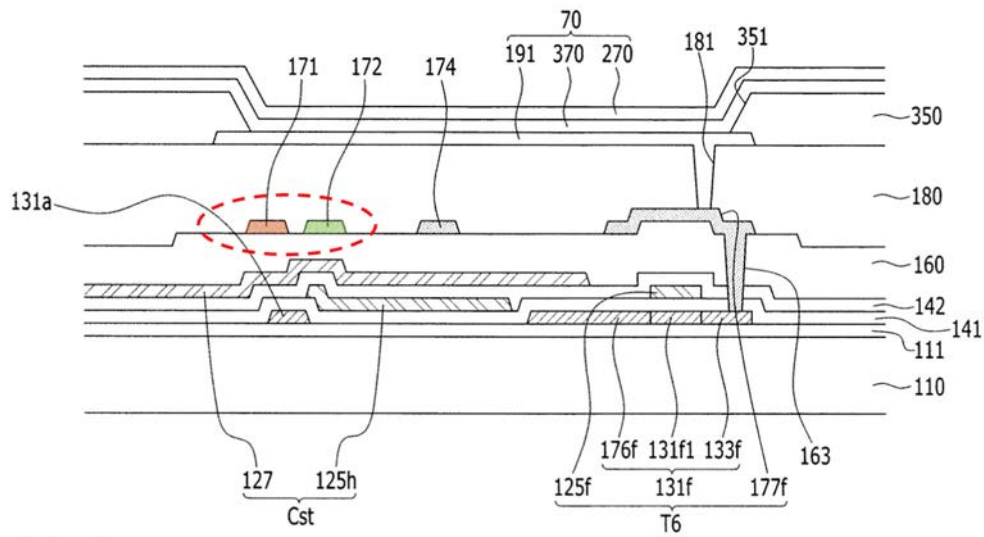


Fig. 4

421. Accordingly, Claim 12 is disclosed by Kim-923 in combination with Han.

5. Claim 13: “The display apparatus of claim 5, wherein the second shield layer is a part of the second electrode layer.”

422. In my opinion, Kim-923 in combination with Han teaches or suggests Claim 13.

423. As I have explained in the discussion of Claim 5 (*see* §VIII.E.2.c), it would have been obvious to a POSITA that the top electrode of second capacitor C2 would be in the same layer, and would be connected to the top plate of the storage capacitor because the two plates are required to be connected together (*see* Han’s Fig. 2), were in close vicinity of each other, and the top storage capacitor plate was already connected to ELVDD. As I have also explained in the discussion of Claim 2 in Ground 2A, the top plate of the storage capacitor was part of the second electrode

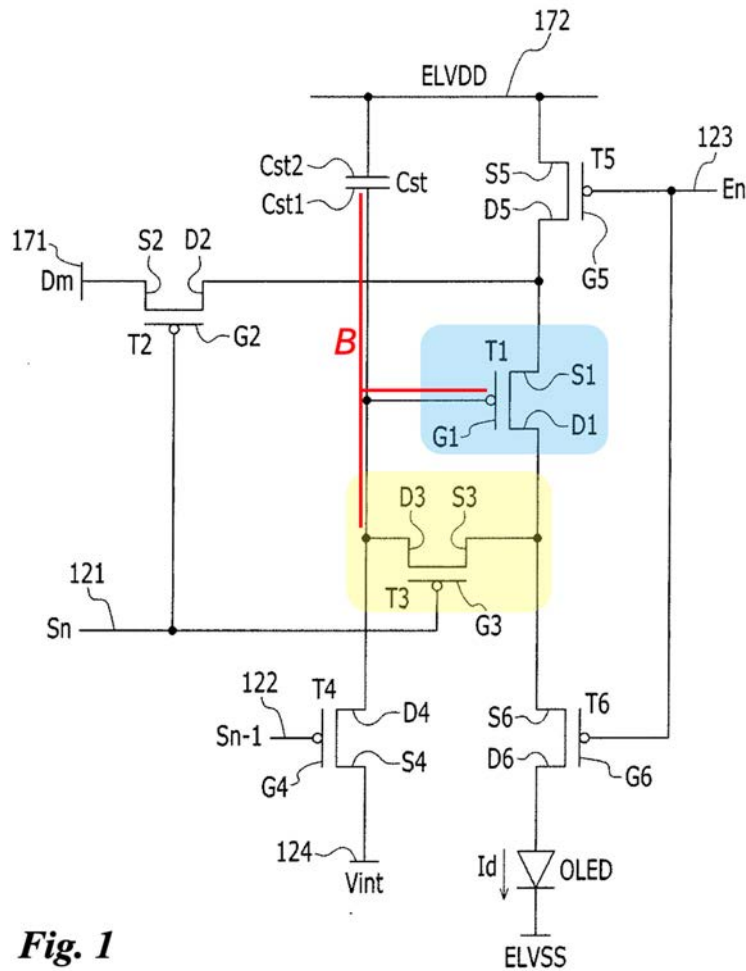
layer (see §VIII.C.3), and therefore the top plate of capacitor C2 (“second shield layer”) would also be in the second electrode layer in the Kim-923–Han combination.

424. Accordingly, Claim 13 is disclosed by Kim-923 in combination with Han.

6. Claim 14: “further comprising a connecting line connecting the other end of the third semiconductor and the first electrode layer and being in the same layer as the first signal line.”

425. In my opinion, Kim-923 in combination with Han teaches or suggests Claim 14.

426. Kim-923 shows that the drain of T3 (“other end of the third semiconductor” 177c) is connected to storage capacitor plate Cst1 and to gate electrode G1 of TFT T1 (“the first electrode layer”), which I have annotated in Fig. 1 below with line B.



427. As I have shown in annotated Fig. 3 of Kim-923 below, the drain of T3 is connected to the gate electrode/first storage capacitor plate 125h/125a via connection member 174 (yellow), which is in the same layer as data line 171 (“first signal line”).

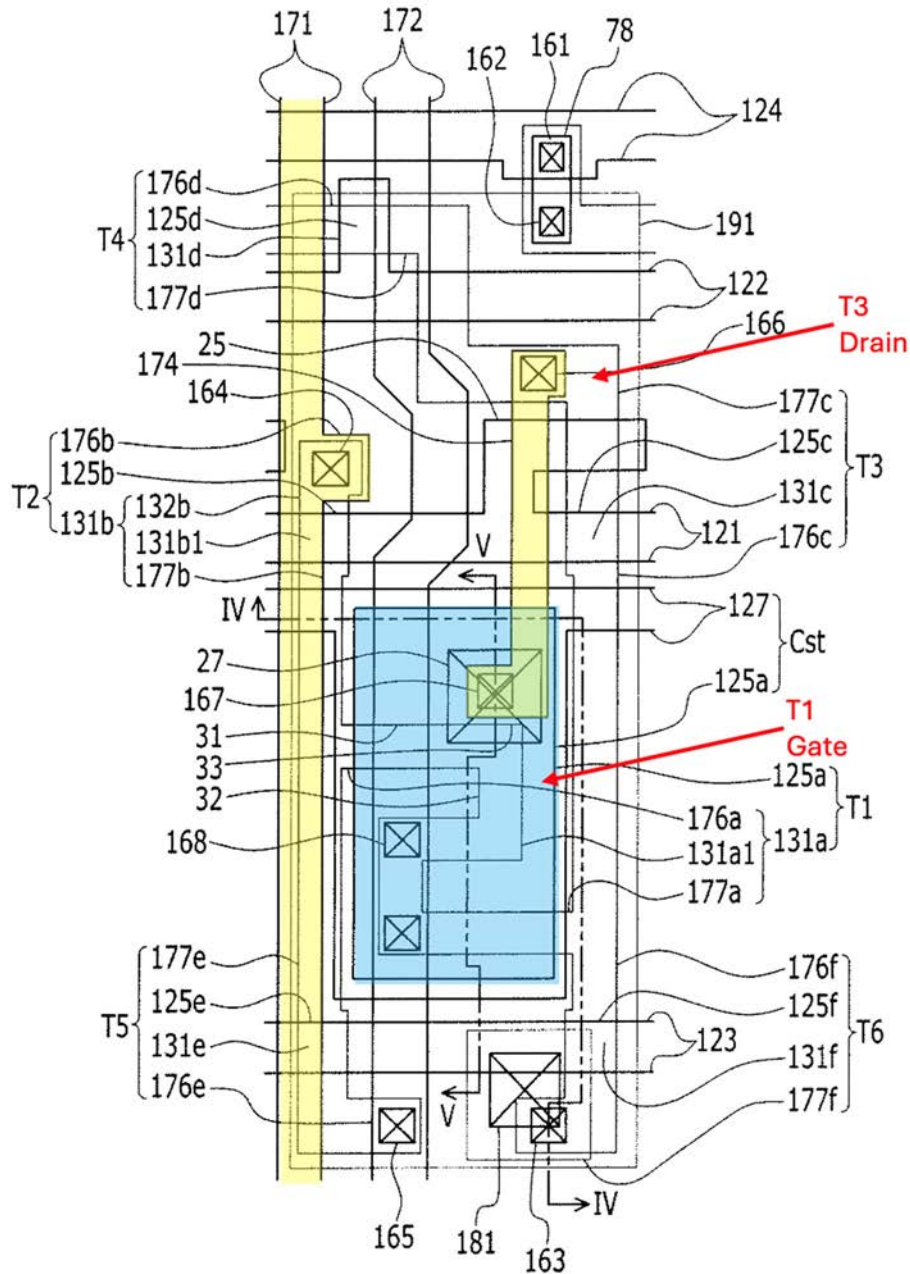


Fig. 3

428. Kim-923 explains: “**The connection member 174 is formed on the same layer as the data line 171, an end of the connection member 174 is coupled through a contact hole 166 formed in the first gate insulating layer 141, in the second**

gate insulating layer 142, and in the interlayer insulating layer 160 **to the compensation drain electrode 177c** and to the initialization drain electrode 177d, and **another end of the connection member 174 is coupled** through a contact hole 167 formed in the second gate insulating layer 142 and in the interlayer insulating layer 160 **to the first storage capacitor plate 125h.**" Kim-923, ¶96. *See also* annotated Fig. 4 below showing connection line 174 and data line 171 (both highlighted in yellow) are in the same layer.

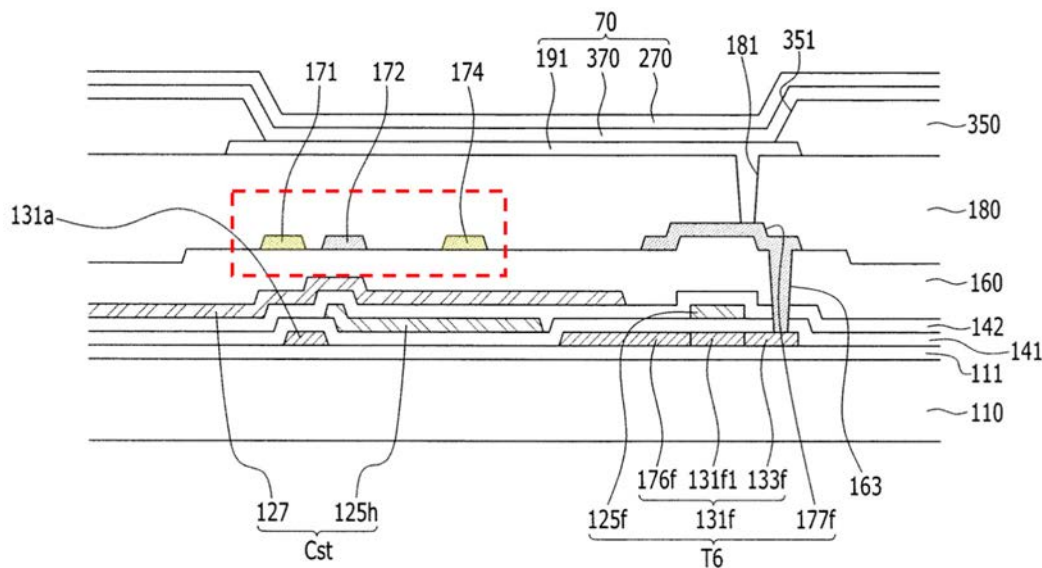


Fig. 4

429. Accordingly, Claim 14 is disclosed by Kim-923 in combination with Han.

7. Claim 28

a. 28[pre]: “A display apparatus comprising:”

430. Kim-923 and Han both relate to displays, and in particular to OLED displays. See, e.g., Kim-923, Abstract and Han, Abstract.

b. 28[a]: “a first thin-film transistor comprising a first semiconductor;”

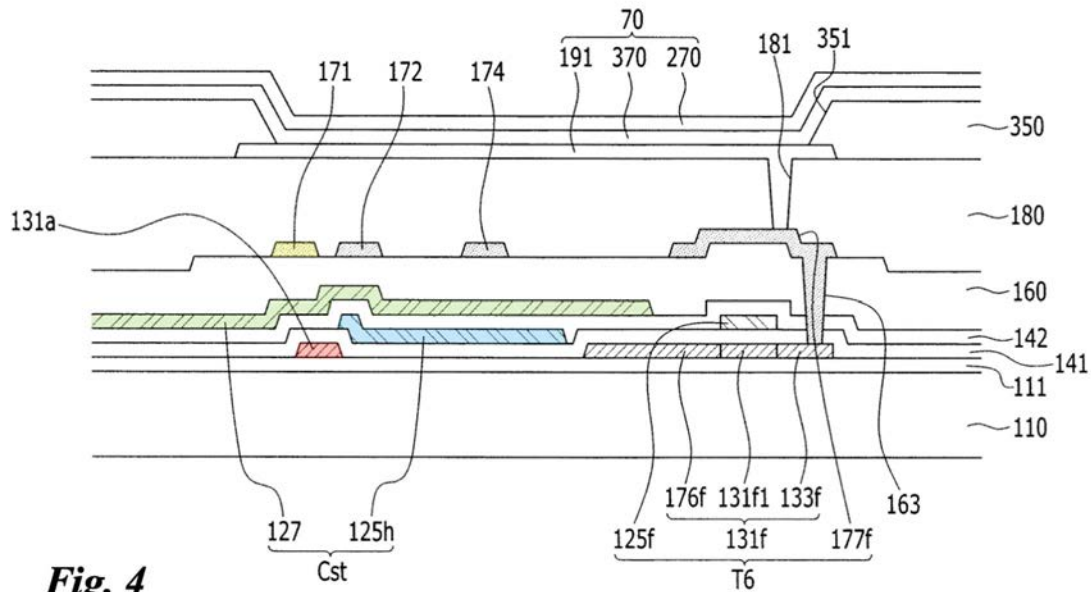
431. See the discussion of Ground 2A, Claim 1, limitation 1[b] above. Kim-923 teaches a first thin-film transistor comprising a first semiconductor, driving thin film transistor T1. See §VIII.C.2.c.

c. 28[b]: “a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;”

432. See the discussion of Ground 2A, Claim 1, limitation 1[c] above. See §VIII.C.2.d.

d. 28[c]: “a first signal line over the first electrode layer;”

433. See the discussion of Ground 2A, Claim 1, limitation 1[d] above. See §VIII.C.2.e. While 1[d] recites “over the second electrode layer,” Kim-923 discloses that data line 171 (“first signal line” shown in yellow) is over both lower capacitor plate 125h (“first electrode layer” shown in blue) and upper capacitor plate 127h (“second electrode layer” shown in green), as illustrated in annotated Fig. 4 below.



434. Accordingly, limitation 28[c] is disclosed by Kim-923.

- e. **28[d]: “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and”**

435. In my opinion, Kim-923 teaches or suggests limitation 28[d].

436. Kim-923 discloses this limitation because it discloses a TFT T3 (“second thin-film transistor” shown in yellow) having its source (“one end of second semiconductor”) connected to the drain of TFT T1 (“one end of first semiconductor” denoted A) and its drain (“one end of second semiconductor” denoted B) connected to gate electrode G1 of TFT T1 and to storage capacitor plate Cst1 (“first electrode layer”), as shown in annotated Fig. 1 below, and similar to the

discussion of Ground 2C, Claim 5. *See* §VIII.E.2. While Claim 5 recited a “third” TFT (as opposed to a “second” TFT” in Claim 28), TFT T3 of Kim-923 is mapped to the “second” TFT” in Claim 28.

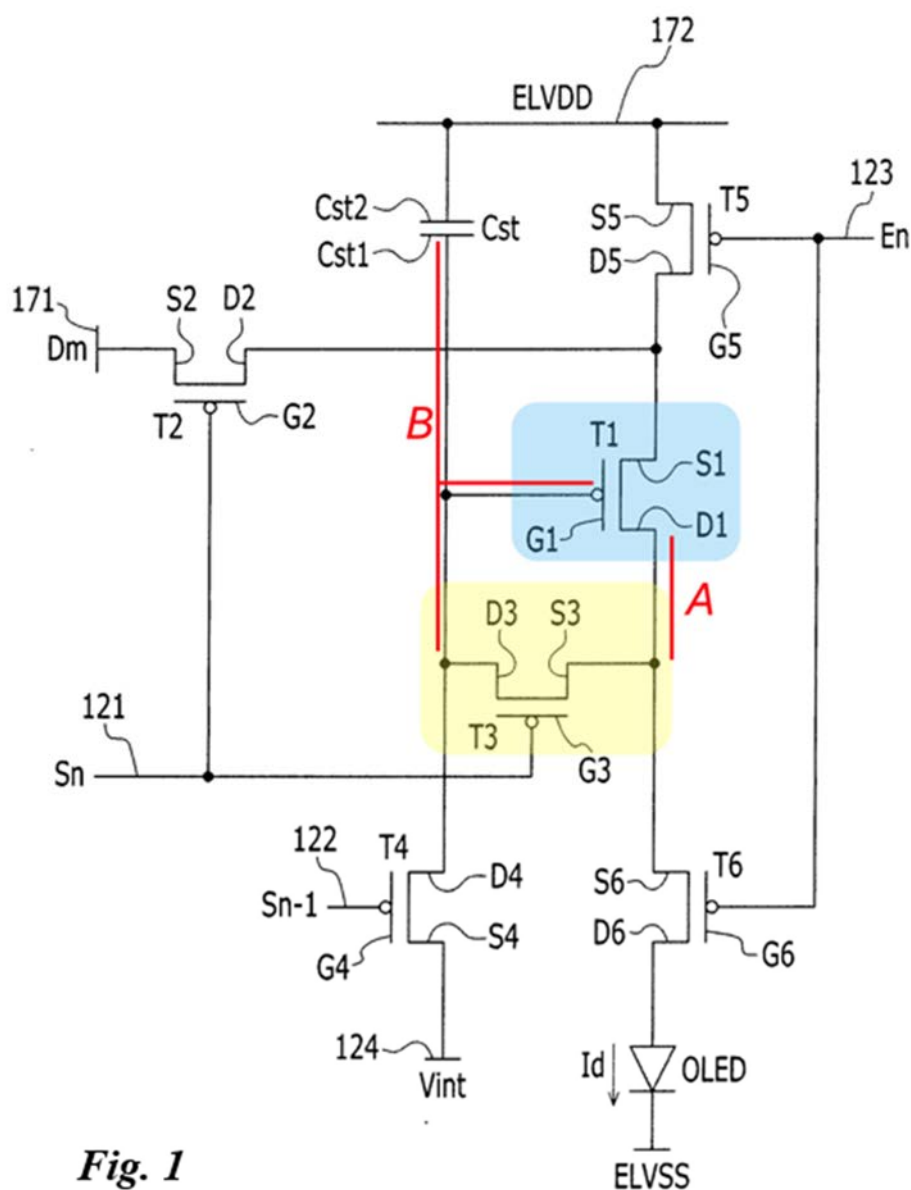


Fig. 1

437. Accordingly, limitation 28[d] is disclosed by Kim-923.

- f. **28[e]: “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.”**

438. See the discussion of Ground 2C, Claim 5, limitation 5[b] above. See §VIII.E.2.c. In Claim 28 (similar to Claim 5), the top capacitor plate of capacitor C2 constitutes “a shield layer.” I note that the top capacitor plate of C2 is connected to ELVDD and therefor acts as a shield and is naturally disposed over the second semiconductor channel.

439. Accordingly, limitation 28[e] is disclosed by Kim-923 in combination with Han.

8. Claim 29

- a. **29[a]: “The display apparatus of claim 28, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and”**

440. See the discussion of Ground 2C, Claim 11, limitation 11[a] above. In Claim 29 (similar to Claim 11), TFT T3 is construed as the “second” TFT.

- b. 29[b]: “wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.”**

441. See the discussion of Ground 2C, Claim 11, limitation 11[b] above.

- 9. Claim 30: “The display apparatus of claim 28, further comprising a voltage line in the same layer as the first signal line, wherein the shield layer is connected to the voltage line.”**

442. See the discussion of Ground 2C, Claim 12 above. Therein, Claim 12 recites a “first voltage line,” whereas Claim 30 recites “a voltage line” (both of which are mapped to voltage line 172 of Kim-923). Further, Claim 12 recites “the second shield layer,” whereas Claim 30 recites “the shield layer” (both of which are mapped to top capacitor plate of capacitor C2 in the Kim-923–Han combination).

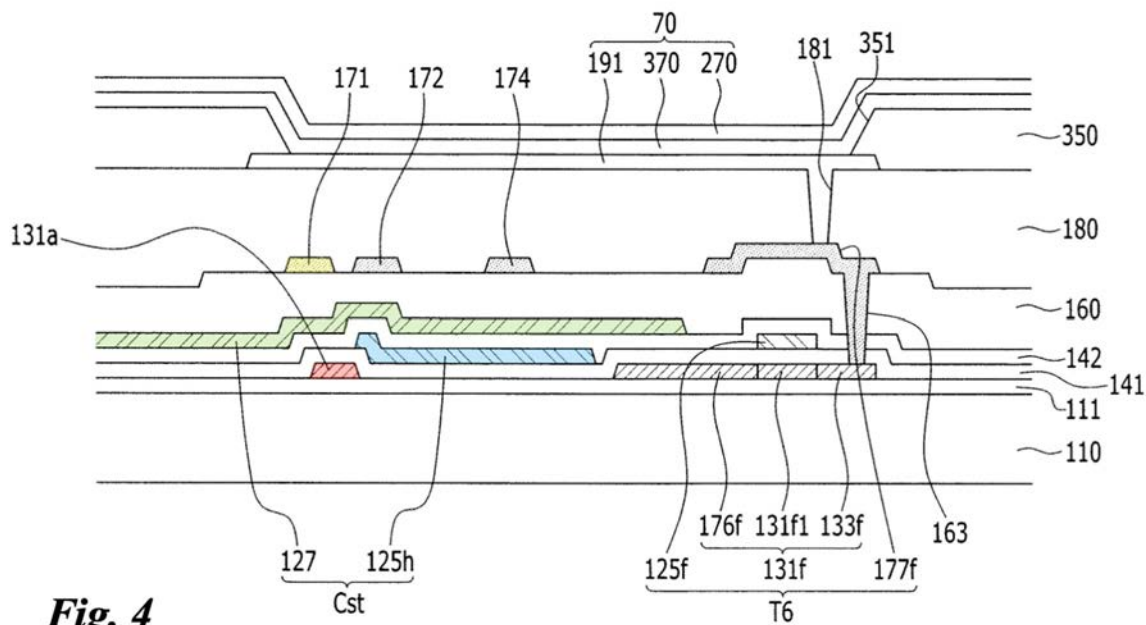
443. Accordingly, Claim 30 disclosed by Kim-923 in combination with Han.

- 10. Claim 31: “The display apparatus of claim 28, further comprising a second electrode layer over the first electrode layer and overlapping the first electrode layer, wherein the shield layer is a part of the second electrode layer.”**

444. See the discussions in Ground 2A, Claim 1, limitation 1[c] and Ground 2C, Claim 13 above. As explained in §§VIII.C.2.d and VIII.E.5, the claim limitations related to a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer, and the shield layer being part

of the second electrode layer are taught or suggested by Kim-923 in combination with Han.

445. In Claim 28, the shield layer corresponds to the top plate of the capacitor C2, which as explained in connection with Claim 13, is part of the second electrode layer. Kim-923's annotated Fig. 4 below shows the overlap of second (127) and first (125h) electrode layers. In the combination, the shield layer is part of C2's top plate, which is in the same layer as C1's top plate (127). *See also* the discussion of Ground 2C, Claim 28, limitation 28[c].



446. Accordingly, Claim 31 is disclosed by Kim-923 in combination with Han.

11. Claim 32: “The display apparatus of claim 31, further comprising a voltage line in the same layer as the first signal line, wherein the voltage line is connected to the second electrode layer.”

447. See the discussion of Ground 2A, Claim 4 above. Herein, the voltage line is line 172. *See* §VIII.C.5.

F. Ground 3: The combination of Moon and Jeon-078 renders Claims 24-27 obvious.

1. Summary of Jeon-078

448. In my opinion, Jeon-078 is in the same field as Moon and relates to organic light emitting displays. Jeon-078, ¶3. Jeon-078 utilizes a similar circuit as Moon, with six transistors and two capacitors (6T2C), both of which are reproduced below for comparison and are identical except for T1 structures D11 and D12 in Moon. Jeon-078 explains that “the OLED display may have a plurality of TFTs and at least one capacitor at one pixel” and that its invention is not limited to 6T2C circuits. *Id.*, ¶38. Jeon-078 intends to solve the problem of non-uniform luminance and explains that “[i]n order to express uniform luminance, a capacitance ratio of a storage capacitor and a boosting capacitor should be uniformly sustained between a plurality of pixels.” Jeon-078, ¶40.

FIG. 3 (Moon)

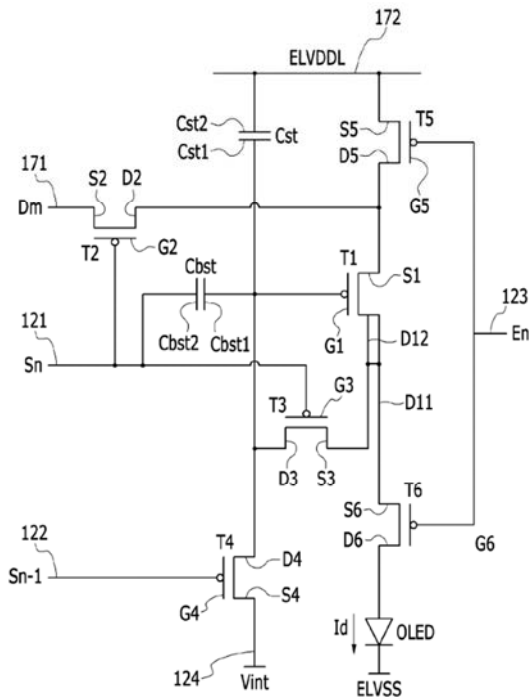
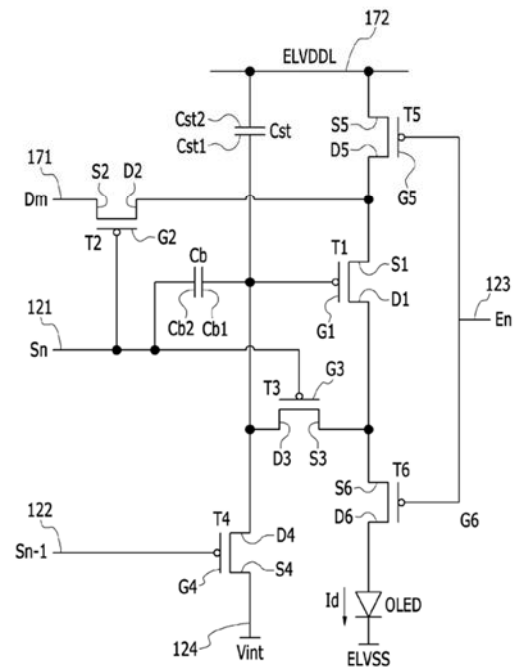


FIG. 1 (Jeon-078)



449. In Ground 3, I primarily rely on Jeon-078 for its illustration of the relative positioning of data line 171 and initialization voltage line 124 in the OLED pixel layout, as further explained below.

2. Motivation to Combine Moon and Jeon-078

450. In my opinion, there are several reasons that motivate combining the teachings of Moon with Jeon-078.

451. Both references related to OLED display devices that utilized TFTs, and more particularly to OLED display devices that utilize six TFTs and two capacitors in a typical OLED driving configuration. Moon, ¶¶3, 42, Fig. 3; Jeon-078,

¶3, 42, Fig. 1. Further, the aim of both Moon and Jeon-078 was to improve the operation of OLED display devices. Moon, ¶26; Jeon-078, ¶ 9. In my opinion, to understand and implement specific features that Moon may not have explicitly described, a POSITA would have readily turned to the teachings of Jeon-078 for guidance.

452. In particular, it is my opinion that a POSITA would have been motivated to identify and implement a voltage line, a data line and a connection line in the appropriate locations in an OLED circuit to Moon's OLED circuit to yield the predictable result of that placement of the voltage line, data line and connection line. Furthermore, there would have been a reasonable expectation of success, because placement of traces associated with TFT voltage and signal lines in OLED display circuits was well-known by 2014, as evidenced by the teachings of Jeon-078 and other known prior art references (*see generally* Weste, Kobayashi, Tomida and Kim-507 (EX1012, EX1029-EX1031, respectively), and such modifications were well within the skill set of a POSITA.

453. Additional explanations regarding the Moon-Jeon-078 combination are described in connection with specific claim limitations below.

3. Claim 24

a. 24[pre]: "A display apparatus comprising:"

454. In my opinion, Moon teaches or suggests limitation 24[pre].

455. Moon describes a display apparatus: “The described technology relates generally to a thin film transistor and an organic light emitting diode (OLED) display including the same.” Moon, ¶¶3, 12, 42.

b. 24[a]: “a first thin-film transistor comprising a first semiconductor;”

456. In my opinion, Moon teaches or suggests limitation 24[a].

457. Moon discloses a first TFT comprising a first semiconductor as TFT T1 and its associated semiconductor. Moon describes, “[o]ne embodiment provides a **thin film transistor including: a semiconductor** formed on a substrate and having a source region, a first drain region separated from the source region by a first current channel, and a second drain region separated from the source region by a second current channel.” Moon, ¶8. TFT T1 (“first TFT) is a “driving transistor.” *Id.*, ¶¶43, 45. The arrangement of TFT T1 within a circuit of a pixel is shown below in annotated Fig. 3 of Moon.

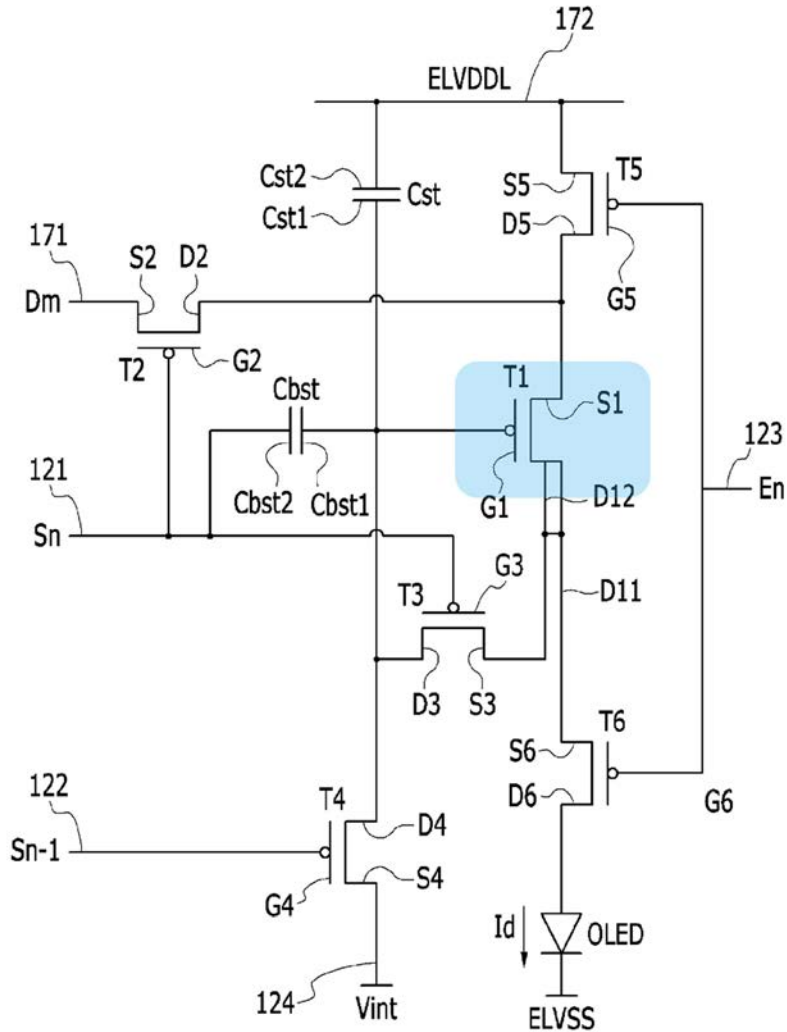


Fig. 3

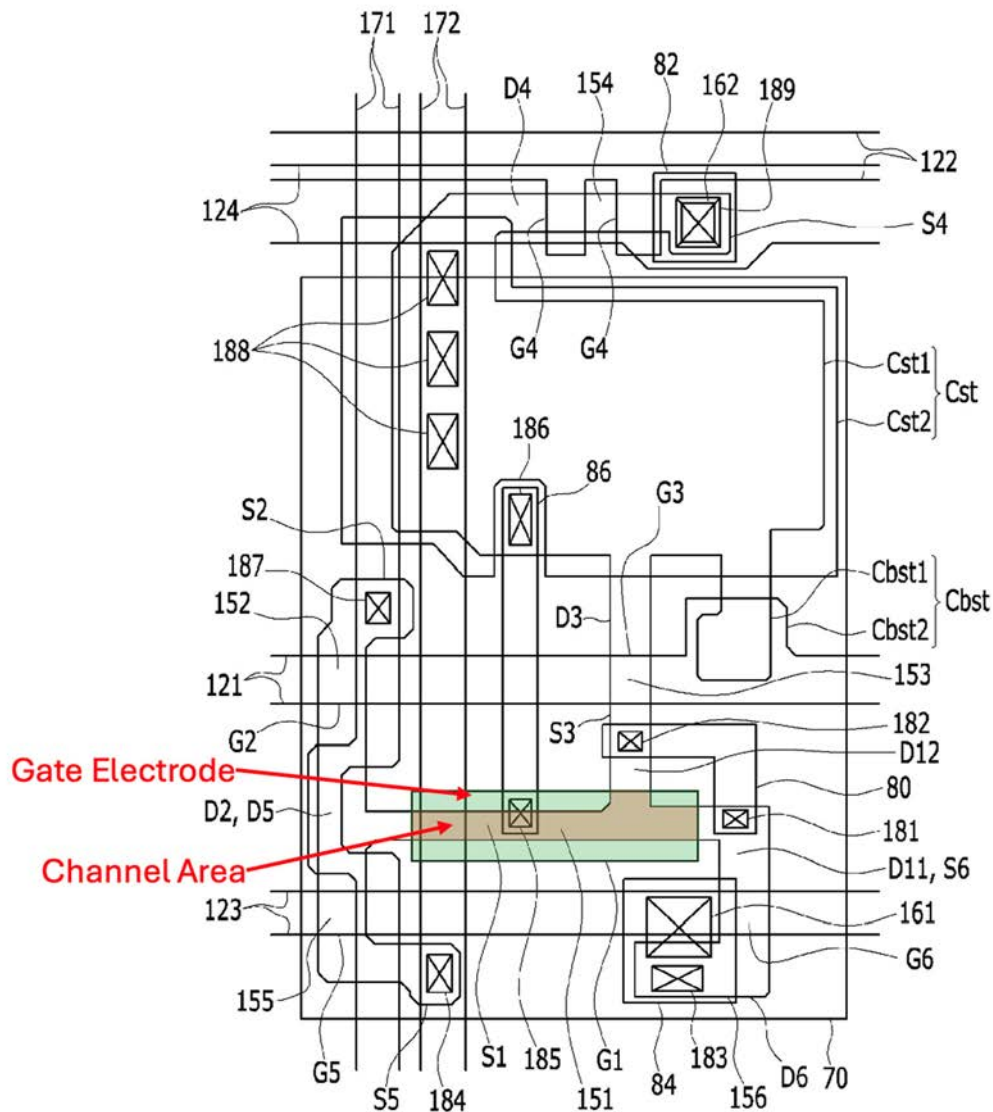
458. Accordingly, limitation 24[a] is disclosed by Moon.

c. **24[b]: “a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;”**

459. In my opinion, Moon teaches or suggests limitation 24[b].

460. Moon discloses “a first electrode layer” as the layer that contains gate electrode G1 of TFT T1. Moon, ¶45. Moon further discloses the first electrode layer

overlaps a channel area of T1: “[t]he gate electrode G1 of the driving transistor T1 **overlaps the semiconductor 151**” Moon, ¶75. In my opinion, Moon explains, and a POSITA would have known, an area overlapped by a TFT’s gate electrode corresponds to a channel area. *Id.*, ¶35, Fig. 4 (annotated below in green and brown, respectively).



461. Accordingly, limitation 24[b] is disclosed by Moon.

d. 24[c]: “a first signal line over the first electrode layer;”

462. In my opinion, Moon in combination with Jeon-078 teaches or suggests limitation 24[c].

463. Moon teaches a “first signal line” as data line 171: “a data line 171 crossing scan line 121 and delivering a data signal Dm.” Moon, ¶43; see also *id.*, ¶91, Figs. 3 and 4, showing data line 171. I note that although Moon does not explicitly describe its data line 171 (“first signal line”) is over the first electrode layer, Jeon-078, which has a similar 6T2C circuit as Moon, does. Jeon-078, ¶¶42, 44, Fig. 1.

464. Jeon-078 teaches that data line 171 is formed on interlayer insulating layer 160: “**On the interlayer insulating layer 160, a data wire including a data line 171 ... [is] formed.**” Jeon-078, ¶94. Fig. 4 of Jeon-078, annotated below, shows that data line 171 (shown in yellow) is formed in a layer above other layers that include gate electrodes (e.g., light emission control gate electrode 125f, compensation gate electrode 125c, and driving gate electrode 125a) and capacitor electrodes (e.g., first boosting capacitor plate 128 and second boosting capacitor plate 129).

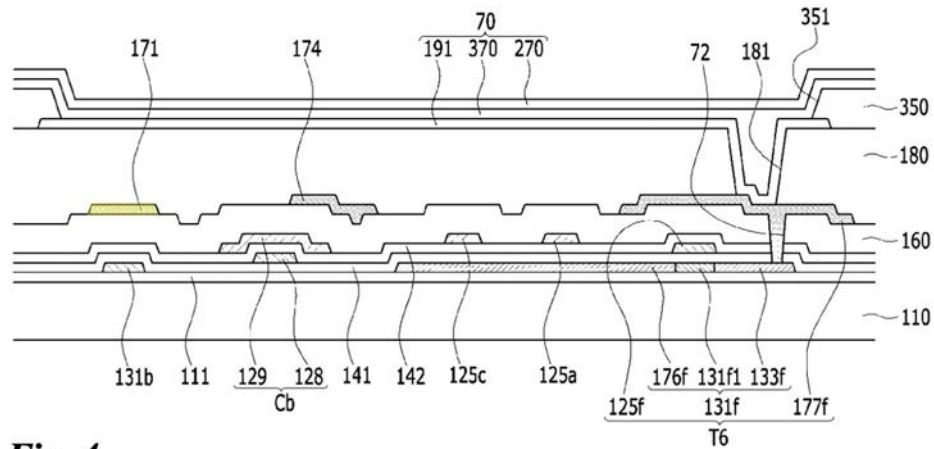


Fig. 4

465. Based on the teachings of Jeon-078, a POSITA would have understood and found it obvious to position data line 171 (“first signal line”) over the layer that included the gate electrode of T1. I note that data lines are commonly located on the top layer to aid external connection and would therefore naturally be over the gate electrode in a multi-metal layer configuration. Therefore, such a modification (to the extent it was needed given that Moon does not explicitly describe the relative positioning of data line 171) would be a routine and known way to position data line 171, e.g., as described in Jeon-078 at the time of alleged invention in 2014.

466. Accordingly, limitation 24[c] is disclosed by Moon in combination with Jeon-078.

- e. 24[d]: “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line; and”

467. In my opinion, Moon teaches or suggests limitation 24[d].

468. Moon discloses a “second” TFT as initialization TFT T4 (shown in yellow in annotated Fig. 3 below). Moon explains that “transistor T4 is turned on in response to the previous scan signal Sn-1 of the low level, an **initialization power Vint is supplied from an initialization power line 124 to the driving transistor T1 through an initialization thin film transistor T4**, so that the driving transistor T1 is initialized.” Moon, ¶54. This configuration is illustrated in Fig. 3, annotated below, which shows drain region D4 of TFT T4 (“one end of second semiconductor”) is connected to gate G1 of TFT T1 (red line A) that resides in the first electrode layer (see limitation 24[b]), and source region S4 of T4 (“other end of the second semiconductor”) is connected to initialization power line 124 (“a voltage line”) (blue line B).

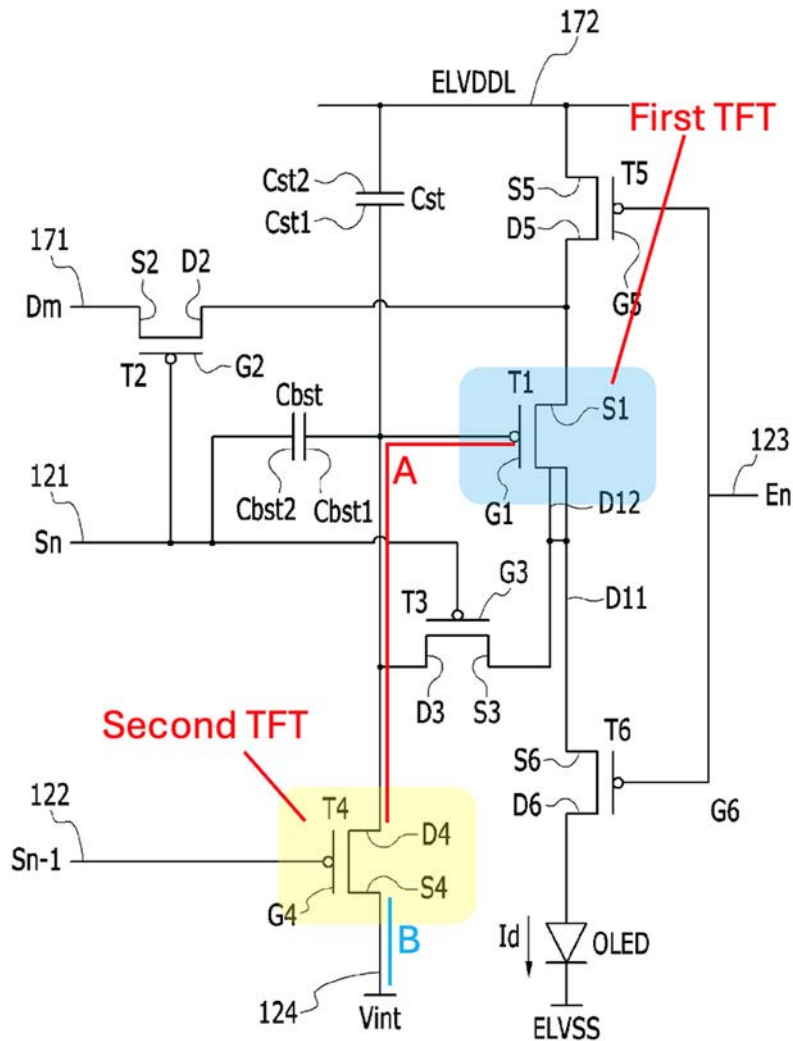


Fig. 3

469. I have also annotated Moon's Fig. 4 below to illustrate the connection (shown by red line A in annotated Fig. 3 above) between the semiconductor region associated with D4 and gate G1 (green arrow) (Moon, ¶¶72, 76, 79), and the connection between the semiconductor region associated with S4 and Vint through contact holes 162, 189 and metal pattern 82 (blue circle). Id., ¶79.

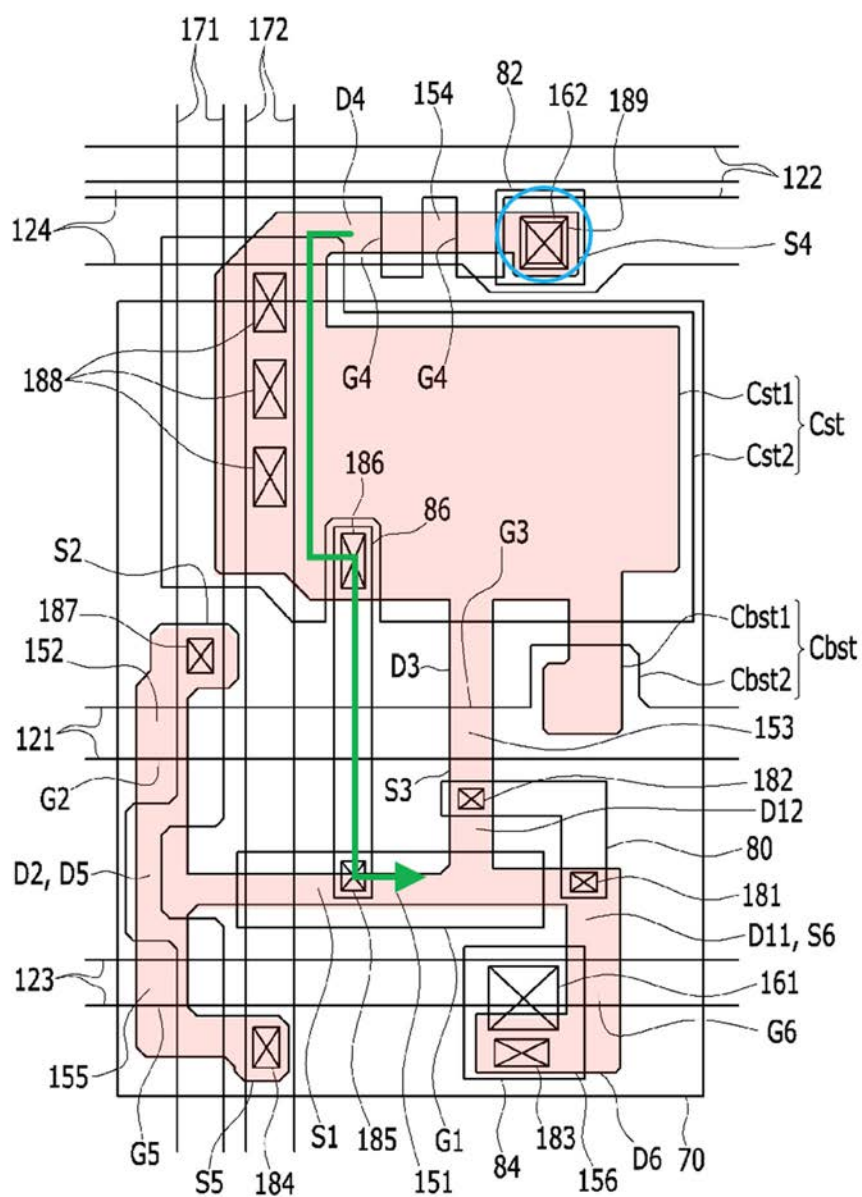


Fig. 4

470. Accordingly, limitation 24[d] is disclosed by Moon.

- f. 24[e]: “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.”**

471. In my opinion, Moon in combination with Jeon-078 teaches or suggests limitation 24[e].

472. Moon shows “a shield layer” in the form of initialization power line 124 as shown in annotated Fig. 4 below (green). As shown in annotated Fig. 4 below, TFT T4 has two gate electrodes, denoted by the red dashed circles and labeled G4 overlapping a semiconductor 154 channel. The shield layer overlaps a part between the first channel area and second channel area of the semiconductor portion of T4 (“second semiconductor”). As I have explained in Ground 2B, a POSITA would have known, based on at least on the layout and annotations of Fig. 4, that T4 in Moon is double gated, and the semiconductor below the two gate electrodes form the “first” and “second” channel regions. See also §VIII.D.3.f regarding the discussion of Ground 2B, Claim 24, limitation 24[e].

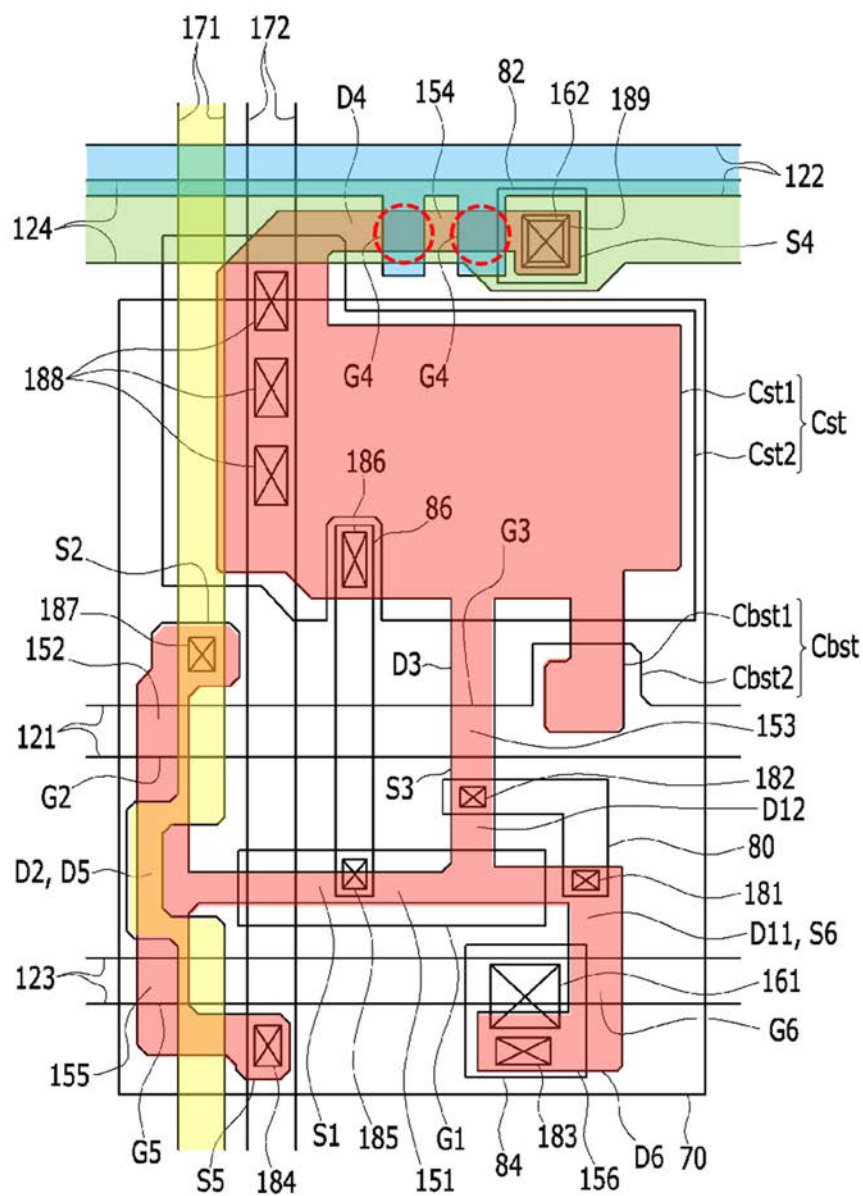


Fig. 4

473. While Moon does not explicitly describe the relative vertical positioning of initialization power line 124 and data line 171, Jeon-078 explains that initialization power line 124 (referred to as “initialization voltage line 124” in Jeon-078) is in a layer below data line 171 and above the semiconductor (“channel area”)

of T4. I note here that although power lines are often located on a top layer, they must be connected to circuit elements and therefore extend into other layers with vias (contact holes), as needed for a circuit layout. Jeon-078 explicitly describes such a configuration, which would have reduced wire lengths for the layout.

474. Specifically, Jeon-078 explains initializing voltage line 124 is formed in the same layer as second storage capacitor plate 127 and top plate 129 of its boost capacitor (Jeon-078, ¶67), Fig. 4 of Jeon-078 (annotated below) shows top plate 129 of the boost capacitor (shown in blue) is positioned over gate insulating layers 141 and 142, which are formed over semiconductor layer 131 (shown in red). Jeon-¶¶79, 89, 91. Therefore, Jeon-078's initialization voltage line 124 is in a layer above the semiconductor of T4 but below data line 171 (shown in yellow).

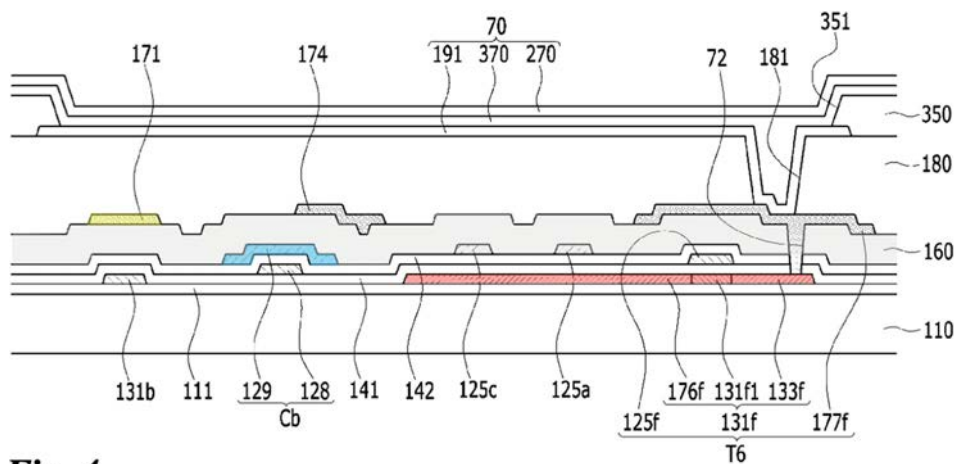


Fig. 4

475. In the Moon-Jeon-078 combination, to the extent Moon does not explicitly describe such a relative vertical positioning of data line 171 and

initialization voltage line 124, it is my opinion that a POSITA would have been guided by the teachings of Jeon-078 to position initialization voltage line 124 below data line 171 but above the semiconductor of T4. Such a modification would be a routine and known way to position the data and voltage lines, as described in Jeon-078 and other references at the time of alleged invention in 2014. See §VI.D.

476. I further note that voltage line 124 in the Moon–Jeon-078 combination would have been a shield for the same reasons as discussed in Ground 2B, Claim 24, limitation 24[e] (see §VIII.D.3.f), and is consistent with the '015 Patent.

477. Accordingly, limitation 24[e] is disclosed by Moon in combination with Jeon-078.

4. Claim 25

- a. **25[a]: “... wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and”**

478. In my opinion, Moon teaches or suggests limitation 25[a].

479. See the discussion of limitation 24[e] above. As shown in annotated Fig. 4 of Moon above, gate electrodes G4 (annotated in red circles in annotated Fig. 4) are formed at locations where previous scan line 122 (shown in blue) overlaps the semiconductor layer. *Id.*, ¶73: “...the previous scan line 122 has the gate electrode

G4 overlapping the semiconductor 154 of the initialization transistor T4.” Both gates are part of previous scan line 122 and are therefore in the same layer.

480. In my opinion, a POSITA would have thus understood from Fig. 4 that T4 of Moon had a double-gated structure with a first gate electrode (one of the G4 labels) that overlapped a corresponding part of the semiconductor below it (i.e., semiconductor 154), and a second gate electrode (the other of the G4 labels) that overlapped a corresponding part the semiconductor below it. *See also* the discussion of Ground 2B, Claim 24, limitation 24[e] in §VIII.D.3.f. Also, as I have discussed in §VI.E, such double-gated TFTs are well-known to reduce leakage as shown in Moon.

481. Accordingly, limitation 25[a] is disclosed by Moon.

b. 25[b]: “wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.”

482. In my opinion, Moon teaches or suggests limitation 25[b].

483. As shown in annotated Fig. 4 (below), Moon’s gate electrodes, G4, are part of previous scan line 122 (“second signal line” shown in blue) which is substantially perpendicular to, and thus “crossing,” data line 171 (“first signal line” shown in yellow).

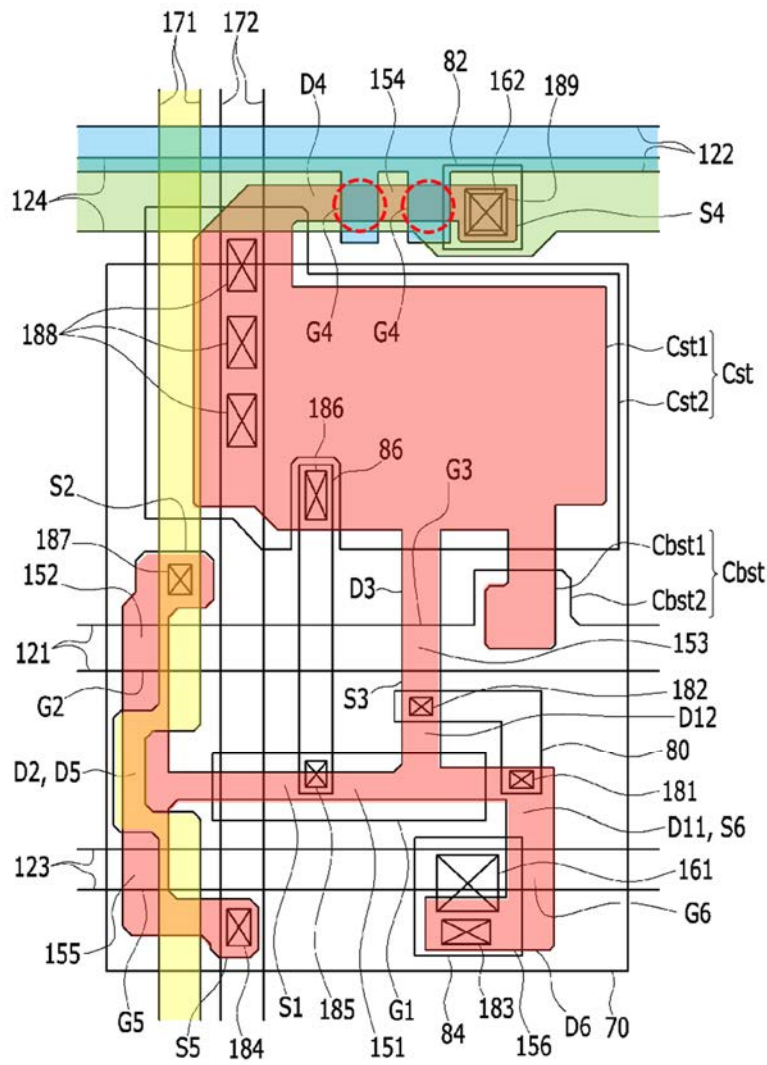


Fig. 4

484. Moon does not explicitly state that the gate electrode of TFT T4 is in the same layer as the first electrode layer (i.e., the layer that contains the gate electrode of T1). However, it is my opinion that it would have been obvious to a POSITA for the gate electrodes of T4 to be in the same layer as gate electrode G1 of TFT T1 because the semiconductors that form T1 and T4 were in the same layer, as shown by the continuous red region marked in Moon's Fig. 4 as annotated above,

and therefore it would have been obvious that the gate electrodes would be on the same layer overlapping the semiconductor. Here, I note that the gates in a TFT should be located as close as possible (accounting for the gate insulating layer) to the channel (semiconductor 154) so that the gates function as well as possible to control current through the channel. This is a standard design for TFTs and therefore if the semiconductor material is in a common layer, the gates would likewise be in a common layer.

485. Accordingly, limitation 25[b] is disclosed by Moon.

5. Claim 26: "... wherein the shield layer is a part of the voltage line."

486. See the discussion of Ground 3, Claim 24, limitation 24[e], where the shield layer is part of initialization voltage line 124.

487. Accordingly, Claim 26 is disclosed by Moon.

6. Claim 27: "... further comprising a connecting line connecting the one end of the second semiconductor and the first electrode layer and being in the same layer as the first signal line."

488. In my opinion, Moon in combination with Jeon-078 teaches or suggests Claim 27.

489. Below, I have annotated Fig. 3 of Moon with line A to show that drain D4 of TFT T4 ("one end of the second semiconductor") is connected to gate electrode G1 of TFT T1 that is part of the "first electrode layer."

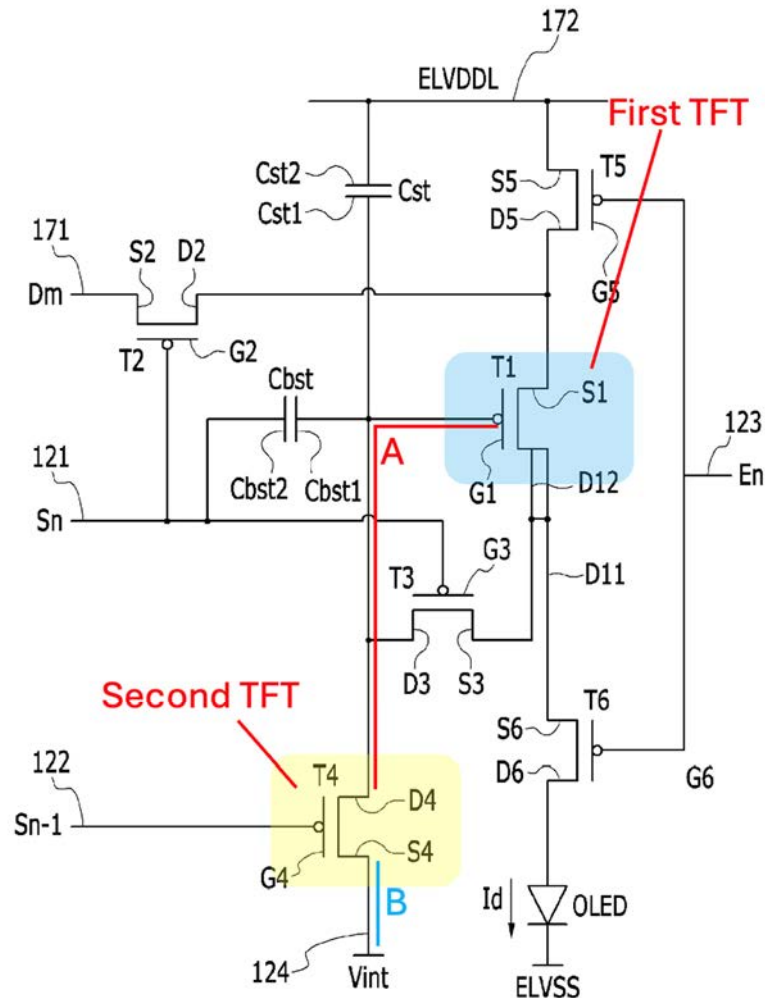


Fig. 3

490. Moon's connectivity between G1 and D4 is implemented though connection member 86 and contact holes 185, 186, which connect G1 to lower capacitor plate Cst1, which is connected to D4. *Id.*, ¶76. I note that although Moon does not explicitly disclose that the connecting line is in the same layer as data line 171 ("first signal line"), Jeon-078 discloses a connection member 174 (highlighted in yellow) that connects the drain of T4 (labeled D4) to the gate of T1 (labeled G1

and colored blue) through a via (contact hole 67), as shown in annotated Fig. 3 below.

Jeon-078, Fig. 3.

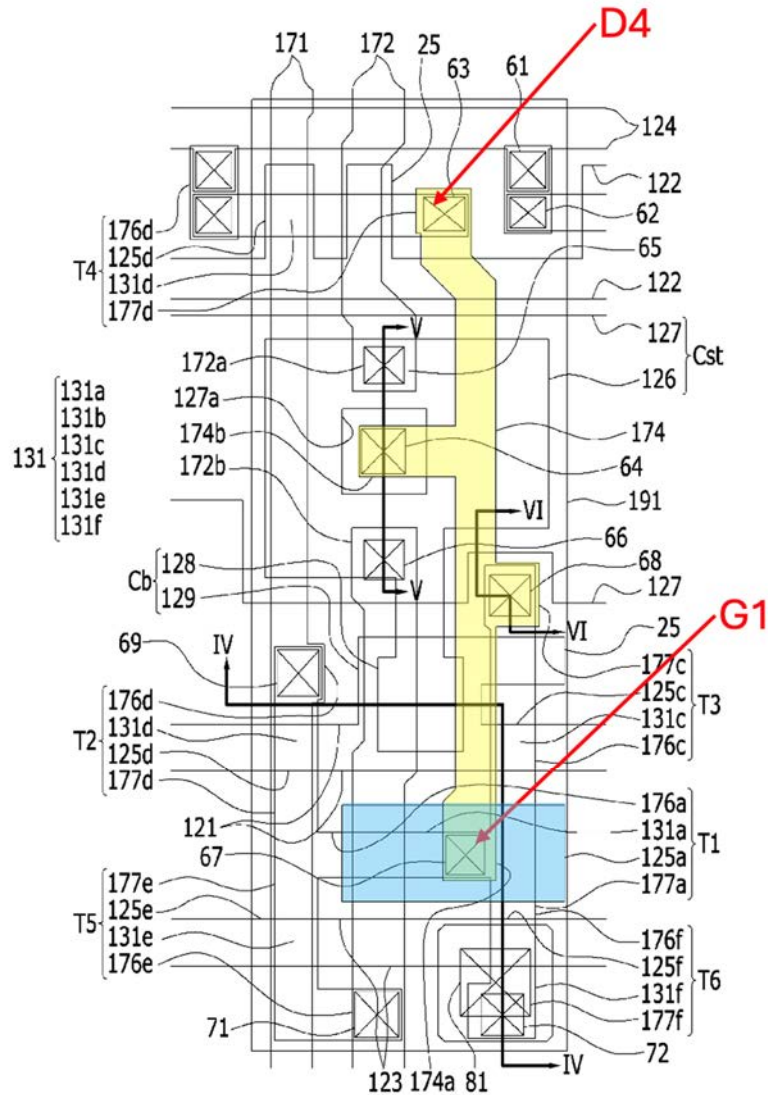


Fig. 3

491. Jeon-078 explains, “**The connection member 174 is formed in the same layer to be parallel to the driving voltage line 172.** The connection member 174 connects the driving gate electrode 125a and the first storage capacitor plate 126.

One end 174a of the connection member 174 is connected to the driving gate electrode 125a.” *Id.*, ¶78. Jeon-078 also explains, “The initialization drain electrode 177d is the other end of a connection member 174.” *Id.*, ¶70.

492. As shown in Fig. 4 of Jeon-078, annotated below, connection member 174 and data line 171 (both shown in yellow) are in the same layer.

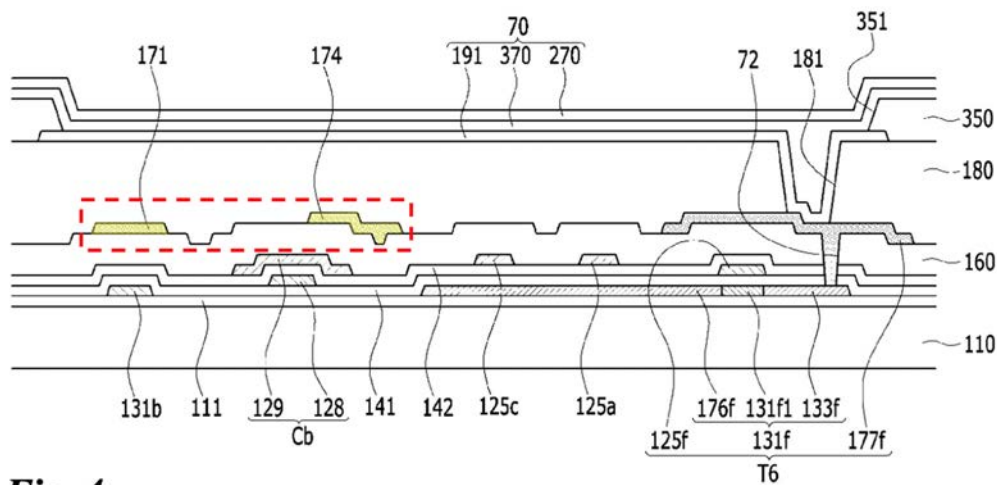


Fig. 4

493. In my opinion, it would have been obvious to place the connection member in the Moon-Jeon-078 combination in the same layer as data line 171, as they were substantially parallel to one another, and placing them in the same layer provided for simpler circuit design and manufacturing. Furthermore, there is a motivation to use existing layers to reduce the number of expensive metal layers – sharing a layer for multiple wires is standard layout practice. Similarly, using a metal connector and associated contact holes to connect two elements in an OLED circuit layout was a routine task, the placement of the connection line in the same layer as

the signal line 171 was taught by Jeon-078, and its implementation would have been well within the skillset of a POSITA.

494. Accordingly, Claim 27 is disclosed by Moon in combination with Jeon-078.

G. Ground 4A: Masao Renders Obvious Claims 1, 2, 8, 9, 10, and 33

1. Summary of Masao

495. Masao is directed to a display technology that uses an active-matrix driving-type electro-optical device using TFTs (Masao, ¶2), and in particular to addressing the effects of noise that arise when signal lines are in close proximity. Masao addresses the problem of noise in signals on signal lines by providing a shield made of a conductive film, which electrically shields the signal line. Masao, ¶8.

496. As I have explained in §III.A, the claims of the '015 Patent do not recite or require an OLED device. '015 Pat., 17:12-20-57. Notably, the preamble of each independent claim generally recites: “A display apparatus comprising.” *Id.* Furthermore, the specification of the '015 Patent makes it clear that its embodiments are “**not limited to an organic light-emitting display apparatus**. An image having high quality may be displayed as long as a display apparatus including a TFT and a data line in a (sub) pixel has a shield layer in the same or similar manner described above.” *Id.*, 16:63-67. Accordingly, Masao, which describes an active-matrix driving-type electro-optical device using TFTs and provides a shield to mitigate the

effects of electrical noise from signal lines, is directly relevant to the claims and description of the '015 Patent. As previously discussed in §VI.D, the use of shields to reduce EMI was well known in the electronic arts and specifically in the display industry prior to the '015 Patent.

497. In my opinion, although Masao does not specifically describe an OLED display, a POSITA would have understood that OLED displays and LCD displays have many similarities, utilize TFTs, and encounter many similar challenges. Both LCD and OLED displays can (and typically do) use thin-film-transistor circuits. Therefore, circuit challenges faced by an LCD TFT control circuit will likely be seen in an OLED display TFT control circuit. Further, all TFT (and integrated circuits) share common concerns with EMI and shielding, regardless of the application. Thus, a solution for one circuit is likely to be useful for another related circuit.

2. Claim 1

a. 1[pre]: “A display apparatus comprising:”

498. In my opinion, Masao teaches or suggests limitation 1[pre].

499. Masao relates to a display apparatus. In particular, Masao relates to “electro-optical devices such as liquid crystal devices.” Masao, ¶1. Masao explains that Fig. 1 “is an equivalent circuit of various elements, wiring, and the like in a plurality of pixels formed in a matrix constituting an image display region of the electro-optical device.” *Id.*, ¶50.

500. Accordingly, limitation 1[pre] is disclosed by Masao.

- b. **1[a]: “a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;”**

501. In my opinion, Masao teaches or suggests limitation 1[a].

502. Masao discloses a circuit that includes a first TFT.⁶ Masao describes “a pixel electrode 9a and **a TFT 30** for switching control of the pixel electrode 9a.” Masao, ¶51, Fig. 1 (below).

⁶ Masao’s Fig. 1 shows nine identical circuits, each including a TFT 30, a capacitor 70 and a pixel electrode 9a. Only one of the nine identical circuits of Masao is used to show obviousness of the challenged claims in this Ground.

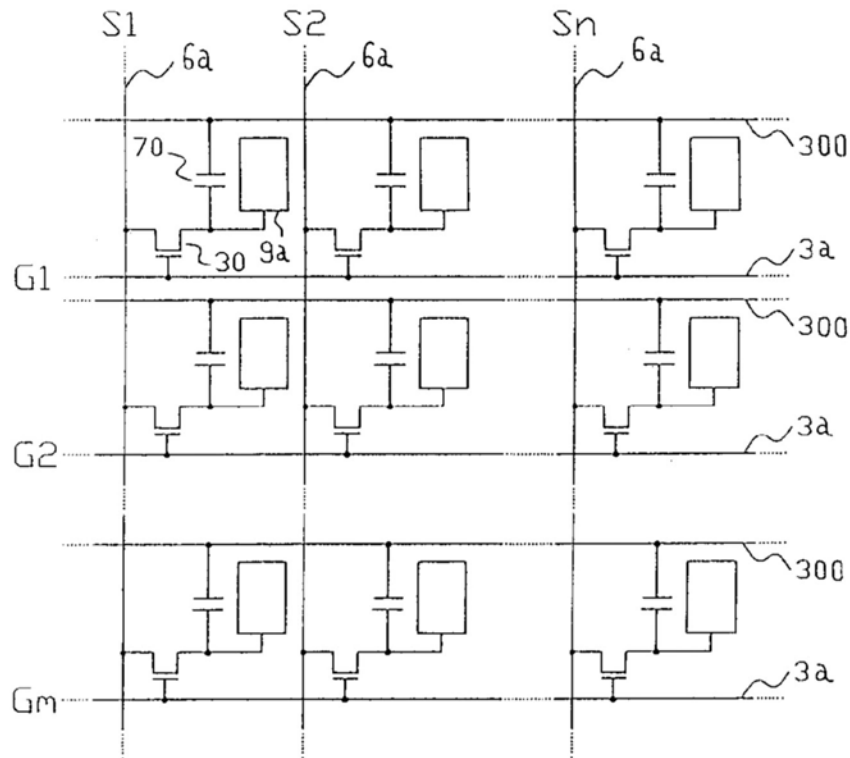


Fig. 1

503. TFT 30 includes a source area, channel area, and drain area in semiconductor layer 1a (“first semiconductor layer”), shown in partial Fig. 3 of Masao below. Masao explains, “In FIG. 3, **the TFT 30** for pixel switching has a LDD (lightly doped drain) structure, and is provided with: the scan line 3a, the **channel region 1a’** of the semiconductor layer 1a in which a channel is formed by an electric field from the scan line 3a, an insulating thin film 2 including a gate insulating film for insulating the scan line 3a and the semiconductor layer 1a, the **low concentration source region 1b** and the **low concentration drain region 1c**

of the semiconductor layer 1a, and the **high concentration drain region 1e** and the **high concentration source region 1d** of the semiconductor layer 1a.” Masao, ¶69.

504. As shown in partial Fig. 3 of Masao, annotated below, channel region 1a’ is between the source regions and drain regions.

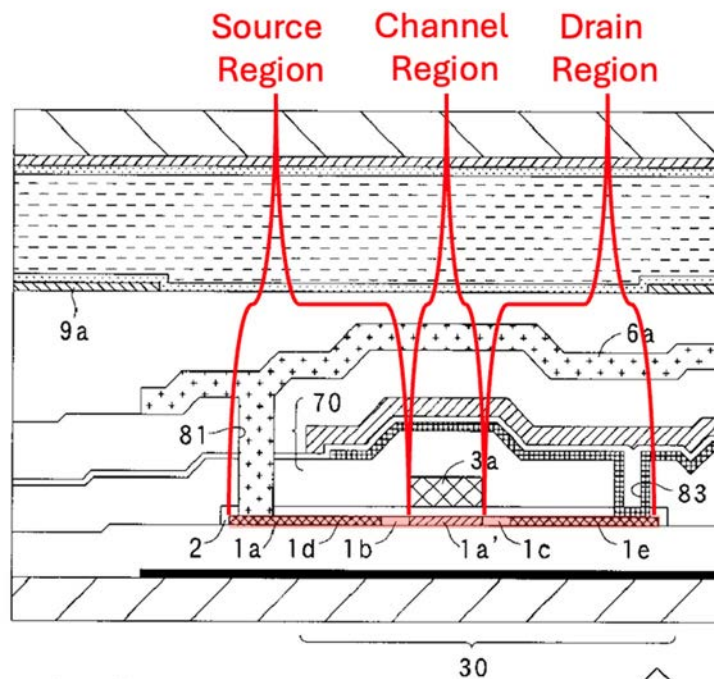


Fig. 3

505. Masao discloses a TFT structure in which the source and drain regions have high- concentration and low-concentration doped regions. In my opinion, it would have been obvious to a POSITA that the inclusion of both high and low-concentration regions is a design choice and that the high- and low-concentration source regions together constitute a source region (and similarly, the high- and low-concentration drain regions together constitute a drain region), and the channel

region is disposed between the source and drain regions, as is typical of TFTs. Thin-film transistors generically require a source region supplying current connected to a source electrode, a drain region for receiving the current connected to a drain electrode, and a channel for modulating the current with a gate electrode.

506. Accordingly, limitation 1[a] is disclosed by Masao.

c. **1[b]: “a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;”**

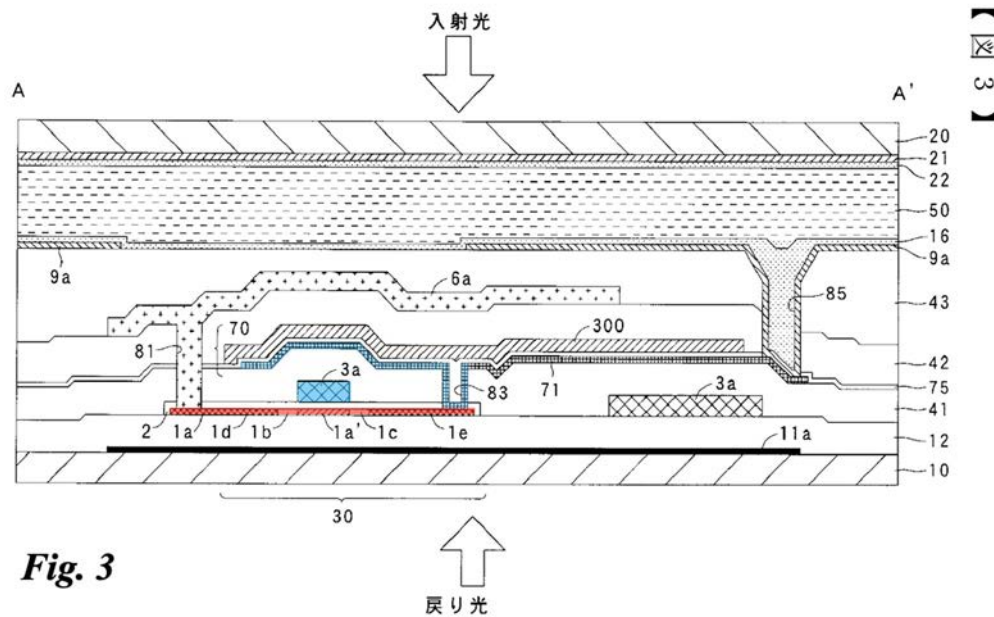
507. In my opinion, Masao teaches or suggests limitation 1[b].

508. As a preliminary matter, I note that the '015 Patent does not define a first electrode layer, but limitation 1[b] outlines specific minimum requirements for the “first electrode layer.” Masao discloses the claimed first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor in several ways. The annotated figures below detail three mappings.⁷

509. **Mapping #1.** Fig. 3, annotated below in blue, shows a first mapping in which the first electrode layer is treated as a layer that includes scan line 3a (gate electrode), relay layer 71 (lower capacitor electrode), and at least the conductive portion within first interlayer insulating film 41 that connects the drain of the TFT

⁷ Unless otherwise noted, any of the “first electrode layer” mappings can be used to show obviousness of limitations of the Challenged Claims.

30 (drain electrode) with the relay layer 71. The described layer in Mapping #1 is an electrode layer (shown in blue) because it includes one or more electrodes and is over the semiconductor layer (highlighted in red).



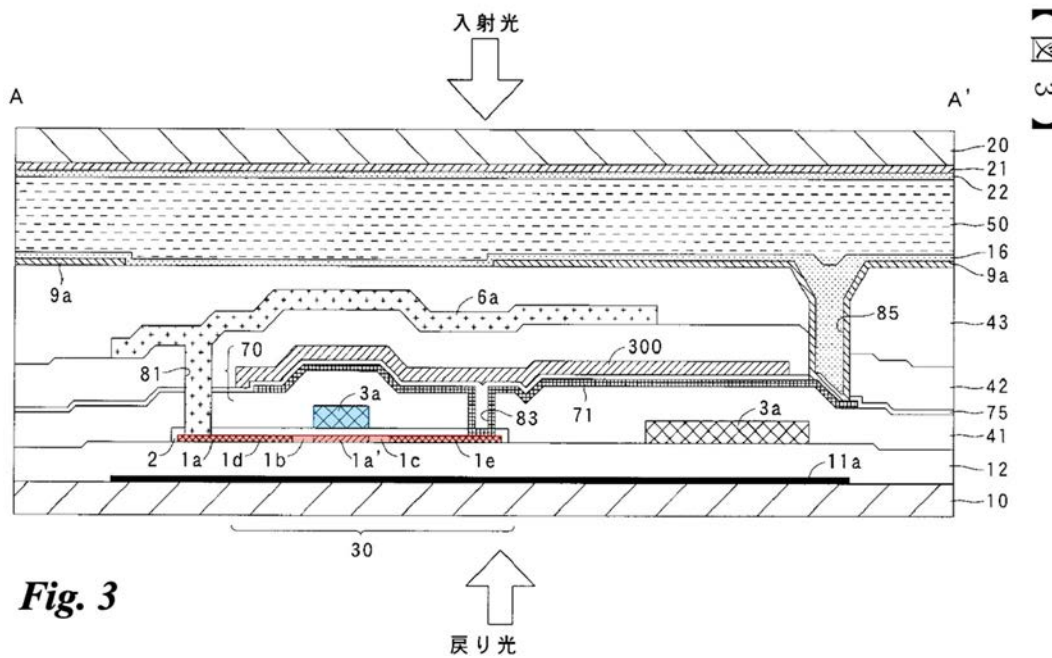
510. Specifically, Masao describes that “the storage capacitor 70 is formed by disposing the following so as to oppose each other, sandwiching a dielectric film 75: **a relay layer 71 serving as a pixel potential side capacitance electrode** connected to a high concentration drain region 1e (and the pixel electrode 9a) of the TFT 30, and one part of a capacitance line 300 serving as a constant potential-side capacitance electrode.” Masao, ¶54. Masao further describes that “the scan line 3a is disposed so as to face a channel region 1a’ . . . in a semiconductor layer 1a, and **the scan line 3a functions as a gate electrode.**” Masao, ¶53. Masao describes the

contact to the drain of TFT 30: “A first interlayer insulating film 41, having drilled therein... **the contact hole 83 leading to the high concentration drain region 1e,** is formed on the scan line 3a.” Masao, ¶70. Accordingly, it is my opinion that at least part of the contact hole that connects to the high-concentration drain region is a drain electrode. Electrical contact hole 83 (e.g., via) typically passes through interlayer insulating films 41 (e.g., an interlayer dielectric or ILD layer to connect electrodes to source, gate, and drain semiconductor areas) as is shown by Masao. The electrodes form an electrode layer.

511. **Mapping #2.** Fig. 3, annotated below, shows a second mapping for the first electrode layer (blue) that includes relay layer 71 (e.g., bottom capacitor electrode) but does not include scan line 3a and the conductive portions within first interlayer insulating film 41. Masao, ¶54: “...**a relay layer 71 serv[es] as a pixel potential side capacitance electrode.**” I note here that relay layer 71 forms a drain electrode as well as a capacitor plate and therefore constitutes an electrode layer.



contact holes 81, 83, and can therefore constitute an electrode layer.



513. Additionally, I note that the extent of “first electrode layer” in all three mappings is not limited to an individual pixel of Masao, but the “layer” extends to neighboring pixels that include electrodes of neighboring pixels.

514. Accordingly, limitation 1[b] is disclosed by Masao.

d. 1[c]: “a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;”

515. In my opinion, Masao teaches or suggests limitation 1[c].

516. Masao discloses “a second electrode layer” as the layer that includes capacitance line 300. Masao states, “[t]he relay layer 71 and the capacitance line 300 are formed on the first interlayer insulating film 41.” Masao, ¶71. The

capacitance line 300 (“second electrode layer”) is shown in green in annotated Fig. 3 below.

517. For brevity, annotated Fig. 3 below shows the first electrode layer based on Mapping #1, but it will be readily appreciated that the same second electrode layer can also be used for Mappings #2 and #3 of the first electrode layer. I note that limitation 1[c] does not limit what conductors can serve as a “second electrode layer” and therefore any suitable conductors found in a layer at an appropriate level in the multi-layer circuit can be a “second electrode layer”.

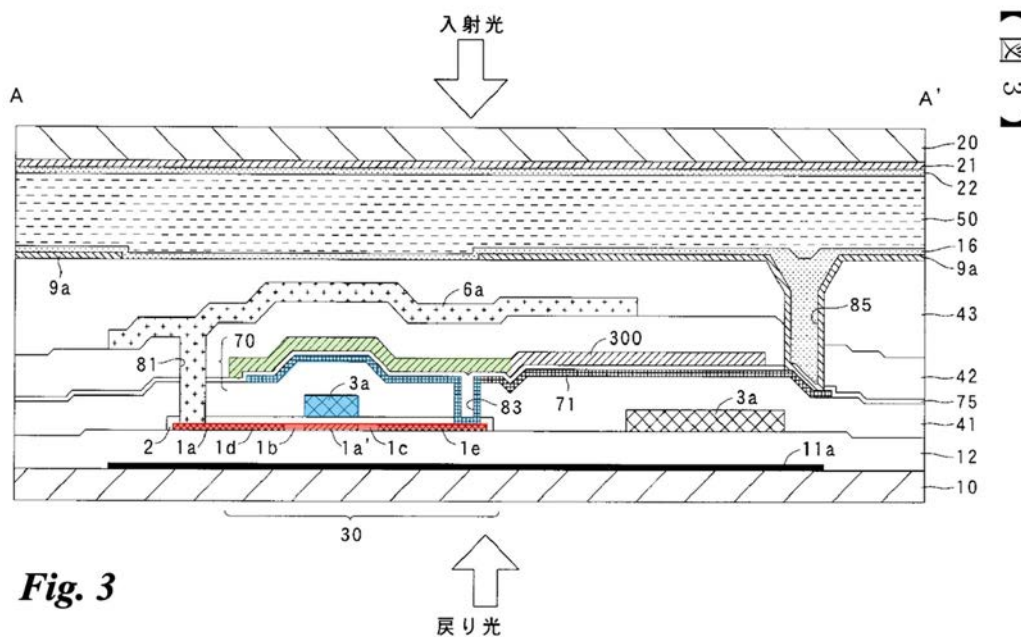


Fig. 3

518. Accordingly, limitation 1[c] is disclosed by Masao.

e. 1[d]: “a first signal line over the second electrode layer; and”

519. In my opinion, Masao teaches or suggests limitation 1[d].

520. Masao discloses “a first signal line over the second electrode layer” as data line 6a. As shown in annotated Figs. 2⁸ and 3 below, data line 6a (shown in yellow) is a signal line that is in a layer over capacitance line 300 (“second electrode layer”). Masao states, “... in the image display region, a second conductive film that forms **the data line 6a is laminated on the first conductive film that forms the capacitance line 300 via the interlayer insulation film.**” Masao, ¶93. Data lines are often routed on a top layer to provide thicker more conductive wires, ease of connection, and ready testing and are then connected to wires in lower layers using contact holes (vias).

⁸ Masao’s Fig. 2 shows four full identical pixels and associated circuits (and partial components of the neighboring pixels). Only one pixel and associated circuit of Masao is used to show obviousness of the challenged claims in this Ground. However, in some instances, to avoid clutter, components of one or more adjacent pixels in Fig. 2 are annotated to illustrate how Masao teaches or suggests the claim limitations.

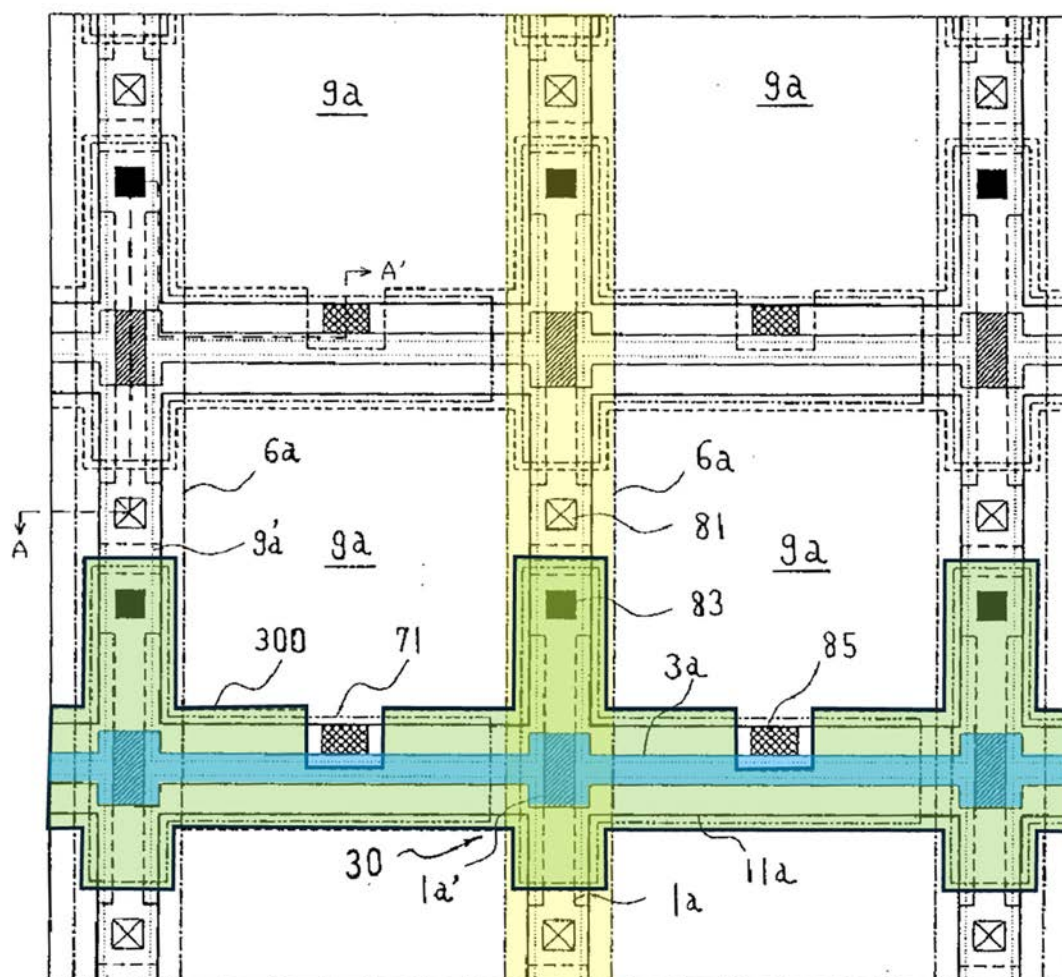


Fig. 2

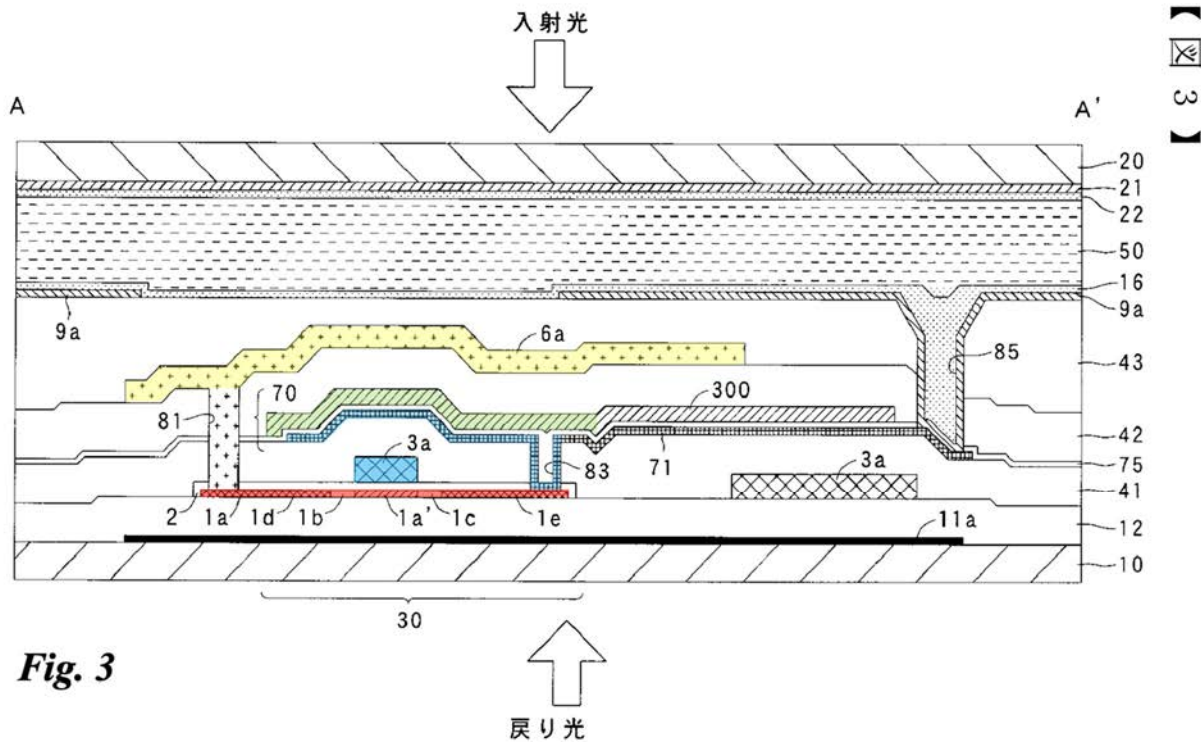


Fig. 3

521. Accordingly, limitation 1[e] is disclosed by Masao.

- f. **1[e]: “a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.”**

522. In my opinion, Masao teaches or suggests limitation 1[e].

523. Masao describes “the first shield layer” as the capacitance line 300 (or a part thereof), as annotated in Figs. 2 and 3 (below) in green.⁹

⁹ While annotated Fig. 3 shows Masao’s shield layer with Mapping #1 for the first electrode layer, I note that the interpretation of the shield layer remains the same for Mappings #2 and #3 of the first electrode layer.

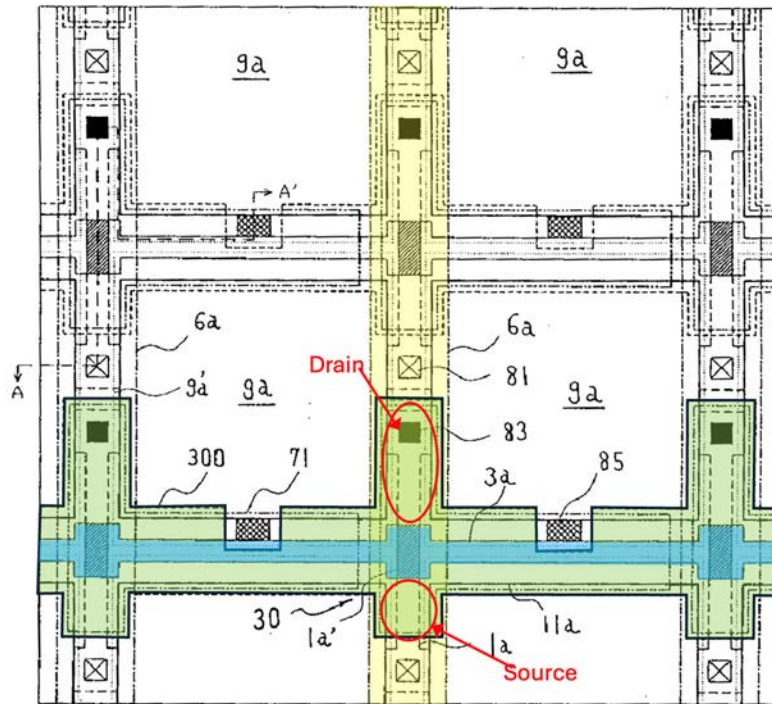


Fig. 2

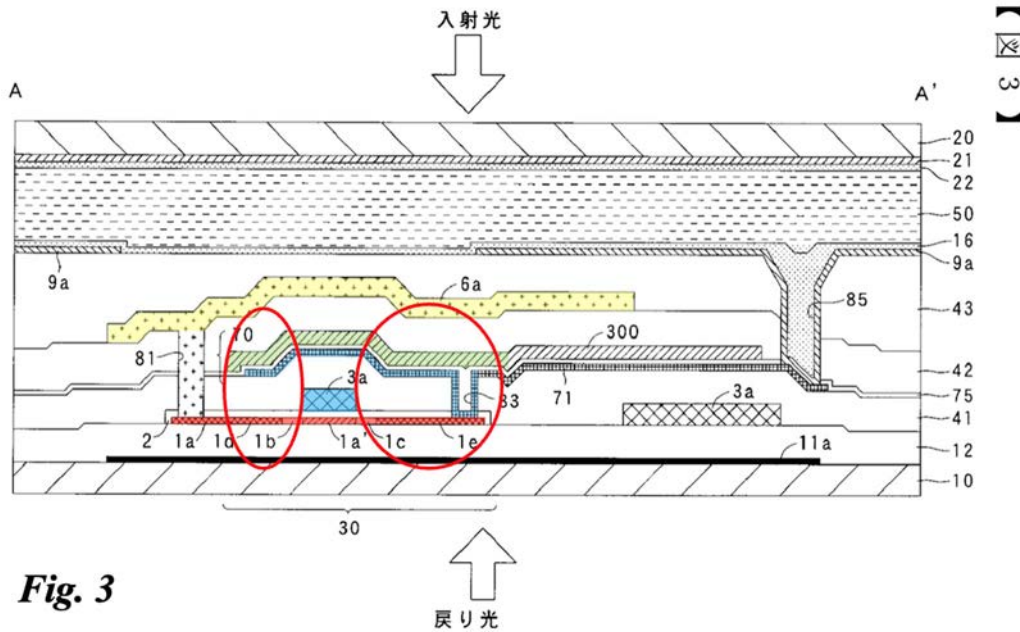


Fig. 3

524. As evident from Fig. 3 above, a portion of capacitor line 300 (“first shield layer” shown in green) is in a layer between data line 6a (“first signal line” shown in yellow) and semiconductor layer 1a-1e (“first semiconductor” shown in red), and overlaps a part of the source area (1d/1b) and drain area (1c/1e) of the first semiconductor. Therefore, in my opinion, the claimed “first shield layer” can be limited only to the portion of capacitance line 300 that overlaps part of the source and drain areas of the first semiconductor of the first TFT. This is also evident from annotated Fig. 2 (above), where the capacitor line 300 (green) overlaps a portion of the source and the drain area of the TFT, shown in red ovals.

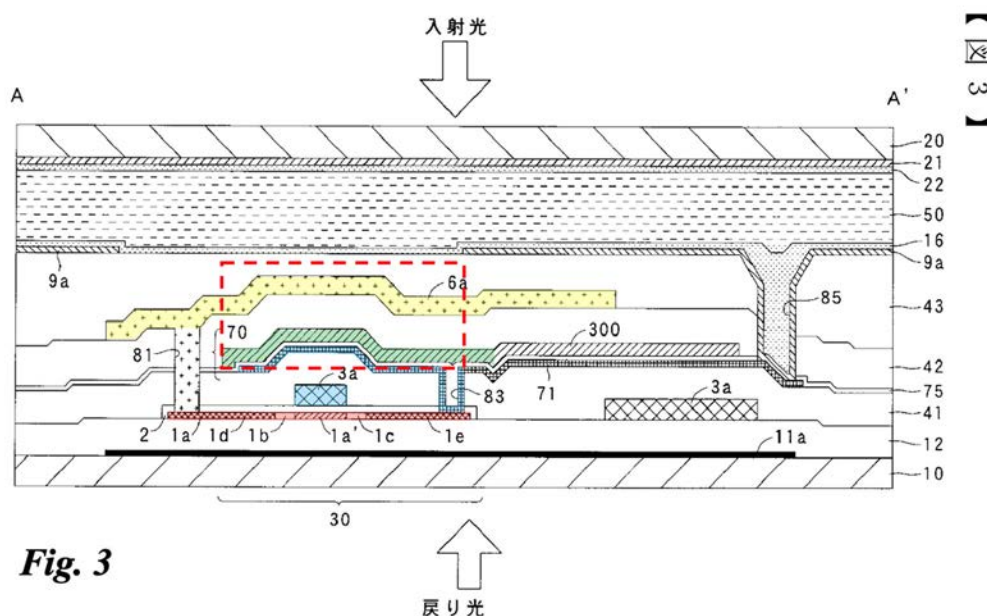
525. Masao does not label the capacitance line 300 as a “shield” but describes that the capacitance line 300 is supplied with a constant voltage. Masao, ¶51: “...capacitance line 300, which includes a constant potential-side capacitance electrode of a storage capacitor 70 and which is fixed to a constant potential;” *see also id.*, ¶54 and Fig. 1, illustrating line 300 is connected to a voltage line VSSY. It is my opinion that a POSITA would have therefore understood that capacitance line 300 being connected to a constant voltage line and placed between data line 6a and semiconductor layer 1a, shielded the TFT from noise on signal line 6a. This interpretation of using a capacitor plate as a shield is also consistent with the ’015 Patent’s description. ’015 Pat., 13:47-48; *see also* §VIII.A.2.f.

3. Claim 2: "... wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line."

526. In my opinion, Masao teaches or suggests Claim 2.

527. As explained in 1[c] and 1[e], Masao describes a "second electrode layer" as capacitance line 300, and "the first shield layer" as the capacitance line 300 (or a portion thereof) that overlaps a part of the source area and the drain area of the first semiconductor and therefore shields it. See §§VIII.G.2.d and VIII.G.2.f, *supra*. Therefore, Masao's first shield layer is part of the second electrode layer.

528. Further, as shown in annotated Fig. 3 below, a portion of Masao's capacitance line 300 ("first shield layer" shown in green) overlaps part of data line 6a ("first signal layer" shown in yellow) as shown in the red dashed box.



529. Annotated Fig. 2 also shows Masao's capacitance line 300 ("first shield layer" shown in green) overlaps a part of data line 6a ("first signal line" shown in yellow). Masao explains, "When viewed in a planar manner, the capacitance line 300 extends in a stripe along the scan line 3a, with locations overlapping the TFT 30 protruding vertically in FIG. 2." Masao, ¶56.

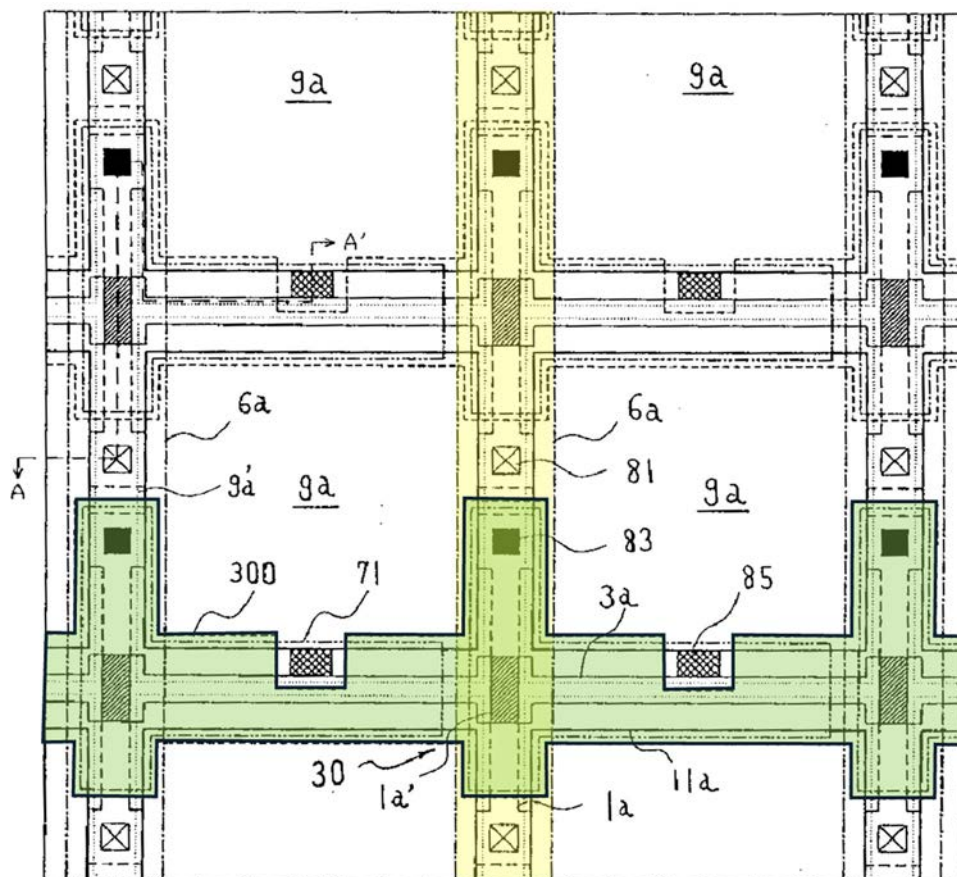


Fig. 2

530. Accordingly, Claim 2 is disclosed by Masao.

4. **Claim 8:**

- a. **8[pre]: “... wherein the first signal line extends in a first direction, and”**

531. In my opinion, Masao teaches or suggests limitation 8[pre].

532. Data line 6a (“first signal line”) extends in a first direction as indicated in annotated Fig. 2 (below). Accordingly, limitation 8[pre] is disclosed by Masao.

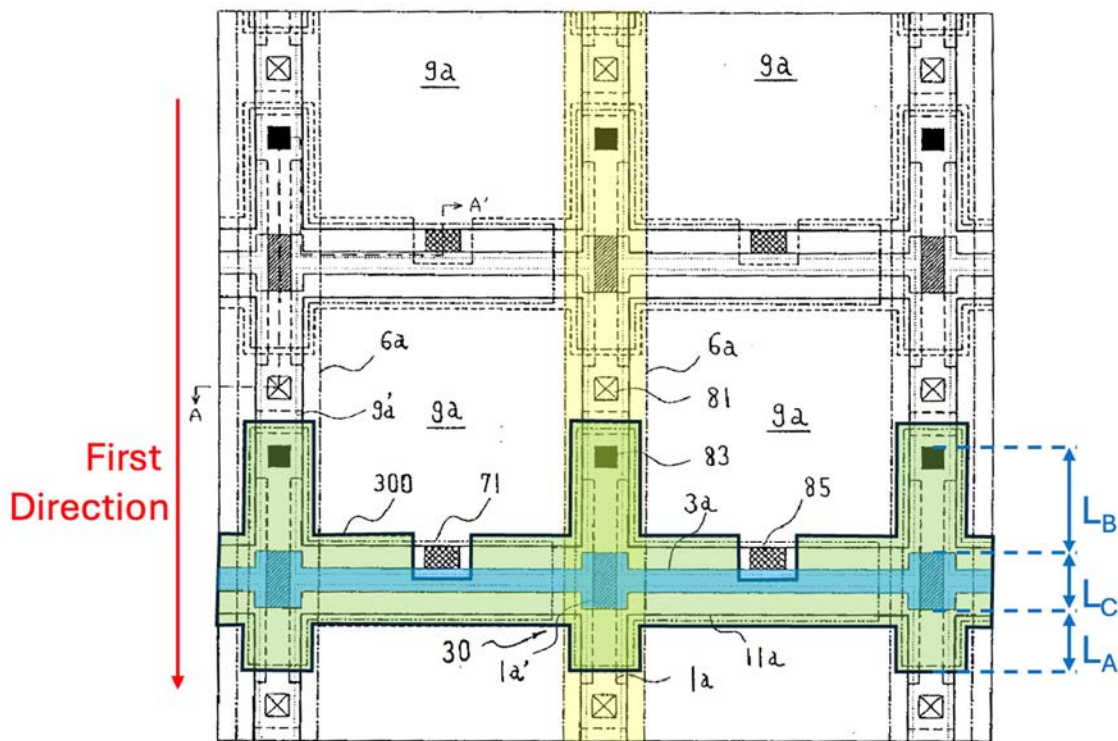


Fig. 2

- b. **8[a]: “wherein a length along the first direction of the overlapping part of the first shield layer with the part of one of the source area and the drain area of the first semiconductor is larger than a length of the first electrode layer along the first direction.”**

533. In my opinion, Masao teaches or suggests limitation 8[a].

534. A length along the first direction of the overlapping part of the first shield layer (capacitance line 300, green) with the source area (denoted L_A) and drain area (L_B) are shown in annotated Fig. 2 above. A length of the first electrode layer (i.e., scan line 3a, blue) in the first direction (L_C) is also annotated in Fig. 2. As shown, at least L_B is larger than L_A , thus meeting claim limitations. In general, it is useful for the shield to overlap all of the source, gate, and drain to reduce EMI rather than overlapping only the gate (scan line 3a) and the shield would preferably be designed to do so, if possible. In my opinion, because Claim 8 recites “a” length, L_C annotated in Fig. 2 represents “a” length of the first electrode layer in the first direction as recited in the claim. In the above analysis, either Mapping #1 or #3 of the “first electrode layer” is applicable because both mappings include scan line 3a that forms the gate of TFT.

535. Accordingly, limitation 8[a] is disclosed by Masao.

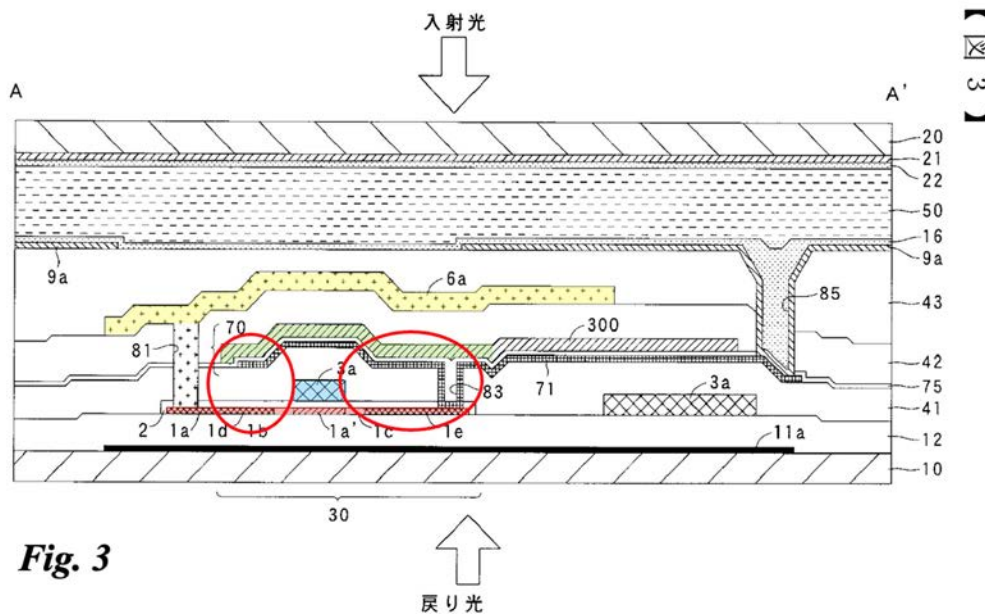
5. Claim 9: "... wherein the first shield layer fully overlaps the part of one of the source area and the drain area of the first semiconductor."

536. In my opinion, Masao teaches or suggests Claim 9.

537. As shown in annotated Figs. 2 and 3 below, the shield layer (300, shown in green) fully overlaps a part of the source and part of the drain, as indicated by the red ovals. I note that Claim 1 of the '015 Patent recites “a” part of the one of the source areas and the drain areas, and thus, in my opinion, there is no requirement

that the entire source area or the entire drain area be covered by the shield layer. Even covering a portion of the source and drain can reduce EMI, as shown in both '015 Patent and Masao.

538. Accordingly, Claim 9 is disclosed by Masao.



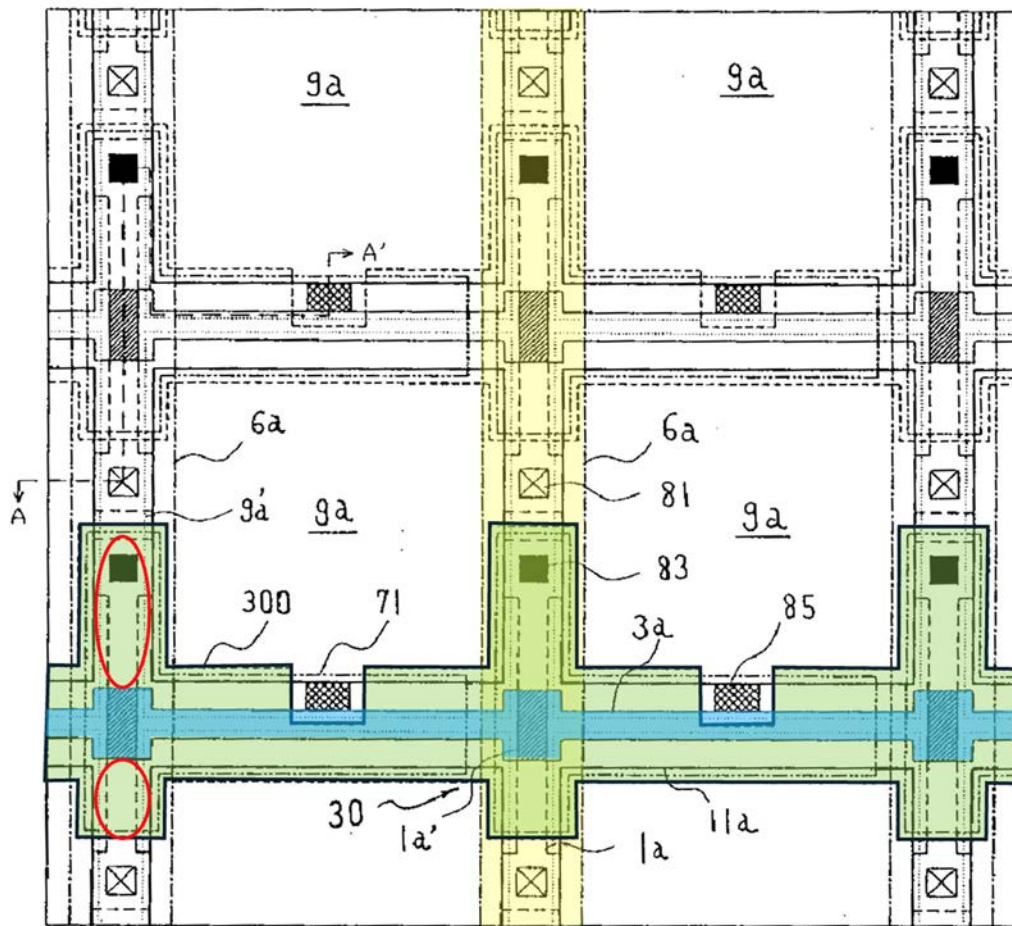


Fig. 2

6. Claim 10

- a. 10[a]: "The display apparatus of claim 1, wherein the first signal line extends in a first direction, and"**

539. In my opinion, Masao teaches or suggests limitation 10[a].

540. The first signal line (data line 6a, shown in yellow) extends in a first direction as shown in annotated Fig. 2 below. Accordingly, limitation 10[a] is disclosed by Masao.

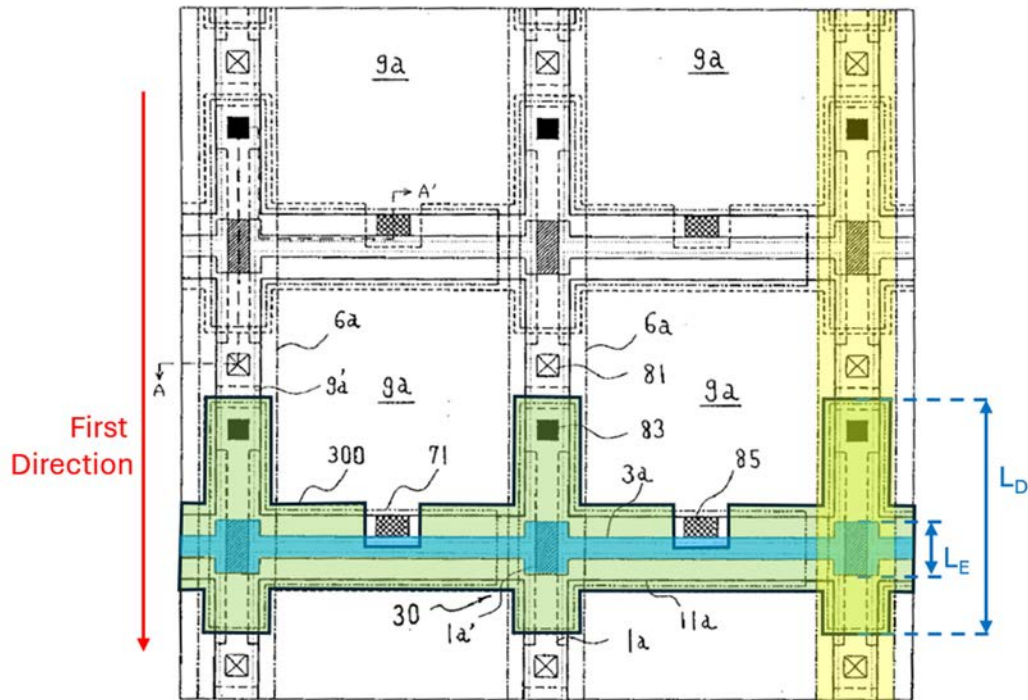


Fig. 2

- b. 10[b]: "wherein a length along the first direction of [[the]] an overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction."

541. In my opinion, Masao teaches or suggests limitation 10[b].

542. In Masao's circuit layout, the part of capacitor line 300 ("first shield layer") that overlaps with data line 6a ("first signal line"), denoted by L_D , is larger than a length along the first direction of scanning line 3a ("first electrode layer"), denoted by L_E . Masao explains the extension of capacitance line 300 ("the first shield layer") along the first direction: "When viewed in a planar manner, the capacitance line 300 extends in a stripe along the scan line 3a, with locations overlapping the TFT 30 protruding vertically in FIG. 2." Masao, ¶56. In the above analysis, either

Mapping #1 or #3 of the “first electrode layer” is applicable because both mappings include scan line 3a that forms the gate of TFT.

543. Accordingly, limitation 10[b] is disclosed by Masao.

7. Claim 33

a. 33[pre]: "A display apparatus comprising:"

544. See the discussion of limitation 1[pre] above.

b. 33[a]: "a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;"

545. See the discussion of limitation 1[a] above.

c. 33[b]: "a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;"

546. See the discussion of limitation 1[b] above.

d. 33[c]: "a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;"

547. See the discussion of limitation 1[c] above.

e. 33[d]: "a first signal line over the second electrode layer; and"

548. See the discussion of limitation 1[d] above.

- f. 33[e]: "a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor,"**

549. See the discussion of 1[e] above.

- g. 33[f]: "wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line,"**

550. See the discussion of Claim 2 above.

- h. 33[g]: "wherein the first signal line extends in a first direction, and**

551. See the discussion of 10[a] above.

- i. 33[h]: "wherein a length along the first direction of the overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction."**

552. See the discussion of 10[b] above.

553. Accordingly, Claim 33 is disclosed by Masao.

H. Ground 4B: The combination of Masao and Ohtani renders Claims 5, 11, 13, 28-29 and 31 obvious.

1. Summary of Ohtani

554. Ohtani relates to the structure for an active-matrix liquid-crystal panel that uses thin-film transistors (TFTs). Ohtani, 1:6-15. Ohtani provides various examples of display devices, such as cameras and portable phones, that utilize its liquid crystal panels. *Id.*, 9:38-10:33. I note that Ohtani describes that in some

implementations, multi-gated TFTs can be used, and in particular, an example TFT (shown in Fig. 10) where an active layer intersects with a gate wiring line at three places, creating a triple-gated TFT. *Id.*, 3:66-4:3, 6:20-21, 9:8-36, Fig. 10.

2. Motivation to Combine Masao and Ohtani

555. In my opinion, there are several reasons that motivate combining the teachings of Masao and Ohtani.

556. Both references related to display devices that utilized TFTs (Masao, ¶2; Ohtani, 1:6-15), such as liquid crystal displays (Masao, ¶49; Ohtani, 3:21-24) and sought to improve the operations of those devices. Masao, ¶47; Ohtani, 3:21-24, 9:32-36, 10:27-33. Therefore, in my opinion, given the related and complementary teachings of Masao and Ohtani, a POSITA would have found it obvious to improve the device of Masao based on the teachings of Ohtani. TFT circuits are generally useful for flat-panel display applications, regardless of the type of light-controlling technology used. The TFT circuits face similar design challenges and constraints, such as layout and EMI, as described in both Masao and Ohtani.

557. In the proposed combination, it is my opinion that a POSITA would have found it obvious to replace the single-gated TFT of Masao with a multi-gated TFT described in Ohtani. In doing so, a POSITA would found express motivation in Ohtani to adopt such a structure: “In the structure as shown in FIG. 10, three channels are formed in the active layer 11, and one-third of the voltage applied between the

source wiring line and the pixel electrode, is applied to the respective channels. **By this, the withstand voltage of a TFT can be increased.**” Ohtani, 9:32-36. Multi-gate channels (plural portions in Ohtani 3:67) for TFTs are a standard method for improving TFT performance.

558. Additionally, I note that multi-gated TFTs were well-known and would have provided other benefits such as reducing leakage current (*see generally* Kim-544, Shin, Tang, Kim-033, and Hong (EX1021-EX1023, EX1025, EX1027)).

559. Specifically, it is my opinion that a POSITA would have been motivated to use multi-gated TFTs to Masao’s display device to yield predictable results such as higher voltage tolerance and reduced leakage current. Further, there would have been a reasonable expectation of success, because using multi-gated TFTs in display device circuits was well-known by 2014, as evidenced by the teachings of Ohtani and other known prior art references (*see generally* Kim-544, Shin, Tang, Kim-033 (EX1021-EX1023, EX1025)), and such modifications were well within the skill set of a POSITA.

3. Claim 5

a. 5[pre]: “The display apparatus of claim 1, further comprising:”

560. See the discussion of Ground 4A, Claim 1, above.

- b. 5[a]: “a third thin-film transistor comprising a third semiconductor, one end of the third semiconductor being connected to one end of the first semiconductor, and the other end of the third semiconductor being connected to the first electrode layer; and”**

561. In my opinion, Masao in combination with Ohtani teaches or suggests limitation 5[a].

562. Masao Fig. 1 shows an array of pixels with a corresponding array of TFTs connected to common control lines in rows (signal 3a) and columns (signal S1, S2,.. Sn). Power is provided on signal (capacitance) lines 300. Masao illustrates the “third thin-film transistor” in its Fig. 1 as another TFT distinct from the first TFT.¹⁰ Annotated Fig. 1 below shows a first TFT (blue) and a “third” TFT (yellow). Masao, ¶¶50, 51.

¹⁰ See §VIII.A.9.a regarding the interpretation of “third.”

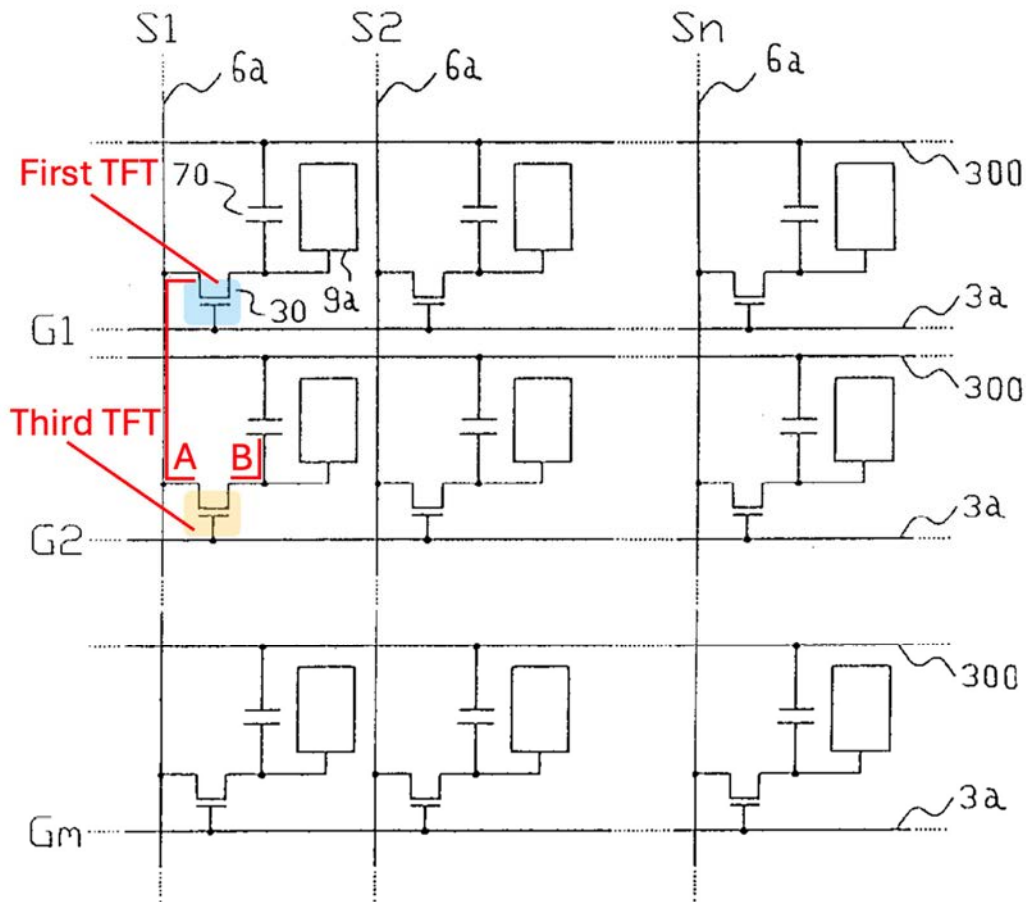


Fig. 1

563. For Claim 5, “the first electrode layer” is construed under either Mapping #1 or Mapping #2. See limitation 1[b] in §VIII.G.2.c. Annotated Fig. 3 below corresponds to Mapping #2.

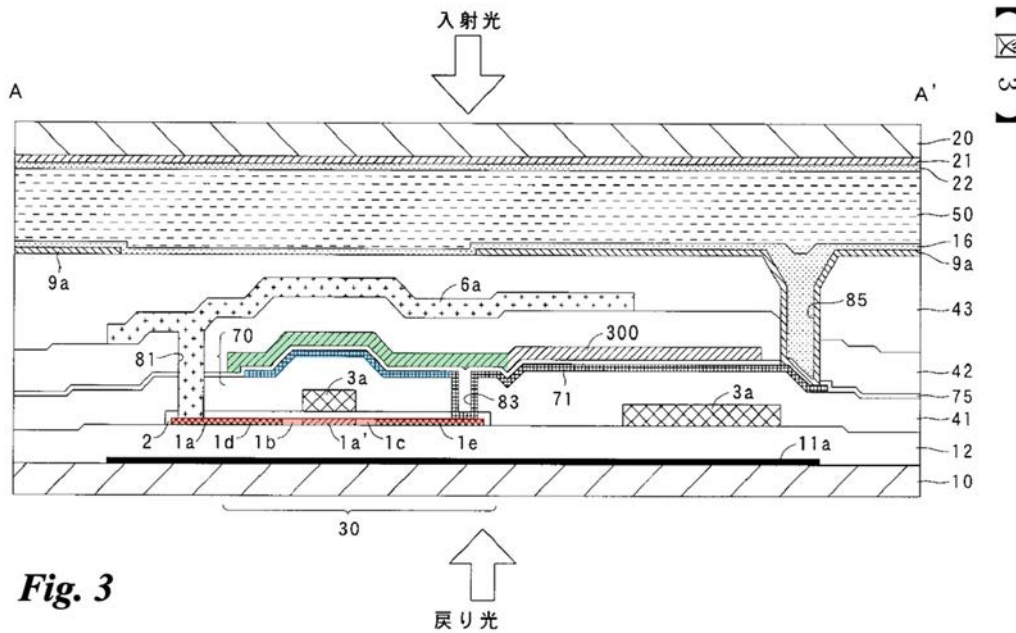


Fig. 3

564. As evident from both annotated Figs. 1 and 3 (above), the sources of the “first” and “third” TFTs are connected through data line 6a (labeled A in Fig. 1). Masao, ¶51: “a data line 6a to which an image signal is supplied is electrically connected to a source of the TFT 30.” As also shown in Figs. 1 and 3 of Masao, the “third” TFT is connected to the lower capacitor electrode, i.e., to relay layer 71 of capacitor 70 (“the first electrode layer”) (labeled B in Fig. 1). Ohtani, ¶50.

565. Accordingly, limitation 5[a] is disclosed by Masao in combination with Ohtani.

- c. **5[b]: a second shield layer in a layer between the first signal line and the third semiconductor and overlapping a part between a first channel area and a second channel area of the third semiconductor.**

566. In my opinion, Masao in combination with Ohtani teaches or suggests limitation 5[b].

567. As discussed above with respect to Ground 4A, Claim 1, limitation 1[e], capacitance line 300 operates as a shield, and Masao discloses the “first shield layer” as the portion of capacitance line 300 that overlaps part of the source and drain areas of the first semiconductor of the first TFT. §VIII.G.2.f. Similarly, Masao discloses “a second shield layer” as a portion of capacitance line 300 that overlaps parts of the source, drain, and channel areas of the “third” semiconductor of the “third” TFT.¹¹ This is illustrated in annotated Fig. 3 below as the green portion of capacitance line 300.¹²

¹¹ The two shield layers can be part of the same component is consistent with the '015 Patent. See Ground 1A, Claim 21.

¹² Masao's Fig. 3 illustrates a cross-sectional view of one of the TFTs shown in its Fig. 1, and in my opinion, a POSITA would have understood that it corresponded to any other TFTs of Fig. 1, including the “third” TFT.

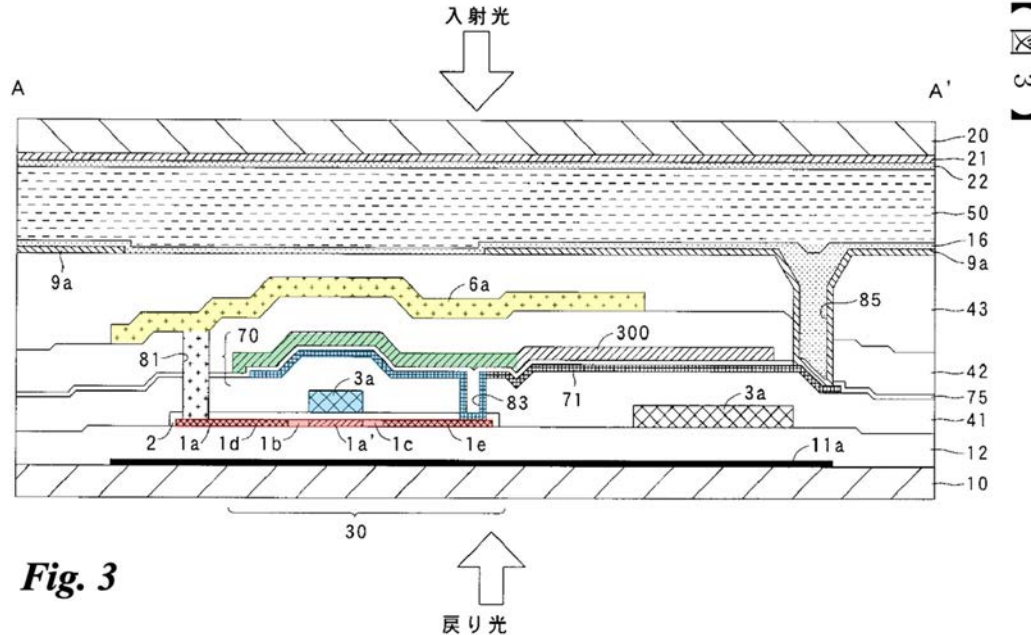


Fig. 3

568. Masao does not explicitly teach a first and a second channel area for its TFT. However, Ohtani, in the same field of endeavor and relating to LCD devices, teaches this feature. Notably, Ohtani describes an embodiment that utilizes a multi-gated TFT. Ohtani, 3:66-4:3, 6:20, 9:8-36, Fig. 10.

569. Ohtani states, “As shown in FIG. 10 in which the outline thereof is seen from the above, an active layer intersects with a gate wiring line at three portions, and gate electrodes are disposed at the portions.” *Id.*, 9:9-12. The multi-part gate of Ohtani is illustrated in Fig. 10, annotated below, shows overlap (green) of gate wiring line 12 at three portions over active layer 11, forming three gate electrodes, labeled G1-G3.

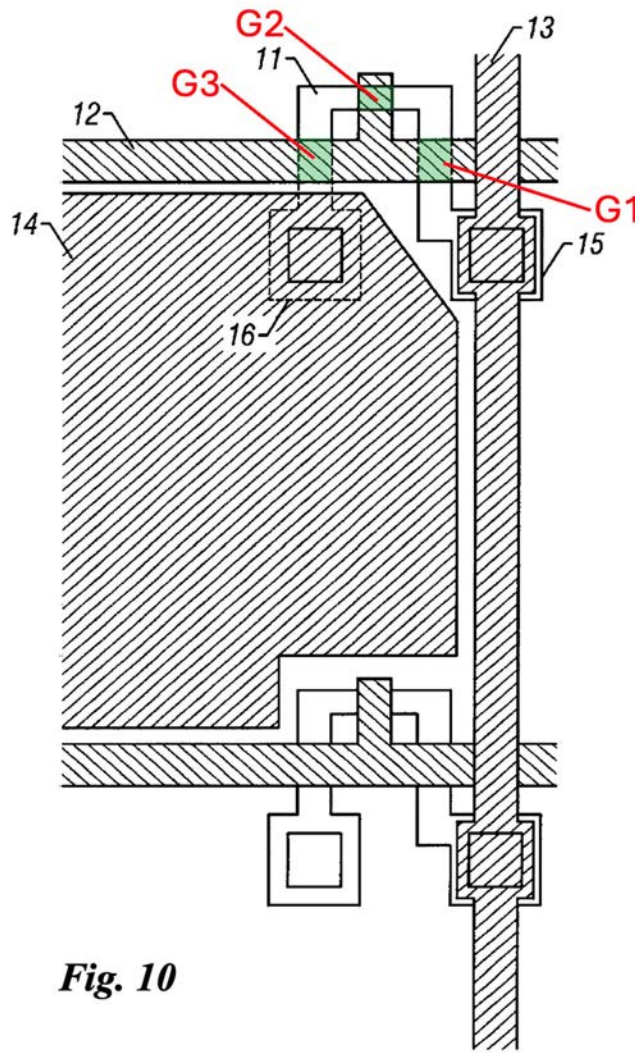


Fig. 10

570. In the Masao-Ohtani combination, it is my opinion that a POSITA would have found it obvious to replace the single-gate TFT of Masao with the multi-gated TFT of Ohtani; the top capacitor electrode (the “second shield layer”) having a large extent (see green annotation in Fig. 2 below), would overlap the “third” TFT, including all three gate electrodes and channel areas therebetween.

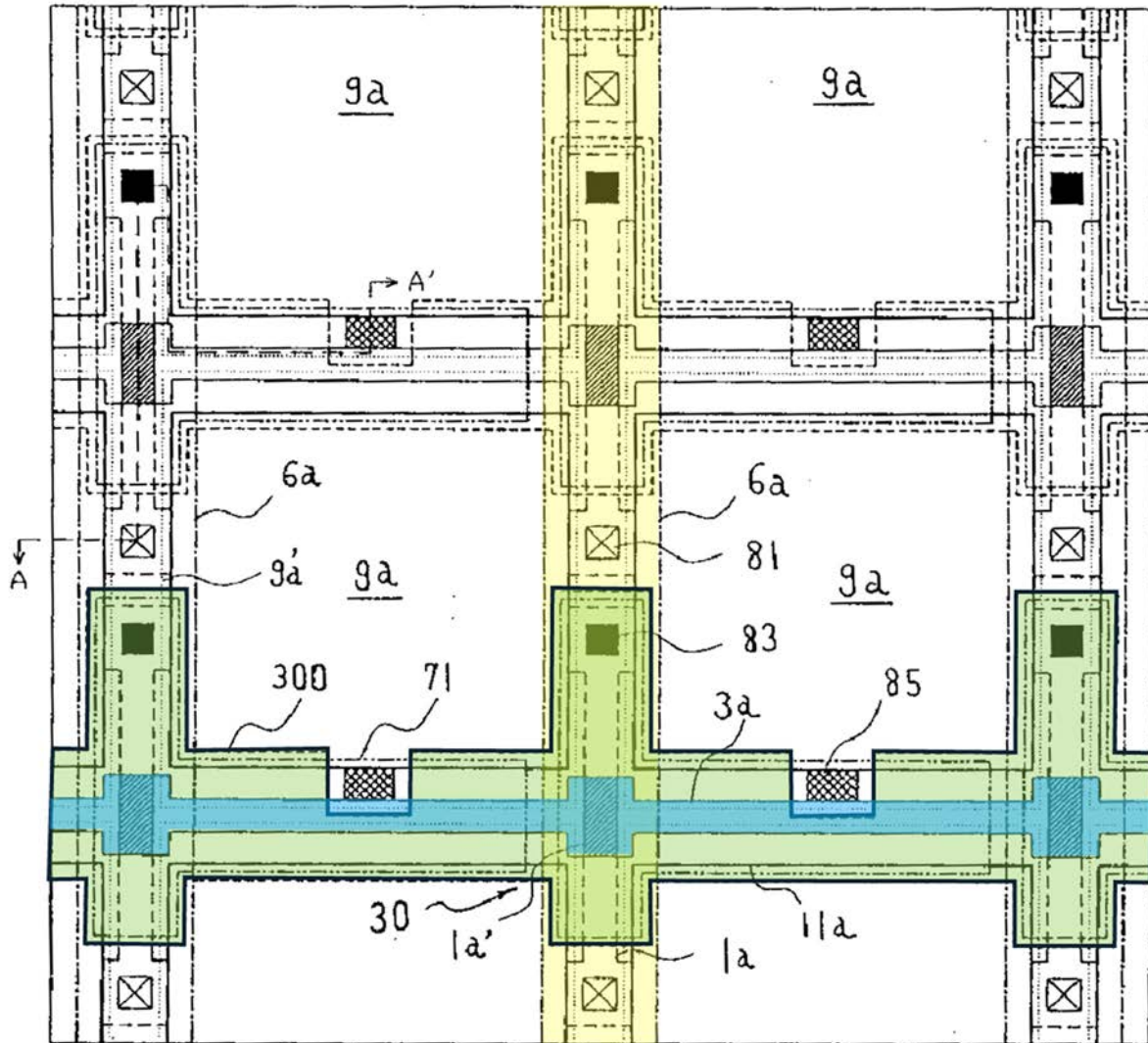


Fig. 2

571. Further, it would have been understood that each area of active layer 11 overlapping the gate wiring line 12 constituted a channel area; thus, the TFT in the Masao-Ohtani combination would include “a first channel area” under one of the gate electrodes, and “a second channel area” under another gate electrode (and a third channel area under the third gate electrode). Because Masao describes its TFT

is overlapped by capacitance line 300 (green color in Figs. 2 and 3 above), a section of capacitance line 300 would overlap a part between the first channel area and the second channel area of the TFT. As I have previously discussed in §VIII.H.2, this combination would have been obvious to a POSITA.

572. I further note that the semiconductor area between gates 1 and 3 would simply comprise a similar common undoped semiconductor. In my opinion, there is no reason or function to dope any portion of the semiconductor area between gates 1 and 3 and doing so would raise costs and reduce yields.

573. Accordingly, limitation 5[b] is disclosed by Masao in combination with Ohtani.

4. Claim 11:

- a. 11[a]: “... wherein a gate electrode of the third thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the third semiconductor, and the second gate electrode overlapping the second channel area of the third semiconductor, and”**

574. In my opinion, Masao in combination with Ohtani teaches or suggests limitation 11[a].

575. Specifically, this claim limitation is rendered obvious by the Masao-Ohtani combination, as described in limitation 5[b], and annotated Fig. 10 of Ohtani (above). All three gate electrodes would be in the same layer because both Masao

and Ohtani describe the gates are formed via overlap of the same gate wiring line with the active layer. Ohtani, 9:9-12; Masao, ¶53.

576. Accordingly, limitation 11[a] is disclosed by Masao in combination with Ohtani.

b. 11[b]: “wherein the gate electrode of the third thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.”

577. In my opinion, Masao in combination with Ohtani teaches or suggests limitation 11[b].

578. Masao describes that the gate electrodes of its TFTs are formed by scan line 3a and are thus part of scan line 3a. Masao, ¶53: “...the scan line 3a functions as a gate electrode (in particular, in the present embodiment, the scan line 3a is formed in a wide manner in a portion serving as the gate electrode).” In my opinion, a POSITA would have understood that in the Masao-Ohtani combination, the gate electrodes of the triple-gated transistor of Ohtani would also be formed by and would be part of Masao’s scan line 3a (“second signal line” shown in blue) that crosses data line 6a (“first signal line” shown in yellow), as shown in annotated Fig. 2 of Masao below.

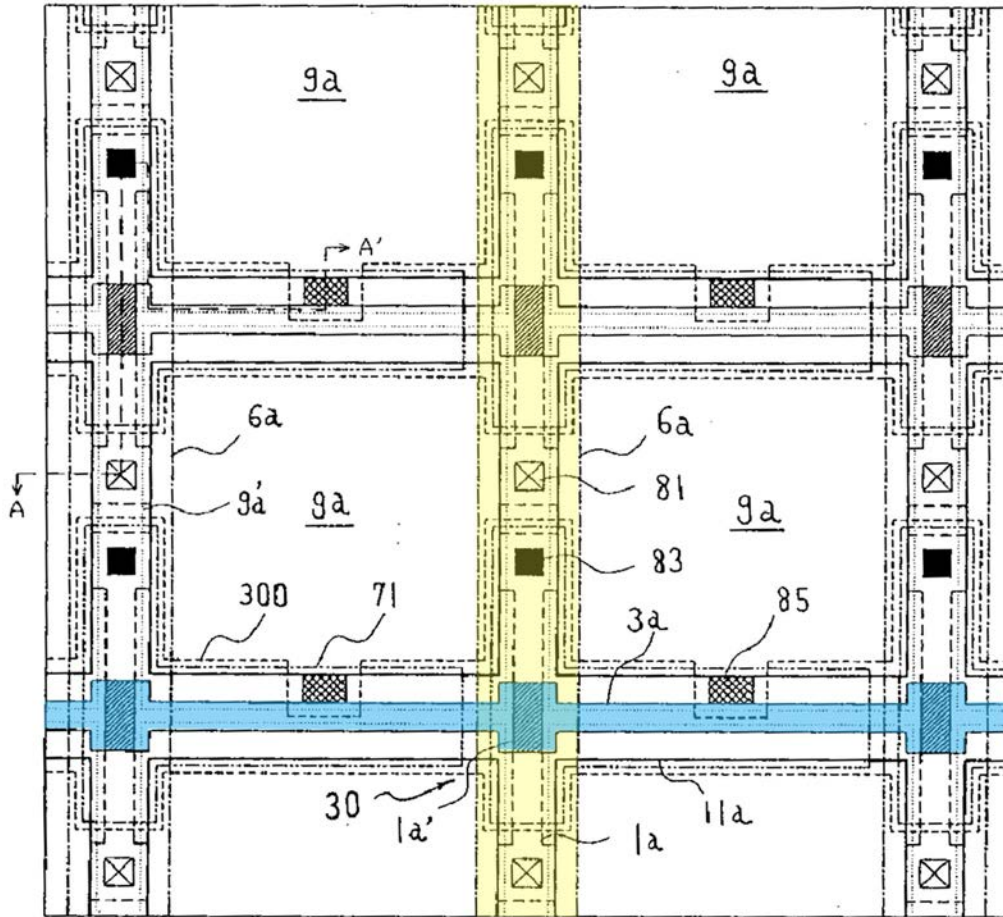


Fig. 2

579. For Claim 11, I am using Mapping #1 for the “first electrode layer.” See §VIII.G.2.c for the details of Mapping #1, and §IV.D.3.a for mapping options for Claim 5. The first electrode layer under Mapping #1 is annotated in blue in Fig. 3 below and includes gate line 3a (as well as bottom capacitor electrode 71). Therefore, scan line 3a (“second signal line”) is in “the same layer as the “first electrode layer.” The location of the various lines and conductive structures are generally a matter of circuit layout optimization subject to the circuit constraints (i.e., shielding

requirements) and can be implemented in a wide variety of ways, as would be understood by a POSITA, and as I have explained in §VI.C.

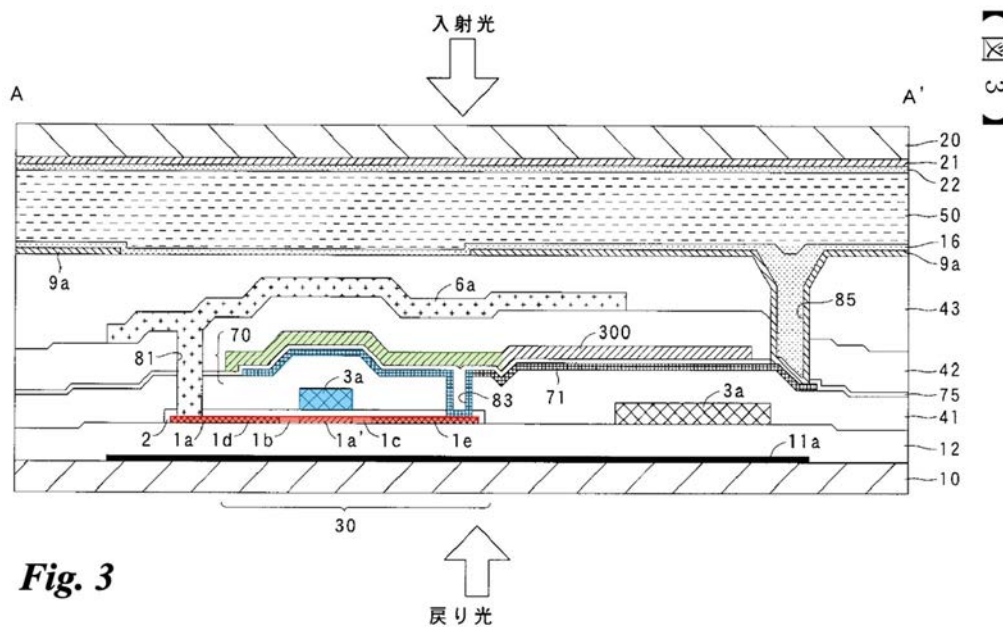


Fig. 3

580. Accordingly, limitation 11[b] is disclosed by Masao in combination with Ohtani.

5. Claim 13: "... wherein the second shield layer is a part of the second electrode layer."

581. In my opinion, Masao in combination with Ohtani teaches or suggests
Claim 13.

582. As explained for 5[b], the second shield layer is a portion of the capacitance line 300 that overlaps the “third” TFT. *See* §VIII.H.3.c. As also explained for Claim 2 in Ground 4A, the top capacitor electrode is part of the second electrode layer. *See* §VIII.G.3; see also annotated Fig. 3 below, showing the top

capacitor electrode which is part of capacitance line 300 (green) disposed over the first electrode layer (shown in blue).

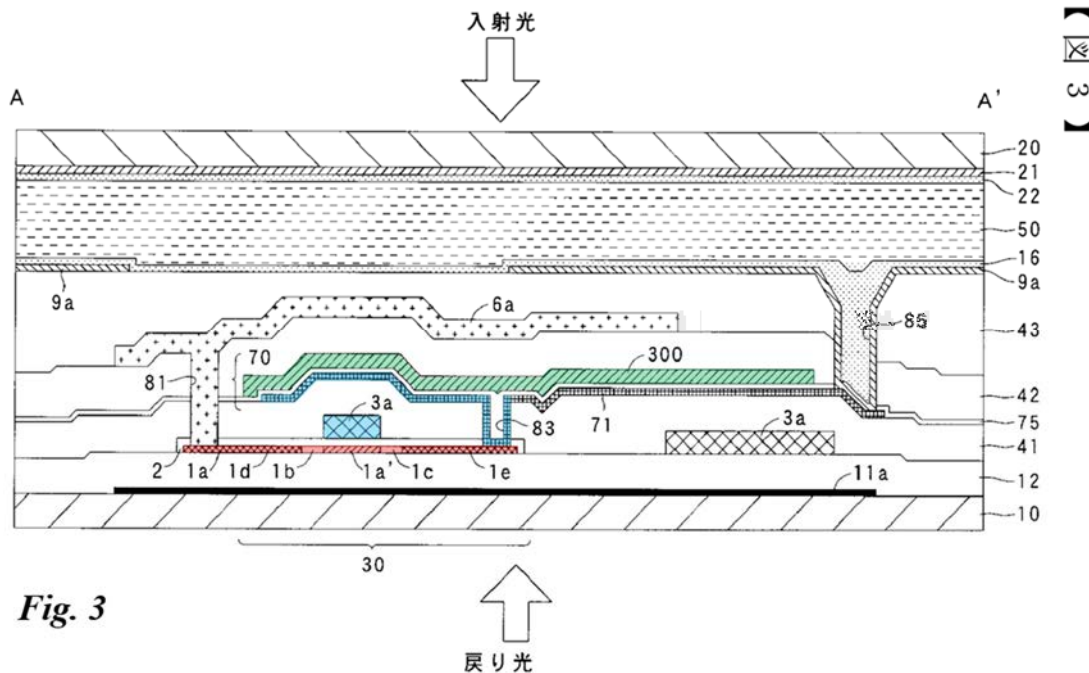


Fig. 3

583. Accordingly, Claim 13 is disclosed by Masao in combination with Ohtani.

6. Claim 28

a. 28[pre]: “A display apparatus comprising:”

584. See the discussion of Ground 4A, Claim 1, limitation 1[pre] above.

b. 28[a]: “a first thin-film transistor comprising a first semiconductor;”

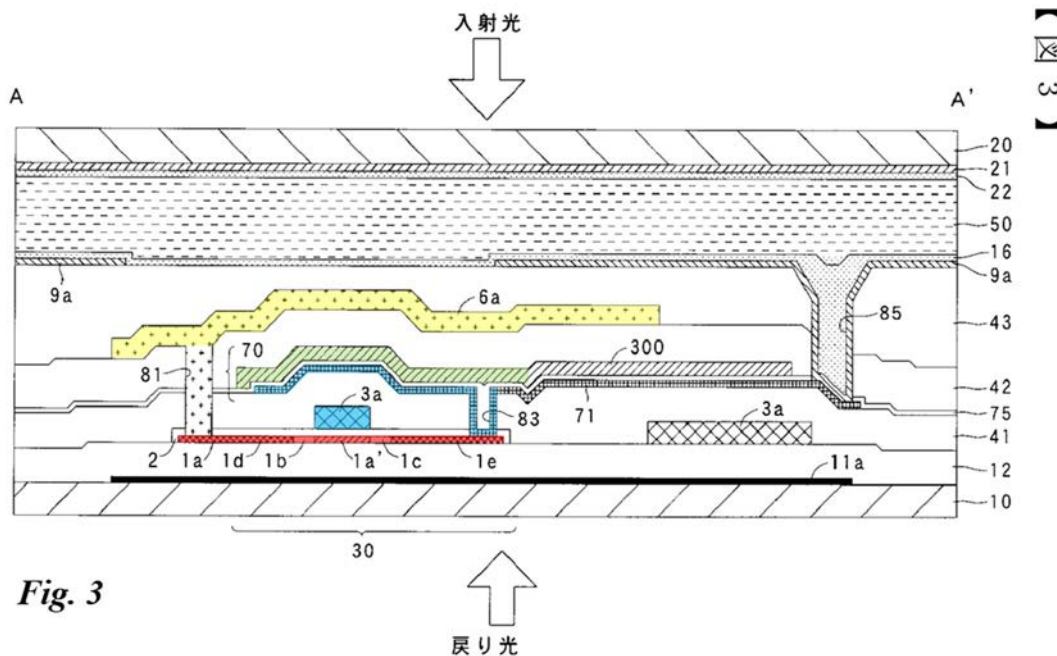
585. See the discussion of Ground 4A, Claim 1, limitation 1[a] above.

c. 28[b]: “a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;”

586. See the discussion of Ground 4A, Claim 1, limitation 1[b] above. For Claim 28, the Masao-Ohtani combination renders “a first electrode layer” obvious under Mappings #1 or #2. See §VIII.G.2.c for the details of Mappings #1 and #2.

d. 28[c]: “a first signal line over the first electrode layer;”

587. Masao’s data line 6a teaches or suggest “a first signal line.” See §VIII.G.2.e; Fig. 3, yellow annotation. Accordingly, limitation 28[c] is disclosed by Masao in combination with Ohtani.



- e. 28[d]: “a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and”

588. See the discussion of Ground 4B, Claim 5, limitation 5[a] above.

§VIII.H.3.b. Herein, the “second” TFT in Claim 28 is construed, similar to Claim 5, to be another TFT in Fig. 1 of Masao, as annotated below in yellow. Accordingly, limitation 28[d] is disclosed by Masao in combination with Ohtani.

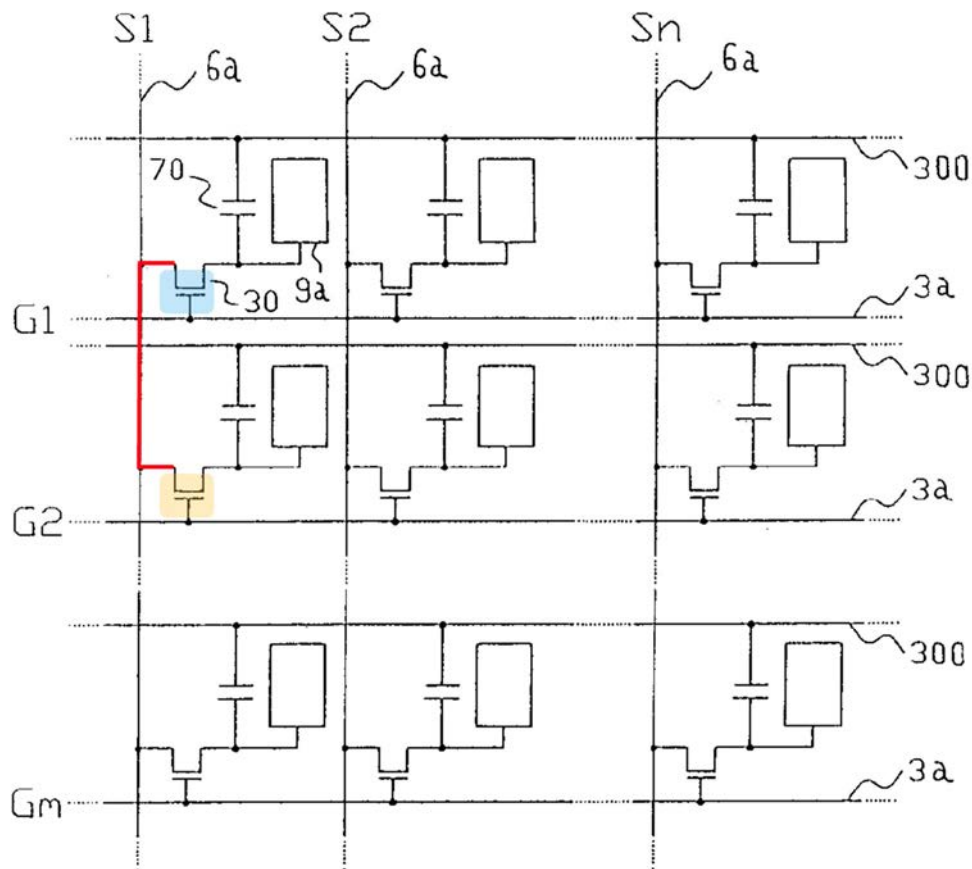


Fig. 1

- f. **28[e]: “a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.”**

589. See the discussion of Ground 4B, Claim 5, limitation 5[b] above.

§VIII.H.3.c. While Claim 5 recites a “second” shield layer and a “third” semiconductor, it will be readily appreciated that these labels do not meaningfully alter the analysis. See the discussion of Ground 1A, Claim 21. I note that in the Masao-Ohtani combination, the “shield layer” is part of the capacitance line 300 that overlaps the second TFT, and in particular, overlaps “a part between a first channel area and a second channel area” of its semiconductor.

590. Accordingly, limitation 28[e] is disclosed by Masao in combination with Ohtani.

7. Claim 29

- a. **29[a]: “... wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and”**

591. See the discussion of Ground 4B, Claim 11, limitation 11[a] above, which is the same as this limitation except that it recites a “third” TFT rather than a “second” TFT. See §VIII.H.4.

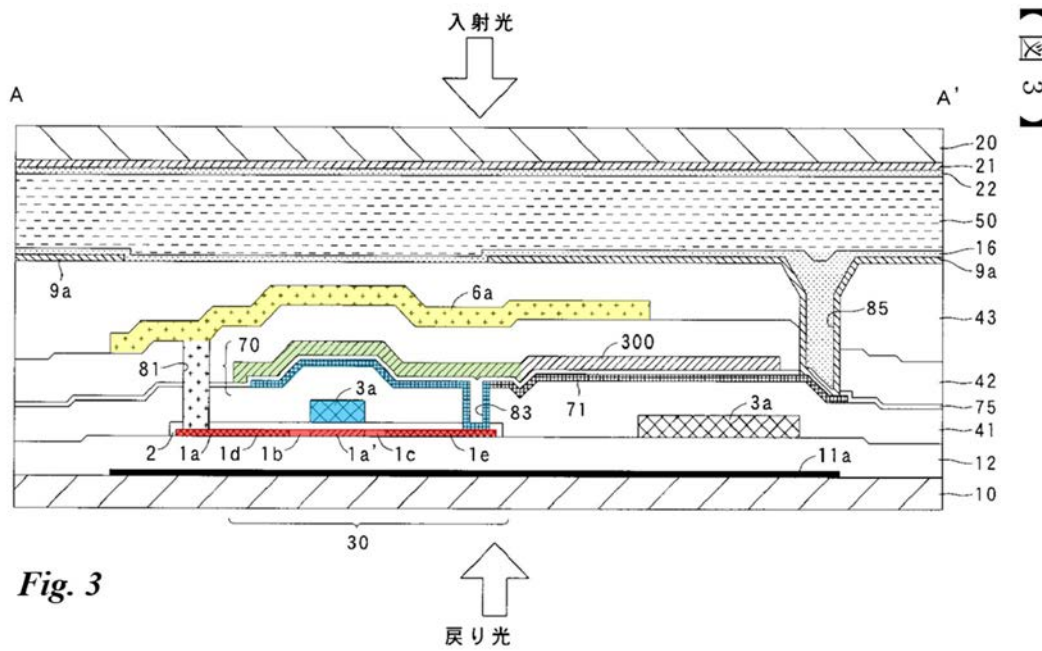
- b. 29[b]: “wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.”**

592. See the discussion of Ground 4B, Claim 11, limitation 11[b] above, which is the same as this limitation except that it recites a “third” TFT instead of a “second” TFT. See §VIII.H.4.

- 8. Claim 31: “... further comprising a second electrode layer over the first electrode layer and overlapping the first electrode layer, wherein the shield layer is a part of the second electrode layer.”**

593. See the discussions of Ground 4A, Claim 2 (in §VIII.G.3) and Ground 4B, Claim 13 (in §VIII.H.5). As shown in Fig. 3, annotated below, the “shield layer” is part of capacitance line 300, forms the top capacitor electrode and is, in my opinion, part a second electrode layer. The shield layer (33 shown in green) overlaps “the first electrode” layer (under either Mappings #1 or #2) of the “first electrode layer” used in base Claim 28); see annotation shown in blue under Mapping #1.

594. Accordingly, Claim 31 is disclosed by Masao in combination with Ohtani.

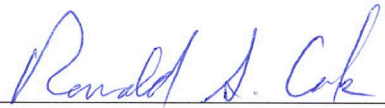


IX. CONCLUSION

595. Based on the foregoing analysis, it is my opinion that the challenged claims of the '015 patent are invalid.

This Declaration and my opinions herein are made to the best of my knowledge and understanding, and based on the material available to me, at the time of signing this Declaration. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 or Title 18 of the United States Code.

Executed on September 15, 2025.



Ronald S. Cok

X. APPENDIX A

Ronald S. Cok

SUMMARY

Extensive experience in research and development in the fields of digital imaging, parallel computing, on-line imaging, organic light-emitting diode (OLED) and inorganic light-emitting diode (ILED) displays, and heterogeneous micro-assembly for photonics and electronics. Strong background in technical project, team, and laboratory management. Worked in a variety of technical areas including physics, mathematics, computer science, optics, electronics, systems, displays, and software engineering. Demonstrated skill in working with scientists, inventors, lawyers, and business managers from a broad variety of backgrounds. Experienced in both large and small domestic and international organizations. Registered Patent Agent. Management Black Belt certified. Computer Science textbook author.

EXPERIENCE

Research Fellow & Chief Scientist

Managed, directed, and participated in display-related research projects. Work included technology development, publication, application, and extensive patent activities for core elements of OLED display technology, systems, and applications.

Managed projects related to quantum dots, wide-format curved displays, touch screens, alternative backplane designs, RGBW pixel designs, and electronic compensation and light output enhancement. Directed pre-commercialization activities for OLED business. Served as liaison for universities and external start-ups for technology development.

Director

Provided technical R&D direction and management for development projects and demonstrations. Engaged in extensive technical development and invention activities. Responsible for company patent portfolio management and oversight.

Developed and managed research activities in micro-transfer printing – heterogeneous integration using micro-transfer printing of micro-devices onto substrates. Provided R&D direction for iLED systems and displays. Demonstrated world's first full-color active- and passive-matrix micro-LED displays on rigid and flexible substrates. Worked on photonic and electronic systems incorporating micro-assembled heterogeneous components.

Senior Lab Head

Established and managed a new research laboratory. Developed a technical project portfolio and team focused on distributed wireless systems, organic LED systems, and digital cinema and immersive imaging systems.

Performed market development, business case analysis, and sales for nascent immersive imaging business. Managed R&D relationship for a digital imaging business unit. Performed business planning and research development for digital cinema, immersive imaging, OLED systems, motion imaging, display image quality, touch screens and materials, and large-format displays. Led Digital Cinema team that won a Technical Achievement Award (Oscar) from the Academy of Motion Picture Arts and Sciences.

OTHER RELEVANT EXPERIENCE

Digital Commercialization Manager for Europe, Asia, and the Middle East

Managed the digital product commercialization function for European R&D. Developed digital commercialization activity and capability, especially for software, small systems, and the Internet. Successfully launched three products on time within budget, including world's first multi-currency on-line image fulfillment system. Certified Black Belt Management; implemented Capability Maturity Model for European research operations. Developed European-specific product prototypes and more than doubled European digital imaging regional activity.

World-Wide Commercialization and Product Development Manager, Research Scientist

EMPLOYMENT

X-Celeprint, Inc.

2015 - Present

Small technology startup with in-house technical staff developing and offering skills, tools, and licenses for the use and application of heterogeneous integration using micro-transfer printing of micro-devices onto substrates. Serve as Director.

Eastman Kodak Company

1981 - 2015

Major imaging company. Worked in Kodak Research Laboratories on digital imaging as Member of Technical Staff Research Scientist, Group Leader, Project Manager, Commercialization, World-Wide, and Product Development Manager for Digital Imaging, Senior Lab Head, and Research Fellow.

EDUCATION

Master of Electrical Science

University of Michigan

Bachelor of Arts / Science in Mathematics and Physics (Honors)

Calvin University

CERTIFICATIONS

Management Black Belt

Registered Patent Agent No. 70,003

PROFESSIONAL ACTIVITIES

Member, Society of Information Display
Adjunct Professor, Rochester Institute of Technology
Associate Editor, Transputer Comm. Journal, Wiley

Textbook Author and Contributor
USA Top Inventor 2003-2005
IR&D 100 Innovation and Excellence