

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.,
Petitioner

v.

SAMSUNG DISPLAY CO., LTD.,
Patent Owner.

IPR2025-01480

U.S. Patent No. 10,439,015

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,439,015**

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EXHIBIT LIST

No.	Exhibit
1001	U.S. Patent No. 10,439,015 (“’015 Patent” or “’015 Pat.”)
1002	File History of the ’015 Patent (“’015FH”)
1003	Declaration of Ronald S. Cok (“Cok”)
1004	U.S. Patent Publication No. 2014/0132584 A1 (“Kim-584”)
1005	U.S. Patent Publication No. 2012/0019504 A1 (“Han”)
1006	U.S. Patent Publication No. 2014/0034923 A1 (“Kim-923”)
1007	U.S. Patent Publication No. 2014/0042405 A1 (“Moon”)
1008	U.S. Patent Publication No. 2014/0098078 A1 (“Jeon-078”)
1009	RESERVED
1010	Japanese Pat. No. 3,858,572 (“Masao”)
1011	U.S. Patent No. 6,225,966 B1 (“Ohtani”)
1012	N. H. E. Weste et al., <i>CMOS VLSI Design: A Circuits and Systems Perspective</i> , Fourth Edition, Addison-Wesley, 2011 (“Weste”)
1013	U.S. Patent No. 5,136,358 (“Sakai”)
1014	U.S. Patent No. 5,285,017 (“Gardner”)
1015	U.S. Patent No. 6,510,545 (“Yee”)
1016	U.S. Patent No. 8,692,297 (“Ho”)
1017	U.S. Patent No. 6,622,294 (“Saxena”)
1018	U.S. Patent No. 8,670,099 (“Xie”)
1019	U.S. Patent No. 8,988,852 (“Signoff”)
1020	Chinese Patent Publication No. 113936600 (“Tian”)

No.	Exhibit
1021	U.S. Patent Publication No. 2014/0320544 (“Kim-544”)
1022	U.S. Patent Publication No. 2014/0070184 (“Shin”)
1023	U.S. Patent Publication No. 2007/0007535 (“Tang”)
1024	RESERVED
1025	Korean Patent Publication No. 20050052033 (“Kim-033”)
1026	U.S. Patent Publication No. 2011/0025585 (“Kim-585”)
1027	Korean Patent Publication No. 870000854 (“Hong”)
1028	U.S. Patent No. 8,487,311 (“Liu”)
1029	U.S. Patent No. 8,514,155 (“Kobayashi”)
1030	U.S. Patent No. 8,269,696 (“Tomida”)
1031	U.S. Patent No. 7,855,507 (“Kim-507”)
1032	U.S. Patent No. 8,653,521 (“Hwang”)
1033	U.S. Patent No. 8,701,068 (“McElvain”)

LISTING OF CHALLENGED CLAIMS

10,439,015
Claim 1
1[pre] A display apparatus comprising:
1[a] a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;
1[b] a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;
1[c] a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;
1[d] a first signal line over the second electrode layer; and
1[e] a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor.
Claim 2
2. The display apparatus of claim 1, wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line.
Claim 3
3. The display apparatus of claim 1, further comprising a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first signal line.
Claim 4
4. The display apparatus of claim 1, further comprising a first voltage line in the same layer as the first signal line and connected to the second electrode layer.

Claim 5
5[pre] The display apparatus of claim 1, further comprising:
5[a] a third thin-film transistor comprising a third semiconductor, one end of the third semiconductor being connected to one end of the first semiconductor, and the other end of the third semiconductor being connected to the first electrode layer; and
5[b] a second shield layer in a layer between the first signal line and the third semiconductor and overlapping a part between a first channel area and a second channel area of the third semiconductor.
Claim 6
6[pre] The display apparatus of claim 1, further comprising:
6[a] a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and
6[b] a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part of the fourth semiconductor.
Claim 7
7[pre] The display apparatus of claim 1, further comprising:
7[a] a fourth thin-film transistor comprising a fourth semiconductor, one end of the fourth semiconductor being connected to the first electrode layer, and the other end of the fourth semiconductor being connected to a second voltage line; and
7[b] a third shield layer in a layer between the first signal line and the fourth semiconductor and overlapping a part between a first channel area and a second channel area of the fourth semiconductor.
Claim 8

8[pre] The display apparatus of claim 1, wherein the first signal line extends in a first direction, and

8[a] wherein a length along the first direction of the overlapping part of the first shield layer with the part of one of the source area and the drain area of the first semiconductor is larger than a length of the first electrode layer along the first direction.

Claim 9

9. The display apparatus of claim 1, wherein the first shield layer fully overlaps the part of one of the source area and the drain area of the first semiconductor.

Claim 10

10[a] The display apparatus of claim 1, wherein the first signal line extends in a first direction, and

10[b] wherein a length along the first direction of ~~[[the]]~~ an overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction.

Claim 11

11[a] The display apparatus of claim 5, wherein a gate electrode of the third thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the third semiconductor, and the second gate electrode overlapping the second channel area of the third semiconductor, and

11[b] wherein the gate electrode of the third thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

Claim 12

12. The display apparatus of claim 5, further comprising a first voltage line in the same layer as the first signal line, wherein the second shield layer is connected to the first voltage line.

Claim 13
13. The display apparatus of claim 5, wherein the second shield layer is a part of the second electrode layer.
Claim 14
14. The display apparatus of claim 5, further comprising a connecting line connecting the other end of the third semiconductor and the first electrode layer and being in the same layer as the first signal line.
Claim 15
15[a] The display apparatus of claim 6, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer and overlapping the fourth semiconductor, and
15[b] wherein the third shield layer is a part of the second voltage line and overlaps a part of the fourth semiconductor between the first gate electrode and the second gate electrode.
Claim 16
16. The display apparatus of claim 15, wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.
Claim 17
17. The display apparatus of claim 7, wherein the third shield layer is a part of the second voltage line.
Claim 18
18[a] The display apparatus of claim 7, wherein a gate electrode of the fourth thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the fourth semiconductor, and the second gate electrode overlapping the second channel area of the fourth semiconductor, and

18[b] wherein the gate electrode of the fourth thin-film transistor is a part of a third signal line crossing the first signal line and is in the same layer as the first electrode layer.

Claim 19

19. The display apparatus of claim 7, further comprising a connecting line connecting the one end of the fourth semiconductor and the first electrode layer and being in the same layer as the first signal line.

Claim 20

20[a] The display apparatus of claim 3, further comprising a fifth thin-film transistor comprising a fifth semiconductor, one end of the fifth semiconductor being connected to the one end of the first semiconductor and the one end of the second semiconductor, and the other end of the fifth semiconductor being connected to a first voltage line,

20[b] wherein the first voltage line is in the same layer as the first signal line and connected to the second electrode layer.

Claim 21

21[a] The display apparatus of claim 20, further comprising a fourth shield layer in a layer between the first signal line and the fifth semiconductor,

21[b] wherein the fourth shield layer overlaps a part of semiconductor between the channel area of the first semiconductor, the channel area of the second semiconductor, and the channel area of the fifth semiconductor.

Claim 22

22. The display apparatus of claim 21, wherein the fourth shield layer is a part of the second electrode layer.

Claim 23

23[a] The display apparatus of claim 22, further comprising a capacitor comprising a first capacitor plate and a second capacitor plate,

23[b] wherein the first capacitor plate is a part of the first electrode layer, and the second capacitor plate is a part of the second electrode layer.

Claim 24

24[pre] A display apparatus comprising:

24[a] a first thin-film transistor comprising a first semiconductor;

24[b] a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;

24[c] a first signal line over the first electrode layer;

24[d] a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to the first electrode layer, and the other end of the second semiconductor being connected to a voltage line; and

24[e] a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

Claim 25

25[a] The display apparatus of claim 24, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and

25[b] wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

Claim 26

26. The display apparatus of claim 24, wherein the shield layer is a part of the voltage line.

Claim 27

27. The display apparatus of claim 24, further comprising a connecting line connecting the one end of the second semiconductor and the first electrode layer and being in the same layer as the first signal line.

Claim 28

28[pre] A display apparatus comprising:

28[a] a first thin-film transistor comprising a first semiconductor;

28[b] a first electrode layer over the first semiconductor and overlapping a channel area of the first semiconductor;

28[c] a first signal line over the first electrode layer;

28[d] a second thin-film transistor comprising a second semiconductor, one end of the second semiconductor being connected to one end of the first semiconductor, and the other end of the second semiconductor being connected to the first electrode layer; and

28[e] a shield layer in a layer between the first signal line and the second semiconductor and overlapping a part between a first channel area and a second channel area of the second semiconductor.

Claim 29

29[a] The display apparatus of claim 28, wherein a gate electrode of the second thin-film transistor comprises a first gate electrode and a second gate electrode in a same layer, the first gate electrode overlapping the first channel area of the second semiconductor, and the second gate electrode overlapping the second channel area of the second semiconductor, and

29[b] wherein the gate electrode of the second thin-film transistor is a part of a second signal line crossing the first signal line and is in the same layer as the first electrode layer.

Claim 30

30. The display apparatus of claim 28, further comprising a voltage line in the same layer as the first signal line, wherein the shield layer is connected to the voltage line.

Claim 31

31. The display apparatus of claim 28, further comprising a second electrode layer over the first electrode layer and overlapping the first electrode layer, wherein the shield layer is a part of the second electrode layer.

Claim 32

32. The display apparatus of claim 31, further comprising a voltage line in the same layer as the first signal line, wherein the voltage line is connected to the second electrode layer.

Claim 33

33[pre] A display apparatus comprising:

33[a] a first thin-film transistor comprising a first semiconductor comprising a source area, a drain area, and a channel area between the source area and the drain area;

33[b] a first electrode layer over the first semiconductor and overlapping the channel area of the first semiconductor;

33[c] a second electrode layer over the first electrode layer, a part of the second electrode layer overlapping the first electrode layer;

33[d] a first signal line over the second electrode layer; and

33[e] a first shield layer in a layer between the first signal line and the first semiconductor and overlapping a part of one of the source area and the drain area of the first semiconductor,

33[f] wherein the first shield layer is a part of the second electrode layer and overlaps a part of the first signal line,

33[g] wherein the first signal line extends in a first direction, and

33[h] wherein a length along the first direction of the overlapping part of the first shield layer with the first signal line is larger than a length of the first electrode layer along the first direction.

BOE Technology Group Co., Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) of claims 1-33 (“Challenged Claims”) of U.S. Patent No. 10,439,015 (“’015 patent”; EX1001).

I. GROUNDS FOR STANDING

Petitioner certifies ’015 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR.

II. IDENTIFICATION OF CHALLENGE

A. Prior Art

Petitioner relies on documents listed in Exhibit list, including prior art references under 35 U.S.C. §§102(a)(1)/(2) in Grounds below, and on declaration of Mr. Ronald S. Cok (“Cok;” EX1003).

B. Grounds for Challenge under 35 U.S.C. §103

Ground	Prior Art	Claims
1A	Kim-584	1-4, 8-10, 20-23, 33
1B	Kim-584+Han	5, 11-14, 28-32
2A	Kim-923	1-4, 8-10, 20-23, 33
2B	Kim-923+Moon	6-7, 15-19, 24-27
2C	Kim-923+Han	5, 11-14, 28-32
3	Moon+Jeon-078	24-27
4A	Masao	1-2, 8-10, 33
4B	Masao+Ohtani	5, 11, 13, 28-29, 31

III. THE '015 PATENT

A. Overview

The '015 patent describes a display apparatus with thin-film transistors (TFTs) each having source, drain and gate electrodes, and a data line in a different layer. EX1001, Abstract. Example embodiments and figures of '015 patent show a circuit and TFT layouts of an organic light-emitting diode (OLED) display pixel. *Id.*, 3:10-34, 4:6-9. But '015 patent explains its embodiments are “**not limited to an organic light-emitting display apparatus.**”¹

Fig. 1 shows a circuit with signal lines (121-124, 171-172), TFTs (T1-T6), a storage capacitor (Cst), and an OLED. *Id.*, 4:39-42.

¹ All emphases are added by Petitioner, unless otherwise indicated.

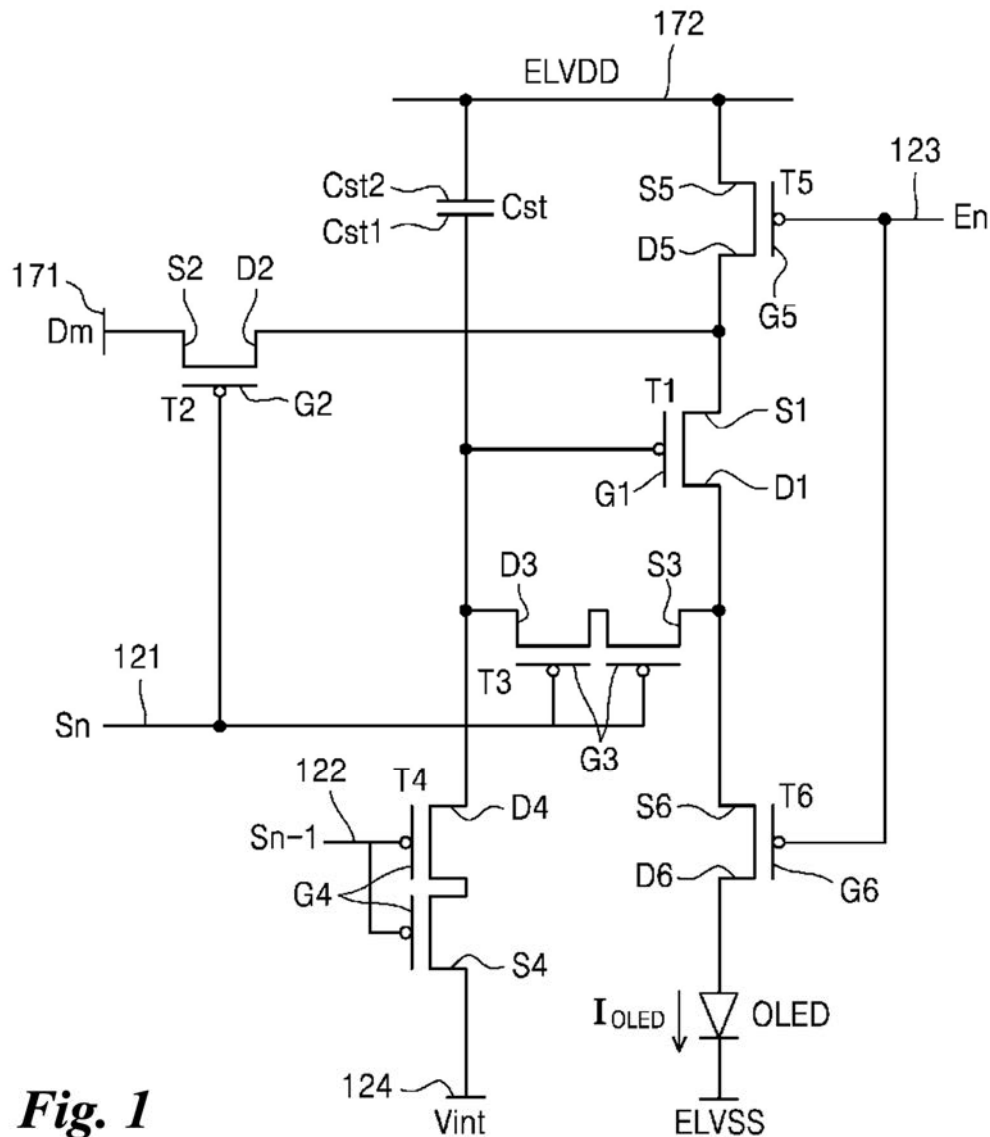


Fig. 1

The TFTs are formed in a semiconductor region. *Id.*, 7:18-24. T3 and T4 may be “dual gate electrode” TFTs to “prevent or reduce generation of a leakage current.” *Id.*, 8:42-47, 14:62-65; 15:36-45; Fig. 1.

To prevent image quality deterioration, one or more shield layers are disposed between a layer containing a signal line and a layer containing the TFTs. *Id.*, 1:34-36, 46-48.

Fig. 5 shows shield layers, which can be parts or extensions of existing components. *Id.*, 15:3-5, 15:51-63. Notably, shield layer SD1, shielding T3 from the noise on data line 171, is an extension of a capacitor plate. *Id.*, 11:11-13. *Id.*, 11:29-33. SD2 is part of voltage line 124 and shields T4. *Id.*, 12:28-30, 52-56. SD3, shielding T3, is a capacitor plate. *Id.*, 13:47-48, 14:16-26.

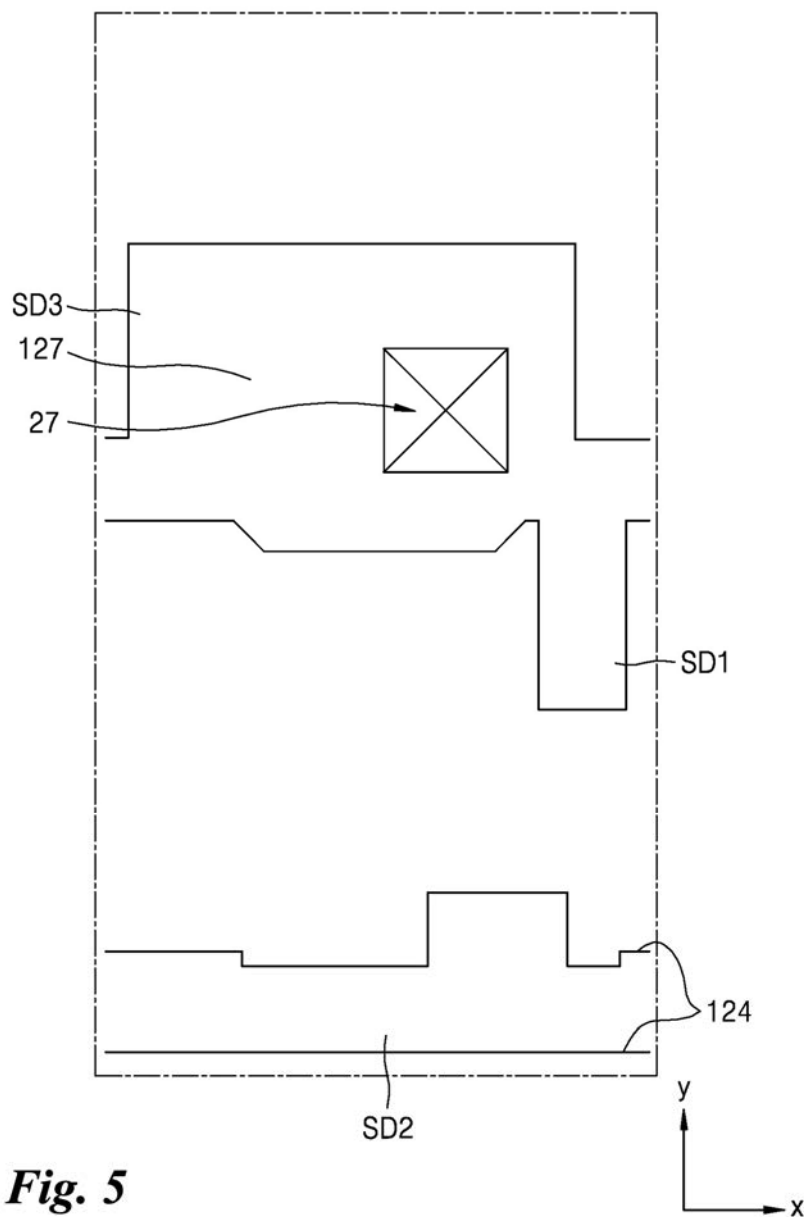


Fig. 5

B. Prosecution History

The '015 patent issued from Application No. 15/838,138, filed December 11, 2017, with an earliest priority date of August 4, 2014² based on a Korean application. EX1001, front page. During prosecution Applicant canceled the originally-filed claim after two Office Actions, which rejected the claim as anticipated by Lee (U.S. 2014/0167009). EX1002, 135-146, 171-174, 243-247. After filing new claims, the application was allowed without further Office Actions. The Notice of Allowability generally listed claim 1 limitations as reasons for allowance. *Id.*, 118; Cok, ¶¶40-42.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) in August 2014 would have had a bachelor’s degree in electrical engineering, physics, materials science or engineering, or a related field and at least four years of practical experience with design or development of display devices, including pixel layout, or the equivalent. Additional education could substitute for industry experience and vice versa. Cok, ¶¶16-20.

D. Claim Construction

Petitioner believes no express constructions are necessary and the claims should be given their plain and ordinary meaning. Cok, ¶59.

² August 4, 2014 priority date is assumed for purposes of this Petition only.

IV. DETAILED EXPLANATION OF GROUNDS

A. Ground 1A: Kim-584 Renders Obvious Claims 1-4, 8-10, 14, 20-23, 33.

Kim-584 describes an OLED device utilizing a mesh structure for wires that supply a voltage to minimize leakage currents. Kim-584, ¶8. Kim-584 discloses active-matrix OLED devices having a six-transistor-one-capacitor (6T1C) structure. *Id.*, ¶95. Some embodiments seek to minimize parasitic capacitance to prevent increasing black luminance. *Id.*, ¶93.

1. Claim 1

Kim-584 renders Claim 1 obvious. *See* Cok, ¶¶62-92.

a. 1[pre]:

Kim-584 describes a “[a]n organic light-emitting **display device**.” Kim-584, Abstract. Fig. 1 illustrates a display device 100 including a plurality of pixels. *Id.*, ¶31.

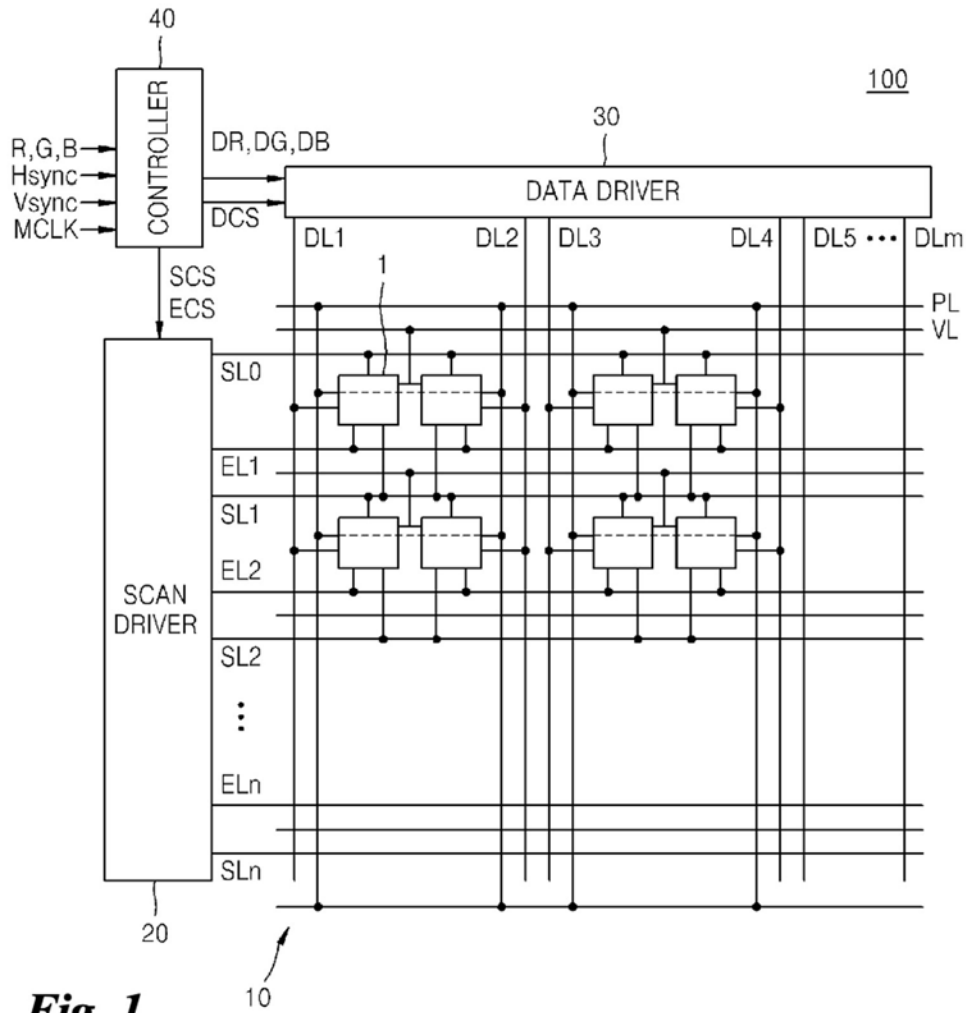


Fig. 1

b. 1[a]:

Kim-584's TFT T1 is "a first thin-film transistor," illustrated in Fig. 3 (annotated below).

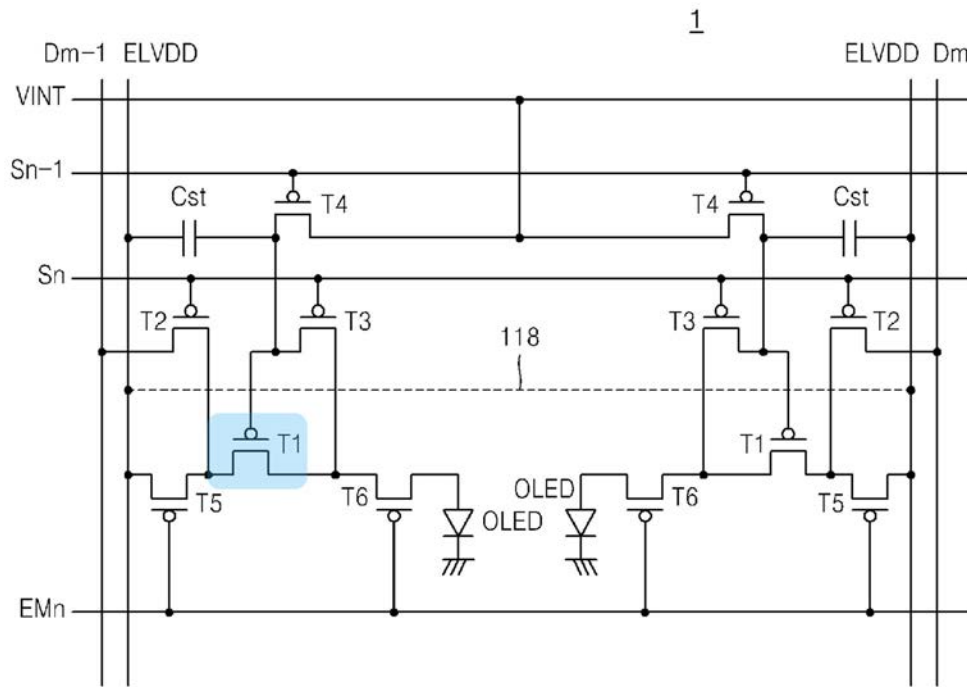


Fig. 3

Kim-584 discloses “a first semiconductor comprising a source area, a drain area, and a channel area” therebetween because T1 has an active layer A1 (“first semiconductor”), and “[a]n active layer of each TFT includes a **channel area** which is not doped with impurities, and **source and drain areas** which are formed by doping **both sides of the channel area** with impurities.” *Id.*, ¶63. Kim-584’s active layers are made of a semiconductor. *Id.*, ¶62.

Fig. 5 illustrates Kim-584’s active layers for two adjacent pixels, where “TFTs of a pixel circuit are formed along the first and second active layers 112-1 and 112-2,” including “[a]ctive layer[] A1 of a **driving TFT T1**.” *Id.*, ¶63, Fig. 5.

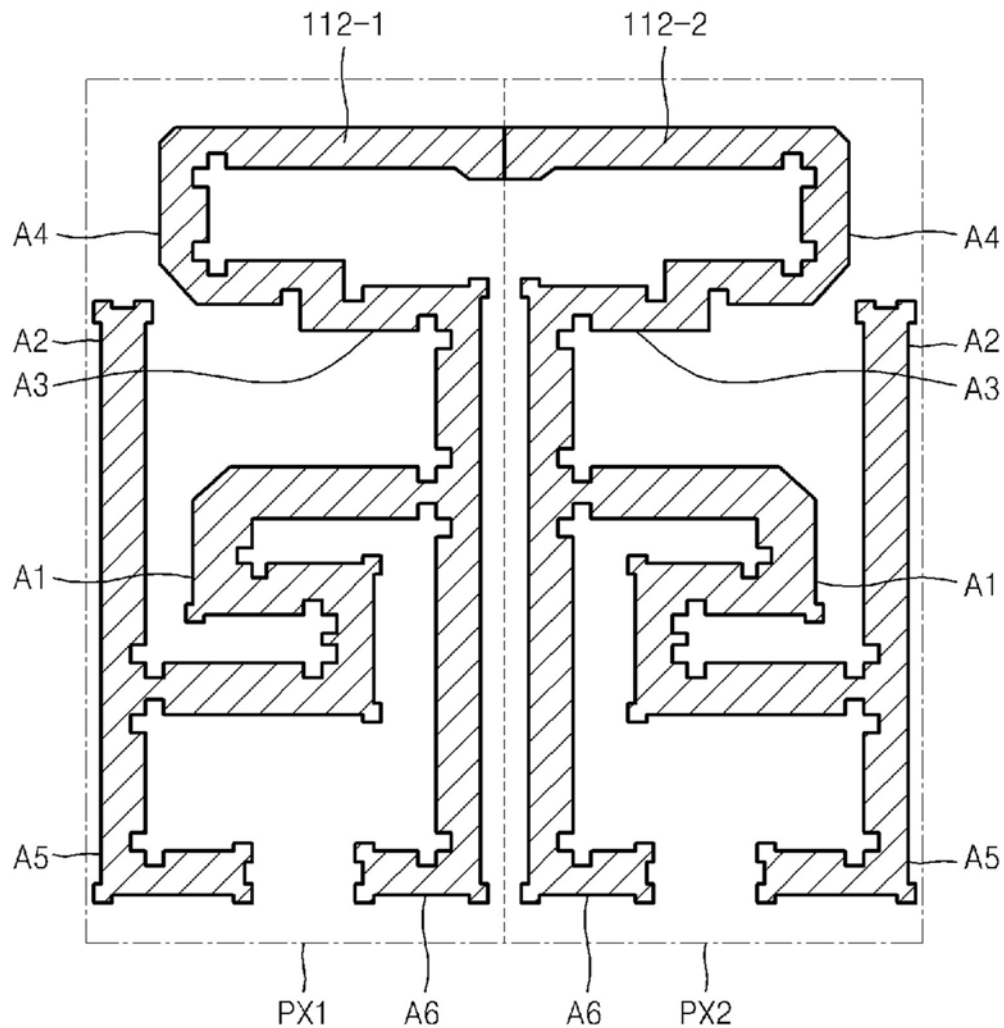


Fig. 5

c. 1[b]:

Kim-584 discloses “a first electrode layer over the first semiconductor” as the electrode layer that includes first capacitor electrode 114-1 (which also operates as T1’s gate). Notably, Kim-584’s “first gate lines are formed on the first gate insulating layer 102. The first gate lines may include...**first capacitor electrodes 114-1 and 114-2.**” *Id.*, ¶66. Kim-584 explains “**first capacitor electrodes 114-1 and**

114-2³ operate as gate electrodes G1 of the driving TFTs T1...and overlap with the channel areas of the active areas A1 of the TFTs T1.” *Id.*, ¶67.

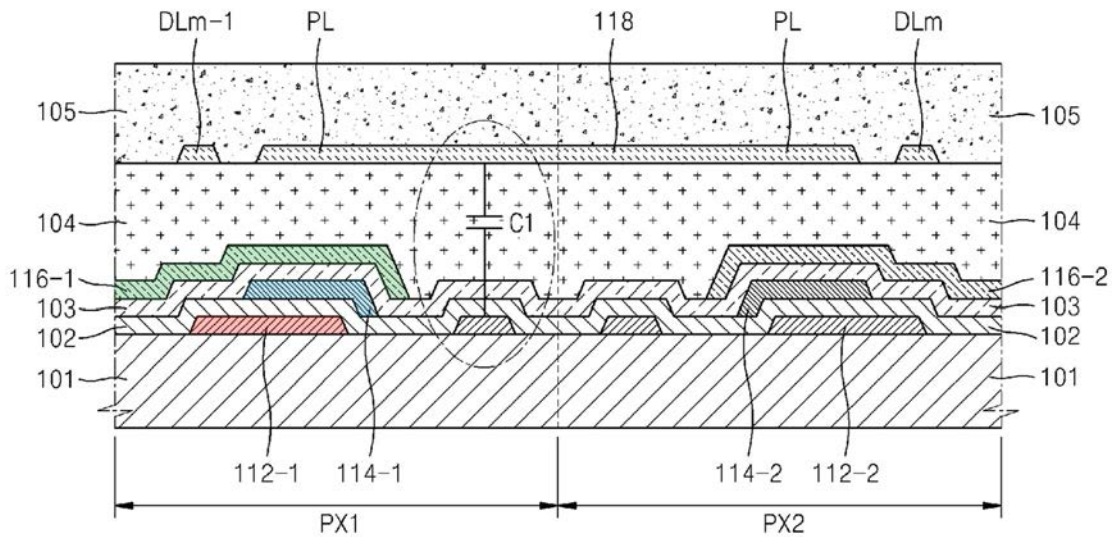


Fig. 9

Annotated Fig. 9 (above) and Fig. 6 (below) also show first capacitor electrode 114-1 (T1’s gate, blue) overlaps first active layer 112-1 (A1, red). *Id.*, ¶¶60, 67.

³ Kim-584’s layout shows two adjacent pixels (PX1, PX2). Kim-584, ¶58. For brevity, this Ground focuses on PX1 features (112-1, 114-1, etc.).

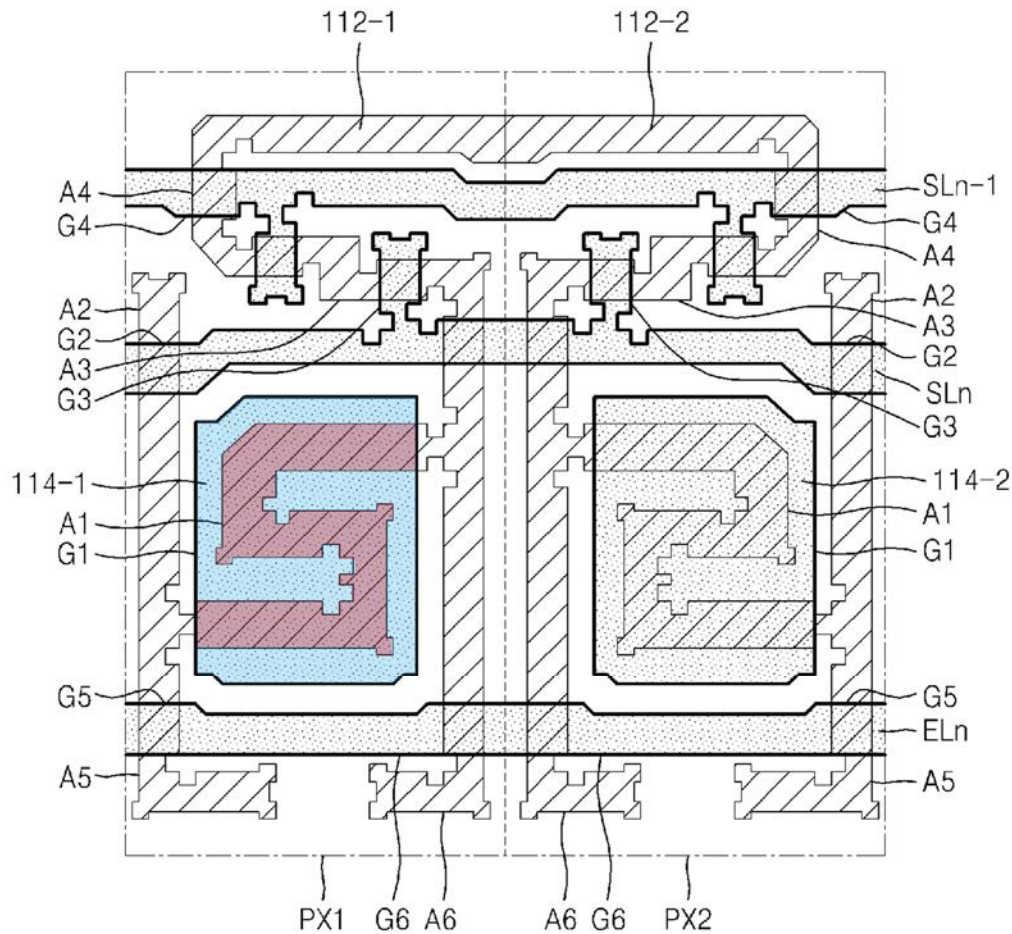


Fig. 6

d. 1[c]:

Kim-584 teaches “a second electrode layer” as the layer that includes second capacitor electrode 116-1. Kim-584 explains, “**second capacitor electrodes 116-1...overlap with the first capacitor electrodes 114-1...to form the storage capacitor Cst.**” Kim-584, ¶70.

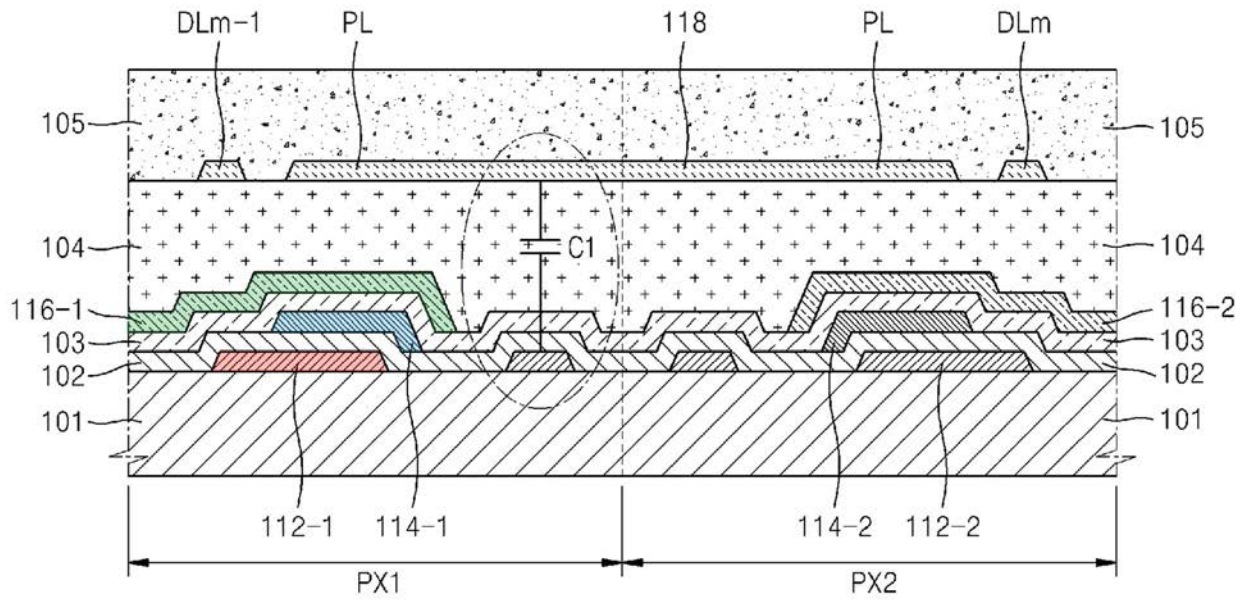


Fig. 9

Annotated Fig. 9 (above) and Fig. 8 (below) both illustrate second capacitor electrode 116-1 (green) (“a part of the second electrode layer”) overlaps first capacitor electrode 114-1 (blue), which is in “the first electrode layer.” *Id.*, ¶70, Figs. 7, 9.

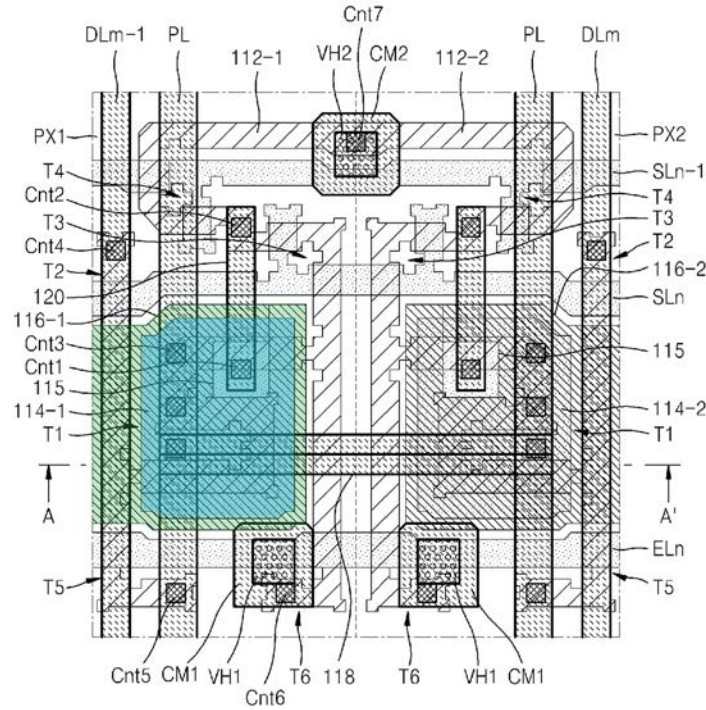


Fig. 8

e. 1[d]:

Kim-584's Fig. 9 (annotated below) illustrates "a first signal line" as data signal line DLm-1.

Kim-584 describes a "substrate 101 on which the **data signal lines DLm-1** and DLm...are formed." Kim-584, ¶78. Fig. 9 (below) illustrates DLm-1 ("first signal line") is over second capacitor plate 116-1 (green), which is in the "second electrode layer."

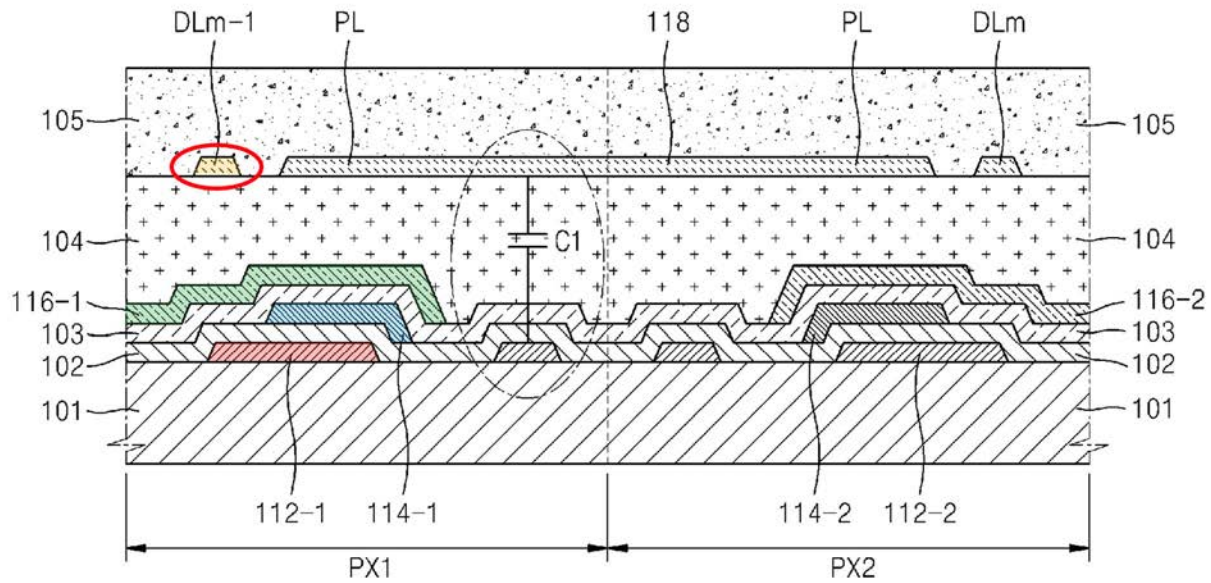


Fig. 9

f. 1[e]:

Kim-584 teaches or suggests “a first shield layer” as second capacitor electrode 116-1, or a part thereof, which overlaps T1, positioned in a layer between DLm-1 (“first signal line”) and T1’s active layer 112-1. Kim-584, ¶¶69-70, Fig. 9. Annotated Fig. 9 (above) illustrates second capacitor electrode 116-1 (green) between DLm-1 and T1’s active layer 112-1 (red), thereby shielding T1 from noise on DLm-1.

POSITAs would have found it obvious that second capacitor electrode 116-1 is a shield layer because it is connected to a constant voltage line, PL (or ELVDD⁴, Kim-584, ¶¶35, 52, Fig. 3) and is positioned between the potential source of electromagnetic interference (DLm-1) and T1's active layer. Treating a capacitor plate as a shield layer is consistent with '015 patent's explanation that "third shield layer SD3 **may be part of the second storage capacitor plate 127.**" EX1001, 13:47-48; *see also id.*, 15:3-5, 15:51-63, Fig. 10; §III.A; Cok, ¶¶86-87.

Kim-584's second capacitor electrode 116-1 has a large area, and a portion thereof overlaps "a part of one of the source area and the drain area of the first semiconductor"—shown in Fig. 7 (annotated below) in purple,⁵ with second capacitor electrode 116-1 in green and bottom capacitor plate 114-1 (T1's gate G1) as a dashed red rectangle. POSITAs would have understood that the active layer under G1 corresponds to T1's channel region, and the portion of active layer (purple) on two sides of the channel correspond to "a part" of T1's source and drain areas. Kim-584, ¶63; Cok, ¶¶88-91.

⁴ Kim-584's "driving voltage line PL transmits a first power supply voltage ELVDD." Kim-523 ¶45; *see also id.*, ¶35. Accordingly, PL and ELVDD are used interchangeably hereinafter.

⁵ Only a portion of the overlapped source region is annotated. *See* Claim 8.

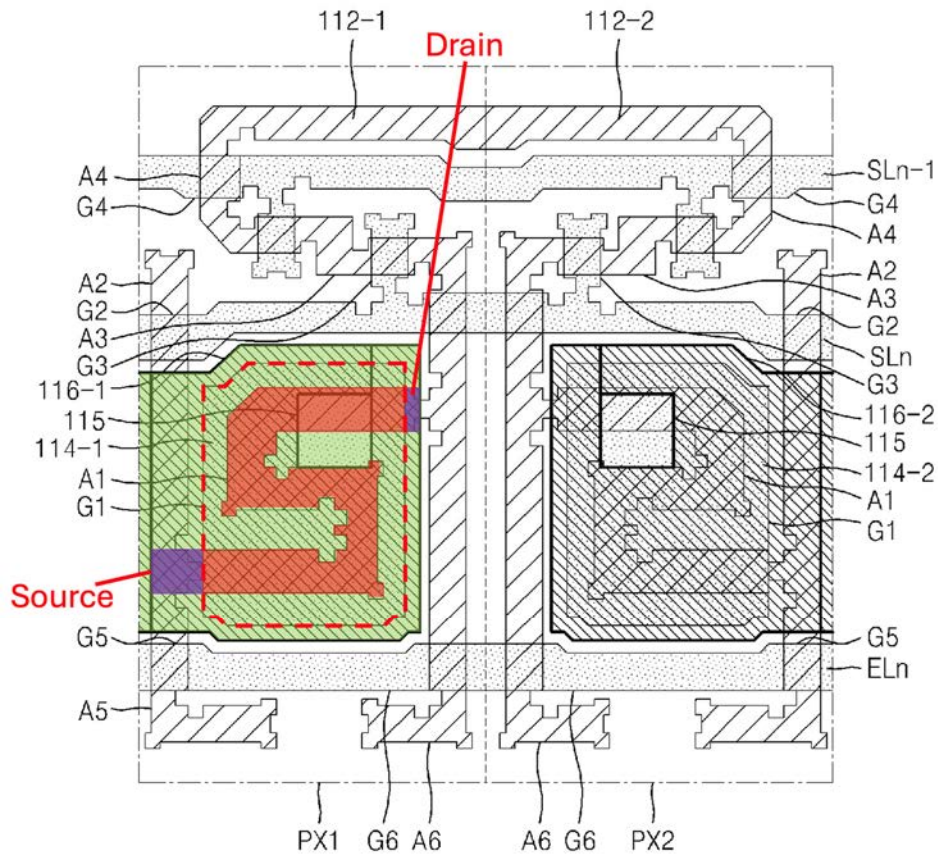


Fig. 7

2. Claim 2

As in 1[e], Kim-584's second capacitor electrode 116-1, or a part thereof, is the "first shield layer," which is part of a "second electrode layer" that also includes gate lines: "[s]econd gate lines are formed on the second gate insulating layer 103. The second gate lines include second capacitor electrodes 116-1." Kim-584, ¶69, Fig. 9 (below).

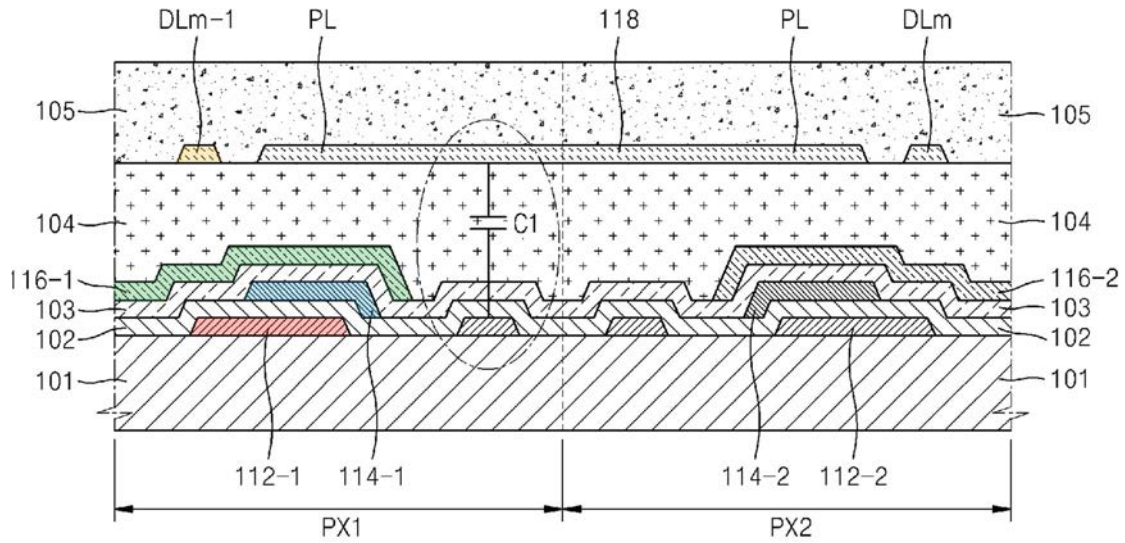


Fig. 9

Kim-584's Fig. 8 (annotated below) shows second capacitor electrode 116-1 overlaps a part of signal line DLm-1 ("first signal line").

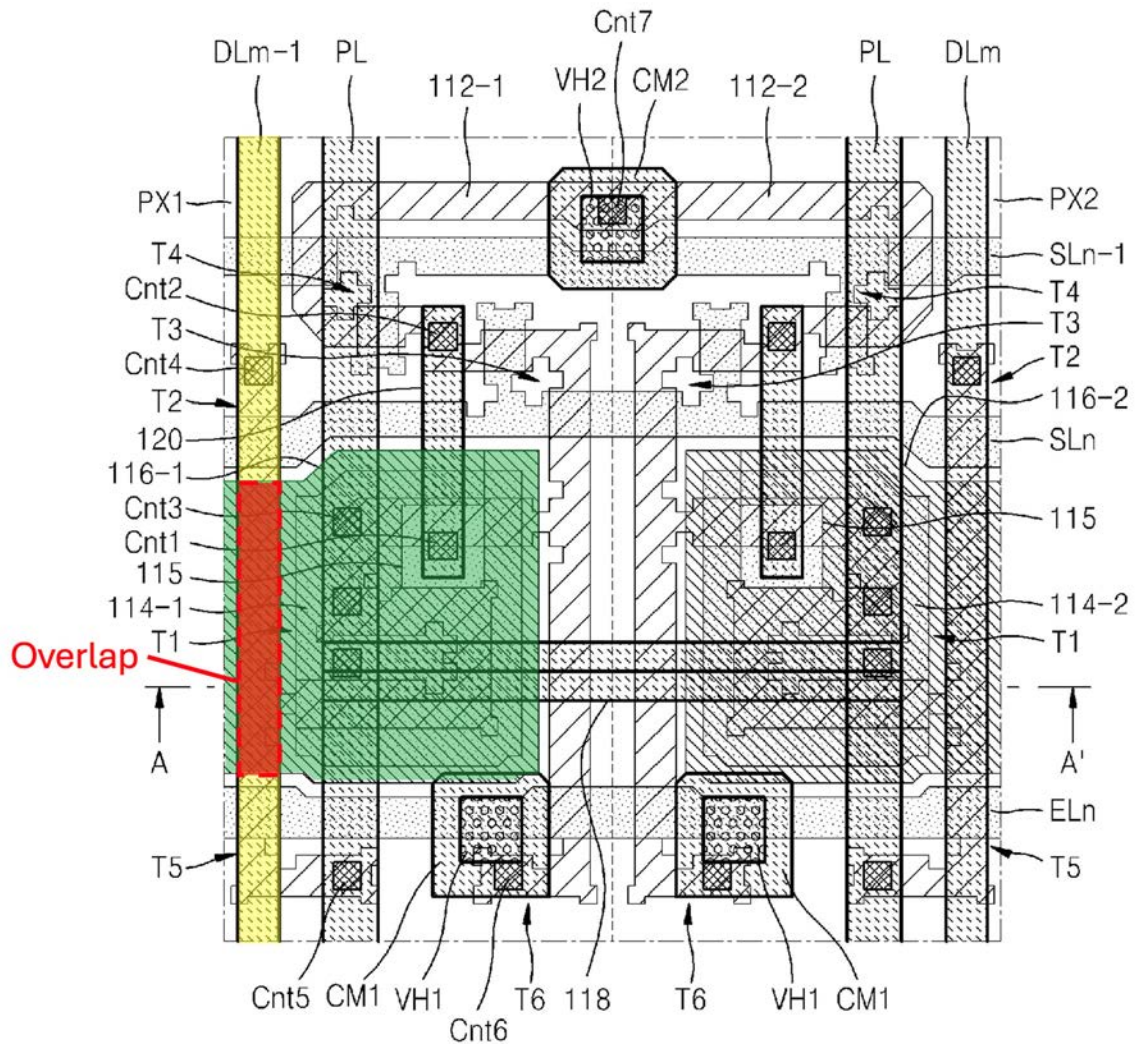


Fig. 8

The interpretation that a component (second capacitor plate) in a lower layer “overlaps” part of another component in a higher level (part of first signal line) is consistent with ’015 patent, which does not limit “overlapping” to mean “above,” and, similar to Kim-584, illustrates shield layers (SD1, SD2, SD3) positioned below signal line 171, while explaining the shield layer overlaps the signal line. EX1001,

Figs, 5-7, 17:27-29. Moreover, POSITAs would have understood that overlapping refers to plan-view, without regard to vertical ordering of elements. Cok, ¶¶93-98.

3. Claim 3

Kim-584 discloses a “second” TFT as TFT T2. Fig. 3 (annotated below) shows T2’s connection at one end (T2’s drain) to one end (source) of T1 (red) and at the other end (T2’s source) to first signal line (DLm-1) (green). Kim-584, Fig. 2-3, ¶47.

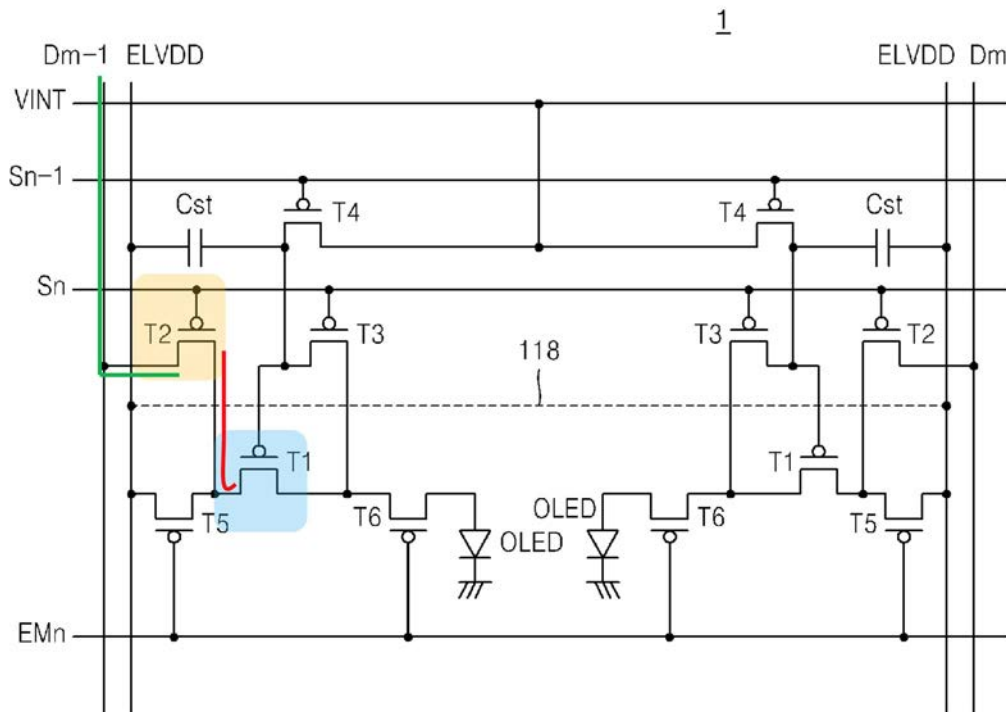


Fig. 3

Kim-584 discloses a semiconductor for each TFT as part of active layer 112-1, including an active layer A2 (“second semiconductor”) for T2 (“second thin-film transistor”): “Active layer[]... A2...of...a switching TFT T2...[is] formed on each

of the first and second active layers 112-1 and 112-2.” Kim-584, ¶63, Fig. 6. The active layers are “semiconductor” layers. Kim-584, ¶62.

It would be obvious to POSITAs that T2’s channel region is the active layer A2 under gate electrode G2, and T2’s source and drain extended on both sides of the channel. Kim-584, ¶63; Cok, ¶¶101-102.

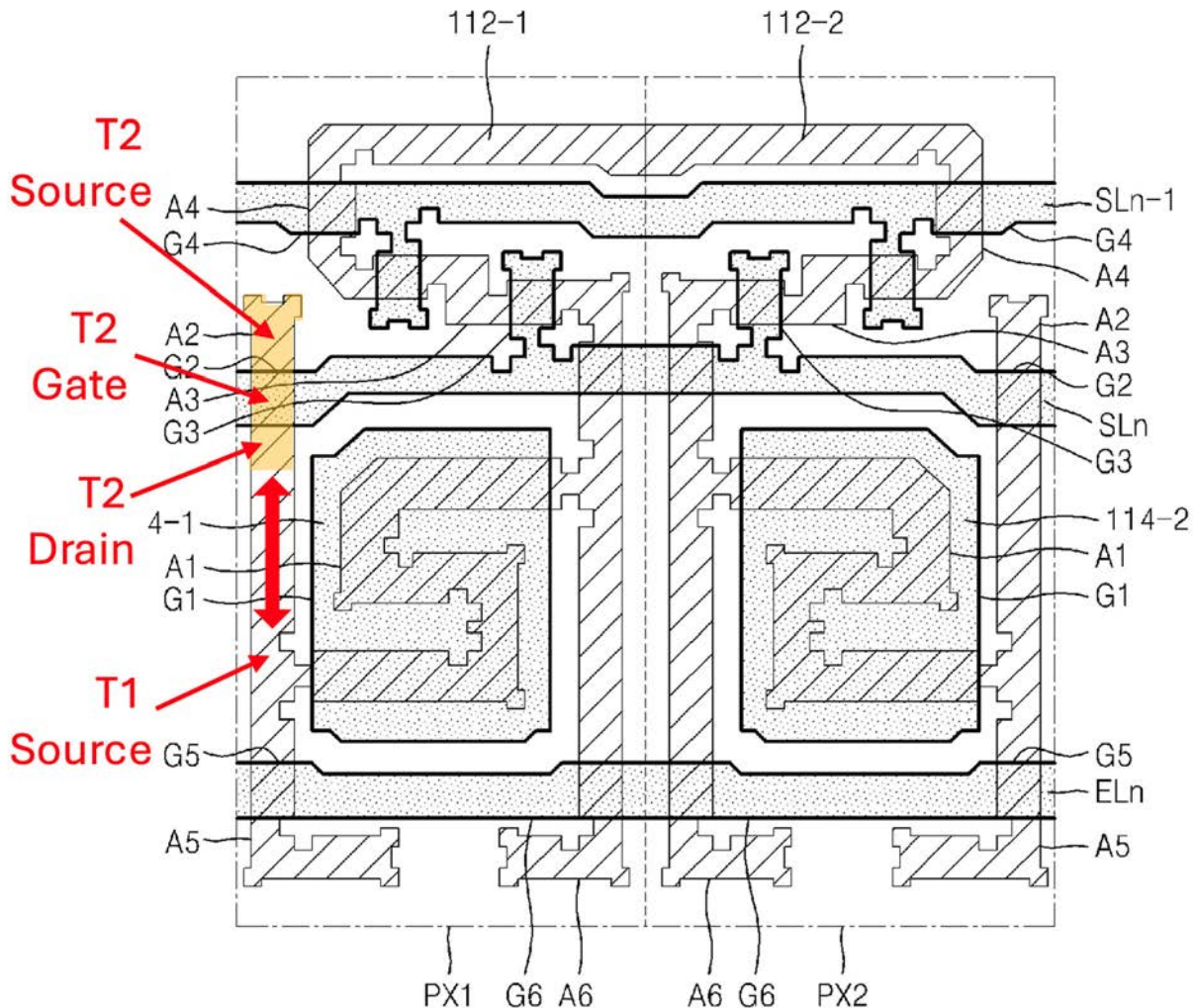


Fig. 6

Connection of T2's semiconductor ends are also evident from Fig. 6 (annotated above), showing T2's drain ("one end of second semiconductor") connected to T1's source ("one end of first semiconductor").

Fig. 8 (annotated below) shows connection of T2's source ("other end of second semiconductor") to DLm-1 ("first signal line") through connection hole Cnt4. Kim-584, ¶74: "signal lines DLm-1...are connected to the switching TFTs T2 through the fourth contact holes Cnt4." Cok, ¶¶99-104.

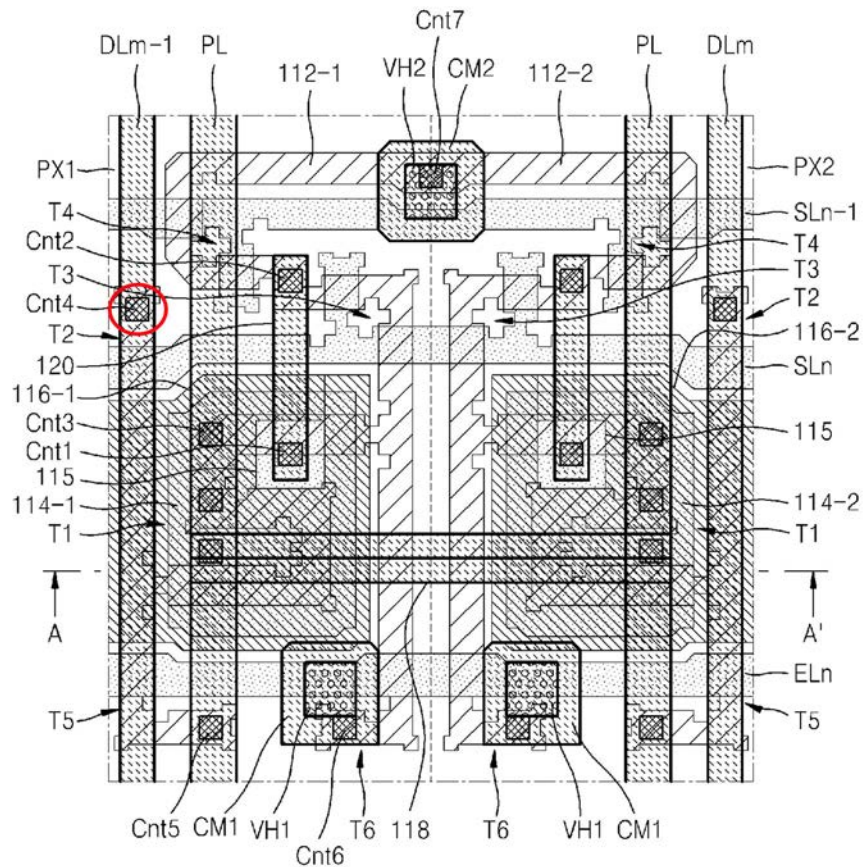


Fig. 8

4. Claim 4

Kim-584 discloses “a first voltage line” as voltage line PL/ELVDD. See §IV.A.1.d. and §IV.A.1.f.

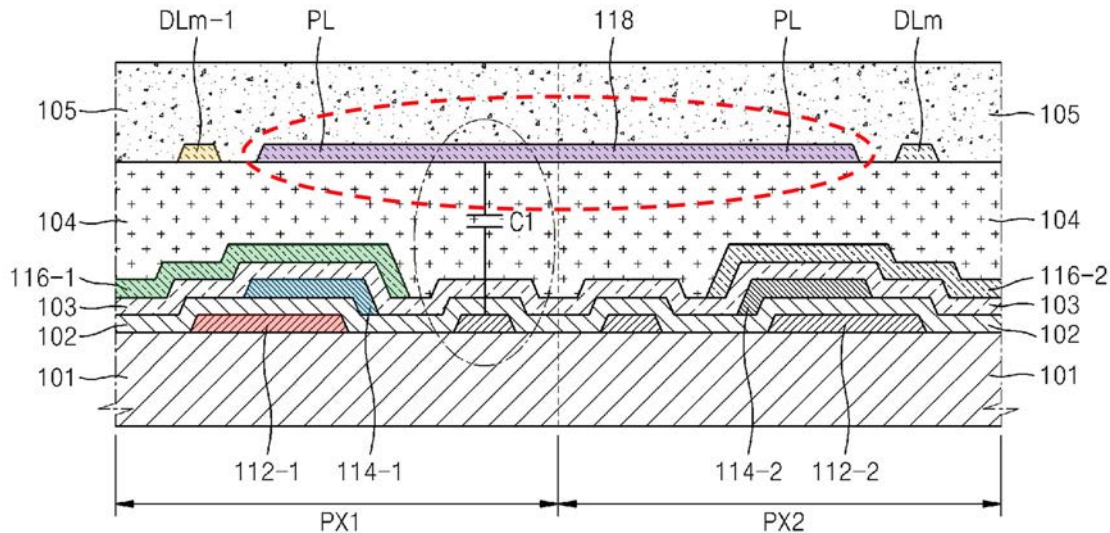


Fig. 9

Kim-584’s Fig. 9 (annotated above) shows voltage line PL (“first voltage line”) in the same layer as DLM-1 (“first signal line”). Kim-584, ¶77: **“data signal lines DLM-1...[and] the driving voltage lines PL...may be formed...on the same layer.”**

Additionally, Fig. 3 (annotated below) shows voltage line ELVDD (“first voltage line”) connected to top electrode Cst2 of capacitor Cst, corresponding to second capacitor electrode 116-1 (“second electrode layer”). *Id.*, Fig. 3, ¶52: “A second electrode Cst2 of the storage capacitor Cst is connected to the driving voltage

line PL.” *See also id.*, ¶¶72, 75, describing connections of PL to second capacitor electrode. Cok, ¶¶105-110.

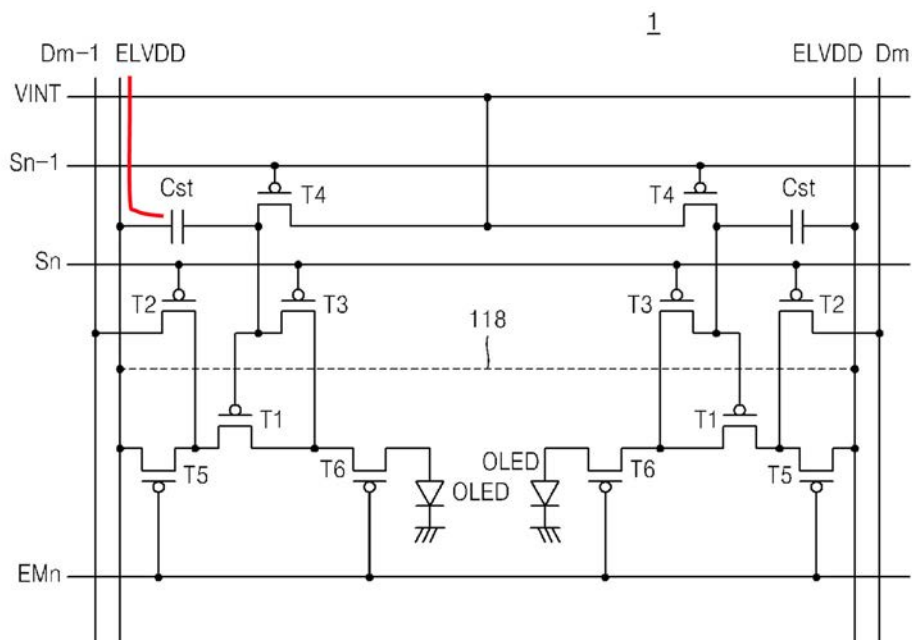


Fig. 3

5. Claim 8

a. 8[pre]:

Fig. 8 (annotated below) shows data line DLm-1 (“first signal line,” yellow) extends in a first direction.

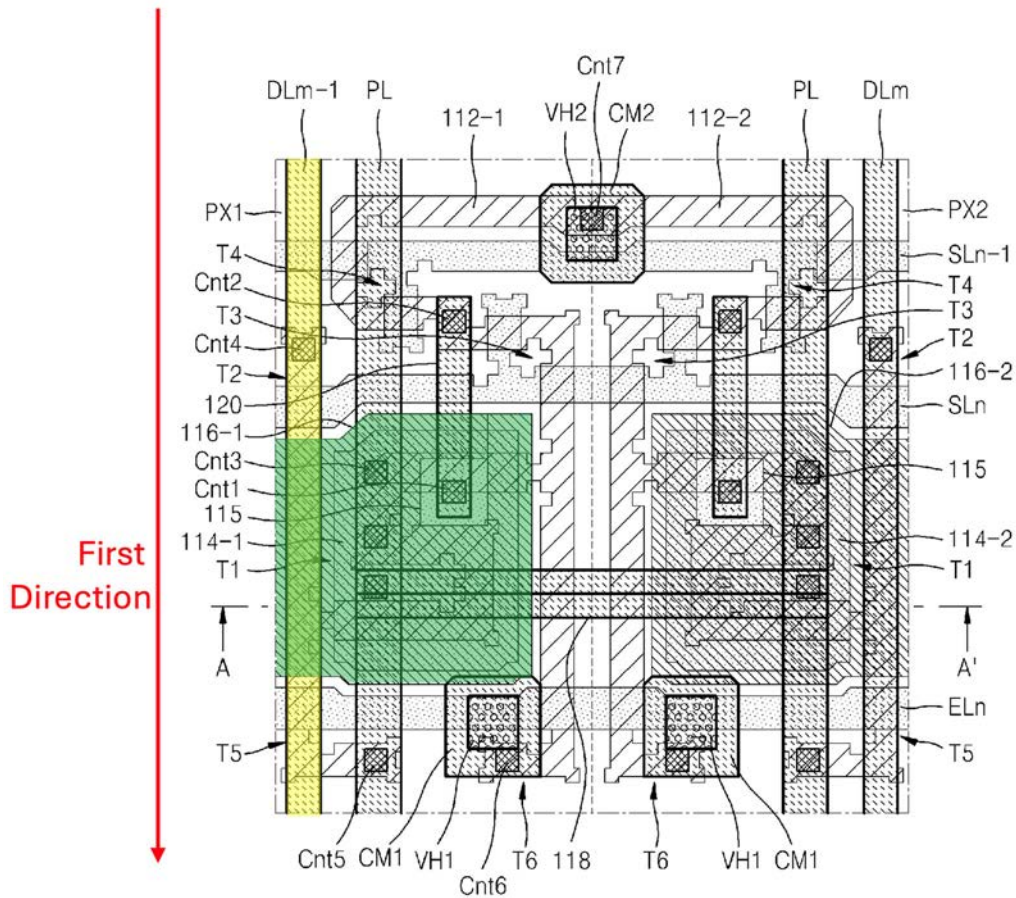


Fig. 8

b. 8[a]:

Fig. 7 (annotated/partially reproduced below) illustrates second capacitor electrode 116-1 (“first shield layer,” green) overlapping T1’s source area along “a”⁶

⁶ Claim 8 recites “a” length without requiring it to represent the shield layer’s longest dimension.

length L_A ,⁷ and second storage capacitor overlapping T1's drain area along length L_C . As shown, L_A is larger than L_B ("a length of the first electrode layer," blue) along the first direction.

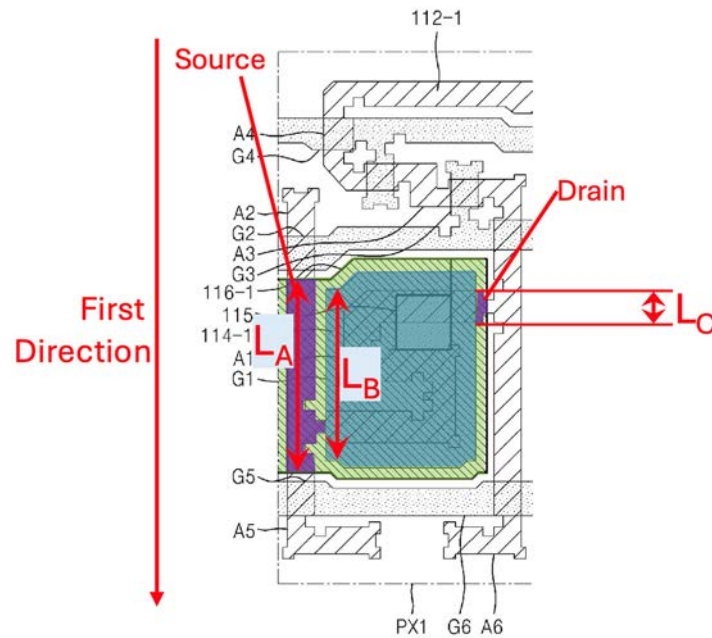


Fig. 7

POSITAs would have understood that source/drain areas comprise doped semiconductor regions (on two ends of the channel region). Notably, T1's source area has a length, L_A , extending to and merging with the semiconductor regions associated with T5's drain (D5) and T2's drain (D2). POSITAs would have readily

⁷ In 1[e], annotated Fig. 7 shows a smaller portion of T1's overlapped source area (purple annotation) than the extended annotation for claim 8. Limitations in 1[e] are also satisfied based on the extended overlapped source area shown here.

recognized this because of direct connections between S1, D2 and D5 in Kim-584's Figs. 7-8 (above) and Fig. 2 (annotated below), indicating doped semiconductor regions would be at the same voltage level, and thus considered a source region of T1.

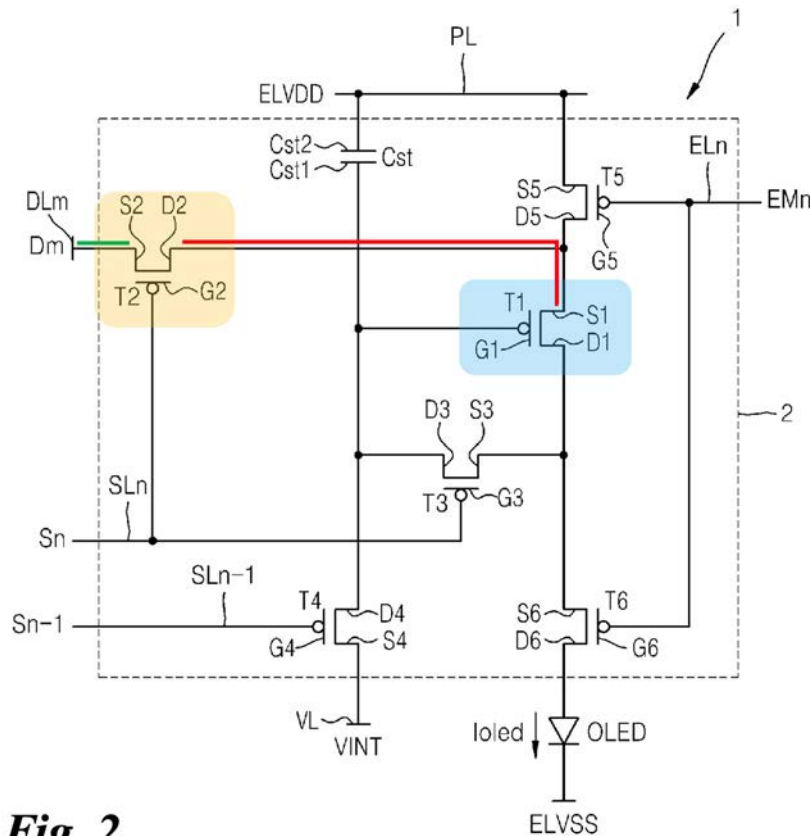
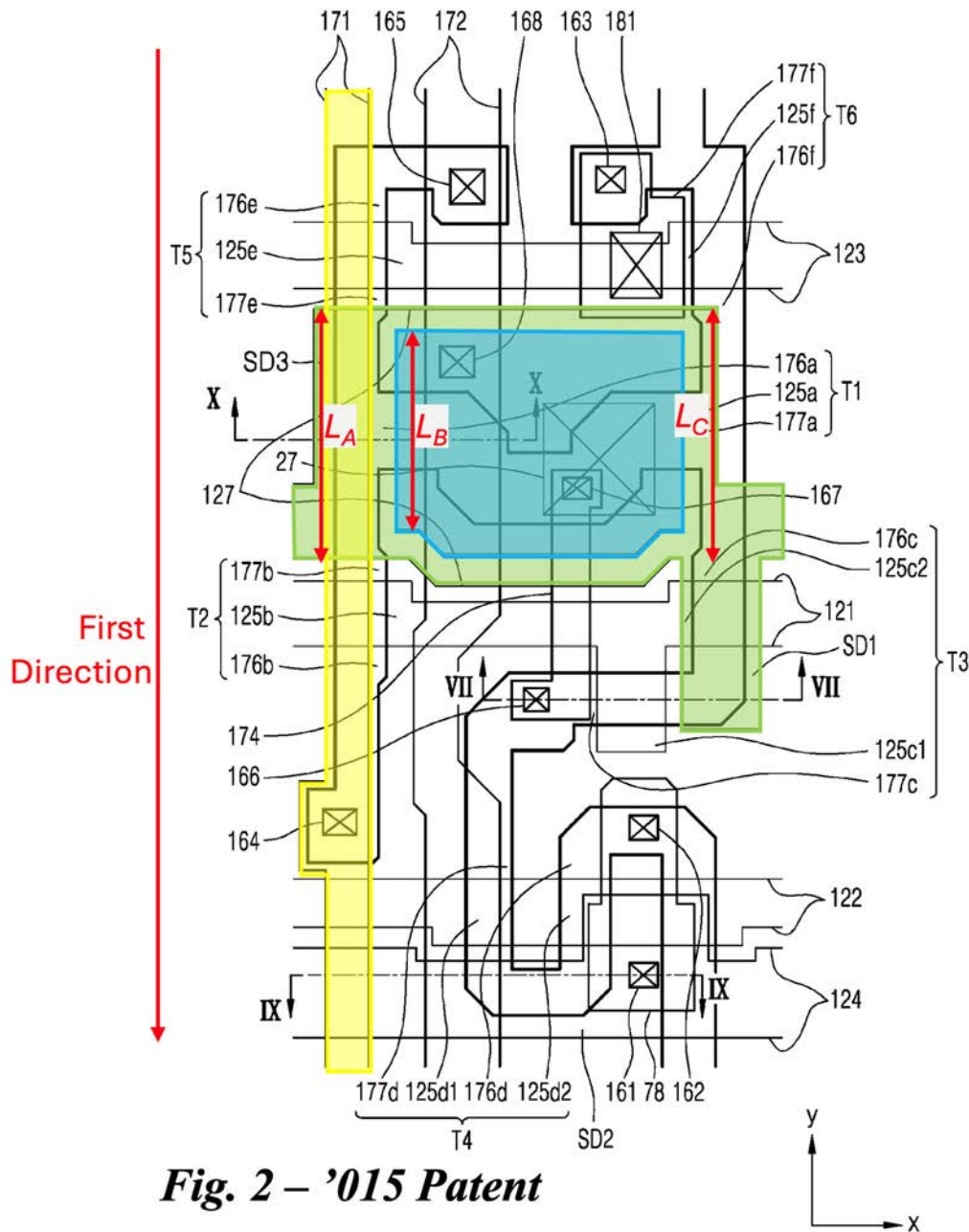


Fig. 2

Notably, Kim-584 explains, “[a]n active layer of each TFT includes a channel area which is not doped with impurities, and source and drain areas which are formed by doping both sides of the channel area with impurities.” Kim-584, ¶63. Accordingly, the contiguous semiconductor areas outside of undoped channel

regions of S1, D2 and D5 all have the same material and the same doping to maintain the same voltage. Cok, ¶¶113-117.

This interpretation is consistent with '015 patent, and indeed is the only way Claim 8 is supported by '015 patent, as illustrated by Fig. 2 (annotated below): length (L_A) of the overlapping part of shield layer (SD3) with source area (176a) and drain area (177a) can only be greater than length (L_B) of first electrode layer (125a) along the first direction, if an extended source region of T1 is adopted. Cok, ¶118.



6. Claim 9

Fig. 7 (annotated below) illustrates “part of one of the source area and the drain area of the first semiconductor” (purple annotations) are fully overlapped by

second capacitor electrode 116-1 (“the first shield layer”), with no gaps or holes.

§IV.A.1.f; Kim-584, Fig. 7; Cok, ¶¶120-124.

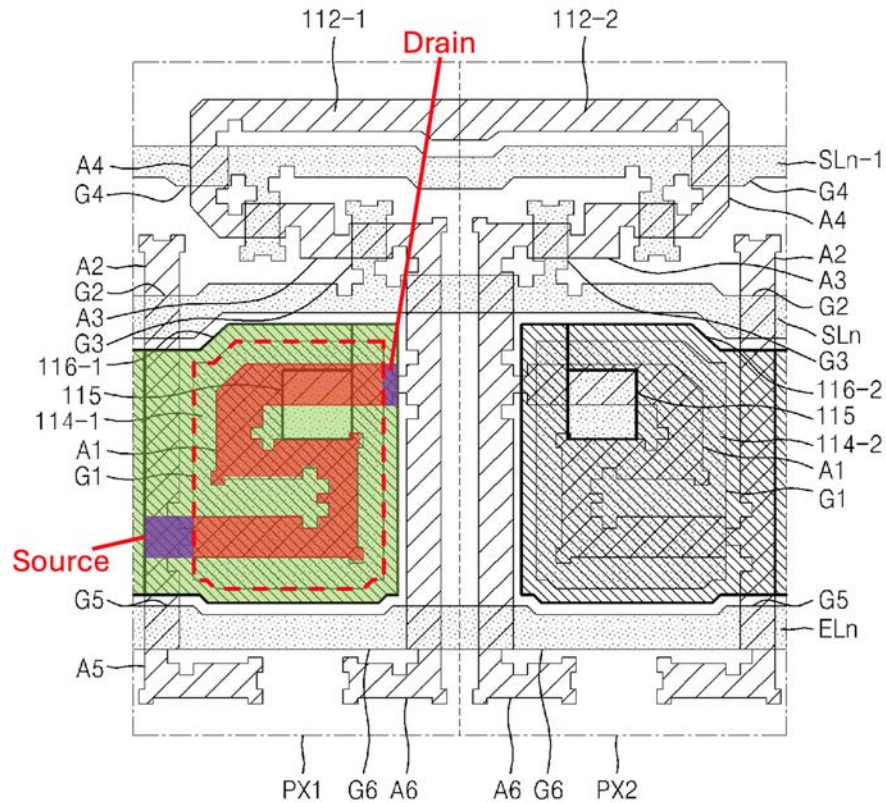


Fig. 7

7. Claim 10

a. 10[a]:

Fig. 8 (annotated below) shows data line DLm-1 (yellow) extends along the first direction.

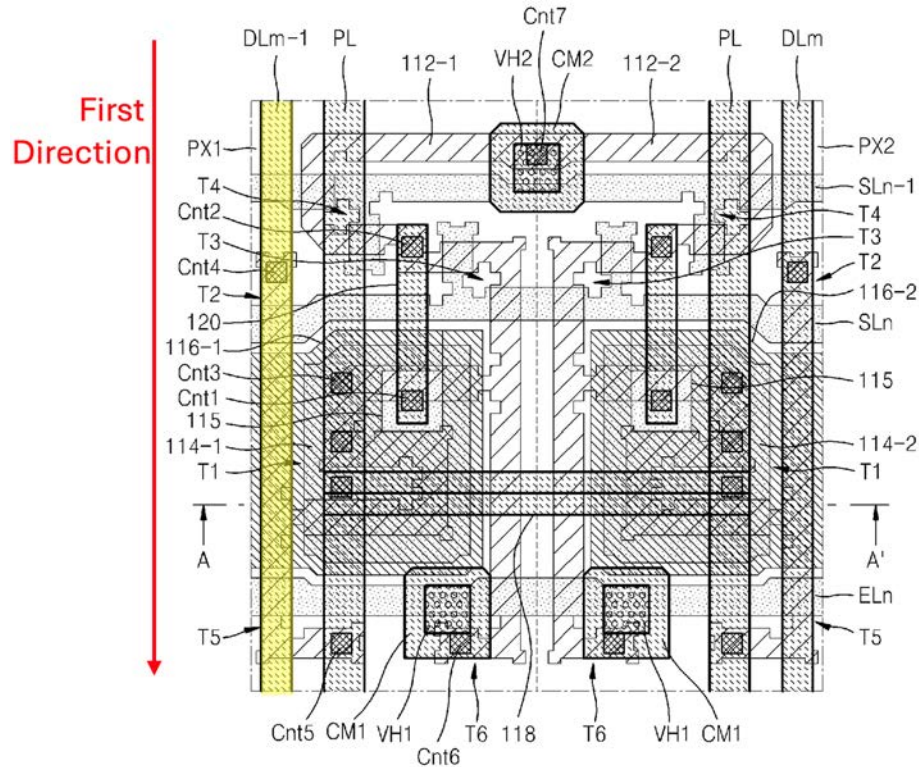


Fig. 8

b. 10[b]:⁸

Fig. 8 (annotated below) illustrates an overlapping part (red dashed box) of second capacitor electrode 116-1 (“first shield layer”) with data signal line DLM-1 (“first signal line”). Fig. 8 illustrates “a length of the first electrode layer along the first direction” (L_1) corresponds to a length of left side of first capacitor plate 114-1, which is part of the first electrode layer. §IV.A.1.c. Claim 10 recites “a” length, and L_1 is “a” length of the first electrode layer that is shorter than a length of the

⁸ In 10[b], “the overlapping part” lacks proper antecedent basis, and is assumed to recite “an overlapping part” in this Petition.

overlapping part (red dashed box) along the first direction, thus meeting limitation 10[b]. Cok, ¶¶125-131.

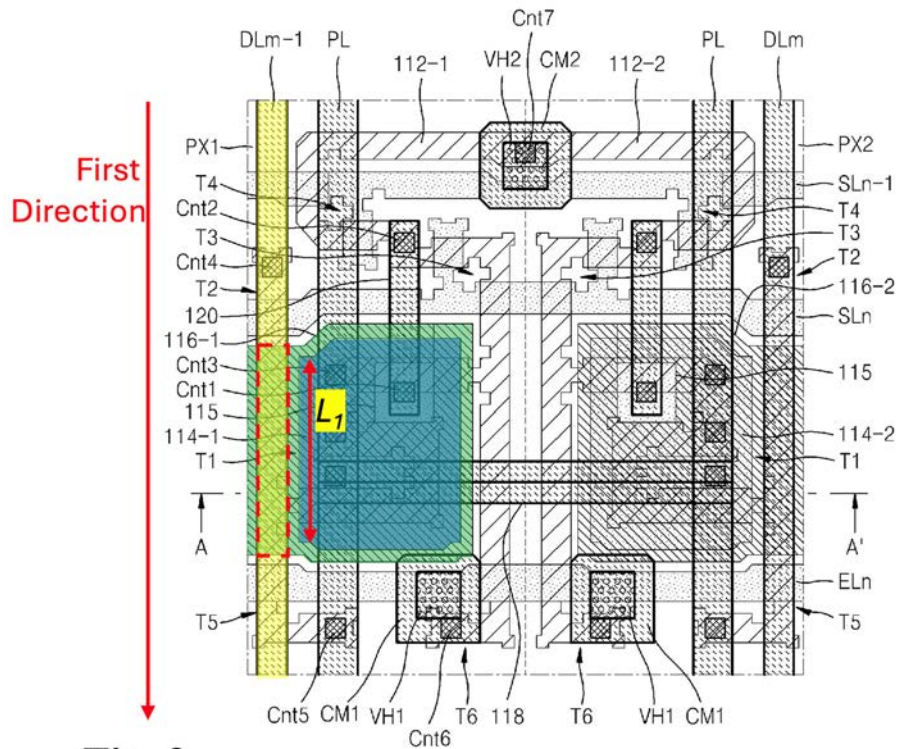


Fig. 8

8. Claim 20

a. 20[a]:

Base Claims 1 and 3 recite a “first” and a “second” TFT, respectively. Petitioner interprets Claim 20’s “fifth” TFT as a TFT other than first and second TFTs of base Claims 1 and 3. POSITAs would have understood that “first,” “second,” and “fifth” used herein were merely for convenience to distinguish the recited TFTs. *Free Motion Fitness, Inc. v. Cybex Int’l, Inc.*, 423 F.3d 1343, 1348 (Fed. Cir. 2005) (“As we have previously held, ‘[t]he use of the terms “first” and “second” is a

common patent-law convention to distinguish between repeated instances of an element or limitation.”).⁹

Kim-584 discloses “a fifth” TFT as TFT T5—see Fig. 3. As in 1[a] and Claim 3, Kim-584 discloses an active layer for each TFT, including an active layer A5 (“fifth semiconductor”) for T5 (“fifth” TFT). Kim-584, ¶63, Fig. 5; Kim-584’s active layers are “semiconductor” layers. Kim-584, ¶62.

Kim-584 explains, and shows in Fig. 3 (annotated below), T5’s drain (“one end of the semiconductor”) is connected (red) to T1’s source (“one end of first semiconductor”), and connected (blue) to T2’s drain (“one end of the second semiconductor”). *Id.*, ¶50, Fig. 3. Further, T5’s source (“other end of the fifth semiconductor”) is connected (green) to power line PL/ELVDD¹⁰ (“first voltage line”). *Id.*, ¶50: “**source electrode S5...is connected to the driving voltage line PL.**”

⁹ Accordingly, this Petition interprets “first,” “second,” “third,” etc., to designate another element without conveying a sequential significance.

¹⁰ PL and ELVDD are used interchangeably. §IV.A.1.f.

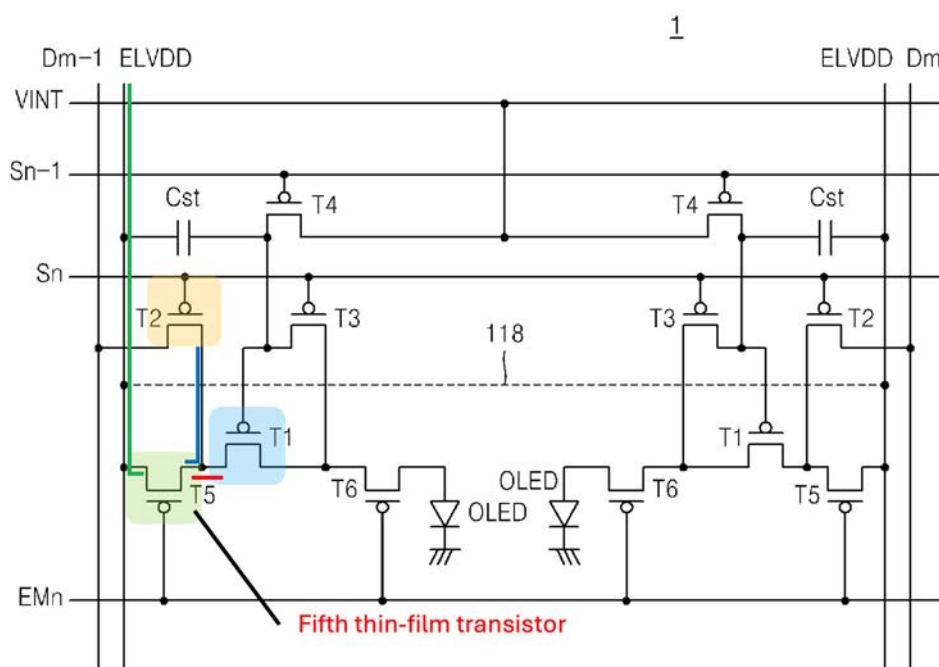


Fig. 3

Fig. 6 (annotated below) further shows connection of T5's semiconductor ends, with T5's drain ("one end of the fifth semiconductor") connected to T1's source ("one end of first semiconductor") and to T2's drain ("one end of the second semiconductor"), all being parts of the same contiguous semiconductor.

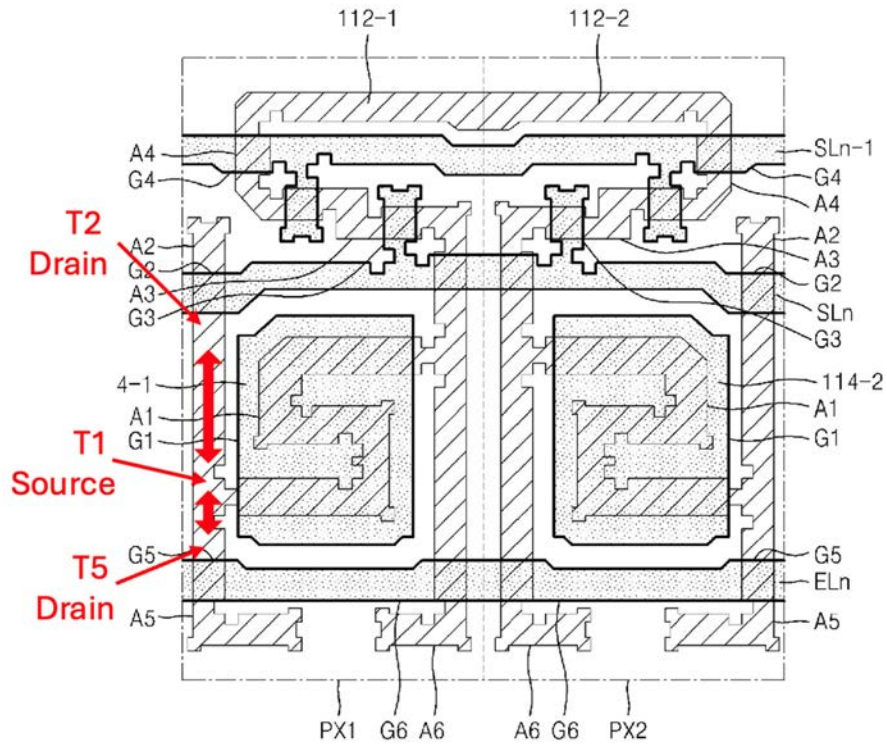


Fig. 6

Annotated Fig. 8 (below) shows connection of T5's source ("other end of the fifth semiconductor") to power line PL/ELVDD ("first voltage line") through contact hole cnt5. Kim-584, ¶72. Cok, ¶¶132-139.

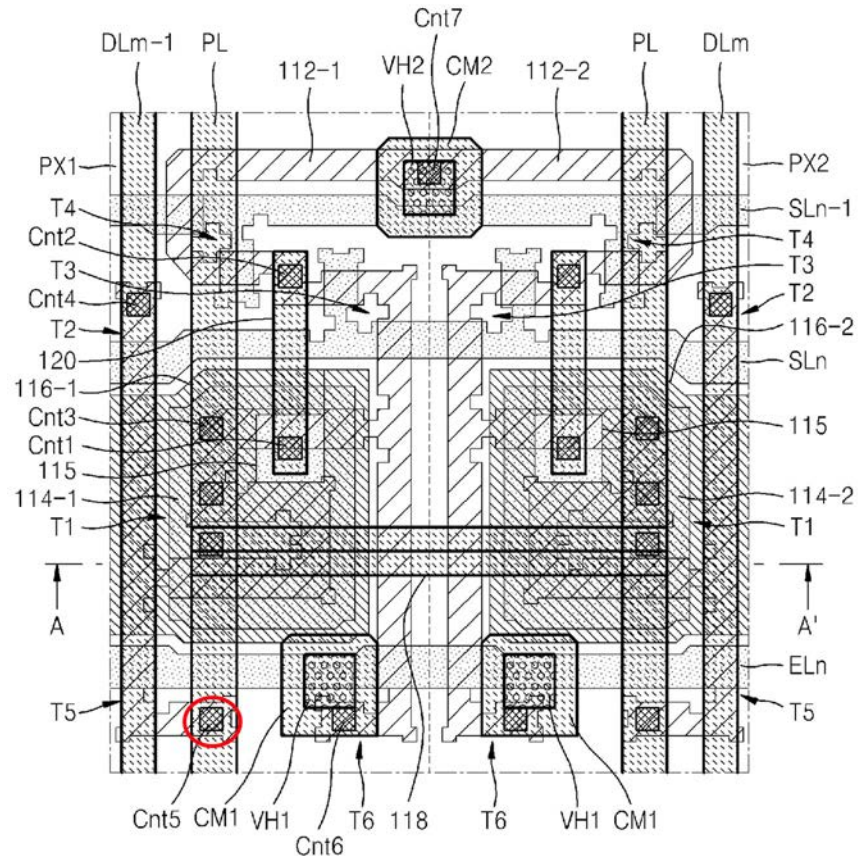


Fig. 8

b. 20[b]:

See Claim 4. § IV.A.4; Cok, ¶¶140-143.

9. Claim 21

a. 21[a]:

Kim-584's Fig. 8 (annotated below) shows a "fourth shield layer" as a portion of second capacitor electrode 116-1 (red rectangle, or a portion thereof). Kim-584, Fig. 8.

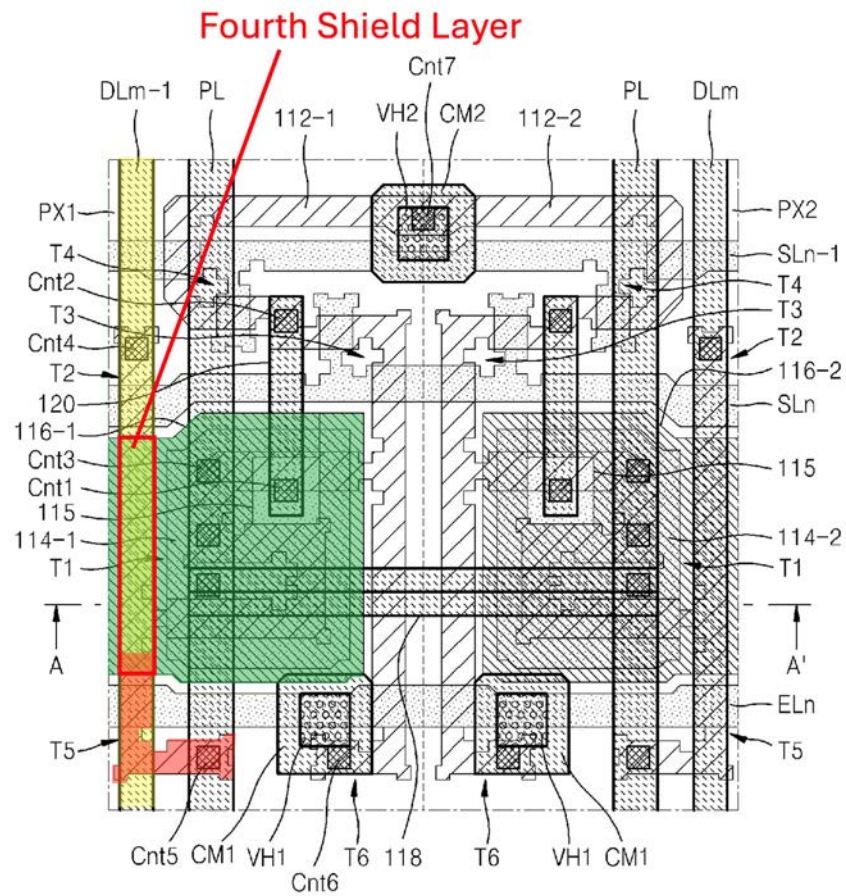


Fig. 8

Interpreting the first and fourth shield layers as parts of the same component (capacitor plate) is consistent with '015 patent, where SD1 and SD3 are parts of the same component. EX1001, FIG. 5.

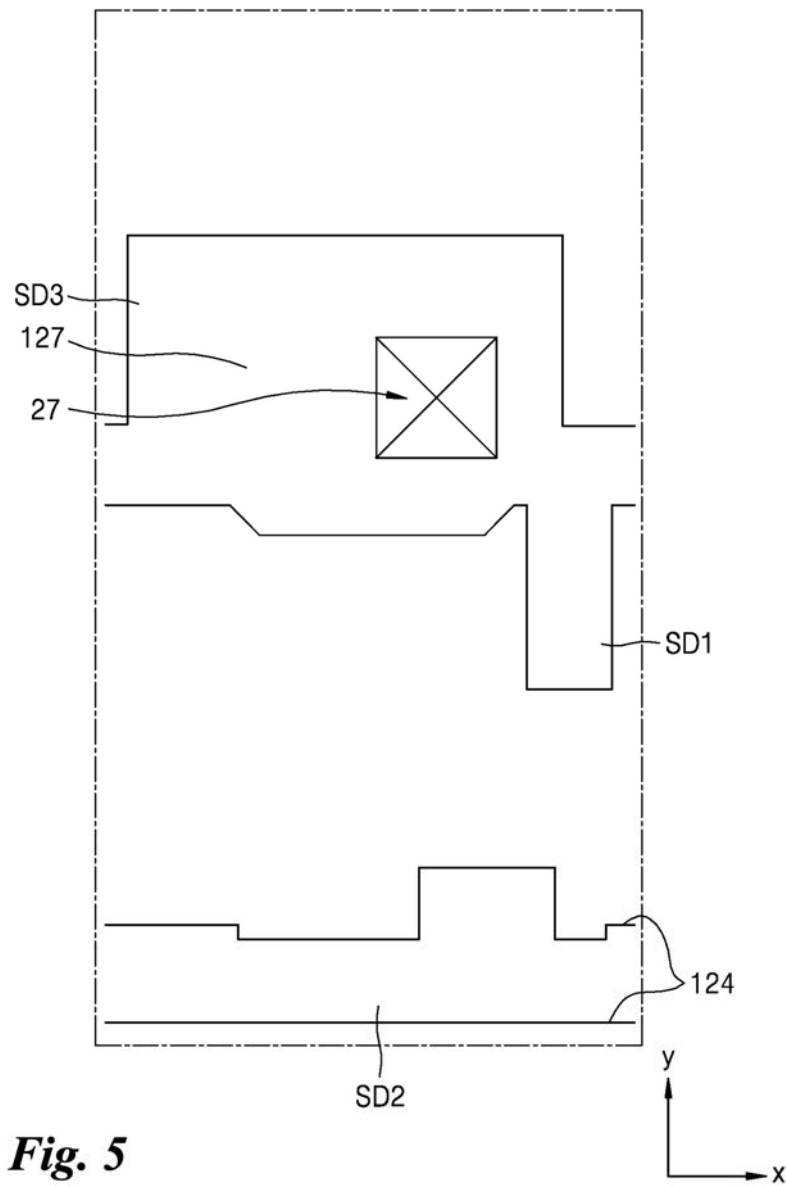


Fig. 5

Annotated Fig. 9 (below) shows second capacitor electrode 116-1 (green), and therefore, its portion forming the “fourth shield layer,” is in a layer between DLm-1 (“first signal line,” yellow) and semiconductor layer 112-1 (red), including its portion A5 (“fifth semiconductor”) that corresponds to T5 (“fifth” TFT). See Claim 20, §IV.A.8.a; Kim-584, ¶¶62, 63, Fig. 6. Cok, ¶¶144-148.

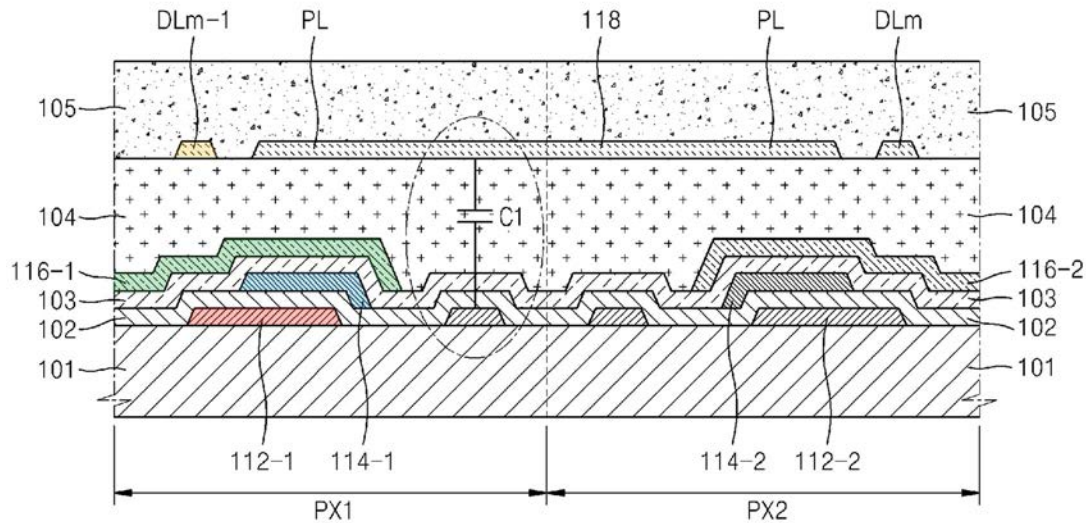


Fig. 9

b. 21[b]:

Kim-584 teaches or suggests this limitation. Kim-584’s Fig. 4 (annotated and cropped below left) shows a part of the semiconductor between the channel areas of T1 (“first” TFT), T2 (“second” TFT) and T5 (“fifth TFT”), and the figure on the right shows the fourth shield layer (red outline) overlapping substantially all of that semiconductor region. As explained in 21[a], all or only a portion of the red rectangle can be the “fourth” shield layer.¹¹ Cok, ¶¶149-152.

¹¹ Petitioner notes that “a” part of semiconductor between channel areas of the three TFTs can encompass a smaller portion of the active layer than the full region annotated in red (below left), in which case a smaller section of the red rectangle (a part of top capacitor electrode) forms the “fourth” shield layer.

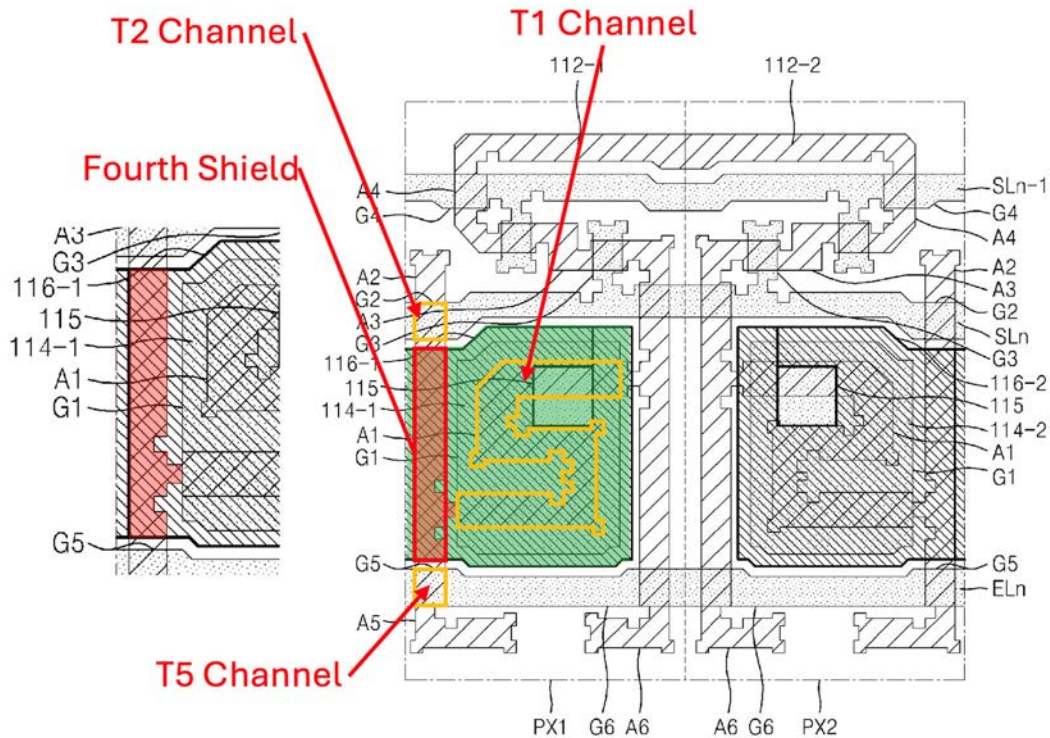


Fig. 7

10. Claim 22

See Claims 22 and 2, explaining the fourth shield layer is part of second capacitor electrode 116-1, which is in the second electrode layer. §§IV.A.10, IV.A.2; Cok, ¶¶153-155.

11. Claim 23

a. 23[a]:

See 1[a]-1[b], and Kim-584's Fig. 8 (annotated below) describing a first capacitor electrode 114-1 (blue) and a second capacitor electrode 116-1 (green) forming storage capacitor Cst. Kim-584, ¶¶46, 52; §§IV.A.1.b, IV.A.1.c. The electrodes have plate-like structures.

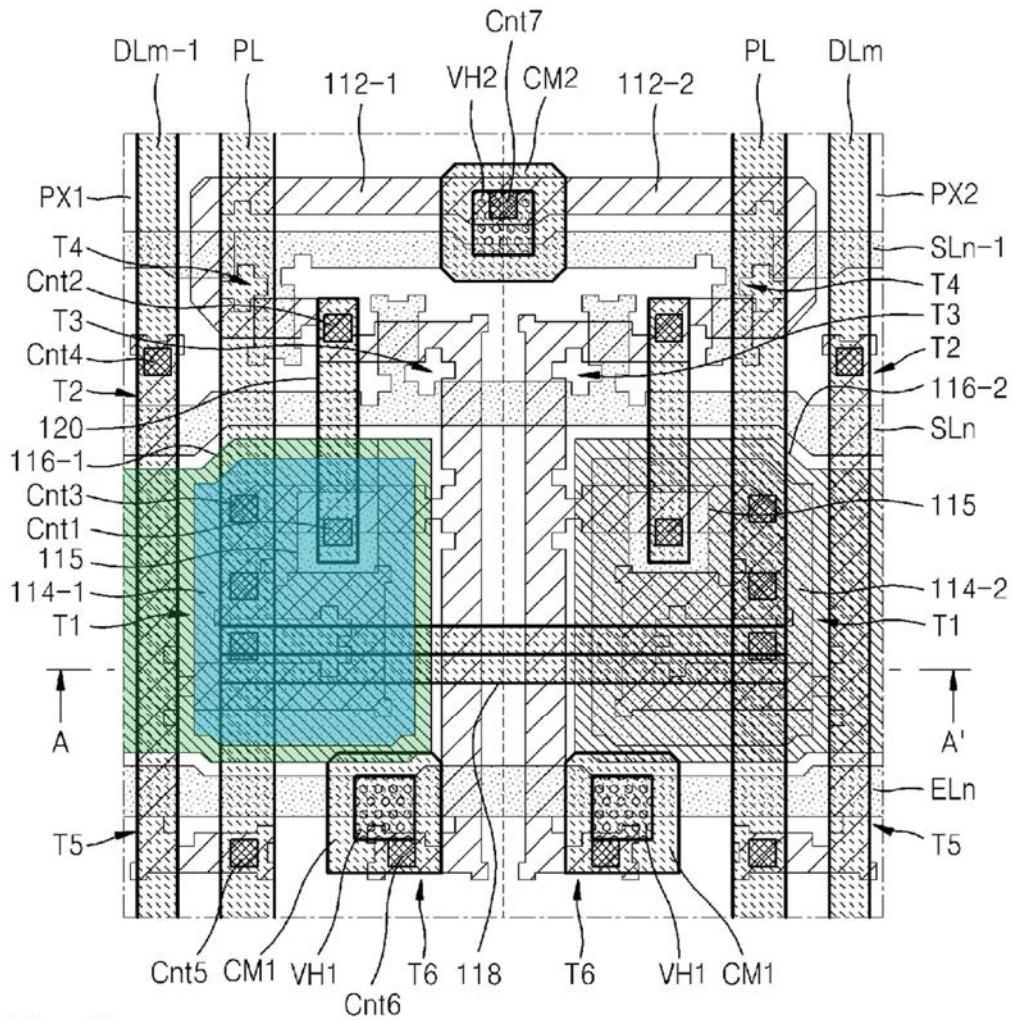


Fig. 8

b. 23[b]:

See 1[b]-1[c], discussing first capacitor plate 114-1 and second capacitor plate 116-1 being in the first and second electrode layers, respectively. §§IV.A.1.c, IV.A.1.d. Cok, ¶¶157-160.

12. Claim 33

a. 33[pre]-[e]:

See 1[pre]-[e]. §IV.A.1.a-§IV.A.1.f.

b. 33[f]:

See Claim 2. §IV.A.2.

c. 33[g]-[h]:

See 10[a]-10[b]. §IV.A.7.a-§IV.A.7.b.

Cok, ¶¶161-171.

B. Ground 1B: Kim-584-Han Combination Renders Obvious Claims 5, 11-14, 28-32.

1. Han

Han describes an OLED driving circuit with six transistors and two capacitors connected to voltage lines and data lines. Han, ¶¶3, 38-41, Fig. 2. Han's invention aims minimize/reduce leakage currents to improve the OLED display. *Id.*, ¶9. Han's driving circuit includes a standard storage capacitor, C1, and a second capacitor, C2, with the same (or similar) voltage as C1, thus maintaining the same voltages at nodes N1, N2 and N3 and minimizing/reducing the leakage currents. *Id.*, ¶¶48-49, 58, Fig. 2. Notably, while Han's Fig. 2 shows three gate-connected TFTs at M3 and M4, it explains two (or more) transistors can be series-connected. *Id.* ¶¶44-45.

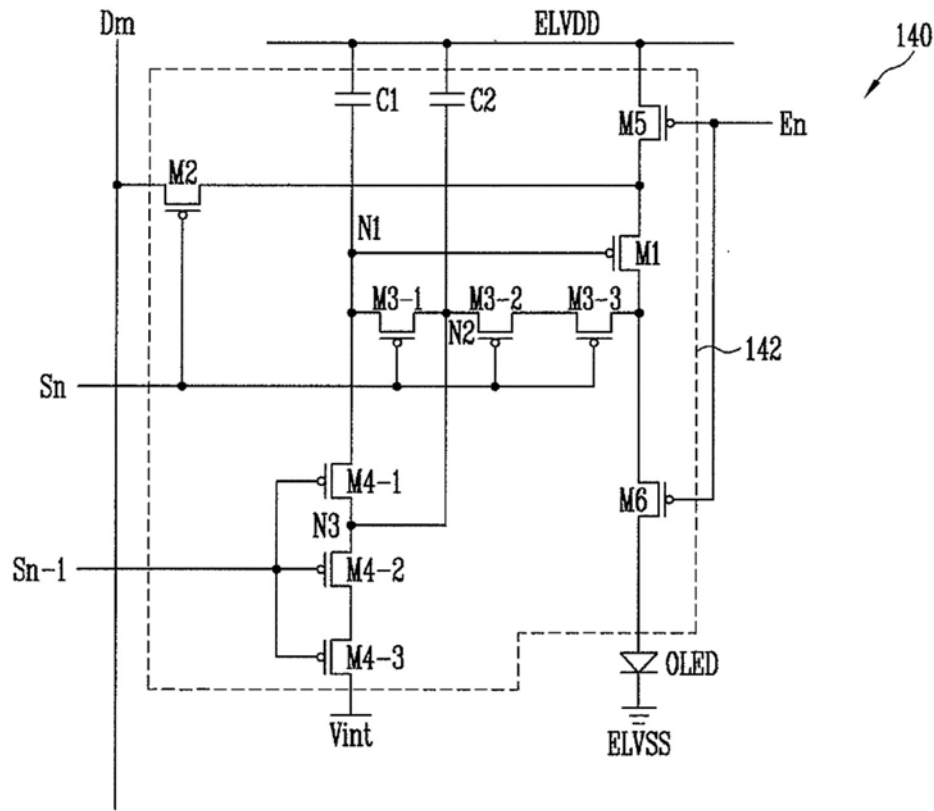


Fig. 2

2. Motivation to Combine

POSITAs would have been motivated to combine Han with Kim-584 because both references related to OLED displays utilizing TFTs, and particularly, six TFTs arranged in a typical OLED driving configuration. Kim-584, ¶¶44, 95, Figs. 2-3; Han, ¶¶38-41, Fig. 2. And both references sought to improve the operations of OLED displays and reduce leakage currents. Kim-584, ¶8; Han, ¶¶9, 58. Therefore, POSITAs would have been guided by the complementary teachings of the two references sharing a common goal, and would have understood that Kim-584's device can be improved based on the teachings of Han.

Notably, in the combination, POSITAs would have found it obvious that the leakage current in Kim-584's display device can be reduced by adding a second capacitor, C2, as Han described. POSITAs would have found motivation based on Han's express teachings that C2 in the designated location between voltage line ELVDD and connection node of multi-gated TFT M3 would "minimize[e] or reduc[e] the leakage currents." *Id.*, ¶58, Fig. 2.

Furthermore, POSITAs would have been motivated to apply a known technique (using Han's second capacitor) to a known device ready for improvement (Kim-584's OLED pixel) to yield predictable results (reduced leakage current). POSITAs would have had a reasonable expectation of success because adding a second capacitor to the OLED circuit was a routine design task, was taught by Han, and modifications were well within POSITAs skillset. *Cok*, ¶¶174-178.

Additional motivations are provided below.

3. Claim 5

a. 5[pre]:

See Claim 1. §IV.A.1.

b. 5[a]:

Kim-584 teaches "a third" TFT, namely T3, which includes an associated active semiconductor layer A3 ("third semiconductor"). Kim-584, ¶¶62-63. Fig. 3 (annotated below) shows T3's source ("one end of third semiconductor") connected

(line A) to T1's drain ("one end of first semiconductor"), and T3's drain ("other end third semiconductor") connected (line B) to storage capacitor plate Cst1, which is in the first electrode layer, operating as T1's gate (G1). *Id.*, Fig. 3, ¶48; *see also* §IV.A.1.c.

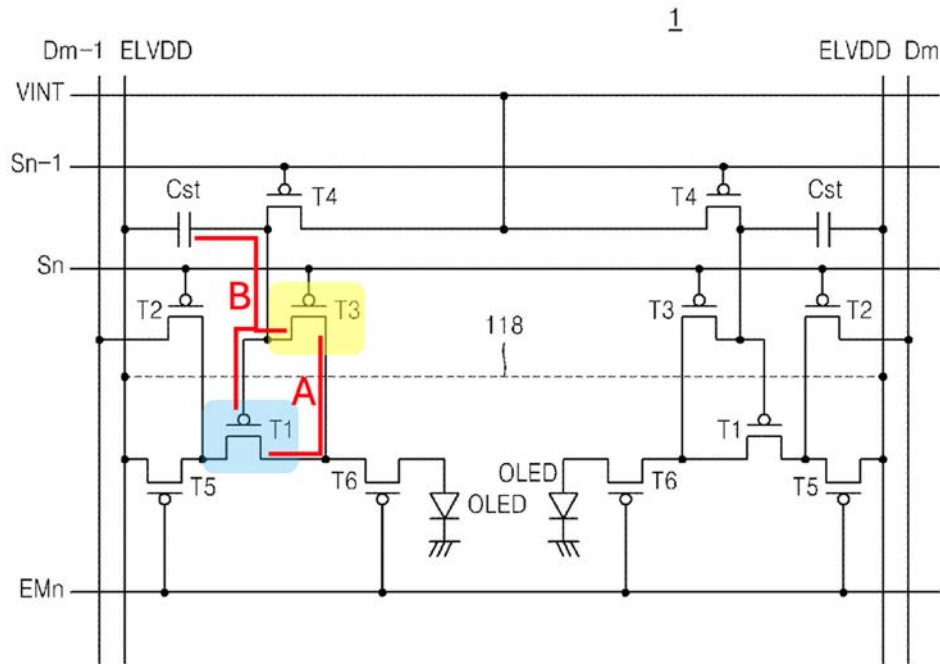


Fig. 3

Fig. 6 (annotated below) shows connection of T3's semiconductor ends, where T3's source ("one end of third semiconductor") is connected to T1's drain ("one end of first semiconductor").

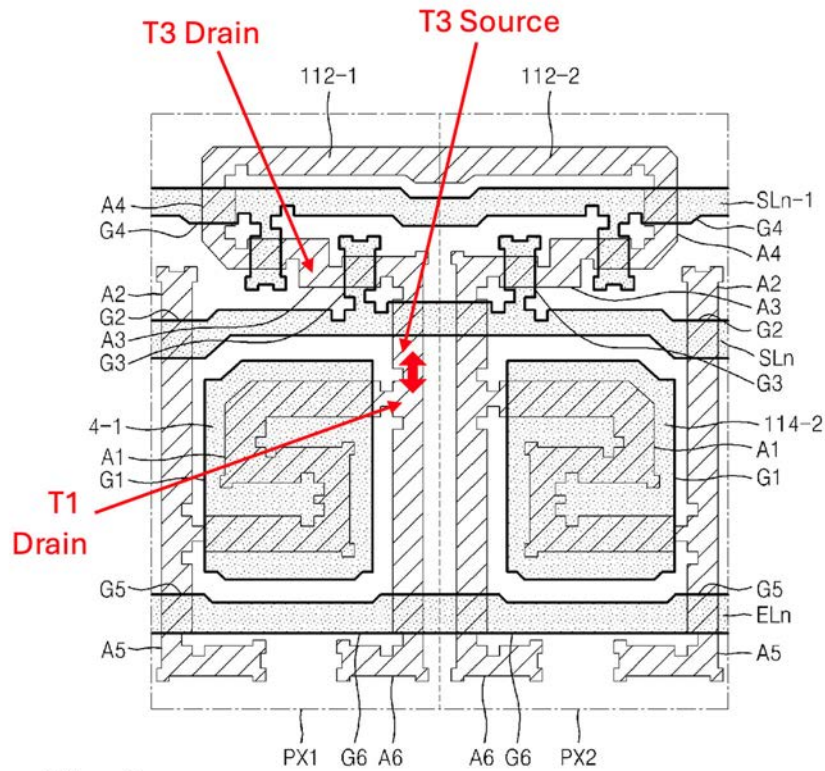


Fig. 6

Fig. 8 (annotated below) shows connection of T3's drain ("other end third semiconductor") to storage capacitor's first electrode Cst1 (114-1) through contact holes cnt1, cnt2 and connection line 120. Kim-584, ¶¶73, 76. Cok, ¶¶179-185.

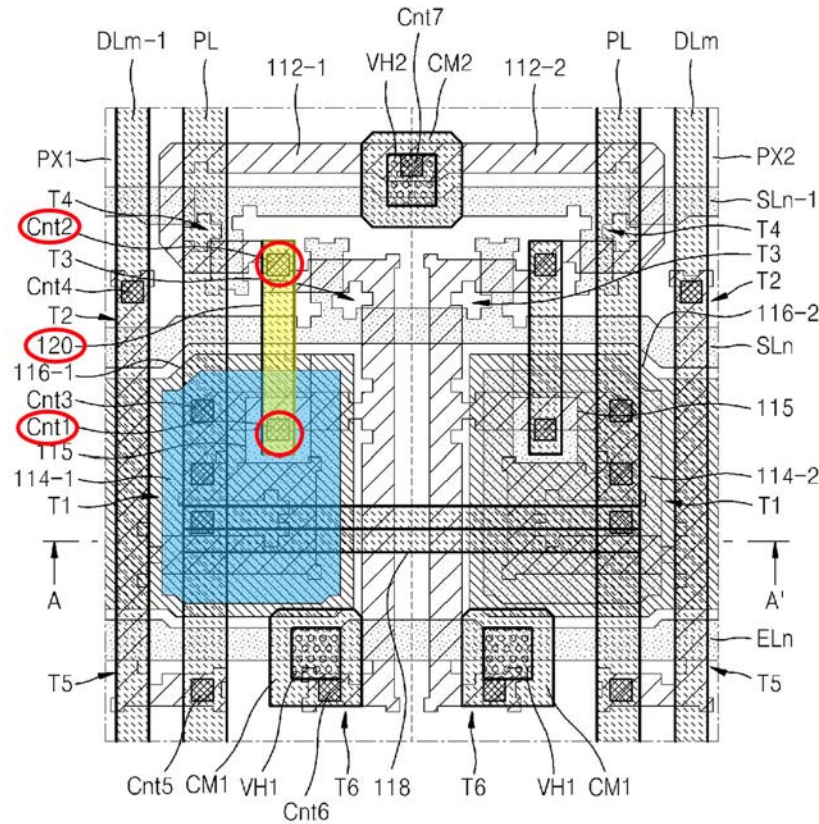


Fig. 8

c. 5[b]:

Kim-584's Fig. 7 illustrates T3 is a double-gated transistor because it includes two gate electrodes (red circles A and B annotated below) where the scan line (blue) overlaps T3's semiconductor A3. Kim-584, ¶¶45, 48. POSITAs would have understood that the semiconductor region under one gate electrode of T3 constitutes the "first channel area" and the semiconductor region under T3's other gate electrode constitutes the "second channel area," and annotated area C is a part of semiconductor A3 between the two channel areas. *Id.* See also Kim-584, ¶63.

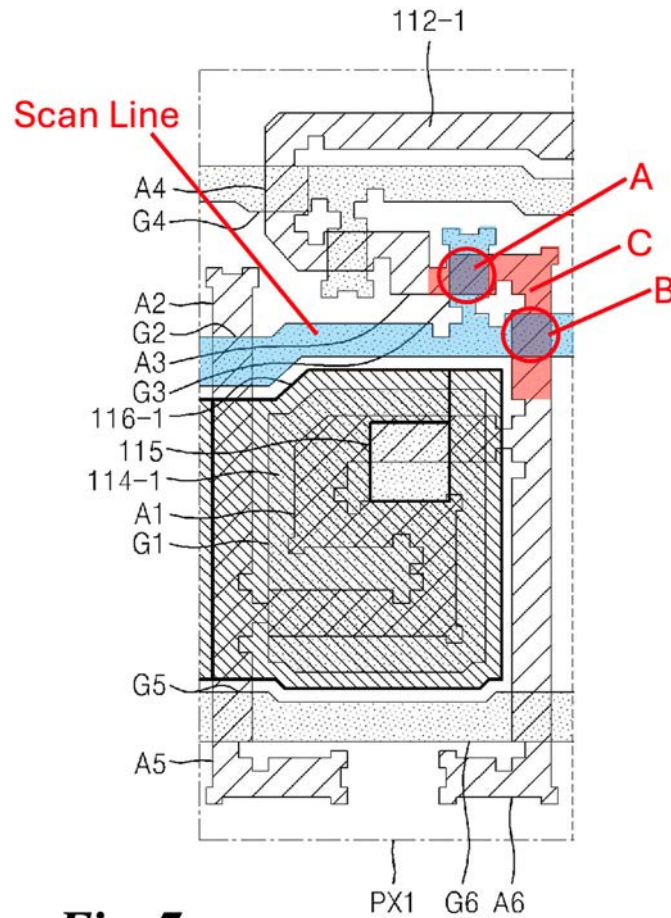


Fig. 7

Kim-584 does not explicitly recite a second shield layer. However, this would have been obvious based on the teachings of Han, which describes a similar 6-TFT circuit, with multi-gated TFTs (at least two transistors in series, Han, ¶¶28, 44-45, Fig. 2) and a storage capacitor (Han's C1; Kim-584's Cst) which additionally includes a second capacitor, C2, to further reduce leakage currents. *Id.*, ¶¶28, 58. POSITAs would have found it obvious to combine Kim-584 with Han to achieve Han's desirable leakage current reduction.

Han does not provide a pixel layout diagram but in Fig. 2 and associated description explains second capacitor C2 is “coupled to the first power supply (ELVDD), and [capacitor’s] first terminal...is coupled to both a second node N2 and a third node N3.” Han, ¶49, Fig. 2 (annotated below).

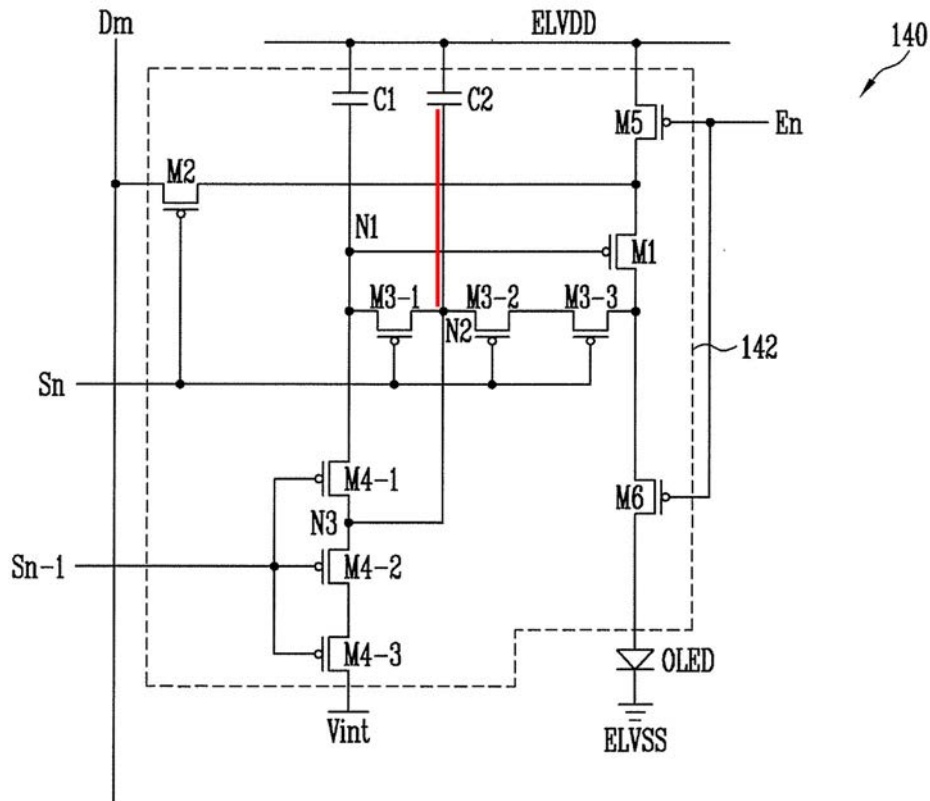


Fig. 2

Based on Fig. 2’s explicit connections, POSITAs would have known the lower plate of capacitor C2 must be connected to the drain-source junction between the two series transistors (at N2). In combination with Kim-584, this junction would be the doped (and thus conductive) semiconductor area between the two gates of T3. Therefore, POSITAs would have understood that an obvious and advantageous

location for placing the plates of capacitor C2 would be at or above the designated junction (see annotated Fig. 7 below) because it was close to (directly above or at) the semiconductor junction of interest (node N2), and would have allowed easy and direct connection of C2's lower capacitor plate to the junction, as required by Han's Fig. 2.

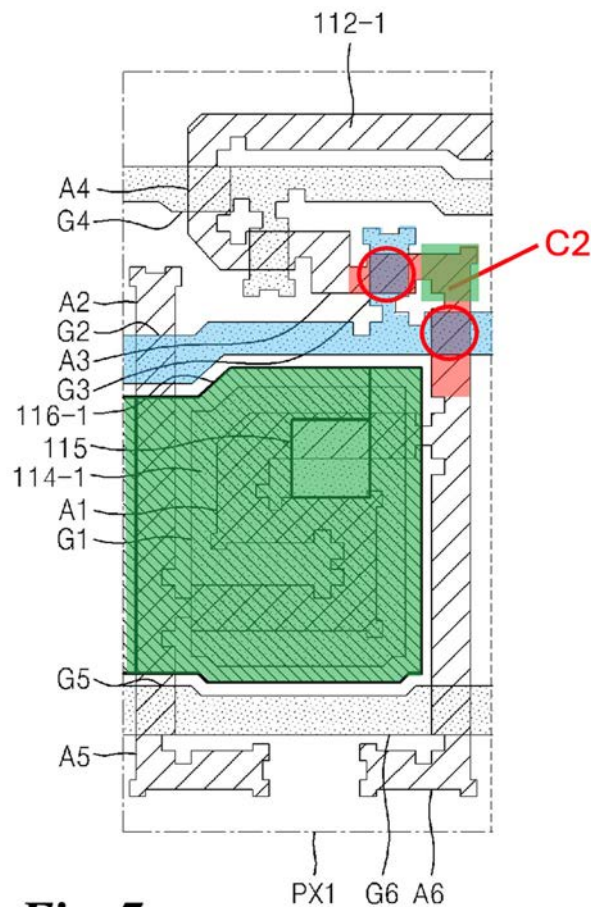


Fig. 7

Notably, POSITAs would have understood that C2's lower plate would be implemented as part of the semiconductor layer at junction N2 between the dual gates, because Kim-584 explained the semiconductor layer can be doped and thus

made conductive (Kim-584, ¶¶62, 63); indeed, this was a known technique. See Moon, ¶76; Cok, ¶191, citing EX1026, Fig. 5, element 110. Alternatively, POSITAs would have understood that C2's lower plate would be positioned above the doped junction (over an insulating layer) between T3's dual gates and connected to the doped junction (e.g., using a "via"); Kim-584 similarly places C1's lower capacitor plate 144-1 above the semiconductor layer over an insulating layer. Kim-584, ¶66, Fig. 9; Cok, ¶¶186-192.

The upper capacitor plate of C2 would be connected to voltage line, ELVDD (line 172), as required by Han's Fig. 2. Han, ¶49, Fig. 2. POSITAs would have found it obvious (and a matter of routine layout design) to implement that connection. For example, POSITAs would have connected the upper capacitor plate of C2 to upper capacitor plate (116-1) of storage capacitor, Cst, using a connection line, as shown for illustration purposes in the annotated figure below. This connection would have been obvious and advantageous because the upper plate of C1 (element 116-1 in Kim-584) was nearby and was already connected to ELVDD. *Id.*, see also Kim-584, Fig. 3, showing Cst-to-ELVDD connection, and Han, Fig. 2, showing C1-to-ELVDD connection. Accordingly, the upper plates of both capacitors would be in the same layer, connected together and connected to ELVDD. Cok, ¶193; see also *id.*, ¶¶408-410, citing EX1012, EX1028.

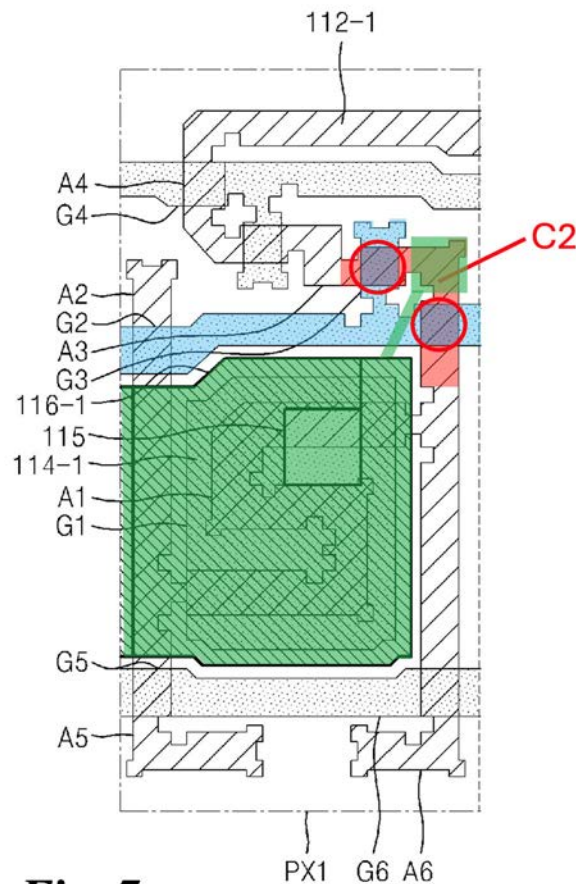


Fig. 7

In the combination, C2's upper capacitor plate, being connected to a constant voltage source (ELVDD), would be the "second shield layer" for the same reasons discussed in §IV.A.1.f. C2 capacitor's upper plate, being above its lower plate, would overlap A3's ("third semiconductor's") region between T3's dual gates (annotated figure above), and would thus overlap "a part between a first channel area and a second channel area of the third semiconductor." Furthermore, the "second shield layer" would be in "a layer between the first signal line and the third semiconductor" because C2's upper plate would reside in the same layer as storage

capacitor's upper plate (element 116-1, green in Fig. 7 below), which as explained in §IV.A.1.f, is between the semiconductor layer (active layer 112-1 and A3 portion) and the first signal line, DLm-1. *Id.* Cok, ¶¶194-195.

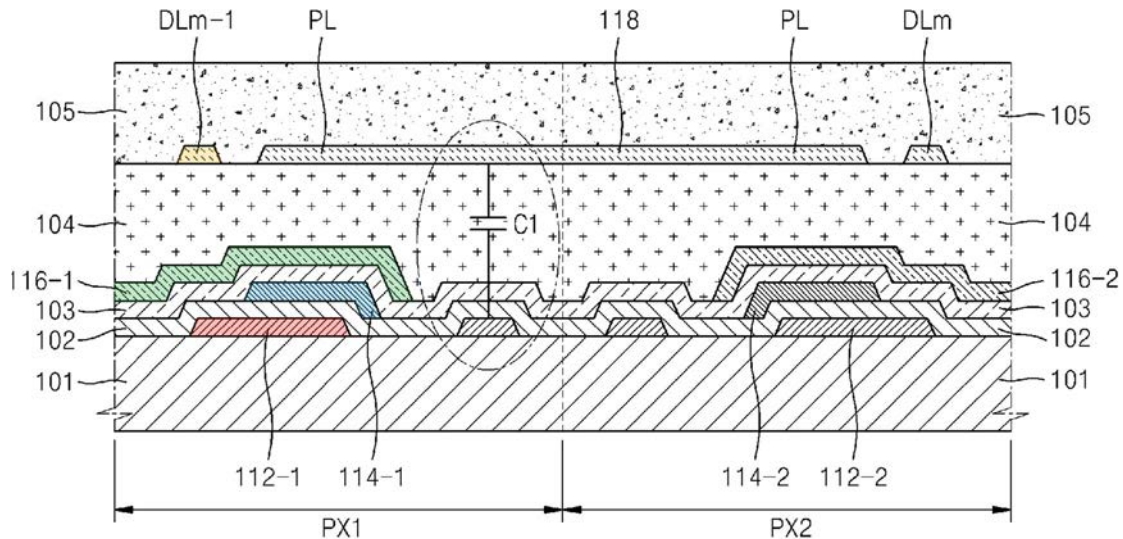


Fig. 9

4. Claim 11

a. 11[a]:

See Claim 5 (§IV.B.3.c), explaining T3's two gate electrodes at locations where scan line (blue) overlaps active layer A3 (red). Kim-584, ¶¶45, 48, 63. POSITAs would have understood, from Kim-584's Fig. 7, that one gate electrode of T3 overlaps the first channel area ("first channel area of third semiconductor"), and the other gate electrode overlaps the second channel area ("second channel area of third semiconductor"). *Id.* The two gate electrodes are in the same layer because they are both part of the same scan line. *Id.*

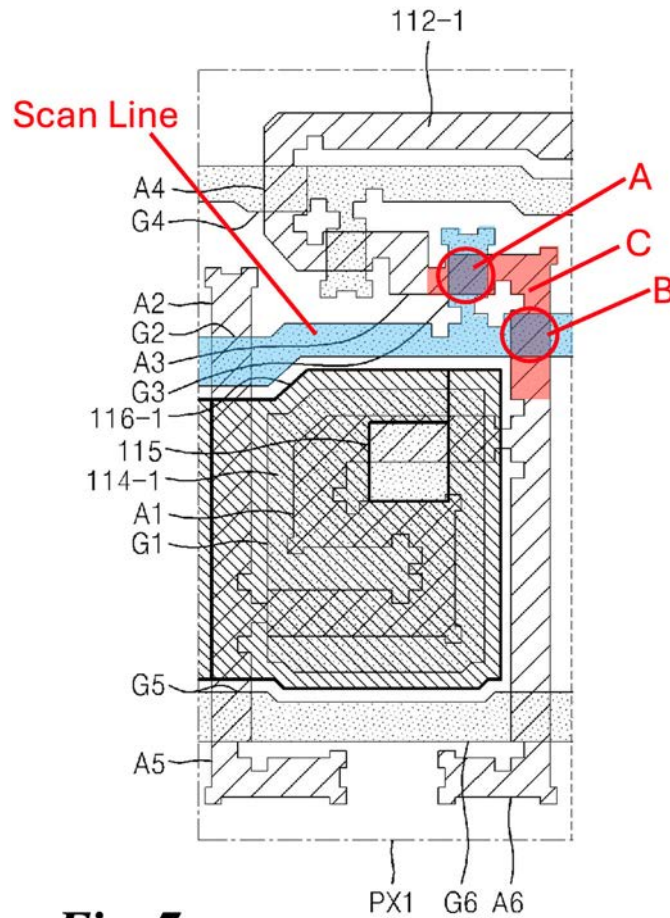


Fig. 7

b. 11[b]:

T3's gate electrodes are formed as part of scan line SLn ("second signal line"). Kim-584, ¶48: "A gate electrode G3 of...T3 is connected to the first scan line SLn." SLn ("second signal line") crosses data line DLm ("first signal line"): "The data signal line DLm intersects with the first scan line SLn." *Id.*, ¶45; see also *id.*, Fig. 8, showing SLn crossing DLm-1; §IV.A.1.e, explaining DLm-1 being the "first signal line."

Kim-584's SLn ("second signal line") is in the same layer as the first capacitor electrode 114-1 ("first electrode layer;" *see* §IV.A.1.d): "A **first gate lines are formed on the first gate insulating layer 102. The first gate lines may include a first scan line SLn...and first capacitor electrode[] 114-1.**" Kim-584, ¶66. Cok, ¶¶196-202.

5. Claim 12

Kim-584's voltage line PL/ELVDD ("first voltage line;" *see* §IV.A.1.d) is in the same layer as data line DLm-1 ("first signal line"). Kim-584 ¶45, Fig. 9 (annotated below). As explained in Claim 5, top electrode of capacitor C2 ("second shield layer") is connected to ELVDD ("first voltage line"). *See* §IV.B.3.c; Cok, ¶¶203-205.

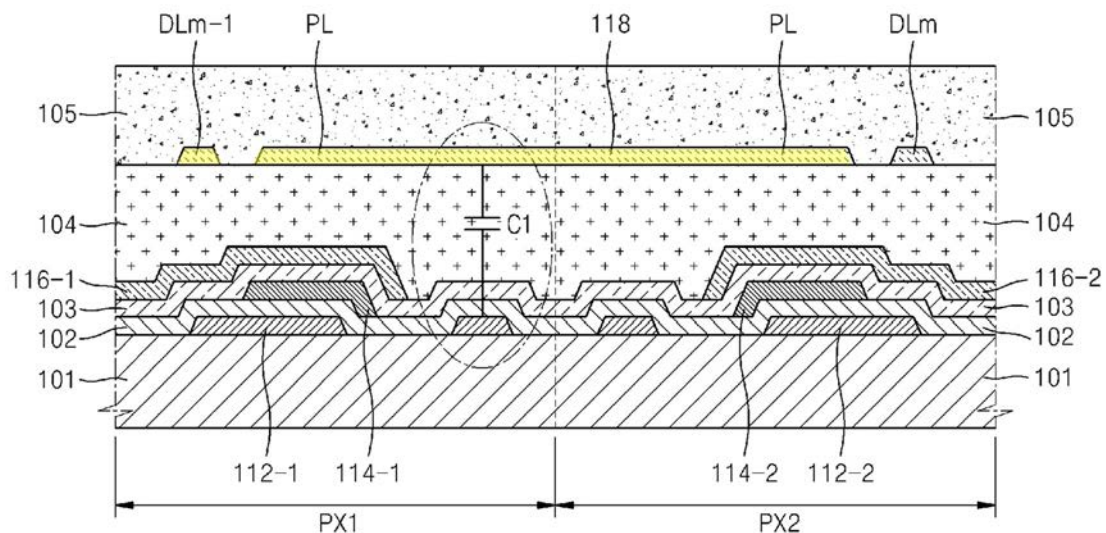


Fig. 9

6. Claim 13

See Claims 2 and 5, explaining C1's top electrode is part of the second electrode layer (see §IV.A.2) and top electrodes of both capacitors C1 and C2, in the combination, would be in the same layer. §IV.B.3.c. Therefore, C2's top electrode ("second shield layer") would be part of the second electrode layer. Cok, ¶¶206-207.

7. Claim 14

Kim-584 Fig. 3 (annotated below) shows T3's drain ("other end of the third semiconductor") connected to storage capacitor's first electrode (lower plate Cst1) and to T1's gate electrode ("first electrode layer")—line B below.

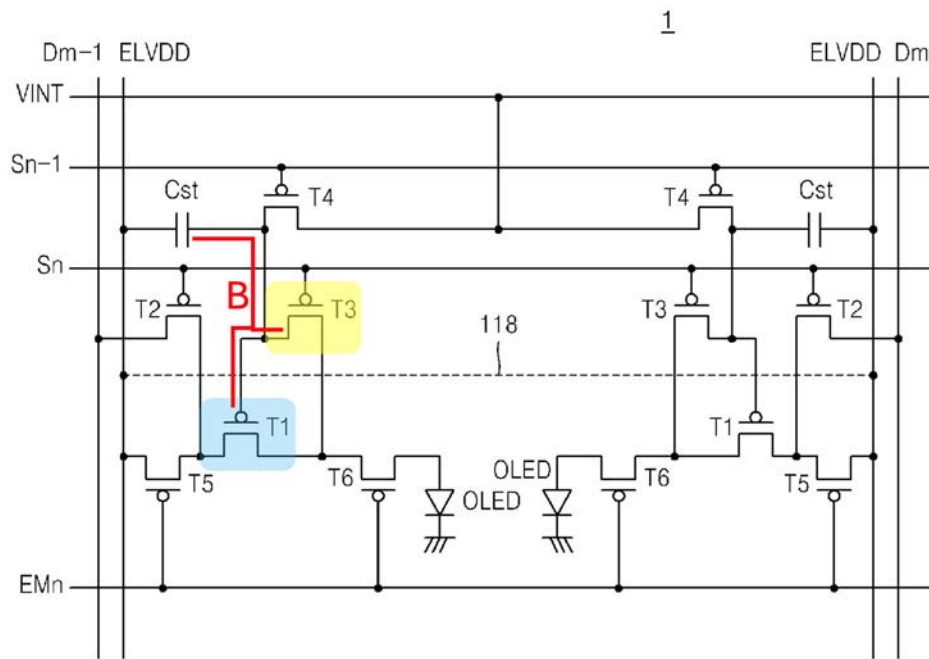


Fig. 3

Kim-584's Fig. 8 (annotated below) shows this connection through connection line 120 (yellow) connecting T3's semiconductor drain region ("other

end of the third semiconductor”) to first capacitor electrode 114-1 (“first electrode layer,” blue). Kim-584, ¶76: “connection line 120 connects the first capacitor electrodes 114-1 [and]...the compensation TFTs T3.”).

Kim-584’s “data signal lines DLm-1...[and] connection line 120...may be formed...on the same layer.” *Id.*, ¶77. Cok, ¶¶208-212.

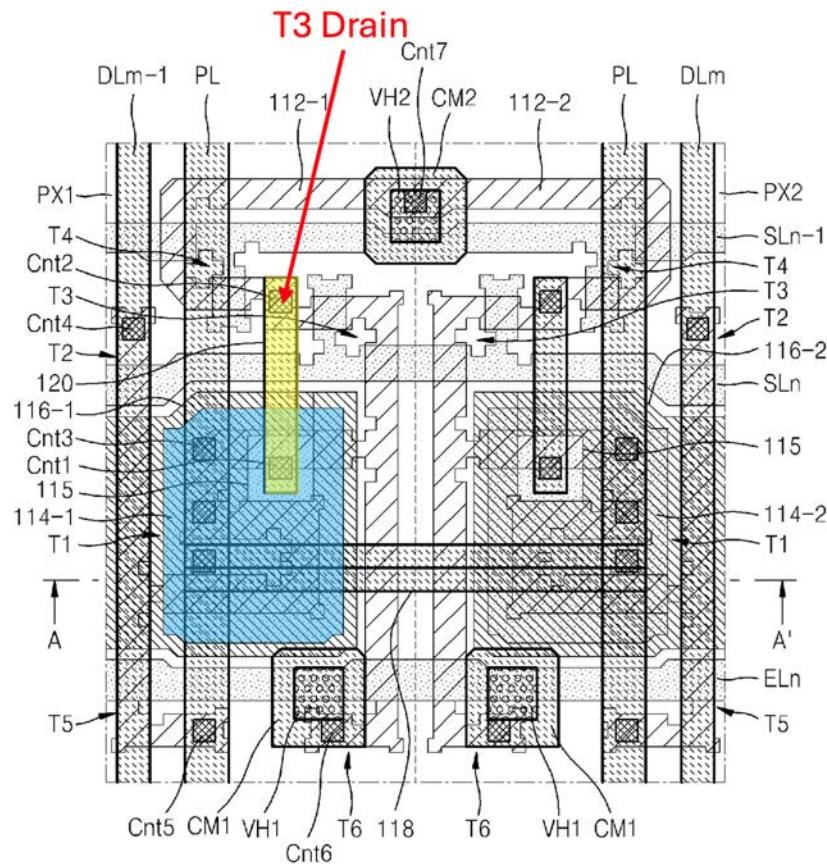


Fig. 8

8. Claim 28

a. 28[pre]-[b]:

See 1[pre]-1[b]. §IV.A.1.a-§IV.A.1.c.

b. 28[c]:

See 1[d]. §IV.A.1.e.

Kim-584's DLm-1 ("first signal line") is over both lower and upper capacitor electrodes 114-1 and 116-1 (first and second "electrode layers")—see Fig. 9 (annotated below).

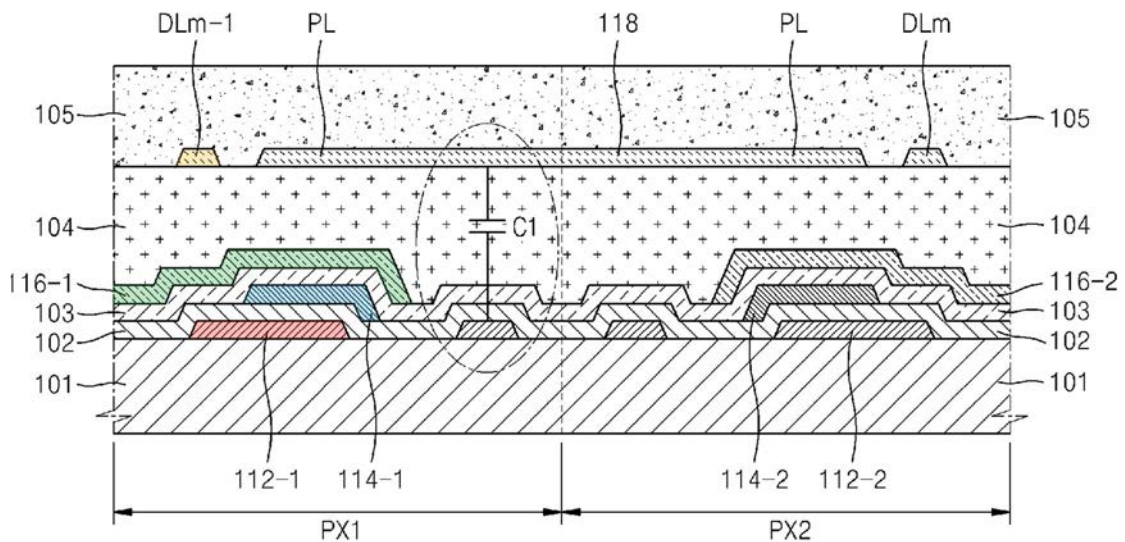


Fig. 9

c. 28[d]-[e]:

See 5[a]-5[b] (§IV.B.3.b-(§IV.B.3.c), with 28[d]'s "second" TFT/semiconductor treated as Claim 5's "third" TFT/semiconductor, and 28[e]'s "shield layer" treated as 5[b]'s "second shield layer."

Cok, ¶¶213-218.

9. Claim 29

a. 29[a]-[b]:

See 11[a]-11[b] (§IV.B.4.a-§IV.B.4.b), with Kim-584's T3 being the "second" TFT.

10. Claim 30

See Claim 12, with Kim-584's voltage line PL/ELVDD being the "voltage line," and top electrode of capacitor C2 being the "shield layer." §IV.B.5; Cok, ¶221.

11. Claim 31

This claim is rendered obvious by Kim-584-Han combination, with C2's top electrode being the "shield layer." *See also* 1[c] (§IV.A.1.d) and Claim 13 (§IV.B.6) regarding a second electrode layer over, and a part thereof overlapping, the first electrode layer, and the shield layer being part of the second electrode layer. Cok, ¶222.

12. Claim 32

See Claim 4. §IV.A.4.

C. Ground 2A: Kim-923 Renders Obvious Claims 1-4, 9-10, 20-23, 33.

Kim-923 describes an OLED display with a circuitry including TFTs to control operation of each OLED pixel. Kim-923, ¶¶3, 6, 60. Kim-923 addresses the problem of prior OLED displays having a narrow driving range for a gate voltage

applied to a driving TFT, which limits the number of gray levels that can be displayed. *Id.*, ¶¶ 7, 9, 40-41.

1. Claim 1

a. 1[pre]:

Kim-923 describes an OLED display apparatus. Kim-923 ¶3.

b. 1[a]:

Kim-923 discloses “a first” TFT as TFT T1, illustrated in Fig. 1 (annotated below).

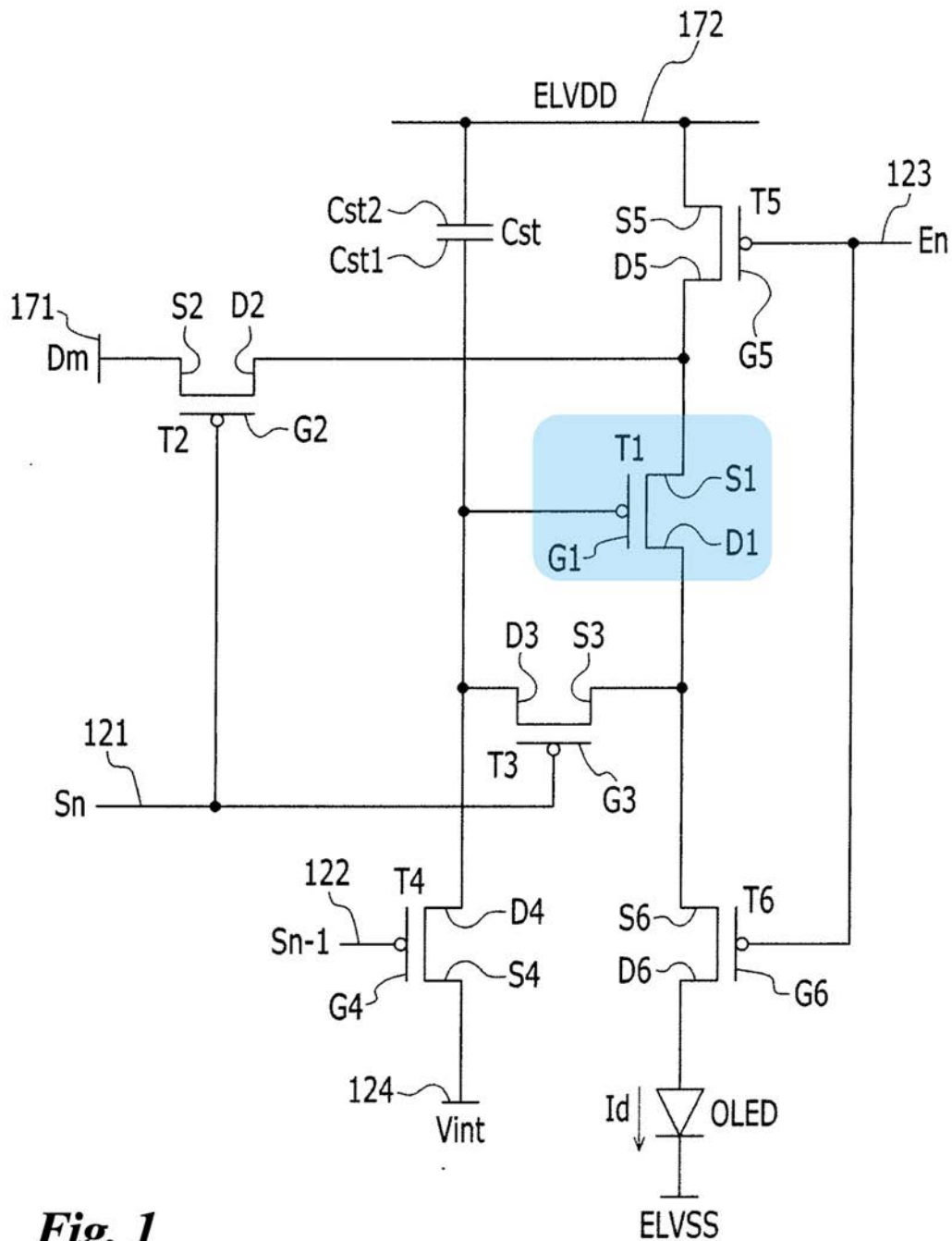


Fig. 1

Kim-923’s “**driving thin film transistor T1** [“first” TFT is]...**formed along the semiconductor layer 131**” (Kim-923, ¶79), which “**includes a channel region,** which is not doped with an impurity, and **a source region and a drain region**

formed at respective sides of the channel region to be doped with the impurity.”

Id. T1’s semiconductor is labeled 131a. *Id.* ¶¶79, 85; and *id.*, Fig. 3 (below).

c. 1[b]:

Kim-923 discloses “a first electrode layer” as a layer that includes a “**driving gate electrode 125a** [that]...**overlaps the driving channel region 131a1 of the driving semiconductor layer 131a.**” Kim-923, ¶106, Fig. 3 (annotated below), showing driving gate electrode 125a (blue) overlaying T1’s channel 131a1 (red).

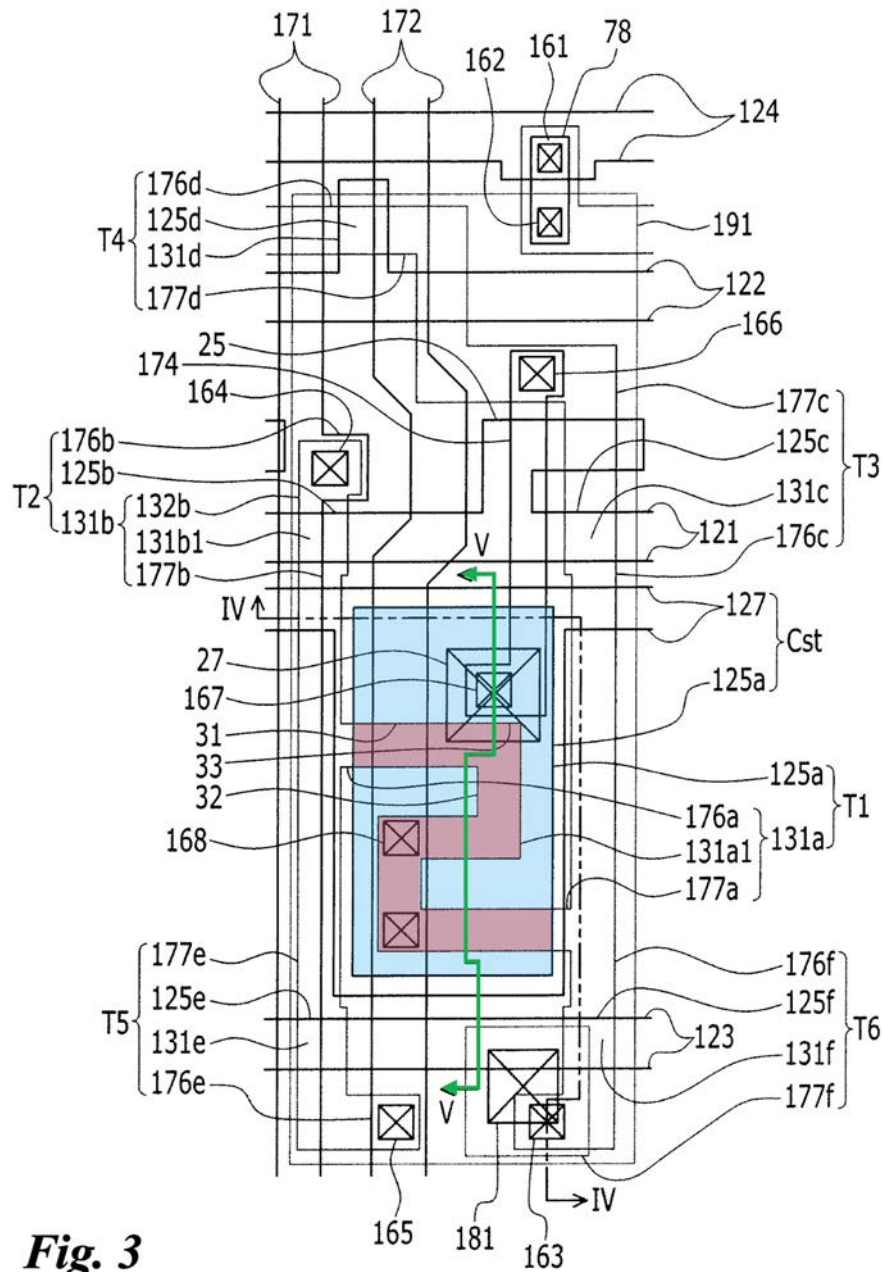


Fig. 3

Fig. 5 (cross-section along Fig. 3's line V-V) shows element 125h, rather than 125a. However, Kim-923's 125h and 125a are the same element: "driving gate electrode 125a also plays a role of the first storage capacitor plate 125h." Kim-923, ¶86. As illustrated, first storage capacitor plate 125h/driving gate electrode 125a is

in a layer above/over driving channel region 131a1 (“channel area of the first semiconductor”).

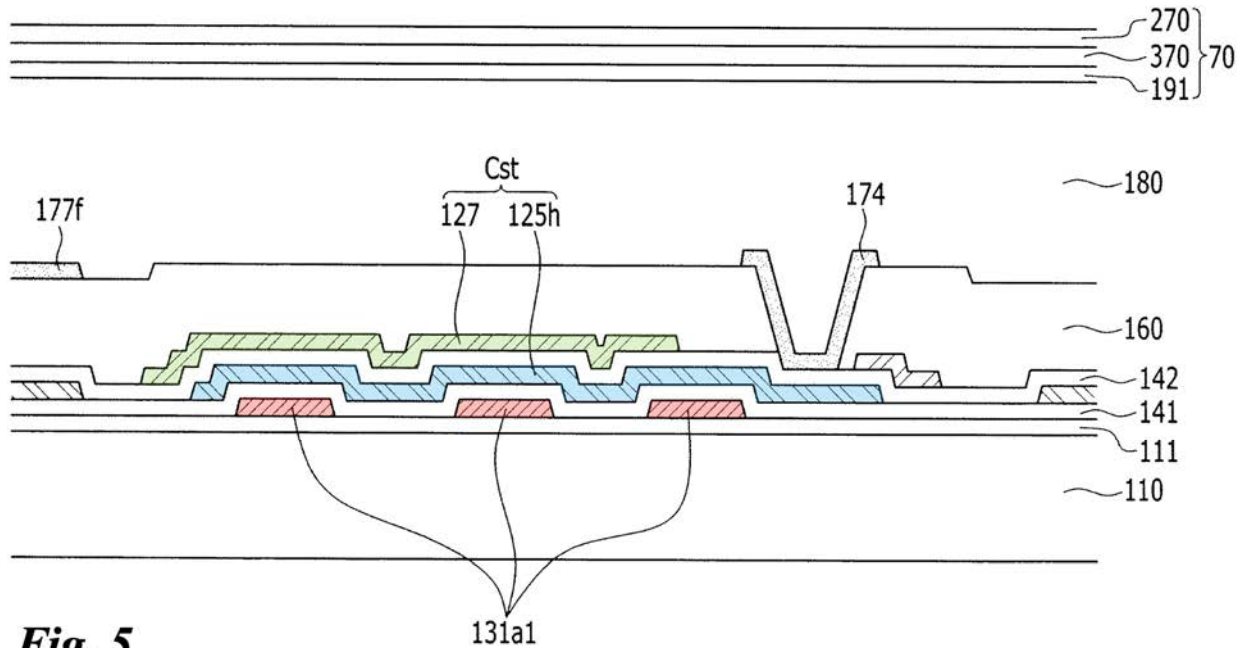


Fig. 5

d. 1[c]:

As annotated Fig. 5 (above) illustrates, Kim-923 discloses “a second electrode layer” as a layer that includes second storage capacitor plate 127 (green) positioned over (and overlapping) the electrode layer that includes driving gate electrode 125a/h (“first electrode layer,” blue). Annotated Fig. 3 (below) also illustrates second storage capacitor plate 127 (“second electrode layer,” green) overlapping driving gate electrode/first capacitor plate 125a/125h (“first electrode layer,” blue), as explicitly described by Kim-923 in ¶109. *See also id.*, Fig. 8, element 127.

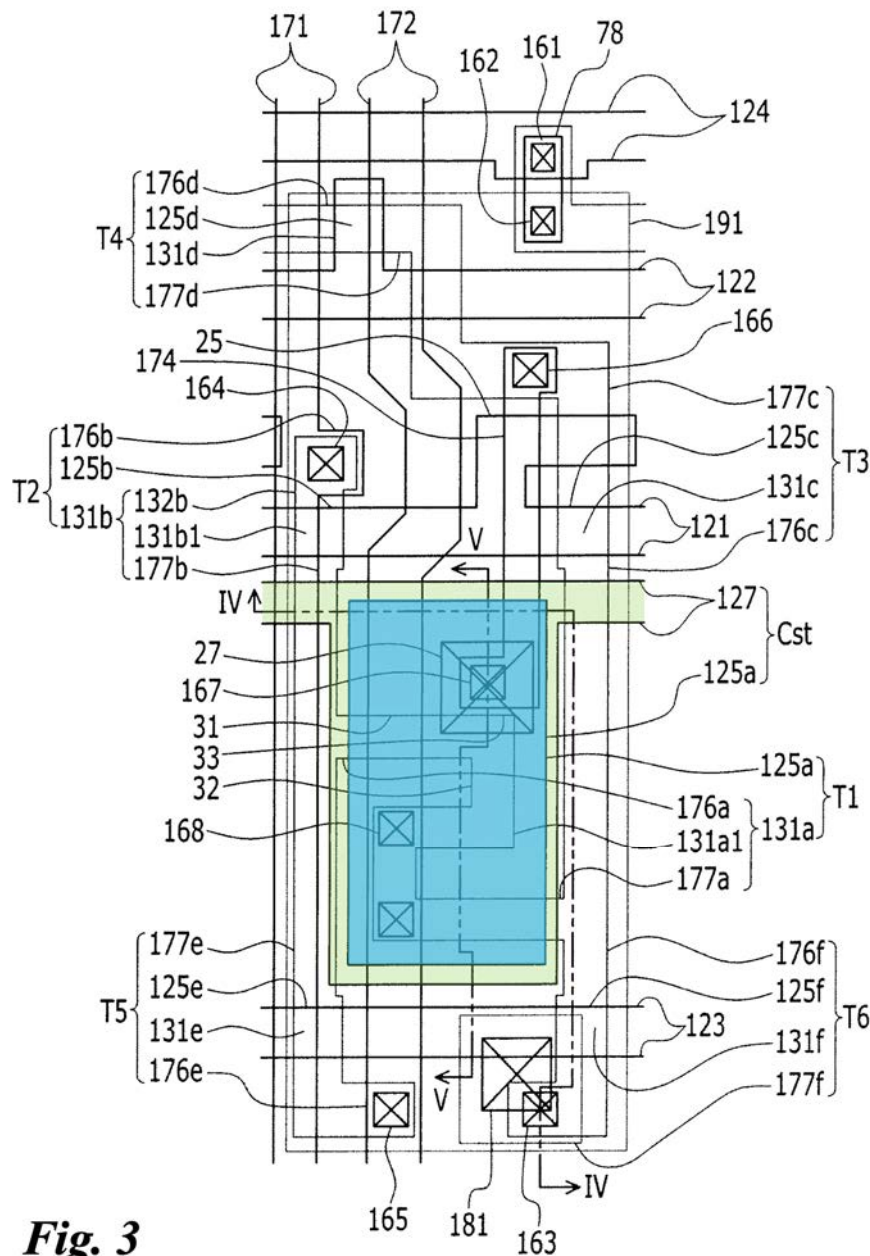


Fig. 3

e. 1[d]:

Kim-923 discloses a “first signal line” as data line 171. Kim-923, ¶62.

Kim-923’s Fig. 4 (annotated below) shows data line 171 “over” the second electrode layer (electrode layer containing second storage capacitor plate 127).

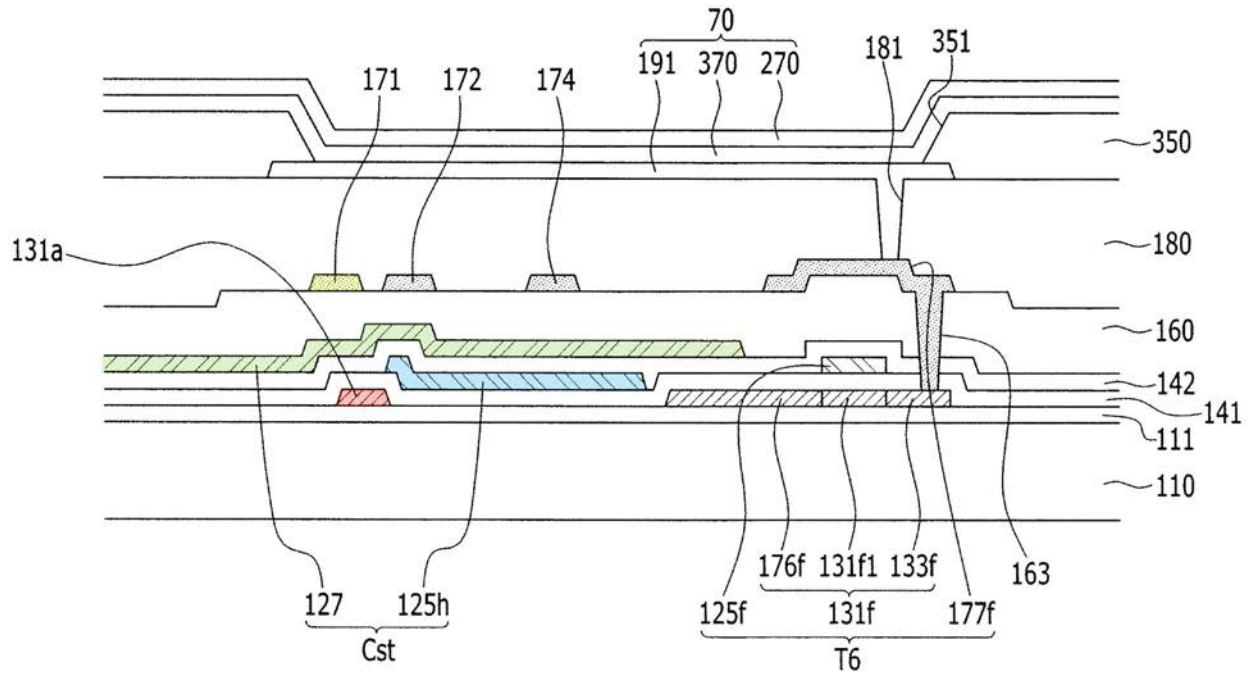


Fig. 4

f. 1[e]:

Kim-923 teaches or suggests “a first shield layer” as second storage capacitor plate 127, or a part thereof, positioned in a layer between data line 171 (“first signal line”) and “first semiconductor” 131a. Kim-923, Fig. 4 (annotated below).

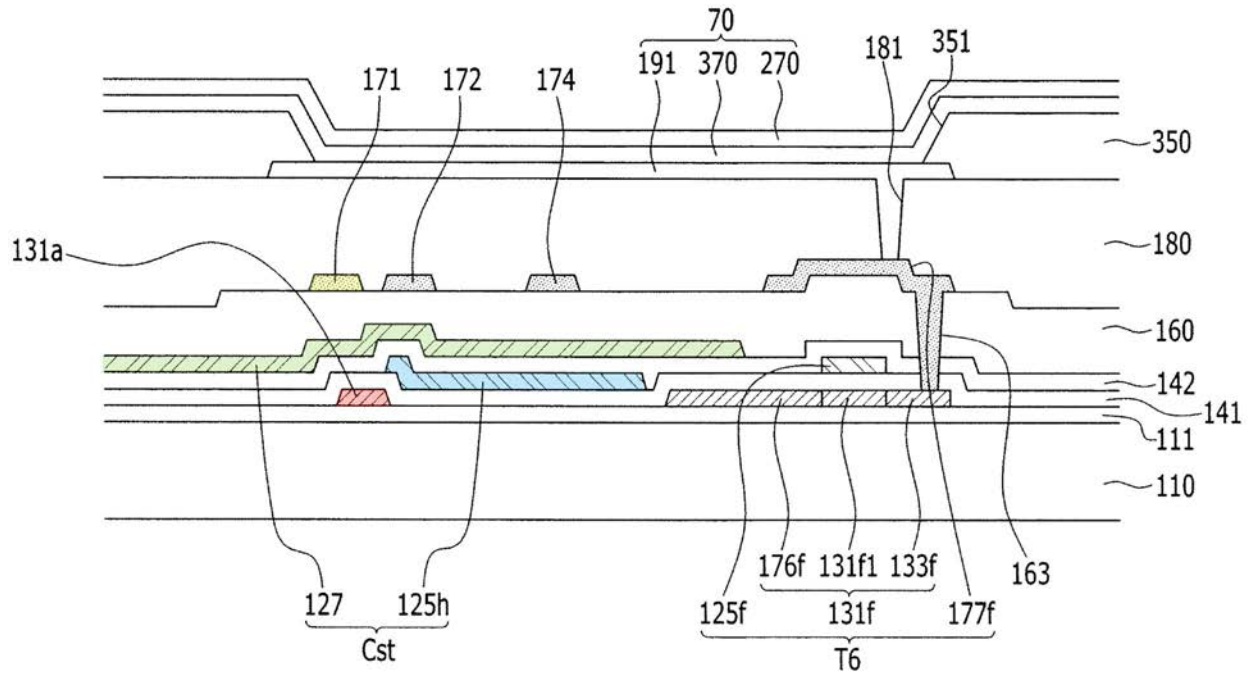


Fig. 4

Annotated Fig. 3 (below) shows “a part of one of the source area and the drain area of the first semiconductor” in purple color, which is overlapped by second storage capacitor plate 127 (“first shield layer”).¹² T1’s channel region (131a1) is under T1’s gate 125a, and parts of T1’s “first semiconductor” 131a that are not overlapped by gate electrode 125a comprise the source, on one end, and the drain, on the other end of the channel region. Kim-923, ¶¶79-80.

¹² Purple annotation only illustrates a portion of the overlapped source region. See Claim 8.

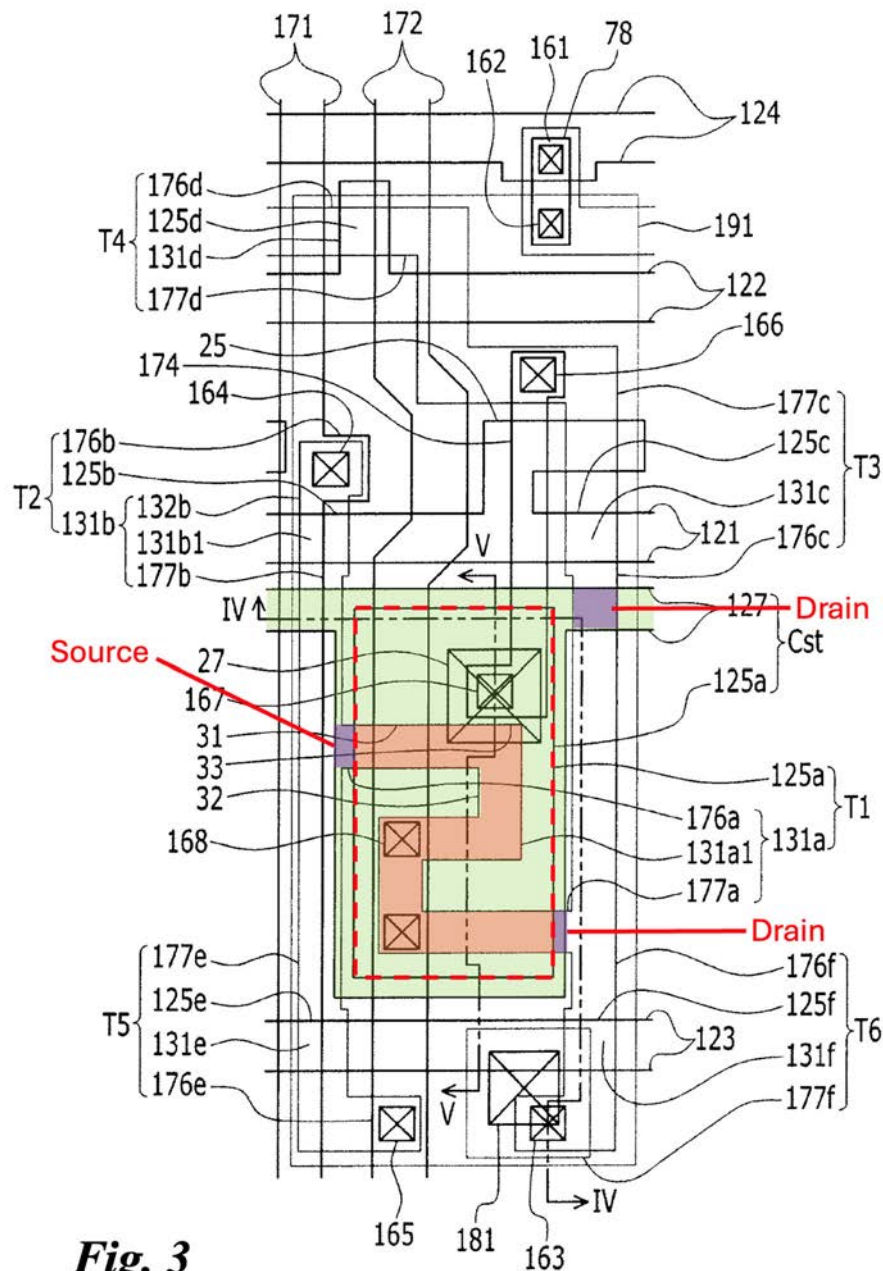


Fig. 3

Alternatively, Kim-923 shows the “first shield layer” as a larger capacitor plate 127 in Fig. 8 embodiment (annotated below), overlapping “a” part of source/drain area of the first semiconductor (purple). Kim-923, ¶129, Fig. 8. Either embodiment in Fig. 3 or 8 renders 1[e] obvious.

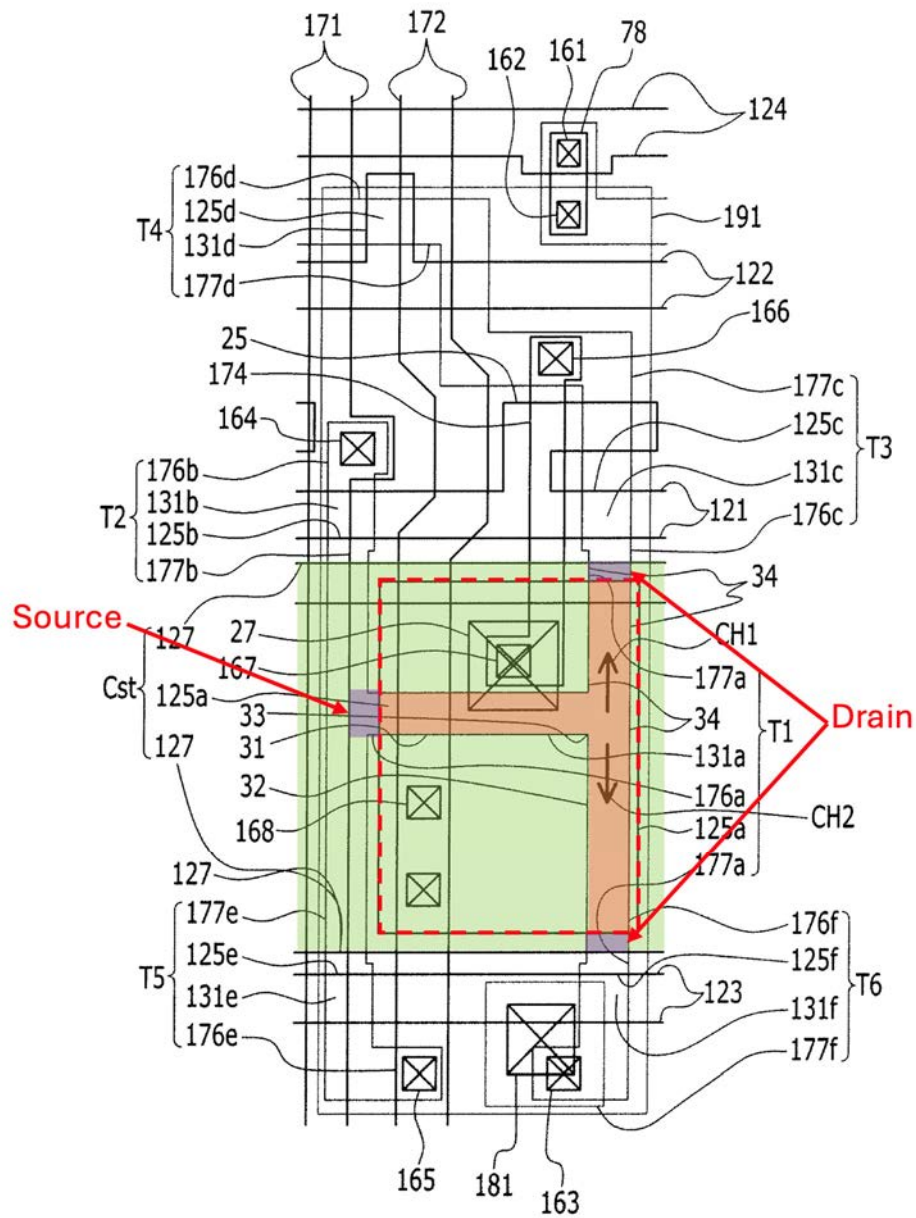


Fig. 8

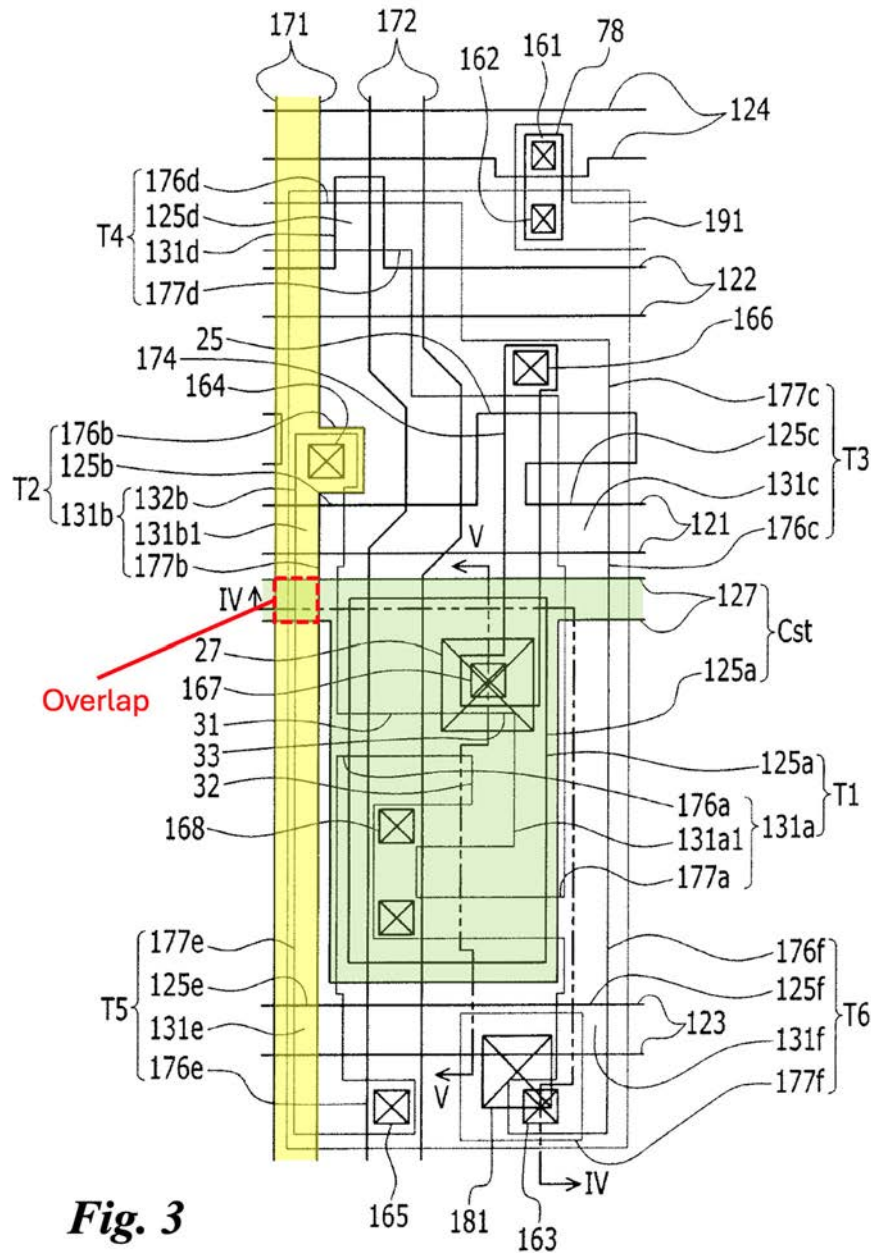
POSITAs would have found it obvious that Kim-923's top capacitor plate 127 (or a part thereof) (in either Fig. 3 or 8 embodiment) is a shield because it was a conductor disposed in a layer above T1 (above driving semiconductor layer 131a), was connected to a constant voltage source ELVDD (see Fig. 2), and would thus

shield T1 from the electromagnetic interference/noise of the signal lines disposed in upper layers for the same reasons discussed in §IV.A.1.f.

See also Cok, ¶¶225-250.

2. Claim 2

Kim-923 explains second capacitor plate 127 (“first shield layer”) is part of a “second electrode layer” because it is in a layer distinct from the first capacitor plate 125a, and includes other metal components, such as voltage lines. Kim-923, ¶88. Further, Fig. 3 (annotated below) shows second storage capacitor plate 127 overlaps part of signal line 171 (“first signal line”). Cok, ¶¶251-254.



3. Claim 3

Kim-923 discloses “a second” TFT as TFT T2 (Kim-923, ¶60, Fig. 1), including a second semiconductor (131b). *Id.*, ¶¶79, 90. Fig. 1 (annotated) below shows, and Kim-923 explicitly describes, T2’s drain (“one end of second

semiconductor”) connected (red) to T1’s source (“one end of the first semiconductor”), and T2’s source (“other end of second semiconductor”) connected (green) to signal line 171 (Dm) (“first signal line”). Kim-923, ¶64, Fig. 1.

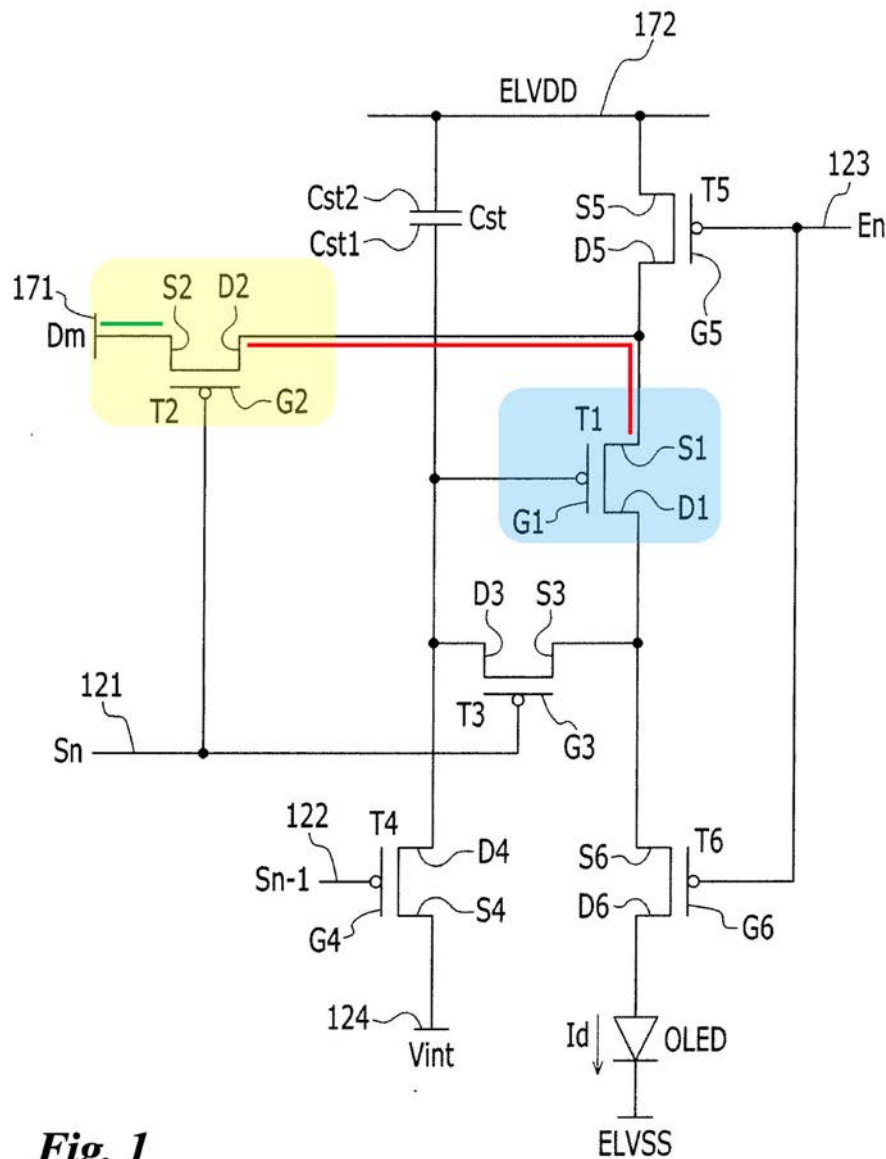


Fig. 1

Kim-923 explains each TFT is formed along a portion of semiconductor 131 (131b for T2) and includes source/drain electrodes formed as doped regions of the

semiconductor. Kim-923 ¶¶79, 85. Therefore, the Fig. 1 connectivity of source/drain of each TFT is through the doped region of semiconductor 131 forming that drain/source electrode. *Id.* Fig. 3 (annotated below) also illustrates connection of T2's drain (177b) to T1's source through the semiconductor layer (red), and connection of T2's source (176b) to signal line 171 through connection member 174. Kim-923, ¶90; Cok, ¶¶255-260.

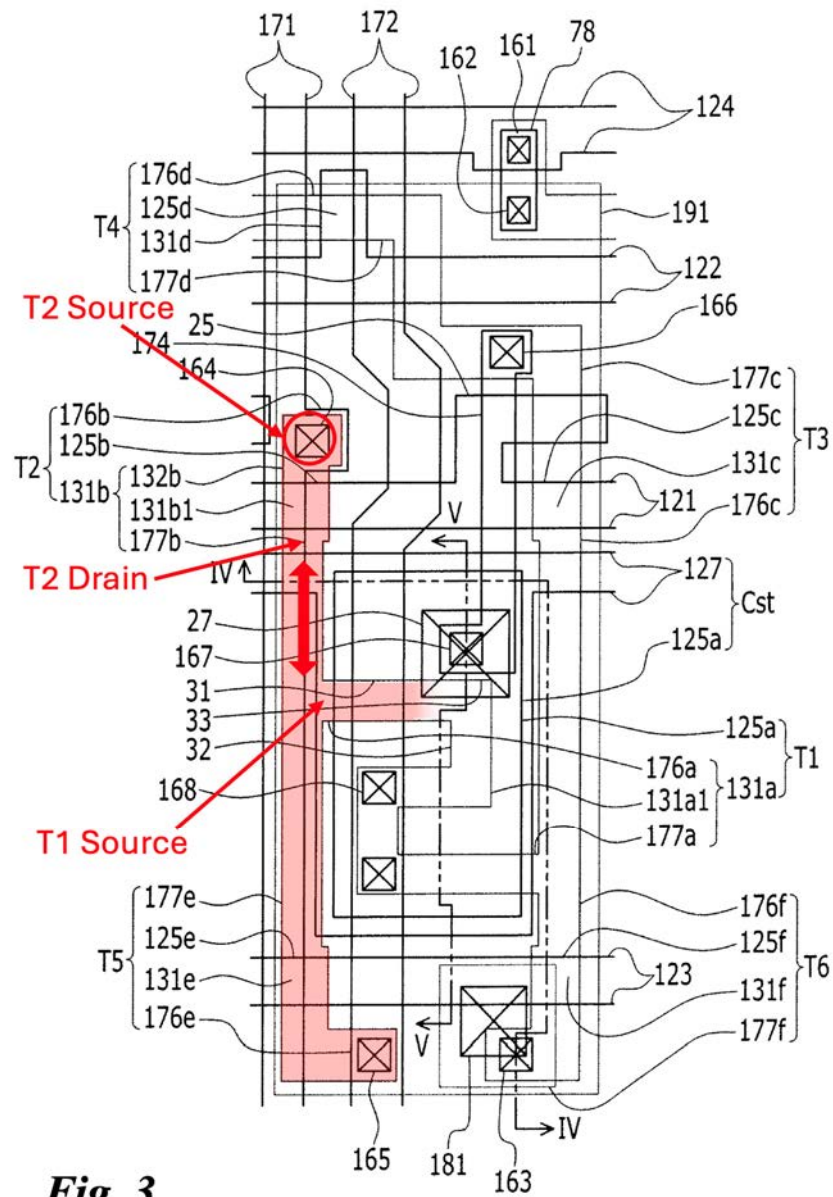


Fig. 3

4. Claim 4

Kim-923's voltage line 172 is "a first voltage line" in the same layer as data line 171. Kim-923, ¶1111, Fig. 4 (annotated below), showing 171 and 172 in the same layer.

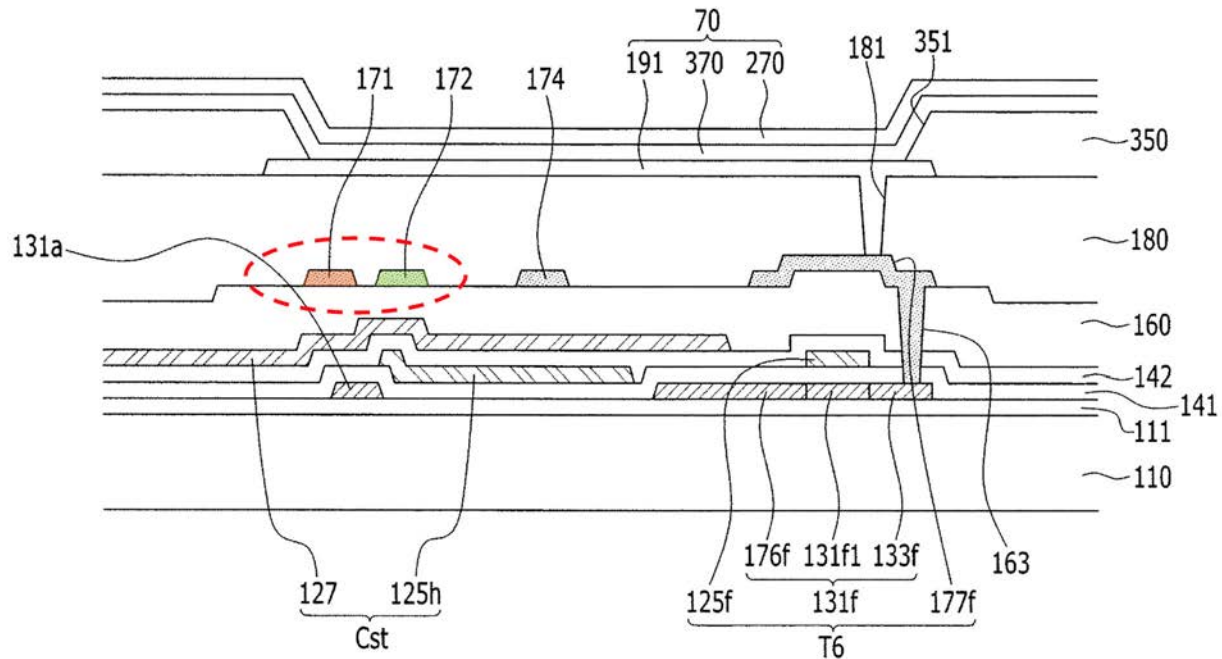


Fig. 4

Kim-923's voltage line 172 ("first voltage line) is connected to second capacitor plate 127 (Cst2) ("second electrode layer"): "[a]nother end **Cst2 of the storage capacitor Cst is coupled to the driving voltage line 172.**" Kim-923, ¶¶69, 86; §IV.C.1.d; Cok, ¶¶261-264.

5. Claim 8

a. 8[pre]:

Fig. 3 (annotated below) shows data line 171 ("first signal line") extends in a first direction.

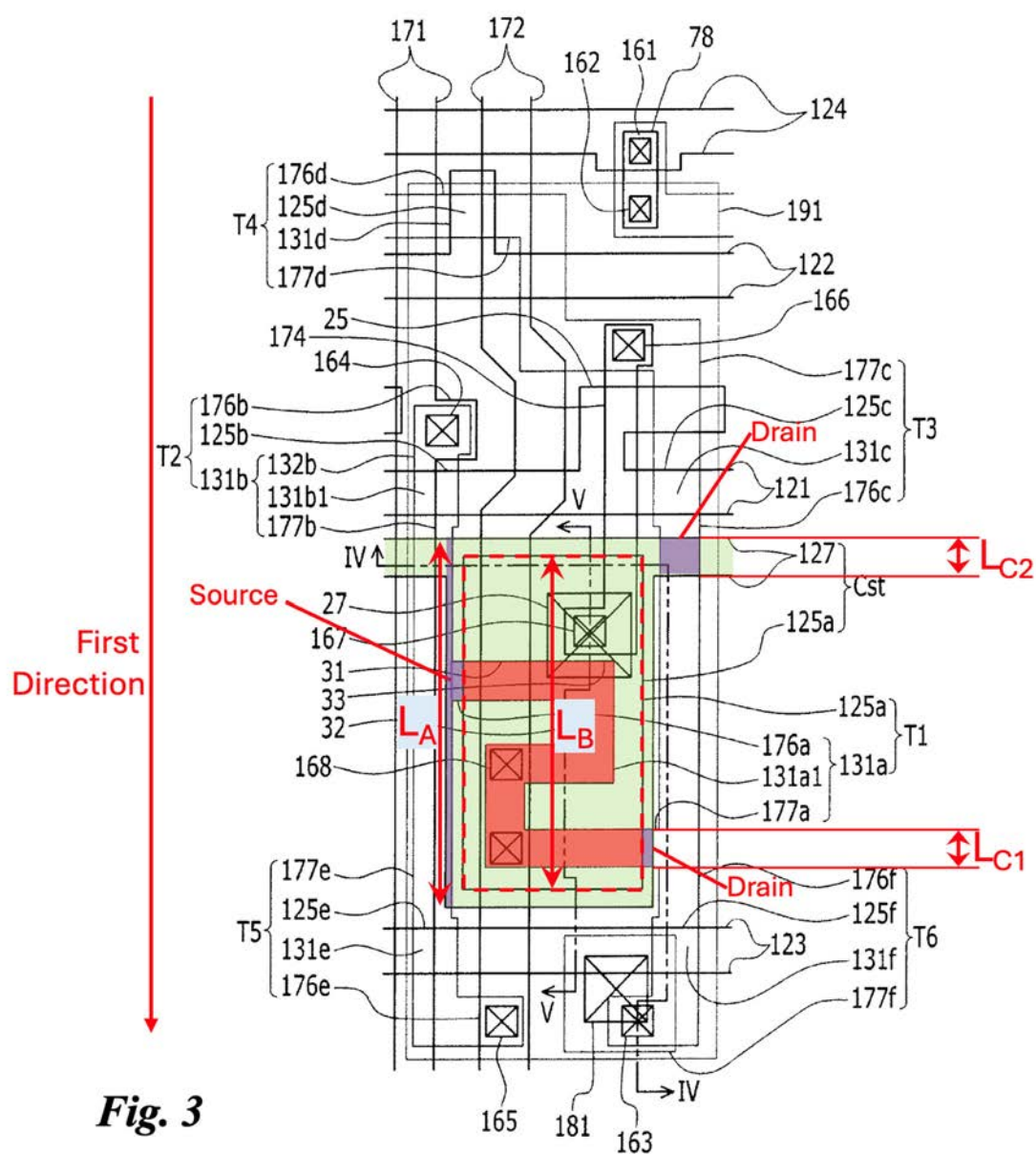
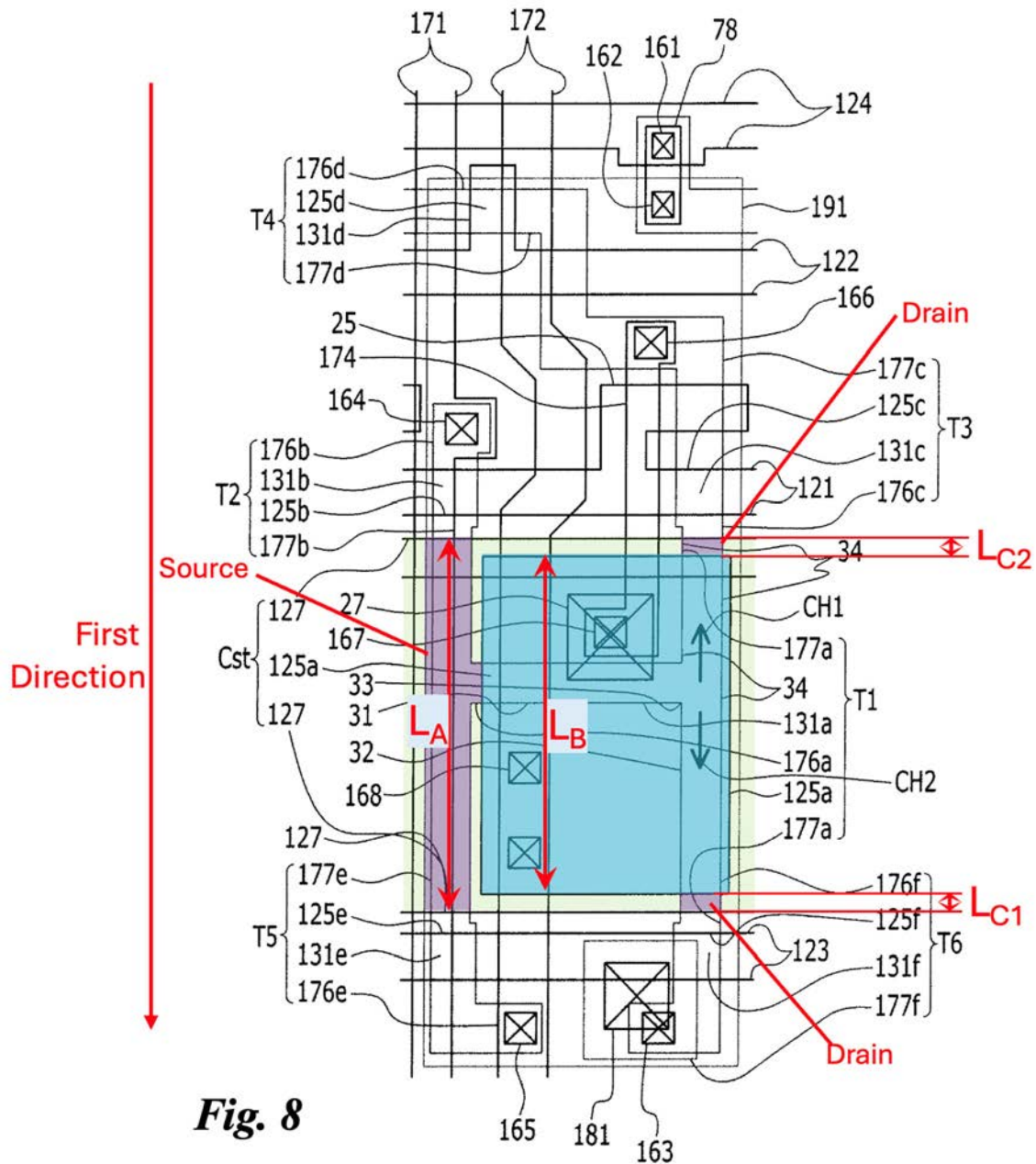


Fig. 3

Fig. 8's embodiment (annotated below, having a larger top capacitor plate 127) also shows data line 171 extending in first direction. Claim 8 is obvious under either embodiment.



b. 8[a]:

Figs. 3 and 8 (above) illustrate second storage capacitor plate 127 (“first shield layer,” green) overlaps T1’s source area along a length L_A , and T1’s drain area along a length L_{C1} and a length L_{C2} . Notably, L_A is larger than L_B , which is a length of one

side of the bottom capacitor plate (“a length of the first electrode layer”) along the first direction.

POSITAs would have found it obvious that T1’s source region would extend along the purple area of annotated Figs. 3 and 8 (above) between T1, T2 and T5 (see annotated Fig. 1 below) for the same reasons discussed in Ground 1A’s Claim 8. *See* §IV.A.5.b.¹³

¹³ In 1[e], annotated Fig. 3 shows a smaller portion of T1’s overlapped source area than Claim 8, but 1[e] is also rendered obvious by Claim 8’s extended overlapped source area.

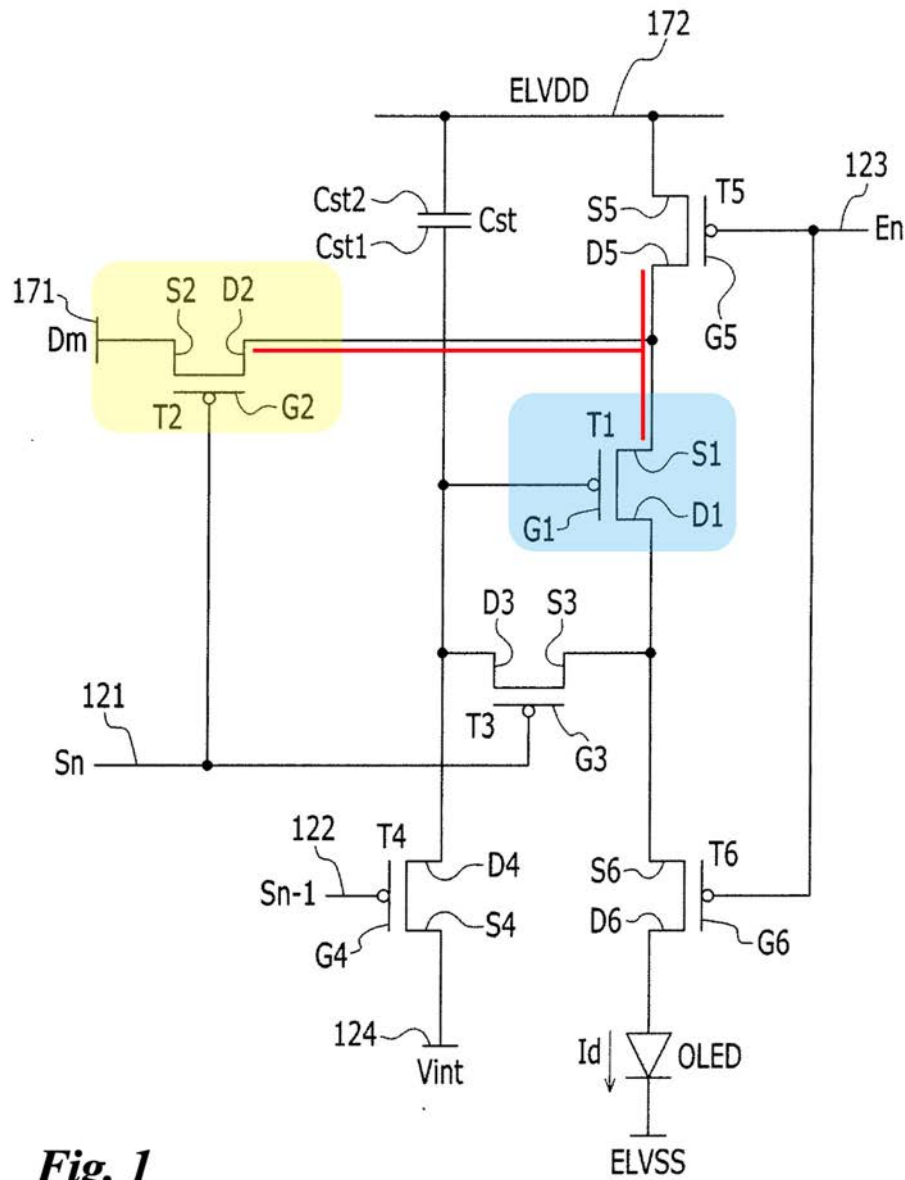


Fig. 1

Notably, Kim-923 explains undoped semiconductor regions are the channel regions, whereas drain/source electrodes are formed by doping the semiconductor. Kim-923, ¶¶79, 85, 94. Accordingly, the semiconductor areas outside of the undoped

channel regions associated with S1, D2 and D5 all have the same material and the same doping to maintain the same voltage. Cok, ¶¶265-274.

6. Claim 9

Either Fig. 3 or 8 (annotated below) discloses this limitation, showing second storage capacitor plate 127 (green) (“first shield layer”) extending beyond gate electrode 125a (red dashed box), fully overlapping “the part of one of the source area and the drain area of the first semiconductor” (purple-colored areas). See 1[e], *supra*. Cok, ¶¶275-277.

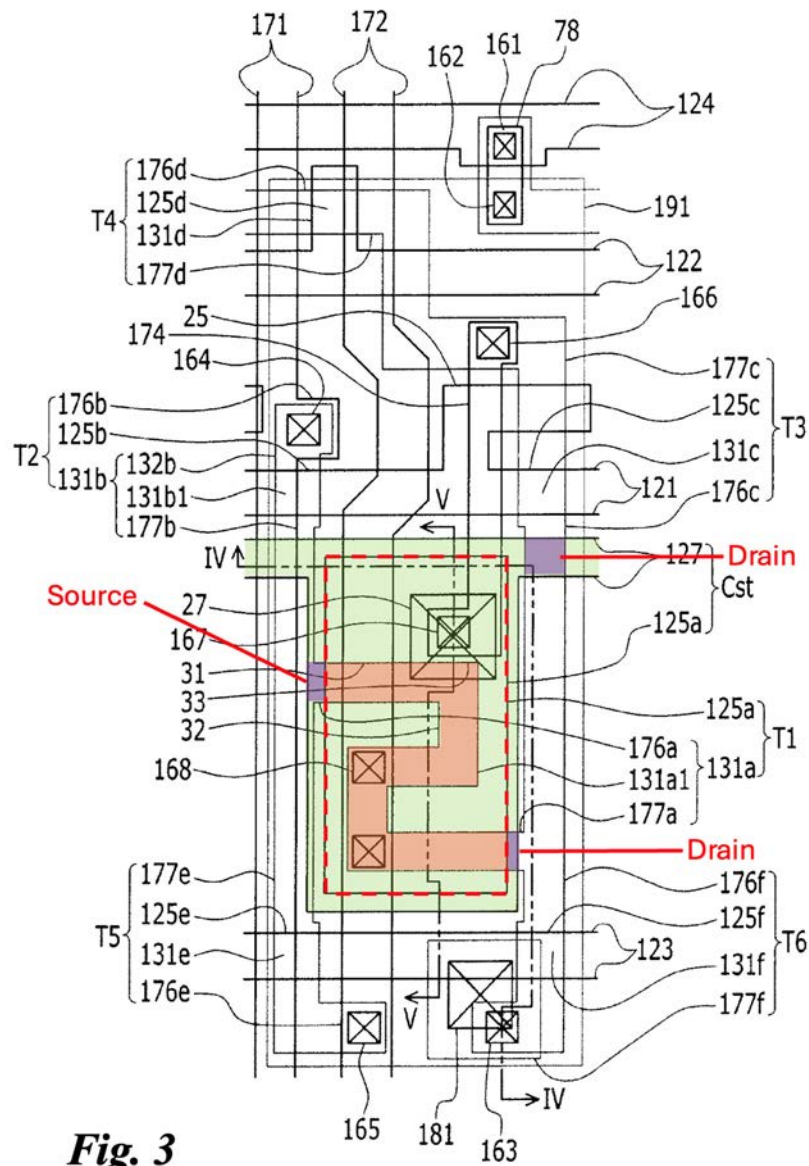


Fig. 3

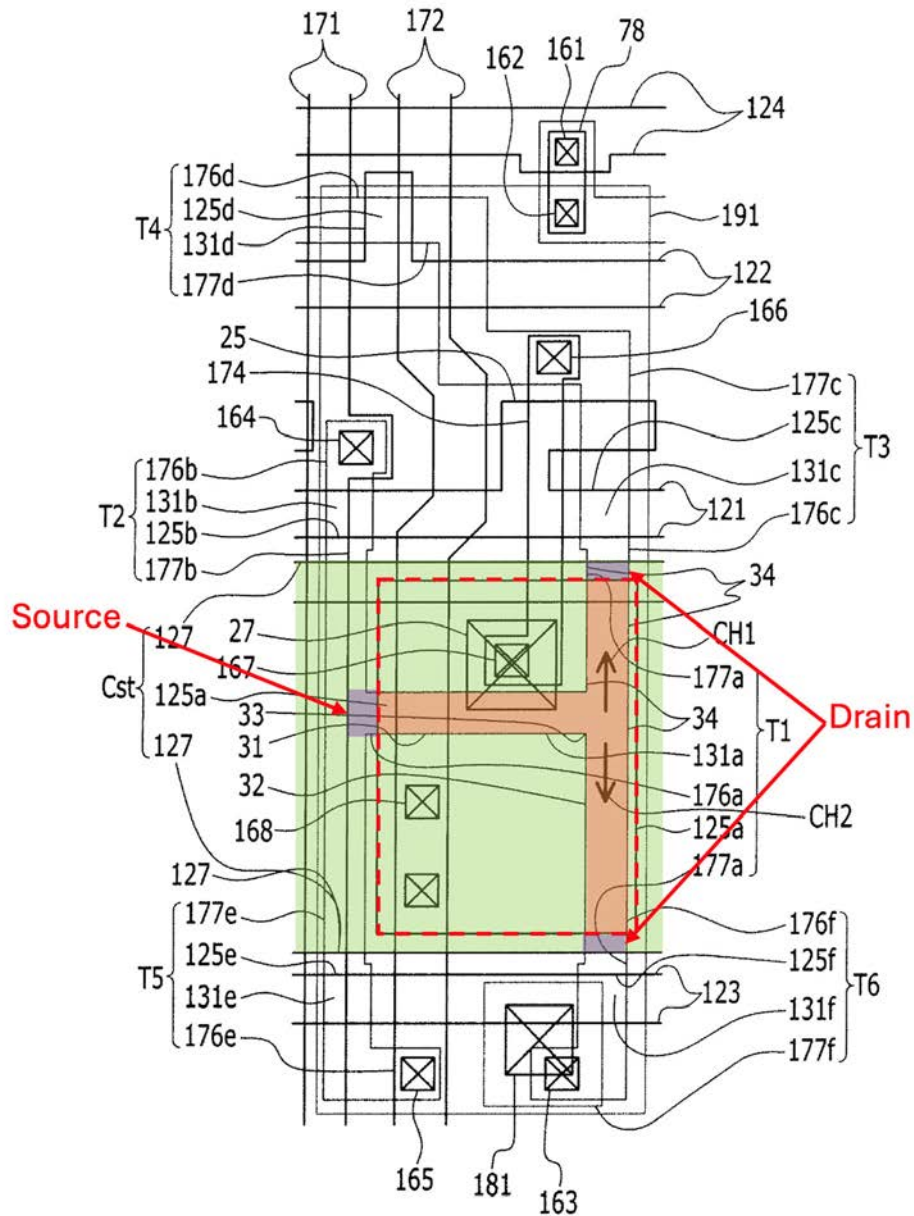


Fig. 8

7. Claim 10

a. 10[a]:

Kim-923's Fig. 8 embodiment renders this claim obvious, illustrating line 171 ("first signal line") extends in a first direction. Kim-923, Fig. 8 (annotated below).

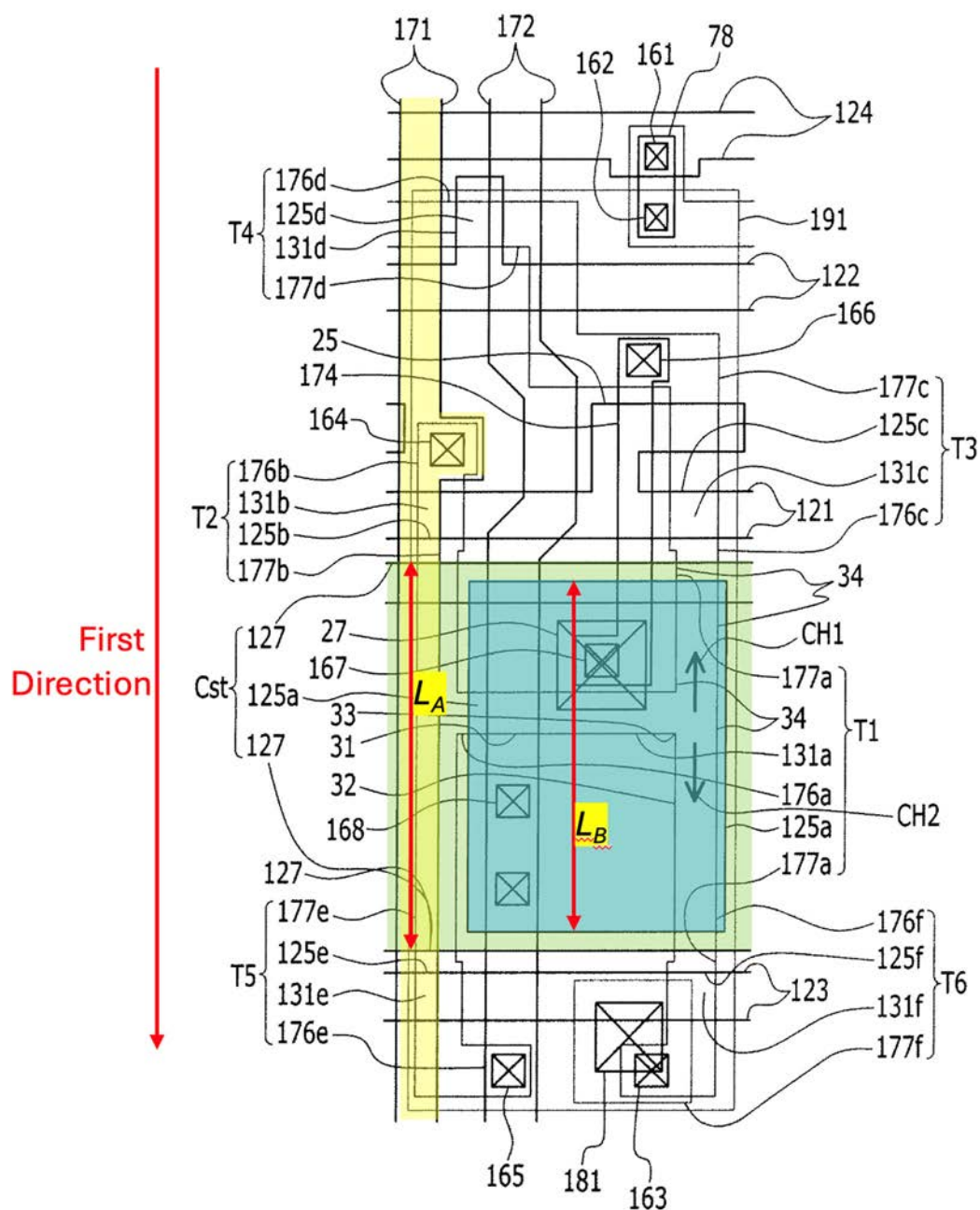


Fig. 8

b. 10[b]:

Fig. 8 (annotated above) discloses this limitation; a length, L_A , of the overlapped area of second storage capacitor plate 127 (“first shield layer”) with

driving voltage line 172 (“first signal line”), is longer than a length, L_B , of driving gate electrode 125a (“first electrode layer”) along the first direction. Kim-923, Fig. 3; Cok, ¶¶278-284.

8. Claim 20

a. 20[a]:

Kim-923 discloses “a fifth” TFT as T5. Kim-923, Fig. 1. As discussed in 1[a] and Claim 3, Kim-923 discloses a semiconductor for each of its transistors, including 131e for T5. §IV.C.1.b, §IV.C.3.

Fig. 1 (annotated below) shows, and Kim-923 describes, T5’s drain (“one end of the fifth semiconductor”) connected (line “A”) to T1’s source (“one end of the first semiconductor”), and also connected (line “B”) to T2’s drain (“one end of the second semiconductor”). Additionally, T5’s source (“other end of the fifth semiconductor”) is connected (line “C”) to driving voltage line 172 (“first voltage line”). Kim-923. ¶67.

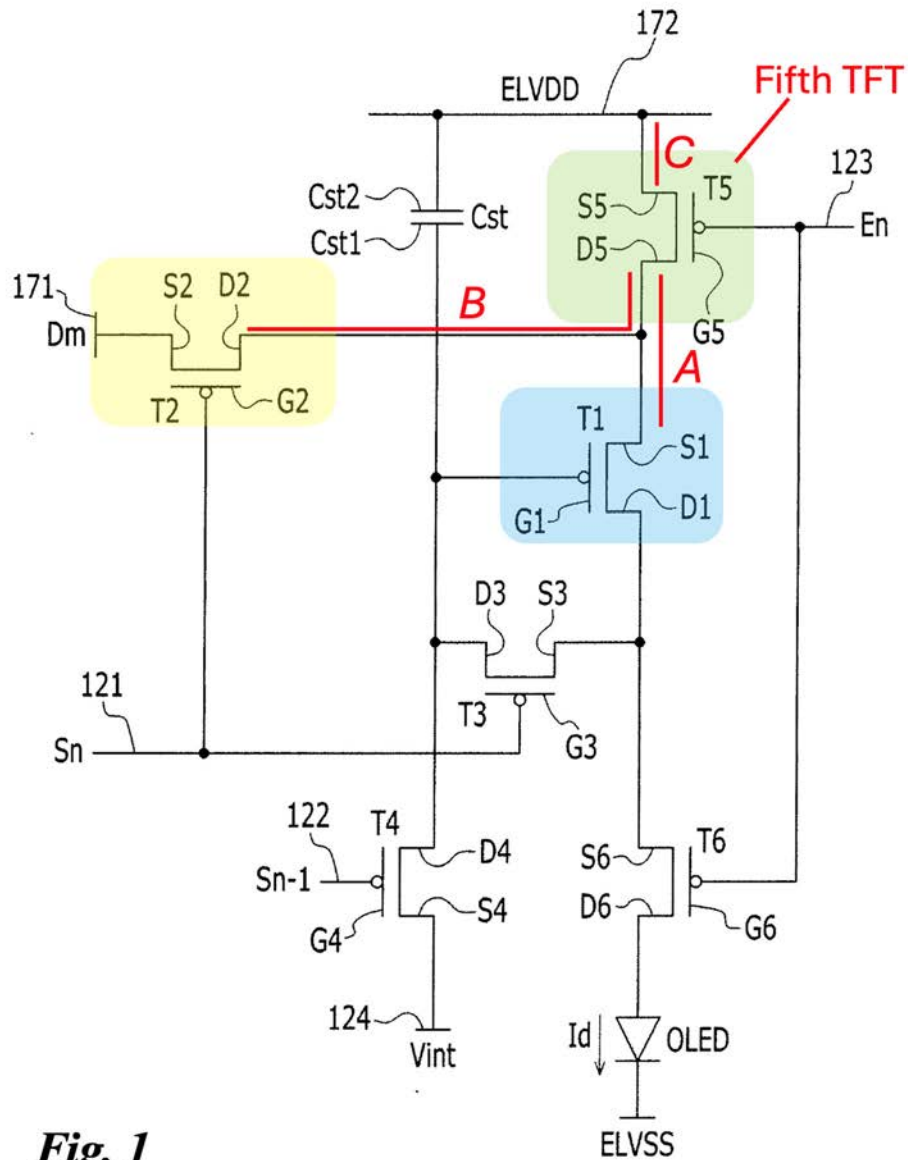
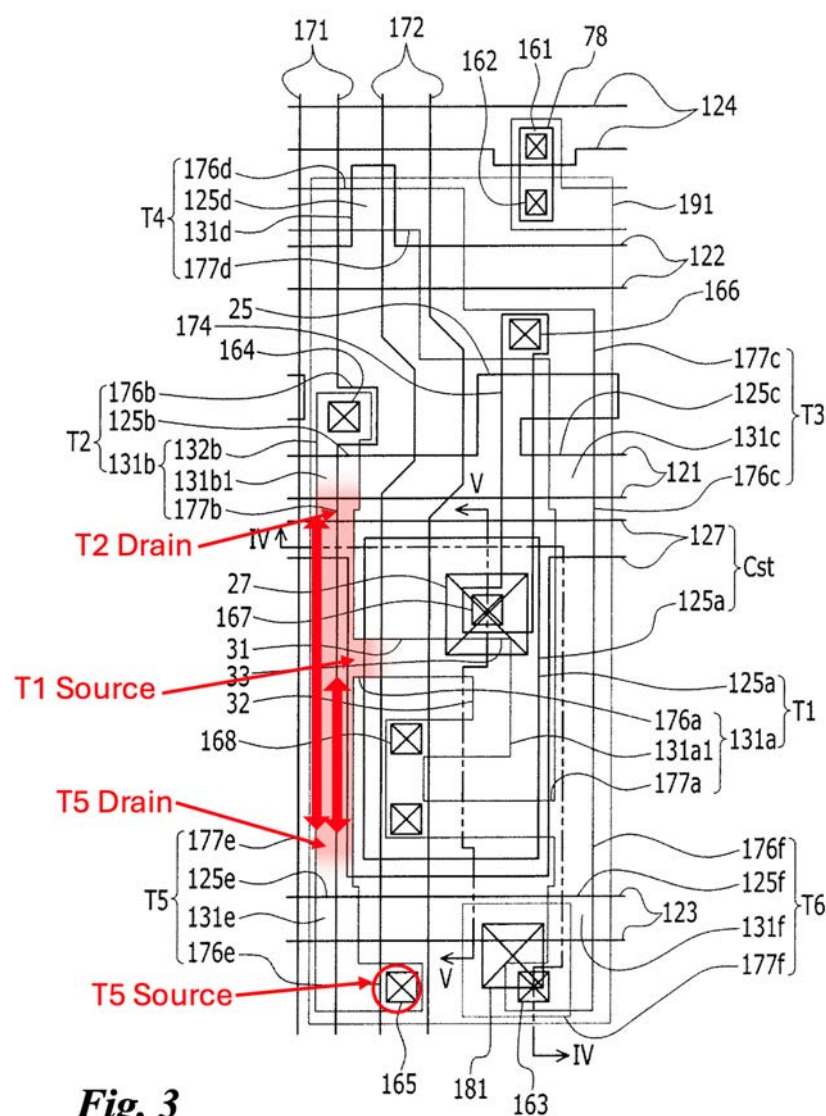


Fig. 3 (annotated below) also illustrates the semiconductor connectivity, showing T5's drain (177e) connected to T1's source (176a) and to T2's drain (177b); and T5's source (176e) connected to voltage line 172 through connector 165. *Id.*, ¶93.



b. 20[b]:

Annotated Fig. 4 (annotated below) shows voltage line 172 (“first voltage line”) is in the same layer as data line 171 (“first signal line”). Kim-923, ¶111.

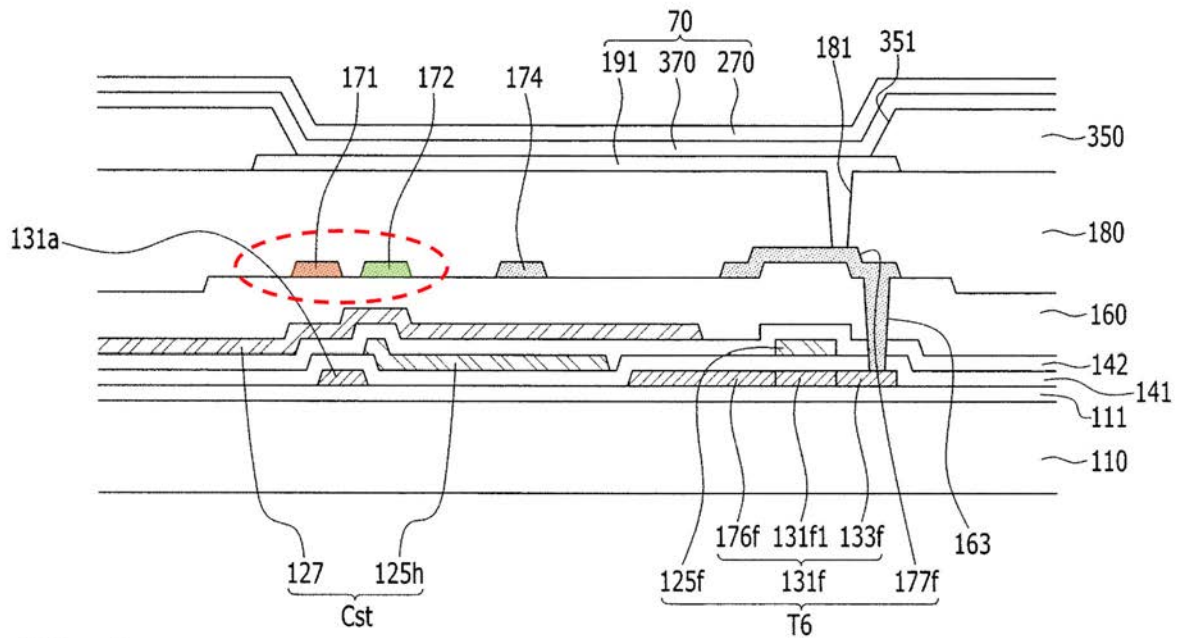


Fig. 4

Kim-923's voltage line 172 ("first voltage line") is "connected to the second electrode layer" because Fig. 1 shows line 172 is connected to second storage capacitor plate 127, labeled Cst2 in annotated FIG. 1, which is part of the second electrode layer.¹⁴ §IV.C.1.d; Cok, ¶¶285-296.

¹⁴ Cst2 is the same as second storage capacitor plate 127. Kim-923, ¶86.

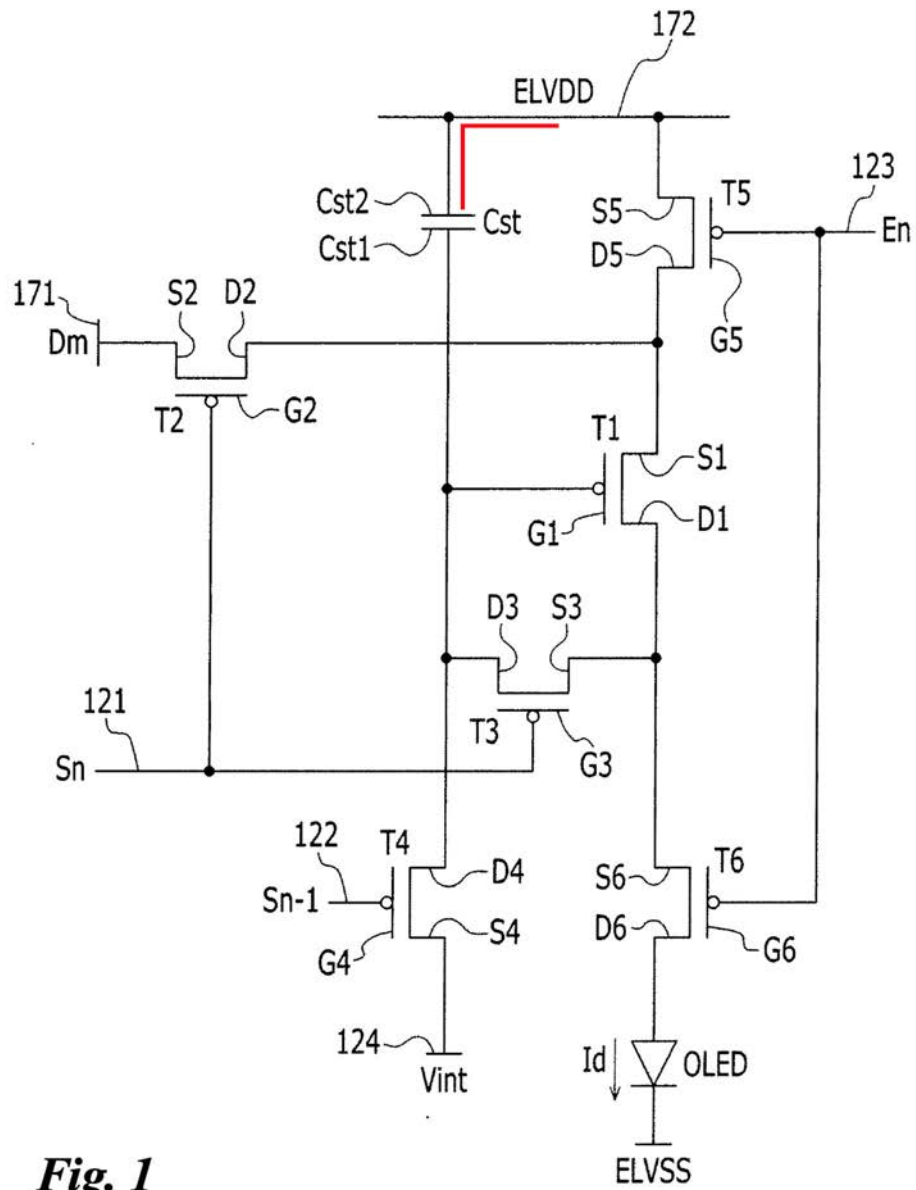


Fig. 1

9. Claim 21

a. 21[a]:

Kim-923 teaches or suggests a “fourth” shield layer as a portion of second storage capacitor plate 127, outlined below in red (or a portion thereof). Kim-923, Fig. 3. The “fourth” shield is in a layer between line 171 (“first signal line”) and T5’s semiconductor (part of semiconductor 131) because it is part of the second capacitor plate 127 with the same positioning over the semiconductor 131 and below 171. §IV.C.1.f.

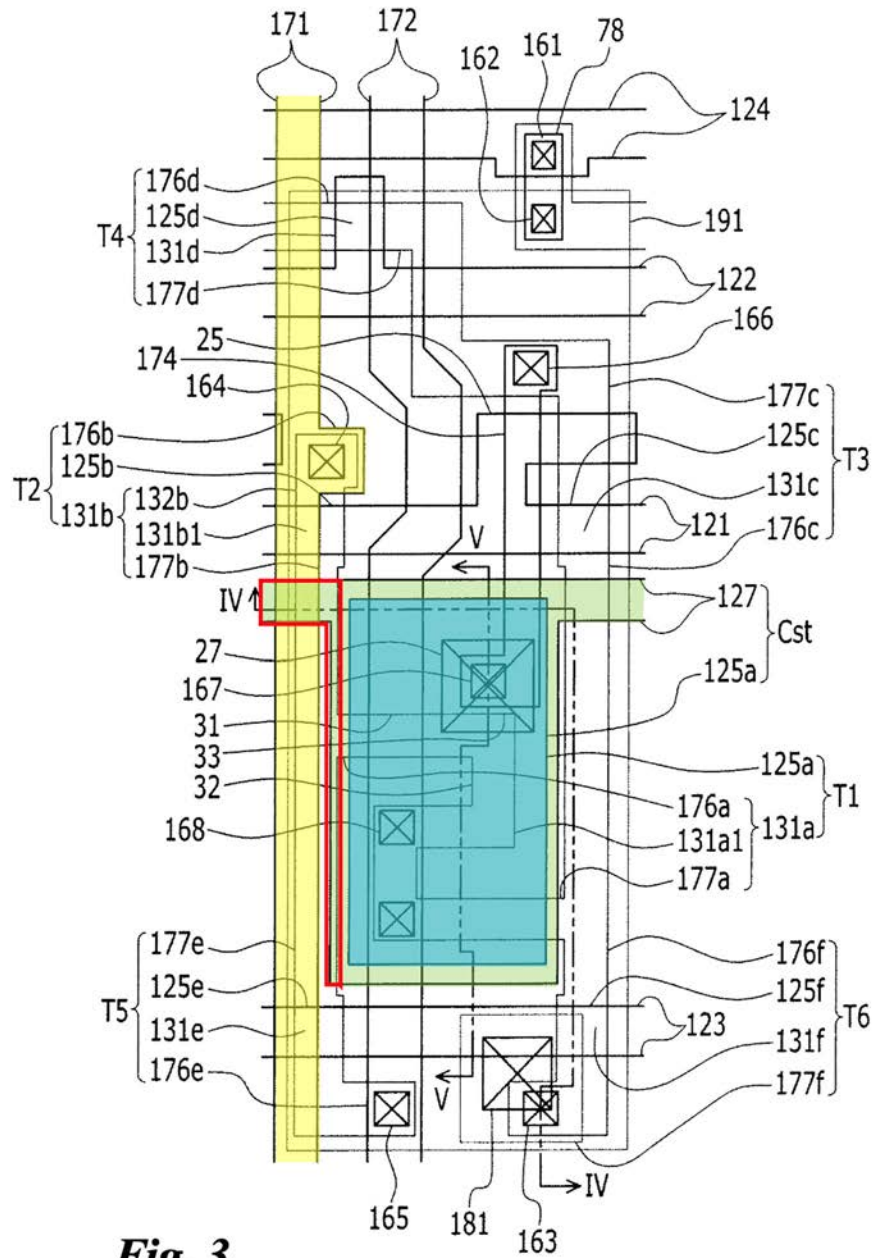


Fig. 3

Alternatively, Kim-923's teaches or suggests the "fourth shield layer" as part of second storage capacitor plate 127 of Fig. 8 embodiment, as outlined in red

rectangle below (or a portion thereof),¹⁵ relative vertical positioning of element 127 is the same as in Fig. 3. Kim-923, Fig. 8 embodiment. Cok, ¶¶297-301.

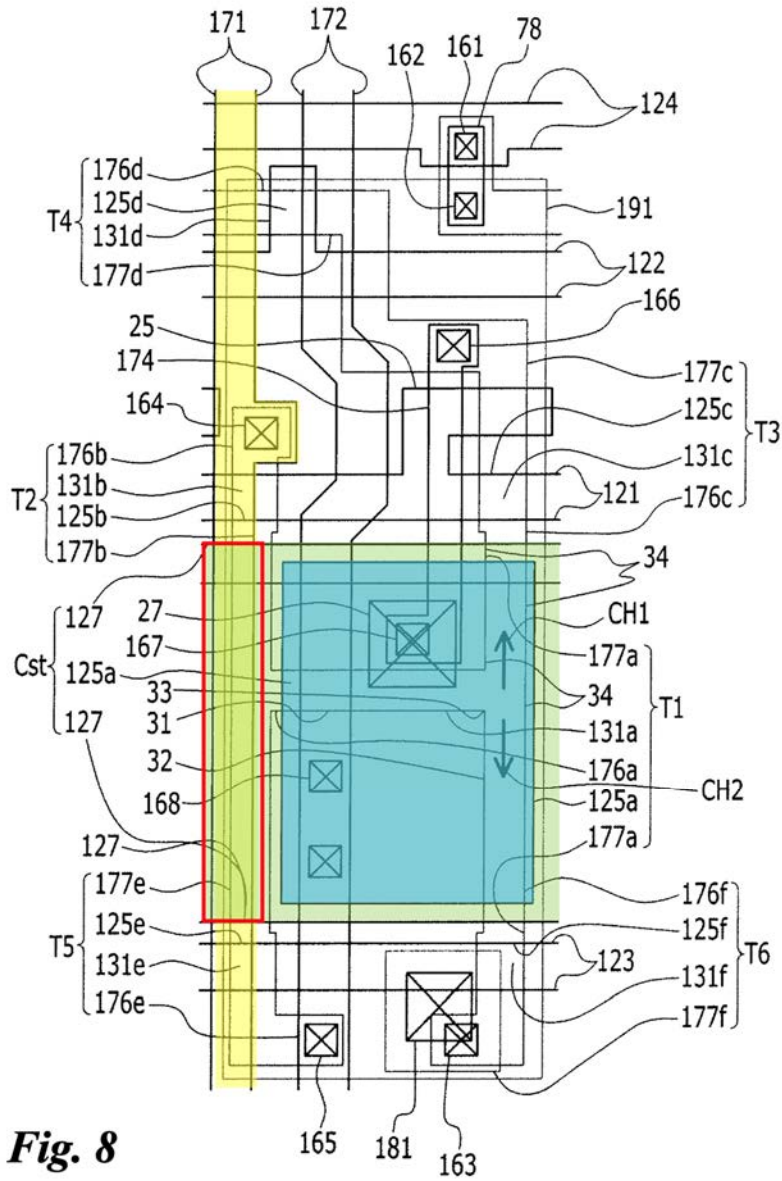


Fig. 8

¹⁵ The use of either Fig. 3 or Fig. 8 embodiment does not alter the analysis for Claims 21-23.

As discussed in Ground 1A, identifying a portion of a metal component as the shield layer is consistent with '015 patent. See §IV.A.9.a.

b. 21[b]:

Kim-923 teaches or suggests this limitation because the red rectangle in annotated Figs. 3 and 8 (“fourth shield layer”) overlaps the semiconductor region between T1’s gate, which overlaps “channel area of first semiconductor”, T2’s gate, which overlaps “channel area of second semiconductor,” and T5’s gate, which overlaps “channel area of fifth semiconductor.” The overlapped region is illustrated below in red in left panels’ partial reproduction of Figs. 3 and 8. Cok, ¶¶302-304.

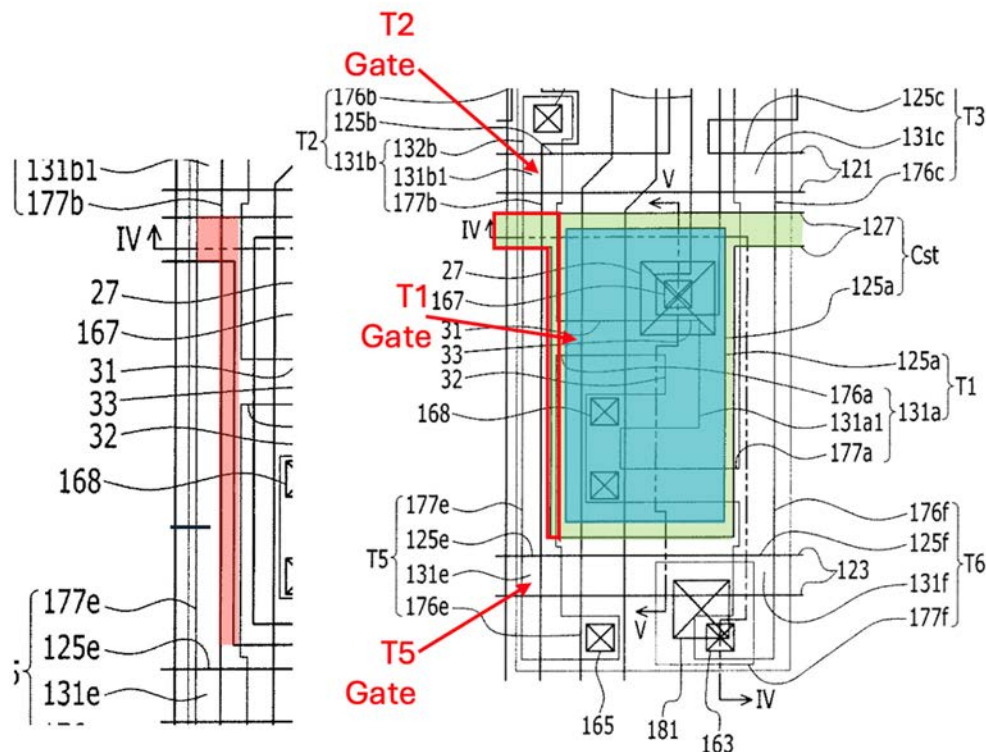


Fig. 3 (Annotated, Partial)

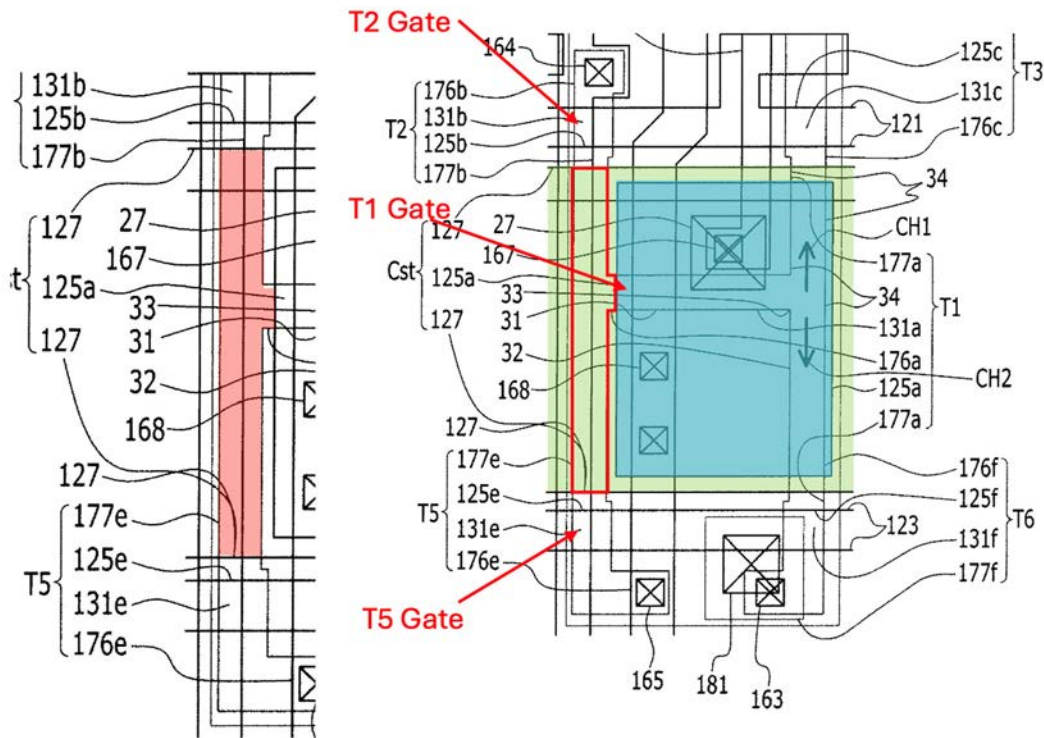


Fig. 8 (Annotated, Partial)

10. Claim 22

Kim-923's fourth shield layer is part of second storage capacitor plate 127, which is in the second electrode layer. *See* Claims 2, 21. §§IV.C.2, IV.C.9.

11. Claim 23

a. 23[a]:

See 1[b]-1[c], describing a first storage capacitor plate 125h and a second storage capacitor plate 127, forming a “first capacitor.” §IV.C.1.c, §IV.C.1.d.

b. 23[b]:

See 1[b]-1[c], discussing first and second capacitor plates being in the first and second electrode layers, respectively. §IV.C.1.c, §IV.C.1.d.

See also Cok, ¶¶308-311.

12. Claim 33

a. 33[pre]-[e]:

See 1[pre]-1[e] (§IV.C.1.a-§IV.C.1.f), Fig. 8 embodiment's element 127 forming the "first shield layer."

b. 33[f]:

See Claim 2. §IV.C.2.

c. 33[g]-[h]:

See 10[a]-10[b]. §IV.C.7.a-§IV.C.7.b.

See also Cok, ¶¶312-323.

**D. Ground 2B: Kim-923-Moon Combination Renders Obvious
Claims 6-7, 15-19, 24-27.**

1. Moon

Moon describes TFTs and OLED displays, while recognizing pixels may not have proper luminance to represent an image. Moon, ¶¶3, 26. Each pixel in Moon's OLED display includes a 6-transistor-2-capacitor (6T2C) driving circuit connected to voltage lines and data lines. *Id.*, ¶42, Fig. 3. Moon's driving transistor, T1, has two current channels with different lengths to provide different current levels to storage capacitor, Cst, and to the OLED. *Id.*, ¶¶61-63.

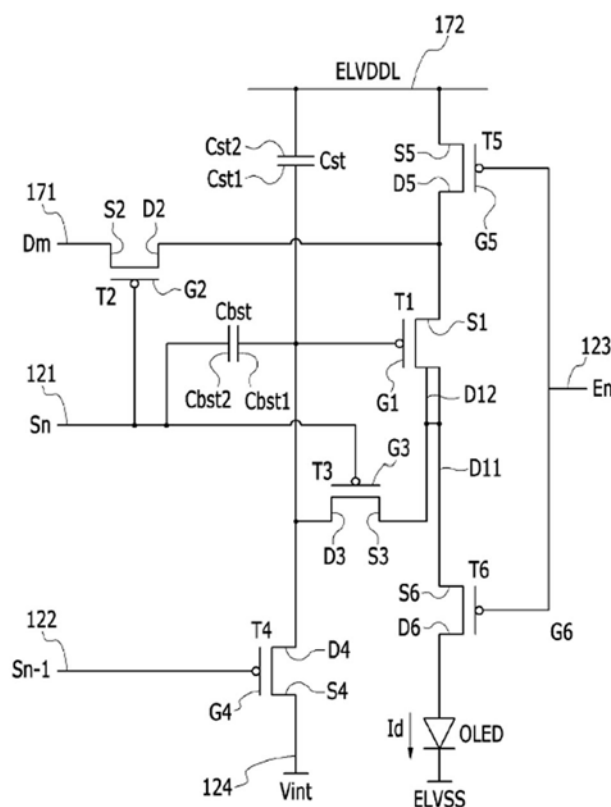


Fig. 3

Moon’s Fig. 4 (annotated below) illustrates the layout of TFTs, capacitors, and voltage/signal lines (*id.*, ¶¶25, 68-84, Fig. 4), illustrating T4 (initialization TFT, red oval) and its two gates (G4), source (S4) and drain (D4), and voltage line 124 (initialization power line, green) overlapping T4. *Id.*, ¶¶48, 54, 79, 90, Fig. 4.

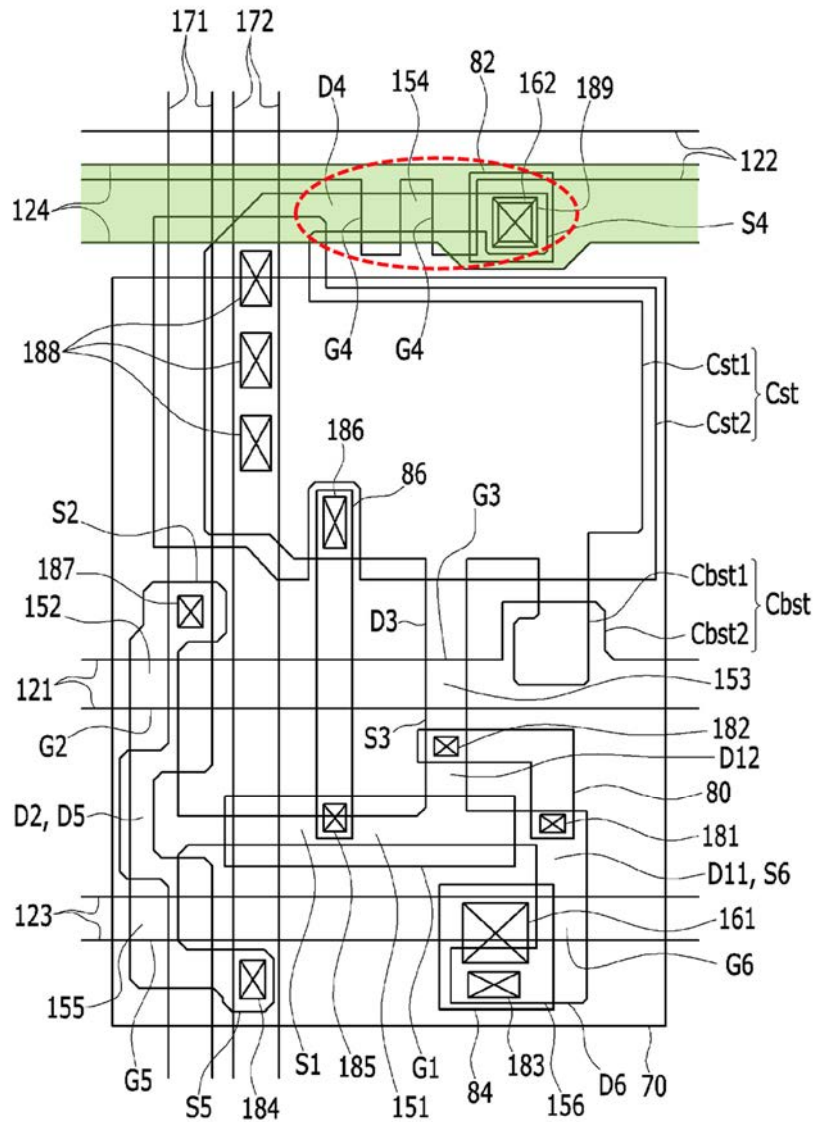


Fig. 4

2. Motivation to Combine

POSITAs would have been motivated to combine Moon with Kim-923 because both references related to OLED display circuits utilizing six TFTs. Kim-923, ¶¶3, 60, Fig. 1; Moon, ¶¶3, 42, Fig. 3. And both sought to improve the operations of OLED displays. Kim-923, ¶9; Moon, ¶26. Therefore, POSITAs would

have been guided by the complementary teachings of Kim-923 and Moon sharing a common goal, and would have recognized that Kim-923's device can be improved based on Moon's teachings.

POSITAs would have also been motivated to apply a known technique (implementing a multi-gated TFT and moving a voltage line in the pixel layout) to a known device ready for improvement (Kim-923's OLED pixel) to yield predictable results (reducing leakage current, simplifying design, with a smaller footprint). POSITAs would have had a reasonable expectation of success, because using multi-gated TFTs in display circuits was well-known by 2014, as evident by Moon and other prior art references (Cok, ¶¶57-58, citing EX1021-EX1023, EX1025, EX1027), and such modifications were well within POSITAs skillset of. *Id.*, ¶¶326-329.

Additional motivations are described in claim limitations below.

3. Claim 24

a. 24[pre]-[b]:

See 1[pre]-1[b], Ground 2A. §IV.C.1.a-§IV.C.1.c.

b. 24[c]:

See 1[d], Ground 2A. §IV.C.1.e. Claim 24 recites the first signal line over the first electrode layer vs. Claim 1's second electrode layer. Kim-923's line 171 ("first signal line," yellow) is over both the first (125h, blue) and the second (127, green) electrode layers. *See*, Kim-293, Fig. 4 (annotated below).

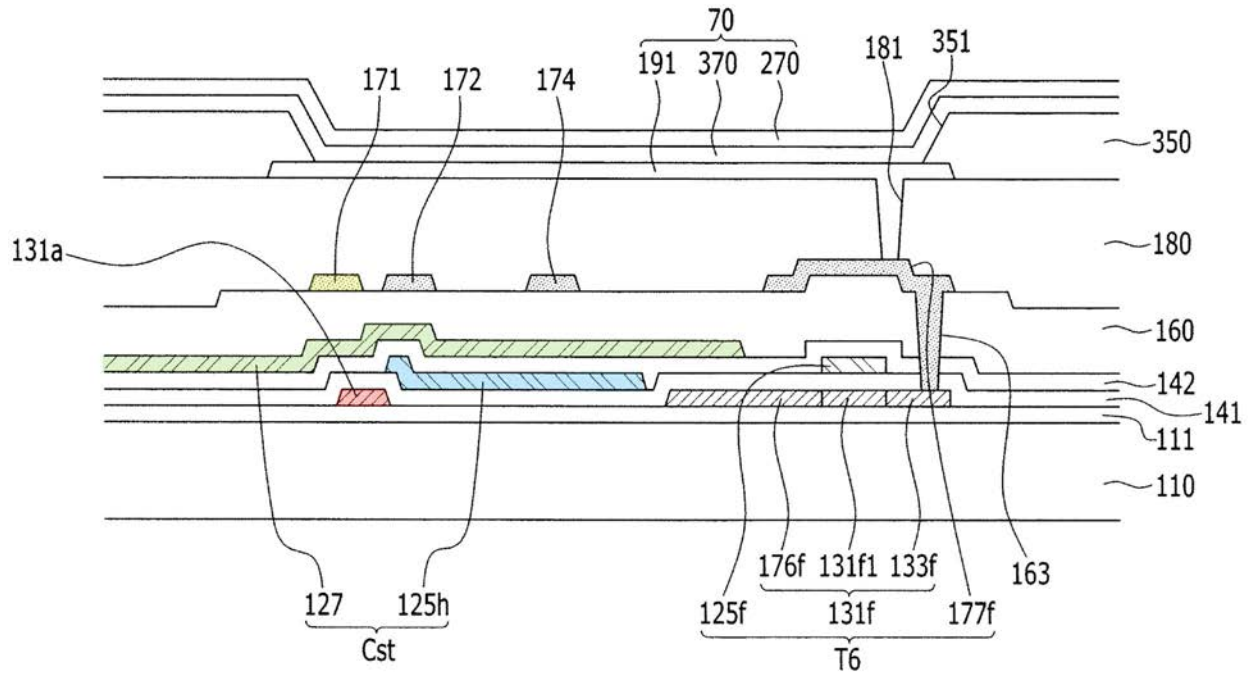


Fig. 4

c. 24[d]:

Kim-923's T4 is the "second" TFT formed along a semiconductor layer (131d) ("second semiconductor"): "...**initialization thin film transistor T4...**[is] **formed along the semiconductor layer 131**" Kim-927, ¶¶79, 92.

Annotated Fig. 3 (below) shows, and Kim-923 describes, T4's drain ("one end of the second semiconductor") connected (red line A) to T1's gate and to lower storage capacitor plate Cst1 ("first electrode layer"), and T4's source ("other end of the second semiconductor") connected (red line B) to initialization voltage line 124 ("a voltage line"). Kim-923, ¶66. As discussed in §IV.C.1.c., T1's gate electrode, G1, is in the "first electrode layer."

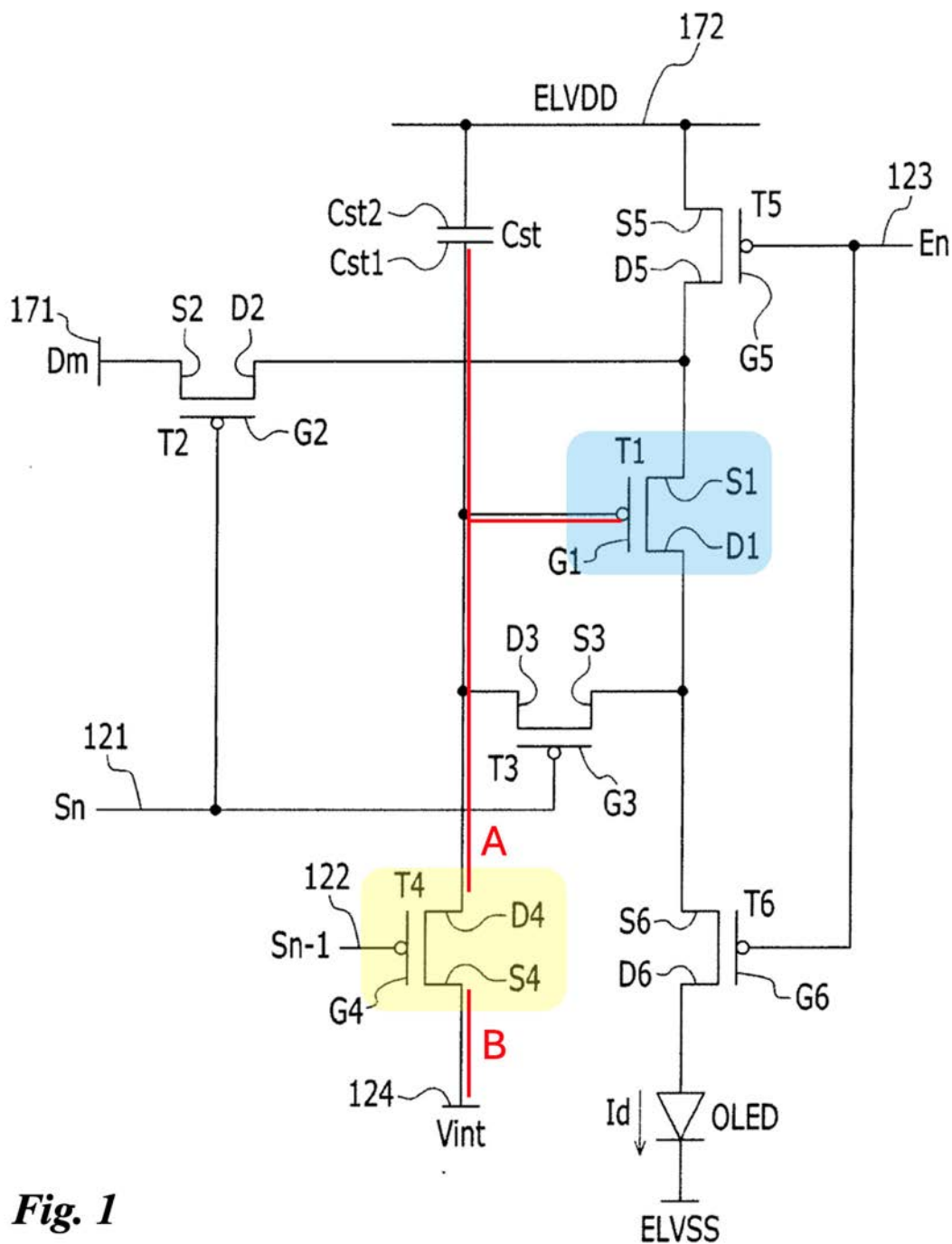


Fig. 1

Kim-923 explains T4 is formed along a portion 131d of semiconductor 131 and includes source/drain electrodes formed as semiconductor's doped regions.

Kim-923 ¶¶79, 85, 92. Therefore, the Fig. 1 connections of T4's source/drain are

through the doped semiconductor regions that form the drain/source electrodes. *Id.*, see also Figs. 2 and 3 (annotated below), showing T4's drain (177d) connecting to T1's gate/lower storage capacitor plate Cst1 (125a) through contact holes 166, 167 and connection line 164 (*id.*, ¶112), and connection of T4's source (176d) to initialization voltage line 124 through contact holes 161, 162 and connection line 78. *Id.*, ¶92.

Vint-to-T4 connection is also illustrated in Kim-923's Fig. 2, where line 124 supplies Vint to T4's source from an adjacent pixel.

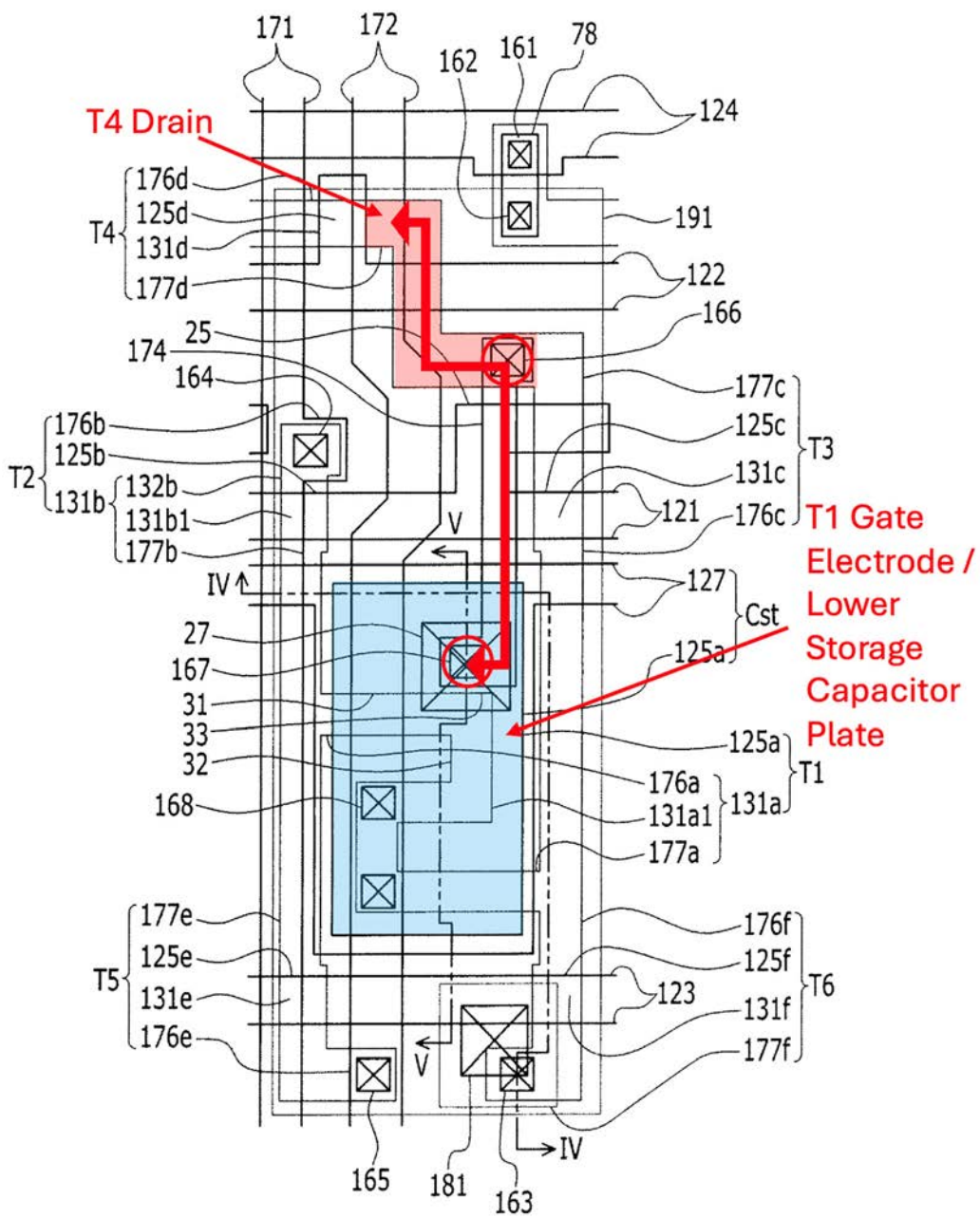


Fig. 3

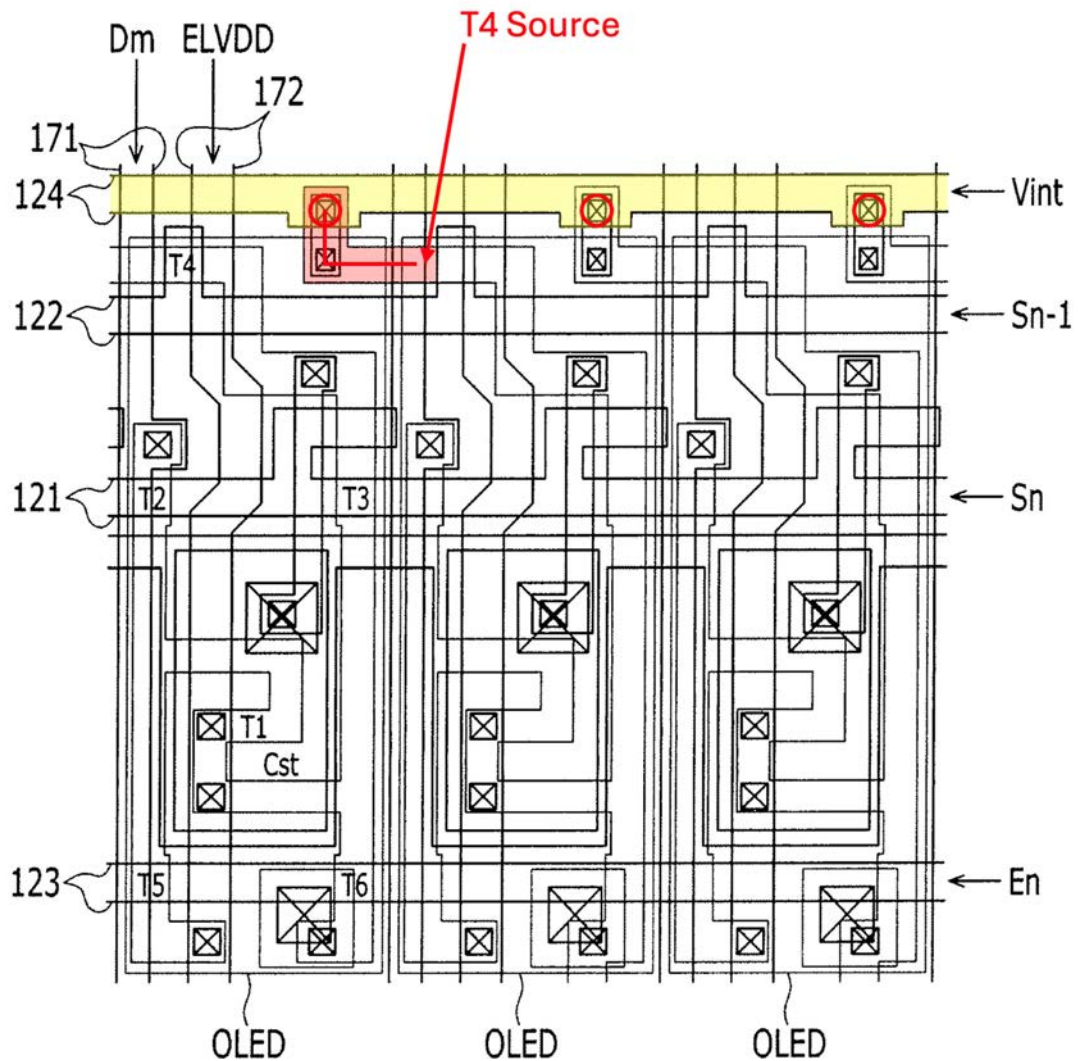


Fig. 2

d. 24[e]:

The Kim-923-Moon combination teaches or suggests this limitation.

Kim-923 teaches data line 171 is in a layer above initialization power line 124. POSITAs would have known this because Fig. 4 (annotated below) shows second storage capacitor plate 127 (green) is in a layer above semiconductor layer 131 (red) and below data line 171 (yellow), and Kim-923 explains, “**second storage capacitor**

plate 127...is formed on the same layer as the initialization voltage line 124."

Kim-923, ¶88. Therefore, line 124 is also above T4's semiconductor layer ("second semiconductor") and below signal line 171 ("first signal line.")

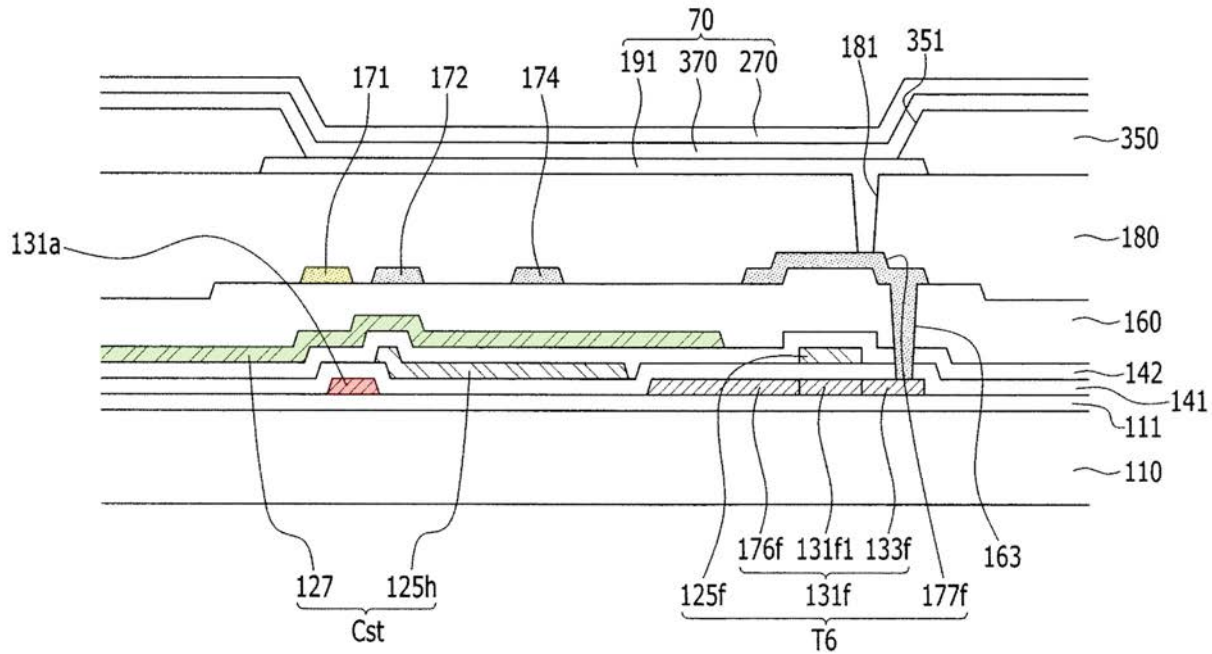


Fig. 4

Kim-923 does not describe a shield layer, and although its Fig. 3 shows the previous scan line 122 overlapping T4's semiconductor at two locations, it does not explicitly identify T4 as a dual-gate TFT. However, Moon clearly discloses these limitations.

Moon's Fig. 4 (annotated below) shows initialization power line 124 (green) overlaps Moon's T4 transistor forming two gates (red circles). Moon, ¶¶43, 48. Initialization power line 124 overlaps the entire T4, including a part between the first channel area and second channel area, i.e., between T4's dual gates. *Id.*, Fig. 4. T4's

gates (labeled G4 by Moon—red circles) are at locations where previous scan line 122 (blue) overlaps T4's semiconductor layer. *Id.*, ¶73: "...previous scan line 122 has the gate electrode G4 overlapping the semiconductor 154 of the initialization transistor T4."

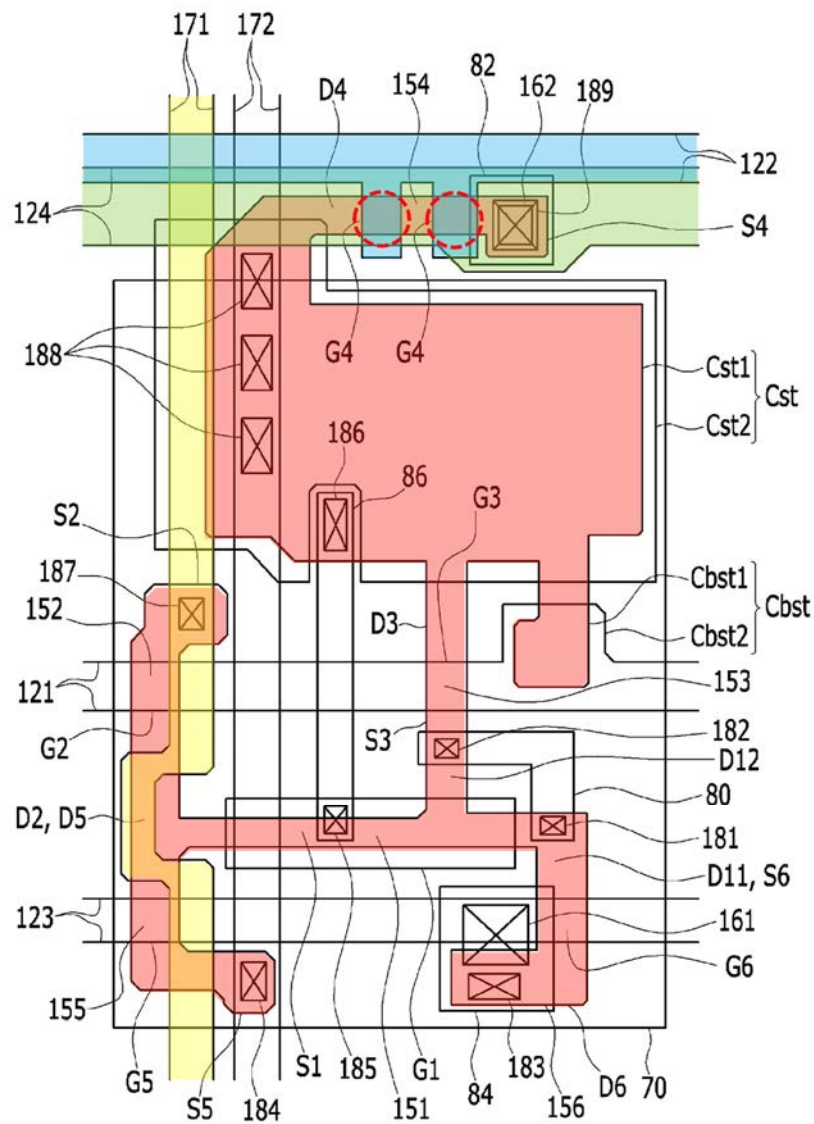
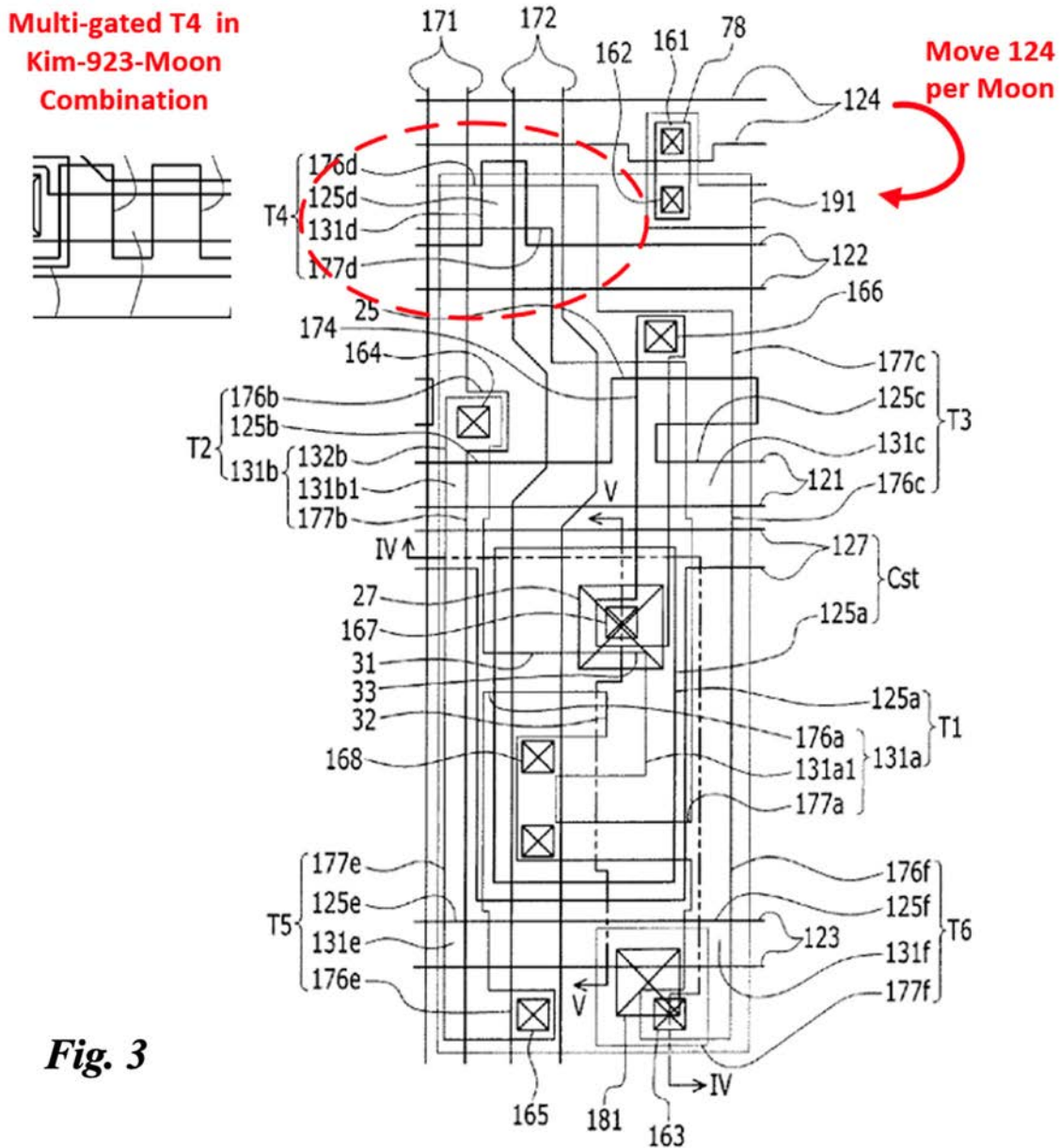


Fig. 4

In the combination, Kim-923's TFT T4 would be a multi-gated TFT structure as confirmed by Moon, and initialization voltage line 124 of Kim-923 would be moved to overlap T4, as taught by Moon. A rudimentary sketch of the modification steps is below. Cok, ¶¶345-346.



Aside from reasons articulated in §IV.D.2, POSITAs would have been motivated to combine Kim-923 with Moon because it would have improved the operation of Kim-923's display device; having a multi-gated TFT structure would have reduced leakage current, which was well-known in the art, routinely done in OLED drive circuits (*see e.g.* Kim-584, Cok, ¶¶57-58, 347), and acknowledged by Kim-923 in describing TFT T3. Kim-923, ¶91. Further, it would have been advantageous to move Kim-923's initialization voltage line 124 down to overlap T4 (as shown in Moon) because such rearrangement would have freed up the space occupied by line 124, allowing the pixel area to be made more compact, thus enabling a higher-resolution display. The rearrangement of voltage line 124 would have also made the circuit layout simpler because Vint, in the combination, would directly pass over T4's source and would connect directly thereto by a simple "via" (formed in insulation layer between Vint and T4's source) as opposed to connection line 78 and two contact holes 161, 162 described in Kim-923 (prior to modification), which would occupy more space and require more material. Kim-923, ¶92;

POSITAs would have had a reasonable expectation of success because T4 and voltage line 124 performed similar operations in both references (Kim-923, ¶¶71, 79; Moon, ¶48), modifications were already described in Moon, and the layout changes were routine tasks well within POSITAs skillset. Cok, ¶¶348-349.

The combination renders element 24[e] obvious because Kim-923's initialization voltage line 124 is at the same layer as top capacitor plate 127 (green annotation in Fig. 4 below, Kim-923, ¶88), and would be between data line 171 and T4's semiconductor (i.e., portion 131d of semiconductor layer 131 that also includes 131a). The initialization voltage line would overlap “a part between a first channel area and a second channel area of the second semiconductor” because it would overlap T4's semiconductor between T4's two gates (G4), as shown in Moon and described above. Cok, ¶¶350-351.

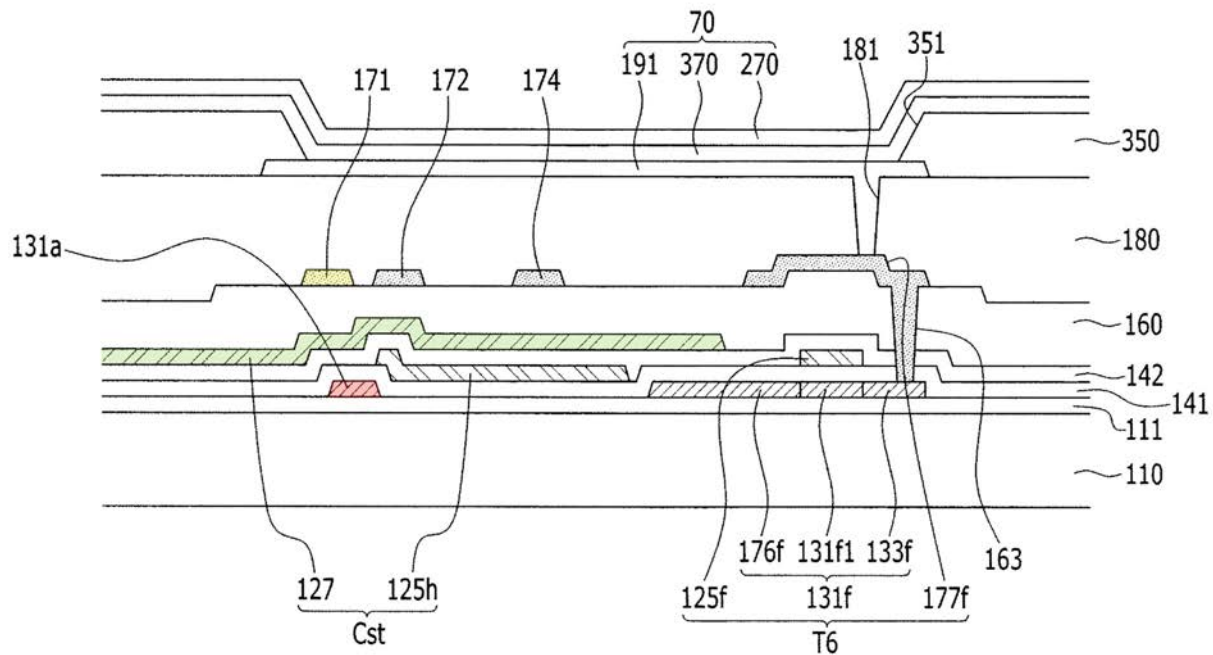


Fig. 4

Initialization voltage line 124 would be a “shield layer” because it carries a constant voltage (V_{int}) (Kim-923, ¶62) and shields T4 from electrical noise of data line 171, consistent with '015 patent, explaining “the second shield layer SD2 may

be a part of the initialization voltage line 124.” Ex. 1001, 13:47-48. Using voltage lines for shielding data lines was well-known and obvious. *See* Cok, ¶¶330-352, *see also id.*, ¶¶52-56, citing EX1013-EX1020, EX1026, EX1032-EX1033.

4. Claim 25

a. 25[a]:

See 24[e] (§IV.D.3.d) and Moon’s annotated Fig. 4, showing two gate electrodes (G4) formed where previous scan line 122 overlaps T4’s semiconductor (each gate is over a corresponding channel region). Moon, ¶73. It would have been obvious that both gates were in the same layer because they were formed by the same line 122. Cok, ¶¶353-356.

b. 25[b]:

Kim-923’s Fig. 6 (annotated below), shows prior scan line 122 (“second signal line,” blue) crossing signal line 171 (“first signal line,” yellow). In the combination, prior scan line 122 would remain in the same location and form two gate electrodes. *See* 25[a]. Prior scan line 122 is in the first electrode layer that includes the lower capacitor plate/T1’s gate electrode. Kim-923 ¶105: “...**the prior scan line 122, which includes the initialization gate electrode 125d...are formed on the first gate insulating layer 141.**” *See also* §IV.C.1.c; Cok, ¶¶357-359.

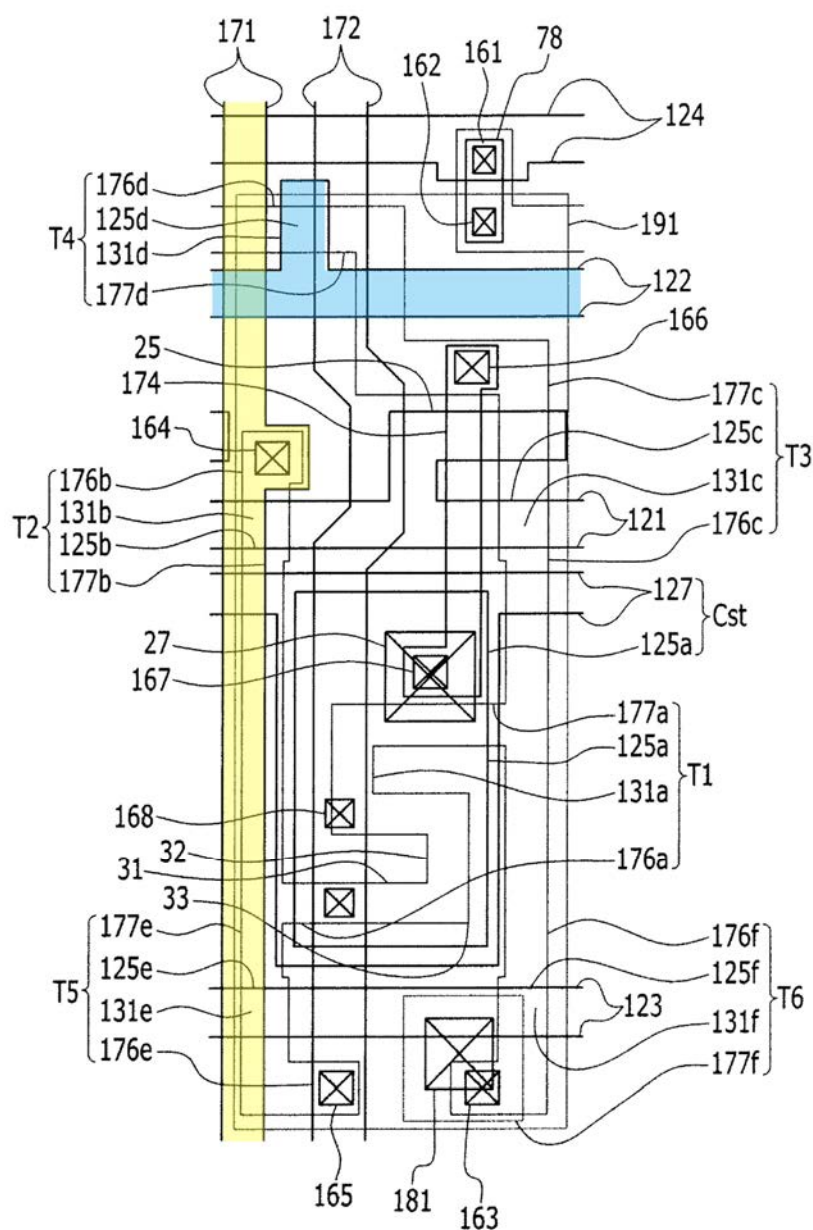


Fig. 6

5. Claim 26

Initialization voltage line 124 (“voltage line”) in the combination forms the shield layer. See §IV.D.3.d; Cok, ¶¶360-361.

6. Claim 27

Kim-923 shows one end of the second semiconductor (T4) connected to the first electrode layer (T1's gate/lower capacitor plate Cst1), labeled A in annotated Fig. 1 of Kim-923 below.

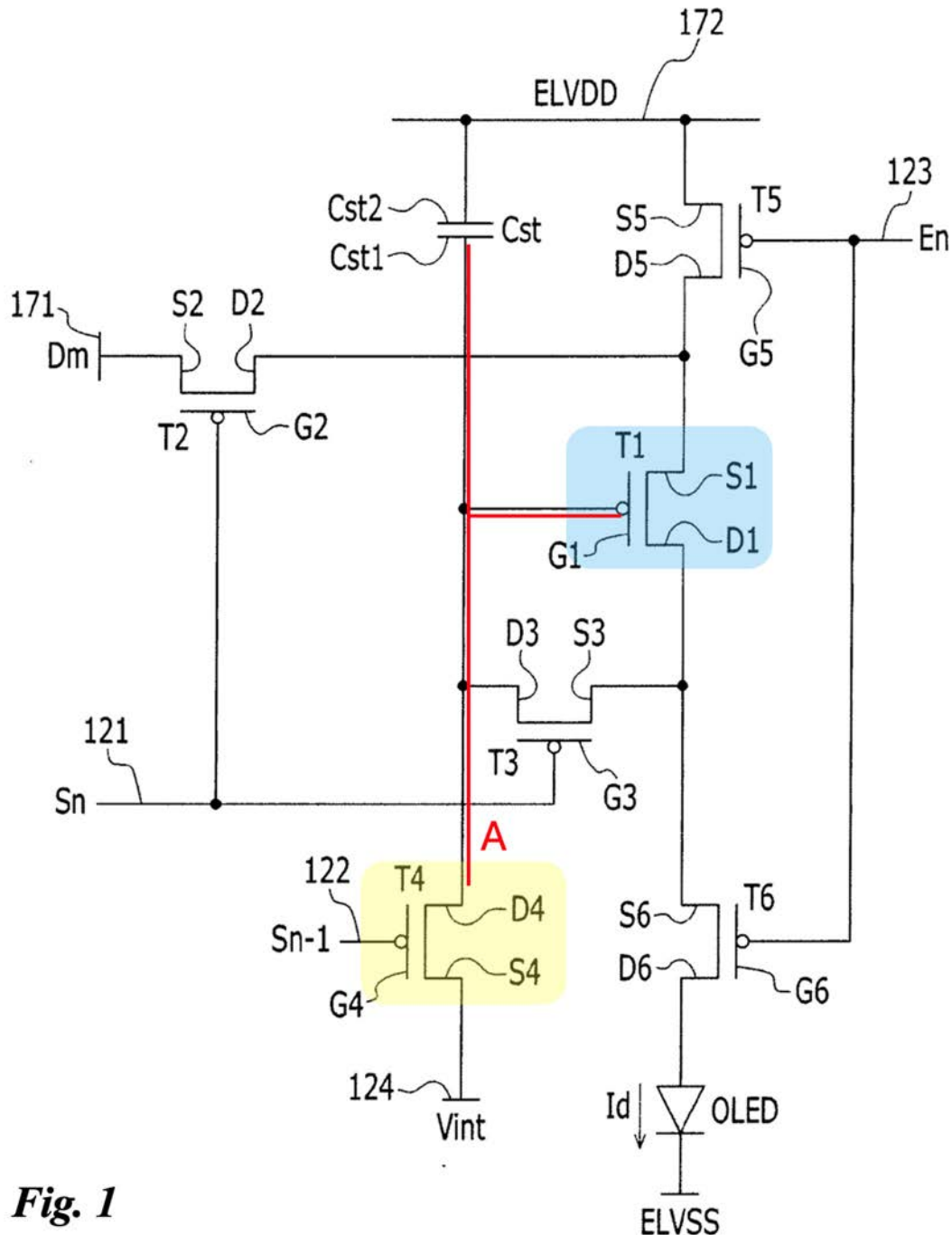


Fig. 1

This connection is made using connection member 174: “[t]he first storage capacitor plate 125h...is coupled through the connection member 174...to the initialization drain electrode 177d.” Kim-923, ¶96. *See also* annotated Fig. 3 below, showing connection member 174 (yellow) connecting T4’s drain (177d) (“one end of the second semiconductor”) to capacitor plate/gate electrode 125a/125h (blue) (“first electrode layer”).

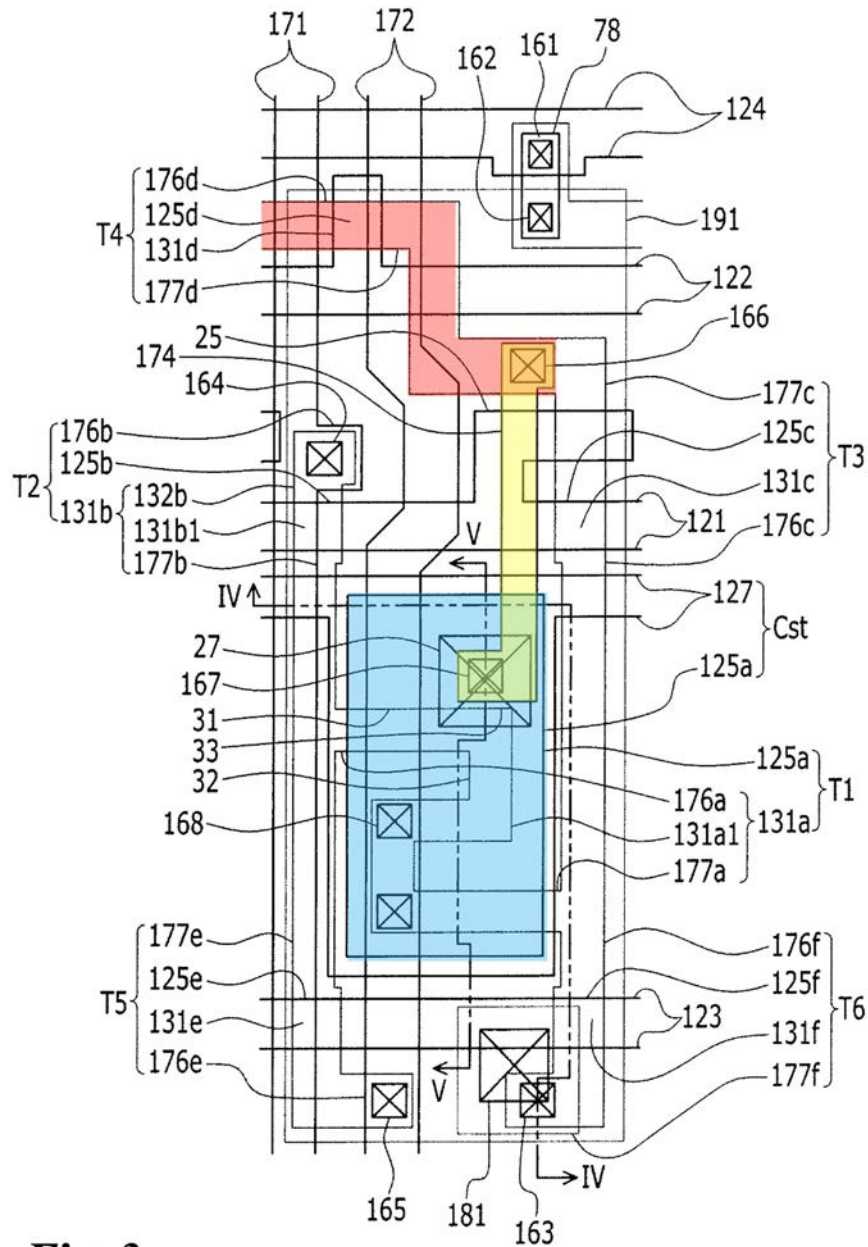


Fig. 3

Kim-923's annotated Fig. 4 below shows connection member 174 is in the same layer as data line 171 ("first signal line"). Cok, ¶¶362-366.

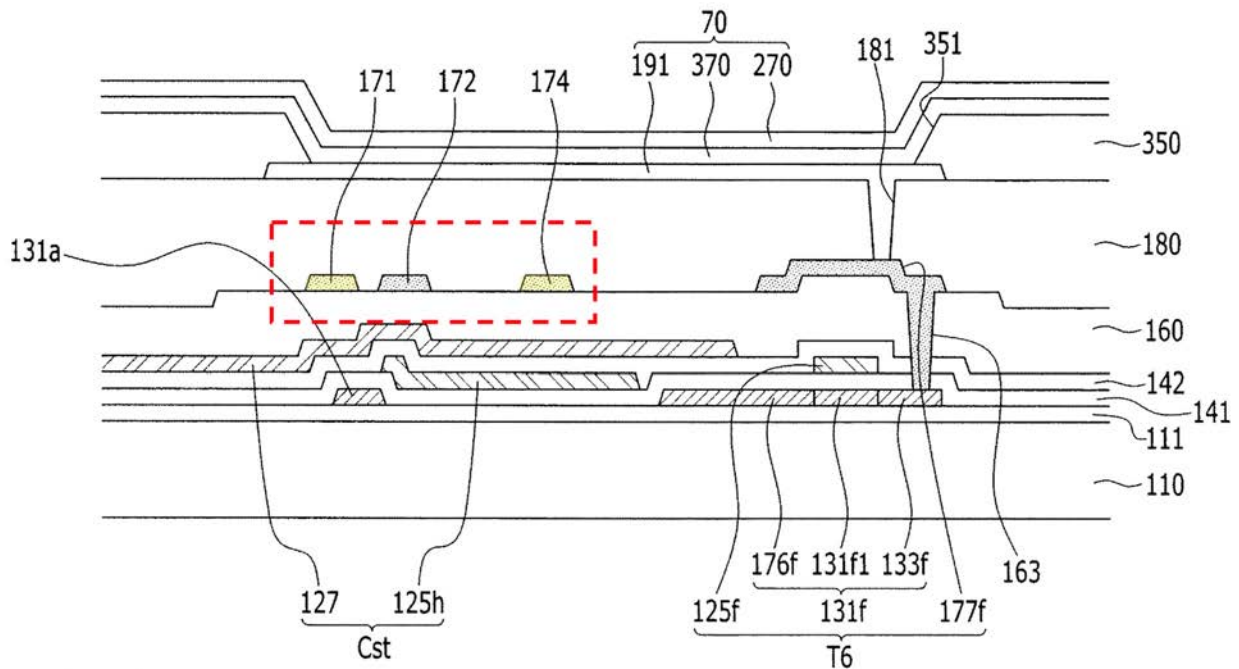


Fig. 4

7. Claim 6

a. 6[pre]:

See Claim 1. §IV.C.1.

b. 6[a]:

See 24[d] (§IV.D.3.c), with 6[a]’s “fourth” TFT/semiconductor treated as T4/associated semiconductor in the Kim-923-Moon combination. Claim 6’s “second voltage line,” is treated as 24[d]’s “voltage line” (124).

c. 6[b]:

See 24[e]. §IV.D.3.d. Claim 6’s “third shield layer” is treated as 24[e]’s “shield layer,” and is mapped to initialization voltage line 124 (or part thereof) that

overlaps T4. Unlike 24[e], 6[b] requires the third shield layer merely overlap “a part” of fourth semiconductor, which is satisfied by explanations in 24[e].

See Cok, ¶¶367-372.

8. Claim 7

a. 7[pre]:

See Claim 1. §IV.C.1.

b. 7[a]:

See 6[a]. §IV.D.7.b.

c. 7[b]:

See 24[e] (§IV.D.3.d) and 6[b]. §IV.D.7.c.

See Cok, ¶¶373-376.

9. Claim 15

a. 15[a]:

See 25[a] (§IV.D.4.a), with Claim 15’s “fourth” TFT/semiconductor treated as T4/associated semiconductor in the Kim-923-Moon combination.

b. 15[b]:

As in Claim 26 (and 24[e]), the “third” shield layer is part of “voltage line” 124. §IV.D.3.d, §IV.D.5. Claim 15’s “second voltage line” is treated as Claim 24’s “voltage line.”

See Cok, ¶¶377-380.

10. Claim 16

See 25[b]. §IV.D.4.b. Claim 16’s “third” (prior scan line 122 in Kim-923-Moon combination) is treated as Claim 25’s “second signal line.” Cok, ¶¶381-382.

11. Claim 17

See Claim 26 (§IV.D.5), with Claim 17’s “third shield layer” treated as Claim 26’s “second shield layer.” Cok, ¶¶383-384.

12. Claim 18

a. 18[a]-[b]:

See 25[a]-25[b] (§IV.D.4.a-(§IV.D.4.b), with the “fourth” TFT mapped to T4 in the combination, and 18[b]’s “third signal line” (prior scan line 122 of Kim-923-Moon combination) treated as 15[b]’s “second signal line.”

Cok, ¶¶385-388.

13. Claim 19

See Claim 27 (§IV.D.6), with Claim 19’s “fourth” semiconductor treated as Claim 27’s “second” semiconductor.

E. Ground 2C: Kim-923-Han Combination Renders Obvious Claim 5, 11-14, 28-32.

1. Motivation to Combine

POSITAs would have been motivated to combine Han with Kim-923 because both references related to OLED display devices that utilized six TFTs arranged in

a typical OLED driving configuration. Kim-923, ¶¶3, 60, Fig. 1; Han, ¶¶38-41, Fig. 2. Han uses triple-switched TFT structures that act in concert because they have a common gate control, similar to a double- or triple-gated TFT. And both references sought to improve OLED display devices and advocated for reducing leakage currents. Kim-923, ¶¶9, 91; Han, ¶¶9, 58. Therefore, POSITAs would have been guided by the complementary teachings of the two references sharing a common goal, and would have understood that the device of Kim-923 can be improved based on the teachings of Han.

In the combination, POSITAs would have found it obvious that leakage currents in Kim-923's OLED display can be further reduced, per Han, by adding a second capacitor, C2, to Kim-923's circuit. Han provided express motivation for the combination, explaining that adding capacitor C2 at the designated location between the voltage line ELVDD and TFT M3 would have "minimize[ed] or reduc[ed] the leakage currents." *Id.*, ¶58, Fig. 2.

Furthermore, POSITAs would have been motivated to apply a known technique (adding a second capacitor per Han) to a known device ready for improvement (Kim-923's OLED pixel) to yield predictable results (reduced leakage current). POSITAs would have had a reasonable expectation of success because adding a second capacitor to an OLED driving circuit was a routine design task, was

taught by Han, and such modifications were well within POSITA's skillset. Cok, ¶¶390-395.

Additional motivations are provided below.

2. Claim 5

a. 5[pre]:

See Claim 1. §IV.C.1.

b. 5[a]:

Kim-923's T3 is "a third" TFT. *See* Kim-923, Fig. 1 (annotated below). T3 is formed along a semiconductor portion (131c) ("third semiconductor") and includes source/drain electrodes formed as semiconductor's doped regions. *Id.*, ¶¶79, 85, 91. Therefore, Fig. 1's connection of T4's source/drain is through semiconductor doped regions forming T4's drain/source electrodes.

Annotated Fig. 1 (below) illustrates, T3's source ("one end of third semiconductor") connected (labeled A) to T1's drain ("one end of the first semiconductor"), and T3's drain ("other end of third semiconductor") connected (labeled B) to lower storage capacitor plate Cst1, which is T1's gate electrode (G1) ("first electrode layer"). Kim-923, ¶¶, 65, 86, Fig. 3.

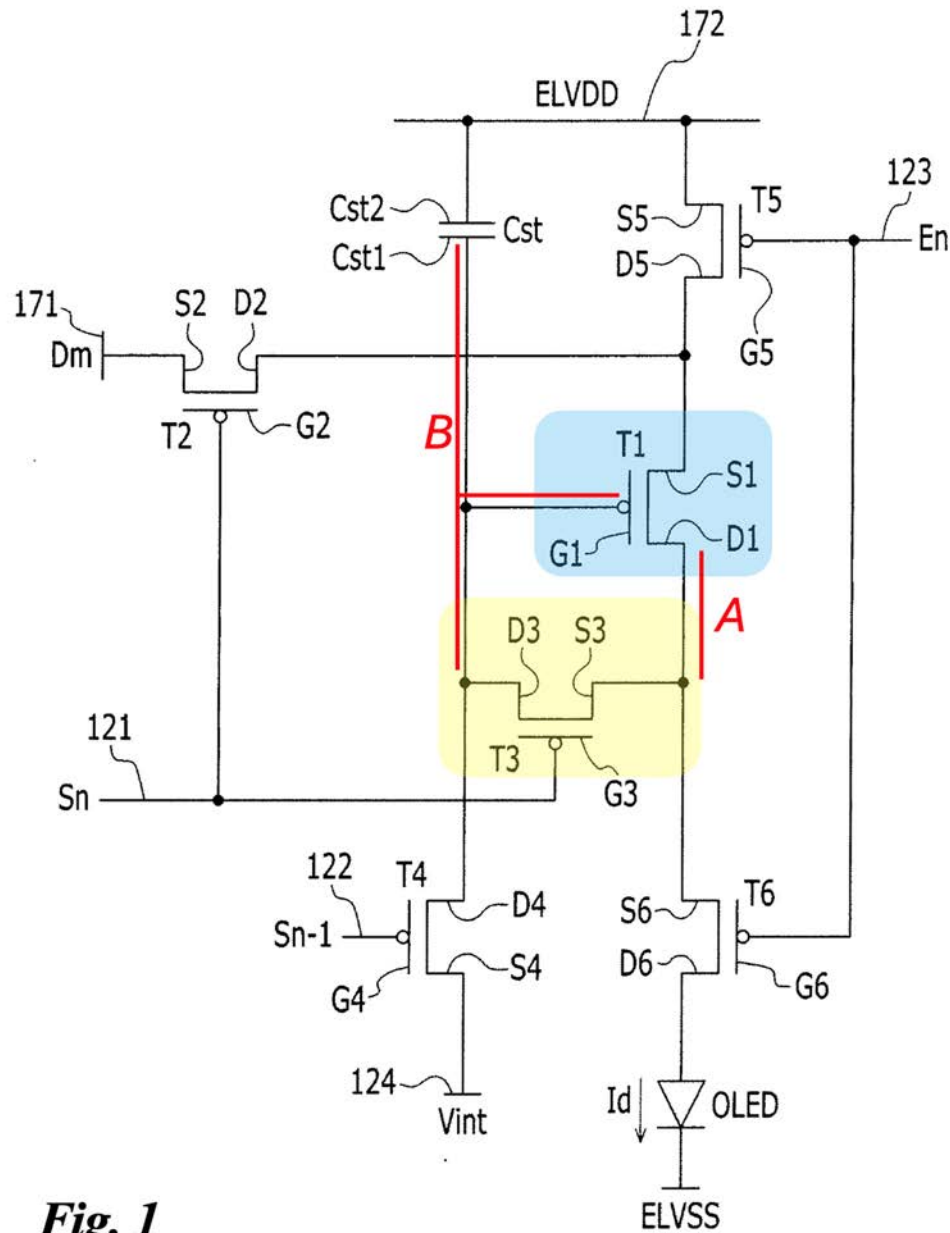
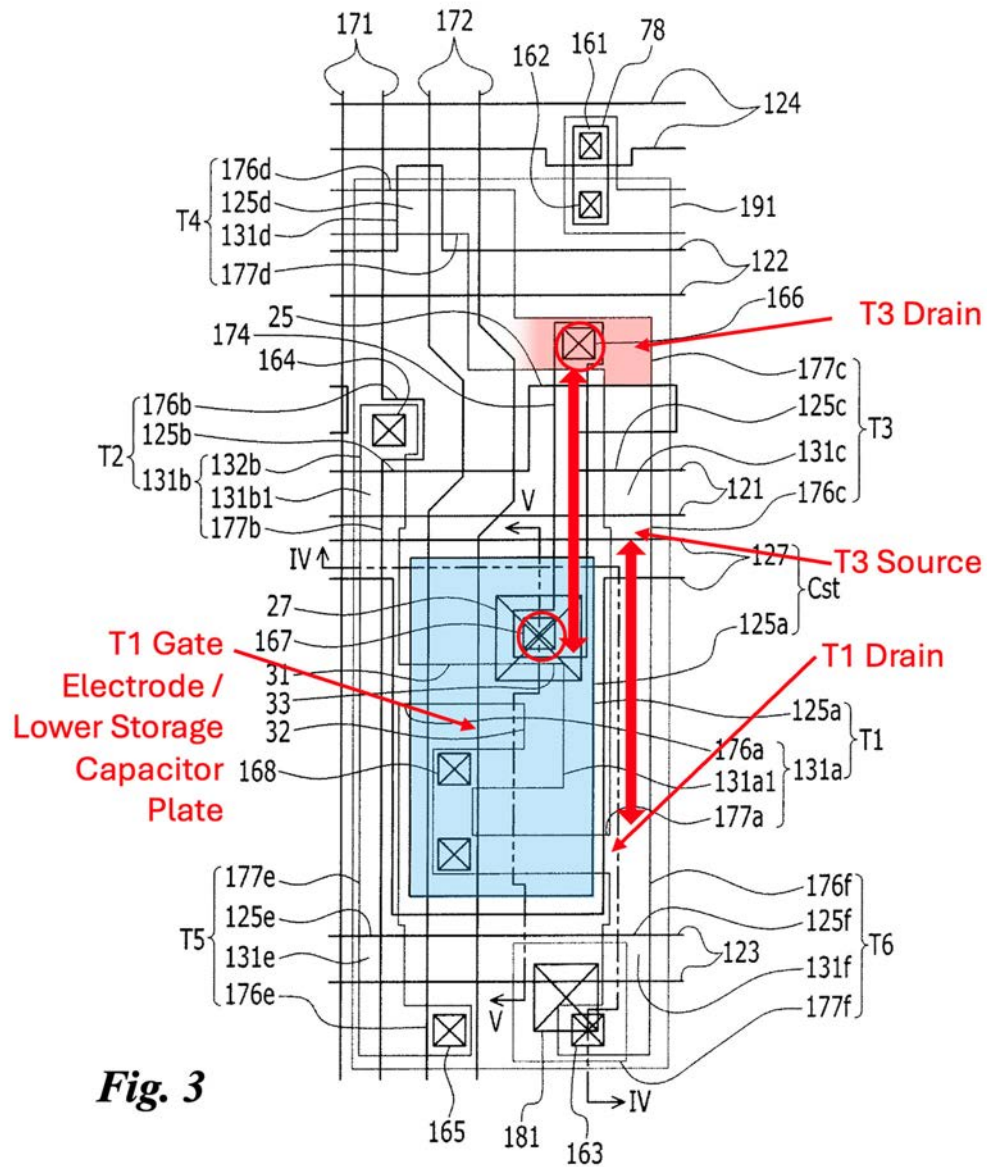


Fig. 1

Fig. 3 (annotated below) also shows semiconductor (131c) connectivity:
T3's source (176c) is connected to T1's drain (177a), and T3's drain (177c) is connected to lower storage capacitor plate/T1's gate electrode (125a) through holes 166, 167 and connection line 174. *Id.* ¶96. Cok, ¶¶396-401.



c. 5[b]:

Kim-923's T3 is double-gated. See Kim-923, ¶¶79, 91, 105, Fig. 3 (annotated below), with two gates (red circles) where scan line 121 (blue) overlaps semiconductor 131c (red). POSITAs would have understood that the semiconductor region under one gate electrode of T3 constitutes the “first channel area” and the semiconductor region under the other gate electrode constitutes the “second channel area.” *Id.*

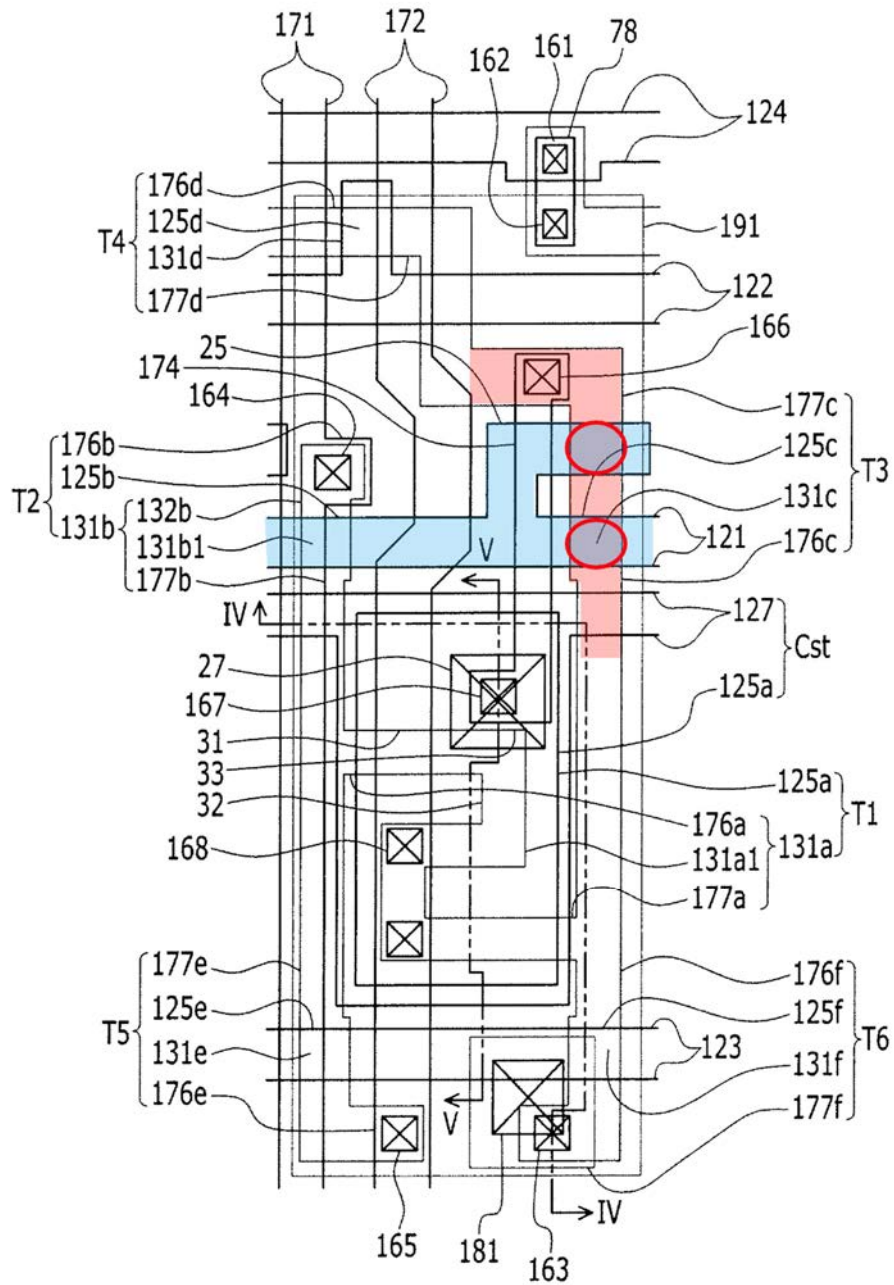


Fig. 3

Kim-923 does not explicitly disclose a second shield layer. However, this would have been obvious based on Han. *Id.*, ¶¶28, 58. As explained in §IV.E.1,

POSITAs would have found it obvious to add Han's capacitor C2 to Kim-923's circuit to further reduce leakage currents. Han, ¶¶28, 44, 58, Fig. 2.

Han's Fig. 2 and associated description explain capacitor C2 is "coupled to the first power supply (ELVDD), and a first terminal...is coupled to both a second node N2 and a third node N3." Han, ¶49, Fig. 2. As Fig. 2 illustrates, N2 is between M3-1 and M3-2 (first dual-gate TFTs).¹⁶

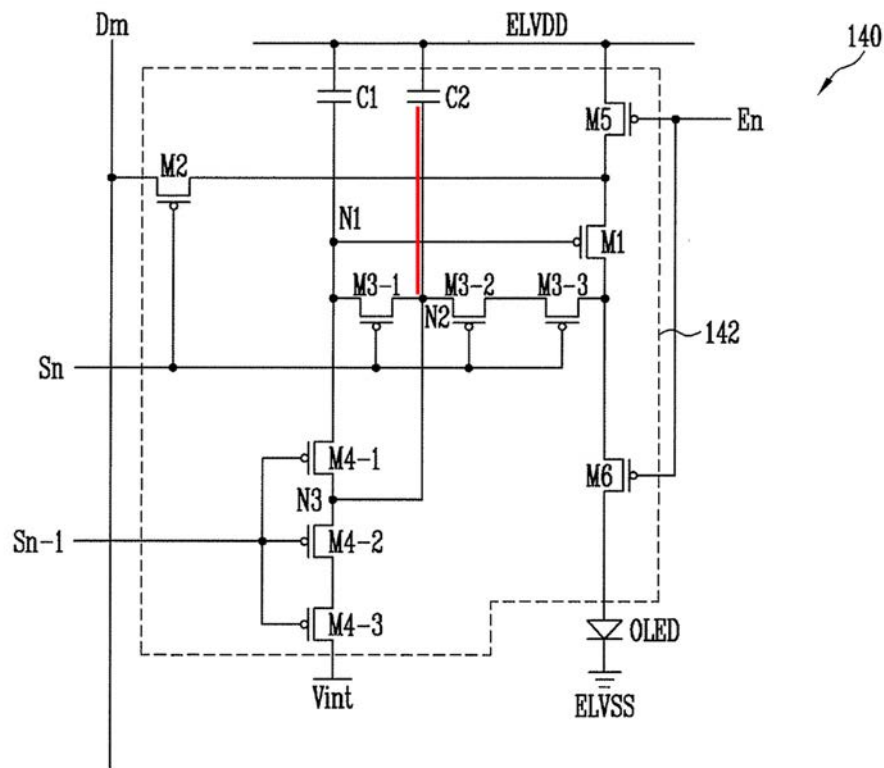


Fig. 2

¹⁶ While Fig. 2 illustrates three series-connected TFTs for M3/M4, Han explains M3 and M4 each can include two series-connected TFTs. Han, ¶¶44-45.

Therefore, POSITAs would have known that C2's lower plate must be connected to the drain-source junction between M3-1 and M3-2 TFTs (i.e., at N2). In the combination, this junction would be the doped (and thus conductive) semiconductor area between the two gates of T3, illustrated in Kim-923's Fig. 3 (annotated below). POSITAs would have understood that an obvious location for placing the plates of capacitor C2 would be at or above the designated junction; POSITAs would have found such a placement obvious and advantageous because it was close to (directly above or at) the semiconductor region of interest (node N2), and it would have allowed easy and direct connection of C2's lower capacitor plate to the junction, as required by Han's Fig. 2.

Notably, POSITAs would have understood that C2's lower plate would be implemented as part of the doped semiconductor layer at junction N2 between the dual gates, because Kim-923 explained the semiconductor layer can be doped and thus made conductive (Kim-923, ¶¶79, 90), and implementing one capacitor plate as part of the semiconductor layer was a known technique. *See* Moon, ¶76; Cok, ¶¶406, 191, citing EX1026, Fig. 5, element 110. Alternatively, POSITAs would have understood that C2's lower plate would be positioned above the junction between T3' dual gates over an insulating layer and connected to the junction (e.g., using a "via"), given that Kim-923's similarly placed C1's capacitor plate 125h above the semiconductor layer (131a). Kim-923, ¶¶79, 86, Fig. 4. Cok, ¶¶402-406.

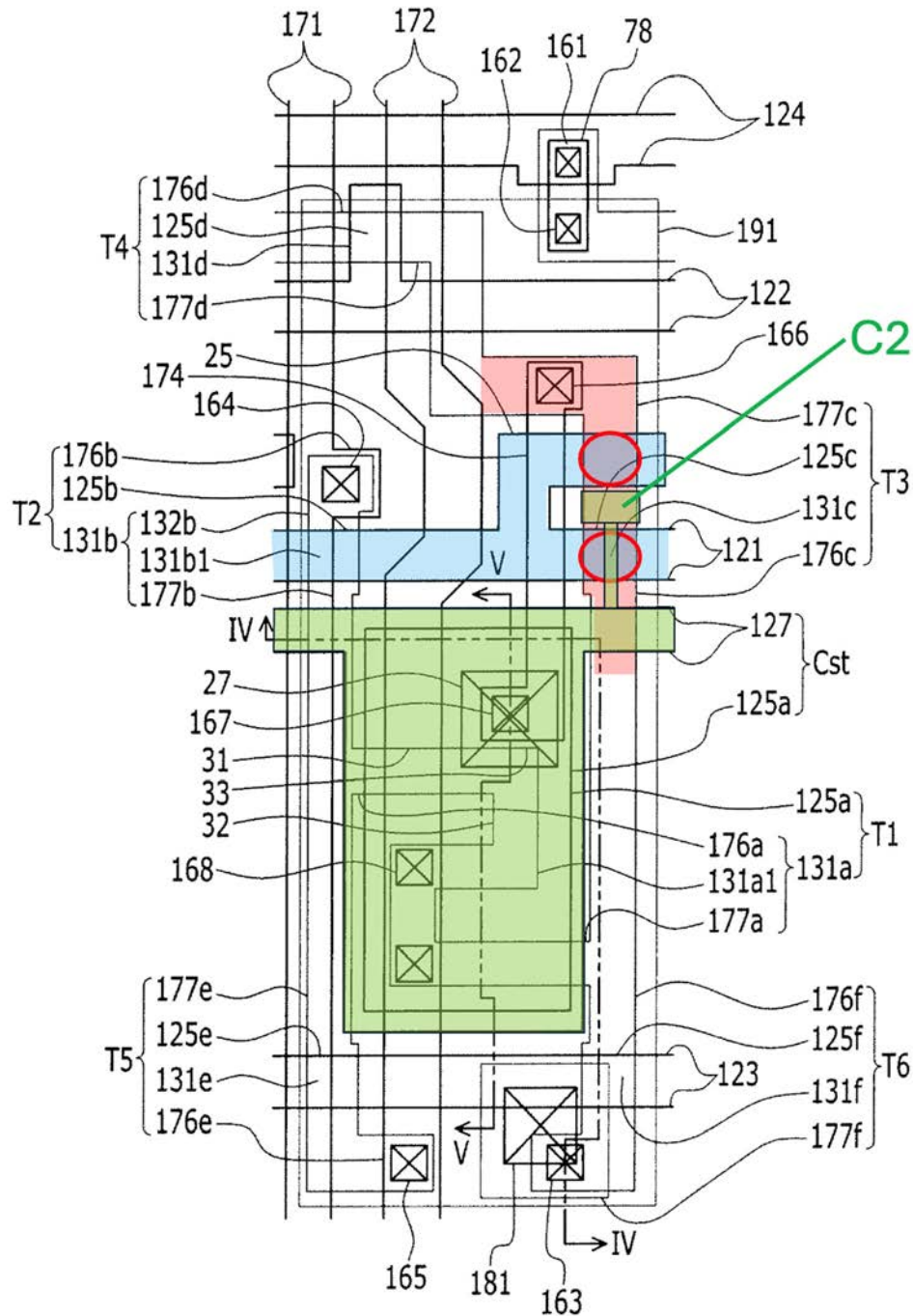


Fig. 3

C2's upper capacitor plate would connect to voltage line, ELVDD (172), per Han's Fig. 2. Han, ¶49. POSITAs would have found it obvious (and a routine layout design task) to implement that connection. For example, POSITAs would connect

C2's upper plate to upper plate (127) of storage capacitor, Cst, using a connection line, as shown in below illustration. The connection would have been obvious, routine, and advantageous because C1's upper plate (Kim-923's element 127) was nearby and already connected to ELVDD. Kim-923, ¶97, and Fig. 1, showing connection of Cst to ELVDD, and Han's Fig. 2, showing C1's connection to ELVDD. Accordingly, the upper plates of both capacitors would be in the same layer, connected together and connected to ELVDD. Cok, ¶406.

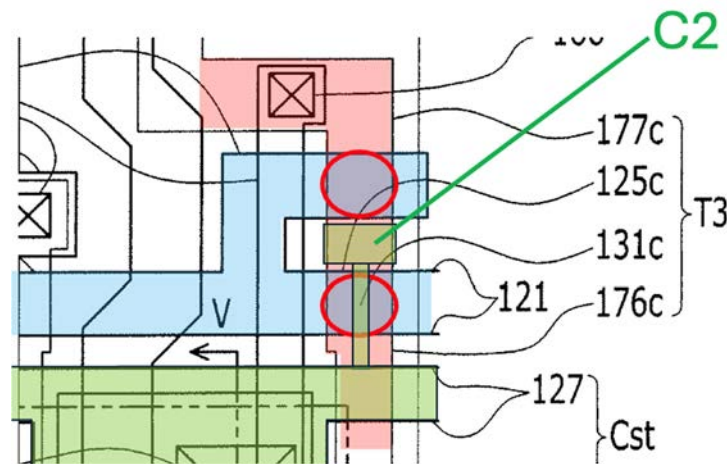
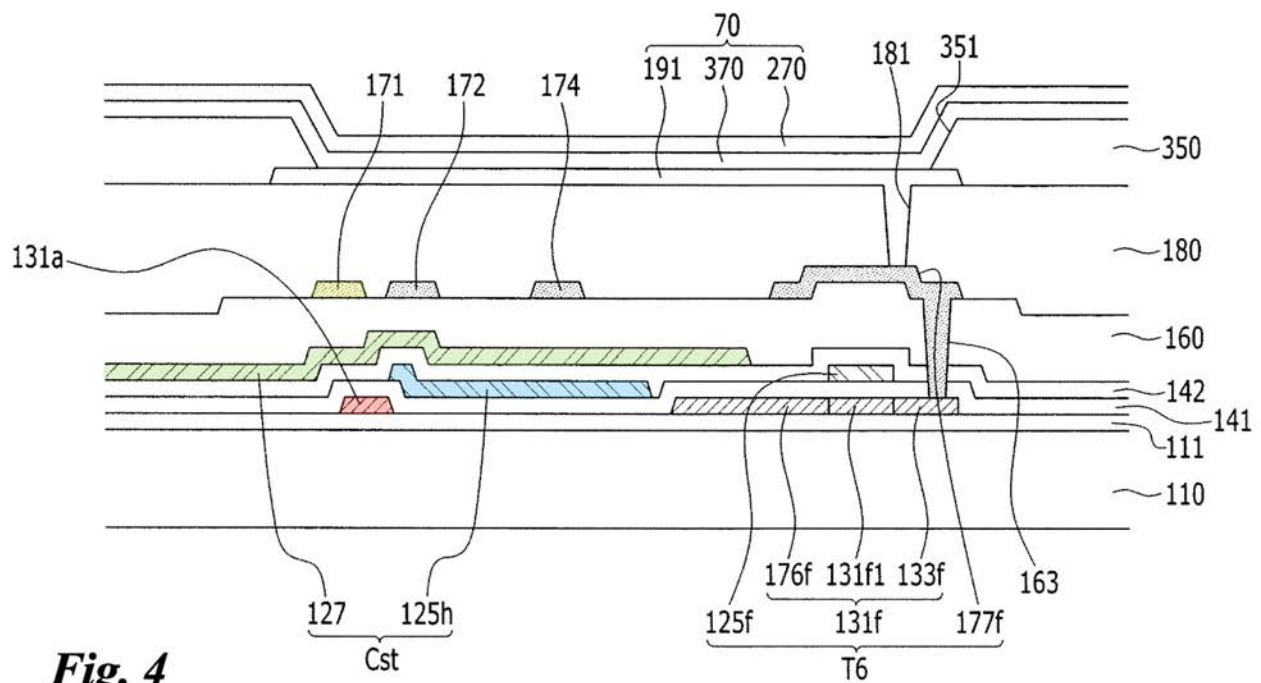


Fig. 3

In the combination, C2's upper plate, being connected to a constant voltage source, would be the "second shield layer." See §IV.A.1.f.

C2's upper capacitor plate would also overlap the semiconductor region between T3's gates (see annotated figure above) and would thus overlap "a part between a first channel area and a second channel area of the third semiconductor." Furthermore, the "second shield layer" would be in "a layer between the first signal

line and the third semiconductor” because C2’s upper capacitor plate would reside in the same layer as storage capacitor’s upper plate 127, (green annotation in Fig. 4 below, that resides (as explained in §IV.C.1.f) between the semiconductor layer (red) and data line 171 (“first signal line”).¹⁷ Cok, ¶¶407-412.



¹⁷ While Fig. 4 shows semiconductors 131a/131f, all of Kim-923’s TFT semiconductors, including 131c for T3 (“third semiconductor”) are part of the same semiconductor layer 131. Kim-923, ¶79.

3. Claim 11

a. 11[a]:

See claim 5. §IV.E.2. POSITAs would have understood that T3's gate electrodes overlap a first and a second channel area. The two gate electrodes are in the same layer because they are both part of scan line 121. Kim-923, ¶105.

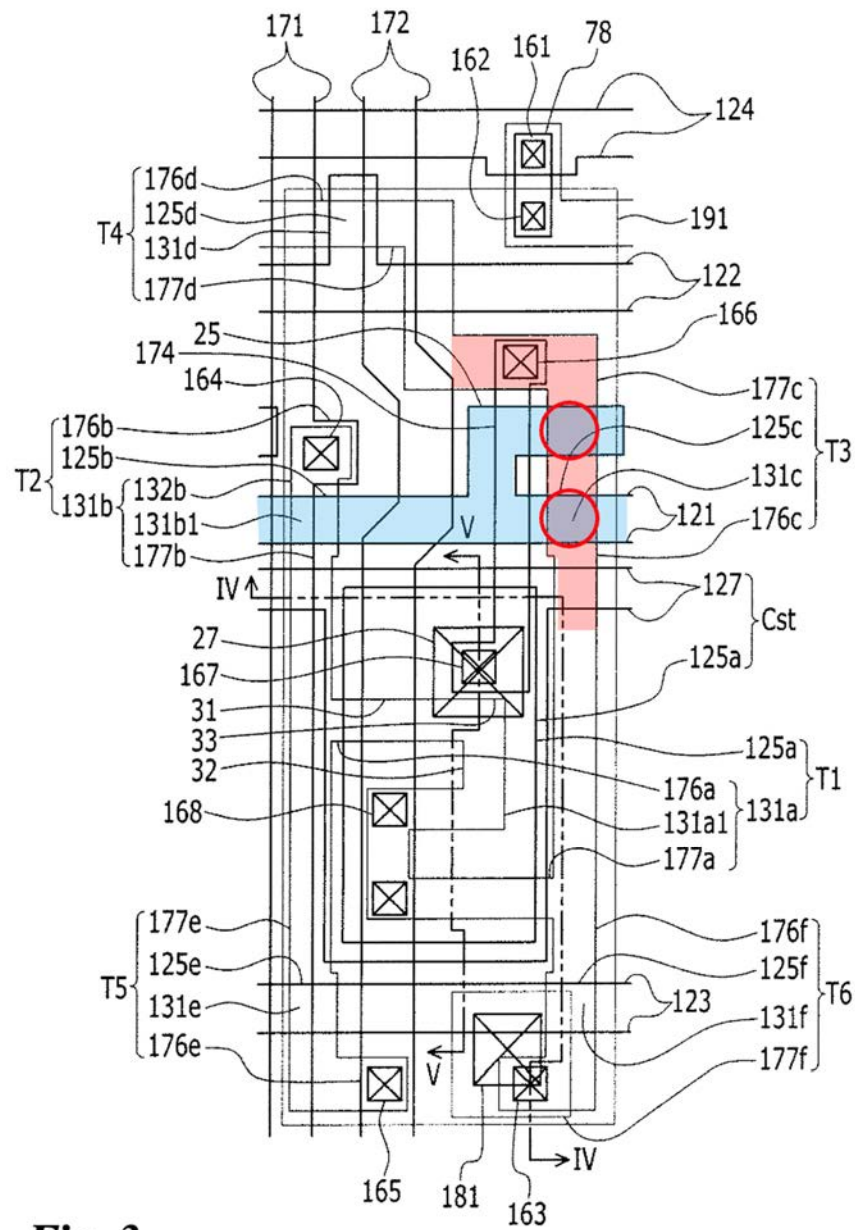


Fig. 3

b. 11[b]:

As annotated Fig. 3 shows, T3's gate electrodes are parts of scan line 121 ("second signal line," blue) that crosses data line 171 ("first signal line," yellow). Kim-923, ¶105; *see also* §IV.C.1.e.

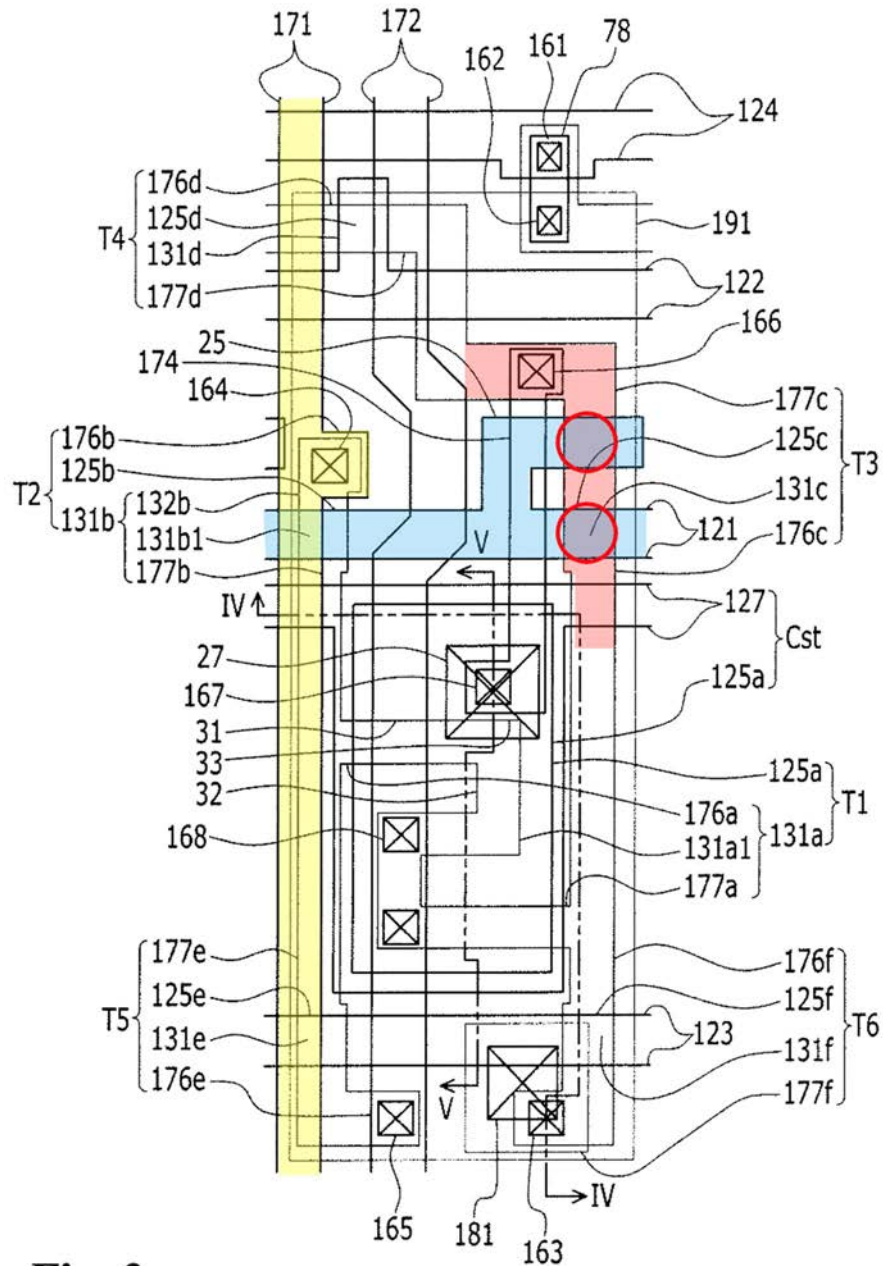


Fig. 3

Scan line 121 is in the same layer as the first storage capacitor plate/gate of T1 (“first electrode layer;” §IV.C.1.c): **“The first storage capacitor plate 125h...is formed of the same material as the scan line 121...which are on the same layer first storage capacitor plate 125h.”** Kim-923, ¶87. Cok, ¶¶413-418.

4. Claim 12

Kim-923’s voltage line 172 (“first voltage line;” see §IV.C.4) is in the same layer as data line 171 (“first signal line”)—see annotated Fig. 4 below. Voltage line 172 provides “a driving voltage ELVDD” (Kim-923, ¶62) and connects to capacitor C2’s top electrode (“second shield layer”) in the combination. See §IV.E.2; Cok, ¶¶419-421.

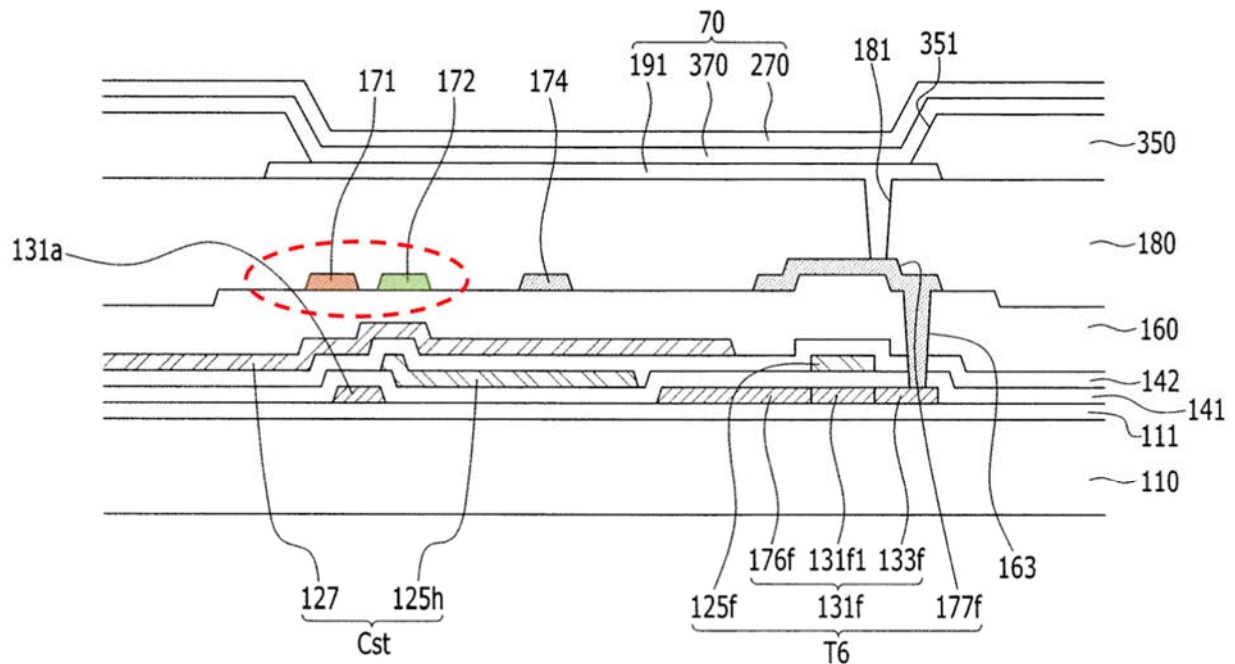


Fig. 4

5. Claim 13

In the combination, C2's top electrode would be in the same layer, and would connect to, C1's top plate because the two plates are required to be connected to ELVDD (see Han's Fig. 2), were in close proximity, and C1's top plate was already connected to ELVDD. *See* §IV.E.2.c and annotated Fig. 3; C1's top plate was part of the second electrode layer (*see* §IV.C.2), and therefore C2's top plate would also be in "second electrode layer." Cok, ¶¶422-424.

6. Claim 14

Kim-923 shows T3's drain (D3) ("other end of the third semiconductor") is connected to storage capacitor plate Cst1 and to T1's gate electrode (G1) ("first electrode layer")—see annotated Fig. 1 below, line B.

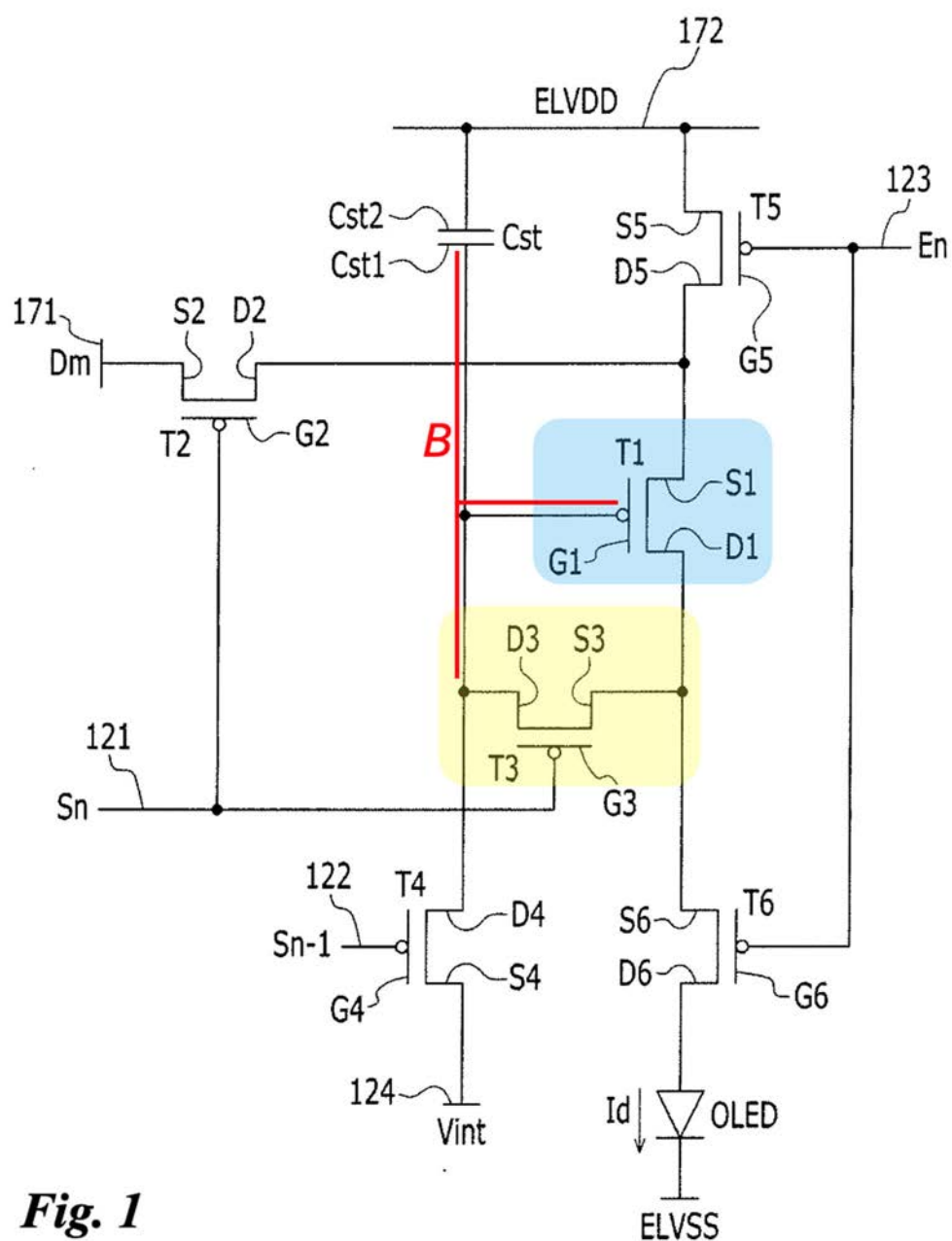


Fig. 1

Fig. 3 (annotated below) shows this connection is implemented using connection member 174 (yellow), which is in the same layer as the data line 171 (“first signal line”). Kim-923, ¶96, Fig. 3.

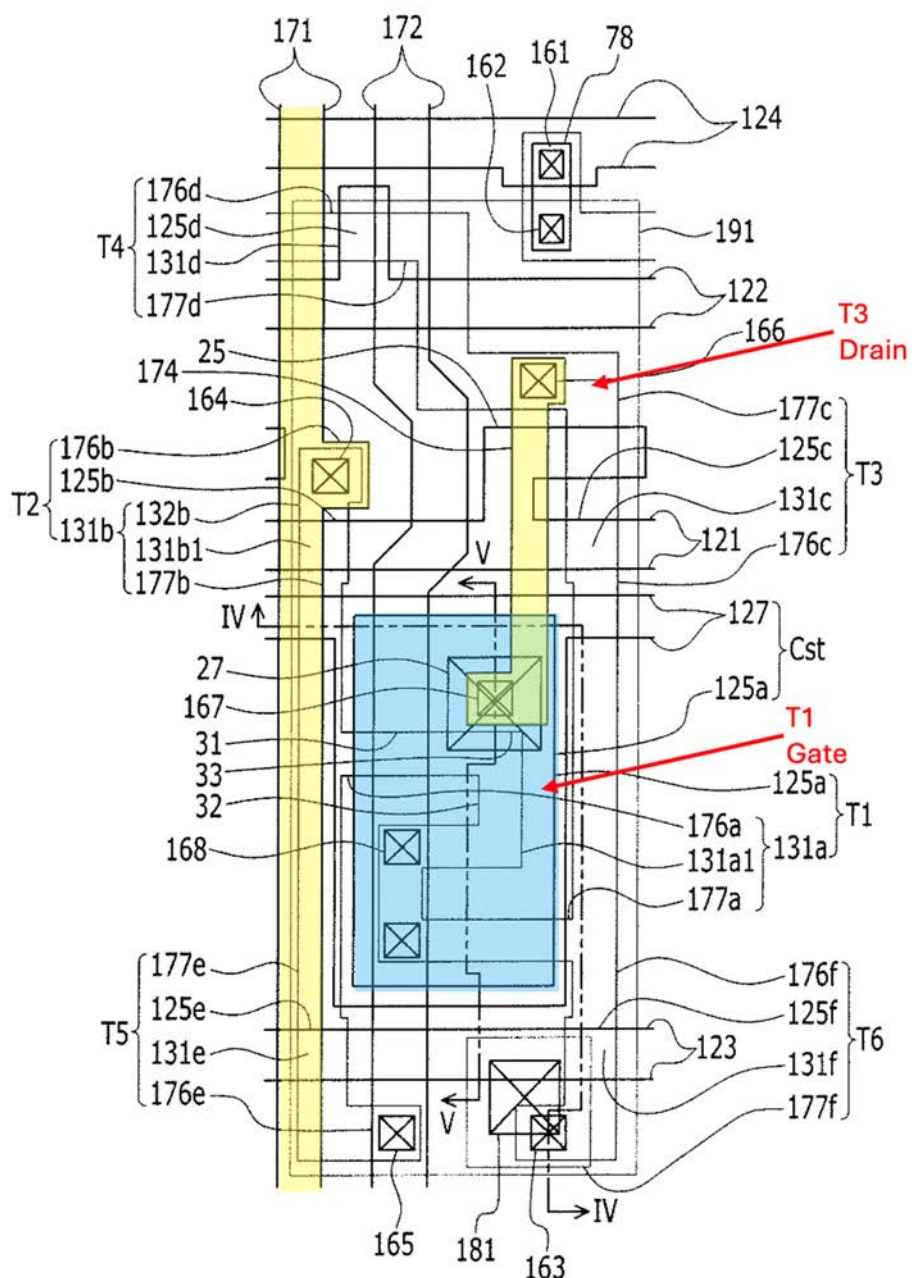


Fig. 3

Kim-923 explains: “...**connection member 174 is formed on the same layer as the data line 171, an end of the connection member 174 is coupled...to the compensation drain electrode 177c...and another end of the connection member**

174 is coupled ...to the first storage capacitor plate 125h.” *Id.*; see also annotated

Fig. 4 showing 174 and 171 in the same layer. Cok, ¶¶425-429.

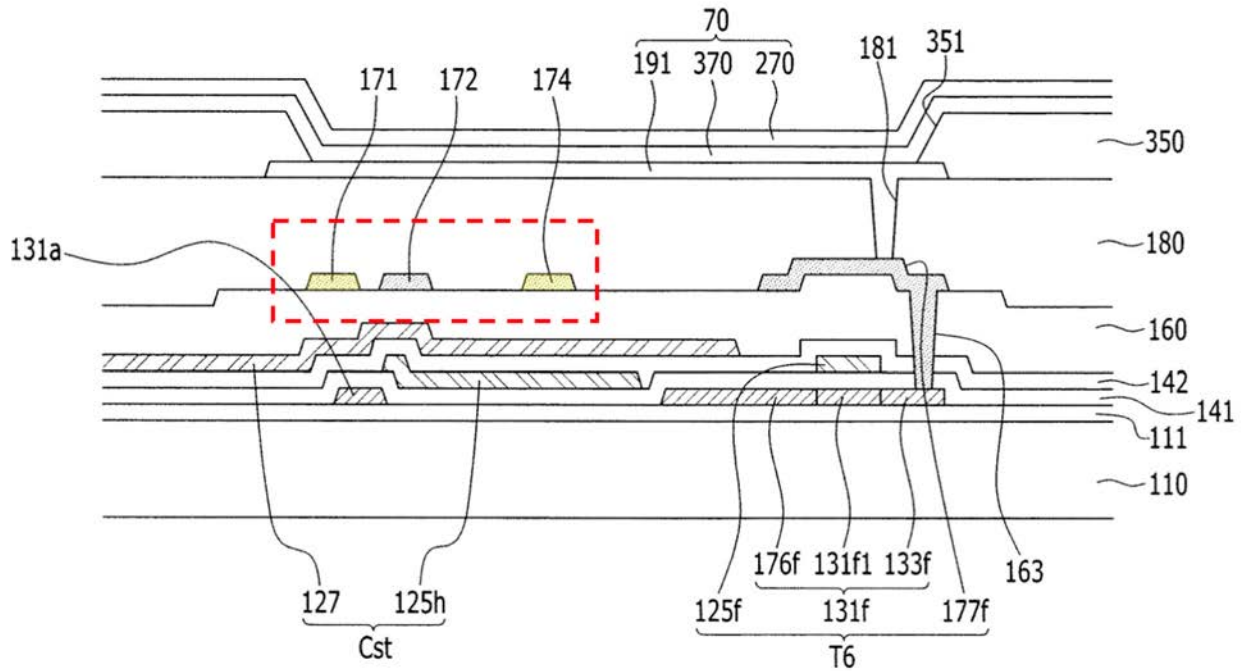


Fig. 4

7. Claim 28

a. 28[pre]-[b]:

See 1[pre]-1[b]. §IV.C.1.a-§IV.C.1.c.

b. 28[c]:

See 1[d]. §IV.C.1.e. While 1[d] recites “over the second electrode layer,” Kim-923’s data line 171 (“first signal line”) is over both lower (125h) and upper (127) capacitor plates (first and second “electrode layers”)—see Fig. 4 (annotated below).

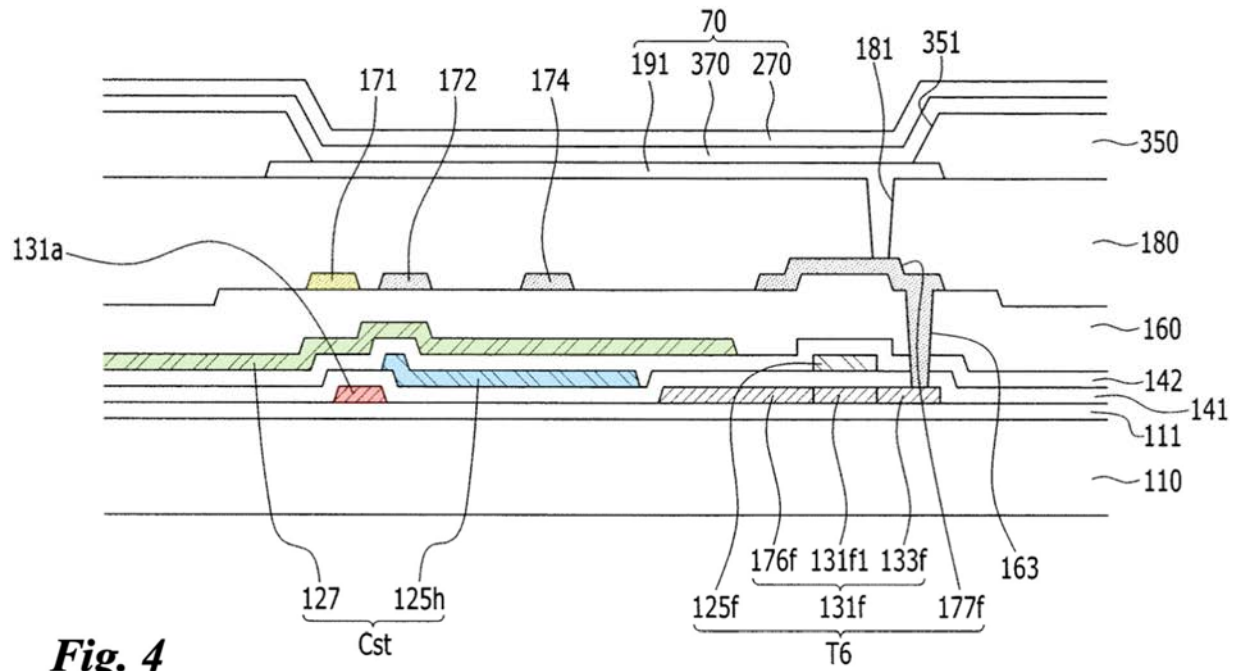


Fig. 4

c. 28[d]-[e]:

See 5[a]-[b] (§IV.E.2.b-§IV.E.2.c.), with 28[d]’s “second” TFT/semiconductor treated as 5[a]’s “third” TFT/semiconductor, and 28[e]’s “shield layer” is treated as 5[b]’s “second shield layer.”

See Cok, ¶¶430-439.

8. Claim 29

a. 29[a]-[b]:

See 11[a]-11[b]. §IV.E.3.a-§IV.E.3.b; Cok, ¶¶440-441.

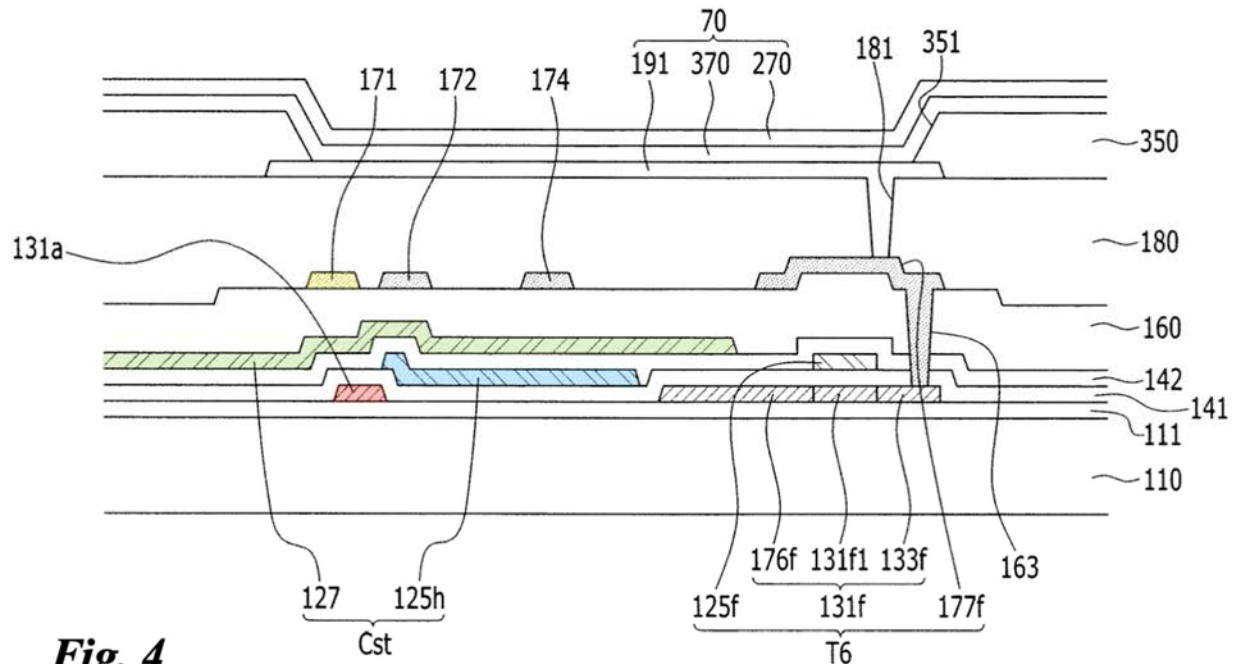
9. Claim 30

See Claim 12. §IV.E.4. Claim 30's "voltage line" and "shield layer" are treated as Claim 12's "first voltage line" and "second shield layer," respectively. Cok, ¶¶442-443.

10. Claim 31

See Claim 13 (§IV.E.5) explaining "shield layer" being part of second electrode layer.

See 28[c] (§0) and Kim-923's annotated Fig. 4 below, showing overlap of second (127) and first (125h) electrode layers. In the combination, the shield layer is part of C2's top plate, which would be in the same layer as C1's top plate (127). §§IV.E.2.c, IV.E.7.f; Cok, ¶¶444-446.



11. Claim 32

See Claim 12. §IV.E.4. Claim 32’s “voltage line” is treated as Claim 12’s “first voltage line” and mapped to line 172, connected to top plates of both C1 and C2 capacitors that are part of “second electrode layer.” §IV.E.10; Cok, ¶447.

F. Ground 3: Moon-Jeon-078 Combination Renders Obvious Claims 24-27.

1. Jeon-078

Jeon-078 in the same field as Moon, relates to OLED displays and utilizes a similar six-transistor-two-capacitor (6T2C) circuit—reproduced below for comparison. Jeon-078, ¶3; Fig. 1. Jeon-078 explains “[i]n order to express uniform luminance, a capacitance ratio of a storage capacitor and a boosting capacitor should be uniformly sustained between a plurality of pixels.” *Id.*, ¶40.

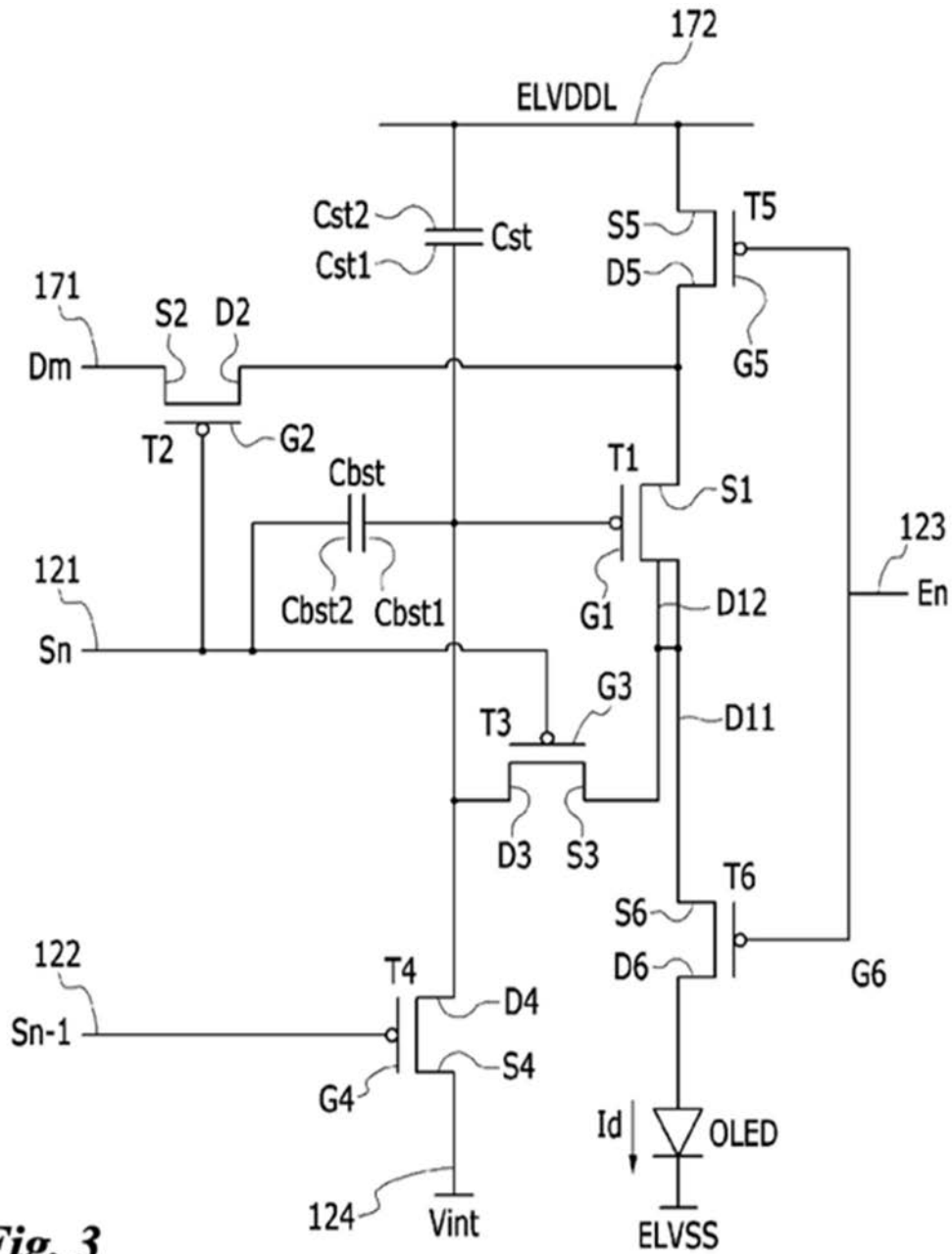
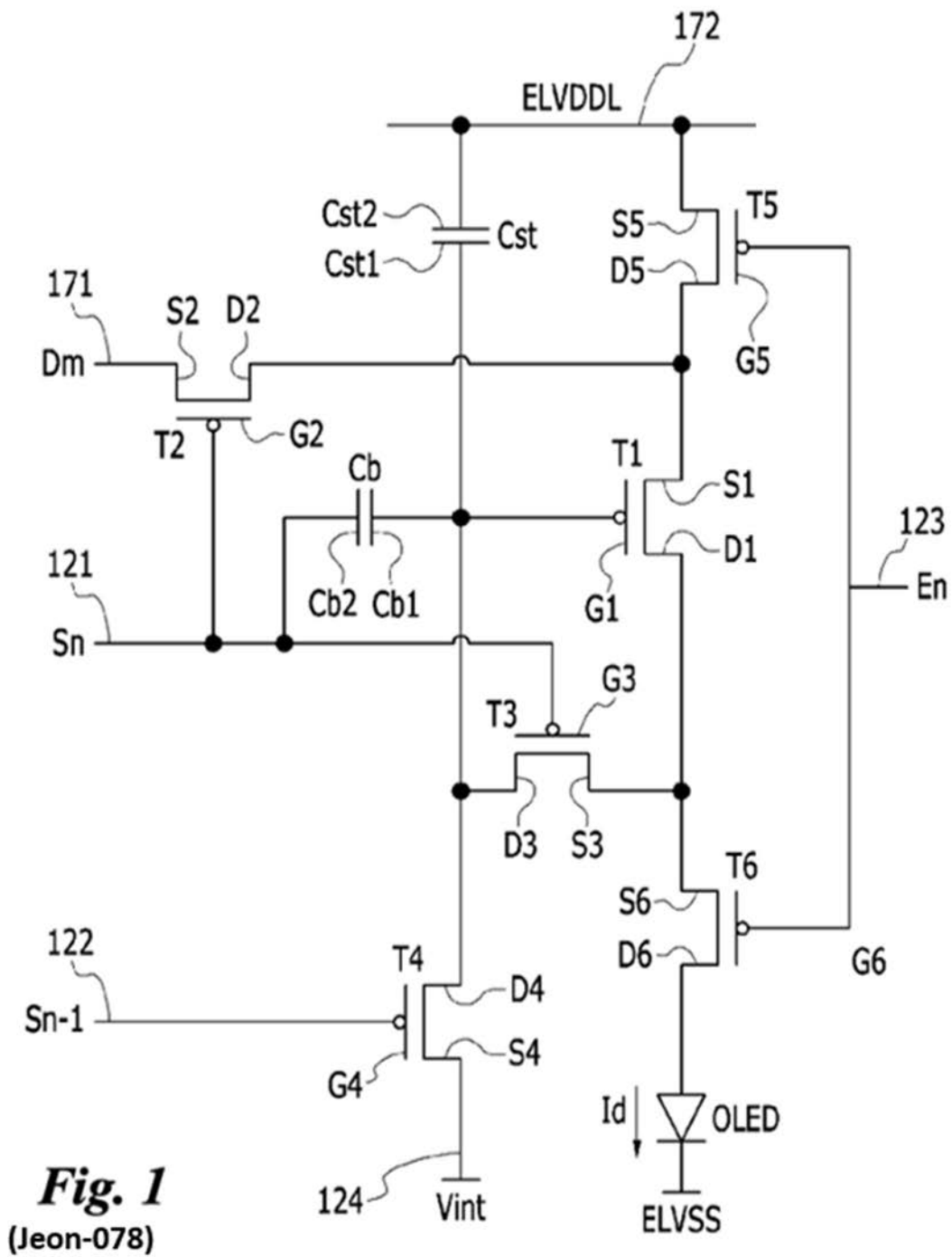


Fig. 3
(Moon)



Jeon-078 is used in this Ground to illustrate relative positioning of data (171) and initialization voltage (124) lines in an OLED pixel layout.

Jeon-078 was cited in an IDS during the original examination (EX1002, 322) but was neither discussed nor used in a rejection. Jeon-078 here is not cumulative over the original examination at least because Jeon-078 is used in combination with Moon, which was not previously in front of the Office; the Office also lacked expert testimony regarding the Moon-Jeon-078 combination.

2. Motivation to Combine

POSITAs would have been motivated to combine Moon with Jeon-078 because both references related to OLED displays utilizing a 6T2C circuit configuration (Moon, ¶¶3, 42, Fig. 3; Jeon-078, ¶3, 42, Fig. 1) and both sought to improve OLED operations. Moon, ¶26; Jeon-078, ¶9. POSITAs would have been encouraged to rely on Jeon-078's teachings to understand and implement common features that may not have been explicitly described in Moon.

POSITAs would have also been motivated to apply a known technique (identifying and implementing locations of voltage/data/connection lines in an OLED layout) to a known device ready for improvement (Moon's OLED circuit) to yield predictable results (placement of voltage/data/connection lines). POSITAs would have had a reasonable expectation of success, because placement of traces for TFT voltage/signal lines was well-known by 2014, as evident by Jeon-078 and other known references (Cok, ¶¶452, 50, citing EX1012, EX1029-1031), and such modifications were well within POSITAs skillset. *Id.*, ¶¶450-453.

Additional motivations are described below.

3. Claim 24

a. 24[pre]:

Moon describes an OLED display apparatus. Moon, ¶¶3, 12, 42.

b. 24[a]:

Moon's T1 is "a first" TFT over a "first semiconductor:" "[o]ne embodiment provides a **thin film transistor including: a semiconductor** formed on a substrate."

Moon, ¶8; *see also id.*, ¶¶43, 45, Fig. 3 (annotated below).

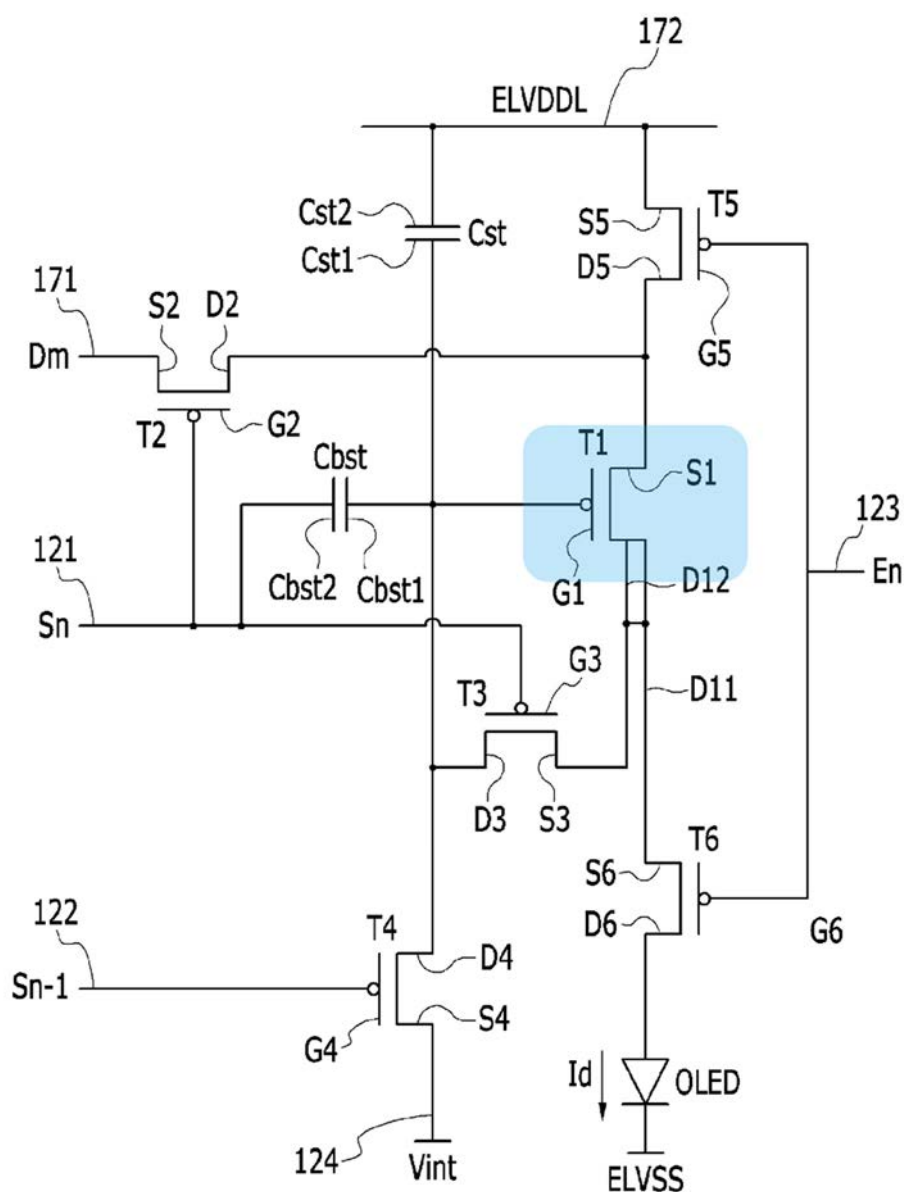


Fig. 3

c. 24[b]:

Moon discloses “a first electrode layer” as the layer containing gate electrode (G1) of T1. Moon, ¶45. Moon’s “gate electrode G1 of the driving transistor T1 overlaps the semiconductor 151” *Id.*, ¶75. Moon explains, and POSITAs would

have known, an area overlapped by TFT's gate electrode is TFT's channel area. *Id.*, ¶35, Fig. 4 (annotated below).

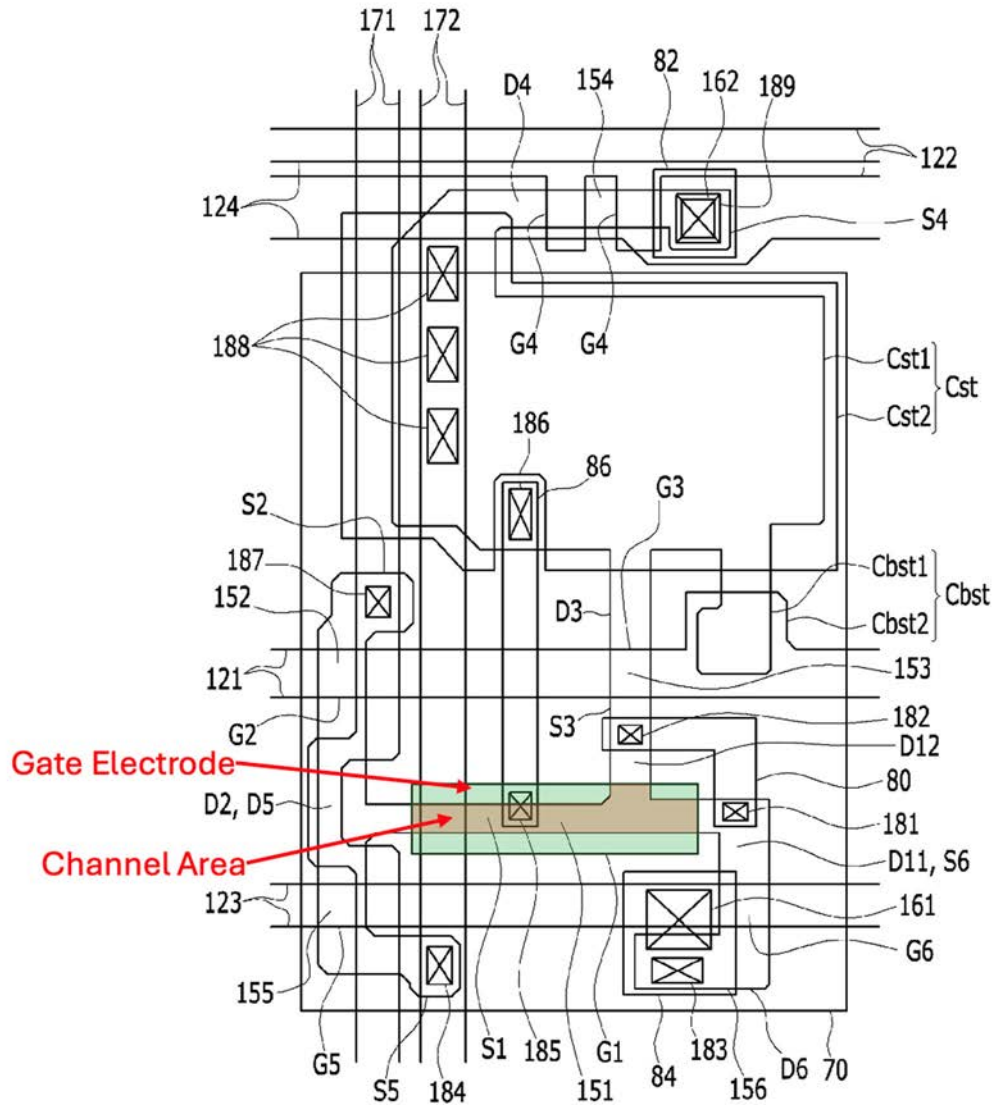


Fig. 4

d. 24[c]:

Moon teaches a “first signal line” as data line 171. Moon, ¶43; see also *id.*, ¶91, Figs. 3 and 4, showing data line 171. Moon is not explicit that data line 171

(“first signal line”) is over the first electrode layer, but Jeon-078 is. Jeon-078, ¶¶42, 44, Fig. 1.

Jeon-078’s explains: **“On the interlayer insulating layer 160, a data wire including a data line 171 ... [is] formed.”** *Id.*, ¶94, Fig. 4 (annotated below) showing data line 171 in a layer above gate electrodes (125f) and capacitor electrodes (128, 129).

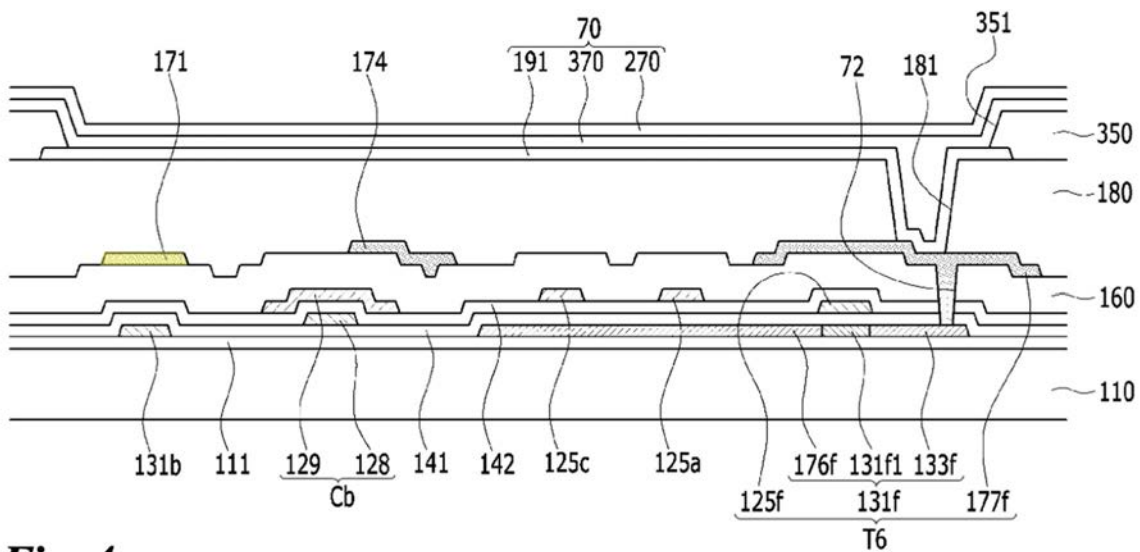


Fig. 4

To the extent Moon did not explicitly disclose relative positioning of voltage/data lines, POSITAs, based on Jeon-078, would have understood and found it obvious to position data line 171 (“first signal line”) over the “first electrode layer” that included gate electrode of T1. This would have been a routine task and a known way to position data line 171, as described in Jeon-078 and other references at the

time of alleged invention in 2014. *See e.g.*, Kim-923, Fig. 4; Kim-584, Fig. 9; Cok, ¶446.

e. 24[d]:

Moon's T4 is a "second" TFT. Moon, ¶54, Fig. 3 (annotated below), showing T4's drain (D4) ("one end of second semiconductor") is connected (red, A) to T1's gate (G1) that resides in "the first electrode layer" (*see* 24[b]), and T4's source (S4) ("other end of the second semiconductor") is connected (blue, B) to initialization power line 124 ("a voltage line").

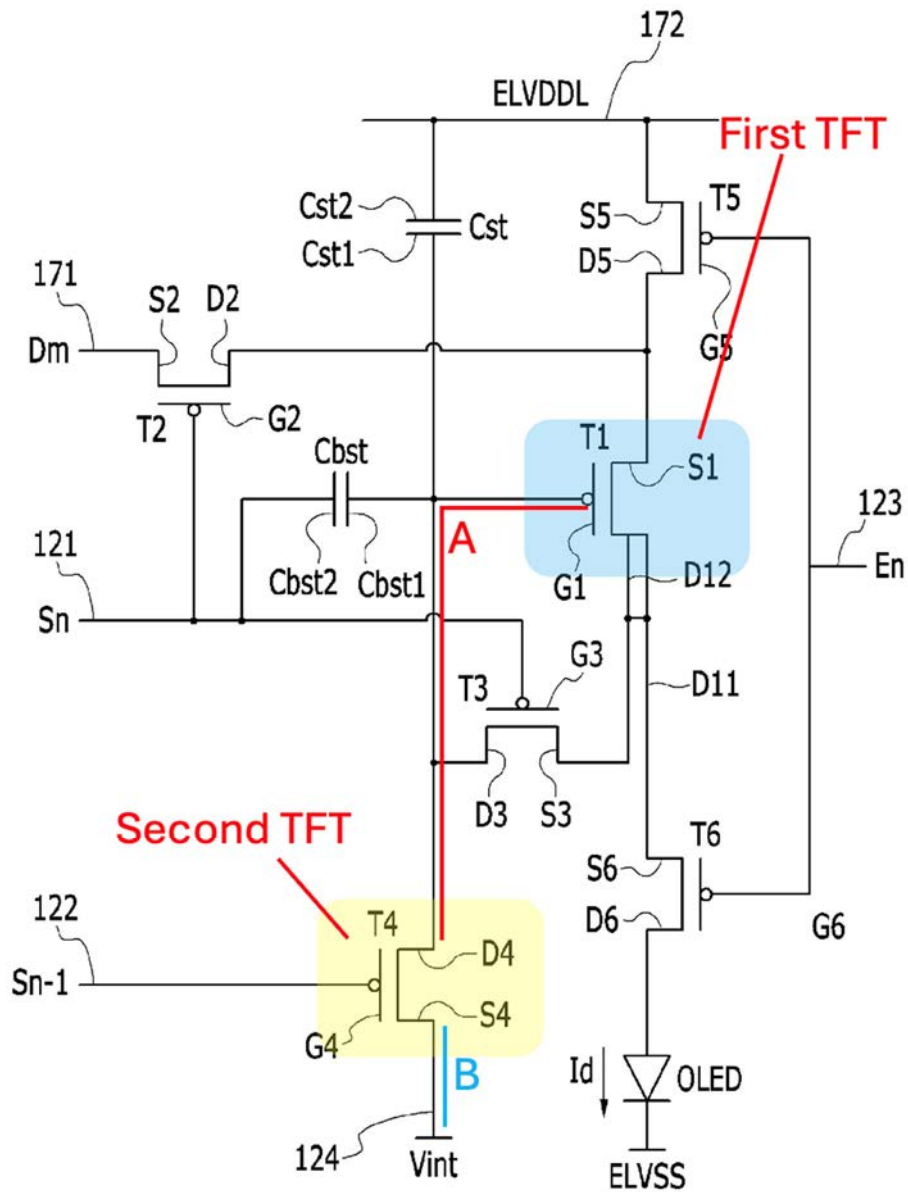


Fig. 3

Moon's Fig. 4 (annotated below) illustrates semiconductor region (154) for D4-to-G1 connection (green arrow) (Moon, ¶¶72, 76, 79), and S4-to-Vint connection through contact holes 162, 189 and metal pattern 82 (blue circle). *Id.*, ¶79.

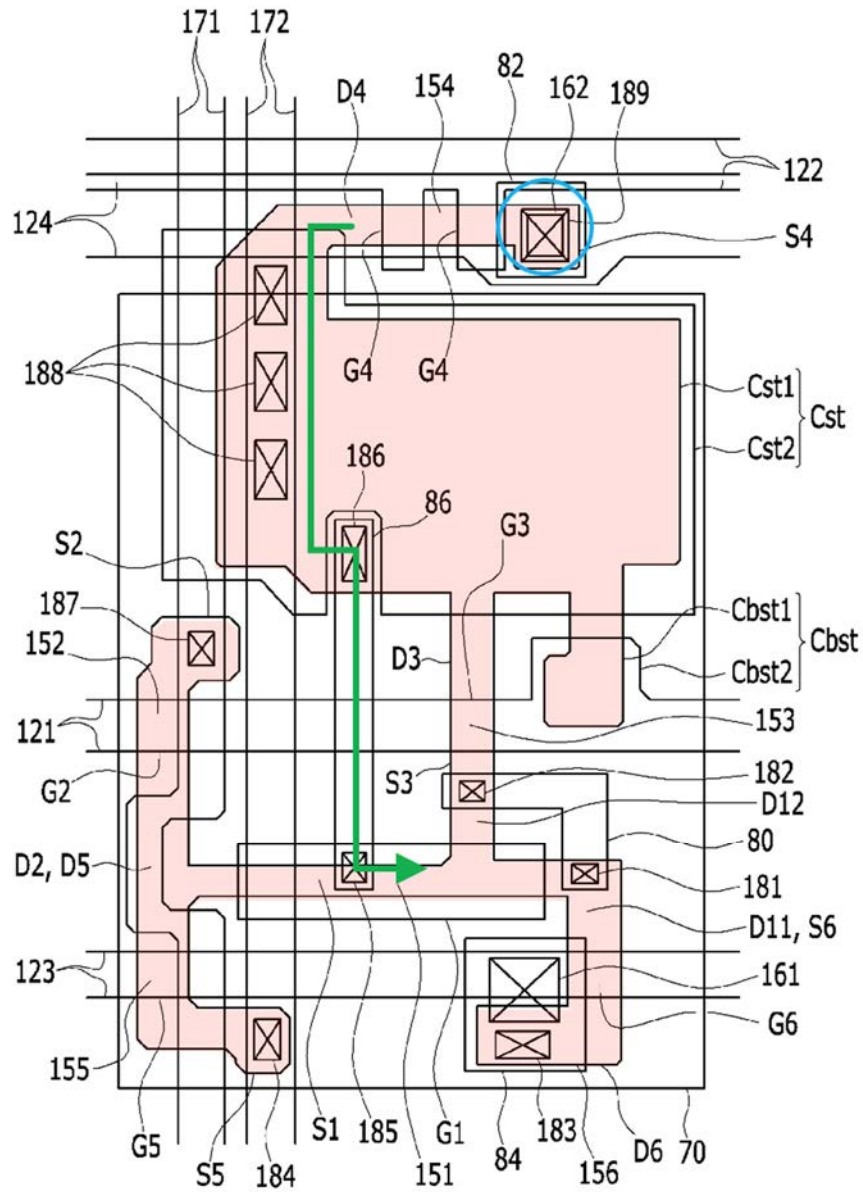


Fig. 4

f. 24[e]:

Moon shows “a shield layer” as initialization power line 124—see Fig. 4 below (green)—overlapping a part between the first channel and second channel areas of T4’s semiconductor (“second semiconductor”). T4 has two gate electrodes

(red dashed circles); the semiconductor below those gate electrodes forms the “first” and “second” channel regions. See §IV.D.3.d.

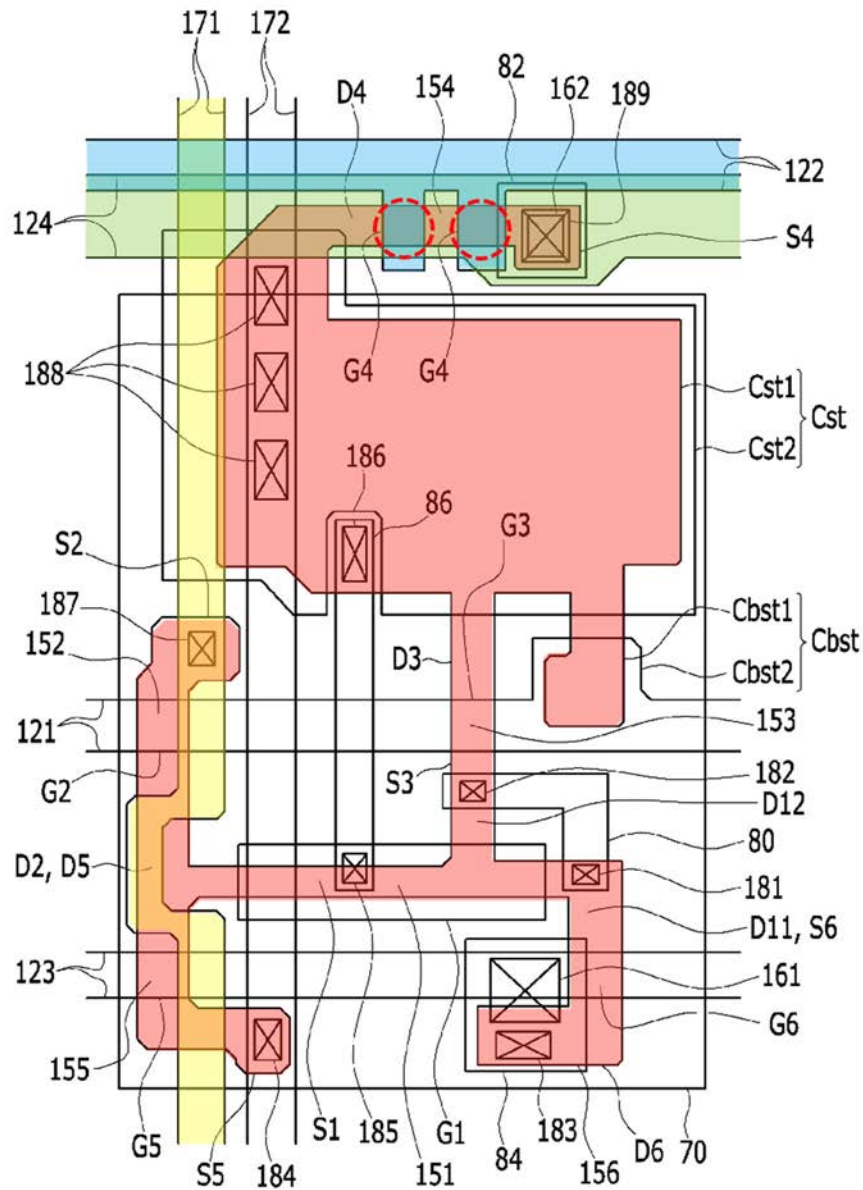


Fig. 4

While Moon is not explicit regarding relative vertical positioning of initialization power (124) and data (171) lines, Jeon-078 explains initialization

power line 124 (referred to as “initialization voltage line 124”) is in a layer below data line 171 and above T4’s semiconductor.

Notably, Jeon-078’s initializing voltage line 124 is formed in the same layer as top storage capacitor plate 127 and top boost capacitor plate 129 (Jeon-078, ¶67), Fig. 4 (annotated below) shows top plate 129 is positioned over gate insulating layers 141/142, which are formed over semiconductor layer 131. *Id.*, ¶¶79, 89, 91. Therefore, Jeon-078’s initialization voltage line 124 is in a layer above the semiconductor of T4 but below the data line 171.

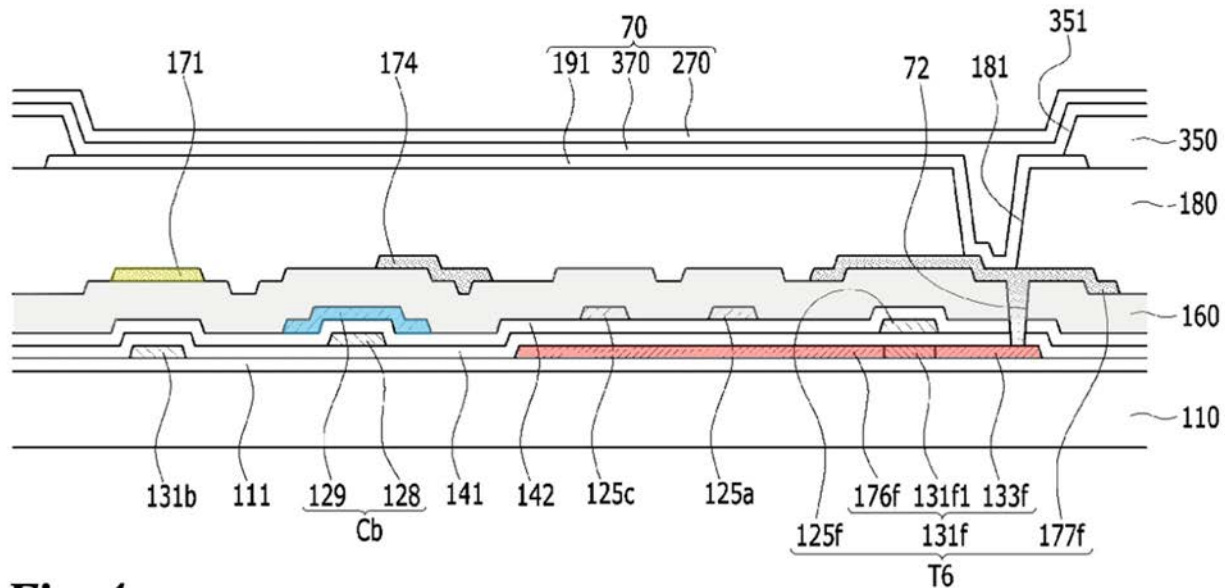


Fig. 4

In the combination, POSITAs would have been guided by Jeon-078 and would position initialization voltage line 124 below data line 171 but above the semiconductor of T4. Such an arrangement would have been a routine, predictable

and known way to position data and voltage lines, as described in Jeon-078 and other references in 2014. Cok, ¶¶474-475; *see also* §§IV.F.2.

Voltage line 124 in the Moon-Jeon-078 combination would have been a shield layer for the same reasons discussed in §IV.D.3.d, consistent with '015 patent.

See also Cok, ¶¶454-477.

4. Claim 25

a. 25[a]:

See 24[e]. §IV.F.3.f. Moon's T4 gate electrodes (G4) (red circles) are formed where previous scan line 122 (blue) overlaps the semiconductor layer. *Id.*, ¶73: "...the previous scan line 122 has the gate electrode G4 overlapping the semiconductor 154 of the initialization transistor T4." Both gates are in the same layer because they are part of the same previous scan line 122.

b. 25[b]:

Moon's Fig. 4 (annotated below) shows gate electrodes (G4) are part of previous scan line 122 ("second signal line," blue), which is substantially perpendicular to, and thus "crossing," data line 171 ("first signal line," yellow).

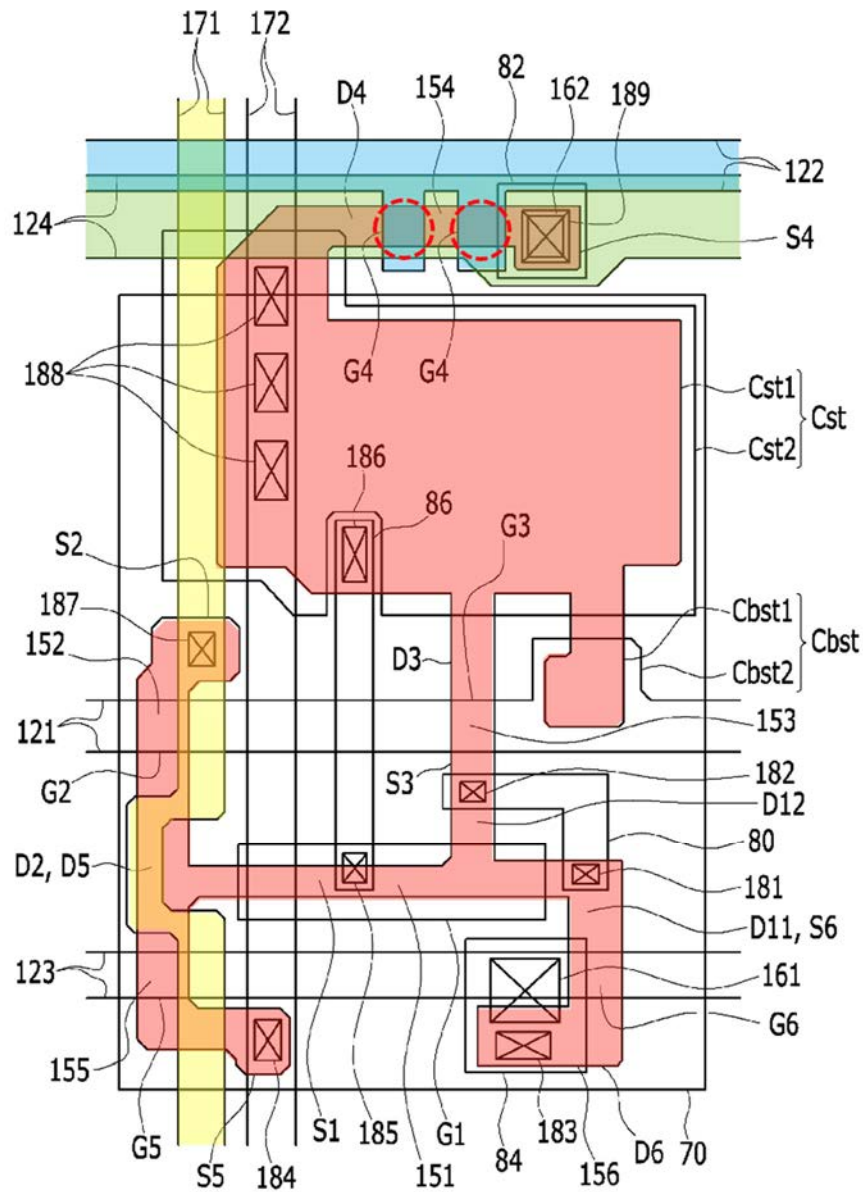


Fig. 4

POSITAs would have found it obvious that T4's gate electrodes (G4) are in the same layer as T1's gate electrode (G1) because the semiconductors that form T1 and T4 were in the same layer, as the continuous red region in Moon's annotated Fig. 4 shows, and the gate electrodes would be on the same layer overlapping the semiconductor. Cok, ¶¶478-485.

5. Claim 26

See 24[e]. §IV.F.3.f.

6. Claim 27

Moon's Fig. 3 shows (annotated below) T4's drain (D4) ("one end of the second semiconductor") is connected (line A) to T1's gate (G1) that is part of the "first electrode layer." *See* §IV.F.3.c.

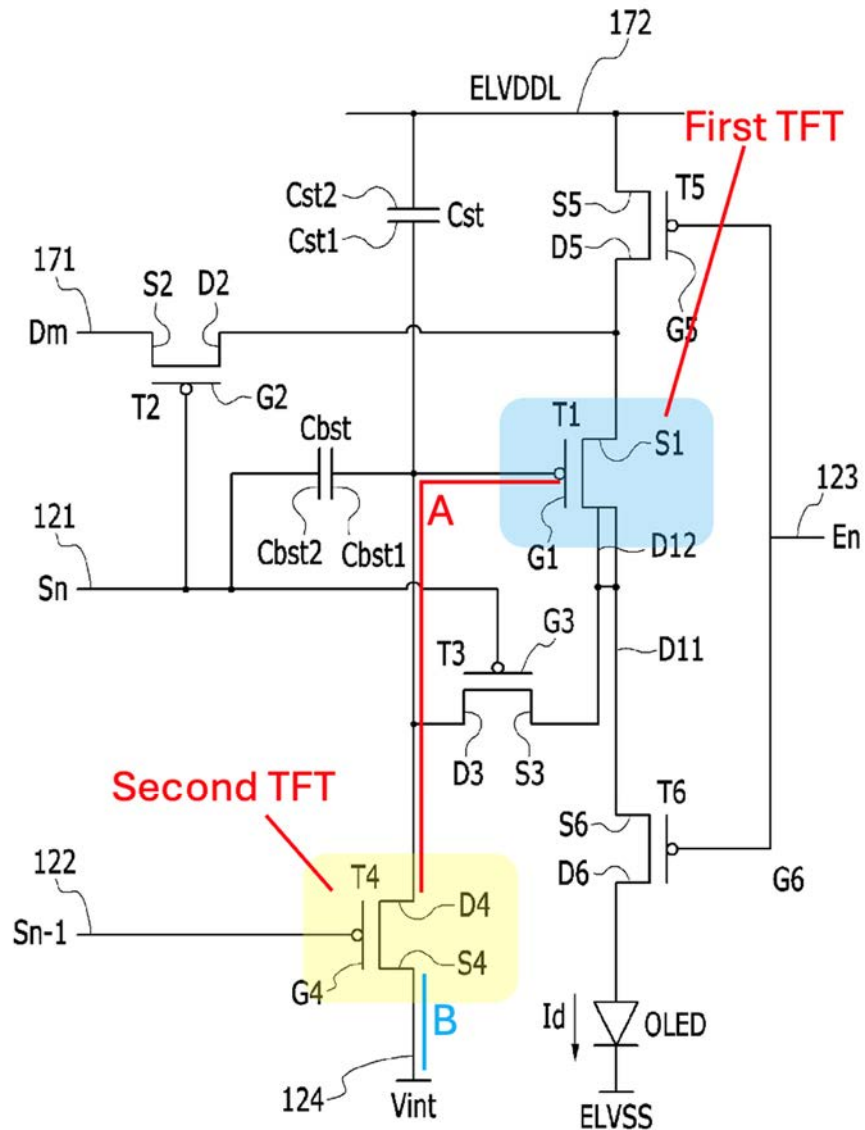
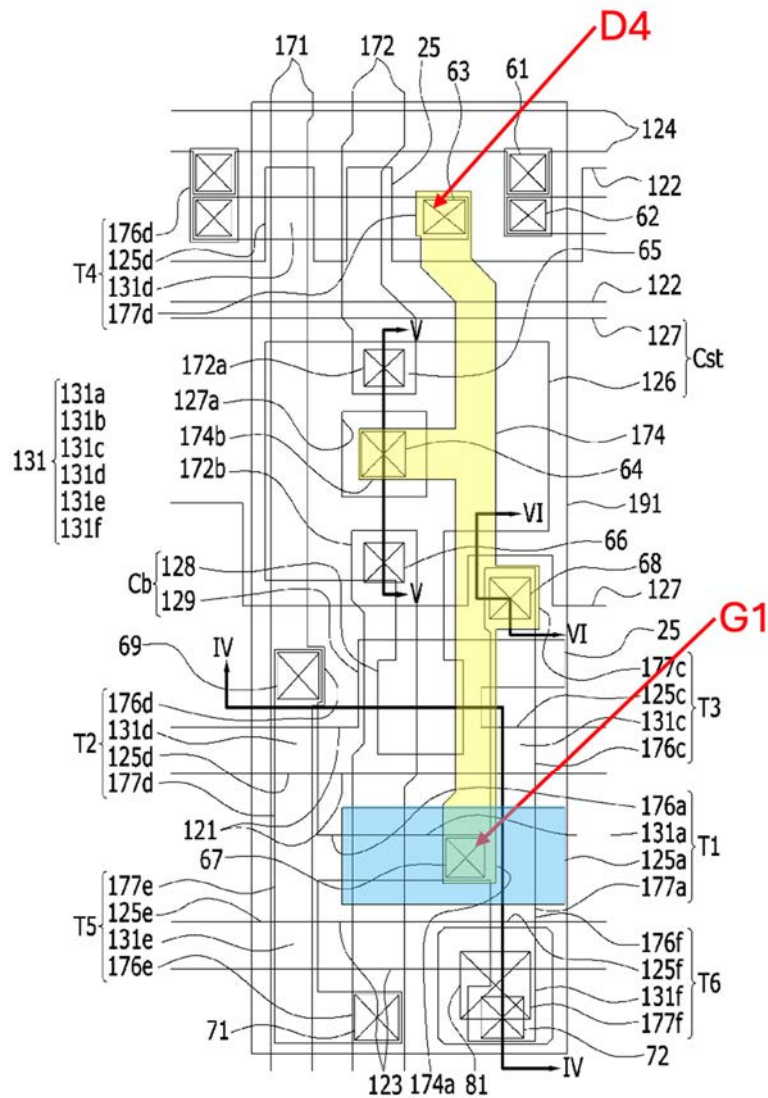


Fig. 3

Moon's G1-to-D4 connectivity is implemented by connection member 86 and contact holes 185, 186, connecting G1 to lower capacitor plate Cst1, which is connected to D4 region on the semiconductor. *Id.*, ¶76. Moon does not explicitly disclose the connecting line is in the same layer as data line 171 ("first signal line"). But Jeon-078 discloses a similar connection member 174 connecting T4's drain (D4)

to T1's gate (G1) (blue)—see annotated Fig. 3 below. Jeon-078, ¶¶70, 78, Fig. 3. Jeon-078 also explains “**connection member 174 is formed in the same layer to be parallel to the driving voltage line 172.**” *Id.*, ¶70.



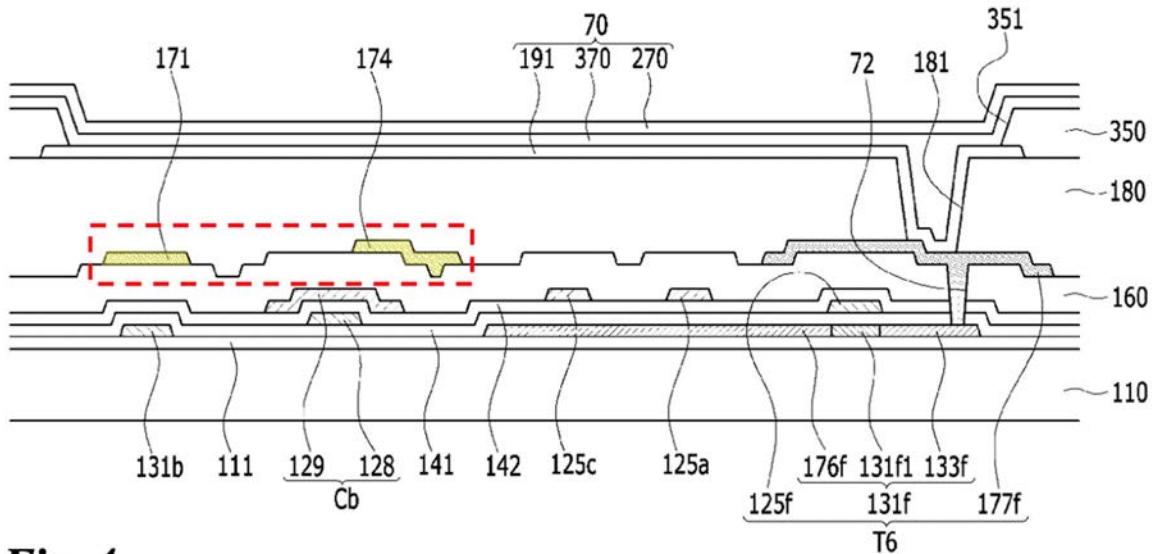


Fig. 4

POSITAs would have found it obvious to place the connection member and data line 171 in the Moon-Jeon-078 combination in the same layer because they were substantially parallel to one another, and placing them in the same layer provided for simpler circuit design and manufacturing. Using a metal connector and associated contact holes to connect two elements in an OLED circuit layout was a routine task with a predictable outcome, placement of the connection line in the same layer as signal line 171 was taught by Jeon-078, and its implementation would have been well within POSITAs skillset. Cok, ¶¶488-494.

G. Ground 4A: Masao Renders Obvious Claims 1-2, 8-10, 33.

Masao relates to an active matrix electro-optical device using TFTs. Masao, ¶2. Masao's active matrix electro-optical device uses TFTs, and provides a shield to

mitigate electrical noise from signal lines, is directly related to, and is analogous art to, the claims and description of '015 patent. Notably, the Challenged Claims do not recite an OLED device (EX1001, 17:12-20-57) and the preamble of each independent claim generally recites: “A display apparatus comprising.” *Id.* Furthermore, the '015 specification explains its embodiments are “**not limited to an organic light-emitting display apparatus**. An image having high quality may be displayed as long as a display apparatus including a TFT and a data line in a (sub) pixel has a shield layer in the same or similar manner described above.” *Id.*, 16:63-67.

Accordingly, while Masao does not specifically describe an OLED display, POSITAs would have understood that OLED displays and LCD displays have many similarities, utilize TFTs, and encounter many similar challenges. Cok, ¶¶496-497.

1. Claim 1

a. 1[pre]:

Masao discloses a display apparatus “capable of displaying high-quality images” (Masao, ¶7) including an “electro-optical devices such as liquid crystal devices.” *Id.*, ¶1, 50.

b. 1[a]:

Masao's circuit includes a first TFT 30.¹⁸ Masao, ¶51, Fig. 1.

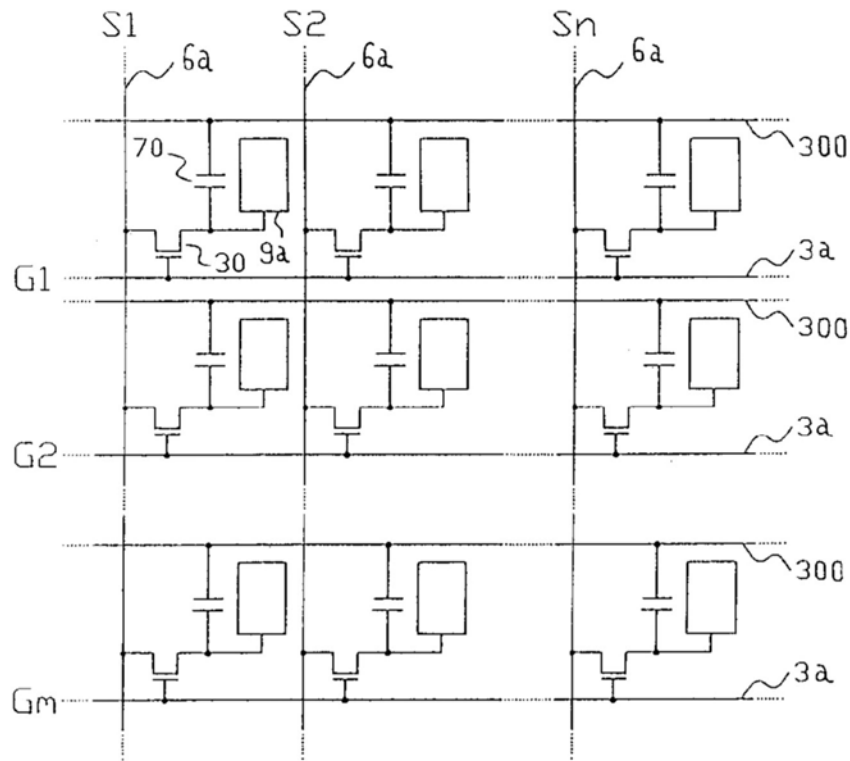


Fig. 1

TFT 30 includes a source, a channel, and a drain area in semiconductor layer 1a (“first semiconductor layer”) (see Masao’s Fig. 3 partially reproduced below), having low concentration source (1b), source (1d), high concentration drain (1e), and drain (1c) regions, with channel region (1a’) therebetween. *Id.*, ¶69, Fig. 3.

¹⁸ Masao’s Fig. 1 shows nine identical circuits, each including a TFT 30, a capacitor 70 and a pixel electrode 9a. Only one of the identical circuits is used in this Ground.

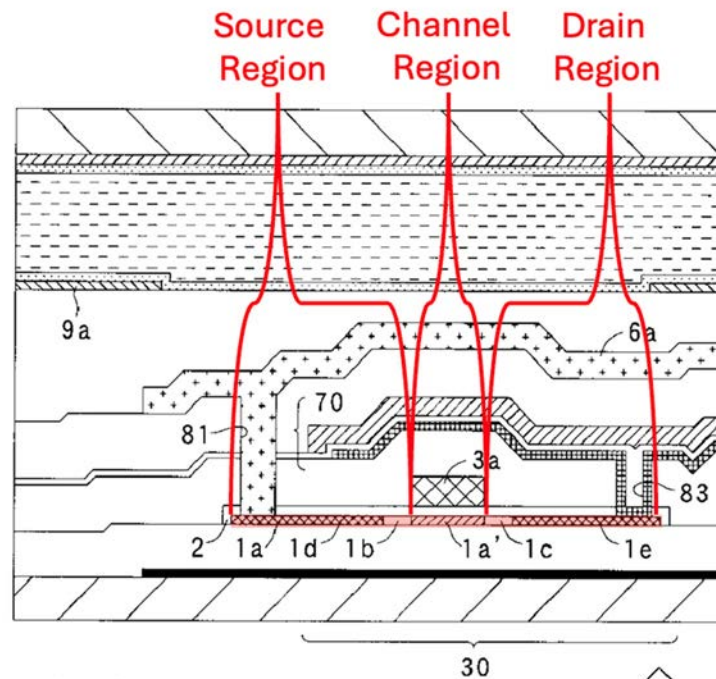


Fig. 3

c. 1[b]:

Element 1[b] outlines the requirements of an “electrode layer,” which are satisfied by Masao under three different mappings.¹⁹

Mapping #1. Annotated Fig. 3 below shows a first mapping where the first electrode layer (blue) is a layer that includes scan line 3a (gate electrode), relay layer 71 (lower capacitor electrode), and at least conductive portion connecting TFT’s drain to relay layer 71.

¹⁹ Unless otherwise noted, Challenged Claims are rendered obvious under all mappings.

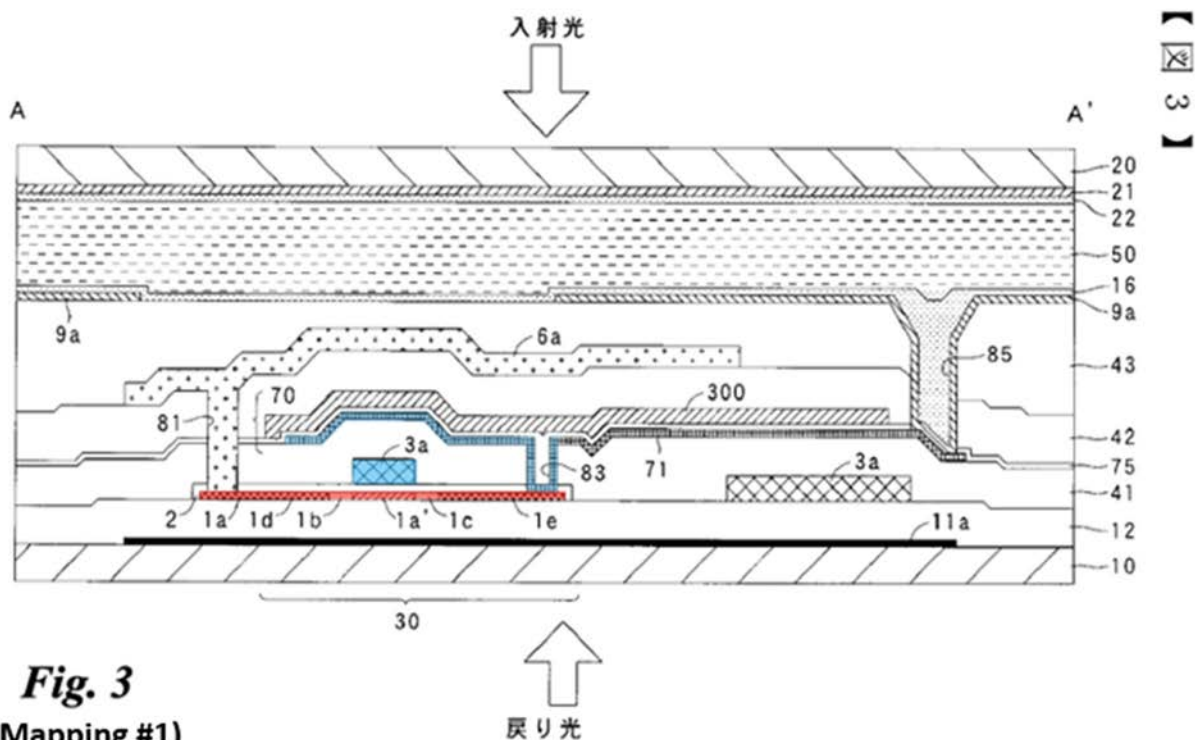


Fig. 3
(Mapping #1)

Mapping #1 is an electrode layer because it includes one or more electrodes, Notably, Masao's relay layer 171 and scan line 3a form a capacitor electrode (Masao, ¶54) and a gate electrode (*id.*, ¶53), respectively. And at least part of contact hole 83 that connects to the high concentration drain region is drain electrode that is also connected to relay layer 171. *Id.*, ¶70.

Mapping #2. Annotated Fig. 3 below shows a second mapping (blue) that includes relay layer 71 (e.g., bottom capacitor electrode). Masao, ¶54.

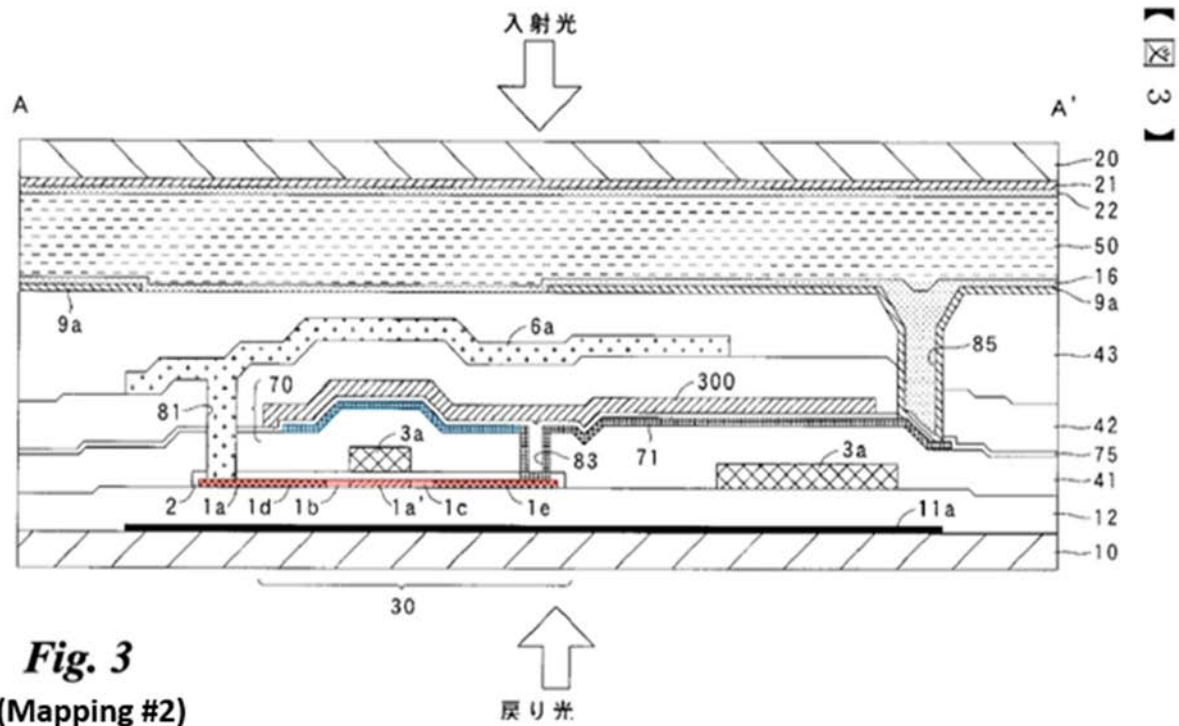
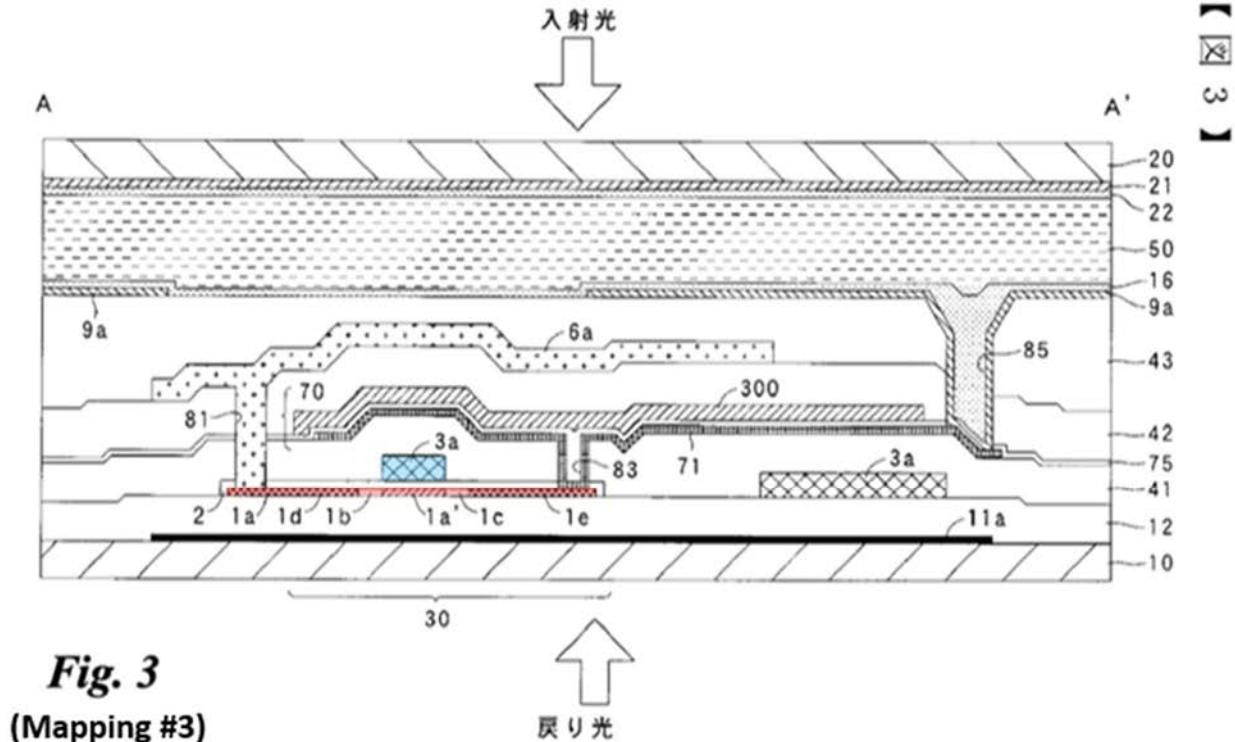


Fig. 3
(Mapping #2)

Mapping #3. Annotated Fig. 3 below shows a third mapping as a layer that includes scan line 3a. Masao, ¶53.



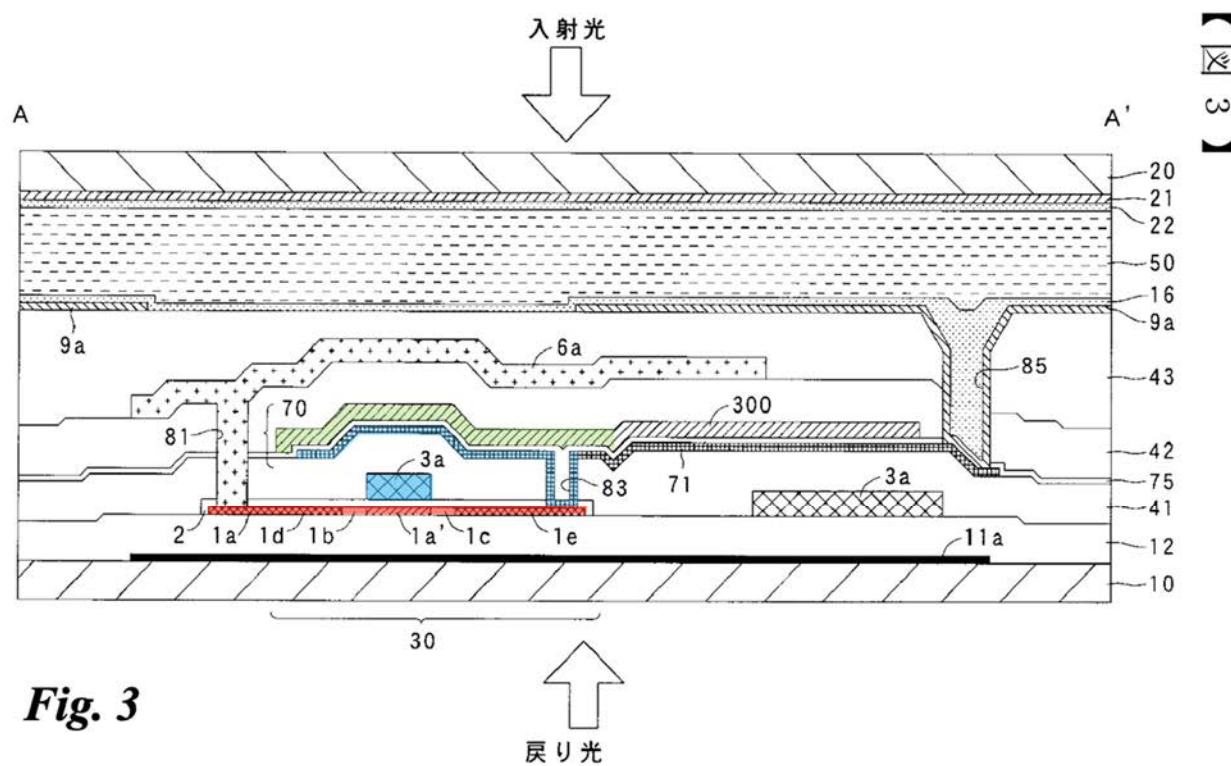
Additionally, the extent of “first electrode layer” in all three mappings is not limited to an individual pixel of Masao, but the “layer” extends to neighboring pixels that include electrodes of neighboring pixels.

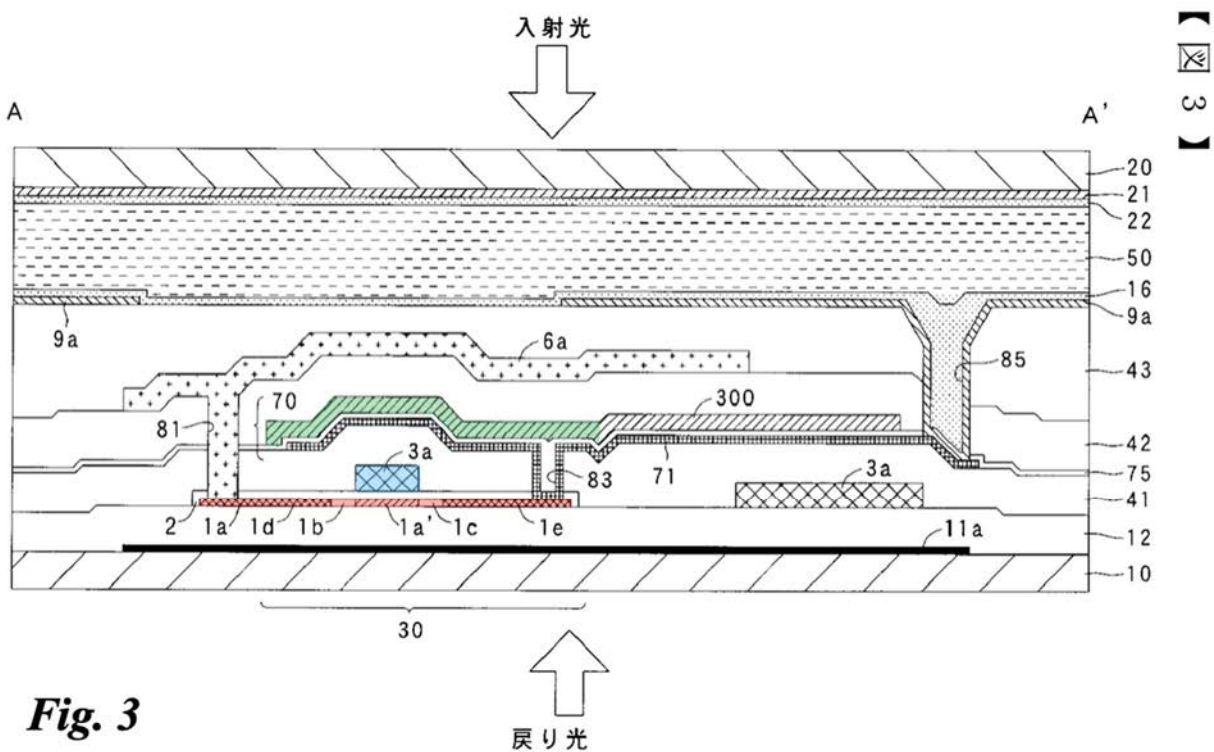
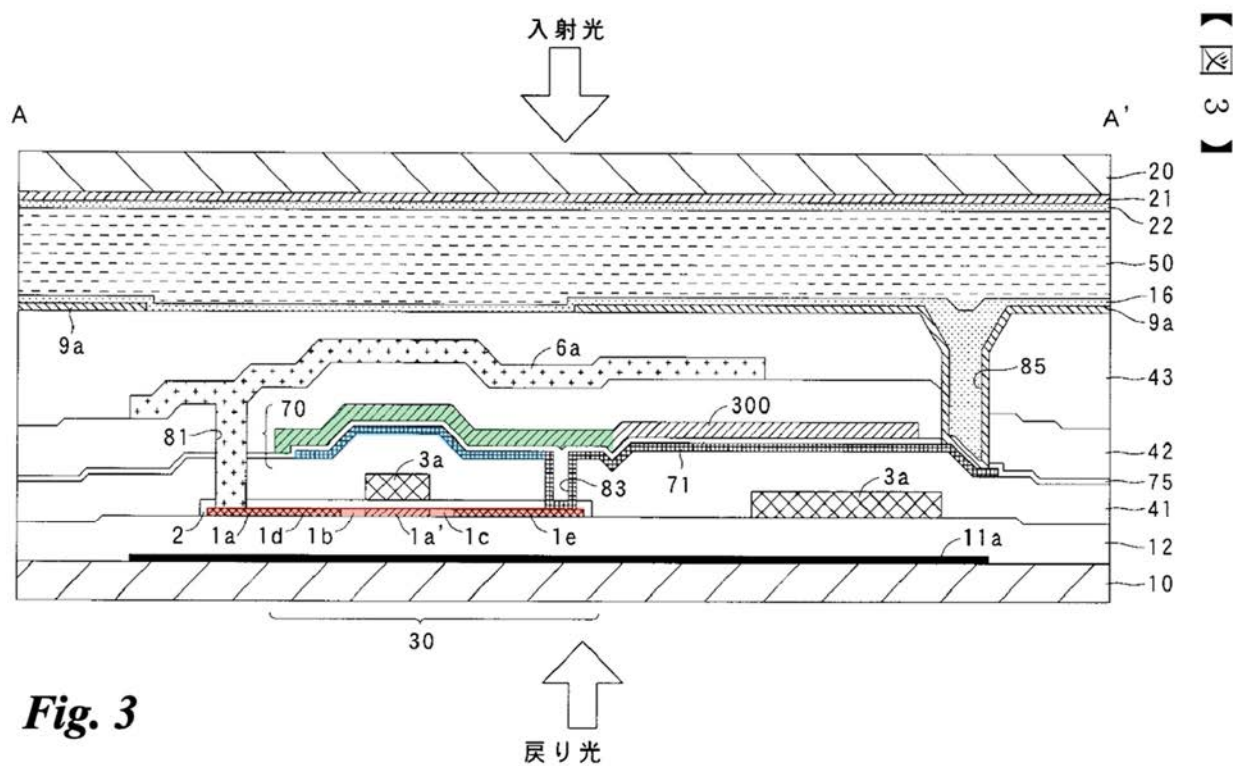
Cok, ¶¶507-514.

d. 1[c]:

Masao discloses “a second electrode layer” as the layer that includes capacitance line 300 (or part thereof): “one part of a capacitance line 300 serving as a constant potential-side capacitance electrode.” Masao, ¶54, *see also id.*, ¶71. Annotated Figs. 3 below show capacitance line 300 (“second electrode layer,” green)

overlaps the “first electrode layer” (blue) under Mapping #1, #2 and #3. Cok,
¶¶5515-518.





e. 1[d]:

Masao's line 6a is "a first signal line." See annotated Figs. 2 and 3 below, showing data line 6a (yellow) in a layer over capacitance line 300 ("second electrode layer").²⁰ Masao ¶93.

²⁰ Masao's Fig. 2 shows multiple pixels, but this Ground relies on one pixel and associated circuit. To avoid clutter, sometimes components of a neighboring pixel are annotated to identify certain elements.

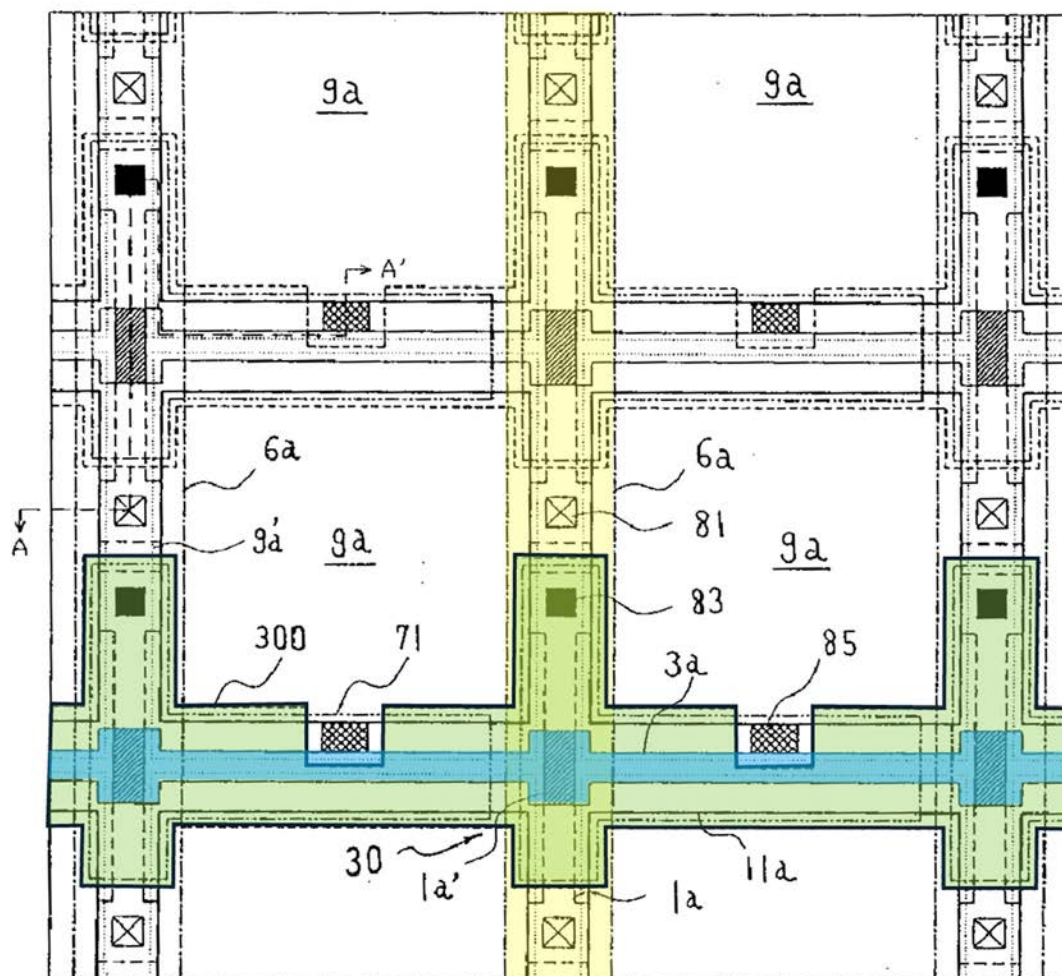
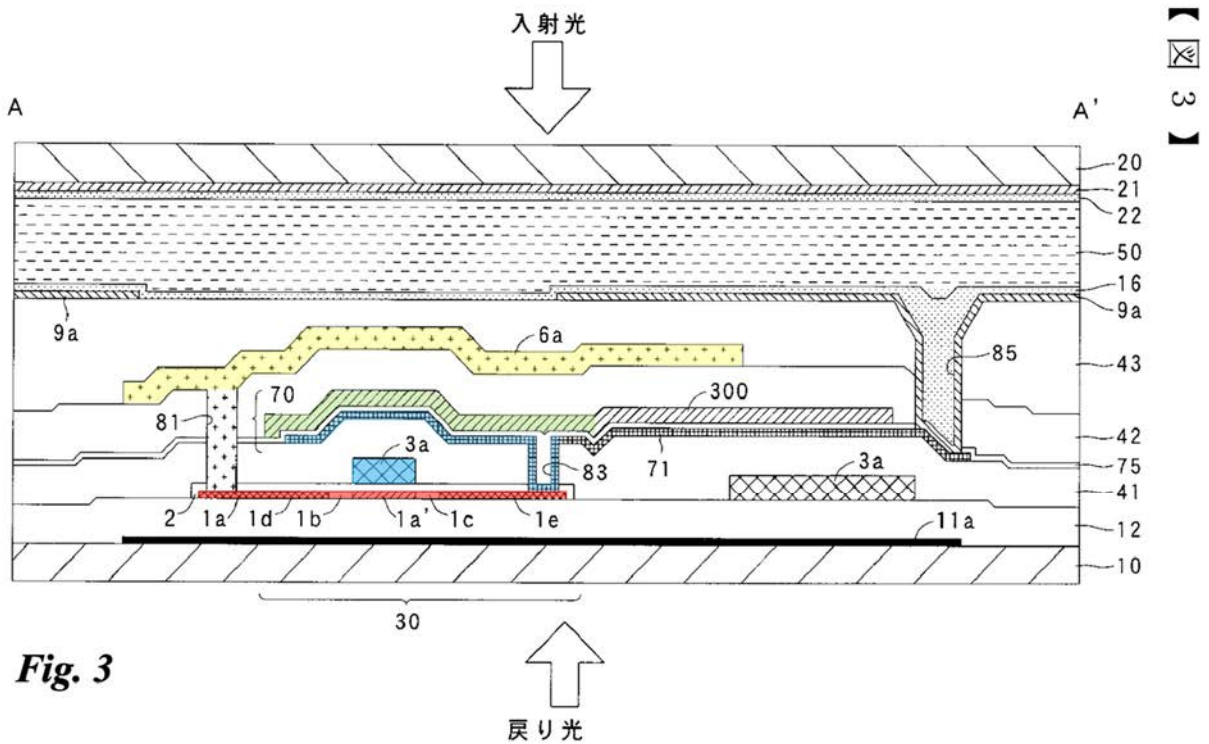


Fig. 2



f. 1[e]:

Masao's capacitance line 300 (or a part thereof) is "a first shield layer"—green annotation in Figs. 2 and 3 (below).²¹

²¹ The interpretation of shield layer remains the same for Mappings #2 and #3 of the first electrode layer.

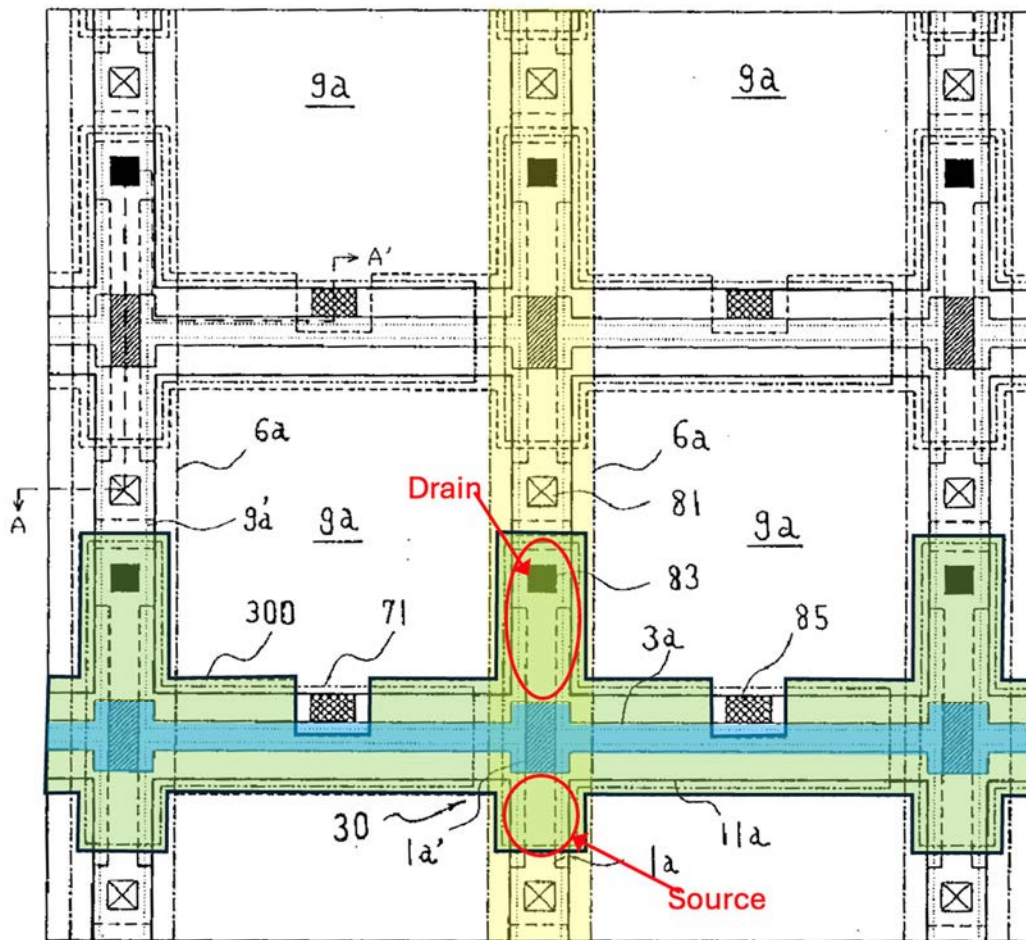


Fig. 2

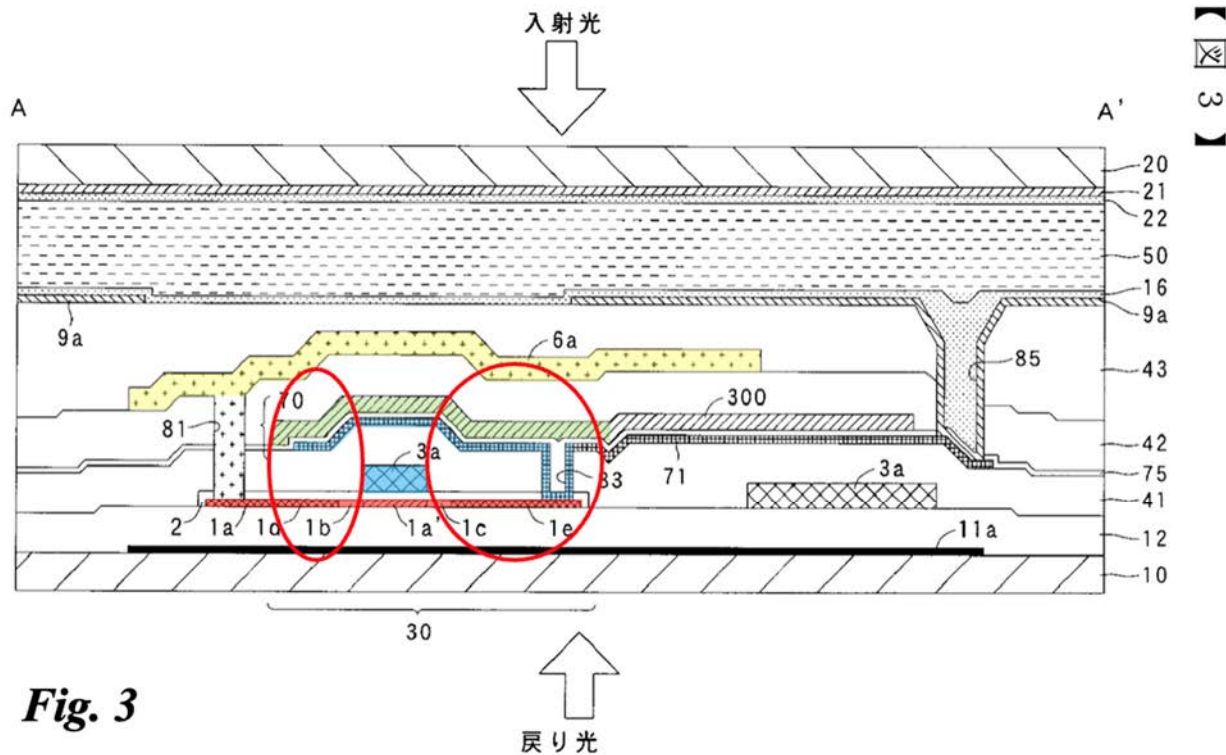


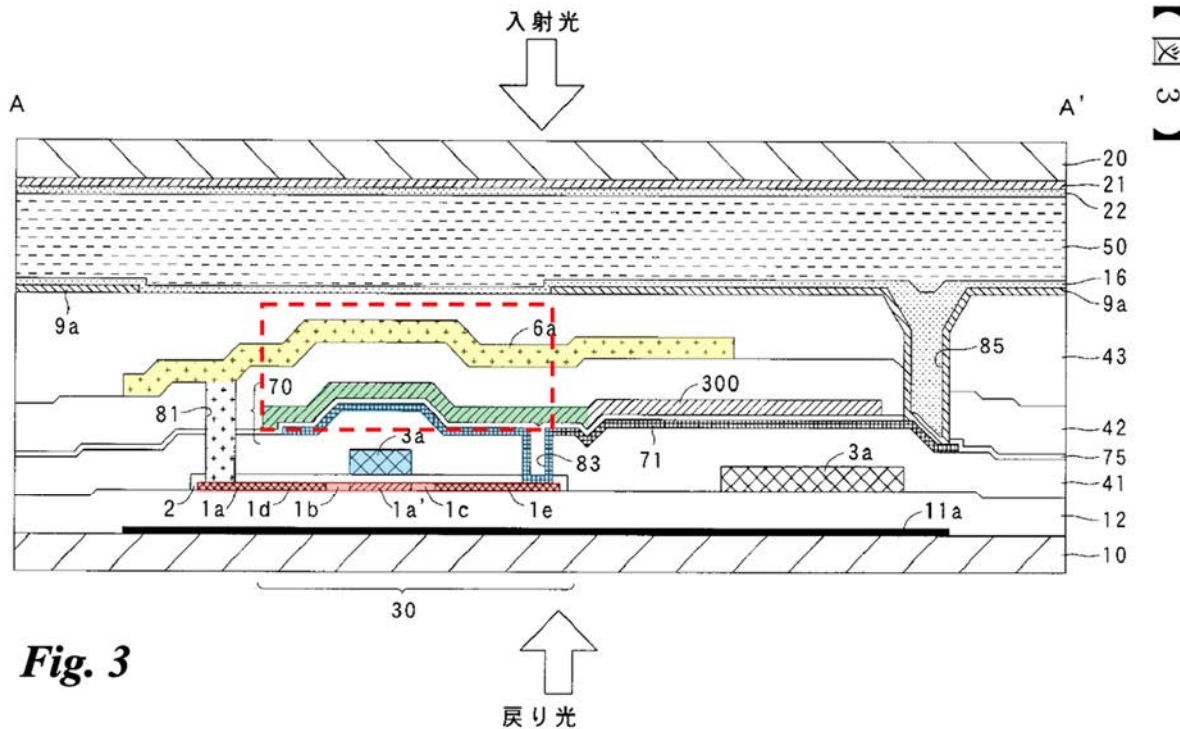
Fig. 3 shows a portion of capacitor line 300 (“first shield layer”) is in a layer between data line 6a (“first signal line”) and semiconductor layer 1a (“first semiconductor”) and overlaps a part of first semiconductor’s source area (1d/1b) and drain area (1c/1e). Similarly, annotated Fig. 2 (above) shows capacitor line 300 (green) overlaps a portion of TFT’s source and drain areas. *Id.*

POSITAs would have found it obvious that Masao’s capacitance line 300 is a “shield” because it was supplied with a constant voltage (Masao, ¶51; *see also id.*, ¶54 and Fig. 1, illustrating line 300 is connected to a voltage line VSSY), and shielded the TFT from noise associated with signal line 6a. Therefore, POSITAs

would have understood that it was a shield consistent with '015 patent. See §IV.A.1.f. Cok, ¶¶498-525.

2. Claim 2

Masao's shield is a portion of capacitance line 300, which forms a capacitor electrode ("second electrode layer"). §§IV.G.1.d and IV.G.1.f. Annotated Fig. 3 (below) shows (red dashed box) Masao's capacitance line 300 ("first shield layer," green) overlaps part of data line 6a ("first signal line," yellow).



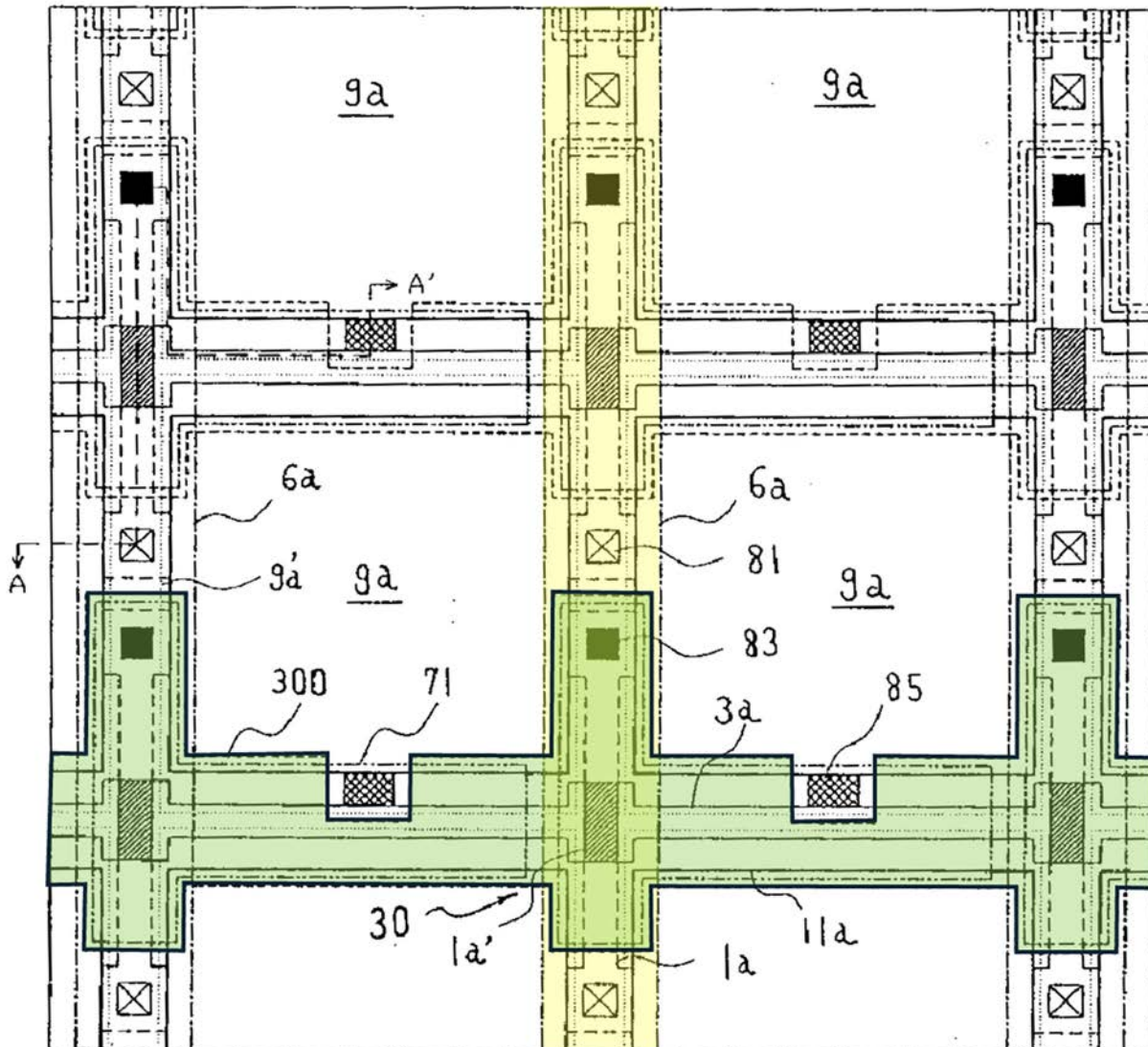


Fig. 2

3. Claim 8:

a. 8[pre]:

Masao's Data line 6a ("first signal line," yellow) extends in a first direction.

See annotated Fig. 2 (below).

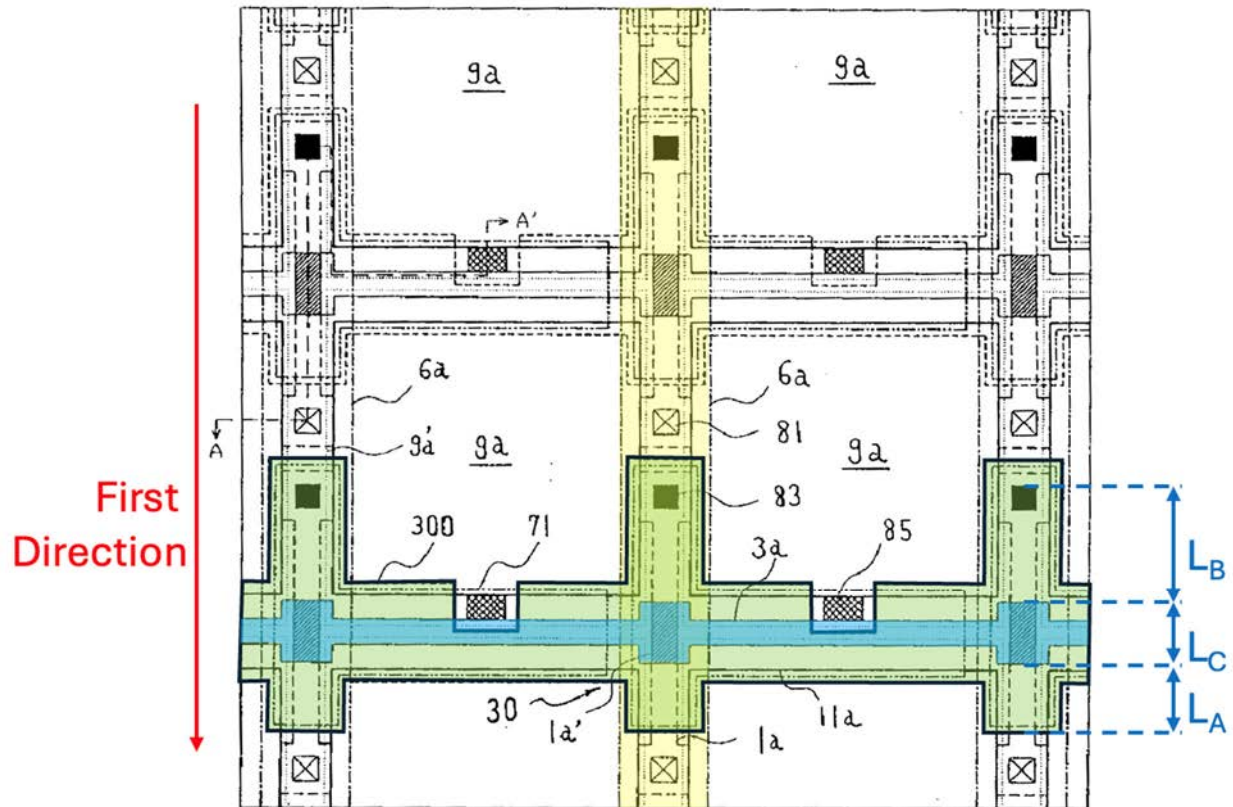


Fig. 2

b. 8[a]:

Annotated Fig. 2 illustrates a length of the overlapping part of the first shield layer (capacitance line 300, green) with the source area (L_A) and drain area (L_B), and “a” length (L_C) of the first electrode layer (scan line 3a, blue) along the first direction.

As shown, at least L_B is larger than L_A , thus rendering 8[a] obvious.

Either Mapping #1 or #3 of the “first electrode layer” renders claim 8 obvious because both include TFT’s gate electrode, which is formed by scan line 3a. Cok, ¶¶531-535.

4. Claim 9:

Annotated Figs. 2 and 3 below show shield layer 300 (green) fully overlaps a part of TFT's source and drain (red ovals). Base Claim 1 recites "a" part of the one of the source area and the drain area, which does not necessitate overlap over entire source/drain regions. Cok, ¶¶536-538.

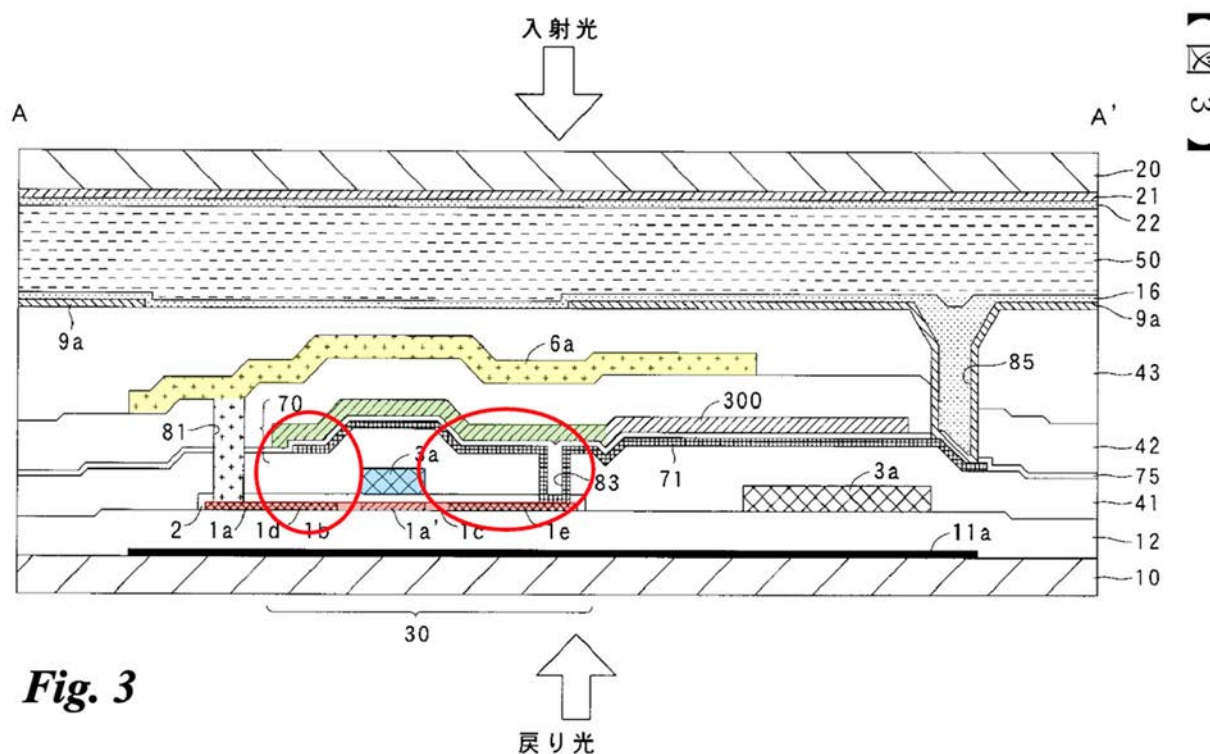


Fig. 3

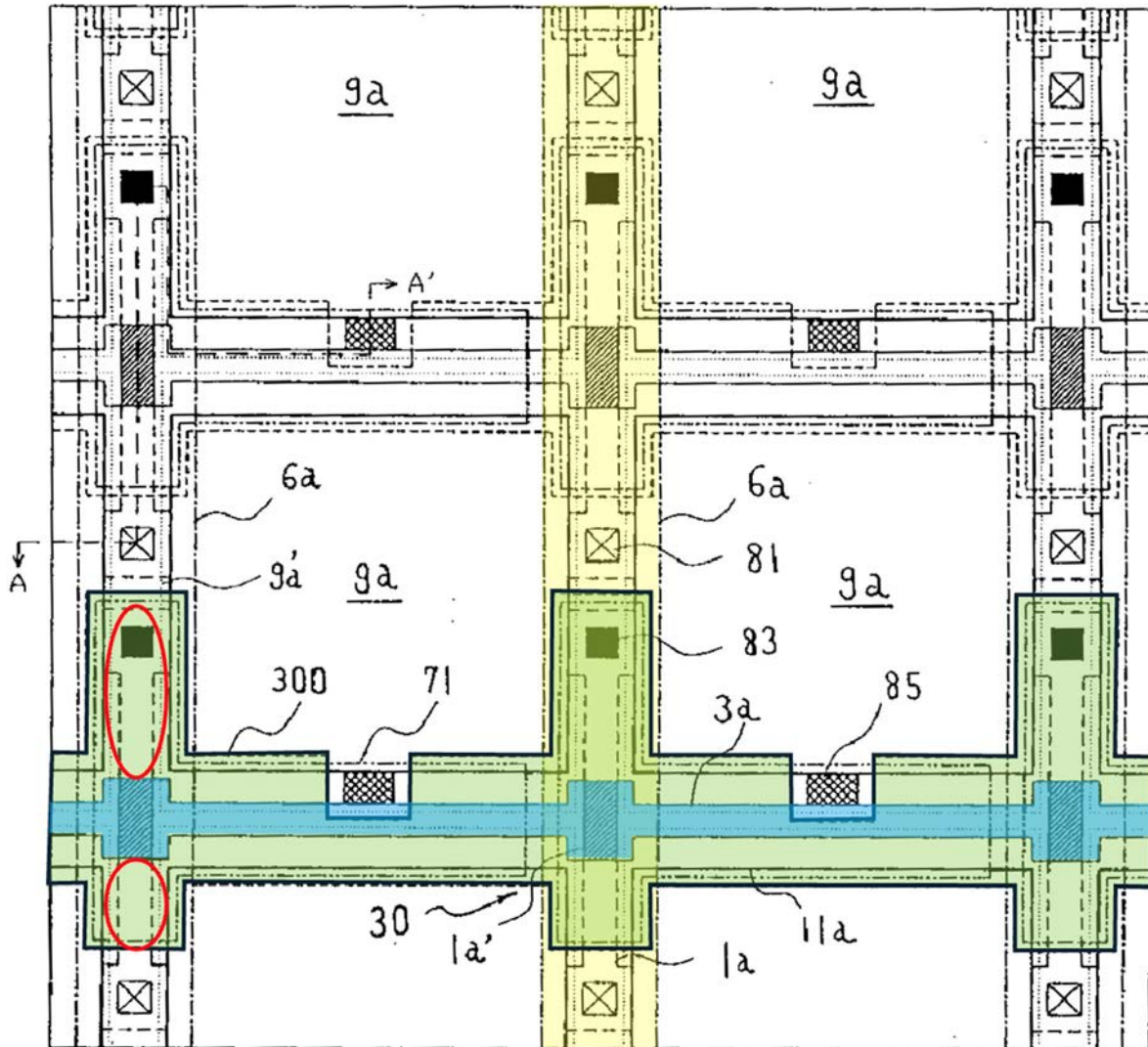


Fig. 2

5. Claim 10

a. 10[a]:

Annotated Fig. 2 shows data line 6a (“first signal line,” yellow) extends in a first direction.

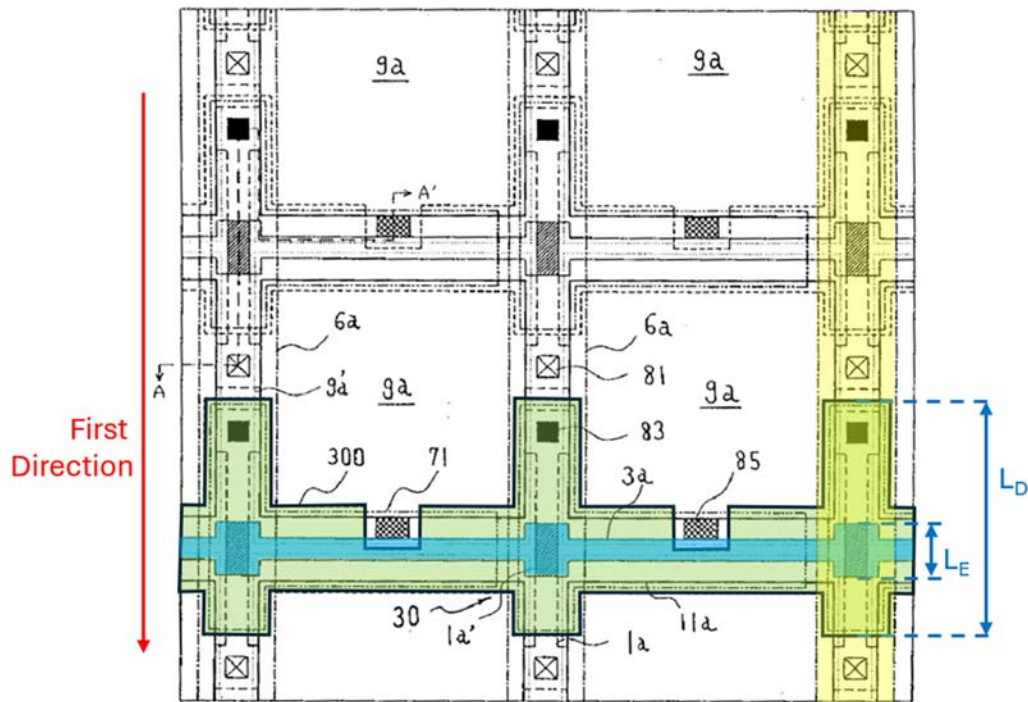


Fig. 2

b. 10[b]:

A length (L_D) of capacitor line 300 (“first shield layer”) that overlaps data line 6a (“first signal line”) is larger than a length (L_E) along the first direction of scanning line 3a (“first electrode layer”). *See also* Masao, ¶56. Either Mapping #1 or #3 of the “first electrode layer” renders Claim 10 obvious because both mappings include scan line 3a that forms TFT’s gate electrode. *Id.*

Cok, ¶¶539-543.

6. Claim 33

a. 33[pre]-[e]:

See 1[pre]-1[e]. §IV.G.1.a-§IV.G.1.f.

b. 33[f]:

See Claim 2. §IV.G.2.

c. 33[g]-[h]:

See 10[a]-10[b]. §IV.G.5.a-§IV.G.5.b.

See Cok, ¶¶544-553.

H. Ground 4B: Masao-Ohtani Combination Renders Obvious Claims 5, 11, 13, 28-29, 31.

1. Ohtani

Ohtani describes an active matrix liquid crystal panel that uses TFTs (Ohtani, 1:6-15) for various display devices. *Id.*, 9:38-10:33. Ohtani describes, in some implementations, multi-gated TFTs are used, further providing an example TFT (Fig. 10) where an active layer intersects with a gate wiring line at three places, creating a triple-gated TFT. *Id.*, 3:66-4:3, 6:20-21, 9:8-36, Fig. 10.

2. Motivation to Combine

POSITAs would have been motivated to combine Ohtani with Masao because both references related to display devices utilizing TFTs (Masao, ¶2; Ohtani, 1:6-15), such as liquid crystal displays (Masao, ¶49; Ohtani, 3:21-24) and sought to improve the operations of those devices. Masao, ¶47; Ohtani, 3:21-24, 9:32-36, 10:27-33. Therefore, POSITAs would have been guided by these complementary

teachings, and would have understood that Masao's device can be improved based on the teachings of Ohtani.

In the combination, POSITAs would have found it obvious to replace Masao's single-gated TFT with a multi-gated TFT per Ohtani. POSITAs would have found express motivation in Ohtani, explaining that “...*the withstand voltage of a TFT can be increased.*” Ohtani, 9:32-36.

Additionally, multi-gated TFTs were well-known, and would have provided other benefits such as reducing leakage current. Cok, ¶¶558-559, 57-58, citing EX1021-EX1023, EX1025, EX1027.

Further, POSITAs would have been motivated to apply a known technique (using multi-gated TFTs) to a known device ready for improvement (Masao's display device) to yield predictable results (higher voltage tolerance/reduced leakage current). POSITAs would have had a reasonable expectation of success, because using multi-gated TFTs in display circuits was well-known by 2014, as evident by Ohtani and other known references, and such modifications were within POSITAs skillset. Cok, ¶¶555-559.

3. Claim 5

a. 5[pre]:

See Claim 1. §IV.G.1.

b. 5[a]:

Masao's Fig. 1 (annotated below) illustrates a "third thin-film transistor" (yellow) as another TFT distinct from first TFT (blue).²² Masao, ¶¶50-51.

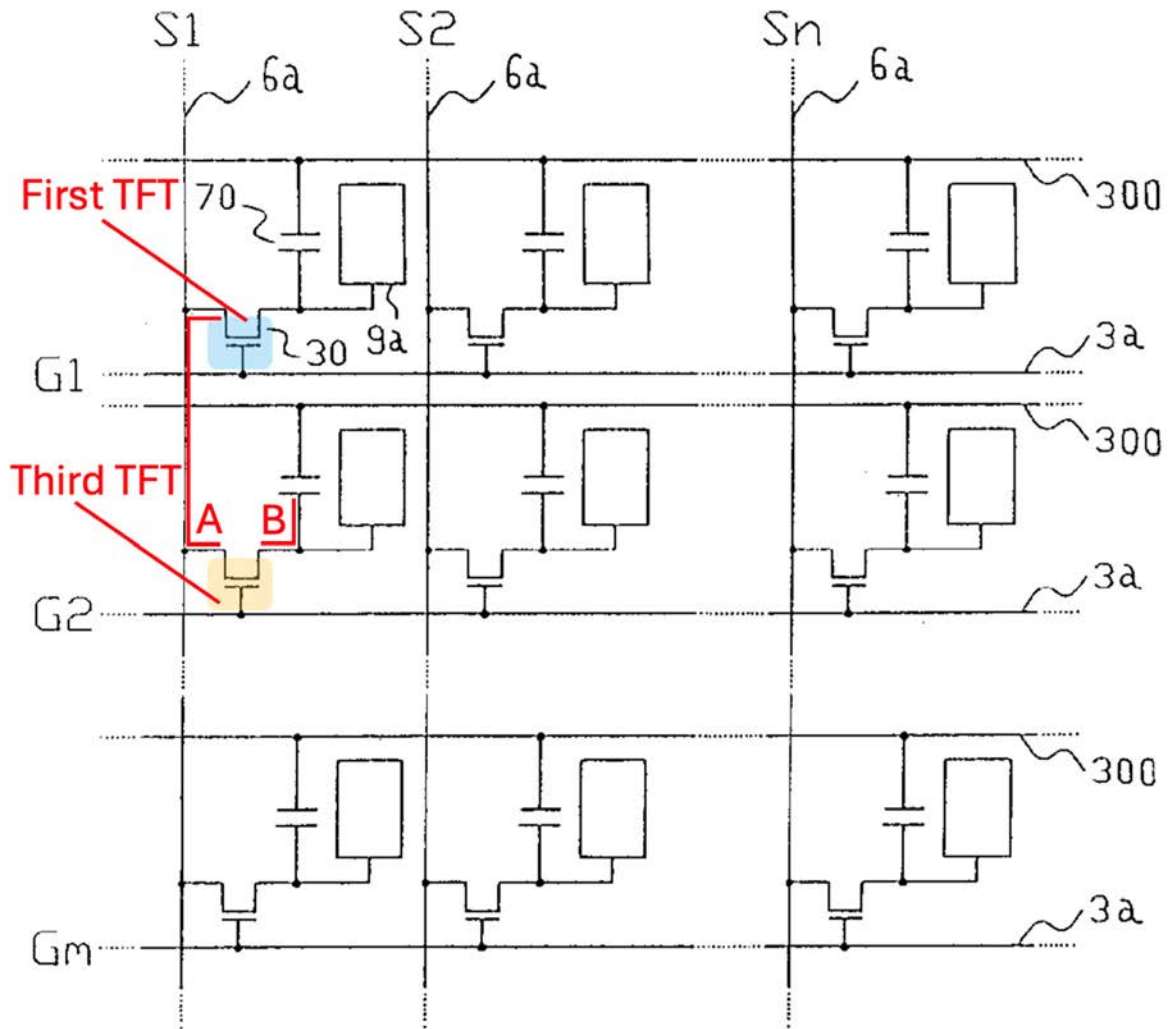


Fig. 1

²² See §IV.A.8.a regarding "first," "second," "third," etc.

Either Mappings #1 or #2 of the “first electrode layer” renders claim 5 obvious.

Annotated Fig. 3 below corresponds to Mapping #2.

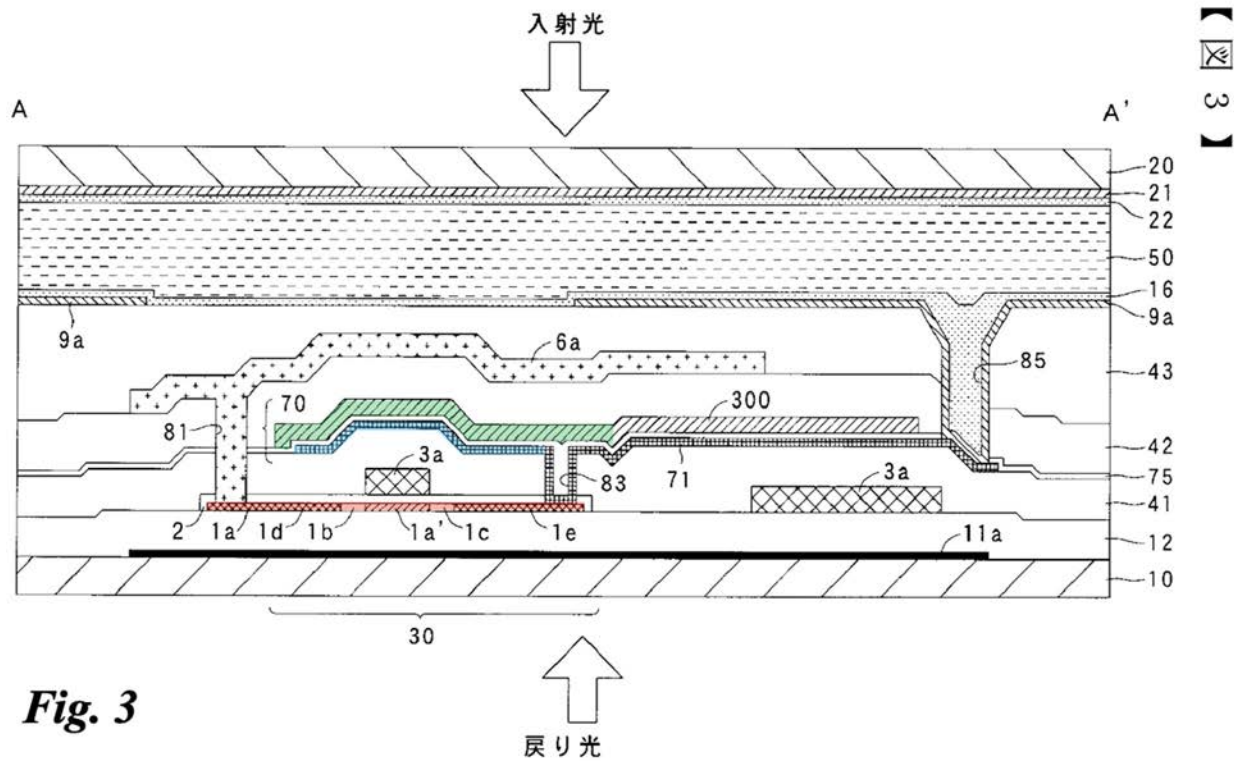


Fig. 3

Masao’s annotated Fig. 1 (above) shows sources “first” and “third” TFTs (“one end of” first and third semiconductors) are connected together (line A) through line 6a (Masao, ¶51), and Fig. 3 shows this connection is made through one end of semiconductor (high concentration source region 1d). *Id.*, ¶60. Fig. 1 also shows drain (“the other end of third semiconductor”) connected (line B) to relay layer 71, i.e., lower plate of capacitor 70 (which is in the “first electrode layer”), and Fig. 3 shows this connection through the other end of third semiconductor (high concentration drain 1e) Ohtani, ¶50.

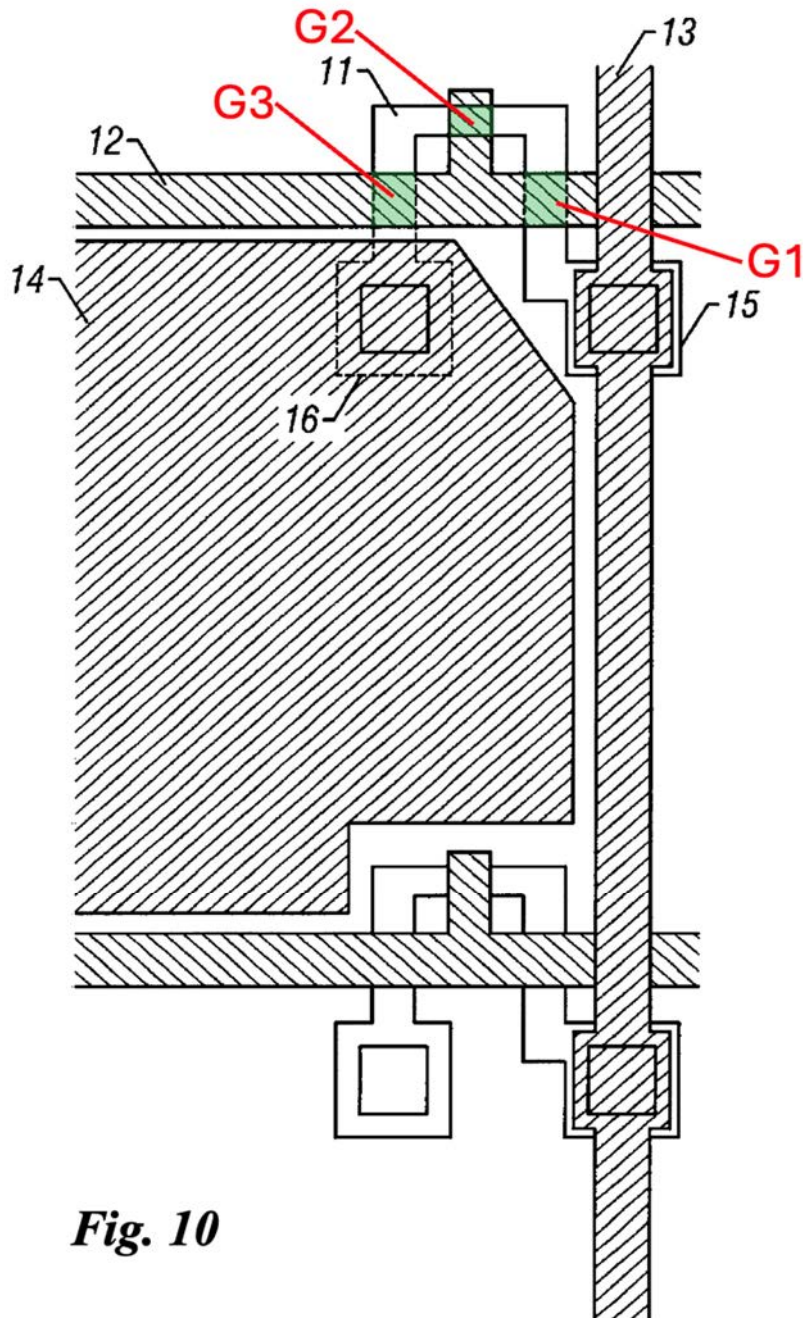


Fig. 10

POSITAs would have found it obvious to replace Masao's single-gated TFT with Ohtani's multi-gated TFT; the top capacitor electrode ("second shield layer") having a large extent (green annotation in Fig. 2 below) would overlap and shield he

“third” TFT, including all three gate electrodes and channel areas therebetween, from line 6a. Cok, ¶¶569-571.

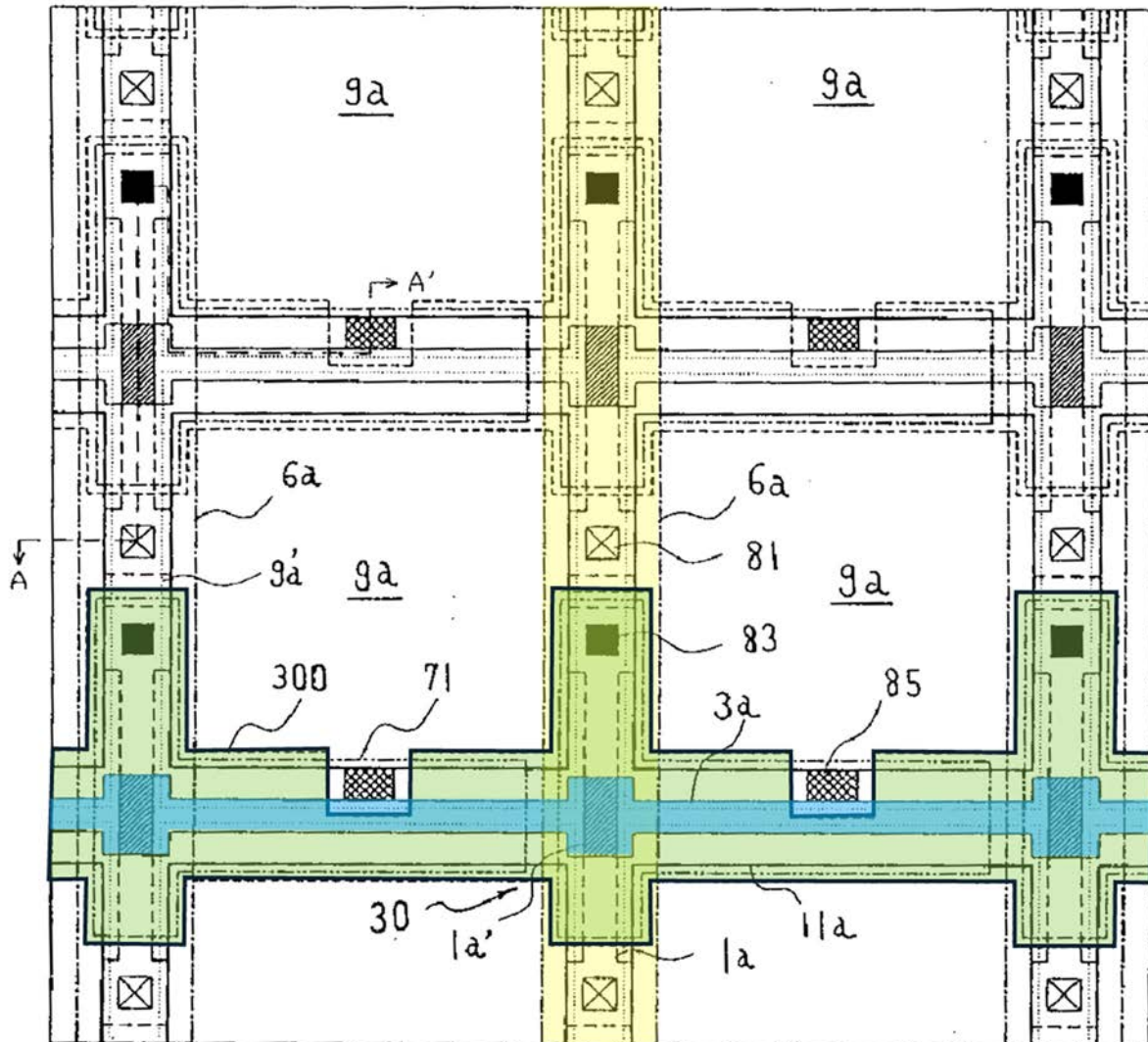


Fig. 2

POSITAs would have understood that each of the three gates overlapped a corresponding channel region; thus, the TFT in the Masao-Ohtani combination would include “a first channel area” under one gate electrode, and “a second channel area” under another gate electrode. Because Masao’s capacitance line 300 (green

color) overlaps the entire TFT, it would overlap a part between the first and second channel areas. Cok, ¶¶560-573. This combination would have been obvious to POSITAs. *See* §IV.H.2.

4. Claim 11

a. 11[a]:

See 5[b]. §IV.H.3.c. All three gate electrodes would be in the same layer because the gates in both Masao and Ohtani are formed via overlap of the same gate wiring line with active layer. Ohtani, 9:9-12; Masao, ¶53.

b. 11[b]:

Masao's gate electrodes (part of first electrode layer) are formed by, and are part of, scan line 3a ("second signal line") (Masao, ¶53), which POSITAs would have understood would be used to implement the combination's triple-gated TFT. Cok, ¶¶577-580. Annotated Fig. 2 below shows scan line 3a ("second signal line," blue) crossing data line 6a ("first signal line", yellow). *Id.*

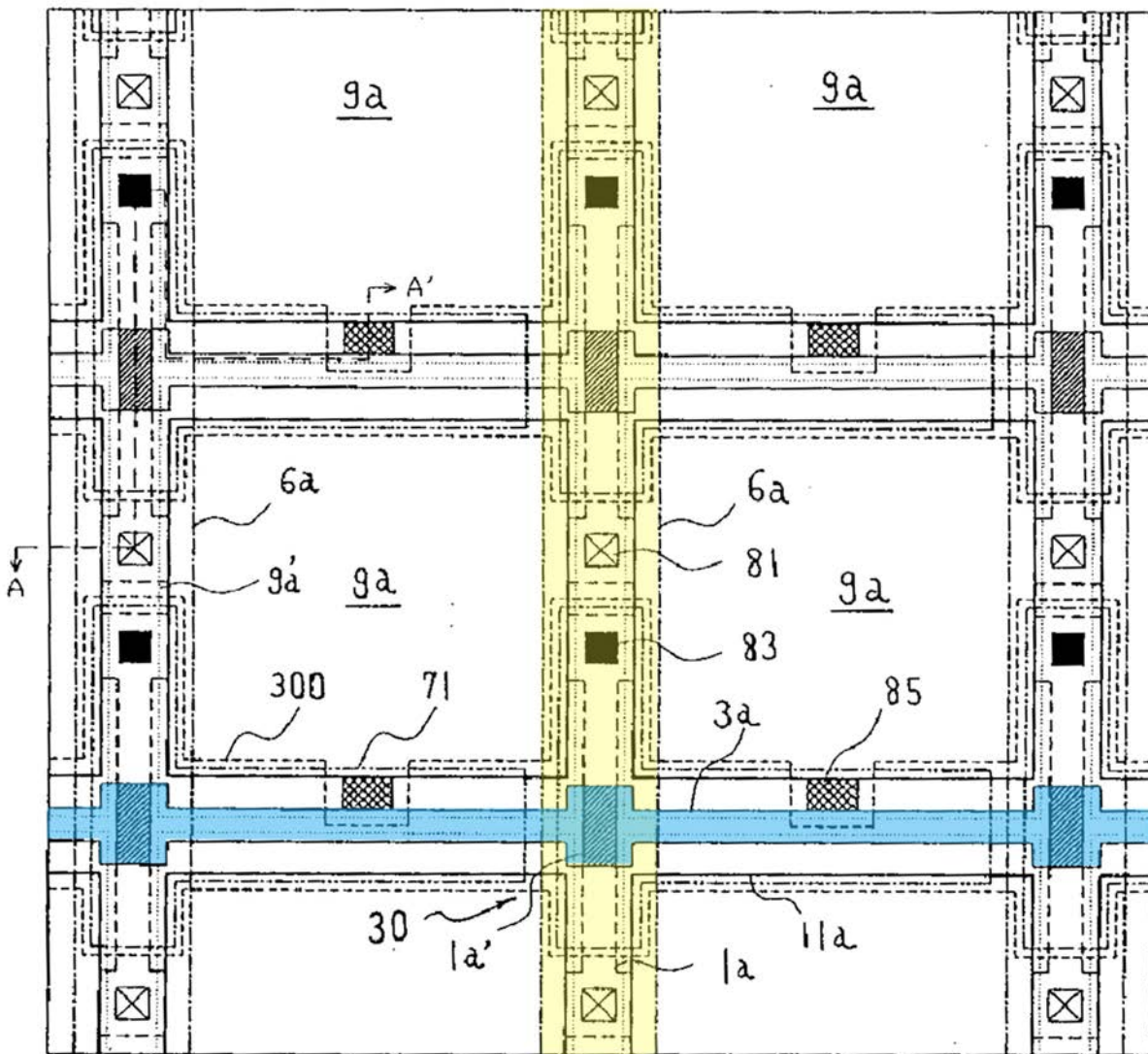
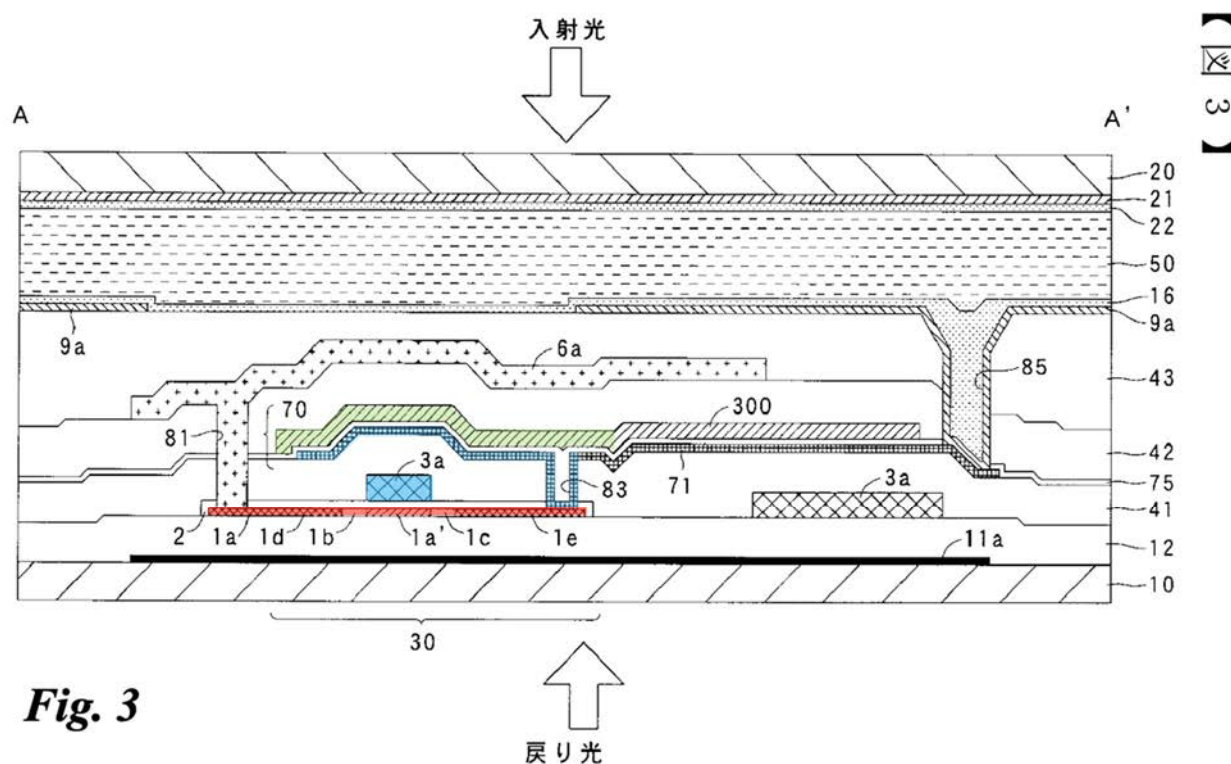


Fig. 2

For Claim 11, Petitioner is using Mapping #1 for the “first electrode layer.”

Cok, ¶¶574-580.



5. Claim 13

See Claim 2. §IV.G.2. Cok, ¶¶581-582.

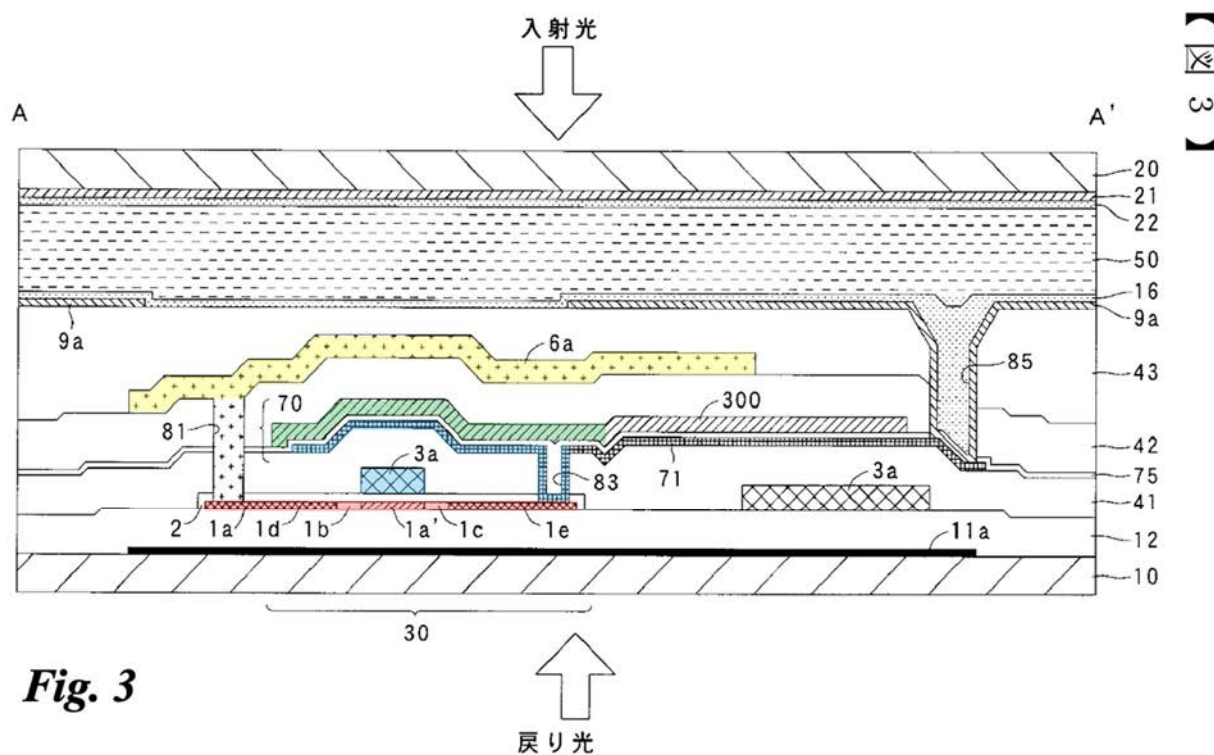
6. Claim 28

a. 28[pre]-[b]:

See 1[pre]-1[b] (§IV.G.1.a-§IV.G.1.c), using Mappings #1 or #2.

b. 28[c]:

Masao’s data line 6a (yellow) teaches or suggests “a first signal line,” and is over the first electrode layer (blue). See §IV.G.1.e; Fig. 3 (annotated below).



c. 28[d]:

See 5[a] (§IV.H.3.b), with claim 28’s “second” TFT/semiconductor treated as Claim 5’s “third” TFT/semiconductor. See Fig. 1 (annotated below in yellow).

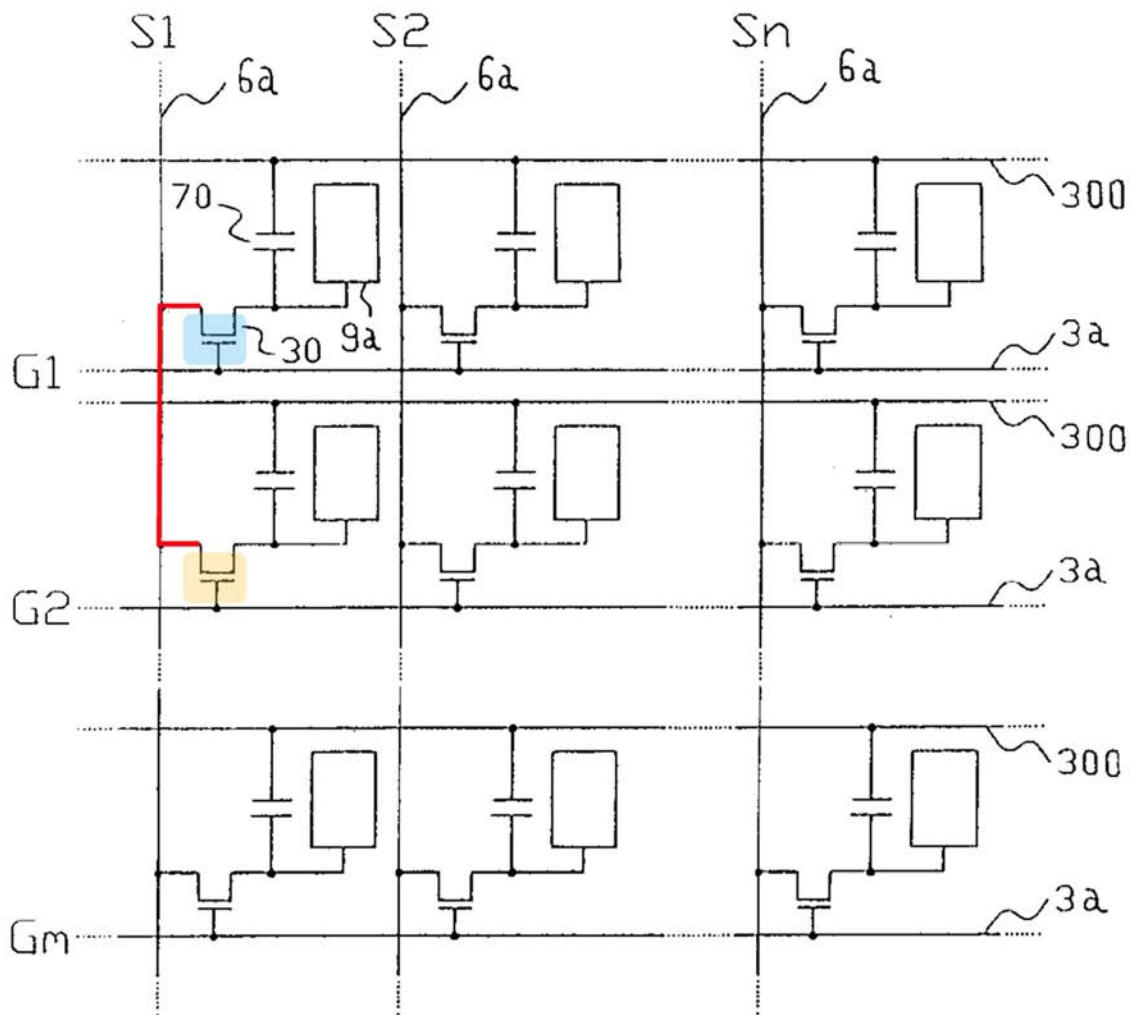


Fig. 1

d. 28[e]:

See 5[b]. §IV.H.3.c. In Claim 28, “shield layer” is part of capacitance line 300 overlapping second TFT, and notably, overlapping “a part between a first channel area and a second channel area” of its semiconductor.

Cok, ¶¶584-590.

V. CONCLUSION

IPR of the Challenged Claims is respectfully requested.

VI. MANDATORY NOTICES

A. Real Party in Interest

Petitioner identifies itself as a real party in interest. The following are identified as additional real parties in interest: Mianyang BOE Optoelectronics Technology Co., Ltd., Ordos Yuansheng Optoelectronics Co., Ltd., Chengdu BOE Optoelectronics Technology Co., Ltd., Chongqing BOE Optoelectronics Technology Co., Ltd., Wuhan BOE Optoelectronics Technology Co., Ltd., Yunnan Invensight Optoelectronics Technology Co., Ltd. f/k/a/ BMOT f/k/a Kunming BOE Display Technology, and BOE Technology America, Inc.

B. Related Matters

To the best of Petitioner's knowledge, the '015 patent has been involved in the following matters:

- *Samsung Display Co. v. BOE Technology Group Co.*, No. 2:25-cv-00412-JRG (E.D. Tex.).

C. Notice of Counsel and Service Information

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Petitioner consents to electronic service. All services and communications to the attorneys listed above may be sent to:

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D. Power of Attorney

A power of attorney is filed herewith according to 37 C.F.R. §42.10(b).

Date: September 15, 2025

Respectfully submitted,

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CERTIFICATE OF WORD COUNT UNDER 37 CFR §42.24(d)

Pursuant to 37 C.F.R. §42.24(a), Petitioner hereby certifies that portions of the above-captioned Petition for *inter partes* review of U.S. Patent No. 10,439,015, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,982. Pursuant to 37 C.F.R. §42.24(a), this word count is in compliance and excludes the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing. This word count was prepared using Microsoft Word.

Date: September 15, 2025

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that true copies of the Petition for *inter partes* review of U.S. Patent No. 10,439,015 and supporting materials (Exhibits and Power of Attorney) were served via overnight delivery on the Patent Owner at the correspondence address of record as listed on PAIR:

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