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Wire bonding using insulated wire and new challenges in wire bonding

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Abstract

Purpose – This paper attempts to review recent advances in wire bonding using insulated wire and new challenges in wire bonding for advanced microelectronics packaging.

Design/methodology/approach – Dozens of journal articles, conference articles and patents published or issued in 2004-2007 are reviewed.

Findings – The advantages and problems/challenges related to wire bonding using insulated wire are briefly analysed, and several solutions to the problems and recent findings/developments related to wire bonding using insulated wire are discussed.

Research limitations/implications – Because of page limitation of the paper, only brief review is conducted. Further reading is needed for more details.

Originality/value – This paper attempts to provide introduction to recent developments and the trends in wire bonding using insulated wire. With the references provided, readers may explore more deeply by reading the original articles and patent documents.

Keywords Electrical insulation, Electronic engineering, Bonding, Wires

Paper type General review

1. Introduction

Integrated circuit (IC) technologies are resulting in the required advances through size reductions following Moore's law (Jackson *et al.*, 2005), and this leads to an industrial competition of shrinking lithography (Ronse *et al.*, 2004; Blaikie *et al.*, 2006; Eloy and Depeyrot, 2006; Henry *et al.*, 2006; Zell, 2006). Recently, Moore's law appears to slow down, and the capacity-doubling period has become three years towards five, with the passing of the lithographic threshold of 10 nm being postponed to 2015 (Eloy and Depeyrot, 2006). Precision manufacturing of silicon and various substrates also face more new challenges (Shankar and Zhong, 2006; Young *et al.*, 2006; Zhong *et al.*, 2006; Paehler *et al.*, 2007; Schoenfelder *et al.*, 2007). Silicon nanowires may become crucial components for ultra-low power devices (Pott and Ionescu, 2006). Nano-roughness is also very important in nano-structures and nano-devices (Gogolides *et al.*, 2006). Nano-imprinting is a potential patterning technology (Trybula, 2006). Imprint lithography is proposed as a low-cost method for next generation lithography for fabrication of IC chips with nodes of 45 nm and below (Maltabes and Mackay, 2006).

This paper attempts to review recent advances in wire bonding using insulated wire and new challenges in wire bonding for advanced microelectronics packaging. Dozens of journal articles, conference articles and patents published or issued in 2004-2007 are reviewed. Relevant conference articles and patents are included because recently published journal articles reporting wire bonding using insulated wire

are scarce. The new challenges related to wire bonding are briefly analysed, and several solutions to the problems and recent findings/developments related to wire bonding using insulated wire are discussed.

2. Wire bonding and new challenges

The importance of microelectronics packaging is tremendously increasing, as the microelectronics industry moves into the nano-era (Brillouet, 2006). The future's nanometer-scale circuits require advanced packaging technologies to distribute reliable power and signals among IC chips and microelectronics devices (Kaushik *et al.*, 2006). Manufacturers should understand recently-enacted environmental legislation and directives in the USA, Japan and the European Union, and study their effects on the microelectronics industry (Ciocci and Pecht, 2006). Intensive research and developments of lead-free products (Arulvanan and Zhong, 2006) are stimulated by a US congress bill that has proposed to ban lead from a wide variety of uses (Kamal and Gouda, 2006). Developments of wearable microelectronics devices are also increasing (Whitmarsh, 2005). Today's hand-phones usually include three modern packages: wafer level, leadless and area array packages such as ball-grid-array packages, being miniaturized for higher integration density (Plieninger *et al.*, 2006).

Advanced packaging technologies continue to be developed to deal with the new challenges for advanced microelectronics devices, driven by the smaller, faster and cheaper demands (Longford, 2005). Although flip chip (Jang *et al.*, 2006), wafer-level packaging (Oberhammer and Stemme, 2005), and tape automated bonding (Kassamakov *et al.*, 2007) technologies are also increasingly employed, wire bonding is the most widely used microelectronics packaging technology in the industry (Zhong *et al.*, 2007a).

In the microelectronics packaging industry, economic improvement is measured in fractions of pennies, and ultimately cost rules. A production manager has to consider

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costs, not only package performance. Wire bonding dominates more than 90 per cent of the packaging market because of its cost effectiveness and flexibility. It has an established huge base of materials, equipment and manpower. A recent study by Yole confirms wire bonding is currently the lowest-cost IC interconnect technology (Lyn and Crockett, 2007).

As the industry moves into a new era, new challenges in wire bonding emerge for advanced microelectronics packaging, such as reduction in wire size, cost and bond pad pitch (BPP), emergence of alloyed gold wires, copper wires and advanced packages, increase in I/O numbers, and enhanced manufacturability of capillaries for wire bonding of ultra-fine-pitch low- k devices. To deal with these challenges, capillaries must have very small holes and tip diameters for wire bonding of devices with BPPs < 50 μm using small wire sizes, good ultrasonic energy transfer (Zhong and Goh, 2006), and customized designs for advanced applications such as multi-tier bonding (Zhong and Goh, 2004), stacked-dies wire bonding (Tee *et al.*, 2006), wire bonding of low- k ultra-fine-pitch devices, and wire bonding with copper wire and insulated wire. The wire must have high-tensile strength and a short heat affected zone for low-loop requirements. The surface roughness and hardness of the substrate also become important, because stitch and tail bonds on tiny bumps will cause non-sticking on lead. Wire bonders must have sufficient bonding speeds, Z-resolution, bond placement accuracy, free air ball (FAB) forming consistency and looping algorithms (Goh and Zhong, 2007b).

The permittivity of interconnection insulators has to be reduced to have good circuit performance and limit parasitic coupling effects (Vitiello *et al.*, 2006). To meet the demand of lower interconnection delay, porous low- k materials are required (Hsia, 2006). To reduce the resistance-capacitance delay in very large integrated interconnections, the industry has replaced SiO_2 with a low- k dielectric and the Al conductor with Cu (Hoofman *et al.*, 2005). A method to obtain ultra-low- k dielectrics is incorporating porosity into the existing low- k materials (Iacopi *et al.*, 2004).

Low- k materials introduce new challenges to the mechanical integrity of IC devices (Zhao, 2005) and wire bonding. Cu electromigration is also a key issue that limits the lifetime of advanced interconnection systems (Chhun *et al.*, 2006). A critical challenge for the integration of porous low- k materials is their degradation during different processes (Baklanov *et al.*, 2006). Such materials have low-fracture toughness, a low-elastic modulus and poor adhesion to capping and liner layers (Gottfried *et al.*, 2006; Leduc *et al.*, 2006). Chip-packaging interaction becomes a critical reliability issue due to mechanically weak low- k materials used in advanced ICs (Dang *et al.*, 2006). Compared to the SiO_2 material, a low- k material needs longer wire bonding time to overcome the energy loss because of the compliance of the low- k material (Tan *et al.*, 2005).

There are more challenges in wire bonding for low- k devices if the BPP is ultra fine. Small wire sizes must be used, and this leads to various problems such as wire short due to possible wire sweeping, and decreased bonding strength. Therefore, investigations of the effects of small wire sizes are performed and search of solutions to the problems is conducted worldwide (Zhong, 2007).

The demand for low- k device bonding ranges from fine pitch to ultra-fine pitch. The ball bond becomes a major

challenge because lower parameter settings result in non-sticking and higher parameter settings cause metal pad peeling (Goh and Zhong, 2006). Smaller wire sizes also cause stitch bond problems: the tail bond may be detached away during the wire termination process, causing non-sticking on lead or wire open. Stitch bond problems also result from inconsistent substrate quality. The BPP reduction requires the capillary tip diameter to be reduced significantly. Optimal bonding machine performance and capillary designs are needed. Advanced equipment is required to handle small capillary tip manufacturing, and ultra-precision finishing processes are also needed to avoid weakened bottlenecks (Goh and Zhong, 2007b). Investigations have revealed that after thermal aging, the ball bonds formed using gold wires of small sizes have voids and intermetallic compound growth (Murali *et al.*, 2006).

Gold wires are the most widely employed in wire bonding, but Al-Si wires (Qin *et al.*, 2004) and Cu wires are also used for interconnections in microelectronics devices. Copper wire is better than Au wire in terms of electrical conductivity, production cost, and resistance to wire sweeping (Ratchev *et al.*, 2006). Despite its many advantages, Cu wire has not been widely used like Au wire, because of its poor bondability for stitch bonds due to surface oxidation (Kaimori *et al.*, 2006).

The wire cost may not be the driving force for fine-pitch copper wire applications due to the additional cost of forming gas during copper wire bonding (Goh and Zhong, 2007a). To improve stitch bondability, higher parameter settings are used, causing heavy cap marks and potential short tails or wire open. Cu/Au stitch bonds are weak. Therefore, copper wire bonding has wire open and short tail defects, poor process control, and low-stitch pull readings. Wire bonding using Cu wire also introduces hardness issues. There is a need to investigate the effects of the process parameters on the hardness of Cu FABs (Zhong *et al.*, 2007b), because Cu exhibits a larger strain-hardening effect at a higher strain rate (Bhattacharyya *et al.*, 2005).

In this focused review paper, only solutions to the problems/challenges in wire bonding using insulated wire are discussed.

3. Advantages of wire bonding using insulated wire

A problem using small wire sizes in a microelectronics package is that a wire may short to another conductive structure due to sweeping, which may occur during encapsulation when the liquid encapsulant moves the soft wire towards another conductive structure (Downey and Harper, 2006). Smaller diameter wires tend to have higher wire sweeping and shorting rejects (Harun *et al.*, 2007). Besides, using copper wire, using insulated wire can be one of the solutions to the wire shorting problem.

Insulated wires are not new. They are traditionally and currently used in many applications such as coils used in motors, electronics circuits and transformers incorporated into a large variety of cars, electrical devices and machines (Mesaki and Tatsumatsu, 2004).

Wire bonding using insulated wire was developed more than ten years ago. Owing to the high-processing cost and lack of sufficient market demands, insulated wire bonding was not popular. As IC packages become more complicated, insulated

wire has market demands today and in the future because it can prevent wire short, which becomes a new problem due to the reduction in BPPs and wire sizes (Goh and Zhong, 2007b), as also discussed in the previous section.

Insulated wire technology was identified on the 2006 ITRS Roadmap as a cost-effective solution to enhance package performance, enable complex package designs, and improve the yield of high-density packaging. It allows wire touching, crossing and sweeping, long wires, and wire routing configurations that were previously prohibited. Insulated wires use existing platforms and wire bonding infrastructure and should meet industry standard test specifications (Lyn and Crockett, 2007).

The industry has been seeking insulated wire bonding solutions for almost as long as wire bonding has been available. The advantages have been well known for many years, and they are summarised in Table I. Insulated wire bonding can use the lowest-cost packaging infrastructure and reduce wire shorting rejects. It allows flexible routing without requiring a fan-out area, and can connect stack dies directly. It can overcome the previous limitation of wire bonding that the interconnections are confined to the chip perimeter, with its area array capability using crossed and closely packed insulated wires. Wire bonding with insulated fine gold or copper wire and low-*k* pad structures are possible (Harun and Tiu, 2005; Ibrahim and Bee, 2005; Lyn *et al.*, 2006; Harun *et al.*, 2007; Lyn and Crockett, 2007).

4. Challenges in wire bonding using insulated wire

Despite many advantages/benefits of insulated wires, there were problems and challenges that had to be solved and dealt with before insulated wires could be widely used in wire bonding for advanced microelectronics packaging. The challenges of wire bonding using insulated wire are summarized in the second column of Table I.

Insulated wires cannot be bonded in the usual way bonding bare wires. If a ground is not provided properly, the electricity can jump through the insulation layer to the ground, burning a hole in the insulation layer and resulting in damaged wire (Lyn *et al.*, 2004, 2005).

There is no concern with ball bonds because the firing of the electronic-flame-off (EFO) to form a FAB will melt the insulation layer on the wire (Goh and Zhong, 2007b), while the rest of insulation layer remains on the portions of the wire that is not melted because the melting temperature of the insulation layer is higher than that of the wire (Downey and Harper, 2006).

However, to obtain reliable stitch bonds between the insulated wire and the substrate lead is a challenge. Non-sticking on lead is a common problem with the stitch bonds due to the presence of the insulation layer (Goh and Zhong, 2007b; Harun *et al.*, 2007). Very often, stitch bonds are weak because of the insulation layer partially existing between the wire and the lead, preventing good adhesion. Insulated ultra-fine wire usually leads to very low-wire peel strength (Harun and Tiu, 2005), and there are frequent machine stoppages due to non-uniform stitch formation and non-sticking on lead (Ibrahim and Bee, 2005).

Thinner insulation leads to better bonding but results in “kissing effect” after about 100 temperature cycling, while thicker insulation has a bondability issue in tearing off the insulation layer. Lower insulation melting temperature leads to insulation layer pushed out to one side of the wire during moulding with the bare wire exposed, potential to wire short. Lower coating temperature is good for wire bonding but may also cause the exposure problem (Ibrahim and Bee, 2005).

5. Solutions and findings for reliable wire bonding using insulated wire

Attempts made in the past to deal with the challenges in wire bonding using insulated wire had limited success (Lyn *et al.*, 2006). Recently, several articles and approved patents are published, reporting good solutions and findings for reliable wire bonding using insulated wire. They are briefly summarised in Table II.

A ground is properly provided to prevent the insulation layer on the wire remote from the free end from being damaged. One method is to provide a ground adjacent to the free end of the insulated wire by replacing a dielectric capillary with a conducting capillary. Another method is to

Table I Advantages and challenges of wire bonding using insulated wire

Advantages	Challenges
Prevents wire shorts and enables cross bonding	Damaged wire with a hole burned in the insulation layer
Uses existing platforms and lowest-cost packaging infrastructure (wire bonding)	Non-sticking on lead
Is suitable for multi-row, ultra fine pitch and area array wire bonding	Low-stitch pull readings
Is suitable for system in package, stacked dies and side-by-side chip-to-chip bonding	Frequent machine stoppages
Enables flexible routing, simplified substrate and packaging of small dies	“Kissing effect” after temperature cycling
Enables complex package designs and improves the yield of high-density packaging	Insulation layer pushed out to one side of the wire during moulding
Allows use of the Z dimension and wasted space created by parallelism of bare wires	
Enables wire bonding with insulated fine gold or copper wire and low- <i>k</i> pad structures	

Sources: Lyn *et al.* (2004, 2005, 2006), Harun and Tiu (2005), Ibrahim and Bee (2005), Harun *et al.* (2007) and Lyn and Crockett (2007)

Table II Solutions and findings for reliable wire bonding using insulated wire

Solutions and findings	References
Provide a ground adjacent to the free end of the insulated wire with a conducting capillary	Lyn <i>et al.</i> (2004, 2005)
Add a ground at a spool end of the wire at a far side of the insulated wire path from the free end	
Form a bump on the second wire bond, offset by a distance of about one half of a diameter of the bump	Harun and Tiu (2005, 2006)
Provide a special capillary movement to achieve mechanical abrasion	Ibrahim and Bee (2005)
Use a special surface-treated capillary for effective tearing of the insulation layer	
Choose a proper combination of insulation thickness, melting and coating temperatures, capillary and wire bonding parameters	
Use shorter EFO gap and lower-EFO current compared to bare wire to achieve optimal FAB quality	Lyn <i>et al.</i> (2006) and Lyn and Crockett (2007)
Provide a coating material that easily cracks only at the stitch bond with available bonding parameters	
Apply high-initial bonding force with low-ultrasonic energy, apply high-initial impact during touch-down, and provide slight scrub motions to promote coating removal	
Use a smaller capillary hole, which does not scrape the coating during looping	
Use a smaller capillary outside radius, which maximizes the capillary area contacting the stitch bond	
Use a matte capillary tip	
Move the capillary tip with the wire over the stitch bond pad	Harun <i>et al.</i> (2007)
Roughen the outer surface of the capillary tip	

add a ground at a spool end of the wire at a far side of the insulated wire path from the free end (Lyn *et al.*, 2004, 2005).

A method is invented to form a bump on the second wire bond. The bump is offset by a distance of about one half of a diameter of the bump, which depends on the wire diameter used. The bump may have a diameter of about 40–50 μm for a $\phi 25 \mu\text{m}$ wire used. This can enhance the bondability of insulated wire with increased wire pull/wire peel strength (Harun and Tiu, 2005, 2006).

A special capillary movement is provided to enable a mechanical thermal compression of the wire to the lead at the stitch bond, using a special surface-treated capillary for effective tearing of the insulation layer. The peel strength is increased by 150 per cent. An optimal insulation thickness is important. Higher coating temperature does not result in exposed insulation layer. Choosing a proper combination of insulation thickness, melting and coating temperatures, capillary and wire bonding parameters can lead to good reliability results with insulated wire, comparable with those with normal gold wire (Ibrahim and Bee, 2005).

The coating thickness must be thin enough so that insulated wires do not require increased capillary hole diameters. The bottom half of a FAB is free of insulated materials to form reliable electrical connections. The wire bonding window is within standard bonding parameter ranges for stitch bonding, but may be shifted compared to that using bare wire (Lyn *et al.*, 2006).

Insulated wire requires shorter EFO gap and lower-EFO current compared to bare wire to achieve optimal FAB quality. Development is focused on providing a coating material that easily cracks only at the stitch bond with available bonding parameters. The method includes applying high-initial bonding force with low-ultrasonic energy, applying high-initial impact during touch-down, and providing slight scrub motions to promote coating removal. A smaller capillary hole, which does not scrape the coating during

looping, is preferred for insulated wire. A smaller capillary outside radius is preferred, which maximizes the capillary area contacting the stitch bond. The capillary tip finish recommended for insulated wire is a matte compared to a polished surface for bare wire (Lyn and Crockett, 2007).

A method is invented to bond insulated wire by moving the capillary tip with the wire over the stitch bond pad such that the wire is rubbed between the capillary tip and the pad, tearing the insulation layer so that a portion of the metal core contacts the pad. The wire is then bonded to the pad by thermocompression bonding. The outer surface of the capillary tip is roughened and has a roughness of between two to five times the surface roughness of current capillaries to enhance the tearing of the wire insulation. This can result in increased wire pull/wire peel strength and near elimination of rejection of parts due to non-sticking on lead (Harun *et al.*, 2007).

6. Conclusions

Insulated wire has market demands today and in the future because it can prevent wire shorting, which becomes a new challenge due to the further reduction in BPPs and wire sizes. However, there were problems, which had to be solved before insulated wires could be widely used in wire bonding for advanced microelectronics packaging. Non-sticking on lead was a common problem. Several solutions to the problems have been proposed by several groups of researchers and engineers. Although, recently published relevant journal articles are scarce, with much more anticipated advanced microelectronics devices packaged by wire bonding using insulated wires in the near future, more articles reporting more new solutions, lower costs, better results and innovative applications are expected.

This paper briefly introduces the published articles and issued patents. For the detailed and accurate description of an

invention, readers may closely read the published original document with detailed figures or drawings provided by its authors and publisher.

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