

Impact of 3D Design Choices on Manufacturing Cost

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Abstract—The available options in 3D IC design and manufacturing have different impact on the cost of a 3D System-on-Chip. Using the 3D cost model developed at IMEC, the cost of different system integration options is analyzed and the cost effectiveness of different technology solutions is demonstrated. The cost model is based on the IMEC 3D integration process flows and includes the cost of manufacturing equipment, fabrication facilities, personnel, and materials. Using the IMEC 3D cost model, the cost of various 3D stacking strategies is compared to single die (*i.e.* 2D) integration. In addition, the effect on cost of different Through-Silicon-Via (TSV) manufacturing technologies is evaluated. The effectiveness of different 3D testing strategies and their impact on system cost is also investigated.

I. INTRODUCTION

The scaling of the on-chip feature size has been the major driving force for the evolution of microelectronic technology in the last 30 years. However, for certain applications, the pursue for further feature size scaling is debatable as the increased manufacturing cost narrows significantly the profit margins [1], [2]. Alternatively, stacking of integrated circuits in the third dimension emerges as a promising solution to the scaling issues [3]–[6]. With 3D integration, the trend in the number of devices within an integrated system as described by Moore's law can be maintained for future generations of integration technologies. Furthermore, 3D stacking allows the integration of heterogeneous subsystems which may require incompatible implementation steps in current single-die technologies [7], [8].

There are many options to vertically stack and interconnect circuits implemented on different silicon chips [9]–[11]. These options specify a range of trade-offs related to the silicon thickness, bonding method, and electrical interface among stacked dies. Additional trade-offs arise when considering the density, the dimensions, the materials, and the electrical characteristics of 3D interconnects. Different implementation options are investigated that leverage these trade-offs to provide reliable and cost effective 3D process flows [12], [13]. As 3D integration technology matures, many of these options will be further pursued and developed, while others will be abandoned.

The adoption of a 3D integration approach depends on the performance specifications and cost requirements for a specific application [13], [14]. Therefore, a comprehensive and detailed cost model can be utilized to leverage efficiently the many trade-offs in 3D design and manufacturing processes. In addition a 3D cost model can be used to identify those process

steps that are cost critical and evaluate alternative approaches. The 3D cost model developed at IMEC is presented in this paper and it is applied to evaluate the impact of various design choices on the 3D manufacturing cost. An outline of the model is discussed in Section II. The cost of 3D stacking is compared to system integration on a single die in Section III. TSV manufacturing technologies with different integration densities are compared in Section IV. The cost of testing in 3D systems is considered in Section V. Finally some conclusions are presented in Section VI.

II. IMEC 3D COST MODEL

The IMEC 3D cost model is based on actual 3D process flows implemented at IMEC and it is built in a modular way to be easily adaptable for different flows. The foundation of the model is the sequence of the processing steps that are required for 3D integration. For each process step the processing time per wafer is considered and used to determine the throughput of the corresponding processing tool. For tools that have multiple processing units, parallel processing of wafers is considered that results at a higher tool throughput.

In addition to the process time for each step, a target production volume is specified in number of wafers per year. Based on the throughput of each processing tool, the number of tools required to achieve the targeted production volume is calculated. For each tool, the depreciation and maintenance costs, the area occupied in the clean room, and the required number of operators are considered. In this way the annual equipment cost, infrastructure cost, and personnel cost figures can be calculated. The costs for tool consumables, and materials are also taken into account for each processing step. An outline of the calculation flow for the IMEC 3D cost model is illustrated in Figure 1.

The cost model is organized in a modular way allowing existing processing steps to be removed or new processing steps to be inserted into a 3D process flow. All the parameters of the processing steps such as processing times, tool configurations and costs, personnel salaries, and infrastructure costs are considered as variable values and can be modified. Therefore, the cost figures of alternative process flows can be investigated and compared. Also, the contribution of each process step on the total manufacturing cost is evaluated, thus allowing further development and optimization of the most cost-critical steps.

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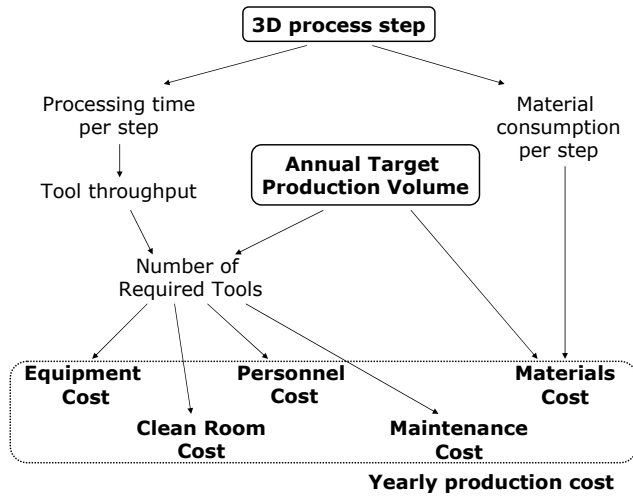


Fig. 1. Outline of the IMEC 3D cost model.

The processing steps for a 3D integration process flow are grouped into three major tasks: The first task is the formation of the Through-Silicon Vias (TSVs) for vertical interconnects. The second task includes the wafer thinning and the backside processing steps and the third task is the chip stacking process. The overall 3D processing cost per wafer is the sum of the costs of these three tasks. Using one of the IMEC 3D process flows [15] as an example, the cost of each task is calculated and illustrated in Figure 2 for variable annual wafer production volume. The processing cost of each task can also be separately calculated considering different equipment sets, infrastructure facilities, and production volumes for each task.

In the following sections of this paper the IMEC 3D cost model is used to investigate different design trade-offs for 3D system integration. Different aspects of the 3D stacking process are discussed in each section and figures of merit related to manufacturing cost are determined.

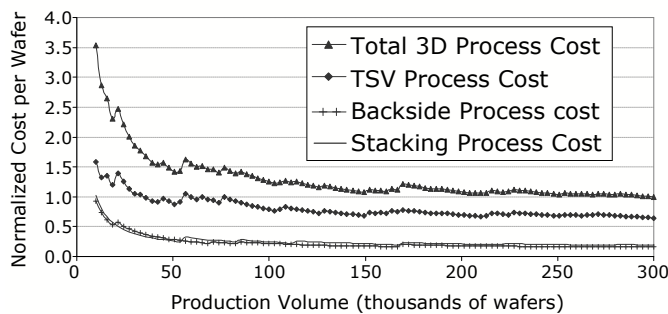


Fig. 2. Normalized 3D processing cost per wafer for each processing task. Annual production volume varies from 10k to 300k wafers.

III. 3D VS 2D INTEGRATION COST

In this section, the effect of increasing die area on the system yield and the benefits of the smaller die sizes enabled

by 3D integration are investigated. This cost analysis can be performed very early in the design cycle of a system to determine whether 3D integration can provide an efficient implementation choice.

As the number of gates in a system is increased with the integration of more subsystems on a single die, the die size increases as well. This has a negative effect on the die yield per wafer as the probability of a process defect existing on a die is proportional to die size. Furthermore, with increasing die size, the number of printed dies on a wafer is smaller and the cost per good die is higher. Alternatively, in the case of a 3D integrated system, a partition of the system into two dies with equal size that are vertically stacked is considered. There is additional processing cost for the creation of the TSVs, the thinning of the stacked dies, and the 3D stacking and bonding steps. However, the die yield is improved due to the smaller die sizes used for stacking. This trade-off is investigated using the IMEC 3D cost model.

Three different system integration options are considered: i) Single die system integration (2D approach). ii) 3D integration in two layers using die-to-wafer (D2W) stacking. iii) 3D integration in two layers using wafer-to-wafer (W2W) stacking. In die-to-wafer stacking, a pre-selected known-good-die (KGD) is stacked on top of another known-good-die resulting in improved stacking yield [16]. Alternatively for wafer-to-wafer stacking, an entire wafer is aligned and stacked on top of another wafer without selecting the dies that are stacked together [9]. Therefore, one defected die in a stack will result in an overall defected stack and the stacking yield will be lower. To make a fair comparison between the two alternative 3D integration approaches, the die sizes for both the D2W and W2W cases are considered equal.

The cost of a homogeneous system (*e.g.* CMOS logic) integrated in each one of the three approaches described above is used for comparison. The technology node is assumed at 65 nanometers and processing is done at 200mm silicon wafers. For this example, the process yield per unit area for CMOS processing is considered at 90% per cm^2 and the yield for the 3D stacking process is assumed at 95%. The cost comparison among the three integration approaches is illustrated in Figure 3 for a system size that varies from 10 to 200 million gates. As shown in Figure 3, single die integration is cost efficient for a system size up to 70 million gates, for the example considered in this paper. For higher gate count the area of a single die becomes too large, die yield deteriorates, and the system cost increases. For 3D integration the system cost is lower due to the improved yield resulting from smaller die sizes. Furthermore, it is shown in Figure 3 that the improved yield of the D2W stacking of known-good-dies results in an overall lower system cost when compared to W2W stacking.

As shown, 3D integration has a positive effect on the die yield, especially for large systems. The developed IMEC 3D cost model can be used to analyse the trade-offs for each particular system implementation and determine an optimal integration strategy depending on system size.

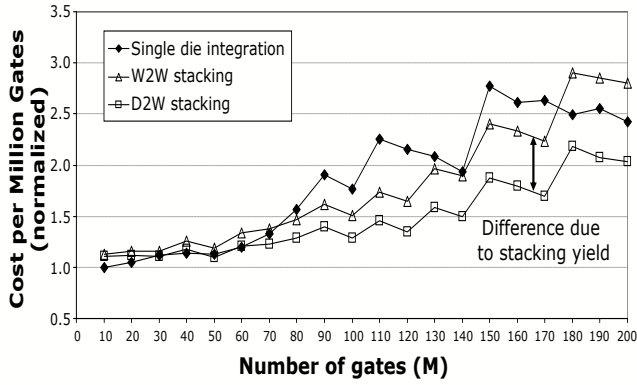


Fig. 3. Normalized integration cost for one million gates using different integration options.

IV. TSV INTEGRATION DENSITY

Different integration schemes exist for implementing the Through-Silicon-Vias. TSVs may be manufactured at different geometries, with different materials, and at different steps during the 3D process flow (*i.e.*, via first, via last, etc). Each TSV manufacturing scheme offers a different solution in terms of integration density and cost. In this section, an example on the impact of the TSV manufacturing schemes on the die size and therefore the system cost is presented.

Two different TSV integration schemes with different TSV diameters, aspect ratios, and integration densities are considered for comparison. In the first TSV scheme a *via middle* approach is assumed where the TSVs are fabricated after the active devices but before the interconnect metal layers – Stacked IC (3D-SIC) TSVs [15]. The diameter of a 3D-SIC TSV is considered at 5 micrometers and the minimum TSV pitch at 10 micrometers. These TSVs achieve high integration density and may be fabricated with a high aspect ratio between values 5 and 25. For the second TSV scheme a *via last* approach is considered where the TSVs are fabricated after the wafers are thinned by processing the backside of the wafer – Wafer level processing (3D-WLP) TSVs [17]. In this example the TSV diameter is 35 micrometers and the TSV pitch is 60 micrometers. The aspect ratio for the 3D-WLP TSVs is between 1.5 and 4 and the integration density is lower than the 3D-SIC TSVs. However the 3D-WLP processing cost is lower than the cost for processing the 3D-SIC TSVs.

To make a comparison between these two TSV implementation schemes, a 3D stacked system with a constant number of gates but variable TSV count is considered. The system is integrated in two stacked layers and the die size on both the top and bottom layer is the same. As in the example presented in Section III, the CMOS processing yield is assumed at 90% per cm^2 and the yield of the stacking process at 95%. The impact of the choice of TSV technology on the top and bottom die sizes is investigated by varying the total number of TSVs within the stacked system.

The effect on the size of the stacked dies is illustrated in Figure 4. It is shown that as the number of TSVs within a stack increases from 50 to 1,000,000, the top and bottom die sizes increase and the number of dies on a wafer drops. As shown in Figure 4, the number of dies per wafer is significantly reduced when 3D-WLP TSVs are used.

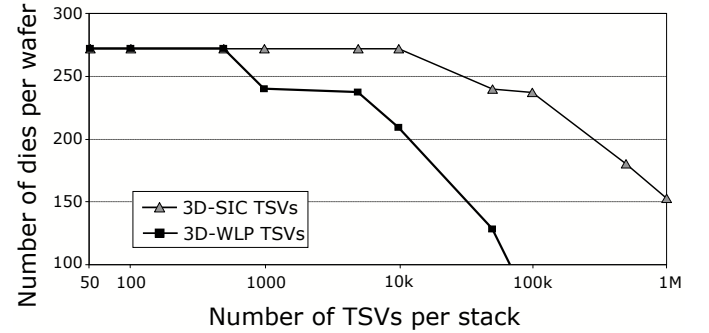


Fig. 4. Effect of TSV count per die on the number of dies per wafer.

Increasing the die size also impacts the system cost. This effect is illustrated in Figure 5, where the cost of stacks implemented with the 3D-SIC and 3D-WLP approaches are compared for a varying range of TSVs per stack. As shown in Figure 5, the lower integration density of the 3D-WLP TSVs makes the cost of this integration scheme prohibitive for a large number of vertical interconnects. In addition, two different stacking strategies, D2W and W2W are considered for each TSV fabrication technology. As illustrated in Figure 5, the lower stacking yield of the W2W stacking strategy results in a higher system cost for both the 3D-SIC and the 3D-WLP implementation schemes.

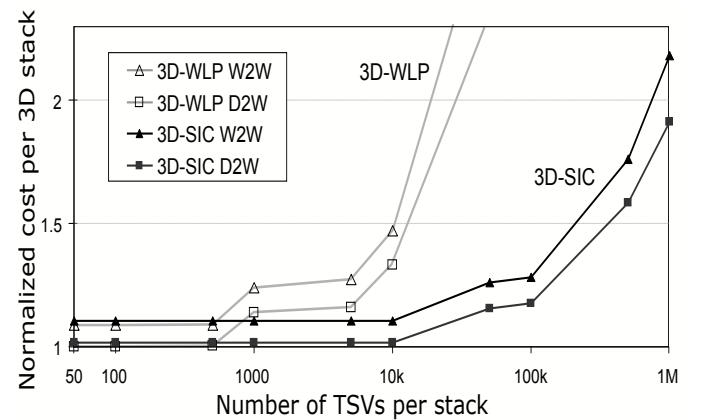


Fig. 5. Normalized cost of 3D system for a variable number of TSVs per stack.

V. TEST COST IN 3D SYSTEMS

Testing of an integrated system ensures that the final product offered to end customers meets the required quality specifications. Additionally, intermediate tests during the fabrication process of a system can avoid the additional processing of

faulty units, therefore reducing processing cost. For example, IC die testing prior to packaging can ensure that the additional cost of packaging is only spent on good dies, thus improving the efficiency of the packaging process.

In 3D integrated systems the principle of intermediate tests can also be applied by testing each individual die level prior to 3D stacking [18]. This is possible in Die-to-Die (D2D) and Die-to-Wafer (D2W) stacking approaches where the stacked dies are individually selected and placed on top of other dies within a stack. Using testing, only the known-good-dies at each level are selected for stacking thus improving the 3D stacking yield. In addition, testing of the entire stacked system can be performed prior to packaging to verify the quality of the overall stacking process and to avoid the packaging cost of faulty stacks.

The cost of testing of 3D systems is included in the developed 3D cost model by considering the overhead in die area, testing equipment, and processing time used for testing. It is assumed that flip-flop scan chains are used for testing each individual die level and also the entire 3D stack [19]. In addition, extra I/O pads are necessary on the upper level dies in a stack to provide access for test probes since it is assumed that probing on the TSV tips or TSV contact pads is not possible. The area overhead of the additional circuitry required for the scan chains and I/O pads is considered at each stacked die together with the overhead of the test processing time and test equipment cost.

To demonstrate the effect of 3D testing on system cost a two-level stacked system is considered. On both the top and bottom dies CMOS logic circuits are assumed at 65nm technology node and the D2W approach is used for selecting and stacking the dies. The KGDs at the bottom level are determined by testing at wafer level. It is assumed that the I/O pads of the entire system exist on the bottom die and are utilized for both the individual testing of the bottom die and the entire stack test after die bonding. The increase in the bottom die area due to the additional circuitry for the scan chains is taken into account for calculating the system cost. For the top level die three different testing options are considered:

- 1) *No testing*. The top level die is not tested and dies are stacked only on the top of KGDs at the bottom wafer. However, scan chains for testing exist on the top die that are used for testing of the entire stacked system. The access to those scan chains is provided through the TSVs after the stacking of the dies. No additional I/O pads are required on the top die and no test time overhead is necessary for individual die testing.
- 2) *Logic-Built-In-Self-Test (LBIST)*. Additional logic is included within the top level die that produces a large number of pseudo random test patterns used for individual scan-testing of the die [20], [21]. An additional area overhead of 5% of the logic die is assumed for generating the test patterns. A small number of extra I/O pads is also required to power the die for testing, initiate the test, and receive the test outcome once the test is completed. The fault coverage of the LBIST approach

is moderate: For the CMOS logic system used in this example, it is assumed that 90% of the total faults are detected.

- 3) *Reduced Pin Count Testing (RPCT)*. In this test approach a relative small number of test patterns are applied externally to the top level die [22]. These patterns are carefully computed to correspond with possible faults within the tested circuit structures. Therefore, circuit-specific faults are targeted and a good fault coverage of 99% is considered for this approach. No additional logic is necessary on-chip, however a large number of I/O pads may be required that is proportional to the number of scan chains in the die. Increasing the number of I/O pads provides parallel access to scan chains thus reducing the testing time. There is a trade-off between the faster test time achieved by increasing the number of scan chains and the increase in die size due to additional I/O pads. Using the 3D cost model the optimum number of scan chains can be evaluated. For the top level logic die considered in this example, an optimum number of 122 scan chains is determined.

The total cost of the 3D stacked system is evaluated for each one of the three different top die testing approaches for variable process yield per unit area, as illustrated in Figure 6. As shown in Figure 6, for very high values of process yield, where the probability of a circuit fault is low, the no testing approach for the top level die results at the lowest system cost. However as the process yield drops, the additional cost required for 3D testing pays off and the overall system cost is reduced when compared with the no-testing approach. The cost break-even points among the three testing strategies are also presented in Figure 6. It is shown that for the particular circuit considered in this example, the RPCT testing approach is more cost effective than no testing when process yield drops below 95.5%. The corresponding break-even point between the LBIST and the no testing costs is at process yield of 93.8%. It is also shown in Figure 6 that for the example considered here, RPCT testing is always more cost efficient than LBIST due to

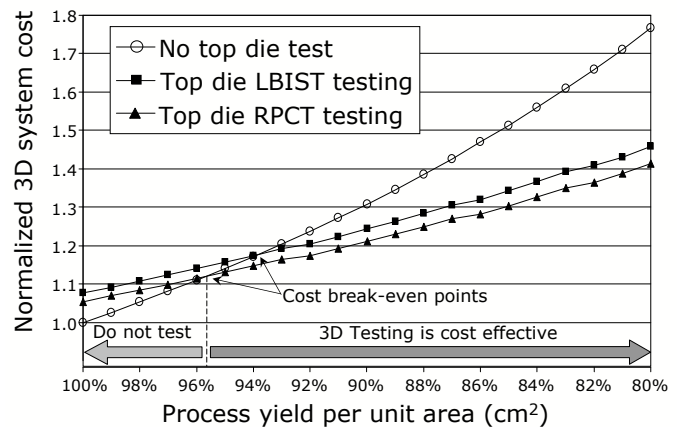


Fig. 6. Total cost per 3D system for different 3D testing strategies.

the additional area overhead on the top die for the generation of the LBIST test patterns.

VI. CONCLUSIONS

The 3D cost model developed at IMEC and its application in investigating cost trade-offs in 3D design are presented in this paper. The IMEC 3D cost model is based on real 3D process flows that are developed at IMEC. It is built in a modular way that allows evaluation of alternative processing steps and pathfinding of future 3D integration flows by calculating the corresponding manufacturing costs. The choice of 3D integration technology can significantly affect the cost of a system depending on the total system size and the TSV density. Also the effect of different 3D testing strategies on the overall system cost is demonstrated using the IMEC 3D cost model. It is shown that the additional cost for individual die testing can be compensated by the resulting improvements in stacking yield.

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