

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE Technology Group Co., Ltd.,
Petitioner,

v.

Paneltouch Technologies LLC,
Patent Owner.

U.S. Patent No. 8,704,762
Original Issue Date: April 22, 2014
Title: DISPLAY DEVICE

Case No. IPR2025-01482

**DECLARATION OF RICHARD A. FLASCK, M.S.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 8,704,762**

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I. INTRODUCTION

I, Richard A. Flasck, declare as follows:

1. I have been retained by counsel for BOE Technology Group Co., Ltd. (“BOE”) in the above-captioned *inter partes* review as an independent consultant to offer opinions regarding the validity of the Challenged Claims in U.S. Patent No. 8,704,762 (the “’762 patent”).
2. In the preparation of this Declaration, I have confined my analysis to the materials and opinions that were available at the time of the preparation of this Declaration, supplemented with my own knowledge and experience in the field. Should new materials, analyses, or opinions be introduced subsequent to the filing of this Declaration, I reserve the right to provide supplementary declarations to the extent necessary to address any such newly introduced items.
3. If requested, I am prepared to explain in a deposition or at a trial before the Patent Trial and Appeal Board (the “Board”) the technology disclosed in the ’762 patent, including the state of the art in 2010, the earliest possible priority date of the ’762 patent. Similarly, I am prepared to explain the technology disclosed in the prior art references cited herein. This may include, among other things, background information on the fields of display devices and touch panels.

II. QUALIFICATIONS AND COMPENSATION

4. My qualifications to testify as an expert in display devices and touch panels are set forth in my *curriculum vitae*, attached as Exhibit 1022. I have decades of experience as a scientist and consultant in the display device and touch panel fields.

5. I received a Bachelor of Science in Physics from the University of Michigan, Ann Arbor in 1970. After receiving my bachelor's degree, I was employed as a scientist and manager from 1970 through 1982 by Energy Conversion Devices, Inc., where my work focused on the development of electroluminescent displays, thin film transistors, thin film photovoltaics, ablative imaging films, non-volatile memory, multi-chip modules, and superconducting materials.

6. I received a Master of Science in Physics from Oakland University in Rochester, Michigan, in 1976. After completing my master's degree, I continued my employment with Energy Conversion Devices, Inc. until 1982.

7. After leaving Energy Conversion Devices, I founded and served as CEO of Alphasil, Inc., where I developed amorphous silicon thin film transistor (TFT) active-matrix liquid crystal displays ("AMLCDs"). My work at Alphasil included thin film transistor array substrate process and circuit design, data driver and gate driver design, scalars, video circuits, gamma correction circuits, backlighting, and inverter design. At Alphasil, I also designed and incorporated touch panel screens

into active-matrix display devices. The touch panel technologies included resistive and capacitive sensing. I worked at Alphasil from 1982 through 1989.

8. I am the founder and Chief Executive Officer of RAF Electronics Corp. (“RAF”), a company that I established after leaving Alphasil, Inc. (“Alphasil”) in 1989. At RAF, I have developed and patented Liquid Crystal on Silicon (“LCOS”) microdisplay projection technology using active-matrix transistor arrays, as well as proprietary Light Emitting Diode (“LED”) based Solid State Lighting (“SSL”) products. My work at RAF has also included the development of High-Definition Television (“HDTV”) projection technology, including transistor array substrates for LCOS devices and the associated optical systems, as well as advancements in lighting systems using both traditional LED and OLED (Organic Light Emitting Diode) technologies. In 2016, I was granted a patent, U.S. Patent No. 9,328,898, which covers LED and OLED technology and lighting systems, and in 2019, RAF received a CalSEED grant—an early-stage funding award provided by the California Energy Commission, the state’s primary agency for energy policy and innovation—to develop ultra efficient lighting products and explore options on establishing a Central Valley manufacturing facility.

9. From 2002 to 2007, I also served as a co-founder and Chief Operating Officer of Diablo Optics, Inc., where I developed, produced, and commercialized key optical components for HDTV projectors, such as polarization optics,

condenser lenses, projection lenses, and ultra-high performance optical interference filters using thin film stacks in conjunction with LED and thin film transistor arrays and devices.

10. Between 1997 to 1999, I held the positions of President and Chief Operating Officer at Alien Technology Corporation, where I was responsible for completing a Defense Advanced Research Projects Agency (“DARPA”) contract and implementing MicroElectroMechanical (“MEM”) fluidic self-assembly (“FSA”) technology for flat panel displays. I left that position in 1999.

11. I have over fifty-five years of professional experience focused heavily on the design and development of flat panel displays, transistor array substrates, touch panels, and OLED and LED devices.

12. I am listed as an inventor on twenty-six patents issued in the United States and foreign countries, including one United States design patent. My inventions concern technologies that include LED devices, semiconductor materials, glass materials, non-volatile memory cells, thin film transistors, flat panel backplanes and displays, and wafer based active matrices, and various transistor array substrates. I have also authored or co-authored more than 25 publications in journals and major international conference proceedings, many of which are specifically related to displays, touch screens, and the associated thin film

technologies. My *curriculum vitae* (Exhibit 1022) lists these articles, conference presentations, and patents.

13. I am also a member of several professional organizations, including Optica (formerly the Optical Society of America (“OSA”)), the International Society for Optics and Photonics (“SPIE”), the Audio Engineering Society (“AES”), the Society for Information Display (“SID”), and the Institute of Electrical and Electronics Engineers (“IEEE”).

14. I have served as an expert witness in over sixty patent cases, written scores of expert reports and declarations, and testified in district courts or before the International Trade Commission (“ITC”) eight times. Since 2019, I have also served as an expert witness in eight Patent Trial and Appeal Board (“PTAB”) proceedings involving touch panel screen technology.

15. My *curriculum vitae* contains further details regarding my experience, education, publications, and other qualifications that support my ability to render expert opinions in connection with this proceeding.

16. I am being compensated for my work in this matter at an hourly rate of \$495 for consulting services.

17. My compensation is not contingent upon the opinions I render or the outcome of this proceeding.

III. MATERIALS CONSIDERED

18. In preparing this Declaration, I reviewed and considered the following materials, along with any other documents referenced in the body of my Declaration:

- U.S. Patent No. 8,704,762 (the “’762 patent”), Ex. 1001;
- Prosecution History of U.S. Patent No. 8,704,762, Ex. 1002;
- Japanese Patent Publication No. JP 2006-171386A (“Miyagawa”) and certified translation, Ex. 1004;
- U.S. Patent Application Publication No. 2008/0074594A1 (“Tanabe”), Ex. 1005;
- U.S. Patent Publication No. 2009/0322704A1 (“Anno ’704”), Ex. 1006;
- U.S. Patent Publication No. 2009/0244021A1 (“Matsuo”), Ex. 1007;
- Japanese Patent Publication No. JP 2009-053390A (“Nakamura”) and certified translation, Ex. 1008;
- U.S. Patent Application Publication No. 2010/0220071A1 (“Nishihara”), Ex. 1009;
- U.S. Patent Application Publication No. 2009/0231516A1 (“Okada”), Ex. 1010;
- U.S. Patent Application Publication No. 2011/0007251A1 (“Yamamoto”), Ex. 1011;
- U.S. Patent Application Publication No. 2011/0226726A1 (“Song”), Ex. 1012;

- U.S. Patent Application Publication No. 2010/0134137A1 (“Kida”), Ex. 1013;
- U.S. Patent Application Publication No. 2006/0038580A1 (“Hasegawa”), Ex. 1014;
- U.S. Patent Application Publication No. 2008/0062373A1 (“Kim”), Ex. 1015;
- European Patent Specification No. EP1533848B1 (“Chung”), Ex. 1016;
- U.S. Patent Application Publication No. 2010/0123592A1 (“Nurmi”), Ex. 1017;
- Wiley Electrical and Electronics Engineering Dictionary (2004), Ex. 1018;
- Microsoft Computer Dictionary (5th ed.) (2002), Ex. 1019;
- U.S. Patent Publication No. 2008/0158453A1 (“Segawa”), Ex. 1020;
- U.S. Patent Publication No. 2010/0085326A1 (“Anno ’326”), Ex. 1021;
- U.S. Patent Publication No. 2008/0007538A1 (“Kotera”), Ex. 1023;
- U.S. Patent Publication No. 2004/0141110A1 (“Yu”), Ex. 1024;
- U.S. Patent Publication No. 2001/0005200A1 (“Suzuki”), Ex. 1025;
- Den Boer, “Active Matrix Liquid Crystal Displays” (2005), Ex. 1026.

19. I may use these documents and information, or other information obtained during the course of this proceeding, as well as representative charts, graphs, schematics and diagrams, animations, and models based on those documents and information, to support and to explain my testimony.

20. My opinions are based in part on a review and analysis of the above-mentioned documents and materials. I have also drawn on my education, experience, and knowledge of basic engineering and scientific principles in forming my opinions.

IV. UNDERSTANDING OF THE LAW

21. I am not an attorney, but I have been informed of several legal principles, which I have employed when forming my opinions in this Declaration. I have been informed and understand that each patent claim is considered separately for purposes of validity and that a dependent claim that depends from another claim includes all of the limitations of the claim it depends from.

A. Claim Construction

22. I have been informed and understand that the claims of the challenged patents in this proceeding are to be construed using the same claim construction standard that is applied in district court. I have been informed and understand the claim construction analysis begins with the ordinary meaning of a claim term, and there is a presumption that the term carries its plain and ordinary meaning to persons of ordinary skill in the art (“POSITA”) as of the effective filing date of the patent. I have also been informed and understand that the most important sources for determining the meaning of a claim term are the claims, the specification, and the prosecution history of the patent at issue, which collectively is called “intrinsic

evidence.” I have been further informed and understand that the meaning of a claim term may also be guided by “extrinsic evidence,” such as contemporaneous dictionaries and treatises.

B. Burden of Proof

23. I have been informed and understand that the petitioner in an *inter partes* review bears the burden of establishing invalidity by “a preponderance of the evidence.” I have been further informed and understand that, to prove an assertion by “a preponderance of the evidence,” the party with the burden of proof must demonstrate that it is more likely than not that the assertion is true.

C. Obviousness

24. I have been informed and understand that a patent claim is invalid if it would have been obvious to a POSITA at the time of the claimed invention. I have been further informed and understand that a claimed invention is not patentable if differences between it and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the pertinent art. I have been informed and understand that factors relevant to the determination of obviousness include the scope and content of the prior art, the level of ordinary skill in the art at the time of the invention, differences between the claimed invention and the prior art, and “secondary considerations” or objective indicia of non-obviousness.

25. I have been informed that a single reference alone can render a patent claim obvious, if any differences between the reference and the claim would have been known or obvious to a POSITA at the time of the invention. That is, if a POSITA could have adapted the reference to meet the claims of the patent by applying known concepts to achieve the expected results, then the patent claims are rendered obvious by that reference.

26. I have been informed and understand that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I have been further informed and understand that when a patent claim simply arranges old elements, with each performing the same function it had been known to perform, and yields no more than one of ordinary skill would expect from such an arrangement, the combination is obvious.

27. I have been informed and understand that a patent claim composed of several limitations is not obvious merely because each limitation was independently known in the prior art. Hindsight reasoning is not an appropriate basis for combining references to form an obviousness combination. I have been further informed and understand that it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine multiple prior art references.

28. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that even strong evidence of secondary considerations may not be sufficient to rebut a strong showing of obviousness. I have been informed that the patentee bears the burden of showing the existence and effect of secondary considerations of non-obviousness, after which the burden of coming forward with rebuttal evidence shifts to the party arguing obviousness. I have been informed that the following secondary considerations may indicate non-obviousness:

- Copying: evidence that others, including an accused infringer, copied the patented invention.
- Long-standing problem or need: evidence of a persistent problem or need in the art that was resolved by the patented invention.
- Prior failure: evidence that others have tried and failed to solve the problem or failed to provide the need resolved by the claimed invention.
- Commercial acquiescence of competitors: the willingness of industry to license the patent at issue.
- Skepticism: evidence that those of ordinary skill in the art were skeptical as to the merits of the invention.
- Praise: evidence of praise directed to an invention by others in the field.

- Unexpected results: evidence that those of ordinary skill in the art were surprised by the capabilities of the claimed invention.

29. I have also been informed that the near-simultaneous invention by others can be evidence that a claimed invention is obvious. I have further been informed and understand that the patentee bears the burden of showing a “nexus” between the claimed invention and the evidence proffered on secondary considerations (*e.g.*, proof of commercial success of a product that practices the claimed invention is not enough; there must be evidence that the commercial success resulted, at least in part, from the claimed invention).

D. Priority Date

30. I have been informed and understand that a U.S. patent may claim “priority” to the filing date of one or more earlier filed applications. I have been informed that the priority date, also called the “effective filing date,” is the earliest filing date to which a claim is entitled and that such date is relevant for determining what qualifies as prior art. I understand that a claim must have written description support in the application(s) to which it claims priority to be entitled to an earlier effective filing date. I have been informed that the priority date determination is done on a claim-by-claim basis and that claims in the same patent may have different priority dates.

31. I understand that when a U.S. patent or application is invoked as prior art, its effective filing date may be deemed to be the filing date of a related foreign

application when said related foreign applications discloses the same subject matter as said U.S. patent or application, and that a related U.S. application was filed within a year of the foreign application.

32. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

33. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the type of problems encountered in the art; (2) prior art solutions to those problems; (3) the rapidity with which innovations are made; (4) the sophistication of the technology; and (5) the education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art is also a person of ordinary creativity.

V. LEVEL OF SKILL IN THE ART

34. In light of the above factors relevant to determining the level of ordinary skill, I have developed an opinion on the appropriate level of ordinary skill in the art that I have applied in my analysis set forth in this Declaration. As explained below, the Challenged Patent pertains generally to the fields of displays and touch panels. A POSITA at the time of the alleged invention would have had at least a

bachelor's degree in electrical engineering, physics, or a similar discipline, along with at least two years of experience with display devices having touch panels.

Relevant experience can substitute for education and vice versa. I was, at all relevant times, at least a POSITA relevant to the Challenged Patent.

35. While it is my opinion that the above stated level of ordinary skill in the art is correct, my opinions set forth herein remain unchanged under a different articulation of the level of ordinary skill in the art. I reserve the right to explain how, if at all, my opinions would differ if the Patent Owner alleges that a different level of ordinary skill in the art should apply.

VI. SUMMARY OF OPINIONS

36. I have been asked to compare various prior art references to Claims 1-4, 6-10, and 12 of the '762 patent (the "Challenged Claims"). In my opinion, all Challenged Claims are unpatentable as obvious – based on these prior art references, combined with the knowledge of a POSITA.

37. My substantive analysis in Section X provides examples of why these prior art references render the Challenged Claims unpatentable. I reserve the right to cite and rely on additional portions of these references in any future declarations or depositions.

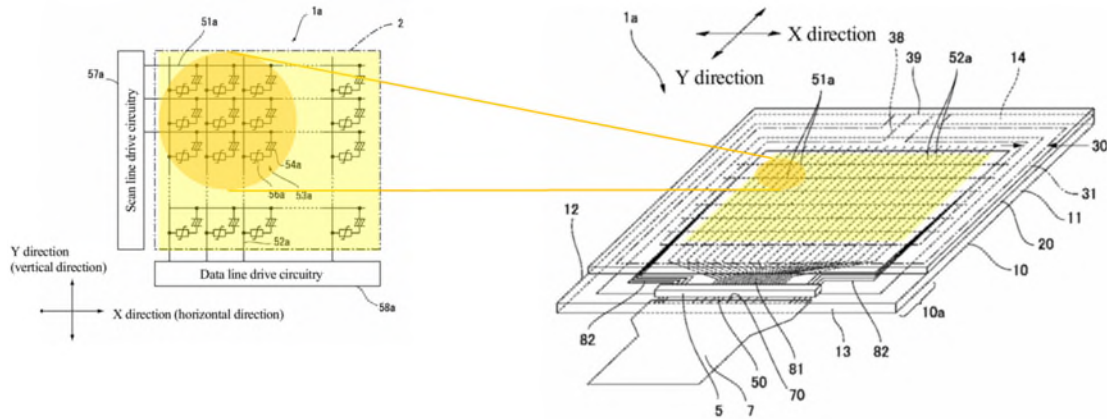
VII. TECHNOLOGY BACKGROUND

38. The purported invention of the '762 patent is related to display devices—such as liquid crystal displays (“LCDs”) and touch panels—commonly used in products like smartphones, tablets, laptops, and other electronic screens. The '762 patent describes structures and methods used to detect cracks and chips in display substrates.

39. Some background about the structure and manufacturing of displays is helpful to understand the purported utility and operation of the '762 patent disclosure. Flat panel displays, such as LCDs, are built from one or more substrates layered upon one another. In the case of LCDs, a layer of liquid crystal material is sealed between the substrates. Nakamura, [0003].

40. Display panels comprise an array of pixels that create the visuals seen on devices like TVs, monitors, smartphones, tablets, and laptops. A display's pixels are coupled through wirings around the array to components that provide the image signals for display. Pixels are connected to drive circuits via two types of wiring: scan lines and data lines. Scan lines are formed on the substrate, row-by-row, to select rows of pixels during operation. Data lines run perpendicular to the scan lines delivering image data signals to the pixels. Together, these lines enable the drive circuits to control each pixel on the panel. As shown in the image below, the scan and data lines are connected to wires (also called interconnect) around the

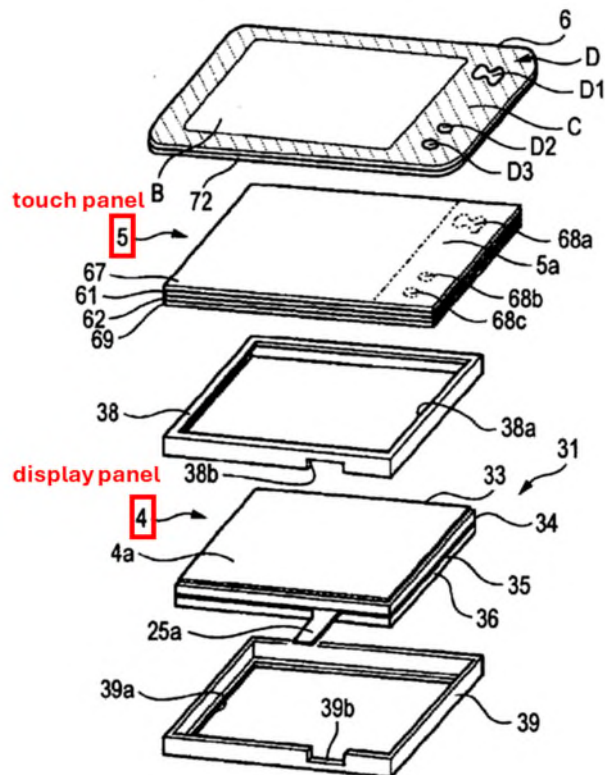
periphery of the substrate and to the components responsible for controlling the display and sending it image signals.



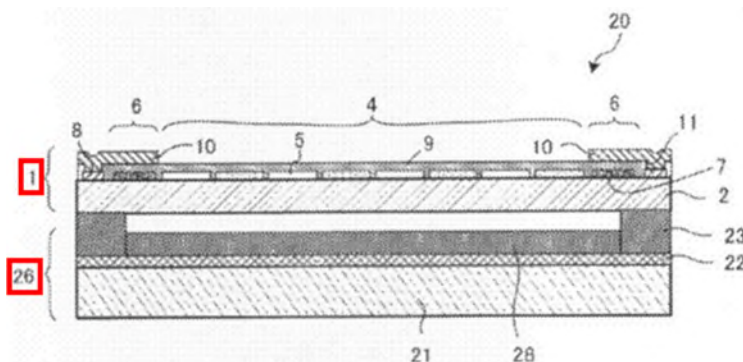
Miyagawa, Figs. 1–2; ¹ *see also id.*, Figs. 6–7; Ex. 1015, Fig. 4; Ex. 1020, Fig. 3.

41. The display device disclosed in the '762 patent may comprise a touch panel. Ex. 1001, Abstract. It was conventional to integrate display panels with touch panels in electronic devices. Anno '704, [0046]–[0048]. A touch panel 5 is added to a display panel 4 to function as a touch screen, as shown in the exploded view below from Kotera:

¹ All color annotations to figures herein are added.

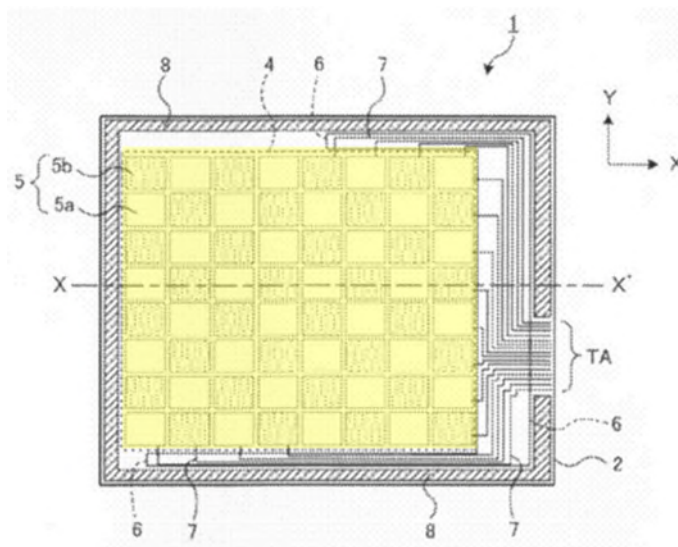


Ex. 1023, Fig. 3 (partial), [0024]. It was also well known in the prior art to tightly integrate the touch panel substrate with the display panel substrate. For example, the following cross-sectional view shows a common arrangement, with touch panel 1 above display panel 26:



Ex. 1009, Fig. 8, [0066].

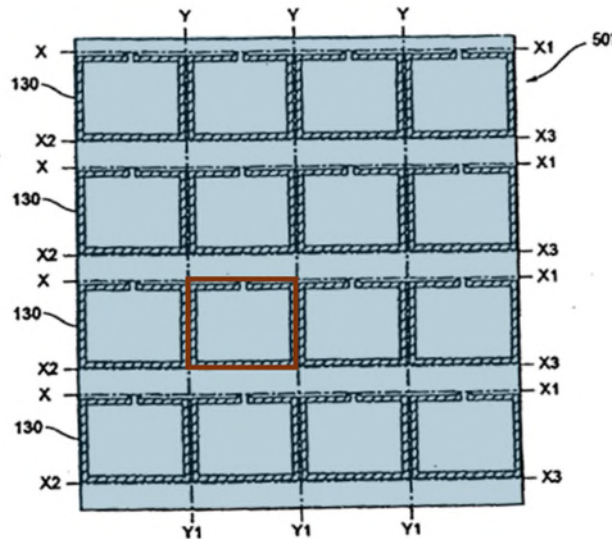
42. There are several types of touch panels, with capacitive and resistive types being most common. Ex. 1017, [0016]; Ex. 1024, [0006]–[0007]. Similar to the structure of display panels, touch panels typically have signal interconnect wirings in their periphery that connect with detection elements—such as detection electrodes (components within the detection region that sense contact positions)—within the touch sensing region of the panel:



Ex. 1009, Fig. 1A, [0042]–[0045]; *see also* Matsuo, Fig. 2 (capacitive); Ex. 1025, Fig. 2 (electrodes 6A–6B and 9A–9B and wiring lines 11A–11B of a resistive touch panel), [0032]–[0036]; Ex. 1026, 193–94 (resistive).

43. Manufacturers process large mother substrates (shaded below), typically made of glass and containing many individual display panels (one outlined in red below) or touch panels, as a batch to improve efficiency. After all the necessary

A cross-sectional view of a substrate assembly. A top layer, labeled 501, is positioned above a bottom layer, labeled 130. The top layer 501 has a central region with three vertical lines labeled Y and two side regions labeled X and X1. The bottom layer 130 is shown as a solid block.

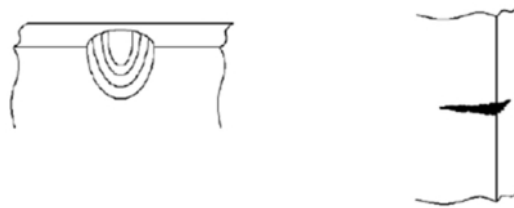


separately—one for the display’s addressing electronics and one for the color filter.

23

BOE Ex. 10
BOE v. Pa

substrate into individual panels, chips or cracks may form at the edges of the glass substrate. If such a defect occurs during the cutting process, wiring patterns and circuits that are positioned close to the edges are vulnerable to being damaged. As a result, chips or cracks can lead to broken or disconnected wiring, causing defects in an individual panel.

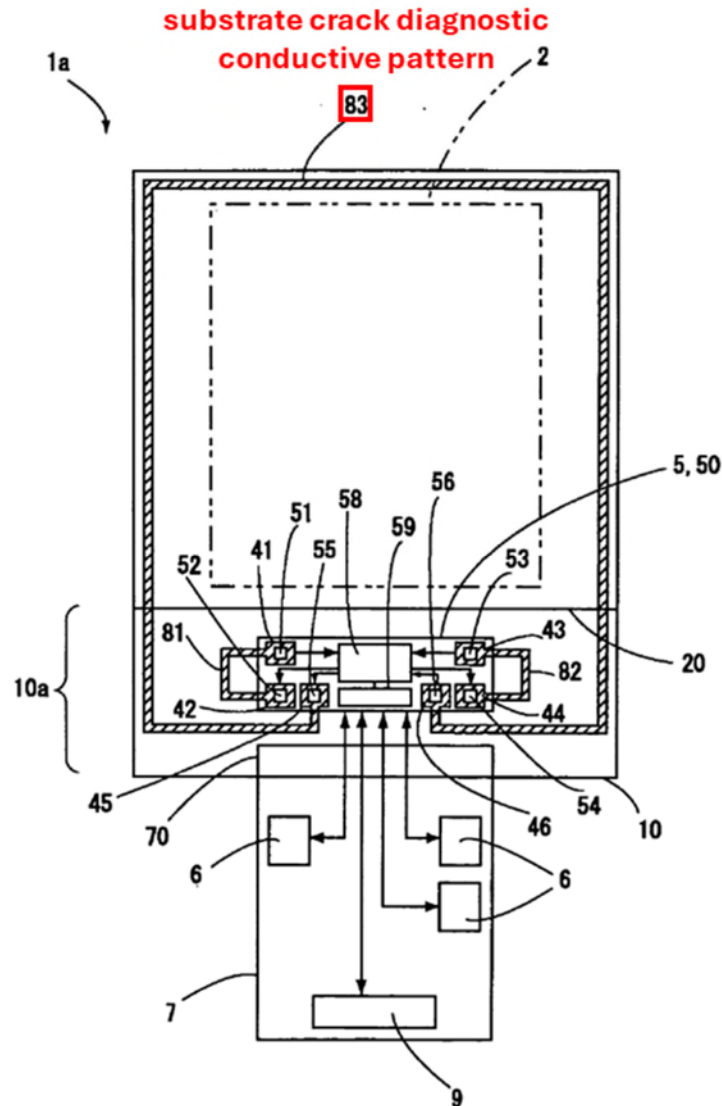


Nakamura, Figs. 9B–9C; *see also* Ex. 1013, [0006]–[0008].

45. It is advantageous to detect such defects early during manufacturing to avoid wasted time, effort, and components that would otherwise be spent on a defective panel. Nakamura, [0043]–[0044]. Crack detection can be performed either before or after the panel is assembled.

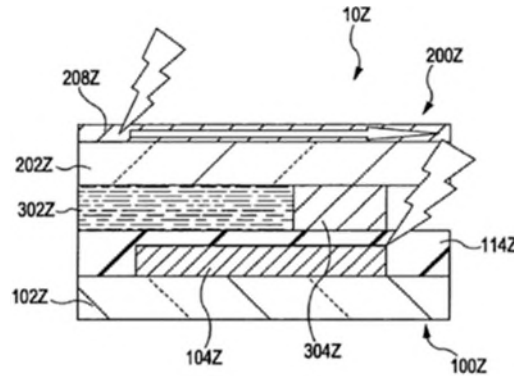
46. A typical crack detection technique uses a wire deposited on the mother substrate around the edges of each display or touch panel. After cutting, an electrical continuity check is performed by attempting to pass a current through the wire. The peripheral, crack detecting wire, is closer to the device edge than the operative interconnect wiring and other circuitry. If a current successfully passes through the crack detecting wire, it indicates no serious defects occurred during the cutting process. On the other hand, if a current does not pass through the crack

detecting wire, that indicates a crack or chip has broken the peripheral wire and likely damaged operative components, such as the interconnect wiring.



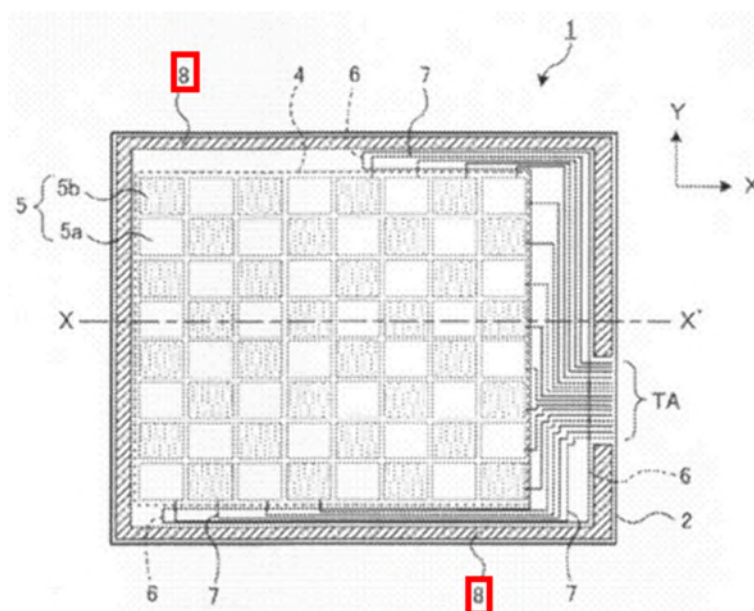
Ex. 1014, Fig. 4, [0051]–[0053]; *see also* Miyagawa, Fig. 3; Ex. 1017, Fig. 9, [0043].

47. Touch screens (display panels and touch panels) may also be subject to environmental stress, such as electrostatic discharge and other forms of electromagnetic noise, that could degrade or damage the panel.



Ex. 1020, Fig. 6 (illustrating electrostatic discharge).

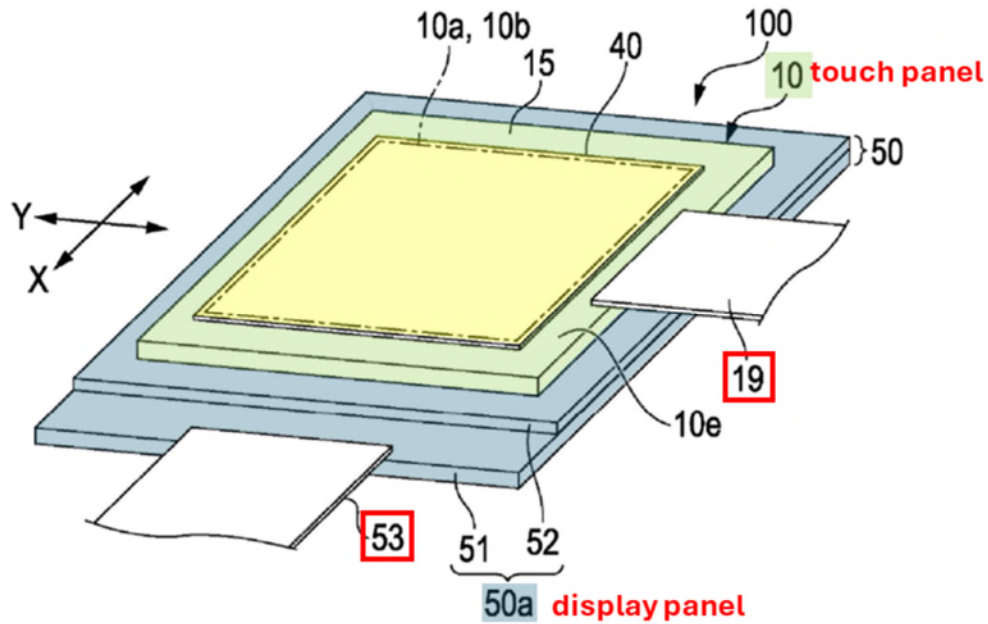
48. As shown in Nishihara, a wire (8) formed around the panel's peripheral edges protects it from such stress. Such environmental stress tends to affect the touch screens during post-manufacturing operations of the screen, for example, by end users.



Ex. 1009, Fig. 1A, [0043] (shield electrode 8); *see also* Ex. 1020, Fig. 3; Matsuo, Fig. 2; Ex. 1015, Fig. 2, [0032]–[0033]; Ex. 1016, Fig. 3, [0030]–[0031]. Like the crack detection wire, these shielding wires are simply a conductive trace run around the periphery of the substrate.

49. Structurally, wires used for crack detection and electrostatic and noise shielding are both a conductive trace run around the periphery of the substrate. Operationally, wires for crack detection are used in manufacturing and wires for shielding are used in operation. Therefore, these two types of wires are structurally similar or identical and are functionally compatible, and the same wire can perform both functions. This was recognized in the art by 2007, as Nakamura taught that a single wire could be used to perform both functions, stating that “each [of] defective line detection patterns D1 and D2 [for crack detection] may be formed using a conventional shield line and the like as typically formed.” Nakamura, [0041].

50. It was also routine to connect touch and display panels to control circuitry via flexible wiring boards or substrates (*e.g.*, ribbon cables) for signal and power transmission. For example, the flexible substrates 19 and 53 in Matsuo are respectively connected to touch and display panels in the device below:



Matsuo, Fig. 1.

51. Another example is provided in Anno '326, which describes using a flexible printed circuit board to connect a touch panel to control circuitry for transmitting signals from the control circuit to the panel. Ex. 1021, [0095]–[0097]; *see also* Nakamura, [0047]–[0048], [0051]. Control circuitry was commonly implemented using integrated circuit (“IC”) chips placed on a substrate of the panel, a flexible substrate, or on another component coupled to the flexible substrate. Miyagawa, [0020], [0040].

VIII. THE '762 PATENT

52. U.S. Patent No. 8,704,762 (“the '762 patent” or “the Challenged Patent”) is entitled “Display Device.” The '762 patent claims priority to foreign application JP 2010-126877, filed on June 2, 2010. For the purpose of this Declaration, I have

been instructed to use June 2, 2010 as the priority date of the '762 patent. My opinions in this Declaration were formed from the perspective of a POSITA as of June 2, 2010, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the prior art.

53. The '762 patent is related to “a technique of facilitating the inspection for signal interconnects [wirings] formed in the region outside detection and display areas for [a] display device.” Ex. 1001, 1:13–16. As I have mentioned above, according to the '762 patent, the prior art in the area already included LCD panels consisting of two glass substrates sandwiching a liquid crystal layer, with one substrate carrying the transistors and electrodes and the other containing color filters. *Id.*, 1:19–24. During manufacturing, the substrates were sealed together with the liquid crystal in between and then cut into individual panels. *Id.* 1:25–31. Touch panels, often attached to the display surface, included detection electrodes for sensing user input. Both the display and touch panels relied on signal interconnects (wirings) to function properly. The '762 patent itself acknowledges that these types of touch and display devices, as well as their basic structure and operation, were well established and considered conventional by 2010. *Id.*, 4:11–14.

A. Problem Addressed by the '762 Patent and the Alleged Invention

54. As I have just discussed, the '762 patent admits that a common manufacturing problem was that during the cutting process or subsequent handling, the glass substrates could chip or crack at the edges. *See* Ex. 1001, 1:51–60, 2:24–27. Such defects frequently resulted in the unintended breakage of signal interconnects located near the periphery of the panels that were difficult to detect, especially after assembly, when the interconnects were obscured by other layers. *See id.*, 2:7–23.

55. The '762 patent, like many other patents at the time, sought to solve this problem by introducing a dedicated detection interconnect: a thin conductive trace formed along the outer edge of the substrate, surrounding the functional wiring regions. *See, e.g., id.*, 2:53–60, 3:19–27. This detection interconnect was connected to electrode terminals at both ends, enabling a simple electrical test (such as measuring resistance) to quickly determine whether a crack or chip had severed the interconnect, thus providing a straightforward pass/fail indication without increasing manufacturing complexity. *See id.*, 2:30–2:34, 2:58–60, 3:23–25, 9:8–15.

B. Prosecution History of the '762 Patent

56. The '762 patent was filed as Application No. 13/151,362 ("362 application") on June 2, 2011, and claims priority from Japanese application JP 2010-126877 filed on June 2, 2010. Ex. 1001, Cover.

57. The '362 application, as filed, included claims 1-12. Ex. 1002, 44-48. On May 30, 2013, the Examiner issued a Non-Final Rejection, finding all claims of the '362 application obvious under 35 USC §103(a).*Id.*, 209-12. Specifically, the Examiner rejected all pending claims over U.S. Patent No. 7,034,442 ("Hirayama") in view of U.S. Patent Nos. 7,167,154 ("Sato") and 6,262,579 ("Chazan").

58. In response, Applicant amended claim 1, requiring the detection interconnect be "disposed along the peripheral edge of three sides of the transparent substrate." Ex. 1002, 223-24. Applicant similarly amended independent claim 7 to require the detection interconnect on "three sides" of the "transparent" substrate. *Id.*, 224-25.

59. The Examiner allowed the amended claims on December 02, 2013, after which the Applicant submitted an additional Information Disclosure Statement with a copy of Nakamura in Japanese. *Id.*, 241-250, 261-262, 308-323. The '762 patent was issued on April 22, 2014. Ex. 1001, Cover.

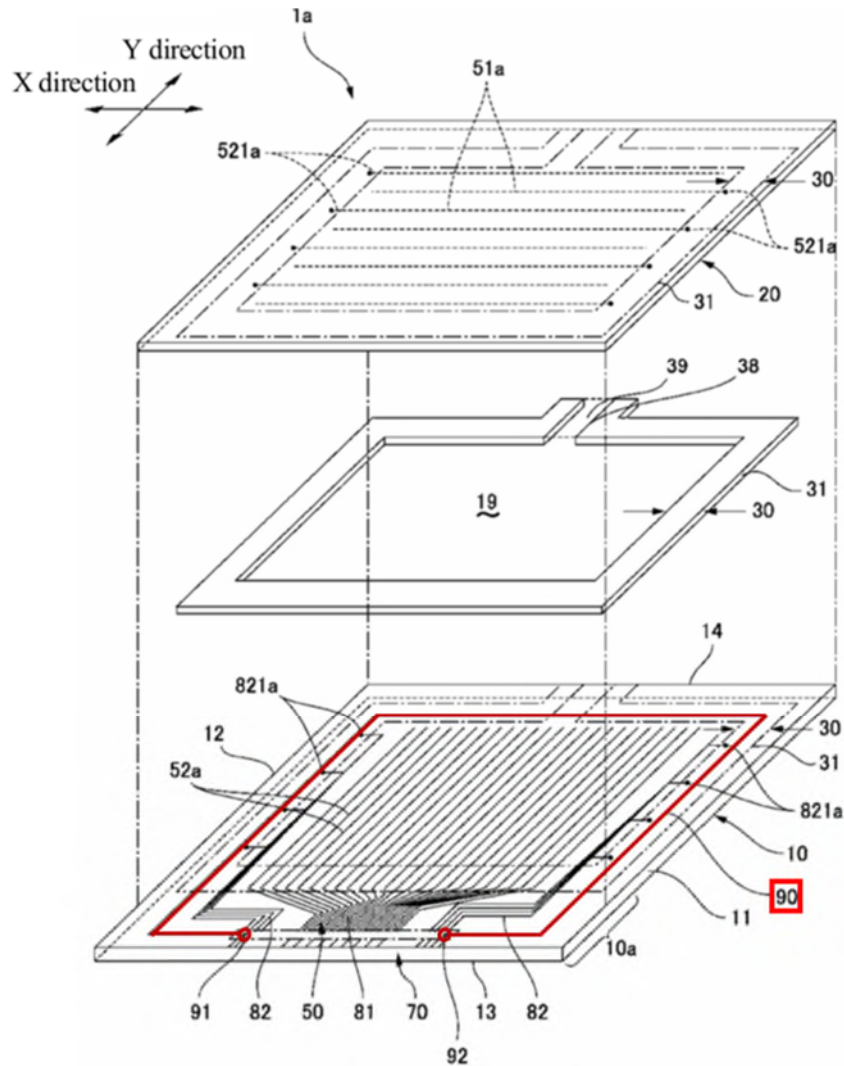
C. Claim Construction

60. In my opinion, the claims of the '762 patent should be interpreted according to their plain and ordinary meaning as understood by a POSITA. It is my view that claim construction is not necessary for the purpose of this IPR.

IX. PRIOR ART REFERENCES**A. Miyagawa**

61. Miyagawa, titled "Electro-optical device and electronic apparatus," was filed on December 16, 2004, published on June 29, 2006. Miyagawa at (22), (43).

62. Miyagawa discloses LCD displays "capable of properly diagnosing a defect caused by a substrate crack even at a mid-manufacturing stage, and ... easily identify ... the cause of the defect is a substrate crack." *Id.*, Abstract. In particular, Miyagawa teaches placing a diagnostic wiring around the edges of the display panel substrate; if this wire is damaged, it becomes electrically discontinuous, signaling the presence of a crack. *Id.* Miyagawa's diagnostic wiring is placed around the display-panel substrate as shown below:



Id., Fig. 3.

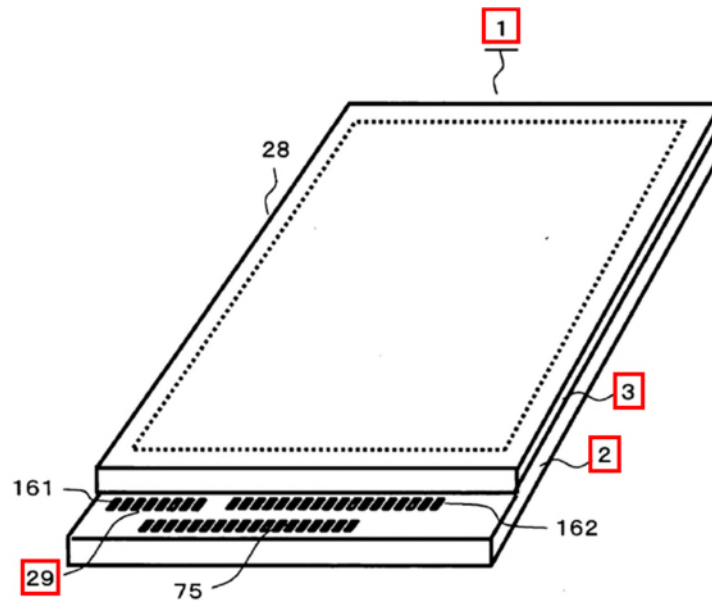
B. Tanabe

63. Tanabe, titled “Display Device,” was filed on September 11, 2007, published on March 27, 2008, and claims priority to a Japanese patent application filed in 2006. Tanabe at (22), (30), and (43).

64. Tanabe describes LCD displays with improved structural uniformity.

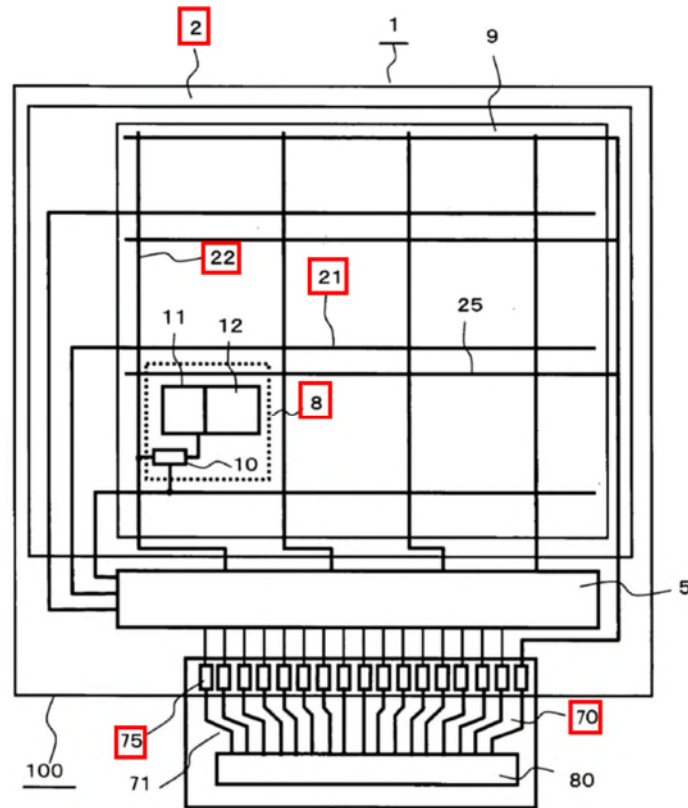
Tanabe, [0023]–[0024]. In Tanabe’s LCD display 1, a TFT (thin film transistor)

substrate 2 is positioned below an opposing substrate 3. The TFT substrate is extended on one side to form a terminal connection portion 29 on the bottom:



Id., Fig. 2, [0059].

65. Tanabe's TFT substrate 2 includes "gate signal lines (also called scan lines) 21" and "drain signal lines (also called video signal lines) 22," which deliver signals to pixel portions 8. *Id.*, [0056], [0058].



Id., Fig. 1.

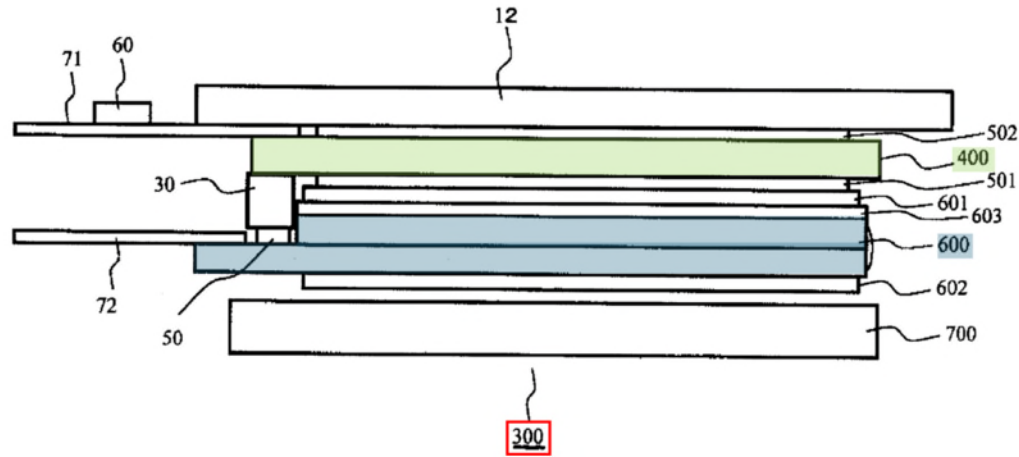
66. These signals are routed from outside of the LCD panel through a flexible substrate 70, and then enter the TFT substrate via terminals 75. *Id.*, [0054].

C. Anno '704

67. Anno '704, titled "Display Device with Touch Panel," was filed on June 29, 2009, published on December 31, 2009, and claims priority to a Japanese patent application filed in 2008. Anno '704 at (22), (43).

68. Anno '704 and the challenged '762 patent share a common inventor, Kouichi Anno; however, the Anno '704 reference was not cited during prosecution of the '762 patent. Anno '704 at (75); '762 patent at (75), (56). Anno '704

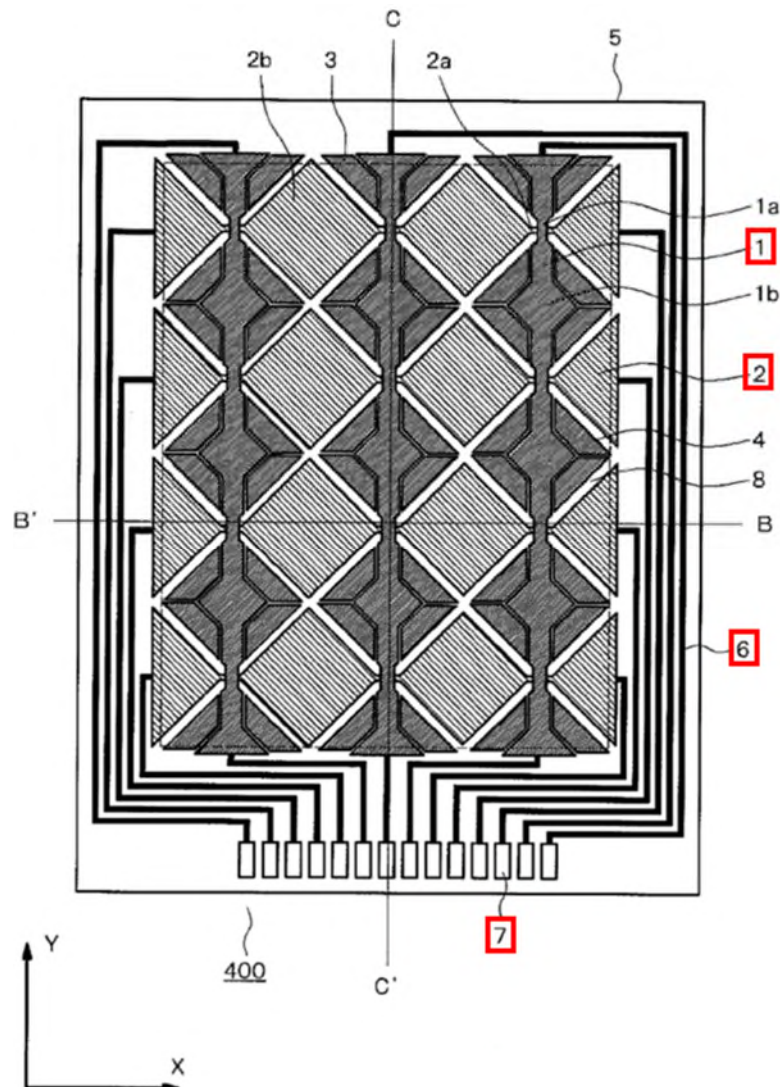
discloses a touch display 300, comprising a touch panel 400 stacked on top of an LCD panel 600. Anno '704, Abstract, [0048].



Id., Fig. 2.

69. The touch panel also includes electrodes 1–2 coupled to connection terminals 7 via the wiring lines 6 formed along the outer periphery of the substrate.

Id., [0059]–[0061]; *id.*, [0079] (“peripheral wiring lines 6”).

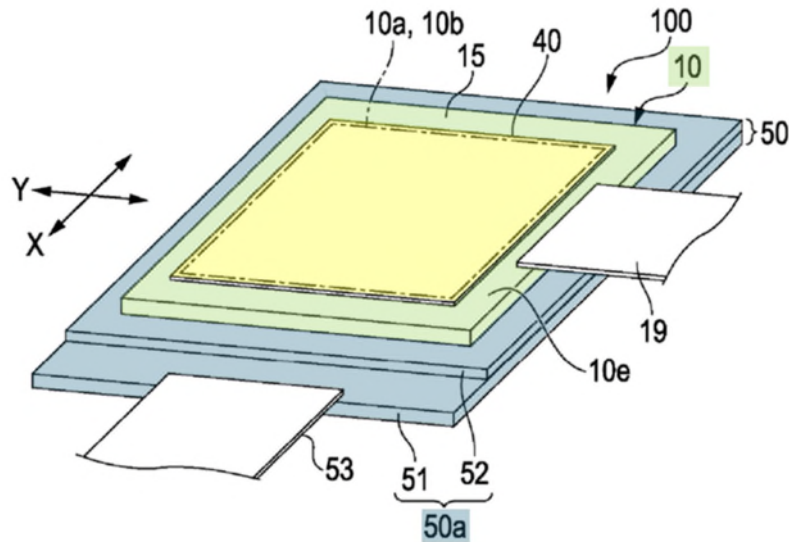


Id., Fig. 3.

D. Matsuo

70. Matsuo, titled “Electrical Capacitance Input Device, Display Apparatus with Input Function and Electronic Apparatus,” was filed on February 24, 2009, published on October 1, 2009, and claims priority to a Japanese patent application filed in 2008. Matsuo at (22), (30), (43).

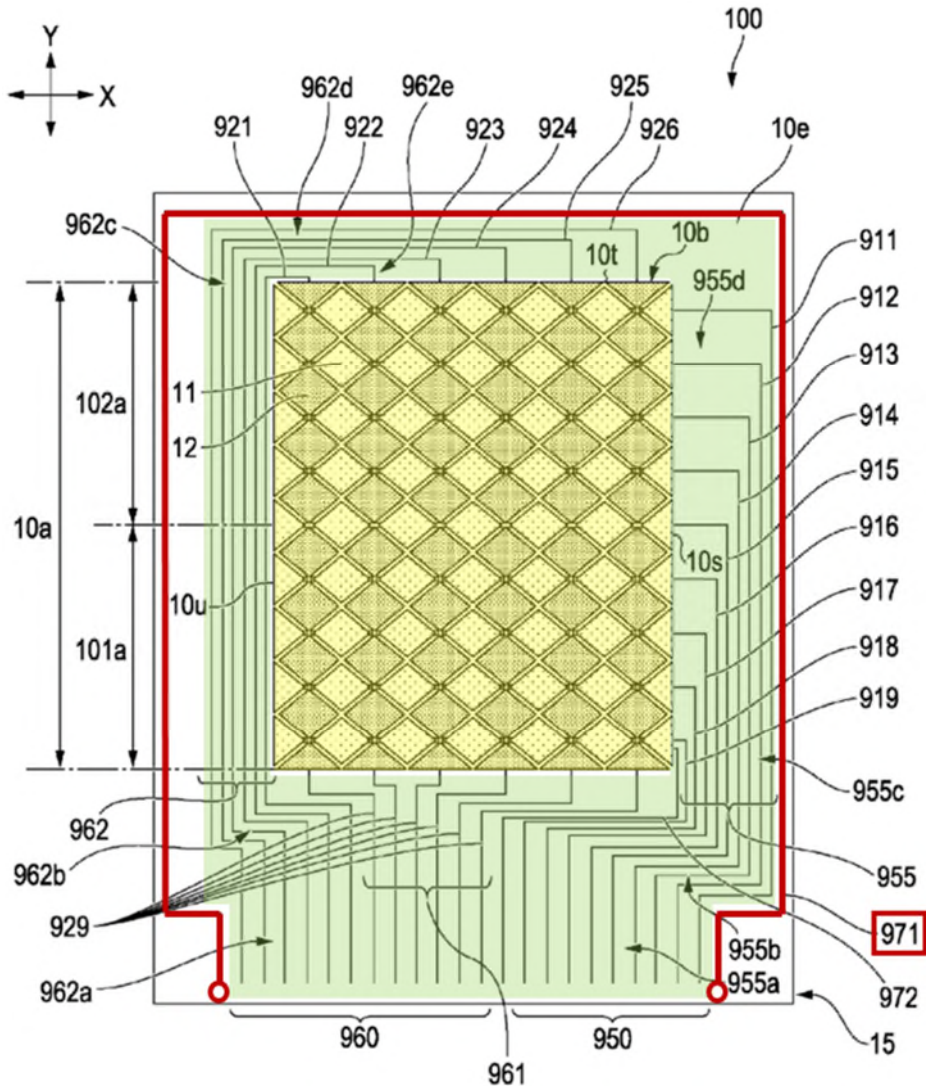
71. Matsuo describes a touchscreen device, in which a touch panel is stacked on top of a display panel. See Matsuo, [0038].



Id., Fig. 1.

72. The touch panel includes an auxiliary wiring positioned around its edges.

Id., [0054]–[0056].



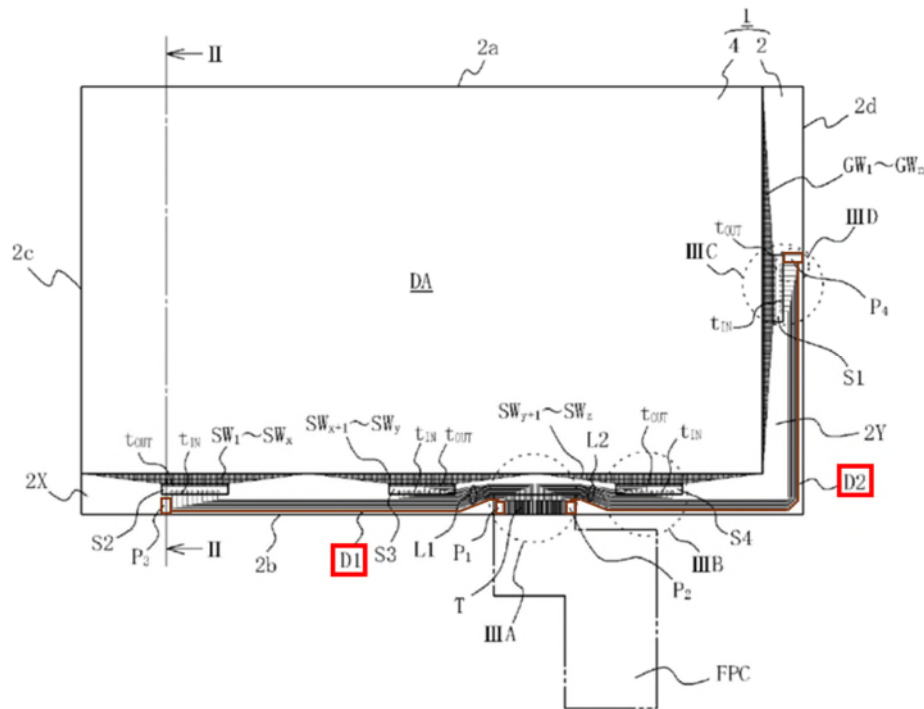
Id., Fig. 2.

73. The auxiliary wiring protects the panel from external noise, thereby preserving the sensitivity of touch detection. *Id.*, [0046], [0056], [0077].

E. Nakamura

74. Nakamura, titled “Electro-Optical Panel, Panel Inspection Method, and Electronic Apparatus,” was filed on August 27, 2007 and published on March 12, 2009. Nakamura at (22), (43).

75. Nakamura describes LCD displays that include a defective line detection pattern “disposed on the peripheral edge of a panel substrate,” allowing inspection for defects before an IC chip is installed. Nakamura, Abstract. A broken detection pattern, as revealed through an electrical discontinuity, can indicate damage to the functional wiring inside of the detection pattern. *Id.*



Id., Fig. 1.

76. Nakamura also notes that this pattern, *i.e.*, a panel-crack-detection line, “may be formed using a conventional shield line.” *Id.*, [0041].

X. INVALIDITY ANALYSIS

77. As explained in detail in my analysis below, it is my opinion that the Challenged Claims of the '762 patent are invalid.

A. Ground 1 – Miyagawa Renders Obvious Claims 7–10 and 12

78. In my opinion, Miyagawa renders Claims 7-10 and 12 of the '762 patent obvious.

1. Independent Claim 7

79. In my opinion, Miyagawa renders obvious Claim 7 of the '762 patent.

a) 7[pre]

80. In my opinion, Miyagawa discloses “*a display device*” – referred to as an electro-optical device 100b.²

81. Miyagawa explains that its electro-optical device is suitable for use in both “direct-view display devices and projection type display devices.” Miyagawa, [0012]. Miyagawa further describes that such devices encompass “an active matrix type liquid crystal device using a thin film transistor (TFT). . . .” *Id.* [0042]–[0043].

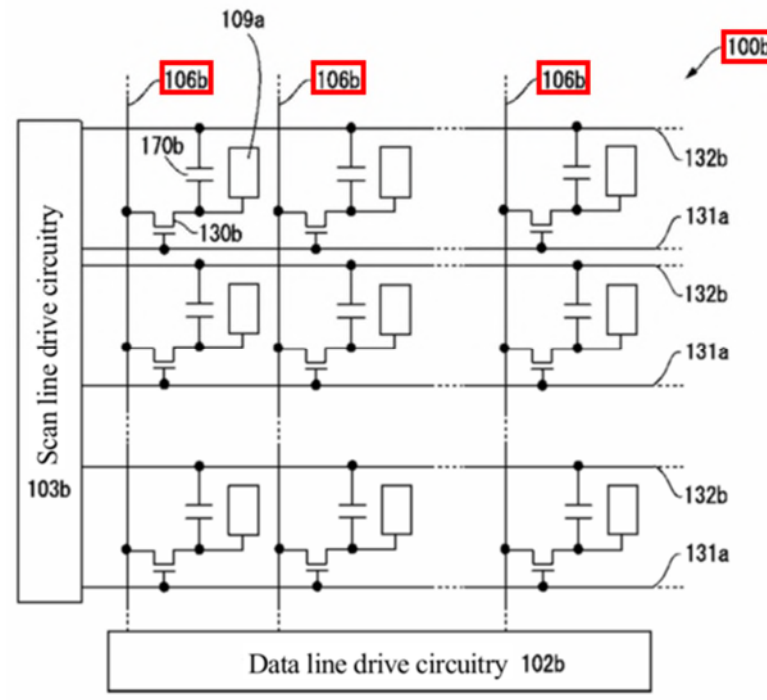
b) 7[a.1]

82. In my opinion, Miyagawa discloses a display device that includes “*a transparent substrate formed with a plurality of video signal lines.*”

83. Specifically, Miyagawa discloses a transparent substrate, referred to as a “TFT array substrate,” is formed with a plurality of video signal lines, referred to

² Red *italics* denote verbatim claim language covered in the present limitation-by-limitation section.

as “data lines 106b.” Miyagawa, [0043]–[0044]. Miyagawa’s Figure 6 shows the arrangement of these video signal lines, below:



Id., Fig. 6.

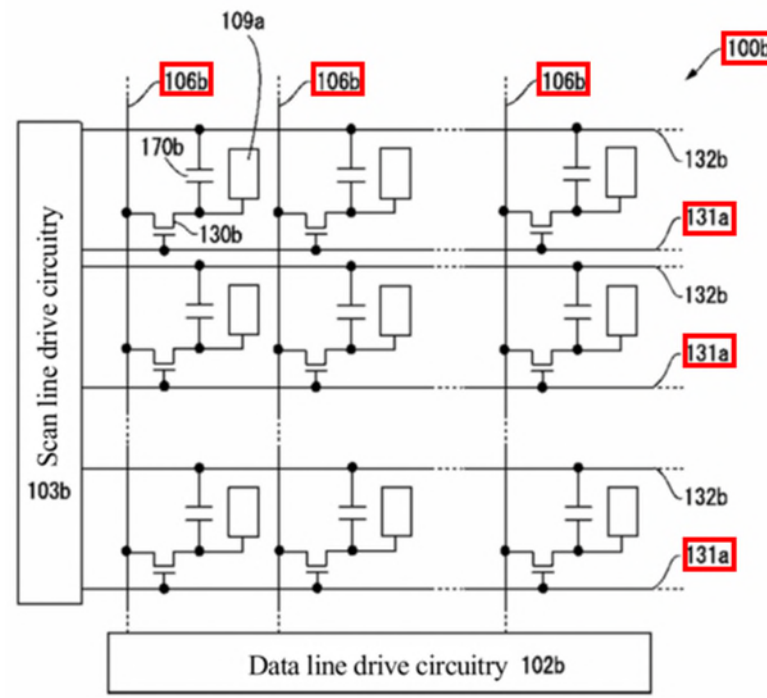
84. Similar to Miyagawa’s first embodiment, the TFT array substrate of Miyagawa’s other embodiments is transparent, allowing backlighting originating beneath it to pass through the liquid crystal layer above it. *See id.*, [0044], [0017]; *see also id.*, [0020] (backlighting). The ’762 patent admits that transparent substrate made of glass was well known. Ex. 1001, 5:36–40.

85. These data lines are fabricated on the TFT array substrate and receive image signals. *Id.*, [0043]–[0044].

c) 7[a.2]

86. In my opinion, Miyagawa discloses “*a transparent substrate formed with³ ... a plurality of scanning signal lines intersecting the video signal lines.*”

87. Specifically, Miyagawa discloses a display device that includes a “transparent substrate” (TFT array substrate), on which “a plurality of scanning signal lines” (scan lines 131b) are formed and arranged to intersect “the video signal lines” (data lines 106b).



Miyagawa, Fig. 6.

³ *Blue italics* show claim limitations first recited in a prior claim limitation.

88. Scan lines 131b in Miyagawa's specification is identified as scan lines 131a in Figure 6. This is merely a typographical difference, immaterial to Miyagawa's teaching of the scan lines. I refer to them as 131b in this Declaration.

89. As shown above in Figure 6, both the scan lines 131b and the data lines 106b are formed on the TFT array substrate and arranged to intersect. *Id.*, [0044], Fig. 6.

d) 7[a.3]

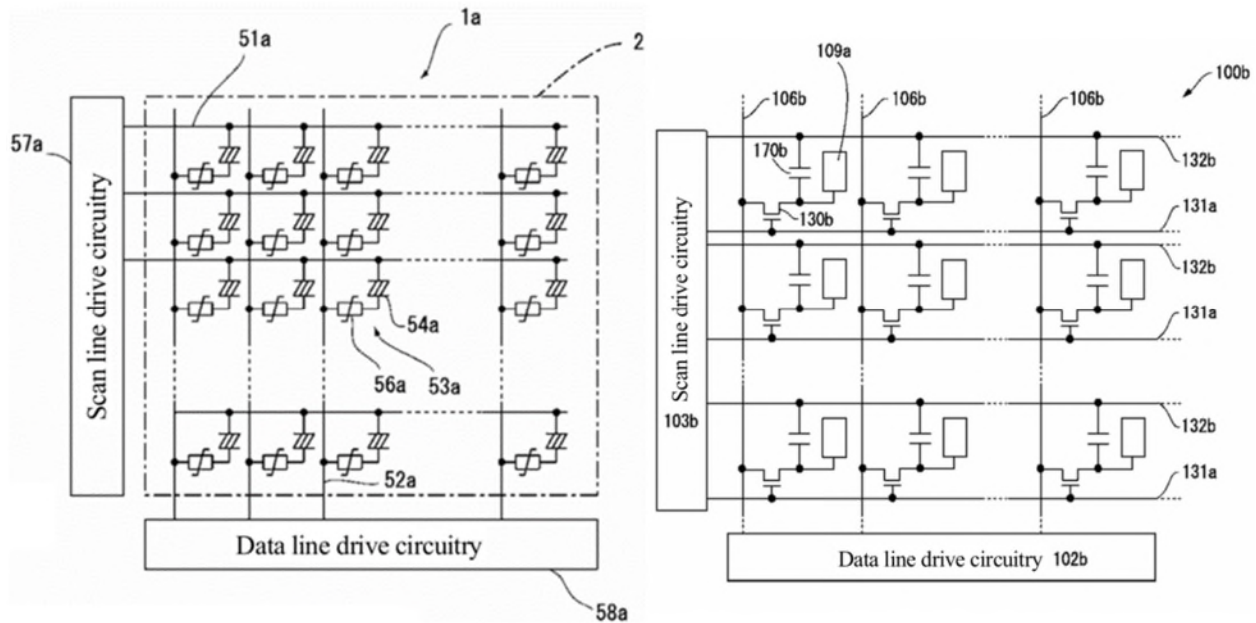
90. In my opinion, Miyagawa discloses or renders obvious “*a transparent substrate formed with ... electrode terminals receiving a driving signal and a control signal from the video signal lines, the scanning signal lines, and an external system.*”

91. Specifically, Miyagawa discloses a display device that includes “a transparent substrate” (TFT array substrate) equipped with ... “electrode terminals” (pads). These pads are configured to receive both driving signals and control signals from “the video signal lines” (data lines 106b), “the scanning signal lines” (scan lines 131b), and from “an external system” (electronic apparatus body).

92. By 2010, it was routine in the field of displays to generate operating signals from a driving circuit, which supplies signals necessary to control display elements, such as the display's pixels. *See, e.g.*, Ex. 1001, 1:38–43, 4:48–49.

Typically, image data or control signals are delivered to the display elements via electrode terminals that are connected to an external system through a flexible substrate (*e.g.*, a ribbon cable), which interfaces with the transparent substrate. *Id.*, 14:62–15:16. External systems (*e.g.*, a memory or a communication device coupled to the display) were typical to enable displays to present a wide variety of videos, interactive user interfaces, and data provided by their host devices. All of these were well known, as the '762 patent itself admits. Ex. 1001, 4:11–14.

93. Miyagawa's invention is readily applicable to the "electro-optical device" depicted in Figure 6, which is a "a block diagram schematically illustrating a configuration of an electro-optical device composed of an active matrix type liquid crystal device using a thin film transistor (TFT) as a pixel switching element." Miyagawa, [0041]-[0042]. Similarly, Figure 1, which underlies Miyagawa's first embodiment, is "a block diagram schematically illustrating a configuration of an [analogous] electro-optical device composed of an active matrix type liquid crystal device using a TFD [thin film diode] element as a pixel switching element." *Id.*, [0014].



Id., Figs. 1 (left), 6 (right).

94. A POSITA would have understood that the crack diagnostic wiring features described in Miyagawa's first embodiment (Fig. 1), which uses a TFD-based substrate, are equally applicable to the embodiment shown in Figure 6, which employs a conventional TFT-based substrate. Miyagawa explicitly states that its invention can be "applied to the electro-optical device ... [depicted in] FIG. 6...."

Id., [0041]. A POSITA would have understood from Miyagawa why that is so. It describes both embodiments as "electro-optical devices," and explains that the TFT array substrate in the Figure 6 embodiment is formed of a light-transmitting material such as glass or quartz, with data lines and scan lines arranged in a matrix and the same type of peripheral crack diagnostic wiring applied. *See* Miyagawa, [0015], [0017], [0043]–[0044]. A POSITA would have recognized that any

substantive difference between these analogous embodiments is related to the pixel switching element (TFD versus TFT). The structure and function of the crack diagnostic wiring of Miyagawa's first embodiment with a TFD based substrate would remain unchanged when applied to the TFT array substrate. *See id.*, [0043]–[0044].

95. Miyagawa describes drive circuits for data lines, which supply image signals to data lines, as well as drive circuits for scan lines, which supply scanning signals to scan lines. *Id.*, [0043]. Miyagawa explains that the “image signal to be written on the data lines 106b is supplied from the data line drive circuit 102b” whereas the “scanning signal is supplied to the scan lines 131b pulsed from the scan line drive circuit 103b at a predetermined timing.” *Id.* Such predetermined timing corresponds to a frequency known as the refresh rate. These signals lead to the pixels holding a certain voltage to display an image. *See id.*

96. As discussed above, a POSITA would have understood that these drive circuits generate their output signals from input signals received from an external system. Consistent with this, Miyagawa's display comprises a flexible substrate 7, which connects to “an electronic apparatus body” and is mounted in the substrate mounting region 70. *Id.*, [0020]. The electronic apparatus body (“such as mobile computers and mobile phones, and electronic apparatus such as direct-view display devices and projection type display devices”) provides image signals that are

transmitted through the flexible substrate, processed by the drive circuits, and then delivered to the data lines to produce display images. *Id.*, [0012], [0043].

97. Additionally, Miyagawa discloses that the drive circuits may be located either on the transparent substrate (*e.g.*, element substrate 10 or TFT array substrate) or on the flexible substrate. *Id.*, [0040]. In both arrangements, pads are placed on each substrate to facilitate signal transfer, and signals from the electronic apparatus body passes through the pads (*i.e.*, electrodes/terminals) to reach the TFT array substrate. Both of these configurations were well known in the art and represented routine design choices.

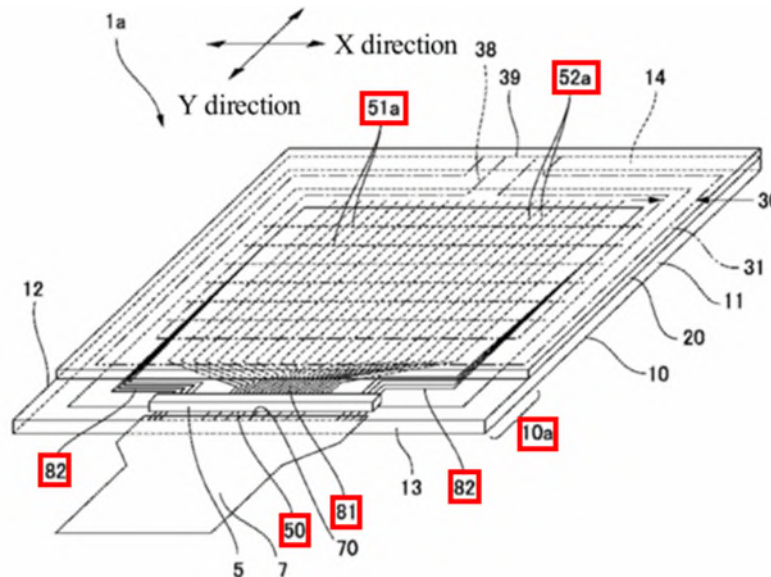
e) 7[a.4]

98. In my opinion, Miyagawa discloses or renders obvious “*a transparent substrate formed with ... a third signal interconnect connecting the video signal lines and the scanning signal lines with the electrode terminals.*”

99. Specifically, Miyagawa describes a display device in which the “transparent substrate” (TFT array substrate) is formed with ... “a third signal interconnect” (wiring patterns 81–82) “connecting the video signal lines” (data lines 106b) “and the scanning signal lines” (scan lines 131b) “with the electrode terminals” (pads).

100. A POSITA would understand that the term “connect” as used in the Challenged Patent encompasses both direct and indirect connections. *See, e.g.*, Ex. 1001, 4:60–61 (direct connection); 6:33–39, 7:22–26 (indirect connection).

101. Miyagawa's disclosure makes clear that wiring patterns 81–82 are formed on the substrate and are connected to the data lines 52a/106b and scan lines 51a/131b, respectively. Miyagawa, [0018], [0043].



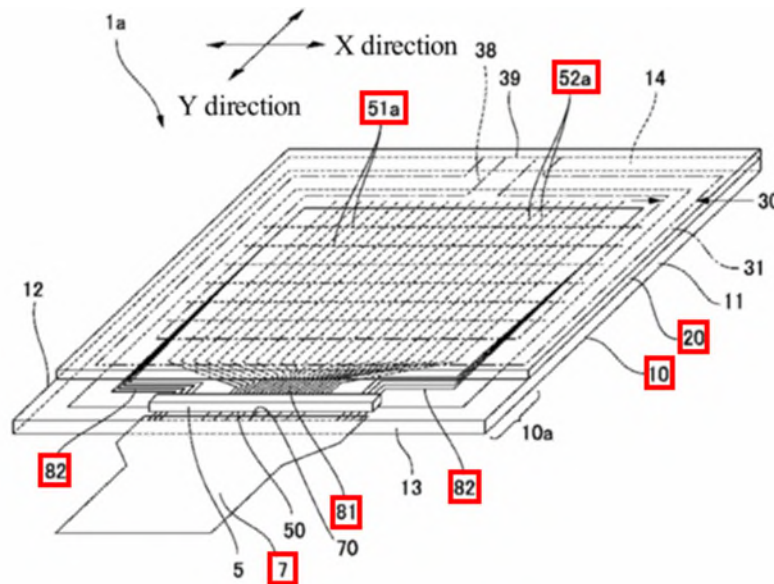
Id., Fig. 2.

102. Figure 2 shows the overhang region 10a with pads for connection to the flexible substrate. Based on these teachings of Miyagawa, a POSITA would have recognized that these wiring patterns 81–82 terminate at the overhang region 10a, where one end of the wiring patterns is connected to the pads. These pads either directly interface with a driving IC on the display substrate or to matching pads on the flexible substrate, which then connect to a driving IC mounted on the flexible substrate. *Id.*, [0018], [0040]. In both configurations, the wiring patterns 81–82 are coupled to pads in the overhang region 10a. These pads serve as the interface for delivering image and control signals, which are transmitted from the external

f) 7[b]

104. Specifically, Miyagawa teaches a display device that includes “a flexible interconnect substrate” (flexible substrate 7) “connected to the first transparent substrate” (TFT array substrate). The flexible interconnect substrate is used to deliver the “driving signal to the video signal lines” (data lines 106b) “and the

scanning signal lines” (scan lines 131b) via “the electrode terminals” (pads) “and the third signal interconnect” (wiring patterns 81–82).



Miyagawa, Fig. 2.

105. Miyagawa discloses that the “flexible substrate 7 ...[is] mounted in ... the substrate mounting region 70.” *Id.*, [0020]; *see also id.*, [0040]. This flexible substrate interfaces with an electronic apparatus body, which provides the signals necessary to generate displayed images. *Supra* §X.A.1.d. As depicted above, the signal path extends from the electronic apparatus body, through the flexible substrate and the matching pads (coupled to the flexible substrate and to the display substrate), and then through the wiring patterns 81–82 to reach the data and scan lines 106b/52a and 131b/51a. *Supra* §X.A.1.e. In this way, Miyagawa establishes a continuous connection path from the electronic apparatus body,

through the flexible substrate and the wiring patterns 81–82, and to the data and scan lines.

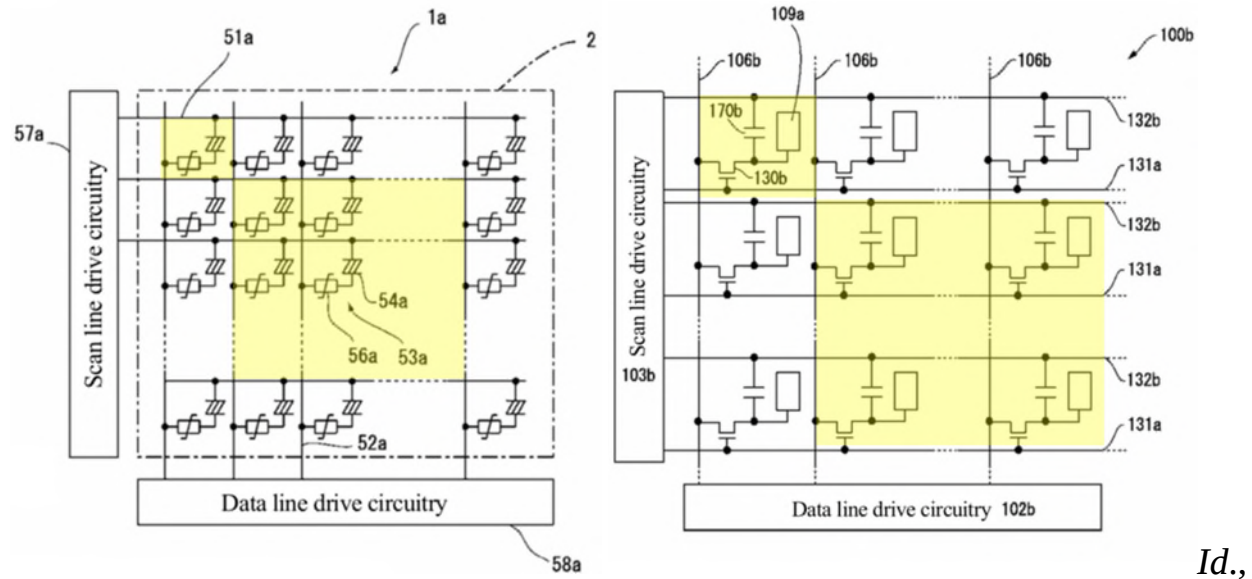
g) 7[c]

106. In my opinion, Miyagawa discloses “*a region surrounded by the video signal lines and the scanning signal lines being a pixel area.*”

107. Specifically, Miyagawa describes a display device in which “a region surrounded by the video signal lines” (data lines 106b) “and the scanning signal lines” (scan lines 131b) defines the “pixel area” (pixel matrix).

108. Furthermore, similar to the TFD substrate described in embodiment 1, Miyagawa’s TFT array substrate includes “a plurality of pixels formed in a matrix.” *Id.*, [0043] The electro-optical device features an image display region 2 that contains this matrix of pixels and each pixel in the matrix is surrounded by video signal lines and scanning signal lines. *Id.*, [0015], *see also id.*, Fig. 6.

109. The pixel area referenced in the claims may correspond to any portion of this region, whether it comprises one, multiple, or all pixels may constitute the claimed pixel area because the limitation simply requires a pixel area to be surrounded by the video and scanning signal lines, that is, a plurality of video and scanning signal lines as recited in claim limitation 7[a.1] and 7[a.2], not necessarily all of the video and scanning signal lines on the substrate. Illustrative examples of such pixel areas are highlighted below in Figures 1 and 6 of Miyagawa:

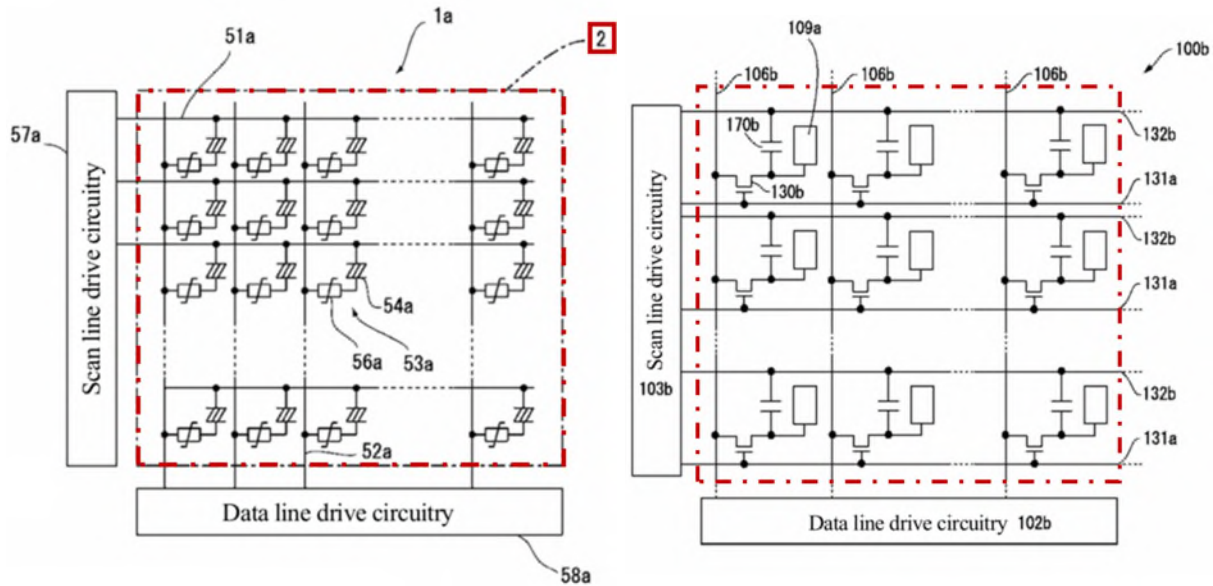


Figs. 1, 6.

h) 7[d]

110. In my opinion, Miyagawa discloses, “*a region where the pixels are formed in a matrix being a display area.*”

111. In particular, Miyagawa’s display device includes “a region” in which “the pixels” (pixels 53a) are arranged in “a matrix,” forming “a display area” (image display region 2). As discussed above, this region constitutes the “display area” as recited in Claim 7.



Miyagawa, Figs. 1, 6; *see also supra* §X.A.1.g.

i) 7[e]

112. In my opinion, Miyagawa discloses or renders obvious “*the third signal interconnect being formed in a region outside the display area.*”

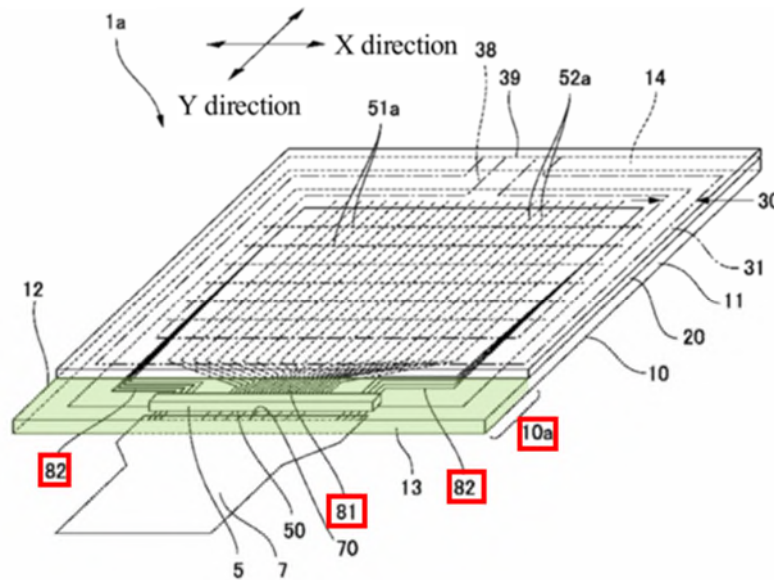
113. Specifically, Miyagawa discloses or renders obvious a display device in which “the third signal interconnect” (wiring patterns 81–82) is “formed in a region outside the display area” (image display region 2).

114. Pixels are formed at the intersections of the data lines and scan lines within the image display region, resulting in a matrix of pixels. Miyagawa, [0015].



116. Furthermore, portions of these wiring patterns 81–82 are located in the overhang region 10a, which Miyagawa identifies as being outside the display area.

Id., [0018] (stating that the wiring patterns 81-82 “extend into the overhang region 10a”), Fig. 2.



Id. Fig. 2.

j) 7[f]

117. In my opinion, Miyagawa discloses or renders obvious, “*a fourth signal interconnect disposed outside the third signal interconnect but near the peripheral edge of the transparent substrate, the fourth signal interconnect surrounding the area where the display area is included and the third signal interconnect is formed, the fourth signal interconnect being opened at opposite ends thereof and being connected to respective electrode terminals for inspection at the open ends.*”

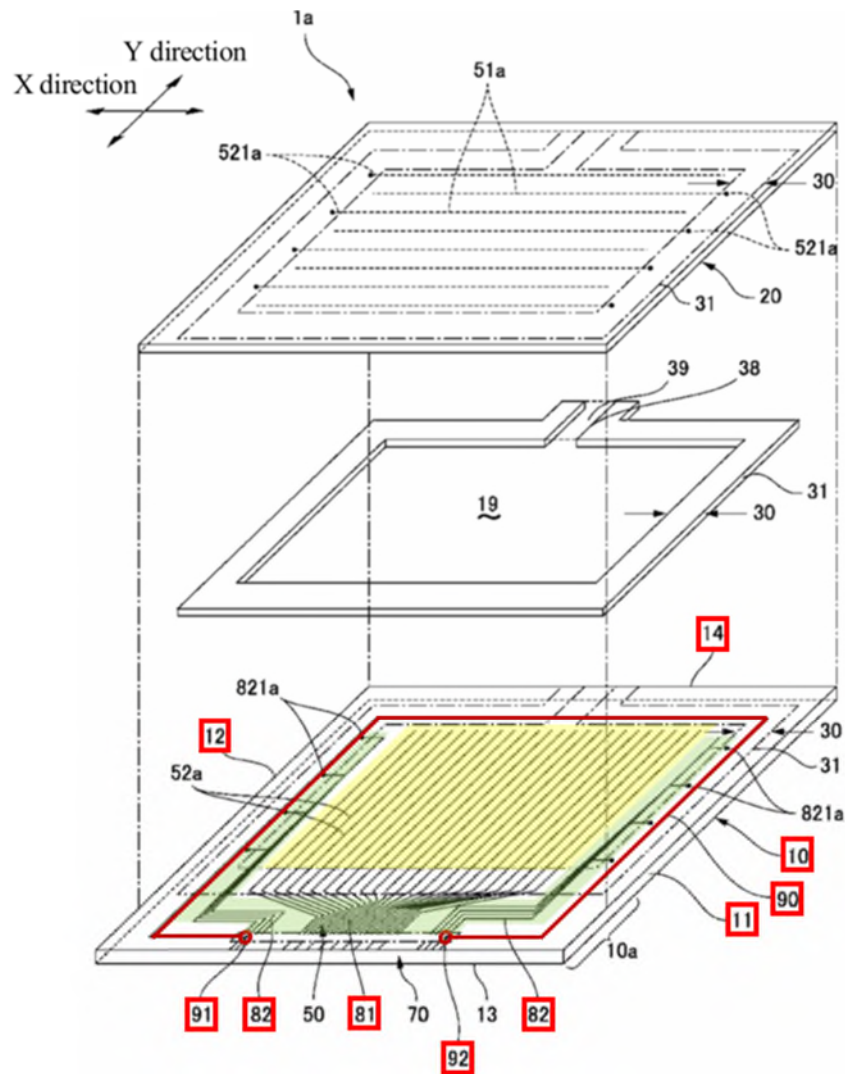
118. In particular, Miyagawa discloses or renders obvious a display device in which “a fourth signal interconnect” (diagnostic wiring 90) is “disposed outside the third signal interconnect,” (wiring patterns 81–82) “but near the peripheral edge” (sides 11, 12 and 14) “of the transparent substrate” (TFT array substrate). This diagnostic wiring surrounds the region containing both “the display area” (image

display region 2) and “the third signal interconnect” (wiring patterns 81–82).

“[T]he fourth signal interconnect” (diagnostic wiring 90) is open at its opposite ends, where it “connects to respective electrode terminals” (first and second diagnostic pads 91–92) for inspection purposes.

119. Miyagawa discloses that the diagnostic wiring is intended to detect “whether a substrate crack has occurred.” Miyagawa, Abstract; *id.*, [0027], [0030], [0044].

The diagnostic wiring 90 is situated near the edges of the element substrate 10 (or the TFT array substrate in the Figure 6 embodiment), as shown in Miyagawa’s Figure 3 below, specifically to enable crack detection after individual substrates are cut from a mother substrate:



Id., Fig. 3.

120. In Figure 3 above, the diagnostic wiring (in dark red) is located outside the wiring patterns 81–82 (light green), near the substrate’s edges, and encircles the area where both the image display region (light yellow) and the wiring patterns 81–82 are formed. *Id.*, Abstract, [0024]–[0025], [0031], [0044].

121. The diagnostic wiring extends along three sides of the substrate but remains open at the bottom, in the overhang region 10a. *Id.*, [0024]. The ends of the

diagnostic wiring are connected to the diagnostic pads 91–92 (shown as dark red circles annotated in Figure 3 above). *Id.*, Abstract, [0006]–[0007], [0023]–[0024].

122. These diagnostic pads 91 and 92 are intended for inspection by checking electrical continuity between them. *Id.*, [0007]. If a crack occurs on the substrate and breaks the diagnostic wiring, the two pads will become electrically disconnected. *Id.*

123. Inspection can be performed by probing the diagnostic pads to check for continuity, either after the substrate is cut from the mother substrate or after two substrates are bonded, and before components are mounted—thereby reducing waste. *Id.*, [0028], [0004], [0030]. Alternatively, the inspection can be conducted by connecting two pins (“bumps” in Miyagawa) of the driving IC to the diagnostic pads and using a substrate crack diagnostic unit implemented on the IC to check continuity. *Id.*, [0011], [0026], [0029]. The IC may be located on the flexible substrate, in which case the diagnostic pads are connected to the IC via the flexible substrate. *Id.*, [0040].

124. These features apply equally to the TFD and TFT-array embodiments. *Id.*, [0041]. In particular, Miyagawa positions the substrate crack diagnostic wiring at the outer periphery of the substrate in the TFD embodiment. Given the structural and functional similarities between TFD and TFT array substrates, the same approach would be expected to apply to the TFT embodiment, enabling effective

detection of cracks regardless of whether the array substrate uses TFDs or TFTs.

This undergirds Miyagawa's teaching that the crack detection approach is equally applicable to both types of array substrates.

k) 7[g]

125. In my opinion, Miyagawa at least renders obvious “*wherein the fourth signal interconnect is formed of a conductive thin film disposed along the peripheral edge portion of three sides of the transparent substrate.*”

126. In particular, Miyagawa at least renders obvious a display device in which “the fourth signal interconnect” (diagnostic wiring 90) is implemented as a conductive thin film positioned “along the peripheral edge of three sides of the transparent substrate” (TFT array substrate).

127. As shown above in Figure 3 of Miyagawa, the diagnostic wiring is arranged along the edges of three sides of the substrate. *Supra* §X.A.1.j; Miyagawa, [0024]. Miyagawa describes this wiring as “a conductive film” that is fabricated at the same time as other thin-film components, such as the “data lines 51a [sic, 52a/106b]⁴, a TFD element, a pixel electrode, or the like.” Miyagawa, [0024]. In the TFT-based embodiment, thin-film transistors are used in place of thin-film diodes as the pixel switches. *Id.*, [0014], [0042]. Because the diagnostic wiring is

⁴ All other occurrences of data lines in this embodiment are designated 52a.

produced concurrently with these thin-film elements, it is also formed as a thin film, or this would at least have been obvious. Fabricating the diagnostic wire as a thin film, similar to other components, is a design choice to leverage existing manufacturing steps, ensure compatibility with the substrate, and avoid additional complexity or cost. It would have been routine and expected for a skilled artisan to implement the diagnostic wiring as a thin film, or at a minimum, it would have been obvious to do so.

2. Dependent Claim 8

128. Claim 8 of the '762 patent depends from Claim 7 and recites, “[a] *display device according to claim 7, wherein the fourth signal interconnect has a colored thin film layer or a thin film layer having a transmittance at a predetermined level or less.*”

129. Claim 7 is rendered obvious by Miyagawa for at least the reasons I describe above.

130. In my opinion, Miyagawa also renders obvious that “the fourth signal interconnect” (diagnostic wiring 90) is implemented as “a colored thin film layer or a thin film layer having a transmittance at a predetermined level or less.”

131. Miyagawa discloses that the diagnostic wiring is fabricated as a conductive thin film. *Supra* §X.A.1.k. Miyagawa explains that this diagnostic wiring “is a conductive film formed simultaneously with data lines 51a [*sic*, 52a, or 106b in the

TFT embodiment],” meaning that both the diagnostic wiring and the data lines are created in the same manufacturing step. Miyagawa, [0024]. In standard thin-film manufacturing, it is routine for features formed in the same step, such as these diagnostic wirings and data lines, to be made from the same material. Miyagawa further specifies that data lines are “composed of a plurality of chrome lines or the like....” *Id.*, [0017]. Thus, a POSITA would have recognized that chrome would be an appropriate and obvious choice for the diagnostic wiring as well particularly because using the same material for both features streamlines processing, reduces manufacturing complexity, and ensures material compatibility.

132. At the thickness typically used for signal lines in display panels, chrome is well known in the art to be opaque and can exhibit a transmittance below the unspecified predetermined level of the claim. It would have been routine for a skilled artisan to use chrome for the diagnostic wiring, resulting in a low-transmittance thin film. This approach is consistent with established practices in the field and would ensure both functional and inspection advantages from uniformity and consistency.

3. Dependent Claim 9

133. Claim 9 of the '762 patent depends from Claim 7 and recites “[a] *display device according to claim 7, wherein the fourth signal interconnect has a thin metal film layer.*”

134. Claim 7 is rendered obvious by Miyagawa for at least the reasons I describe above.

135. In my opinion, Miyagawa also renders obvious “[a] display device according to claim 7,” including the feature that “the fourth signal interconnect” (diagnostic wiring 90) “has a thin metal film layer.”

136. As previously discussed, Miyagawa renders obvious that the diagnostic wiring is formed of a conductive thin film. Claim 9 simply specifies that this thin film is made of metal.

137. Additionally, Miyagawa expressly discloses that the data lines are made of chrome, a metal, and that the diagnostic wiring is fabricated at the same time and by the same process as the data lines. Miyagawa, [0017], [0024]. Thus, it would have been obvious to form the diagnostic wiring using chrome, a metal. *Supra* §X.A.2. This approach leverages existing materials and fabrication steps, making the use of a thin metal film for the diagnostic wiring a routine and expected design choice.

4. Dependent Claim 10

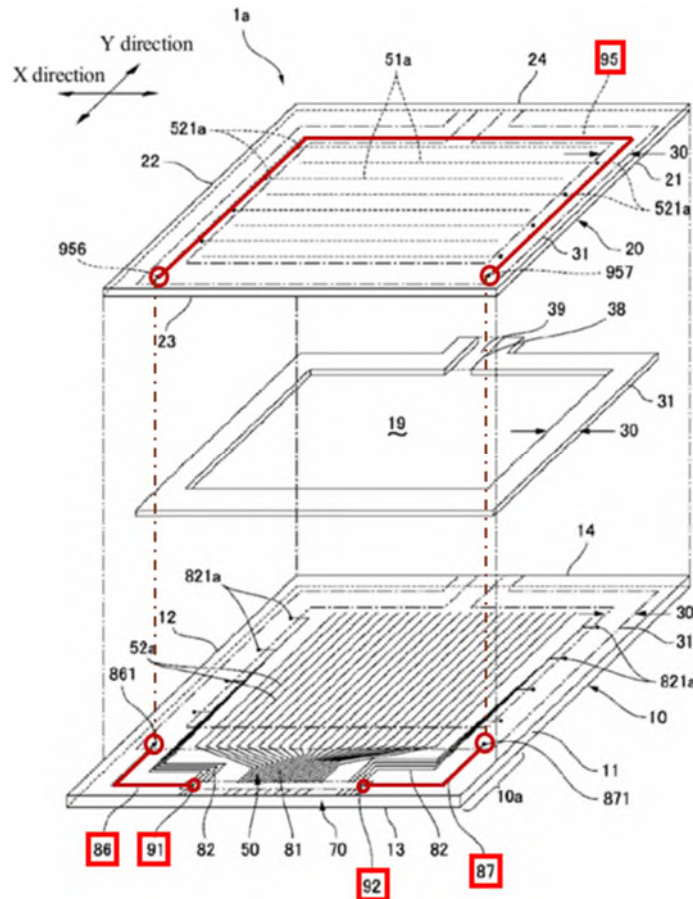
138. Claim 10 of the '762 patent depends from Claim 7 and recites “[a] *display device according to claim 7, wherein the fourth signal interconnect is formed of two or more conductive thin films.*”

139. Claim 7 is rendered obvious by Miyagawa for the reasons I describe above.

140. In my opinion, Miyagawa also renders obvious “[a] display device according to claim 7, wherein the fourth signal interconnect” (diagnostic wiring 95, first wirings 86, and second wiring 87) is “formed of two or more conductive thin films.”

141. As previously discussed, Miyagawa renders obvious that the diagnostic wiring is formed as a conductive thin film. Claim 10 simply specifies that this diagnostic wiring is formed of at least two conductive thin films or two layers. Ex. 1001, 8:12–15 (describing a detection interconnect formed of two or more thin films or layers). Thus, a POSITA would have understood that this limitation does not require these films to be stacked or contiguous; rather, it is sufficient that the diagnostic wiring includes two or more thin films or layers.

142. Miyagawa’s second embodiment describes a configuration in which a diagnostic wiring 95 is formed on the opposing substrate 20 and is electrically connected through two segments of wirings 86 and 87 on the element substrate 10 to the diagnostic pads. Miyagawa, [0037]–[0039]; Fig. 5.



Id., Fig. 5 (broken lines visualizing coupling in this exploded view).

143. This embodiment “is otherwise the same as that in [the] embodiment” supporting claim 7, and thus satisfies the requirements of claim 7 as well. *Id.*, [0039]; [0034]–[0036]. Miyagawa further explains that this arrangement is particularly useful for detecting cracks in the opposing substrate. *See Id.*

144. Additionally, Miyagawa discloses an alternative configuration in which the multi-layer configuration is reversed, such that “a substrate crack diagnostic wiring is formed on the element substrate 10 and a diagnostic pad is formed on the

opposing substrate 20....” *Id.*, [0040]. This alternative is suitable for the TFT embodiment and enables detection of cracks in the TFT array substrate.

145. In either configuration, the diagnostic wiring 95 and second wirings 86 and 87 are each comprised of at least one conductive thin film or layer, with one of the wirings located on the TFT array substrate and the other on the opposing substrate. *See id.*, [0043]–[0044]. A POSITA would have recognized this as an obvious and uninventive design choice as it was already routine practice to manufacture signal lines with multiple films — such ITO, chrome, titanium, and aluminum — to achieve desired electrical and mechanical properties. Thus, employing two or more conductive thin films or layers for the diagnostic wiring would not have required any inventive step.

5. Dependent Claim 12

146. Claim 12 of the ’762 patent depends from Claim 7 and recites “[a] *display device according to claim 7, wherein the flexible interconnect substrate has electrode terminals connected to the fourth signal interconnect at a position different from that of the region forming the electrode terminal connected with the external system.*”

147. Claim 7 is rendered obvious by Miyagawa for at least the reasons I describe above.

148. In my opinion, Miyagawa also renders obvious a display device according to claim 7, including the feature that “the flexible interconnect substrate” (flexible substrate 7) “has electrode terminals connected to the fourth signal interconnect” (diagnostic wiring 90) at a location distinct from the region where the electrode terminals for connection to “the the external system” (electronic apparatus body) are formed.

149. Specifically, in the configuration disclosed by Miyagawa in which the driving IC is mounted on the flexible substrate, the flexible substrate includes electrode terminals that are connected to the first and second diagnostic pads within the area where the flexible substrate overlaps the substrate mounting region. *Id.*, [0040].

150. Additionally, by 2010, it was standard practice in the field to connect the flexible substrate to an external system via electrode terminals at the opposite end of the substrate. A POSITA would have considered such a configuration to be routine and expected in light of the teachings of Miyagawa, including the illustration of the flexible substrate in Figure 2.

B. GROUND 2: Tanabe in View of Miyagawa Renders Obvious Claims 7–10 and 12

151. In my opinion, Tanabe in view of Miyagawa renders Claims 7-10 and 12 of the '762 patent obvious.

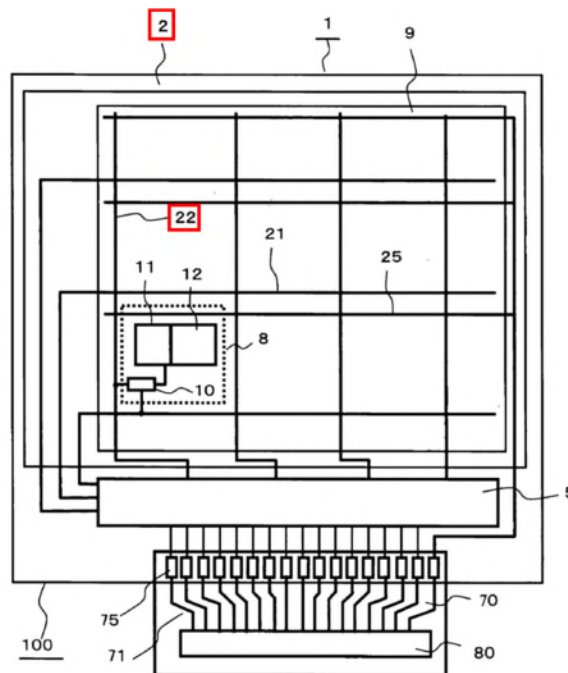
1. Independent Claim 7**a) 7[pre]**

152. Tanabe discloses *a display device*, referred to as a “a liquid crystal display device.” Tanabe, [0054].

b) 7[a.1]

153. In my opinion, Tanabe discloses “*a transparent substrate formed with a plurality of video signal lines.*”

154. Specifically, Tanabe discloses a display device that includes “a transparent substrate” (TFT substrate 2) on which “a plurality of video signal lines” (drain signal lines 22) are formed. Tanabe, [0058].



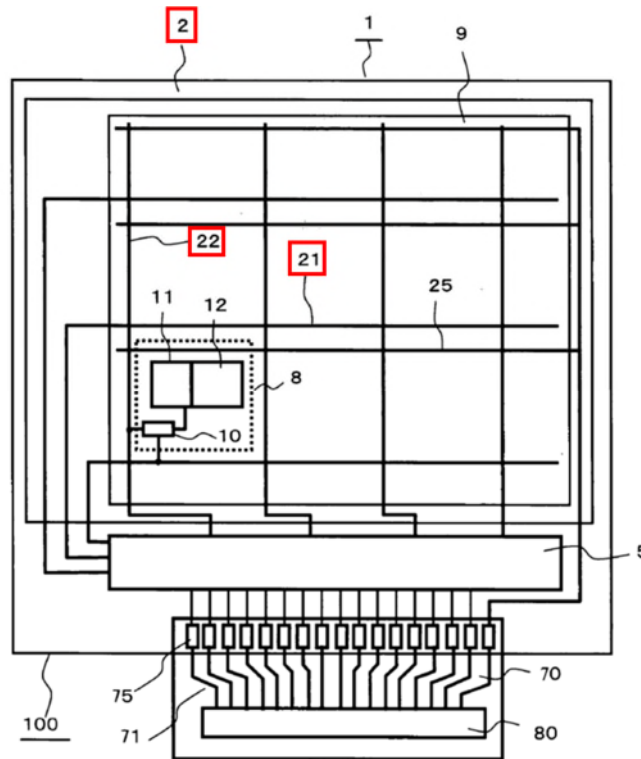
Id., Fig. 1.

155. The TFT substrate “is formed from transparent glass or resin.” *Id.*, [0073]. As discussed above, the ’762 patent admits that transparent substrate made of glass was well known. Ex. 1001, 5:36–40. The drain signal lines are fabricated directly on this transparent TFT substrate. Tanabe, [0058]. Furthermore, Tanabe clarifies that these drain signal lines are also known as “video signal lines.” *Id.*, [0056].

c) 7[a.2]

156. In my opinion, Tanabe discloses “*a transparent substrate formed with ... a plurality of scanning signal lines intersecting the video signal lines.*”

157. Specifically, Tanabe discloses a display device that includes “a transparent substrate” (TFT substrate 2) on which “a plurality of scanning signal lines” (gate signal lines 21) are formed to intersect with the “the video signal lines” (drain signal lines 22).



Tanabe, Fig. 1.

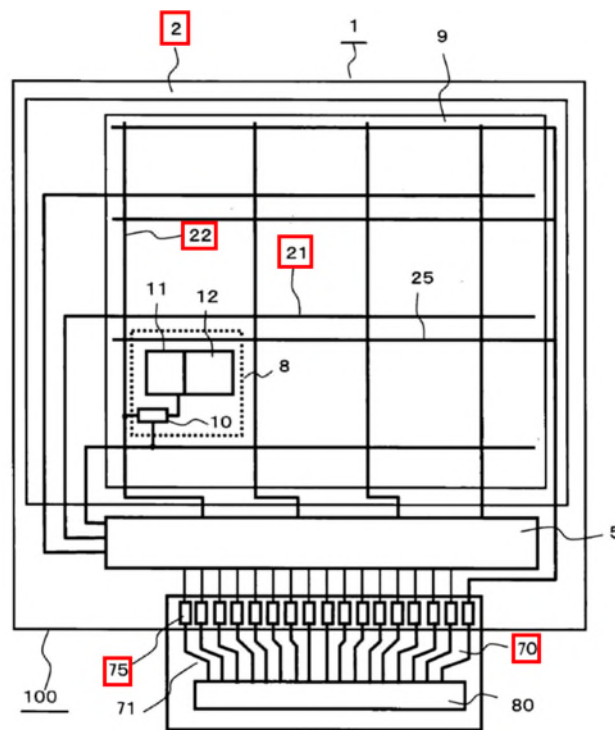
158. Tanabe discloses that these gate signal lines are formed on the TFT substrate. *Id.*, [0058]. Tanabe also refers to the gate signal lines as “scan lines.” *Id.*, [0056].

159. According to Tanabe, the gate signal lines and the drain signal lines intersect in the vicinity of switching elements 10, which are located in the pixel portions 8. *Id.*, [0056], [0069]. Each pixel portion is a pixel of an image. *Id.*, [0055].

d) 7[a.3]

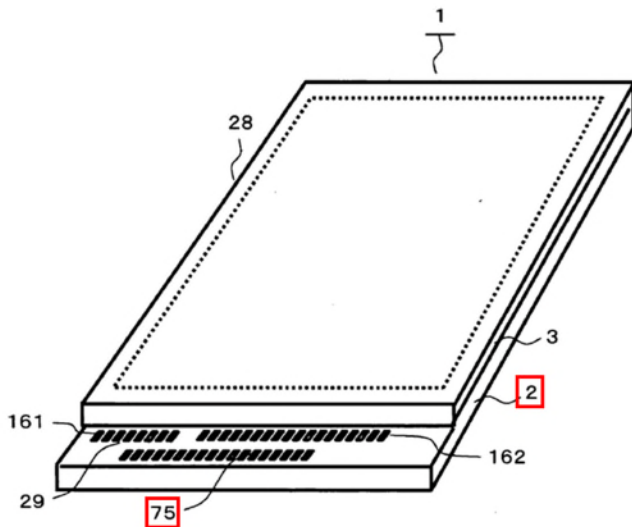
160. In my opinion, Tanabe discloses “*a transparent substrate formed with ... electrode terminals receiving a driving signal and a control signal from the video signal lines, the scanning signal lines, and an external system.*”

161. Specifically, Tanabe describes a display device that includes “a transparent substrate” (TFT substrate 2) equipped with “electrode terminals” (terminals 75) that receive both driving and control signals from “the video signal lines” (drain signal lines 22), “the scanning signal lines” (gate signal lines 21), as well as from “an external system” (portable device). *See supra* §X.A.1.d (explaining the limitation).



Tanabe, Fig. 1.

162. Tanabe illustrates in Figure 1 above that the “flexible substrate 70 is connected to the connection terminals 75.” *Id.*, [0059]. The “FPC [Flexible Printed Circuit] connection terminals 75” are located “on the terminal connection portion 29” of the TFT substrate 2. *Id.*



Id., Fig. 2.

163. Tanabe further explains that the signals required to drive the display “are transmitted to the liquid crystal panel 1” through the “terminals 75.” *Id.*, [0054].

These signals include “[c]ontrol signals ... supplied” via “the gate signal lines” and “video signals” delivered through “the drain signal lines 22.” *Id.*, [0057]–[0058].

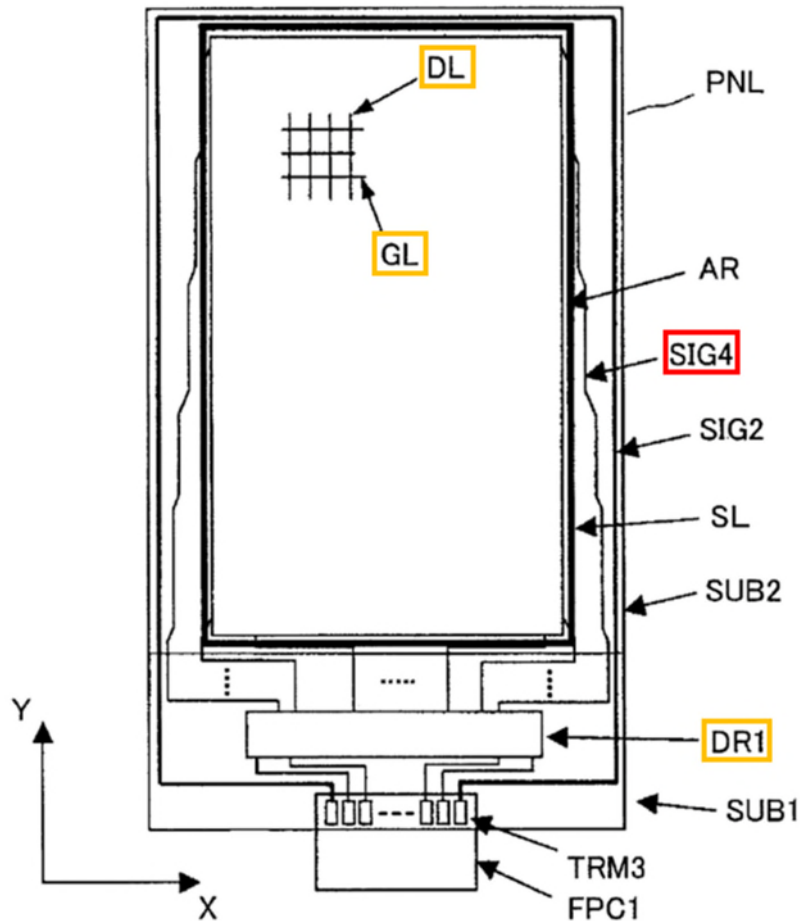
164. A POSITA would have understood that the flexible substrate is connected to an external system (*i.e.*, a portable device), which provides the image data to be displayed. *Id.*, [0004], [0061]. For example, a mobile phone or a laptop computer, which includes a processor running applications that render images for display on a screen, was well known as an external system.

e) 7[a.4]

165. In my opinion, Tanabe discloses “*a transparent substrate formed with ... a third signal interconnect connecting the video signal lines and the scanning signal lines with the electrode terminals.*”

166. Specifically, Tanabe discloses a display device in which the “transparent substrate” (TFT substrate 2) is provided with “a third signal interconnect” — specifically, the unnamed bus wires that extend from “the video signal lines” (drain signal lines 22) and “the scanning signal lines” (gate signal lines 21), and connect these lines to “the electrode terminals” (terminals 75). Although these bus wires are not explicitly named as such in Tanabe, that their function is clearly described and is identical to the function of “a third signal interconnect” recited in the Challenged Claim. *See* Tanabe, Fig. 2, [0058].

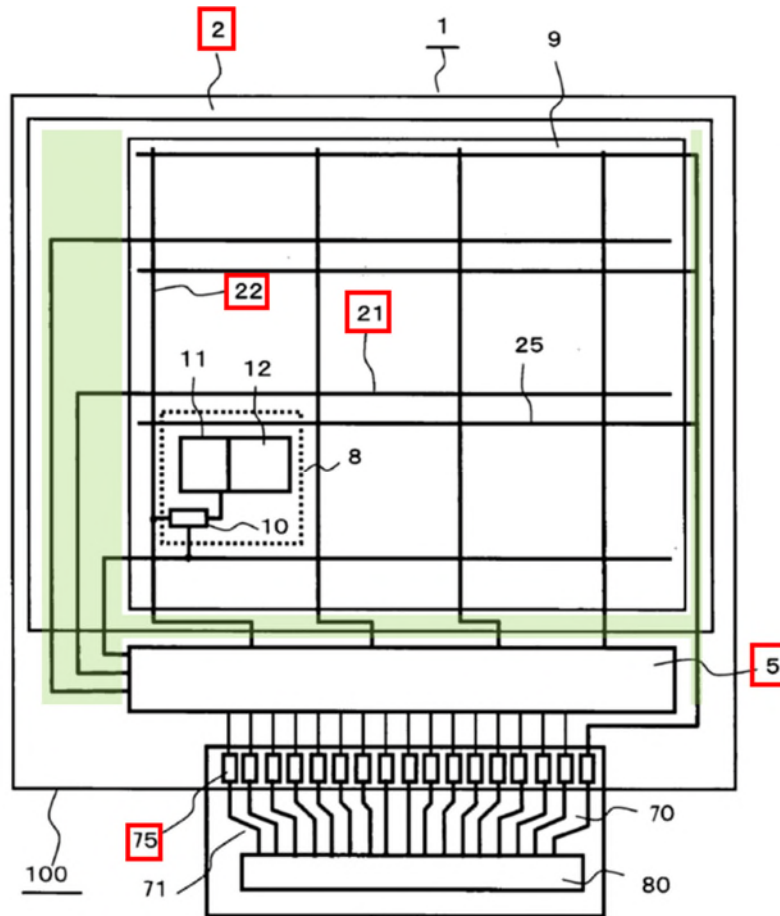
167. As discussed previously, the term “[c]onnect[ion]” of the ’762 patent encompasses both direct and indirect electrical connections. *Supra* §X.A.1.e. The third signal interconnect (SIG4) in the ’762 patent is described as bus wires that connect the video and scanning signal lines (DL and GL) to the driving circuit (DR1). Ex. 1001, 15:7–16.



Id., Fig. 9.

168. Tanabe's disclosure, including Figure 1 below, illustrates this arrangement.

Tanabe's TFT substrate 2 features signal interconnects (shown in green shaded areas) that serve as bus wires connecting drain signal lines 22 and gate signal lines 21 to the drive circuit 5:



Tanabe, Fig. 1, [0058].

169. Tracing the signal flow, the image signals are received from an external system (such as a processor in a laptop) and are delivered to the display components via the flexible substrate 70, passing through terminals 75 on the TFT substrate. *Id.*, [0054]. These terminals 75 are connected to the drive circuit 5, which outputs both control signals and the video signals. *Id.*, [0058]–[0059]. The signals from the drive circuit are then routed to the drain and gate signal lines through the third signal interconnect, the unidentified bus wires. *Id.*, Fig. 2.

f) 7[b]

170. In my opinion, Tanabe discloses “*a flexible interconnect substrate connected to the first transparent substrate, the flexible interconnect substrate used for supplying the driving signal to the video signal lines and the scanning signal lines by way of the electrode terminals and the third signal interconnect.*”

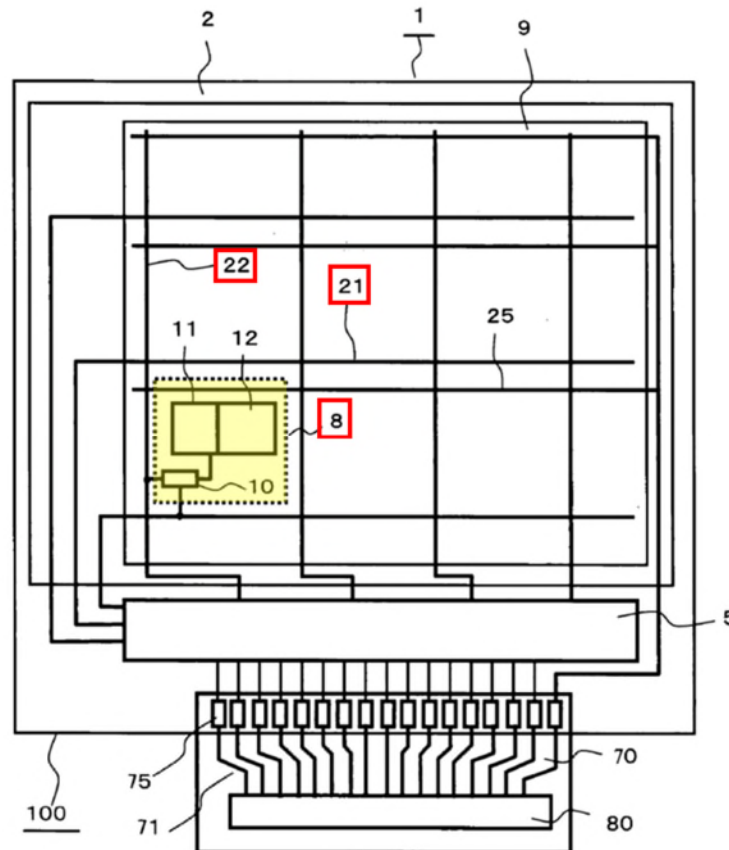
171. Specifically, Tanabe discloses a display device that includes “a flexible interconnect substrate” (flexible substrate 70) connected to “the first transparent substrate” (TFT substrate 2). “[T]he flexible interconnect substrate [is] used for supplying the driving signal to the video signal lines” (drain signal lines 22) and “the scanning signal lines” (gate signal lines 21). The signals are supplied by way of “the electrode terminal” (terminals 75) and are routed through “the third signal interconnect,” which consists of (unnamed) bus wires extending from the gate and drain signal lines.

172. This configuration, as shown above in Figure 2 of Tanabe, enables transmission of control and image signals from an external system, through the flexible substrate and electrode terminals, and ultimately to the appropriate signal lines on the display panel. *Supra* §X.B.1.e.

g) 7[c]

173. In my opinion, Tanabe discloses “*a region surrounded by the video signal lines and the scanning signal lines being a pixel area.*”

174. Specifically, Tanabe describes a display device in which “a region surrounded by the video signal lines” “and the scanning signal lines” defines “a pixel area.”



Tanabe, Fig. 1.

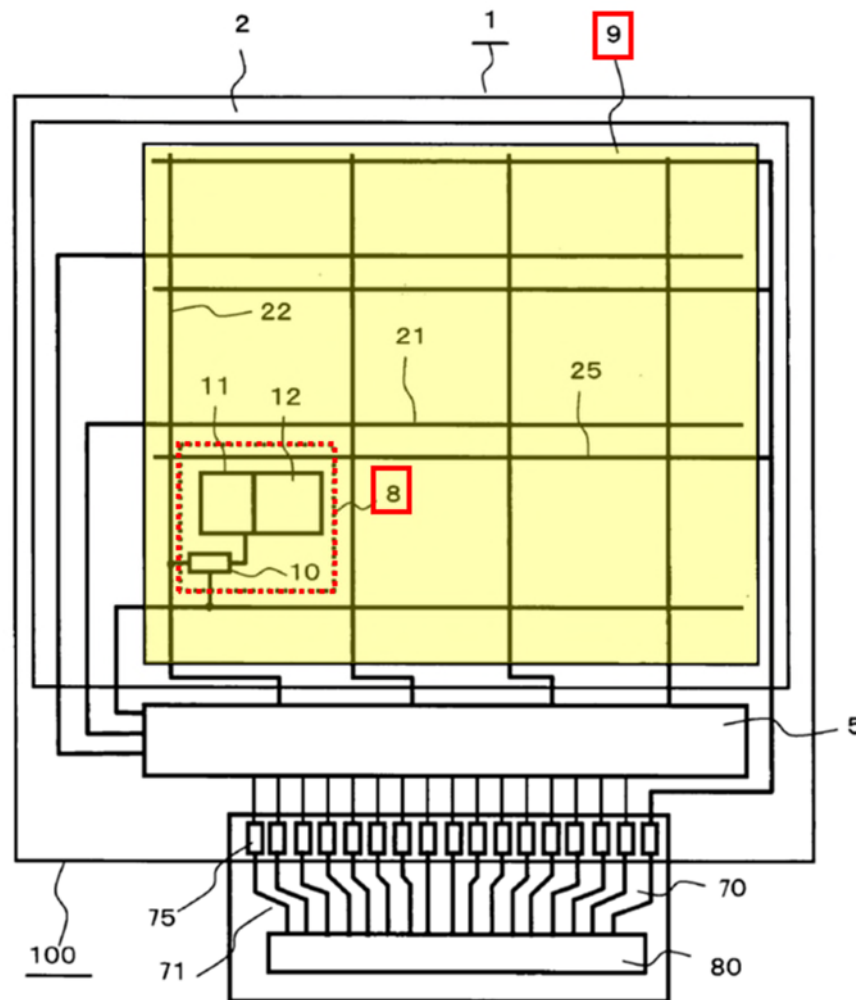
175. Figure 1 of Tanabe illustrates that “[t]he pixel portions 8 are formed in regions surrounded by the gate signal lines 21 and the drain signal lines 22.” *Id.*, [0056].

h) 7[d]

176. In my opinion, Tanabe discloses “*a region where the pixels are formed in a matrix being a display area.*”

177. In particular, Tanabe’s display device includes “a region where the pixels” (pixel portions 8) “are formed in a matrix being a display area” (display region 9).

Id., [0055] (teaching that “[t]he pixel portions 8 arranged in a matrix form a display region 9...”).



Tanabe, Fig. 1.

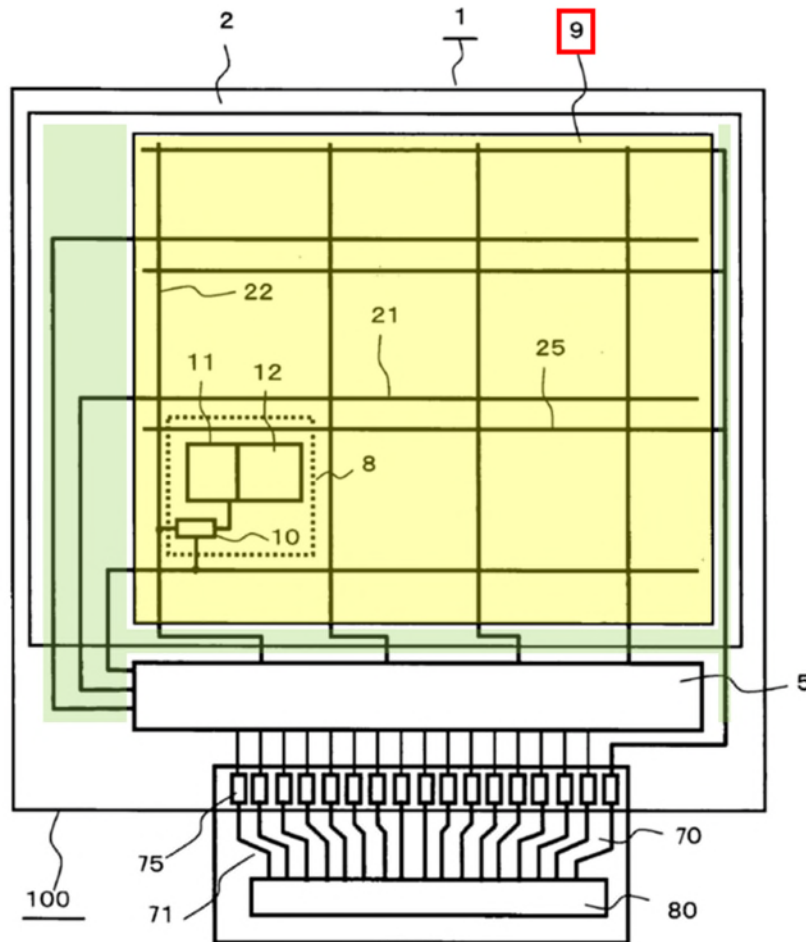
178. A POSITA, familiar with LCD technology, would have understood that a “pixel area” refers to the region occupied by an individual pixel or a group of pixels, while a “matrix-based display area” refers to the larger region where these pixels are organized in a two-dimensional grid to create the active display.

Tanabe’s disclosures align with these established concepts, and a POSITA would have readily recognized the configuration described above satisfies the requirements for both a pixel area and a matrix-based display area as recited in Claim 7.

i) 7[e]

179. In my opinion, Tanabe discloses “*the third signal interconnect being formed in a region outside the display area.*”

180. Tanabe discloses a display device in which “the third signal interconnect,” which are the (unnamed) bus wires extending from gate and drain signal lines, is “formed in a region outside the display area” (display region 9):



Tanabe, Fig. 1.

181. Tanabe's Figure 1 illustrates that these bus wires are positioned outside the matrix of pixels that make up the display area (*i.e.*, display region 9 in yellow), thereby routing signals to and from the pixel circuitry without occupying space within the active display region itself. This arrangement is consistent with standard display panel design, where signal interconnects are located outside the area dedicated to image display.

j) 7[f]

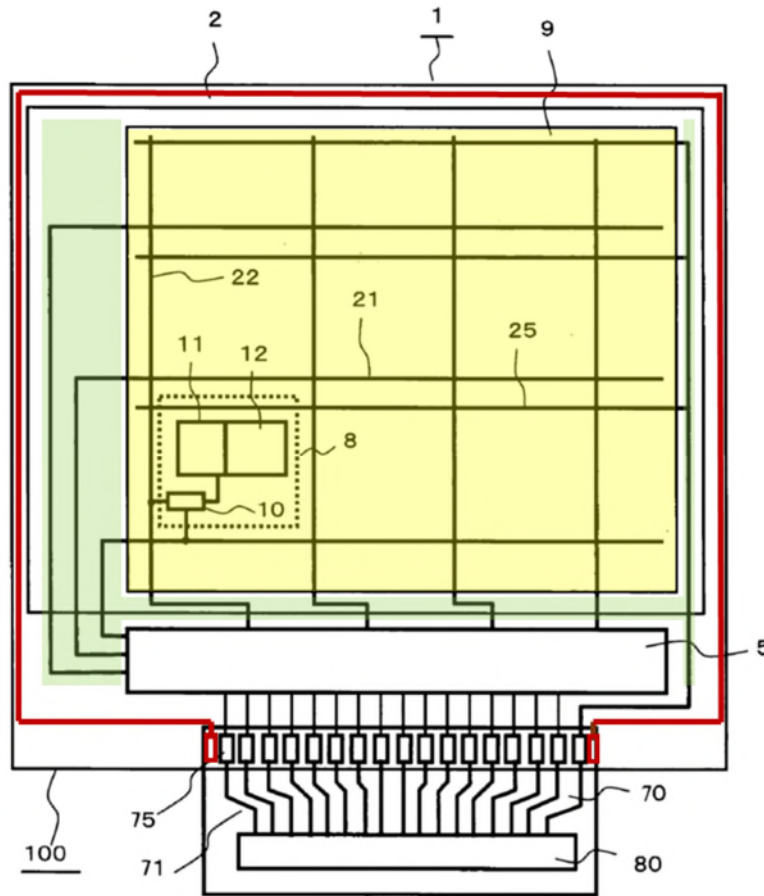
182. In my opinion, Tanabe in view of Miyagawa renders obvious in view of Miyagawa renders obvious “*a fourth signal interconnect disposed outside the third signal interconnect but near the peripheral edge of the transparent substrate, the fourth signal interconnect surrounding the area where the display area is included and the third signal interconnect is formed, the fourth signal interconnect being opened at opposite ends thereof and being connected to respective electrode terminals for inspection at the open ends.*”

183. Specifically, Tanabe’s and Miyagawa’s combined teachings render obvious a display device in which “a fourth signal interconnect” (Miyagawa: diagnostic wiring 90) is positioned “outside the third signal interconnect,” (Tanabe: (unnamed) bus wires extending from gate and drain signal lines, analogous to Miyagawa: wiring patterns 81–82) “but near the peripheral edge” (Miyagawa: sides 11, 12 and 14) “of the transparent substrate” (Tanabe: TFT substrate 2; Miyagawa: TFT array substrate). In this configuration, “the fourth signal interconnect surrounds” both “the display area” (Tanabe: display region 9, analogous to Miyagawa: image display region 2) and “the third signal interconnect” (Tanabe: bus wires extending from gate and drain signal lines, analogous to Miyagawa: wiring patterns 81–82), and is open at both ends, where it

is “connected to respective electrode terminals” (Miyagawa first and second diagnostic pads 91–92) “for inspection at the open ends.”

184. It is important to note that, aside from allegedly the crack-detection interconnect, the structure and operation of LCD panels, including the TFT LCD panels such as those disclosed by both Miyagawa and Tanabe, were well known in the art, as the ’762 patent admits. Ex. 1001, 1:18–30, 4:11–14. A POSITA would have recognized that the combination of Miyagawa and Tanabe does not involve any inventive step beyond what was already established and practiced.

185. Miyagawa explicitly discloses diagnostic wiring that meets the requirements of claim limitation 7[f]. *Supra* §X.A.1.j. A POSITA would have readily appreciated that incorporating a crack-detection wire, as taught by Miyagawa, into Tanabe’s manufacturing process would provide significant benefits by enabling early detection of substrate defects and thereby improving manufacturing efficiency. Miyagawa, [0028]. It would have been straightforward for a POSITA to add such a crack-detection wire around the periphery of the substrate to detect cracks, as demonstrated by Miyagawa. When applied to Tanabe’s device, this crack-detection wire would surround both the third signal interconnect and the display area, ending at electrode terminals that are open and accessible for inspection. The combination is illustrated in the annotated Figure 1 of Tanabe (below), with an added crack-detection wire:



Tanabe, Fig. 1 (annotated to add diagnostic wiring and terminals).

186. It would have been obvious to add the diagnostic wiring as disclosed in Miyagawa to the TFT substrate as disclosed in Tanabe. The purpose of the diagnostic wiring is to detect broken signal lines, and Tanabe's signal lines are arranged on the TFT substrate, in a manner similar to those on Miyagawa's TFT array substrate. Miyagawa, [0007], [0031], [0043]–[0044]; *supra* §X.B.1.b–e. By incorporating Miyagawa's crack-detection wiring into Tanabe's configuration, the resulting arrangement of the diagnostic wiring on Tanabe's TFT substrate would be analogous to that found on Miyagawa's TFT array substrate. This arrangement

would also be beneficial for the same design considerations that are described in Miyagawa, such as ensuring early detection of cracks or breaks in substrate periphery and damage to functional wirings. Miyagawa, [0007], [0031], [0043]–[0044]. This approach can be readily adapted to account for the routing of common signal lines, such as signal lines 25 in Tanabe, which are essential to device operation and should be protected against cracking. For these reasons, this combination would have been straightforward and obvious to a POSITA, as it involves the application of well-understood principles to achieve predictable results.

187. While Tanabe provides an inspection scheme for evaluating gate and drain electrodes within the pixel region, a POSITA would have recognized that this approach is limited to detecting defects such as disconnections in signal lines or terminals at the pixel level. Tanabe does not address the detection of cracks or breaks at the substrate periphery, which can occur during the cutting of the mother substrate into individual display panels. As discussed above, a POSITA would have been aware that such peripheral cracks are a well-known source of yield loss in LCD manufacturing and that early detection of these defects is beneficial to quality control and production efficiency. Miyagawa directly addresses this problem by teaching the use of a peripheral crack-detection wire, which enables early and reliable detection of cracks at the substrate edges. Thus, even though

Tanabe includes an inspection scheme, a POSITA would have been motivated to look to Miyagawa and incorporate its peripheral crack-detection wiring to achieve more comprehensive defect detection.

k) 7[g]

188. In my opinion, Tanabe in view of Miyagawa at least at least renders obvious, *“wherein the fourth signal interconnect is formed of a conductive thin film disposed along the peripheral edge portion of three sides of the transparent substrate.”*

189. Specifically, Tanabe in view of Miyagawa at least at least renders obvious a display device in which “the fourth signal interconnect” (Miyagawa: diagnostic wiring 90) is formed as a conductive thin film positioned along the peripheral edge of “three sides of the transparent substrate” (Tanabe: TFT substrate 2; Miyagawa: TFT array substrate).

190. As illustrated above in the annotated Figure 1 of Tanabe, the diagnostic wiring is arranged along the edges of three sides of the substrate, consistent with the configuration described in Miyagawa. *Supra* §X.B.1.j; Miyagawa, [0024]. Miyagawa specifically describes this wiring as “a conductive film formed simultaneously with data lines 51a [*sic*, 52a/106a], a TFD [or TFT] element, a pixel electrode, or the like.” Miyagawa, [0024]. A POSITA would have recognized the advantages of using the same thin-film fabrication process for the crack-

detection wire as for other wiring on the panel. Forming all of the wiring in a single process step is more efficient and reduces manufacturing complexity and cost. Additionally, constructing the crack-detection wire using the same process as the functional wiring ensures that any process-related factors would be reflected in both, thereby improving the reliability of defect detection.

191. Furthermore, Tanabe also uses thin-film manufacturing for its wiring structures. Tanabe, [0069]. Because both references use compatible fabrication methods, it would have been obvious to a skilled artisan to fabricate the diagnostic wiring as a thin film, formed at the same time as other thin-film features—such as the bus lines—on the device. This approach is consistent with standard industry practice and would be expected to yield predictable, reliable results.

2. Dependent Claim 8

192. Claim 8 of the '762 patent depends from Claim 7 and recites, “[a] display device according to claim 7, *wherein the fourth signal interconnect has a colored thin film layer or a thin film layer having a transmittance at a predetermined level or less.*”

193. Claim 7 is rendered obvious by Tanabe in view of Miyagawa for at least the reasons I describe above.

194. In my opinion, Tanabe in view of Miyagawa renders obvious “[a] display device according to claim 7, wherein the fourth signal interconnect” (Miyagawa:

diagnostic wiring 90) “has a colored thin film layer or a thin film layer having a transmittance at a predetermined level or less.”

195. Tanabe discloses fabrication of multilayer gate and drain signal lines, where one layer may be composed of chrome and another of aluminum. Tanabe, [0073]–[0074]. Tanabe further instructs that the same materials can be used for different components in in the same layer, a practice that promotes manufacturing efficiency. *Id.*, [0076], [0086]. A POSITA would have recognized the benefit of this approach for streamlining production and ensuring material compatibility across device components. Similarly, Miyagawa discloses that multiple components, including the diagnostic wiring, are formed simultaneously, and further specifies that chrome may be used for signal lines. Miyagawa, [0024], [0017]. Given the compatible teachings of Tanabe and Miyagawa, it would have been obvious to use chrome for the diagnostic wiring in the combined device.

196. Furthermore, at the thickness typically used for signal lines, chrome is not transparent and exhibits a transmittance at or below the unspecified predetermined level referenced in the claim. A skilled artisan would have understood that using chrome for the diagnostic wiring would naturally result in a low-transmittance thin film, consistent with the requirements of claim 8. This approach would have been suitable because chrome is a good conductor and commonly formed on display panels using thin film deposition.

3. Dependent Claim 9

197. Claim 9 of the '762 patent depends from Claim 7 and recites “[a] *display device according to claim 7, wherein the fourth signal interconnect has a thin metal film layer.*”

198. Claim 7 is rendered obvious by Tanabe in view of Miyagawa, for at least the reasons I describe above.

199. In my opinion, Tanabe in view of Miyagawa renders obvious “[a] display device according to claim 7, wherein the fourth signal interconnect” (Miyagawa: diagnostic wiring 90) “has a thin metal film layer.”

200. Claim 9 simply adds the requirement that the fourth signal interconnect is made of metal, which is a straightforward design choice in light of the disclosures discussed above. *Supra* §X.A.3.

201. Given that chrome is a well-known and commonly used metal in thin-film display fabrication, a POSITA would have found it obvious to use chrome as the material for the diagnostic wiring. *Supra* §X.B.2. This choice would be consistent with standard manufacturing practices.

4. Dependent Claim 10

202. Claim 10 of the '762 patent depends from Claim 7 and recites “[a] *display device according to claim 7, wherein the fourth signal interconnect is formed of two or more conductive thin films.*”

203. Claim 7 is rendered obvious by Tanabe in view of Miyagawa, for at least the reasons described above.

204. In my opinion, Tanabe in view of Miyagawa renders obvious “[a] display device according to claim 7, wherein the fourth signal interconnect” (Miyagawa: diagnostic wiring 90) “is formed of two or more conductive thin films.”

205. Claim 10 simply adds the requirement that the diagnostic wiring consists of at least two layers of conductive thin film. *Supra* §X.A.4.

206. Both Tanabe and Miyagawa provide analogous teachings regarding the construction of signal lines using thin film technology. *Supra* §X.B.2. Notably, Tanabe explicitly discloses the use of multilayer signal lines, where one layer may be chrome and another aluminum. Tanabe, [0073]–[0074]. Both materials are well known to be conductive.

207. A POSITA would have found it obvious to fabricate the diagnostic wiring as a multilayer structure, formed simultaneously with Tanabe’s gate or drain signal lines, using established thin-film deposition techniques. This approach would be consistent with common manufacturing practices and would ensure that the diagnostic wiring possesses the desired electrical and physical properties to be compatible with other components of the display device.

5. Dependent Claim 12

208. Claim 12 of the '762 patent depends from Claim 7 and recites “[a] *display device according to claim 7, wherein the flexible interconnect substrate has electrode terminals connected to the fourth signal interconnect at a position different from that of the region forming the electrode terminal connected with the external system.*”

209. Claim 7 is rendered obvious by Tanabe in view of Miyagawa, for at least the reasons described above.

210. In my opinion, Tanabe in view of Miyagawa renders obvious “[a] display device according to claim 7, wherein the flexible interconnect substrate,” (Tanabe: flexible substrate 70) “has electrode terminals connected to the fourth signal interconnect” (Miyagawa: diagnostic wiring 90) “at a position different from that of the region forming the electrode terminal connected with the external system.”

211. As previously discussed, it would have been a matter of design choice for a POSITA to couple the diagnostic wiring directly to the flexible substrate in Tanabe’s configuration. *Supra* §§X.A.5; X.B.1.j. Based on Tanabe’s and Miyagawa’s combined teaching, the diagnostic wiring is routed on the TFT substrate directly to the electrode terminals, which are in turn coupled to the flexible substrate. *Supra* §X.B.1.j. The external system is connected to the opposite end of the flexible substrate. This common configuration was suitable for routing

signal lines from the external system to the substrate and allowed the flexible substrate (*e.g.*, a ribbon cable) to be bent at an appropriate angle.

6. Motivation to Combine

212. In my opinion, a POSITA would have been motivated to incorporate Miyagawa's diagnostic wiring to Tanabe's LCD panel.

213. Tanabe recognizes that defects can arise during display manufacturing and therefore discloses an inspection scheme for evaluating gate and drain electrodes within the pixel region. Tanabe, [0061]–[0065]. While Tanabe discloses a technique to simplify inspection of drain and gate electrodes of pixels, it does not address peripheral crack detection. As discussed above, a POSITA would have understood that the process of cutting a mother substrate into individual display panels can introduce cracks into the substrate. *Supra* §VII. Given this industry-wide challenge and the importance of early defect detection, a POSITA would have been motivated to incorporate additional solutions—such as the peripheral crack-detection wiring taught by Miyagawa—to further enhance defect detection capabilities in LCD panels.

214. Miyagawa provides a solution for diagnosing substrate cracks by making it easy to identify them, thereby improving manufacturing yield and reducing waste. *See* Miyagawa, [0004], [0031]. Miyagawa also explains that detecting cracks after each manufacturing stage that could cause these cracks helps prevent unnecessary

installation of components on defective substrates, further enhancing efficiency and reducing waste. *See Id.*, [0004], [0028], [0030]. Additionally, it was well understood in the field that glass substrates like those used in Tanabe are inherently brittle, rendering obvious that Miyagawa's benefits apply to Tanabe and making it clear that the advantages of Miyagawa's crack-detection strategy would be equally relevant to Tanabe's device. Given these benefits, and considering that Tanabe already emphasizes the importance of defect inspection, a POSITA would have been motivated to add a diagnostic wiring for crack detection. *See also supra* §X.B.1.j.

215. Implementing this addition would simply have involved forming an additional thin-film conductor around the periphery of Tanabe's TFT substrate. This task would have been well within the capabilities of a POSITA, as it merely requires surrounding the panel with a thin-film wire in a manner analogous to Miyagawa's diagnostic wiring. *See* Ex. 1014, Fig. 4; Ex. 1017, Fig. 9, [0043] (showing conventional traces for panel-crack detection). The modification is straightforward because the diagnostic wiring is electrically isolated from other circuits and components, so its inclusion does not introduce the complexity associated with interconnected circuitry.

216. Because this modification is simple and builds on well-understood technology, a POSITA would have had a reasonable expectation of success in

implementing it. Both Tanabe and Miyagawa disclose TFT LCDs with similar components and design principles. Adding a diagnostic wire to Tanabe's substrate based on Miyagawa's teachings is simply an application of a known technique to achieve a similar improvement, yielding predictable results. The '762 patent itself acknowledges that the LCD devices in its embodiments were "well-known." Ex. 1001, 4:11–14. The same is true for the devices described by Tanabe and Miyagawa.

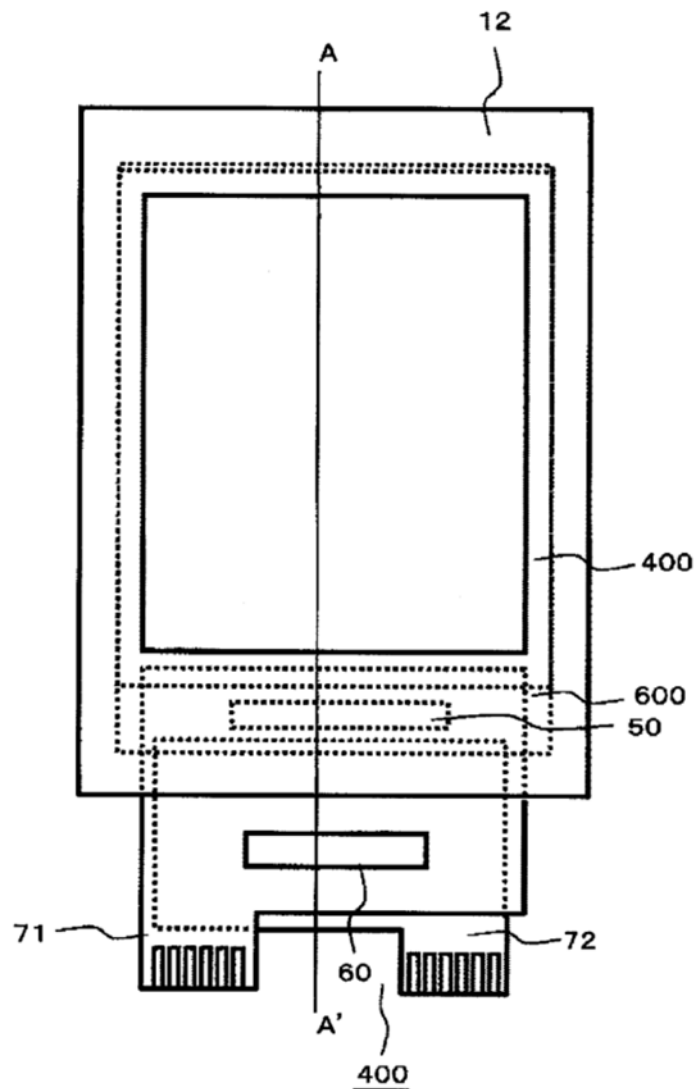
C. GROUND 3: Anno '704 in View of Miyagawa Renders Obvious Claims 1–4 and 6

1. Independent Claim 1

217. In my opinion, Anno '704, in combination with Miyagawa, renders Claims 1-4 and 6 of the '762 patent obvious.

a) 1[pre]

218. In my opinion, Anno '704 discloses *a display device* (display device 300 with a touch panel 400). Anno '704, Abstract; [0048].



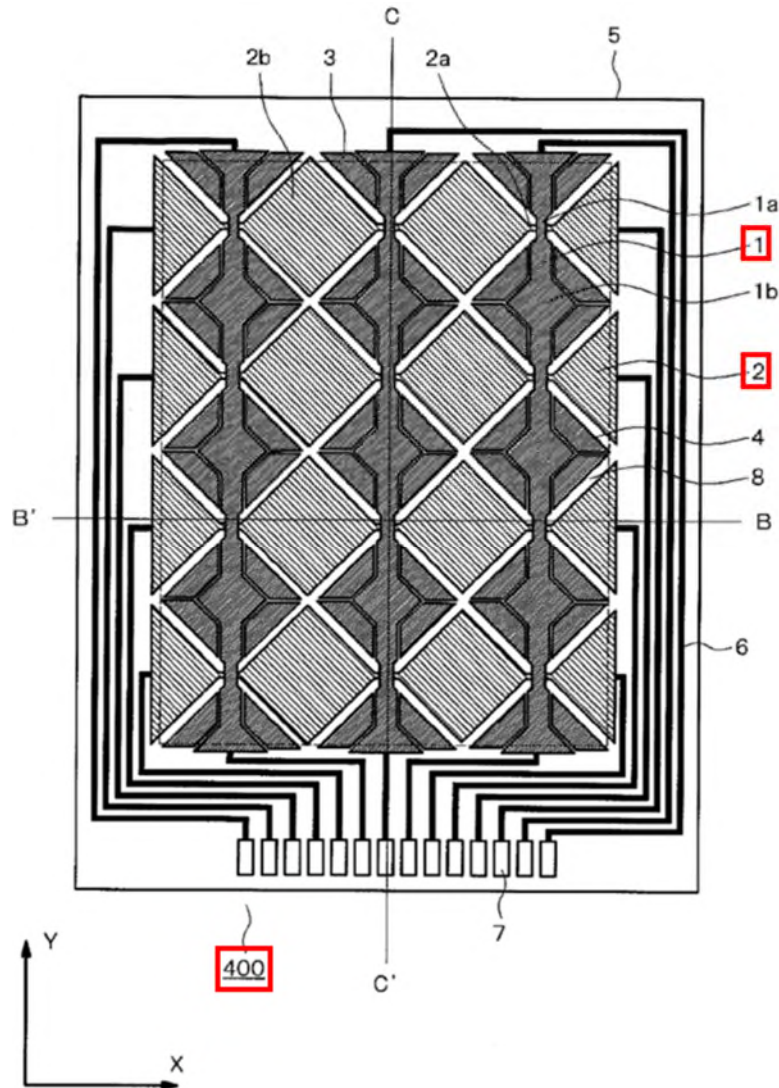
Id., Fig. 1⁵, Abstract; [0048].

b) 1[a]

219. In my opinion, Anno '704 discloses “*a coordinate input device.*”

⁵ The numeral 400 on the bottom of Figure 1 should be 300 based on paragraph [0048].

220. Specifically, Anno '704's display device comprises "a coordinate input device," referred to as a touch panel 400. Anno '704, Abstract, [0060]–[0061].



Id., Fig. 3.

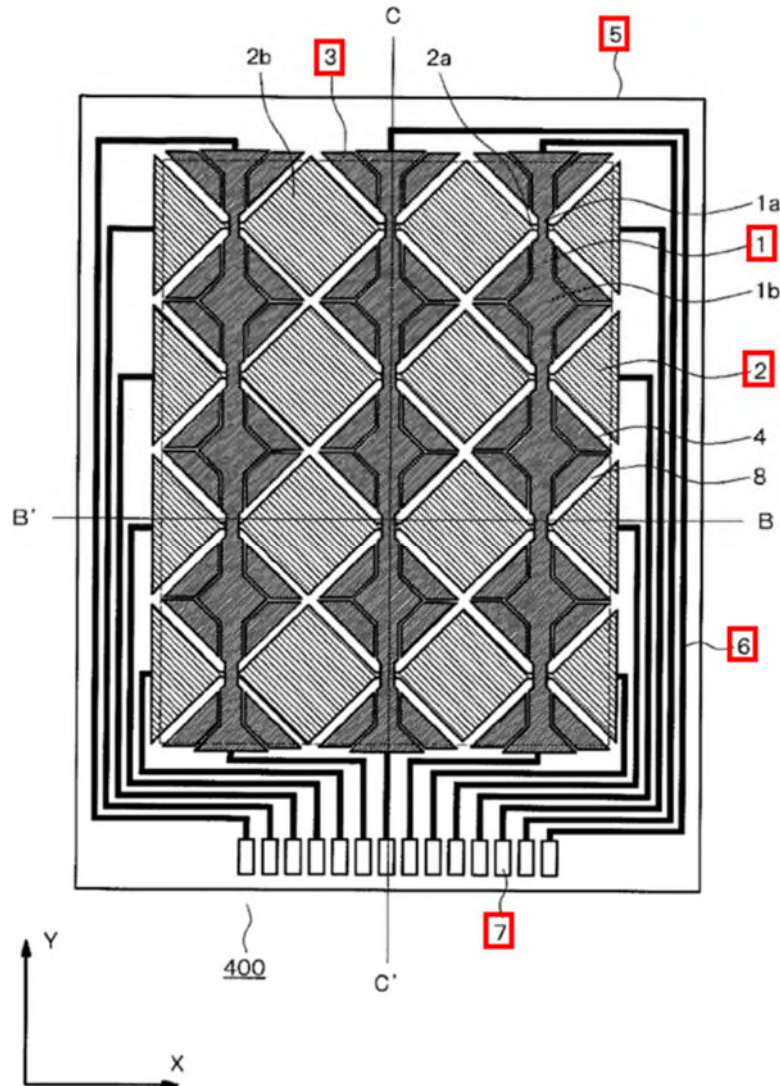
221. Anno '704 discloses a touch panel structure similar to that of the '762 patent, in which the touch panel has two sets of X/Y (electrodes 1 and 2), arranged perpendicularly to each other to detect a point of touch. Anno '704, Abstract,

[0060]–[0061]. Touch is detected by detecting a change in capacitance of the electrodes. *Id.*, [0060].

c) 1[a.1]

222. In my opinion, Anno '704 discloses a touch panel “*including a transparent substrate having detection electrodes disposed in a detection region corresponding to a contact position, the transparent substrate having a first signal interconnect disposed in a region outside the detection region, the first signal interconnect having one end connected to the detection electrodes and being formed with a first electrode terminal at the other end thereof.*”

223. Specifically, Anno '704 discloses a touch panel “including a transparent substrate” (glass substrate 5) “having detection electrodes” (X/Y electrodes 1–2) “disposed in a detection region” (input region 3) “corresponding to a contact position, the transparent substrate having a first signal interconnect” (wiring lines 6) “disposed in a region outside the detection region, the first signal interconnect having one end connected to the detection electrodes and being formed with a first electrode terminal” (connection terminals 7) “at the other end thereof.”



Anno '704, Fig. 3.

224. The touch panel 400, as disclosed in Anno '704, includes a glass substrate 5, which is “employed as a transparent substrate.” *Id.*, [0058]–[0059]. The “glass substrate 5” is a foundational layer for the touch panel 400. For example, Anno '704 explains that the X/Y electrodes 1,2 (*i.e.*, detection electrodes) are formed on a surface of this substrate and are designed to detect changes in capacitance resulting from contact within an input region 3. *Id.*, [0059]–[0060], [0011]. When a

user touches the input region, the user's finger behaves as a conductive object that increases the capacitance of the electrodes at the contact area. The increase in capacitance results in a longer voltage rise time. *Id.*, [0089]–[0094], Figs. 13–14. A control circuit monitors this voltage rise time, and when it exceeds a predetermined threshold, the system interprets this as a touch event at that specific location.

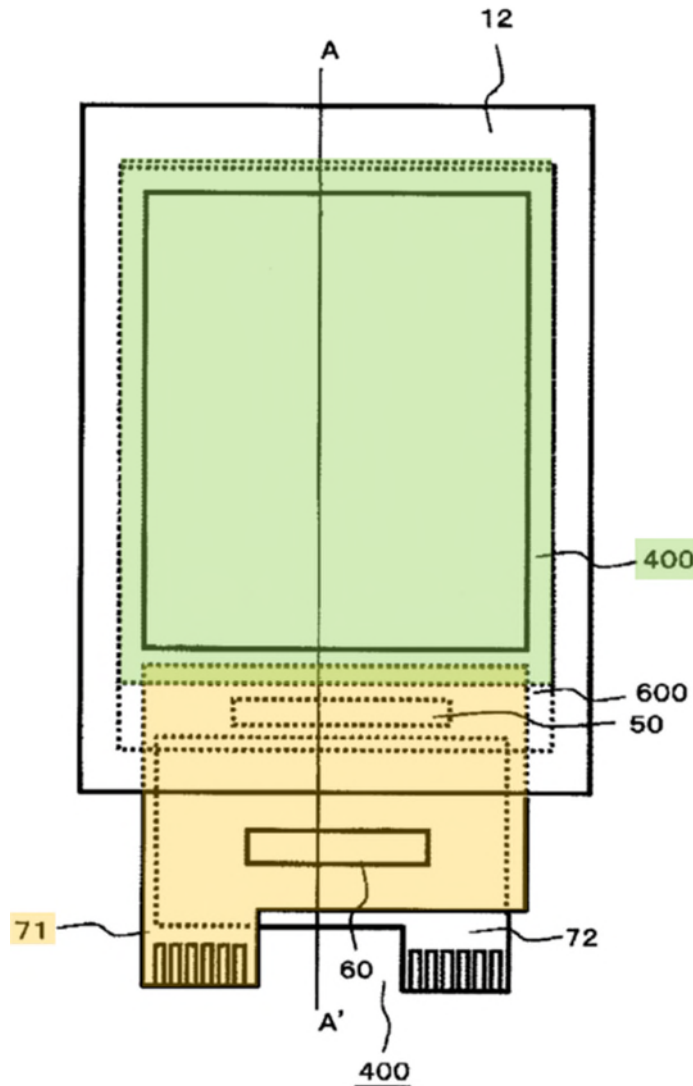
225. Additionally, peripheral wiring lines 6 are formed outside of the input region 3 on the glass substrate. Peripheral wiring lines 6 serve to connect the connection terminals 7 to the X/Y electrodes 1–2 (*i.e.*, detection electrodes). *Id.*, Fig. 3, [0059], [0078]–[0079]. The wiring lines convey signals between the X/Y electrodes 1–2 and a control circuit to facilitate the touch functionality. *Id.*, [0056], [0060].

d) 1[a.2]

226. In my opinion, Anno '704 discloses or at least renders obvious a display device that includes, “*a flexible interconnect substrate connected to the first electrode terminal, the flexible interconnect substrate used for supplying a driving signal to the detection electrodes by way of the first signal interconnect and extracting a detection signal from the detection electrodes.*”

227. Specifically, Anno '704 discloses or at least renders obvious a touch panel including “a flexible interconnect substrate” (flexible printed circuit board 71) “connected to the first electrode terminal” (connection terminals 7), “the flexible

interconnect substrate used for supplying a driving signal to the detection electrodes” (X/Y electrodes 1–2) “by way of the first signal interconnect” (wiring lines 6) “and extracting a detection signal from the detection electrodes.”



Anno '704, Fig. 1 (showing touch panel 400 attached to circuit board 71), Fig. 2 (showing same in a cross-sectional view), [0056].

228. Anno '704 teaches that a touch panel control circuit 60 is mounted to the flexible printed board 71 to control the detection of an input point and other

operations. *Id.*, [0056]. In order for the control circuit to perform these functions, a POSITA would have understood that the flexible printed board must be connected to the connection terminals, which are connected to the electrodes and the wirings on the touch panel.

229. As discussed above, the control circuit is responsible for detecting input positions, for example, by calculating the touch location from detection signals derived from changes in capacitance. *Id.*, [0056], [0060]. This involves supplying the detection electrodes with a constant current, measuring the rise times to a reference voltage at the electrodes, and determining the touch location based on the rise times. *Id.*, [0089]–[0094], Figs. 13–14. This control functionality necessarily involves both supplying driving signals to, and extracting detection signals from, the X/Y electrodes, as these operations are essential to the functioning of the touch panel. Additionally, a POSITA would have recognized that wiring lines 6 connect the X/Y electrodes to the control circuit, a point further confirmed by a later patent publication from the same inventor. *See* Ex. 1021, [0089]–[0090], [0093]–[0096]. Thus, it is clear that signals are supplied to and extracted from the detection electrodes via the wiring lines.

e) 1[b]

230. In my opinion, Anno '704 discloses “*a display panel for image display based on a video signal from an external system, the coordinate input device being disposed on the display panel at the side of a display screen.*”

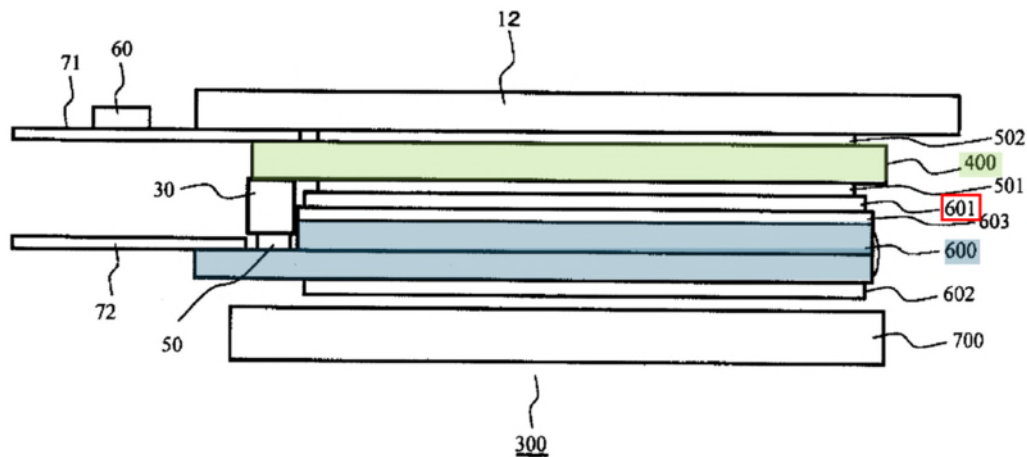
231. Specifically, Anno '704 discloses a liquid crystal “display panel” (liquid crystal display panel 600) “for image display based on a video signal from an external system, the coordinate input device” (touch panel 400) “being disposed on the display panel at the side of a display screen” (polarizing plate 601).

232. In preferred embodiments of the '762 patent, the external system is connected to the flexible printed substrate (FPC) through electrode terminals (TRM2). Ex. 1001, 8:33–38, 14:62–15:2. This was well known and routine by the time of the patent. *Id.*, 4:11–14.

233. Anno '704's display device comprises liquid crystal display panel 600, which is capable of displaying images such as video. Anno '704, [0012], [0055], [0100]; *see also* Fig. 2. Anno '704 further describes the use of a flexible printed circuit board to carry signals “from the outside,” *i.e.*, from an external system, such as a mobile device, to the display panel. *Id.*, [0005], [0055]; *see also* Miyagawa, [0020] (an electronic apparatus body). This configuration, in which the external system communicates with the display device via a flexible printed circuit and dedicated connection terminals, is directly analogous to the arrangement in the

'762 patent, where the external system is connected to the flexible printed substrate (FPC) via electrode terminals (TRM2). Furthermore, by 2010, connecting to an external system was already a common practice for a display panel in an electronic device.

234. As in the '762 patent, Anno '704's touch panel 400 is arranged "on an observer side of the liquid crystal display panel 600." Anno '704, [0048].



Id., Fig. 2. This too was routine because the touch detection mechanisms such as detecting changes in capacitance require the touch surface to be positioned at the very top on which direct contact with a touching finger can occur without intervening layers such as a display panel to potentially interfere with a sensitive measurement with small signals.

f) 1[c]

235. In my opinion, Anno '704 in view of Miyagawa renders obvious a display device "*wherein the coordinate inputting device has a second signal interconnect*

disposed outside the first signal interconnect but near the peripheral edge of the transparent substrate, the second signal interconnect surrounding the area where the detection region is included and the first signal interconnect is formed, the second signal interconnect being opened at opposite ends thereof and being connected to respective electrode terminals for inspection at the open ends.”

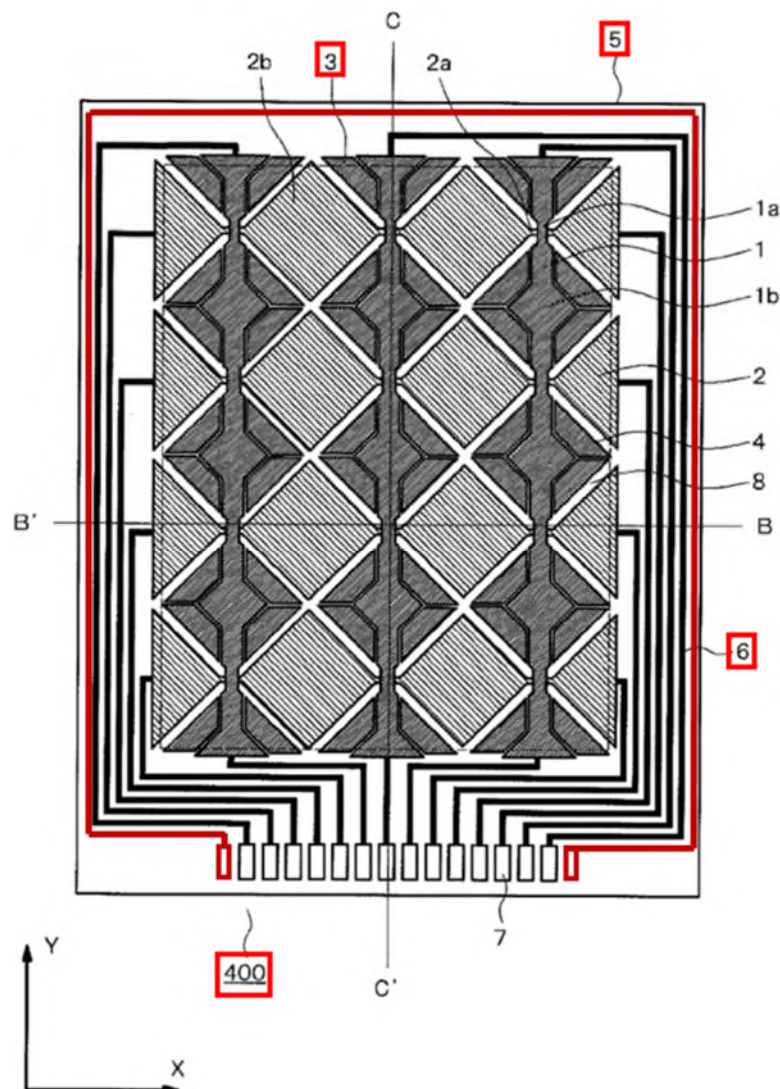
236. Specifically, Anno '704 in view of Miyagawa renders obvious a display device “wherein the coordinate inputting device” (Anno '704: touch panel 400) “has a second signal interconnect” (Miyagawa: diagnostic wiring 90) “disposed outside the first signal interconnect” (Anno '704: wiring lines 6) “but near the peripheral edge of the transparent substrate” (Anno '704: glass substrate 5), “the second signal interconnect surrounding the area where the detection region” (Anno '704: input region 3) “is included and the first signal interconnect is formed, the second signal interconnect being opened at opposite ends thereof and being connected to respective electrode terminals” (Miyagawa: first and second diagnostic pads 91–92) “for inspection at the open ends.”

237. Notably, claim limitation 1[c] closely parallels claim limitation 7[f], with the primary distinction being that the crack-detection wiring in 1[c] surrounds the detection region on the touch-panel substrate, whereas in 7[f] it surrounds the display area on a display-panel substrate. The nomenclature also differs in immaterial ways, with claim 1[c] referring to the “second signal interconnect” and

“first signal interconnect,” and claim 7[f] referring to the “fourth signal interconnect” and “third signal interconnect,” respectively:

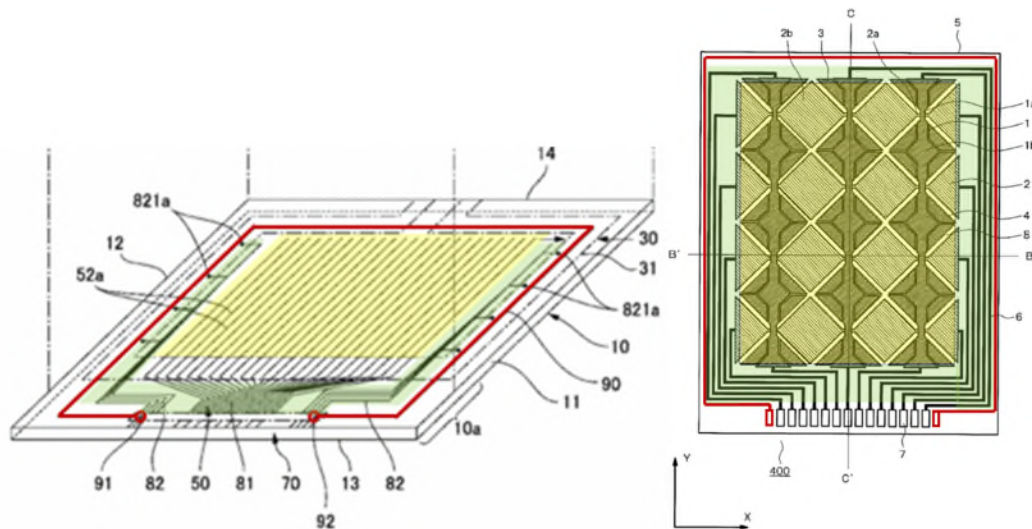
Claim Limitation 1[c]	Claim Limitation 7[f]
second signal interconnect	fourth signal interconnect
first signal interconnect	third signal interconnect

238. Miyagawa discloses or renders obvious claim limitation 7[f], as discussed above. *Supra* X.A.1.j. It would have been obvious to a POSITA to apply Miyagawa’s teaching on diagnostic wiring on Anno ’704’s touch panel 400, positioning the diagnostic wiring outside wiring line 6 and near the peripheral edge of the glass substrate 5, such that the diagnostic wiring surrounds both the input region 3 and wiring line 6:



Anno '704, Fig. 3 (diagnostic wiring and pads in dark red added).

239. This configuration would have been obvious due to the structural similarities between touch-panel and display-panel substrates—both feature an active region (for display or detection) that is surrounded by functional wiring:



Miyagawa, Fig. 3 (partial); Anno '704, Fig. 3 (diagnostic wiring and pads in dark red added).

240. Furthermore, it is standard practice in the field to place panel-crack-detection wiring near the edges of the substrate, close to the dividing lines used to separate a mother substrate into individual substrates, and to have such wiring surround the functional components and wiring that the crack-detection feature is intended to monitor. This arrangement ensures that any crack or break affecting the functional area or wiring will also disrupt the crack-detection wiring, thereby enabling reliable inspection for substrate integrity. *Supra* §VII.

g) 1[d]

241. In my opinion, Anno '704 in view of Miyagawa at least renders obvious a display device “*wherein the second signal interconnect is formed of a thin conductive film disposed along the peripheral edge portion of the transparent substrate.*”

242. Specifically, Anno '704 in view of Miyagawa at least renders obvious a display device wherein the second signal interconnect (Miyagawa: diagnostic wiring 90) is formed of a thin conductive film disposed along the peripheral edge portion of the transparent substrate (Anno '704: glass substrate 5).

243. Claim limitation 1[d] is substantially similar to claim limitation 7[g], with the primary differences being the nomenclature (“second signal interconnect” versus “fourth signal interconnect” and “thin conductive film” versus “conductive thin film”), and the fact that limitation 1[d] does not require the film to be disposed along “three sides” of the substrate. Thus, Miyagawa at least renders obvious claim limitation 1[d] for the same reason it at least renders obvious claim limitation 7[g].

Supra §X.A.1.k.

244. Specifically, Miyagawa discloses using a thin conductive film for the diagnostic wiring, which is formed simultaneously with the main signal lines and is positioned along the periphery of the substrate. *See supra* §X.A.1.k. Applying this teaching to Anno '704's touch panel would have been obvious to a POSITA, as both references describe transparent substrates with functional wiring, and it was standard practice to form multiple wirings in one step for manufacturing efficiency. Thus, the combination of Anno '704 and Miyagawa renders obvious claim limitation 1[d].

245. Additionally, a POSITA would have considered multiple materials to be obvious choices for the second signal interconnect. Miyagawa teaches that “chrome lines or the like” can be used for both data lines and diagnostic wiring, making chrome an obvious option. *See* Miyagawa, [0017]; *supra* §X.A.2.

Additionally, Anno '704 describes forming its wiring lines 6 from a silver alloy film. *See* Anno '704, [0078]. Given that Miyagawa allows for materials similar to chrome, it would also have been obvious to use silver alloy for the second signal interconnect, or even for the first signal interconnect if desired. That is, both the wiring lines 6 and the diagnostic wiring may be formed of chrome or silver alloy (among other choices) on Anno '704's substrate.

h) 1[e]

246. In my opinion, Anno '704 in view of Miyagawa renders obvious, “*wherein the second signal interconnect is disposed along the peripheral edge of three sides of the transparent substrate.*”

247. Specifically, Anno '704 in view of Miyagawa renders obvious a display device “wherein the second signal interconnect” (Miyagawa: diagnostic wiring 90) “is disposed along the peripheral edge of three sides of the transparent substrate” (Anno '704: glass substrate 5). *Supra* §X.C.1.f; §X.A.1.j–k.

248. It would have been obvious for a POSITA to apply Miyagawa's diagnostic wiring configuration to Anno '704's touch panel, given the structural similarities

between the devices and the well-established practice of arranging crack-detection or inspection wiring along the edges of a substrate to monitor for cracks. Thus, the combination of Anno '704 and Miyagawa renders obvious the arrangement required by this claim limitation.

2. Dependent Claim 2

249. Claim 2 of the '762 patent depends from Claim 1 and recites, “[a] *display device according to claim 1, wherein the second signal interconnect has a colored thin film layer or a thin film layer having a transmittance at a predetermined level or less.*”

250. In my opinion, Anno '704 in view of Miyagawa renders obvious “[a] display device according to claim 1.” *Supra* §X.C.1. Anno '704 in view of Miyagawa further renders obvious a display device “wherein the second signal interconnect” (Miyagawa: diagnostic wiring 90) “has a colored thin film layer or a thin film layer having a transmittance at a predetermined level or less.”

251. The additional limitation of claim 2 is identical to that of claim 8, with the second and the fourth signal interconnects serving as analogous counterparts in the respective claims. Miyagawa renders this limitation obvious, as discussed above. *Supra* §X.A.2.

252. Alternatively, Anno '704 in combination with Miyagawa renders it obvious to use a silver alloy for the second signal interconnect. *See supra* §X.C.1.g. Anno

'704 specifically notes that “the silver alloy film 15 ... is opaque,” meaning it has a transmittance at or below some predetermined level (which Claim 2 does not specify).

3. Dependent Claim 3

253. Claim 3 of the '762 patent depends from Claim 1 and recites, “[a] *display device according to claim 1, wherein the second signal interconnect has a thin metal film layer.*”

254. In my opinion, Anno '704 in view of Miyagawa renders obvious “[a] display device according to claim 1.” *Supra* §X.C.1. Anno '704 in view of Miyagawa further renders obvious a display device “wherein the second signal interconnect” (Miyagawa: diagnostic wiring 90) “has a thin metal film layer.”

255. The additional limitation of claim 3 is identical to that of claim 9, with the second and the fourth signal interconnects serving as analogous counterparts in the respective claims. Miyagawa renders this limitation obvious. *Supra* §X.A.3.

256. Alternatively, Anno '704 in combination with Miyagawa renders obvious that the second signal interconnect could also be formed from a silver alloy film. *See supra* §X.C.1.g. A silver alloy film is a thin metal film layer.

4. Dependent Claim 4

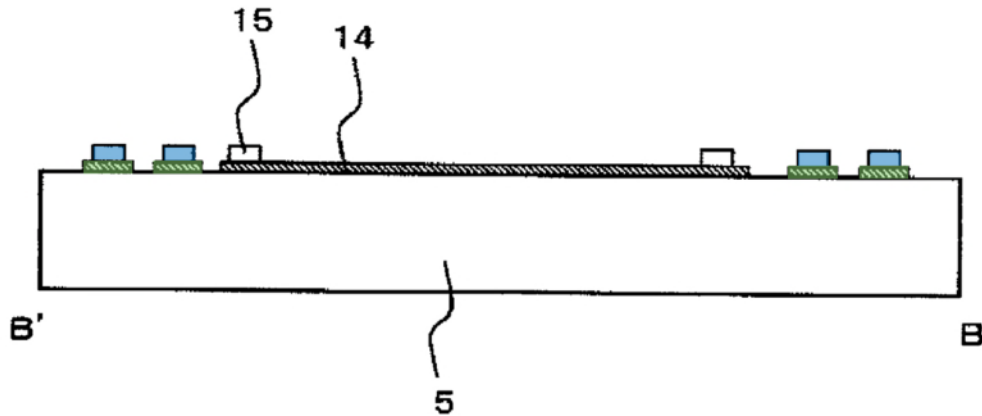
257. Claim 4 of the '762 patent depends from Claim 1 and recites, “[a] *display device according to claim 1, wherein the second signal interconnect is formed of two or more conductive thin films.*”

258. In my opinion, Anno '704 in view of Miyagawa renders obvious “[a] display device according to claim 1.” *Supra* §X.C.1. Anno '704 in view of Miyagawa further renders obvious “wherein the second signal interconnect” (Miyagawa: diagnostic wiring 90) “is formed of two or more conductive thin films.”

259. The additional limitation of claim 4 is identical to that of claim 10, with the second and the fourth signal interconnects serving as analogous counterparts in the respective claims. Miyagawa renders this limitation obvious, as discussed above. *Supra* §X.A.4.

260. Alternatively, a POSITA would have found it obvious to utilize Anno '704's disclosure regarding wiring lines 6 to form the second signal interconnect, as discussed above in Section X.C.1.g. Anno '704 describes the fabrication of wiring lines 6 by sequentially depositing an indium tin oxide (ITO) film 14 and a silver alloy film 15, followed by patterning the wiring using a standard photolithography process. Anno '704, [0074]–[0079]. This process yields a wiring structure composed of two conductive thin films. Anno '704's figures illustrate the resulting multi-layer wiring pattern. For example, Figures 5 and 9 provide cross-sectional

views of the wiring lines corresponding to two cross sections of the plan view of Figure 3.



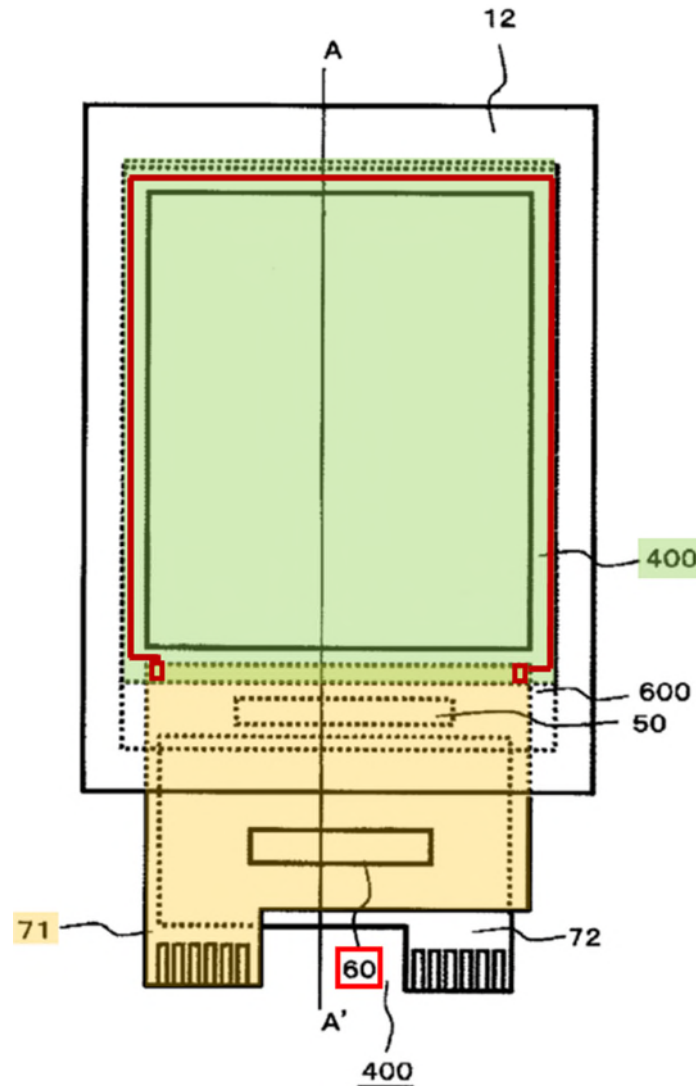
Id., Fig. 5 (cross-sectional view); see also *id.*, Fig. 9 (same), Fig. 3 (plan view).

5. Dependent Claim 6

261. Claim 6 of the '762 patent depends from Claim 1 and recites, “[a] display device according to claim 1, wherein the flexible interconnect substrate has a third electrode terminal connected to the second signal interconnect at a position different from that of the region for forming the second electrode terminal connected with an external system.”

262. In my opinion, Anno '704 in view of Miyagawa renders obvious “[a] display device according to claim 1.” *Supra* §X.C.1. Anno '704 in view of Miyagawa further renders obvious “wherein the flexible interconnect substrate” (Anno '704: flexible printed circuit board 71) “has a third electrode terminal connected to the second signal interconnect” (Miyagawa: diagnostic wiring 90) “at a position

different from that of the region for forming the second electrode terminal connected with an external system.”



Anno '704, Fig. 1 (diagnostic wiring and pads in dark red added on the peripheral of touch panel 400).

263. As illustrated in Figure 1, Anno '704 discloses a touch panel control circuit 60 mounted to the flexible printed board 71. *Id.*, [0056]. Likewise, Miyagawa describes an embodiment in which a driving IC is mounted on a flexible substrate,

and the diagnostic pads are connected to the IC via the flexible substrate.

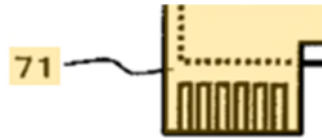
Miyagawa, [0040]; *supra* §X.A.1.j.

264. A POSITA would have would have recognized that the diagnostic wiring approach described in Miyagawa could be readily applied on Anno '704's touch panel architecture. Specifically, a POSITA would have understood that it was an obvious design choice to add diagnostic or test features—such as crack detection—to an IC because ICs were routinely used to implement control, processing, and detection functions.

265. Moreover, a POSITA would have appreciated that integrating the substrate crack diagnostic unit of the driving IC, as taught by Miyagawa, into Anno '704's control circuit would not have required any unconventional modifications. Instead, it would have simply involved adding diagnostic functionality to the existing control circuit, which is a straightforward enhancement with a predictable result. Indeed, ICs typically comprised multiple modules performing various functions, and a diagnostic or test feature simply would have been an additional function to incorporate into an IC design. Such an implementation would be well within the routine skill set of a POSITA, who is accustomed to adapting known circuit configurations to achieve desired testing or diagnostic capabilities.

266. In this arrangement, the diagnostic wiring would be electrically connected to the flexible printed circuit board through electrode terminals interfacing with

diagnostic pads at the ends of the diagnostic wiring. These terminals are positioned where the glass substrate overlaps with the flexible printed circuit board, consistent with conventional layouts for signal and diagnostic connections. At the opposite end of the flexible printed circuit board is the second electrode terminal, which connects to an external system:



Anno '704, Fig. 1 (partial). A later prior-art publication by the same inventor expressly discloses such a configuration. *See* Ex. 1021, [0090] (external-device-side input/output terminals 74 on flexible printed circuit board 71), Fig. 5.

267. Thus, in this typical configuration, the electrode terminals on the flexible printed circuit board that are connected to the diagnostic wiring and those connected to an external system are located at opposite ends of the flexible printed circuit board, as would be expected by a POSITA seeking to optimize layout and functionality. Examples of an external system include the mobile equipment disclosed in Anno '704 and the electronic apparatus body disclosed in Miyagawa. *See* Anno '704, [0005]; Miyagawa, [0020].

268. Accordingly, the combination of Anno '704 and Miyagawa reflects nothing more than the application of well-known engineering principles and routine design choices that a POSITA would employ to achieve predictable and reliable results.

6. Motivation to Combine

269. A POSITA would have been motivated to implement diagnostic wiring for panel-crack detection, as taught by Miyagawa, on Anno '704's touch panel, and would have had a reasonable expectation of success in doing so.

270. The motivation for this combination is grounded in the same rationale discussed above with respect to Tanabe in view of Miyagawa. *Supra* §X.B.6.

Specifically, both display panels and touch panels are typically fabricated by cutting a brittle mother substrate into individual panels, a process that unavoidably causes the formation of edge cracks or chips that can compromise panel integrity.

See supra §VII. For instance, Anno '704's touch substrate, like Tanabe's, is constructed from glass—a brittle material. *See* Tanabe, [0073]; Anno '704, [0059].

Additionally, the functional wiring layouts of touch substrates closely resemble those of display substrates, as both feature an active region (containing touch or display elements) surrounded by signal wiring. Therefore, a POSITA would have readily appreciated that the advantages described in Miyagawa, such as early detection of broken signal lines and reduced manufacturing waste, are directly applicable to Anno '704's touch panel device. Additionally, the use of diagnostic wiring for crack detection—such as that described in Miyagawa—would be equally applicable and beneficial in the context of Anno '704's touch panel.

271. The addition of diagnostic wiring to Anno '704's touch-panel glass substrate would have been a straightforward and routine modification for a POSITA. This step merely involves adding an additional thin-film conductor around the periphery of the panel, in a manner analogous to Miyagawa's diagnostic wiring. *See* Ex. 1014, Fig. 4; Ex. 1017, Fig. 9, [0043] (showing a conventional trace for panel-crack detection for either "[a] touch panel or display panel"). Anno '704 already uses conductive thin film in the touch panel structure. *See* Anno '704, [0054], [0060], [0068], [0078]. The implementation of diagnostic wiring would not require any fundamental changes to the panel's operation or circuitry, as such wiring is isolated from other functional circuits and components. This isolation greatly simplifies integration, as it avoids the complexity and risk of unintended interactions that can arise when modifying interconnected circuit elements.

272. Furthermore, a POSITA would recognize that touch panels and LCDs share similar configurations. This similarity is expected, as the touch-detection area of a touch panel is often designed to overlap the display area, enabling users to interact directly with displayed images. The addition of diagnostic wiring to Anno '704's substrate, following Miyagawa's approach, would thus represent nothing more than the application of a well-known and widely adopted technique for improving panel reliability—a technique that has already been proven effective in analogous contexts.

273. Given these factors, a POSITA would have had a reasonable expectation of success in combining the teachings of Anno '704 and Miyagawa. The modification involves a simple and predictable enhancement, leveraging established industry practices to achieve a known benefit—namely, early detection of substrate cracks to improve manufacturing yield and product reliability.

274. Indeed, the '762 patent itself acknowledges the LCD devices of its embodiments were “well-known.” Ex. 1001, 4:11–14. The same is true for the devices described in Anno '704 and Miyagawa, further supporting the predictability of the outcome.

275. Therefore, the combination of Anno '704 and Miyagawa reflects the routine application of established engineering principles and industry practices that a POSITA would have employed to achieve reliable and predictable improvements in touch panel technology.

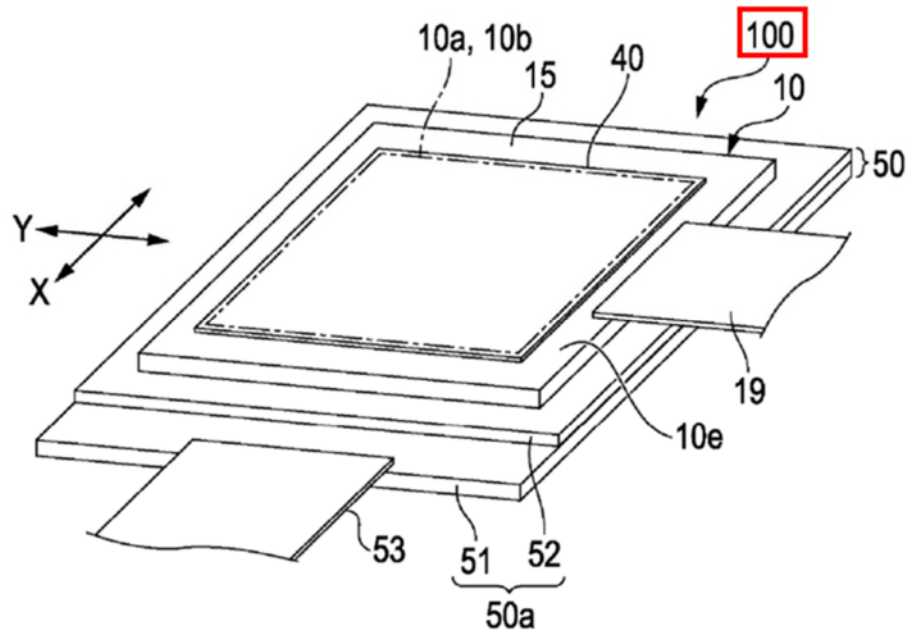
D. GROUND 4: Matsuo in View of Nakamura Renders Obvious Claims 1–4 and 6

1. Independent Claim 1

276. In my opinion, Matsuo in view of Nakamura renders Claims 1-4 and 6 of the '762 patent obvious.

a) 1[pre]

277. In my opinion, Matsuo discloses *a display device*, such as “a display apparatus with an input function 100.” Matsuo, [0038].

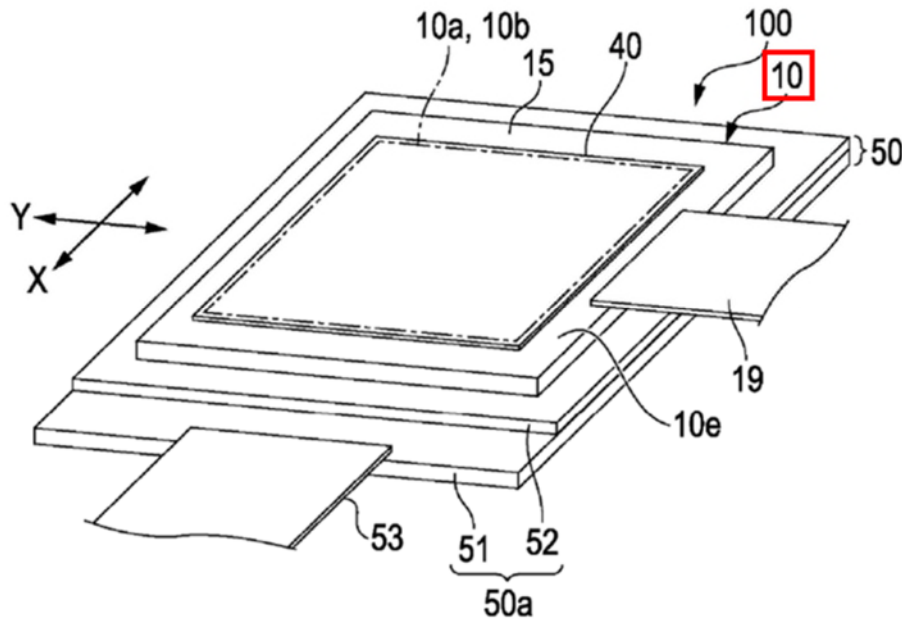


Id., Fig. 1.

b) 1[a]

278. In my opinion, Matsuo discloses a display device that includes “*a coordinate input device.*”

279. Specifically, Matsuo’s display device incorporates “a coordinate input device,” such as “a panel-shaped input device 10 (touch panel)” of the display apparatus 100. Matsuo, [0038].

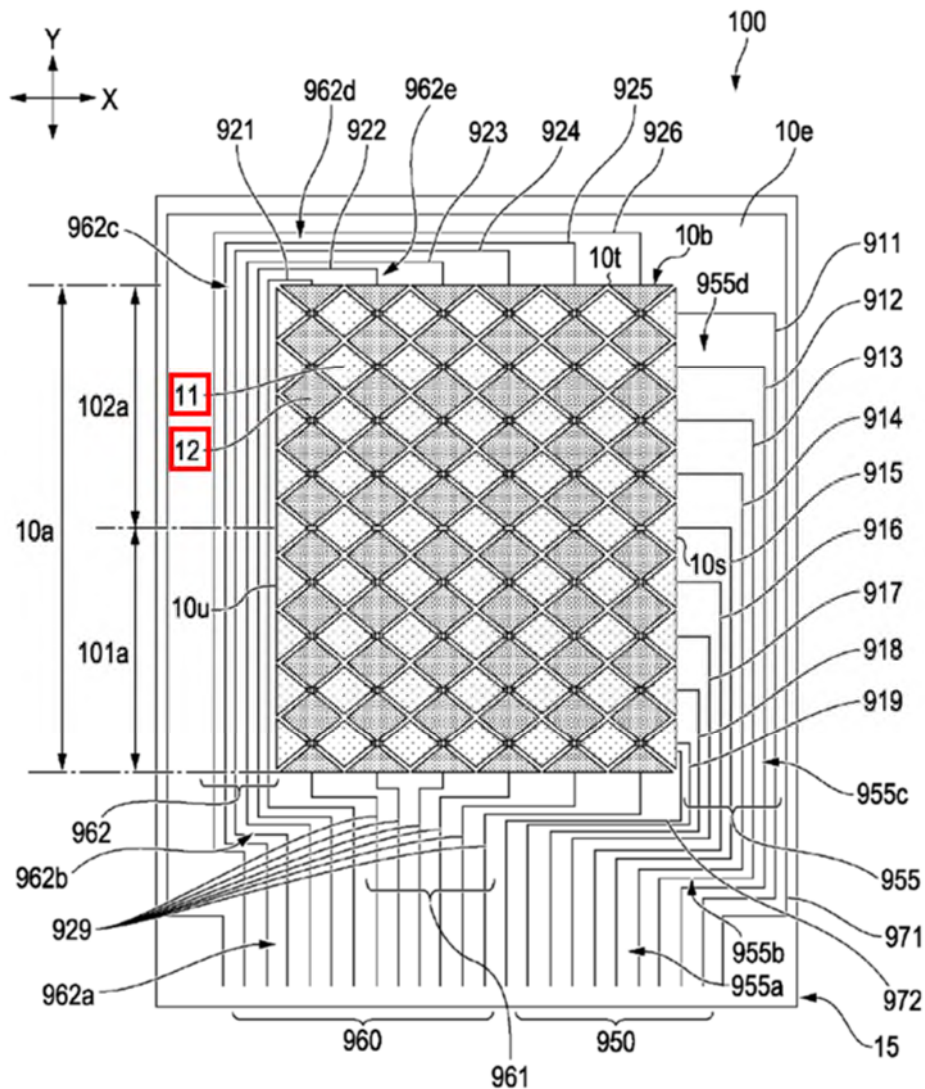


Id., Fig. 1.

280. A coordinate input device in a display system enables detection of the position of a user's touch or input in both the X and Y directions on the display panel. *See* Ex. 1001, 4:26–28. This capability can be achieved through the use of electrodes within the coordinate input device that extend along the X and Y axes.

Id., 6:56–7:2.

281. Consistent with this common understanding of a coordinate input device of a touch display, Matsuo's input device 10 is equipped with two sets of detection electrode patterns, identified as 11 and 12, which are arranged to extend in perpendicular directions across the top surface of the panel. *See* Matsuo, Abstract, [0039]–[0041], Figs. 2, 3A. These directions are indicated by the arrows marked X and Y in the figure below:



Id., Fig. 2.

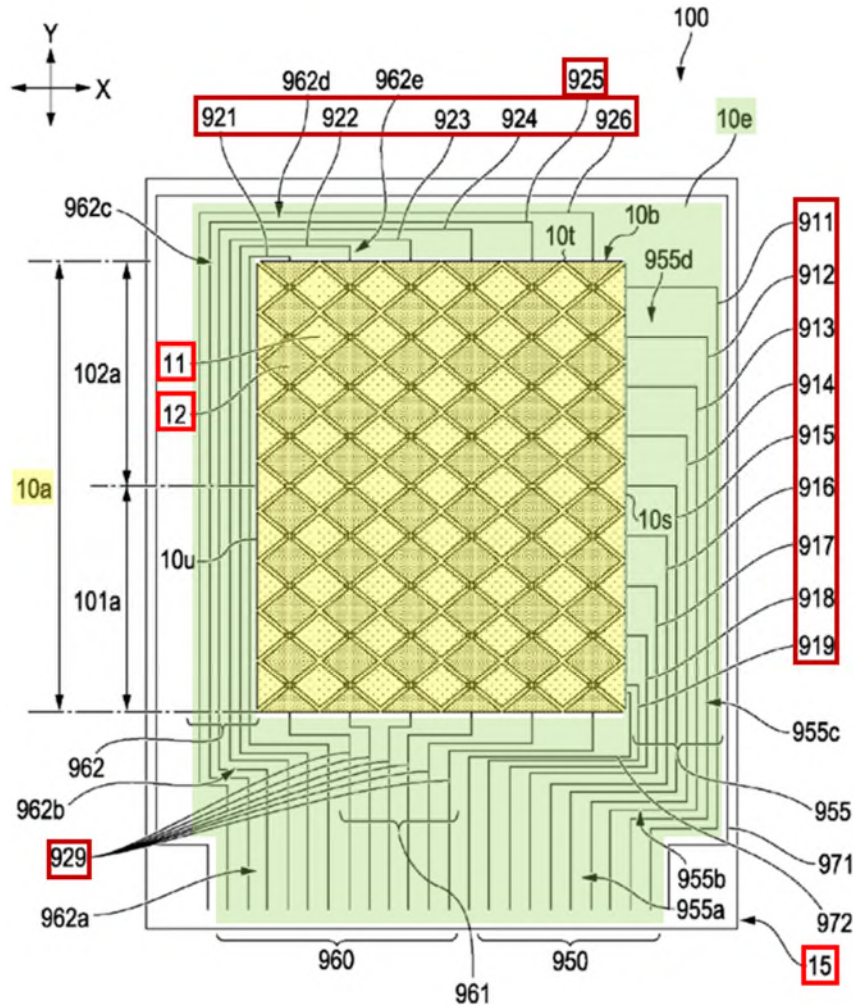
c) 1[a.1]

282. In my opinion, Matsuo discloses an input device that includes, “*a transparent substrate having detection electrodes disposed in a detection region corresponding to a contact position, the transparent substrate having a first signal interconnect disposed in a region outside the detection region, the first signal*

interconnect having one end connected to the detection electrodes and being formed with a first electrode terminal at the other end thereof.”

283. Matsuo’s input device 10 includes “a transparent substrate” (translucent substrate 15) “having detection electrodes” (electrode patterns 11–12) “disposed in a detection region” (input area 10a) “corresponding to a contact position, the transparent substrate having a first signal interconnect” (metal lines 9a, which includes lines 911–919, 921–926, and 929) “disposed in a region” (peripheral area 10e) “outside the detection region, the first signal interconnect having one end connected to the detection electrodes and being formed with a first electrode terminal” (terminals 19a) “at the other end thereof.”

284. More specifically, Matsuo discloses that the input device is constructed on a translucent substrate 15, upon which the detection electrode patterns 11–12 are formed. Matsuo, [0040]. These electrodes form an input area 10a. *Id.* A voltage is applied to the detection electrodes sequentially. *Id.*, [0041]. When a user touches any location within this area, the user’s finger forms capacitors with the electrodes nearby, changing the capacitance and the waveforms of the applied voltage around the position of contact. The device is able to detect this change and determine the position of contact. *Id.*



Id., Fig. 2, [0048]–[0049] (description of Figure 2).

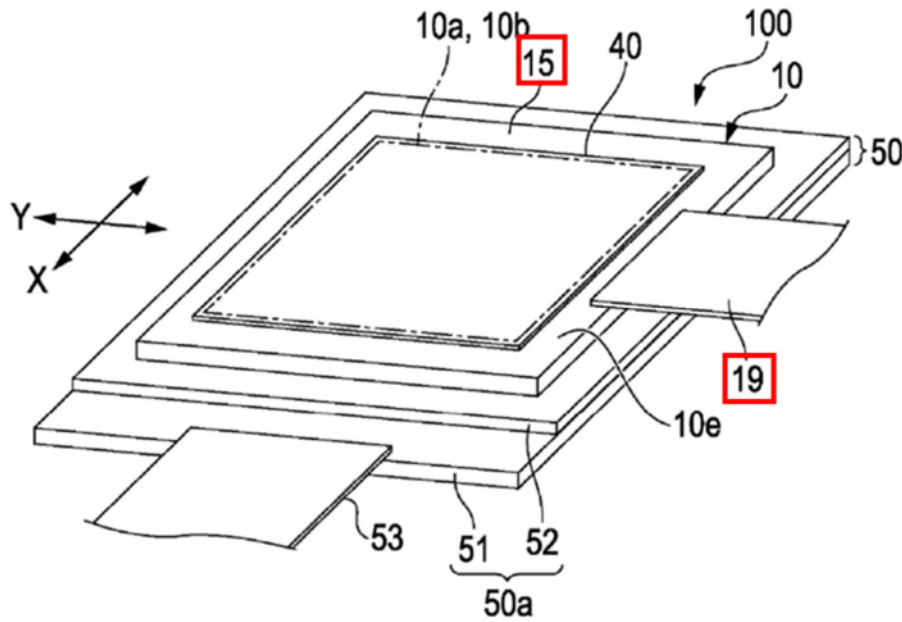
285. As illustrated in Figure 2 of Matsuo, metal lines 9a—including lines 911–919, 921–926, and 929—are formed in the “the outer area (peripheral area 10e) of the input area 10a” of the substrate. *Id.*, [0046]. One end of these metal lines is connected to the detection electrodes, establishing the necessary electrical contacts with the electrodes. *Id.* The opposite end of the metal lines is terminals 19a, which are designed to interface with “[a] flexible substrate 19” to connect to external circuitry for further signal processing. *Id.*

d) 1[a.2]

286. In my opinion, Matsuo discloses an input device 10 that includes *“a flexible interconnect substrate connected to the first electrode terminal, the flexible interconnect substrate used for supplying a driving signal to the detection electrodes by way of the first signal interconnect and extracting a detection signal from the detection electrodes.”*

287. Specifically, Matsuo discloses an input device 10 that incorporates “a flexible interconnect substrate” (flexible substrate 19) “connected to the first electrode terminal” (terminals 19a). This “flexible interconnect substrate” is used to deliver “driving signals to the detection electrodes” (electrode patterns 11–12) via “the first signal interconnect” (metal lines 9a) “and to extract detection signals from the detection electrodes.”

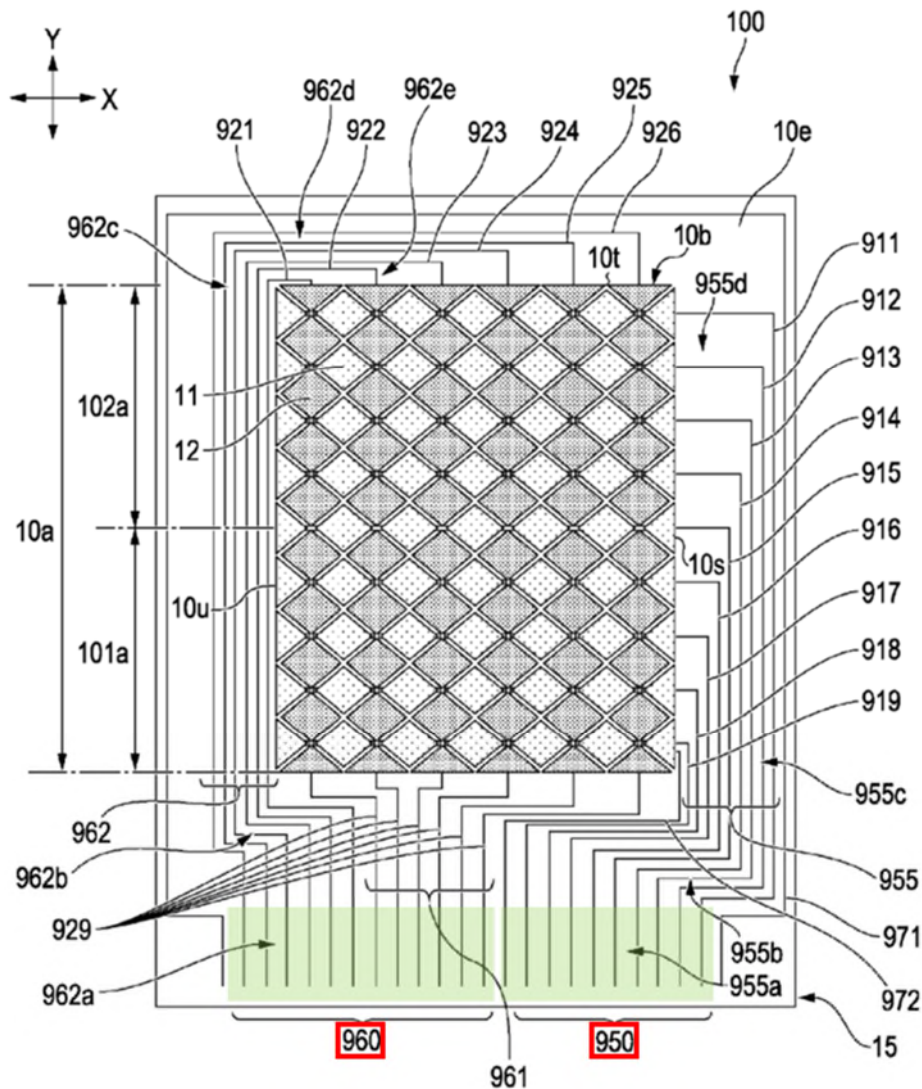
288. Matsuo describes an input device 10 that includes “a flexible substrate 19 connected to an end of the translucent substrate 15,” as illustrated below in Figure 1. Matsuo, [0039].



Id., Fig. 1.

289. The flexible substrate is connected to terminals 19a. *Id.*, [0046]. It is further connected to a drive circuit responsible for touch detection. *Id.*, [0039]. A chip-on-film technique was well known to attach ICs such as drive circuits to a flexible substrate, such as a ribbon cable.

290. It would have been at least obvious to a POSITA that the flexible substrate is used both “*for supplying a driving signal to the detection electrodes*” (i.e., electrode patterns 11, 12) via the metal lines and for “*extracting detection signals*” *from those electrodes*. See *id.* Matsuo refers to first and second signal input/output areas (950 and 960) at the terminal ends of the metal lines, which are terminal 19a connected to the flexible substrate. Matsuo, [0048]–[0049]; Fig. 3C.



Id., Fig. 2.

291. The metal lines serve as the conduits for both input signals, which “charge” the detection electrodes by applying a voltage, and output signals, which indicate the detected touch point by reflecting reductions in electrostatic capacitance.

Matsuo, [0041]. This arrangement was common for capacitive touch panel in the field, as it enables the necessary two-way communication between the detection electrodes and the drive circuit.

292. Furthermore, the metal lines electrically connect the detection electrodes to the flexible substrate, which is coupled to the drive circuit for touch detection.

Supra §X.D.1.c. As shown in Matsuo's Figure 2 above, the detection electrodes are only connected to other circuits through the metal lines. Because the detection electrodes must both receive input signals and transmit output signals to function as intended, it is necessary for these signals to be routed through the electrodes' only connections, *i.e.*, the metal lines, and to the terminals and the flexible substrate. This configuration is consistent with established design practices and would have been an obvious and routine implementation for a skilled artisan.

e) 1[b]

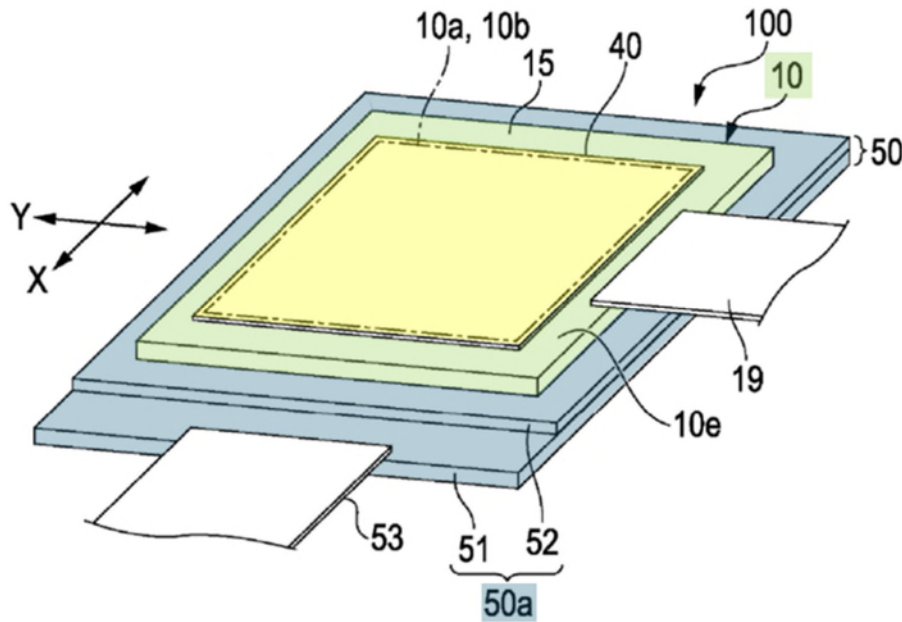
293. In my opinion, Matsuo discloses “*a display panel for image display based on a video signal from an external system, the coordinate input device being disposed on the display panel at the side of a display screen.*”

294. Specifically, Matsuo discloses a display device that includes “a display panel” (liquid crystal panel 50a) “for image display,” which operates “based on a video signal[s] from an external system.” “[T]he coordinate input device” (input device 10) is positioned “on the display panel” specifically on “the side facing the display screen” (polarizing plate).

295. In preferred embodiments of the '762 patent, the external system is connected to the flexible printed substrate (FPC) through electrode terminals (TRM2). Ex. 1001, 8:33–38, 14:62–15:2.

296. Matsuo's display device incorporates a liquid crystal device capable of "display[ing both] moving . . . and still images." Matsuo, [0038]. The images are generated based on video signals, which may be provided through a drive IC. *Id.* The liquid crystal panel is connected to a flexible substrate 53 that routes video signals from an external system, such as electronic apparatuses (*i.e.*, mobile phone sets), to the display panel. *Id.*, [0038], [0023], [0082].

297. Furthermore, Matsuo's input device 10 is mounted on the liquid crystal panel 50a at the side of a display screen, meaning it is positioned on the surface of the liquid crystal panel from which "display light is emitted." *Id.*, [0038]; *see also id.* cl. 9; Fig. 1. The light is often emitted from a polarizing plate. *Id.*, [0038]; Anno '704, Fig. 2, [0049]. This arrangement is consistent with routine practices in the field because the touch detection mechanism such as detecting changes in capacitance requires the touch surface to be positioned at the very top on which direct contact with a touching finger can occur without intervening layers such as a display panel to potentially interfere with a sensitive measurement with small signals.



Matsuo, Fig. 1.

f) 1[c]

298. In my opinion, Matsuo in view of Nakamura renders obvious a display device “*wherein the coordinate inputting device has a second signal interconnect disposed outside the first signal interconnect but near the peripheral edge of the transparent substrate, the second signal interconnect surrounding the area where the detection region is included and the first signal interconnect is formed, the second signal interconnect being opened at opposite ends thereof and being connected to respective electrode terminals for inspection at the open ends.*”

299. Specifically, Matsuo in view of Nakamura renders obvious a display device “wherein the coordinate inputting device” (Matsuo: input device 10) “has a second signal interconnect” (Matsuo: first auxiliary line 971), positioned “outside the first

signal interconnect” (Matsuo: metal lines 9a) “but near the peripheral edge of the transparent substrate” (Matsuo: translucent substrate 15). This “second signal interconnect” surrounds the region containing both “the detection region” (Matsuo: input area 10a) and the first signal interconnect, is open at both ends, and is “connected to respective electrode terminals for inspection at the open ends.”

300. Matsuo discloses the first auxiliary line 971, which is structurally a conductive line located outside the metal lines 9a, near the edges of the substrate, and enclosing both the input area 10a and the metal lines 9a. *See* Matsuo [0054]–[0055], Fig. 2. The first auxiliary line 971 serves as a shield line surrounding the detection area to reduce the impact of external noise on touch-detection sensitivity. Matsuo, [0019], [0056], [0077].

301. The shielding is accomplished by coupling the first auxiliary line 971 to a ground potential, thus forming an electrical ground around the substrate. *Id.*, [0056]. It is clear from the disclosure that the first auxiliary line 971 is located outside the metal lines 9a (lines 911–919, 921–926, and 929), near the edges of the translucent substrate 15, and encloses both the input area 10a and the metal lines 9a:



BOE Ex. 1003, p. 131
BOE v. Paneltouch
IPR2025-01482

terminals are accessible for electrical continuity testing at various stages of manufacturing, not just for grounding or noise shielding.

303. Functionally, the first auxiliary line 971 acts as as a shield line to which a ground potential may be applied to reduce the effect of external noise on touch-detection sensitivity. *Id.*, [0056]–[0057]. However, as Nakamura discloses, a “conventional shield line” can also serve as a panel-crack-detection line.

Nakamura, [0041]. Nakamura explains that “each defective line detection patterns D1 and D2 [crack detection lines] may be formed using a conventional shield line and the like as typically formed.” *Id.* A POSITA would have recognized that Matsuo’s first auxiliary line 971 is a conventional shield line and that conventional shield lines and conventional panel-crack-detection lines are similarly structured and can serve a dual purpose. *See supra* §VII. Therefore, it would have been obvious to use Matsuo’s first auxiliary line 971 as a panel-crack-detection line for inspection, as the structural design of Matsuo allows for continuity testing and the dual use is supported by Nakamura’s explicit teaching.

304. This inspection function can be accomplished by performing a simple continuity check: by applying a voltage between the terminals at the open ends of the first auxiliary line 971, a crack can be detected if electrical connection is interrupted due to a break in the line (*i.e.*, Matsuo: first auxiliary line 971; Nakamura: defective line detection pattern). Nakamura, [0043]. Nakamura’s use of

such a line for manufacturing crack detection complements Matsuo's operational usage of its first auxiliary line 971 for noise shielding. As further disclosed by Nakamura, such a panel-crack-detection line is formed along and near the edges of the substrate, just like Matsuo's first auxiliary line. Nakamura, Abstract, Fig. 1. This combination is straightforward and would have been readily implemented by a skilled artisan, as it leverages well-known techniques for both noise reduction and defect detection, and does not require any substantial redesign or change to the manufacturing sequence.

g) 1[d]

305. In my opinion, Matsuo in view of Nakamura at least renders obvious *“wherein the second signal interconnect is formed of a thin conductive film disposed along the peripheral edge portion of the transparent substrate.”*

306. Specifically, Matsuo teaches a display device in which “the second signal interconnect” (Matsuo: first auxiliary line 971) “is formed of a thin conductive film disposed along the peripheral edge portion of the transparent substrate” (Matsuo: translucent substrate 15).

307. Matsuo discloses that the first auxiliary line 971 is made from a conductive material, which allows a constant potential to be applied to reduce the impact of noise on touch detection. Matsuo, [0056], [0077]. This conductive material is

structurally and functionally suitable for use as a signal interconnect, and its placement along the substrate periphery is disclosed in Matsuo.

308. Additionally, Matsuo at least renders obvious that the first auxiliary line is formed of a thin film. The translucent electrode patterns, as described in Matsuo, are fabricated from thin films of ITO or IZO. *Id.*, [0047]. Matsuo also explains that the first auxiliary line 971 is fabricated simultaneously with metal lines that are connected to the electrode patterns. *Id.*, [0057]–[0058]. A POSITA would have recognized that all these features are formed together in a single step to enhance productivity and avoid unnecessary manufacturing complexity. This approach aligns with Matsuo’s stated objective of forming these components together in a single step to enhance productivity and avoid unnecessary manufacturing complexity. *Id.*, [0057]. Furthermore, it would have been routine and efficient for a POSITA to manufacture the auxiliary line using the same thin-film process as the other circuit features, particularly since industry-standard thin-film deposition techniques are commonly used for both signal lines and auxiliary/shield lines, as reflected in standard definitions of thin film. Ex. 1018, 3 (defining thin film as a technology “usually employed to form active or passive circuit components and interconnections”); Ex. 1019, 3 (defining thin film as using “metals and metal oxides that are ‘evaporated’ and then deposited on the substrate in the desired pattern to form the integrated circuit's passive components (wires, resistors, and

capacitors).” The use of thin-film conductive materials for such interconnects was well known and would have been an obvious design choice for a POSITA seeking to optimize process efficiency and device performance.

309. Furthermore, the first auxiliary line 971 is clearly disposed along the peripheral edge portion of the translucent substrate 15 (*e.g.*, “on the outer peripheral side”). Matsuo, Fig. 2, [0056], [0077]. My explanation above of claim limitation 1[c] also shows this configuration. *See supra* §X.D.1.f.

h) 1[e]

310. In my opinion, Matsuo discloses “*wherein the second signal interconnect is disposed along the peripheral edge of three sides of the transparent substrate.*”

311. Specifically, Matsuo teaches a display device in which “the second signal interconnect” (Matsuo: first auxiliary line 971) is positioned “along the peripheral edge of three sides of the transparent substrate” (Matsuo: translucent substrate 15). *Supra* §X.D.1.f; *see also* Matsuo, [0054]–[0055]. As discussed above, the first auxiliary line is arranged to run along three edges of the substrate, surrounding the detection region and associated circuitry. This configuration is apparent from the figures and descriptions in Matsuo, and would have been recognized by a POSITA as a routine and effective approach for implementing a shield wire or crack detection wire in such devices.

2. Dependent Claim 2

312. Claim 2 of the '762 patent depends from Claim 1 and recites, “[a] *display device according to claim 1, wherein the second signal interconnect has a colored thin film layer or a thin film layer having a transmittance at a predetermined level or less.*”

313. In my opinion, Matsuo in view of Nakamura renders obvious “[a] display device according to claim 1,” including that “the second signal interconnect” (Matsuo: first auxiliary line 971) is formed as a thin film layer. *Supra* §X.D.1. Furthermore, Matsuo in view of Nakamura further renders it obvious to implement “the second signal interconnect” (Matsuo: first auxiliary line 971) as “a colored thin film layer or a thin film layer with a transmittance at” or below a “predetermined level.”

314. Matsuo discloses that the first auxiliary line can be fabricated at the same time as the metal lines 9a, indicating that the first auxiliary line is made of metal. Matsuo, [0057]. Nakamura teaches the use of “a light-shielding metal material, for example, Cr, Al, [or] Ti” for both its connection lines L1–L2 (which are analogous to Matsuo’s metal lines 9a) and its defective line detection patterns D1–D2 (which are analogous to Matsuo’s first auxiliary line 971). Nakamura, [0035]–[0036], [0040]. These metals are known to have low optical transmittance, providing a “light-shielding” property. Each of chromium, aluminum, and titanium has a well-

known transmittance, and their use would satisfy a predetermined transmittance level as required by Claim 2.

315. A POSITA would have found it obvious to apply Nakamura's materials to Matsuo's first auxiliary line, thereby meeting the requirements of claim 2. Each of chromium, aluminum, and titanium is a metal and can be used to form Matsuo's metal lines and the first auxiliary line to perform their respective functions, which require that they are conductive.

3. Dependent Claim 3

316. Claim 3 of the '762 patent depends from Claim 1 and recites, “[a] *display device according to claim 1, wherein the second signal interconnect has a thin metal film layer.*”

317. In my opinion, Matsuo in view of Nakamura renders obvious “[a] display device ” as recited in claim 1. Additionally, this combination makes it obvious to implement “the second signal interconnect” (Matsuo: first auxiliary line 971) as “a thin metal film layer.”

318. This additional limitation is substantively identical to the requirements set forth in claims 1[d] and 2, and my discussions in those sections above apply. *Supra* §§X.D.1.g, X.D.2. Given that Matsuo discloses forming the first auxiliary line as a thin film, and Nakamura teaches the use of metal materials for similar structures, a

POSITA would have found it obvious to construct the second signal interconnect as a thin metal film layer.

4. Dependent Claim 4

319. Claim 4 of the '762 patent depends from Claim 1 and recites, “[a] *display device according to claim 1, wherein the second signal interconnect is formed of two or more conductive thin films.*”

320. In my opinion, Matsuo in view of Nakamura renders obvious “[a] display device” as recited in claim 1. Additionally, this combination makes it obvious to form “the second signal interconnect” (Matsuo: first auxiliary line 971) using “two or more conductive thin films.”

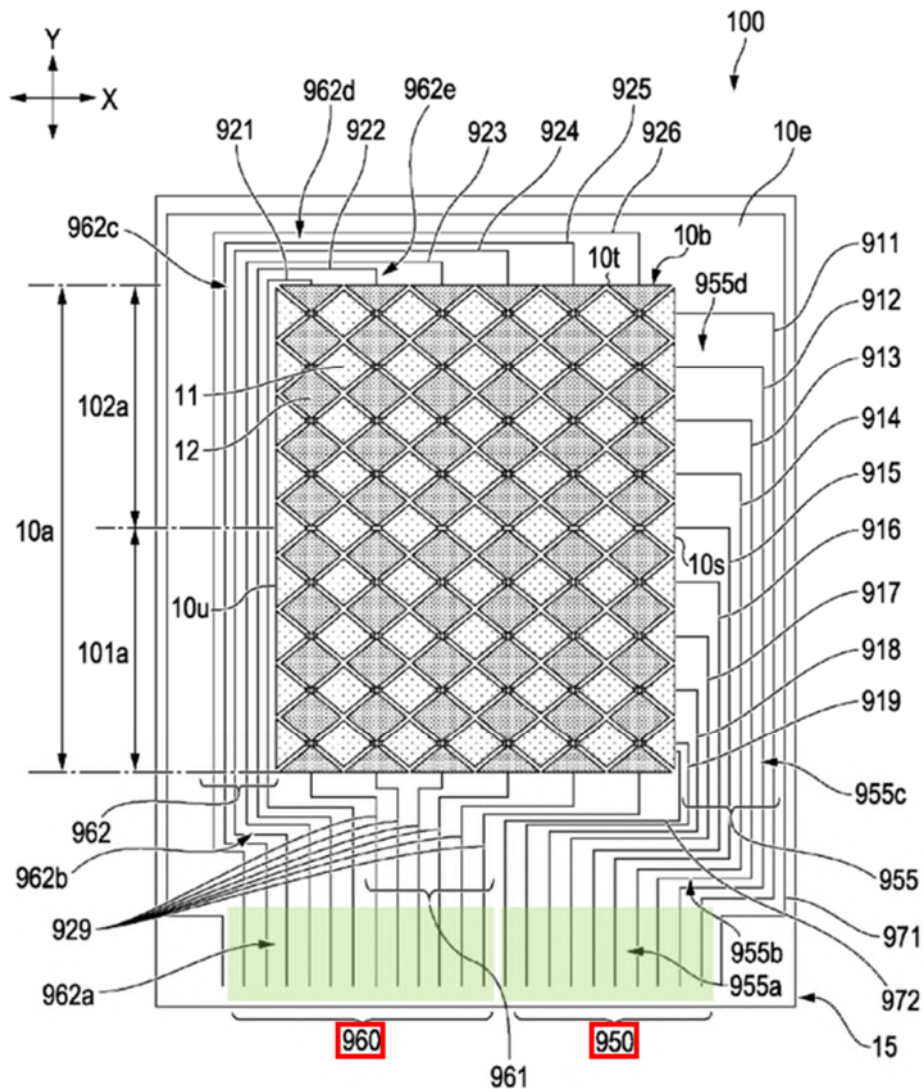
321. As previously discussed, Matsuo in view of Nakamura renders obvious that the first auxiliary line is constructed from conductive thin films. *Supra* §X.D.1.g. Claim 4 simply adds the requirement that the first auxiliary line consists of at least two layers of such films. Nakamura directly supports this limitation, as it discloses that its detection patterns (which are analogous to the Matsuo’s first auxiliary line) may be formed with “a *multilayer* structure....” Nakamura, [0035]. A POSITA would have found it obvious to fabricate the auxiliary line as a multilayer thin film, given the compatible teachings of Matsuo and Nakamura and the routine nature of multilayer thin film fabrication in the field.

5. Dependent Claim 6

322. Claim 6 of the '762 patent depends from Claim 1 and recites, “[a] *display device according to claim 1, wherein the flexible interconnect substrate has a third electrode terminal connected to the second signal interconnect at a position different from that of the region for forming the second electrode terminal connected with an external system.*”

323. In my opinion, Matsuo in view of Nakamura renders obvious “[a] *display device*” as recited in claim 1. Furthermore, this combination makes it obvious to implement a configuration in which “the flexible interconnect substrate” (Matsuo: flexible substrate 19) includes “a third electrode terminal connected to the second signal interconnect”(Matsuo: first auxiliary line 971) at a location “different from . . . the region” where “the second electrode terminal,” which is “connected with an external system,” is formed.

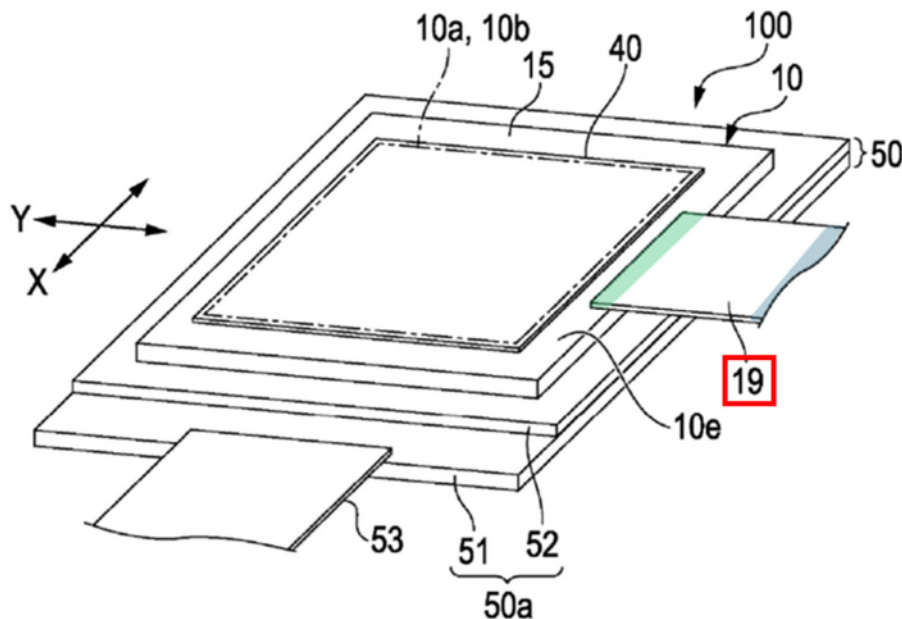
324. Matsuo discloses that the metal lines 9a end at electrode terminals 19a, which are used “for connecting the flexible substrate 19.” Matsuo, [0046]. These terminals are positioned within a first and second signal input/output area 950 and 960, as shown below. Matsuo, [0048]–[0049]; Fig. 2.



Id., Fig. 2.

325. Additionally, Matsuo specifies that the first auxiliary line is “connected to the outside via [respective] terminals,” which are “arranged in parallel” in the first and second signal input/output area 950 and 960. *Id.*, [0057]. This arrangement means that the flexible substrate 19 includes corresponding terminals that overlap and connected with the terminals of the first auxiliary line in a plan view.

326. It was a routine practice, or at least would have been obvious to a POSITA, to position “the region for forming [a] second electrode terminal connected with an external system” at the end of the flexible substrate 19 away from the panel substrate. This configuration facilitates straightforward connections between the flexible substrate with the external system, “such as mobile phone sets....”. *Id.*, [0023], [0082]. For example, the third electrode terminal (green shaded area), and the region for connecting with an external system (in or near the blue shaded area) are annotated and illustrated in Figure 1 of Matsuo below:



Id., Fig. 1.

6. Motivation to Combine

327. In my opinion, a POSITA would have been motivated to use Matsuo’s first auxiliary line for panel-crack detection in view of Nakamura.

328. As Nakamura explains, it was a routine practice to fabricate large mother substrates and then cut them into individual panels. Nakamura, [0003]. However, this routine process was also known to introduce defects, such as cracks or chips during this cutting process. *Id.*, [0011]. If such defects are not detected until after panel assembly, manufacturers risk wasting not only the panel itself but also expensive components, such as ICs, that may have already been installed before a defect is detected late in the manufacturing process. *Id.*, [0012]. Therefore, detecting panel cracks early in the manufacturing process, ideally before any components are installed, was a recognized need in the art for reducing manufacturing waste and associated cost. *Id.*

329. A POSITA, familiar with Matsuo, would have recognized that while Matsuo's first auxiliary line is described primarily as a shield for noise reduction, Matsuo does not address the problem of detecting cracks or breaks at the substrate periphery caused by the cutting process. Given the industry's ongoing challenge of yield loss due to undetected cracks, a POSITA would have been motivated to look for additional solutions. Nakamura directly addresses this gap by teaching the use of a peripheral detection pattern for crack detection, and further clarifies that such a pattern can be implemented using a conventional shield line. Nakamura, [0041]. Thus, Nakamura provides explicit guidance that the same type of line used for shielding can also serve as a crack-detection line.

330. Nakamura's solution for early crack detection would have motivated a POSITA to apply this teaching to Matsuo's device to reduce manufacturing waste. Nakamura specifically teaches that the detection pattern "may be formed using a conventional shield line and the like as typically formed." *Id.*; *supra* §VII. Because Matsuo's shield line (the first auxiliary line) and Nakamura's crack-detection line are structurally similar, both being conductive traces located at the panel periphery, it would have been obvious and straightforward for a POSITA to use Matsuo's first auxiliary line for crack detection. This dual function can be achieved by performing a simple continuity check, as Nakamura describes, by applying a voltage between the terminals at the ends of the auxiliary line and checking for electrical continuity. *See* Nakamura, [0043].

331. The fact that Matsuo discloses both a touch panel and a display panel, and Nakamura focuses solely on a display panel, does not diminish a POSITA's motivation to combine their teachings. Both touch panels and display panels are fabricated from large substrates and are susceptible to cracking or chipping during the cutting process. A POSITA would have recognized that a crack-detection trace is useful for both types of panels, since the underlying manufacturing challenges and risks are the same. *See* Ex. 1017, [0043]. Furthermore, Matsuo's figures show that its display panel and touch panel are of different sizes, showing that display

and touch panels undergo similar but separate cutting processes and can benefit from crack detection. *See* Matsuo, Fig. 1 (different panel sizes).

332. This rationale applies regardless of whether cutting or bonding occurs first, because in either manufacturing approach, the crack-detection traces are structurally fabricated prior to any cutting. These traces are designed to maintain their structural integrity throughout the singulation process, regardless of when it occurs, and thus the risk of crack-induced wiring defects exists in both scenarios. Accordingly, implementing crack detection using peripheral wiring is structurally applicable and beneficial in either case. Moreover, incorporating such peripheral wiring for crack detection enables testing for defects at an early stage in the manufacturing process, before additional components are added, thereby reducing waste and improving overall manufacturing efficiency.

333. Using Matsuo's auxiliary line for crack detection offers the additional benefit that the same component can serve two functions. Matsuo identifies its auxiliary line as a conventional shield line. Matsuo, [0019], [0077]. Nakamura teaches such shield lines are suitable for crack detection. Nakamura, [0041]. The crack-detection pattern is useful in manufacturing. *Supra* §X.D.1.f. The auxiliary line is useful to improve touch-detection sensitivity in operation. Matsuo, [0019], [0077]. Thus configuring the same wiring for both functions would have been a desirable dual use, avoiding additional manufacturing or material cost without

introducing complexity while improving device reliability and functionality. The functions are complementary and do not interfere with each other.

334. Furthermore, it would have been obvious to a POSITA that Matsuo's first auxiliary line is an example of Nakamura's conventional shield line. Both patents are assigned to Epson Imaging Devices Corp., and were contemporaneous in the same field. Matsuo, cover; Nakamura, Cover. It is reasonable to conclude that Nakamura and Matsuo were aware of their concurrent developments in the same company and both would consider a "conventional shield line" to encompass Matsuo's auxiliary line, especially given the shared assignee and overlapping subject matter.

335. Additionally, a POSITA would have been motivated to use Nakamura's single- or multilayer light-shielding material for Matsuo's first auxiliary line. Nakamura teaches using the same process and material to form both the connection lines and defective line detection pattern. Nakamura, [0040]. Leveraging the same process and material improves manufacturing efficiency. Similarly, Matsuo discloses forming the auxiliary line in the same step as forming the metal lines, which are analogous to Nakamura's connection lines. Matsuo, [0057]. Their analogous disclosures would have rendered it obvious to apply Nakamura's single- or multilayer metal thin films in the combination. This would have been nothing

more than exercising a design choice to apply a known process to achieve a predictable result.

336. Furthermore, a POSITA would have had a reasonable expectation of success in applying Nakamura's teachings of forming panel-crack detection lines using conventional shield line to Matsuo's first auxiliary line. Matsuo's auxiliary line is a conventional shield line, as a POSITA would have recognized and is similar in form to conventional crack-detection lines. *Supra* §VII. Specifically, both the auxiliary line for shielding and crack-detection lines are formed near the edges of the substrate surrounding the active areas for their respective functions. Using Matsuo's auxiliary line for crack detection simply involves performing a continuity check at an appropriate time during manufacturing. Both wirings are conductors with end terminals, allowing for applying an electrical potential and easy electrical continuity testing. Additionally, neither wiring contacts any other components on the substrate, as shown in Matsuo's Figure 2 and Nakamura's Figures 1 and 3A–3C. This physical isolation makes the combination of Matsuo and Nakamura's teachings straightforward. For example, applying a voltage for crack detection would not affect other circuits, and vice versa, because the physical isolation also electrically isolates the applied voltage from other components.

337. Finally, Nakamura's identification of metal materials and alternative single- or multilayer process for forming the detection patterns simply focuses the design

choice from Matsuo's broad disclosure to Nakamura's specific recommendations. Since the panels disclosed by both are used in familiar electronic devices, such as laptops with opaque display borders, using light-shielding metals for Matsuo's auxiliary line would have been an obvious design choice that would not detract from the appearances of these electronic devices. Such metals were known to be good conductors and methods to deposit them as a thin film on a substrate were well known. Applying Nakamura's specific recommendations would have involved nothing more than applying a known method for a known problem to achieve predictable results.

XI. SECONDARY CONSIDERATIONS

338. I am not aware of any secondary considerations that would overcome the strong showing of obviousness provided in this Declaration. None were identified during prosecution. *See generally* Ex. 1002. In the event that Patent Owner proffers any such evidence, I shall provide my opinions on such evidence in a reply declaration.

XII. DECLARATION

339. In signing this Declaration, I understand that it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the USPTO.

340. I am aware that willfully false statements and the like made by me in connection with this Declaration are punishable by fine or imprisonment, or both

(18 U.S.C. §1001) and may jeopardize the validity of the Petition. All statements herein made by me of my own knowledge are true and all statements made on information and belief are believed to be true.

Declaration of Richard A. Flasck, M.S.

U.S. Patent No. 8,704,762

I declare under penalty of perjury that the foregoing is true and correct.

Executed this 17th day of September, 2025 in San Ramon, CA.

A handwritten signature in blue ink, reading "Richard A. Flasck", is positioned above a horizontal line.

Richard A. Flasck, M.S.