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(54) **FLAT PANEL DISPLAY DEVICE**

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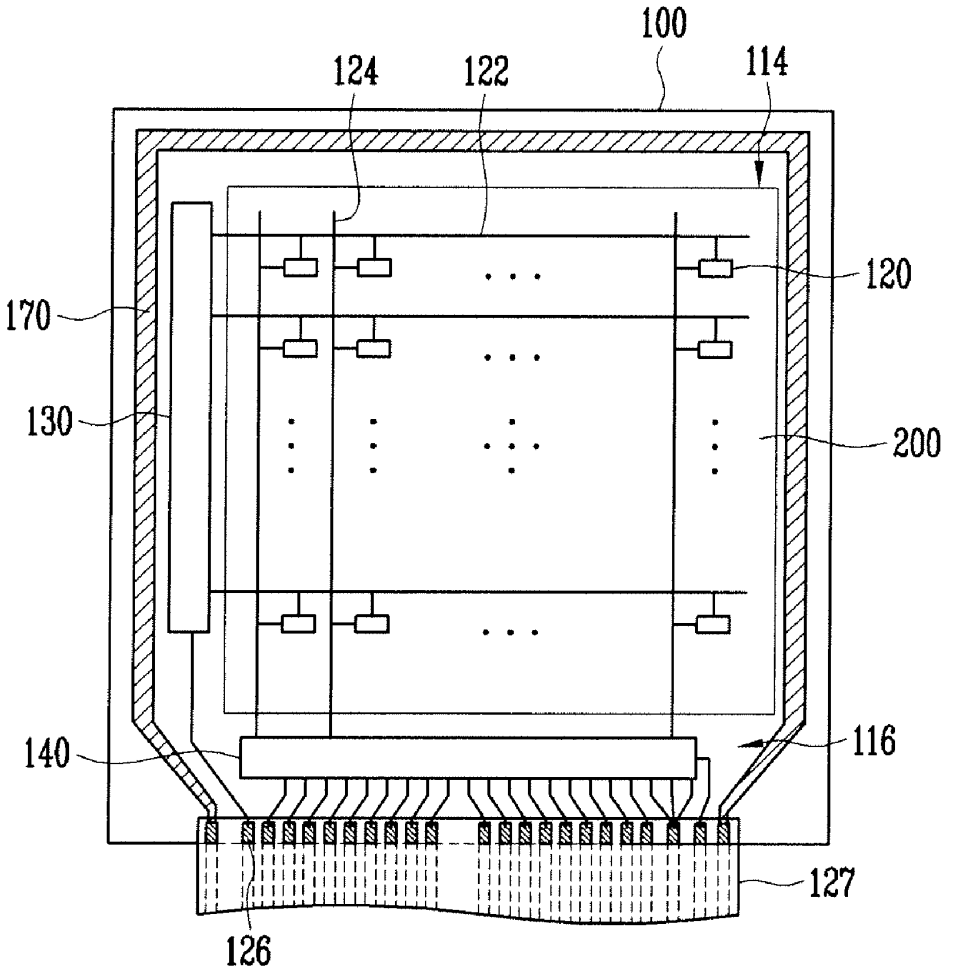
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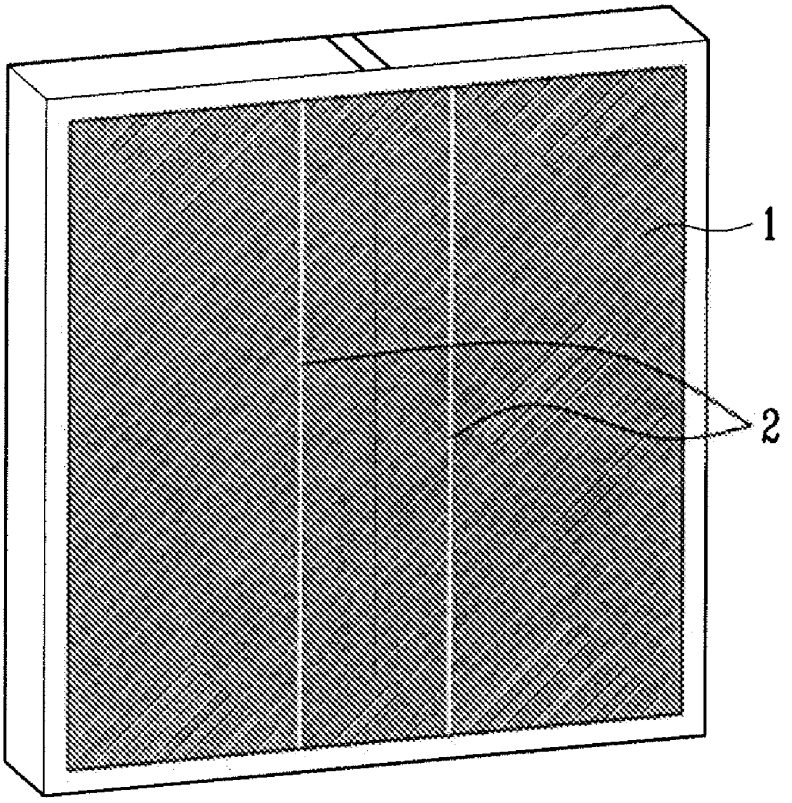
(57) **ABSTRACT**

A flat panel display device includes a first substrate having a first electrode and a shield wiring thereon, a second substrate having a second electrode thereon; a liquid crystal layer in a sealed space between the first electrode and the second electrode; and a driving circuit coupled with the first electrode and the second electrode through signal wirings, the shield wiring extending along an edge of the first substrate and electrically connected to ground.




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FIG. 1
(PRIOR ART)




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FIG. 2

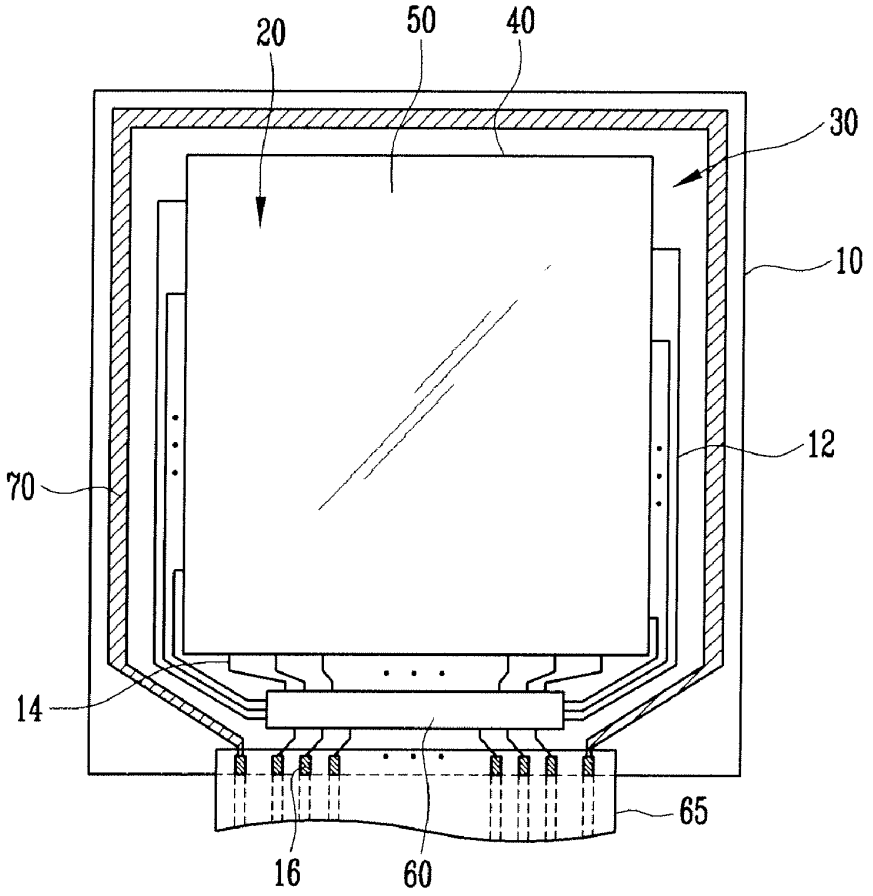
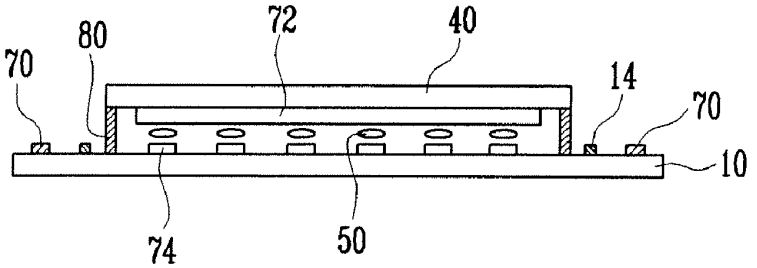



FIG. 3




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FIG. 4

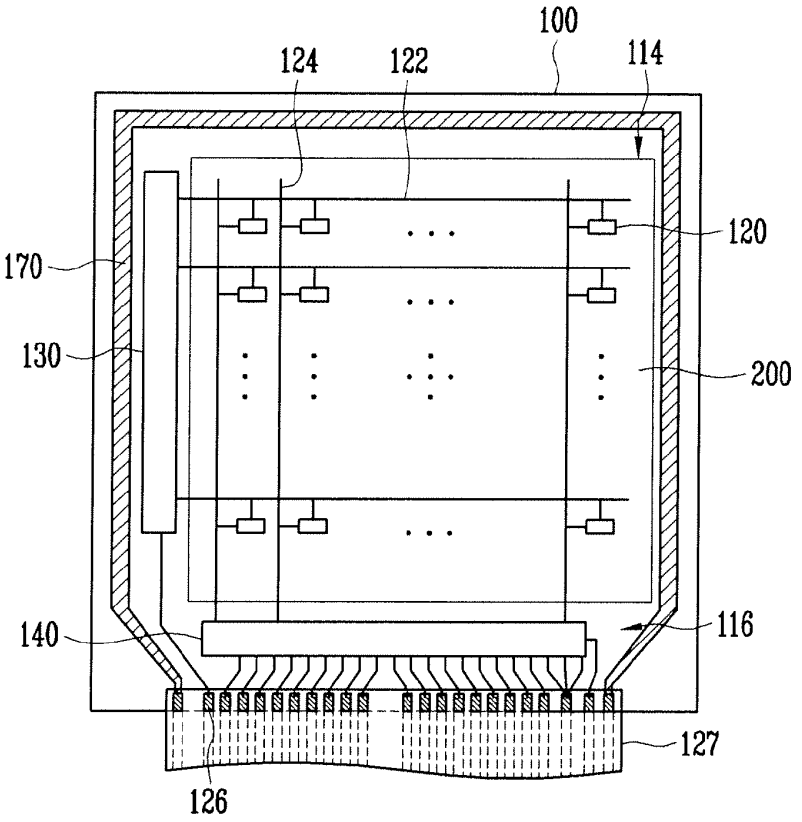
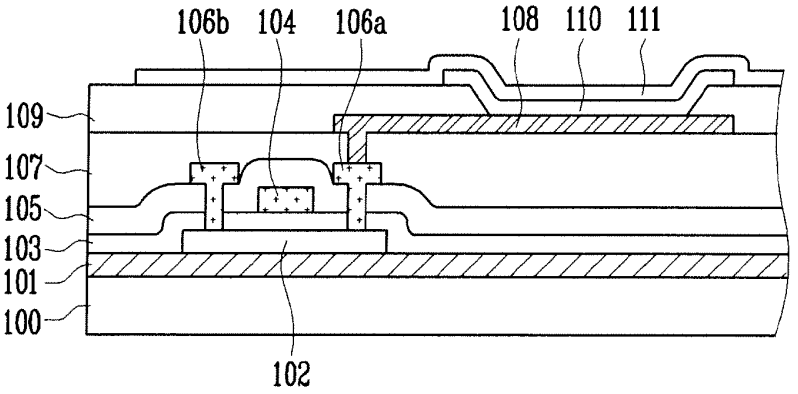



FIG. 5




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# FLAT PANEL DISPLAY DEVICE

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0001]** This application claims priority to and the benefit of Korean Patent Application No. 10-2006-0087396, filed on Sep. 11, 2006, in the Korean Intellectual Property Office, the entire content of which is incorporated herein by reference

## BACKGROUND OF THE INVENTION

**[0002]** 1. Field of the Invention

**[0003]** The present invention relates to a flat panel display device.

**[0004]** 2. Description of the Related Art

**[0005]** A liquid crystal display (LCD) having excellent color reproduction and low power consumption can be manufactured with low thickness. Further, an organic light emitting diode (OLED) display, considered as a next generation display device having a self light emitting property, has better properties in terms of field of view, contrast, response time, power consumption, etc., than those of LCDs, and can be manufactured with light weight and low thickness since it does not require a backlight.

**[0006]** In general, an LCD is composed of a liquid crystal display panel, a backlight positioned behind the liquid crystal display panel and used as a light source, and a driving circuit for driving the liquid crystal display panel.

**[0007]** A liquid crystal display panel includes two substrates arranged opposite to each other and a liquid crystal layer injected into the space between the two substrates, and pixels are defined by electrodes arranged in a matrix array on the two substrates.

**[0008]** The driving circuit converts electric signals provided from the outside into scanning signals and data signals to drive the respective pixels selectively. The driving circuit is arranged on the substrate during manufacturing of the elements, or manufactured as a driving circuit chip (i.e., a drive IC) to be mounted on the substrate via a tape automated bonding (TAB) or a chip on glass (COG) method. The electric signals are provided through a flexible printed circuit (FPC) in the form of film electrically coupled with a pad unit connected with the driving circuit.

**[0009]** However, since such flat panel display device is composed of glass substrates, electrostatic discharges (ESD) occur frequently during the manufacturing process or during the use of the flat panel display device. If an electrostatic discharge is applied to the liquid crystal layer or the driving circuit that operates at high speed with low voltage, such flat panel display device may malfunction or be damaged by electric influence. That is, if the externally occurring electrostatic discharge is applied to the driving circuit through the internal wiring, the operation of a driving voltage generation unit is suspended for an instant to generate vertical or horizontal lines and, furthermore, if the occurrence frequency of the electrostatic discharge or the applied voltage is increased, the circuit wiring may be disconnected or short-circuited, or insulation layer may be destroyed, thus causing a white defect. Such damages caused by the electrostatic discharge occur more seriously as the driving circuits become increasingly highly integrated (e.g., miniaturized).

**[0010]** FIG. **1** depicts a vertical line **2** defect of a conventional liquid crystal display panel **1**, in which such vertical lines **2** occur symmetrically with respect to a liquid crystal injection opening as the electrostatic discharge is applied through the liquid crystal injection opening sealed by a material having a relatively low resistance.

**[0011]** To prevent the damages caused by the electrostatic discharge, an element for discharging high voltages or a protection circuit was added to the display panel in the past, however, such element or protection circuit was designed primarily to prevent the electrostatic discharge occurring during the manufacturing process and was typically not helpful in preventing damages occurring during the use of the flat panel display device.

## SUMMARY OF THE INVENTION

**[0012]** An aspect according to an exemplary embodiment of the present invention is to provide a flat panel display device that can protect a driving circuit from electrostatic discharges (ESD).

**[0013]** Another aspect according to an exemplary embodiment of the present invention is to provide a flat panel display device that can prevent damages caused by an electrostatic discharge, without adding a separate element or a protection circuit for preventing the electrostatic discharge.

**[0014]** A flat panel display device in accordance with an aspect of an exemplary embodiment of the present invention includes: a first substrate having a first electrode and a shield wiring thereon; a second substrate facing the first substrate and having a second electrode thereon; a liquid crystal layer in a sealed space between the first substrate and the second substrate; and a driving circuit coupled with the first electrode and the second electrode through signal wirings, the shield wiring extending along an edge of the first substrate and electrically connected to a ground.

**[0015]** A flat panel display device in accordance with another aspect of an exemplary embodiment of the present invention includes: a first substrate having a shield wiring thereon; a second substrate facing the first substrate; light emitting diodes between the first substrate and the second substrate; and a driving circuit coupled with the light emitting diodes through signal wirings, the shield wiring extending along an edge of the first substrate and electrically connected to a ground.

**[0016]** A flat panel display device in accordance with another aspect of an exemplary embodiment of the present invention includes: first and second substrates facing each other and having a display region and a non-display region surrounding the display region; a plurality of pixels on the display region; a driving circuit for controlling display of images on the plurality of pixels, the driving circuit coupled to the plurality of pixels through a plurality of signal wirings; and a shield wiring at a non-display region and electrically coupled to a ground, the shield wiring extending along a periphery of the display region.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0017]** These and/or other features and aspects of the invention will become apparent and are more readily appreciated from the following description of exemplary embodiments, taken in conjunction with the accompanying drawings of which:

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**[0018]** FIG. **1** is a perspective view illustrating a display defect of a conventional liquid crystal display device caused by an electrostatic discharge;

**[0019]** FIG. **2** is a plan view illustrating a flat panel display device in accordance with a first exemplary embodiment of the present invention;

**[0020]** FIG. **3** is one exemplary schematic sectional view of the flat panel display device depicted in FIG. **2**;

**[0021]** FIG. **4** is a plan view illustrating a flat panel display device in accordance with a second exemplary embodiment of the present invention; and

**[0022]** FIG. **5** is one exemplary schematic sectional view of the flat panel display device depicted in FIG. **4**.

## DETAILED DESCRIPTION

**[0023]** The embodiments of the present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those having skill in the art.

**[0024]** FIG. **2** is a plan view illustrating a flat panel display device in accordance with a first exemplary embodiment of the present invention, and FIG. **3** is one exemplary sectional view, in which a flat panel display device is depicted schematically. The flat panel display device includes a display panel, including two substrates **10** and **40** and a liquid crystal layer **50** between the two substrates **10** and **40**, and a driving circuit **60** for driving the display panel.

**[0025]** A lower substrate **10** includes a pixel area **20** and a non-pixel area **30**. In the pixel area **20**, a plurality of segment electrodes is formed in case of a super twisted nematic liquid crystal display (STN-LCD), or a plurality of pixel electrodes and a plurality of thin film transistors (TFTs) for controlling the operations of the respective pixels are arranged in case of a thin film transistor-liquid crystal display (TFT-LCD).

**[0026]** The non-pixel area **30** includes a peripheral region of the pixel area **20**, e.g., an area outside of (or surrounding) the pixel area **20**, and includes wirings **12** and **14** coupled with electrodes **72**, **74** in the pixel area **20**, a driving circuit **60** coupled with the electrodes in the pixel area **20** through the wirings **12** and **14**, a shield wiring **70** arranged along the edge (or periphery), and a pad unit **16** coupled with the driving circuit **60** and the shield wiring **70**. The driving circuit **60** is arranged on the substrate while manufacturing the elements, or manufactured as a driving circuit chip (i.e., a drive IC) to be mounted on the substrate via a tape automated bonding (TAB) or chip on a glass (COG) method. In FIGS. **2** and **3**, reference numeral **12** denotes scan lines and reference numeral **14** denotes data lines.

**[0027]** An upper substrate **40** is made of transparent glass or any other suitable material, and includes a plurality of common electrodes arranged in the region opposite to (i.e., facing) the pixel area **20**.

**[0028]** The upper substrate **40** is arranged on the top of the lower substrate **10** so that the above-mentioned electrodes cross with each other. A sealed space is formed between the lower substrate **10** of the pixel area **20** and the upper substrate **40** using a sealing material **80** interposed between the lower and upper substrates **10** and **40**. Here, the common electrodes of the upper substrate **40** are electrically coupled with the wirings of the lower substrate **10**.

**[0029]** A plurality of pixels is defined by electrodes arranged in a matrix array on the lower and upper substrates **10** and **40**, and a liquid crystal layer **50** is injected into the sealed space between the substrates.

**[0030]** The pad unit **16** of the flat panel display device configured as above is electrically coupled with a flexible printed circuit (FPC) **65** in the form of film. Signals from the outside are provided to the flat panel display device through the pad unit **16**. The signals including power supply voltage, control signal, data, etc., are input to the pad unit **16** electrically connected with the driving circuit **60**, and the pad unit **16** coupled with the shield wiring **70** is electrically connected to ground.

**[0031]** When a signal is input to the driving circuit **60** in a state where the shield wiring **70** is connected to ground through the FPC **65**, the driving circuit **60** generates scanning signals and data signals to transmit the signals to the corresponding scan lines **12** and data lines **14**, respectively. Accordingly, light corresponding to the data signals is emitted by a liquid crystal array of pixels selected by the scanning signals.

**[0032]** The flat panel display device in accordance with an exemplary embodiment of the present invention includes the shield wiring **70** arranged along the edge (or periphery) of the lower substrate **10**. At least one side (or at least one end) of the shield wiring **70** is electrically connected to ground. In the described embodiment, the shield wiring **70** is formed to at least partly surround (e.g., formed along three of the four sides) the wirings **12** and **14** and the driving circuit **60**. The shield wiring **70** may be formed with a material that has a resistance value lower than those of the wirings **12** and **14** or the same material as the wirings **12** and **14**. In the described embodiment, the shield wiring **70** is formed wider than the wirings **12** and **14** so as to have a lower resistance value. By way of example, the shield wiring **70** may be formed of indium tin oxide (ITO), indium tin zinc oxide (ITZO), indium zinc oxide (IZO), potassium tin oxide (PTO), antimony tin oxide (ATO), antimony zinc oxide (AZO), $In_2O_3$, $SnO_2$, ZnO, CdO, $Cd_2SnO_4$, $Cd_2InO_4$, $In_4Sn_3O_{12}$, etc., and be fabricated at the same time as the wirings **12** and **14** during the manufacturing process or be made during a separate manufacturing process. In other embodiments, the shield wiring **70** may be formed with metals, such as molybdenum (Mo), tungsten (W), titanium (Ti), aluminum (Al), etc., or their alloys, or in a stacked structure including two or more of these metals and/or other suitable materials,

**[0033]** Accordingly, if an electrostatic discharge is applied to the surface or the side of the display panel, the electrostatic discharge is dissipated to the outside ground through the shield wiring **70** having a resistance value lower than those of the electrodes or the wirings **12** and **14**, thus substantially preventing the driving circuit from being damaged.

**[0034]** The flat panel display device manufactured in accordance with the first exemplary embodiment of the present invention was tested in contact and non-contact modes in full compliance with International Electrotechnical Commission (IEC) 1000-4-2 standard. The electrostatic discharges of ±8 kV were applied to the flat panel display device of the first exemplary embodiment of the present invention ten times in the contact mode and the electrostatic

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discharges of ±15 kV were applied ten times in the non-contact mode. During the test, no defect caused by the electrostatic discharges was found in the display panel or the driving circuit.

**[0035]** FIG. **4** is a plan view illustrating a flat panel display device in accordance with a second exemplary embodiment of the present invention, and FIG. **5** is a sectional view, in which an exemplary flat panel display device is depicted schematically. The flat panel display device includes a display panel, including two substrates **100** and **200**, organic light emitting diodes **120** located between the two substrates **100** and **200**, and driving circuits (or driving units) **130** and **140** for driving the display panel. While the elements **120** are being referred to as organic light emitting diodes in reference to FIG. **4**, the elements **120** in embodiments of the present invention (e.g., active matrix type display device) may be pixel circuits including organic light emitting diodes as well as other elements (e.g., TFTs) (see FIG. **5**, for example).

**[0036]** A lower substrate **100** is composed of a pixel area **114** and a non-pixel area **116**. In the pixel area **114**, scan lines **122** and data lines **124** are arranged to cross each other and the organic light emitting diodes **120** are located at crossing regions of the scan lines **122** and the data lines **124** in a matrix array to configure pixels.

**[0037]** The non-pixel area **116** is a peripheral region of the pixel area **114**, e.g., an area outside of (or surrounding) the pixel area **114**, and includes the scan lines **122**, the data lines **124**, that are extended from the scan lines **122** and the data lines **124** of the pixel area **114**, respectively, a power voltage supply line, which is not depicted in FIGS. **4** and **5**, a scan driving unit **130**, a data driving unit **140**, coupled to the scan lines **122** and the data lines **124**, respectively, a shield wiring **170** along the edge (or periphery), and a pad unit **126**, coupled with the scan driving unit **130** and the data driving unit **140**.

**[0038]** The scan driving unit **130** and the data driving unit **140** may be formed on the lower substrate **100** of the non-pixel area **116** during the process of manufacturing the organic light emitting diodes **120**, or manufactured as a driving circuit chip (i.e., a drive IC) and mounted on the substrate **100** to be coupled with the scan lines **122** and the data lines **124** via a tape automated bonding (TAB), a chip on glass (COG) or a wire bonding method.

**[0039]** In a passive matrix type display device, the organic light emitting diodes **120** are coupled between the scan lines **122** and the data lines **124** in a matrix array, whereas, in an active matrix type display device, the organic light emitting diodes **120** are connected between the scan lines **122** and data lines **124** in a matrix array, and thin film transistors (TFTs) for controlling the operations of the organic light emitting diodes **120** and capacitors for maintaining the signal are further included.

**[0040]** FIG. **5** is a sectional view for illustrating one of the organic light emitting diodes (or pixel circuits) **120** in more detail, in which an active matrix type OLED display is schematically depicted.

**[0041]** A buffer layer **101** is formed on the lower substrate **100**, and a semiconductor layer **102** providing an active layer is formed on the buffer layer **101**. The semiconductor layer **102** provides a source area, a drain area and a channel area for a thin film transistor. A gate insulating film **103** is formed on the overall top surface including the semiconductor layer **102**, and a gate electrode **104** is formed on the gate insulating film **103** on the top of the semiconductor layer **102**. An interlayer insulating film **105** is formed on the overall top surface including the gate electrode **104**, and contact holes are formed via the interlayer insulating film **105** and the gate insulating film **103** to expose specific parts of the semiconductor layer **102**. A source electrode **106***a* and a drain electrode **106***b* connected with the semiconductor layer **102** through the contact holes are provided on the interlayer insulating film **105**, and a planarization layer **107** is formed on the overall top surface including the source and drain electrodes **106***a* and **106***b*. A via hole is established via the planarization layer **107** to expose the source electrode **106***a* or the drain electrode **106***b*, and an anode electrode **108** coupled with the source electrode **106***a* or the drain electrode **106***b* through the via hole is provided on the planarization layer **107**. Moreover, a pixel defining film **109** for exposing the anode electrode **108** in the light emitting region is formed on the planarization layer **107**, and an organic thin film layer **110** and a cathode electrode **111** are provided on the exposed anode electrode **108**. The organic thin film layer **110** may be formed having a structure where a hole transfer layer, an organic emission layer and an electron transfer layer are stacked, in which a hole injection layer and an electron injection layer may be further included.

**[0042]** In the organic light emitting diode **120** configured as above, when suitable voltages (e.g., predetermined voltages) are applied to the anode electrode **108** and the cathode electrode **111**, holes injected from the anode electrode **108** and electrons injected from the cathode electrode **111** are coupled with each other in the organic thin film layer **110**, thus emitting light by the energy difference generated during the coupling process.

**[0043]** A sealed space is formed between the lower substrate **100** of the pixel area **114** and the upper substrate **200** using a sealing material, which is not depicted in FIGS. **4** and **5**, interposed between the lower substrate **100** and the upper substrate **200** facing the lower substrate **100**.

**[0044]** The pad unit **126** of the flat panel display device in accordance with an exemplary embodiment of the present invention is electrically coupled with a flexible printed circuit (FPC) **127** in the form of film, through which signals including power supply voltage, control signal, data, etc., are input from the outside. In one embodiment, the pad unit **126** (i.e., one of the contacts/terminals of the pad unit **126**) coupled with the shield wiring **170** is electrically connected to ground.

**[0045]** When signals are input to the scan driving unit **130** and the data driving unit **140** in a state where the shield wiring **170** is connected to ground through the FPC **127**, the scan driving unit **130** and the data driving unit **140** generate scanning signals and data signals to transmit the signals to the corresponding scan line **122** and data line **124**, respectively. Accordingly, light corresponding to the data signals are emitted by the organic light emitting diodes **120** selected by the scanning signals.

**[0046]** The flat panel display device in accordance with an exemplary embodiment of the present invention includes the shield wiring **170** arranged along the edge (or periphery) of the lower substrate **100** and at least one side (or at least one end) of the shield wiring **170** is connected to ground. Here, the shield wiring **170** is formed to at least partly surround (e.g., formed along three of the four sides) the scan lines **122**, the data lines **124**, the scan driving unit **130** and the data driving unit **140**. The shield wiring **170** may be formed with a material that has a resistance value lower than those of the scan line **122** and the data line **124** or the same material as the scan line **122** and the data line **124**. In the described embodiment, the shield wiring **170** is formed wider than the scan line **122** and the data line **124** so as to have a lower resistance value. For example, the shield wiring **170** may be

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formed with metals, such as molybdenum (Mo), tungsten (W), titanium (Ti), aluminum (Al), etc., or their alloys, or in a stacked structure including two or more of these metals and/or other suitable materials, and be fabricated at the same time as the scan lines **122** and the data lines **124** during the manufacturing process or be made during a separate manufacturing process.

**[0047]** Accordingly, if an electrostatic discharge is applied to the surface or the side of the display panel, the electrostatic discharge is dissipated to the outside ground through the shield wiring **170** having a resistance value lower than those of the scan line **122** and the data line **124**, thus substantially preventing the driving circuit from being damaged.

**[0048]** As described in detail above, the present invention forms the shield wiring along the edge (or periphery) of the substrate and connects at least one side (or at least one end) of the shield wiring to ground. Accordingly, the electrostatic discharge is dissipated to the outside ground through the shield wiring having a resistance value lower than those of the electrodes or the wirings, thus preventing the display panel and the driving circuit from being damaged, to improve the durability. Moreover, the present invention does not require an additional element or a protection circuit for preventing electrostatic discharges, thus reducing the manufacturing cost as well as the volume of the device. Further, while the embodiments of the present invention are described primarily in reference to LCD and/or OLED displays, the principles of the present invention can be applied to any other suitable display devices.

**[0049]** As above, exemplary embodiments of the present invention have been disclosed herein and, although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims and their equivalents.

What is claimed is:

**1**. A flat panel display device comprising:
a first substrate having a first electrode and a shield wiring thereon;
a second substrate facing the first substrate and having a second electrode thereon;
a liquid crystal layer in a sealed space between the first substrate and the second substrate; and
a driving circuit coupled with the first electrode and the second electrode through signal wirings,
the shield wiring extending along an edge of the first substrate and electrically connected to a ground.

**2**. The flat panel display device of claim **1**,
wherein the sealed space is formed by the first substrate, the second substrate and a sealing material between the first substrate and the second substrate.

**3**. The flat panel display device of claim **1**,
wherein the signal wirings and the driving circuit are on the first substrate.

**4**. The flat panel display device of claim **3**,
wherein the driving circuit is mounted on the first substrate using a chip on glass (COG) method.

**5**. The flat panel display device of claim **1**,
wherein the shield wiring is wider than the signal wirings.

**6**. The flat panel display device of claim **1**, further comprising a transistor connected between the first electrode and a corresponding one of the signal wirings.

**7**. The flat panel display device of claim **1**,
wherein at least one end of the shield wiring is electrically connected to an outside ground through a printed circuit.

**8**. The flat panel display device of claim **1**,
wherein signals are input from outside through an input terminal of the driving circuit.

**9**. The flat panel display device of claim **1**,
wherein the shield wiring at least partly surrounds the signal wirings and the driving circuit.

**10**. A flat panel display device comprising:
a first substrate having a shield wiring thereon;
a second substrate facing the first substrate;
light emitting diodes between the first substrate and the second substrate; and
a driving circuit coupled with the light emitting diodes through signal wirings,
the shield wiring extending along an edge of the first substrate and electrically connected to a ground.

**11**. The flat panel display device of claim **10**,
wherein the signal wirings and the driving circuit are on the first substrate.

**12**. The flat panel display device of claim **11**,
wherein the driving circuit is mounted on the first substrate using a chip on glass (COG) method.

**13**. The flat panel display device of claim **10**,
wherein the shield wiring is wider than the signal wirings.

**14**. The flat panel display device of claim **10**, further comprising transistors connected between the light emitting diodes and the signal wirings.

**15**. The flat panel display device of claim **10**,
wherein at least one end of the shield wiring is electrically connected to an outside ground through a printed circuit.

**16**. The flat panel display device of claim **10**,
wherein signals are input from outside through an input terminal of the driving circuit.

**17**. The flat panel display device of claim **10**,
wherein the shield wiring is formed to at least partly surround the signal wirings and the driving circuit.

**18**. A flat panel display device comprising:
first and second substrates facing each other and having a display region and a non-display region surrounding the display region;
a plurality of pixels on the display region;
a driving circuit for controlling display of images on the plurality of pixels, the driving circuit coupled to the plurality of pixels through a plurality of signal wirings; and
a shield wiring at a non-display region and electrically coupled to a ground, the shield wiring extending along a periphery of the display region.

**19**. The flat panel display device of claim **18**, wherein the shield wiring, the plurality of wirings and the driving circuit are on the first substrate, and the shield wiring at least partly surrounds the plurality of wirings and the driving circuit.

**20**. The flat panel display device of claim **18**, wherein the shield wiring is formed along the periphery of the display region at at least three of four sides of the display region.

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