

A Quick Intelligent Page-Programming Architecture and a Shielded Bitline Sensing Method for 3 V-Only NAND Flash Memory

Tomoharu Tanaka, Yoshiyuki Tanaka, Hiroshi Nakamura, Koji Sakui, *Member, IEEE*, Hideko Oodaira, Riichiro Shirota, Kazunori Ohuchi, Fujio Masuoka, *Senior Member, IEEE*, and Hisashi Hara, *Senior Member, IEEE*

Abstract— This paper describes a quick intelligent page-programming architecture with a newly introduced intelligent verify circuit for 3 V-only NAND flash memories. The new verify circuit, which is composed of only two transistors, results in a simple intelligent program algorithm for 3 V-only operation and a reduction of the program time to 56%. This paper also describes a shielded bitline sensing method to reduce a bitline-bitline capacitive coupling noise from 700 mV to 35 mV. The large 700 mV noise without the shielded bitline architecture is mainly caused by the NAND-type cell array structure. A 3 V-only experimental NAND flash memory, developed in a 0.7- μ m NAND flash memory process technology, demonstrates that the programmed threshold voltages are controlled between 0.4 V and 1.8 V by the new verify circuit. The shielded bitline sensing method realizes a 2.5- μ s random access time with a 2.7-V power supply. The page-programming is completed after the 40- μ s program and 2.8- μ s verify read cycle is iterated 4 times. The block-erasing time is 10 ms.

I. INTRODUCTION

FUTURE high-quality hand-held computers require low-cost and high-density flash memories instead of magnetic memories. Such flash memories must be operable with a 3 V-only power supply, because the computer industry moves toward the standard of a 3.0 V (or 3.3 V) power supply. A NAND flash memory, which has the advantage of a small cell size [1], [2] and a high reliability [3], [4], is expected to be one of these devices.

In the NAND flash memory, 256- or 512-byte memory cells are simultaneously programmed (page-programming). The threshold voltage of the programmed memory cell (program V_t) must be controlled between 0 V and the power supply voltage for a successful read operation [5]. If the memory cells are programmed with the same program time, the threshold voltages have a wide distribution resulting from the differences in the program characteristics of the memory cells. This wide program V_t distribution causes difficulties in operating the NAND flash memory with 3 V instead of 5 V. The program V_t distribution width must be narrowed down to 60% for 3 V-only operation.

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T. Tanaka, H. Nakamura, K. Sakui, H. Oodaira, R. Shirota, K. Ohuchi, F. Masuoka, and H. Hara are with the ULSI Research Center, Toshiba Corporation, Kawasaki, 210 Japan.

Y. Tanaka is with Toshiba Semiconductor System Engineering Center, Toshiba Corporation, Kawasaki, 210 Japan.
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To achieve this, an intelligent page-programming method was proposed [5]. By using this method, a tight program V_t distribution is realized, because the program time is optimized for each individual memory cell. Easy-to-program memory cells are effectively programmed with a short program time, and difficult-to-program ones are effectively programmed with a long-program time. As a result, the program V_t distribution width can be narrowed down to less than 50% [5]. This intelligent page-programming method is performed by iterating 5 procedures: (1) a read step to verify the program V_t (verify-read), (2) the comparison of the verify-read data with the program data, (3) the preparation of the re-program data to re-program only those memory cells which require more time to reach the programmed state, (4) the data re-load, and (5) the re-program.

However, this programming algorithm is very complicated, especially due to the procedures (2) and (3). In addition, the page-programming time is long, and the external microprocessor is very busy during the data programming of the NAND flash memory.

This paper describes a quick intelligent page-programming architecture with a new verify circuit, named "bit-by-bit verify circuit." The complicated procedures (2), (3), and (4) are simultaneously and automatically carried out on chip by the bit-by-bit verify circuit, which is composed of only two transistors. No external processor is required for these three procedures.

The other problem in 3 V-only NAND flash memories is a bitline-bitline capacitive coupling noise during the read operation.

An 8-b NAND-type cell array has only 1/16 contact holes per memory cell. Therefore, the capacitance ratio of the n^+ diffusion layer/p-well capacitance and the total bitline capacitance is small in comparison with a NOR-type flash memory. In other words, the bitline-bitline coupling ratio is large in the NAND flash memory. This large capacitive coupling ratio causes a large bitline-bitline capacitive coupling noise. As a result, a wide margin of bitline voltage difference between "H" and "L" level in the read operation is required, and it takes a long time to achieve the read operation. For example, the random access time is over 10- μ s in a 4-Mb NAND flash memory.

This paper describes a shielded bitline sensing method to eliminate the bitline-bitline capacitive coupling noise. More-

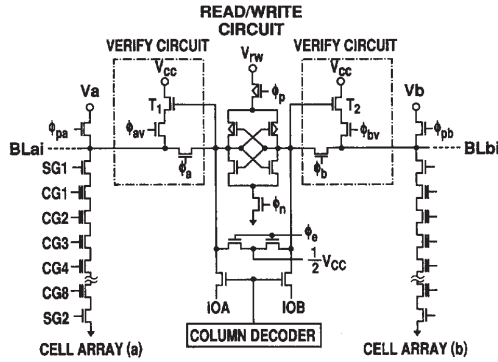


Fig. 1. Bit-by-bit verify circuit and READ/WRITE circuit for a 3 V-only NAND flash memory.

over, the bit-by-bit verify circuit and the shielded bitline sensing method are demonstrated with a 3 V-only experimental NAND flash memory developed in a 0.7- μm NAND flash memory process technology.

II. BIT-BY-BIT VERIFY CIRCUIT

A. Circuit Scheme

The NAND-structured cells are divided into two arrays (array (a) and array (b)), shown in Fig. 1 [6], by bit-by-bit verify (B^3V) circuits and READ/WRITE (R/W) circuits. A B^3V circuit is connected to each bitline. Two bitlines and B^3V circuits share a common R/W circuit like in an open-bitline architecture of a DRAM.

The R/W circuit acts as a flip-flop type differential sense amplifier in the read operation and as a data latch circuit in the program operation.

Fig. 2 shows the clock timing diagrams of each operation (program, read and verify-read) in the case that a control gate $CG4$ in array (a) is selected.

B. Program Operation

Initial program data are loaded by a page sequence and latched into the R/W circuits. The memory cells which share the same control gate are programmed simultaneously.

For “0”-programming, the bitlines are charged up to 8 V with the power supply voltage V_{rw} of the R/W circuits which is pumped up to 8 V from the external power supply V_{cc} . For “1”-programming, the bitlines are held to be grounded. The program is accomplished by applying 20 V to the selected control gate ($CG4$) while 10 V is applied to the unselected control gates ($CG1-3, 5-8$), as shown in Fig. 2(a).

In “1”-programming, electrons are injected to the floating gate from the inversion layer by Fowler-Nordheim tunneling, and the threshold voltage V_t of the memory cell changes from negative of the erased state to positive [5]. In “0”-programming, the memory cell is kept at the same state as before the program operation, because the voltage over the

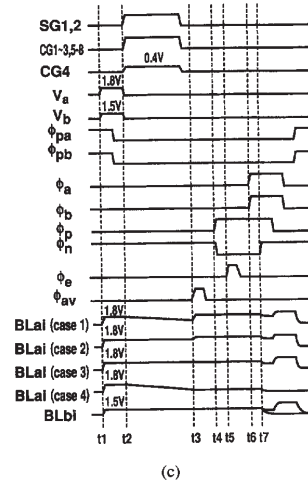
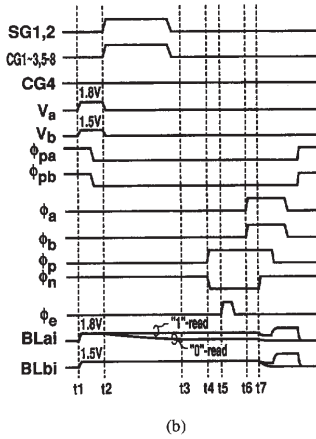
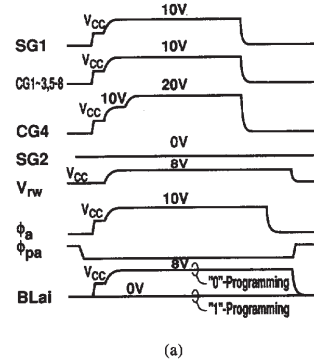


Fig. 2. Clock timing diagrams. (a) Program. (b) Read. (c) Verify-read.

tunnel oxide under the floating gate is too low to cause a tunnel current [5].

TABLE I
DATA MODIFICATION RULE

PROGRAM DATA (LATCHED DATA)	0	0	1	1
CELL DATA	0	1	0	1
RE-PROGRAM DATA (RE-LATCHED DATA)	0	0	1	0

C. Read Operation

The selected bitlines (BL_{ai}) are pre-charged to $3/5 V_{cc}$ and the dummy bitlines (BL_{bi}) are pre-charged to $1/2 V_{cc}$ at times $= t_1$ in Fig. 2(b). After pre-charging, the unselected control gates ($CG1-3$, $5-8$) are raised to V_{cc} while the selected control gate ($CG4$) is grounded (t_2).

If the V_t of the selected memory cell is smaller than $0 V$, a cell read current flows and the selected bitline voltage decreases below $1/2 V_{cc}$ ("0"-read). On the other hand, if the V_t is larger than $0 V$, no cell read current flows and the bitline voltage is kept at $3/5 V_{cc}$ ("1"-read) (t_3).

After all control gates turn low, the R/W circuits are reset (t_4) and equalized (t_5), and the bitlines are connected to the R/W circuits by turning the clock ϕ_a and ϕ_b to high (t_6). The voltages of the bitlines are sensed by the open-bitline differential sensing manner (t_7).

The read-out of the sensed data is done by a page mode sequence.

D. Verify-Read Operation

After the program operation, a verify-read operation is performed to detect the memory cells which require more time to reach the "1"-programmed state. In the verify-read operation, the program data latched in the R/W circuit is modified to the re-program data, according to the data modification rule shown in Table I. As a result, a reprogram operation is performed only on the memory cells which did not reach the "1"-programmed state. Thereby, the program time is optimized bit-by-bit.

The verify-read operation is similar to the read operation except that the selected control gate ($CG4$) is raised to the verify-voltage $0.4 V$ at t_2 in Fig. 2(c) and the B^3V circuits and enabled by turning the clock ϕ_{av} to high (t_3). The R/W circuits act as program data latch circuits until t_4 , and as sense amplifiers after t_4 . The sensed data are latched as the re-program data.

In the case that the R/W circuit latches the program data "0," the state of the transistor $T1$ in the B^3V circuit is "ON." The bitline after "0"-programming is re-charged over $1/2 V_{cc}$ by the B^3V circuit (t_3). Therefore, the latched reprogram data is "0" independent of the memory cell data (case 1, 2).

In the case that the R/W circuit latches the program data "1," the state of the transistor $T1$ is "OFF." So, the bitlines are not re-charged by the B^3V circuits even if the clock ϕ_{av} turns high. If the memory cell has been successfully programmed "1," the bitline voltage after "1"-programming is over $1/2$

TABLE II
DEVICE PARAMETERS

Technology	0.7 μ m Lithography N-sub Double-well CMOS Triple-Polysilicon Single-Aluminum		
Memory Cell	Cell Size	16.1 μ m $\times$ 2.4 μ m / 8bit	
	Tunnel Oxide	10nm	
	Inter-Poly ONO	25nm	
	Program Time	200 μ sec/Page	
	Erase Time	10msec/Block	
Periphery	Gate Length	1.2 μ m(4.0 μ m:High Voltage)	
	Gate Oxide	25nm(50nm:High Voltage)	
Device	Chip size	5.13mm $\times$ 7.41mm	
	Organization	64byte $\times$ 8b $\times$ 16page $\times$ 256block	
	Stand-by Power	1 μ A	
	Active Power	25mW	
	Random access	2.5 μ sec	
	Page access	100nsec	

V_{cc} . On the other hand, if the memory cell does not reach the "1"-programmed state, the bitline voltage decreases below $1/2 V_{cc}$. The latched re-program data is "0" for the memory cell which is in the "1"-programmed state (case 3). The re-program data is "1" for the memory cell which did not reach the "1"-programmed state yet (case 4).

By using the B^3V circuit, the program data is automatically and simultaneously modified to the re-program data according to Table I.

III. QUICK INTELLIGENT PAGE-PROGRAMMING ALGORITHM

Fig. 3(a) shows a new quick page-programming algorithm. At first, the initial program starts. The data load sequence is done by page mode. After the initial program, the first verify-read is performed. If the verify-read data is all "1," the program operation is completed. Otherwise, the reprogram and the verify-read are repeated until the verify-read data becomes all "1." The verify-read data of all "1" indicates that there is no memory cell which requires more time to reach the "1"-programmed state, because it indicates that the re-program data is all "0."

The new quick algorithm has no complicated modify-operation and no data re-load compared with a conventional one [5] shown in Fig. 3(b). So, utilizing the quick algorithm, the total page-programming time is significantly reduced.

Under the condition that: 1) the page size is 512 bytes, 2) the page access time is 100 ns, 3) the random access time is 2.5 μ s, 4) the programming pulse width is 40 μ s, 5) the number of verify-read and re-program cycles is 5, and 6) the operating frequency of the external processor unit is 25 MHz; by the conventional algorithm, the total program time is

$$\begin{aligned}
 & \text{VERIFY-READ} && \text{DATA MODIFICATION} \\
 & ((2.5 \mu\text{s} + 511 \text{ byte} \times 100 \text{ ns}) &+& (512 \text{ byte} \times 40 \text{ ns}) \\
 & \text{DATA RE-LOAD} && \text{PROGRAMMING} \\
 & + (512 \text{ byte} \times 100 \text{ ns}) &+& 40 \mu\text{s}) \times 5 = 826.4 \mu\text{s}.
 \end{aligned}$$

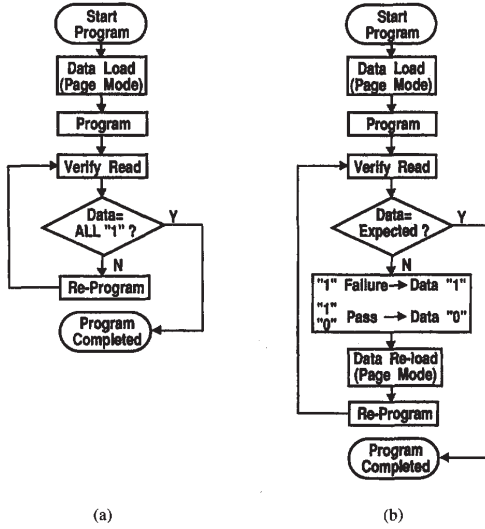


Fig. 3. Page-programming algorithm. (a) Quick algorithm. (b) Conventional algorithm.

By the quick algorithm,

$$\begin{aligned} & \text{VERIFY-READ} \quad \text{PROGRAMMING} \\ & ((2.5 \mu\text{s} + 511 \text{ byte} \times 100 \text{ ns}) + 40 \mu\text{s}) \times 5 = 468.0 \mu\text{s}. \end{aligned}$$

Thus, the total page-programming time by the quick algorithm can be reduced to 56% of that by the conventional one. Moreover, no external processor is needed for the data modification and the data re-load.

IV. SHIELDED BITLINE ARCHITECTURE

As the integration density of the NAND flash memory has increased, the bitline-bitline (*BL-BL*) coupling noise has become a serious problem during the read operation. The coupling noise is increased as the bitline pitch becomes smaller. In this section, the *BL-BL* coupling noise will be investigated, and subsequently a new bitline architecture to reduce this noise will be proposed.

A. Bitline-Bitline Coupling Noise

The 8-b NAND-type cell array structure is illustrated in Fig. 4. The cell array is formed on a p-well in an n-substrate. The first polysilicon layer is used for the floating gates while the second polysilicon is used for the control gates. A 10-nm tunnel oxide is used and the thickness of the interpoly ONO layer is 25 nm. The third polysilicon layer is used for the source lines and wiring of the row decoder circuits. The bitlines are formed by aluminum and n^+ diffusion layers.

A simplified model for the coupling noise is shown in Fig. 5(a). Where a capacitance $C1$ is defined as the coupling capacitance to the adjacent bitline, and $C2$ is defined as the bitline capacitance excluding $2 \times C1$. The capacitance $C2$ consists of the capacitances between the bitline and the p-well, select gates, control gates, and the third polysilicon wiring. In

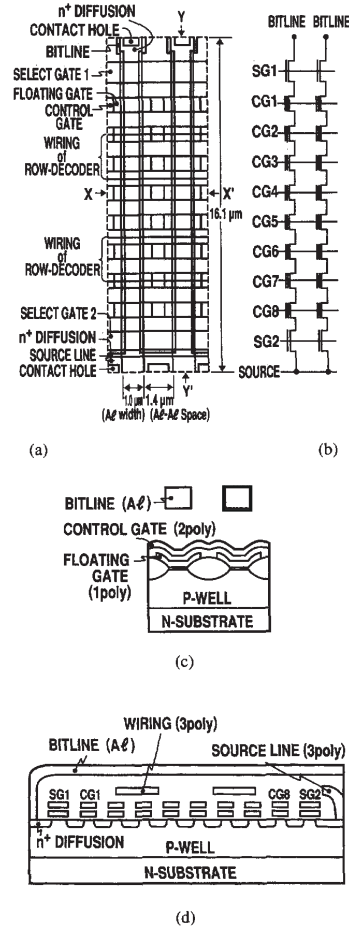


Fig. 4. 8-b NAND-type cell array structure. (a) Layout. (b) Equivalent circuit. (c) $X-X'$ cross sectional view. (d) $Y-Y'$ cross sectional view.

the NAND-types cell array, the capacitance between the bitline and the p-well is small, because only 1/16 contact hole per memory cell is used. The measured capacitances $C1$ and $C2$ of the cell array shown in Fig. 4 are, respectively, 300 fF and 950 fF. The bitline length is $1.6 \mu\text{m} \times 130$ NAND-type cells.

In the read operation, the coupling noise ΔV_{BL} is generated in the bitline $BL1$ when the select gates and the control gates are activated and a signal voltage appears in the adjacent bitlines $BL0$ and $BL2$. Fig. 5 represents the worst case in which "1"-data appears on the concerned bitline $BL1$ and "0"-data on the neighboring bitlines $BL0$ and $BL2$.

The bitline $BL1$ voltage should stay at the pre-charged voltage of 1.8 V. However, the bitline $BL1$ voltage is decreased through the *BL-BL* capacitive coupling as the voltages of both neighboring bitlines $BL0$ and $BL2$ decreased from 1.8 V to 0 V. The maximum coupling noise ΔV_{BL} is

$$\Delta V_{BL} = 1.8 \text{ V} \times (2 \times C1 / (2 \times C1 + C2)).$$

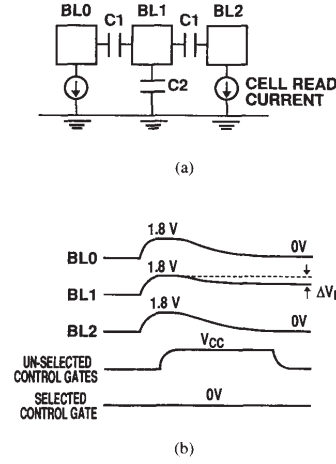


Fig. 5. The maximum bitline-bitline capacitive coupling noise. (a) Simplified model of unshielded bitline. (b) Bitline waveforms in read operation.

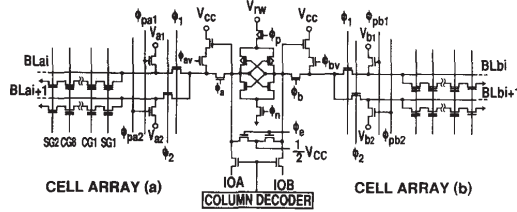


Fig. 6. Shielded bitline architecture.

Under the condition that $C1 = 300$ fF and $C2 = 950$ fF, the noise ΔV_{BL} is 697 mV.

In the read operation, the pre-charged voltage difference between the selected bitline and the dummy bitline must be larger than this coupling noise. Therefore, the large noise causes a malfunction of the device, or results in a long read access time.

B. Shielded Bitline Architecture

In order to reduce the BL - BL capacitive coupling noise, the shielded bitline architecture is proposed. Fig. 6 illustrates the circuit configuration of the shielded bitline architecture. Four bitlines (BL_{ai} , BL_{ai+1} , BL_{bi} , BL_{bi+1}) share the common R/W circuit. In a read operation, the bitlines are alternately selected, and the unselected bitlines are grounded. If BL_{ai} is selected, BL_{bi} becomes the dummy bitline while BL_{ai+1} and BL_{bi+1} are grounded. In this case, the clocks ϕ_1 , ϕ_{pa2} and ϕ_{pb2} are activated and the voltages V_{a2} and V_{b2} are 0 V.

Fig. 7 shows a simplified model to estimate the BL - BL coupling noise in the case of the shielded bitline. A capacitance $C3$ is defined as a BL - BL coupling capacitance between a bitline and its second nearest bitline. The maximum coupling

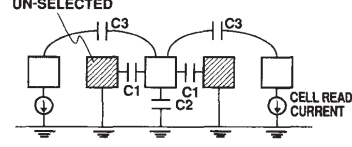


Fig. 7. Simplified model of shielded bitline.

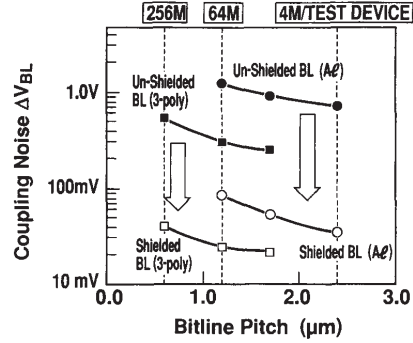


Fig. 8. Calculated bitline-bitline coupling noise in read operation.

noise becomes

$$\Delta V_{BL} = 1.8 \text{ V} \times (2 \times C3 / (2 \times C3 + 2 \times C1 + C2)).$$

The measured capacitance $C3$ is 15 fF, so that the noise ΔV_{BL} decreases drastically down to 5%, from 700 mV to 35 mV.

In a program operation, unselected bitlines are raised to 8 V to prevent "1"-programming. If BL_{ai} is selected, BL_{ai+1} is raised to 8 V while BL_{bi} and BL_{bi+1} are grounded.

C. Bitline-Bitline Coupling Noise Evaluation

The BL - BL coupling noise in a read operation was calculated as a function of the bitline pitch with two types of bitline materials in Fig. 8. In a 4-Mb NAND flash memory, having an aluminum bitline pitch of $2.4 \mu\text{m}$, the coupling noise ΔB_{BL} becomes 700 mV. This noise causes over $-10 \mu\text{s}$ random access time in the 4-Mb device. With the shielded bitline architecture, the coupling noise is greatly suppressed by a factor 20, and the noise is reduced to only 35 mV.

In the case of the third polysilicon bitline, the thickness of the bitlines can be decreased to lower the BL - BL coupling noise. Even in a 256-Mb device and beyond, where the bitline pitch is less than $0.6 \mu\text{m}$, the noise is suppressed below 100 mV by adopting the third polysilicon shielded bitline architecture.

The effect of this noise suppression and a stable operation of the NAND flash memory is demonstrated with a 3 V-only test device described in the next section.

V. 3 V-ONLY NAND FLASH MEMORY

To verify the performance of the bit-by-bit verify circuit and the shielded bitline architecture, an experimental 3 V-only 2

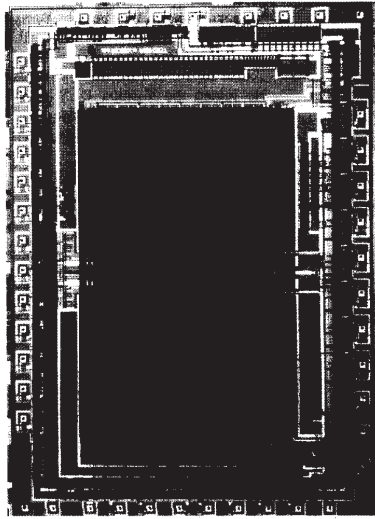
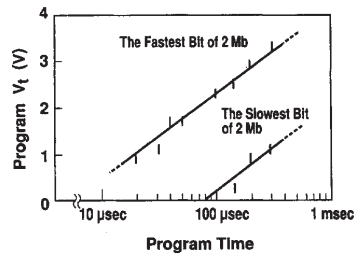


Fig. 9. Microphotograph of 3 V-only test device.

Fig. 10. 2-Mb array program characteristics without verify ($V_{cc} = 3$ V).

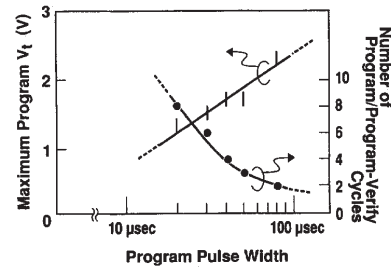
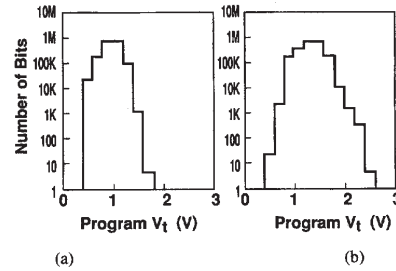
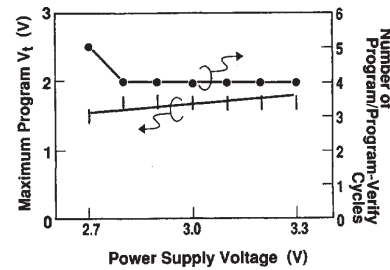
Mb NAND flash memory was designed and evaluated. The memory cell structure and the circuit diagram are shown in Fig. 4 and 6.

A microphotograph of this device is shown in Fig. 9. The memory array is divided into 2 arrays of 1024 rows $\times$ 1024 columns by the R/W circuits. The page and block size are 64 bytes and 1 K bytes, respectively. The die size is 5.13 mm $\times$ 7.41 mm, and the area of the bit-by-bit verify circuits occupies 0.76% of the die. The increased die size for the controllers for the bit-by-bit verify circuits and the shielded bitline sensing is 1.5% of the die. The device parameters are represented in Table II.

A. Program Characteristics

The 2-Mb array program characteristics without verify-read operation are shown in Fig. 10. It takes about 150 μ s to raise the V_t of the slowest bit to the verify voltage of 0.4 V, under that condition, the V_t of the fastest bit is larger than 2.6 V.

The 2-Mb array program characteristics with the bit-by-bit verify-read operation are shown in Fig. 11. If the program operation is performed with 40- μ s pulses, it takes 4 cycles to complete the page-programming and the maximum program

Fig. 11. 2-Mb array program characteristics with bit-by-bit verify ($V_{cc} = 3$ V).Fig. 12. Difference of program V_t distribution. (a) With bit-by-bit verify ($V_{cc} = 3$ V, Program Pulse Width = 40 μ s). (b) Without verify ($V_{cc} = 3$ V, Program Time = 160 μ s).Fig. 13. Program characteristics versus power supply voltage (Program Pulse Width = 40 μ s).

V_t is reduced to less than 1.8 V. Fig. 12 illustrates the difference in the program V_t distribution and shows that the maximum program V_t is successfully lowered from 2.6 V to 1.8 V by the bit-by-bit verify circuits.

The number of program/verify-read cycles versus V_{cc} is shown in Fig. 13. At $V_{cc} = 2.7$ V, the page-programming is completed after 5 cycles. The program time dependence on V_{cc} results from a fluctuation of the program voltage, because the charge pump circuit, which generates the program voltage, is not able to generate the maximum program voltage if V_{cc} becomes lower.

B. Read Characteristics

A schmo plot of the random access time versus V_{cc} is shown in Fig. 14. For this test, one of the 8 memory cells

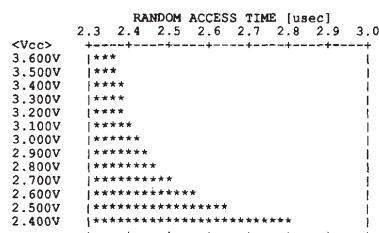


Fig. 14. Random access schmo plot.

which compose a NAND-structured cell is programmed "0," and the other 7 memory cells are programmed "1." Such data pattern yields the minimum cell read current. By utilizing the shielded bitline architecture, the internal noise, which has an adverse effect on the read operation, is minimized, and a stable read operation over a wide range of V_{cc} is achieved. The random access time is 2.5 μ s at $V_{cc} \approx 2.7$ V.

VI. CONCLUSION

A 2-Mb NAND flash memory has been successfully developed for operation with a 3 V-only power supply.

Using a newly developed bit-by-bit verify circuit, the program V_t distribution is controlled between 0.4 V and 1.8 V, and the total program time is reduced to 56%. Moreover, no external processor is required for the complicated procedures in the intelligent page-programming algorithm. By utilizing a shielded open-bitline differential sensing method, a random access time of 2.5 μ s is achieved at $V_{cc} = 2.7$ V.

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Tomoharu Tanaka was born in Yamaguchi, Japan, on July 8, 1962. He received the B.E. and M.E. degrees in applied physics from the University of Tsukuba, Japan, in 1985 and 1987, respectively.

He joined the Toshiba ULSI Research Center, Kawasaki, Japan, in 1987. Since then, he has been working on the circuit design of high-density EEPROM's.



Yoshiyuki Tanaka was born in Tokyo, Japan, on August 22, 1963. He received the B.E. and M.E. degrees in instrumental engineering from Keio University, Japan, in 1986 and 1988, respectively.

He joined the Toshiba ULSI Research Center, Kawasaki, Japan, in 1988. Since then he has been working on the circuit design of high-density EEPROM's. He is now with the Toshiba Semiconductor System Engineering Center, Kawasaki, Japan.

Mr. Tanaka is a member of the Japan Society of Applied Physics.



Hiroshi Nakamura was born in Yamaguchi, Japan, on August 16, 1965. He received the B.E. and M.E. degrees in electronic engineering from Osaka University, Japan, in 1988 and 1990, respectively.

He joined the Toshiba ULSI Research Center, Kawasaki, Japan, in 1990. Since then he has been working on the circuit design of high-density EEPROM's.



Koji Sakui (M'92) was born in Tokyo, Japan, on April 29, 1956. He received the B.E. and M.E. degrees in instrumental engineering from Keio University, Japan, in 1979 and 1981, respectively.

He joined the Toshiba ULSI Research Center, Kawasaki, Japan, in 1981. Since then he has been engaged in the development of high-density DRAM's and EEPROM's. From 1991 to 1993, he was a Visiting Scholar at Stanford University, Stanford, CA, doing research in the field of Multi-Chip Module and BiCMOS technologies.



Hideko Oodaira was born in Aomori, Japan, on December 31, 1967. She graduated from Hirosaki Technical High School, Japan, in 1986.

She joined the Toshiba ULSI Research Center, Kawasaki, Japan, in 1986. Since then, she has been working on the circuit design of high-density EEPROM's.



Riichiro Shirota was born in Hyogo, Japan, on February 22, 1954. He received the B.E., M.E., and Ph.D. degrees in physics from Nagoya University, in 1977, 1979, and 1982, respectively.

In 1982, he joined the Toshiba ULSI Research Center, Kawasaki, Japan. Since then, he has been engaged in the research and development of EEPROM's.



Kazunori Ohuchi was born in Tochigi, Japan, on June 7, 1947. He received the B.E. degree in electronic engineering from Tohoku University, Japan, in 1970.

In 1970, he joined the Toshiba Research and Development Center, Kawasaki, Japan. Since then, he has been working on the circuit and device design of MOS memories, including EEPROM's, static RAM's, and dynamic RAM's. His current interests are in advanced device structures and circuits for high-density DRAM's and EEPROM's.

Mr. Ohuchi is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Fujio Masuoka (A'88-SM'94) was born in Takasaki, Japan, on May 8, 1943. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Tohoku University, Japan, in 1966, 1968, and 1971, respectively.

In 1971, he joined the Toshiba Research and Development Center, Kawasaki, Japan, where he has been working on MOS LSI memories. He is currently managing the device research department at the Toshiba ULSI Research Center. His research interests have been in new memory cells such as EEPROM, MROM, SRAM, and DRAM.

Dr. Masuoka received the Watanabe Award and the National Invention Award in 1977 and 1978, respectively.



Hisashi Hara (SM'94) was born in Tosashimizu, Japan, on May 8, 1938. He received the B.S. degree in electrical engineering from Yokohama University in 1962, and the M.S. and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1964 and 1978.

He joined Toshiba Corporation in 1964. From 1965 to 1969, he was engaged in the development of PMOS IC's for the calculator. From 1970 to 1973, his research interest was focused on MOSFET physics, such as mobility and breakdown phenomena, which led to avalanche injection MOS devices. From 1974 to 1981, he was engaged in the development of new NMOS LSI's, such as 8-, 12-, and 16-b microprocessors and many memories (DRAM, SRAM, and EPROM). From 1982 to 1987, he was engaged in the development of the ASIC CAD system. Recently, his main research interest was on short-channel MOS device physics and new memories.

Dr. Hara is a member of the Institute of Electronics and Communication Engineers of Japan.