IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

MOSAID TECHNOLOGIES INC., *Plaintiff*, v. INFINEON TECHNOLOGIES AG and INFINEON TECHNOLOGIES AMERICAS CORP., *Defendants*.	Civil No. 1:25-cv-00436 **JURY TRIAL DEMANDED**

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff MOSAID Technologies Inc. ("Plaintiff" or "MOSAID") files this Complaint for Patent Infringement against Defendants Infineon Technologies AG ("Infineon AG") and Infineon Technologies Americas Corp. ("Infineon Americas") (collectively, "Defendants" or "Infineon") alleging as follows:

NATURE OF SUIT

1. This is a claim for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code.

PARTIES, JURISDICTION, AND VENUE

2. This action arises under the patent laws of the United States, 35 U.S.C. § 101, *et seq.* This Court has jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

I. MOSAID

3. MOSAID (f/k/a Conversant Intellectual Property Management, Inc.) is a Canadian company having a principal place of business at 515 Legget Drive, Suite 100, Ottawa, ON, Canada.

INFINEON-1010

4. MOSAID was founded in 1975 by engineers Richard Foss and Robert Harland. MOSAID focused its early efforts on inventing ways to improve Dynamic Random Access Memory (DRAM) semiconductor chips. MOSAID's engineers also designed and built test equipment for debugging prototype memory chips.

5. MOSAID is now a leading patent management company with a world-class licensing team and an enviable record of success. MOSAID's success is defined by the numerous licenses it has signed with industry leaders. MOSAID prides itself on its patent expertise, a determination to engage in meaningful negotiation, and a commitment to transparency and the principled enforcement of high-quality patents.

6. MOSAID owns approximately 800 active patents as of February 2025. A large portion of the portfolio was developed in-house from research and development efforts focusing on flash memory technologies. MOSAID's microcomponents patents also include marquee patents relating to power management, based on various inventions derived from MOSAID's own R&D and product development businesses.

7. MOSAID is the assignee and owns all right, title, and interest to United States Patent No. 7,685,393 ("the '393 Patent"), United States Patent No. 9,972,381 ("the '381 Patent"), and United States Patent No. 10,140,028 ("the '028 Patent"). The '393 Patent, '381 Patent, and '028 Patent are collectively referred to herein as the "Asserted Patents."

II. INFINEON

8. Defendant Infineon Technologies AG ("Infineon AG") is a corporation organized and existing under the laws of the Federal Republic of Germany, and is located at Am Campeon 1-15, 85579 Neubiberg, Germany.

9. Infineon AG is listed on the Frankfurt Stock Exchange (ticker symbol: IFX) and in the USA on the over-the-counter market OTCQX International Premier (ticker symbol: IFNNY).

10. On information and belief, with a global presence, Infineon AG operates through its subsidiaries in the U.S.

11. Defendant Infineon Technologies Americas Corp. ("Infineon Americas") is a corporation duly organized and existing under the laws of the state of Delaware and may be served with process through its Texas registered agent, Corporation Service Company d/b/a CSC – Lawyers Incorporating Service Company, 211 E. 7th Street, Suite 620, Austin, Texas 78701. Infineon Americas has a regular and established place of business in the Western District of Texas, including at 5204 E. Ben White Blvd, Austin, Texas 78741. On information and belief, Infineon Americas also maintains other offices in the State of Texas, including in Houston, Texas.

12. On information and belief, Infineon Americas is a wholly owned subsidiary of Infineon AG.

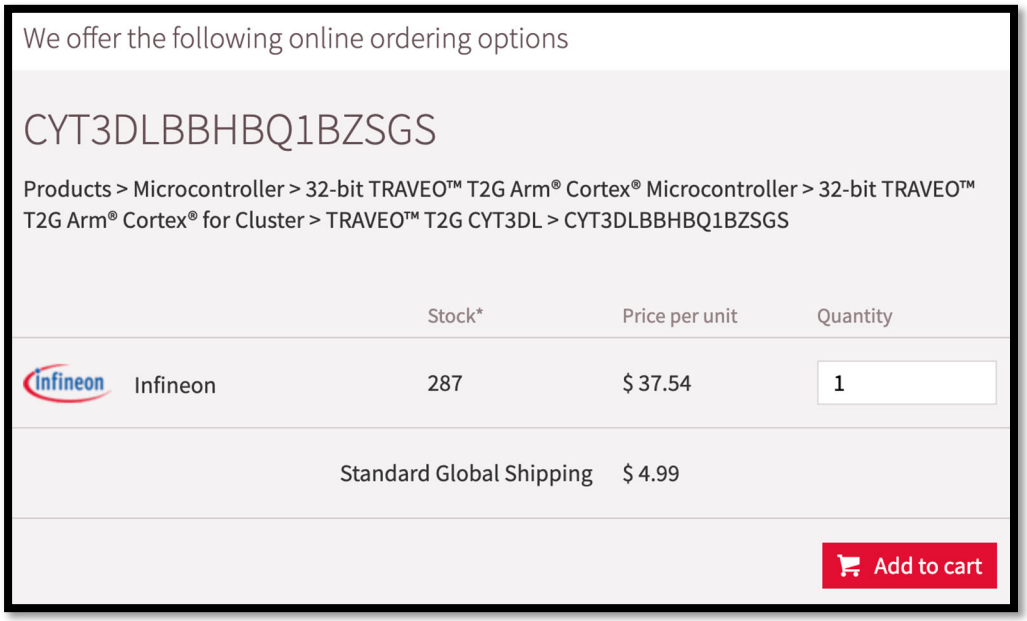
13. Cypress Semiconductor Corporation ("Cypress") was an American semiconductor design and manufacturing company offering products such as NOR flash memories, F-RAM and SRAM Traveo microcontrollers, PSoCs, and others. On or around April 16, 2020, Infineon AG acquired 100% ownership of Cypress. On information and belief, at the time of the acquisition, Cypress was registered to do business in Texas, was transacting business in Texas and in this District, and maintained a regular and established place of business in this District at 5204 E. Ben White Blvd, Austin, Texas 78741. On information and belief, at least Infineon Americas took over Cypress's operations at 5204 E. Ben White Blvd, Austin, Texas 78741 following Infineon AG's acquisition of Cypress.

14. On information and belief, each Defendant, Infineon AG and Infineon Americas (collectively, "Infineon"), is a semiconductor company that designs, develops, makes, uses, offers for sale, sells in the United States, and/or imports into the United States, a variety of semiconductor

products for the communications, Internet of Things ("IoT"), automotive, computer, and/or consumer electronics industries.

15. On information and belief, Infineon designs, develops, makes, uses, offers for sale, sells in the United States, and/or imports into the United States, certain processor products such as microcontrollers including at least the TRAVEO T2G series, among other substantially similar processor products (hereinafter, the "Accused Processor Products"), and flash memory products including at least the Serial NOR Flash, HYPERFLASH, and SEMPER Flash families, among other substantially similar memory products (hereinafter, the "Accused Memory Products") that utilize the inventions of the Asserted Patents (collectively, the "Accused Products").

16. On information and belief, Infineon offers for sale and sells its products, including the Accused Products, directly to consumers in the United States, including in this District. For example, Infineon AG offers for sale and sells its products, including the Accused Products, in the United States via its website https://www.infineon.com:



(Exemplary TRAVEO T2G product available for purchase on Infineon's website.)

We offer the following online ordering options

S26KS512SDPBHB020

Products > Memories > NOR flash > Serial NOR flash > HYPERFLASH™ > S26KS512SDPBHB020

	Stock*	Price per unit	Quantity
Infineon	1628	$ 14.81	1
Standard Global Shipping		$ 4.99	

Add to cart

(Exemplary HYPERFLASH product available for purchase on Infineon's website.)

We offer the following online ordering options

S28HS512TGABHM010

Products > Memories > NOR flash > SEMPER™ NOR flash family > SEMPER™ NOR flash > S28HS512TGABHM010

	Stock*	Price per unit	Quantity
Infineon	219	$ 17.68	1
Standard Global Shipping		$ 4.99	

Add to cart

(Exemplary SEMPER Flash product available for purchase on Infineon's website.)

17. Infineon AG operates https://www.infineon.com, as stated in the website's footer and linked Terms of Use:

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› Usage of this website is subject to our Usage Terms

› Imprint › Contact › Privacy Policy › Glossary

(https://www.infineon.com.)

Terms of Use

1. Scope
Any use of this web site provided by Infineon Technologies AG (hereinafter "Infineon") under the URL › **http://www.infineon.de** and/or › **http://www.infineon.com** (hereinafter "Web Site") is subject to these Terms of Use.

(https://www.infineon.com/cms/en/about-infineon/usage-terms.)

18. Infineon AG is also the Registrant Contact in the domain registration record for https://www.infineon.com.

19. Infineon also sells its Accused Products in the United States through Infineon Distribution Partners, including eCommerce Partners, Franchised Distributors, and Specialty Distributors.

20. On information and belief, Infineon sells its Accused Products to numerous companies in the United States, including companies in this District, for use in consumer end products. For example, Infineon's NOR Flash memory products are used in Tesla vehicles, including at least the display system for the Tesla Model Y, which are manufactured in Austin, Texas at Tesla, Inc.'s global headquarters.

21. On information and belief, Infineon AG has substantial connections to the State of Texas. For example, Infineon AG has partnered with Texas companies to provide products to

customers in the United States, including in this District. For example, in 2023, Infineon AG announced its partnership with Spark Connected to provide a 500W wireless charging solution named Yeti. On information and belief, Spark Connected is a company organized under the laws of Texas and headquartered in Dallas, Texas. The Yeti 500W is a ready-to-integrate wireless charging module intended for the powering and charging of industrial machinery, autonomous mobile robots, automated guided vehicles, light electric vehicles, e-Mobility and other power-intensive applications. The module integrates at least Infineon's dual-core PSoC 63 Bluetooth Low Energy MCU, a microcontroller unit within Infineon's PSoC 6 product family.

22. In addition, on information and belief, Infineon AG has been collaborating with Siemens Industry Software Inc. (d/b/a Siemens Digital Industries Software) since at least November 19, 2024, to integrate Siemens' automotive embedded software platform with Infineon's AURIX microcontroller. Siemens Digital Industries Software is headquartered in Plano, Texas.

23. On information and belief, Infineon AG has showcased its products at trade shows in Texas, including at the Applied Power Electronics Conference ("APEC"). For example, Infineon AG showed several new products, including new packaging for its MOSFET family of products, at APEC 2022 held in Houston, Texas, and played a large role as a contributor to the conference program, participating in over 20 sessions. Infineon AG also had an exhibit at the APEC 2018 conference in San Antonio, Texas, where Infineon AG showcased its power semiconductor technologies and participated in 15 sessions and seminars. In addition, Infineon AG attended the APEC 2011 conference in Fort Worth, Texas, where Infineon AG highlighted its OptiMOS 60-150V in CanPAK product. Infineon AG also showed its families of OptiMOS 3 power semiconductors and other products at the APEC 2008 conference held in Austin, Texas. At

the APEC 2006 conference held in Dallas, Texas, Infineon AG introduced its OptiMOS 2 100V family of MOSFET devices and its second-generation silicon carbide Schottky diodes. In addition, at APEC 2005 held in Austin, Texas, Infineon AG introduced its CoolMOS CS Server series of high-performance power transistors.

24. Infineon AG is subject to specific and general personal jurisdiction in this Court. This Court has personal jurisdiction over Infineon AG because, on information and belief, Infineon AG has engaged in continuous, systematic, and substantial activities within this State, including substantial marketing and sales of products and services within this State and District. Furthermore, on information and belief, this Court has personal jurisdiction over Infineon AG because Infineon AG has committed acts of infringement giving rise to MOSAID's claims for patent infringement within and directed to this District.

25. On information and belief, Infineon AG has conducted, and does conduct, substantial business in this District, directly and/or through subsidiaries, agents, representatives, or intermediaries, including, but not limited to: (i) at least a portion of the acts of infringement alleged herein; (ii) purposefully and voluntarily placing one or more Accused Products into the stream of commerce with the expectation that they will be purchased by consumers in this District; and/or (iii) regularly doing or soliciting business, engaging in other persistent courses of conduct, or deriving substantial revenue from goods and services provided to individuals in this State and in this District. Thus, Infineon AG is subject to this Court's specific and general personal jurisdiction pursuant to due process and the Texas Long-Arm Statute.

26. To the extent Infineon AG is not subject to jurisdiction in any state's courts of general jurisdiction, this Court has personal jurisdiction over Infineon AG pursuant to Federal Rule

of Civil Procedure 4(k)(2) because MOSAID's claims arise under federal law and exercising jurisdiction is consistent with the United States Constitution and laws.

27. The exercise of personal jurisdiction over Infineon AG would not offend traditional notions of fair play and substantial justice.

28. Infineon AG has acknowledged that this Court has personal jurisdiction over it. *See, e.g.*, *Staktek Group, L.P. v. Infineon Technologies AG*, No. 1:03-cv-00219-LY (W.D. Tex.) (Dkt. No. 3). Infineon AG has also admitted that personal jurisdiction existed over it in cases filed in other Texas district courts. *See, e.g.*, *Third Dimension Semiconductor, Inc. v. Infineon Technologies North America Corp. & Infineon Technologies AG*, No. 6:08-cv-00129-LED (E.D. Tex.) (Dkt. No. 24).

29. Infineon AG has also previously filed suit in this District. *See, e.g.*, *Infineon Technologies AG v. Harthcock*, No. 1:10-cv-00316-LY (W.D. Tex.) (Dkt. No. 1); *Infineon Technologies AG v. Infixeon, L.L.C.*, No. 1:07-cv-00039-SS (W.D. Tex.) (Dkt. No. 1).

30. Under 28 U.S.C. §§ 1391(b)-(d) and 1400(b), venue is proper in this District as to Infineon AG at least because Infineon AG is a foreign corporation subject to personal jurisdiction in this District and has committed acts of infringement within this District giving rise to this action.

31. To the extent that there is no district in which an action may otherwise be brought against Infineon AG, venue is proper in this District as to Infineon AG under 28 U.S.C. § 1391(b)(3) because Infineon AG is subject to personal jurisdiction in this Court.

32. On information and belief, Infineon Americas has substantial connections to the State of Texas, including this District. For example, Infineon Americas has a regular and established place of business in this District at 5204 E. Ben White Blvd, Austin, Texas 78741. This Austin location is a Production site for Infineon products.

33. Infineon operates its largest North American semiconductor factory, also known as "Fab25," in Austin, Texas. Infineon's Fab25 employs more than 1,000 people and plays a critical role in the global semiconductor supply chain, producing up to one billion semiconductor chips per year for major automotive, industrial, and communications companies throughout the world. On information and belief, the Infineon products manufactured at Fab25 include high-speed NOR Flash memory products and custom microcontrollers that include one or more of the Accused Products.

34. On information and belief, a number of Infineon's Austin employees are former Cypress employees who joined Infineon through the Cypress acquisition in 2020. On information and belief, these Austin employees include engineers, managers, technicians, and/or other personnel who work on research, development, design, manufacturing, testing, support, marketing, and/or sales of Accused Products.

35. On information and belief, Infineon Americas operates Fab25.

36. On information and belief, Infineon AG plays a role in the operation of Fab25, including because Infineon AG represents itself to the public as having a semiconductor manufacturing facility in Austin, Texas. For example, in March 2021, Infineon AG issued a press release from Munich stating that "Infineon Technologies (FSE: IFX / OTCQX: IFNNY) continues ramping up its manufacturing facility in Austin, Texas." In addition, in May 2022, Infineon AG issued a press release stating "Infineon Technologies AG (FSE: IFX / OTCQX: IFNNY), today announced that it has switched the operation of its Austin, Texas semiconductor factory, also known as 'Fab25,' to 100 percent renewable power."

37. Infineon Americas is subject to specific and general personal jurisdiction in this Court. This Court has personal jurisdiction over Infineon Americas because it has engaged in

continuous, systematic, and substantial activities within this State, including substantial research, development, production, marketing, and/or sales of products and services within this State and District. Furthermore, on information and belief, this Court has personal jurisdiction over Infineon Americas because Infineon Americas has committed acts of infringement giving rise to MOSAID's claims for patent infringement within and directed to this District.

38. On information and belief, Infineon Americas has conducted and does conduct substantial business in this District, directly and/or through subsidiaries, agents, representatives, or intermediaries, such substantial business including, but not limited to: (i) at least a portion of the acts of infringement alleged herein; (ii) purposefully and voluntarily placing one or more Accused Products into the stream of commerce with the expectation that they will be purchased by consumers in this forum; and/or (iii) regularly doing or soliciting business, engaging in other persistent courses of conduct, or deriving substantial revenue from goods and services provided to individuals in Texas and in this District. Thus, Infineon Americas is subject to this Court's specific and general personal jurisdiction pursuant to due process and the Texas Long-Arm Statute.

39. The exercise of personal jurisdiction over Infineon Americas would not offend traditional notions of fair play and substantial justice.

40. On information and belief, Infineon Americas has committed acts of infringement in this District and has regular and established places of business within this District under 28 U.S.C. § 1400(b). Thus, venue is proper in this District as to Infineon Americas under 28 U.S.C. § 1400(b).

41. Infineon maintains a permanent physical presence within this District. For example, Infineon maintains regular and established places of business at 5204 E. Ben White Blvd, Austin, Texas 78741.

42. On information and belief, Infineon's location(s) in this District are regular and established places of business under 28 U.S.C. § 1391, 28 U.S.C. § 1400(b), and *In re Cray, Inc.*, 871 F.3d 1355, 1360 (Fed. Cir. 2017).

a. On information and belief, Infineon's location(s) in this District are physical, geographical locations in this District. Each office location comprises one or more buildings or office spaces from which the business of Infineon is carried out. On information and belief, the location(s) are set apart for the purpose of carrying out Infineon's business, including, but not limited to, making, using, selling, offering for sale, and/or supporting Accused Products. On information and belief, Infineon advertises its physical location(s) in this District as places of its business.

b. On information and belief, Infineon's location(s) in this District are regular and established. Infineon identifies on its website (https://www.infineon.com/cms/en/about-infineon/company/find-a-location/) its address in this District as a regular and established place of Infineon's business.

c. On information and belief, Infineon's location(s) in this District are places of business of Infineon. On information and belief, Infineon conducts business from its location(s) in this District, including but not limited to, making, using, selling, offering for sale, and/or supporting Accused Products.

d. On information and belief, Infineon's location(s) in this District are physical, geographical location(s) in this District from which Infineon carries out its business.

e. On information and belief, Infineon employees work at Infineon's location(s) in this District. On information and belief, these Infineon employees are

regularly and physically present at Infineon's location(s) during business hours and conduct Infineon's business while working there.

FACTUAL ALLEGATIONS

I. ASSERTED PATENTS

A. THE '393 PATENT

43. United States Patent No. 7,685,393 ("the '393 Patent") is entitled "Synchronous Memory Read Data Capture." The United States Patent and Trademark Office duly and legally issued the '393 Patent on March 23, 2010, from U.S. Patent Application No. 11/477,659, filed on June 30, 2006.

44. MOSAID is the current owner of all rights, title, and interest in and to the '393 Patent, including the right to sue for past damages.

45. A true and correct copy of the '393 Patent is attached hereto as **Exhibit A** and is incorporated by reference herein.

46. The '393 Patent generally relates to synchronous memories and associated memory controllers. More particularly, the inventions of the '393 Patent relate to the control and transfer of read and write data between a memory controller and a synchronous memory using bidirectional data buses and bidirectional data strobe signals.

47. Claim 1 of the '393 Patent is directed to:

> 1. A method for controlling a synchronous memory comprising:
>
> establishing a read data path delay between the memory and a memory controller by:
>
> the memory controller writing an initialization sequence to predetermined locations of the memory;
>
> the memory controller sending a read command to the memory to read the predetermined locations and receiving returned data signals;

a predetermined time after sending the read command, the memory controller sampling the returned data signals to produce a single initialization sample;

using the initialization sample to determine the read data path delay between the memory and the memory controller.

48. The ’393 Patent solves a technological problem relating to read timing delay in Double Data Rate (“DDR”) SDRAM memory systems using bidirectional read/write buses. As the ’393 Patent explains, in source synchronous signaling, a data strobe clock is driven by the transmitting device along with the data. The clock and data paths from transmitter to receiver are matched. At the receiving device the data strobe clock is used to latch incoming data. In DDR SDRAM memory systems, the external data buses are bidirectional. Write data is sent to the memory from a memory controller and read data is sent from the memory to the controller.

49. During write operations, the write data instruction and the write data itself arrive source synchronously from the controller and the skew between the two sets of signals will be less than one bit period. However, during read operations the alignment between read command and read data on the bidirectional bus is much less certain. The delay through the command and address output drivers, through the package and printed circuit board connections to the memory device, back through the read data output buffers, package, and printed circuit board, and finally through the input buffers of the memory controller can vary by many bit periods depending on the system configuration and operating conditions. As the ’393 Patent explains, this alignment of read command and data creates several problems, including determining where in time to position the read data DQS enable signal, how to adjust for timing drift during operation, and how to transfer data clocked in with DQS to the system clock domain.

50. Accordingly, the ’393 Patent recognized a need for dynamic adjustment of the DQS enable time for certain DDR devices. The patent therefore provides solutions including systems

and methods relating to data training to determine the read delay and the optimum timing of the DQS enable signal.

51. Infineon is not licensed to the ’393 Patent and was not licensed during the six years preceding this action.

B. THE ’381 PATENT

52. United States Patent No. 9,972,381 (“the ’381 Patent”) is entitled “Memory with Output Control.” The United States Patent and Trademark Office duly and legally issued the ’381 Patent on May 15, 2018, from U.S. Patent Application No. 15/868,219, filed on January 11, 2018.

53. The ’381 Patent is a continuation of U.S. Patent Application No. 15/692,206, filed August 31, 2017 (now U.S. Patent No. 9,966,133), which is a continuation of U.S. Patent Application No. 15/345,552 filed November 8, 2016 (now U.S. Patent No. 9,779,804), which is a continuation of U.S. Patent Application No. 14/984,303, filed December 30,2015 (now U.S. Patent No. 9,524,783), which is a continuation of U.S. Patent Application No. 14/156,047, filed January 15, 2014 (now U.S. Patent No. 9,257,193), which is a continuation of U.S. Patent Application No. 13/867,437, filed April 22, 2013 (now U.S. Patent No. 8,654,601), which is a continuation of U.S. Patent Application No. 13/463,339, filed May 3, 2012 (now U.S. Patent No. 8,427,897), which is a continuation of U.S. Patent Application No. 12/882,931, filed September 15, 2010 (now U.S. Patent No. 8,199,598), which is a continuation of U.S. Patent Application No. 12/275,701, filed on November 21, 2008 (now U.S. Patent No. 7,826,294), which is a continuation of U.S. Patent Application No. 11/583,354, filed on October 19, 2006 (now U.S. Patent No 7,515,471), which is a continuation-in-part of U.S. Patent Application No. 11/324,023, filed December 30, 2005 (now. U.S. Patent No. 7,652,922), which claims the priority benefit of U.S. Provisional Application No. 60/722,368, filed September 30,2005 and U.S. Provisional

Application No. 60/847,790, filed September 27, 2006. The ’381 Patent is entitled to the benefit of these earlier filed applications.

54. MOSAID is the current owner of all rights, title, and interest in and to the ’381 Patent, including the right to sue for past damages.

55. A true and correct copy of the ’381 Patent is attached hereto as **Exhibit B** and is incorporated by reference herein.

56. The ’381 Patent generally relates to semiconductor memory devices, and more particularly to a memory architecture for improving the speed and/or capacity of semiconductor flash memory devices. For example, the ’381 Patent generally relates to an apparatus, system, and method for controlling data transfer to an output port of a serial data link interface in a semiconductor memory. In one example, a flash memory device may have multiple serial data links, multiple memory banks, and control input ports that enable the memory device to transfer the serial data to a serial data output port of the memory device. In another example, a flash memory device may have a single serial data link, a single memory bank, a serial data input port, and a control input port for receiving output enable signals. The flash memory devices may be cascaded in a daisy-chain configuration using echo signal lines to serially communicate between memory devices.

57. Claim 1 of the ’381 Patent is directed to:

> 1. A flash memory device comprising:
>
> a flash memory comprising a plurality of erasable blocks, each erasable block comprising a plurality of pages, each page comprising a plurality of flash memory cells;
>
> a clock input port configured to receive a clock signal;
>
> at least one common data interface configured to transfer command data, address data, input data and output data, wherein at least one of command data, address data, input data and

output data is transferred in synchronization with both rising and falling edges of the clock signal when the flash memory device is in a double data rate configuration;

a control input port configured to receive a control signal, wherein a transition of the control signal from an inactive state to an active state indicates a beginning of command data being received at the at least one common data interface;

a control circuitry configured to execute a page program operation to store the input data on a selected page, and to execute a read operation to retrieve the output data from the flash memory cells in accordance to the command data and address data received at the at least one common data interface; and

a status register configured to indicate a status of the flash memory device.

58. The ’381 Patent solved a technological problem relating to improving speed and/or capacity of flash memory devices. As the ’381 Patent explains, mobile electronic devices such as digital cameras, portable digital assistants, portable audio/video players, and mobile terminals continue to require mass storage memory, preferably non-volatile memory with ever increasing capacities and speed capabilities. Flash memory is popular because of its high density, non-volatility, and small size relative to hard disk drives. While flash memory modules existing in the prior art operated at speeds sufficient for many then-current consumer electronic devices, the ’381 Patent recognized that such memory modules likely would not be adequate for use in further devices where high data rates are desired. For example, a mobile multimedia device that records high definition moving pictures is likely to require a memory module with a programming throughput of at least 10 MB/s, which was not obtainable with prior art flash memory technology with typical programming data rates of 7 MB/s.

59. Programming and read throughput for flash memory could be directly increased by increasing the operating frequency of the flash memory; however, there was a significant problem

with signal quality at such high frequencies, which set a practical limitation on the operating frequency of the flash memory. High speed operating would cause well known communication degrading effects such as cross-talk, signal skew, and signal attenuation, for example, which degraded signal quality. In addition, flash memory communicates with other components using a set of parallel input/output (I/O) pins, which receive command instructions, receive input data, and provide output data. This is commonly known as a parallel interface. Such parallel interfaces use a large number of pins to read and write data. As the number of input pins and wires increases, so do a number of undesired effects, including inter-symbol interferences, signal skew, and cross-talk (which becomes more of a problem as the operating speed of the memory device increases).

60. Therefore, the ’381 Patent recognized a need in the art for memory modules, for use in mobile electronic devices, and solid-state drive applications that have increased memory capacities and/or operating speeds while minimizing the number input pins and wires required to access the memory modules. Accordingly, the ’381 Patent discloses, among other inventions, flash memory devices configured to receive serial input data and control signals from an external source and to provide data and control signals to an external device. The external source and external device may be other flash memory devices within the system. The devices may be configured to parse a target device information field in serial input data. If the memory device is not the target device, it may ignore the serial input data, thus saving additional processing time and resources. In addition, control signals may be used for the enabling/disabling of input/output ports. Therefore, the memory controller can have more flexibility to control communication between memory devices and the controller itself. These features allow the flash memory devices to be serially cascaded in a system to form a daisy-chain cascading scheme. The whole system can be easily expanded in terms of memory density without sacrificing the system’s overall performance.

61. Infineon is not licensed to the ’381 Patent and was not licensed during the six years preceding this action.

C. THE ’028 PATENT

62. United States Patent No. 10,140,028 (“the ’028 Patent”) is entitled “Clock Mode Determination in a Memory System.” The United States Patent and Trademark Office duly and legally issued the ’028 Patent on November 27, 2018, from U.S. Patent Application No. 15/957,120, filed on April 19, 2018.

63. The ’028 Patent is a continuation of U.S. Patent Application No. 15/655,336, filed July 20, 2017 (now U.S. Patent No. 9,971,518), which is a continuation of U.S. Patent Application No. 15/378,650, filed December 14, 2016 (now U.S. Patent No. 9,740,407), which is a continuation of U.S. Patent Application No. 15/183,162, filed January 15, 2016 (now U.S. Patent No. 9,552,889), which is a continuation of U.S. Patent Application No. 14/720,317, filed May 22, 2015 (now U.S. Patent No. 9,384,847), which is a continuation of U.S. Patent Application No. 14/491,440, filed September 19, 2014 (now U.S. Patent No. 9,042,199), which is a continuation of U.S. Patent Application No. 14/158,215, filed January 17, 2014 (now U.S. Patent No. 8,854,915), which is a continuation of U.S. Patent Application No. 13/871,487, filed April 26, 2013 (now U.S. Patent No. 8,644,108), which is a continuation of U.S. Patent Application No. 13/006,005, filed January 13, 2011 (now U.S. Patent No. 8,432,767), which is a divisional application that claims priority to U.S. Patent Application No. 12/032,249, filed on February 15, 2008 (now U.S. Patent No. 7,885,140), which claims the priority benefit of U.S. Provisional Application No. 60/902,003, filed February 16, 2007. The ’028 Patent is entitled to the benefit of these earlier filed applications.

64. MOSAID is the current owner of all rights, title, and interest in and to the ’028 Patent, including the right to sue for past damages.

65. A true and correct copy of the ’028 Patent is attached hereto as **Exhibit C** and is incorporated by reference herein.

66. The ’028 Patent generally relates to a clock mode configuration circuit for a memory device. For example, a memory system includes any number of memory devices serially connected to each other, where each memory device receives a clock signal. The clock signal can be provided either in parallel to all the memory devices or serially from memory device to memory device through a common clock input. The clock mode configuration circuit in each memory device is set to a parallel mode for receiving the parallel clock signal, and to a serial mode for receiving a source synchronous clock signal from a prior memory device. Depending on the set operating mode, the data input circuits will be configured for the corresponding data signal format, and the corresponding clock input circuits will be either enabled or disabled. The parallel mode and the serial mode is set by sensing a voltage level of a reference voltage provided to each memory device.

67. Claim 1 of the ’028 Patent is directed to:

> 1. A configurable non-volatile memory device comprising:
>
> plurality of non-volatile memory blocks;
>
> a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device;
>
> a first clock input port configured to receive a first clock input signal;
>
> a second clock input port configured to receive a second clock input signal, the second clock input signal being complementary to the first clock input signal;
>
> a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal;

one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of non-volatile memory blocks;

a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and the second clock input signal as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal and the second clock input signal as a single ended signal; and

one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks, the output data synchronized with the clock output signal in a double data rate configuration.

68. The ’028 Patent solved a technological problem relating to the performance of a flash memory system comprising multiple flash memory devices connected in parallel to the channel including data and control lines. The ’028 Patent explains that flash memory is a commonly used type of non-volatile memory in widespread use as mass storage for consumer electronics, such as digital cameras and portable digital music players for example. The density of an available flash memory component, consisting of 2 stacked dies, could be up to 32Gbits (4GB), which was suitable for use in popular USB Flash drives, since the size of one flash component is small.

69. The advent of 8 mega pixel digital cameras and portable digital entertainment devices with music and video capabilities spurred demand for ultra-high capacities to store the large amounts of data, which could not be met by the single flash memory device. Therefore,

multiple flash memory devices were combined together into a memory system to effectively increase the available storage capacity.

70. However, there were specific issues that would adversely impact performance of the system. For example, the configuration of a flash memory system with memory devices connected in parallel with respect to the channel imposed physical performance limitations. With the large number of parallel signals extending across the system, the signal integrity of the signals they carry would be degraded by crosstalk, signal skew, and simultaneous switching noise (SSN). Power consumption in such a configuration became an issue as each signal track between the flash controller and flash memory devices was frequently charged and discharged for signaling. With increasing system clock frequencies, the power consumption would increase. There was also a practical limit to the number of memory devices that could be connected in parallel to the channel. Furthermore, in order to accommodate a memory system having a large number of memory devices, either a controller having more channels would need to be used and/or the system would need to be clocked at a lower frequency.

71. Therefore, the ’028 Patent recognized a need to provide a memory system device architecture capable of high-speed operation while overcoming issues associated with the prior art memory system having memory devices connected in parallel. Accordingly, the ’028 Patent discloses and claims, for example, improved serial memory systems where the clock signal can be provided either in parallel to all the memory devices or serially from one memory device to another, providing high-speed operation overcoming the prior-art issues discussed above.

72. Infineon is not licensed to the ’028 Patent and was not licensed during the six years preceding this action.

II. DEFENDANTS’ KNOWLEDGE OF THE ASSERTED PATENTS

73. Infineon had knowledge of the Asserted Patents prior to the filing of this suit.

74. Between at least November 2017 and August 26, 2024, MOSAID (f/k/a Conversant Intellectual Property Management) engaged in many discussions, including through emails, letters, and business and technical meetings, with Cypress and/or Infineon regarding their infringement of MOSAID's patents, including the Asserted Patents.

75. On or about November 3, 2017, MOSAID sent a letter and exemplary claim charts to Cypress exhibiting Cypress's infringement of several patents, including the '393 Patent. MOSAID's November 3, 2017 exemplary claim charts included infringement assertions for at least Claim 1 of the '393 Patent. Receipt was confirmed by Terence Woodsome, Cypress's then-Deputy General Counsel.

76. On January 24, 2018, MOSAID followed up with Cypress regarding Cypress's response to MOSAID's letter and with a request to schedule a face-to-face meeting to further discussions.

77. On April 17, 2018, MOSAID sent Cypress additional information and updated exemplary claim charts regarding Cypress's infringement of the '393 Patent.

78. On June 29 and July 30, 2018, MOSAID followed up with Cypress regarding MOSAID's infringement allegations and again requested a face-to-face meeting.

79. On August 2 and August 22, 2018, MOSAID again contacted Cypress to request a face-to-face meeting to occur sometime in September 2018.

80. On September 26, 2018, MOSAID met with Cypress for further discussion. During the meeting, MOSAID shared additional information and updated exemplary claim charts. MOSAID sent copies of the updated exemplary claim charts for the '393 Patent to Cypress by email on October 2, 2018.

81. On February 27, 2019, MOSAID followed up with Cypress after having received no further responses from Cypress following the September 2018 meeting. In that February 27 correspondence, MOSAID also provided new exemplary claim charts for new infringement assertions and asked to continue discussions. The new exemplary claim charts included charts for the ’381 Patent (which included infringement assertions for at least Claim 1).

82. Between February 2019 and February 2020, MOSAID and Cypress exchanged numerous communications and materials regarding Cypress’s infringement. MOSAID also requested another meeting to discuss any outstanding technical matters and present its thoughts on business terms for a license to MOSAID’s patent portfolio.

83. On February 21, 2020, MOSAID provided exemplary claim charts for three additional patents, including the ’028 Patent. The exemplary claim chart for the ’028 Patent included infringement assertions for at least Claim 1.

84. The parties engaged in another year of back and forth between February 2020 and February 2021. By then, Infineon had completed its acquisition of Cypress, and Cypress’s personnel, including Mr. Woodsome, became employees of Infineon and transitioned to using Infineon email addresses.

85. MOSAID and Infineon held meetings on February 24 and March 10, 2021. MOSAID indicated its desire to work on a formal license proposal based on the active patents still in discussion, which included the Asserted Patents.

86. On February 28, 2023, MOSAID reconnected with Infineon on the parties’ outstanding discussions, and for the next year the parties exchanged further communications regarding Infineon’s infringement of the Asserted Patents.

87. In February and April 2024, MOSAID noted that technical discussions between MOSAID and Infineon (including Cypress) had been going on for many years, so MOSAID was now at a point where it would appreciate knowing whether Infineon was ready and willing to take a license or provide feedback on MOSAID's business proposal.

88. On May 23, 2024, MOSAID again reached out to Infineon in an effort to license Infineon to the Asserted Patents, and requested "business discussions to finally resolve these issues." However, Infineon ignored MOSAID's request and did not respond.

89. On August 26, 2024, MOSAID followed up yet again and suggested "a call so that we don't misunderstand your position on this matter." MOSAID again offered to license its patent portfolio, including the Asserted Patents, to Infineon on reasonable terms. But again, Infineon ignored MOSAID's correspondence.

90. Before filing this lawsuit, on March 11, 2025, MOSAID attempted one last time to resolve this dispute, noting that "Infineon's refusal to respond to our emails dated May 23, 2024, and August 26, 2024, as well as its general unwillingness to engage in business discussions toward a license" was leaving MOSAID with few alternatives. Nonetheless, MOSAID reiterated that it "remains committed to reaching a licensing agreement with Infineon." Once again, Infineon did not respond.

91. Ultimately, since at least November 3, 2017, MOSAID and Infineon (including Cypress) have engaged in numerous technical and business discussions relating to a license for MOSAID's patent portfolio, including each of the Asserted Patents. During those discussions, MOSAID offered to provide a license to the Asserted Patents. But to date, Infineon has not made any offer to license MOSAID's patent portfolio, including the Asserted Patents. Nor has Infineon ceased its infringing conduct.

III. THE ACCUSED PRODUCTS

92. Infineon manufactures, uses, offers for sale, and/or sells in the United States, and/or imports into the United States, flash memory and microcontrollers, including the Accused Products, for use in a variety of end-products in the communications, IoT, automotive, computer, and/or consumer electronics industries. Both the Accused Products and the consumer end-products incorporating the Accused Products have been, and continue to be, widely available for sale in the United States.

93. Infineon's Accused Products include at least the Accused Processor Products, Accused Memory Products, and substantially similar products, made, used, sold, or offered for sale in the United States, and/or imported into the United States.

94. Infineon has advertised, offered for sale, and sold—and continues to advertise, offer for sale, and sell—the Accused Products on Infineon's website.

95. Infineon advertises, offers for sale, and sells the accused TRAVEO T2G series microcontrollers on its website, including for example at https://www.infineon.com/cms/en/product/microcontroller/32-bit-traveo-t2g-arm-cortex-microcontroller/, and as shown above in paragraph 16.

96. Infineon advertises, offers for sale, and sells accused flash memory products on its website, including for example at https://www.infineon.com/cms/en/product/memories/nor-flash/, and as shown above in paragraph 16.

COUNT I: INFRINGEMENT OF THE '393 PATENT

97. MOSAID incorporates by reference and realleges paragraphs 1 through 96 as if specifically set forth herein.

98. In violation of 35 U.S.C. § 271(a), Infineon is and has been directly infringing one or more of the claims of the '393 Patent, including at least Claim 1, either literally and/or under

the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least one of the Accused Products.

99. Claim 1 of the ’393 Patent recites:

> 1. A method for controlling a synchronous memory comprising:
>
> establishing a read data path delay between the memory and a memory controller by:
>
> the memory controller writing an initialization sequence to predetermined locations of the memory;
>
> the memory controller sending a read command to the memory to read the predetermined locations and receiving returned data signals;
>
> a predetermined time after sending the read command, the memory controller sampling the returned data signals to produce a single initialization sample;
>
> using the initialization sample to determine the read data path delay between the memory and the memory controller.

100. The Accused Processor Products, including at least the TRAVEO T2G microcontroller products, practice each element of Claim 1 of the ’393 Patent.

101. The Accused Processor Products perform a method for controlling a synchronous memory. For example, the TRAVEO T2G microcontroller products include a Serial Memory Interface (“SMIF”) that provides an interface to memories using Serial Peripheral Interface (“SPI”) or HYPERBUS protocols. For example, as shown below, the TRAVEO T2G supports a dual-quad SPI mode, where data can be written to and read from two Quad SPI memories:

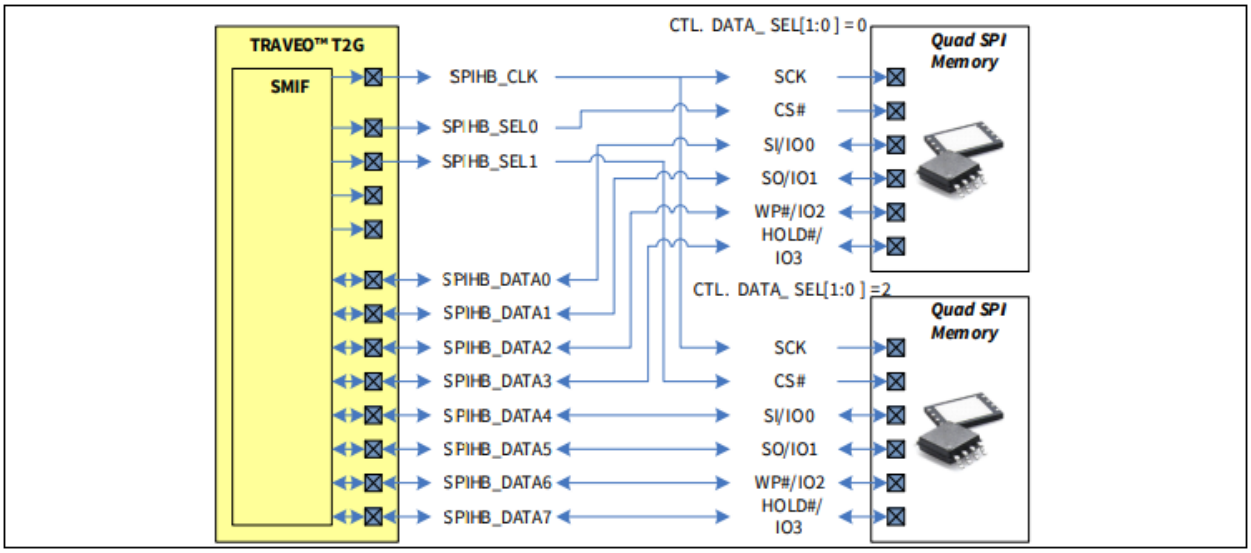


Figure 5 **Dual-quad configuration**

(Infineon "Using the SMIF in TRAVEO T2G family" Application Note, at 10.)

102. The method performed when the Accused Processor Products are used includes establishing a read data path delay between the memory and a memory controller. For example, the SMIF of the TRAVEO T2G supports various data capture schemes, including delay line and data learning pattern ("DLP")-based capture. In the dual-quad SPI mode, for example, the TRAVEO T2G products use the DLP feature to optimize dual data rate ("DDR") read performance for the Quad SPI memory.

103. In the Accused Processor Products, a memory controller writes an initialization sequence to predetermined locations of the memory. For example, when the TRAVEO T2G products use DLP to optimize read performance for Quad SPI memories, the memory's nonvolatile data learning register ("NVDLR") and volatile data learning register ("VDLR") are used to define a sequence of data learning pattern values that are used during a read transaction. During power-up or reset, the value in the NVDLR is loaded into the VDLR. The sequence stored in the VDLR can be changed by the host during system operation.

104. In the Accused Processor Products, the memory controller sends a read command to the memory to read the predetermined locations and receives returned data signals. For example, when the TRAVEO T2G products use DLP to optimize read performance for Quad SPI memories, the host memory controller transfers the command operation, among other instruction data, to the memory in order to initiate retrieval of the DLP pattern stored in the NVDLR and/or VDLR:

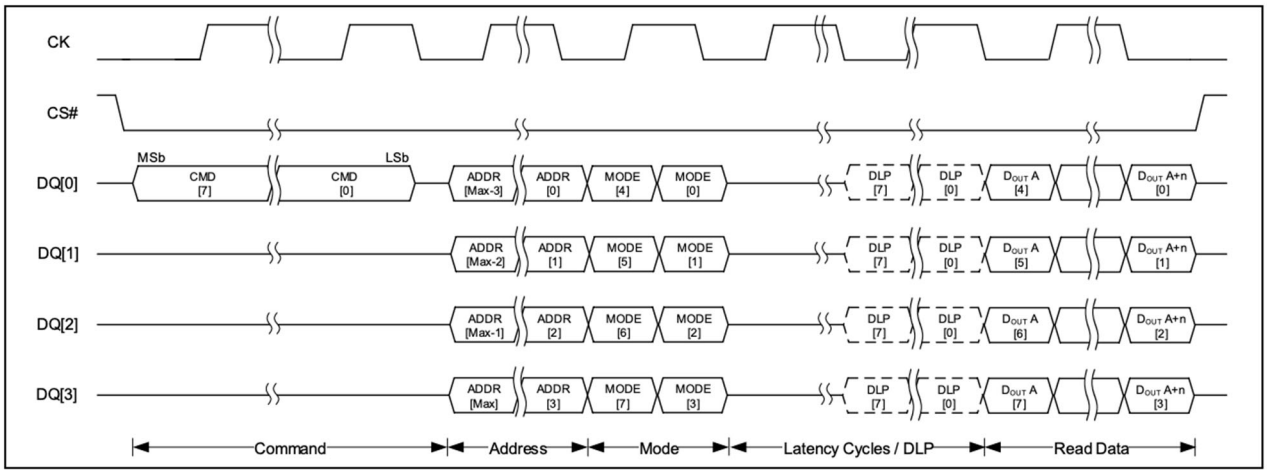


Figure 6 **DDR QUAD IO Read (DDRQIOR) Command (1S-4D-4D)**

(Infineon "DLP Optimized Read Performance for Quad SPI Flash FL-S, FS-S, and FL-L Families" Application Note, at 8.)

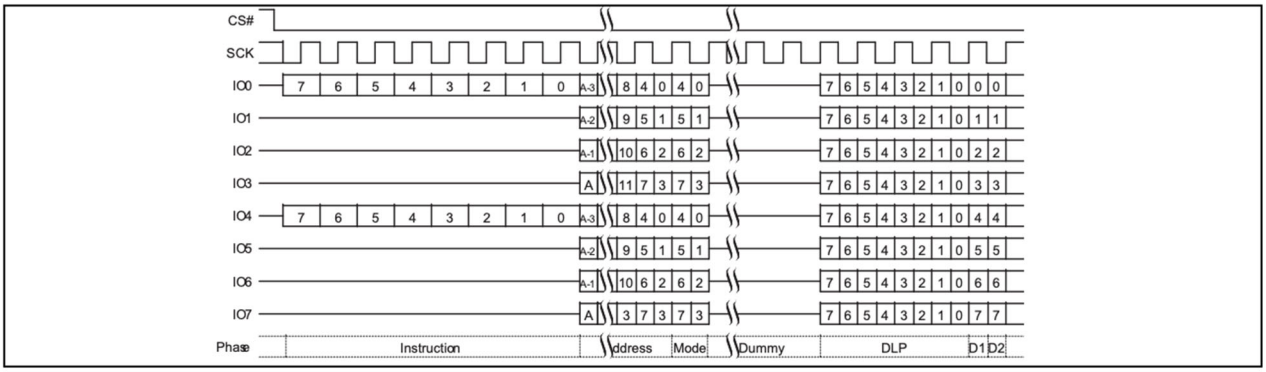


Figure 57 **Dual-Quad SPI DDR Quad I/O Read initial access**[41, 42]

(Infineon 256 Mb (32 MB) / 512 Mb (64MB) FL-S Flash Datasheet, at 91.)

105. In response, the host memory controller receives returned data signals, such as the sequence of DLP values in the VDLR:

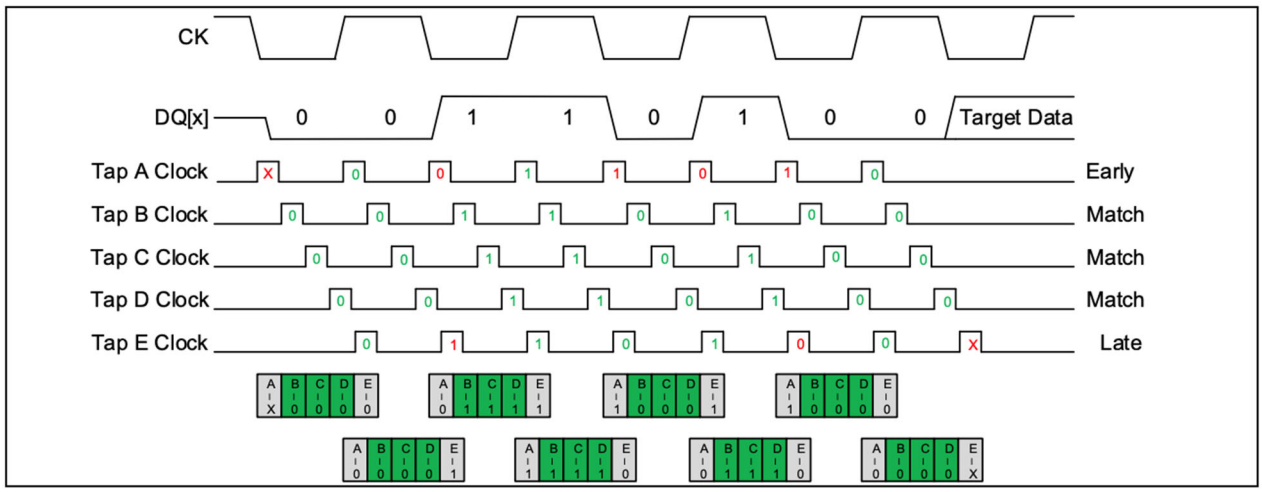


Figure 9 **Host Capture Strategy DDR**

(Infineon "DLP Optimized Read Performance for Quad SPI Flash FL-S, FS-S, and FL-L Families" Application Note, at 11.)

106. In the Accused Processor Products, the memory controller samples the returned data signals to produce a single initialization sample. For example, as shown above in Figure 9, when the TRAVEO T2G products uses DLP to optimize read transactions, the host memory controller samples the target DQ while the DLP is being output. In addition, the sampling occurs a predetermined time after sending the read command. For example, there is a latency period of dummy cycles between the command phase and the host memory controller's sampling of returned data signals. An example of the latency or dummy period is illustrated below:

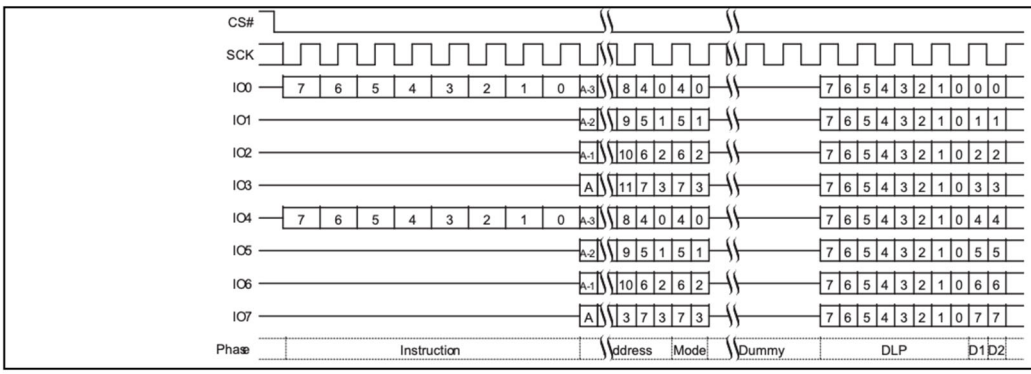


Figure 57 **Dual-Quad SPI DDR Quad I/O Read initial access**[41, 42]

(Infineon 256 Mb (32 MB) / 512 Mb (64MB) FL-S Flash Datasheet, at 91.)

107. The Accused Processor Products use the initialization sample to determine the read data path delay between the memory and the memory controller. For example, when the TRAVEO T2G products uses DLP to optimize read transactions, the host memory controller uses the data sampled during the DLP portion of the read sequence in order to determine the skew time to capture the data during the rest of the read operation.

108. During license discussions, MOSAID provided Infineon with exemplary claim charts explaining in detail Infineon's infringement of the'393 Patent, including at least Claim 1.

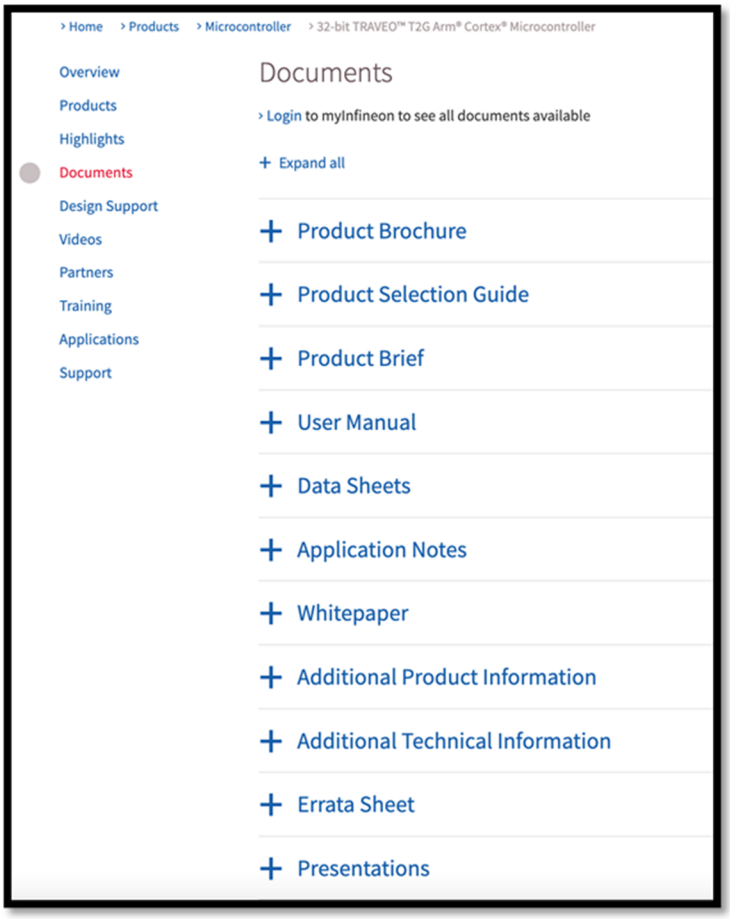
109. In violation of 35 U.S.C. § 271(b), Infineon is and has been infringing one or more of the claims of the '393 Patent, including at least Claim 1, indirectly by inducing infringement by third parties, including for example Infineon's customers and/or end-users of the Accused Processor Products, in this District and elsewhere in the United States. For example, on information and belief, at least the TRAVEO T2G has been and is being used by Infineon's customers and/or end-users in consumer automotive products, including for seat control units, immobilizers, tire pressure monitoring system sensors, door control units, central gateways, body control modules, instrument clusters, head-up displays, digital mirrors, matrix LED headlight control units, and HVAC systems, including HVAC systems with displays. Direct infringement

by Infineon's customers and/or end-users occurs at least by the use of the Accused Processor Products, including at least the TRAVEO T2G, including use of consumer products incorporating them.

110. On information and belief, Infineon supplies hardware, firmware, and/or software that are especially made or especially adapted to practice the inventions claimed in the '393 Patent, including at least Claim 1, to induce third parties, including for example Infineon's customers and/or end-users of the Accused Processor Products, including at least the TRAVEO T2G, to use such products in a manner that would infringe one or more claims of the '393 Patent, including at least Claim 1.

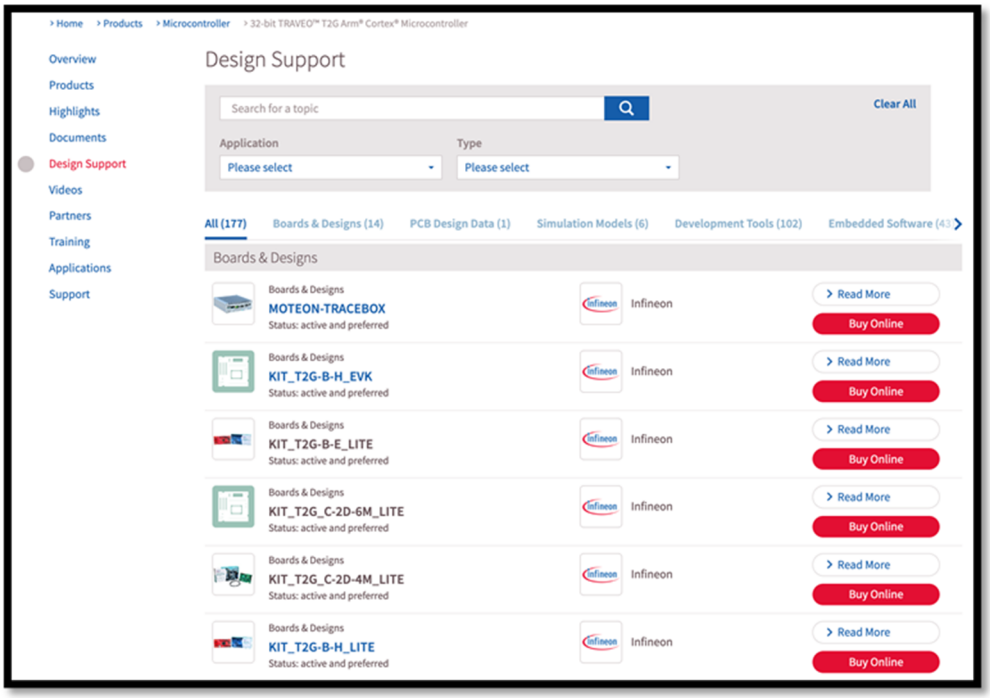
111. On information and belief, Infineon markets and advertises the Accused Processor Products, including at least the TRAVEO T2G, including on its website, to induce third parties, including Infineon's customers and/or end-users, to use the products in a manner that would infringe one or more claims of the '393 Patent, including at least Claim 1. *See, e.g.*, https://www.infineon.com/cms/en/product/microcontroller/32-bit-traveo-t2g-arm-cortex-microcontroller.

112. On information and belief, Infineon furnishes instructive materials, technical support, and information concerning the operation and use of the Accused Processor Products, including at least the TRAVEO T2G, to induce third parties, including Infineon's customers and/or end-users, to use the products in a manner that would infringe one or more claims of the '393 Patent, including at least Claim 1. For example, on its website, Infineon furnishes at least product brochures, product selection guides, product briefs, user manuals, data sheets, application notes, whitepapers, errata sheets, presentations, and additional product and technical information such as architecture technical reference manuals:



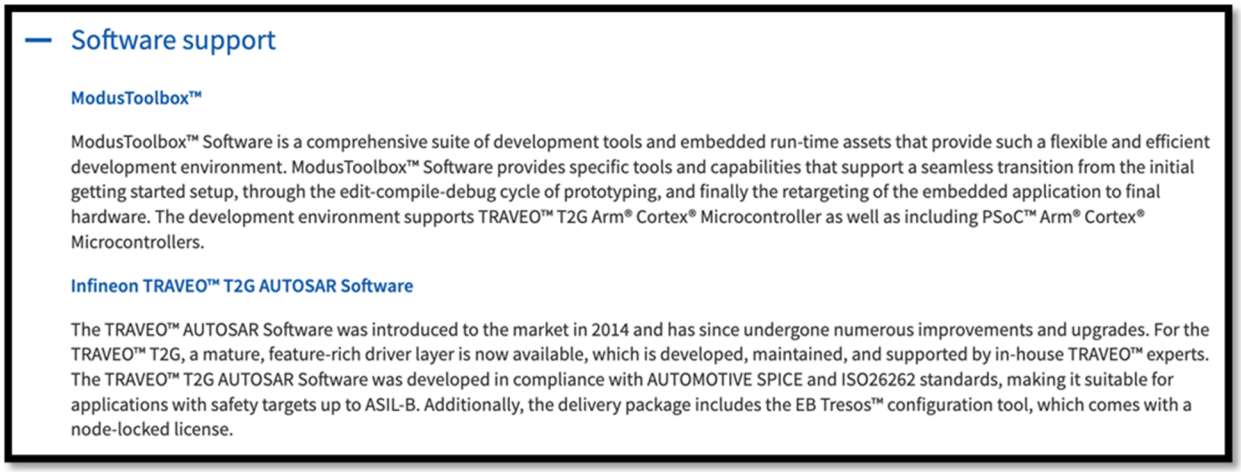
(Exemplary categories of instructive materials provided for the TRAVEO T2G, with additional materials provided for each product subcategory under their respective web subpages.)

113. On its website, Infineon also furnishes development tools and design support materials for the Accused Processor Products, including at least the TRAVEO T2G:



(Exemplary design support materials for TRAVEO T2G.)

114. Further, Infineon provides software, including code examples and drivers:



Software support

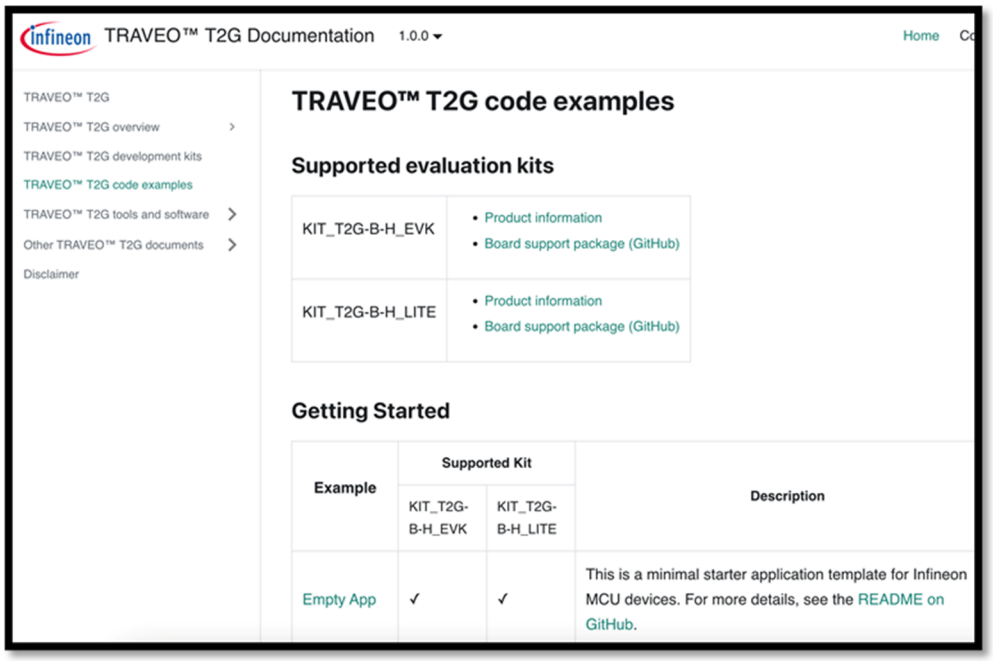
ModusToolbox™

ModusToolbox™ Software is a comprehensive suite of development tools and embedded run-time assets that provide such a flexible and efficient development environment. ModusToolbox™ Software provides specific tools and capabilities that support a seamless transition from the initial getting started setup, through the edit-compile-debug cycle of prototyping, and finally the retargeting of the embedded application to final hardware. The development environment supports TRAVEO™ T2G Arm® Cortex® Microcontroller as well as including PSoC™ Arm® Cortex® Microcontrollers.

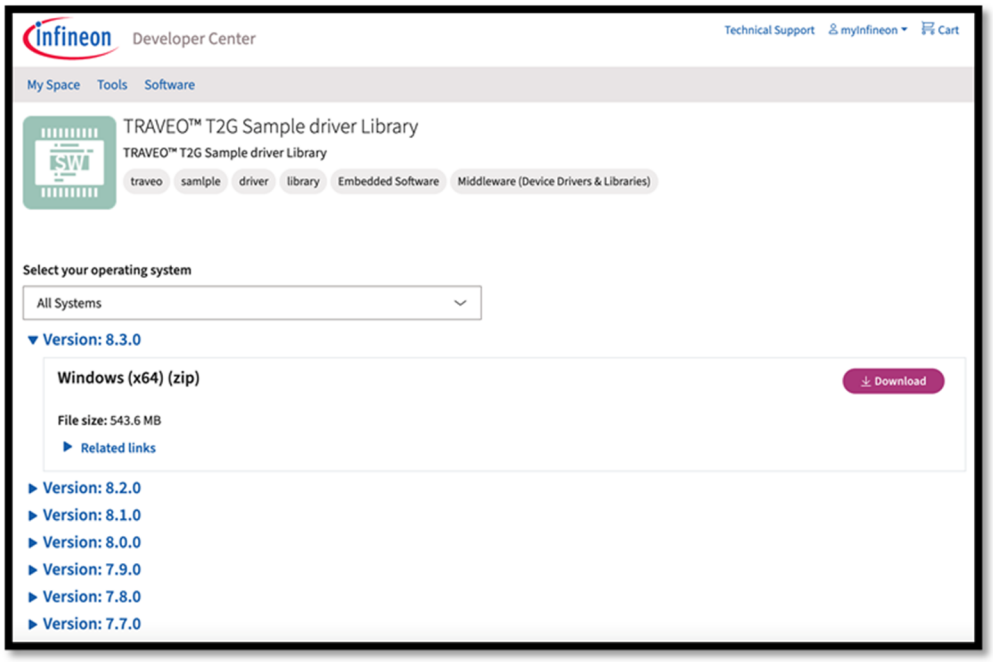
Infineon TRAVEO™ T2G AUTOSAR Software

The TRAVEO™ AUTOSAR Software was introduced to the market in 2014 and has since undergone numerous improvements and upgrades. For the TRAVEO™ T2G, a mature, feature-rich driver layer is now available, which is developed, maintained, and supported by in-house TRAVEO™ experts. The TRAVEO™ T2G AUTOSAR Software was developed in compliance with AUTOMOTIVE SPICE and ISO26262 standards, making it suitable for applications with safety targets up to ASIL-B. Additionally, the delivery package includes the EB Tresos™ configuration tool, which comes with a node-locked license.

(TRAVEO T2G Overview, Software Support.)

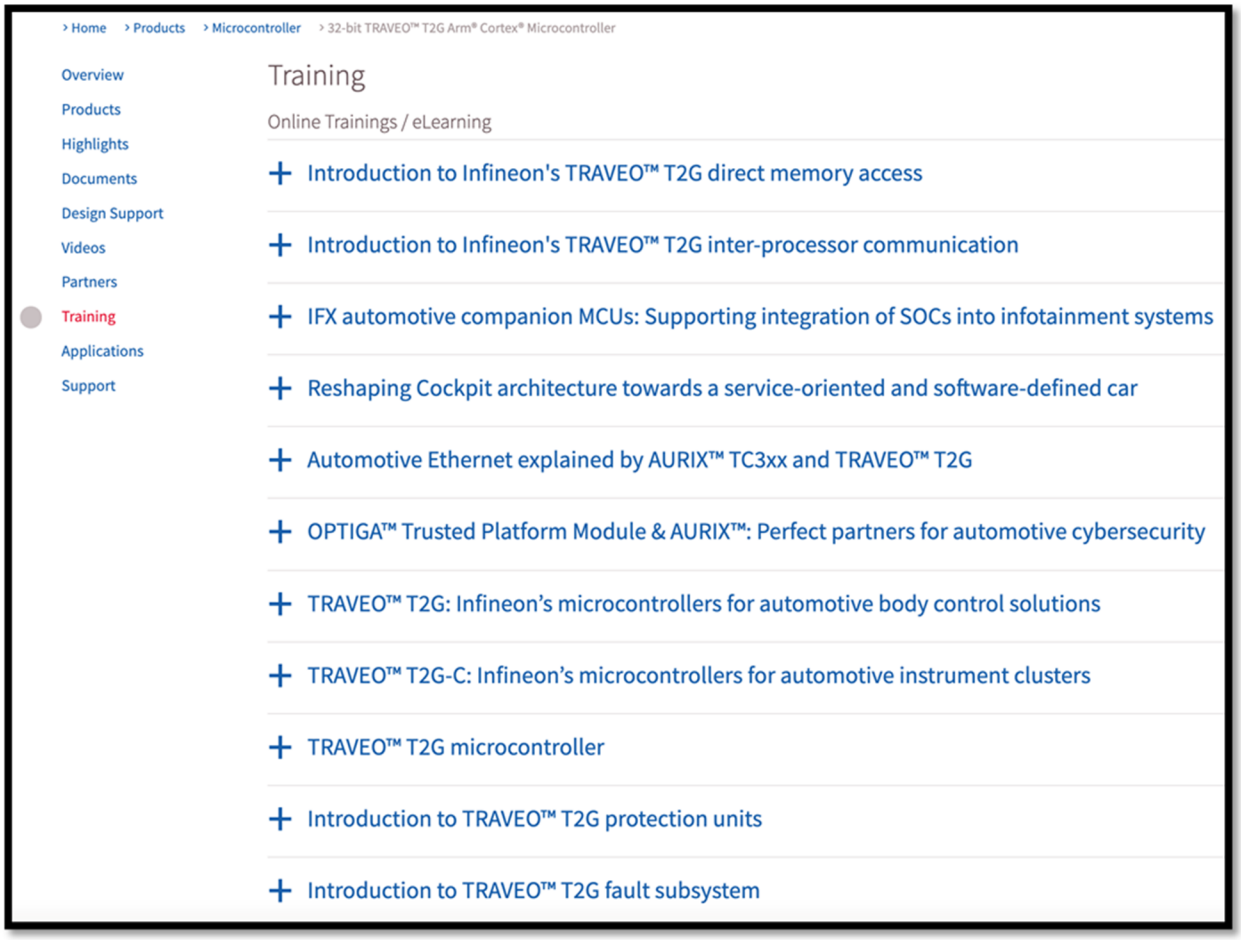


(Infineon TRAVEO™ T2G Documentation 1.0.0, TRAVEO™ T2G code examples.)

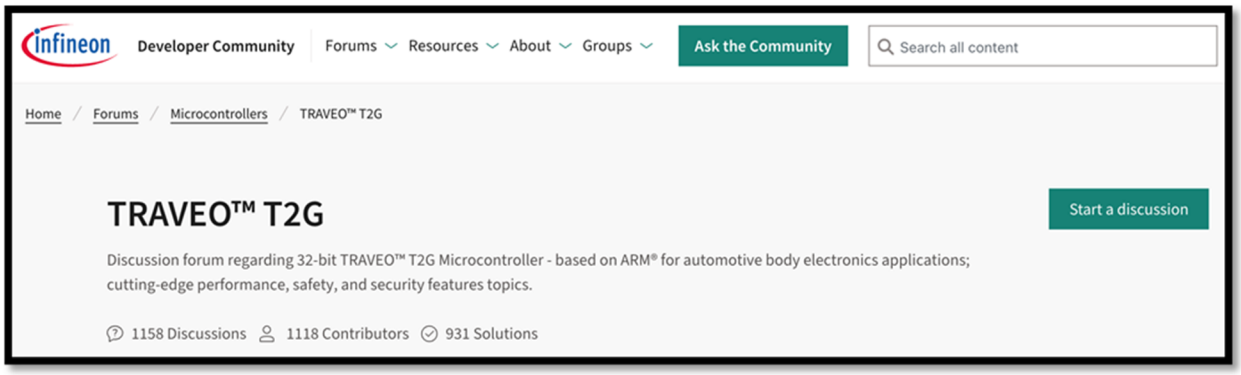


(Infineon Developer Center, TRAVEO™ T2G Sample driver Library.)

115. In addition, on its website, Infineon provides training materials and help from Infineon support engineers:



(Exemplary Training Materials for TRAVEO T2G.)



(Infineon Developer Community for TRAVEO T2G.)

116. Infineon knew or should have known of the '393 Patent and its infringement through a series of correspondence and meetings expressly notifying Infineon of the '393 Patent and Infineon's infringement thereof. As a result, Infineon knew or should have known it infringed

one or more claims of the ’393 Patent, including at least Claim 1, at least as early as November 3, 2017, when MOSAID began discussions with Cypress regarding the ’393 Patent and provided actual notice of infringement.

117. Alternatively, Infineon knew or should have known of the ’393 Patent and its infringement no later than April 2020, when Infineon acquired Cypress and continued discussions with MOSAID regarding the ’393 Patent and Infineon’s infringement thereof.

118. At a minimum, both Infineon Defendants have had actual knowledge of the ’393 Patent, and their infringement thereof, at least as of the date of filing of this Complaint.

119. Despite this knowledge, Infineon has continued to induce third parties, including Infineon’s customers and/or end-users of the Accused Processor Products, including at least the TRAVEO T2G, to infringe one or more claims of the ’393 Patent, including at least Claim 1, with the specific intent to cause infringement. Infineon knew or should have known that those acts would induce actual infringement by third parties, including Infineon’s customers and/or end-users of the Accused Processor Products, including at least the TRAVEO T2G, of one or more of the claims of the ’393 Patent, including at least Claim 1.

120. Therefore, Infineon has induced infringement by others of one or more of the claims of the ’393 Patent, including at least Claim 1, with the specific intent to induce acts that constitute infringement of the ’393 Patent and with knowledge that such acts infringe one or more claims of the ’393 Patent, including at least Claim 1.

121. In violation of 35 U.S.C. § 271(c), Infineon is and has been infringing one or more of the claims of the ’393 Patent, including at least Claim 1, indirectly by contributing to infringement by third parties, including for example Infineon’s customers and/or end-users of the Accused Processor Products, including at least the TRAVEO T2G, in this District and elsewhere

in the United States. Direct infringement by Infineon's customers and/or end-users occurs at least by the use of the Accused Processor Products, including at least the TRAVEO T2G, including use of consumer products incorporating them.

122. On information and belief, Infineon made and sold hardware, firmware, and/or software components (*e.g.*, processors and/or software drivers) especially made or especially adapted to practice the invention claimed in the '393 Patent, including at least Claim 1. For example, as explained above, Infineon made and sold TRAVEO T2G MCU hardware and accompanying software, firmware, and driver code. On information and belief, such hardware, firmware, and/or software components (i) are a material part of the invention and (ii) are not staple articles or commodities of commerce suitable for substantial non-infringing use at least because they are specifically designed to perform the claimed functionality. Any other use of such hardware, firmware, and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

123. Therefore, Infineon has contributed to the infringement by others of one or more of the claims of the '393 Patent, including at least Claim 1.

124. Infineon's infringement of one or more claims of the '393 Patent, including at least Claim 1, has been, and continues to be, willful.

125. As explained above, Infineon had actual knowledge of the '393 Patent and its infringement thereof at least as early as November 3, 2017, when MOSAID began discussions with Cypress regarding the '393 Patent, and in any event no later than April 2020, when Infineon acquired Cypress and continued discussions with MOSAID.

126. As explained above, on several occasions beginning at least as early as November 3, 2017, MOSAID notified Infineon (including Cypress) of the '393 Patent and Infineon's infringement thereof, including infringement of at least Claim 1.

127. Despite knowing of the '393 Patent at least as early as November 3, 2017 (and no later than April 2020), Infineon did not cease its infringing activities. Infineon has continued to infringe one or more claims of the '393 Patent, including at least Claim 1, in disregard of MOSAID's patent rights. As a result, Infineon deliberately and intentionally infringed the '393 Patent, and continues to do so, after receiving express and actual knowledge of both the '393 Patent and its infringement thereof.

128. Therefore, Infineon's infringement of the '393 Patent, including at least Claim 1, has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys' fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

COUNT II: INFRINGEMENT OF THE '381 PATENT

129. MOSAID incorporates by reference and realleges paragraphs 1 through 128 as if specifically set forth herein.

130. In violation of 35 U.S.C. § 271(a), Infineon is and has been directly infringing one or more of the claims of the '381 Patent, including at least Claim 1, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least one of the Accused Products.

131. Claim 1 of the '381 Patent recites:

> 1. A flash memory device comprising:

a flash memory comprising a plurality of erasable blocks, each erasable block comprising a plurality of pages, each page comprising a plurality of flash memory cells;

a clock input port configured to receive a clock signal;

at least one common data interface configured to transfer command data, address data, input data and output data, wherein at least one of command data, address data, input data and output data is transferred in synchronization with both rising and falling edges of the clock signal when the flash memory device is in a double data rate configuration;

a control input port configured to receive a control signal, wherein a transition of the control signal from an inactive state to an active state indicates a beginning of command data being received at the at least one common data interface;

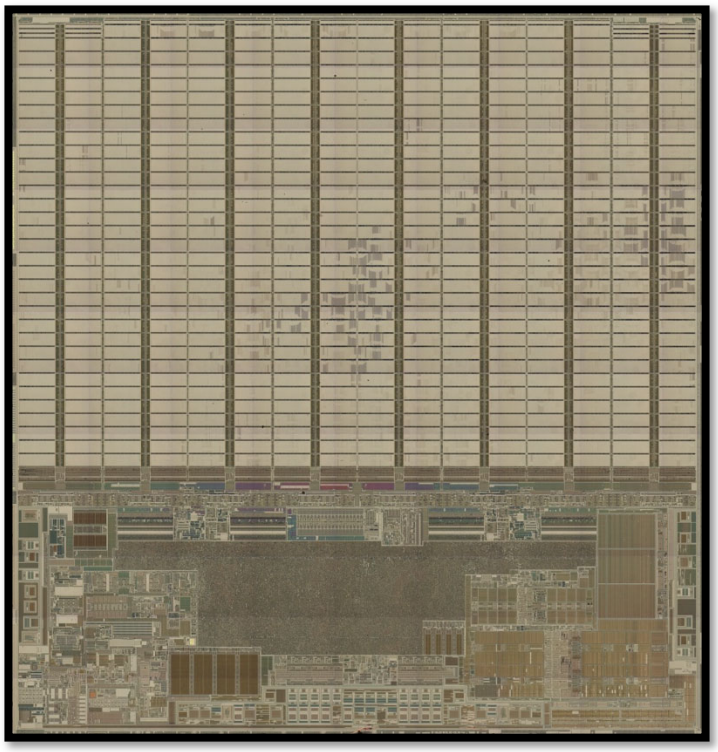
a control circuitry configured to execute a page program operation to store the input data on a selected page, and to execute a read operation to retrieve the output data from the flash memory cells in accordance to the command data and address data received at the at least one common data interface; and

a status register configured to indicate a status of the flash memory device.

132. The Accused Products, including at least the HYPERFLASH products, practice each element of Claim 1 of the ’381 Patent.

133. The Accused Products, for example the HYPERFLASH products, are flash memory devices.

134. The Accused Products include a flash memory comprising a plurality of erasable blocks, each erasable block comprising a plurality of pages, each page comprising a plurality of flash memory cells. For example, the HYPERFLASH products include a main flash memory array comprising a plurality of erasable blocks, wherein each erasable block includes a plurality of pages, and each page includes a plurality of flash memory cells:



(Image of S26KS Memory Array)

512 Mb (64 MB) / 256 Mb (32 MB) / 128 Mb (16 MB) HYPERFLASH™ family
HYPERBUS™, 3.0 V / 1.8 V

General description

Each random read accesses a 32-byte length and aligned set of data called a page. Each page consists of a pair of 16-byte aligned groups of array data called half-pages. Half-pages are aligned on 16-byte address boundaries. A read access requires two clock cycles to define the target half-page address and the burst type, then an additional initial latency. During the initial latency period the third clock cycle will specify the starting address within the target half-page. After the initial data value has been output, additional data can be read from the page on subsequent clock cycles in either a wrapped or linear manner. When configured in linear burst mode, while a page is being burst out, the device will automatically fetch the next sequential page from the MIRRORBIT™ flash memory array. This simultaneous burst output while fetching from the array allows for a linear sequential burst operation that can provide a sustained output of 333 MBps data rate [1-byte (8-bit data bus) × 2 (Data on both clock edges) × 166 MHz = 333 MBps].

Table 1 S26KS and S26KL address map

Type	Count	Addresses	Note
Word address within a half-page (16-byte)	8 (word addresses)	A2–A0	16 bytes
Word address within write buffer line (512-byte)	256 (word addresses)	A7–A0	512 bytes
Half-pages (16 bytes) within erase sector (256 KB)	8192 (half-pages)	A16–A3	–
Write buffer lines (512 bytes) within erase sector (256 KB)	512 (lines)	A16–A8	–
Total number of erase sectors (256 KB)	256 (512 Mb) 128 (256 Mb) 64 (128 Mb)	Amax–A17	–

(Infineon 512 Mb (64 MB) / 256 Mb (32 MB) / 128 Mb (16 MB) HYPERFLASH family Datasheet, at 6.)

135. The Accused Products include a clock input port configured to receive a clock signal. For example, the HYPERFLASH products include a Clock ("CK") input.

136. The Accused Products include at least one common data interface configured to transfer command data, address data, input data and output data. For example, the HYPERFLASH products include a DQ bus that can transfer command, address, and data information.

137. In the Accused Products, at least one of command data, address data, input data and output data is transferred in synchronization with both rising and falling edges of the clock signal when the flash memory device is in a double data rate configuration. For example, during read and write operations in the HYPERFLASH products, bytes of data are presented on the rising and falling edges of CK:

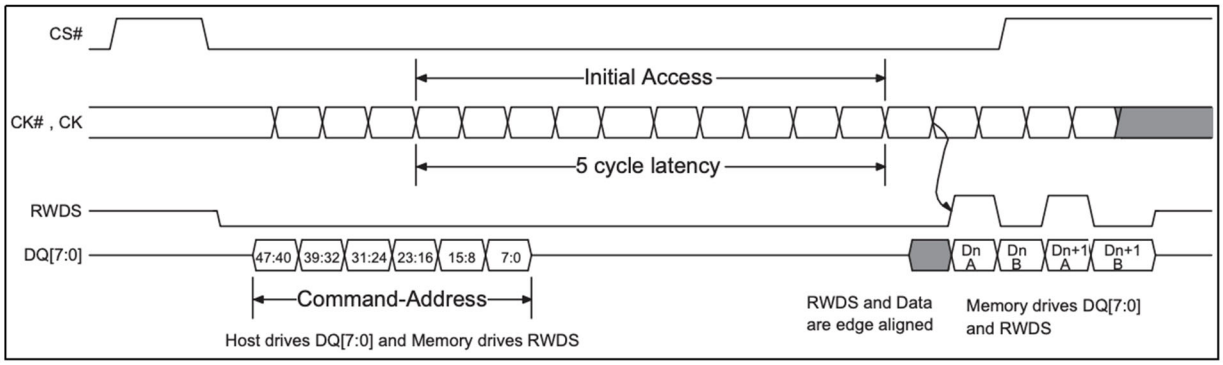


Figure 7 **Read operation**[5, 6, 7, 8]

(Infineon 512 Mb (64 MB) / 256 Mb (32 MB) / 128 Mb (16 MB) HYPERFLASH family Datasheet, at 15.)

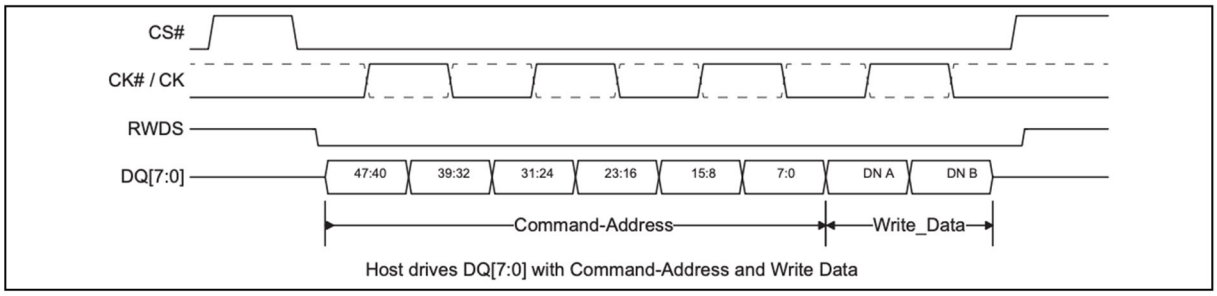


Figure 10 **Write operation**[21, 22, 23]

(Infineon 512 Mb (64 MB) / 256 Mb (32 MB) / 128 Mb (16 MB) HYPERFLASH family Datasheet, at 19.)

138. The Accused Products include a control input port configured to receive a control signal. For example, the HYPERFLASH products include a Chip Select ("CS#") signal.

139. In the Accused Products, a transition of the control signal from an inactive state to an active state indicates a beginning of command data being received at the at least one common data interface. For example, in the HYPERFLASH products, bus transactions are initiated by a "High" to "Low" transition of the CS# signal. As shown above in Figure 10 for example, the transition of the CS# signal indicates a beginning of command data being received.

140. The Accused Products include a control circuitry configured to execute a page program operation to store the input data on a selected page. For example, the HYPERFLASH products include control logic circuitry, including for example an Embedded Algorithm Controller ("EAC"), configured to execute page program operations to store input data on a selected page.

141. In the Accused Products, the control circuitry is also configured to execute a read operation to retrieve the output data from the flash memory cells in accordance to the command data and address data received at the at least one common data interface. For example, the control logic circuitry of the HYPERFLASH products is also configured to execute read operations to retrieve data in accordance with the command/address data received at the DQ bus.

142. The Accused Products include a status register configured to indicate a status of the flash memory device. For example, the HYPERFLASH products include a status register containing bits indicating the status of Embedded Algorithms.

143. During license discussions, MOSAID provided Infineon with exemplary claim charts explaining in detail Infineon's infringement of the '381 Patent, including at least Claim 1.

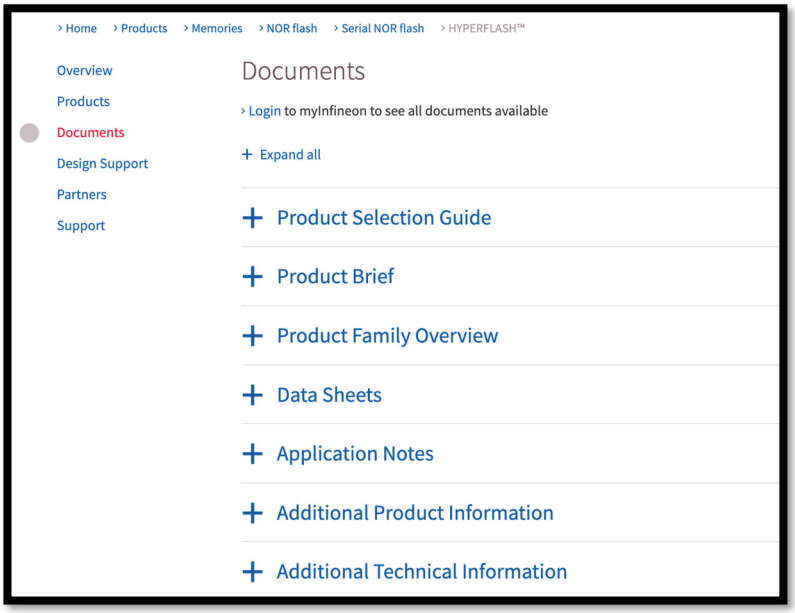
144. In violation of 35 U.S.C. § 271(b), Infineon is and has been infringing one or more of the claims of the '381 Patent, including at least Claim 1, indirectly by inducing infringement by third parties, including for example Infineon's customers and/or end-users of the Accused Products, including at least the HYPERFLASH products, in this District and elsewhere in the United States. For example, on information and belief, at least the HYPERFLASH products have been and are being used by Infineon's customers and/or end-users in consumer products, including for automotive advanced driver assistance systems, instrument clusters, and infotainment systems, factory automation, and networking routers and switches. Direct infringement by Infineon's customers and/or end-users occurs at least by the use of the Accused Products, including at least the HYPERFLASH products, including use of consumer products incorporating them.

145. On information and belief, Infineon supplies hardware, firmware, and/or software that are especially made or especially adapted to practice the inventions claimed in the '381 Patent, including at least Claim 1, to induce third parties, including for example Infineon's customers and/or end-users of the Accused Products, including at least the HYPERFLASH products, to use such products in a manner that would infringe one or more of the claims of the '381 Patent, including at least Claim 1.

146. On information and belief, Infineon markets and advertises the Accused Products, including at least the HYPERFLASH, including on its website, to induce third parties, including

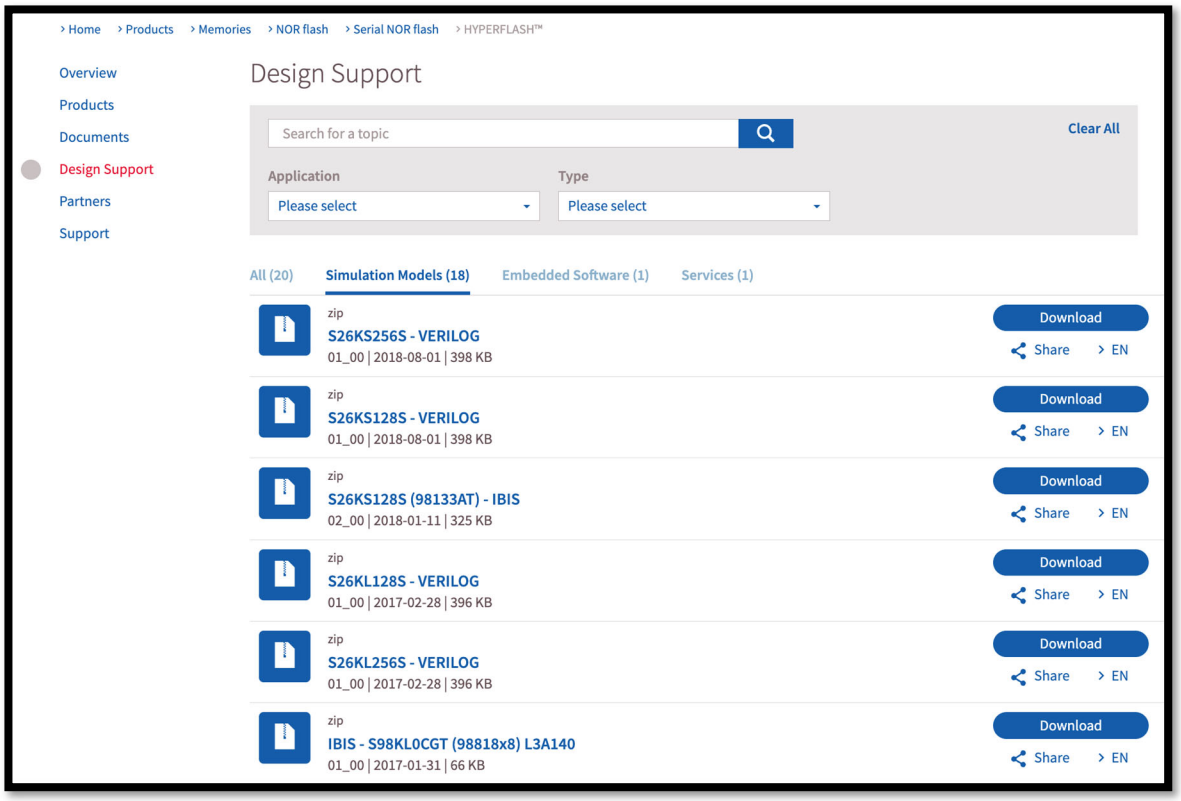
Infineon's customers and/or end-users, to use the products in a manner that would infringe one or more claims of the '381 Patent, including at least Claim 1. *See, e.g.*, https://www.infineon.com/cms/en/product/memories/nor-flash/serial-nor-flash/hyperflash.

147. On information and belief, Infineon furnishes instructive materials, technical support, and information concerning the operation and use of the Accused Products, including at least the HYPERFLASH, to induce third parties, including Infineon's customers and/or end-users, to use the products in a manner that would infringe one or more claims of the '381 Patent, including at least Claim 1. For example, on its website, Infineon furnishes at least product selection guides, product briefs, product family overviews, data sheets, application notes (including programmer's guides), and additional product and technical information:

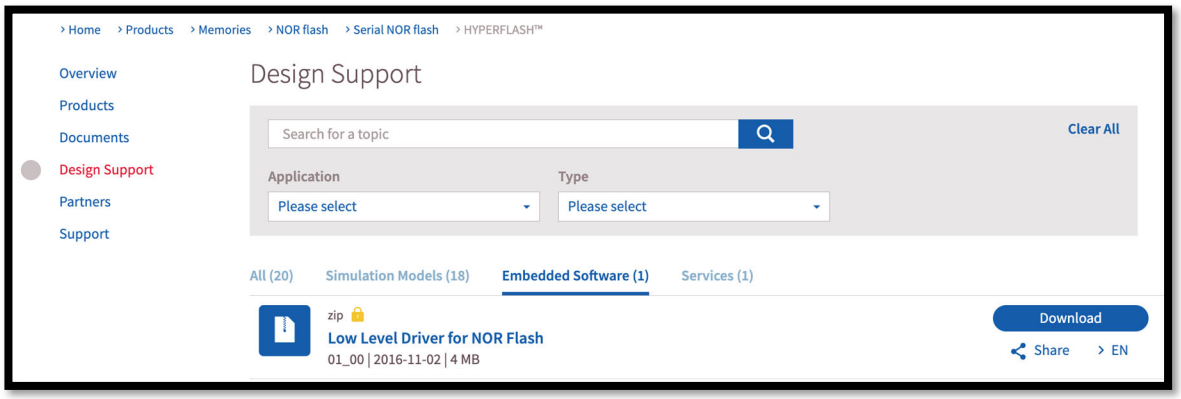


(Exemplary categories of instructive materials provided for the HYPERFLASH products.)

148. On its website, Infineon also furnishes design support materials, including simulation models and drivers, for the Accused Products, including at least the HYPERFLASH products:

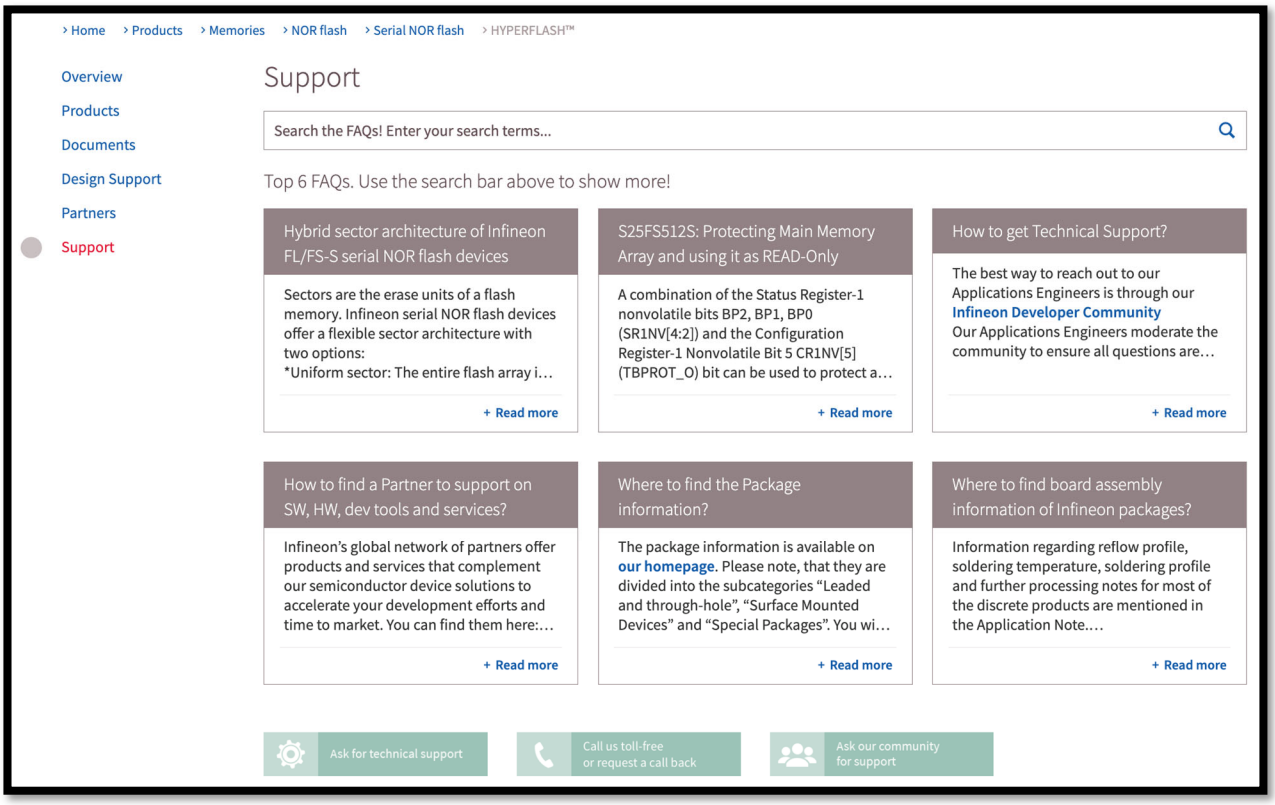


(HYPERFLASH Design Support, Simulation Models.)

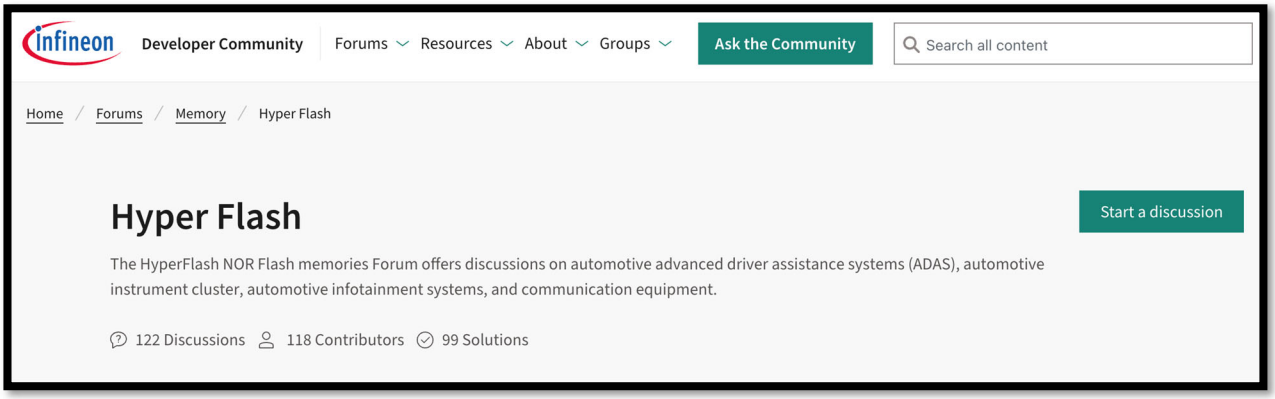


(HYPERFLASH Design Support, Driver.)

149. In addition, on its website, Infineon provides support/training materials and help from Infineon support engineers:



(Exemplary Support Materials for HYPERFLASH.)



(Infineon Developer Community for HYPERFLASH.)

150. Infineon knew or should have known of the '381 Patent and its infringement through a series of correspondence and meetings expressly notifying Infineon of the '381 Patent and Infineon's infringement thereof. As a result, Infineon knew or should have known it infringed one or more of the claims of the '381 Patent, including at least Claim 1, at least as early as

February 27, 2019, when MOSAID provided actual notice of infringement during ongoing discussions with Cypress.

151. Alternatively, Infineon knew or should have known of the ’381 Patent and its infringement no later than April 2020, when Infineon acquired Cypress and continued discussions with MOSAID regarding the ’381 Patent and Infineon’s infringement thereof.

152. At a minimum, both Infineon Defendants have had actual knowledge of the ’381 Patent, and their infringement thereof, at least as of the date of filing of this Complaint.

153. Despite this knowledge, Infineon has continued to induce third parties, including Infineon’s customers and/or end-users of the Accused Products, including at least the HYPERFLASH products, to infringe one or more claims of the ’381 Patent, including at least Claim 1, with the specific intent to cause infringement. Infineon knew or should have known that those acts would induce actual infringement by third parties, including Infineon’s customers and/or end-users of the Accused Products, including at least the HYPERFLASH products, of one or more of the claims of the ’381 Patent, including at least Claim 1.

154. Therefore, Infineon has induced infringement by others of one or more of the claims of the ’381 Patent, including at least Claim 1, with the specific intent to induce acts that constitute infringement of the ’381 Patent and with knowledge that such acts infringe one or more claims of the ’381 Patent, including at least Claim 1.

155. In violation of 35 U.S.C. § 271(c), Infineon is and has been infringing one or more of the claims of the ’381 Patent, including at least Claim 1, indirectly by contributing to infringement by third parties, including for example Infineon’s customers and/or end-users of the Accused Products, including at least the HYPERFLASH products, in this District and elsewhere in the United States. Direct infringement by Infineon’s customers and/or end-users occurs at least

by the use of the Accused Products, including at least the HYPERFLASH products, including use of consumer products incorporating them.

156. On information and belief, Infineon made and sold hardware, firmware, and/or software components (*e.g.*, processors and/or software drivers) especially made or especially adapted to practice the invention claimed in the ’381 Patent, including at least Claim 1. For example, as explained above, Infineon made and sold HYPERFLASH memory hardware and accompanying driver code. On information and belief, such hardware, firmware, and/or software components (i) are a material part of the invention and (ii) are not staple articles or commodities of commerce suitable for substantial non-infringing use at least because they are specifically designed to perform the claimed functionality. Any other use of such hardware, firmware, and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

157. Therefore, Infineon has contributed to the infringement by others of one or more of the claims of the ’381 Patent, including at least Claim 1.

158. Infineon’s infringement of one or more of the claims of the ’381 Patent, including at least Claim 1, has been, and continues to be, willful.

159. As explained above, Infineon had actual knowledge of the ’381 Patent and its infringement thereof at least as early as February 27, 2019, when MOSAID provided actual notice of infringement during discussions with Cypress regarding the ’381 Patent, and in any event no later than April 2020, when Infineon acquired Cypress and continued discussions with MOSAID.

160. As explained above, on several occasions beginning at least as early as February 27, 2019, MOSAID notified Infineon (including Cypress) of the ’381 Patent and Infineon’s infringement thereof, including infringement of at least Claim 1.

161. Despite knowing of the ’381 Patent at least as early as February 27, 2019 (and no later than April 2020), Infineon did not cease its infringing activities. Infineon has continued to infringe one or more claims of the ’381 Patent, including at least Claim 1, in disregard of MOSAID’s patent rights. As a result, Infineon deliberately and intentionally infringed the ’381 Patent, and continues to do so, after receiving express and actual knowledge of both the ’381 Patent and its infringement thereof.

162. Therefore, Infineon’s infringement of the ’381 Patent, including at least Claim 1, has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

COUNT III: INFRINGEMENT OF THE ’028 PATENT

163. MOSAID incorporates by reference and realleges paragraphs 1 through 162 as if specifically set forth herein.

164. In violation of 35 U.S.C. § 271(a), Infineon is and has been directly infringing one or more of the claims of the ’028 Patent, including at least Claim 1, either literally and/or under the doctrine of equivalents, by making, using, selling, and/or offering for sale in the United States, and/or importing into the United States, without authority, at least one of the Accused Products.

165. Claim 1 of the ’028 Patent recites:

> 1. A configurable non-volatile memory device comprising:
>
> plurality of non-volatile memory blocks;
>
> a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device;
>
> a first clock input port configured to receive a first clock input signal;

a second clock input port configured to receive a second clock input signal, the second clock input signal being complementary to the first clock input signal;

a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal;

one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data, the input data to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data, and the output data to be retrievable from the one of the plurality of non-volatile memory blocks;

a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration, the differential signaling configuration for utilizing the first clock input signal and the second clock input signal as differential signals, and the single ended signaling configuration for utilizing one of the first clock input signal and the second clock input signal as a single ended signal; and

one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks, the output data synchronized with the clock output signal in a double data rate configuration.

166. The Accused Products, including at least the SEMPER Flash products, practice each element of Claim 1 of the ’028 Patent.

167. The Accused Products comprise a configurable non-volatile memory device. For example, the SEMPER Flash products are configurable flash memory products.

168. The Accused Products include a plurality of non-volatile memory blocks. For example, the SEMPER Flash products include a main flash array divided into units or physical sectors.

169. The Accused Products include a chip enable port configured to receive a chip enable signal for enabling the configurable non-volatile memory device. For example, the SEMPER Flash products include a Chip Select ("CS#") signal, and driving the CS# signal "Low" enables the device.

170. The Accused Products include a first clock input port configured to receive a first clock input signal. For example, the SEMPER Flash products include a Clock ("CK") input.

171. The Accused Products include a second clock input port configured to receive a second clock input signal, the second clock input signal being complementary to the first clock input signal. For example, the SEMPER Flash products include a Clock ("CK#") input. As shown below, the CK and CK# clocks can be used for differential signaling:

256Mb/512Mb/1Gb SEMPER™ Flash
HYPERBUS™ interface, 1.8V/3.0V

Interface overview

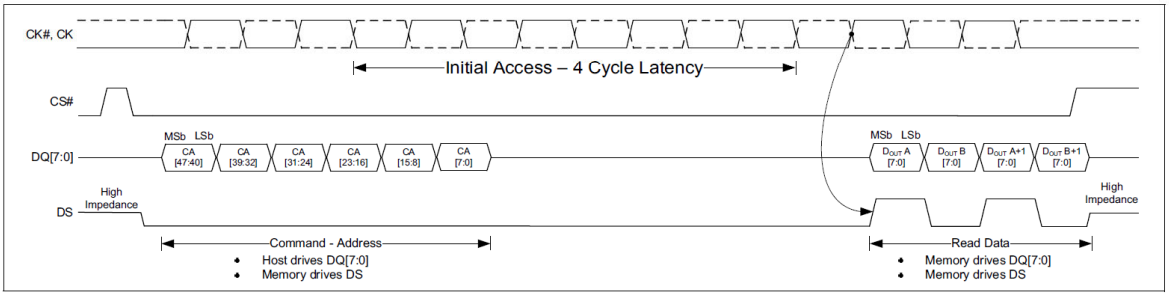


Figure 3 **Read operation (single initial latency)**[4, 5, 6, 7, 8]

(Infineon 256Mb/512Mb/1Gb SEMPER Flash Datasheet, at 12.)

172. The Accused Products include a clock output port configured to transfer a clock output signal, wherein the clock output signal is referenced to the first clock input signal. For example, the SEMPER Flash products include a Data Strobe ("DS") output clock signal that is referenced to the first clock input signal:

256Mb/512Mb/1Gb SEMPER™ Flash
HYPERBUS™ interface, 1.8V/3.0V

Interface overview

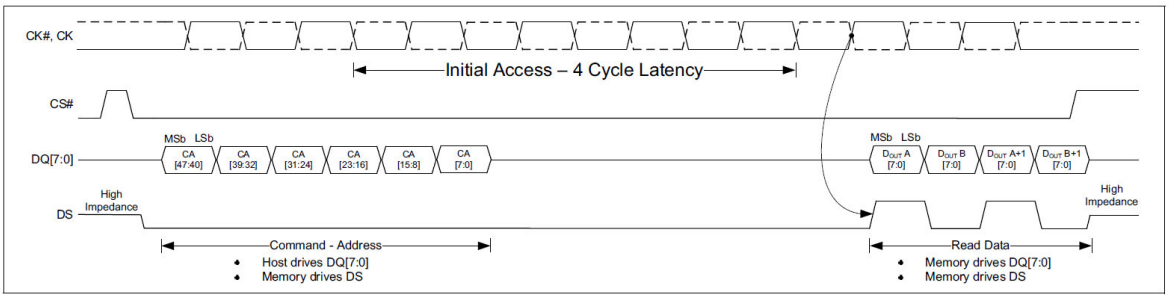


Figure 3 **Read operation (single initial latency)**[4, 5, 6, 7, 8]

(Infineon 256Mb/512Mb/1Gb SEMPER Flash Datasheet, at 12.)

173. The Accused Products include one or more common data ports configured to transfer common data signals carrying at least one of command data, address data, input data and output data. For example, the SEMPER Flash products include a DQ bus that can transfer command, address, and data information.

174. In the Accused Products, the input data is to be programmed into one of the plurality of non-volatile memory blocks accessible based on the command data and the address data. For example, the SEMPER Flash products perform write operations as shown below, where the DQ bus includes command/address data and write data:

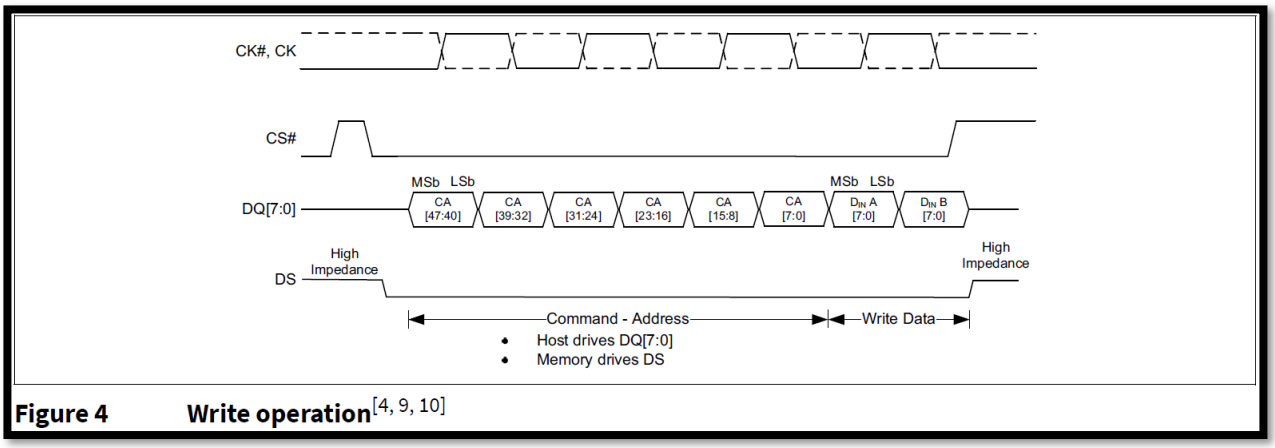


Figure 4 **Write operation**[4, 9, 10]

(Infineon 256Mb/512Mb/1Gb SEMPER Flash Datasheet, at 12.)

175. Further, in the Accused Products, the output data is to be retrievable from the one of the plurality of non-volatile memory blocks. For example, the SEMPER Flash products perform read operations as shown below:

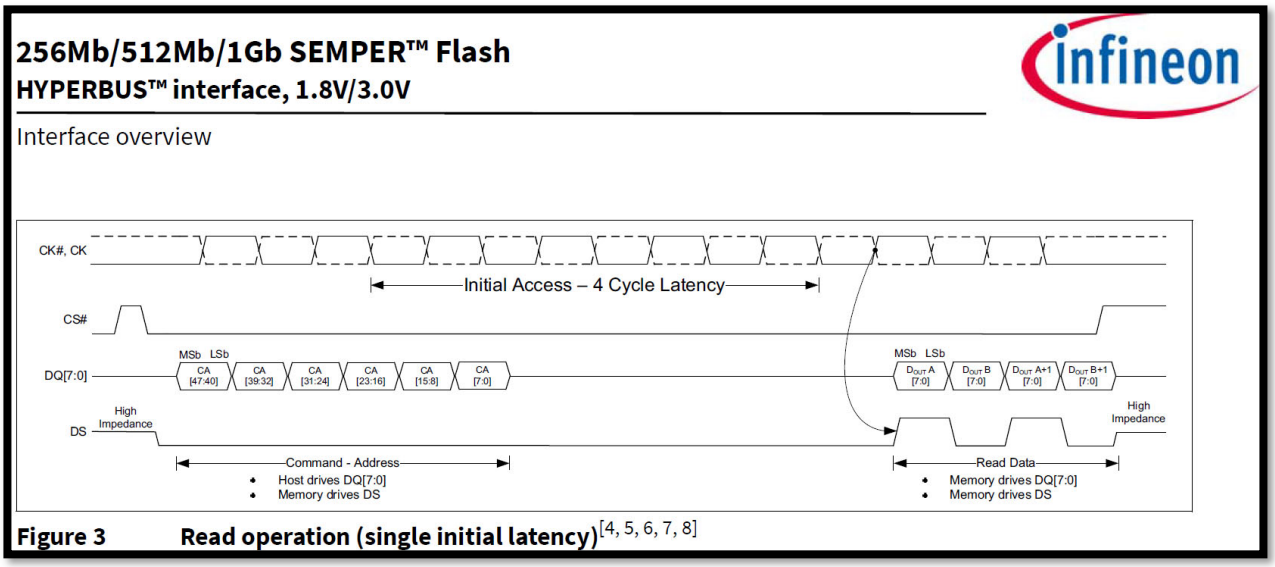


Figure 3 **Read operation (single initial latency)**[4, 5, 6, 7, 8]

(Infineon 256Mb/512Mb/1Gb SEMPER Flash Datasheet, at 12.)

176. The Accused Products include a configurable clock input buffer configurable to one of a single ended signaling configuration and a differential signaling configuration. For example, the SEMPER Flash products include a clock configuration register allowing selection of single ended and differential signaling.

177. In the Accused Products, the differential signaling configuration is for utilizing the first clock input signal and the second clock input signal as differential signals. For example, in the differential signaling configuration for the SEMPER Flash products, the CK and CK# signals are used as differential signals.

178. Further, in the Accused Products, the single ended signaling configuration is for utilizing one of the first clock input signal and the second clock input signal as a single ended signal. For example, in the single ended signaling configuration of the SEMPER Flash products, the CK signal is used as a single ended signal.

179. The Accused Products include one or more configurable output buffers configurable to one of a plurality of output buffer drive strengths to transfer the output data retrieved from the one of the plurality of non-volatile memory blocks. For example, the SEMPER Flash products include a configuration register allowing for selection of one of a plurality of I/O driver output impedances or drive strengths.

180. In the Accused Products, the output data is synchronized with the clock output signal in a double data rate configuration. For example, in the SEMPER Flash products, the read data is synchronized with the DS clock output signal as shown below:

256Mb/512Mb/1Gb SEMPER™ Flash
HYPERBUS™ interface, 1.8V/3.0V

Interface overview

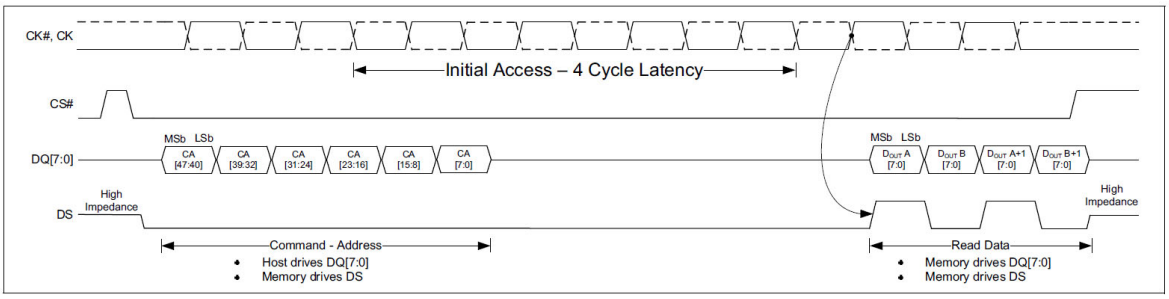


Figure 3 **Read operation (single initial latency)**[4, 5, 6, 7, 8]

(Infineon 256Mb/512Mb/1Gb SEMPER Flash Datasheet, at 12.)

181. During license discussions, MOSAID provided Infineon with exemplary claim charts explaining in detail Infineon's infringement of the '028 Patent, including at least Claim 1.

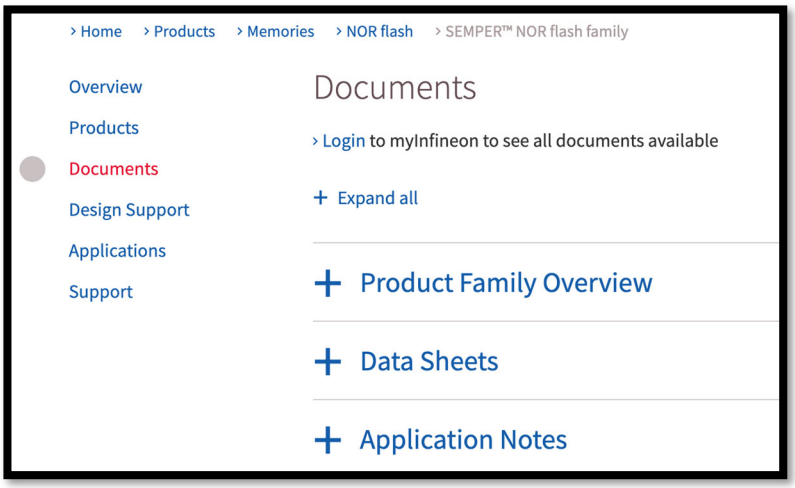
182. In violation of 35 U.S.C. § 271(b), Infineon is and has been infringing one or more of the claims of the '028 Patent, including at least Claim 1, indirectly by inducing infringement by third parties, including for example Infineon's customers and/or end-users of the Accused Products, including at least the SEMPER Flash products, in this District and elsewhere in the United States. For example, on information and belief, at least the SEMPER Flash products have been and are being used by Infineon's customers and/or end-users in consumer products, including in automotive, industrial, communications, and data center applications. Direct infringement by Infineon's customers and/or end-users occurs at least by the use of the Accused Products, including at least the SEMPER Flash products, including use of consumer products incorporating them.

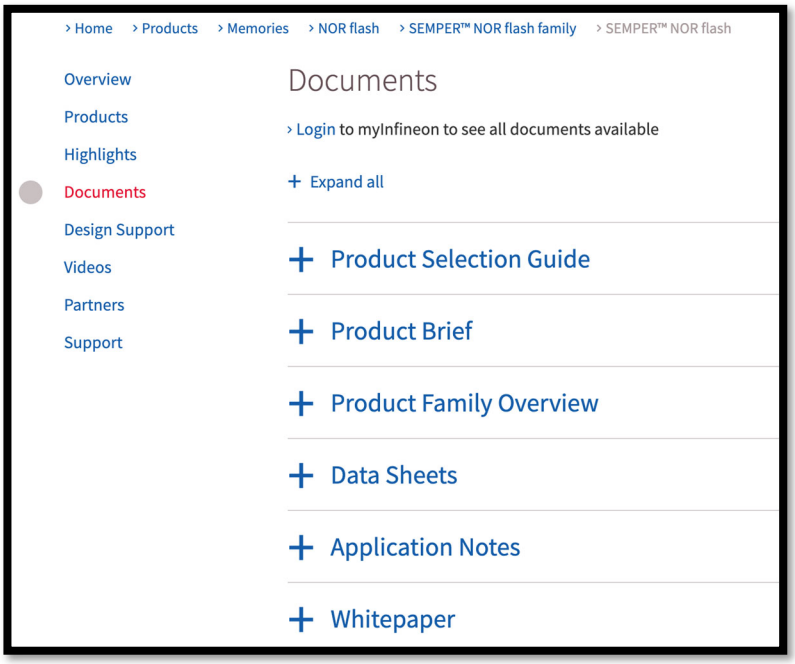
183. On information and belief, Infineon supplies hardware, firmware, and/or software that are especially made or especially adapted to practice the inventions claimed in the '028 Patent, including at least Claim 1, to induce third parties, including for example Infineon's customers

and/or end-users of the Accused Products, including at least the SEMPER Flash products, to use such products in a manner that would infringe one or more claims of the ’028 Patent, including at least Claim 1.

184. On information and belief, Infineon markets and advertises the Accused Products, including at least the SEMPER Flash products, including on its website, to induce third parties, including Infineon’s customers and/or end-users, to use the products in a manner that would infringe one or more claims of the ’028 Patent, including at least Claim 1. *See, e.g.*, https://www.infineon.com/cms/en/product/memories/nor-flash/semper-nor-flash-family.

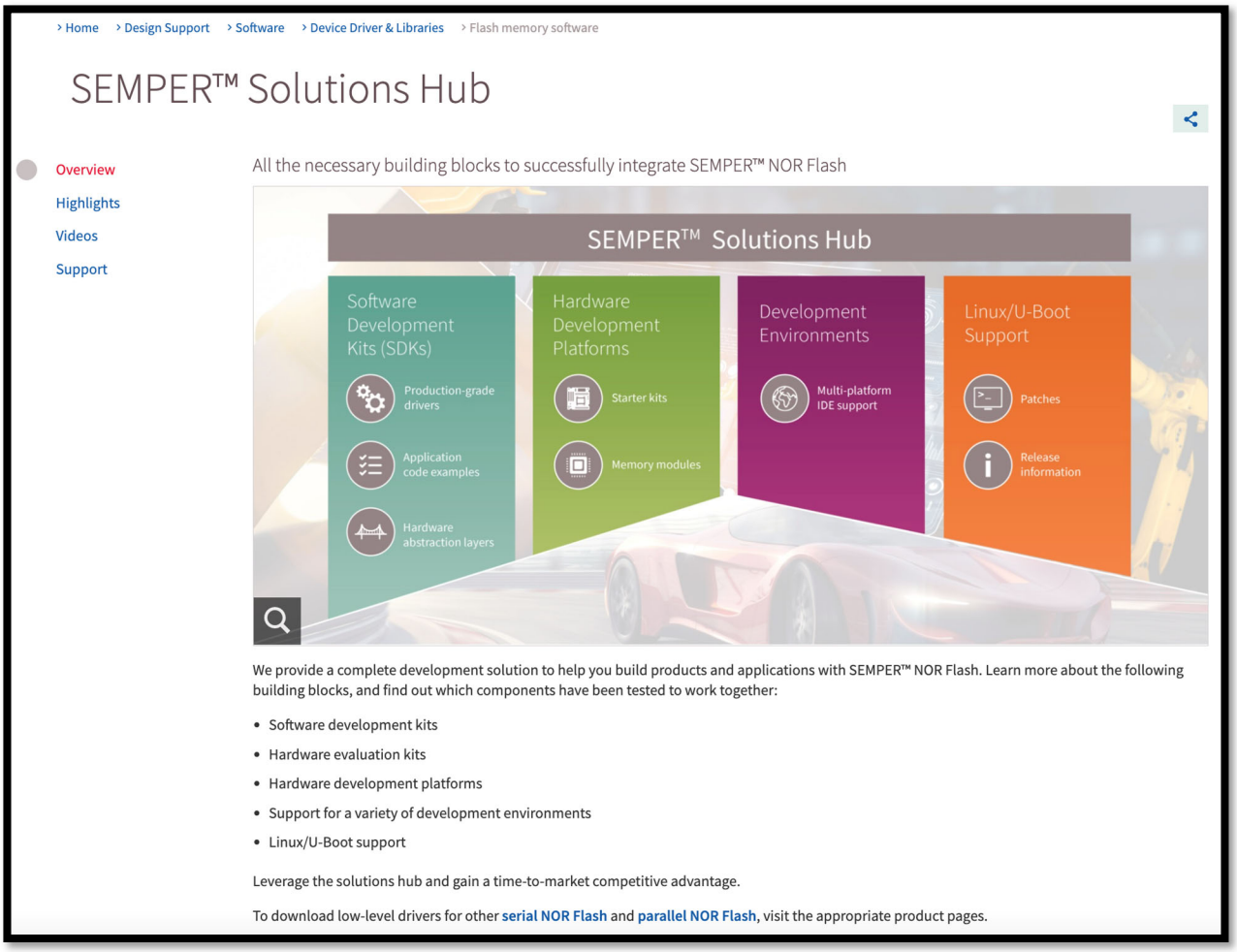
185. On information and belief, Infineon furnishes instructive materials, technical support, and information concerning the operation and use of the Accused Products, including at least the SEMPER Flash products, to induce third parties, including Infineon’s customers and/or end-users, to use the products in a manner that would infringe one or more claims of the ’028 Patent, including at least Claim 1. For example, on its website, Infineon furnishes at least product selection guides, product briefs, product family overviews, data sheets, application notes (including programmer’s guides), and whitepapers:





(Exemplary categories of instructive materials provided for the SEMPER Flash products.)

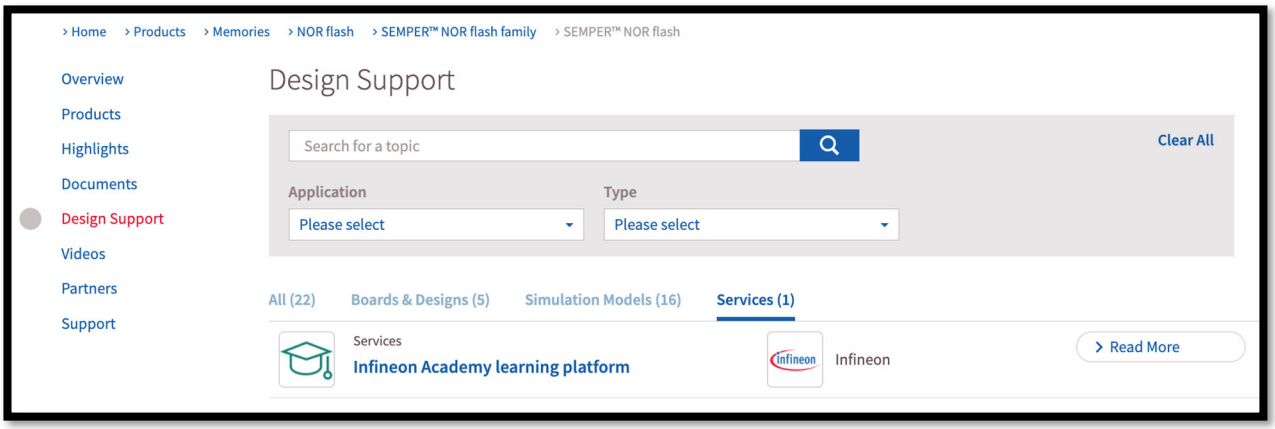
186. On its website, Infineon also provides the SEMPER Solutions Hub, which furnishes software development kits (including production-grade drivers, application code examples, and hardware abstraction layers); hardware development platforms (including starter kits and memory modules); development environments (including multi-platform IDE support); and Linux/U-Boot support (including patches and release information):



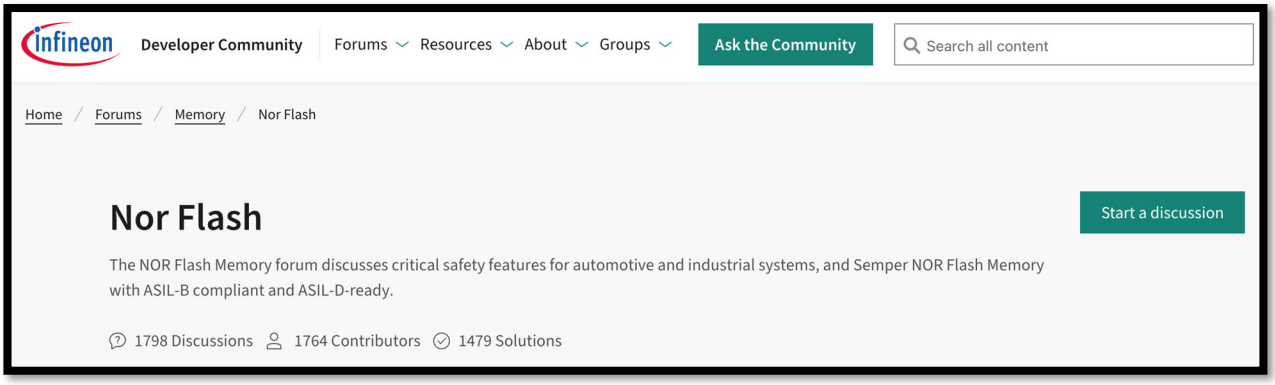
(SEMPER™ Solutions Hub.)

187. With the SEMPER Solutions Hub, Infineon provides a complete development solution to help its customers build products and applications with SEMPER NOR Flash.

188. In addition, on its website, Infineon provides learning materials and help from Infineon support engineers:



(Link to Infineon Academy learning platform for SEMPER Flash.)



(Infineon Developer Community for NOR Flash, including SEMPER NOR Flash Memory.)

189. Infineon knew or should have known of the ’028 Patent and its infringement through a series of correspondence and meetings expressly notifying Infineon of the ’028 Patent and Infineon’s infringement thereof. As a result, Infineon knew or should have known it infringed one or more claims of the ’028 Patent, including at least Claim 1, at least as early as February 21, 2020, when MOSAID provided actual notice of infringement during ongoing discussions with Cypress.

190. Alternatively, Infineon knew or should have known of the ’028 Patent and its infringement no later than April 2020, when Infineon acquired Cypress and continued discussions with MOSAID regarding the ’028 Patent and Infineon’s infringement thereof.

191. At a minimum, both Infineon Defendants have had actual knowledge of the ’028 Patent, and their infringement thereof, at least as of the date of filing of this Complaint.

192. Despite this knowledge, Infineon has continued to induce third parties, including Infineon’s customers and/or end-users of the Accused Products, including at least the SEMPER Flash products, to infringe one or more claims of the ’028 Patent, including at least Claim 1, with the specific intent to cause infringement. Infineon knew or should have known that those acts would induce actual infringement by third parties, including Infineon’s customers and/or end-users of at least one of the Accused Products, including at least the SEMPER Flash products, of one or more of the claims of the ’028 Patent, including at least Claim 1.

193. Therefore, Infineon has induced infringement by others of one or more of the claims of the ’028 Patent, including at least Claim 1, with the specific intent to induce acts that constitute infringement of the ’028 Patent and with knowledge that such acts infringe one or more claims of the ’028 Patent, including at least Claim 1.

194. In violation of 35 U.S.C. § 271(c), Infineon is and has been infringing one or more of the claims of the ’028 Patent, including at least Claim 1, indirectly by contributing to infringement by third parties, including for example Infineon’s customers and/or end-users of the Accused Products, including at least the SEMPER Flash products, in this District and elsewhere in the United States. Direct infringement by Infineon’s customers and/or end-users occurs at least by the use of the Accused Products, including at least the SEMPER Flash products, including use of consumer products incorporating them.

195. On information and belief, Infineon made and sold hardware, firmware, and/or software components (*e.g.*, processors and/or software drivers) especially made or especially adapted to practice the invention claimed in the ’028 Patent, including at least Claim 1. For

example, as explained above, Infineon made and sold SEMPER Flash memory hardware and accompanying software, including production-grade drivers and application code examples. On information and belief, such hardware, firmware, and/or software components (i) are a material part of the invention and (ii) are not staple articles or commodities of commerce suitable for substantial non-infringing use at least because they are specifically designed to perform the claimed functionality. Any other use of such hardware, firmware, and/or software would be unusual, far-fetched, illusory, impractical, occasional, aberrant, or experimental.

196. Therefore, Infineon has contributed to the infringement by others of one or more of the claims of the ’028 Patent, including at least Claim 1.

197. Infineon’s infringement of one or more claims of the ’028 Patent, including at least Claim 1, has been, and continues to be, willful.

198. As explained above, Infineon had actual knowledge of the ’028 Patent and its infringement thereof at least as early as February 21, 2020, when MOSAID began discussions with Cypress regarding the ’028 Patent, and in any event no later than April 2020, when Infineon acquired Cypress and continued discussions with MOSAID.

199. As explained above, on several occasions beginning at least as early as February 21, 2020, MOSAID notified Infineon (including Cypress) of the ’028 Patent and Infineon’s infringement thereof, including infringement of at least Claim 1.

200. Despite knowing of the ’028 Patent at least as early as February 21, 2020 (and no later than April 2020), Infineon did not cease its infringing activities. Infineon has continued to infringe one or more claims of the ’028 Patent, including at least Claim 1, in disregard of MOSAID’s patent rights. As a result, Infineon deliberately and intentionally infringed the

’028 Patent, and continues to do so, after receiving express and actual knowledge of both the ’028 Patent and its infringement thereof.

201. Therefore, Infineon’s infringement of the ’028 Patent, including at least Claim 1, has been and continues to be willful, wanton, malicious, in bad faith, deliberate, consciously wrongful, flagrant, or characteristic of a pirate, entitling MOSAID to increased damages pursuant to 35 U.S.C. § 284 and to attorneys’ fees and costs incurred in prosecuting this action pursuant to 35 U.S.C. § 285.

DAMAGES

202. Defendants’ acts of infringement have caused damages to MOSAID, and MOSAID is entitled to recover the damages it has sustained as a result of Defendants’ wrongful acts in an amount to be determined at trial.

203. MOSAID is entitled to, and now seeks to, recover damages in an amount not less than the maximum amount permitted by law caused by Defendants’ acts of infringement.

204. As a result of Defendants’ acts of infringement, MOSAID has suffered actual and consequential damages. To the fullest extent permitted by law, MOSAID seeks recovery of damages in an amount to compensate for Defendants’ infringement. MOSAID further seeks any other damages to which MOSAID would be entitled to in law or in equity.

INJUNCTIVE RELIEF

205. Defendants’ acts of infringement have caused—and unless restrained and enjoined, Defendants’ acts of infringement will continue to cause—irreparable injury and damage to MOSAID for which MOSAID has no adequate remedy at law. Unless enjoined by this Court, Defendants will continue to infringe the claims of the Asserted Patents.

ATTORNEYS' FEES

206. MOSAID is entitled to recover reasonable and necessary attorneys' fees under applicable law.

DEMAND FOR JURY TRIAL

207. Pursuant to Rule 38 of the Federal Rules of Civil Procedure, MOSAID demands a trial by jury on all issues so triable.

PRAYER FOR RELIEF

WHEREFORE, MOSAID prays for judgment and requests that the Court find in its favor and against Defendants. MOSAID respectfully requests that the Court enter preliminary and final orders, declarations, and judgments against Defendants as are necessary to provide MOSAID with the following relief:

a. A judgment that Defendants have infringed and/or are infringing one or more claims of the Asserted Patents, literally or under the doctrine of equivalents, as alleged above;

b. A judgment that Defendants have infringed and/or are infringing one or more claims of the Asserted Patents, directly, as alleged above;

c. A judgment that Defendants have infringed and/or are infringing one or more claims of the Asserted Patents, indirectly, as alleged above;

d. A judgment that Defendants' infringement of the claims of the Asserted Patents has been willful;

e. An award for all damages and costs arising out of Defendants' infringement, to adequately compensate MOSAID for Defendants' infringement of the Asserted Patents, but in no event less than a reasonable royalty, including supplemental damages for any

continuing post-verdict infringement up until entry of the final judgment, with an accounting, as needed;

f. Pre-judgment and post-judgment interest, jointly and severally, in an amount according to proof;

g. Treble damages based on Defendants' willful infringement;

h. An accounting of damages and any future compensation due to MOSAID for Defendants' infringement (past, present, or future) not specifically accounted for in a damages award (or other relief), and/or permanent injunctive relief;

i. A judgment that this case is exceptional and an award of reasonable attorneys' fees as provided by 35 U.S.C. § 285 and enhanced damages as provided by 35 U.S.C. § 284;

j. An award of costs of suit;

k. The entry of an order enjoining and restraining Defendants and their parents, affiliates, subsidiaries, officers, agents, servants, employees, attorneys, successors, and assigns and all persons in active concert or participation therewith, from making, importing, using, offering for sale, selling, or causing to be sold any product falling within the scope of any claim of the Asserted Patents, or otherwise infringing or inducing infringement of any claim of the Asserted Patents; and

l. All further relief in law or in equity as the Court may deem just and proper.

Dated: March 25, 2025

Respectfully submitted,

/s/ Jamie H. McDole

Max Ciccarelli (SBN 00787242)
CICCARELLI LAW FIRM
100 N 6th Street, Suite 503
Waco, Texas 76701
Telephone: 214-444-8869
Email: max@ciccarellilawfirm.com

Jamie H. McDole (SBN 24082049)
Lead Counsel
Phillip B. Philbin (SBN 15909020)
Michael D. Karson (SBN 24090198)
Miranda Y. Jones (SBN 24065519)
David W. Higer (SBN 24127850)
David A. Neal (SBN 24144868)
Cody M. Carter (SBN 24131091)
Matthew L. Vitale (SBN 24137699)
WINSTEAD PC
2728 N. Harwood Street, Suite 500
Dallas, Texas 75201
Tel.: (214) 745-5400
Fax: (214) 745-5390
Email: jmcdole@winstead.com
pphilbin@winstead.com
mkarson@winstead.com
mjones@winstead.com
dhiger@winstead.com
dneal@winstead.com
ccarter@winstead.com
mvitale@winstead.com

Nadia E. Haghighatian (SBN 24087652)
Austin C. Teng (SBN 24093247)
Daniel S. Shuminer (SBN 24124688)
WINSTEAD PC
600 W. 5th Street, Suite 900
Austin, Texas 78701
Tel.: (512) 370-2800
Fax: (512) 370-2850
Email: ateng@winstead.com
nhaghighatian@winstead.com
dshuminer@winstead.com

Attorneys for Plaintiff
MOSAID Technologies Inc.