

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INFINEON TECHNOLOGIES AMERICAS CORP.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

Case IPR2025-01487
Patent 9,972,381

PATENT OWNER RESPONSE

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PATENT OWNER'S EXHIBIT LIST

Exhibit	Description
2001	Lowenstein Declaration In Support of Notice of Intent
2002	Woo Declaration In Support of Notice of Intent
2003	Courtney Declaration In Support of Notice of Intent
2004	Complaint in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D Tex.), Dkt. 1 (Mar. 25, 2025) [Complaint]
2005	November 3, 2017 Notice Letter to Cypress Semiconductor Corporation [11/03/17 Letter] (CONFIDENTIAL)
2006	First Amended Scheduling Order in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.), Dkt. 43 (Oct. 17, 2025) [Amended-Scheduling-Order]
2007	Defendant's Opening Claim Construction Brief in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.), Dkt. 44 (Oct. 27, 2025) [Opening-Claim-Construction-Brief]
2008	Defendants' Election of Asserted Prior Art Grounds in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.) (served Nov. 3, 2025) [Election-of-Grounds]
2009	<i>Reserved</i>
2010	<i>Reserved</i>
2011	<i>Reserved</i>
2012	Declaration of Boris Teksler [Teksler-Decl.] (CONFIDENTIAL)
2013	Press Release, Infineon Technologies AG Completes Acquisition Of Cypress Semiconductor Corporation (Apr. 16, 2020) [Press-Release-Cypress]

Exhibit	Description
2014	Letter from Cypress (May 5, 2019) [05/05/19 Letter] (CONFIDENTIAL)
2015	Email from Conversant (Feb. 27, 2019) [02/27/19 Letter] (CONFIDENTIAL)
2016	Conversant Presentation (Oct. 2018) [10/18 Presentation] (CONFIDENTIAL)
2017	Conversant Response Presentation (June 11, 2019) [06/11/19 Conversant Response Presentation] (CONFIDENTIAL)
2018	Cypress Response Letter (Oct. 11, 2019) [10/11/19 Cypress Response Letter] (CONFIDENTIAL)
2019	Conversant Response Presentation (Dec. 4, 2019) [12/04/19 Conversant Response Presentation] (CONFIDENTIAL)
2020	Cypress Response Letter (Mar. 6, 2020) [03/06/20 Cypress Response Letter] (CONFIDENTIAL)
2021	Cypress Response Letter (Sept. 9, 2020) [09/09/20 Conversant Patents] (CONFIDENTIAL)
2022	MOSAID – Infineon/Cypress Presentation (February 28, 2023) [02/28/23 MOSAID-Infineon/Cypress Presentation] (CONFIDENTIAL)
2023	Email chain (April 14, 2023) [4/14/23 Email] (CONFIDENTIAL)
2024	[11/06/23 Cypress Response] (CONFIDENTIAL)
2025	Infineon’s Preliminary Invalidity Contentions in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00436 (W.D. Tex.) (served Aug. 15, 2025) [Invalidity-Contentions]
2026	Declaration and CV of Sunil P. Khatri, Ph.D.
2027	Declaration and CV of Steven Przybylski, Ph.D.

Exhibit	Description
2028	Transcript of Deposition of Carl Sechen, Ph.D.
2029	JESD79-2 DDR2 SDRAM Standard (dated September 2003)

All emphasis in quotations is added unless otherwise stated.

I. INTRODUCTION

Petitioner’s sole ground rests on a purported Grundy-Kilbuck combination. But the Petition never identifies a single, coherent “Grundy-Kilbuck” device. Instead, Petitioner treats Grundy as a general platform and invokes Kilbuck—often “to the extent” needed—for selected claim features, without explaining what the resulting device is, how it is structured, or how Grundy’s controllers and devices and Kilbuck’s flash-specific circuitry are integrated into one flash memory device. Such analysis leaves no defined combination against which obviousness, motivation, or reasonable expectation of success can be assessed. *See* Section II.

Petitioner’s dependent-claim challenges compound these failures of proof. For claims 4, 5, and 19, Petitioner proposed in district court that “clock output signal” means “a periodic signal that synchronizes system operations,” and the Director has bound Petitioner to that construction in this proceeding. The Petition never applies that construction, and thus cannot show that Grundy’s alleged clock output signal “synchronizes system operations.” Indeed, the Petition does not address what Petitioner even means by “synchroniz[ing] system operations.” Petitioner cannot cure this omission now. *See* Section III.

For dependent claim 2, Petitioner likewise fails to prove a timing limitation specifically requiring “the command data” to be latched “*at the first* rising edge of the clock signal after the transition of the control signal.” Petitioner does not

consistently identify the claimed “command data.” Petitioner also relies on Grundy’s Figure 6 to establish aspects of timing, although Figure 6 depicts the timing of transmissions by Grundy’s memory controller, not the timing of any latching of data by any memory device. Petitioner also relies on a “logic level clock signal” that is not the same “clock signal” that it identified in connection with claim 1, and never proves the required timing relationship. *See* Section IV.

For claims 13 and 21, Petitioner again pieces together embodiments that are not reconciled with its independent-claim mappings. Petitioner relies on Grundy’s Figure 4A and Kilbuck’s Figures 3A/3B to suggest overlapping read and page-program operations, when these embodiments were not the basis for Petitioner’s independent-claim mapping. Petitioner never identifies a coherent combination in which the same claimed flash memory device, operations, and control circuitry mapped for claims 1 and 17 satisfy the required limitations. Nor does Petitioner provide a reasoned motivation to make the undefined modifications its theory would require. *See* Section V.

Because Petitioner’s asserted ground is built on an undefined combination and unsupported dependent-claim mappings, Petitioner has failed to meet its burden. The patentability of all challenged claims should be confirmed.

II. PETITIONER FAILS TO SHOW A MOTIVATION TO COMBINE WITH A REASONABLE EXPECTATION OF SUCCESS (ALL CLAIMS).

The Petition's sole ground asserts that the challenged claims are obvious over a purported combination of Grundy and Kilbuck. At a high level, Petitioner contends that a POSITA would have applied Kilbuck's flash-memory teachings to Grundy's system to achieve "predictable results." *See, e.g.,* Pet., 15-16. But that high-level formulation is never translated into a defined combination. Instead, Petitioner advances a shifting, limitation-by-limitation theory in which Grundy is treated as a general starting point and Kilbuck is repeatedly invoked, "to the extent" needed, to supply whatever features Grundy is alleged not to disclose. *See, e.g.,* Pet., 20-22, 37, 39, 41, 46, 73. Petitioner thus presents a series of conditional substitutions untethered to any single, coherent configuration.

That failure is dispositive. An obviousness theory must identify a specific combination of prior art and provide a "clear[] explan[ation]" of "how the combination of the two references was supposed to work." *PersonalWeb Techs. LLC v. Apple, Inc.*, 848 F.3d 987, 994 (Fed. Cir. 2017). Here, because Petitioner never clearly defines a combination, there is no basis to assess whether the claimed limitations are satisfied, how the cited features operate together, or whether a POSITA would have been motivated to make the combination with a reasonable expectation of success. The claims require a single "flash memory device"

comprising the recited elements. But Petitioner never defines a single “Grundy-Kilbuck” system, Section II.A, never reconciles the embodiments it invokes, Section II.B, and never shows a non-hindsight-based motivation to combine or a reasonable expectation of success. *See* Section II.C.

A. Petitioner Fails To Identify A Coherent “Grundy-Kilbuck” Combination.

Petitioner does not present a defined “Grundy-Kilbuck” combination that is alleged to satisfy any claim. Instead, Petitioner proceeds on a conditional basis in which Kilbuck is invoked only “to the extent” that Grundy is asserted not to disclose a particular feature. Pet., 20-22, 37, 39, 41, 46, 73.

That approach is legally insufficient. *PersonalWeb*, 848 F.3d at 994. And “a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). A petitioner must therefore do more than identify disparate features across multiple disclosures—it must explain how those features are combined in a single system.

Petitioner does not identify such a combination. Instead, Petitioner repeatedly relies on conditional formulations under which each limitation is attributed to Grundy or, if Grundy is deemed insufficient, to Kilbuck. For example, Petitioner asserts:

- “To the extent that it is argued that Grundy does not teach or suggest [[1a]]¹ “a flash memory comprising a plurality of erasable blocks”], Kilbuck describes that flash memory includes a plurality of erasable blocks.” Pet., 20.
- “To the extent that it is argued that Grundy does not teach or suggest [[1a] “each erasable block comprising a plurality of pages”], Kilbuck does.” *Id.*, 21.
- “To the extent that it is argued that Grundy does not teach or suggest [[1a] “each page comprising a plurality of flash memory cells”], Kilbuck does.” *Id.*, 22.
- “To the extent that it is argued that Grundy does not teach or suggest [[1e] “execute a page program operation to store the input data on a selected page”], Kilbuck does.” *Id.*, 37.
- “To the extent that it is argued that Grundy does not teach or suggest [[1e] “execute a read operation to retrieve the output data from the flash memory cells in accordance to the command data and address

¹ Here and elsewhere Patent Owner uses Petitioner’s labeling of individual claim elements ([1a], [1b], etc.). See Pet., iv-vii.

data received at the at least one common data interface”], Kilbuck does.” *Id.*, 39.

- “To the extent that it is argued that Grundy does not teach or suggest [[1f] “a status register configured to indicate a status of the flash memory device”, Kilbuck does.” *Id.*, 41.
- “To the extent that it is argued that Grundy does not teach or suggest [[17f] “providing a read status command to access the status register and determine a status of the flash memory device”], Kilbuck does.” *Id.*, 46.
- “To the extent that it is argued that Grundy does not teach or suggest [[15] “[t]he flash memory device as claimed in claim 1, further comprising an error correcting code (ECC) configured to be utilized during the page program operation], Kilbuck does.” *Id.*, 73.

As this listing confirms, Petitioner applies a rote template: cite Grundy and invoke Kilbuck only as a fallback. The result shifts within and across limitations, and amounts to the “mere identification ... of individual components of claimed limitations,” which is legally insufficient. *In re Kotzab*, 217 F.3d 1365, 1371 (Fed. Cir. 2000); *see also Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016).

Nor does the Petition identify the differences between the claimed “flash

memory device” and any defined embodiment of Grundy, or set out the specific modifications that would be required to incorporate Kilbuck’s teachings into such an embodiment, as required under § 103 and *Graham*. *See also* Section II.C.2. Instead, even assuming *arguendo* that Petitioner has correctly identified where individual features appear in Grundy or Kilbuck, those disparate disclosures do not specify a “Grundy-Kilbuck” combination. Petitioner’s treatment of the “double data rate” limitation [1c-ii], Pet., 28-30, illustrates the same defect, even within Grundy alone. Here Petitioner relies on Grundy’s paragraph 88, which states that “double-data rate capture” is achieved by providing one set of storage elements to capture receiver outputs on rising edges and a second set to capture receiver outputs on falling edges. Pet., 29-30 (quoting Ex. 1005 [Grundy] [0088]). A POSITA would recognize this second set of outputs (which is not depicted in Figure 17) to be a **modification** of a device that is not itself already operating in the claimed double-data-rate configuration. Ex. 2027 [Przybylski-Decl.] ¶ 65-79. A POSITA would further understand that such a change is not self-contained: once the input register captures values on both clock edges, the downstream data path must be able to accept, order, buffer, decode, and route those values—implicating, at a minimum, the I/O controller of Grundy’s Figure 19, including its command buffer 351, input data buffer 353, select logic 357, output buffer 355, and associated protocol timing. *Id.*; *see also* Ex. 1005 [Grundy] [0090]-[0096]. And if—as Petitioner elsewhere

proposes for claims 4 and 19—the output of a Grundy device provides double-data-rate functionality, the Grundy’s output-side registering/buffering and driver circuitry would also have to be modified from their disclosed forms. *Cf.* Pet., 55-56. Petitioner never identifies any downstream modifications necessitated by the modification described in paragraph 88, never explains how the two-edge captured values are presented to Figure 19’s buffers and protocol engine, and never shows how any output-side path is to be modified as to produce double data rate output.

Because Petitioner never identifies a combination or explains how it operates, it provides no basis to evaluate how the claimed features are arranged or how any such system would function.

B. Petitioner’s Theory Varies From Limitation To Limitation And Never Identifies A Combination.

Petitioner’s failure to identify a coherent “Grundy-Kilbuck” combination is evident from the structure of its claim-by-claim analysis. Rather than map the limitations of claim 1 to a single, defined device, Petitioner proceeds on a limitation-by-limitation basis, invoking different disclosures—and, critically, different implementations—depending on the requirement at issue. Petitioner alternates between Grundy’s system-level controller, Grundy’s devices, and Kilbuck’s internal flash controller, without identifying how or whether all of these are part of the claimed “flash memory device.”

Claim 1’s preamble provides “a flash memory device comprising.” Petitioner,

however, never identifies what the claimed “flash memory device” is within its alleged “Grundy-Kilbuck” combination with clarity. Petitioner first points to “memory devices 107” in Grundy’s Figure 3 and “memory devices 155” from Grundy’s Figure 5A. Pet., 17-18. Then, as the claimed device is a *flash* memory device, Petitioner also cites to Kilbuck, which discloses flash memory devices with internal flash-specific circuitry. *See, e.g.*, Pet., 18 (citing Kilbuck for flash memory devices). But the Petition never explains whether the claimed “flash memory device” is (i) a Grundy memory device assumed to use flash, (ii) a Kilbuck flash memory device, or (iii) some modified Grundy device incorporating Kilbuck’s flash-memory teachings.² Nor does the Petition identify how any such device is structured or how it corresponds to claim 1 as a whole.

Limitation 1[a] next requires “a flash memory comprising a plurality of

² Petitioner’s expert stated that he “focused on” implementations of Grundy in which “all these memory devices were flash memory devices,” Ex. 2028 [Sechen-Tr.] 39:14–18, although he admitted that his motivation to combine opinion does not depend on how many devices were involved or whether individual devices were identical to one another. *Id.*, 40:12-41:9. He also “ha[d]n’t really considered the possibility” of whether “Grundy-Kilbuck” could involve devices that weren’t flash memory devices. *Id.*, 41:10–16.

erasable blocks, each erasable block comprising a plurality of pages, each page comprising a plurality of flash memory cells.” Petitioner again does not map this limitation to a single structure. Instead, Petitioner begins with Grundy’s generic disclosure of “semiconductor storage arrays” that may include “flash EEPROM,” Pet., 19-20 (citing Ex. 1005 [Grundy] [0035]), but repeatedly invokes Kilbuck “to the extent” Grundy is alleged not to disclose specific aspects of flash memory structure. *See, e.g.*, Pet., 20-22 (asserting that, “to the extent” Grundy does not disclose erasable blocks, pages, or flash memory cells, “Kilbuck does”). Under Petitioner’s approach, the claimed flash memory is not tied to any particular embodiment of Grundy, but instead is “defined” by selectively importing features from Kilbuck as needed. Petitioner never explains how the claimed “flash memory” resides within a Grundy memory device, or whether it corresponds to flash in Kilbuck’s flash memory device. Nor does Petitioner identify what modifications to Grundy would be required to implement aspects of Kilbuck’s implementation of flash memory. As a result, even for this foundational limitation, Petitioner presents a conditional mapping in which the structure of the alleged “flash memory” shifts depending on whether portions of Grundy are sufficient in themselves or need supplementation by Kilbuck.

Claim 1 further requires [1b] “a clock input port configured to receive a clock signal, [1c-i] “at least one common data interface configured to transfer command

data, address data, input data and output data,” [1c-ii] “wherein at least one of command data, address data, input data and output data is transferred in synchronization with both rising and falling edges of the clock signal when the flash memory device is in a double data rate configuration,” and [1d] “a control input port configured to receive a control signal”

For these limitations, Petitioner abandons Kilbuck and instead relies exclusively on Grundy, including Grundy’s clock line 152, command line 156, and multi-purpose lines 158 as depicted in Figure 5A and related embodiments. *See, e.g.,* Pet., 23-34. Unlike its analysis of the flash-memory structure in limitation [1a], Petitioner does not invoke Kilbuck “to the extent” Grundy is deficient, but instead treats Grundy’s interface and signaling disclosures as sufficient on their own.

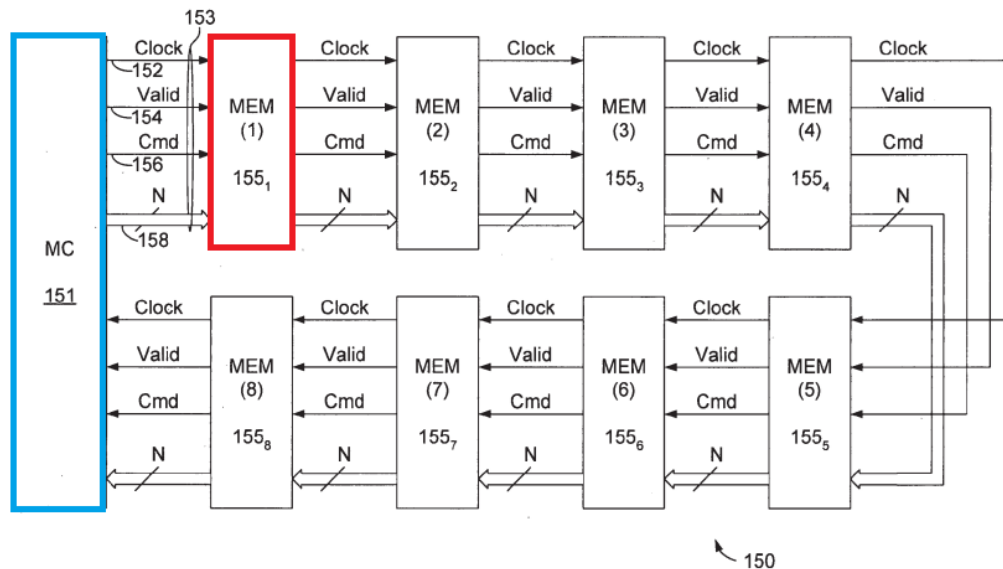
This shift is significant. Petitioner thus implicitly treats Grundy’s memory device—and specifically Grundy’s Figure 5A signaling embodiment—as the claimed “flash memory device” for purposes of limitations [1b], [1c], and [1d]. But Petitioner never reconciles that reliance on Grundy’s signaling architecture with its earlier reliance on Kilbuck to supply the flash-memory structure and device-level characteristics required by limitation [1a]. In particular, Petitioner does not explain how or whether Kilbuck’s flash memory devices—with their own internal controllers and interfaces distinct from the one disclosed in Grundy—are integrated into Grundy’s signaling chain, or how the resulting device would implement

Grundy's communication protocol between Grundy's devices and Grundy's controller. Nor does Petitioner identify whether the claimed "common data interface" and "control input port" belong to a Grundy device, a Kilbuck device, or some hybrid of the two.

Accordingly, for limitations [1b], [1c], and [1d], Petitioner again fails to identify a single configuration. Instead, it relies on Grundy alone to supply the claimed interface and signaling behavior, while relying on Kilbuck elsewhere to supply the underlying flash memory device—without explaining how these fundamentally different disclosures combine to teach the single claimed device.

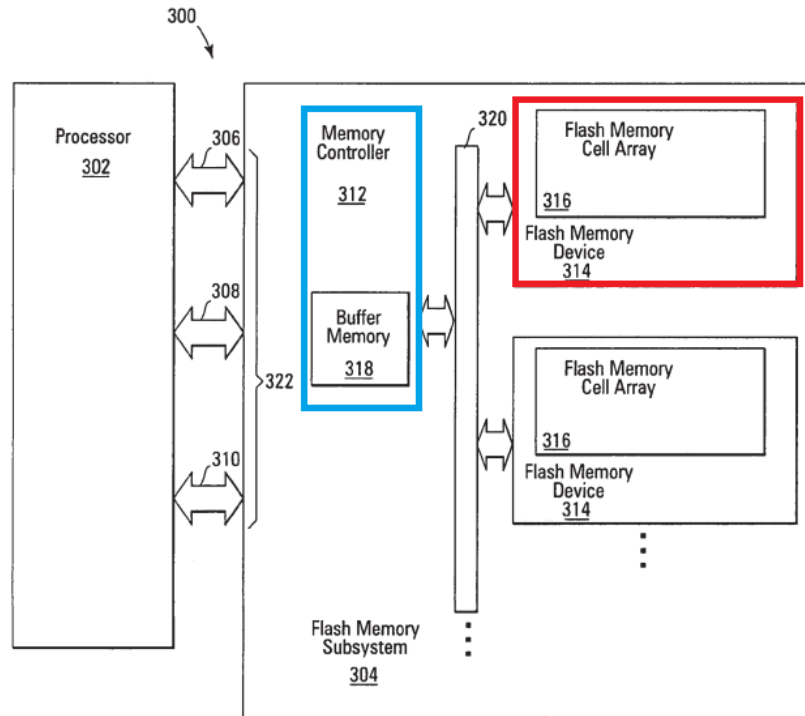
Claim 1 further requires [1e] "a ***control circuitry*** configured to execute a page program operation to store the input data on a selected page, and to execute a read operation to retrieve the output data from the flash memory cells in accordance to the command data and address data received at the at least one common data interface." Petitioner's analysis of this limitation does not identify a single "control circuitry" within a defined device. Instead, Petitioner alternates among multiple, materially different control structures. First, Petitioner asserts that "each of Grundy's ***memory devices*** includes control circuitry configured to execute operations associated with various commands such as read and write commands." Pet., 35. In the same paragraph, however, Petitioner also asserts that "Grundy's ***memory controller*** also includes control circuitry configured to execute operations

associated with various commands.” *Id.*



Ex. 1005 [Grundy], Fig. 5A (Patent Owner annotation showing Grundy’s **memory controller** 151 and exemplary **memory device** 155₁). Petitioner thus relies simultaneously on device-level control within Grundy’s memory devices and system-level control within Grundy’s memory controller, without identifying which of these is the claimed “control circuitry” of the claimed “flash memory device.”

Petitioner then invokes Kilbuck “to the extent” Grundy is alleged not to disclose flash-specific operations. *See, e.g.,* Pet., 37, 39 (relying on Kilbuck for page program and read operations). Kilbuck, however, discloses a flash memory device having its own internal memory controller that manages flash-specific operations such as page selection, programming, and reading.



Ex. 1006 [Kilbuck], Fig. 3A (Patent Owner annotation showing Kilbuck’s **memory controller** 312 and flash **memory device** 314). Petitioner does not explain whether Kilbuck’s controller is incorporated into each Grundy memory device, replaces Grundy’s controller, or operates alongside it. Nor does Petitioner explain how Kilbuck’s flash-specific control circuitry interacts with the command and signaling architecture that Petitioner relies upon in Grundy for limitations [1b]-[1d].

As Dr. Przybylski explains:

From a technical perspective, Petitioner’s analysis does not identify a single implementation of the claimed ‘control circuitry’ within a ‘flash memory device.’ Grundy describes both device-level control functionality—*e.g.*, memory devices that monitor and respond to commands—and a system-level memory controller that issues and

coordinates those commands. *See* Ex. 1005 [Grundy] [0032]-[0033], [0036]. Kilbuck, by contrast, describes a flash memory device having an internal controller that manages flash-specific operations such as page selection, programming, and reading. *See* Ex. 1006 [Kilbuck] [0030]-[0031].

Petitioner does not identify which of these control structures is the claimed ‘control circuitry,’ nor does the Petition explain how or whether Kilbuck’s internal controller would be incorporated into Grundy’s memory devices or reconciled with Grundy’s command propagation and signaling architecture. As a result, it is unclear what specific device is alleged to include the claimed control circuitry, or how the proposed combination would operate as a single flash memory device that performs the claimed page program and read operations.

Ex. 2027 [Przybylski-Decl.] ¶¶ 59-60.

A POSITA would further recognize that the alternatives discussed by Petitioner are not different characterizations of the same system, but materially different systems. If Kilbuck’s flash-specific controllers were incorporated into each of Grundy’s memory devices, for example, then each device would need to include flash-management functionality (*e.g.*, page selection, programming control, and related operations), altering the role of Grundy’s memory controller and requiring coordination between multiple device-level controllers within the chain. Ex. 2027 [Przybylski-Decl.] ¶ 61. If, instead, such functionality were centralized in Grundy’s memory controller, then that system-level controller—not any circuitry within a

memory device—might be responsible for executing the claimed operations, which would not correspond to the claimed “control circuitry” of a “flash memory device.” Petitioner does not address these materially different implementations or explain how any of them yields a single device having the claimed control circuitry operating in accordance with the claimed interface. Ex. 2027 [Przybylski-Decl.] ¶ 62. Petitioner’s lack of attention to these issues was only confirmed by Petitioner’s expert, who hedged at deposition about where flash memory management takes place in the combined system. Ex. 2028 [Sechen-Tr.], 22:7–17 (admitting that Grundy does not disclose its memory controller mapping bad blocks or monitoring wear levels in a NAND flash memory device), 23:6–11 (agreeing that bad block management would be performed somewhere in an implementation of Grundy with NAND flash memory devices), 23:12–15 (“Q. Would it necessarily be performed by Grundy’s memory controller? A. Well, certainly, by the ultimate memory controller that’s used by the combination”).

Claim 1 further requires [1f] “a status register configured to indicate a status of the flash memory device.” Petitioner again does not map this limitation to a single, defined device. Instead, Petitioner relies on Grundy for the general concept of “status requests” and “status responses,” while invoking Kilbuck “to the extent” needed to supply an actual flash-memory “status register.” *See, e.g.,* Pet., 41 (asserting that, “to the extent” Grundy does not disclose a status register, Kilbuck

does). As with limitation [1a], Petitioner thus does not identify a concrete structure within a defined device, but instead conditionally substitutes Kilbuck's flash-device implementation for Grundy's system-level behavior.

This shift is material. Grundy describes status in the context of its chain protocol: commands may include "status requests," and each memory device monitors commands propagating through the chain to determine whether responsive action is required. Ex. 1005 [Grundy] [0032]-[0033]. Grundy's interface involves command packets directed to target devices and device responses propagated through the signaling queue. *Id.*, [0065], [0069], [0076]-[0082]. Petitioner's expert admitted that Grundy's "status responses" would not need to be stored in a status register, and that the hardware of an implementation of Grundy that did not have status registers would have to be modified to include them. Ex. 2028 [Sechen-Tr.], 27:2–15.

Kilbuck, by contrast, discloses a flash-memory architecture in which an internal controller manages the flash array and associated control/status functionality, including RAM control registers, erase-block-management registers, and uses either a "ready/busy" pin or "internal status register/flag" to indicate to an external device whether the flash memory device is busy. Ex. 1006 [Kilbuck] [0030]-[0034]. Petitioner does not explain whether or how Kilbuck's status register would be incorporated into each Grundy memory device, how it would be accessed

through Grundy’s command protocol, or how it relates to the “control circuitry” identified for limitation [1e].

As Dr. Przybylski explains:

Incorporating Kilbuck’s status register into Grundy’s system would require defining where that register resides, how it is accessed through Grundy’s command protocol, and how it interacts with the control circuitry responsible for executing flash operations. Petitioner does not address any of these issues. Without such an explanation, it is unclear how Petitioner’s “Grundy-Kilbuck” is alleged to include the claimed ‘status register,’ or how that register is used in the proposed combination.

Ex. 2027 [Przybylski-Decl.] ¶ 64.

Petitioner offers only alternative elementwise mappings that are never reconciled into a single device satisfying all limitations. The Petition thus provides no basis to assess how the proposed combination would operate.

C. Petitioner Fails To Show A Motivation To Combine With A Reasonable Expectation Of Success.

Beyond its failure to state a defined combination, Petitioner’s theory fails for three additional independent reasons. First, rather than identify a single system from the cited art, Petitioner assembles the claimed invention from disparate disclosures only after consulting the claims—an impermissible hindsight reconstruction. *See* Section II.C.1. Second, because Petitioner never identifies a coherent “Grundy-

Kilbuck” configuration, Petitioner does not show that a POSITA would have been motivated to arrive at its proposals. *See* Section II.C.2. Third, Petitioner fails to show that any such hypothetical combination would have been expected to function as claimed. *See* Section II.C.3.

1. Petitioner’s Analysis Impermissibly Relies On Hindsight.

Petitioner’s theory is an impermissible hindsight reconstruction that uses the challenged claims as a roadmap. Rather than start with a defined prior-art system and explain how and why a POSITA would have modified it, Petitioner proceeds limitation by limitation, invoking Kilbuck “to the extent” needed to supply whatever feature Grundy is alleged not to disclose. *See, e.g.,* Pet., 20-22, 37, 39, 41, 46, 73; Section II.A *supra*. As explained in Section II.B, Petitioner’s mapping correspondingly shifts among materially different embodiments without reconciling them into a single, coherent system. The repeated “to the extent” substitutions underscore that Petitioner is not describing a single identified system, but rather filling gaps using the claims as a roadmap. This is not analysis of a proposed combination; it is reconstruction of the claimed invention from disparate prior-art pieces.

The Federal Circuit has repeatedly rejected this form of reasoning. In *TQ Delta*, the Court cautioned that such analysis “risks allowing the challenger to use the challenged patent as a roadmap to reconstruct the claimed invention using

disparate elements from the prior art—*i.e.*, the impermissible ex post reasoning and hindsight bias that *KSR* warned against.” *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1361 (Fed. Cir. 2019). Likewise, in *InTouch*, the Court rejected an invalidity opinion where the expert “relied on [the patent] itself as her roadmap for putting what she referred to as pieces of a ‘jigsaw puzzle’ together.” *InTouch Techs., Inc. v. VGo Commc’ns, Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014). And in *Ruiz*, the Court explained that “[t]his form of hindsight reasoning, using the invention as a roadmap to find its prior art components,” is not a permissible basis for obviousness. *Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 1275 (Fed. Cir. 2004).

2. Petitioner Fails To Show A Motivation To Combine.

Even if its reliance upon impermissible hindsight were overlooked, Petitioner fails to show that a person of ordinary skill in the art would have been motivated to combine Grundy and Kilbuck in the manner required by the claims. An obviousness theory must do more than identify prior-art disclosures corresponding to individual claim limitations; it must articulate a reasoned basis—grounded in the record—why a POSITA would have selected and combined those teachings to arrive at the claimed invention. *KSR*, 550 U.S. at 418; *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016).

Petitioner does not meet that burden because Petitioner never identifies what combination a POSITA would have been motivated to make. As explained in

Section II.A, Petitioner’s analysis proceeds on a limitation-by-limitation basis in which Kilbuck is invoked only “to the extent” needed to supply whatever Grundy is alleged not to disclose. And as explained in Section II.B, Petitioner’s mapping draws from materially different and incompatible embodiments of the prior art without reconciling them into a single system. Petitioner thus does not present a defined configuration to which a motivation analysis can be applied.

That failure is dispositive because a POSITA’s assessment of whether to modify Grundy—and how to do so—necessarily depends on the specific configuration under consideration. Because Petitioner never identifies which configuration it relies upon, it never provides a basis to determine what a POSITA would have been motivated to do. For example, as discussed in Section II.B, materially different design choices arise depending on how exactly “Grundy-Kilbuck” incorporates flash memory. Those choices would lead a POSITA to evaluate different potential modifications, tradeoffs, and design paths. For example, whether control functionality is implemented within each memory device or centralized in a system-level controller would present different design constraints and would not lead a POSITA to the same modification of Grundy. Because Petitioner never identifies which of these configurations it relies upon, it provides no basis to determine what a POSITA would have been motivated to do.

Petitioner’s failure also reflects a more fundamental defect: it never performs

the analysis required under *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966):

Petitioner does not identify the differences between the claimed invention and any specific Grundy embodiment, or any modifications needed to Grundy to incorporate Kilbuck’s alleged teachings. Without a specified baseline system and identified changes, there is no basis to assess a motivation to combine.

Instead, Petitioner relies on generalized assertions that a POSITA would have “appl[ied]” Kilbuck’s teachings to Grundy to achieve “predictable results.” Pet., 15-16. But such statements merely restate the legal standard at a high level; they do not identify any particular combination, do not explain why a POSITA would have selected the specific features at issue, and do not address the architectural and operational differences discussed above. Courts have repeatedly rejected such conclusory reasoning as insufficient to establish a motivation to combine. *See, e.g., TQ Delta*, 942 F.3d at 1360.

Even assuming *arguendo* that Petitioner has correctly identified individual features in Grundy or Kilbuck, that is not enough. The question is not whether a POSITA could have combined those features, but whether a POSITA would have been motivated to do so in the manner required by the claims. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). Petitioner never answers that question because it never identifies a concrete system to which the question can be applied. Indeed, Petitioner’s shifting reliance on different embodiments avoids

committing to any particular configuration—presumably because doing so would require confronting the incompatibilities discussed above.

Even within a single reference (like Grundy), a motivation must exist for combining features of different embodiments or otherwise modifying the teachings of a reference. *See, e.g., In re Kotzab*, 217 F.3d at 1370. Petitioner’s failure to do this in the context of the “status register” limitation present in all challenged claims was already discussed above. *See* Section II.B *supra*. The compounding nature of Petitioner’s failure to motivate “Grundy-Kilbuck” becomes even more evident in dependent claims that recite additional features. In connection with dependent claim 5 (“[t]he flash memory device as claimed in claim 4, further comprising a delay lock loop (DLL) to synchronize the clock output signal with the clock signal”), for example, Petitioner simply points to a disclosure of delay lock loop in one embodiment of Grundy, and argues that “[a] POSITA would have recognized that Grundy’s DLL is used to synchronize the clock output signal with the clock signal,” Pet., 57. But Petitioner’s expert admitted that delay lock loops are not necessarily present in embodiments of Grundy that Petitioner elsewhere relies upon, Ex. 2028 [Sechen-Tr.], 86:21-87:16 (stating that Grundy’s disclosure of delay lock loops is for “Figure 5A but modified with the concept that you could have a single clock source”), 89:1–4 (admitting that an embodiment of Grundy’s Figure 5A would not need to include a delay lock loop), 90:20–24 (admitting that an embodiment of

Grundy's Figure 17 would not need to include a delay lock loop "[b]ut it's a design choice that one could make"), and Petitioner offers no motivation for their presence in modifications of those embodiments beyond the bare assertion that they would satisfy claim language if present. Pet., 57. As another example, in connection with dependent claims 13 and 21, Petitioner relies without comment or motivation upon Grundy's Figure 4A—an embodiment discussed nowhere else in the Petition, and an embodiment that Petitioner does not discuss in its analysis of the underlying independent claims. *See* § V *infra*. With all of this, Petitioner at most argues that Grundy separately discloses aspects of dependent claims in different embodiments. This does not satisfy Petitioner's obligation to show a ***motivation*** to combine such aspects into systems that embody the claimed inventions.

3. Petitioner Fails To Show A Reasonable Expectation Of Success.

Petitioner also fails to show that a POSITA would have had a reasonable expectation of success. Even where a motivation to combine is alleged, a petitioner must demonstrate that the proposed combination would have been expected to function as claimed. *Magnum*, 829 F.3d at 1380. That requires more than identifying individual features in the prior art; it requires a reasoned explanation, grounded in the record, that the proposed system would operate successfully when those features are combined.

Petitioner provides no such explanation because the Petition never defines a

single system to evaluate for functionality and effectiveness. As explained in Sections II.A and II.B, Petitioner's theory relies on materially different and incompatible embodiments of the prior art, which are never reconciled into a coherent configuration. Without identifying a specific system, Petitioner cannot show that such a system would have been expected to function.

This failure is particularly acute here because the embodiments on which Petitioner relies reflect fundamentally different design assumptions. As discussed in Section II.B, those embodiments differ in how memory devices are organized, how control functionality is allocated, and how memory operations are performed.

Nor does Petitioner address the technical consequences of its proposed modifications. Integrating flash-specific functionality into a controller such as Grundy's, which is designed for "media including, without limitation, various forms of magnetic and optical media" and "storage arrays of different types (e.g., different underlying storage media) ... provided in different memory devices of the chain," Ex. 1005 [Grundy] [0035], or combining features drawn from distinct embodiments of Grundy's memory devices with different operating assumptions, presents non-trivial design and implementation challenges. A POSITA would need to resolve such issues to achieve a functioning system. Petitioner identifies none of them and provides no explanation as to how they would be addressed.

Instead, Petitioner assumes that once any relevant features are identified in

Grundy or Kilbuck, they can be combined without difficulty. This assumption is insufficient. A reasonable expectation of success cannot be established by simply asserting that known elements could be combined; the petitioner must show that the combination would have been expected to work. *See Magnum*, 829 F.3d at 1380; *see also Belden*, 805 F.3d at 1073.

Accordingly, Petitioner fails to establish a reasonable expectation of success.

III. PETITIONER FAILS TO ADDRESS ITS DISTRICT COURT CLAIM CONSTRUCTION OF “CLOCK OUTPUT SIGNAL” (CLAIMS 4, 5, AND 19).

Claims 4, 5, and 19 of the '381 patent all recite a “clock output signal.” In district court, Petitioner proposed construing “clock output signal” as “a periodic signal that synchronizes system operations.” Ex. 2007 [Opening-Claim-Construction-Brief] 12. Petitioner further argued that the term requires a “synchronous, periodic signal.” *Id.*, 13. But in this proceeding, Petitioner told the Board that “no claim terms require a formal construction for purposes of addressing the grounds in this Petition.” Pet., 2.

The Director already addressed that inconsistency. The Institution Decision found that “Petitioner’s failure to provide an explanation for its different positions is problematic, and typically weighs in favor of denying institution.” Inst. Dec. (Paper 27), 2-3. The Director nevertheless instituted because Petitioner’s conduct “only affects three dependent claims out of twenty-one challenged claims.” *Id.*, 3. But the

Director did not excuse Petitioner's inconsistency or leave the term unconstrued. Instead, the Director ordered that "Petitioner shall be bound by its proposed district court construction of the term 'clock output signal' in its analysis of claims 4, 5, and 19 of the '381 patent." *Id.*, 4; *see also id.*, 3 ("Petitioner is bound by its proposed district court construction of 'clock output signal,' thereby ensuring consistency in claim construction between the two proceedings.").

That ruling is dispositive for claims 4, 5, and 19. Petitioner bore the burden to show in the Petition that the challenged claims are unpatentable under the construction by which Petitioner is now bound. Petitioner did not do so. The Petition never argues that Grundy's alleged "clock output signal" is "a periodic signal that synchronizes system operations." Pet., 53-57. Indeed, the Petition's discussion of claims 4, 5, and 19 does not use the word "periodic," does not use the word "synchronous," and does not explain what "system operations" are supposedly synchronized by any alleged "clock output signal." *Id.* Nor does Petitioner's expert apply Petitioner's construction. Petitioner's expert instead confirmed that his declaration applied the "ordinary and customary meanings" of the claim terms. Ex. 2028 [Sechen-Tr.] 12:6–10 ("Q: So in the opinions expressed in your declaration, you have applied the ordinary and customary meanings of the terms in the '381 patent claims that are at issue, correct? A: Yes, that's right.").

This is not a harmless omission. Petitioner’s district-court construction imposes specific requirements: the claimed “clock output signal” must be periodic, must be synchronous, and must synchronize system operations. Ex. 2007 [Opening-Claim-Construction-Brief] 12-13. The Petition does not identify any “system operations” that are allegedly synchronized, or state what it would mean for those operations to be synchronized, or show how any alleged clock output signal in Grundy performs that function. The Petition likewise does not show that the signal satisfies Petitioner’s “synchronous, periodic” requirement. The Petition instead relies primarily on Grundy’s use of the phrases “clock signal” or “outgoing clock signal” and then asserts that the claim language is therefore satisfied. *See* Pet., 53-57. This is not an application of Petitioner’s binding construction.

This defect of the Petition is further evidenced by the substance of Petitioner’s district court claim construction arguments. Petitioner’s district court briefing emphasized that “the claimed function of the ‘clock output signal’ [is] synchronizing system operations,” Ex. 2007 [Opening-Claim-Construction-Brief], 3, and argued that the claimed “clock output signal” could not include a “strobe.” *Id.*, 4-7. The Petition addresses none of those issues. The Petition does not connect Grundy’s cited disclosures to the claimed function of synchronizing system operations. The Petition does not explain why Grundy’s alleged “clock output signal” is not a “strobe,” or some other timing indicator that Petitioner suggests is excluded by its

own construction. *See id.*, 12 (arguing that the claimed clock output signal “does not encompass *all* timing signals”) (emphasis in original); 4 (arguing that an interpretation of “clock output signal” that “sweep[s] broadly enough to encompass control signals like strobes” would “rewrit[e]” claim language). And Petitioner does not provide expert testimony applying its district court construction to Grundy.

Petitioner therefore stands in the same position as the Petitioner in *Apple Inc. v. Gesture Tech. Partners, LLC*, 129 F.4th 1367 (Fed. Cir. 2025). There, an IPR petitioner advocated a claim construction, but “the petition presented no argument as to how Numazaki, alone or in view of the knowledge of a person of ordinary skill in the art, would meet this claim construction.” *Id.*, 1374. The Federal Circuit affirmed the Board’s finding that the petitioner failed to show unpatentability. *Id.*, 1375. The same result follows here: Petitioner is bound by its construction of “clock output signal,” and yet the Petition presents no evidence or argument showing that Grundy or “Grundy-Kilbuck” satisfies that construction.

Recent Director decisions confirm the same point. In *Revvo*, the Director held that when a petitioner takes different claim-construction positions before the Board and district court, the petitioner must, “at a minimum, explain why alternative positions are warranted.” *Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20, 3-4 (Director Nov. 3, 2025) (precedential). The Director later applied that rule to deny institution where the petitioner’s “wait and see”

explanation did not justify maintaining different constructions in district court and before the Board. *Revvo Techs., Inc. v. Tire Stickers LLC*, IPR2025-00631, Paper 34, 2-3 (Director Feb. 3, 2026). *Tesla* likewise denied institution where the petitioner advanced a district-court position inconsistent with the petition and failed to show, even assuming its district-court position, that the prior art met the limitation. *Tesla, Inc. v. Intellectual Ventures II LLC*, IPR2025-00340, Paper 18, 2-4 (Director Nov. 5, 2025) (informative). Here, the Director already chose the remedial path of binding Petitioner to its district-court construction. Inst. Dec. (Paper 27), 3-4. But Petitioner also cannot prevail on claims 4, 5, and 19 on this Petition and this record, because the Petition never applies the construction that Petitioner is now bound to apply.

Nor can Petitioner cure this defect now. “Unlike district court litigation—where parties have greater freedom to revise and develop their arguments over time and in response to newly discovered material—the expedited nature of IPRs bring with it an obligation for petitioners to make their case in their petition to institute.” *Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (quoting 35 U.S.C. § 312(a)(3)). “Ultimately, it is the petitioner’s burden to present a clear argument,” *Netflix, Inc. v. DivX, LLC*, 84 F.4th 1371, 1377 (Fed. Cir. 2023), and the Board may not supply arguments “that could have been included in a properly-drafted petition.” *Magnum*, 829 F.3d 1364 at 1380-81. Because the Petition never applies Petitioner’s binding construction of “clock output signal,”

Petitioner has failed to meet its burden for claims 4, 5, and 19.

Claims 4, 5, and 19 should therefore be confirmed patentable.

IV. PETITIONER FAILS TO SHOW “THE COMMAND DATA IS LATCHED AT THE FIRST RISING EDGE OF THE CLOCK SIGNAL AFTER THE TRANSITION OF THE CONTROL SIGNAL” (CLAIM 2).

Claim 2 recites the flash memory device of claim 1 “wherein the command data is latched at the first rising edge of the clock signal after the transition of the control signal.” Petitioner and its expert rely exclusively upon Grundy to satisfy this limitation. *See* Pet., 47-50; Ex. 1003 [Sechen-Decl.] ¶¶ 106-109.

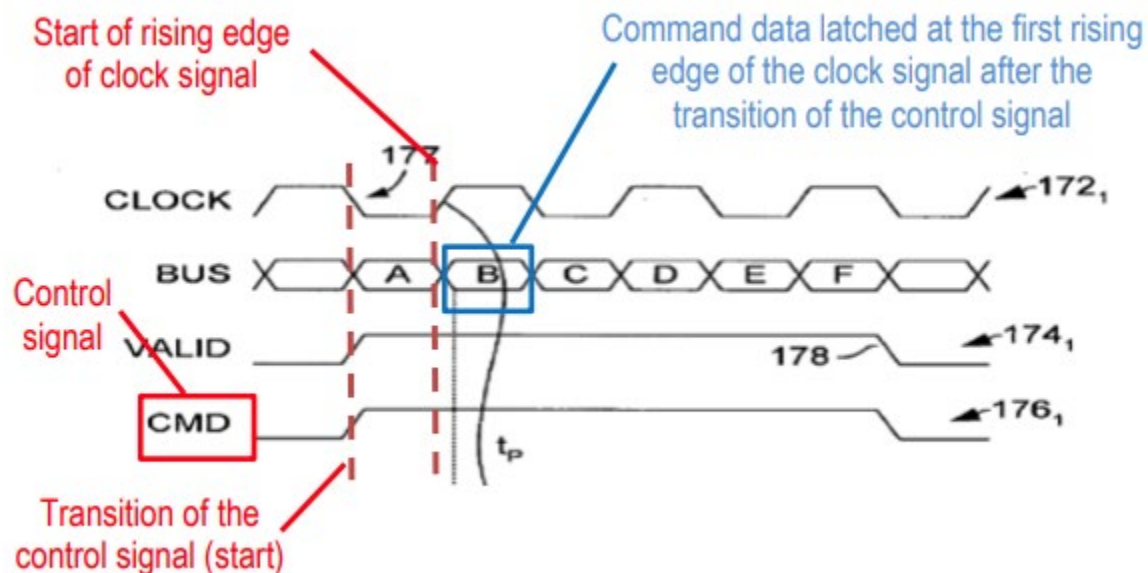
Petitioner’s claim 2 theory fails for three reasons. First, it never consistently identifies the claimed “command data.” *See* Section IV.A. Second, it mistakenly relies upon a figure that shows the timing of controller-side transmissions for information about the timing of latching in a memory device. *See* Section IV.B. Third, it never proves latching at the first rising edge of the “clock signal” recited in claim 1. *See* Section IV.C. Each failure independently shows that Petitioner has not met its burden to show that claim 2 is obvious.

A. Petitioner Does Not Consistently Identify Any “command data” In Claim 2.

Petitioner does not consistently identify what constitutes the claimed “command data” in claim 2, and that failure prevents it from establishing the required timing relationship for any identified data. Claim 1 recites “command

data”—including, for example, in a recitation of a control input port configured to receive a control signal whose transition “from an inactive state to an active state indicates a beginning of *command data* being received at the at least one common data interface.” Claim 2 further requires that “the command data”—referring back to claim 1—be latched “at the first rising edge of the clock signal after the transition of the control signal.” Claim 2 thus imposes a requirement on specific, previously identified “command data” that relates that command data to a previously recited “transition of [a] control signal.”

In connection with claim 2, Petitioner identifies the value “B” in Grundy’s Figure 6 as the claimed “command data” in its annotation of Figure 6:



Pet., 48, 47 (quoting Ex. 1005 [Grundy] [0047]); *see also* Ex. 2028 [Sechen-Tr.], 60:6–11 (Petitioner’s expert confirming reliance upon value “B” as the claimed “command data”).

But elsewhere in its analysis—particularly in addressing the limitations of claim 1 from which claim 2 depends—Petitioner identifies multiple different values in Figure 6 as “command data,” including “A, B, C, *etc.*” *See, e.g.*, Pet., 34; *see also id.*, 28. In other portions of the Petition, Petitioner refers more generally to “data (e.g., command, address, input, or output)” without distinguishing which specific values correspond to “command data.” *See id.*, 27-28.

Petitioner never reconciles these conflicting identifications. It does not explain whether the claimed “command data” is limited to B, includes A, or encompasses a sequence of values, nor does it tie any such identification to the timing requirement of claim 2. As a result, Petitioner never shows that any specific data—whether B or otherwise—is latched at the required time.

This failure is dispositive. Claim 2 requires identified “command data” to be latched at a particular clock edge; Petitioner’s shifting identifications do not prove this timing for any “command data.”

B. Grundy’s Figure 6 Depicts When “Values” Are Transmitted By Grundy’s Memory Controller, Not When “Values” Are Captured By Grundy’s Memory Device.

Claim 2 requires that the command data be “*latched* at the first rising edge of the clock signal after the transition of the control signal.” This limitation concerns the timing of when command data is latched at the claimed “flash memory device.” Petitioner presents no evidence demonstrating that this limitation is satisfied by its combination. Petitioner relies on Grundy’s Figure 6 to satisfy this requirement. *See* Pet., 47-50; Ex. 1003 [Sechen-Decl.] ¶¶ 106-109. But Figure 6 concerns when Petitioner’s alleged “command data” is *transmitted* by Grundy’s memory controller to Grundy’s memory device; it does *not* identify when any data is latched by Grundy’s memory device, and therefore does not show the specific timing relationship required by the claim. A memory controller transmitting a value is not the same event as a memory device latching that value, let alone doing so “at the first rising edge of the clock signal after the transition of the control signal.”

Grundy itself describes Figure 6 (shown below) as “*an exemplary timing diagram* showing the relative timing of signals *transmitted by the memory controller* of FIG. 5A ...” Ex. 1005 [Grundy] [0011].

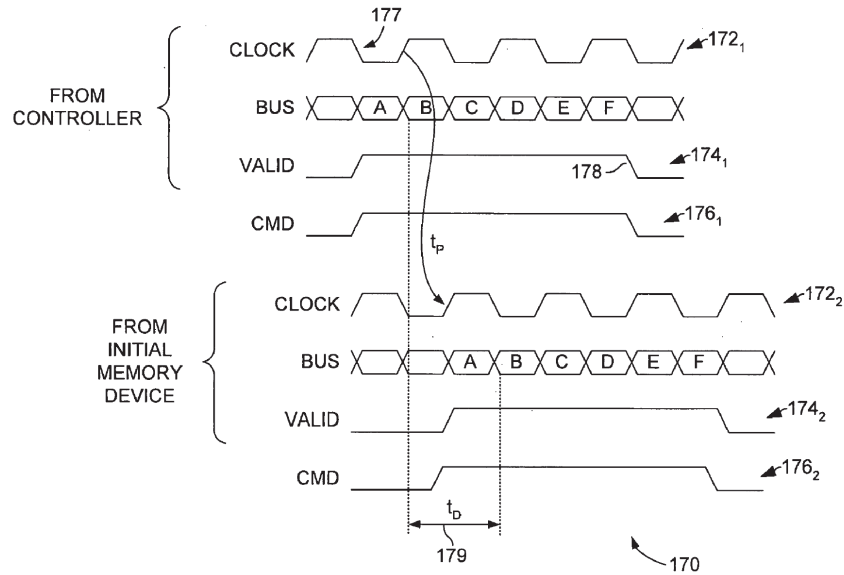
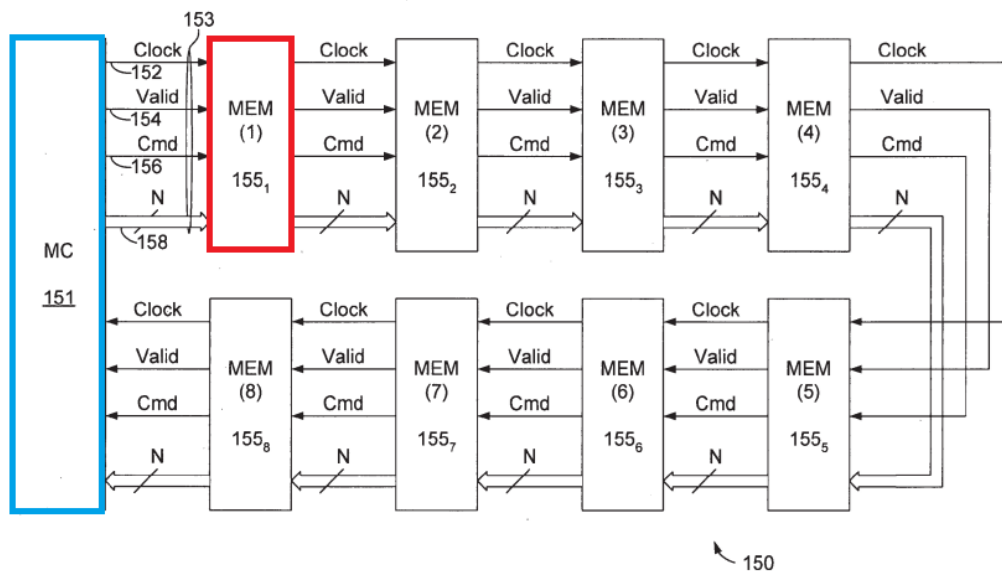


FIG. 6

Grundy's Figure 5A correspondingly and expressly depicts Grundy's [memory controller](#) 151 and exemplary [memory device](#) 155₁ as different things:



Ex. 1005 [Grundy], Fig. 5A (Patent Owner annotation); *see also id.*, [0047] (stating that “the memory controller 151 outputs a free-running clock signal 172₁,”

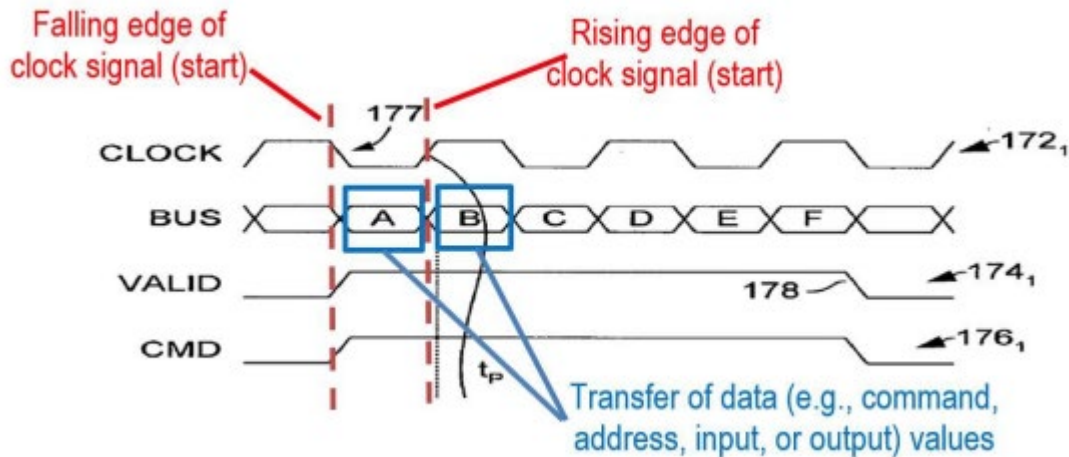
“simultaneously asserts a valid signal 174₁ ... (and a command signal 176₁ ... if a command is being transmitted)” and “drives a first value, A, onto the bus 158” and that subsequent values “are transmitted onto the bus 158 in successive transmit intervals”). These disclosures describe controller-side transmission events. They do not describe when any of those values are latched by memory device 155₁. As Dr. Przybylski explains,

Grundy’s Figure 6 depicts the timing of signals transmitted by the memory controller, not the timing of when those signals are latched. A POSITA would not understand Figure 6 to show when any value is latched at the memory device. As a threshold matter, neither Fig. 6 nor Fig. 5A conveys any information about the physical placement of these devices or the lengths of the links between them. A POSITA therefore cannot assume any particular relationship between the transmit time from one device and the receive time at the next, other than that the link propagation delay is some part of the overall propagation delay t_p . Because Figure 6 similarly does not depict when data is captured after being received, it does not show that any data is latched at a particular clock edge at a specific time, let alone “at the first rising edge of the clock signal after the transition of the control signal” as required by claim 2.

Ex. 2027 [Przybylski-Decl.] ¶ 89.

Petitioner’s expert confirmed that Figure 6 provides no evidence of when data is received or latched at the memory device. As one example, he agreed that Figure

6 “doesn’t depict when the value A is received by the memory device 155₁,” and that “there’s nothing here ... to indicate when it’s received, per se.” *See* Ex. 2028 [Sechen-Tr.], 55:3–56:12. As another example, when discussing Petitioner’s annotation of Figure 6,



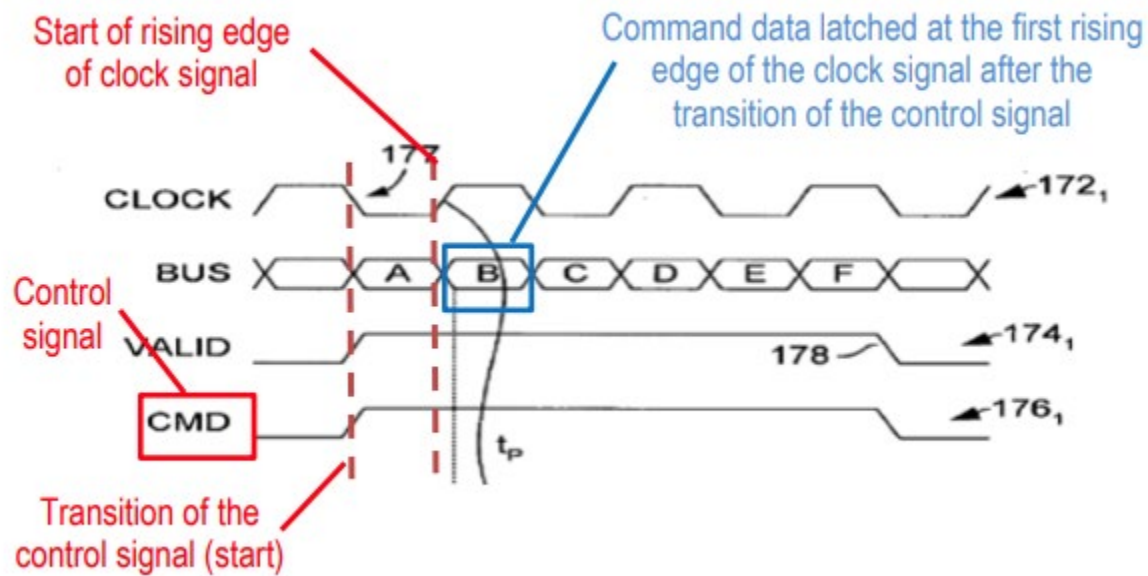
Pet., 29 (citing Ex. 1003 [Sechen-Decl.] ¶ 86), Petitioner’s expert was asked “by the time indicated by the other side of that [first] blue box, Grundy’s memory device 155₁ has received the value A; is that correct?” and he responded “No, we can’t say that for sure.” Ex. 2028 [Sechen-Tr.], 56:6–12. When asked directly whether Figure 6 shows that value B is latched at the time required by the claims, he answered unequivocally: “No.” *Id.*, 60:12–21.

This is dispositive because claim 2 concerns when command data is latched at the claimed “flash memory device,” not when values are transmitted by Grundy’s memory controller. Petitioner identifies Grundy’s memory device—not Grundy’s memory controller—as the claimed “flash memory device.” In particular, Petitioner

maps the claimed device-level interface limitations to Grundy's memory device MEM(1) 155₁, including by locating the claimed "common data interface" at the input to MEM(1) 155₁ in Grundy's Figure 5A. *See, e.g.,* Pet., 26 n.7. Claim 1 likewise refers to "command data being received at the at least one common data interface" of the flash memory device, and claim 2 then requires that "the command data" be latched at the specified clock edge. Ex. 1001 ['381] cls. 1-2.

Thus, the relevant question is not when Grundy's memory controller drives a value onto the bus, but when Grundy's memory device latches the claimed command data and which clock edge it uses. As both experts confirm, Figure 6 does not disclose or render obvious command data being "***latched***" at the first rising edge of the clock signal after the transition of the control signal."

Petitioner's annotation of Figure 6 bears no relationship to anything actually depicted or described in Grundy. Petitioner labels value "B" in the controller-side portion of Figure 6 as "Command data latched at the first rising edge of the clock signal after the transition of the control signal":



Pet., 48 (excerpt of Grundy's Figure 6, as annotated by Petitioner). But Petitioner's label is not a disclosure in Grundy. The cited portion of Figure 6 shows value B being present on the bus in a controller-side timing diagram. It does not show value B being captured by MEM(1) 155₁, much less latched at the particular clock edge required by claim 2.

Nor does the lower half of Figure 6 cure the problem. The lower half shows signals retransmitted by the initial memory device after delay. Ex. 1005 [Grundy] [0011], [0048]. Grundy explains that retransmitted signals are delayed relative to the controller's signals by propagation delay and hop time, and that command/data values are stored before retransmission. *Id.*, [0048]. But Figure 6 still does not identify any latching event at MEM(1) 155₁.

As Dr. Przybylski explains:

Grundy's Figure 6, again, is not a timing diagram of latching inside memory device 155₁. The upper portion of Figure 6 shows the timing of signals driven by Grundy's memory controller 151 to the first Grundy memory device 155₁. The lower portion shows the timing of signals later retransmitted by memory device 155₁ onto the next point-to-point link. The link length and hop time are not specified elsewhere in Grundy (or otherwise discussed by Petitioner), and so the reception and capture times relevant to Grundy's Figure 6 cannot be inferred indirectly from Grundy's disclosure. In particular, neither portion of Figure 6 indicates the time at which memory device 155₁ receives, captures, or latches any particular bus value.

This distinction is important because claim 2 requires command data to be latched at the flash memory device at a particular clock edge. A value being driven onto a bus by the memory controller is not the same thing as that value being latched by the memory device. Likewise, a value being retransmitted by the memory device is not the same thing as the earlier latching of that value within the memory device. Whether and when data is latched would depend upon the timing of the incoming signals at the memory-device input circuitry, the receiver circuitry, the internal clocking used by the memory device, and any subsequent buffering. Figure 6 does not identify any latching within the memory device or any timing relative to a purported "first rising edge of the clock signal after the transition of the control signal." Accordingly, a POSITA would not understand Figure 6 to show that value B—or any other alleged "command data" identified by Petitioner—is latched by memory device 155₁ at the claimed time.

Ex. 2027 [Przybylski-Decl.] ¶¶ 92-93.

Petitioner's expert confirmed the same point in deposition. He agreed that the upper portion of Figure 6 depicts "the timing of signals being transmitted from Grundy's controller MC 151 to the first device, 155₁, in the chain depicted in Figure 5A." Ex. 2028 [Sechen-Tr.] 44:7–11; *see also id.*, 50:21-51:1. When asked directly about Petitioner's claim 2 theory for value B, he confirmed that Figure 6 does not show the required latching:

Q. [I]f we were looking at, say, the left edge of this rectangle, Figure 6 is not depicting that the value B is latched at Grundy's memory device 155₁ at the time of that left edge of this rectangle; is that correct?

A. That's correct.

Q. Would the value B be latched at Grundy's memory device 155₁ at the time indicated by the right edge of the rectangle?

A. No, we cannot say that.

Q. Would it be possible to indicate on Figure 6 the first time at which the value B would be latched at Grundy's memory [device] 155₁?

A. No.

Ex. 2028 [Sechen-Tr.], 60:22-61:12.

Petitioner attempts to avoid this deficiency by pointing to general disclosures about Grundy's internal circuitry. But those disclosures and Petitioner's arguments about them do not directly address what Figure 6 itself fails to show. Petitioner

argues that “Grundy’s memory device latches command data based on the clock signal,” Pet., 48, that Grundy discloses latching because “a command word is loaded into a command buffer,” *id.*, 49-50, and that “Grundy’s clock signal drives this latching” because command packets are loaded into command buffer 351 “in response to transitions of the clock signal 326.” *Id.*, 50. None of those statements establishes that the command data identified in Figure 6 is latched at the particular clock edge required by claim 2.

At most, Petitioner here argues that Grundy’s Figure 17 and Figure 19 suggest information being captured or loaded inside Grundy’s memory device at some unspecified time. For example, Grundy discloses edge-triggered storage elements 315 in interface register 311, Ex. 1005 [Grundy] [0088], and later discloses command packets being loaded from the interface register into command buffer 351 “one word at time in response to transitions of the clock signal 326,” *id.*, [0092]. But Petitioner does not show that either of those internal events occurs at the first rising edge identified in Figure 6, or that the value allegedly latched at that time is the same “command data” identified for claim 2. Loading a command word from an interface register into a command buffer has also not been shown to be the same event as receiving and initially latching command data at the memory-device interface. Petitioner does not distinguish those events, identify which one supposedly satisfies claim 2, or show that either occurs at the specific clock edge required by the claim.

As Dr. Przybylski further explains:

Grundy's disclosures concerning interface register 311 and command buffer 351 do not supply the missing timing information. The interface register disclosure indicates that receiver outputs may be captured using edge-triggered storage elements. The command-buffer disclosure indicates that command packets may later be loaded from the interface register into command buffer 351 in response to transitions of internal clock signal 326. These are internal device operations that are distinct from the controller-side transmission timing depicted in Figure 6.

Even assuming that these disclosures show that command information is captured or loaded somewhere inside Grundy's memory device, they do not show that the command data identified by Petitioner is latched "at the first rising edge of the clock signal after the transition of the control signal." In particular, Grundy does not tie the loading of command buffer 351 to the specific edge annotated by Petitioner in Figure 6, and Petitioner does not identify any disclosure that does so.

Ex. 2027 [Przybylski-Decl.] ¶¶ 90-91.

Petitioner's claim 2 theory therefore rests on unsupported inferences from Figure 6. Figure 6 shows bus values transmitted in relation to clock edges. Grundy elsewhere describes internal buffering in vaguer relation to clock transitions than claim 2 requires. But Petitioner never connects those disclosures by showing that the command data identified in Figure 6 is latched inside memory device 155₁ at the first rising edge after the control-signal transition. Figure 6 does not show latching.

Figures 17 and 19 do not tie any latching event to the specific edge required by claim

2. Petitioner's own expert confirmed that Figure 6 cannot be used to identify when value B is latched by memory device 155₁.

Petitioner therefore fails to show that Grundy discloses or renders obvious "the command data is latched at the first rising edge of the clock signal after the transition of the control signal." *Magnum*, 829 F.3d at 1380 (petitioner must "articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness").

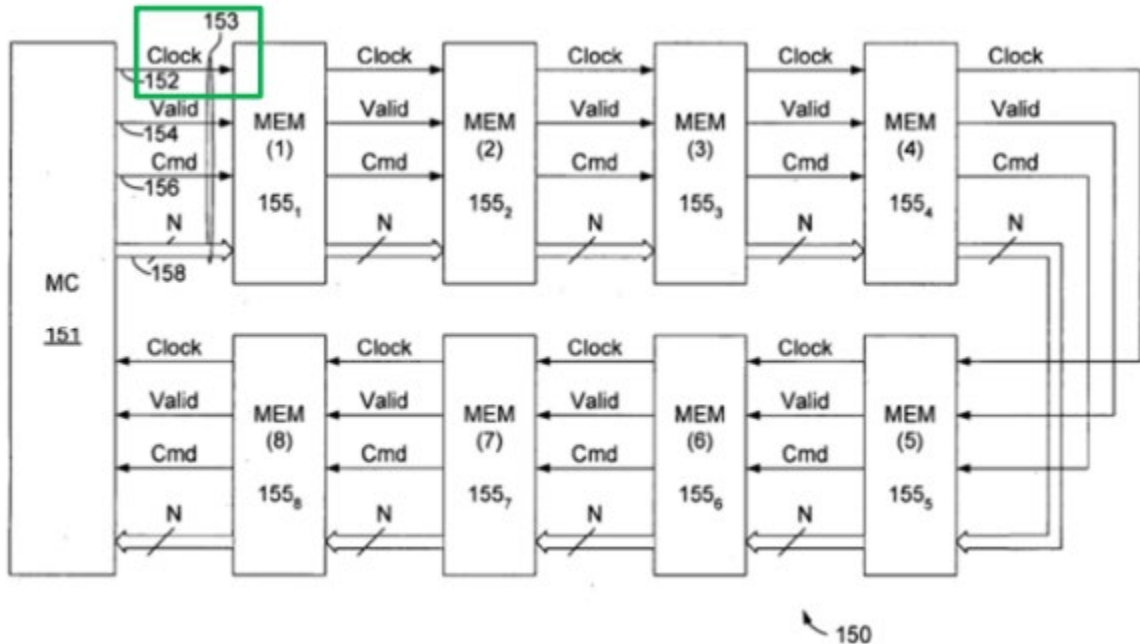
C. Petitioner Does Not Show The Required Timing With Respect To "the clock signal" In Claim 2.

Petitioner's claim 2 theory also fails for the independent reason that Petitioner never shows the required timing with respect to "the clock signal." Claim 2 requires that "the command data" be latched at the first rising edge of "the clock signal" after the transition of the control signal. Ex. 1001 ['381] cl. 2. The phrase "the clock signal" refers back to the clock signal recited in claim 1: "a clock input port configured to receive a clock signal." *Id.*, cl. 1. Petitioner was therefore required to show that the command data is latched at the first rising edge of the same clock signal it identified for claim 1. *See Convolve, Inc. v. Compaq Comput. Corp.*, 812 F.3d 1313, 1342 (Fed. Cir. 2008) ("This reference to 'the processor,' refer[s] back to the 'a processor' recited in preamble ...").

The Petition does not make that showing. Petitioner's claim 2 theory proceeds

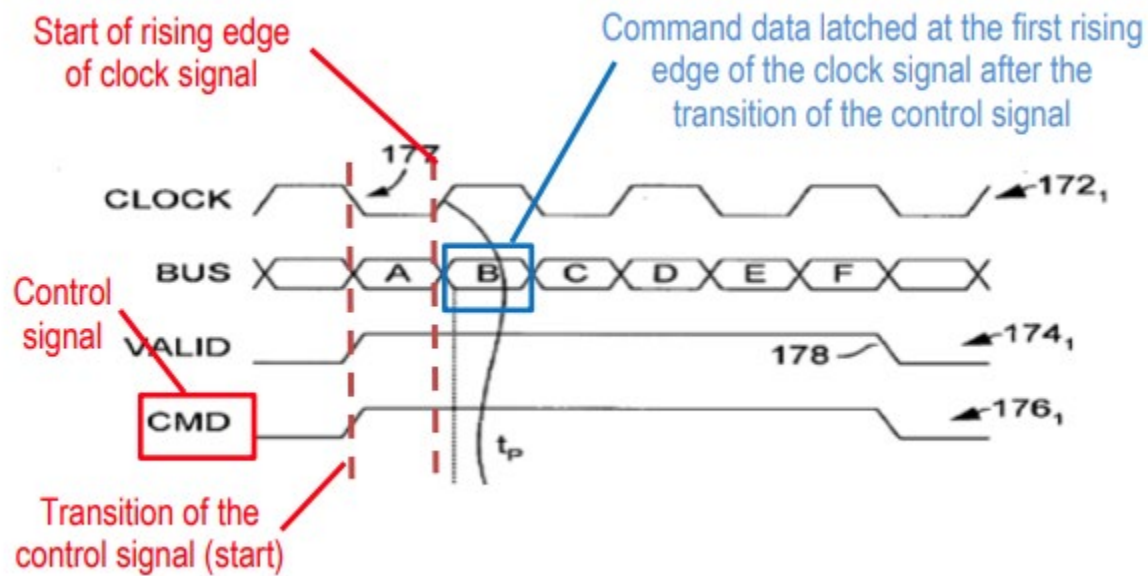
in two disconnected steps. First, Petitioner relies on Grundy's incoming clock signal—shown in Figure 5A as the “Clock” signal on clock line 152 and in Figure 6 as clock signal 172₁—to identify the claimed “first rising edge.” Pet., 23-24, 48. Second, when attempting to show the alleged latching, Petitioner relies on a later internal signal—Grundy's “logic level clock signal 326”—that is generated inside the memory device from the incoming clock. Pet., 49-50; Ex. 1005 [Grundy] [0088], [0092]. Petitioner never ties those two steps together. It never shows that any alleged latching event occurs at the first rising edge of the incoming clock signal identified for claim 1, and it never provides any timing analysis to reconcile Grundy's delayed internal clock signal 326 with the incoming clock signal.

For claim 1, Petitioner identifies the claimed “clock signal” as the clock signal received at Grundy's memory device over clock line 152. Pet., 23-24. In particular, Petitioner relies on Grundy's Figure 5A, annotating the “Clock” line between Grundy's memory controller 151 and the first memory device 155₁ as the claimed “clock signal”:



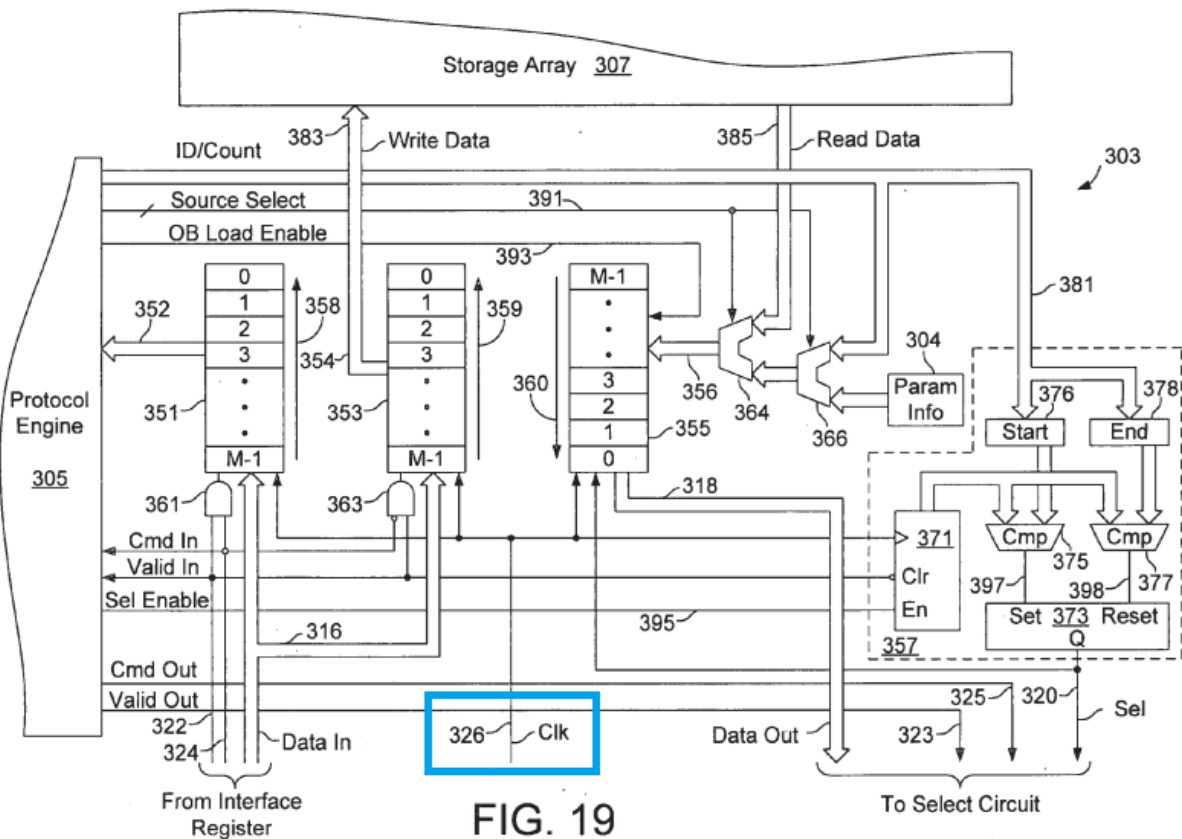
Pet., 23 (Grundy’s Figure 5A, annotated by Petitioner). Petitioner likewise cites Grundy’s disclosure that each point-to-point link includes “a clock line 152” used “to conduct a clock signal,” *id.*, 23-24, and relies on Grundy’s Figure 17, which labels the corresponding input to the memory device as “Clock In.” *Id.*; Ex. 1005 [Grundy] Fig. 17. Thus, for claim 1, Petitioner maps the claimed “clock signal” to the incoming clock signal provided to the memory device at its clock input.

Petitioner’s claim 2 analysis initially appears to use the same clock. Petitioner’s annotation of Grundy’s Figure 6 identifies the “Start of rising edge of clock signal” on the controller-side “CLOCK” waveform, corresponding to Grundy’s clock signal 172₁:



Pet., 48 (Petitioner’s annotation of Grundy’s Figure 6). But, as explained above, Figure 6 does not show when any data is latched by the memory device. *See* Section IV.B *supra*. Figure 6 at most identifies transmission timing relative to the incoming clock signal; it does not identify a memory-device latching event. *Id.*

When Petitioner attempts to show the claimed latching, it points elsewhere—to Grundy’s internal “[logic level clock signal 326](#)” shown in Figure 19:



Ex. 1005 [Grundy] Fig. 19 (Patent Owner annotation). Petitioner argues that “Grundy’s clock signal drives this latching” because “Grundy’s clock signal 326 is coupled with the command buffer, and controls when command packets are loaded into the command buffer.” Pet., 50. In other words, Petitioner uses Figure 6’s incoming clock signal to identify the claimed “first rising edge,” but then uses Figure 19’s internal clock signal 326 when discussing the alleged latching event.

That two-step theory leaves an essential timing gap. Grundy explains that “a logic level clock signal 326 is generated by the signal receiver 310 coupled to the input-side clock line 152,” and that this internal clock signal is supplied to internal circuitry including the protocol engine, I/O controller, and interface register. Ex.

1005 [Grundy] [0088]. Thus, clock signal 326 is a later internal signal generated from the incoming clock after receiver circuitry. Petitioner's expert confirmed that the incoming clock and internal logic-level clock signal 326 are not identical in timing:

Q. So that clock signal provided via clock in and the logic level clock signal 326 are not the same signal, are they?

A. Not exactly. There would be some delay.

Ex. 2028 [Sechen-Tr.] 77:4–7.

He confirmed the same point again when comparing the signal labeled “Clock” in Figure 5A to Grundy's internal logic-level clock signal 326:

Q. So the signal labeled “Clock” in Figure 5A is not the same as the signal labeled “Logic level clock signal 326” in Grundy's Figure 17?

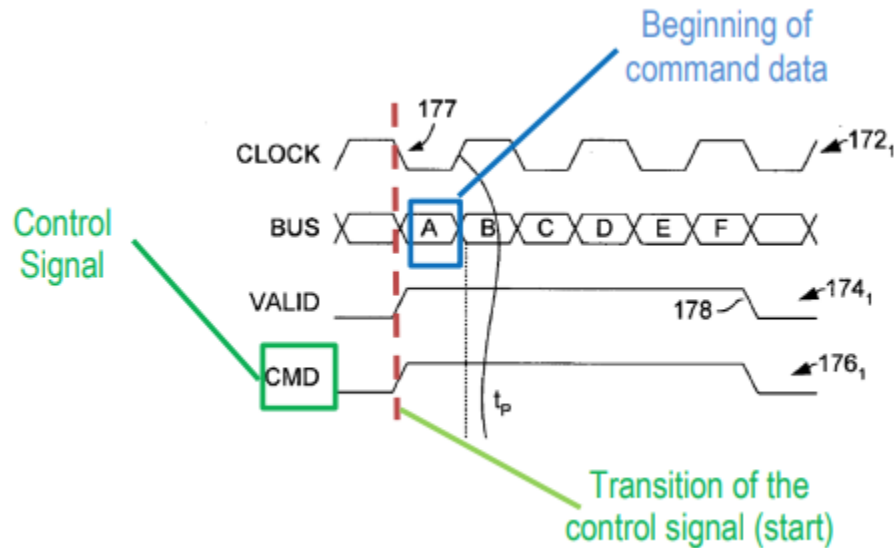
A. Yeah, there's a propagation delay there.

Id., 78:13–18. As Dr. Przybylski explains,

I agree with Dr. Sechen that a POSITA would understand there to be a delay between Grundy's “Logic level clock signal 326” and Grundy's “Clock” in Figure 5A. A necessary consequence of the existence of this delay, however, is a gap between Petitioner's occasional use of the “Clock” signal in Figure 5A and Petitioner's timing theory for claim 2. Taking Petitioner's analysis of Figure 19 for granted, for example, the delay implies that *nothing* would happen in Grundy's Figure 19 at a first rising edge of Figure 5A's “Clock” signal.

Ex. 2027 [Przybylski-Decl.] ¶ 107 (emphasis in original).

The point is not merely that Grundy's logic level signal 326 is derived from (rather than being the same thing as) the incoming clock signal. The point is that claim 2 requires a precise timing relationship, and Petitioner never proves it. Claim 2 does not merely require that command data be latched in *some kind of response* to *some* clock signal at some later time. It requires that command data be "latched *at* the first rising edge of the clock signal after the transition of the control signal," Ex. 1001 ['381] cl. 2, where "the clock signal" refers back to claim 1's "clock signal," and where "the transition of the control signal" refers back to claim 1's recitation of "wherein *a transition of the control signal* from an inactive state to an active state indicates a beginning of command data being received at the at least one common data interface." *Id.* cl. 1. The only "transition of the control signal" that Petitioner identified in Grundy in connection with claim 1 is indicated by Petitioner's annotation of part of Figure 6's depiction of transmissions from Grundy's memory controller:



Pet., 33-34. If Petitioner identifies the claimed “clock signal” as Grundy’s incoming clock on line 152 for claim 1, then Petitioner must show latching at the first rising edge of that same incoming clock signal after *this* alleged transition of the control signal. If Petitioner instead relies on Grundy’s internal clock signal 326 for the alleged latching, then Petitioner must at least show a timing relationship between the incoming clock (identified by Petitioner as the “clock signal” in claim 1), internal clock signal 326 (identified by Petitioner as a “clock signal” in claim 2), Petitioner’s alleged transition of the control signal (as identified by Petitioner in claim 1), and the alleged latching event. But the Petition does neither of these things.

As Dr. Przybylski explains:

A POSITA would understand that Grundy’s incoming clock on clock line 152 and Grundy’s internal logic-level clock signal 326 are related, but not interchangeable for purposes of the precise timing required by claim 2. Grundy states that logic-level clock signal 326 is

generated by receiver circuitry coupled to the input-side clock line. That generation process introduces delay between the incoming clock at the memory-device input and the internal clock signal used by downstream internal circuitry.

Accordingly, even if Grundy's Figure 19 is assumed to evidence some internal loading or latching of data at Grundy's memory device in response to clock signal 326, that would not establish the timing required by claim 2, unless Petitioner were also to show that this internal event occurs at the *first* rising edge of the *same* clock signal identified for claim 1 after the transition of the control signal. The Petition provides no such analysis.

Ex. 2027 [Przybylski-Decl.] ¶¶ 108-109 (emphasis in original).

Petitioner's reliance on Figure 19 has a further problem: even as to internal clock signal 326, Grundy's cited disclosure does not identify the required "first rising edge." The portion of Grundy Petitioner quotes states only that "data packets and command packets are loaded from the interface register into the input data buffer 353 and command buffer 351, respectively, one word at time in response to transitions of the clock signal 326." Ex. 1005 [Grundy] [0092]; Pet., 50. That disclosure refers generically to "transitions" of internal clock signal 326. It does not identify a first rising edge after a control-signal transition, does not tie any particular command word—such as Petitioner's value B—to such an edge, and does not relate the internal transition of clock signal 326 to the incoming clock edge Petitioner annotated in Figure 6. Thus, Petitioner's arguments based on Grundy's logic level

clock signal 326 do not show the claimed timing.

Petitioner's analysis therefore fails at the precise point where claim 2 requires precision. For claim 1 and for its annotated claim 2 timing, Petitioner relies on Grundy's incoming clock signal on clock line 152 / clock signal 172₁. For the alleged latching, Petitioner relies on Grundy's later internal logic-level clock signal 326. Petitioner never shows the required timing for either signal. It never shows that any identified command data is latched at the first rising edge of the incoming clock signal after the control-signal transition. And once Petitioner pivots to internal clock signal 326, it never supplies the additional timing analysis needed to show that an event controlled by that delayed internal signal occurs at the first rising edge of "the clock signal" required by claim 2.

For this additional and independent reason, Petitioner fails to show that claim 2 is rendered obvious.

V. PETITIONER FAILS TO SHOW THE OVERLAPPING READ/PAGE-PROGRAM LIMITATIONS OF CLAIMS 13 AND 21.

Claim 13 depends from claim 1 and requires "the control circuitry" of "the flash memory device as claimed in claim 1" to perform "the read operation during a time period that overlaps with a time period for the page program operation." Ex. 1001 ['381] cl. 13. Claim 21 recites a similar limitation as a step of a method claim, and Petitioner provides no separate analysis for claim 21, instead relying entirely upon its claim 13 analysis. *See* Pet., 70; Ex. 1003 [Sechen-Decl.] ¶ 165.

The Petition never identifies a coherent Grundy-Kilbuck combination in which the same claimed flash memory device and control circuitry mapped for the independent claims also perform the claimed overlapping operations. Instead, in connection with the limitations of dependent claims 13 and 21, Petitioner’s analysis cites disclosures relating to other embodiments—Grundy’s Figure 4A and Kilbuck’s Figures 3A/3B—that Petitioner never discusses in connection with independent claims, and which Petitioner never reconciles with its independent-claim mappings. *See* Sections V.A-V.C. Because Petitioner never identifies how these isolated disclosures are present in “Grundy-Kilbuck,” the Petition’s additional motivation-to-combine arguments for claims 13 and 21 are conclusory and unsupported. *See* Section V.D.

A. Claims 13 And 21 Require The Same Claimed Device, Operations, And Control Circuitry Mapped For The Independent Claims.

Claim 13 does not recite free-floating read and program activity somewhere in a memory system. Claim 13 depends from claim 1 and recites “[t]he flash memory device as claimed in claim 1, wherein *the* control circuitry is configured to perform *the* read operation during a time period that overlaps with a time period for *the* page program operation.” Ex. 1001 [’381] cl. 13. Claim 13 therefore carries forward the same “flash memory device,” “control circuitry,” “read operation,” and “page program operation” recited in claim 1. *Id.*, cls. 1, 13. Claim 21, which depends from method claim 17, similarly incorporates the features of its independent

claim, *id.*, cls. 17, 21, and Petitioner provides no separate analysis for claim 21, but refers back to its claim 13 theory. *See* Pet., 70; Ex. 1003 [Sechen-Decl.] ¶ 165.

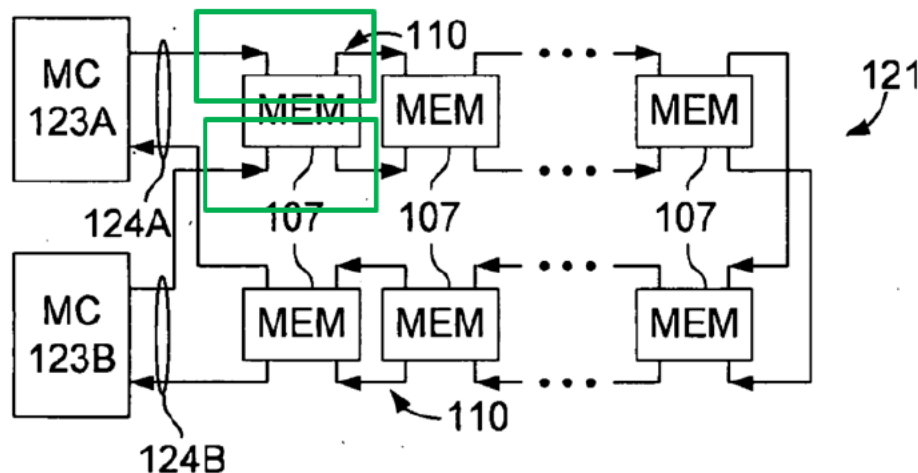
In analyzing claims 13 and 21, then, Petitioner therefore had to connect the overlapping operations of these dependent claims to the device, control circuitry, and operations Petitioner mapped for independent claim 1. For claim 1, Petitioner relies principally on Grundy's Figure 5A system and related disclosures, including the memory devices in Figure 5A, clock line 152, command line 156, multi-purpose lines 158, Figure 6 timing, and circuitry disclosed in Grundy's Figures 17, 19, and 20. *See, e.g.*, Pet., 18, 23-34, 35-39.

For claim 13, Petitioner changes focus. For the first time, Petitioner invokes Grundy's Figure 4A and Kilbuck's Figures 3A and 3B embodiments, now arguing that signaling paths and devices present in these embodiments teach the claimed overlapping read and page program operations. Pet., 67-70.

That is insufficient. Claims 13 and 21 depend from independent claims 1 and 17, respectively. Petitioner cannot show claims 13 and 21 are obvious by merely identifying potentially overlapping operations across various *disclosures* in Grundy and Kilbuck. The Petition had to identify a combination of Grundy and Kilbuck that satisfies the independent claims *and* the overlapping-operation limitations at the same time. As we now explain, the Petition never does so.

B. Petitioner’s Grundy Figure 4A Theory Does Not Reconcile Figure 4A With Petitioner’s Independent-Claim Mapping.

Petitioner’s first claim 13 theory relies on Grundy’s Figure 4A. According to Petitioner, Grundy “describes that a memory device can have multiple signaling paths,” and “[i]t would have been obvious to a POSITA to modify Grundy’s memory device in view of Kilbuck such that it can perform overlapping read and page program operations since the dual signaling paths enable such overlapping of read and page program operations,” relying upon the following annotated version of Grundy’s Figure 4A:



Pet., 67. Petitioner’s expert likewise relies on Figure 4A for an embodiment in which “each memory device has two signaling paths, one depicted on top and another depicted on the bottom.” Ex. 1003 [Sechen-Decl.] ¶ 130.

But Grundy’s Figure 4A is not the embodiment Petitioner mapped for claim 1. Petitioner’s claim 1 analysis relies principally on Grundy’s Figure 5A system and

associated disclosures. Petitioner identifies Figure 5A memory devices as examples of the claimed “flash memory device,” Pet., 18; identifies Figure 5A’s clock line 152 as carrying the claimed “clock signal,” *id.*, 23-24; identifies Figure 5A’s “set of N multi-purpose lines 158” as the claimed “common data interface,” *id.*, 25-28; identifies Figure 5A’s command line 156 as carrying the claimed “control signal,” *id.*, 31-34; and relies on Figure 6, which Grundy describes as a timing diagram for signals transmitted by the memory controller of Figure 5A, for the timing and “double data rate” aspects of claim 1. *Id.*, 29, 33; Ex. 1005 [Grundy] [0011], [0043]-[0047].

Figure 4A is a different embodiment “in which two separate signaling queues 124A and 124B, each including the same chain of memory devices 107, are controlled by separate memory controllers 123A and 123B.” Ex. 1005 [Grundy] [0041]. Figure 4A therefore introduces not merely “multiple signaling paths,” but separate signaling queues controlled by two separate memory controllers. Petitioner never explains how Grundy’s Figure 4A could be used to modify or evidence the behavior of the Figure 5A embodiment it identified in connection with claim 1. Petitioner does not identify which Figure 4A controller provides the claimed “clock signal,” which provides the claimed “control signal,” where the claimed “common data interface” is found in Figure 4A, or how Figure 6’s timing disclosures about Figure 5A apply to Figure 4A’s multi-controller system.

Petitioner simply blends Figure 5A and Figure 4A without acknowledging the difference. For example, in the claim 13 section, Petitioner quotes Grundy's description of Figure 5A's "point-to-point signaling links 153" with "clock line 152, valid line 154, command line 156 and a set of N multi-purpose lines 158," Pet., 67, while relying on Figure 4A for the alleged "dual signaling paths." But Grundy's cited "set of N multi-purpose lines 158" is part of the Figure 5A embodiment Petitioner used for claim 1. Petitioner does not show that Figure 4A includes the same interface, uses the same command/clock signaling, or operates according to the same timing.

Dr. Przybylski explains the problem:

A POSITA would understand that Grundy's Figure 4A and Figure 5A embodiments are different embodiments. Figure 5A depicts a single memory controller 151 coupled to memory devices through point-to-point links 153 that include clock, valid, command, and multi-purpose lines. Petitioner relies on those Figure 5A features for claim 1.

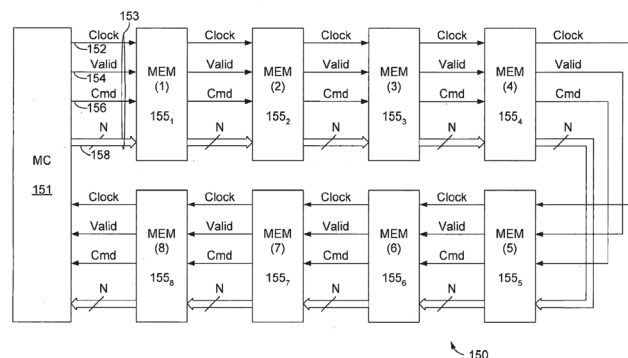


FIG. 5A

Ex. 1005 [Grundy], Fig. 5A.

Figure 4A, by contrast, depicts two separate signaling queues controlled by two separate memory controllers 123A and 123B:

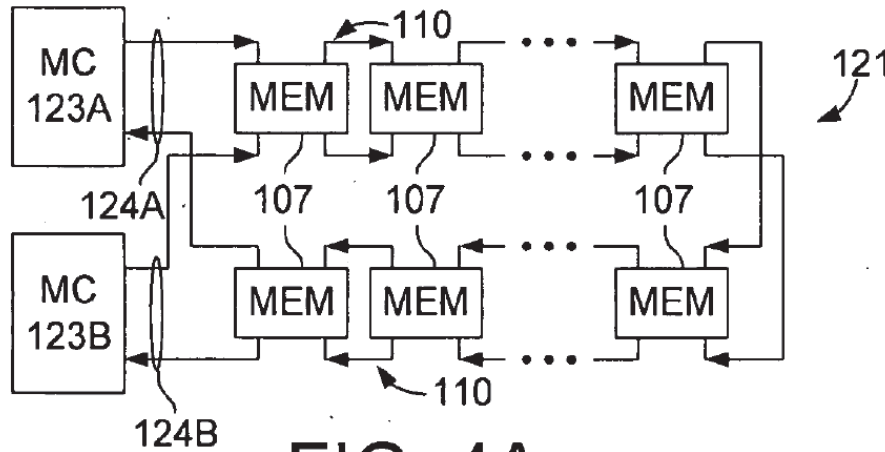


FIG. 4A

Ex. 1005 [Grundy], Fig. 4A.

The Petition does not explain how the Figure 4A embodiment supplies the same “clock signal,” “control signal,” and “common data interface” that Petitioner identified in Figure 5A. Nor does the Petition explain how Figure 6, which Grundy describes depicting the timing of transmissions made by the one memory controller of Figure 5A, applies to the two-controller Figure 4A embodiment. Without such explanation, I cannot determine what device Petitioner contends satisfies both claim 1 and dependent claim 13.

Ex. 2027 [Przybylski-Decl.] ¶¶ 123-125.

Nor does the existence of two signaling paths itself show the overlap required by claim 13. Claim 13 requires “the control circuitry” of the claimed flash memory device to be “configured to perform the read operation during a time period that overlaps with a time period for the page program operation.” Ex. 1001 [’381] cl. 13.

Petitioner never identifies control circuitry in Figure 4A that is allegedly configured to perform those overlapping operations, never identifies the read and page-program operations in the same claimed device, and never explains how commands from two separate signaling queues or two separate controllers would be coordinated to produce the claimed overlap. Petitioner simply asserts that “dual signaling paths enable such overlapping of read and page program operations.” Pet., 67. This is not an identification of control circuitry configured to perform the claimed overlapping read and page-program operations. As Dr. Przybylski further explains:

Petitioner’s analysis of claim 1 repeatedly relies on Grundy’s Figures 5A and 17, for example, *see, e.g.*, Pet., 23-25 (discussing limitation [1b]), 26-27 (discussing limitation [1c-i]), 32-33 (discussing limitation [1d]), 35 (citing Figs. 5A and 17 in connection with the alleged “control circuitry” of limitation [1e]). But nowhere in Grundy’s Figures 5A and 17, or their descriptions, is there any suggestion of having two commands operate on Grundy’s flash memory arrays in parallel in these embodiments of Grundy.

Ex. 2027 [Przybylski-Decl.] ¶ 115.

The Board should not fill these gaps. The Petition was required to identify with particularity how each challenged claim is allegedly unpatentable. Petitioner’s Figure 4A theory does not do so. It invokes a different Grundy embodiment to supply allegedly overlapping operations, but never reconciles that embodiment with the mapping on which its claim 1 analysis relies. For this reason alone, Petitioner

fails to show that Grundy's Figure 4A theory renders claim 13 or claim 21 obvious.

C. Petitioner's Kilbuck Figures 3A And 3B Theory Does Not Map A Single Claimed Flash Memory Device Or Control Circuitry.

Petitioner's second claim 13 theory fares no better. Petitioner argues that "[i]t would have been obvious to a POSITA to modify Grundy's memory device based on Kilbuck's flash memory architectures such as the one shown by Kilbuck's Figs. 3A or 3B." Pet., 69. According to Petitioner, Kilbuck teaches systems with "two or more 'Flash memory devices 314,'" *id.*, 68, and "each of Kilbuck's flash memory devices is capable of performing read operations and page program (write) operations because each has its own circuitry to access (read/program) its own flash memory array." *Id.*, 69. Petitioner then asserts that "one of Kilbuck's memory devices can perform a read operation during a time period that overlaps with a time period for a page program operation which is performed by another one of Kilbuck's memory devices." *Id.*

This theory does not show claim 13. Claim 13 depends from claim 1 and requires "the control circuitry" of "*the* flash memory device as claimed in claim 1" to be configured to perform the overlapping read and page-program operations. Ex. 1001 ['381] cl. 13. But Petitioner's Kilbuck theory relies on multiple distinct Kilbuck "Flash memory devices 314," with one device performing a read while another device performs a page program. Pet., 69. Petitioner never explains how those multiple distinct Kilbuck devices become the single claimed "flash memory

device,” or how the “control circuitry” of that single claimed device is configured to perform the claimed overlapping operations.

Kilbuck itself distinguishes the relevant structures. Kilbuck’s Figure 3A depicts a “Flash memory subsystem 304” that includes a “memory controller 312” and “one or more NAND architecture Flash memory devices 314 internal to it.” Ex. 1006 [Kilbuck] [0040]. Kilbuck’s Figure 3B similarly depicts a subsystem including a memory controller 312, one or more Flash memory devices 314, and additional SDRAM/DDR memory. *Id.*, [0041]-[0042]. Thus, the disclosures Petitioner cites concern a subsystem containing multiple flash memory devices, not a single flash memory device whose identified control circuitry performs both claimed operations in the required overlapping manner.

Petitioner tries to avoid that problem by saying that “[a] POSITA would have incorporated two or more of Kilbuck’s flash memory devices in Grundy’s memory device such that Grundy’s memory device can perform overlapping operations in response to receiving commands on respective signaling paths.” Pet., 69. But that assertion only creates another gap. Petitioner never identifies the resulting “Grundy’s memory device” after this incorporation. It never explains whether the claimed “flash memory device” is a Grundy memory device, a Kilbuck Flash memory device 314, Kilbuck’s larger subsystem 304, or some newly aggregated structure composed of multiple Kilbuck devices inside a Grundy device. Nor does

Petitioner identify where, in that alleged structure, the claim 1 “clock signal,” “control signal,” “common data interface,” and “control circuitry” are found.

The “respective signaling paths” language also ties Petitioner’s Kilbuck theory back to the same unresolved Figure 4A problem discussed above. Petitioner’s expert cites Grundy’s Figure 4A for the proposition that commands may be received on separate signaling paths. Ex. 1003 [Sechen-Decl.] ¶¶130-133. But, as explained in Section V.B, Petitioner never reconciles Grundy’s Figure 4A embodiment with the Figure 5A-based mapping used for claim 1. Petitioner therefore has not shown how Kilbuck’s multiple-device subsystem, inserted into some version of Grundy, satisfies the same claim 1 device and interface limitations from which claim 13 depends.

Dr. Przybylski explains:

Kilbuck’s Figures 3A and 3B depict a flash memory subsystem containing multiple Flash Memory Devices 314 controlled by a memory controller 312. A POSITA would understand those Flash Memory Devices 314 to be distinct devices within the subsystem. Thus, Petitioner’s assertion that one Kilbuck device may read while another Kilbuck device programs does not, by itself, show that a single claimed flash memory device has control circuitry configured to perform the overlapping operations required by claim 13.

To map Kilbuck’s Figures 3A and 3B to claim 13, Petitioner would need to explain what structure in the proposed Grundy-Kilbuck combination is the claimed “flash memory device,” what structure is the claimed “control circuitry,” and how that same device and control

circuitry satisfy the claim 1 limitations while also performing the overlapping operations of claim 13. The Petition does not provide that explanation.

Ex. 2027 [Przybylski-Decl.] ¶¶ 117-118.

Petitioner's Kilbuck theory therefore fails for the same basic reason as its Figure 4A theory: it identifies a feature that might suggest overlapping operations within parts of *some* system, but it never maps these features to the devices or control circuitry of the '381 patent. Claim 13 is not satisfied by showing that one device in some system might read while another device in some system programs. Petitioner needs to show a single device that satisfies claim 1 and is configured to perform the claimed overlapping operations of claim 13. Because Petitioner does not do so, its Kilbuck Figures 3A/3B theory fails. This same failure defeats claim 21, for which Petitioner offers no separate analysis. *See* Pet., 70; Ex. 1003 [Sechen-Decl.] ¶165.

D. Petitioner's Motivation Theory Is Conclusory And Unsupported.

Petitioner's challenge to claims 13 and 21 also fails because Petitioner never provides a reasoned motivation to make the modifications its theory would require. Petitioner states that "[i]n addition to the reasons provided [for the independent claims], a POSITA would have been further motivated to make this modification to increase operational speed and/or provide 'fast random read/write and/or burst capabilities.'" Pet., 68. But Petitioner never defines "this modification" with enough specificity to make its assertion meaningful.

As explained above, Petitioner’s claim 13 theory departs from the Figure 5A-based mapping used for claim 1 and introduces new theories based on Grundy’s Figure 4A and Kilbuck’s Figures 3A and 3B. Petitioner’s Figure 4A theory appears to require modifying the Figure 5A-based Grundy device to include separate signaling queues controlled by separate memory controllers. *See* Ex. 1005 [Grundy] [0041]; Section V.B *supra*. Petitioner’s Kilbuck theory appears to require incorporating “two or more of Kilbuck’s flash memory devices in Grundy’s memory device.” Pet., 69; Section V.C *supra*. And Petitioner’s reference to overlapping operations “in response to receiving commands on respective signaling paths,” *id.*, appears to combine the Kilbuck multi-device theory with Grundy’s Figure 4A multi-path, multi-controller embodiment. The Petition never identifies how these disclosures fit together in a device that teaches the entirety of claim 13 or 21.

A petitioner cannot establish a motivation to combine by asserting a desired result—here, overlapping read and page-program operations—and then leaving the Board to infer that some system would allegedly achieve it. *Magnum*, 829 F.3d at 1380-81. Nor is a generic desire for improved speed enough. Petitioner had to explain why a POSITA would have combined the features on which Petitioner relies in the manner recited in the claims. *See TQ Delta*, 942 F.3d at 1360-61. The Petition does not do so.

Petitioner’s reliance on Grundy’s Figure 4A underscores the problem. Figure

4A does not merely add a second path to the Figure 5A embodiment. Grundy describes Figure 4A as having “two separate signaling queues 124A and 124B,” each controlled by a separate memory controller, “123A and 123B.” Ex. 1005 [Grundy] [0041]. If Petitioner’s modification depends on those separate controllers issuing overlapping read and page-program commands to the same chain of memory devices, the Petition needed to explain how those controllers would coordinate commands, avoid conflicts, and preserve the claim 1 signaling structure Petitioner mapped elsewhere. It does not. Dr. Przybylski explains:

Petitioner’s proposed modification is not sufficiently defined to evaluate. If Petitioner is relying on Grundy’s Figure 4A, then the proposed system includes two separate signaling queues controlled by separate memory controllers. If those controllers are permitted to issue overlapping read and page program commands to the same memory device or same memory array, the system must address scheduling and arbitration issues. For example, one controller could issue a read command to a location at or near the same time another controller issues a program command affecting that same location. The order in which those commands are performed may determine what data is returned by the read operation.

A POSITA would understand that a system allowing overlapping operations from multiple controllers would need a mechanism for coordinating such operations or preventing conflicts. The Petition does not identify any such mechanism in Grundy, Kilbuck, or the proposed combination. Nor does the Petition explain how the alleged modified

device would maintain the clock, control signal, common data interface, and control circuitry mappings Petitioner relied on for elements of independent claims.

Ex. 2027 [Przybylski-Decl.] ¶¶ 134-135.

Petitioner's expert confirmed that Grundy's Figure 4A leaves such coordination issues unresolved. When asked how Figure 4A handles write operations from multiple controllers, Dr. Sechen testified that it "might depend on how a processor outside of Figure 4A is configured." Ex. 2028 [Sechen-Tr.] 80:12–25. Such testimony confirms that the proposed modification depends on system-level coordination that is neither disclosed in Grundy nor supplied by the Petition.

Nor does Kilbuck cure the defect. Kilbuck's "fast random read/write and/or burst capabilities" are tied to its own flash memory devices. *See* Ex. 1006 [Kilbuck] [0032], [0040]-[0042]. Petitioner never explains how or why a POSITA would import Kilbuck's multiple-device subsystem into Grundy's Figure 5A/Figure 4A architecture in any particular way as to satisfy claims 13 and 21. Petitioner likewise never explains why doing so would predictably yield the claimed overlap within the same claimed flash memory device and control circuitry, rather than merely producing a broader system containing multiple devices that operate independently.

Thus, Petitioner says a POSITA would have modified Grundy to increase speed, but never identifies the modified architecture, explains how it satisfies the independent and dependent limitations together, and never addresses coordination

issues introduced by its theory that depend on details not supplied by Petitioner that would impact the speed of the device. Such a conclusory narrative cannot provide a motivation to combine.

VI. CONCLUSION

The patentability of the challenged claims should be confirmed.

Respectfully submitted,

Dated: May 27, 2026

By: /Kenneth Weatherwax/

Kenneth Weatherwax (Reg. No. 54,528)

Nathan Lowenstein (*pro hac vice*)

Dennis Courtney (*pro hac vice*)

Colette Woo (*pro hac vice*)

LOWENSTEIN & WEATHERWAX LLP

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITS

This Patent Owner Response (the “POR”) consists of 13,977 words, excluding table of contents, table of authorities, certificate of service, this certificate, or table of exhibits. The POR complies with the type-volume limitation of 14,000 words as mandated in 37 C.F.R. § 42.24. In preparing this certificate, counsel has relied on the word count of the word-processing system used to prepare the paper (Microsoft Word).

Respectfully submitted,

Dated: May 27, 2026

By: /Michael Cosley/

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the following documents were served by electronic service, by agreement between the parties, on the date below:

PATENT OWNER RESPONSE

EXHIBIT 2027

EXHIBIT 2028

EXHIBIT 2029

The names and addresses of the parties being served are as follows:

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Respectfully submitted,

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By: /Michael Cosley/