

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INFINEON TECHNOLOGIES AMERICAS CORP.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

Case IPR2025-01487
Patent 9,972,381

EXHIBIT 2027

DECLARATION OF STEVEN PRZYBYLSKI, Ph.D.

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I.	Petitioner Fails To Show “transferring command data, address data, input data and output data to and from the at least one common data interface” (Element [17b-i]) is present in the presented prior art.	63
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I. INTRODUCTION

1. My name is Steven Przybylski. I have been retained as an expert witness to provide my independent opinion in regard to the matters at issue in *inter partes* review of U.S. Patent No. 9,972,381 (“the ’381 patent”) in IPR2025-01487. I have been retained by MOSAID Technologies Inc. (“MOSAID” or “Patent Owner”), the Patent Owner in this proceeding. I will refer to the petitioner in this proceeding, Infineon Technologies Americas Corp., as “Infineon,” or as “Petitioner.”

2. I am being compensated at my regular hourly rate for my time spent working in connection with this case. My compensation is in no way related to the outcome of this litigation. If called as a witness, I would testify as to the statements and opinions contained in this report.

3. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

II. QUALIFICATIONS

4. My qualifications, including past cases in which I offered an expert opinion, are stated more fully in my curriculum vitae which is attached to this declaration as Appendix A. I also provide a brief summary of my qualifications here.

5. I earned a Bachelor of Applied Science from the University of Toronto in 1980. I was enrolled in the Engineering Science program, completing a course of study combining the Electrical Engineer and Computer Science options. I earned a Master of Science in Electrical Engineering degree and a Ph.D. in Electrical Engineering in 1982 and 1988 respectively, both from Stanford University. I also earned a Masters of Business Administration from the Haas School of Business at the University of California at Berkeley in 2000.

6. I have extensive experience with memory integrated circuits and memory systems constructed using them, including flash memory systems.

7. At Stanford, my dissertation was on the optimization of single- and multi-level cache hierarchies to maximize system-level performance. Also at Stanford, I was a member of the core team that architected, designed, built, and tested the seminal MIPS processor. I was responsible for the design of the instruction decode and control units as well as architecting the virtual memory support. I assembled and debugged the entire microprocessor design and oversaw its fabrication and testing.

8. In 1984 and 1985, I took a leave of absence from Stanford to become a member of the founding team of MIPS Computer Systems, a startup in California that designed, built, and sold processors and computer systems. In 1989, after

finishing my doctorate and brief post-doctorate at Stanford, I returned to MIPS Computer Systems.

9. Throughout my two periods of employment at MIPS Computer Systems, I had a number of titles and worked on a variety of projects. Noteworthy were stints as processor architect, systems architect, hardware-software team liaison, and Chief Scientist of the High-End Systems group. During the second period, I also served as a Consulting Assistant Professor in the Department of Electrical Engineering at Stanford. I designed and taught an advanced graduate level course on cache and memory system design.

10. In 1991, I left MIPS to become an independent consultant. In that capacity I have provided technical, strategic, marketing, and intellectual property services to a large number of clients both domestically and internationally.

11. The technical consulting I performed was principally related to advancements in semiconductor memories and their application in systems. Specifically with respect to non-volatile memories and Flash memories in particular, I advised companies on a variety of memory types and on trends in NAND and NOR Flash memories and the processes used in their manufacture. In the 2000s, I helped develop a new NAND Flash architecture and separately a universal memory interface that was optimized for use in heterogeneous memory systems and that was equally applicable to DRAMs and to NAND Flash devices.

12. I am a member of both the Institute of Electrical and Electronics Engineers (IEEE) and the Association of Computing Machinery (ACM). In addition, in 1997 I became a registered patent agent. I am listed as the inventor on 11 domestic patents and their foreign counterparts. The subject matters of these patents include memory devices, memory subsystems, networks, error detection and correction codes, processors and cache memories.

13. Between 1994 and approximately 2000, I was a leading independent analyst following, writing, and teaching about both the technical and business aspects of the DRAM industry.

14. Overall, I have written three books and over 25 articles in the areas of memory, processors, and computer systems. In particular, I wrote and revised an 850-page book entitled “New DRAM Technologies: A Comprehensive Analysis of the New Architectures.” I have presented many lectures, classes and seminars on semiconductor memories and their memory systems, processors and computer systems. I have presented full and half-day seminars on DRAMs, Flash memories, other memory types, and the memory systems constructed with them to over 2,500 engineers, marketers, managers, and financial analysts.

III. BASES OF OPINIONS

15. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited in the Petition and herein, including materials from the list below:

- i. U.S. Patent No. 9,972,381 (Ex. 1001) (“the ’381 patent”),
- ii. U.S. Patent No. 9,972,381 File History (Ex. 1002),
- iii. Expert Declaration of Carl Sechen, Ph.D. (Ex. 1003) (“Sechen-Decl.”),
- iv. Curriculum Vitae of Carl Sechen, Ph.D. (Ex. 1004),
- v. U.S. Patent App. Pub. 2004/0148482 to Grundy et al. (Ex. 1005) (“Grundy”),
- vi. U.S. Patent App. Pub. 2005/0204091 to Kilbuck et al. (Ex. 1006) (“Kilbuck”),
- vii. Petitioner’s excerpts from Wiley Electrical and Electronics Engineering Dictionary, 2004 (Ex. 1007),
- viii. T. Tanaka et al., “A quick intelligent page-programming architecture and a shielded bitline sensing method for 3 V-only NAND flash memory,” in IEEE Journal of Solid-State Circuits, vol. 29, no. 11, pp. 1366-1373, Nov. 1994, doi: 10.1109/4.328638 (Ex. 1008) (“Tanaka”),

- ix. P. Cappalletti et al., “Flash Memories,” Kluwer Academic Publishers, 1999 (excerpts) (Ex. 1009) (“Cappalletti”),
- x. Complaint, MOSAID Techs. Inc. v. Infineon Techs. AG et al., W.D. Tex., filed March 25, 2025 (Ex. 1010).
- xi. Transcript of the Deposition of Dr. Carl Sechen dated April 24, 2026 (Ex. 2028).
- xii. JESD79-2 DDR2 SDRAM Standard dated September 2003 (Ex. 2029).

16. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

17. All emphases (such as bolding, underlining, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. APPLICABLE LEGAL STANDARDS

A. Level Of Ordinary Skill In The Art

18. My understanding of a “person of ordinary skill in the art” is as described to me by the attorneys for MOSAID. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA,” “POSA,” or “PHOSITA,” as of the time of the invention. I understand

that the earliest provisional application to which the '381 patent claims priority was filed on September 30, 2005—a date that the Petition refers to as the “Critical Date.”

Pet., 2. Accordingly, I treat this date as the time of the inventions claimed in the '381 patent. I reserve the right to revisit this issue should Petitioner make arguments premised upon some other date being taken as the date of invention. I have been told that the person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I am instructed that in this context, “relevant” means relevant to the challenged claims of the '381 patent.

19. I have been told that factual indicators of the level of ordinary skill in the art include the various prior art approaches employed, the types of problems encountered in the art, the rapidity with which innovations are made, the sophistication of the technology involved, and the educational background of those actively working in the field. I have been told that, in assessing the level of skill of a person of ordinary skill in the art, one should consider the type of problems encountered in the art, the prior solutions to those problems found in the prior art references, the rapidity with which innovations are made, the sophistication of the technology, the level of education of active workers in the field, and my own experience working with those of skill in the art at the time of the invention.

20. In this case, Dr. Sechen has asserted in his declaration that a person of ordinary skill in the art as of the time of the '381 patent would have had

a bachelor of science degree in electrical engineering, computer engineering, or a related field, and at least three years of experience in the research, design, or development of electronic memory circuits. Additional education could substitute for experience and vice versa.

Ex. 1003 [Sechen-Decl.] ¶ 31; *see also* Pet., 8.

21. For purposes of this declaration, I accept Dr. Sechen's proposed qualifications of a POSITA.

22. As further discussed below, my opinions as stated in this declaration are valid even if the Board adopts a somewhat higher or somewhat lower level of ordinary skill in the art than proposed. For example, as will be discussed throughout my report, Petitioner has not shown that a person with the level of knowledge or experience described by Dr. Sechen would have had a motivation to combine the elements of the cited art as proposed by Petitioner as of the priority date of the '381 patent, and I would hold this opinion even if the Board were to adopt a somewhat higher or somewhat lower level of ordinary skill in the art. I reserve the right to revisit this issue, however, if additional evidence or argument regarding this issue is brought to my attention.

23. In this report, the absence of an expressed opinion about any section or paragraph of the Petition or Dr. Sechen's declaration, does not indicate my agreement with the section or paragraph.

B. My Understanding Of Legal Standards

24. When considering the '381 patent and stating my opinions, I rely on the following legal standards as described to me by the attorneys for MOSAID.

25. I understand that a patent claim is unpatentable if the claimed invention was anticipated by a prior art reference or would have been obvious to a person of ordinary skill in the art at the time of the purported invention.

26. I understand that anticipation requires that every limitation of the claim at issue be disclosed, either expressly or under principles of inherency, in a single prior art reference.

27. I understand that inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Instead, it must be proven that the claim limitation not expressly found in the reference necessarily follows from what is found there.

28. I understand that an obviousness analysis involves comparing a claim to the prior art to determine whether the claimed invention would have been obvious to a person of ordinary skill in the art at the time of the invention in view of the prior art and in light of the general knowledge in the art as a whole. I also understand that

obviousness is ultimately a legal conclusion based on underlying facts of four general types, all of which must be considered: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) any objective indicia of non-obviousness.

29. I also understand that obviousness may be established under certain circumstances by combining or modifying the teachings of the prior art. Specific teachings, suggestions, or motivations to combine any first prior art reference with a second prior art reference can be explicit or implicit, but must have existed before the date of purported invention. I understand that prior art references themselves may be one source of a specific teaching or suggestion to combine features of the prior art, but that such suggestions or motivations to combine art may come from the knowledge that a person of ordinary skill in the art would have had.

30. I understand that a reference may be relied upon for all that it teaches, including uses beyond its primary purpose, but also including teachings that lead away from the invention. I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the invention, although the mere disclosure of alternative designs does not teach away.

31. I further understand that whether there is a reasonable expectation of success in combining references in a particular way is also relevant to the analysis.

32. I understand that it is improper to use hindsight to combine references or elements of references to reconstruct the invention using the claims as a guide. My analysis of the prior art is made from the perspective of a person of ordinary skill in the art at the time of the invention.

33. I am not offering any legal opinions in this declaration nor am I qualified to do so. I only consider such legal standards in framing my opinions and conclusions as well as placing assertions made by Petitioner in the Petition into the proper context. Additionally, from a subject matter perspective, I understand that the petitioner always has the burden of persuasion regarding a challenge of patentability of an invention under an inter partes review.

V. CLAIMS AT ISSUE (CLAIMS 1–21)

34. I understand that Petitioner has challenged the claims 1-21 of the '381 patent in a single ground, based on obviousness over Grundy in view of Kilbuck. Pet., 1. The '381 patent has two independent claims, claim 1 and claim 17. Petitioner's arguments relating to independent claim 17 incorporate the elements of Petitioner's arguments relating to independent claim 1. *See generally* Pet., 42-47. Similarly, Petitioner's arguments regarding dependent claims 2-16, which depend from claim 1, incorporate Petitioner's arguments regarding independent claim 1, and Petitioner's arguments regarding claims 18-21, which depend from claim 17, incorporate Petitioner's arguments regarding independent claim 17 (which, in turn,

as already mentioned, incorporate elements of Petitioner's arguments relating to independent claim 1). Because the Petition focuses in large part on independent claim 1, for example, I have therefore focused my analysis largely upon Petitioner's arguments regarding independent claim 1. I will not expressly indicate every time that, by virtue of Petitioner's incorporation of arguments by reference, an opinion I have as to one claim (for example, claim 1) also impacts other claims. Unless otherwise noted, however, my opinions in connection with any aspect of one claim would also apply to any other claim where Petitioner incorporates arguments about that aspect by reference.

35. I reserve the right to supplement the opinions expressed here if new evidence or argument is brought to my attention.

VI. OPINIONS

A. Overview Of The '381 Patent.

36. Historically, Flash memories have had interfaces that have been much slower and more limited than those of DRAMs. This largely was because the internal operations and organizations of commercially available Flash memory devices did not facilitate high bandwidth or low latency data transfers. As Flash memories became more important through the first decade of the present century in a wide variety of system types, the standard low bandwidth high latency Flash interfaces became increasingly a bottleneck. The inventors of the '381 patent sought

to alleviate this growing bottleneck by innovating around internal organization and the interface of Flash memories and the corresponding memory system structures to make Flash memories higher performance and thus more useful. The interfaces in the 2005 time frame typically operated at 20 – 30MHz, which was inadequate for the present and future Flash applications. It was impractical to simply dramatically increase the interface frequency. Further, increasing the width of the interface was also not desirable. Indeed, it was desirable, if possible, to decrease the number of pins allocated to the interface.

37. Figure 2A shows an exemplary embodiment: a Flash memory device with two standard Flash memory arrays (202 and 204) and 2 separate link interfaces (205 and 207) coupled with an address and data switch (206).

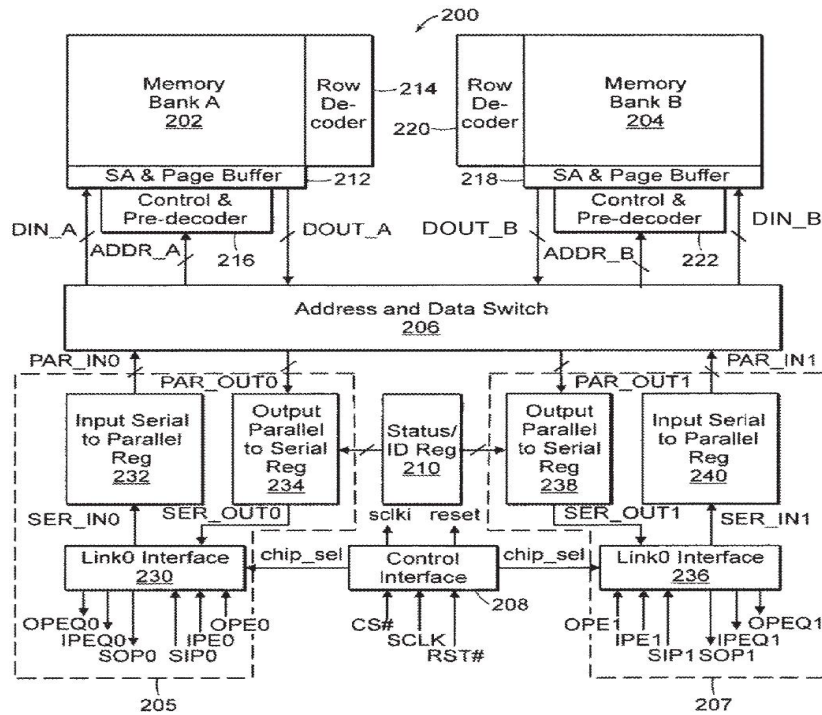
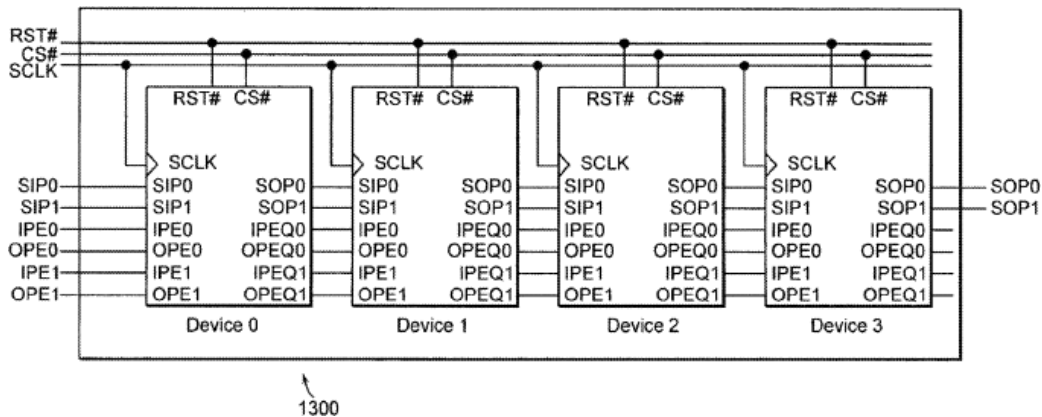


FIG. 2A

Ex. 1001 ['381], Fig. 2A.

38. This embodiment receives serial data including commands, address and program data and passes it on to the next device in a daisy-chain configuration that facilitates high performance memory systems, optionally using memory modules, as shown in Figure 13A.



Id., Fig. 13A.

39. Since the two links are independent, data can be transferred simultaneously from different memory devices, but also from different banks within a single device, greatly increasing both the bandwidth and flexibility of the memory system architecture.

B. Overview of Grundy.

40. Grundy is a patent application entitled “Memory Chain.” Grundy relates to high-speed memory systems and components of high-speed memory systems and discloses a memory device with a memory interface that includes a serial link. This facilitates a memory system comprising a plurality of memory devices in a ring.

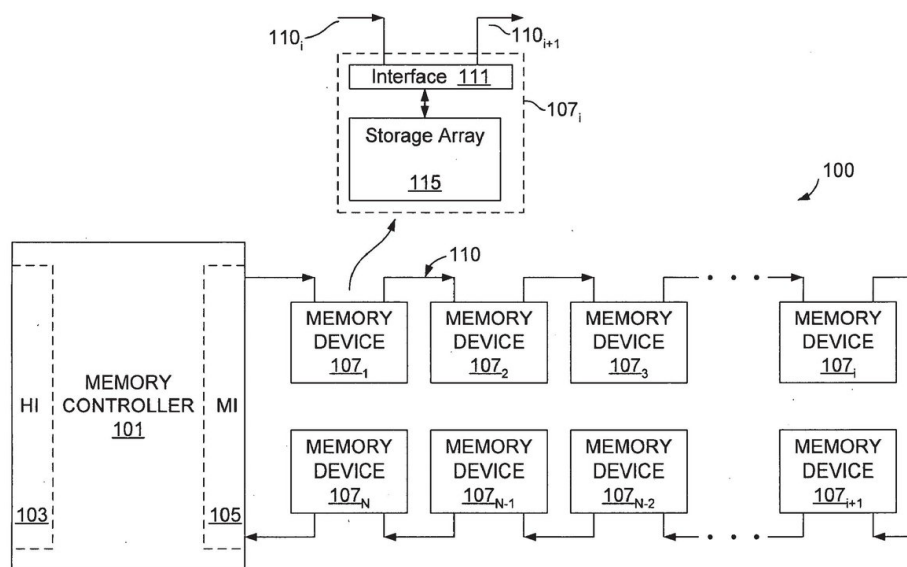
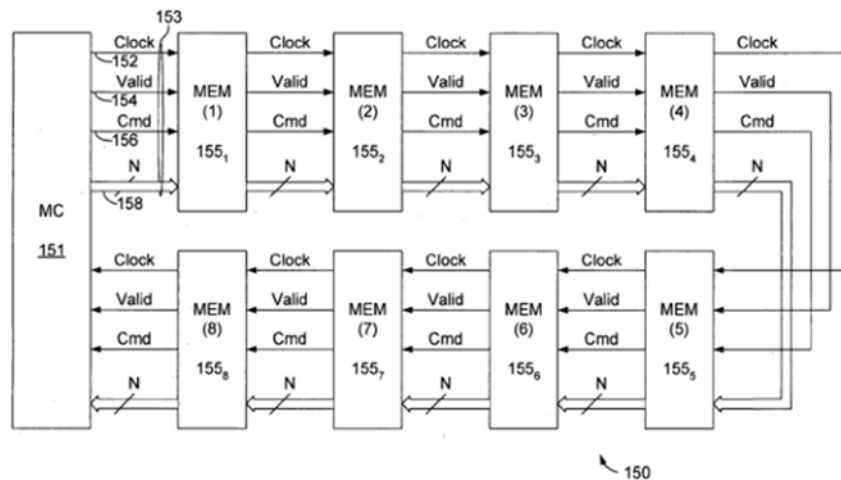


FIG. 3

Ex. 1005 [Grundy], Fig. 3.

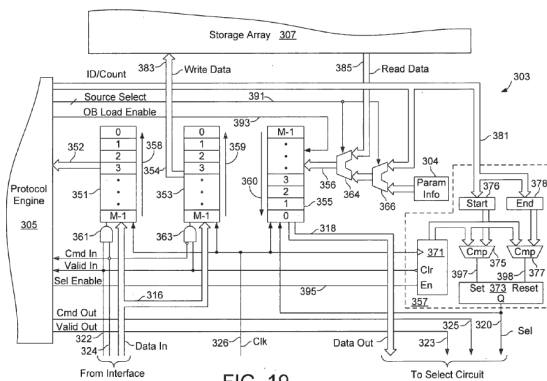
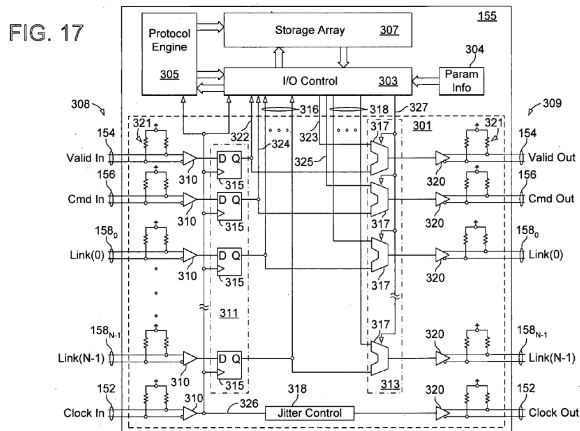
41. Grundy's disclosure focuses on the interface 111 and the links 110_i and is relatively agnostic about the type of non-volatile memory being compounded into this ring-structured memory system. The physical dimensions or the maximum number of memory devices in the ring are not discussed.

42. Grundy's links 110 are used to convey clock, command, and data lines. Auxiliary lines include a Valid indicator and a Command indicator.



Ex. 1005 [Grundy], Fig. 5A.

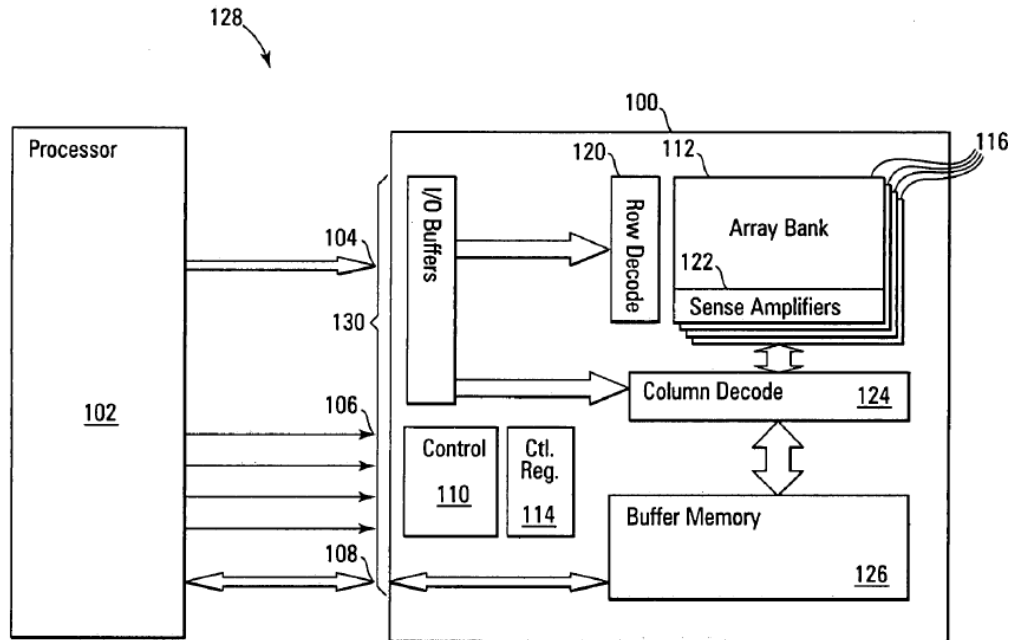
43. Grundy also includes a number of logic diagrams that show the internal structure of an interface unit. This implementation shows single-data-rate input and output ports as well as command recognition and decode functions.



Ex. 1005 [Grundy], Figs. 17, 19.

C. Overview of Kilbuck.

44. Kilbuck discloses a high-density non-volatile memory device or system with a synchronous interface along the lines of a conventional SDRAM interface. The non-volatile memory device includes an address unit/interface, a control unit, and a data interface/unit. Together these allow the processor or intermediate memory controller to initiate read and write accesses to the memory device. Kilbuck's memory device also includes an internal memory controller that directs internal operations such as managing the Flash memory array.

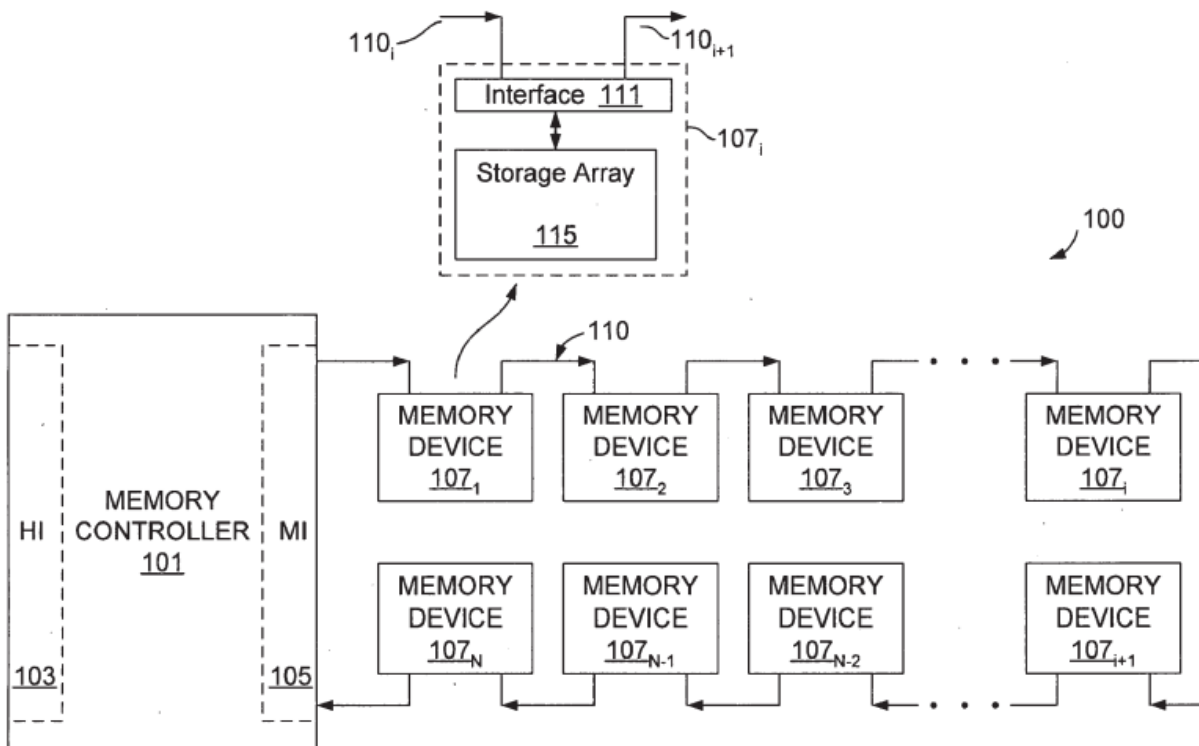


Ex. 1006 [Kilbuck], Fig. 1.

D. Petitioner Does Not Show A Motivation To Combine.

45. The Petitioner offers only one ground: obviousness in view of what Petitioner terms “Grundy-Kilbuck,” which is some combination of Grundy and Kilbuck. *See* Pet., 1. Petitioner does not contend that either Grundy or Kilbuck alone renders the claims obvious. *See id.* As I will explain below, however, Petitioner does not explain why a POSITA would be motivated to arrive at the combination that Petitioner terms “Grundy-Kilbuck,” let alone do so with a reasonable expectation of success. Petitioner’s failure to explain this is, at least in part, a consequence of Petitioner’s failure to elaborate relevant aspects of the design choices that define what “Grundy-Kilbuck” even is.

46. Petitioner’s element-by-element analysis of claim 1 begins with Grundy, and, in particular, with Grundy’s Figure 3. *See* Pet., 17-18. Grundy’s Figure 3 depicts a memory controller 101 coupled to a chain of memory devices 107, each having its own signaling interface 111 and storage array 115:



Ex. 1005 [Grundy] Fig. 3; *see also id.*, [0035].

47. Grundy explains that its “storage arrays” need not be homogeneous and may include arrays of different types (including “magnetic and optical media”), but also that each “storage array” has a single point of access and control, such that “separate memory controllers for the various storage types are not needed.” *Id.*, [0035].

48. Petitioner relies upon Grundy's memory devices as the claimed "memory device[s]" (Pet., 17-18) and elsewhere relies exclusively on Grundy for various claim limitations. *See, e.g.*, Pet., 25-28 (relying exclusively on Grundy for the claimed "common data interface"), 31-34 (same, for the claimed "control input port").

49. Petitioner describes the role of Kilbuck in "Grundy-Kilbuck" combination by stating, for example, that "Kilbuck provides additional details of flash memory systems including its associated circuitry." Pet., 13. Petitioner further characterizes "the Grundy-Kilbuck Combination" as "the application of a known technique (Kilbuck's techniques for implementing flash memory) to a known system (Grundy's memory system) to achieve predictable results (a memory system with flash memory and supportive circuitry)" in which "[e]ach element in combination merely performs the same function as it does separately." Pet., 16.

50. Petitioner never identifies what "details" from Kilbuck are incorporated into Grundy's memory devices 107, or how. When combining memory circuitry, however, such specifics are crucially important. The specifics of the combination can plainly affect whether and how the proposed combination operates, whether and how a POSITA might (or might not) be motivated to arrive at that combination, and whether and how a POSITA who *was* assumed to have the motivation to make that combination would actually have a reasonable expectation of success in doing so.

51. In fact, the Petition never clearly identifies what the proposed combination is supposed to be. Throughout the Petition, trying to understand the exact proposed combination is like standing on quicksand that is always shifting underfoot. By repeatedly invoking “to the extent that it is argued that Grundy does not teach or suggest” an element or a portion of an element then Kilbuck does, Petitioner does not provide the POSITA with enough information to understand what the proposed combination actually is or how exactly it is proposed to operate. Without that context, it is difficult to assess or rebut whether a POSITA would have been motivated to arrive at “Grundy-Kilbuck,” or be able to make this combination (whatever it is) with a reasonable likelihood of success. One is instead left to assess the plausibility of the various alternatives offered by Petitioner, not in reference to any patent claim as a whole, but with respect to individual claim limitations.

52. The list of limitations that Petitioner applies this tactic to is long: a plurality of erasable blocks (Pet., 19-21), pages of flash memory comprising a plurality of flash memory cells (Pet., 21-22), the execution of a page program operation to store input data into a selected page of a Flash memory (Pet., 36-38), and a status register to indicate a status of the flash memory device (Pet., 40-41). For each of these elements which may or may not implicate Kilbuck as part of the combination, Petitioners do not explain how these things are to be combined with

any one embodiment of Grundy (or multiple embodiments of Grundy) to construct a working Flash memory device that satisfies all of the claim elements.

53. Petitioner's element-by-element approach begins with claim 1. Rather than map all of claim 1 onto a single combination whose features are clearly articulated as coming from a specified combination of Grundy, or Kilbuck, or the knowledge of the POSITA, Petitioner proceeds on a limitation by limitation basis, invoking different disclosures as need be. For example, Kilbuck's flash memory structures and logic and device level circuitry are invoked "to the extent" the required claim elements are not found in Grundy without explanation of a rationale of any details of the presumed combined embodiment.

54. Not only is Petitioner not clear as to which aspects of Kilbuck are to be included in the Grundy-Kilbuck combination, but it is equally vague about what Kilbuck is being combined with. Grundy includes several embodiments that include significant differences from one another. For example, Grundy's Figures 3 and 4B at a minimum show different numbers of memory controllers with different devices being accessible by each. Also, though the Petition frequently refers to the embodiment of Figure 3, the Petitioner refers to other embodiments of Grundy as well. Pet., 67. Thus, what Petitioner refers to as "Grundy-Kilbuck" may apparently rely upon different base embodiments of Grundy, depending on context.

55. Nor did Dr. Sechen supply details of the combination that Petitioner left to the imagination. At his deposition, for example, Dr. Sechen said that he “focus[ed] on” implementations of Grundy where “all these memory devices were flash memory devices,” but that his analysis of the motivation to combine did not depend upon the number of such devices, or whether the devices in an implementation of Grundy were identical to one another or not, or whether some of the devices in the implementation of Grundy were flash memory devices and others were not (although he granted that he “ha[d]n’t really considered that possibility.” Ex. 2028 [Sechen-Tr.] 39:14–18, 40:12–41:9, 41:10–16. This “possibility” is expressly contemplated by Grundy, Ex. 1005 [Grundy] [0035] (“[T]he storage arrays 115 within the memory devices 107 need not be homogeneous. Rather, storage arrays of different types (e.g., different underlying storage media) and/or capacity may be provided in different memory devices of the chain, thereby enabling diverse memory systems to be constructed according to application needs and yet with a single point of access and control (i.e., separate memory controllers for the various storage types are not needed).”), and in my opinion, whether a POSITA would be motivated to arrive at some particular implementation of Grundy (whether or not modified by Kilbuck or knowledge of the POSITA) might well depend on the number and nature of devices in Grundy’s “memory chain.”

56. Claim 1 requires [1e] “a ***control circuitry*** configured to execute a page program operation to store the input data on a selected page, and to execute a read operation to retrieve the output data from the flash memory cells in accordance to the command data and address data received at the at least one common data interface.” Petitioner’s analysis of this limitation is incomplete. It does not identify a single “control circuitry” within the presumed hypothetical combined device. Petitioner instead alternates among several different control structures and hypothetical devices. For example, Petitioner begins by asserting that “each of Grundy’s ***memory devices*** includes control circuitry configured to execute operations associated with various commands such as read and write commands.” Pet., 35. In the same paragraph, however, Petitioner also asserts that “Grundy’s ***memory controller*** also includes control circuitry configured to execute operations associated with various commands.” *Id.* It is not clear how Petitioner understands this element to be satisfied by Grundy. Petitioner’s analysis points simultaneously to device-level control in the memory devices and system-level control in the memory controller. Next, the Petition invokes Kilbuck “to the extent” that Grundy is alleged not to disclose flash-specific operations. *See e.g.*, Pet., 37, 39. In this circumstance, Petition relies on Kilbuck for program and read operations under the control of Kilbuck’s own internal memory controller.

57. This ambiguity and lack of specificity of the proposed combination is not remedied by Petitioner’s expert declaration. Dr. Sechen purports to find the required control circuitry somewhat specifically in Grundy’s memory devices and a memory controller 151, both of which include circuitry to execute operations. Ex. 1003 [Sechen-Decl.] ¶¶ 96-97, 101-102. Then, with similar specificity, Dr. Sechen purports to find control circuitry in Kilbuck, configured as to execute operations. Ex. 1003 [Sechen-Decl.] ¶ 100, 103. But Dr. Sechen never describes a combination of Grundy and Kilbuck or indicates which of one of these exemplary circuitries provide the claimed control circuitry in “Grundy-Kilbuck.”

58. Returning to the Petition, where all possible control circuits are cited to, the possible combination of Grundy and Kilbuck includes any of the three controllers in the prior art: the one in Kilbuck and the two in Grundy. Petitioner does not disclose the relationships between these three, in the case that Kilbuck is part of the combination, nor does Petitioner expressly discuss the case where Kilbuck is not part of providing this circuitry.

59. From a technical perspective, Petitioner’s analysis does not identify a single implementation of the claimed ‘control circuitry’ within a ‘flash memory device.’ Grundy describes both device-level control functionality—*e.g.*, memory devices that monitor and respond to commands—and a system-level memory controller that issues and coordinates those commands. *See* Ex. 1005 [Grundy]

[0032]-[0033], [0036]. Kilbuck, by contrast, describes a flash memory device having an internal controller that manages flash-specific operations such as page selection, programming, and reading. *See* Ex. 1006 [Kilbuck] [0030]-[0031].

60. Petitioner does not identify which of these control structures is the claimed ‘control circuitry,’ nor does the Petition explain how or whether Kilbuck’s internal controller would be incorporated into Grundy’s memory devices or reconciled with Grundy’s command propagation and signaling architecture. As a result, it is unclear what specific device is alleged to include the claimed control circuitry, or how the proposed combination would operate as a single flash memory device that performs the claimed page program and read operations.

61. This is material because the alternatives suggested (Grundy alone and Grundy with Kilbuck incorporated) are significantly different systems. Altering Grundy’s memory controller and the role it plays in the memory systems changes the nature of flash-management functionality. For example, If Kilbuck’s flash-specific controllers were incorporated into each of Grundy’s memory devices, then each device would need to include flash-management functionality related to page selection, programming control, and related operations. This would alter the role of Grundy’s memory controller and require additional coordination between multiple device-level controllers within the chain.

62. If, instead, Grundy’s memory controller were to be unchanged in the combination and such functionality were centralized in Grundy’s memory controller, then that system-level controller—not any circuitry within a memory device—might be responsible for executing the claimed operations, which would not correspond to the claimed “control circuitry” of a “flash memory device.” Petitioner does not address these materially different implementations or explain how any of them yields a single device having the claimed control circuitry operating in accordance with the claimed interface.

63. A similar lack of specificity in the proposed combination of Grundy and Kilbuck occurs in the Petition and Declaration with regard to the status register claimed in element [1f]. Again, the Petitioner fails to map this limitation to a single, defined device. Rather, Petitioner relies on Grundy for the general concept of “status requests” and “status responses,” invoking Kilbuck “to the extent” that it is argued that Grundy does not teach or suggest the limitation. *See, e.g.,* Pet., 41 (asserting that, “to the extent” Grundy does not disclose a status register, Kilbuck does). As with limitation [1a], Petitioner thus does not identify a concrete structure within a defined device, but instead conditionally substitutes Kilbuck’s flash-device implementation for Grundy’s system-level behavior.

64. Incorporating Kilbuck’s status register into Grundy’s system would require defining where that register resides, how it is accessed through Grundy’s

command protocol, and how it interacts with the control circuitry responsible for executing flash operations. Petitioner does not address any of these issues. Without such an explanation, it is unclear how Petitioner's "Grundy-Kilbuck" is alleged to include the claimed 'status register,' or how that register is used in the proposed combination.

E. Petitioner Fails To Show A Double-Data-Rate Interface Required by Element [1c-ii] (Claim 1).

65. Elements [1c-i] and [1c-ii] together recite:

at least one common data interface configured to transfer command data, address data, input data and output data,

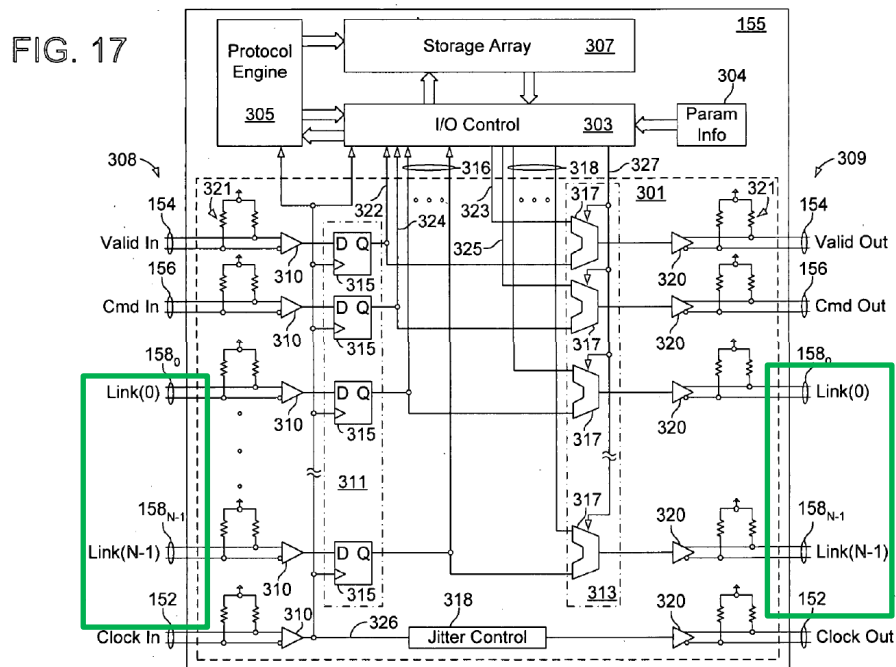
wherein at least one of command data, address data, input data and output data is transferred in synchronization with both rising and falling edges of the clock signal when the flash memory device is in a double data rate configuration ...

Ex. 1001 ['381], 27:52-58.

66. The claim thus recites a double-data-rate configuration of the flash memory device in which transfer is synchronized with both the rising and falling edges of the clock signal. Petitioner's approach to this element, which relies exclusively on Grundy, Pet., 26-28, is flawed.

67. Petitioner's presentation begins with a discussion of Grundy's ring architecture, illustrated by Figure 5A, Pet., 26, identifying the data links in that figure with the claimed common data interface, being "used at alternate times to transfer

N-bit wide data values and command values.” Pet 25-26. In annotating Figure 5A, the Petition highlights the bus going into MEM(1) and the bus coming out of MEM(1) (in green) indicating their commonality. This citation is paired with a citation to Grundy’s paragraph [0044], which says that the “bus may be a point-to-point link as in FIG. 5A, or a multi-drop structure.” Pet., 26; *see also* Ex. 1003 [Sechen-Decl.] ¶ 80 (quoting Ex. 1005 [Grundy] [0044]). The Petition identifies the Figure 17 embodiment of Grundy as the embodiment of the organization of Figure 5A that shows the input and output ports in more detail and identifies the differential input and output ports 308 and 309, respectively.



Pet., 27 (displaying Ex. 1005 [Grundy], Fig. 17, as annotated by Petitioner).

68. The second half of element [1c] requires that when in a DDR configuration, data be “transferred in synchronization with both rising and falling

edges of the clock signal.” Ex. 1001 [’381] 27:55-57. For this, Petitioner points to the top half of Figure 6, annotated to show rising and falling edges of CLOCK and two pieces of data (A and B) on the bus. Pet., 29-30 (discussing Grundy’s Figure 6, as annotated by Petitioner), Ex. 1003 [Sechen-Decl.] ¶ 86 (stating that Figure 6 evidences double-data-rate data transfer).

69. A problem with this presentation with regard to element [1c] as a whole is Petitioner’s reliance on Figure 17 and the other related figures (Figures 19, 20 and 21) of Grundy. The Petition appears to acknowledge that Figure 17 includes only one set of single edge-triggered D-flip flops storage elements 315, each of which can only capture one bit of information on every complete cycle of the clock. The input circuitry depicted in Figure 17 only can capture 1 datum (e.g. the A datum) per cycle, and not both the A datum and the B datum as would be required in a double-data-rate configuration.

70. This figure, as well as other figures disclosing aspects of the implementation, notably Figures 19, 20, and 21, disclose a single-data-rate transfer in which data capture and the subsequent processing and data output only happens in synchronization with one of the two edges of the clock. The Petition implicitly acknowledges where Grundy states that the implementation of Figure 17 is a single-data-rate design when the Petition quotes Grundy’s disclosure that the storage elements 315 shown in Figure 17 could achieve double-data rate capture by

“providing ... a *second set* of storage elements 315 to capture outputs of the differential receivers 310 in response to a falling edge of the clock signal.” Pet., 30 (quoting Ex. 1005 [Grundy] [0088]). Here, a POSITA would understand Grundy to be describing a *modification* of Grundy’s Figure 17. Grundy’s Figure 17 has one set of storage element 315, each of which can capture one bit per cycle in their disclosed form, unmodified by the modification proposed in Grundy’s paragraph 88. Grundy’s description of unmodified Figure 17 makes clear that this embodiment is incompatible with the disclosure of Figure 6. A POSITA would recognize this and realize that Figure 6 in view of unmodified Figure 17 would not meet the requirements of element [1c-ii].

71. Further, in paragraph [0088], Grundy says “In one embodiment, the interface register 311 includes edge-triggered storage elements 315 (e.g., D flip-flops) coupled to outputs of the differential receivers 310 and having strobe inputs coupled to receive the clock signal 326 to capture signals generated by the differential receivers 310 at each rising edge and falling edge of the clock signal 326.” Ex. 1005 [Grundy] [0088]. This is technically inaccurate at a basic level. A POSITA would understand that a “D flip-flop,” properly drawn in Figure 17 with the standard symbol for this circuit, captures data only on the rising edge of its clock signal, never on the rising edge and the falling edge of its clock signal. A POSITA reading this disclosure would also understand that the disclosure of Grundy needs

adjustment or clarification before it is usable in the way that Petitioner proposes it could be used.

72. The Petition tries to address double-data-rate issue by referring to the last portion of paragraph [0088] of Grundy:

In one implementation, such double-data rate capture is achieved by providing a first set of storage elements 315 to capture outputs of the differential receivers 310 in response to each rising edge of the clock signal 326, and a second set of storage elements 315 to capture outputs of the differential receivers 310 in response to a falling edge of the clock signal 326 (or in response to a rising edge of a complement of the clock signal 326).

Ex. 1005 [Grundy] [0088].

73. An embodiment of Figure 17 modified in the way proposed by this sentence could indeed potentially capture $2N$ bits of data per cycle, though not necessarily the command data or received data supposed by Petitioners. But the hypothetical embodiment of Grundy suggested by this proposed modification of Figure 17 (in view of paragraph [0088]) in combination with Grundy's Figures 19, 20, and 21 (presumably unmodified, as neither Petitioner nor Petitioner's expert discusses modifying them) would be a non-functional hodgepodge apparently capable of accepting double-data-rate input data and commands, but which does not have the internal facilities to process or respond to that data at that rate.

74. The internal buses of Figure 17 are single-data rate by-N buses, and the entire output stage receiving data from the input buffers and the I/O control and driving that data via differential buffers 320 is single-data rate. This output stage of the Figure 17 embodiment cannot drive the signals depicted on the bottom portion of Figure 6. In addition, if one takes the suggestion of the last portion of paragraph [0088] seriously in order to transform the memory device 155 into a double-data-rate memory device, the apparently simple modification of doubling the number of D flip flops 315 (and causing half to capture on one edge of clock the other half to capture of the opposite edge of the clock) unlocks a Pandora's box of additional design difficulties that show how the apparently simple duplication of flip flops as described in paragraph [0088] is not enough to describe a flash memory device in a double data rate configuration.

75. In light of this, if all of the memory devices of Figure 5A were changed according to the description found in [0088] as apparently suggested by Petitioner, then the first bus could have data transmitted at double data rate, but that data would not be received or operated on at DDR speeds. Further, since all of the memory device cannot *transmit* at double-data-rate speeds, none of the other memories in the ring would transmit at double data rate, and so none of the buses in the ring would transfer data according to a double-data-rate configuration.

76. There are additional reasons why the disclosure of Grundy's paragraph [0088] as suggested by Petitioner fails to satisfy the language of element [1c-ii]. First, the two ranks of D flip flops hypothesized in the second half of [0088] necessarily capture data out of phase from each other as one set is clocked by the rising edge of Clock 326 and the other is clocked on the falling edge of Clock 326. These two N-bit quantities need to be temporally aligned before the different portions of the memory controller in the memory device can use them together and on a single clock edge. This alone is not trivial, and the Petition does not explain how achieving this would be obvious to the POSITA.

77. Once each pair of N-bit input words is aggregated into a single 2N-bit word with consistent timing (i.e. temporally aligned with each other), all the data buses in Figures 17 and 19 would have to be doubled in width. The command buffer, the input data buffer, and output buffer would also have to be doubled in width. Correspondingly, the protocol engine optionally could interpret 2N bits of command and address at a time.

78. The largest source of complexity related to the forcing of double-data-rate links into the embodiment of Grundy derives from the difference between t_P and t_D in Figure 6. t_D is clearly about a phase longer than t_P . As odd as this would seem to a POSITA, a quick review of Figure 17 shows the absence of any mechanism that would equalize the paths for clock and data. The difference in these delays derives

from the fact that the path from Clock Out on the memory controller to Clock Out on the first memory device is longer than the path from the Bus output on the memory controller to a Bus output on the first memory device. This mismatch means that subsequent memory devices receive the first N-bit chunk of data and the corresponding VALID and CMD signal on the Bus relative to a random phase of its input clock depending on its position in the ring. This variability can be very difficult to compensate for, particularly in a double-data-rate environment.

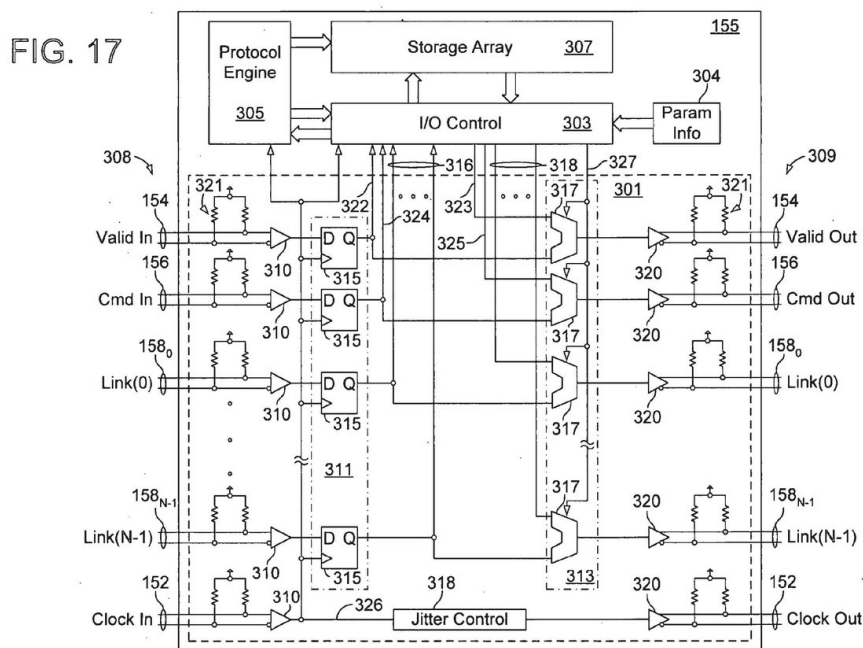
79. In conclusion, with regard to a double-data-rate configuration, the disclosure of Grundy is incomplete and non-functional. Petitioners chose to rely on Grundy alone, without looking to Kilbuck or another reference to address Grundy's deficiencies. The consequences of this choice are fatal with respect to their attempt to show element [1c], and consequently to the attempt to show claim 1 obvious as a whole, because the modifications to Figure 17 suggested by Grundy's paragraph 88 are not carried through to modifications of other components of Grundy such that the result is a functioning system.

F. Grundy's Input Receiver Circuits Are Flawed.

80. There is another issue with Grundy's Figures 6 and 17 related to element [1c-ii] and several subsequent claims that Petitioners do not address. Simply put, the timing diagram in Figure 6 and the input and output circuitry of Figure 17, aside from the lack of double-data-rate operation, is clumsy to the point

of incompetence and non-functional regardless. Again, Petitioner and Petitioner's expert take isolated disclosures in Grundy at face value and do not attempt to reconcile them.

81. In a nutshell, the input circuitry for all of the incoming signals on the left-hand side of the memory device 155 in Figure are treated identically.



Ex. 1005 [Grundy], Fig. 17.

82. Each differential signal 152-158_{N-1} that together make up the signaling link 153 encounters a pair of termination resistors 321 and then the inputs to a differential receiver 310, all of which are presumed to be identical. Figure 6, below, shows the data and control signals and clock all leaving the memory controller towards MEM(1) at approximately the same time.

83. Without any indication otherwise from Grundy, and because the figures throughout the patent do nothing to dispel the suggestion of roughly similar path lengths for the various busses, clocks and control signals, a POSITA would have no reason to expect a systematic shift in the relative arrival times of the signals at MEM(1) or their delay through the input buffers of that memory device. Thus the D flip-flops 315 will experience their input D signal transitioning at approximately the same time as their clock input. A POSITA would recognize, however, that a DFF has to have its triggering clock edge (e.g. the rising edge of clock for D flip-flops with this symbol) occur while its data input D is stable at the value to be captured. If clock and D change at approximately the same time, the value captured is indeterminate and not guaranteed.

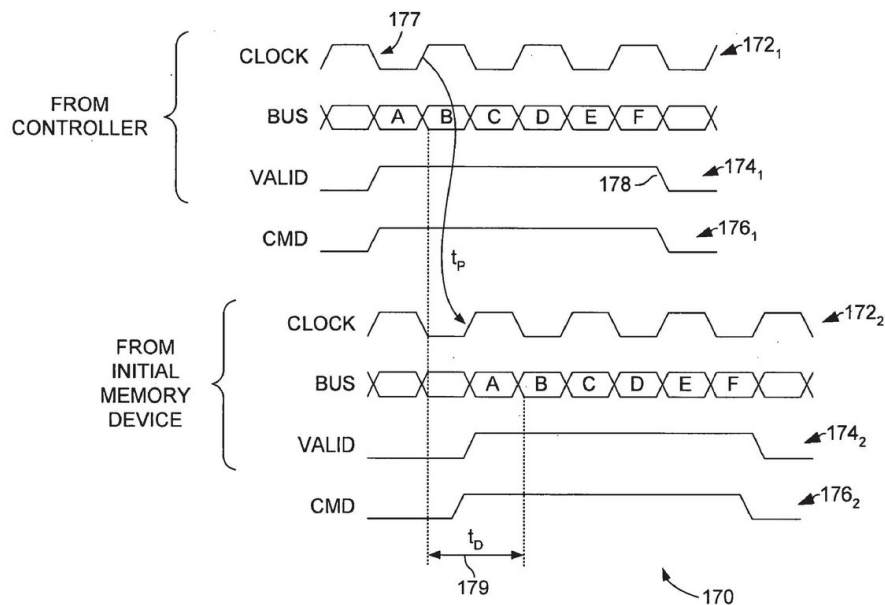


FIG. 6

Ex. 1005 [Grundy], Fig. 6.

84. This idea that Clock has to change when data is stable is especially well understood in the domain of JEDEC defined SDRAMs with DDR data transfers. For example, for DDR2 SDRAMs, the standard for which was first published in September 2003, a DQS signal is sent in parallel with the data signals to facilitate the capture of the data in the memory much the same as the Clock signal in Grundy. But as seen in Figure 29 from JESD79-2, data that is being written to the memory array has the corresponding edges of the differential DQS offset by a $\frac{1}{2}$ phase (i.e. $\frac{1}{4}$ cycle) so that the DQS always transitions in the middle of the data eye on DQ.

2.2.4.4 Burst Write Operation (cont'd)

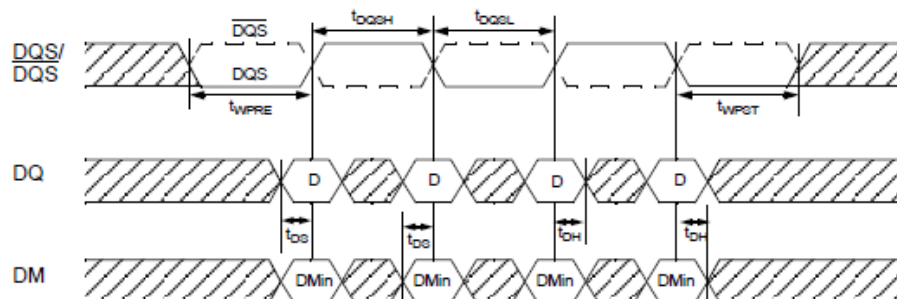


Figure 29 — Data Input (Write) Timing

Ex. 2029 [JESD79-2] (DDR2 SDRAM Standard, September 2003), Fig. 29.

85. In Grundy, since Clock is not offset relative to the data eyes in Figure 6, proper capture of the data requires that Clock In must be delayed by a quarter cycle (or half a phase) to make sure that the DFFs 315 are receiving a rising clock edge when the probability of properly capturing the data is maximized—or at least is non-zero. Grundy does not do this and a POSITA would recognize this as a fatal

flaw in the disclosure of Grundy. Thus, with the particular alignment of the CLOCK signal and the data eyes on the Bus in Figure 6 combined with the use of D flip flops as depicted in Figure 17, any attempt to capture the Bus values after they traverse the differential input receivers would fail. It would be clear to a POSITA that the disclosure of Grundy is broken and no data—command or otherwise—can be captured in the input receiver 311. But since the Petitioners accept and use Grundy as is without modification of correction, both the DDR claim element ([1c-ii]) and the latching of the command data element ([2], see Section VI.G *infra*) of claim 1 and at least element [17b] of claim 17 are not shown in Grundy or Petitioner’s “Grundy-Kilbuck” by Petitioner’s analysis.

G. Petitioner Fails To Show “the command data is latched at the first rising edge of the clock signal after the transition of the control signal” (Claim 2).

86. Claim 2 recites the flash memory device of claim 1 “wherein the command data is latched at the first rising edge of the clock signal after the transition of the control signal.”

87. When Grundy discloses that “[i]n the embodiment of FIGS. 5 and 6, the transmit interval is a half cycle of the clock signal 172₁ such that a new command or data value is transmitted on the bus in response to each rising and falling edge of

the clock signal 172₁ following edge [177],”¹ Grundy is describing how its *memory controller* places data on its bus in response to rising and falling edges of the clock signal 172₁ that the memory controller is itself also outputting. A POSITA would understand that each data value depicted in the top half of Figure 6 arrives at the memory device 155₁ somewhat later than shown due to the transmission delay between the memory controller and the first memory device MEM(1) 151₁. In contrast, the indicated time delay t_p , which is the delay from the CLOCK signal leaving the controller to when the CLOCK signal leaves the initial memory device, includes this transmission delay as well as the time from the clock signal arriving at MEM(1) and the time that it is sent on towards MEM(2). Grundy’s Figures 5, 6, and 17 do not offer any indication how much of T_p is spent in transit from the memory controller to the initial memory device, and how much of it is spent in that memory device traversing the input pads (not shown), the input receives 310, the internal clock net 326, the Jitter Control circuit 318, and the output drivers 320. Consequently, we cannot know from Figure 5 or 6 when exactly the embodiment of Grundy is plausibly capturing data from the bus or whether that capturing is at all possible given the circuitry disclosed in Figures 17 etc. *See* Section IV.F *supra*.

¹ As Petitioner indicates, Grundy’s reference to “edge 167” of Figure 6 is most likely a typographical error, and “edge 177” was intended. Pet., 29 n. 8.

88. Petitioner's expert confirmed the same point in deposition. He agreed that the upper portion of Figure 6 depicts "the timing of signals being transmitted from Grundy's controller MC 151 to the first device, 1551, in the chain depicted in Figure 5A." Ex. 2028 [Sechen-Tr.] 44:7–11; *see also id.*, 50:21-51:1. When asked directly about Petitioner's claim 2 theory for value B, he confirmed that Figure 6 does not show the required latching:

Q. [I]f we were looking at, say, the left edge of this rectangle, Figure 6 is not depicting that the value B is latched at Grundy's memory device 155₁ at the time of that left edge of this rectangle; is that correct?

A. That's correct.

Q. Would the value B be latched at Grundy's memory device 155₁ at the time indicated by the right edge of the rectangle?

A. No, we cannot say that.

Q. Would it be possible to indicate on Figure 6 the first time at which the value B would be latched at Grundy's memory [device] 155₁?

A. No.

Ex. 2028 [Sechen-Tr.], 60:22-61:12.

89. Grundy's Figure 6 depicts the timing of signals transmitted by the memory controller, not the timing of when those signals are latched. A POSITA would not understand Figure 6 to show when any value is latched at the memory

device. As a threshold matter, neither Fig. 6 nor Fig. 5A conveys any information about the physical placement of these devices or the lengths of the links between them. A POSITA therefore cannot assume any particular relationship between the transmit time from one device and the receive time at the next, other than that the link propagation delay is some part of the overall propagation delay t_p . Because Figure 6 similarly does not depict when data is captured after being received, it does not show that any data is latched at a particular clock edge at a specific time, let alone “at the first rising edge of the clock signal after the transition of the control signal” as required by claim 2.²

90. Grundy’s disclosures concerning interface register 311 and command buffer 351 do not supply the missing timing information. The interface register disclosure indicates that receiver outputs may be captured using edge-triggered storage elements. The command-buffer disclosure indicates that command packets may later be loaded from the interface register into command buffer 351 in response to transitions of internal clock signal 326. These are internal device operations that are distinct from the controller-side transmission timing depicted in Figure 6.

² This paragraph focuses on Grundy’s Figure 6 because Figure 6 is the focus of Petitioner’s analysis of claim 2. *See* Pet., 47-50. As discussed elsewhere, were the POSITA look to other disclosures in Grundy such as Grundy’s Figure 17, which Petitioner does not discuss in connection with claim 2, these disclosures would not show that the claim is satisfied. *See, e.g.*, paragraph 95 (discussing Grundy’s Figure 17); *see also, e.g.*, Section VI.F (discussing Grundy’s Figures 6 and 17 generally).

91. Even assuming that these disclosures show that command information is captured or loaded somewhere inside Grundy's memory device, they do not show that the command data identified by Petitioner is latched "at the first rising edge of the clock signal after the transition of the control signal." In particular, Grundy does not tie the loading of command buffer 351 to the specific edge annotated by Petitioner in Figure 6, and Petitioner does not identify any disclosure that does so.

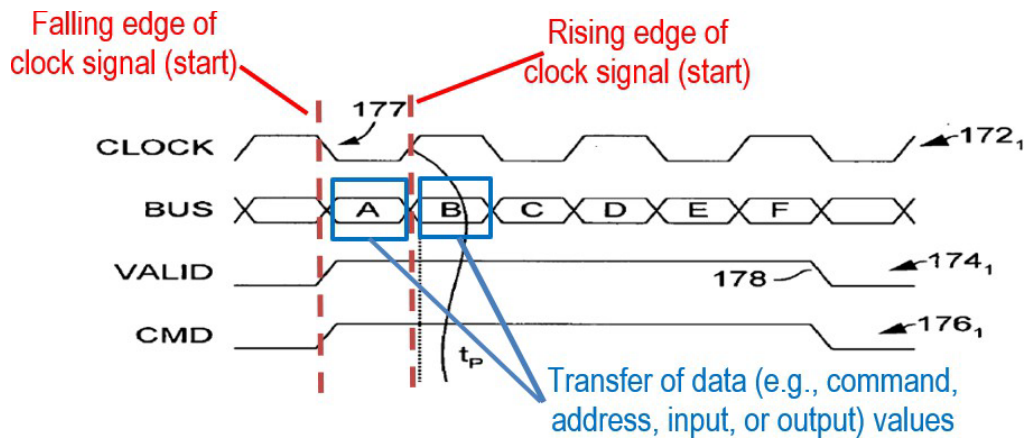
92. Grundy's Figure 6, again, is not a timing diagram of latching inside memory device 155₁. The upper portion of Figure 6 shows the timing of signals driven by Grundy's memory controller 151 to the first Grundy memory device 155₁. The lower portion shows the timing of signals later retransmitted by memory device 155₁ onto the next point-to-point link. The link length and hop time are not specified elsewhere in Grundy (or otherwise discussed by Petitioner), and so the reception and capture times relevant to Grundy's Figure 6 cannot be inferred indirectly from Grundy's disclosure. In particular, neither portion of Figure 6 indicates the time at which memory device 155₁ receives, captures, or latches any particular bus value.

93. This distinction is important because claim 2 requires command data to be latched at the flash memory device at a particular clock edge. A value being driven onto a bus by the memory controller is not the same thing as that value being latched by the memory device. Likewise, a value being retransmitted by the memory device is not the same thing as the earlier latching of that value within the memory

device. Whether and when data is latched would depend upon the timing of the incoming signals at the memory-device input circuitry, the receiver circuitry, the internal clocking used by the memory device, and any subsequent buffering. Figure 6 does not identify any latching within the memory device or any timing relative to a purported “first rising edge of the clock signal after the transition of the control signal.” Accordingly, a POSITA would not understand Figure 6 to show that value B—or any other alleged “command data” identified by Petitioner—is latched by memory device 155₁ at the claimed time.

94. Accordingly, a POSITA would not understand Figure 6 to show that value B—or any other alleged “command data” identified by Petitioner—is latched by memory device 155₁ at the first rising edge of the clock signal after the transition of the control signal.

95. A POSITA would recognize, as Petitioner’s expert did, that in the top half of Figure 6, the data eyes for each of the pieces of data on the bus show that valid data begins after the corresponding edge in clock is complete. Simply put, as annotated by Petitioners, the left edge of each blue block (indicating valid data) is after the dashed red line, indicating the transition of the clock. So not only does Figure 6, in conjunction with Figures 5 and 17, not teach about the latching of data by the flash memory device at the first rising edge of the clock signal, it affirmatively shows that this would not be possible outside the memory device either.



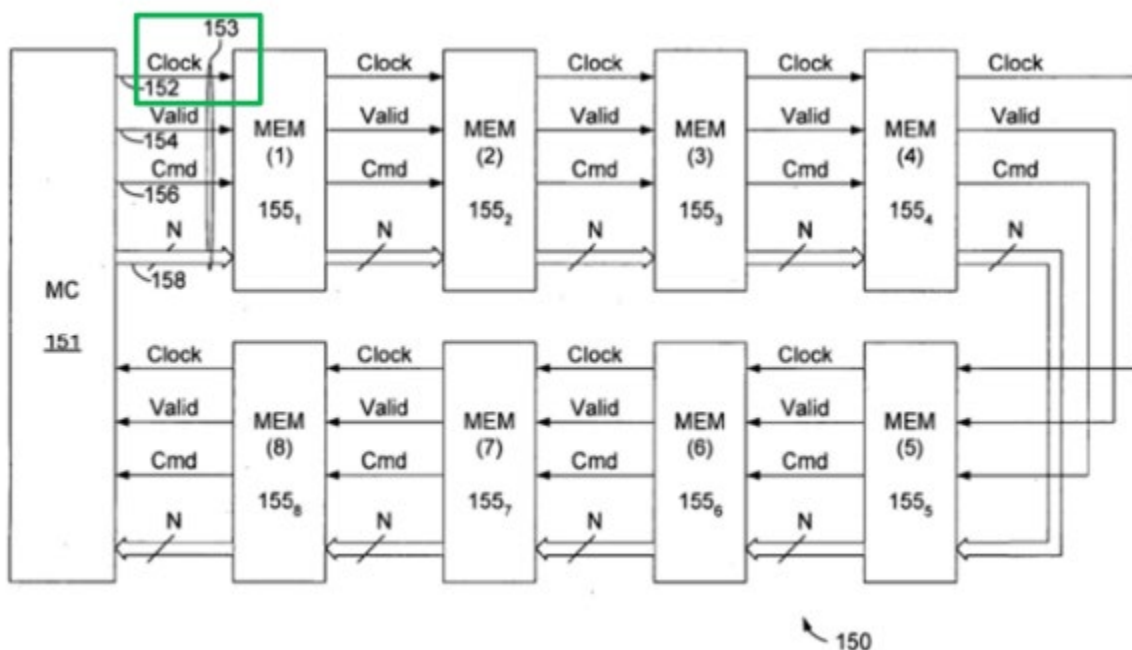
Petition at 29, showing Ex. 1005 [Grundy], Fig. 6, excerpted and annotated.

96. With regard to the reference in the text of claim 2 to the latching of command data, it is clear from the above that the embodiments of Figure 6 and/or Figure 17 do not latch or capture any command data at the first rising edge of the clock signal, either within the memory device or otherwise.

97. I do not agree that the cited disclosures evidence data being “latched” precisely when Petitioner’s bare annotation of Figure 6 suggests that it occurs, *i.e.*, “at the first rising edge of the clock signal after the transition of the control signal,” as required by claim 2. In particular, for example, Grundy’s disclosure of its memory device loading “command packets” into its “command buffer” “*in response to* transitions of the clock signal,” *id.*, is non-functional and regardless does not imply that the data any “command packet” is latched at “a first rising edge of the clock signal” as claim 2 requires.

98. Petitioner’s analysis of claim 2 also conflates two distinct signals, alternatively identifying both of them with the “clock signal” recited in claim 2 and in claim 1 from which claim 2 depends.

99. For claim 1, Petitioner first identifies the claimed “clock signal” as the clock signal received at Grundy’s memory device over clock line 152. Pet., 23-24. One example of Petitioner’s identification is provided by Petitioner’s annotation of Grundy’s Figure 5A, where the “Clock” line between Grundy’s memory controller 151 and the first memory device 1551 is highlighted by Petitioner and identified in the Petition with the claimed “clock signal.”

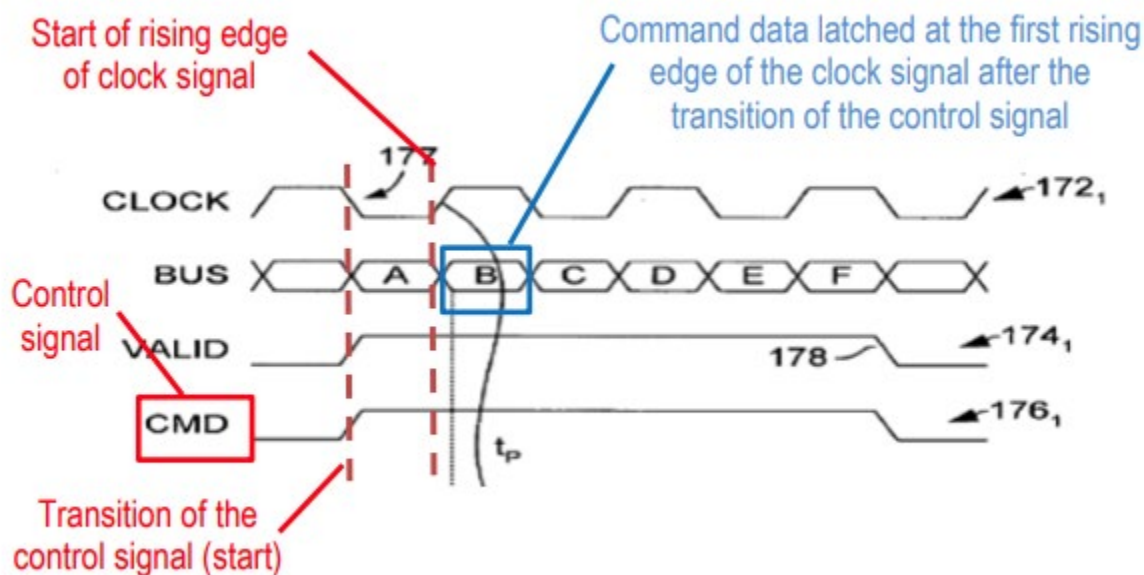


Pet., 23 (Grundy’s Figure 5A, annotated by Petitioner).

100. Petitioner also cites Grundy’s disclosure that each point-to-point link includes “a clock line 152” used “to conduct a clock signal,” *id.*, 23-24, and relies

on Grundy's Figure 17, where the corresponding input to the memory device is labeled "Clock In." *Id.*; Ex. 1005 [Grundy] Fig. 17. Thus, for claim 1 at least, Petitioner appears to identify the claimed "clock signal" with the incoming clock signal provided to the first memory device in Grundy's chain at its clock input.

101. Petitioner's claim 2 analysis initially appears to use the same clock. Petitioner's annotation of Grundy's Figure 6 identifies the "Start of rising edge of clock signal" on the controller-side "CLOCK" waveform, corresponding to Grundy's clock signal 172₁:

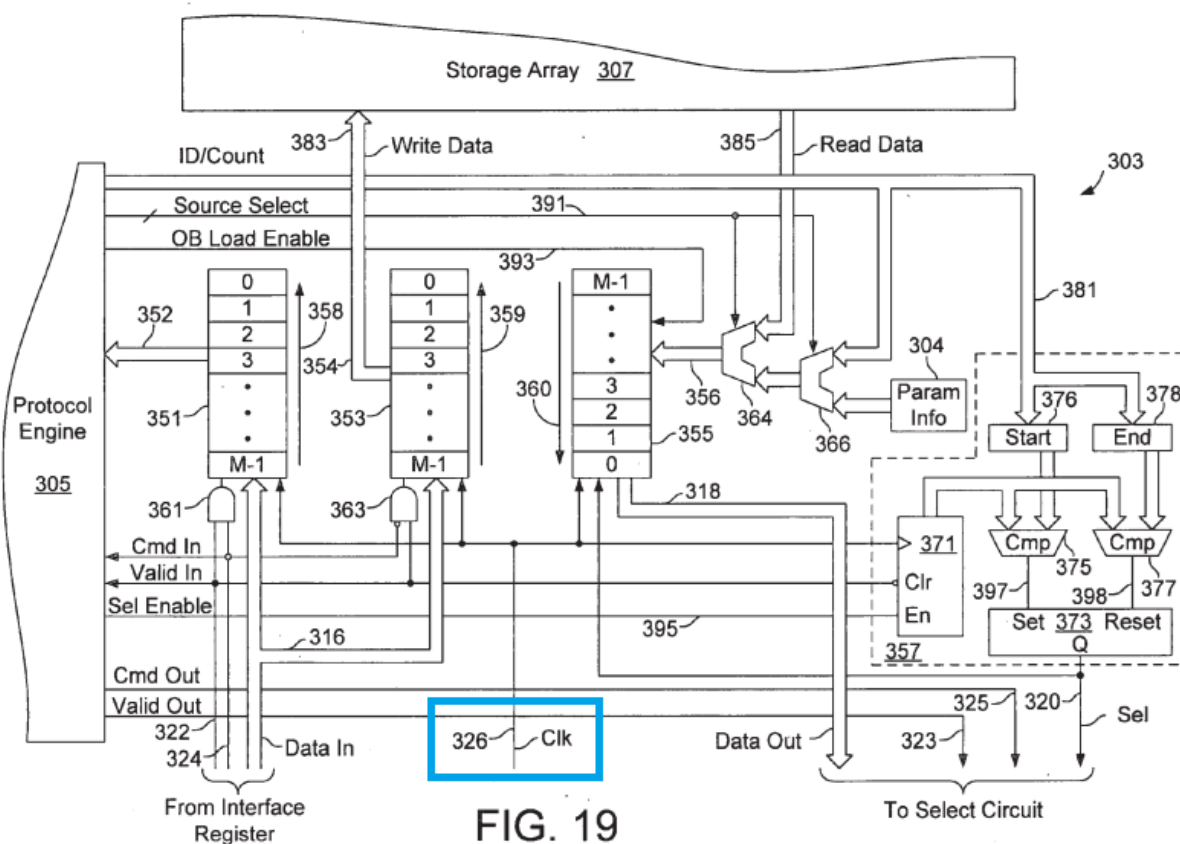


Pet., 48 (Petitioner's annotation of Grundy's Figure 6).

102. But, as already explained above, Figure 6 does not show when any data is latched by the memory device. Figure 6 at most identifies transmission timing

relative to the incoming clock signal; it does not identify a memory-device latching event.

103. When Petitioner attempts to show the claimed latching, then, Petitioner points elsewhere—to Grundy’s internal “[logic level clock signal 326](#)” shown in Figure 19 as shown below:



Ex. 1005 [Grundy] Fig. 19 (Patent Owner annotation).

104. Petitioner then argues that “Grundy’s clock signal drives this latching” because “Grundy’s clock signal 326 is coupled with the command buffer, and controls when command packets are loaded into the command buffer.” Pet., 50. Here, in other words, Petitioner has used Figure 6’s incoming clock signal to identify

the claimed “first rising edge,” but then uses Figure 19’s internal clock signal 326 when discussing the alleged latching event.

105. But Grundy explains that “a logic level clock signal 326 is generated by the signal receiver 310 coupled to the input-side clock line 152,” and that this internal clock signal is supplied to internal circuitry including the protocol engine, I/O controller, and interface register. Ex. 1005 [Grundy] [0088]. Thus, clock signal 326 is a later internal signal generated from the incoming clock, and in particular, the clock signal 326 is not identical to the signal that Petitioner identified in connection with claim 1. Petitioner’s expert Dr. Sechen confirmed that the incoming clock and internal logic-level clock signal 326 are not identical in timing:

Q. So that clock signal provided via clock in and the logic level clock signal 326 are not the same signal, are they?

A. Not exactly. There would be some delay.

Ex. 2028 [Sechen-Tr.] 77:4–7.

106. Dr. Sechen also confirmed this point when comparing the signal labeled “Clock” in Figure 5A to Grundy’s internal logic-level clock signal 326:

Q. So the signal labeled “Clock” in Figure 5A is not the same as the signal labeled “Logic level clock signal 326” in Grundy’s Figure 17?

A. Yeah, there’s a propagation delay there.

Id., 78:13–17.

107. I agree with Dr. Sechen that a POSITA would understand there to be a delay between Grundy's "Logic level clock signal 326" and Grundy's "Clock" in Figure 5A. A necessary consequence of the existence of this delay, however, is a gap between Petitioner's occasional use of the "Clock" signal in Figure 5A and Petitioner's timing theory for claim 2. Taking Petitioner's analysis of Figure 19 for granted, for example, the delay implies that *nothing* would happen in Grundy's Figure 19 at a first rising edge of Figure 5A's "Clock" signal.

108. A POSITA would understand that Grundy's incoming clock on clock line 152 and Grundy's internal logic-level clock signal 326 are related, but not interchangeable for purposes of the precise timing required by claim 2. Grundy states that logic-level clock signal 326 is generated by receiver circuitry coupled to the input-side clock line. That generation process introduces delay between the incoming clock at the memory-device input and the internal clock signal used by downstream internal circuitry.

109. Accordingly, even if Grundy's Figure 19 is assumed to evidence some internal loading or latching of data at Grundy's memory device in response to clock signal 326, that would not establish the timing required by claim 2, unless Petitioner were also to show that this internal event occurs at the *first* rising edge of the *same* clock signal identified for claim 1 after the transition of the control signal. The Petition provides no such analysis.

110. Accordingly, in my opinion, Petitioner has not shown that claim 2 is rendered obvious by what it terms “Grundy-Kilbuck.”

H. Petitioner Fails To Show “control circuitry ... configured to perform the read operation during a time period that overlaps with a time period for the page program operation” (Claim 13) And “wherein ... providing a read command occurs during a time period that overlaps with a time period for the page program operation” (Claim 21).

111. Claim 13 recites “[t]he flash memory device as claimed in claim 1, wherein the control circuitry is configured to perform the read operation during a time period that overlaps with a time period for the page program operation.” Method claim 21, which depends from independent method claim 17, recites “[t]he method of claim 17, wherein the providing a read command occurs during a time period that overlaps with a time period for the page program operation.” Petitioner does not make separate arguments regarding method claim 21, but instead deals with claim 21 purely by reference to Petitioner’s argument for system claim 13. *See* Pet., 70; *see also* Ex. 1003 [Sechen-Decl.] ¶ 165.

112. Significantly, claim 13 depends on claim 1 and claim 21 depends on claim 17. Ex. 1001 [’381] 28:41-44, 30:14-16. The arguments in the Petition for claims 13 and 21 are based principally on the Figures 5A, 6, and 17 embodiments of Grundy, combined with generalities in Kilbuck about Flash memories. *See, e.g.*, Pet., 18, 20, 21, 22, 37, 39, 41.

113. Here, Petitioner attempts to show this claim is present in the Grundy-Kilbuck combination by saying, in part:

It would have been obvious to a POSITA to modify Grundy's memory device based on Kilbuck's flash memory architectures such as the one shown by Kilbuck's Figs. 3A or 3B. INFINEON-1003, ¶¶131-133. A POSITA would have incorporated two or more of Kilbuck's flash memory devices in Grundy's memory device such that Grundy's memory device can perform overlapping operations in response to receiving commands on respective signaling paths

Pet., 69.

114. When Petitioner says “Grundy’s memory device,” Petitioner is presumably referring to the Grundy embodiments of Figure 5A, 6, and 17, as this is the sole focus of attention in Petitioner’s discussion of independent claim 1. Grundy’s Figure 5A embodiment has one input signaling path, one output signaling path, one protocol engine, and one storage array. *See, e.g.,* Ex. 1005 [Grundy] Figures 5, 17. Yet here, Petitioners switch to the Figure 4 embodiments of Grundy, which have multiple signaling paths in and out of each memory device. *See, e.g.,* Pet., 67.

115. Petitioner’s analysis of claim 1 repeatedly relies on Grundy’s Figures 5A and 17, for example, *see, e.g.,* Pet., 23-25 (discussing limitation [1b]), 26-27 (discussing limitation [1c-i]), 32-33 (discussing limitation [1d]), 35 (citing Figs. 5A and 17 in connection with the alleged “control circuitry” of limitation [1e]). But

nowhere in Grundy's Figures 5A and 17, or their descriptions, is there any suggestion of having two commands operate on Grundy's flash memory arrays in parallel in these embodiments of Grundy.

116. Petitioner goes on to say in the Petition and Declaration that "It would have been obvious to a POSITA to modify Grundy's memory device in view of Kilbuck such that it can perform overlapping read and page program operations since the dual signaling paths enable such overlapping of read and page program operations." Pet., 67-68. Granted, Kilbuck's Figures 3A and 3B show two Flash memory Devices 314 in its Flash Memory subsystem. But Kilbuck never discloses that these devices perform different operations concurrently. The entire Flash Memory Subsystem 304 is a single unit with a single memory controller and Kilbuck does not describe or hint at the ability of its two Flash Memory Devices to perform two operations, let alone two different operations, at the same time.

117. Kilbuck's Figures 3A and 3B depict a flash memory subsystem containing multiple Flash Memory Devices 314 controlled by a memory controller 312. A POSITA would understand those Flash Memory Devices 314 to be distinct devices within the subsystem. Thus, Petitioner's assertion that one Kilbuck device may read while another Kilbuck device programs does not, by itself, show that a single claimed flash memory device has control circuitry configured to perform the overlapping operations required by claim 13.

118. To map Kilbuck's Figures 3A and 3B to claim 13, Petitioner would need to explain what structure in the proposed Grundy-Kilbuck combination is the claimed "flash memory device," what structure is the claimed "control circuitry," and how that same device and control circuitry satisfy the claim 1 limitations while also performing the overlapping operations of claim 13. The Petition does not provide that explanation.

119. Petitioners say:

A POSITA would have understood that each of Kilbuck's flash memory devices is capable of performing read operations and page program (write) operations because each has its own circuitry to access (read/program) its own flash memory array such that one of Kilbuck's memory devices can perform a read operation during a time period that overlaps with a time period for a page program operation which is performed by another one of Kilbuck's memory devices. INFINEON-1003, ¶134; INFINEON-1006, [0030] (discussing that each device has its own buffer, controller, row/column decode), [0040]-[0042], Figs. 1, 2, 3A, and 3B.

Pet., 69.

120. This assertion is false. Even though Kilbuck's memory devices are apparently independent, the memory controller is not. There is no suggestion in Kilbuck that the memory controllers in Figures 3A or 3B are sophisticated enough to receive and perform multiple commands and process them concurrently, thereby

dealing with issues of temporal and functional conflict and management of shared resources outside the memory devices. These issues are complicated, and there is no cited support to indicate to the POSITA how these issues are resolved, whether in Kilbuck alone, or whether in Petitioner's proposed combination involving Kilbuck. In the absence of any such cited prior art disclosure or other evidence, a POSITA would not presume from the separate disclosures in Grundy and Kilbuck that these issues had been resolved in combination with one another, let alone in a way that satisfies the claim.

121. A POSITA would also immediately appreciate numerous differences between Grundy's Figures 4A, 4B, 4C, and 4D and Grundy's Figure 5A embodiment. As one example, the Petition does not identify where in Figures 4A, 4B, 4C, or 4D Petitioner might find the single "common data interface" that Petitioner finds in Grundy's Figure 5A in connection with claim 1. All that might be inferred from the Petition's express reliance on the multiple signaling paths of Figure 4A, *see, e.g.*, Pet., 67, and Grundy's express disclosure that the signaling paths of Figure 4A "are controlled by separate memory controllers 123A and 123B," Ex. 1005 [Grundy] [0041], is that Petitioner's argument for claim 13 would simultaneously implicate **both** of the two memory controllers of Grundy's Figure 4A and 4B, when Petitioner's arguments for claim 1 refer only to an embodiment involving a single memory controller.

122. Grundy’s Figures 4A and 4B involve two “separate memory controllers 123A and 123B” respectively controlling “separate signaling queues 124A and 124B.” Ex. 1005 [Grundy] [0041]. Even if one were to assume that each of the two “signaling queues” 124A and 124B were designed and operated similarly to the single signaling path depicted in Grundy’s Figure 5A—and this is neither a possibility that Petitioner expressly addresses one way or the other, nor a possibility mandated by Grundy (which expressly discloses using different signaling queues differently, *see, e.g.*, Ex. 1005 [Grundy] [0041] (describing embodiments in which a “first signaling queue may be used to deliver commands and write data to the memory devices 107, and the second signaling queue used to deliver read data to the memory controller 101”))—this assumption would not, by itself, identify which portions of the two “signaling queues” 124A and 124B carry the single claimed “clock signal” and single claimed “command signal” that Petitioner identifies in Grundy’s Figure 5A in connection with claim 1, for example, or which memory controllers 123A and 123B in Grundy’s Figure 4A produce those signals.

123. A POSITA would understand that Grundy’s Figure 4A and Figure 5A embodiments are different embodiments. Figure 5A depicts a single memory controller 151 coupled to memory devices through point-to-point links 153 that include clock, valid, command, and multi-purpose lines. Petitioner relies on those Figure 5A features for claim 1.

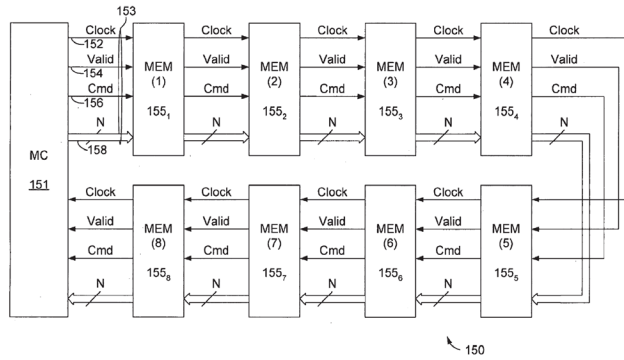


FIG. 5A

Ex. 1005 [Grundy], Fig. 5A.

124. Figure 4A, by contrast, depicts two separate signaling queues controlled by two separate memory controllers 123A and 123B:

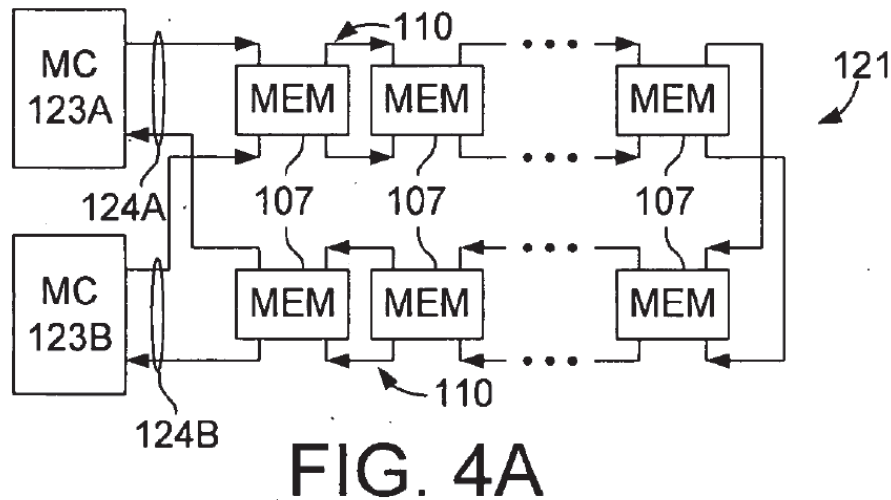


FIG. 4A

Ex. 1005 [Grundy], Fig. 4A.

125. The Petition does not explain how the Figure 4A embodiment supplies the same “clock signal,” “control signal,” and “common data interface” that Petitioner identified in Figure 5A. Nor does the Petition explain how Figure 6, which Grundy describes depicting the timing of transmissions made by the one memory

controller of Figure 5A, applies to the two-controller Figure 4A embodiment. Without such explanation, I cannot determine what device Petitioner contends satisfies both claim 1 and dependent claim 13.

126. Having two independent memory controllers sending commands to memory devices 107 places a huge burden on those devices to deal with the case of conflicting or overlapping commands arriving concurrently or nearly concurrently. These problems are non-trivial since relationships between successive commands to a singular Flash memory array can be disrupted irretrievably by commands from a second memory controller. Nowhere in Grundy or Kilbuck are these issues addressed, leaving a POSITA trying to make sense of the combination without any assistance.

127. Even in the simpler case of a single memory controller 131 sending commands down through two parallel signal paths 124A and 124B, as in Figures 4C and 4D, there are additional complexities in the memory controller that are not addressed in either reference. Putting aside the difficult and unaddressed issues of clock skew and variability in such a system, memory devices 107 would have to be able to receive commands, queue them, and dispatch them to the protocol engine simultaneously from two input signaling paths. Regardless of whether there are one or two (as suggested in Petition) storage arrays, the infrastructure of Figures 17, 19

and 20 of Grundy do not facilitate starting or concluding multiple commands simultaneously.

128. Even if one were to assume for purposes of argument that Petitioner is proposing that two of what Kilbuck depicts as distinct “Flash Memory Devices” in Kilbuck’s Figure 3A can be aggregated into a single “flash memory device” for purposes of claim 1—for example, with some of the claimed “control circuitry” existing within each of the multiple “Flash Memory Devices” 314 depicted in that Figure—Petitioner does not reconcile this proposal with Petitioner’s analysis of claim 1, and in particular does not explain how this hypothetical “flash memory device” would satisfy the remainder of claim 1. Petitioner does not, for example, identify how the claimed “control signal” and “clock signal” are provided to the hypothetical Kilbuck “memory device” in the combination: are they provided by the “memory controller 151” of Grundy’s Figure 5A (as they are in Petitioner’s analysis of claim 1, Pet., 23, 31), by the “memory controller 312” of Kilbuck’s Figure 3A, or by some other component? The Petition does not say.

129. Any analysis of Petitioner’s argument is further complicated by Petitioner’s statement that this hypothetical Kilbuck device “can perform overlapping operations in response to receiving commands on respective signaling paths,” Pet., 69 (citing Ex. 1003 [Sechen-Decl.] ¶¶ 131-133), where Petitioner’s expert declaration clarifies that Petitioner’s reference to “respective signaling paths”

for different commands is a reference not to any signaling path in Grundy's Figure 5A (which Petitioner relied upon for its analysis of claim 1), but to signaling paths in Grundy's multi-path multi-controller Figure 4A embodiment. Ex. 1003 [Sechen-Decl.] ¶ 133. But as previously explained, I do not agree that Petitioner has shown that Grundy's Figure 4A teaches claim 13, and for at least those reasons, I also do not understand how Kilbuck's Figures 3A and 3B would teach claim 13 in some combination with Grundy's Figure 4A embodiment.

130. When speaking of “modif[ying] Grundy's memory device ... such that it can perform overlapping read and page program operations,” Petitioner appears to acknowledge that “overlapping read and page program operations” are neither expressly disclosed in Grundy, nor are they a necessary consequence of the mere existence of multiple signaling paths in Grundy's Figure 4A. I agree with Petitioner that some modification of Grundy's Figure 4A would be necessary to produce a system that satisfied claim 13. Without an account of what Petitioner's proposed modification would actually involve, however, I cannot agree that this unspecified modification would have been obvious.

131. In addition to disclosing multiple signaling paths, for example, Grundy's Figure 4A discloses multiple *memory controllers* for its memory devices. See Ex. 1005 [Grundy] [0041] (describing Figure 4A as “an embodiment of a memory system ... in which two separate signaling queues ... each including the

same chain of memory devices ... are controlled by separate memory controllers 123A and 123B”) & Fig. 4A (elements labeled “MC 123A” and “MC 123B”). Although Petitioner’s analysis repeatedly focuses on Figure 4A’s disclosure of “multiple signaling paths,” Pet., 67, Petitioner never acknowledges that these “paths” are, at least in Grundy’s Figure 4A, connected to two memory controllers.

132. Petitioner’s proposal, for example, introduces the possibility that the “MC 123A” in Grundy’s (modified) Figure 4A might issue a command to read from a location in flash memory at or near the same time that the memory controller “MC 123B” issues a command to program new data at the same location in flash memory. To be clear, such commands are potentially conflicting because the order in which they are carried out will affect whether the data returned to “MC 123A” in response to its read command is the data that existed in the flash memory system before the program operation requested by “MC 123B” is carried out, or after that program operation is carried out. Equally fatal and even more difficult to discover and address are the hazards related to the relationship between read commands and data pickup commands. Ex. 1005 [Grundy] [0033]. If a second read command comes in from the other memory controller between coupled read and data pickup commands from the first controller such that the second read command alters the data available to the data pickup, the first memory controller will have no way of knowing that the data it received as a result of the data pickup command was not what it asked for.

Such crippling hazards are prevalent in multi-controller and multi-signal path systems.

133. Resolving such potential scheduling conflicts (or arranging so that they do not arise in the first instance) is an integral part of the design of any system in which multiple memory controllers access the same memory. This aspect of “Grundy-Kilbuck” is completely unaddressed by Petitioner. Accordingly, without more information about how this modified system is argued to operate, I cannot agree with Petitioner that “a POSITA would have been further motivated to make this modification to increase operational speed and/or provide ‘fast random read/write and/or burst capabilities.’” *Cf.* Pet., 68. The “operational speed” of the combined system cannot be meaningfully assessed without information about how the Petitioner’s “modification” would handle potential conflicts, and no such information is provided by Grundy, by Kilbuck, or by the Petitioner.

134. Petitioner’s proposed modification is not sufficiently defined to evaluate. If Petitioner is relying on Grundy’s Figure 4A, then the proposed system includes two separate signaling queues controlled by separate memory controllers. If those controllers are permitted to issue overlapping read and page program commands to the same memory device or same memory array, the system must address scheduling and arbitration issues. For example, one controller could issue a read command to a location at or near the same time another controller issues a

program command affecting that same location. The order in which those commands are performed may determine what data is returned by the read operation.

135. A POSITA would understand that a system allowing overlapping operations from multiple controllers would need a mechanism for coordinating such operations or preventing conflicts. The Petition does not identify any such mechanism in Grundy, Kilbuck, or the proposed combination. Nor does the Petition explain how the alleged modified device would maintain the clock, control signal, common data interface, and control circuitry mappings Petitioner relied on for elements of independent claims.

136. Accordingly, in my opinion, Petitioner has not shown that claims 13 and 21 of the '381 Patent are obvious in view of the proposed "Grundy-Kilbuck" combination.

I. Petitioner Fails To Show “transferring command data, address data, input data and output data to and from the at least one common data interface” (Element [17b-i]) is present in the presented prior art.

137. Element [17b-i] requires “transferring command data, address data, input data and output data to and from the at least one common data interface.” The Petition attempts to show the presence of this element by referring back to its analysis of element [1c-i] in Section V.A.4 of the Petition. As critiqued above, the corresponding [1c-i] element (“wherein at least one of command data, address data, input data and output data is transferred in synchronization with both rising and

falling edges of the clock signal when the flash memory device is in a double data rate configuration”), is not found because, fundamentally, the Grundy embodiment is broken and the transfer of data into the memory device is not possible with the circuitry disclosed in Figure 17. *See, e.g., Section VI.E supra.*

138. The language of element [17b-i] is somewhat different in that it relies on “transferring” instead of “is transferred” and it does not incorporate the double-data-rate language. Arguably, “transferring” and “is transferred” include both transmission and reception of data. Thus, the proofs in the Petition for element [1c-ii] and [17b-i] are both fatally flawed because they both rely on the broken embodiment of Figure 17 of Grundy which cannot receive data. Neither the Petition nor the Declaration of Dr. Sechen recognize this problem nor propose any remedy within the powers of a POSITA that would render their arguments plausible. With the falling of the argument relating to element [17b-i], so too fall all of claim 17 and all its dependent claims.

J. Summary Of Opinions.

139. It is my opinion that:

- Grundy in view of Kilbuck does not disclose or render obvious any of the challenged claims, and
- In particular, Grundy in view of Kilbuck does not disclose “[t]he flash memory device as claimed in claim 1, wherein the command data is

latched at the first rising edge of the clock signal after the transition of the control signal,” and

- In particular, Grundy in view of Kilbuck does not disclose “control circuitry ... configured to perform the read operation during a time period that overlaps with a time period for the page program operation” or “providing a read command ... during a time period that overlaps with a time period for the page program operation.”

VII. CONCLUSION

140. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required, I will appear for cross-examination within the United States during the time allotted. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also, I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

141. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are

believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Respectfully submitted,

Dated: 5/27/2026

A handwritten signature in black ink, appearing to read 'Steven Przybylski', written in a cursive style.

Steven Przybylski, Ph.D.

APPENDIX A

CV of Steven Przybylski, Ph.D.

Steven A. Przybylski

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Professional Experience

2003 - Present **President, Verdande Group, Inc**

An inventor, registered patent agent, strong communicator and seasoned technical expert, I provide intellectual property services to a diverse set of clients across the digital electronics spectrum. I provide patent, trade secret, and contract dispute litigation support services, and have extensive experience as a testifying and non-testifying expert in matters before district courts, the PTAB, the ITC, and foreign jurisdictions. I have testified by expert report, deposition, and live testimony on matters of claim construction, infringement, and invalidity, and have assisted in evaluations of potential damages and monetization strategies. With strong written and verbal skills, I provide tutorials to those of both technical and non-technical backgrounds, including judges and attorneys. In addition, I offer pre- and post-transaction portfolio evaluations and due diligence analyses.

I have been retained for these services with regard to:

Computer Systems

Processor design
Processor architecture
Multiprocessing
Graphics systems
Graphics/CUDA processors
Cache memories
Memory systems
Memory modules
Floating point computation
Operating systems
I/O systems
System boot issues

Consumer Electronics

Infotainment systems
Video encoding and decoding
Medical equipment
Embedded systems
Portable electronic systems
User interface design
Wired and wireless networking
Power/energy management
Standards development
Display interconnects
Integrated memories
Digital signal processing
Cloud-based content navigation
and serving

Semiconductors

DRAMs
Flash
SRAMs
Other non-volatile memories
Memory controllers
High-speed interconnects
Signal integrity
2D, 2.5D and 3D packaging
Error detection and correction
Clock distribution techniques
Semiconductor processing
IC and system testing
Computer aided design
FPGAs

2000 – 2003 **Manager, SSM Technologies, LLC.**

I managed, developed and sold a significant patent portfolio relating to DRAMs. Recognizing the intrinsic value of a long-neglected portfolio, I negotiated control of the portfolio and developed a new patent prosecution strategy. I oversaw and participated in the implementation of this strategy, culminating in the issue of a new set of broad method and apparatus claims. I then worked to monetarize the portfolio and to maximize return to the inventors and SSM's investors by analyzing the sell/license decision and guiding the stakeholders through the decision-making process. I gathered relevant documentation and analyses, approached likely purchasers, presented interested parties with the collected materials, actively sold the offensive and defensive utility of the portfolio, and orchestrated an auction-style final sales process.

1991 – 2003 **President and Principal Consultant, Verdande Group, Inc**

I have consulted on product strategy, comparative technical analysis, and system-level design in the areas of DRAMs, Flash, SRAMs and other semiconductor memories, computer systems and CPU architecture, and uni- and multi-processor memory hierarchy design. Technical engagements have included serving as memory system architect for Flash and DRAM memory devices and systems. In addition, I offered: general business planning and analysis services to computer and semiconductor companies; intellectual property management, including portfolio evaluation, development and brokering, and litigation support services to IP holders and legal firms; and due-diligence analyses to venture capitalists and securities firms.

My writing and analysis encompasses an extensive range of topics for trade magazines, conferences, and academic journals. As one of the leading independent analysts of the semiconductor memory industry, I wrote (1994) and substantially revised (1996) an 850-page research report entitled *New DRAM Technologies: A Comprehensive Analysis of the New Architectures*, available from the publishers of *The Microprocessor Report*. I have also taught and presented tutorials to both technical and non-technical audiences on subjects including semiconductor memory architecture, memory hierarchy design, and computer systems and CPU architecture. In particular, I have presented over 50 full- and partial-day seminars on these topics to over 2,500 managers, engineers, marketers, and analysts. I have also served on the advisory boards of high-technology start-ups, advising on processor, DRAM and Flash memory trends and general business opportunities.

- 1989 - 1991 **Chief Scientist and Systems Architect, MIPS Computer Systems.**
I played a variety of roles within MIPS, including assistant to the Senior Vice President of Engineering, technical lead for a group of designers that investigated the technical and economic feasibility of developing a companion chip to the R3000 CPU and R3010 FPU, troubleshooter within the High-End Systems Group responsible for taking on any short or long term task that was in need of additional manpower, chief scientist for the group in charge of planning and investigating options for future high-end systems, systems architect for both a new R4000 based symmetrical multi-processor and a low-cost desk-top machine.
- 1990 - 1991 **Consulting Assistant Professor, Dept. of Elect. Eng., Stanford University.**
I designed and taught an advanced graduate level course on cache and memory hierarchy design and supervised the students' research activities. Two groups of students continued their research and ultimately published their efforts under my direction.
- 1989 - 1989 **Postdoctoral Scholar, Department of Electrical Engineering, Stanford University.**
As a postdoctoral scholar, I continued my dissertation research into the analysis of cache behaviour and performance-optimal memory hierarchy design.
- 1984 - 1985 **Computer Architect and Systems Designer, MIPS Computer Systems.**
My main contribution during MIPS' first year was the specification of the architecture and micro-organization of the R2000 VLSI RISC CPU, including the CPU interface and the cache sub-system. I was integrally involved in the implementation of both the CPU and system-level design. My most important role was that of liaison between the VLSI, board-level hardware, compiler and operating system teams.
- 1981 - 1988 **Research Assistant, Department of Electrical Engineering, Stanford University.**
I was a key participant in the MIPS VLSI CPU design team, involved in the design, debugging and testing of the IC design. I also oversaw the development of a prototype CPU board, and subsequently aided in the architectural specification of the MIPS-X VLSI CPU. My dissertation research used analytical and empirical techniques to examine memory hierarchy design from the perspective of optimizing system level performance.

Education

Haas School of Business, University of California at Berkeley, M.B.A. (2000).

Coursework and final project included a combined emphasis on business strategy and financial analysis.

Stanford University, M.S.E.E. (1982), Ph.D. (1988).

Research areas: Computer systems design and VLSI integrated circuit design. Concentrated areas of study spanned the breadth of both electrical engineering and software systems. Topics of extensive coursework included digital systems design, computer architecture, semiconductor devices, error correction codes, control theory, and system software — including user interface design, operating systems, compilers, and I/O systems. Doctoral dissertation title: Performance-Directed Memory Hierarchy Design.

University of Toronto, B.A.Sc. with Honours (1980).

My unique, specially approved course of study within the Engineering Science Programme combined the computer science and electrical engineering degree programs. This provided a broad and deep background in both areas. Coursework and undergraduate thesis covered digital systems design, computer systems, control theory, network analysis, analog circuit design, semiconductor physics, human-computer interfaces, operating systems, compilers, database design, and AI.

Honors and Publications

Awards

Most Influential Paper Award, ACM/IEEE International Symposium on Computer Architecture, 1989, with Mark Horowitz and John Hennessy.

Micro Test-of-Time Award, for one of the ten most influential papers of the first 25 years of the IEEE Micro Symposium, with John Hennessy, Norman Jouppi, Christopher Rowen, Thomas Gross, Forest Baskett, and John Gill. 1994.

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- An Introduction to Semiconductor Memories, A Verdande Group presentation in cooperation with Citibank Inc, Taipei, Taiwan ROC, June 1998.
- Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar. Presented more than 10 times to corporations between September 1997 and October 1999
- The New DRAMs for Main Memory and Graphics, Full day Seminar, Verdande Group Seminar Series, Portland, Austin, San Jose, and Boston, September 1997.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar, Verdande Group Seminar Series, Portland, Austin, San Jose, and Boston, September 1997.

Sorting Out the New DRAMs, Half-Day Tutorial, Hot Chips IX, August 1997.

Embedded DRAMs: Today and Toward System-Level Integration, Half-day seminar, Presented at 24th Annual International Symposium on Computer Architecture, May 1997.

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Foreign counterparts of the above.

Additional Information

Registered US Patent Agent, 1997 - present

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