

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INFINEON TECHNOLOGIES AMERICAS CORP.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner,

Case IPR2025-01487
Patent 9,972,381

REMOTE DEPOSITION OF CARL SECHEN, PH.D.
FRIDAY, APRIL 24, 2026

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Reported by:

Kelly Schindele, CSR No. 8357

Job No. 1519600

1 UNITED STATES PATENT AND TRADEMARK OFFICE

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3 BEFORE THE PATENT TRIAL AND APPEAL BOARD

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5 INFINEON TECHNOLOGIES AMERICAS CORP.,
6 Petitioner,

7 v.

8 MOSAID TECHNOLOGIES INC.,
9 Patent Owner,

10 -----
11 Case IPR2025-01487
12 Patent 9,972,381
13
14

15 Deposition of CARL SECHEN, taken remotely via
16 Zoom, commencing at 8:04 a.m. and ending at
17 11:00 a.m., on Friday, April 24, 2026, before
18 Kelly Schindele, Certified Shorthand Reporter
19 No. 8357.
20
21
22
23
24
25

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1	I N D E X		
2	WITNESS: CARL SECHEN, PH.D.		
3	EXAMINATION	PAGE	
4	BY MR. COURTNEY		5
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8	1005 Patent Application Publication US 2004/0148482 A1		13
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10	2005/0204091 A1		
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1 REMOTE DEPOSITION; FRIDAY, APRIL 24, 2026

2 8:04 A.M. - 11:00 A.M.

3

4 THE REPORTER: Good morning. My name is
5 Kelly Schindele, California CSR number 8357.

6 Please raise your right hand.

7

8 CARL SECHEN, PH.D.,
9 having been first duly administered an
10 oath remotely by the reporter, was examined
11 and testified as follows:

12

13 EXAMINATION

14 BY MR. COURTNEY:

15 Q. All right. Well, good morning, Dr. Sechen.

16 A. Good morning.

17 Q. Could you please state your name for the
18 record.

19 A. Yeah. Carl Sechen. That's my usual
20 pronunciation, but I'm familiar with others, so --

21 Q. I may have to rewire my brain a little bit
22 because I've only read your name until now, and that
23 will be some adjustment.

24 Where are you located today, Dr. Sechen?

25 A. In Richardson, Texas.

1 Q. Okay. Is there anyone there in the room
2 with you?

3 A. No.

4 Q. And you have been deposed before, correct?

5 A. Yes.

6 Q. Have you been deposed in an IPR proceeding?

7 A. Yes.

8 Q. How recently was that, the last one?

9 A. Oh, may- -- yeah, I don't remember exactly,
10 but maybe a year or so.

11 Q. Okay. So, I will just remind you, under
12 the rules for depositions in PTAB proceedings, now
13 that we have begun until we finish, you are not
14 permitted to communicate with your counsel about the
15 substance of your testimony, unless it's to discuss
16 whether to assert a privilege, and your counsel
17 can't suggest to you the manner in which you should
18 answer questions.

19 Do you understand that?

20 A. Yes.

21 Q. And you understand that your testimony
22 today is under oath?

23 A. I do.

24 Q. Is there any reason why you cannot give
25 your best testimony today?

1 A. No.

2 Q. Okay. From time to time your counsel may
3 make objections. But unless counsel specifically
4 instructs you not to answer, you will still need to
5 answer.

6 Do you understand that?

7 A. Yes.

8 Q. And I think you know we have a court
9 reporter here today. She is writing down everything
10 we say, so it's important for us not to talk over
11 each other or cut each other off.

12 Does that make sense?

13 A. Yes.

14 Q. It's also important that you answer my
15 questions in a way that can be transcribed. So, for
16 example, nodding your head or saying uh-huh might be
17 difficult to understand in a transcript, and while
18 it isn't the sort of thing that a polite person
19 would call out in a casual conversation, because
20 this is a deposition, if that happens, I might
21 mention it and ask for a clear answer. Is that
22 okay?

23 A. Okay.

24 Q. So please let me know if you don't
25 understand a question and I will try to clarify or

1 rephrase it. Will you do that?

2 A. Yes.

3 Q. And we can take breaks from time to time.
4 If you need a break, just let me know. Is that
5 okay?

6 A. Yes.

7 Q. Do you agree that during the deposition you
8 will not use any pre-written notes or any documents
9 that may be available to you other than the exhibits
10 in the IPR?

11 A. Yes.

12 Q. Okay. Do you agree that if you take any
13 notes or write things down during the deposition,
14 that you will make those materials available to us?

15 A. Yes.

16 Q. And do you agree that while we are on the
17 record, you won't have any communication with
18 counsel or anyone else that would not appear on the
19 deposition transcript?

20 A. Yes.

21 Q. So, when were you retained for this case,
22 Dr. Sechen?

23 A. I don't remember exactly, but I'm thinking
24 about a year ago or so.

25 Q. Okay. What did you do to prepare for

1 today's deposition?

2 A. Well, I started a few weeks back reviewing
3 my declaration, some other -- all the relevant
4 patents and so forth. And then this week there were
5 meetings with counsel for a few days.

6 Q. Okay. Was there anyone at the meetings who
7 wasn't counsel?

8 A. No.

9 Q. Did counsel show you any documents during
10 your meetings that refreshed your recollection as to
11 any facts?

12 MR. STEPHENS: I caution the witness not to
13 divulge any communications with counsel.

14 THE WITNESS: Well, certainly we discussed
15 the -- you know, my declaration and the prior art in
16 the 381 patent.

17 BY MR. COURTNEY:

18 Q. Did you review any documents that aren't
19 exhibits in this proceeding?

20 A. No.

21 Q. Okay. So, you understand these proceedings
22 relate to US Patent Number 9972381, correct?

23 A. Yes.

24 Q. Okay. And I will call that the 381 patent
25 from time to time, as you do. Is that okay?

1 A. Yes.

2 Q. And you understand these proceedings have a
3 case number, IPR2025-01487, correct?

4 A. Yes, I think that's right.

5 Q. I probably won't use that a lot, but if I
6 do talk about the 1487 proceeding or the 1487 case,
7 I'm talking about this case. Is that okay?

8 A. Okay. Yes.

9 Q. So, if we could, I would now like to bring
10 up exhibit marked 1003. This is your declaration.
11 It might take a while to upload.

12 (Exhibit 1003 marked for
13 identification.)

14 BY MR. COURTNEY:

15 Q. So if you could, could you just let me know
16 if you recognize that as the declaration filed as
17 Exhibit 1003 in this case.

18 A. That's going to be in the chat or on --

19 Q. Yeah. It should be -- it should have just
20 uploaded in the chat.

21 A. Oh, okay. Let me see. How do I do this
22 now? Let me just check this. How did that come
23 through?

24 Okay. Yeah, here we go. Yes.

25 Q. Okay. So you mentioned before we started

1 that you have a clean paper copy of this
2 declaration; is that correct?

3 A. Yeah, I do.

4 Q. Okay. So feel free to review that instead,
5 if that's easier.

6 A. Okay.

7 Q. So this declaration contains a complete
8 statement of your opinions regarding the 381 patent
9 in connection with the 1487 proceeding, correct?

10 A. Well, certainly at the time I drafted this,
11 yes. I don't -- yeah, none of these opinions
12 changed since that time.

13 Q. Okay. So, there's nothing you would have
14 added to this document on August 29th, 2025, that
15 somehow didn't make it in?

16 A. Well, it's always possible to explain
17 something more clearly, but, yeah, I stand by
18 everything I wrote there.

19 Q. Okay. So if we turn to page 30 --
20 paragraph 35 of your declaration, which is on
21 page 16. Could you turn there and let me know when
22 you're there?

23 A. Page 16. Okay. Here we go. Yes.

24 Q. Okay. So you say, "the terms that appear
25 in the claims of the 381 Patent should be

1 interpreted according to their 'ordinary and
2 customary meaning,' which is sometimes called the
3 Phillips standard."

4 Do you see that?

5 A. Yes, yes.

6 Q. So in the opinions expressed in your
7 declaration, you have applied the ordinary and
8 customary meanings of the terms in the 381 patent
9 claims that are at issue, correct?

10 A. Yes, that's right.

11 Q. Okay. So in paragraphs 1 to 14 of your
12 declaration, which is, basically, the first couple
13 of pages, you discuss your background in your CV,
14 and there's quite a lot there, of course.

15 But for the present moment, what would you
16 say is your background in flash memory devices.

17 A. I have taught that for many years as part
18 of my advanced VLSI class for graduate students here
19 at UT Dallas, and so that would be for about 21
20 years now. And I have also done a number of, shall
21 we say, expert witness cases on this topic as well.

22 Q. Okay. Have you ever been involved in the
23 design of a flash memory device?

24 A. Certainly the components, yes. I mean, I'm
25 thoroughly familiar with all aspects of digital

1 circuit design, you know, row decoders, column
2 decoders, latches, flip-flops, you know, anything,
3 and as well as mixed-signal design and analog
4 design.

5 Q. Okay. So, I'd also like to introduce
6 Exhibit 1005, which will be hitting the chat
7 shortly. It is a 55-page patent publication
8 entitled "Memory Chain," listing Kevin P. Grundy as
9 an inventor, and it bears a stamp of INFINEON-1005
10 on its first page.

11 A. Okay.
12 (Exhibit 1005 marked for
13 identification.)

14 BY MR. COURTNEY:

15 Q. When that comes through, could you just
16 kind of look it over and let me know when you are
17 done?

18 A. Yes, that's what I expected to see.

19 Q. So I will call this Grundy, as you do in
20 your declaration. Is that okay?

21 A. Yes.

22 Q. At a high level, what kinds of problems is
23 Grundy trying to solve?

24 A. Let's see. I believe that is articulated
25 in my report on -- and I'm not sure, yeah, if I want

1 to say anything other than what's there.

2 Certainly, improving the speed of accessing
3 memories of various types, including flash. Let's
4 see. Let's go to the relevant.

5 Yeah, it's, basically, speed of access,
6 accessing data or writing data for a variety of
7 memories, including flash.

8 Q. Okay. And Grundy describes various ways in
9 which a memory controller can interact with memory
10 devices of various types, correct?

11 A. That's basically right.

12 Q. So Grundy discloses, for example, that its
13 memory controller might be used with static RAM
14 arrays and dynamic RAM arrays, correct?

15 A. In addition to other types, like flash and
16 EEPROM, which is a precursor to flash, and including
17 SRAM and DRAM, yes.

18 Q. Yeah. So Grundy also discloses that its
19 memory controller can be used with nonvolatile
20 storage arrays, such as flash, EEPROM, as you
21 mentioned.

22 What is EEPROM?

23 A. Well, that stands for electrical --
24 electrically erasable programmable read-only memory,
25 and which is, basically, what flash is in the

1 beginning, is the concept of having separate blocks
2 and erasable blocks was -- well, particularly
3 peculiar to NAND flash.

4 But it all started from EEPROM and the
5 intention to make it accesses -- to make accesses
6 faster, you know, both read and writes.

7 Q. Okay. If we could turn to paragraph 141 of
8 your declaration. And if you prefer page numbers, I
9 think this is page 106.

10 A. All right. Let's see.

11 Q. If you just let me know when you are there.

12 A. 141, yes. Okay.

13 Q. Okay. So, here you are quoting, actually,
14 from another exhibit, Kilbuck. Let me know if you'd
15 like me to introduce that exhibit now. But I think
16 for what I'm about to ask about flash, we can just
17 start with what's quoted here in your declaration.

18 So, could you review this first quote from
19 Kilbuck and let me know when you are done.

20 MR. STEPHENS: Counsel, why don't we
21 just -- if you wouldn't mind sharing Kilbuck, so if
22 he's going to be answering questions about it, if he
23 can have the reference in front of him.

24 MR. COURTNEY: Yeah, sure. So here we have
25 landing in the chat an exhibit marked 1006. It is a

1 17-page patent publication entitled "Non-Volatile
2 Memory with Synchronous DRAM Interface," listing
3 Kevin M. Kilbuck as an inventor, and bearing a stamp
4 INFINEON-1006 on its first page.

5 (Exhibit 1006 marked for
6 identification.)

7 THE WITNESS: Yes.

8 BY MR. COURTNEY:

9 Q. Can you let me know --

10 A. I do see that, yes.

11 Q. Okay. Is that the document you refer to in
12 your declaration as Kilbuck?

13 A. Yes.

14 Q. Okay. I will also refer to it as Kilbuck.
15 Turning to either your declaration or to
16 paragraph 5 in Kilbuck, could you review that
17 paragraph and let me know when you are done?

18 A. Yeah, I think I'm ready to respond to that.

19 Q. Okay. So, here Kilbuck is talking about
20 NAND flash memory. What is NAND flash memory?

21 A. It's, basically, where the -- there's a
22 string of memory cells, and in order to get
23 conduction through that string, you, basically, have
24 to turn to all those cells. And so that's much like
25 a NAND gate or AND gate or what have you. They call

1 it NAND, because if they are all on, meaning high
2 input, you get a low at the top of the string. And
3 so they are, basically, connected in series, is what
4 that means.

5 So, if you want to access one particular
6 cell to check its -- whether it's storing, say, a
7 one or a zero, you have to turn on all the other
8 cells to allow that selected cell to influence
9 whether you get a one or a zero output. And that's
10 in contrast to a NOR flash.

11 Q. So what is NOR flash memory?

12 A. Well, in NOR flash, each cell is
13 independently connected to the so-called bit line,
14 and so you just have to activate that one cell to
15 tell if your output is one or zero. And so that's
16 much like a NOR gate where all the cells are in
17 parallel in some sense.

18 Q. Okay. In this part of the paragraph that
19 you are quoting, paragraph 5 of Kilbuck, it says,
20 "Typically this means that a majority of control and
21 management of a NAND flash memory device is external
22 from the memory device and expensive dedicated
23 hardware or a software driver that is executed on a
24 coupled memory controller or processor."

25 Do you agree with that statement?

1 A. You know, at the time that was written,
2 that was certainly true. And, you know, as the
3 ability to integrate more and more transistors on a
4 chip became possible, then it was, in fact, possible
5 to put a controller on the chip it- -- the flash
6 chip itself or at least part of it.

7 Q. If we could move to the next page of your
8 declaration, that's page 107. We are still in the
9 same paragraph, 141 of your declaration, but you're
10 beginning with a new quote from Kilbuck, which is
11 Kilbuck's paragraph 31.

12 Do you see where that is?

13 A. Yeah.

14 Q. So this paragraph has a sentence beginning,
15 "The internal memory controller 110 also controls
16 the specialized flash memory interfacing and
17 interaction with the memory array," and then there's
18 a list of things. Do you see that?

19 A. Yes.

20 Q. What is "address abstraction"?

21 A. Well, that's, basically, you know, you get
22 an address from outside which pertains to a certain
23 row in your flash memory, and that row is, if you
24 are doing a read, for example, that row is brought
25 out into what's called a page buffer, and then

1 there's also a column address which further narrows
2 down which cells you want to have the data for, and
3 it starts -- say, in a read, it starts outputting
4 data starting with the data located at that column
5 address.

6 Q. Okay. What are "bad blocks"?

7 A. Yeah, that -- if you write to a page in a
8 block and it's -- since you -- nowadays especially,
9 but even in the beginning, you know, when you write
10 data, you also check whether or not it actually got
11 written as you intended. And if it did not, you --
12 well, you could try again in principle, but in any
13 event, if that second attempt fails, then you
14 declare that page to not work and that block to be
15 bad, and you would not want any further reads or
16 writes to proceed in that block.

17 So, first you would move the good data out
18 of the block to a completely valid block, and then
19 you would label that block as, you know, unusable or
20 bad.

21 Q. Okay. And is that movement process you
22 were just talking about what Kilbuck is talking
23 about when it refers to mapping bad blocks?

24 A. Yeah, that's indeed part of it, yes. And
25 there's also a -- sort of like a translation,

1 look-aside buffer, or I forgot the name of it now
2 specifically here, but the CPU is looking for
3 specific addresses and there's a mapping to where
4 that data really is on the flash.

5 So, when you move data from one block to
6 another, you have to update that table.

7 Q. What is "wear leveling"?

8 A. Yeah. That's where -- where with an H --
9 where you want all of the blocks that have been
10 written a similar number of times.

11 Actually, the erase process is somewhat
12 damaging to flash cells, and the reason is, is they
13 are forcing electrons through an insulator, like
14 oxide. And if you do that, every time you do that,
15 it can break some of the bonds in the insulator, and
16 at some point it can get to where it just leaks
17 electrons, in which case you can no longer store a
18 specific logic value there.

19 So, every time you do an erase, you are, in
20 some sense, reducing the life of that block. And so
21 you want to try to use the blocks the same number of
22 times. And that's what's called wear leveling.

23 Q. Okay. And you said the erase process is
24 damaging to flash cells. Is wear leveling something
25 generally that is specifically done in flash memory

1 systems as opposed to other kinds of memory system?

2 A. Yeah, as opposed to SRAM and DRAM, for
3 sure. And the reason, again, is because you are
4 forcing, at a high voltage, electrons to penetrate
5 and go through an insulator like oxide, which is
6 damaging to that oxide.

7 Q. So would you agree that the operations that
8 Kilbuck is describing here, mapping bad blocks, wear
9 leveling, erase block management, are a necessary
10 part of managing a NAND flash memory device?

11 A. That's correct, yeah. That would be
12 according to the ONFI standard that's been around
13 for a long time.

14 Q. What would happen if a memory controller
15 wrote to or erased NAND flash memory without any
16 regard for wear levels?

17 A. Oh, well, yeah, you could do that, and
18 certainly early flash memories didn't have wear
19 leveling, like the very early ones, and what would
20 happen is a block would wear out sooner than the
21 others. And so you have to label that as a bad
22 block. And so now your total pool of available
23 memory has decreased.

24 And as this keeps on going on, your
25 available pool of memory keeps decreasing, and then

1 at some point you may not have enough capacity to
2 store what you need to store in that flash memory.
3 So, and then you will have to, you know, basically,
4 swap out that whole memory system. So wear leveling
5 will just enable you to not run out of valid blocks
6 for a lot longer time.

7 Q. Okay. Is there any disclosure in Grundy of
8 Grundy's memory controller mapping bad blocks in a
9 NAND flash memory device?

10 A. I don't believe it goes into details on
11 that.

12 Q. Okay. Is there any disclosure in Grundy of
13 its memory controller monitoring wear levels in a
14 NAND flash memory device?

15 A. Well, let's see. I should be certain about
16 this.

17 I do not believe it describes that.

18 Q. In an implementation of Grundy that
19 involved a NAND flash memory device, would Grundy's
20 memory controller perform bad block management?

21 MR. STEPHENS: Objection. Form.

22 THE WITNESS: Certainly a person of
23 ordinary skill in the art, or shall I say POSITA,
24 would have known to implement bad block management
25 and wear leveling in the -- a flash memory system

1 that he was -- he or she was seeking to develop, and
2 certainly Kilbuck would call attention to that fact,
3 as would the standards for producing flash memories
4 that were available at the time.

5 BY MR. COURTNEY:

6 Q. Okay. Would it be fair to say that if one
7 were to implement Grundy with NAND flash memory
8 devices, the bad block management would be performed
9 somewhere in that system?

10 A. Certainly, yeah, I think that's fair to
11 say, yeah.

12 Q. Would it necessarily be performed by
13 Grundy's memory controller?

14 A. Well, certainly, by the ultimate memory
15 controller that's used by the combination.

16 Q. Yeah, but -- okay.

17 If we could turn to paragraph 104 on
18 page 70 of your declaration. This is the beginning
19 of your discussion of a limitation of Claim 1 that
20 you call 1f, which recites, "a status register
21 configured to indicate a status of the flash memory
22 device."

23 A. Yes.

24 Q. Do you see that?

25 A. I do.

1 Q. What is a status register?

2 MR. STEPHENS: Objection to form.

3 THE WITNESS: Well, a status is not -- in
4 Claim 1 it's not -- it just says a status. So, it
5 could be -- depending on the design of the flash
6 memory device, it could mean a variety of things
7 according to Claim 1. It's not nailed down.

8 Where values are stored, a digital value,
9 for example, would be in a register as a person of
10 ordinary skill in the art would understand.

11 So, a status register would be a register
12 which is typically comprised of one or more
13 flip-flops that would contain the value of the
14 status.

15 BY MR. COURTNEY:

16 Q. Okay. Is the status register a hardware
17 component?

18 A. Yes. Ultimately a hardware component, yes.

19 Q. So you mentioned flip-flops as one example
20 of a hardware component that might constitute a
21 register. Are there other examples?

22 A. That's the most common, certainly.

23 Q. Okay. So starting near the bottom of
24 page 104 here, you say, "A POSITA would have
25 understood or at least found obvious that data

1 representative of Grundy's status response would be
2 available from memory such as a register to ensure
3 the memory device could obtain the status response
4 data to return in response to a status request."

5 Do you see that?

6 A. Yes.

7 Q. And your reference there to "Grundy's
8 status response" I think is a reference back to
9 Grundy's use of that term, as you quote it up above
10 from Grundy's paragraph 32.

11 A. Yes.

12 Q. Is that correct?

13 A. Yes.

14 Q. Okay. So I'd like to sort of explore the
15 two alternatives in your phrase "understood or at
16 least found obvious."

17 When you say that "A POSITA would have
18 understood that data representative of Grundy's
19 status response would be available from memory such
20 as a register," are you saying that Grundy discloses
21 storing its status response in a register?

22 MR. STEPHENS: Objection to form.

23 THE WITNESS: There is that suggestion, but
24 Kilbuck makes it extra clear by saying it would be
25 literally stored in a register.

1 BY MR. COURTNEY:

2 Q. Okay. What component in Grundy corresponds
3 to the status register of Claim 1?

4 A. It does not identify a component literally,
5 but, like I said, a POSITA would understand that,
6 you know, if you have a value, a digital value like
7 a status, which might be one or a few bits, would be
8 almost assuredly stored in a register, but that we
9 don't have that absolute guarantee.

10 Q. Okay. Is anything that's capable of
11 storing a status necessarily a status register?

12 A. It's the -- by far the most efficient way
13 to access the value stored as the status. If you
14 used -- if you were to store it in a memory, you
15 would have to go and decode addresses and move data
16 to a buffer and so forth. It would just take many
17 times longer to access it. So, therefore, registers
18 are by far the preferred way to do this.

19 Q. Okay. In the same sentence of
20 paragraph 104 of your declaration, you say, "A
21 person of ordinary skill would have at least found
22 obvious that data representative of Grundy's status
23 response would be available from memory such as a
24 register."

25 Do you see that?

1 A. Yes.

2 Q. Okay. So to be clear, Grundy wouldn't
3 necessarily have to store its status response in a
4 status register, would it?

5 A. Well, it's -- let's see. What I'm saying
6 is a POSITA would have found it obvious that it
7 would be stored -- the status would be stored on the
8 chip, and the most common way by far would be a
9 register.

10 Q. Okay. If an implementation of Grundy
11 didn't store its status response in a status
12 register, adding a status register to that kind of
13 implementation would require modifying the hardware
14 of that implementation, wouldn't it?

15 A. Yeah, that's probably true.

16 Q. Nearer to the end of paragraph 104, so now
17 we are on page 71, you quote a textbook by someone
18 named Cappelletti?

19 A. Yes.

20 Q. Just for fun, I will introduce that
21 exhibit. This is -- I will put it up. It is an
22 eight-page document bearing the title "Flash
23 Memories," listing Paolo Cappelletti as an editor,
24 and it's bearing a Bates stamp INFINEON-1009 on its
25 first page.

1 (Exhibit 1009 marked for
2 identification.)

3 THE WITNESS: Yes.

4 BY MR. COURTNEY:

5 Q. Can you take a look at what I have sent
6 over and verify that that's what you call
7 Cappelletti, or Exhibit 1009, in your declaration?

8 A. Yes.

9 Q. In this quote from Cappelletti, I mean, you
10 can go to the source or just your declaration, you
11 are quoting it, you say, "The user or the external
12 microcontroller can check the status of the
13 operation using either the R/B pin on the status on
14 DQ0 to DQ7," parenthesis, "the former can be issued
15 in either the 'Data Poling - Toggle Bits' or 'Status
16 Register' fashion," end parenthesis.

17 Do you see that?

18 A. Yes.

19 Q. Cappelletti's R/B pin isn't mentioned
20 anywhere in Grundy, is it?

21 A. I don't believe so.

22 Q. And, similarly, Cappelletti's DQ0 through
23 DQ7 aren't mentioned anywhere in Grundy, are they?

24 A. Well, not that name, but that bus for data,
25 various types of data, is shown.

1 Q. Okay. And Cappelletti's external
2 microcontroller isn't the same thing as Grundy's
3 memory controller, is it?

4 A. That's -- well, yeah, Grundy is seeking to
5 build an on-chip, but in any event, it's a
6 microcontroller, so it would certainly have the same
7 function.

8 Q. Do you agree that it would be possible to
9 implement a flash memory device without implementing
10 Cappelletti's R/B pin?

11 A. Let's see. Let's -- I -- while I did dig
12 up that reference, I'm going to have to review it.

13 Let's see. Certainly you would not need
14 the R/B pin if you are building this on-chip, as
15 Grundy is doing.

16 Q. Do you agree that it would be possible to
17 implement a flash memory device without implementing
18 Cappelletti's DQ0 through DQ7?

19 MR. STEPHENS: Objection. Form.

20 THE WITNESS: Well, Grundy has the exact
21 equivalent in the N, capital N, lines, bus lines for
22 input and output of the memories, and in this case
23 Cappelletti is showing that as eight bits wide.

24 BY MR. COURTNEY:

25 Q. Returning to the sentence from Cappelletti

1 that you quote, it ends at the remark where
2 Cappelletti says that "the former can be issued in
3 either 'Data Polling - Toggle Bits' or 'Status
4 Register' fashion."

5 When Cappelletti says, "the former," what
6 do you understand that to be referring to?

7 A. The R/B pin.

8 Q. Okay.

9 A. And since the microcontroller is external,
10 you know, you need to have a pin that -- where you
11 can access that data. But if -- in Grundy, that
12 controller is on the chip, so you wouldn't have a
13 pin for it.

14 Q. What is "'Data Polling -Toggle Bits'
15 fashion"?

16 A. Yeah. You can have what's effectively a
17 flip-flop that is toggled. Say, when you start a
18 read, you could flip the -- well, it's like a
19 register, too, a flip-flop. You flip it to -- say,
20 from zero to one, which means a read is taking
21 place, or it could be a write. And then when that
22 command is done executing, you flip it back to zero
23 or toggle it back to zero.

24 So, it's much like a register. You know,
25 in fact, it contains almost all of a flip-flop in

1 each case.

2 Q. Is Cappelletti's R/B pin a status register?

3 A. That would be a -- that's how you view
4 the -- what the toggle bit is or the content of the
5 status register. You know, that's how the
6 microcontroller can access it.

7 Q. So Cappelletti also says that this pin can
8 be used in "'Status Register' fashion." What is
9 "'Status Register' fashion"?

10 A. Well, status he defines as the status of an
11 operation, like is it -- has it initiated, has it
12 completed. And so that status would -- as I
13 mentioned, a POSITA would understand that that would
14 likely be stored in a register.

15 You could have a slightly modified register
16 that just automatically toggles. Like since there's
17 only -- in most cases you might want to have just
18 two states, meaning that a command is currently
19 being executed or it's not -- nothing is being
20 executed because, for example, it's done.

21 Q. Okay. Turning to paragraph 105 on the same
22 page, 71, you say that "Kilbuck also teaches a
23 status register configured to indicate a status of
24 the flash memory device," and you quote and cite,
25 among other things in Kilbuck, Kilbuck's

1 paragraph 33. Do you see that?

2 A. Yes.

3 Q. In the portion you quote, Kilbuck begins
4 its paragraph 33 by saying that certain features
5 could be present, quote, "in one embodiment of the
6 present invention," end quote.

7 Do we agree that an embodiment of Kilbuck
8 would not necessarily have to use a status register?

9 A. Well, okay. So here you see that Kilbuck
10 does have the R/B pin, you know, ready or busy. And
11 its notice says be sharp up above in the
12 paragraph 104, because that means not busy, so ready
13 or not busy, which means the same thing.

14 And so Kilbuck does teach that pin, but
15 that's only if you need it externally. Like if you
16 were going to use an external controller, then you
17 would need a pin by which you can access the -- get
18 the status register value to a different chip via
19 the pin.

20 But if you are doing this on-chip with an
21 internal controller, then it is internal like a flag
22 bit or status bit stored in the register.

23 Q. Is Kilbuck's ready/busy pin a status
24 register?

25 A. I didn't hear that clearly.

1 Q. Sorry. Is Kilbuck's ready/busy pin a
2 status register?

3 A. No. It's a pin. And it's how chips
4 communicate with one another, say, on a printed
5 circuit board. So if you want data from internal to
6 a chip to go outside, you bring it out to a pin.
7 And that pin is -- can then be accessed via the
8 printed circuit board to another chip. So that is
9 completely a different concept than a register.

10 Q. Okay. If we could turn to paragraph --
11 well, now let's actually go back to Grundy,
12 Exhibit 1005. If we could turn to paragraph 39 of
13 Grundy. Could you review that paragraph and let me
14 know when you are done?

15 A. You said Grundy paragraph 35?

16 Q. 39.

17 A. Oh, 39.

18 Q. Yeah.

19 A. Yes, I have reviewed 39.

20 Q. Okay. So paragraph 39 begins, "In a
21 specific embodiment." And when Grundy says that, is
22 he talking about a specific embodiment of its
23 Figure 3?

24 A. That is likely.

25 Q. Okay.

1 A. Kind of the main -- kind of his default or
2 main architecture, Figure 3.

3 Q. So Grundy says, "In a specific embodiment,
4 each of the point-to-point signaling links is
5 implemented by conductive traces printed on a
6 substrate to which the memory devices are mounted,
7 enabling signaling rates of 12.8 gigabits per second
8 per pin and higher."

9 Is that a typical signaling rate for flash
10 memory devices in the 2005 time frame?

11 A. I think it's appreciably higher than what
12 was available commercially at that time.

13 Q. What would have been a typical signaling
14 rate for flash memory devices in the 2005 time
15 frame?

16 A. I haven't reviewed that recently, so I
17 don't remember that number offhand.

18 Q. Was 12.8 gigabits per second per pin a
19 typical signaling rate for DRAM memory devices in
20 the 2005 time frame?

21 A. Let's see. You know, that's a -- that
22 number is -- was, say, typical for very short
23 connections. And so in the case of Grundy, you
24 know, there's a serial connection of chips that are
25 one next to the other so the interconnect links are

1 very short, so the delays are very short there, and
2 not a whole lot of noise on those wires because they
3 are so short, and so such high rates were possible.

4 But if you are talking about, you know,
5 access into memories themselves where there's
6 decoding that take place and so forth, it's, yeah,
7 probably not nearly that high.

8 Q. Is 12-point rate -- sorry -- 12.8 gigabits
9 per second per pin a typical signaling rate for
10 flash memory devices today?

11 A. Yeah. I don't have that number handy. I
12 could not comment on that.

13 Q. Okay.

14 A. I certainly could find out, but I --

15 Q. Sure.

16 A. We can do that during a break. But I don't
17 know that offhand.

18 Q. So Grundy's paragraph 39 also says, "In
19 other embodiments, direct-connect structures may be
20 used to establish electrical signaling rates
21 approaching and possibly exceeding 40 gigabits per
22 second per pin."

23 Is that a typical signaling rate for flash
24 memory devices in the 2005 time frame?

25 A. Well, again, that would be rather high for

1 the 2005 time frame, but so the 40 is what's claimed
2 in that patent application.

3 Q. Do you know of any flash memory system that
4 achieves a signaling rate of 40 gigabits per second
5 today?

6 A. Again, I have not researched that in
7 preparation here for the deposition, so I don't
8 know.

9 Q. Okay. So let's turn to your declaration,
10 and let's go to paragraph 65 of your declaration.
11 That's on page 39. Could you let me know when you
12 are there?

13 A. Yes, I am there.

14 Q. So this is your discussion of the preamble
15 of Claim 1 in the 381 patent which recites, "A flash
16 memory device comprising," and then in this
17 following paragraph, 66, you quote and then
18 reproduce Grundy's Figure 3.

19 Do you see that?

20 A. Yes.

21 Q. Okay. So, you say that Grundy describes
22 that the memory devices can include flash memory.

23 Do you see that?

24 A. Yes.

25 Q. So, in Grundy's Figure 3, which you

1 reproduce on the next page, are you saying that each
2 of the devices 107-1, 107-2, et cetera, can be flash
3 memory devices?

4 A. Yes.

5 Q. Okay. And Grundy also says that storage
6 arrays of different types can be part of the chain
7 in Figure 3, correct?

8 A. That is possible. He does claim that as a
9 possibility, yes.

10 Q. So, for example, Grundy says that the
11 memory devices could include static RAM and dynamic
12 RAM arrays, correct?

13 A. Yes.

14 Q. Okay. When you discuss Grundy's Figure 3
15 in the context of Claim 1, are you considering an
16 implementation of Figure 3 in which all of the
17 devices, 107-1, 107-2, so forth, are flash memory
18 devices?

19 A. That -- yeah, that's right. I think that's
20 fair to say.

21 Q. Okay. So Grundy's Figure 3 uses a symbolic
22 parameter N to denote the number of devices in the
23 chain of Figure 3. When you identify flash memory
24 devices in Figure 3, are you assuming any particular
25 value of N?

1 A. No. It could be any integer.

2 Q. Okay. So, as a preface to this next
3 question, I'll just say, what I'm generally trying
4 to get at here is, in your declaration there's
5 various statements about what Grundy-Kilbuck teaches
6 or renders obvious, and I'm just trying to explore
7 what might matter in what Grundy-Kilbuck is and what
8 doesn't matter in what Grundy-Kilbuck is, and this
9 would certainly be a lot easier if Grundy had only
10 one figure without any ellipses or parameters in it,
11 but it doesn't.

12 It's not a question, but I'm just putting
13 that out there to help you understand my next
14 question, which will involve paragraph 76 on page 45
15 of your declaration.

16 Could you let me know when you are there?

17 A. Yes, I am there.

18 Q. So this is where you begin to discuss -- I
19 mean, it runs over the next page as well -- the
20 clock input port and clock signal elements of
21 Claim 1, and you reproduce Grundy's Figure 5A.

22 Do you see that?

23 A. Yes.

24 Q. So here we are discussing Figure 5A where
25 the quoted paragraph expressly says has "eight

1 chained memory devices," correct?

2 A. That's literally what's shown in that
3 Figure 5A, yes.

4 Q. Okay. And they are labeled 155-1, 155-2,
5 up to 155-8, correct?

6 A. Yes.

7 Q. Okay. So for purposes of what Figure 5A is
8 telling us about what you call Grundy-Kilbuck, you
9 would be taking device 155-1 of Figure 5A to be a
10 flash memory device, correct?

11 A. Yes.

12 Q. And would device 155-2 of Figure 5A also be
13 a flash memory device, in your reading?

14 A. In my combination, it would be if I -- but
15 I -- yeah, it depends on the specific embodiment
16 that one had in mind, but I did focus on
17 implementations that were -- all these memory
18 devices were flash memory devices.

19 Q. Okay. And when you do that, are you
20 assuming that all eight of those flash memory
21 devices in Figure 5A are identical to one another?

22 A. I think that would be what one would expect
23 most commonly to be used in the system, not
24 exclusive, but most common.

25 Q. Okay. So let's briefly turn to

1 paragraph 59 of your declaration on page 35.

2 A. Okay.

3 Q. It's a paragraph beginning "Motivations."
4 Do you see that?

5 A. Yes.

6 Q. Okay. So in the next couple of paragraphs
7 here you discuss aspects of how, in your opinion, a
8 person of ordinary skill would have been motivated
9 to pursue what you call the Grundy-Kilbuck
10 combination, correct?

11 A. Yes.

12 Q. Would your opinion on the motivation to
13 combine Grundy and Kilbuck change depending on how
14 many flash memory devices are in the combination?

15 A. No.

16 Q. Would your opinion on the motivation to
17 combine Grundy and Kilbuck change depending on
18 whether different flash memory devices in the
19 Grundy-Kilbuck combination were identical to one
20 another?

21 A. If the different devices were identical?

22 Q. Yeah.

23 A. Is that what you're asking, or --

24 Q. Meaning identical in design. They are
25 physically different objects, but --

1 A. Yeah. Okay. All right. Well, perhaps
2 read it -- read the question again or --

3 Q. Sure. Would your opinion on the motivation
4 to combine Grundy and Kilbuck change depending on
5 whether there were -- those devices were identical
6 or not?

7 A. Or not?

8 Q. Yeah.

9 A. No, it would not change.

10 Q. Would your opinion on the motivation to
11 combine Grundy and Kilbuck change depending on
12 whether some of the devices in the Grundy chain
13 weren't flash memory devices?

14 A. I don't think so, but then I haven't really
15 considered that possibility. So I haven't thought
16 that one through.

17 Q. Okay. So, in Grundy's Figure 5A
18 embodiment, does Grundy disclose any way by which
19 Grundy's memory controller can determine which
20 devices in the chain are flash memory devices?

21 A. I mean, normally a controller is
22 implemented to specifically deal with what the
23 architecture of the memory devices is, so, you know,
24 you would not normally have a memory controller and
25 then say, "Hey, memory controller, go figure out

1 what you are connected to." That's not normally
2 what would be done, so --

3 Q. Could there be an embodiment of Grundy's
4 Figure 5A in which the memory controller has no
5 information about which devices on the chain are
6 flash memory devices?

7 A. I do believe it's possible that a memory
8 controller could be implemented that would deal with
9 a non-homogenous type -- set of memory devices, but
10 I believe that the memory controller would need to
11 know that information before it's fully implemented.

12 Q. Okay. So, let's see which paragraph to
13 discuss. If we could move to page 45 of your
14 declaration, paragraph 76, where you quote Grundy's
15 paragraph 43, which describes Grundy's Figure 5A,
16 and then you reproduce Grundy's Figure 5A.

17 Do you see where that is in your
18 declaration?

19 A. Yes, I do.

20 Q. Okay. So MC 151 in Figure 5A is Grundy's
21 memory controller, correct?

22 A. Yes.

23 Q. And this box labeled MEM 1, 155 sub 1 is
24 the first in a chain of Grundy's memory devices,
25 correct?

1 A. Yes.

2 Q. Okay. So in your analysis you are
3 considering an embodiment of Figure 5A where this
4 block 155 sub 1 is a flash memory device, correct?

5 A. Yeah, that's the combination that I am
6 considering, yes.

7 Q. Okay. So in your combination, you would be
8 identifying this block 155 sub 1 with the claimed
9 flash memory device of Claim 1, correct?

10 A. Yes, that's correct.

11 Q. Okay. So, if we could -- I mean, we are
12 looking at a Grundy figure here. Why don't we turn
13 to Grundy itself. Let's look at paragraph 47 of
14 Grundy. It's page 37 of the exhibit. The exhibit
15 has its own page numbering at the bottom.

16 A. Yeah, I'm there.

17 Q. Okay. So here Grundy begins to discuss
18 Figure 6, which -- well, let's see. Grundy's
19 Figure 6 is a timing diagram, showing the relative
20 timing of signals transmitted by the memory
21 controller 151 of Figure 5A, correct?

22 A. Yes.

23 Q. So if we turn to Figure 6 itself. And I'm
24 sorry that I don't have a way of putting both of
25 those things up at the same time.

1 A. Yeah, I'm there, though.

2 Q. Figure 6 has this annotation at the top
3 left that says, "from controller." That controller
4 in that annotation is the controller MC 151 of
5 Grundy's Figure 5A, correct?

6 A. Yes.

7 Q. In the upper half of Figure 6 is depicting
8 the timing of signals being transmitted from
9 Grundy's controller MC 151 to the first device, 155
10 sub 1, in the chain depicted in Figure 5A, correct?

11 A. Yes.

12 Q. So in the lower half of Grundy's Figure 6,
13 there's a legend that says, "From Initial Memory
14 Device." Do you see that?

15 A. Yes.

16 Q. So the initial memory device in that
17 notation in Figure 6 would refer to the first
18 device, 155 sub 1, in Grundy's Figure 5, is that
19 right, 5A?

20 A. Yes, the output of that one -- yeah, that
21 first device, yes.

22 Q. Okay. In the lower half of Grundy's
23 Figure 6, it's depicting the timing of a
24 transmission of signals from the device 155 sub 1 in
25 Figure 5A to the device 155 sub 2 in Figure 5A?

1 A. Well, certainly, yeah, what is output from
2 the first device.

3 Q. Oh, okay. Do you see where Grundy's
4 Figure 6 has this annotation T sub P?

5 A. Yes.

6 Q. What is T sub P?

7 A. It's, basically, how much the clock signal
8 is delayed by, you know, due to wire delays, and
9 then also if that clock is, say, buffered to -- you
10 know, typically it would have to be buffered if you
11 are passing it along, so there would be -- it's the
12 delay in getting the clock to the next device -- or
13 from the controller to the first device.

14 Q. Okay. So the top half of Figure 6 is
15 showing us relative timing of signals clock, bus,
16 valid, and CMD, which I might verbalize as command,
17 being transmitted from Grundy's controller 151,
18 correct?

19 A. Yes.

20 Q. And then the bottom half is showing the
21 relative timing of the same signals as they are
22 transmitted from Grundy's device 155 sub 1?

23 A. Yes. Let's see. Check one thing here.

24 Yes.

25 Q. Okay. So if we could turn -- you have an

1 annotated version of part of this figure in
2 paragraph 86 of your declaration, which begins on
3 page 55, but the annotated figure itself is on
4 page 56.

5 A. Okay.

6 Q. Are you able to see that?

7 A. Yes.

8 Q. This excerpt is showing us the upper
9 portion of Grundy's Figure 6; is that right?

10 A. It is.

11 Q. So it's depicting the timing of signals
12 transmitted by the memory controller 151 in Grundy's
13 Figure 5A?

14 A. Yes. Let's just absolutely verify that
15 that's what I'm seeing here.

16 Yes, that is correct.

17 Q. So I have a few questions about the
18 labeling here, in particular what these labels are
19 trying to tell us about the contents of
20 transmissions and what these labels are trying to
21 tell us about the timing of those transmissions.

22 So, first, just to understand what some of
23 these labels mean, what is the label "Clock"?

24 A. That is the clock that's being sent to the
25 first device, basically, that -- you know, it's

1 immediately output from the controller.

2 Q. Okay. And what is "Bus"?

3 A. That would be the data lines emanating from
4 the controller.

5 Q. And the sort of horizontal axis in this
6 figure represents time; is that right?

7 A. Yeah.

8 Q. All right. So things that are like
9 directly above one another are being depicted as
10 happening at the same time?

11 A. Yes, yeah.

12 Q. Okay. So, in this part of the diagram
13 that's on the bus portion, we have this -- I don't
14 know what you call it -- a lozenge labeled A. Do
15 you see that?

16 A. Yes.

17 Q. What is A?

18 A. It's the first data element. It could be a
19 single bit. It could be a group of parallel bits.

20 Q. Okay. And in your claim mapping, A is
21 identified with an example of at least one of
22 command data, address data, input data, and output
23 data in the sense of Claim 1; is that correct?

24 A. Yes.

25 Q. Okay. So around this lozenge we have this

1 blue box with the legend that says, "Transfer of
2 data (e.g., command, address, input, or output)
3 values."

4 Do you see that?

5 A. Yes. This didn't come out the way I sure
6 thought I had it drawn when I sent it to the
7 attorneys, but -- but that's the gist of it.

8 Q. Okay. So what is Figure 6 telling us about
9 when Grundy's controller 151 begins transmitting the
10 value A?

11 A. Basically, it's at the -- the convention by
12 POSITAs is that the middle of the clock
13 transition, 50 percent point of the clock
14 transition, is when it's understood, you know, that
15 data propagation would begin, and that's where you
16 see the -- sort of the X in the beginning of data A.
17 So there is a potential transition there.

18 It's drawn with an X like that, meaning
19 that it's not known if you are changing one to zero
20 or zero to one. It's just there's a change going on
21 there, and that change on the bus data is
22 synchronous with the center of the clock waveform
23 transition.

24 Q. Okay.

25 A. So that dashed line, the falling edge is --

1 I thought I had that drawn right through the X,
2 but --

3 Q. I see.

4 A. -- it didn't quite come out that way. That
5 not where I want it.

6 Q. As it's drawn, it's a little to the left of
7 that tip of the A lozenge.

8 A. Yes.

9 Q. But you would imagine drawing it right down
10 the middle?

11 A. Yes.

12 Q. And that indicates a time that would be
13 telling us, in your reading, that is the beginning
14 of the transmission of the value A, correct?

15 A. Yes, that's right.

16 Q. Okay. And as you interpret the figure,
17 that transmission is beginning while the clock
18 signal is falling; is that correct?

19 A. Yes, at the 50 percent point is the
20 standard.

21 Q. Okay. So, I'd like to understand a little
22 more about what is happening at Grundy's controller
23 in between these two red dotted lines.

24 So, on the previous page of your
25 declaration, which is actually also the previous

1 paragraph I'm now interested in, paragraph 85, you
2 quote Grundy's paragraph 47. Can you go to that?

3 A. Yes.

4 Q. Okay. In the portion you quote, Grundy
5 says, "the transmit interval is a half cycle of the
6 clock signal 172 sub 1."

7 Is that indicating to us that in that
8 interval of time indicated by the region between
9 those two red dotted lines in Figure 6, Grundy's
10 controller is transmitting that value A?

11 A. Yeah. It's from 50 percent to 50 percent,
12 and that's the, in this case, the low half of the
13 clock cycle.

14 Q. Okay. So then in the interval of time
15 indicated by the second blue box, Grundy's
16 controller is transmitting the value B?

17 A. Right. Again, from the 50 percent point of
18 the clock rising to the 50 percent point of the
19 clock falling, which is the upper half of the clock
20 cycle, data element B is transmitted.

21 Q. Okay. So we have been talking about all of
22 this from the point of view of transmissions from
23 Grundy's controller and the timing of transmissions
24 from Grundy's controller, because that's what's
25 depicted in this portion of Figure 6; is that right?

1 A. Yes.

2 Q. So in the lower half of Grundy's Figure 6,
3 which, unfortunately, is excerpted in 86, it's also
4 a transmission diagram, right?

5 A. Let's see. Did you want me to move to a
6 different paragraph, you said?

7 Q. If you could look at the lower half of
8 Grundy's Figure 6. We just need to peek at it.

9 A. Oh, sure, sure. Okay.

10 Q. So this is also a transmission diagram,
11 right?

12 A. Yes.

13 Q. Only now it's depicting the timing of
14 transmissions from Grundy's first memory device,
15 155-1, to the second memory device, 155-2; is that
16 right?

17 A. Yes.

18 Q. So if we could look right -- now I'm
19 looking at Figure 6, because this is something that
20 isn't in your annotated version because it's only
21 got half of it.

22 If we could look right at Figure 6 for a
23 moment in Grundy. There is this dotted vertical
24 line running sort of from the -- near the edge of
25 the B lozenge up top, down through to the second

1 half of the diagram below, sort of a blank lozenge
2 down below, and it seems to be used to define the
3 start of an interval -- or to indicate the start of
4 an interval TP. Do you see that?

5 A. Yes.

6 Q. So is that vertical line -- I'm wondering,
7 because it's one of the few things in this diagram
8 that sort of connects them. It runs from one to the
9 other.

10 Does that vertical line indicate that those
11 two portions of the diagram at different parts of
12 the vertical line are the same moment in time?

13 MR. STEPHENS: Objection. Form.

14 THE WITNESS: Yeah. The dotted lines, like
15 the usual convention would be to take them at the
16 50 percent point, but they chose to pick at least
17 the same point within the clock window or the bus
18 transition, whatever, and so faithfully measured the
19 number of cycles. In this case it's two half
20 cycles. Delay is the TP.

21 But, yeah, it is assumed that, at least in
22 this hypothetical example, that that vertical line
23 is a particular time point common to both.

24 BY MR. COURTNEY:

25 Q. Okay. So at the moment of time indicated

1 by that dotted line, Grundy's memory controller
2 155-1 has stopped transmitting the value A and has
3 begun to transmit the value B; is that right?

4 A. Well, they are indicating that that's right
5 between the two, but that's -- but I would have
6 preferred that that dotted line be right at the X
7 point in each case.

8 Q. Right at the X point?

9 A. Because their intention is that that's
10 right between the two --

11 Q. Oh.

12 A. -- but they just chose a slightly different
13 point on the waveform. I mean, you have to keep in
14 mind these waveforms in reality on a chip don't look
15 anything as ideal as this. But this is all very
16 hypothetical.

17 Q. Since we are to the right of the X point a
18 little bit, like as they have drawn it, I just want
19 to make sure I'm reading this correctly, if I'm at
20 the actual point of that dotted line where it's
21 actually on part of the B lozenge, at that moment in
22 time we are not transmitting -- the memory
23 controller is not transmitting the value A anymore;
24 is that correct?

25 A. That's true.

1 Q. And the memory controller is transmitting
2 the value B at that moment in time; is that right?

3 A. It's certainly about to, yeah.

4 Q. Okay. So at the same moment in time, if we
5 look down below at the lower half, we see that
6 Grundy's memory device 155-1 at that moment in time
7 is not transmitting anything on bus to the memory
8 device 155-2; is that right?

9 A. That's true. Certainly, yeah, nothing
10 worth paying attention to.

11 Q. Yeah. And then looking midway between the
12 two vertical dotted lines where this lozenge labeled
13 A begins on the bottom half of the diagram, that
14 represents -- where that lozenge A begins, is that a
15 depiction of where Grundy's memory device 155-1
16 begins to transmit the value A on the bus to memory
17 device 155-2?

18 A. Yeah. The X lines up in time with the
19 rising edge of the clock right above it and also to
20 the 50 percent point of valid, for example.

21 Q. Okay. So let's go back to page 56 of your
22 declaration, which was where we were before in the
23 annotated version of the diagram.

24 Are you back there yet?

25 A. Page 56, was it?

1 Q. Yeah, paragraph 86.

2 A. Oh, yes.

3 Q. Yeah. Okay. Did we agree that this
4 portion of Figure 6 that you are excerpting here
5 doesn't depict when the value A is received by the
6 memory device 155-1?

7 A. Yeah. It's when it's being sent to the
8 device, so there may be some delay until it actually
9 receives that data.

10 Q. Okay. So, in your annotated Figure 6 on
11 page 56, we have this blue box you have drawn around
12 A. I want to talk about sort of two times
13 corresponding to the left edge of the box and the
14 right edge of the box. Okay?

15 At the time that we are talking about, at
16 the time indicated by the left edge of the box,
17 Grundy's memory device 155-1 hasn't yet received
18 value A; is that correct?

19 A. Yeah. Again, let me remind you that the
20 way I drew this in my draft was that that box starts
21 at the X --

22 Q. At the X?

23 A. -- for A and ends at the X after A.

24 Q. Okay.

25 A. Similarly for B. But, yeah, subject to

1 that.

2 Q. So at that X that begins the A lozenge, at
3 that time Grundy's memory device 155-1 hasn't yet
4 received the value A; is that right?

5 A. That's correct, yes.

6 Q. And by the time indicated by the other side
7 of that blue box, Grundy's memory device 155-1 has
8 received the value A; is that correct?

9 A. No, we can't say that for sure. It's just
10 that's the interval at which the data is being sent
11 from the controller. There's nothing here to
12 indicate when it's received, per se.

13 Q. Okay. So now, I guess, it might be helpful
14 to focus on disclosures about the memory device
15 itself as it receives that value.

16 So, let's turn to --

17 MR. STEPHENS: Counsel.

18 MR. COURTNEY: Yeah.

19 MR. STEPHENS: We have been going for about
20 an hour and 20 minutes. Do you want to take a break
21 within a few minutes?

22 MR. COURTNEY: Oh, yeah, sure. Well, let's
23 stop here, actually. This will be a good place to
24 stop.

25 THE WITNESS: Yeah, that would be good.

1 MR. STEPHENS: Ten minutes?

2 MR. COURTNEY: Yeah, sounds good.

3 MR. STEPHENS: Thanks, everyone.

4 (Recess taken from 9:26 a.m. to 9:36 a.m.)

5 MR. COURTNEY: Are we back on? I can't
6 tell. Sorry. Is anyone else having an issue with
7 realtime?

8 MR. STEPHENS: I'm seeing everything.

9 MR. COURTNEY: Here we go. Sorry. There
10 was a little hiccup there.

11 BY MR. COURTNEY:

12 Q. So, if we could turn, Dr. Sechen, to the
13 portion of your declaration that begins at
14 paragraph 106.

15 A. 106.

16 Q. That's page, I think, 72, if I'm not
17 mistaken.

18 A. Okay.

19 Q. We are talking, this is in the context of
20 Claim 2, which you reproduce there, "The flash
21 memory device is claimed in Claim 1, wherein the
22 command data is latched at the first rising edge of
23 the clock signal after the transition of the control
24 signal."

25 What does it mean to say the command data

1 is latched?

2 A. Well, in some sense it's -- you know, it
3 kind of means that a flip-flop is latching the data
4 in response to that edge.

5 Q. Okay. Claim 2 uses latch as a verb, and
6 when we were discussing at the beginning your
7 experience with flash memory and the components of
8 flash memories, you mentioned a thing called a
9 latch. What is a latch?

10 A. Typically a flip-flop or a bank of
11 flip-flops --

12 Q. When you say "typically," are there other
13 things that can be latches?

14 A. Well, there's what's known as literally a
15 latch which is half of a flip-flop. And a latch is
16 transparent half a clock cycle and opaque the other
17 half cycle. Whereas a flip-flop grabs the data in
18 response to an edge of the clock driving it.

19 Q. Let's look at your annotation of Grundy's
20 Figure 6 that begins on page -- it's paragraph 107.
21 It's actually two pages ahead on page 74 -- or 70 --
22 yeah, 74 is where this annotated figure is.

23 Could you just review paragraph 107, which
24 runs across pages 73 and 74, and let me know when
25 you are done?

1 A. Okay. Yes, I'm ready.

2 Q. At this point in your declaration, are each
3 of the values A, B, C, and so on in this annotated
4 figure being identified with the command data of
5 Claim 2?

6 A. Certainly, the buses in Grundy N, being N,
7 capital N, wide, as I recall, they are used for
8 sending command data as well as input and output
9 data.

10 Q. Okay. So on your annotated figure, we have
11 this blue text labeled "Command data latched at the
12 first rising edge of the clock signal after the
13 transition of the clock signal."

14 And just as a preface, again, I'm not a
15 person of ordinary skill, it seems like this
16 annotation might be telling us multiple things. It
17 might be indicating what the claimed command data is
18 in the mapping between Grundy's Figure 6 in Claim 2,
19 and it might also be identifying a moment in time in
20 which the command data of Claim 2 is latched in
21 Grundy, or it might be doing both of those things or
22 more one than the other. So, that's just some
23 context for these questions. I will take them one
24 at a time.

25 A. Uh-huh.

1 Q. In this annotated figure -- like there's,
2 basically -- it's kind of like what we did with the
3 last figure. There's a content issue and there's a
4 timing issue, and we will just take them one by one.
5 Pardon me.

6 So, in this annotated figure on page 74, is
7 the value B in this box what you identify as the
8 command data that is latched at the first rising
9 edge of the clock signal after the transition of the
10 control signal in the sense of Claim 2?

11 A. Yes.

12 Q. Okay. So as you read Figure 6, the value B
13 is latched by the memory device 155 sub 1 of
14 Grundy's Figure 5A during the interval of time
15 that's specified by this blue box?

16 A. No. This is really the output of the
17 controller, and it has to itself capture data and
18 send it. So, a flip-flop receives and passes data
19 along on the either rising edge or falling edge of
20 the clock. So it's actually capturing that data B
21 and sending it towards the first device.

22 Q. Okay. So if we were looking at, say, the
23 left edge of this rectangle, Figure 6 is not
24 depicting that the value B is latched at Grundy's
25 memory device 155-1 at the time of that left edge of

1 this rectangle; is that correct?

2 A. That's correct.

3 Q. Would the value B be latched at Grundy's
4 memory device 155-1 at the time indicated by the
5 right edge of the rectangle?

6 A. No, we cannot say that.

7 Q. Would it be possible to indicate on
8 Figure 6 the first time at which the value B would
9 be latched at Grundy's memory controller 155-1?

10 A. No.

11 Q. Or, sorry, memory device 155-1.

12 A. No.

13 Q. Does it make sense to talk about the last
14 time at which a value B would be latched at Grundy's
15 memory device?

16 A. Well, if you look at the lower half of the
17 Figure 6, you can get an indication of when B has
18 certainly arrived at that device because it's about
19 to be passed along as output as it's latched.

20 Q. I see. So if we are looking in the lower
21 part of Figure 6, it's that right-most vertical line
22 that's pointing at the beginning of the B lozenge,
23 and you're saying that that's an indication that the
24 value B has been latched at memory device 155-1 by
25 that time?

1 A. Yeah. Let's see. I'm looking at the lower
2 half of Figure 6, and between the B and C datas
3 there at that X point, certainly by that rising edge
4 of the clock, it surely has passed along the data --
5 has latched and passed along data B by that time at
6 the latest. It may have been a little earlier.

7 Q. Okay. Does memory device 155-1 have to
8 latch the data before it passes it along?

9 A. Yes.

10 Q. Okay.

11 A. It's sort of in concert, you know. As it's
12 latching it, that means it's stable on the output
13 bus, and so a subsequent device is -- can use it
14 with confidence.

15 Q. Okay. Could we turn to paragraph 108 of
16 your declaration. This is actually -- if we were
17 previously on page 74, this is just the next page.

18 A. Okay.

19 Q. This is a reproduction of Grundy's
20 Figure 19 here, and then also a fairly long quote
21 from Grundy's paragraph 92 here.

22 Do you see that?

23 A. Yes.

24 Q. Can you review paragraph 108, including the
25 quote, and let me know when you are done?

1 A. I think I'm ready.

2 Q. Okay. So after quoting paragraph 92 of
3 Grundy, you say, "A POSITA would have recognized
4 that Grundy discloses latching of command data
5 because a command word is loaded into a command
6 buffer."

7 When you say this, are you identifying the
8 loading of a command word into Grundy's command
9 buffer with latching in the sense of the 381 patent?

10 A. Well, 351 is the command buffer, and, you
11 know, you add elements to the buffer by toggling the
12 clock and it will be latching, and it does so on
13 each half of the clock cycle. So that command data
14 is loaded into that command buffer via latching it.

15 Q. Okay. I guess I'm wondering, one reading
16 of this sentence is just that Grundy's discussion of
17 the loading of a command word into Grundy's command
18 buffer is evidence of data being latched, even if
19 the latching actually occurs at some time other than
20 when it's loaded into the command buffer.

21 So, I'm wondering, is that what you mean,
22 or are you actually equating latching with loading a
23 command word into Grundy's command buffer?

24 A. Well, the command buffer is comprised of
25 flip-flops and they are going to capture -- you

1 know, you can present data on the -- command data on
2 the so-called data in line, and which points up to M
3 minus 1, let's say, in the figure of 351, and so
4 that data only securely resides there on a clock
5 toggle, and there's a clock input 326, and only on a
6 toggling of that clock will any data presented to
7 location M minus 1 be latched into that command
8 buffer.

9 Q. Okay. So to be clear, as you're applying
10 Grundy to Claim 2, the claimed latching occurs at
11 the moment a command word is transferred into the
12 command buffer of Grundy's Figure 19?

13 MR. STEPHENS: Objection. Form.

14 THE WITNESS: Well, this is one embodiment
15 illustrating that concept.

16 BY MR. COURTNEY:

17 Q. Okay. So, this is an example of when the
18 claimed latching occurs is when a command word is
19 transferred into the command buffer of Grundy's
20 Figure 19?

21 MR. STEPHENS: Objection. Form.

22 THE WITNESS: Yeah. This is, as I said,
23 it's just -- it's one embodiment and it does
24 illustrate a command being latched in the command
25 buffer in response to a clock rising edge, let's

1 say.

2 BY MR. COURTNEY:

3 Q. And in your view, Grundy discloses that a
4 command word is transferred into Grundy's command
5 buffer at the first rising edge of the clock signal
6 after the transition of the control signal, correct?

7 A. It --

8 MR. STEPHENS: Objection. Form.

9 THE WITNESS: It -- like we saw in the
10 waveforms, that it's actually latching data
11 depending on how many data elements there are, like,
12 you know, A through F or whatever, or more. It's
13 capturing and latching data on every edge of the
14 clock, and surely one of those rising edges occurs
15 after the command signal is raised.

16 BY MR. COURTNEY:

17 Q. Okay. Let's talk about the clock signal
18 that appears in Claim 2 for a minute.

19 So, if we just go back one page in your
20 declaration to page 75, you reproduce Figure 19
21 there. Is what you identify with the clock signal
22 in Claim 2 indicated anywhere in Figure 19?

23 A. It's 326.

24 Q. Okay. So near the bottom there's an
25 annotation 326 and there's a label CLK? Are we

1 looking at the same thing?

2 A. Yes, yes.

3 Q. So that input labeled CLK 326 is where
4 you -- is what you identify with the claimed clock
5 signal?

6 A. For this embodiment, yes.

7 Q. Okay. So at the first rising edge of the
8 signal CLK 326 in Figure 19, the command word is
9 transferred into the command buffer of Grundy's
10 Figure 19; is that correct?

11 A. Yeah. Certainly at a first rising edge
12 after the command N is raised, there would be
13 command data that would be latched into the command
14 buffer.

15 Q. Okay. I'm reasking this question because
16 there's a point at which you said "at a first rising
17 edge of the clock signal," and I just -- I want to
18 be clear whether we are using the same words.

19 The question was, is it true that at the
20 first rising edge of the signal CLK 326 in
21 Figure 19, after the transition of the control
22 signal, a command word is transferred into the
23 command buffer of Grundy's Figure 19?

24 MR. STEPHENS: Objection. Form.

25 THE WITNESS: Well, we know that, as this

1 is a so-called double data rate embodiment, that
2 data is latched on both the rising and falling edges
3 after the command N signal is raised, and so there
4 certainly would be data latched at the first rising
5 edge.

6 BY MR. COURTNEY:

7 Q. The first rising edge of the clock signal
8 after the transition of the control signal?

9 A. Yes.

10 Q. Okay. So let's go to the next paragraph,
11 which is 109 that begins on page 76.

12 A. Okay.

13 Q. So here it's a sentence, unfortunately,
14 that breaks across the two pages from 76 to 77.

15 A. Okay.

16 Q. You say, "Grundy's device loads a word of a
17 command packet into the buffer at each transition of
18 the clock signal, one on a rising edge and one on a
19 falling edge."

20 Now, again, I'm not a person of ordinary
21 skill. It's possible to read this language as
22 saying only that there's a one-to-one relationship
23 between clock transitions and words entering
24 Grundy's command buffer where maybe Grundy isn't
25 telling us the exact timing of when the word is

1 loaded into Grundy's command buffer. It's also
2 possible to read this as suggesting more than that.

3 And so my question is, with this statement,
4 are you saying here that Grundy's Figure 19
5 embodiment literally loads a word of a command
6 packet into its buffer at a rising edge of the clock
7 signal CLK 326?

8 A. It does, and it certainly initiates that
9 loading of the data because that's when the
10 flip-flop storing the data or capturing the data is
11 on the transition of the clock signal so -- or on
12 the first rising edge, for example, as well as a
13 falling edge.

14 Q. Okay. So further on in this paragraph, now
15 on page 77, you quote Grundy again twice. And let's
16 take the first one.

17 You quote paragraph 88, which says, "a
18 logic level clock signal 326 is generated by the
19 signal receiver 310 coupled to the input-side clock
20 line 152 and is supplied to the protocol engine 305,
21 I/O controller 303 and interface register 315."

22 Do you see that?

23 A. Yes.

24 Q. Okay. So what they are calling a logic
25 level clock signal in that sentence is the clock

1 signal CLK 326 we were just talking about in
2 Figure 19, correct?

3 A. Yes.

4 Q. And then we quote paragraph -- or, sorry,
5 then you quote paragraph 92 to the effect that it
6 says, "data packets and command packets are loaded
7 from the interface register into the input data
8 buffer 353 and command buffer 351, respectively, one
9 word at a time in response to transitions of the
10 clock signal 326." That's the quote.

11 A. Yes.

12 Q. Is it your opinion that when Grundy says
13 the command packets are loaded from the interface
14 register into the command buffer in response to
15 transitions of the clock signal, that that is
16 telling the person of ordinary skill that command
17 packets are loaded from the interface register into
18 the command buffer literally at transitions of the
19 clock signal?

20 A. Well, they are certainly latched in
21 response to a transition on the clock signal.

22 Q. I guess the question is about timing. Is
23 saying that they are latched in response to
24 transitions of the clock signal telling us when
25 latching occurs?

1 A. Well, it's the transition in the clock that
2 triggers the latching of the data, be that data
3 packets or command packets. So the clock is
4 triggering that loading of the data.

5 Q. Okay. So this quote from the same sentence
6 also mentions loading in command packets from
7 interface register. What is the interface register
8 in Grundy's embodiment that we are talking about
9 here?

10 A. Let's see. So the interface is shown on
11 Figure 17 of Grundy, and it would be a block 311.

12 Q. Okay. And so if we look at Grundy's
13 Figure 19, which you have two pages before in your
14 declaration, there's an annotation at the lower left
15 of this figure labeled "From Interface Register."

16 Is that Figure 19 reference to the
17 interface register referring to the interface
18 register that paragraph 92 is talking about?

19 A. I believe so. Let me just check here one
20 thing. Yeah, so 311 is indeed the interface
21 register. And, yes, Figure 19 expands on the I/O --
22 what's called I/O control on Figure 17, which is
23 also labeled 303, so --

24 Q. Oh, I see. In Figure 17 there's that clock
25 303?

1 A. Yeah.

2 Q. Okay. So the interface register is also
3 part of Grundy's memory device, isn't it?

4 A. It is.

5 Q. And so before a command word is loaded into
6 the command buffer of Figure 19, that command word
7 must first be captured in Grundy's interface
8 register, correct?

9 A. Yes.

10 Q. Is a command word latched when it first
11 appears in Grundy's interface register?

12 A. Certainly the data is latched multiple
13 times on the chain. There's no question about that.
14 And it would be latched by the interface register
15 first.

16 Q. Okay. Does a command word first appear in
17 Grundy's interface register at the first rising edge
18 of the clock signal after the transition of the
19 clock signal?

20 A. Yes, it would.

21 Q. Okay. Let's turn back to your annotation
22 of Figure 6 on page 74 in your paragraph 107. This
23 is that Figure 6 thing that we keep coming back to.
24 Let me know when you've got that in front of you.

25 A. Okay.

1 Q. So is it possible to indicate on this
2 figure the time when value A is captured in the
3 interface register of memory device 155-1?

4 A. Well, this would be -- the top part of the
5 figure would be indicated as to when the data is
6 latched and transmitted from the controller.

7 Q. Okay. Would it be more helpful to look at
8 the full Figure 6 from Grundy?

9 A. Yeah.

10 Q. Okay. I will give you a moment. Let me
11 know when you have got that up.

12 A. Okay.

13 Q. So is it possible to identify on this
14 figure the first time at which the value A is
15 captured in the interface register of memory device
16 155-1?

17 A. Again, it depends on different embodiments
18 of Grundy that are possible, but you certainly could
19 say that A in the 172-2 portion or the bottom half,
20 that -- well, actually, no. That's data put on the
21 output of the -- put on the output -- oh, yes.

22 So, let's see. So, Grundy also passes data
23 through from one device to the next, to the next,
24 and if it's doing that, then you could say, rightly,
25 that where A comes out on -- where it says from

1 initial memory device, where A comes out, that
2 that's from the interface register.

3 Now, let's see. But there is different
4 things that go on here. You know, for example, you
5 might be writing data into the storage array in
6 Figure 19, so you've -- and that's where you are
7 writing it, and you may not be passing it along any
8 further. So, in other words, the data transmission
9 is stopping there.

10 So, you know, I don't think the claim
11 element is particular as to which latch we are
12 talking about. I did not see a difference there,
13 whether it's latching at 351 in Figure 19 or the
14 interface register, because, depending on what's
15 going on, it's captured in both places.

16 Q. Okay. Let's turn to paragraph 87 in your
17 declaration, which is page 56, if I'm not mistaken,
18 where you are quoting from Grundy's paragraph 88.
19 Do you see this?

20 A. Yes.

21 Q. It may help to actually have Grundy along
22 with you here, but this paragraph that you are
23 quoting, Grundy's paragraph 88, that's discussing
24 Grundy's Figure 17; is that right?

25 A. Let's double-check, but I believe that's

1 right. Yes, that's right.

2 Q. Okay. So, in paragraph 88 in your
3 declaration, there's discussion of, in paragraph 88
4 as you quote it there, which refers to the logic
5 level clock signal 326.

6 Do you see that? It's near the beginning.

7 A. Oh, the beginning? Yeah, okay.

8 Q. That logic level clock signal 326 in
9 paragraph 88, is that indicated anywhere on
10 Figure 17?

11 A. Let's see. Which one are you asking about?

12 Q. Logic level clock signal 326.

13 A. Yeah, that's shown on Figure 17.

14 Q. Okay. Where is it?

15 A. At the bottom just to the left of "Jitter
16 Control."

17 Q. Oh, I see. Okay. And when Grundy says, I
18 guess, in the same quote that the logic level clock
19 signal 326 is generated by the signal receiver
20 310 --

21 A. Yes.

22 Q. -- does that correspond to the element
23 labeled 310 in Figure 17 --

24 A. Yes.

25 Q. -- to the left?

1 A. Yes.

2 Q. So in the same quote, Grundy is talking
3 about the input side clock line 152. Do you see
4 that in the --

5 A. Oh, yes.

6 Q. Okay. Now, does that correspond to the
7 element labeled "Clock In 152" in Figure 17?

8 A. Yeah, I guess in general 152 is the
9 clock -- is -- well, unfortunately, the output is
10 labeled the same, but -- although, they are not
11 going to be exactly the same waveforms, for sure.
12 But certainly there is a 152 that is the clock
13 input.

14 Q. Okay. If we could turn to paragraph 108 of
15 your declaration on page 75. Could you let me know
16 when you have that in front of you?

17 A. Yes.

18 Q. Okay. So here you reproduce Figure 19 and
19 you quote from Grundy's paragraph 92. Do you see
20 that?

21 A. Oh, 92, you said?

22 Q. Yeah.

23 A. Yes.

24 Q. Okay. So Grundy's paragraph 92 is
25 discussing the I/O controller 303 of Figure 17,

1 right?

2 A. Yes.

3 Q. Okay. And so that -- I think we actually
4 covered this earlier, but that's referencing that
5 block labeled "I/O Control 303" in Figure 17?

6 A. Yes. It is, yes.

7 Q. Okay. So in Figure 19 there's an input
8 labeled "CLK 326," which we discussed before. It's
9 near the bottom.

10 A. Yes.

11 Q. Okay. Is that signal the same signal as
12 the logic level clock signal 326 in Figure 17?

13 A. Let's see. I got to get these figures
14 lined up here. Yeah. Yes, it is the -- 326 is the
15 common signal there. It's the same clock.

16 Q. Okay. If we could go back to Grundy's
17 Figure 17 for a minute.

18 A. Yes.

19 Q. Okay. So there's this block at the
20 bottom -- or not a block. There's an input labeled
21 "Clock In 152" that we were just discussing.

22 Does that input receive a signal?

23 A. 152?

24 Q. Yeah.

25 A. That is the clock that's coming into --

1 Q. Okay. Where is the clock coming in from?

2 A. The clock output port of the previous
3 device or the controller, if it's the first.

4 Q. Okay. So that clock signal provided via
5 clock in and the logic level clock signal 326 are
6 not the same signal, are they?

7 A. Not exactly. There would be some delay.

8 Q. Okay.

9 A. But I did say one thing that was not
10 precise earlier, and that is, yeah, the interface
11 clock 311 is the same clock that goes to I/O control
12 303. So all that capturing happens at, basically,
13 the -- well, let's see. Let me check that
14 carefully.

15 No, I guess I'm going to stand by what I
16 said before.

17 Q. Okay. Is the device depicted in Figure 17
18 an example of what you would regard as a flash
19 memory device in a chain like one appearing in
20 Grundy's Figure 5A?

21 A. It's one embodiment that one could choose.

22 Q. Okay. So if we could turn to Grundy's
23 Figure 5A for a minute. Just stitching all these
24 figures together.

25 Do you have Grundy's Figure 5A in front of

1 you?

2 A. Yes.

3 Q. Okay. So if we look at Grundy's Figure 5A,
4 there's a signal labeled "Clock 152" coming out of
5 the memory controller. Do you see that?

6 A. Yes.

7 Q. So as you read Grundy, if you are
8 implementing this first memory device 155-1 with an
9 embodiment of Figure 17, would the signal labeled
10 152 in Figure 5A correspond to the signal clock in
11 152 in Grundy's Figure 17?

12 A. It would.

13 Q. Okay. So the signal labeled "Clock" in
14 Figure 5A is not the same as the signal labeled
15 "Logic level clock signal 326" in Grundy's
16 Figure 17?

17 A. Yeah, there's a propagation delay there.
18 Yes.

19 Q. Okay. While we are in Grundy, could we
20 just -- if we are in the figures of Grundy, can we
21 scroll back to Grundy's Figure 4A for a minute?

22 A. Yes.

23 Q. Okay. So this is a different embodiment
24 from Grundy's Figure 5A; is that correct?

25 A. Yes.

1 Q. What is MC 123A in Grundy's Figure 4A?

2 A. It's one of two presumably identical memory
3 controllers.

4 Q. Okay. And the other one would be MC 123B,
5 correct?

6 A. Yes.

7 Q. Okay. So Figure 4A has this annotation
8 where a kind of loop or something has been drawn
9 around, half's coming out of MC 123A, and there's
10 just a label 124A. Do you see that there?

11 A. Yes.

12 Q. What is that element 124A? What is that
13 indicating in Figure 4?

14 A. Well, that there's two ports there, an
15 output port and an input port.

16 Q. Okay. And would that be the same thing in
17 124B, there's an indication that the controller 223B
18 has an input and an output port?

19 A. Yes.

20 Q. Okay. And both memory controllers 123A and
21 123B are capable of sending signals to the chain of
22 memory devices; is that right?

23 A. They are.

24 Q. And these memory controllers 123A and 123B
25 actually send their signals via separate signaling

1 cues; is that correct?

2 A. They do.

3 Q. In embodiment of Grundy's Figure 4A, would
4 each memory controller, meaning both 123A and 123B,
5 transmit a clock signal to the first memory device
6 in the chain?

7 A. They would.

8 Q. And in the Grundy Figure 4A embodiment,
9 would each memory controller send commands to the
10 first memory device in the chain?

11 A. They could do that.

12 Q. Okay. What happens in Grundy's Figure 4A
13 embodiment if both memory controllers command that
14 first device in the chain to write to the same
15 location in memory at the same time?

16 A. Yeah, that cannot work, actually.
17 Generally that would not be allowed. So, you know,
18 and the process -- overall processor handling this
19 would have to make sure, as it could routinely do,
20 make sure not to give two writes to the same
21 location at the same time.

22 Q. Okay. So, it would be fair to say that how
23 that is handled might depend on how a processor
24 outside of Figure 4A is configured?

25 A. Yes.

1 Q. In particular, the order in which those
2 requests are carried out might depend on something
3 outside of Figure 4A?

4 A. Well, in particular, you have to make sure
5 that, yeah, you're not writing to the same location
6 in particular, and you wouldn't really -- probably
7 wouldn't want to read the same location either. But
8 that's a little -- that's an implementation detail,
9 but certainly you wouldn't want to write to the same
10 location.

11 Q. Okay. So, I guess, similarly, what would
12 happen if controller 124A asks to write to a
13 location, and before that request is carried out,
14 controller 124B asks to read from that same
15 location?

16 A. It would certainly -- what could be done in
17 an implementation is that would be one use of the
18 status register, would be to check the status of
19 that memory to see that the write has completed
20 before, and it will stall the read until that write
21 is complete as determined by the status register.

22 Q. Okay. So at least in one implementation of
23 Figure 4A, the status register could be used to, I
24 guess, delay a response to the read request until
25 the write request is complete?

1 A. That's correct.

2 Q. And you say this is one way of handling
3 that situation. Could there be other ways of
4 handling that situation consistent with Figure 4A?

5 A. That would probably be the -- that may be
6 the fastest way or best way to deal with it.
7 Because if you, you know, delay completely issuing
8 requests to the same location like that, it might be
9 a much longer delay, rather than just waiting for
10 the status light to switch, which might be a
11 fraction of a clock cycle.

12 Q. Okay. If we could just dig into this a
13 little further. Suppose we are in that kind of
14 situation and controller 124B asks to read from a
15 location, and what it's learning is that that
16 location is busy.

17 I guess my question is, is there a
18 circumstance in which controller 124B might no
19 longer wish to read from that location once the
20 memory device is ready again?

21 A. I can't think of one right now.

22 Q. I'm imagining a situation in which the two
23 controllers maybe are on different devices and they
24 are not in dialogue with one another, and controller
25 123B expects a certain data to be there, and when it

1 goes to read it and it sees that the device is busy,
2 in particular busy due to a write request, it might
3 learn from that that the data it's seeking to read
4 there is not going to be there anymore.

5 A. No. The addresses that the processor are
6 using are distinct from where it's stored in that
7 device. And so if the processor wants to read that
8 specific location, that means it really does. And
9 it -- and the processor, you know, the computer
10 program, whatever, that's writing the data and then
11 subsequently reading it, probably indeed did want to
12 read it right after the update.

13 Q. Okay.

14 A. I can't think of a reason where you would
15 want to terminate a read because it was just
16 written. I cannot think of a case like that
17 offhand.

18 Q. Okay. Grundy's Figure 4A doesn't depict
19 the two memory controllers 123A and 123B
20 communicating with each other, does it?

21 A. Well, it doesn't prohibit that possibility
22 either, but it does not specifically show that.
23 They certainly would both be communicating with one
24 or more processors.

25 Q. As you read Figure 4A, do you understand

1 that both memory controller 123A and 123B would
2 necessarily be in communication with the same one or
3 more processors?

4 A. They could be, and we are really getting
5 into computer architecture details here --

6 Q. Yeah.

7 A. -- but --

8 Q. Could there be embodiments of Grundy's
9 Figure 4A in which memory controller 123A is in
10 communication with one set of processors and memory
11 controller 123B is in communication with a different
12 set of processors?

13 A. That's possible. I cannot say it's not,
14 so --

15 Q. Okay. If we could, maybe let's turn to
16 page 83 of your declaration, paragraph 115.

17 A. Okay.

18 Q. Are you there?

19 A. Yes.

20 Q. Okay. So here we have discussion again
21 from Grundy about memory devices that may include
22 delay-locked loops.

23 A. Yes.

24 Q. What is a delay-locked loop?

25 A. This is where you want to create a delay in

1 circuitry that matches a particular clock period or
2 matches -- yeah, or at least matches a certain
3 signal duration.

4 So, say you want a delay that is equal to
5 one nanosecond. A delay-locked loop will give you
6 circuitry that has exactly or nearly exactly that
7 delay.

8 Q. Okay. So delay-locked loop is a form of
9 circuitry; is that right?

10 A. Yes.

11 Q. So in this quote, this first part here,
12 Grundy begins, "Referring again to Figure 5A, it
13 should be noted that different clocking schemes may
14 be used to control the propagation of signals
15 through the signaling queue in alternative
16 embodiments. For example, rather than having each
17 memory device issue a clock signal to its downstream
18 neighbor, a clock signal may be supplied from a
19 single source to all memory devices in the memory
20 system and/or to the memory controller."

21 This second sentence here, this memory
22 device that issues a clock signal to its
23 downstream -- instead of having a memory device
24 issue its clock signal to its downstream neighbor,
25 you have a clock signal supplied from a single

1 source to all memory devices, that second kind of
2 embodiment is a different embodiment than the
3 Figure 5A embodiment of Grundy, right?

4 A. Yeah, it is.

5 Q. So then the paragraph continues, "The
6 memory devices may include delay-locked loops,
7 phase-locked loops, or other clock-phase adjustment
8 circuitry to adjust the phase of the clock signals
9 as necessary to sample incoming signals at a desired
10 sampling instant."

11 Now, when Grundy says "the memory devices"
12 here, he's referring to the memory devices of his
13 previous sentence; is that right?

14 A. Well, it's the chain of memory devices in
15 Figure 5A, for example.

16 Q. Oh, okay. So to be clear, he's saying here
17 that -- this teaching about the use of delay-locked
18 loops is for embodiments of Figure 5A and not just
19 the last example of the embodiments that he was
20 talking about?

21 A. Well, no. It's Figure 5A but modified with
22 the concept that you could have a single clock
23 source, but you still have to delay the clock from
24 one device to the next.

25 And so you could -- you know, in fact, it

1 says -- see at the bottom? -- "adjust the phase of
2 the clock signals as necessary to sample incoming
3 signals at a desired sampling instant."

4 So you do need -- even though there's one
5 clock source, you still have to delay it evermore as
6 you go down the chain so that it does sample at the
7 desired instant. And you can insert such a precise
8 delay using a delay-locked loop, for example.

9 Q. Okay. But is Grundy saying that you do
10 that in Figure 5A or that you do that in these other
11 embodiments?

12 A. Well, it's the modification of 5A where you
13 are -- you have one clock source.

14 Q. Where there's a single clock source to --
15 going out to all the memory devices?

16 A. Yeah. Basically, yeah.

17 Q. Okay. Would an implementation of Grundy's
18 Figure 5A that, I guess, literally follows what's
19 depicted in Figure 5A where each device in the chain
20 is the source of a clock for the next device, would
21 an implementation like that contain delay-locked
22 loops?

23 A. It could. I mean, this is just one
24 embodiment. The point is that, you know, it teaches
25 a POSITA that the delay-locked loop or a

1 phase-locked loop can be used to adjust clock signal
2 phases as necessary, so --

3 Q. Okay. In an embodiment of Figure 5A, like
4 literally depicted in Figure 5A where the clock
5 signal propagates from one device to the next,
6 rather than being sent from a single source, what
7 would be the purpose of using delay-locked loops in
8 an embodiment like that?

9 A. In the original embodiment?

10 Q. Yes.

11 A. Well, let's see. You could -- let's see.
12 What figure is this?

13 Yeah. Like, for example, in Figure 6, you
14 see that there's a delay TP that, basically, you
15 want from the output of the memory controller to the
16 output of the first device. You could create a
17 delay that is -- with a DLL that equals TP, and then
18 the nice thing is -- and then just implement it like
19 that.

20 And then if there are any process
21 variations or temperature variations, that delay
22 that's set up by the DLL will actually flex with the
23 process variation. So it has that nice feature. So
24 that's sometimes something someone would want to
25 use.

1 Q. Do you agree that an embodiment of Grundy's
2 Figure 5A would not have to include delay-locked
3 loops?

4 A. It wouldn't have to, but it's certainly one
5 thing that is in the toolbox for a POSITA in
6 designing a flash memory of the Grundy and Kilbuck
7 type.

8 Q. So we were just talking about with
9 reference to Figure 6. Can you tell from looking at
10 Figure 6 whether it's depicting the timing of an
11 embodiment of Figure 5A that uses delay-locked
12 loops?

13 A. You can't tell from the figure necessarily,
14 but certainly a POSITA would understand that you
15 could use a delay-locked loop to effect that.

16 Q. So you are saying that this picture is
17 consistent with an embodiment of Figure A that uses
18 delay-locked loops?

19 A. Or certainly compatible with, yes.

20 Q. And it's also compatible with an embodiment
21 that doesn't use delay-locked loops?

22 A. Yeah. It's a question of which way, you
23 know, based on cost and so forth, other parameters
24 that a POSITA would worry about, as to which way you
25 want to go.

1 Q. Okay. So as long as we are in Grundy,
2 let's go back to Figure 17.

3 A. Okay.

4 Q. So, does Grundy's Figure 17 memory device
5 include delay-locked loops?

6 A. It does not illustrate that in this figure.

7 Q. If you were to -- could you conceive of
8 adding delay-locked loops to an embodiment like
9 Figure 17?

10 A. Well, you know, for example, the jitter
11 control adjusts -- well, that's adjusting the period
12 of a clock to make it, you know, presumably more
13 50/50, in other words, 50 percent of the time high,
14 50 percent of the time low. And so it's in that --
15 between 310 and 320 is where you would apply a DLL
16 if you were going to do -- use that.

17 Q. Okay. So that's down at the bottom in that
18 sort of line that includes jitter control?

19 A. Yes.

20 Q. Okay. And we agree that this device in
21 Figure 17 would not necessarily have to include a
22 delay-locked loop; is that right?

23 A. Not necessarily. But it's a design choice
24 that one could make.

25 Q. Okay. I have no further questions.

1 A. Okay.

2 MR. STEPHENS: Can we take 15 minutes?

3 MR. COURTNEY: Sure.

4 MR. STEPHENS: Why don't we just come back
5 at the top of the hour. Does that sound good?

6 MR. COURTNEY: Sounds good.

7 THE WITNESS: Yeah. And I will sign off
8 because I need to use the facilities. I will come
9 back on at 1:00, then, Central?

10 MR. COURTNEY: Yep.

11 MR. STEPHENS: Correct. 1:00 Central,
12 11:00 Pacific.

13 THE WITNESS: All right.

14 (Recess taken from 10:40 a.m. to
15 11:00 a.m.)

16 MR. STEPHENS: I'm ready to go back on.
17 Are we back on the record now?

18 THE REPORTER: Yes.

19 MR. STEPHENS: We have no questions for the
20 witness.

21 MR. COURTNEY: Okay.

22 MR. STEPHENS: Off the record.

23 THE REPORTER: I need copy orders on the
24 record.

25 MR. STEPHENS: We will do a standard

1 delivery, and a rough, please.

2 MR. COURTNEY: And same for us.

3 (The proceedings concluded at 11:00 a.m.)

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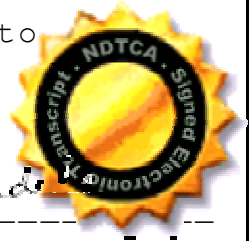
I further certify that I am not of counsel or attorney for any of the parties hereto or in any way interested in the event of this cause and that I am not related to any of the parties thereto

Dated: May 4, 2026

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