

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____)
INFINEON TECHNOLOGIES AMERICAS
CORP.,

Petitioner,

v.

Case No.

IPR2025-01487

Patent 9,972,381

MOSAID TECHNOLOGIES INC.,

Patent Owner.

_____)

DEPOSITION OF
DR. STEVEN PRZYBYLSKI, PH.D.

Friday, August 7, 2026

10:00 a.m.

Eastern Daylight Time

Reported by: Lori J. Goodin, RPR, CRR, RSA,
California CSR #13959

Job No. 00191084

1 REMOTE DEPOSITION OF
2 DR. STEVEN PRZYBYLSKI, PH.D.,
3 Witness in the above-titled action, held on
4 Friday, August 7, 2026, commencing at
5 approximately 10:00 a.m. before Lori J. Goodin,
6 RPR, CRR, RSA, California CSR #13959, Registered
7 Professional Reporter, Certified Realtime
8 Reporter, Realtime Systems Administrator, and
9 Certified Shorthand Reporter, and Notary Public
10 of the State of Florida, State of California and
11 the District of Columbia.

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8 WITNESS: DR. STEVEN PRZYBYLSKI, PhD

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3

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Lori J. Goodin, RPR, CRR, RSA

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California CSR #13959

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PREVIOUSLY MARKED EXHIBITS

6

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EXHIBIT

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Exhibit 1001

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Exhibit 1005

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Exhibit 1006

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Exhibit 2027

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16 (REPORTER'S NOTE: All quotations from exhibits
17 are reflected in the manner in which they were
18 read into the record and do not necessarily
19 denote an exact quote from the document.)

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21

22

1 FRIDAY, AUGUST 7, 2026, 10:03 A.M.

2 PROCEEDINGS

3

4 THE REPORTER: Unless an objection
5 is heard at this time, all parties to this
6 deposition are appearing remotely and have
7 agreed to the witness being sworn in
8 remotely.

9 Doctor, will you please raise your
10 right hand.

11

12 Whereupon,

13 DR. STEVEN PRZYBYLSKI, Ph.D.,
14 a witness called for examination, having been
15 first duly sworn, was examined and testified as
16 follows:

17 THE REPORTER: You may proceed.

18

19 * * *

20 (Whereupon, previously marked
21 Exhibit 1001,
22 first referral.)

1 (Whereupon, previously marked
2 Exhibit 1005,
3 first referral.)

4 (Whereupon, previously marked
5 Exhibit 1006,
6 first referral.)

7 (Whereupon, previously marked
8 Exhibit 2027,
9 first referral.)

10

11 EXAMINATION

12

13 BY MR. STEPHENS:

14 Q. Good morning, Dr. Przybylski.

15 A. Good morning.

16 Q. My name is Nick. I am an attorney
17 with Fish & Richardson, and I will be taking the
18 deposition today on behalf of the petitioner in
19 this IPR, Infineon Technologies Americas
20 Corporation.

21 Do you understand?

22 A. Yes, I do.

1 Q. And I am here with my colleagues,
2 John-Paul Fryckman and Brandon Avers, also on
3 behalf of Infineon, okay?

4 A. Okay.

5 MR. STEPHENS: Would Counsel for
6 patent owner like to state his appearance?

7 MR. COURTNEY: Sure. This is Dennis
8 Courtney of Lowenstein & Weatherwax for the
9 patent owner and the witness.

10 BY MR. STEPHENS:

11 Q. Dr. Przybylski, we are here today
12 regarding the IPR proceeding in IPR 2025-01487
13 involving the '381 patent.

14 Do you understand?

15 A. I do.

16 Q. This deposition is being transcribed
17 by the court reporter, do you understand?

18 A. Yes.

19 Q. And, to ensure a clean record, I
20 will aim not to interrupt you during your
21 answers. I, likewise, just request that you give
22 me a chance to speak my question so that we are

1 not speaking over each other and we can ensure a
2 clean record that way.

3 Does that sound good?

4 A. I understand.

5 Q. I will aim to take a break every
6 hour or so. But, it -- of course, at any time if
7 you ever would like to take a break, please feel
8 free to let me know and we will try to work in a
9 moment to take a break.

10 A. Certainly.

11 Q. Can you please state your full name?

12 A. Steven Alan Przybylski.

13 Q. And what is your city of residence?

14 A. Ann Arbor, Michigan.

15 Q. Do you understand that you are under
16 oath for the deposition today?

17 A. Yes, I was sworn in.

18 Q. Is there any reason that you cannot
19 give truthful and accurate testimony?

20 A. No.

21 Q. For the record, I will just define
22 several terms that I will use throughout the

1 deposition.

2 So, when I use the terms patent
3 owner or MOSAID, I am referring to MOSAID
4 Technologies, Incorporated.

5 Do you understand?

6 A. The proper way to say it is MOSAID.

7 Q. MOSAID. I'm sorry. Yes.

8 And when I use the term petitioner
9 or Infineon, I am referring to the petitioner,
10 Infineon Technologies Americas Corporation?

11 A. I understand.

12 Q. And I will be referring to the '381
13 patent today. That is shorthand for the patent
14 that is challenged in this IPR, U.S. Patent
15 Number 9,972,381, which has been marked as
16 Exhibit 1001.

17 Do you understand?

18 A. I do.

19 Q. And do you have an electronic
20 version of Exhibit 1001, correct?

21 A. Yes, I have downloaded it from the
22 Chat.

1 Q. You have no other copies of the '381
2 patent or other materials before you, correct?

3 A. That is correct, no.

4 Q. I may also refer to your
5 declaration.

6 And your declaration was submitted
7 as Exhibit 2027 in this proceeding.

8 Do you understand?

9 A. Yes, that is accurate.

10 Q. And you also have an electronic
11 version of the declaration, correct?

12 A. I have downloaded it, the electronic
13 version from the Chat.

14 Q. I may also refer to some prior art
15 at issue in the proceeding.

16 One is the Grundy reference, which
17 is U.S. Pub 2004/0148482 marked as Exhibit 1005.

18 Do you understand?

19 A. Yes. 1005, correct.

20 Q. I may refer to the Kilbuck
21 reference, which is U.S. Pub 2005/0204091 marked
22 as Exhibit 1006 in this proceeding.

1 Do you understand?

2 A. Yes, 1006. That is correct.

3 Q. And I'm going to use the term
4 POSITA, which is an acronym for Person of
5 Ordinary Skill in the Art.

6 Will you understand what I am
7 referring to when I use the term POSITA?

8 A. Yes.

9 Q. Can you describe how you prepared
10 for the deposition today?

11 A. I have read the -- my declaration a
12 couple of times and I have reviewed the documents
13 that you have downloaded. My previous copies of
14 them before, I removed them from my computer.

15 I also met with counsel.

16 Q. Approximately how much time would
17 you say that you spent preparing for the
18 deposition?

19 A. I started last Friday. I did not
20 get much done over the weekend.

21 So I would say about 15 hours, plus
22 or minus. Probably plus -- yeah, how about that.

1 Q. Did you review any documents in
2 preparation for the deposition?

3 A. As I just noted, I reviewed the
4 declaration, the '381, Kilbuck, Grundy, and some
5 of the other references that are in the record
6 but not in any detail.

7 Q. Can you describe the process by
8 which you prepared your declaration in this
9 proceeding?

10 A. My declaration was prepared a number
11 of months ago, prior to the deadline for its
12 submission.

13 I reviewed the petition and
14 Dr. Sechen's declaration. I developed arguments
15 that I thought would be relevant to rebutting the
16 -- those two documents. I discussed them with
17 counsel, prepared a first draft of those
18 arguments, and then thereafter, worked with
19 counsel to refine the declaration and make it
20 consistent with the needs of the client.

21 Q. Did you personally prepare that
22 first draft for the declaration?

1 A. Yes, I did.

2 Q. Are you aware that MOSAID submitted
3 a declaration from another witness, Dr. Sunil
4 Khatri earlier in the proceeding?

5 A. I am aware of that. I was brought
6 in at the POR stage, not the POPR stage.

7 So, yes, I am aware that that is
8 prior history to my involvement in the case.

9 Q. Are you familiar with Dr. Khatri's
10 declaration?

11 A. No, I have not looked at it.

12 Q. You have not reviewed it in the
13 course of preparing your declaration?

14 A. No, I have not.

15 Q. And to this day, you have not
16 reviewed Dr. Khatri's declaration?

17 A. No. I know it is in the record. I
18 have seen it there, but I have not reviewed it.

19 Q. Have you ever had any discussions
20 with Dr. Khatri?

21 A. No, I never met the man.

22 Q. Are you aware of any errors in your

1 declaration?

2 A. Errors, no.

3 Q. Do you stand by the analysis in your
4 declaration?

5 A. Yes, I do.

6 Q. Is this your first time being
7 deposed, Dr. Przybylski?

8 A. No, it is not.

9 Q. Approximately how many times would
10 you say you have been deposed in your career?

11 A. About 30.

12 Q. Of those 30, how many would you say
13 relate to patent cases?

14 A. All of them.

15 Q. Are they, and I -- among those 30,
16 how many would you estimate pertain to IPR
17 proceedings?

18 A. Probably more than half, yeah. So,
19 I would have to review document -- my case
20 history.

21 But, more than half.

22 Q. And the ones that were not IPR

1 proceedings, what were the nature of those
2 disputes?

3 A. ITC cases and District Court cases.
4 Oh, and there is also trade secret was also
5 District Court.

6 So, yeah, those are the three types
7 of venues are the standard ones.

8 Q. The prior IPR proceedings in which
9 you have been involved, have they involved other
10 patent owner, work on behalf of other patent
11 owners?

12 A. Yes.

13 Q. Have you been an expert in
14 proceedings in -- on behalf of petitioners?

15 A. On behalf of petitioners, I have
16 been retained on behalf of petitioners. I do not
17 recall whether there have been any depositions on
18 behalf of petitioners.

19 Q. So, it is fair to say that a
20 majority of your IPR work has involved work in
21 which you have been retained on behalf of patent
22 owners?

1 A. The majority - yes, I would say the
2 majority has been on the -- on behalf of patent
3 owners.

4 Q. And have you been retained by MOSAID
5 in any other IPR proceedings?

6 A. No. I believe this is the first IPR
7 proceeding for MOSAID.

8 Q. The other IPR proceedings in which
9 you have been involved, have many of them
10 involved memory, digital memory technologies?

11 A. Yes. Quite a few. It is my bread
12 and butter.

13 Q. Is your compensation for your work
14 on this case in any way contingent on the outcome
15 of the proceeding?

16 A. No.

17 Q. Are you aware that MOSAID at one
18 point had renamed their business to Conversant
19 Intellectual Property Management?

20 A. Yes.

21 Q. And they have since reverted to the
22 MOSAID name?

1 A. Yes. Their own -- ownership
2 structure has changed a number of times over the
3 years.

4 Q. I will ask some questions about your
5 relationship with MOSAID, but in doing so,
6 depending on the time frame, but please
7 understand that it may be -- I may be referring
8 to either MOSAID or Conversant, depending on when
9 the events occurred.

10 A. I understand.

11 Q. How long have you had a professional
12 relationship with MOSAID?

13 MR. COURTNEY: Objection to the
14 form.

15 THE WITNESS: I certainly had a
16 professional relationship with the
17 individuals who have been employed with
18 MOSAID all of the way back to the early
19 1990s.

20 With the company itself, I believe
21 the first retention was in the late 1990s.

22 BY MR. STEPHENS:

1 Q. Who are the individuals with which
2 you had a professional relationship?

3 A. I had a relationship with one of the
4 original founders of MOSAID, a Dick Foss, who has
5 since deceased.

6 I have also had professional
7 relationships with Peter Gillingham who was
8 there, a long time employee of MOSAID and
9 Conversant. So, I don't know if he -- if he
10 worked at Conversant. But, certainly for MOSAID.

11 And then a number of the other
12 technical contributors to MOSAID in the period,
13 in the early days, in 1990s.

14 Q. What was the name of the founder?

15 A. Dick Foss, F-O-S-S.

16 Q. And, can you describe the nature of
17 your relationship with Dick Foss?

18 A. Casual professional relationship.
19 We knew each other. We would say hi at
20 conferences, that sort of thing.

21 Q. Have you ever collaborated with him
22 on any work?

1 MR. COURTNEY: Objection to the
2 form.

3 THE WITNESS: He was more or less
4 retired by the time of my first engagement
5 with MOSAID.

6 So, I would not say I had any
7 professional collaboration with Dick.

8 BY MR. STEPHENS:

9 Q. And how, to your recollection, how
10 did you come to know Dick?

11 A. Let's see. How did I come to know
12 Dick?

13 I think it was, MOSAID was founded
14 and was based in Ottawa, which is my -- Ottawa,
15 Canada, which is my home town. So, I was aware
16 of MOSAID from that respect. And then, you know,
17 I met Dick at some conference and, you know,
18 stuck -- struck up a conversation with regard to,
19 you know, technology industries, technology
20 companies in Ottawa, and, you know, what is that
21 like and so forth.

22 Q. And you mentioned a Peter

1 Gillingham.

2 A. Yes.

3 Q. How did you know Peter?

4 A. Similar relationship. Met at
5 conferences first. And then, yeah, the -- it was
6 a casual professional relationship for a while,
7 before I was retained by MOSAID and before some
8 MOSAID employees, including Peter, attended some
9 of my seminars.

10 Q. When did you first meet -- excuse
11 me.

12 When did you first meet Peter?

13 A. I don't remember exactly. It would
14 have been in the mid-1990s, I imagine. He was
15 involved as MOSAID's representative at JEDEC and
16 that was an aspect that I was very interested in.
17 And so, if I had conversations with him about
18 that, at least in the mid-1990s.

19 Q. And what was your understanding of
20 Peter's role at MOSAID?

21 A. It changed substantially over the
22 time. He's -- initially, he was a technical lead

1 and then he ended up as vice president of
2 something or other before he left the company.

3 Q. Do you recall about the time frame
4 that he left the company?

5 A. It had to do with the transition
6 from MOSAID to Conversant. The structure of the
7 company changed and I don't know the details of
8 his departure.

9 Q. You mentioned that you were retained
10 by MOSAID at some point in the time frame of your
11 relationship with Peter.

12 What was the nature of your
13 retention?

14 MR. COURTNEY: Objection to the
15 form.

16 THE WITNESS: There were several
17 phases to that relationship, that -- with the
18 company.

19 Initially, I was retained at the
20 level of the president of the company to help
21 them identify market opportunities related to
22 their embedded DRAM technology. They were

1 trying to transition from being a purely a
2 design house to being something more than
3 that.

4 So, that was -- that was the first
5 retention. And then subsequently, I was
6 recruited to be part of their technical
7 advisory board, which I was -- and that was
8 in the 2000s. I was associated with, or I was
9 a member of, the technical advisory board for
10 probably about seven years or so. And then
11 that relationship spun off to being a
12 contributor to their HLNAND architecture, and
13 in parallel with the technical advisory
14 board. And then ultimately, I don't remember
15 exactly when they transitioned to the
16 Conversant ownership structure. But, my --
17 the -- my involvement ended prior to that.

18 BY MR. STEPHENS:

19 Q. Would that be around the mid-2010s?

20 A. No. My recollection is that I, the
21 technical advisory was -- board was disbanded
22 before 2010.

1 But, I don't remember exactly when.

2 Q. And you mentioned that your initial
3 retention was, in what capacity again?

4 A. It was a consultant to the company,
5 principally the president of the company was the
6 person who was setting the direction of my
7 consulting. And it was to evaluate market
8 opportunities for their embedded DRAM
9 technologies.

10 Q. Do you recall the name of the
11 president at the time?

12 A. Oh, dear. I should. But, I'm
13 sorry, I do not.

14 Q. That is okay. And about how long
15 did that role last for you?

16 A. That was a relatively short
17 consulting role of probably less than six months.

18 Q. And you were a member of the
19 technical advisory board in the 2000s, correct?

20 A. Yes, that is what I said.

21 Q. And can you just describe again what
22 your role was on the technical advisory board?

1 A. We would meet once or twice a year.
2 And the board was made up of external experts.
3 Three was the typical number, although sometimes
4 there was a fourth that came and went.

5 And, the MOSAID staff presented to
6 us what they were doing, what their recent
7 milestones were, what their plans were for
8 various projects and, you know, we commented on
9 them.

10 Q. My apologies. You may have
11 mentioned other roles.

12 But, were there other, apart from
13 your consulting work on behalf of the president
14 and then working for the -- on the technical
15 advisory board, were there other aspects to your
16 relationship with MOSAID?

17 A. Yes, the --

18 MR. COURTNEY: Objection to the
19 form. Sorry.

20 THE WITNESS: The final engagement
21 was two aspects of it.

22 One was to help them develop a

1 architecture and device called HLNAND, so,
2 H-L-N-A-N-D, for the reporter.

3 And, that was a novel flash memory
4 architecture and systems architecture that
5 they developed and tried to propagate into
6 the industry, ultimately unsuccessfully.

7 And so, I was a contributor to the
8 development of that architecture, since
9 memory systems and memory device architecture
10 is one of my core competencies.

11 So, I was working with them for a
12 couple of years during, as a consultant
13 towards that project.

14

15 BY MR. STEPHENS:

16 Q. And again what time frame would that
17 have been?

18 A. That would have been the middle
19 2000s. And then ultimately, I helped develop some
20 patent applications related to the work that we
21 did on HLNAND.

22 Q. I think you mentioned there were two

1 aspects. The one might have been with respect to
2 HLNAND?

3 A. Yes.

4 Q. Was there another aspect?

5 A. The patent work. Developing patent
6 applications related to the HLNAND work.

7 Q. What was your role in developing the
8 patent applications?

9 A. For the patents on which I was a
10 principal or a sole inventor, I drafted the
11 patent, the specification and initial claims, and
12 then handed it off to a patent attorney.

13 Q. And, you are a registered patent
14 agent, correct?

15 A. I am, yes.

16 Q. Okay.

17 A. I haven't checked recently, but last
18 time I did, I was in good standing.

19 Q. When did you become a registered
20 patent agent?

21 A. 1997 is my recollection.

22 Q. Did you ever file applications on

1 behalf of MOSAID?

2 A. No, I have never used my patent
3 agent number. I have always, whenever it -- in a
4 prosecution, a patent prosecution role, there was
5 always a patent attorney that was the attorney of
6 record for the application.

7 Q. Have you used your patent
8 registration number or patent agent status for
9 other clients, but not MOSAID?

10 A. Yes. So, I have used my skills as
11 relating to patent prosecution and patent
12 development for other clients, not just MOSAID.
13 I think that is a clear way to state the answer
14 to your question.

15 Q. Thank you. Yes. I understand. But
16 for MOSAID, you have been either a sole inventor
17 or coinventor on a number of applications filed
18 by MOSAID, correct?

19 A. Yes. And I think the number is two.
20 May -- it might be more than that. I have to
21 check the, my records on that. But, it is -- it
22 was one that I was sole inventor on and then

1 there were at least one possibly two in which I
2 was co-inventor with some of the technical staff
3 at MOSAID.

4 Q. Are those patents listed on your CV
5 in the declaration?

6 A. The ones that reached, that were
7 issued, yes. They were -- there is none on --
8 that have not been issued that are not on my CV.

9 Q. I am looking at your CV right now on
10 Page 75 of the declaration where there is a
11 listing of patents in which you are a named
12 inventor.

13 A. I am looking at a clean hard copy of
14 my declaration. Just so you know.

15 Q. Okay. Yeah.

16 A. Okay. Seminars, patents, yes.

17 Q. And the first patent listed is U.S.
18 Patent Number 8,984,249.

19 A. Yes.

20 Q. Do you see that?

21 A. I do.

22 Q. And you are listed as one of -- it

1 appears, four co-inventors?

2 A. Yes, that is correct.

3 Q. Who are the other co-inventors?

4 A. Those are, as I indicated, were
5 members of technical staff at MOSAID.

6 Q. Do you recall your work with them?

7 A. This was related to the HLNAND
8 architecture that I have been talking about
9 recently.

10 Q. Likewise, the third entry in your
11 listing of patents, the '768 patent,
12 U.S. 8,812,768, do you see that one?

13 A. I do.

14 Q. And, I believe this has the same set
15 of inventors.

16 Is this also related to the HLNAND
17 work?

18 A. It is not the identical set. There
19 are two inventors in common between those
20 patents, in addition to myself.

21 But, they are not identical. And
22 so, the answer to your question is yes, it is

1 relating to the work done on the HLNAND
2 architecture.

3 Q. The fifth entry for U.S. 8,671,252,
4 I believe that also has overlapping inventors
5 with the first and, with the '249 and '768
6 patents.

7 Is that also related to HLNAND?

8 A. Yes, in that case, that one is the
9 identical inventorship to the first patent. And
10 it came out of the development of the HLNAND
11 architecture.

12 Q. To the best of your recollection,
13 could you identify for each of the patents listed
14 here, which ones pertain to your work with
15 MOSAID?

16 A. No. I refreshed my memory on this
17 subject matter. The, 1, 2, 3 -- first 8 patents
18 are owned by MOSAID and came out, one way or
19 another, from the work at the technical advisory
20 board or in conjunction with my work on HLNAND.

21 Q. Did you collaborate closely with the
22 technical staff on these applications for which

1 you are a co-inventor?

2 A. Well, I certainly collaborated with
3 the members of technical staff on the HLNAND work
4 to the extent that our joint work yielded a
5 patent application with multiple inventors, of
6 which I was one. It came out of that
7 collaboration.

8 Q. Are you aware that -- strike that
9 question.

10 Who is H. Oh?

11 A. Mr. Oh, I have forgotten his first
12 name. He was just one of the technical staff at
13 MOSAID.

14 Q. And had same for H-P-Y-E-O-N. I may
15 be mispronouncing that, P-Y-E-O-N?

16 A. Yes, same answer.

17 Q. And the same for Mr. Kim?

18 A. Same answer.

19 Q. Are you aware that Mr. Oh, Mr. Kim,
20 and Mr. Pyeon are all co-inventors on the '381
21 patent?

22 A. I can check if you want me to but I

1 am aware that there is at least some overlap.

2 Q. Have you ever had any communications
3 with Mr. Pyeon, Mr. Oh, or Mr. Kim regarding the
4 subject matter of the '301 patent?

5 MR. COURTNEY: Objection to the
6 form.

7 THE WITNESS: I have had no contact
8 with any of those individuals since my last
9 engagement with MOSAID in the late 2000s,
10 mid-to late 2000s.

11 BY MR. STEPHENS:

12 Q. You have had no contact with them in
13 connection with your retention for this
14 proceeding, correct?

15 A. That -- I have had no contact in any
16 capacity with those individuals.

17 Q. Did you receive any compensation
18 from MOSAID in connection with the patents that
19 have issued for which you are a co-inventor?

20 MR. COURTNEY: Objection to the
21 form.

22 THE WITNESS: Certainly the patent

1 applications that I developed, wrote the
2 first drafts of, et cetera, or that worked on
3 revising applications that would have come
4 under my hourly retention with MOSAID.

5 I am -- they did have a patent
6 compensation plan in the early days. I do
7 not recall if I received any compensation as
8 a result of the filing or issuance of any of
9 these patents. That would have been small,
10 regardless.

11 BY MR. STEPHENS:

12 Q. Would, primarily, your compensation
13 for the work related to the subject matter of
14 these patents have been under your contract for
15 work on the technical advisory board?

16 A. There -- my recollection is that
17 there was a separate re -- relationship and
18 engagement for the HLNAND work that was
19 compensated differently than the technical
20 advisory board work.

21 But, this was 20 years ago now and
22 I, my recollection of the details of those

1 arrangements is fading.

2 Q. Do you currently receive any
3 compensation from MOSAID apart from your
4 retention for this IPR?

5 A. No. My relationship with MOSAID
6 currently is strictly through the Lowenstein
7 legal group for work on this IPR.

8 Q. I would like to look at Paragraph 20
9 of your declaration.

10 A. Yes, I am there.

11 Q. And this paragraph pertains to the
12 definition of a person of ordinary skill in the
13 art for the '381 patent, correct?

14 A. Yes. That is what it relates to.

15 Q. In this paragraph, you have quoted
16 from Dr. Sechen's declaration, regarding
17 Dr. Sechen's opinions of a person of ordinary
18 skill in the art, correct?

19 A. Yes, also citing to the petition.

20 Q. Yes, thank you.

21 And you have noted in Paragraph 21
22 that for purposes of this declaration, I accept

1 Dr. Sechen's proposed qualifications of a POSITA,
2 correct?

3 A. Those are my words in Paragraph 21,
4 yes.

5 Q. Do you agree with Dr. Sechen's
6 definition?

7 A. I haven't formed an opinion as to
8 what, whether a alternate definition would have
9 been better or more appropriate for this subject
10 matter.

11 For the purposes of this
12 declaration, I accept his definition as adequate.

13 Q. And Paragraph 22 you note that my
14 opinions as stated in this declaration are valid,
15 even if the board adopts a somewhat higher or
16 somewhat lower level of ordinary skill in the art
17 than proposed, correct?

18 A. Let me review. Yes. That is a --
19 that is the content of the first paragraph of
20 para -- first sentence of Paragraph 22. I go on
21 to elaborate somewhat, what I mean by that. But,
22 in essence, yes.

1 Q. Is it correct then that your
2 opinions would not meaningfully change -- well,
3 strike that question.

4 I would like to turn to the '381
5 patent.

6 A. Let me open it. Okay. I have that
7 open in front of me.

8 Q. The '381 patent relates to memory
9 devices, correct?

10 A. Memory devices and by association,
11 memory systems involving those memory devices,
12 yes.

13 Q. Have you read have -- you reviewed
14 the '381 patent?

15 A. Not in excruciating detail. Only to
16 the extent necessary to form my opinion related
17 to the petition and Dr. Sechen's declaration.

18 Q. Are there portions of the '381
19 patent that you have not reviewed?

20 A. There are certainly portions of it
21 that I have not reviewed in tremendous detail. I
22 have reviewed all of it in -- to some degree of

1 detail.

2 Q. Are you familiar with clock signals,
3 Dr. Przybylski?

4 A. Generally speaking, yes.

5 Q. Do the memory systems in the '381
6 patent utilize clock signals?

7 A. Yes. There are clock signals in at
8 least some of the embodiments of the '381.

9 Q. What is a clock signal?

10 MR. COURTNEY: Objection to the
11 form.

12 THE WITNESS: As with most patents,
13 the '381 uses clock signal without actually
14 defining it first because it is a term that
15 is widely used in the field of digital
16 electronics.

17 The exact definition of it, I think,
18 would be a matter of personal, some personal
19 variation from practitioner to practitioner,
20 and what would be a clock signal and not
21 might have differences around the edges of
22 the scope of the term.

1 In general, it is a, an alternating
2 signal of, generally, regular frequency and
3 period that is used to control the operation
4 of a digital circuit.

5 That is off the top of my head, not
6 something that I have put a lot of thought
7 into.

8 BY MR. STEPHENS:

9 Q. How about an alternating signal,
10 there would be transitions from a low signal to a
11 high signal in the clock signal, correct?

12 MR. COURTNEY: Objection to the
13 form.

14 THE WITNESS: Yes. Most of the time
15 the clock signal is alternating between a
16 high value and a low value that engages or
17 disengages the circuitry that it is seeking
18 to control.

19 We can see this in Figure 14 of
20 the '381 where there is an S clock signal
21 which is referred to as a clock signal in the
22 text and it is, for the portions of the time

1 when there is activity, it is alternating
2 between a low and a high, with transitions
3 between them.

4 BY MR. STEPHENS:

5 Q. Is it fair to say that the
6 transition from a low to high can be referred to
7 as a rising edge?

8 A. Yeah, that is a pretty commonly
9 understood term.

10 Q. And the transition from high to low
11 would be a falling edge?

12 A. Similarly.

13 Q. And the transition would occur at
14 regular intervals?

15 MR. COURTNEY: Objection to the
16 form.

17 THE WITNESS: Generally speaking,
18 that would be true in most digital systems,
19 but not necessarily.

20 There is also techniques relating to
21 power smoothing and jitter control where
22 there are small variations in the period

1 between rising edges and/or falling edges.

2 But, for the most part, that is a
3 true statement.

4 BY MR. STEPHENS:

5 Q. What do you mean by the period
6 between rising and falling edges?

7 A. The period is the time between
8 repeating events.

9 So, whether it is, in a clock
10 signal, the period is the time between one rising
11 edge and the next rising edge, or alternatively
12 from a falling edge to the next falling edge.

13 Q. Do clock signals serve to
14 synchronize operations among components in the
15 digital system?

16 MR. COURTNEY: Objection to the
17 form.

18 THE WITNESS: The word synchronize
19 is not well-defined in the industry amongst
20 practitioners. It could mean a variety of
21 different things in different contexts.

22 So, I'm going to ask you to be more

1 specific in terms of what you mean by that
2 word in that question.

3 BY MR. STEPHENS:

4 Q. I will refer to Column 14 at Line 61
5 of the '381 patent.

6 A. Let me get there. Column 14, Line
7 -- I'm sorry?

8 Q. 61. Take a moment to just read the
9 sentence that begins on Line 61.

10 A. So, the '381 in this column is using
11 synchronized to mean that portions of the
12 circuitry that is being controlled in a way by
13 the clock signal, operate or begin operations at
14 rising and falling edges.

15 Q. So, here the clock signal does serve
16 to synchronize operations in the memory system?

17 A. Well, that is how the word is being
18 used in the '381, in this column, that portions
19 of the memory device that are using the S clock
20 signal, do so based on the same clock signal.
21 And, therefore, they are synchronous with that
22 clock signal. And, so, the patent drafter has

1 used the word synchronized to indicate that
2 portions of the memory device operate together at
3 the same time according to the rising and/or
4 falling edges of the S clock signal.

5 Q. In the transition, does a clock
6 signal trigger actions in a digital circuit?

7 A. For a synchronous systems, the --
8 there is a clock signal that, in some
9 circumstances, trigger operations on the rising
10 or falling edge. But, there are also digital
11 systems and devices in which the clock edges
12 don't initiate actions, they terminate actions.

13 So, it is, again, as I indicated at
14 the start of this portion of the deposition,
15 there was, the word synchronized is fluid and
16 doesn't have a consistent meaning across all
17 systems.

18 In this case, that is how it is
19 being used in the '381, specifically at Line 64
20 it says: Operations and data transfers occur at
21 the rising and/or falling edge of the clock
22 signal.

1 So, the way that it is being used in
2 this patent is that the clock signal initiates at
3 least some operations and some data transfers at
4 those edges of the clock signal.

5 Q. Okay. And are you familiar with
6 D flip-flops?

7 A. Yes, I am familiar with
8 D flip-flops.

9 Q. Can you briefly describe what a D
10 flip-flop is?

11 A. A D flip-flop is one variety of
12 storage element that is commonly used in digital
13 systems. It has typically three outputs, three
14 inputs -- I'm sorry, let me start that again.

15 It typically has two inputs and one
16 output, although there can be variants that have
17 additional inputs or outputs.

18 The principal input is data in, its
19 principal output is data out, and it has a clock
20 input that is edge sensitive.

21 Q. So, what happens when there is a
22 transition in the clock signal at the input of

1 the D flip-flop?

2 MR. COURTNEY: Objection to the
3 form.

4 BY MR. STEPHENS:

5 Q. Oh, I can rephrase the question.

6 A D flip-flop can latch data at the
7 data input, correct?

8 A. I think a POSITA would understand
9 that a D flip-flop, its purpose in life is to
10 capture data at an edge, either rising or
11 falling, depending on the variety that is
12 present, for a period of time before that edge on
13 the data input.

14 Q. Some D flip-flops are triggered by a
15 rising edge?

16 A. Yes.

17 Q. And others are sensitive to the
18 falling edge?

19 A. They have a different symbol if they
20 are falling edge versus rising edge, triggered.
21 So, you can tell from the picture of it in a
22 schematic, whether it is a rising edge or a

1 falling edge sensitive D flip-flop.

2 Q. What would the symbol look like to
3 distinguish the rising edge from falling edge?

4 A. The falling edge sensitive D
5 flip-flop would have a little circle on the clock
6 input as well as the triangular shape.

7 If we look at, I -- I don't know if
8 there are any in the '381. There are certainly
9 pictures of that in Grundy. Just quickly
10 scanning the figures of the '381, I do not see
11 any D flip-flops -- oh, so, yes, Figure 2B has
12 D flip-flops, all of a rising edge variety.

13 And we have to check the text to be
14 sure that there is not an error in the symbology,
15 but the standard symbology is that the three flip
16 flops in Figure 2B are rising edge flip-flops,
17 rising edge trigger flip-flops to be precise.

18 MR. STEPHENS: We have been going
19 now for about an hour. Would you like to
20 take a 5 or 10 minute break?

21 THE WITNESS: That sounds good.

22 (Recess taken -- 11:04 a.m.)

1 (After recess -- 11:15 a.m.)

2 BY MR. STEPHENS:

3 Q. Dr. Przybylski, did you have any
4 discussions with Counsel during the break?

5 A. No, not at all.

6 Q. All right. I would like to continue
7 our review of the '381 patent.

8 So, let's first look at Claim 1,
9 which is at Column 27 starting at line, around
10 Line 47.

11 A. I see it.

12 Q. You have reviewed Claim 1, correct?

13 A. Yes.

14 Q. And line -- around Line 52 there is
15 a limitation directed to at least one common data
16 interface, do you see that?

17 A. Yes, I do.

18 Q. And the claim recites that the: At
19 least one common data interface is configured to
20 transfer command data, address data, input data,
21 and output data, wherein, at least one of command
22 data, address data, input data, and output data

1 is transferred and in synchronization of both
2 rising and falling edges of the clock signal when
3 the flash memory device is in a double data rate
4 configuration.

5 Do you see that?

6 A. You read that accurately.

7 Q. What is your understanding of a
8 double data rate configuration?

9 MR. COURTNEY: Objection to the
10 form.

11 THE WITNESS: A POSITA would
12 understand that a double data rate refers to
13 transferring two pieces of data per cycle,
14 one, in -- generally in connection with one
15 of the edges of a clock or a strobe, and
16 another in relation to a falling edge of a
17 clock or strobe.

18 We can look and see if the '381 has
19 defined it more precisely for this context.

20 So, on Column 14 at the bottom, it
21 says: Alternatively, in a double data rate,
22 DDR implementation, both rising and falling

1 edges of S clock signals may be used to latch
2 information.

3 So, this is somewhat narrower than
4 what I said earlier, and that is specifically
5 referring to the -- an S clock signal as the
6 source of the edges that are used to latch
7 information.

8 Q. So, in a double data rate
9 configuration as described in the sentence that
10 you have just read from Column 14 to Column 15,
11 the memory device would latch information on
12 twice per clock cycle, once on the falling edge
13 and once on the rising edge; is that correct?

14 A. It says that those edges are used to
15 latch. The exact timing of that may vary from
16 implementation to implementation.

17 But, conceptually, there are two
18 pieces of data per cycle as you said, and that
19 the two edges are the critical temporal events
20 that initiate those -- the termination of those
21 communications. So, the latching of the data at
22 the destination.

1 Q. Is double data rate or DDR a term
2 that is commonly used in the field?

3 A. Yes. There are standard memory
4 devices that have that term in their titles, and
5 in which the meaning of those terms are precisely
6 defined within those standards.

7 Q. And what would a configuration be
8 referred to in which data is latched just once
9 per clock cycle?

10 A. Generally, that does not require
11 characterization since that is the normal
12 situation within digital systems.

13 If there is a juxtaposition of that
14 with double data rate than it is frequently
15 called single data rate.

16 But, you don't need to say single
17 data rate over and over again for the -- for
18 systems and configurations that are not double
19 data rate.

20 Q. Okay. I may use the term single
21 data rate at times in our discussion here to
22 juxtapose it against a double data rate.

1 And when I refer to single data
2 rate, I will be referring to configurations in
3 which data is latched as once per clock cycle.

4 Does that sound okay?

5 A. Understood.

6 Q. Are you aware of any other
7 disclosure in the '381 patent apart from the
8 sentence that we have just been examining at
9 Column 14, Line 66 that discloses DDR
10 implementation?

11 MR. COURTNEY: Objection to the
12 form.

13 THE WITNESS: Not off the top of my
14 head. But, there may be. I don't know.

15 BY MR. STEPHENS:

16 Q. You have an electronic version of
17 the '381 patent, correct?

18 A. Yes. That is what I am looking at,
19 that you put in Chat, yes.

20 Q. Are you able to search through the
21 specification for any other descriptions of DDR?

22 A. I can. Did you want me to do that?

1 It was not clear.

2 Q. I'm sorry, yes. Please take a
3 moment and let me know if you see any other
4 description of DDR in the '381 specification.

5 A. In my searching of the '381 has the
6 one instance of DDR that we talked about
7 previously and several instances of double data
8 rate in the claims.

9 Q. But apart from those instances in
10 the claims, you don't -- you have not yet
11 identified any other disclosure of DDR in the
12 specification?

13 A. That is correct. As I said at the
14 outset of this deposition, I have not reviewed
15 the '381 in the -- to the same degree as I have
16 the prior art references at issue in this matter.

17 Q. The sentence that we were looking at
18 at Column 14, Line 66 states that or it describes
19 DDR implementation in the alternative, correct?

20 A. Yes, it says alternatively as the
21 first word of that sentence.

22 Q. And then the next sentence beginning

1 at Line 2 of Column 15 refers to Figure 3A and
2 states: In the example of Figure 3A, however,
3 input data is latched on the falling edge of
4 system clock and output data, 322, appears on the
5 serial output panel 312 SOPx after the rising
6 edge of system clock.

7 Did I read that correctly?

8 A. Yes, you did.

9 Q. So, in Figure 3A, is Figure 3A
10 relates to a standard data rate implementation,
11 correct?

12 A. You said standard data rate.

13 Q. I'm sorry, single data rate.

14 A. Would you repeat the whole question,
15 please?

16 Q. Would you agree that Figure 3A
17 depicts a single data rate configuration?

18 A. It implies that in the text. The
19 figure itself, actually looks like it is double
20 data rate, but it is the use of the double
21 squiggly lines to indicate arbitrary amounts of
22 time between various events is not consistently

1 used.

2 So, for example, the SOPx Line
3 Item 312 shows one byte being transferred in, it
4 looks like 1, 2, 3, 4 edges which would be --
5 could be two bits on each edge or some other
6 characterization. We would have to look at what
7 it means as far as the width of SOPx to
8 understand whether that is a single data rate or
9 double data rate.

10 Q. In Figure 2B, there is a signal
11 SIP0?

12 A. SIP0. I see SIP0, yes.

13 Q. And that signal is received by an
14 input buffer 242, do you see that?

15 A. Yes. One of the several input
16 buffers described, depicted there is, has SIP0 as
17 an input.

18 Q. And the output of input buffer, of
19 the 242 buffer that receives SIP0, is provided as
20 input to and gate 252 that feeds into a D
21 flip-flop 246.

22 Do you see that?

1 A. I do.

2 Q. Can you tell from this figure
3 whether the circuitry is configured as single
4 data rate or double data rate?

5 A. Not without looking more closely at
6 the source of the S clock I input. It is not
7 uncommon, if dealing with double data rate at the
8 interface to a device that, to operate the
9 internals of the device at twice the frequency.

10 So, S clock I would, if it is at the
11 same frequency as S clock external to the device,
12 then that would be single data rate.

13 If it is S clock I internally, it is
14 twice the frequency of S clock, then that would
15 be double data rate from the perspective of the
16 interface.

17 Q. I see. So, if the -- if the
18 internal clock, S clock I, has the same frequency
19 as the system clock, then this configuration
20 would represent a single data rate configuration?

21 A. Unless there is additional circuitry
22 attached to SER under IN0, and IN under EN0 that

1 would capture data on the falling edge of
2 S clock I that is, that would not, that is
3 outside of Figure 2B that would be another way
4 that this could be a double data rate
5 implementation.

6 Again, looking at a single figure is
7 often not adequate to understand the full
8 circuitry that is being disclosed in an
9 embodiment of a patent.

10 Q. So, I think you generally
11 characterized maybe two ways to implement a
12 double data rate configuration.

13 One would be to double the frequency
14 of the interface clock as your internal clock,
15 and another being to provide, use a clock -- and
16 use a clock internally that has the same
17 frequency as the interface clock but provided a
18 first set of flip flops that capture on the
19 rising edge and a second set of flip flops that
20 capture on the falling edge.

21 Is that generally correct? Or, do
22 you think anything that I got wrong there?

1 MR. COURTNEY: Objection to the
2 form.

3 THE WITNESS: You have captured the
4 two ways that I articulated that this
5 embodiment could be double data rate, that is
6 not the full set of implementation
7 possibilities for things that are externally
8 double data rate.

9 BY MR. STEPHENS:

10 Q. Let's just -- were those two options
11 that I just characterized in my last question,
12 were they well known by the time of the, let's
13 say, by September 2006 -- I'm sorry,
14 September 2005, which was the earliest
15 provisional filing date listed on the '381
16 patent?

17 A. By well known, you mean by a POSITA
18 as defined in this case?

19 Q. Yes.

20 A. Let me go back and review the
21 precision of that definition, because it, we
22 are -- you are asking about a date where the

1 world was changing very rapidly and so it is not
2 necessarily clear.

3 So, let's see. Dr. Sechen's
4 definition was a bachelor of science in
5 electrical engineering, computer engineering, or
6 related field and at least three years of
7 experience. So, that means the undergraduate
8 degree was finished in the time frame of 2003 or
9 thereabouts, or earlier. And the intervening
10 period of time between the critical date and that
11 completion of the undergraduate degree is spent
12 in research, design, or development of memory
13 circuits.

14 Now, memory circuits encompasses a
15 great many things. Most of which were not double
16 data rate in this time frame. A few things were,
17 it was just -- actually no, there were no
18 commercially available double data rate devices
19 until, if my memory serves me correctly, later
20 than the critical date.

21 If you have data to the contrary,
22 please let me know. Is that -- again, this is

1 20 years back and the exact timing of various
2 events is subject to the vagrancies of memory.

3 So, my presumption here is that a
4 POSITA would not have had direct exposure to a
5 double data rate memory circuit, the -- in the
6 internal implementation of that by the critical
7 date.

8 So, it may, a POSITA may have
9 learned of that by some other means other than
10 direct exposure in the -- his work, his or her
11 workplace.

12 So, maybe they have familiarity with
13 the implementation of double data rate memory
14 circuits, maybe not. It is unclear.

15 Q. So, referring back to the '381
16 patent at Figure 2B, is it fair to say that your
17 opinion is that looking at this figure alone, you
18 were unable to determine whether it is
19 configured, it has a -- has a single data rate or
20 double data rate configuration?

21 A. We would have to look at more of the
22 patent than just Figure 2B to determine that.

1 There certainly is some text associated with 2B
2 that I have not reviewed recently enough to
3 remember what it says.

4 We could do that now if you so
5 choose. And there are also the other figures
6 within the Figure 2 grouping, or other figures
7 that describe the operation of this particular
8 embodiment that would clarify the question.

9 Q. Well, maybe I will put my question
10 like this.

11 We looked earlier through the
12 specification and we are only able to identify
13 one, at least explicit extents of the
14 specification, mentioning double data rate.

15 Would a POSITA have sufficient
16 guidance from the '381 patent to be able to
17 implement its embodiments in a double data rate
18 configuration as of the critical date?

19 MR. COURTNEY: Objection to the
20 form.

21 THE WITNESS: That is not a question
22 I needed to consider in the formulation of my

1 opinions in this matter.

2 As I said, there is the critical
3 date is around the time when things were
4 changing rapidly and I would need to consider
5 that carefully to form a proper opinion on
6 that question. And I can't do that here
7 without additional research or documentation.

8 BY MR. STEPHENS:

9 Q. I think it is a fairly
10 straightforward question and I believe it is
11 relevant to your analysis of Claim 1, which
12 requires, as we established, a double data rate
13 configuration.

14 So, I will just ask again, from your
15 review of the '381 patent, would a POSITA have
16 this skill, the requisite skill, to implement its
17 embodiments in a double data rate configuration?

18 MR. COURTNEY: Objection to the
19 form.

20 THE WITNESS: I think I have to
21 answer in the same way. I disagree with your
22 characterization that I would need to answer

1 that question as a priori to the formulation
2 of my opinions, vis- -vis the validity with
3 regard to the arguments in the petition
4 regarding the val -- the obviousness of these
5 claims in light of the two references that
6 are cited.

7 So, I haven't formed an opinion
8 whether a POSITA would, in that time frame,
9 would be able to actually construct such a
10 memory based solely on the '381 disclosure.
11 And so, I haven't formed that opinion and I
12 am unable to do so right now without further
13 research.

14 BY MR. STEPHENS:

15 Q. Would you say then that in forming
16 your opinions as to the double data rate
17 limitations in your declaration, that you have
18 not considered the level of disclosure of double
19 data rate in the '381 patent?

20 MR. COURTNEY: Objection to the
21 form.

22 THE WITNESS: It is clear that the

1 '381 does disclose double data rate and
2 describes what it means.

3 So, that is sufficient to look at
4 the claims, look at the pr -- at the prior
5 art references, and draw conclusions as to
6 whether there is disclosure of these claims
7 within the prior art references that were put
8 forward. And that is what I did.

9 BY MR. STEPHENS:

10 Q. In Paragraph 79 of your
11 declaration --

12 A. Hold on. Let me get to 79. Okay.
13 I am there.

14 Q. The first sentence you state that in
15 conclusion with regard to a double data rate
16 configuration, the disclosure of Grundy is
17 incomplete and nonfunctional.

18 Do you see that?

19 A. I do.

20 Q. Would you say that the '381 patent
21 has a more complete disclosure than Grundy as it
22 pertains to double data rate configurations?

1 MR. COURTNEY: Objection to the
2 form.

3 THE WITNESS: Certainly it is more
4 accurate because it is not faulty.

5 Grundy tries to do more but in a way
6 that is nonfunctional. And, so, from that
7 perspective, Grundy is less complete and
8 because what it does disclose, doesn't work.

9 BY MR. STEPHENS:

10 Q. So, in your opinion, a POSITA would
11 know how to implement double data rate from less
12 disclosure in the '381 patent than what Grundy
13 provides in its disclosure?

14 MR. COURTNEY: Objection to the
15 form.

16 THE WITNESS: That is not what I
17 said. It is also not one of my opinions in
18 my declaration.

19 What my declaration says in 79 and
20 elsewhere, is that Grundy is a flawed
21 reference, in that what it does try to teach
22 is not functional and a -- it is within the

1 skill of a POSITA to look at what is
2 disclosed and to realize that it wouldn't
3 work.

4 BY MR. STEPHENS:

5 Q. Well, I'm just trying to understand
6 the basis for your opinion here because there
7 seems to be an asymmetry between what the '381
8 patent is disclosing and what Grundy provides.

9 So, in Grundy, or in your
10 declaration I should say, you said two things
11 about Grundy in the first sentence of
12 Paragraph 79.

13 A. Yes.

14 Q. One is that Grundy is incomplete.
15 And second that Grundy is not functional.

16 So, as to the first, Grundy being
17 incomplete, I am wondering in what sense it is
18 incomplete and what incomplete really means
19 relative to a disclosure of double data rate in
20 the '381 patent?

21 A. Okay. So, these are questions that
22 are answered explicitly in the preceding

1 paragraphs. If you would like, I can read them
2 into the record about how Grundy is deficient and
3 both in being incomplete and nonfunctional, if
4 you want to take the time for me to do that.

5 Q. What more would a POSITA need in
6 order to know how to implement Grundy as in a
7 functional double data rate configuration?

8 A. Let me review those paragraphs if
9 you don't mind.

10 Could you repeat the question,
11 please?

12 Q. What additional information would a
13 POSITA need in order to implement Grundy in a
14 double data rate configuration.

15 A. Okay. So, at beginning it -- at my
16 paragraph, where does it really start.

17 Starting basically at Paragraph 67,
18 I go through the disclosure of Grundy in detail
19 and then I characterize its incompleteness with
20 regard to the lack of disclosure of the output
21 stage of Grundy and also of the inadequacy of the
22 protocol engine and I/O control portions of

1 Figure 17 and its associated disclosure to
2 operate at a double data rate, rate of data input
3 and output.

4 Then I also go on to disclose how a
5 POSITA would understand that the described
6 alteration in Paragraph 88, I think, is that
7 accurate -- that suggests that Grundy could be
8 transformed into a double data rate
9 implementation simply by doubling up the input
10 registers 315, that that is -- that disclosure
11 doesn't work because of the relative timing of
12 the data input and the clock.

13 And so that is nonfunctional, in
14 addition to the incompleteness of the disclosure
15 with regard to the rest of the -- in the
16 embodiment of Figure 17.

17 Q. So, in your view, part of the
18 deficiency in Grundy is a lack of disclosure in
19 terms of how the control circuitry would operate
20 in the double data rate configuration; is that
21 correct?

22 A. Let me find the exact paragraph

1 where I do refer to that aspect of it.

2 So, beginning in Paragraph 73 and
3 then continuing into Paragraph 74 of my
4 declaration, I dis -- discuss the issue that the
5 internal buses would need to be doubled up and
6 that the description of Paragraph 88 is
7 insufficient, since it tries to do a description
8 of how you would need to change Figure 17 to make
9 a double data rate. That description is grossly
10 inadequate because it doesn't describe what you
11 have to do to the rest of Figure 17, and the
12 modification that it does propose for the input
13 stage of Figure 17, that is inaccurate also.

14 So, those are the bases of my
15 opinion, in answer to your question.

16 Q. Are any of these types of
17 modifications that would, in your opinion, need
18 to be made to Grundy to implement double data
19 rate configuration? Are those types of
20 modifications described in the '381 patent?

21 A. I don't know.

22 Q. The modifications that would need to

1 be made and the circuits that are depicted in its
2 figures?

3 MR. COURTNEY: Objection to the
4 form.

5 THE WITNESS: I don't know. As I
6 have said before, I haven't reviewed the '381
7 in great detail. Our preliminary searches
8 that we did together, leading to double data
9 rate in the '381, failed to find that.

10 But, I did not search for that as a
11 necessary precondition to forming my opinions
12 about Grundy and so I can't really answer
13 that definitively.

14 BY MR. STEPHENS:

15 Q. Okay. Is it fair to say that you
16 don't, sitting here right now, you don't know
17 whether the '381 patent discloses the underlying
18 technical solutions for a double data rate
19 configuration that you say are missing from
20 Grundy; is that correct?

21 MR. COURTNEY: Objection to the
22 form.

1 THE WITNESS: I am going to take
2 exception to your question because it is --
3 there is not only stuff missing from Grundy,
4 but the stuff that is in Grundy is wrong.

5 So, it is -- that is damming to a
6 much greater extent than just having a brief
7 description of something and leaving it to a
8 POSITA to research and come up with the
9 appropriate circuitry.

10 You know, we understand that patents
11 don't need to disclose every little detail.
12 But, what they disclose has to be correct.

13 So, to answer your question sitting
14 here today, no, I can't say that. I can't
15 say to the level of an opinion about what is
16 or is not in the '381 with regard to
17 implementations of double data rate.

18 It is not a subject matter that I
19 needed to understand to form my opinions. It
20 is not one of my formal opinions within the
21 four corners of my declaration. And, so, I
22 can't say that one way or another today.

1 I think I answered your question.

2 If not, please restate it.

3 BY MR. STEPHENS:

4 Q. No, thank you. I think I understand
5 your position.

6 A. Okay.

7 Q. Let's turn to Figure 16A of the '381
8 patent?

9 A. 16A. Okay. A timing diagram.

10 Q. Yes. It refers to basic input latch
11 timing. Do you see that?

12 A. I do.

13 Q. Can you describe briefly in your own
14 words what you see in Figure 16A?

15 A. I see a timing diagram with inputs
16 CS bar S clock, IPE, SIP, OPE, and SOP as the
17 signals being described over the course of about
18 50 cycles of the S clock.

19 Q. S clock refers to system clock?

20 A. I believe that is the association in
21 the '381. But, that is what we found from our
22 initial searching.

1 Q. What does CS bar stand for?

2 A. Conventionally, it means chip
3 select. But I do not know if that is what it
4 means here. I haven't looked.

5 Q. And the bar refers to active low?

6 A. Yes, that is again, the traditional
7 meaning of that symbology, and I don't know
8 whether the '381 has modified that explicitly.
9 But, certainly the convention across the industry
10 is that the bar, the pound sign indicates bar
11 which means active low.

12 Q. Do you recall what IPE stands for?

13 A. No, I don't.

14 Q. Would that be input enabled?

15 A. Perhaps, I don't know.

16 Q. Can you take a moment and look
17 through the '381 patent and confirm if you agree
18 with that?

19 A. I apologize to the court reporter, I
20 spoke over you.

21 Q. I apologize. I may have spoken over
22 you.

1 A. It is Column 3, Line 42 it says:

2 That IPE stands for Input Port Enable, and OPE
3 stands for Output Port Enable.

4 Q. Okay. Thank you for the
5 clarification.

6 A. Okay. Later in that paragraph, it
7 describes more about the functionality of IPE if
8 you want me to read that into the record.

9 Q. Sure. What does it say there about
10 input port enabled?

11 A. Starting in Line 45, it says: The
12 memory device of the present invention receives
13 an information signal stream through its SIP, SIP
14 port only when IPE stays in a high logic state.

15 In the Figure IPE is active low, if
16 I remember correctly. And so high logic state
17 would actually be a low voltage. And, also, the
18 device transmits the output data signal streams
19 through its SOP port only when the OPE signal
20 stays in a high logic state. That summarizes the
21 fundamental operation of those two signals.

22 Q. That is helpful. And I think

1 actually, it was the CS signal that was active
2 low, I believe. In Figure 16A, IPE is
3 identified?

4 A. You are absolutely correct, I
5 apologize for my error. Yes.

6 Q. The final waveform shown in this
7 timing diagram is SIP.

8 Could you read what SIP refers to in
9 the '381 patent?

10 A. Yeah. It is the Serial Input Port.

11 Q. And in Figure 16A in the serial
12 input waveform, there are some annotations IS and
13 IH, do you see those?

14 A. Yes.

15 Q. Do you have an understanding as to
16 what those refer to?

17 A. Again, conventionally, that would be
18 the set up and hold times for the data around the
19 clock edge. I would have to search the patent to
20 be confirmed that that is the understanding of
21 the inventors of the '381.

22 Q. So, would, conventionally, IS refer

1 to input set up time?

2 A. There is different ways of denoting
3 it. It is not -- the IS and IH are not
4 universally conventional. The timing diagram,
5 the way it is showing the data on the SIP port,
6 input line relative to a clock edge with IS and
7 IH would confirm to a POSITA that it is talking
8 about set up and hold.

9 But, since you are asking about it
10 in more detail, I will search for that. So, set
11 up and hold don't actually appear in the text of
12 the patent. So, we are going to rely on the
13 conventionality of the figure and say that a
14 POSITA would understand that that is the input
15 set up and the input hold time.

16 Q. What does in -- generally, what do
17 the concepts of input set up and input hold time
18 mean to a POSITA?

19 A. A POSITA would understand that
20 various types of storage elements, including flip
21 flops and latches, have some triggering event
22 that causes data to be captured.

1 And that the data on the data input
2 has to be stable around that event.

3 And the set up time is the minimum
4 time that the data has to be stable prior to the
5 capturing event. And the hold time is the
6 minimum time that the data has to be stable after
7 the capturing event.

8 So, in this case, the capturing
9 event is shown in Figure 16A as being the rising
10 edge of S clock, and it shows that there is a
11 non-zero set up and a non-zero hold time around
12 that rising edge of S clock.

13 Q. Was it common as of the critical
14 date to capture data in a storage element during
15 a stable period of the data that you are
16 capturing?

17 A. Yes, that is a fundamental aspect of
18 digital electronics design going back decades and
19 decades.

20 Q. So, in this figure, S clock, the
21 rising edge is shown to be in that middle of the
22 stable period between the set up and hold times.

1 Is -- was it common to align the
2 clock and the data to be captured and in this
3 fashion as shown in Figure 16A?

4 A. All data elements, storage
5 elements -- flip flops, latches, registers, have
6 intrinsically set up and hold times.

7 Those can be altered to some extent
8 based on the design of those storage elements.
9 But, a basic understanding of, that a POSITA
10 would have been exposed to at the undergraduate
11 level, is that you need to have data stable
12 before and after the capturing event at the
13 storage element.

14 Q. So, what would you do then if, in
15 your -- if at the input interface of a device, a
16 clock signal and a data signal arrived that are
17 edge aligned, would there be any phase offset
18 that would be created before capturing the data
19 in the memory device?

20 MR. COURTNEY: Objection to the
21 form.

22 THE WITNESS: What do you mean by

1 phase offset?

2 BY MR. STEPHENS:

3 Q. In order to, let's say, delay the
4 clock signal such that the transitions in the
5 clock signal occur during a stable period of the
6 data to be captured?

7 A. Well, that is certainly one if --
8 let me start again.

9 As a designer of a digital circuit,
10 you want to make sure that it is functional. In
11 other words, that all of your storage elements
12 are configured properly relative to the input
13 that is being captured and the clock or strobe or
14 qualified clock that is going to be doing the
15 capturing.

16 There are numerous ways for ensuring
17 that that is the case. For the particular
18 configuration that you are describing, delaying
19 the clock is one of the possibilities, but not
20 the only one.

21 Q. Were those numerous ways, would they
22 have been known to a POSITA as of the critical

1 date?

2 A. I haven't formed an opinion about
3 that specifically. It was not necessary to do --
4 to form that opinion since the petition didn't
5 suggest that a POSITA would modify Grundy to make
6 it functional.

7 Q. So, sitting here today, thinking
8 back to the critical date of the '381 patent in
9 2005, would a POSITA have been aware of solutions
10 to capture data in a synchronous fashion during
11 the stable period of the data waveform?

12 MR. COURTNEY: Objection to the
13 form.

14 THE WITNESS: That is a slightly
15 different question than your previous one.

16 Did you intend it to be?

17 BY MR. STEPHENS:

18 Q. I can -- you can answer the question
19 that I just asked, that I meant them to be about
20 the same question. I'm not sure if there is a
21 distinction in the meaning.

22 A. Okay. So, please repeat the

1 question as asked.

2 Q. As of the critical date of the '381
3 patent, would a POSITA have been aware of
4 solutions to capturing data synchronously during
5 the stable period of the data waveform?

6 MR. COURTNEY: Objection to the
7 form.

8 THE WITNESS: Possibly. It is,
9 again, a question I have not needed to
10 consider to form my opinions in this matter.
11 I would have to give it thought and research
12 into general practices in the vicinity of the
13 critical date to know for sure.

14 It is possible that a POSITA would
15 have had enough exposure to signal
16 conditioning techniques that would be
17 effective in the circumstance that you have
18 described in the previous question.

19 But everything being edge aligned,
20 or maybe not. That's -- that is a circum --
21 the question of edge aligned versus center
22 aligned data and clocks really didn't come

1 into common consideration until later in that
2 decade with the -- and, so, I don't have an
3 opinion on that question.

4 BY MR. STEPHENS:

5 Q. As of the critical date, would a
6 POSITA have been aware of solutions for capturing
7 data where the data was presented at the input
8 interface edge aligned with the clock?

9 MR. COURTNEY: Objection to the
10 form.

11 THE WITNESS: Again, it was not a
12 question that I needed to answer to form my
13 opinions in this matter.

14 And I'm not in a position to form
15 new opinions on the fly here, relative to
16 what would or would not have been obvious to
17 a POSITA at that time. I would need to
18 research that prior to forming such an
19 opinion.

20 BY MR. STEPHENS:

21 Q. Do you have any serious doubt that
22 in 2005, a POSITA would not have been familiar

1 with solutions to capturing data with an edge
2 aligned clock?

3 A. I don't quite know what you mean by
4 a serious doubt. I do have some doubt and
5 therefore, I am not willing to form that opinion
6 on the fly.

7 Q. In your opinion, how much exposure
8 must a POSITA have to prior art to bring the
9 knowledge of that prior art to bear?

10 In other words --

11 MR. COURTNEY: Objection --

12 BY MR. STEPHENS:

13 Q. Would you agree that a POSITA is
14 charged with the knowledge of all of the prior
15 art as of the critical date?

16 MR. COURTNEY: Objection to the
17 form.

18 THE WITNESS: I have heard that
19 before.

20 BY MR. STEPHENS:

21 Q. In your experience, were you aware
22 of any digital systems before the critical date

1 that capture data within the edge aligned clock?

2 A. Quite possibly, but, I don't --
3 can't think of any off the top of my head.

4 Q. Were you aware of any publications
5 before the critical date of the '381 patent that
6 described digital systems capturing data within
7 an edge aligned clock?

8 A. Capturing with an edge aligned
9 clock.

10 There are so many pieces of
11 literature that I reviewed or even wrote that may
12 have described such a thing, such a circumstance.
13 Again, I don't remember everything that I have
14 read. I don't know sitting here today whether
15 that statement is true.

16 Q. Earlier you testified that as a
17 designer of a digital circuit, you want to make
18 sure that it is functional. In other words, that
19 all of your storage elements are configured
20 properly relatively to input that is being
21 captured and the clock or strobe or qualified
22 clock that is going to be doing the capturing.

1 And you stated that there are numerous ways for
2 ensuring that that is the case.

3 Again, are you -- I will just ask,
4 of those numerous ways that you were thinking of
5 in your testimony there, were any of them known
6 before the critical date of the '381 patent?

7 MR. COURTNEY: Objection to the
8 form.

9 THE WITNESS: I mean, that question
10 that you asked previously was about a design
11 phase of a digital system where you are
12 calculating the arrival time of data at
13 storage latches and/or flip flops or
14 whatever. And to making sure that the whole
15 thing is functional.

16 There are simulation techniques.
17 There are static timing techniques to ensure
18 that that is the case.

19 And if it is not the case you modify
20 the design in order to make it the case.
21 That is, the thought process for a -- in the
22 design phase is different than what we have

1 been previously talking about which is, you
2 know, a POSITA looking at Grundy and deciding
3 that he knows how to fix it. That is a much
4 harder question than the, you know, what is
5 going on within the des -- an engineer's mind
6 as he is designing something from scratch.

7 So, the answer to your question is
8 yes, the techniques are known prior to the
9 critical date. But that is not necessarily
10 the same as saying that a POSITA looking at
11 Grundy would recognize that he has in his
12 tool box a solution to the nonfunctionality
13 of the input buffers.

14 BY MR. STEPHENS:

15 Q. Did you address any of the
16 techniques that were known as of the critical
17 date in your declaration, in your opinions on
18 Grundy?

19 A. No. It was unnecessary for me to do
20 so to rebut the arguments in the petition and to
21 highlight the failures of the references that
22 were presented there and the analysis of them,

1 that was articulated in the petition.

2 MR. STEPHENS: All right. We have
3 been going for a little bit over an hour now.

4 Would this be a good time for a
5 break, Dr. Przybylski?

6 THE WITNESS: From my perspective,
7 any time is a good time for a break.

8 (Recess taken -- 12:23 p.m.)

9 (After recess -- 12:34 p.m.)

10 BY MR. STEPHENS:

11 Q. Dr. Przybylski, I would like to
12 continue our discussion of the '381 patent.

13 But, first, did -- over the break,
14 did you have any discussions with Counsel?

15 A. Not at all.

16 Q. All right. Let's look at Figure 2A,
17 please, of the '381 patent?

18 A. 2A, yes.

19 Q. Are you familiar with Figure 2A?

20 A. I have seen it before.

21 Q. Do you recall reviewing this figure
22 in the preparation of your declaration?

1 A. In the preparation of my
2 declaration, I have looked at Figure 2A and some
3 of the text associated with it to understand the
4 basic operation of this proposed memory device.

5 Q. So, what is depicted in the
6 Figure 2A there is a memory device 200, correct?

7 A. Yes.

8 Q. And then we see a memory bank A202
9 and a memory bank B204, correct?

10 A. That is what is depicted in
11 Figure 2A, yes.

12 Q. And then for the memory banks, there
13 is a block for an address and data switch 206,
14 correct?

15 A. Correct.

16 Q. And we see two interface circuits
17 205 and 207, correct?

18 A. Yes, and those are labeled PAR under
19 IN0 and PAR under IN1, although that may be --
20 that is the actual buses not the circuitry, so,
21 please ignore that last sentence.

22 Q. Interface circuit 205 includes

1 Link 0 Interface 230, Input Serial to Parallel
2 Register 232, and Output Parallel to Serial
3 Register 234, correct?

4 A. That is what is shown in Figure 2A,
5 yes.

6 Q. Figure 2A also shows that the memory
7 device includes a Control Interface 208, correct?

8 A. Yes, 208 is labeled a control
9 interface.

10 Q. There is a CS bar signal, S clock
11 signal and RST bar signal shown as inputs to the
12 Control Interface 208, correct?

13 A. Correct.

14 Q. All right. I would like to look at
15 the description in the patent of the Control
16 Interface 208.

17 So, I believe that starts at
18 Column 8, Line 47.

19 A. Column 8. I'm going there.
20 Column 8, 47. I am looking at that.

21 Q. And the sentence starting at
22 Column 8, Line 47 reads: Control Interface 208

1 includes standard input buffer circuits and
2 generates internal chip select signal chip SEL,
3 internal clock signal SCLKI, and internal reset
4 signal, reset corresponding to CS bar SCLK and
5 RST bar respectively.

6 Did I read that correctly?

7 A. Yes, you did.

8 Q. So, the Control Interface 208 takes
9 the external SCLK signal and through a standard
10 input buffer circuits, generates an internal
11 clock signal called SCLKI, correct?

12 A. That is what it says in Column 8,
13 yes.

14 Q. And SCLKI is the internal clock
15 signal, correct?

16 A. Well, it is shown in Figure 2A. It
17 is going into the central portion of the
18 embodiment. So, it -- and is not shown there as
19 going externally to the memory device. So, the
20 -- and it is called the internal clock signal in
21 Line 49 of Column 8. So, the answer would be
22 yes.

1 Q. So, that internal clock SCLKI is
2 distributed to and used by various components
3 throughout the memory device 200, correct?

4 A. In Line 52 it says: Reset and SCLI
5 are used by many circuits throughout the memory
6 device 200.

7 Q. You are reading from Column 8,
8 Line 52 to 53?

9 A. Yes, exactly so.

10 Q. Now, let's turn to Figure 2B. Are
11 you familiar with Figure 2B?

12 A. We looked at it earlier today, yes.

13 Q. And this depicts the serial data
14 link 232 in more detail, correct? I'm sorry,
15 serial data link 230.

16 A. Right. Yes. There is a commonality
17 of unit numbers between 2A and 2B showing unit
18 Number 230 as being the serial links -- link 0
19 interface.

20 Q. And as shown in Figure 2B, the
21 serial -- well, the link interface 230 includes a
22 number of components, including input buffers 242

1 and D flip-flops 246, correct?

2 A. The 242 are input buffers and 246
3 are D flip-flops. Was that the question you
4 asked?

5 Q. That's correct. You would agree
6 that the link, interface 230 shown in Figure 2B,
7 includes input buffers 242 and D flip-flops 246?

8 A. Yes, that is what is shown clearly
9 in Figure 2B.

10 Q. And in Figure 2B, we can see that
11 the clock inputs to the D flip-flops are the
12 internal clock signal SCLKI, correct?

13 A. Yes, it is shown that way.

14 Q. Let's turn to Figure 2C?

15 A. I am there.

16 Q. This figure shows in greater detail
17 components of the input serial 2 parallel
18 register block 232, correct?

19 A. It is labeled 232. It is not up in
20 Figure 2A. It is identified as an input serial
21 to parallel register as part of 205.

22 Q. And in Figure 2C, we can see that

1 there is an input controller 254, a command
2 register 256, a temporary register 258, and a
3 serial data register 260.

4 Do you see those components?

5 A. I do.

6 Q. At Column 9 at Line 34?

7 A. Line 34. 34 or 35?

8 Q. Yeah, I'm sorry. 35.

9 A. Yeah, I am there.

10 Q. Going out to 36, it reads: The
11 input serial to parallel register block 232
12 includes an input controller 254 for receiving,
13 IN EN0 and SCLKI, among other signals, correct?

14 A. That is what it says at Lines 35
15 and 36 of Column 9 of the '381.

16 Q. All right. And the paragraph just
17 above the paragraph that begins the description
18 in Figure 2C around Line 17 of Column 9 reads:
19 Figure 2C of the schematic of the input serial to
20 parallel register block 232. This blocks
21 receives the clock signal SCLKI, among other
22 signals, correct?

1 A. That is what it says in Column 9,
2 yes.

3 Q. So, as you have reviewed these
4 disclosures, is it your understanding that the
5 internal clock SCLKI and not the external clock
6 signal SCLK directly is used as the inputs to, as
7 the input to controller 254 in block 232?

8 A. I will go back to the figure. Yes,
9 that is what is shown in Figure 2C.

10 Q. The internal clock SCLKI rather than
11 SCLK directly is used to drive the operations of
12 the command register 256 as well?

13 A. So, the command register 256
14 receives an input from the input controller 254.
15 That input is not specified, that I can see in
16 Column 9. It is not labeled SCLKI or anything
17 that would definitively show it to be a
18 derivative of that.

19 But, perhaps you have additional
20 citations that clarify that.

21 Q. I think, let's continue. There may
22 be clarification as we go on.

1 A. Okay.

2 Q. There is a timing diagram shown in
3 Figure 3A, correct?

4 A. There is a timing diagram shown in
5 3A. We looked at it earlier.

6 Q. Yes. At Column 14 at Line 4.

7 A. Okay. Hold on. Column 4 -- 14
8 Line 4, is that what you said?

9 Q. Correct. There is a sentence that
10 reads: The following discussion of the timing
11 diagrams is made with reference to the previously
12 described embodiments of the memory device 200
13 shown in the previous figures in Tables 1 and 2.

14 Do you see that?

15 A. That is what it says in Column 14,
16 yes.

17 Q. And then the next paragraph
18 beginning at Line 8 says: In the example
19 depicted in the timing diagram in Figure 3A, a
20 page read memory command 314 is received at
21 serial data link 230 of the memory device 200 in
22 accordance with the invention.

1 Do you see that?

2 A. That is what it says, yes.

3 Q. So, the timing diagram of Figure 3A
4 is, represents timing in the circuitry that was
5 -- of the memory device 200 that we just looked
6 at in Figure 2A through 2C, correct?

7 A. Yes, in this paragraph on, two
8 paragraphs in Column 14, there is a
9 correspondence made between Figure 2 and
10 Figure 3.

11 Q. And then, if we will go down in
12 Column 14 to Line 40.

13 A. Line 40, I am there.

14 Q. The first sentence in this paragraph
15 reads: Continuing with the example involving the
16 page read memory command as illustrated in
17 Figure 3A, while the chip select signal 302 is
18 set low, and in response to the input port,
19 enables signal 306 at high, the serial input
20 port 308 is sampled on the first rising edge of
21 the serial clock SCLK signal 304 where XX, X acts
22 as a placeholder representing the link interface

1 number.

2 Do you see that?

3 A. Yes, that is what it says.

4 Q. And I would like to consider this
5 disclosure in light of Claim 2.

6 A. Claim 2.

7 Q. Now let's take a look at the
8 language of Claim 2. Claim 2 recites: The flash
9 memory device as claimed in Claim 1, wherein the
10 command data is latched at the first rising edge
11 of the clock signal after the transition of the
12 control signal. Correct?

13 A. That is the language of Claim 2,
14 yes.

15 Q. And the sentence that we just looked
16 at from Column 14, in its description of
17 Figure 3A, does that describe command data being
18 sampled or latched at the first rising edge of
19 the clock signal?

20 A. Okay. What line number were we at?

21 Q. That was around Line 40, Column 14
22 Line 40.

1 A. Thank you. So, the paragraph that
2 we have been focusing on in Column 14 says that
3 the SIPx port is sampled on the first rising edge
4 of the serial clock 304. It doesn't say the
5 first -- first rising edge after what. It just
6 says the first rising edge, but, whereas, the
7 claim language says after the transition of the
8 control signal. So, there is a distinction there
9 between the language of Claim 2 and the language
10 of 14.

11 You know, whether Claim 2 is enabled
12 by Column 14, that is something that I have not
13 had to consider in the preparation of my
14 declaration and is not found in any of my
15 opinions.

16 Q. Figure 3A shows on the serial input
17 port line 308. Is that the first data that
18 appears on assertion of the input port enable
19 signal is the command data CMD 00H, correct?

20 A. Hold on. Okay. Now I am back
21 to 3A. So, commands 00H page read command is,
22 falls within the period of time when IPEX is

1 high. I think that is an answer to your
2 question.

3 Q. Yes, thank you. So, in Figure 3A,
4 we established earlier that this is a timing
5 diagram that relates to the circuitry that we
6 examined earlier in Figures 2A through 2C,
7 correct?

8 A. Yes, we found -- you found for us
9 the corresponding language that links the two.

10 Q. So, in the page read example that is
11 shown in Figure 3A, the command data for that
12 page read command would be presented at the
13 memory device at the serial input port, correct?

14 A. Yes, the architecture is such that
15 there is a single serial input port for all forms
16 of data.

17 Q. And we saw at Figure 2B, that data
18 presented at the -- on the serial input port is
19 first provided to an input buffer 242, correct?

20 A. Along with the chip select, yes.

21 Q. Yes. And after buffering, that the
22 data on the serial input port becomes serial

1 N0SER underscore IN0, correct?

2 A. Yes. It is not clear that that's
3 the -- that the SER means serial. But, the name
4 of the signal is SER under IN0.

5 Q. And SER IN0 is provided to the input
6 of that NAND gate 252, correct?

7 A. Oh, up in this -- 232, is that what
8 you mean?

9 Q. I was saying 252. In Figure 2B,
10 there is a line drawn from SER IN0 down to --

11 A. Oh, down there, I'm sorry. Yes, it
12 goes to the NAND gate, yes, 252.

13 Q. And then in the other input to the
14 NAND gate is the signal IN EN0, correct?

15 A. That is correct.

16 Q. And the output of the NAND gate is
17 provided to the input of the D flip-flop 246,
18 correct?

19 A. To the input to the -- input of one
20 of the flip flops 246, yes.

21 Q. And, the, that D input, or excuse
22 me, that D flip-flop 246 would capture the output

1 of the AND gate based on transitions in the SCLKI
2 internal clock signal, correct?

3 A. Yes, SCLKI is shown going to the
4 clock input of the D flip-flop that we have been
5 talking about.

6 Q. So, would you agree then that the
7 command data in the circuitry of the '381 patent
8 in the embodiments that we are looking at here,
9 are latched based on transitions in the internal
10 clock signal SCLKI, as opposed to the external
11 clock signal SCLK?

12 A. Yes. What is the latching is
13 happening in the D flip-flop that we have been
14 talking about for this particular path in, based
15 on the internal clock SCLKI.

16 Now, there is inevitably additional
17 latching of SCR under IN0. But, what the one
18 that you are talking about is shown in Figure 2B.

19 Q. Now, let's take a look at Figure 2C,
20 then.

21 A. Yes.

22 Q. And we see SCR IN0 is provided as an

1 input to three registers, 256, 258, and 260,
2 correct?

3 A. They are called command REG,
4 temporary REG, and serial data REG. I presume
5 that the spec fleshes out REG to be register.
6 But, that is not shown in 2C.

7 Q. At Column 9 in Line 41 -- take a
8 moment to turn there.

9 A. Starting, for example?

10 Q. Yes. For example, the bits
11 corresponding to a command can be stored in a
12 command register 256.

13 A. There you go, yes. As I presumed.

14 Q. And is it your understanding that
15 the data from SER IN0 would be latched in the
16 command register 256 based on the clock that is
17 derived from the internal clock signal SCLKI?

18 A. As we discussed previously with
19 regard to Figure 2C, the connections between the
20 input controller and the various registers is not
21 labeled.

22 We know that the input controller is

1 -- takes the input enable, IN under EN0, as well
2 as the SCLI internal clock signal to generate
3 that unlabeled signal that goes to two of the
4 three registers.

5 Why it only goes to two of the three
6 is not clear. So, this is probably a qualified
7 clock or some other combination of SCLI and IN
8 under EN0. It may be further described in
9 Column 9. I am not sure.

10 Q. What is a qualified clock?

11 A. It is a clock signal that is gated
12 by a control signal. So, it has all of the
13 characteristics of a clock while it is enabled
14 and is quiescent or low, active low. Not active
15 low, it is either quiescent or at a low level
16 when it is not enabled.

17 So, it is like a clock but not a
18 clock always.

19 Q. At Column 9, like, as you mentioned
20 earlier, there is -- I think we looked at this
21 earlier. Column, or Line 17 refers to the serial
22 input serial to parallel register block 232

1 receiving the clock signal SCLKI, correct?

2 A. 232 receives clock signal -- oh,
3 that is the -- the whole thing is 232; is that
4 right?

5 Q. I believe that is correct.

6 A. Yes, that is correct.

7 Q. So, the command register 256, would
8 store command data from SER IN0, synchronous to
9 some type of clock based on SCLKI. Would you
10 agree that is correct?

11 A. Probably, but not definitively so.
12 I mean, the dis -- disclosure with regard to the
13 output of the input controller 254 is limited so,
14 you know, and there are other possibilities. But
15 I think a POSITA would likely conclude that it is
16 a qualified clock. But, again, it is not -- I am
17 not seeing the definitive description of it as a
18 qualified clock or otherwise.

19 So again, it is -- this is not
20 something that I had to look at carefully or
21 opine on in order to form my opinions in this
22 matter. So, we are working through it. But,

1 there is, without studying it in great detail,
2 there is some ambiguity.

3 Q. And what is your understanding of
4 the difference between the external clock SCLK
5 and the internal clock SCLKI?

6 A. I don't have an opinion on that. It
7 is not something I needed to opine on in my
8 declaration. You know, we have shown that there
9 is some language about block 208 that relates
10 SCLKI to SCLK.

11 But, you know, having a -- you asked
12 my understanding, and I don't really have an
13 understanding that is greater than what you had
14 us read into the record with regard to block 208.

15 Q. And block 208 referred, I think the
16 language that the specification used was that
17 SCLKI is generated by passing SCLK through
18 standard input buffer circuits, correct?

19 A. That was the language we read
20 earlier, yes.

21 Q. Would you agree that a -- well,
22 strike that.

1 What is your understanding of what a
2 standard input buffer circuit would be?

3 A. It would be an input buffer circuit
4 of which there are many different types. That is
5 somewhat, some -- somehow standardized in the
6 mind of the inventors and patent drafter of
7 the '381.

8 Q. And why would they be interested --
9 why would the designer be interested in including
10 standard input buffer circuits?

11 A. Well, you need an input buffer
12 circuit, and they are just saying here that they
13 did not go to great lengths to design a special
14 input buffer circuit.

15 So, they were using standard ones.

16 Q. And what would -- what is the
17 function of a standard input buffer?

18 A. An input buffer, standard or
19 otherwise, is to accept an externally, a signal
20 from outside the chip and to generate an internal
21 version of it according to, you know, the
22 expectations for voltage level changes or other

1 issues related to that transition from outside to
2 inside.

3 Q. So, the buffer may convert signals
4 at one level, say the line level, to voltages
5 that are usable by the circuitry at the logic
6 level; is that correct?

7 A. What do you mean by line level?

8 Q. What would you characterize the
9 voltage levels on the bus to be?

10 A. We haven't seen anything that
11 characterizes those voltage levels in any
12 particular way.

13 But whatever they are, the input
14 buffers are designed to accept those voltage
15 levels and to generate signals that are
16 compatible with the internal circuit.

17 I mean, Grundy as an example of an
18 input buffer circuit, a differential one, I
19 believe, so that is, if you want to talk
20 specifically about that, that would be clear.

21 Q. Would there be a propagation delay
22 resulting from passing SCLK in the '381 patent

1 through the standard input buffer circuits?

2 A. There might be or it just might be
3 very small or it might actually be zero, if it is
4 a nonstandard input buffered circuit.

5 Q. What do you mean by nonstandard?

6 A. Special.

7 Q. So, conventionally, an input buffer
8 circuit would produce a propagation device?

9 A. I don't think there is an idea of a
10 conventional input buffer circuit. There are
11 many different types used in different
12 environments.

13 In this case, the patent drafter of
14 the '381 has left that question entirely to the
15 reader.

16 Q. Okay. Standard input buffer circuit
17 would introduce a propagation delay though,
18 correct?

19 A. Typically, it -- but it might be so
20 small as to be insignificant in the context of
21 the circuit that its included in.

22 Q. Is that propagation time sometimes

1 characterized as a buffer delay?

2 A. Well, this is specifically we are
3 talking about input buffers. So, you would
4 characterize it as an input buffer delay if it --
5 to the extent that it was significant.

6 Q. So, if there is a input buffer delay
7 produced by the standard input buffers in the
8 '381 circuitry, then SCLKI would be a delayed
9 version of the clock signal SCLK, correct?

10 A. Again, we are -- there is no
11 disclosure in the '381 about, that I am aware of,
12 about the details of what it is referring to as a
13 standard input buffer circuit and what the
14 assumptions are being made by the inventors of
15 the '381 about any temporal difference between
16 SCLK and SCLKI.

17 They are merely showing that there
18 are input buffers and that the internal circuit
19 is electrically different than the external
20 circuit.

21 Q. But, the '381 patent at least
22 distinguishes the internal clock signal SCLKI

1 from the external clock signal SCLK, correct?

2 A. Yes, as would be typical. If you
3 just run your external signal straight into your
4 IC, you are running a great risk of electrostatic
5 discharge destroying your whole circuit.

6 It has been done, but it is
7 dangerous.

8 Q. Take a look again at Column 8.

9 A. 8?

10 Q. I'm sorry, Column 14.

11 A. I am looking at Column 14.

12 Q. And at Line 40, we saw that the '381
13 patent discloses here that the serial input
14 port 308 -- I'm starting actually reading from
15 Line 43.

16 The serial input port 308 is sampled
17 on the first rising edge of the serial clock
18 signal 304.

19 Correct? Do you see that
20 disclosure?

21 A. Yes, I see that disclosure.

22 Literally, it is sampled on the SCLKI but

1 conceptually, at the level of the drawing of
2 Figure 3A, it is sampled on the rising edge of
3 SCLK.

4 MR. STEPHENS: We have been going
5 for almost another hour. Shall we take a
6 break?

7 THE WITNESS: Sure.

8 (Recess taken -- 1:20 p.m.)

9 (After recess -- 1:51 p.m.)

10 BY MR. STEPHENS:

11 Q. Dr. Przybylski, I would like to take
12 a look at the '381 patent descriptions of the
13 paid program operation and the read operation.

14 So, if you would turn to Column 17
15 at Line 5.

16 A. I am there.

17 Q. Well, I guess it is around Line 7,
18 the paragraph that begins, regarding Figure 5A.

19 A. Uh-huh.

20 Q. And the patent reads here that:
21 Regarding Figure 5A, a timing diagram for the
22 Page Program command is illustrated.

1 Do you see that?

2 A. Yes.

3 Q. And the next sentence explains that:

4 Since the embodiment illustrated in Figure 2A
5 utilizes a Serial Data Input and output link
6 structure, prior to beginning to program a page,
7 that program data must first be loaded into a
8 bank page register.

9 Do you see that?

10 A. Yes.

11 Q. Could you give a little context; why
12 would the serial data, data received serially
13 need to be first loaded into a bank page
14 register?

15 A. The nature of these nonvolatile
16 memories is that the programming of a row in a
17 bank happens all at once.

18 So, you need to have the entire row
19 of data preloaded into the page buffers 212
20 and 218, corresponding to the two banks, prior to
21 the start of the program operation.

22 Q. Okay. And so, just continuing in

1 the description of the '381 patent, at line
2 about 12 it explains that this is accomplished
3 with the Serial Data Input command. The Serial
4 Data Input command 502 is comprised of a serial
5 data loading period during which up to a page,
6 e.g., 2, 2112 bytes of data is loaded into the
7 page buffer inserted 212.

8 A. Yes, that would be 2112.

9 Q. You understand that to be a typo?

10 A. Where is the typo?

11 Q. I see 2, comma, and then 2112.

12 A. Oh, yes. There is a typo there.

13 Q. And then: After the process of
14 loading the data register is complete, a page
15 start command 504 is issued to transfer the data
16 from the bank register into the appropriate
17 memory bank.

18 Do you see that?

19 A. Yes.

20 Q. And then finally: Once command 504
21 is issued, the internal write state machine
22 executes an appropriate algorithm and controls

1 timing to program and verify the operation.

2 Do you see that?

3 A. Yes, I see that.

4 Q. So, I guess in this sequence, would
5 you agree that the Serial Data Input command
6 loads data into the page buffer, and only
7 afterward does the Page Program or page start
8 command trigger the internal write machine to
9 actually transfer the data into the memory bank
10 array?

11 A. Transfer and verify, the right --
12 the program operation.

13 Q. And what does the verification
14 involve?

15 A. Unlike DRAMs, flash memory devices
16 are programmed sequentially. In other words, you
17 try and program it, you check how far you have
18 gotten, you program it some more, you check how
19 far you have gotten, and you keep doing that
20 until all of the bits that you are programming
21 verify correctly with the data that you are
22 trying to write, or program into the, that row of

1 the memory bank.

2 Q. And prior to the page program, or
3 page start command 504, the data sitting in the
4 page buffer hasn't yet been written to the memory
5 bank, correct?

6 A. That is correct.

7 Q. Let's take a look at Figure 5B. Do
8 you see the figure?

9 A. I do.

10 Q. So, there is a box input command
11 that will start and then input command 80H,
12 Box 506; do you see that?

13 A. Yes.

14 Q. And do the steps in this flow chart
15 generally track the description in the paragraph
16 that we just read?

17 A. Generally, yeah. I think I don't
18 see any discrepancies, but I haven't looked
19 carefully.

20 Q. At Column 17 --

21 A. There is a typo in Figure 5B.

22 Q. And what is that?

1 A. Block 512 is listed input command
2 but also 506 is input command. Well, okay. So,
3 it is saying that input command 10 as opposed to
4 the name of the command.

5 I would have done it differently.
6 But, fine. It is what it is.

7 Q. Let's look at Column 10, and there
8 is a table, Table 1 which provides a command set?

9 A. Yeah.

10 Q. Okay. And we see the command OP
11 code 10H is the base program command?

12 A. Yes.

13 Q. And 80H is the serial data input
14 command, correct?

15 A. So the confusion was that the first
16 one is labeled input command, which could be
17 misinterpreted to mean Serial Data Input command.
18 Whereas, it actually means just give a command.
19 So, that is why it is -- that figure is a little
20 bit confusing.

21 Q. One moment. I lost track of one of
22 my citations, so I want to direct you to a

1 particular area of the specification.

2 Column 17 Line 31. Do you see that?

3 A. I am there.

4 Q. And the first sentence reads:

5 Moreover 5B shows a simplified flow chart

6 paralleling the operation of the Page Program

7 command and the timing diagram of Figure 5A.

8 Do you see that?

9 A. Yes, I see those words.

10 Q. So, all of the steps that we just
11 looked at in Figure 5B, 506, 508, 510 and 512 are
12 shown within a single flow chart that is titled
13 or described as a simplified flow chart
14 paralleling the operation of a Page Program
15 command; is that correct?

16 A. That is what it says.

17 Q. So, the operation of the Page
18 Program command here begins at step 506 in
19 Figure 5B, with the input command 80H and
20 continues through the subsequent address data
21 loading and program trigger steps, correct?

22 A. Yes. Uh-huh. Sorry. Yes.

1 Q. And in Table 1, we were just looking
2 at, there is also a Page Read command, correct?

3 A. Yes.

4 Q. And the associated OP code for the
5 Page Read is 00H, correct?

6 A. Let me go back to that. Page Read
7 is 00H, 00X. H stands for hex.

8 Q. Column 14 at Line 11, do you see
9 that the patent is: Moreover, Figure 3B shows a
10 simplified flow chart paralleling the operation
11 of the Page Read memory command 314 in the timing
12 diagram at Figure 3A?

13 A. Those are the words of Column 14,
14 yes.

15 Q. So, let's look at Figure 3B?

16 A. Okay.

17 Q. And, the flow chart includes a
18 sequence of steps that begins with the read
19 command 00H at 324 and continues through read
20 data 334 plus ECC generation verified, and
21 verified ECC. Correct?

22 A. That is what is shown in Figure 3B,

1 yes.

2 Q. So, the Page Read operation shown in
3 Figure 3B starts with that read command 00H and
4 continues through each of those subsequent steps
5 until the read is completed, correct?

6 A. That is what is shown in Figure 3B,
7 yes.

8 Q. Let's look at Figure 8B.

9 A. 8B. I am there.

10 Q. That timing diagram is shown in
11 Figure 8B, correct?

12 A. Yes.

13 Q. And I apologize for continuing to
14 jump all throughout this document.

15 But, if we turn to Column 19 just to
16 set the -- some context for what is shown in
17 Figure 8B, Column 19, Line 30.

18 A. Let me look at 8B just for another
19 moment before we jump.

20 Q. Sure.

21 A. Okay. Column 19 you said. Okay. I
22 am on 19.

1 Q. Around Line 30. Sorry, Line 50, the
2 paragraph begins with, furthermore.

3 A. I see it.

4 Q. So: Furthermore, according to
5 various aspects of the invention, Figure 8B
6 illustrates a timing diagram of a Page Read
7 command 810 and a Page Program command 812.

8 Do you see that?

9 A. Yes, continuing: Directed at
10 different memory banks in a memory device 200.

11 Q. Yes. And the next sentence refers
12 to a read operation, Page Read, 810, is being
13 performed in one of the plurality of memory banks
14 through the serial data link interface 230.

15 Do you see that?

16 A. Yes, I see that.

17 Q. Meanwhile, simultaneously, a write
18 operation, Page Program 812, is being performed
19 in this another of the plurality of memory banks.

20 Do you see that?

21 A. Yes, I do.

22 Q. All right. So, going back to

1 Figure 8B, we can see in Figure 8B on the serial
2 input port or SIP0 waveform, the Page Read
3 operation 810 beginning with CMD 00H, correct?

4 A. Yes, that is what it shows in
5 Figure 8B on the SIP0 bus.

6 Q. And then, we also see on the SIP1
7 bus, the Page Program operation beginning at CMD
8 80H in that waveform, correct?

9 A. Yes, that is correct.

10 Q. And do the various commands and data
11 shown in SIP0 for the Page Read operation, do
12 those correspond to the sequence of actions shown
13 in Figure 3B?

14 A. Where in the text that we looked at,
15 it is called 19; is that right?

16 Q. We have looked at some disclosure in
17 Column 19.

18 A. Where the description, yeah, 8B is
19 there.

20 There are similarities between the
21 disclosure of Figure 8B and the disclosure of
22 Figure 3B, I guess it was. But they are not

1 100 percent aligned. There are aspects in 3B
2 that are not disclosed or described at all in
3 connection with the disclosure of Figure 8B.

4 Q. And then, as to the Page Program 812
5 shown on the SIP1 line, we see command 80H which
6 was in Table 1, the serial data input command,
7 correct?

8 A. That is what Table 1 says, yes. Let
9 me double-check that. Table 1, 10 is Page
10 Program, is that what you are asking?

11 Q. Correct, yes.

12 A. Yes, that is Table 1's content, yes.

13 Q. And, the Page Program command is
14 signified by 10H in Table 1, correct?

15 A. 10 hex, yes.

16 Q. Okay. So, again, going back to
17 Figure 8B.

18 A. 8B, yes.

19 Q. And the SIP1 waveform we see the CMD
20 10H command, correct?

21 A. Yes. Are you done?

22 Q. I am done. Do you see that?

1 A. Yes, I do see that.

2 Q. So, before that command is issued,
3 the input data has not yet been written to the
4 memory array, correct?

5 A. In this embodiment, that is true.

6 Q. And the input data is, instead, held
7 in a buffer before the command is issued; is that
8 correct?

9 A. I believe that there is disclosure
10 to that effect within the specification. But, I
11 don't know exactly where it is. Is it -- we
12 discussed that earlier before lunch.

13 Q. We have, yes. I will take into
14 consideration our earlier discussion with respect
15 to that.

16 A. So, to the extent that the
17 embodiment of Figure 8B is the same as what we
18 were -- the same embodiment as we were discussing
19 previously with regard to program commands, that
20 would be true.

21 Q. And then on the SOP0 line on, in
22 Figure 8B, we see output data that commences some

1 time at -- by the time TR after the data is
2 received on the SIP0 line, correct?

3 A. Yes, it shows that there was a
4 temporal delay between the two.

5 Q. And what is that temporal delay a
6 result of?

7 A. Well, let's see if the patent
8 actually says what TR is in 8, in the first
9 instance of TR is expected to show up in -- oh,
10 that is a program, TR Figure 4 has a TR. So,
11 let's look at -- for Figure 4.

12 I am not finding a specific
13 reference that explains what TR is. But, it --
14 presumably is just -- it is the time that it
15 takes to complete that command. But again, I
16 don't know that for sure. There may be other
17 components to it.

18 Q. You mentioned that a verification
19 would take place as part of the Page Read
20 operation?

21 A. We talked about verification as part
22 of a program operation, not as a Page Read

1 operation. There are other things that need to
2 happen in conjunction to a Page Read.

3 But again, the patent doesn't
4 describe the components of T sub-R, it only shows
5 it in the figures, and so we don't know exactly
6 what the inventors had in mind for the event that
7 make up TR.

8 Q. Thank you for the clarification.

9 I actually was -- I should have said
10 there is ECC generation and verification of the
11 ECC for a Page Read operation shown in Figure 3B,
12 correct?

13 A. Yes. But, Figure 3B does not
14 indicate where that happens. 3B, let's go back
15 to 3B.

16 So, this is described in Column 16
17 to some extent with regard to 3A and the read
18 operation.

19 Q. Which line you are looking at?

20 A. 16, Line 43, starting: The output
21 data is provided in step 334 which is before the
22 ECC check in 3B.

1 So, the temporal relationship
2 between the ECC verification and the delivering
3 of the data is not clear at this level of
4 analysis. I would have to read everything much
5 more carefully to see. It does say that the ECC
6 hardware is not shown in the figures, but is
7 presumably in the memory device which is
8 uncommon. Well, no, not uncommon.

9 So, but, figure -- the text of
10 Column 16 is a little bit inconsistent with
11 Figure 3B. But it is what it is.

12 Q. I'm sorry, and in what way do you
13 see an inconsistency between the text and the
14 figure?

15 A. Box 334 in Figure 3 is called Read
16 Data and that is before the ECC check.

17 Q. Uh-huh.

18 A. So, that means that the 334 is
19 shown. It is described in Column 16 as being
20 delivering the data to the outside world, which
21 means the deli -- data is delivered before. In
22 this embodiment in this particular device, the

1 error correction happens after the data is
2 delivered to the outside world.

3 Q. Uh-huh.

4 A. And that is highly unusual. That is
5 not clear how -- what is going to happen if there
6 is an error, how is that communicated that back
7 to the memory controller, et cetera. And if the
8 -- if the ECC is being -- ECC error is being
9 corrected on-die in the memory device, how as
10 indicated by Figure 3B. Let's see. 3B shows --
11 that is reclaim error, presumably reclaim error
12 means correct the error, but how that corrected
13 error is transmitted upstream is not clear, given
14 that the data has already been delivered off-die.
15 So, there is some ambiguity here with regard to
16 the whole question of ECC and the sequences of
17 events.

18 Q. The description when the read data
19 step in 334 in Figure 3B refers to outputting the
20 data to the outside role?

21 A. Well, as I read in Column 16, that
22 seems to be the case. But again, we are picking

1 and choosing little paragraphs out of a long
2 specification. There may be other disclosures
3 here that I am not familiar with that fully
4 describe the sequence. But, reading from
5 Column 16, Line 42, the output data is provided
6 in step 334 through the link interface 230, out
7 of the memory device.

8 So, the data is output in 334 and
9 then you check it with the ECC detection
10 circuitry, which is a little bit odd.

11 Q. Is it fair to say that the read data
12 step 334 from Figure 3B corresponds to the output
13 data that is shown in Figure 8B on the SOP0 line
14 or bus?

15 A. It is plausible. Again there may be
16 additional disclosure within this long
17 specification that clarifies that one way or
18 another.

19 There is no reference to Figure 8 in
20 this paragraph on Column 16 that is describing
21 how a read operation happens.

22 So, it seems that way but I do not

1 know for sure.

2 Q. You are not aware of any
3 inconsistent disclosure or, I should say
4 disclosure that would suggest that the read step
5 is anything other than outputting the data from
6 the memory device, correct?

7 A. Again, I'm not aware of any such
8 disclosure. But again, this is a long
9 specification. I have not read it recently. We
10 have not taken the time to read it all now. We
11 are jumping around all over the place within it.
12 I'm -- I can't say for sure what is or is not the
13 read operation.

14 There seems to be some issues in it.
15 There is some minor issues in some of the
16 figures. You know, until I would have the
17 opportunity to study the specification in detail,
18 you can't be certain of exactly what is going on.
19 There is uncertainty.

20 Q. In Figure 8B, though, what is shown
21 here is that the read data or the output data on
22 SOP0 begins transmission before the command 10H

1 is issued, correct?

2 A. Looking just at Figure 8B, it does
3 show that output data happens before the arrival
4 of command 10H on SIP1.

5 Q. And so the output data then begins
6 being output by the memory device before the
7 memory device begins writing the input data to
8 the memory bank array, correct?

9 A. Again looking just at Figure 8B, it
10 does appear to be the case that tPROG, which
11 would reasonably be the programming operation
12 time, begins before the conclusion of the output
13 data operation on SOP0.

14 Q. And Figure 8B is showing an overlap
15 in the Page Read and Page Program operation,
16 correct? Temporal overlap, I should say.

17 A. I'm sorry, I lost focus for a
18 second. Please repeat the question.

19 Q. Figure 8B in the '381 patent depicts
20 a temporal overlap in the Page Read 810 and the
21 Page Program 812, correct?

22 A. That is certainly consistent with

1 how it is described in the list of figures which
2 is -- it illustrates the timing diagrams for
3 concurrent memory operations.

4 So, yes, that is consistent with the
5 description of it and the overlapping of the data
6 output and the data input, and the data output
7 and the beginning of the program operation.

8 MR. STEPHENS: Could we take 5
9 minutes?

10 (Recess taken -- 2:34 p.m.)

11 (After recess -- 2:42 p.m.)

12 BY MR. STEPHENS:

13 Q. Dr. Przybylski, we talked earlier
14 about your prior work with MOSAID. Do you recall
15 that discussion?

16 A. Yes.

17 Q. And, we noted that a number of
18 patents that you were identified as a sole
19 inventor, or a co-inventor on a number of MOSAID
20 patents, correct?

21 A. Yes.

22 Q. And, most of those patents, if not

1 all, pertain to your work on HLNAND technology,
2 correct?

3 A. Some of them are specifically about
4 -- relating to that work. There are some that
5 are relating to discussions and work that I did
6 in the context of the technical advisory board,
7 which have very little or nothing to do with
8 HLNAND.

9 Q. Can you describe what HLNAND refers
10 to?

11 A. It was a memory architecture that
12 MOSAID developed, and they developed a few
13 prototype devices that attempted to significantly
14 increase the bandwidth in flash memory systems.

15 Q. And have HLNAND devices been
16 commercialized?

17 A. No. They failed to develop any
18 significant interest in, amongst the
19 semiconductor manufacturers to commercialize the
20 device. It, I -- I don't remember the details.
21 They may have gotten some traction. But,
22 ultimately there were no systems that dev --

1 designed it and it failed.

2 Q. Does the '381 patent disclose any
3 aspects of HLNAND technology?

4 A. I don't remember very much about the
5 details of the HLNAND architecture. So, I can't
6 say.

7 Q. You don't have an opinion as to
8 whether the '381 patent relates to HLNAND
9 technology?

10 A. Well, they are both relating to
11 flash memory and so that is a commonality.

12 But, beyond that, I have very little
13 memory of the details of the HLNAND architecture.
14 I haven't reviewed any of those patents or any of
15 the other disclosures that may, or may have been
16 made by MOSAID in that time frame.

17 Q. Is it possible that the '381 patent
18 relates to HLNAND technology?

19 A. Again, I have no recollection. So,
20 it may be possible, it may not be possible. I
21 don't know.

22 Q. Is it possible that there would be

1 any overlapping description between the '381
2 patent and any of the MOSAID patents or
3 applications on which you were a named inventor?

4 A. I don't know. I haven't looked at
5 those other patents in decades. So, I can't say.

6 Q. What were some of the characteristic
7 aspects of HLNAND technology?

8 A. As I have indicated, what I remember
9 is that it was an attempt to significantly
10 increase the bandwidth of flash memory devices.
11 And that is about all that I remember of it.

12 Q. Do you recall if any of the patents
13 or applications that you have filed on, or that
14 MOSAID filed with you as the inventor or
15 co-inventor, use the term HLNAND?

16 A. Again, I haven't reviewed those
17 patents in decades. I don't know whether the
18 word HLNAND exists in any of them.

19 Q. Do you recall if there was any
20 nonpatent publications from MOSAID relating to
21 the HLNAND architecture?

22 A. Yes, they did publish some papers,

1 conference papers, I believe, in their efforts to
2 get it adopted as a commercial architecture.

3 Q. To the best of your recollection,
4 when would the time frame of those conference
5 papers have been?

6 A. In the middle portion of the 20 --
7 of the naughts, yeah. Right.

8 Q. All right. I would like to turn to
9 the Grundy prior art reference.

10 A. All right. Let's see. I'm looking
11 at the downloaded version of Grundy that you have
12 previously put in the Chat.

13 Q. Let's take a look at Figure 5A.

14 A. I am looking at Figure 5A.

15 Q. So, Figure 5A there is a single
16 memory controller 151 and a series of memory
17 devices, 155-1 through 155-8, correct?

18 A. That is what is shown in Figure 5A,
19 yes.

20 Q. And between the memory
21 controller 151 and the first memory device 155-1,
22 we can see a number of lines 152, 154, 156,

1 and 158, correct?

2 A. Correct.

3 Q. Can we refer to that as the bus?

4 A. You want -- so, the bus you want to
5 be all of them, not just the data portion?

6 Q. What would you typically refer to,
7 use the term bus for?

8 A. You can use the bus for any
9 collection of wires that have some commonality to
10 them, either temporal or functional.

11 Q. Yeah. For purposes of our
12 discussion, let's just consider the bus to
13 encompass each of these lines, not just the data
14 lines but 152 through 158.

15 A. So, 153 is the bus.

16 Q. That's correct.

17 A. Okay. I will conform to your
18 definition.

19 Q. In Figure 6, we see a set of
20 waveforms, two sets of waveforms, I should say.
21 At the top is a -- are the waveforms that are
22 output on the bus by the memory controller to the

1 first memory device.

2 Is that your understanding?

3 A. That is what it means when it says
4 from controller in the -- beside the brace on the
5 left-hand side of the figure, and top half of the
6 figure.

7 Q. And, the second set of waveforms are
8 the waveforms provided on the bus from the first
9 memory device to the second memory device.

10 Would you agree that is a fair
11 characterization?

12 A. Let's see what the specification
13 actually says. I should read the specification
14 and look at the figure at the same time, but we
15 will get there. So, 172-2 is the critical one,
16 172-2, following edge.

17 Yes, in Paragraph 48 it makes clear
18 that the signals with the subscript 2 are
19 retransmitted by the memory device 155 and can --
20 so, it is between 155-1 and 155-2 of Figure 6, of
21 Figure 5A. Yes.

22 Q. Grundy uses the term, point-to-point

1 link 153, to refer to the collection of lines
2 that I had earlier characterized as a bus,
3 correct?

4 A. Paragraph 47, yes. It says:
5 Point-to-point link 153 and it uses
6 point-to-point 153 numerous times.

7 Q. What is a point-to-point link?

8 A. Generally speaking, it is a term of
9 art that refers to a communication between a
10 single source and a single destination.

11 It could be bi-directional, but it
12 is typically uni-directional from one to the
13 other.

14 Q. In Figure 5A, is the point-to-point
15 link 153 uni-directional?

16 A. Yes, the arrows on each of the
17 signal lines 152, 154, 156, 158, all have a
18 single arrow on one end of them indicating the
19 uni-directional aspect of each of them.

20 Q. As shown in Figure 6, each of the
21 output ports for clock bus valid and command on
22 the memory controller drives signals on the

1 point-to-point link 153 concurrently, correct?

2 A. Yes. The timing diagrams show that
3 each point in time the driven value by -- in the
4 top half by the memory controller at each point
5 in time.

6 Q. And there is a timing relationship
7 between the various signals between the clock,
8 the bus, the valid and command signals, correct?

9 A. Yes. Those are all drawn relative
10 to the same undisclosed timeline along the
11 X-axis.

12 Q. And that timing relationship would
13 be maintained at the input ports of the first
14 memory device 155-1?

15 A. Okay. As I indicate in my
16 declaration in Paragraphs 82 and 83, that these
17 -- the figure shows the timing relationship of
18 these signals at the memory controller, and there
19 is no indication in Grundy that the flight times
20 of these signals would be significantly
21 different.

22 And, that would present a systematic

1 shift in the relative arrival times of signals at
2 the first memory device, or their delay through
3 the input buffers of that memory device.

4 Q. So, you agree that there is no
5 indication in Grundy that the flight times of the
6 signals transmitted by the memory controller to
7 the first memory device would be significantly
8 different from each other, correct?

9 A. That is the essence of my disclosure
10 in Paragraph 83 of my declaration.

11 Q. Likewise, between -- on the
12 point-to-point link 153 between the first memory
13 device and the second memory device in the chain,
14 there is no indication in Grundy that the flight
15 times for the signals there would be
16 significantly different, correct?

17 A. I don't opine about that link. But,
18 consistent with my opinion with regard to the
19 first link, that would be a reasonable conclusion
20 in the absence of a suggestion in Grundy that
21 there is something different going on.

22 Q. You have not cited anything in

1 Grundy suggesting that there would be something
2 different going on, correct?

3 A. Not to my recollection, no.

4 Q. In Figure 17 of Grundy.

5 A. Figure 17. Hold on. Yes, I'm
6 looking at Figure 17.

7 Q. There are a collection of
8 differential receivers, 310, and the input
9 interface, correct?

10 A. Yes, they are referred to as
11 differential receivers in this specification.
12 Well, or just receivers, sometimes.

13 Q. And what is the -- what is the
14 purpose of a differential receiver?

15 A. Differential receivers are sometimes
16 used over single-ended communication because they
17 can be reliably driven at higher frequencies.

18 So, a differential receiver looks at
19 a pair of differential lines, which are in the
20 true and complement form, and uses the pair of
21 them to develop a single-ended version of that
22 input signal.

1 Q. In Paragraph 47 of Grundy?

2 A. 47.

3 Q. Yes.

4 A. Hold on. Yes, I am at 47.

5 Q. The second sentence in Paragraph 47
6 states that although depicted as single-ended
7 waveforms in Figure 6, differential signals are
8 used in the memory system 150 of Figure A, 5A, as
9 discussed single-ended signalling may be used in
10 alternate embodiments. Correct?

11 A. You read that accurately.

12 Q. So, in embodiments that use
13 single-ended signalling, would a POSITA
14 understand that there would be no need for
15 differential receivers in the input interface of
16 the memory device?

17 A. Yes, but it would similarly
18 understand that you need a single-ended receiver
19 just as we saw in the '381 patent over and over
20 again.

21 Q. Like the standard input buffers
22 in '381?

1 A. Not necessarily standard. But, you
2 would need a single-ended receiver of some
3 variety.

4 Q. Can we turn to Paragraph 84 of your
5 declaration?

6 A. Of my declaration, hold on. I am
7 looking at 84.

8 Q. About halfway down the paragraph,
9 you write: But as seen in Figure 29 from
10 JESD79-2, data that is being written to the
11 memory array has the corresponding edges of the
12 differential DQS offset, but a half phase, that
13 is quarter cycle, so that the DQS always
14 transitions in the middle of the data eye on DQ.

15 Did I read that correctly?

16 A. Yes, you did.

17 Q. What is JESD79-2?

18 A. That is the JEDEC standard for DDR2
19 SDRAMs as I mention in the first two sentences of
20 that paragraph.

21 Q. And what was the JEDEC standard that
22 you cited here prior art to the '381 patent?

1 MR. COURTNEY: Objection to the
2 form.

3 THE WITNESS: I note in the second
4 sentence that the JEDEC standard for the DDR2
5 SDRAMs was first published in September of
6 2003.

7 BY MR. STEPHENS:

8 Q. Would that standard have been known
9 to a POSITA as of the critical date?

10 A. Under the model that a POSITA knows
11 everything that has been published, yes.

12 Q. Have you had involvement with JEDEC
13 in your career?

14 A. I have been following JEDEC and its
15 work closely for decades. I have attended a few
16 JEDEC meetings, and I have had conversations with
17 the members that participate as the company
18 representatives from a number of companies quite
19 extensively, in the 1990s and early 2000s.

20 My direct involvement has diminished
21 over the years.

22 Q. Approximately, how many meetings do

1 you think you have attended?

2 A. Two.

3 Q. All within the 1990s?

4 A. In the middle 1990s, yes.

5 Q. Did you ever see anyone, any
6 representatives of MOSAID at the JEDEC meetings?

7 A. As we discussed this morning, Peter
8 Gillingham was MOSAID's principal representative
9 at JEDEC. And whether I saw him at the meetings
10 that I participated in, I have no recollection.
11 Possibly, possibly not, I don't know.

12 Q. Do you recall whether -- or what is
13 the process for attending a meeting? Do you have
14 to become a member, pay a fee, just show up?

15 A. So, the JEDEC is an organization of
16 member companies. So, companies are members and
17 companies send representatives to meetings.

18 In my case, I was the guest of a
19 client that I was working with at the time.

20 Q. That client was not MOSAID?

21 A. No.

22 Q. Were you involved with any

1 particular committees in JEDEC?

2 A. No. I mean, I attended two meetings
3 but I didn't really participate as the
4 representative. The formal representative for my
5 client was the one that, if there was something
6 to be said, would say it. And -- but, I'm not
7 sure that they had anything to contribute in
8 those meetings. I don't remember.

9 Certainly, it was not up to me to
10 say anything instructive in one of those
11 meetings. I was more of an observer.

12 Q. Do you know what JEDEC standards are
13 available to the public or just to the
14 membership?

15 A. During development, they are only
16 available to the members. After they are
17 ratified by JEDEC and JESD, then they are
18 published, sometimes for a fee and sometimes for
19 free.

20 MR. STEPHENS: Could we take a
21 5-minute break?

22 (Recess taken -- 3:13 p.m.)

1 (After recess -- 3:19 p.m.)

2 BY MR. STEPHENS:

3 Q. Just a few last questions,
4 Dr. Przybylski.

5 In preparing the opinion in your
6 declaration, did you run any simulations of
7 Grundy's memory circuits?

8 A. No. There was no need to run any
9 simulations to form my opinions, as articulated
10 in my declaration.

11 Q. Did you build any prototypes of
12 Grundy's circuit?

13 A. Similarly, there was no need to
14 form, build any prototypes in order to form my
15 opinions that are articulated in my declaration.

16 Q. Did you run any simulations of
17 Kilbuck's circuits?

18 A. Similarly, those -- Kilbuck speaks
19 for itself and there was no need to run any
20 simulations of the disclosures of Kilbuck in
21 order to form my opinions.

22 Q. All right. Did you construct any

1 prototypes of Kilbuck's circuits?

2 A. As with Grundy, there was no need to
3 form, to construct any prototypes of Kilbuck's
4 specification in order to form my opinions which
5 were based on the disclosure of the documents as
6 articulated in my declaration.

7 Q. And, did you run any simulations of
8 the Grundy-Kilbuck combination?

9 A. Well, there was no single
10 Grundy-Kilbuck combination articulated in the
11 specification. So, that would not have been
12 possible.

13 Q. Did you perform any calculations on
14 propagation delays in Grundy's circuits?

15 A. Again, there was no need to form any
16 specific propagation delay calculations because
17 the dis -- the specification was abstract away
18 from any specific process, technologies or
19 operating frequencies.

20 And so, my opinions were formed
21 based on the disclosure as it existed in Grundy.

22 MR. STEPHENS: No further questions.

1 MR. COURTNEY: Okay.

2 Dr. Przybylski, I don't have any questions
3 myself. So, I think we might be done.

4 THE WITNESS: Very good.

5 (Off record -- 3:22 p.m.)

6 (Whereupon signature having not been waived, the
7 deposition concluded at 3:22 p.m.)

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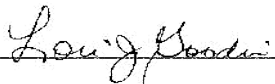
22

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2

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4 CA CSR # 13959 the Notary for this proceeding, do
5 hereby certify that the witness whose testimony
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7 me; that I am neither Counsel for, related to,
8 nor employed by any of the parties to the action
9 in which this deposition was taken; and, further,
10 that I am not a relative or employee of any
11 attorney or Counsel employed by the parties
12 hereto, or financially or otherwise interested
13 in the outcome of this action.

14



15

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16

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18 Notary Commission Number: GG987804

My Commission expires: May 12, 2028

19

STATE OF CALIFORNIA, CA CSR# 13959

20 My Commission expires: February 22, 2027

21 DISTRICT OF COLUMBIA, WASHINGTON DC

My Commission expires: June 1, 2031

22

1 Case: Infineon Technologies Americas Corp. vs Mosaid Technologies Inc.

2 Witness Name: Steven Przybylski, Ph.D.

3 Deposition Date: 08/07/2026

4

5

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8 I do hereby acknowledge that I have read

9 and examined the foregoing pages

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11 (Check appropriate box):

12 () The same is a true, correct and

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14 me to the questions therein recorded.

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16 attached Errata Sheet, the same is a true,

17 correct and complete transcription of the

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1 Errata Sheet

2 NAME OF CASE: Infineon Technologies Americas Corp. vs Mosaid Technologies Inc.

3 DATE OF DEPOSITION: 08/07/2026

4 NAME OF WITNESS: Steven Przybylski, Ph.D.

5 Reason Codes: 1. To clarify the record.

6 2. To conform to the facts.

7 3. To correct transcription errors.

8 Page ____ Line ____ Reason ____

9 From _____ to _____

10 Page ____ Line ____ Reason ____

11 From _____ to _____

12 Page ____ Line ____ Reason ____

13 From _____ to _____

14 Page ____ Line ____ Reason ____

15 From _____ to _____

16 Page ____ Line ____ Reason ____

17 From _____ to _____

18 Page ____ Line ____ Reason ____

19 From _____ to _____

20

21 _____

22 STEVEN PRZYBYLSKI, PH.D.

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