

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INFINEON TECHNOLOGIES AMERICAS CORP.,  
Infineon,

v.

MOSAID TECHNOLOGIES INC.,  
Patent Owner.

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Case IPR2025-01487  
Patent 9,972,381

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**PETITIONER'S REPLY TO PATENT OWNER'S RESPONSE**

**TABLE OF CONTENTS**

|      |                                                                                                                                                                      |    |
|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| I.   | INTRODUCTION .....                                                                                                                                                   | 1  |
| II.  | THE PETITION’S GRUNDY-KILBUCK COMBINATION IS WELL SUPPORTED AND UNREFUTED.....                                                                                       | 2  |
|      | A. The Grundy-Kilbuck Combination is Structurally Sound and Clearly Defined; MOSAID Fails to Refute It.....                                                          | 2  |
|      | B. Precedent Expressly Supports the Petition’s Alternative Mappings on Flash Memory, Mooting MOSAID’s Critique.....                                                  | 7  |
|      | C. The Petition’s Mappings Consistently Rely on Grundy’s Memory Device, Supplemented by Kilbuck’s Conventional Flash Features.....                                   | 8  |
|      | D. The Petition’s Clear, Evidence-Backed Motivation Analysis Forecloses MOSAID’s Hindsight Defense .....                                                             | 10 |
|      | E. The Petition Establishes a Reasonable Expectation of Success That MOSAID Fails to Credibly Rebut.....                                                             | 12 |
| III. | THE PETITION’S OBVIOUSNESS CASE ON CLAIM 2 IS CONSISTENT, CLEAR, AND FACTUALLY CORRECT .....                                                                         | 13 |
|      | A. Claim 2 Narrows “Command Data” and the Petition Follows Suit....                                                                                                  | 14 |
|      | B. MOSAID Mischaracterizes the Petition’s Reliance on Grundy’s Figure 6 Timing Diagram.....                                                                          | 15 |
|      | C. Buffering Does Not Create a New Clock Signal: MOSAID’s Alleged Distinction Between Grundy and Claim 2 Is Illusory .....                                           | 17 |
| IV.  | GRUNDY’S CLOCK OUTPUT SIGNAL SATISFIES PETITIONER’S CONSTRUCTION (CLAIMS 4, 5, 19) .....                                                                             | 20 |
| V.   | GRUNDY-KILBUCK’S OVERLAPPING READ AND PROGRAM OPERATIONS SATISFY CLAIMS 13 AND 21 .....                                                                              | 22 |
|      | A. The Petition’s Mappings for Dependent Claims 13/21 Align Fully With Their Corresponding Independent Claims 1/17, Creating No Structural or Logical Conflict ..... | 22 |
|      | B. Applying Kilbuck’s Teaching of Multiple Flash Memories to Grundy Predictably Yields the Claimed Overlapping Operations .....                                      | 26 |

|    |                                                                                                                            |    |
|----|----------------------------------------------------------------------------------------------------------------------------|----|
| C. | MOSAID's Unfounded Complaints Leave the Petition's Explicit and Compelling Motivation-to-Combine Analysis Unanswered ..... | 29 |
|----|----------------------------------------------------------------------------------------------------------------------------|----|

**LIST OF EXHIBITS**

|                               |                                                                                                                                                                                                                                                                                                 |
|-------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INFINEON-1001                 | U.S. Patent 9,972,381 (the “381 Patent”)                                                                                                                                                                                                                                                        |
| INFINEON-1002                 | U.S. Patent 9,972,381 File History                                                                                                                                                                                                                                                              |
| INFINEON-1003                 | Expert Declaration of Dr. Carl Sechen                                                                                                                                                                                                                                                           |
| INFINEON-1004                 | Curriculum Vitae of Dr. Carl Sechen                                                                                                                                                                                                                                                             |
| INFINEON-1005                 | U.S. Patent App. Pub. 2004/0148482 to Grundy et al.<br>(“Grundy”)                                                                                                                                                                                                                               |
| INFINEON-1006                 | U.S. Patent App. Pub. 2005/0204091 to Kilbuck et al.<br>(“Kilbuck”)                                                                                                                                                                                                                             |
| INFINEON-1007                 | Wiley Electrical and Electronics Engineering Dictionary,<br>2004 (excerpts)                                                                                                                                                                                                                     |
| INFINEON-1008                 | T. Tanaka <i>et al.</i> , “A quick intelligent page-programming<br>architecture and a shielded bitline sensing method for 3 V-<br>only NAND flash memory,” in <i>IEEE Journal of Solid-State<br/> Circuits</i> , vol. 29, no. 11, pp. 1366-1373, Nov. 1994, doi:<br>10.1109/4.328638 (“Tanaka”) |
| INFINEON-1009                 | P. Cappalletti <i>et al.</i> , “Flash Memories,” Kluwer Academic<br>Publishers, 1999 (excerpts) (“Cappalletti”)                                                                                                                                                                                 |
| INFINEON-1010                 | Complaint, <i>Mosaid Techs. Inc. v. Infineon Techs. AG et al.</i> ,<br>W.D. Tex., filed March 25, 2025                                                                                                                                                                                          |
| INFINEON-1011                 | September 24, 2025 Stipulation                                                                                                                                                                                                                                                                  |
| INFINEON-1012                 | Voluntary Search Disclosure Declaration                                                                                                                                                                                                                                                         |
| INFINEON-1013 — INFINEON-1033 | RESERVED                                                                                                                                                                                                                                                                                        |

|               |                                                                                                                                                                                                                                                                                                        |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| INFINEON-1034 | Manual of Patent Examining Procedure, Chapter 600, Ninth Edition, Rev.08.2017                                                                                                                                                                                                                          |
| INFINEON-1035 | Manual of Patent Examining Procedure, Chapter 700, Ninth Edition, Rev.08.2017                                                                                                                                                                                                                          |
| INFINEON-1036 | Manual of Patent Examining Procedure, Chapter 900, Ninth Edition, Rev.08.2017                                                                                                                                                                                                                          |
| INFINEON-1037 | U.S. Patent App. Pub. 2012/0226929                                                                                                                                                                                                                                                                     |
| INFINEON-1038 | “Patent Public Search - Advanced Search overview,”<br>retrieved from <a href="https://www.uspto.gov/sites/default/files/documents/Advanced-search-overview-QRG-Patent-Public-Search.pdf">https://www.uspto.gov/sites/default/files/documents/Advanced-search-overview-QRG-Patent-Public-Search.pdf</a> |
| INFINEON-1039 | <a href="https://web.archive.org/web/20151028000601/https://www.uspto.gov/video/cbt/section2/index.htm">https://web.archive.org/web/20151028000601/https://www.uspto.gov/video/cbt/section2/index.htm</a> (slide 14)                                                                                   |
| INFINEON-1040 | U.S. Patent 8,654,601                                                                                                                                                                                                                                                                                  |
| INFINEON-1041 | Micron DDR SDRAM Unbuffered DIMM datasheet 2004.                                                                                                                                                                                                                                                       |
| INFINEON-1042 | Docket Navigator, Time to Milestones, Judge Alan D. Albright (generated September 20, 2025)                                                                                                                                                                                                            |
| INFINEON-1043 | Excerpts from LegalMetric District Report, Texas Western District Court, in Patent Cases (January 2000-July 2025)                                                                                                                                                                                      |
| INFINEON-1044 | <i>Neonode Smartphone LLC, v. Samsung Elecs. Co. Ltd.</i> , 6:20-cv-00507-ADA, Document 70 (WDTX Mar. 22, 2023)                                                                                                                                                                                        |
| INFINEON-1045 | <i>Viasat, Inc. v. Kioxia Corp.</i> , 6:21-cv-01231-ADA, Document 242 (WDTX Oct. 17, 2024)                                                                                                                                                                                                             |

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| INFINEON-1046 | Declaration of Terence P. Woodsome (CONFIDENTIAL - ATTORNEYS' EYES ONLY)                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| INFINEON-1047 | Infineon Stipulations in IPR2025-01171, IPR2025-01456, and IPR2025-01489                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| INFINEON-1048 | Email dated September 19, 2025, Subject: "Efficiency Proposal re MOSAID v. Infineon"                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| INFINEON-1049 | Press Release: Department of Justice, Federal Trade Commission to Hold Workshop on Patent Assertion Entity Activities, Archives, U.S. Department of Justice, <a href="https://www.justice.gov/archives/opa/pr/departement-justice-federal-trade-commission-hold-workshop-patent-assertion-entity-activities">https://www.justice.gov/archives/opa/pr/departement-justice-federal-trade-commission-hold-workshop-patent-assertion-entity-activities</a> (accessed October 5, 2025)                                                                    |
| INFINEON-1050 | Canadian Patents Database, Search Results, Query: "current-owner:(MOSAID) AND (current-status:Patents)," <a href="https://www.ic.gc.ca/opic-cipo/cpd/eng/search/results.html?query=current-owner%3A%28MOSAID%29+AND+%28current-status%3APatents%29&amp;start=1&amp;num=10&amp;type=advanced_search&amp;newSearch=0">https://www.ic.gc.ca/opic-cipo/cpd/eng/search/results.html?query=current-owner%3A%28MOSAID%29+AND+%28current-status%3APatents%29&amp;start=1&amp;num=10&amp;type=advanced_search&amp;newSearch=0</a> (generated October 5, 2025) |
| INFINEON-1051 | MOSAID Technologies Website, Patent Licensing page, <a href="https://mosaid.com/patent-category/semiconductor-process-portfolio/">https://mosaid.com/patent-category/semiconductor-process-portfolio/</a> (accessed October 5, 2025)                                                                                                                                                                                                                                                                                                                 |
| INFINEON-1052 | United States-Canada Income Tax Convention                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| INFINEON-1053 | U.S. Patent 10,224,098                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| INFINEON-1054 | U.S. Patent 10,679,695                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| INFINEON-1055 | U.S. Patent 11,017,849                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

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|---------------|------------------------------------------------------------------------------------------------------------------------------------------|
| INFINEON-1056 | <i>MOSAID Technologies v. Freescale Semiconductor, Inc. et al.</i> , 6:11-cv-00173-LED, Document 91 (EDTX October 13, 2011)              |
| INFINEON-1057 | <i>MOSAID Technologies v. Freescale Semiconductor, Inc. et al.</i> , 6:11-cv-00173-LED, Document 100 (EDTX November 17, 2011)            |
| INFINEON-1058 | Declaration of Dr. Martin Bayerl (CONFIDENTIAL - ATTORNEYS' EYES ONLY)                                                                   |
| INFINEON-1059 | Complaint in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , Case No. 1:25-cv-00358 (WDTX March 10, 2025)          |
| INFINEON-1060 | Reply Declaration of Dr. Carl Sechen                                                                                                     |
| INFINEON-1061 | Deposition Transcript of Dr. Przybylski                                                                                                  |
| INFINEON-1062 | David A. Patterson & John L. Hennessy, <i>Computer Organization and Design: The Hardware/Software Interface</i> (2d ed. 1997) (excerpts) |
| INFINEON-1063 | John P. Uyemura, <i>CMOS Logic Circuit Design</i> (1999) (excerpts)                                                                      |
| INFINEON-1064 | Neil H.E. Weste & David Harris, <i>CMOS VLSI Design: A Circuits and Systems Perspective</i> (3d ed. 2005) (excerpts)                     |
| INFINEON-1065 | U.S. Patent 5,245,572                                                                                                                    |

*\*All emphasis is added in this brief.*

## **I. INTRODUCTION**

Unable to defend the '381 Patent directly on the merits, MOSAID tries to sidestep the Petition's combination of Grundy and Kilbuck. MOSAID makes hardly any attempt to explain what features are allegedly missing from these references or why a skilled artisan would not have been motivated to combine them. Instead, MOSAID spends most of its brief claiming it cannot understand the Grundy-Kilbuck combination or follow the Petition's mappings. But the Petition is clear, and MOSAID's head-in-the-sand approach is not a credible response.

Even when it dabbles in the merits, MOSAID still fails to persuade. The law refutes MOSAID's position that the Petition should have addressed every possible detail necessary to build a real-world flash memory device from the Grundy-Kilbuck combination. *KSR*'s flexible obviousness test does not require the kind of fastidious blueprints that MOSAID demands, particularly as to details that are not in the claims and that the '381 Patent itself fails to teach.

Because Infineon's Petition conclusively proves obviousness based on the combined teachings of Grundy and Kilbuck, and MOSAID has failed to show otherwise, the '381 Patent's claims must be found unpatentable.

## **II. THE PETITION’S GRUNDY-KILBUCK COMBINATION IS WELL SUPPORTED AND UNREFUTED**

The Grundy-Kilbuck combination is well supported by record evidence and established principles of obviousness law. The Petition starts with Grundy, a reference that identifies “flash EEPROM” as a suitable storage medium for its memory device. Pet., 9-10, 14 (citing INFINEON-1005, [0035], [0062]). Next, the Petition explains that the sparsity of Grundy’s flash EEPROM disclosure would have inspired a POSITA to pursue other prior art references that describe known features of flash memory circuits in greater depth, such as Kilbuck. Pet., 14-16. The combination thus follows the familiar pattern under *KSR* in which a secondary reference (Kilbuck) supplies a “predictable solution” to a clear “design need” of the primary reference (Grundy). *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 405 (2007); *see also In re Translogic Tech., Inc.*, 504 F.3d 1249, 1262 (Fed. Cir. 2007) (upholding a combination where one reference disclosed “2:1 multiplexers” and another disclosed “a well-known circuit” for implementing them).

### **A. The Grundy-Kilbuck Combination is Structurally Sound and Clearly Defined; MOSAID Fails to Refute It**

Even setting aside its flawed legal premise that the combination must yield “a single, coherent ‘Grundy-Kilbuck’ device” (POR, 1, 4-8), MOSAID’s argument necessarily fails because it mischaracterizes the Petition.

The Petition maps the claimed “flash memory device” to the flash version of Grundy’s memory device equipped with internal flash-memory features from Kilbuck. Pet., 17-18; INFINEON-1005, [0035], [0084]-[0085], Figures 17, 19; INFINEON-1003, ¶¶57-67. In the combination, Kilbuck simply supplies teachings regarding conventional flash features, such as erasable blocks, pages, and cells; NAND/NOR architectures; a status register; error correction codes; and program-verification capabilities. Pet., 13-17, 20-22, 41-42, 59-62, 73-75; INFINEON-1006, [0004], [0024]-[0034]; INFINEON-1003, ¶¶57-64.

This is not, as MOSAID suggests, an exercise in grafting disparate technology onto Grundy. Grundy itself describes the option of implementing its storage arrays as flash EEPROM, a type of flash memory. INFINEON-1005, [0035], [0062]; Pet., 18; INFINEON-1003, ¶49; INFINEON-1007, p. 288. The combination simply answers Grundy’s call for flash EEPROM with conventional features of flash memory taught by Kilbuck. *See In re Translogic*, 504 F.3d at 1262; INFINEON-1003, ¶58. In short, the combination entails the following:

- Grundy’s signaling interface for receiving commands, addresses, and data;
- Grundy’s control circuitry, augmented by Kilbuck’s conventional flash features, for performing the page-program and read operations on a flash array; and

- Grundy’s status mechanism, with Kilbuck’s register, for reporting device status.

Pet., 13-42; INFINEON-1003, ¶¶65-105; INFINEON-1060, ¶¶8-11.

MOSAID’s objections to the combination are out of step with the law. Building “a single, coherent ‘Grundy-Kilbuck’ device” as MOSAID demands (POR, 1-8), is “basically irrelevant” because the operative question is “not whether the references could be physically combined,” *In re Etter*, 756 F.2d 852, 859 (Fed. Cir. 1985) (*en banc*). What matters is “whether the claimed inventions are rendered obvious by the teachings of the prior art as a whole.” *Id.*; *see also In re Mouttet*, 686 F.3d 1322, 1332-33 (Fed. Cir. 2012) (“[A] determination of obviousness based on teachings from multiple references does not require an actual, physical substitution of elements.”); *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“[A] skilled artisan may be motivated to combine particular features of different references...even when bodily incorporation would be impossible or inadvisable.”).

MOSAID’s reliance on *PersonalWeb* does not save its flawed single-coherent-device theory. POR, 3 (citing 848 F.3d 987 (Fed. Cir. 2017)). *PersonalWeb* does not require designing a device from the combined references with precise schematics or circuit layouts. Instead, the Federal Circuit vacated the Board’s obviousness determination because the analysis addressed what the combination “would have allowed for” rather than “how the combination of the two references

was supposed to work.” *PersonalWeb*, 848 F.3d at 993-94. As discussed, Infineon’s Petition has no such deficiency.

Moreover, *PersonalWeb* instructs that the amount of explanation required for a combination must account for context, as even “[a] brief explanation may do” if “the technology is simple and familiar and the prior art is clear in its language and easily understood.” 848 F.3d at 994. Again, the proposed Grundy-Kilbuck combination simply involves augmenting Grundy’s flash memory with the conventional flash-memory features taught by Kilbuck. Pet., 13-18; INFINEON-1003, ¶¶49, 57-64. MOSAID identifies no particular complexity that would necessitate further explanation beyond that already articulated in the Petition.

MOSAID also ignores that the Petition describes Kilbuck’s role in the combination at least as fully as the ’381 Patent’s description of its flash-memory features. *See, e.g.*, INFINEON-1001, 14:66-15:5. The ’381 Patent concedes the advanced state of the art by omitting many low-level granular details. *Id.*; INFINEON-1060, ¶¶15, 24. In other words, “that [the applicant] did not provide the type of detail in his specification that [MOSAID] now argues is necessary in prior art references supports [a] finding that one skilled in the art would have known how

to implement the features of the references.”<sup>1</sup> *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994).

MOSAID’s related critiques of Grundy’s DDR solution as allegedly “incomplete” and “non-functional” likewise have no merit. EX2027, ¶79; *see also generally id.*, ¶¶65-79, 137-138; POR, 6-7. Whatever qualms MOSAID may have, Grundy remains “prior art for all that it teaches,” and it teaches DDR. *Beckman Instruments, Inc. v. LKB Produkter AB*, 892 F.2d 1547, 1551 (Fed. Cir. 1989); *see also* INFINEON-1005, [0088]; INFINEON-1061, 56:10-57:8; INFINEON-1060, ¶¶12-13. Any adaptations needed to fully implement DDR would have been well

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<sup>1</sup> Importantly, MOSAID’s expert conceded that he had not carefully reviewed the ’381 Patent before submitting his declaration. INFINEON-1061, 37:13-38:1, 68:16-71:2. Consequently, he applies a double standard in his critiques of Grundy that are inconsistent with the ’381 Patent’s own disclosure. The opinions of MOSAID’s expert are also the product of bias and interests stemming from his longstanding prior and current relationships with MOSAID and the ’381 Patent’s inventors. *Id.*, 18:11-21, 22:9-26:21, 26:16-27:12, 28:15-33:1, 51:6-14, 52:2-13, 61:9-62:13, 69:15-70:22, 83:16-85:13, 88:6-89:22, 100:6-18, 105:15-109:7, 133:6-11, 141:5-142:3; EX-2027, 75 (CV/Patents); INFINEON-1001, cover; INFINEON-1060, ¶¶81-84.

within the level of ordinary skill. INFINEON-1060, ¶¶14-15 (citing INFINEON-1063, EX2029); *Gen. Elec. Co. v. Raytheon Techs. Corp.*, 983 F.3d 1334, 1351-52 (Fed. Cir. 2020) (POSITA is “not an automaton”).

**B. Precedent Expressly Supports the Petition’s Alternative Mappings on Flash Memory, Mooting MOSAID’s Critique**

The Petition’s reliance on Kilbuck to both corroborate and, alternatively, supplement Grundy for the claimed flash-memory features is legally sound and aligns with precedent.

Obviousness does not require that each claim limitation be mapped to one and only one prior art reference, or even that the mappings relate to “a single configuration.” POR, 12. The law is clear that obviousness can be established through alternative theories based on the teachings of one or more references in a combination. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1372-74 (Fed. Cir. 2019) (finding no error in petitioner’s argument that the primary reference disclosed all claim limitations, or “in the alternative that [the secondary prior-art reference] disclosed some of the elements in the claims at issue”).

As in *Realtime Data*, Infineon’s Petition explains that Kilbuck’s teachings render limitations of the ’381 Patent obvious “to the extent” they are not expressly disclosed in Grundy. *See, e.g.*, Pet., 20-22, 37, 39, 41, 46, 73. This is not an improper “shifting” conception of the combination as MOSAID alleges; it instead reflects

Grundy's primary contribution to the combination and Kilbuck's role in supplementing Grundy's less-detailed flash memory teachings. Pet., 13-17, 17-46. Kilbuck corroborates the teaching of claim limitations that a POSITA would have gleaned from Grundy alone or—in the alternative—Kilbuck supplies these limitations even if they are not found at all in Grundy. Employing Kilbuck to show that any alleged gaps in Grundy's disclosure are nonetheless obvious is the very *Graham* factor analysis that MOSAID complains the Petition lacks. POR, 7, 21-22.

**C. The Petition's Mappings Consistently Rely on Grundy's Memory Device, Supplemented by Kilbuck's Conventional Flash Features**

MOSAID's contention that the mappings “var[y] from limitation to limitation” mischaracterizes the Petition, conflating its contextual descriptions of the prior art with its operative claim mappings. *See* POR, 8-18.

**Elements [1pre]-[1a].** The Petition maps Grundy's memory device (as modified in view of Kilbuck) to the claimed “flash memory device,” and the Petition demonstrates how the Grundy-Kilbuck memory device includes erasable blocks, pages, and cells within the device's storage array. Pet., 17-21. Grundy discloses blocks and pages, (INFINEON-1005, [0062], [0101], [0109]), and Kilbuck confirms the conventional organization of flash into erasable blocks, pages, and cells, (INFINEON-1006, [0004], [0028], [0030]). There is no inconsistency. INFINEON-1060, ¶¶16-18.

**Elements [1b]-[1d].** Grundy's device-level signaling framework (*e.g.*, clock, multi-purpose, and command lines) provides these claim features, which MOSAID does not dispute. Pet., 22-34; INFINEON-1005, [0043]-[0044]. Grundy's framework is maintained in the combination with Kilbuck, which disproves MOSAID's consistency complaint. POR, 11-12. There is nothing inconsistent in relying on Grundy's signaling framework in conjunction with Kilbuck's more extensive disclosure of conventional flash-memory details. INFINEON-1060, ¶19.

**Element [1e].** The Petition explains in detail how the Grundy-Kilbuck combination provides a memory device with control circuitry that executes the claimed page program and read operations. Pet., 35-41; POR, 12-16. This circuitry is embodied in, for example, Grundy's I/O controller 303, protocol engine 305, and associated state machine. INFINEON-1005, Figures 17, 19-20. Grundy's control circuitry would be suitably configured to execute read and page program operations on flash, consistent with both Grundy's and Kilbuck's disclosures of a flash storage medium. INFINEON-1005, [0032]-[0033], [0035]; INFINEON-1006, [0004]-[0005], [0030]-[0031], [0039]. The Petition's contextual discussion of Grundy's memory controller's interaction with the memory device is not the inconsistent mapping MOSAID portrays. Pet., 35; INFINEON-1060, ¶¶20-21.

**Element [1f].** The Petition cites Grundy's disclosure of status requests and responses, (INFINEON-1005, [0032]-[0033], [0036], [0068]), and explains that

storing a status of the type contemplated by Grundy in a register was well known. Pet., 40-41 (citing INFINEON-1005, [0032]-[0033], [0036], [0068]; INFINEON-1007, p. 648; INFINEON-1009, p. 256; INFINEON-1003, ¶104). The Petition further cites Kilbuck for its teaching of an internal status register in a flash memory device. Pet., 41-42 (citing INFINEON-1006, [0033]). These disclosures are complementary, not inconsistent, as MOSAID contends. POR, 16-17. A register is the conventional, predictable way to hold status. INFINEON-1003, ¶¶104-105; INFINEON-1060, ¶22.

**D. The Petition’s Clear, Evidence-Backed Motivation Analysis  
Forecloses MOSAID’s Hindsight Defense**

Failing to find any substantive deficiency in the Petition’s motivation-to-combine analysis, MOSAID attempts an indirect attack on the motivations through argument that the Petition never identifies a valid combination in the first place. POR, 18-24. But as discussed above, MOSAID’s complaints are without merit. *Supra*, §§II.A-B.

The Grundy-Kilbuck combination flows logically from the references themselves, which is the antithesis of hindsight. The motivation to employ flash in the context of Grundy’s memory device comes straight from the source—Grundy—which lists “flash EEPROM” among its storage media. Pet., 13-17; INFINEON-1005, [0035]. A POSITA implementing Grundy with flash would have found it

obvious to consult a flash reference like Kilbuck for conventional implementation details. Pet., 13-15; INFINEON-1003, ¶¶59-60; INFINEON-1060, ¶¶23-24. This is the “known technique to a known system” reasoning *KSR* endorses, as reaffirmed in *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023). The *TQ Delta*, *InTouch*, and *Ruiz* decisions that MOSAID cites do not hold otherwise. POR, 19-20, 22. Indeed, these cases are inapposite. In each of them, the challenger assembled disparate references and features without a supporting motivation. Pet., 13-17; INFINEON-1003, ¶¶58-63. Infineon’s Petition does not suffer this flaw.

MOSAID’s “design choices” argument fails for similar reasons. POR, 21; INFINEON-1060, ¶25. That a combination raises design choices along the way does not negate motivation. *KSR*, 550 U.S. at 421. Here, there are no design choices that a POSITA could not manage. In fact, Dr. Przybylski conceded that (i) routine circuitry design can be omitted from a reference and left to a POSITA, (ii) the POSITA knows of all published prior art and fills implementation gaps from background knowledge, and (iii) the techniques underlying the combination were well known before the critical date. INFINEON-1061, 70:10-11 (“we understand that patents don’t need to disclose every little detail”), 74:11-77:13, 82:13-19, 83:16-85:13, 143:8-11.

The *Kotzab* decision is similarly unhelpful to MOSAID because it fails to identify any instance in which the Petition relied on mutually exclusive

embodiments from Grundy. POR, 23-24. MOSAID incorrectly asserts that the Petition's reliance on Grundy's paragraph [0051] to address claim 5's delay lock loop (DLL) limitation relates to an embodiment entirely distinct from Figures 5A and 17 cited elsewhere in the Petition. *Id.*; Pet., 57. But Grundy is clear that the DLL is an optional feature of the memory devices depicted in Figures 5A and 17. INFINEON-1005, [0051] ("Referring again to FIG. 5A[]"). Dr. Sechen's deposition testimony that MOSAID cites is entirely consistent with Grundy's description. POR, 23-24 (citing EX2028, 86:21-87:16, 89:1-4, 90:20-24); INFINEON-1060, ¶¶26-28. Grundy's Figure 4A likewise depicts a variation of the same memory device 107/155 depicted in each of Figures 3 and 5A. *See infra*, §V. Even if these "adjacent" disclosures were taken as mutually exclusive embodiments (which they are not), combining them is a natural extension of Grundy's teachings. *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) ("Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.").

**E. The Petition Establishes a Reasonable Expectation of Success That MOSAID Fails to Credibly Rebut**

As explained in the Petition, success was reasonably expected because the Grundy-Kilbuck combination joins known elements performing known functions. Pet., 17; INFINEON-1003, ¶64. MOSAID's generic assertions fail to identify a

specific incompatibility between Grundy’s memory-device teachings and Kilbuck’s flash-memory teachings that would have prevented a POSITA from expecting to reach the claimed invention. *See* POR, 24-26; *Salix Pharms., Ltd. v. Norwich Pharms. Inc.*, 98 F.4th 1056, 1062 (Fed. Cir. 2024) (“[C]ertainty and absolute predictability are not required to establish a reasonable expectation of success.”); *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) (“The reasonable expectation of success requirement refers to the likelihood of success in combining references to meet the limitations of the claimed invention.”); *see also* INFINEON-1001, 1:62-2:9; INFINEON-1061, 142:17-143:11; EX2027, ¶¶84; INFINEON-1060, ¶¶29-31.

### **III. THE PETITION’S OBVIOUSNESS CASE ON CLAIM 2 IS CONSISTENT, CLEAR, AND FACTUALLY CORRECT**

The Petition shows that Grundy discloses “the command data is latched at the first rising edge of the clock signal after the transition of the control signal” as recited in claim 2. Pet., 47-50; INFINEON-1001, 28:5-7. MOSAID’s objections rest on an erroneous understanding of the claimed “command data,” a mischaracterization of Grundy’s timing diagram, and a false distinction between the incoming (external) and internal versions of Grundy’s clock signal. INFINEON-1060, ¶¶32-56.

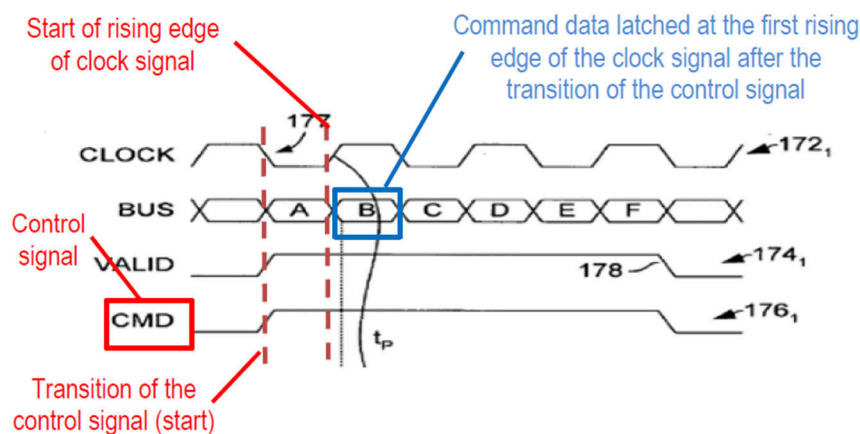
**A. Claim 2 Narrows “Command Data” and the Petition Follows Suit**

MOSAID begins by questioning which specific “values” the Petition relies on as “command data” for each of claims 1-2 and then attempts to identify differences between them. POR, 31-34. But this approach misreads the Petition and misunderstands how a POSITA would have understood the term “command data” in the ’381 Patent. INFINEON-1060, ¶¶32-37.

The unqualified term “command data” recited in claim 1 is not limited to the entire command data stream, nor even to any particular set of values in the stream. It instead encompasses any value(s) of command data that the memory device receives on the common data interface. INFINEON-1060, ¶¶36-37. By contrast, claim 2 narrows this universe to “command data” latched at the first rising edge of the clock signal after transition of the control signal—which may be just a single value. This is the scenario that arises in the ’381 Patent’s serial-transmission embodiments where command data values are transmitted and then latched sequentially one at a time based on transitions in the clock signal. *See, e.g., Id.*; INFINEON-1001, 7:4-7, 14:40-15:5, cls. 2, 11, Figures 3A, 6, 8A.

With MOSAID’s misinterpretation corrected, the merit of the Petition’s analysis is clear. As Grundy’s Figure 6 (below) illustrates, the memory controller asserts the command signal 176 (“control signal”) before the first rising edge of the clock signal 172, this edge corresponds to the start of command data value B.

Because the interface of Grundy's memory device 107/155 captures command data in response to clock signal transitions that follow assertion of the command signal, value B is the command data latched at the first rising edge of the clock signal, just as claim 2 requires. Pet., 47-50; INFINEON-1003, ¶¶106-109; INFINEON-1060, ¶¶34-37. The Petition's focus on Grundy's command value B for claim 2 aligns with the narrower scope of "command data" required by claim 2. *Id.* There is no inconsistency because the Petition likewise identified Grundy's value B as "command data" for claim 1. Pet., 29.



INFINEON-1005, Figure 6 (as excerpted, annotated at Pet., 48).

## **B. MOSAID Mischaracterizes the Petition's Reliance on Grundy's Figure 6 Timing Diagram**

MOSAID's next argument, that Grundy's Figure 6 depicts only the timing of transmissions from the memory controller rather than latching at the memory device, fails because the Petition does not rely on Figure 6 in isolation. POR, 34-44. The

Petition instead analyzes Figure 6 in the context of other disclosures in Grundy that address how data carried by the signals shown in Figure 6 are latched upon arrival at the memory device. Pet., 47-50. MOSAID's argument thus mischaracterizes the Petition and fails to analyze Grundy as a whole. *In re Warsaw Orthopedic, Inc.*, 832 F.3d 1327, 1332 (Fed. Cir. 2016) (“[T]he PTAB...must consider the prior art in its entirety, i.e., as a whole.”); INFINEON-1060, ¶¶38-46.

In more detail, Grundy discloses that Figure 6's signals traverse a short point-to-point link between parallel-routed clock and data lines. INFINEON-1005, Figures 3, 5A, 6. The timing relationship of the transmitted signals is preserved over that link. *Id.*; INFINEON-1060, ¶¶39-40. To show how these arriving signals are captured, the Petition cites Grundy's internal receiver and buffer architecture. Pet., 47-50 (citing INFINEON-1005, [0047], [0065]-[0071], [0088], [0092], [0097], Figures 19-20). For example, the Petition explains that “double-data rate capture is achieved by providing a first set of storage elements 315 to capture outputs of the differential receivers 310 in response to each rising edge of the clock signal 326.” Pet., 29-30.

The Petition further relies on Grundy's Figures 17 and 19 to show that captured command data is latched in response to clock transitions. POR, 42; Pet., 47-50. The Petition specifically quotes Grundy's disclosure that “command packets are loaded from the interface register into the ... command buffer 351, ... one word

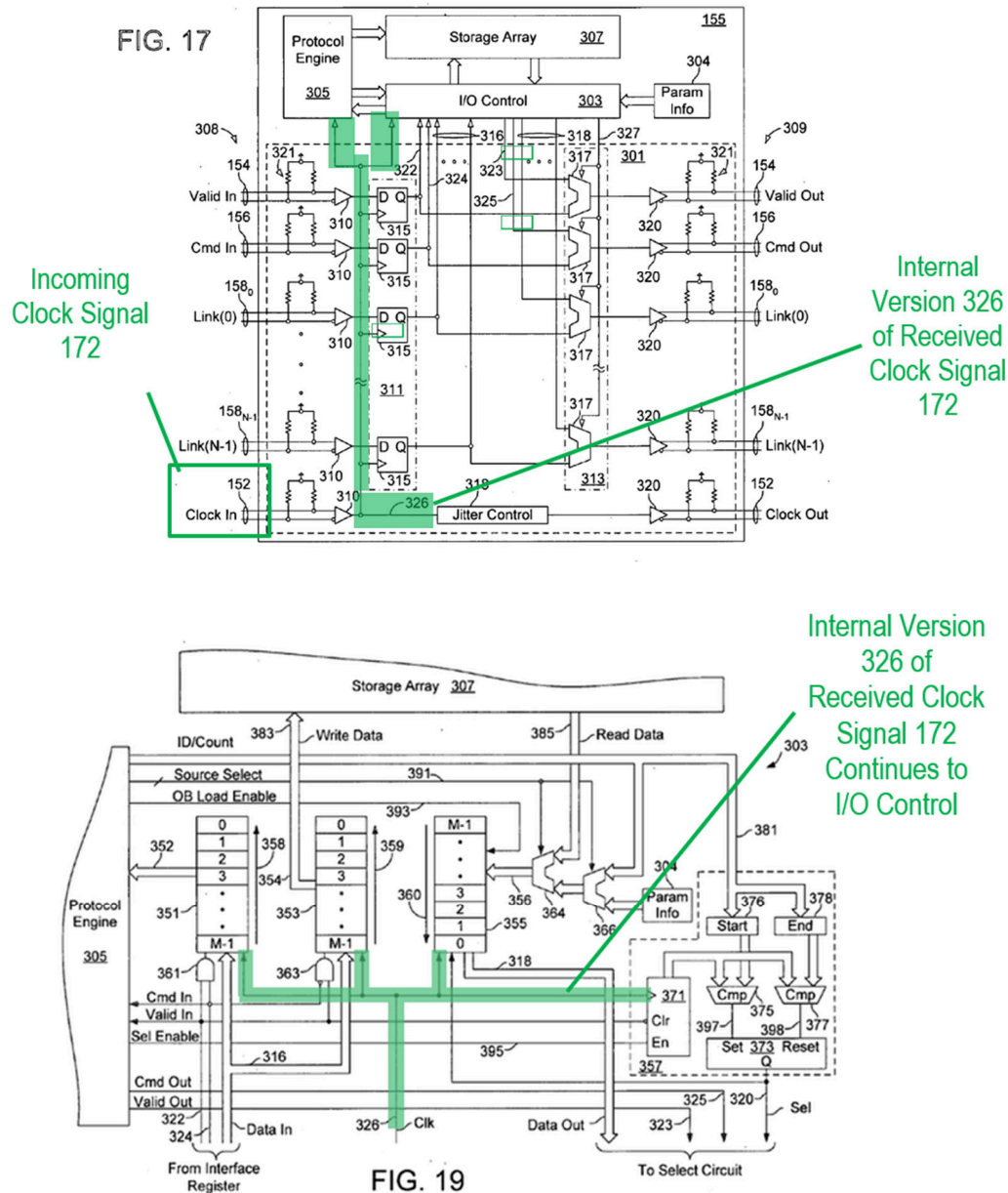
at time in response to transitions of the clock signal 326.” Pet., 50 (citing INFINEON-1005, [0092]). By synthesizing Figure 6’s signals’ edge correspondence with the memory device interface shown in Figures 17 and 19, the Petition demonstrates how the Grundy-Kilbuck combination latches command data in the manner required by claim 2. Pet., 47-50. INFINEON-1003, ¶¶106-109; INFINEON-1060, ¶¶38-46. MOSAID’s insistence that Grundy’s Figure 6 alone must do all the work is legally flawed and factually unsupported.

**C. Buffering Does Not Create a New Clock Signal: MOSAID’s Alleged Distinction Between Grundy and Claim 2 Is Illusory**

MOSAID’s attack on the Petition’s clock-signal mapping likewise fails under scrutiny. POR, 44-53. The premise of this argument, that Grundy’s incoming clock signal 172 and internal clock signal 326 are fundamentally different signals, finds no support in Grundy and defies common sense. INFINEON-1060, ¶¶47-56.

Grundy discloses that clock signal 326 is generated directly by “the signal receiver 310 coupled to the input-side clock line 152,” which is the line that carries clock signal 172. INFINEON-1005, [0088]. Grundy’s signal receivers 310 are simple transistor circuits that convert incoming signals at the bus signal level to a single-ended signal at chip-level voltages. INFINEON-1005, [0086]-[0087], Figures 17, 18A. As such, Grundy’s internal clock signal 326 is simply a buffered, on-chip version of the same clock signal 172 that was received from the memory controller

at the input of the signal receiver 310. INFINEON-1003, ¶¶106-109; INFINEON-1060, ¶¶48-53. This buffering step does not create a different clock signal.



INFINEON-1005, Figures 17, 19 (annotated); INFINEON-1003, ¶¶76-79, 106-109; INFINEON-1060, ¶49.

MOSAID's attempt to conjure a patentable distinction between incoming and internal versions of Grundy's clock signal is problematic because it contradicts the '381 Patent. The '381 Patent discloses the exact architecture that MOSAID's arguments now disclaim. It explains that control interface 208 generates an internal clock (SCLKI) from the incoming clock (SCLK) through "standard input buffer circuits." INFINEON-1001, 6:35-9:16, Figures 2A-2B; INFINEON-1060, ¶¶54-56. The '381 Patent's command data are then latched based on transitions of the internal clock SCLKI (not SCLK). *Id.* Dr. Przybylski agreed. INFINEON-1061, 88:6-90:9, 100:6-18, 107:7-110:3.

The '381 Patent relies on "standard input buffer" and single-ended receivers no different in kind from Grundy's receivers. *See* INFINEON-1001, 6:35-9:16; INFINEON-1005, [0029], [0044], [0047], [0085], Figure 17; *see also* INFINEON-1061, 105:15-109:2, 141:5-142:3; INFINEON-1060, ¶56. Like Grundy's receivers 310, the '381 Patent's standard input buffers introduce propagation delay between the signal at the input to the buffer and the signal produced at the output. INFINEON-1060, ¶¶52-56. But the propagation delay of a single buffer or simple input receiver does not change the underlying identity of the clock signal. To conclude otherwise is inconsistent with the '381 Patent's specification, and the claims that refer both to an incoming version of the "clock signal" in [1b] ("a clock input port configured to receive a clock signal") and an internal version of "the clock

signal” in [2] (the clock signal that synchronizes latching of command data in the memory device). INFINEON-1060, ¶¶54-56.

#### **IV. GRUNDY’S CLOCK OUTPUT SIGNAL SATISFIES PETITIONER’S CONSTRUCTION (CLAIMS 4, 5, 19)**

MOSAID’s arguments on “clock output signal” are an improper attempt to re-litigate issues that the Director resolved at institution. *See* Inst. Dec. (Paper 27), 3-4. The Director already set the terms for this trial, ordering that “Infineon shall be bound by its proposed district court construction of the term ‘clock output signal’ in its analysis of claims 4, 5, and 19 of the ’381 patent.” *Id.* The only question remaining is whether the Grundy-Kilbuck combination satisfies Infineon’s district-court construction of “clock output signal” as “a periodic signal that synchronizes system operations.” EX2007, 12. It plainly does, and MOSAID does not argue otherwise. Pet., 53-57; INFINEON-1003, ¶¶112-116, 163.

**Periodic.** The Petition explains how Grundy’s memory device receives a free-running clock signal and retransmits it as the claimed “clock output signal.” Pet., 53-57 (citing Grundy’s Figure 6, which shows a free-running, periodic clock signal); INFINEON-1005, Figure 6; INFINEON-1003, ¶¶112-116, 163. It is not surprising that Grundy’s clock output signal is periodic—after all, periodicity is the nature of a clock. INFINEON-1060, ¶¶57-60 (citing INFINEON-1062-63). On this point, all experts agree. *Id.*; INFINEON-1061, 38:9-39:4.

**Synchronizes system operations.** The Petition explains that “Grundy’s clock output signal (e.g., clock out) is synchronized with the output data” and that “the next device...would rely on the [output] data to be synchronized with the clock signal to ensure the data could be properly processed according to rising and falling edges of the clock signal.” Pet., 55-56; *see also id.*, 54 (citing Grundy’s Figure 6). A POSITA would have understood synchronizing the operations of the receiving device (and, more broadly, the chain) entails synchronizing system operations. INFINEON-1060, ¶¶61(citing INFINEON-1062-63); INFINEON-1061, 42:8-44:4.

**Not a strobe.** Grundy’s outgoing clock is a continuous periodic clock, not a strobe. Grundy itself distinguishes its “free-running clock signal” from “a strobe signal that is toggled only when data and/or commands are being transmitted.” Pet., 23; INFINEON-1005, [0047]; EX2007, 4, 12; INFINEON-1060, ¶62.

MOSAID’s focus on whether the Petition expressly proposed this construction is irrelevant. Now that the Director has exercised his discretion and ordered that Infineon’s district-court construction will apply to this proceeding, Infineon “must” be afforded “an opportunity to respond.” *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374, 1383-84 (Fed. Cir. 2023).

MOSAID tries but fails to analogize this case to the Federal Circuit’s recent decision in *Apple Inc. v. Gesture Technology Partners, LLC*, 129 F.4th 1367 (Fed. Cir. 2025). *See* POR, 29. Where *Gesture Technology* involved a situation in which

the petition “presented no argument” that “would meet [the] claim construction,” the opposite is true here for the reasons discussed above. 129 F.4th at 1374; Pet., 53-57; INFINEON-1005, [0047]-[0048], [0084], [0088]; INFINEON-1003, ¶¶112-116.

**V. GRUNDY-KILBUCK’S OVERLAPPING READ AND PROGRAM OPERATIONS SATISFY CLAIMS 13 AND 21**

Claim 13 requires that “the control circuitry is configured to perform the read operation during a time period that overlaps with a time period for the page program operation.” INFINEON-1001, 28:41-44. Claim 21 recites similar language. *Id.*, 30:14-16. For the reasons set forth below and in the Petition, the Grundy-Kilbuck combination provides read and program operations that plainly “overlap,” and MOSAID’s objections are all without merit. Pet., 66-70, 13-17; POR, 53-61.

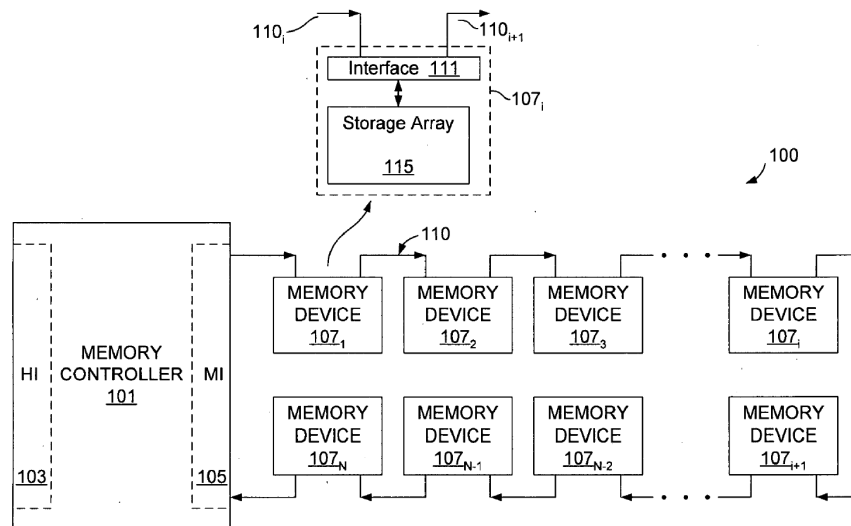
**A. The Petition’s Mappings for Dependent Claims 13/21 Align Fully With Their Corresponding Independent Claims 1/17, Creating No Structural or Logical Conflict**

MOSAID again misrepresents the Petition as shifting mappings from a first embodiment represented by Grundy’s Figures 3/5A for independent claims 1/17 to a materially distinct second embodiment represented by Grundy’s Figure 4A for claims 13/21. POR, 53-61. Not so.

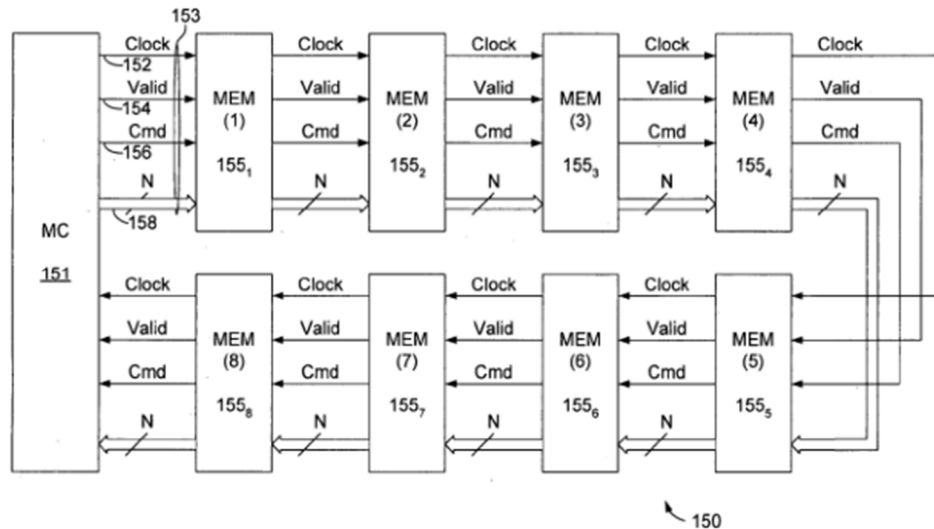
The Petition does not isolate Grundy’s disclosures in the piecemeal fashion MOSAID suggests. For example, the Petition’s claim 13 analysis highlights the ability of Grundy’s device to support multiple signaling paths as shown in Figure

4A, while simultaneously citing Figure 5A and its related description at [0043]. Pet., 67. Likewise, for claim 1, the Petition cites not only Figures 3/5A, but also [0041] of Grundy, which describes variants involving multiple signaling paths. Pet., 26, 44. The law is clear that “[i]f a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, § 103 likely bars its patentability.” *KSR*, 550 U.S. at 417.

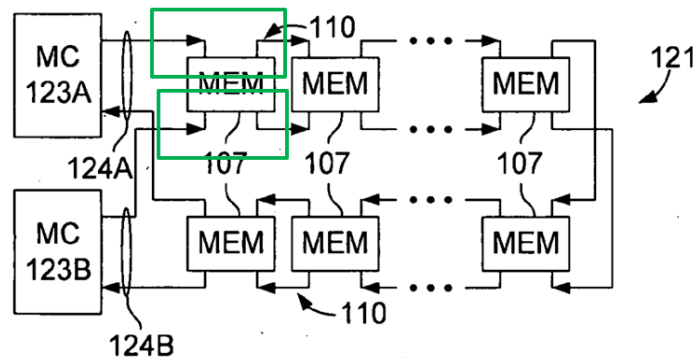
Even with myopic focus on Grundy’s figures, as MOSAID’s argument requires, the Petition’s analyses for claims 13/21 and 1/17 do not diverge in substance. Grundy’s memory device (107/155) remains the focus throughout: Figures 3/5A show device 107/155 in a single-path configuration, while Figures 4A-4D show device 107/155 in a dual-path configuration. Pet., 17-46, 66-70. Grundy ties these figures together by opening the description of Figure 4A with an explicit reference to Figure 3. INFINEON-1005, [0041] (“Still referring to FIG. 3,...”).



INFINEON-1005, Figure 3. The connection is likewise visually evident from the figures themselves. Figure 5A shows that each pathway has a set of links 153.



INFINEON-1005, Figure 5A, [0043]. Figures 4A-4D simply add another path, each having its own set of links 153.



INFINEON-1005, Figure 4A (emphasis to show top/bottom paths), [0041], [0043].

Grundy identifies no difference between the two signaling interfaces of the dual-path variant and the one signaling interface of the single-path variant. INFINEON-1005, [0041]. A POSITA would have understood Grundy's silence in

this regard as an indication that no material differences exist. INFINEON-1060, ¶¶63-68. And because the signaling interfaces are not materially different, the Petition’s mappings for claims 1/17 (which focus on the single-path variant of Figures 3/5A) apply equivalently to the dual-path variant of Figure 4A. It is well settled that “[c]ombining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness.” *Boston Scientific*, 554 F.3d at 991.

MOSAID’s objection that the Petition insufficiently addresses how a multi-controller system would operate is likewise unfounded. POR, 57. This objection overlooks that overlap in read operations and page-program operations can occur in the same memory device, even in the course of typical interactions between that device and any one controller. Pet., 67 (highlighting the initial memory device as an example of the same device where overlap can occur), 69-70 (citing Kilbuck’s disclosure regarding “rapidly changing multiple reads and writes of the memory system”), 70 (discussing POSITA’s knowledge of how a processor typically interacts with memory).

MOSAID’s objection is also moot in view of the Petition’s citation to Grundy’s Figure 4C, which shows a single memory controller “used to control transfers on both signaling queues [(paths)].” Pet., 67; INFINEON-1060, ¶69. MOSAID never addresses this Figure 4C configuration.

**B. Applying Kilbuck's Teaching of Multiple Flash Memories to Grundy Predictably Yields the Claimed Overlapping Operations**

MOSAID extends to dependent claims 13 and 21 the same flawed attacks on the Grundy-Kilbuck combination that it earlier advanced to no avail with respect to independent claims 1 and 17. POR, 56-64.

Contrary to MOSAID's assertions (POR, 61-64), the Petition clearly addresses Kilbuck's contribution and explains how the Grundy-Kilbuck combination achieves the features recited in claims 13 and 21. Pet., 67-70. Specifically, the Petition explains that it would have been obvious to modify one of Grundy's memory devices 107/155 to include Kilbuck's teaching of multiple flash memories. Pet., 68-69; INFINEON-1006, Figures 3A-3B (disclosing multiple flash memories 314 in a single flash memory subsystem 304). Further, Grundy discloses that a memory device can include multiple memories. Pet., 9-11, 17-19, 42-43; INFINEON-1060, ¶¶70, 74 (citing INFINEON-1005, [0035], [0084]).

Kilbuck discloses systems with multiple flash memories, each with independent memory banks (e.g., flash cell arrays 316) and independent access circuitry, such that one device may read while another programs. Pet., 68-70; INFINEON-1003, ¶¶128-136; INFINEON-1006, [0030], [0040]-[0042]. A straightforward application of Kilbuck's teachings to Grundy predictably yields a memory device 107/155 whose control circuitry would independently access each

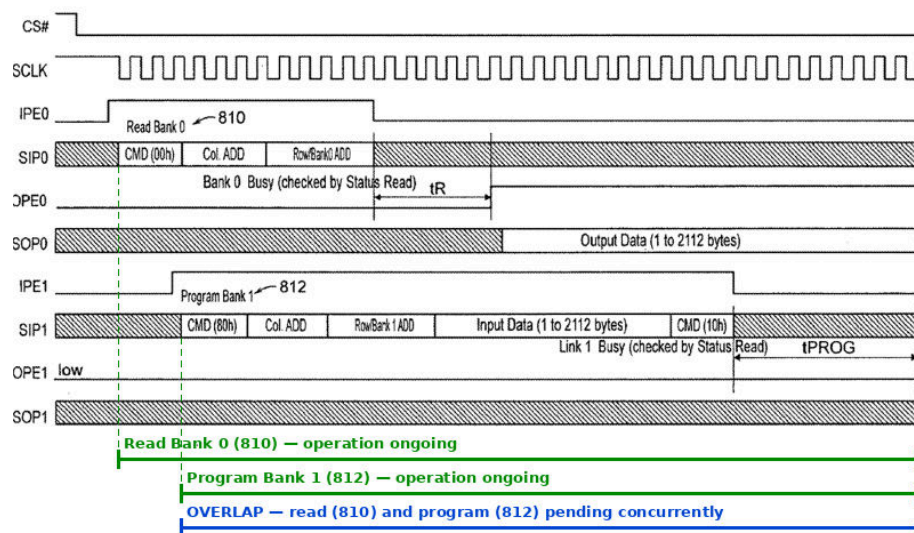
flash memory in the device. Pet., 69-70; INFINEON-1003, ¶¶131-135; INFINEON-1060, ¶71. This independent access facilitates overlapping read and program operations via either a single flash memory or multiple flash memories. *Id.*

MOSAID’s expert Dr. Przybylski opines that “[a] POSITA would understand that a system allowing overlapping operations from multiple controllers would need a mechanism for coordinating such operations or preventing conflicts.” EX2027, ¶135. But these arguments regarding the need for “control circuitry” (or another coordinating mechanism) are entirely inapplicable at least as to claim 21—a method claim that does not require or recite control circuitry. INFINEON-1001, cl. 21.

In any event, the allegation that Grundy-Kilbuck lacks such control circuitry or a coordinating mechanism is incorrect. INFINEON-1060, ¶¶72-75. For example, Grundy describes a “command buffer 351” configured to receive/store commands issued by the memory controller, including “read, write” commands. INFINEON-1005, [0090], [0092]-[0094], Figures 17-19. “After the final word of a command ... is loaded into the command buffer 351, the entire command is transferred to the protocol engine 305...thus freeing the command buffer 351 to receive subsequent commands while the command transferred to the protocol engine 305 is carried out.” *Id.*, [0093]; INFINEON-1060, ¶73.

Grundy’s circuitry that buffers subsequent commands even while an earlier-received command is pushed out for downstream processing provides a control

function and coordinating mechanism that specifically allows Grundy's device to perform a read operation during a time period that overlaps a write/page program operation (*e.g.*, by buffering a command for the read operation while a command for the page program operation is transferred/processed downstream (or vice versa)). INFINEON-1060, ¶¶73-75. This follows from the '381 Patent's broad delineation of the bounds of read and page program operations, each of which spans from initial command receipt and buffering at the memory device through, respectively, the return of read data to the memory controller or the final writing of data to the memory bank. This is shown, *e.g.*, in Figure 8B, which depicts page-read 810 and page-program 812 operations that begin with the reception of a page-read command (CMD 00h) and a page-program command (CMD 80h), respectively (both of which are buffered similar to Grundy)—even before any data is actually read from or written to any memory bank:



INFINEON-1001, Figure 8B (annotated); *see also id.*, 9:35-10:67, 15:16-16:14, 19:1-63, FIG. 2C, Table 1; Pet., 70; INFINEON-1003, ¶136; INFINEON-1061, 118:2-7, 119:1-120:9, 129:19-130:7; INFINEON-1060, ¶¶76-78 (EX2029, INFINEON-1065).

**C. MOSAID’s Unfounded Complaints Leave the Petition’s Explicit and Compelling Motivation-to-Combine Analysis Unanswered**

MOSAID’s remaining arguments that the Petition “never provides a reasoned motivation,” “never identifies the modified architecture,” and “never addresses coordination issues” merely repeat contentions already addressed above in Sections V.A-B. *See* POR, 64-68.

The Grundy-Kilbuck combination provides a dual-path device that performs overlapping operations, a result motivated by increased operational speed and fast random read/write and burst capability. Pet., 66-70, 13-17; INFINEON-1006, [0030], [0040]-[0042]; INFINEON-1003, ¶131. Coordinating such command execution is a routine engineering task, not a prohibitive obstacle, nor is it recited in the claims. INFINEON-1060, ¶¶79-80 (citing INFINEON-1006, EX2029, INFINEON-1065). The law does not require resolving every possible implementation detail to establish obviousness. *KSR*, 550 U.S. at 419 (“What matters is the objective reach of the claim. If the claim extends to what is obvious, it is invalid

under § 103.”); *Axonics*, 73 F.4th at 957; *ClassCo, Inc. v. Apple, Inc.*, 838 F.3d 1214, 1219 (Fed. Cir. 2016); *Gen. Elec.*, 983 F.3d at 1351-52.

Respectfully submitted,

Dated: September 9, 2026

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**CERTIFICATION UNDER 37 C.F.R. § 42.24**

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petitioner Reply to Patent Owner Response totals 5,587 words, which is less than the 5,600 allowed under 37 CFR § 42.24(c)(1).

Respectfully submitted,

Dated: September 9, 2026

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**CERTIFICATE OF SERVICE**

Pursuant to 37 CFR §42.6(e)(4), the undersigned certifies that on September 9, 2026, a complete and entire copy of this Petitioner's Reply to Patent Owner's Response were provided via email, to the Patent Owner by serving the email correspondence addresses of record as follows:

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