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Title:	DISTRIBUTED MULTIPLEXING CIRCUIT WITH BUILT-IN REPEATER	

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PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT NO. 7,349,448 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

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EX1001	U.S. Patent No. 7,349,448 to Chang ("the '448 Patent")
EX1002	Excerpts from the Prosecution History of the '448 Patent ("the Prosecution History")
EX1003	Declaration and Curriculum Vitae of Dr. Andrew Wolfe
EX1004	U.S. Pat. No. 5,572,535 to Carl Pixley *et al.* ("Pixley")
EX1005	U.S. Pub. No. 2003/0056080 to Mitsuhiro Watanabe ("Watanabe")
EX1006	U.S. Pub. No. 2002/0144211 to Fadi Maamari *et al.*
EX1007	U.S. Pub. No. 2002/0057103 to Tony Ngai *et al.*
EX1008	U.S. Pat. No. 4,363,978 to Gary L. Heimbigner
EX1009	U.S. Pat. No. 4,782,250 to Robert D. Adams *et al.*
EX1010	Ken Martin, *Digital Integrated Circuit Design* (2000)
EX1011	Richard F. Tinder, *Engineering Digital Design* (2000)

LISTING OF CLAIMS

Claim 1	
1.pre	A circuit for multiplexing a plurality of data words including a first data word and a second data word, comprising:
1.a	a plurality of data connections;
1.b	first stage logic having a first tristate driver, the first tristate driver configured to receive the first data word from one of the connections and to transmit the first data word received; and
1.c.i	second stage logic configured to receive the first data word from the first stage logic and to receive the second data word from another of the plurality of data connections, the second stage logic configured to select for transmission one of the first data word and the second data word based upon a set of select signals, the second stage logic configured to transmit the data word selected for transmission by the second stage logic,
1.c.ii	the second stage logic having a connection, a second tristate driver, and a third tristate driver, the second tristate driver having an output electrically coupled to an output of the third tristate driver, the second tristate driver configured to receive the first data word from the first tristate driver and to drive the connection of the second stage logic with the first data word if the first data word is selected for transmission by the second stage logic, the third tristate driver configured to receive the second data word and to drive the connection of the second stage logic with the second data word if the second data word is selected for transmission by the second stage logic.
Claim 2	
2	The circuit of claim 1, wherein the second stage logic is further configured to transmit, to a third stage logic, the data word selected for transmission by the second stage logic.

Claim 3	
3	The circuit of claim 1, wherein the second stage logic is further configured to transmit, to a system bus, the data word selected for transmission by the second stage logic.
Claim 4	
4.pre	A multiplexor circuit, comprising:
4.a	a plurality of data connections;
4.b	first stage logic configured to receive a first data word from one of the connections and to transmit the first data word received based on a set of select signals; and
4.c.i	second stage logic configured to receive the first data word from the first stage logic and to select a selected data word between the first data word and a second data word received from another of the plurality of data connections based upon a set of select signals,
4.c.ii	the second stage logic configured to transmit the selected data word to a third stage logic and to increase a signal strength of the first data word when the first data word is transmitted, if the first data word is selected.
Claim 5	
5.pre	A multiplexor circuit, comprising:
5.a	a plurality of data connections;
5.b	first stage logic configured to receive a first data word from one of the connections and to transmit the first data word received; and
5.c	second stage logic configured to receive the first data word from the first stage logic and to select a selected data word between the first data word and a second data word received from another of the plurality of data connections based upon a set of select signals, the second stage logic configured to transmit the selected data word to a third stage logic,

5.d	wherein the second stage logic comprises: a first tristate driver configured to drive a connection with the first data word from the first stage logic, the first tristate driver enabled if a data connection exclusion signal is asserted and disabled if the data connection exclusion signal is deasserted; and a second tristate driver configured to drive the connection with the second data word, the second tristate driver enabled if a data connection select signal is asserted and disabled if the data connection select signal is deasserted.
Claim 6	
6	The circuit of claim 5 wherein the first tristate driver increases the signal strength of the first data word when the selected data word is the first data word.
Claim 7	
7.a	The circuit of claim 5, further comprising: a first latch circuit configured to receive the data connection exclusion signal, the first latch circuit configured to latch the value indicative of the data connection exclusion signal at an output of the first latch circuit, the output of the first latch circuit configured to enable the first tristate driver if the data connection exclusion signal is asserted;
7.b	a second latch circuit configured to receive the data connection selection signal, the second latch circuit configured to latch the value indicative of the data connection selection signal at an output of the second latch circuit, the output of the second latch circuit configured to enable the second tristate driver if the data connection selection signal is asserted;
7.c	a third latch circuit configured to receive the second data word, the third latch circuit configured to latch the second data word at an output of the third latch circuit, the output of the third latch circuit configured for receipt by the second tristate driver;

7.d	a first clock configured to transmit a clock signal to the first, second, and third latch circuits, the clock signal activating latching of the second data word, the data connection selection signal and the data connection exclusion signal at the outputs of the third, second and first latch circuits, respectively.
Claim 8	
8.pre	A circuit comprising
8.a	a plurality of data connections;
8.b	logic associated with a first data connection of the plurality of data connections, the logic associated with the first data connection configured to transmit a first data word corresponding to the first data connection;
8.c	logic associated with a second data connection of the plurality of data connections configured to receive the first data word corresponding to the first data connection from the logic associated with the first of the plurality of data connections, the logic associated with the second data connection configured to select a first selected data word between the first data word and a second data word corresponding to the second data connection based upon a set of select signals; and
8.d	logic associated with a third data connection of the plurality of data connections configured to receive the first selected signal set, the logic associated with the third data connection configured to select a second selected data word between the first data word and a third data word corresponding to the third data connection based upon a set of select signals, the logic associated with the third data connection further configured transmit the second selected data word to a system bus.
Claim 9	
9.pre	A multiplexor circuit, comprising:
9.a	a first tristate driver comprising a first data input, a first data output, and a first enable input, the first tristate driver adapted to receive a first data word via the first data input representative of a first data connection;

9.b	a second tristate driver comprising a second data input, a second data output, and a second enable input, the second tristate driver adapted to receive a second data word representative of a second data connection;
9.c	a third tristate driver having an output coupled to the first data input of the first tristate driver; and
9.d	a connection adapted to receive, via the data output of the first tristate driver, the first data word, if a first signal is asserted at the first enable input of the first tristate driver, the connection further adapted to receive, via the second data output of the second tristate driver, the second data word, if a second signal is asserted at the enable input of the second tristate driver.
Claim 10	
10	The multiplexor circuit of claim 9, further comprising select logic configured to assert the first signal if an application program desires the first data word representative of the first data connection and configured to assert the second signal if the application program desires the second data word representative of the second data connection.
Claim 11	
11	The multiplexor circuit of claim 10, wherein the select logic deasserts the first signal if the application program does not desire the first data word and deasserts the second signal if the application program does not desire the second data word.
Claim 12	
12	The multiplexor circuit of claim 11, wherein the first signal and the second signal enable and disable the first and second tristate drivers simultaneously.
Claim 13	
13.pre-13.a	The multiplexor circuit of claim 12, further comprising: a first latch circuit configured to transmit the first signal to the first tristate driver upon a leading edge of a clock signal; and

13.b	a second latch circuit configured to transmit the second signal to the second tristate driver upon the leading edge of the clock signal.
Claim 14	
14.pre	A method for distributing multiplexing, comprising:
14.a	transmitting a first data word from a first tristate driver to a second tristate driver;
14.b	receiving a second data word; and
14.c	selecting for transmission between the first data word and the second data word based upon a set of select signals;
14.d	driving a first connection with the first data word via the second tristate driver if the first data word is selected by the selecting; and
14.e	driving the first connection with the second data word via a third tristate driver if the second data word is selected by the selecting.
Claim 15	
15	The method of claim 14, wherein the selected data word is transmitted to a discrete integrated circuit (IC) component.
Claim 16	
16	The method of claim 15, wherein the select signals comprise a data connection selection signal indicative of which data word is to be selected and a data connection exclusion signal indicative of which data word is to be excluded.
Claim 17	
17.pre	A method for distributing multiplexing, comprising:
17.a	receiving a first data word corresponding to a first data connection;
17.b	transmitting, via a tristate driver, the first data word to first logic associated with a second data connection;

17.c	selecting a selected data word via the first logic between the first data word and a second data word transmitted from the second data connection based upon a set of select signals; and
17.d	transmitting the selected data word,
17.e	wherein the selecting comprises: driving the second data word to a connection via a first tristate driver if the data connection selection signal is asserted; and disabling a second tristate driver configured to receive the first data word and configured to drive the first data word to the connection if the data connection exclusion signal is asserted.
Claim 18	
18	The method of claim 17, wherein the selecting step further comprises: driving the first data word to the connection via the second tristate driver if the data connection exclusion signal is asserted; and disabling the first tristate driver if the data connection selection signal is deasserted.
Claim 19	
19	The method of claim 18, wherein the driving the first data word to the connection further comprises increasing signal strength of the first data word.
Claim 20	
20.a	The circuit of claim 1, wherein the plurality of data words includes a third data word,
20.b	the circuit further comprising third stage logic configured to receive the third data word and the data word selected for transmission by the second stage logic,
20.c	the third stage logic configured to select for transmission one of the third data word and the data word selected for transmission by the second stage logic based on a set of select signals,

20.d	the third stage logic having a connection, a fourth tristate driver, and a fifth tristate driver, the fourth tristate driver having an output electrically coupled to an output of the fifth tristate driver, the fourth tristate driver configured to receive the data word selected for transmission by the second stage logic and to drive the connection of the third stage logic with the data word selected for transmission by the second stage logic if the data word selected for transmission by the second stage logic is selected for transmission by the third stage logic, the fifth tristate driver configured to receive the third data word and to drive the connection of the third stage logic with the third data word if the third data word is selected for transmission by the third stage logic.
Claim 21	
21	The method of claim 14, further comprising: receiving at a fourth tristate driver the data word selected by the selecting; selecting for transmission between the received data word and a third data word based upon a set of select signals; driving a second connection with the received data word via the fourth tristate driver if the received data word is selected by the selecting for transmission between the received data word and the third data word; and driving the second connection with the third data word if the third data word is selected by the selecting for transmission between the received data word and the third data word.

Petitioner Infineon Technologies Americas Corp. petitions for *Inter Partes* Review of Claims 1-21 ("Challenged Claims") of U.S. Patent No. 7,349,448.

I. REQUIREMENTS FOR IPR—37 C.F.R. §42.104

A. Grounds for Standing—37 C.F.R. §42.104(a)

Petitioner certifies that the '448 Patent is available for IPR, and that Petitioner is not barred or estopped from requesting IPR.

B. Challenge and Relief Requested—37 C.F.R. §42.104(b)

Petitioner requests IPR and cancellation of the Challenged Claims based on the ground below. Petitioner submits that the cited prior art references are themselves sufficient to establish obviousness pursuant to the analysis in Section IV. The Section IV analysis further cites the Declaration of Dr. Andrew Wolfe (EX1003)—an expert with over thirty years of experience in the field of digital circuit design (EX1003, ¶¶4-18)—as well as additional documentary evidence to explain the knowledge of a skilled artisan.

Claims	Asserted Ground
1-21	§103—Pixley (EX1004) in view of Watanabe (EX1005)

As shown below, each of the above identified references pre-dates the '448 Patent's filing date of August 1, 2003.

Reference	Prior Art Date	Status
Pixley	Issued Nov. 5, 1996	§102(b)
Watanabe	Filed Sep. 18, 2002; Published Mar. 20, 2003	§§102(e), 102(a)

II. THE '448 PATENT

A. Brief Description

The '448 Patent relates to "systems for distributing multiplexor functionality." EX1001, 1:52-53. According to the '448 Patent, a standard multiplexor suffered from problems relating to the number of wires on a single integrated circuit (IC) that can lead "to routing congestion and the inherent problems associated therewith, e.g., difficulty in designing and fabricating." EX1001, 1:16-23. In order to address these alleged problems, the '448 Patent purports to provide "a distributed multiplexor circuit select between multiple data connections." EX1001, 2:33-34; EX1003, ¶39.

FIG. 2 (reproduced below[1]) illustrates one embodiment of the purported invention. EX1001, 2:65-67. In FIG. 2, the distributed multiplexor logic (DML) "comprises a plurality of stages 204-207, preferably corresponding to the number of data connections, from which a selected data word is chosen and transmitted via connection 226." EX1001, 3:8-11. Each DML stage is then connected to select logic 202 that "indicate[s] which of the data words from data connection 214a-214d is the 'selected data word' that is to be output from the DML 201 and

[1] Unless otherwise noted, all figures reproduced herein include annotations shown in color.

transmitted, via connection 226, to a system bus 224." EX1001, 3:39-43; EX1003, ¶40.

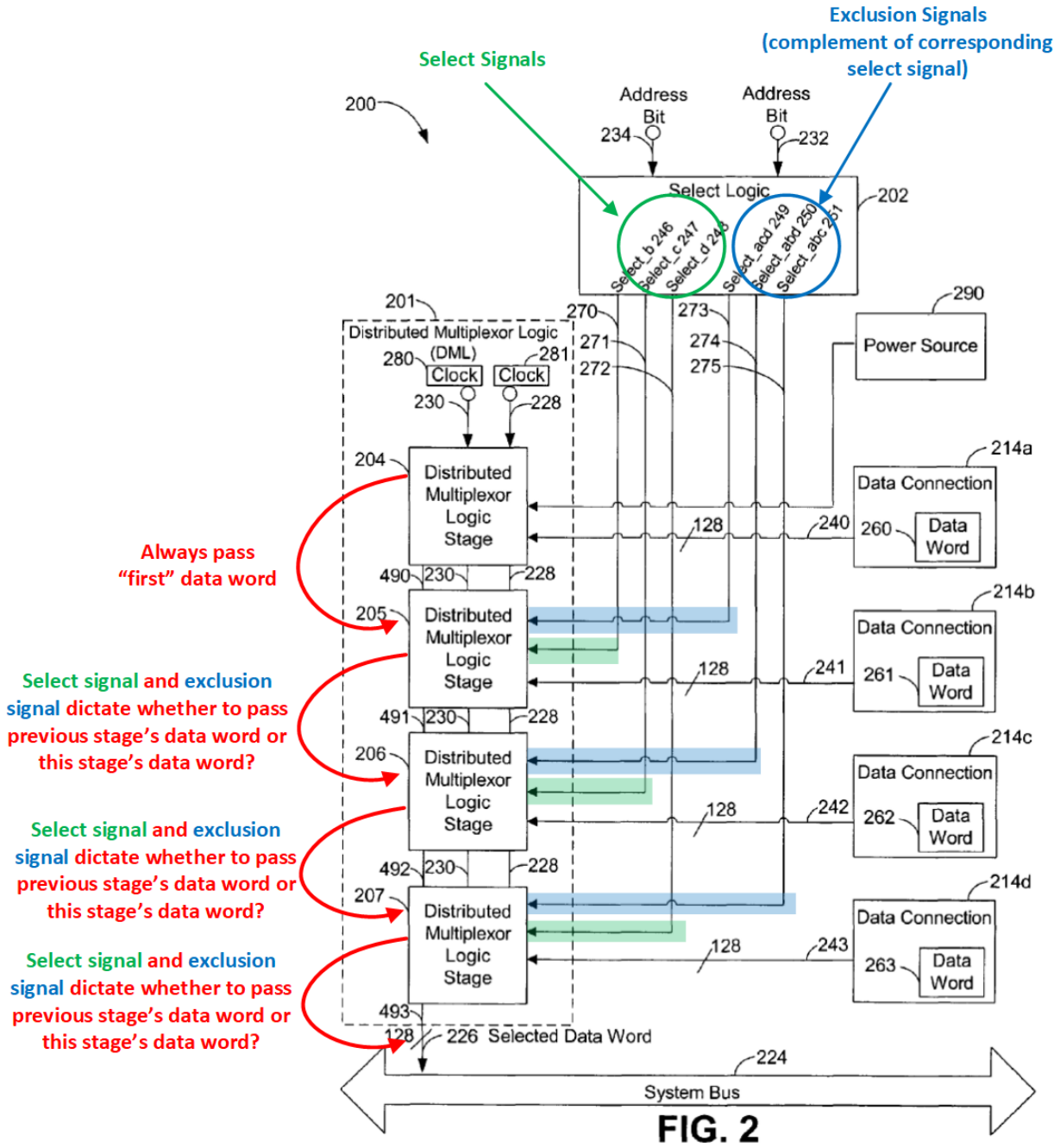


FIG. 2

Each DML stage other than the first receives a "select signal" and an "exclusion signal." EX1001, 3:64-4:9. When the select logic is driven to select a data word

corresponding to a DML stage, that DML stage's select bit is asserted while its exclusion signal is deasserted, and all other DML stage's select bits are deasserted while their exclusion signal is asserted. *See generally* EX1001, 3:64-4:23, 4:66-5:22; EX1003, ¶41.

As illustrated in FIG. 4 (reproduced below) "[e]ach DML stage 204-207, preferably comprises data connection selection tristate drivers 408-411, each of which receives and outputs its associated data word 260-263 to its associated connection 490-493, respectively, based upon select signals 246-251." EX1001, 7:16-20. Except for the first DML stage, the other DML stages include two tristate drivers: a data connection selection tristate driver and a data connection exclusion tristate driver. *See* EX1001, 7:21-48; EX1003, ¶42.

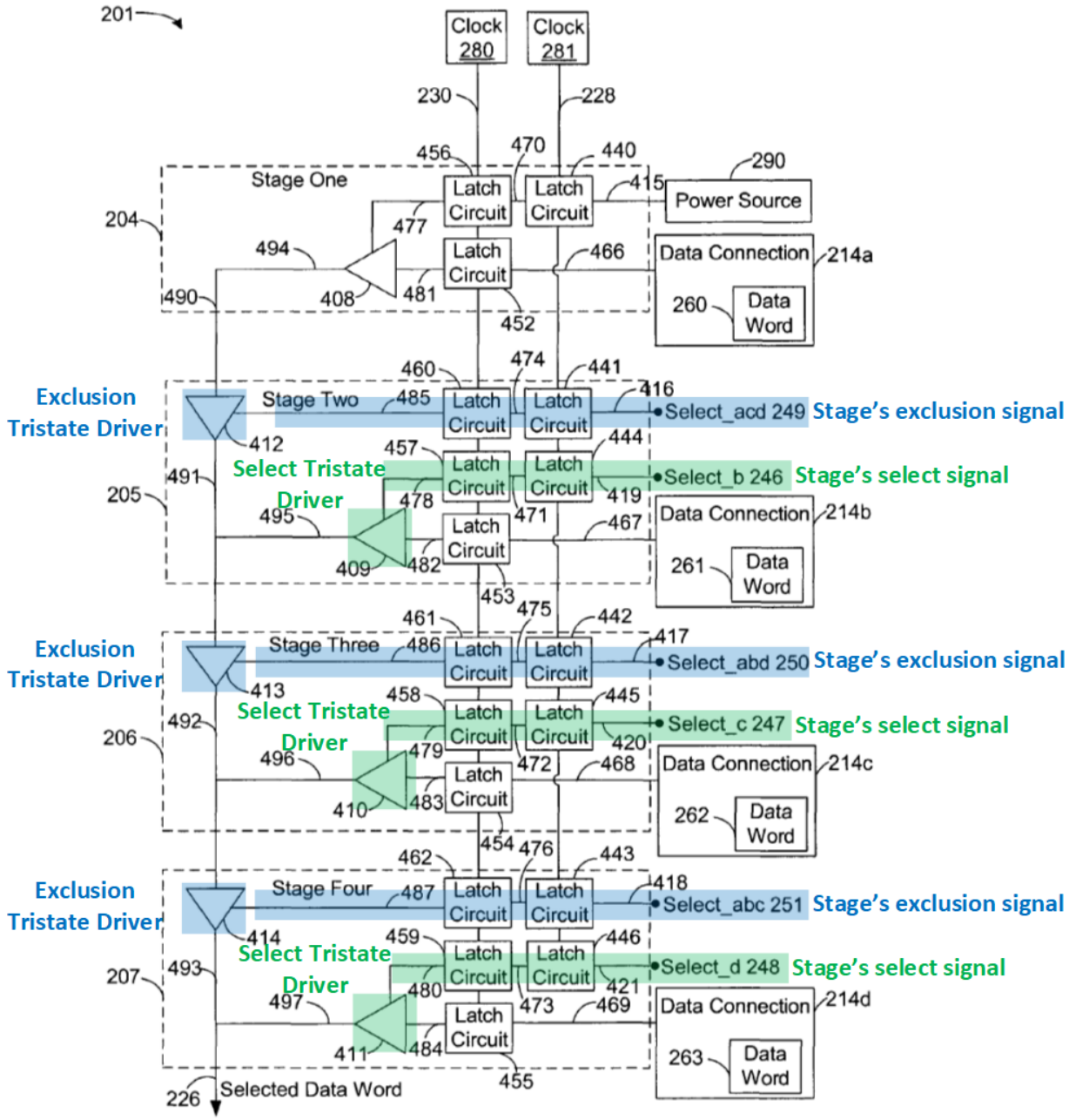


FIG. 4

When the select logic is driven to select a data word corresponding to a DML stage, that DML stage's data connection selection tristate driver is activated by the select signal corresponding to the DML stage and the data connection exclusion tristate driver is deactivated by the exclusion signal corresponding to the

DML stage. *See* EX1001, 7:49-62. The other two-tristate-driver DML stages' data connection selection tristate drivers are deactivated by the corresponding select signal and the data connection exclusion tristate drivers are activated by the corresponding exclusion signal. *See* EX1001, 7:49-62. "In propagating the data words 260-263 from the first stage to the final stage of the circuit 201, the tristate drivers 412-414 located between each stage 204-207 serve to increase the signal strength of the data word propagated from the previous stage, thereby acting as repeaters." EX1001, 9:63-10:3; EX1003, ¶43.

As shown in FIG. 4 (above), each stage includes latch circuits that are driven by out-of-phase clock signals. *See generally* EX1001, 8:1-54. The latch circuits support "[c]oncurrent enablement and disablement of the tristate drivers 408-411 and 412-414" in order to "limit the amount of 'drive fight,' e.g., the time that more than one driver is attempting to drive a connection 490-493 to a different data word 260-263." EX1001, 10:4-15; EX1003, ¶44.

The '448 Patent identifies at least two prior art solutions to the same problems addressed by its distributed MUX. EX1001, 1:39-43. According to the '448 Patent, the first is a "dynamic MUX," which allegedly "requires more power, has smaller noise margins, and takes more time to design correctly." EX1001, 1:39-43. The second prior art solution is "usage of tristate multiplexors," which are "acceptable when the distances between the data connections 102-105 and the

multiplexor logic 110 are small." EX1001, 1:43-48. While the '448 Patent suggests that, for tristate multiplexors, "speed and noise degradation typically increases as the distances between the data connections increase" (EX1001, 1:46-48), the claims of the '448 Patent do not constrain the distance between data connections, the DML stages of the '448 Patent rely upon tristate drivers, and ultimately the Challenged Claims are broad enough to cover solutions based on tristate multiplexors, which will be discussed in greater detail below. EX1003, ¶45.

B. Prosecution History

In order to overcome an office action rejection of the proposed claims over U.S. Pat. No. 7,023,844 (Wolrich), the Applicant pointed to tri-state drivers as the purported point of novelty. *E.g.,* EX1002, pp. 49-50 (arguing, for example, that the prior art reviewed by the Examiner allegedly "fail[ed] to teach the Multiplexer circuit comprising first and second tri state driver that enable if a data connection exclusion signal is asserted"); EX1002, pp. 35-36 (similar); EX1003 ¶¶46-50. However, as illustrated by the prior art cited herein—and as confirmed by Dr. Wolfe—tri-state drivers were a well-known component in the field of digital circuit design, including in the design of multiplexors. *See, e.g.,* EX1003, ¶¶27-36.

C. Level of Ordinary Skill in the Art

A person of ordinary skill in the art ("POSITA") relating to the subject matter of the '448 Patent as of August 1, 2003, would have possessed at least a bachelor's degree in electrical engineering or equivalent degree, and three years of work experience in the field of digital circuit design including the use of multiplexors. EX1003, ¶36. A person could also have qualified with more formal education and less technical experience, or vice versa. *Id*.

D. Claim Construction

No formal claim constructions are necessary because "claim terms need only be construed to the extent necessary to resolve the controversy" (*Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011)) and the prior art teaches each limitation under any reasonable construction. Petitioner reserves the right to respond to any constructions offered by Patent Owner or adopted by the Board; and preserves the right to challenge in parallel litigation that the challenged claims fail to satisfy statutory requirements, including on grounds that cannot be raised in this proceeding.

III. OVERVIEW OF PRIOR ART

A. Pixley

Pixley relates to "tri-state multiplexers in a circuit design." EX1004, 1:8-10. "A tri-state multiplexer provides faster performance and consumes less chip area

and power, over a gate-implemented multiplexer." EX1004, 2:63-65. "However, a circuit with a tri-state multiplexer may generate an undesirable situation if not properly designed." EX1004, 2:65-67. For example, "[i]f two or more select lines are enabled with data inputs driving different logic values, the circuit may show unintended functional behavior, consume excessive power, and may be damaged." EX1004, 2:67-3:3. Accordingly, Pixley "provides a method and apparatus to perform checking of tri-state multiplexers to ensure that the tri-state multiplexers are operating in a proper manner." EX1004, 2:60-63; EX1003, ¶51.

To demonstrate the functionality of its invention, Pixley provides FIGS. 5-11, which are diagrams of "typical" tri-state multiplexer (MUX) circuits that "could be located in the circuit model 37 of FIG. 4," and checked for proper operation by Pixley's tri-state multiplexer checker 38. *See* EX1004, 2:24-45, 4:41-65; EX1003, ¶52. For example, "FIG. 9 and FIG. 10 illustrate how nested multiplexers are processed." EX1004, 7:7-8; EX1003, ¶52.

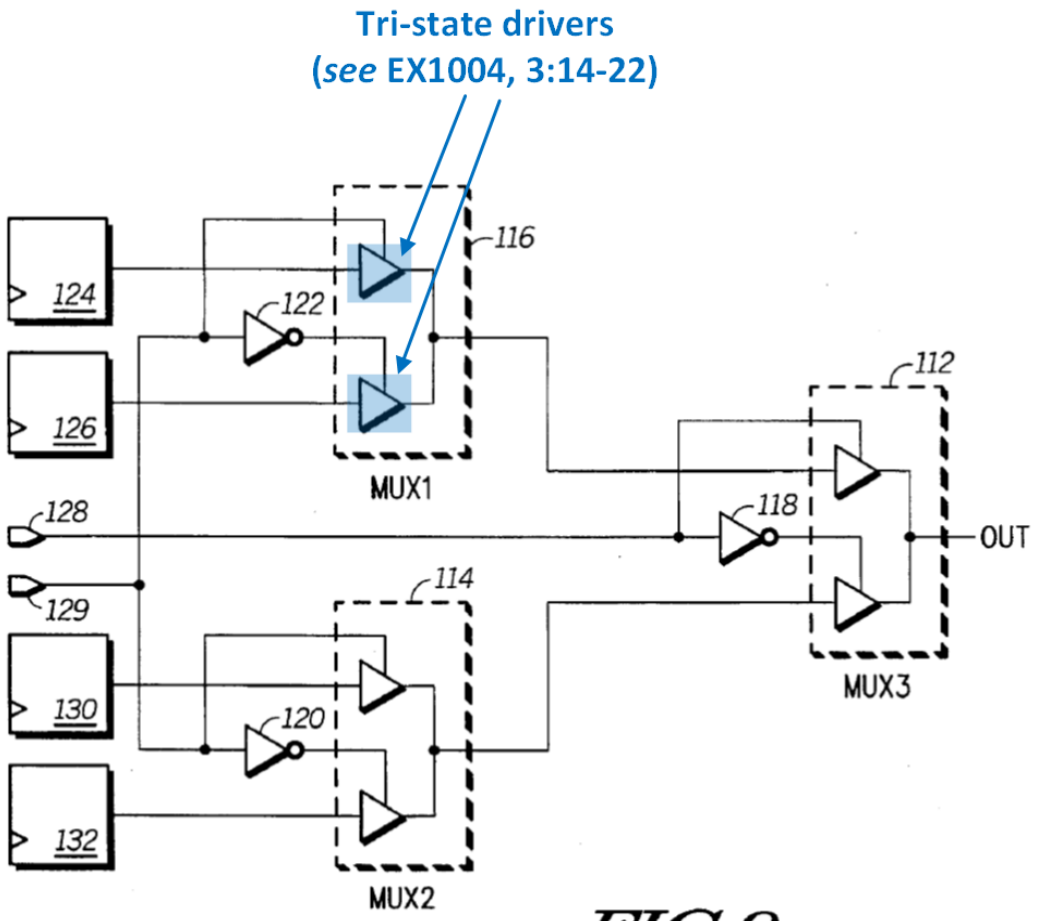


FIG.9

"FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116." EX1004, 7:8-9. Each of these MUXes includes two tri-state drivers. *See* EX1004, FIG. 9, 7:7-14, 3:14-22 (describing the operation of the tri-state drivers included in the described multiplexers). "Each driver [] is enabled only if the corresponding select line (sel-#) is enabled." EX1004, 3:18-19. "When the select line labeled sel-N (wherein N is an integer between 0 and 2 for FIG. 3) is enabled then the [input] value is coupled to the output node OUT." EX1004, 3:19-22. In the example of FIG. 9, the select line of the upper tri-state driver of MUX 116 is

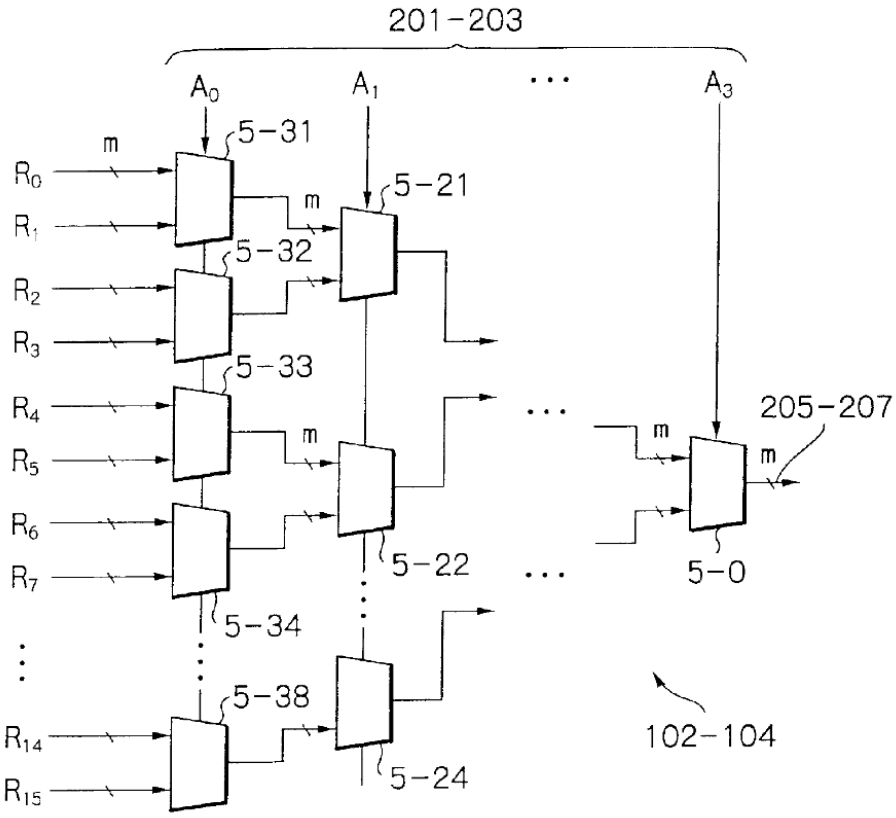
driven by input terminal/pin 129 and the select line of the lower tri-state driver of MUX 116 is driven by the complement (*i.e.*, inverse) of the input terminal/pin 129. *See* EX1004, FIG. 9, 7:7-14; EX1003, ¶53. According to Pixley, the tri-state multiplexer checker 38 would verify the example tri-state MUX design of FIG. 9, because it meets the required conditions. *See* EX1004, 7:14-16; EX1003, ¶53.

B. Watanabe

Watanabe relates generally to "a register read circuit and a microprocessor, which is applicable to, for example, reading out data from a plurality of registers of a register bank." EX1005, [2]. Watanabe claims and discloses improving these registers by "provid[ing] a register read circuit with a structure suitable for implementation, and easy for installation, on an integrated circuit chip." EX1005, [20]; EX1003, ¶54.

To disclose this improvement, though, Watanabe also includes a discussion concerning the then state-of-the-art concerning multiplexors. For example, Watanabe explains that it was known that "[a] 2-to-1 multiplexor of m-bit length is composed of m 2-1 multiplexers of one-bit length." EX1005, [18]. Watanabe also discusses a known "method in which one 16-to-1 multiplexors is used for one operand" and includes a discussion of the known design for such a multiplexor, such as illustrated in Figure 3 from Watanabe, excerpted below:

Fig. 3 PRIOR ART



EX1005, [33], Fig. 3. As illustrated in Figure 3 and explained by Watanabe, the disclosed 16-1 multiplexor is comprised of eight 2-to1 multiplexors 5-31 through 5-38 arranged in a nested pattern. EX1005, [36]-[37], Fig. 3; EX1003, ¶55.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Claim 1

[1.pre] To the extent the preamble is limiting, a combination of Pixley and Watanabe (hereinafter "Pixley-Watanabe") renders it obvious.

Pixley relates to "tri-state multiplexers in a circuit design." EX1004, 1:8-10. As described in §III.A, *supra*, Pixley includes several "typical" tri-state

multiplexer (MUX) circuits in order to demonstrate the operation of its tri-state multiplexer checker. *See* EX1004, 2:24-45, 4:41-65; EX1003, ¶58. For example, "FIG. 9 and FIG. 10 illustrate how nested multiplexers are processed." EX1004, 7:7-8. FIG. 9 includes three 2-to-1 MUXs 112, 114, and 116. *See* EX1004, FIG. 9, 7:11-14; EX1003, ¶58. That is, each multiplexer receives two data inputs (*e.g.*, the output of D flip-flops 124 and 126 provide data inputs to tri-state multiplexer 116) and selects one of the two data inputs for its output. *See* EX1004, FIG. 9, 7:11-14; EX1003, ¶58.

The '448 Patent describes that "[e]ach data connection is preferably capable of transmitting an n-bit data word, where 'n' refers to the number of bits within the data word." EX1001, 2:36-38. The '448 Patent goes on to state that "[a] set of bits, e.g. 128 bits simultaneously transmitted from the same data connection, is hereinafter referred to as a 'data word.'" EX1001, 2:41-43. The '448 Patent does not preclude a "data word" from being one bit. EX1003, ¶59. Yet, even if it did, a POSITA would have at least found it obvious that Pixley's multiplexer would operate with respect to multi-bit data words. EX1003, ¶60.

For example, a POSITA would have understood or at least found obvious that, for certain known use cases, the 2-to-1 multiplexers would have been configured to multiplex m-bit data words. EX1003, ¶60. Specifically, it was known that "[a] 2-to-1 multiplexer of m-bit length is composed of m 2-to-1

multiplexers of one-bit length." *See, e.g.*, EX1005, [0018]. Further, it was known that several m-bit 2-to-1 multiplexers could be nested, similar to the configuration shown in Pixley's FIG. 9. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037]. Because it would have been obvious that each of the connections in such a configuration of Pixley's multiplexor would have thus transmitted a "set of bits," those connections would be transmitting "data words," as that term is broadly defined in the '448 Patent. *See* EX1001, 2:41-43; EX1003, ¶60.

One known use case of such a configuration was the selection and transmission of an operand—which Watanabe describes as a "word"—from a selected register in a register bank for transmission to and use in an arithmetic and logical unit (ALU). *See* EX1005, FIG. 4, [0006] ("This is because the instruction word is also 32 bits or 64 bits long on such a processor and this word length is long enough for specifying the operands"), [0043]; EX1003, ¶61. Thus, a POSITA would have understood or at least found obvious that, in m-bit processing applications in which m-bit data must, for example, be read from registers or memory, each of Pixley's tri-state multiplexors 112, 114, and 116 would have been configured as an m-bit multiplexer composed of m one-bit multiplexers, one for each bit of data—effectively stacking a set of the multiplexer circuits illustrated in FIG. 9. EX1003, ¶61. A POSITA would have been motivated to use m-bit

multiplexors in m-bit processing applications as such applications demand the ability to process m-bit data words. EX1003, ¶62.

Implemented in this way, a POSITA would have understood and found obvious that Pixley-Watanabe provides ***a circuit*** [*e.g.*, the nested multiplexer circuit illustrated in Pixley's FIG. 9] ***for multiplexing a plurality of data words*** [*e.g.*, the m-bit data words input into each of MUXs 112, 114, and 116] ***including a first data word*** [*e.g.*, data input 124 to tri-state MUX 116] ***and a second data word*** [*e.g.*, the m-bit data word output by tri-state MUX 114 and input into tri-state MUX 112], as recited in [1.pre]. EX1003, ¶63.

[1.a] Pixley-Watanabe renders obvious Element [1.a].

With respect to FIG. 9, Pixely describes that "[d]ata inputs and control/select signals to the MUXes 112, 114, and 116 are provided via four D flip-flops 124, 126, 130, and 132 and via two input terminals/pins 128 and 129." EX1004, 7:11-14. Further, as illustrated in FIG. 9, the outputs of tri-state MUXs 114 and 116 are inputs to tri-state MUX 112, connecting tri-state MUX 112 to each of data inputs 124, 126, 130, and 132 via tri-state MUXs 114 and 116. *See* EX1004, FIG. 9; EX1003, ¶65-66.

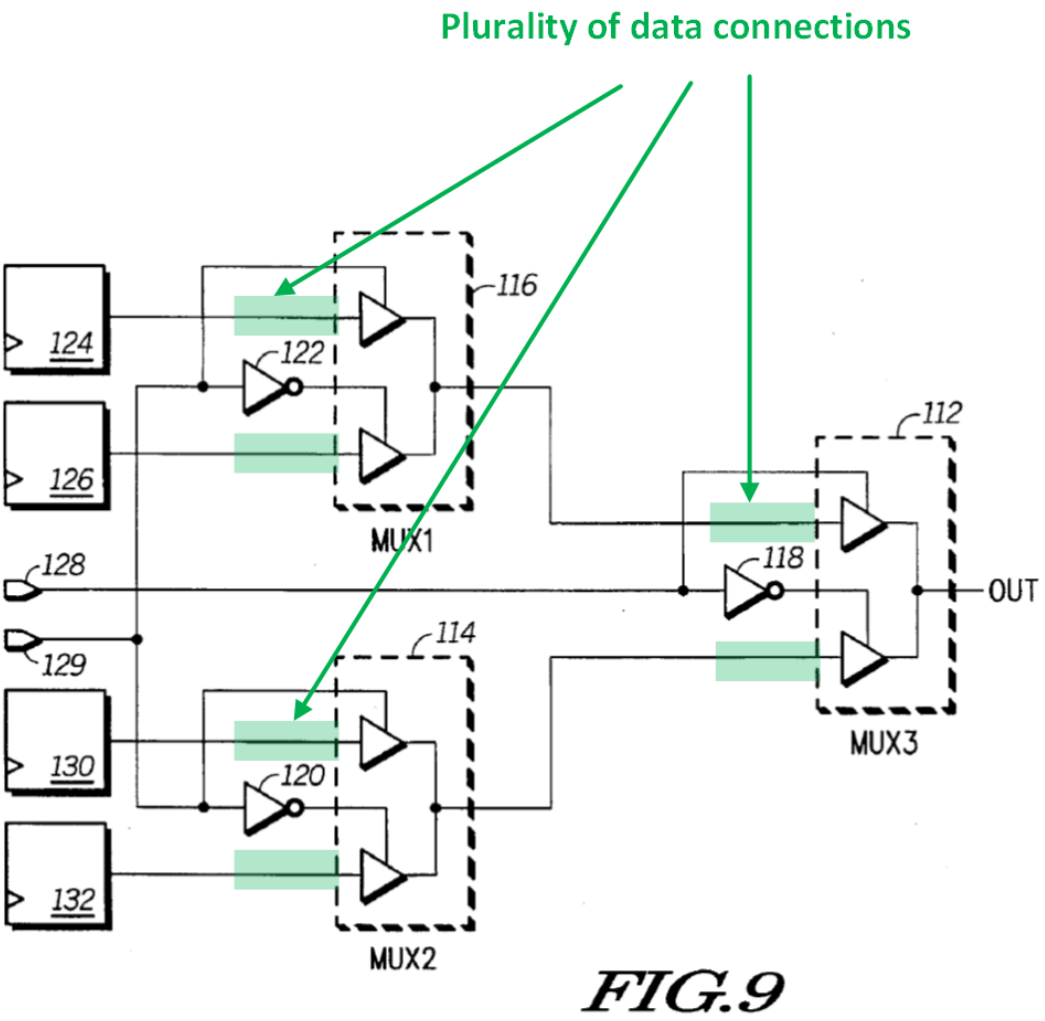


FIG.9

Therefore, a POSITA would have found obvious that Pixley-Watanabe's nested multiplexers of FIG. 9 included ***a plurality of data connections*** [*e.g.*, the data inputs to each of tri-state MUXs 112, 114, and 116], as recited in [1.a]. EX1003, ¶67.

[1.b] Pixley-Watanabe renders obvious Element [1.b].

"FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116." EX1004, 7:8-9. Each of these MUXes include two tri-state drivers. *See* EX1004,

FIG. 9, 7:7-14, 3:14-22 (describing the operation of the tri-state drivers included in the described multiplexors). "Each driver [] is enabled only if the corresponding select line (sel-#) is enabled." EX1004, 3:18-19. "When the select line labeled sel-N (wherein N is an integer between 0 and 2 for FIG. 3) is enabled then the [input] value is coupled to the output node OUT." EX1004, 3:19-22; EX1003, ¶69.

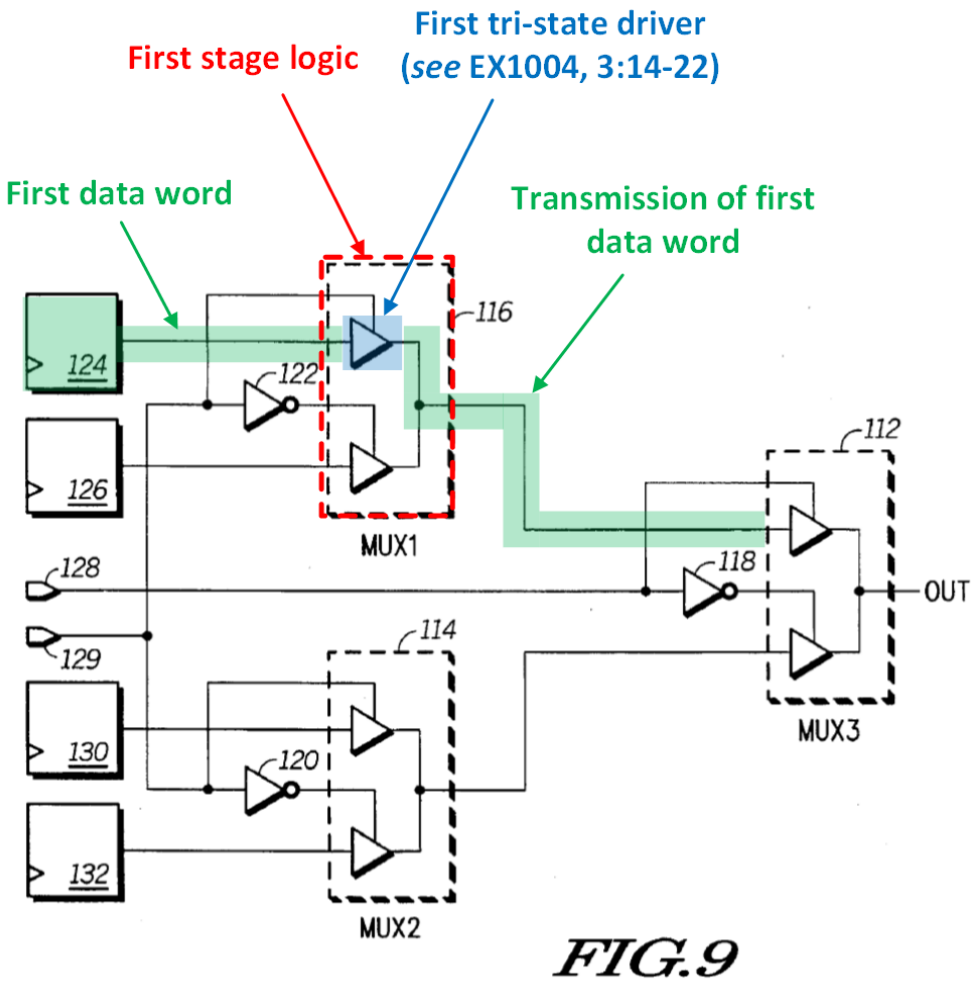


FIG.9

When the select signal input on terminal 129 is enabled (*i.e.*, a logic high), the first/upper tri-state driver of tri-state MUX 116 (highlighted above in blue) is

enabled, and the data word input to the first/upper tri-state driver is coupled to the output of tri-state MUX 116. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶70. Correspondingly, the lower tri-state driver of tri-state MUX 116 receives a complement of the select signal input on terminal 129 from inverter 122 and therefore is disabled. *See id.*

Therefore, a POSITA would have found obvious that Pixley-Watanabe's nested multiplexers of FIG. 9 included ***first stage logic*** [*e.g.*, tri-state MUX 116] ***having a first tristate driver*** [*e.g.*, the upper tri-state driver of tri-state MUX 116, highlighted in blue above]***, the first tristate driver configured to receive the first data word from one of the connections*** [*e.g.*, the m-bit data word received from the m D flip-flops 124] ***and to transmit the first data word received*** [*e.g.*, the upper tri-state driver transmits the m-bit data word received from the m D flip-flops 124 when the select signal input on terminal 129 is enabled], as recited in [1.b]. EX1003, ¶71.

[1.c.i] Pixley-Watanabe renders obvious Element [1.c.i].

As discussed with respect to [1.b], "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶73.

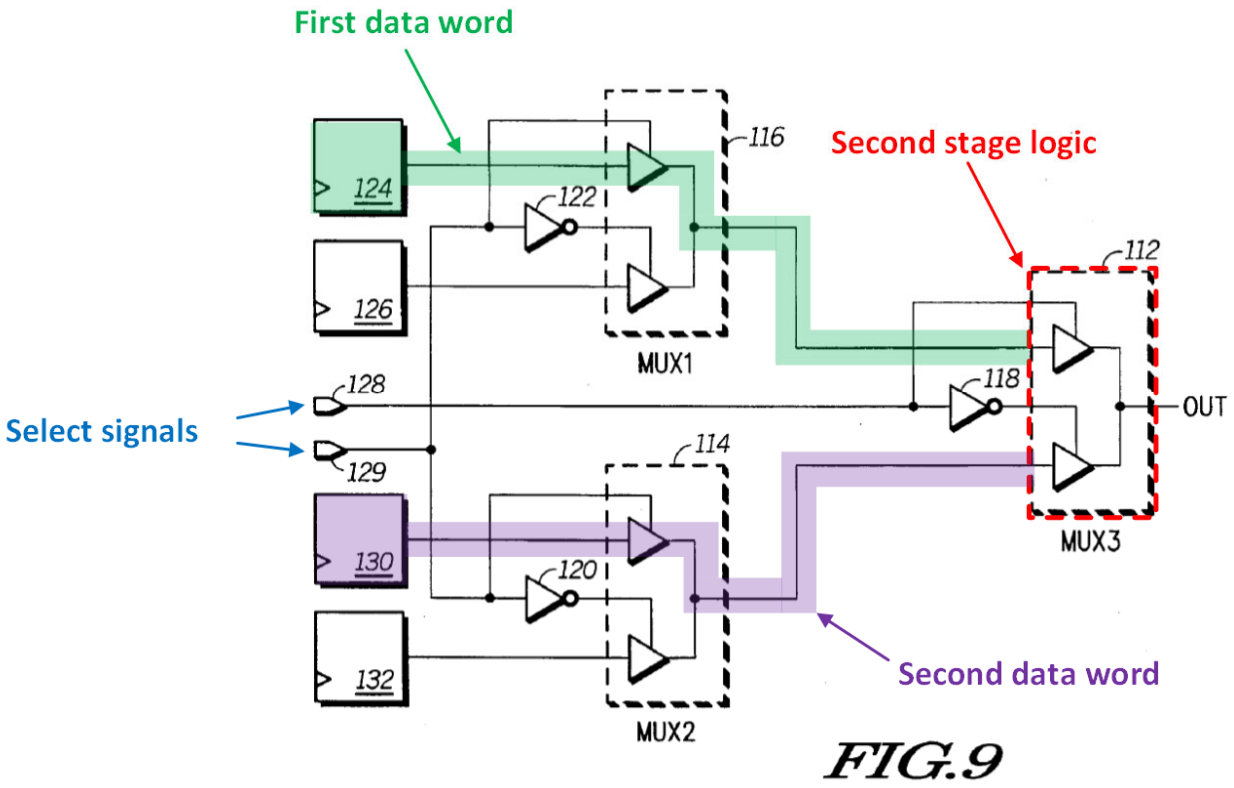


FIG.9

When the select signal input on terminal 129 is enabled (*i.e.*, a logic high), the upper tri-state driver of tri-state MUX 114 is enabled, and the second data word (highlighted in purple above) input to the upper tri-state driver is coupled to the output of tri-state MUX 114 and correspondingly to one of the inputs of tri-state MUX 112. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶74. And, as described with respect to Element [1.b], *supra*, when the select signal input on terminal 129 is enabled (*i.e.*, a logic high), the first/upper tri-state driver of tri-state MUX 116 is enabled, and the first data word (highlighted in green above) input to the first/upper tri-state driver is coupled to the output of tri-state MUX 116 and correspondingly to the other input of tri-state MUX 112. *See id.*

Therefore, a POSITA would have found obvious that Pixley-Watanabe's nested multiplexers of FIG. 9 included ***second stage logic*** [*e.g.*, tri-state MUX 112] ***configured to receive the first data word from the first stage logic*** [*e.g.*, the tri-state MUX 112 receives the m-bit data word of the m D flip-flops 124 from the tri-state MUX 116 when select signal input on terminal 129 is enabled] ***and to receive the second data word from another of the plurality of data connections*** [*e.g.*, the tri-state MUX 112 receives the m-bit data word of the m D flip-flops 130 from the tri-state MUX 114 when select signal input on terminal 129 is enabled]***, the second stage logic configured to select for transmission one of the first data word and the second data word based upon a set of select signals*** [*e.g.*, the tri-state MUX 112 selects between the data words output by each of tri-state MUX 114 and tri-state MUX 116 based on two select signals: the signal input on terminal/pin 128 input to the upper tri-state driver and the signal output by inverter 118 and input into the lower tristate driver]***, the second stage logic configured to transmit the data word selected for transmission by the second stage logic*** [*e.g.*, "OUT" of tri-state MUX 112 transmits the selected data word], as recited in [1.c.i]. EX1003, ¶75.

[1.c.ii] Pixley-Watanabe renders obvious Element [1.c.ii].

As discussed with respect to [1.b]. "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that

are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶77.

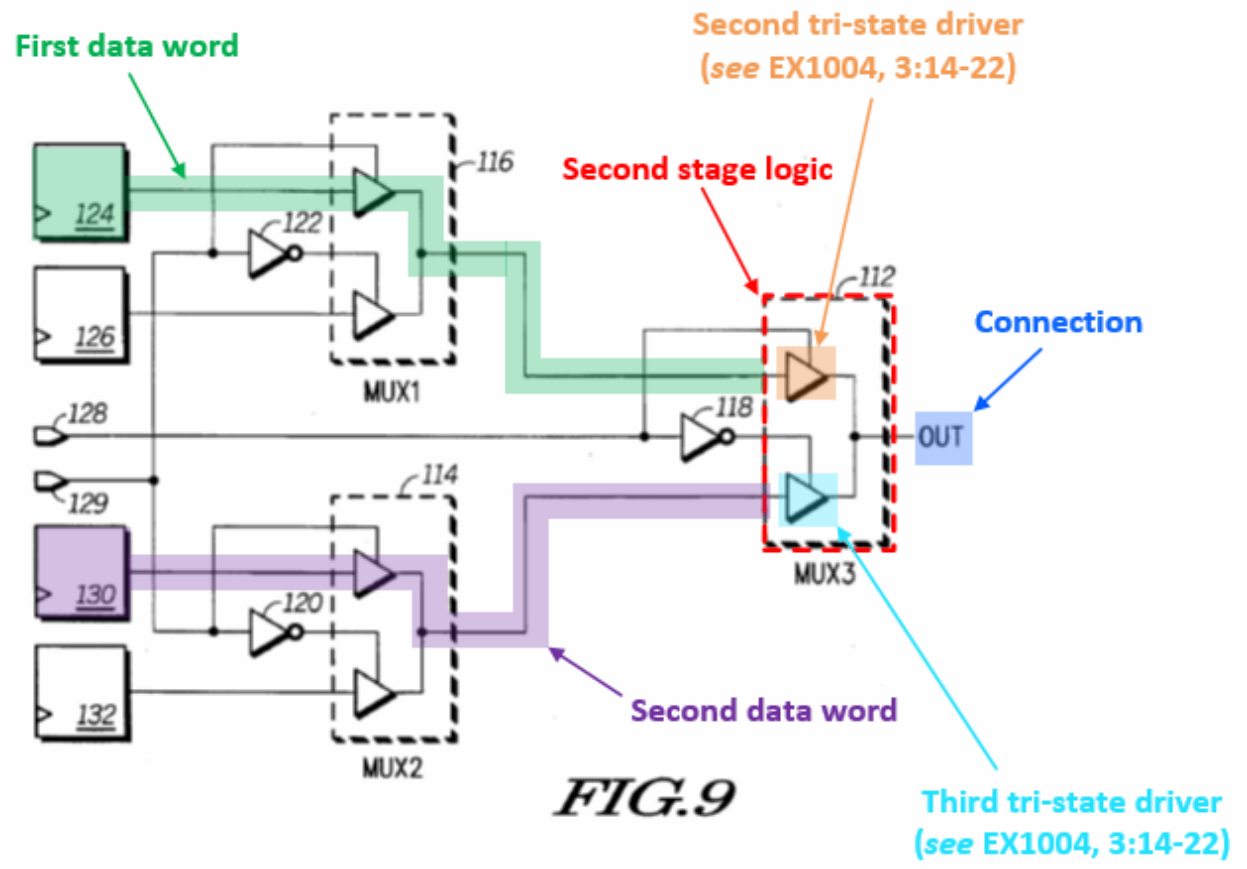


FIG.9

When the select signal input on terminal 128 is enabled (*i.e.*, a logic high), the second/upper tri-state driver of tri-state MUX 112 is enabled, and the first data word (highlighted in green above) input to the upper tri-state driver is coupled to the output OUT of tri-state MUX 112. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶78. Correspondingly, the third/lower tri-state driver of tri-state MUX 112 receives a complement of the select signal input on terminal 128 via inverter 118,

such that when the select signal input on terminal 128 is enabled, the output of inverter 118 is disabled (*i.e.*, a logic low) and the third/lower tri-state driver of tri-state MUX 112 is disabled. *See id.*

On the other hand, when the select signal input on terminal 128 is disabled (*i.e.*, a logic low), the second/upper tri-state driver of tri-state MUX 112 is disabled. *See id.* And, correspondingly, the third/lower tri-state driver of tri-state MUX 112 receives a complement of the select signal input on terminal 128 via inverter 118, so when the select signal input on terminal 128 is disabled, the output of inverter 118 is enabled (*i.e.*, a logic high) and the third/lower tri-state driver of tri-state MUX 112 is enabled such that the second data word (highlighted in purple above) input to the lower tri-state driver is coupled to the output OUT of tri-state MUX 112. *See id.*

Therefore, a POSITA would have found obvious that Pixley-Watanabe's tri-state MUX 112 [the second stage logic] included ***a connection*** [*e.g.*, output OUT of tri-state MUX 112]***, a second tristate driver*** [*e.g.*, the upper tri-state driver of tri-state MUX 112, highlighted in orange above]***, and a third tristate driver*** [*e.g.*, the lower tri-state driver of tri-state MUX 112, highlighted in light blue above]***, the second tristate driver having an output electrically coupled to an output of the third tristate driver*** [*e.g.*, the output of the upper and lower tri-state drivers of tri-state MUX 112 are coupled together at OUT]***, the second tristate driver***

configured to receive the first data word from the first tristate driver [*e.g.*, the upper tri-state driver of tri-state MUX 112 receives the first data word from the upper tri-state driver of tri-state MUX 116 when the select signal input on terminal/pin 129 is enabled] ***and to drive the connection of the second stage logic with the first data word if the first data word is selected for transmission by the second stage logic*** [*e.g.*, the data word received from the tri-state MUX 116 to the upper tri-state driver of tri-state MUX 112 is coupled to OUT for transmission when the select signal input on terminal/pin 128 is enabled]***, the third tristate driver configured to receive the second data word and to drive the connection of the second stage logic with the second data word if the second data word is selected for transmission by the second stage logic*** [*e.g.*, the data word received from the tri-state MUX 114 to the lower tri-state driver of tri-state MUX 112 is coupled to OUT for transmission when the select signal output from inverter 118 is enabled, which is when the select signal input on terminal/pin 128 is disabled], as recited in [1.c.ii]. EX1003, ¶79.

B. Claim 2

[2] Pixley-Watanabe renders Claim [2] obvious.

As discussed with respect to [1.b]. "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that are enabled only if the corresponding select line is enabled and which couple the

input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶81.

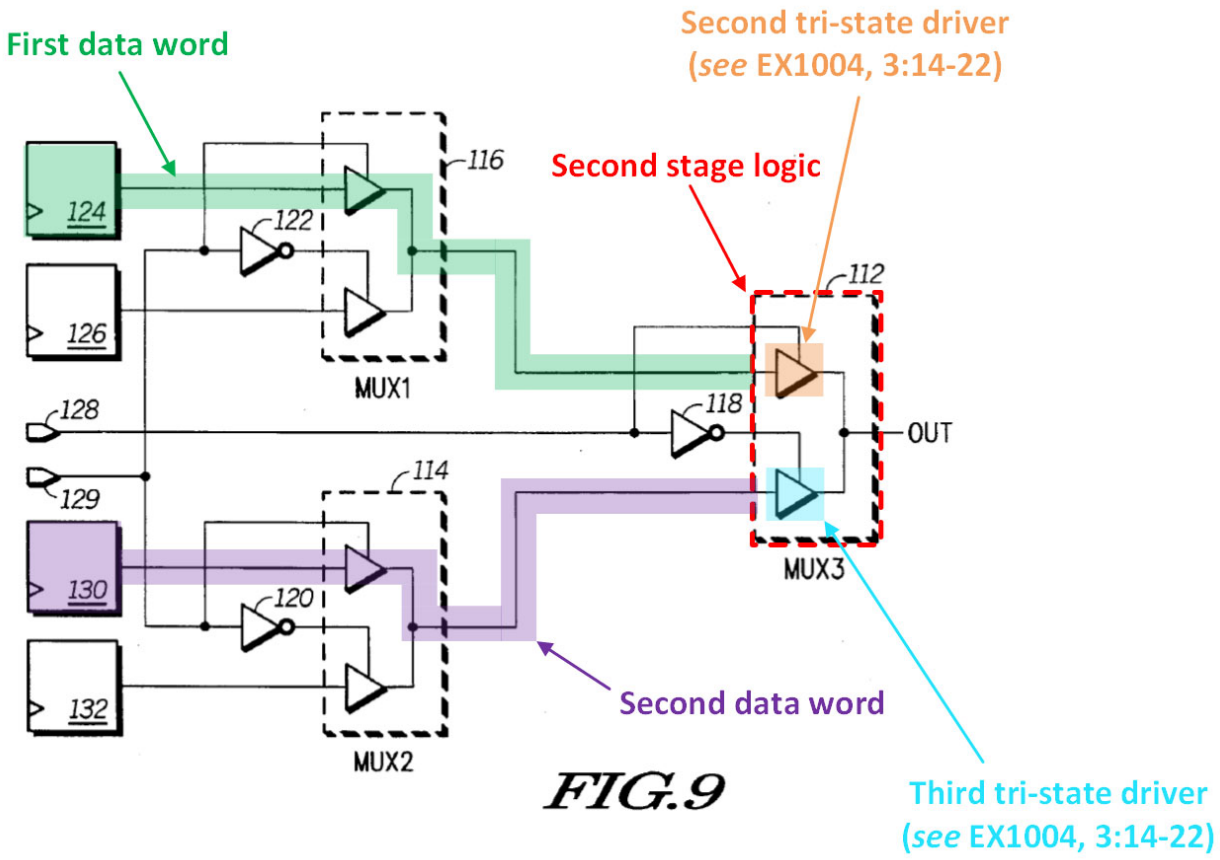
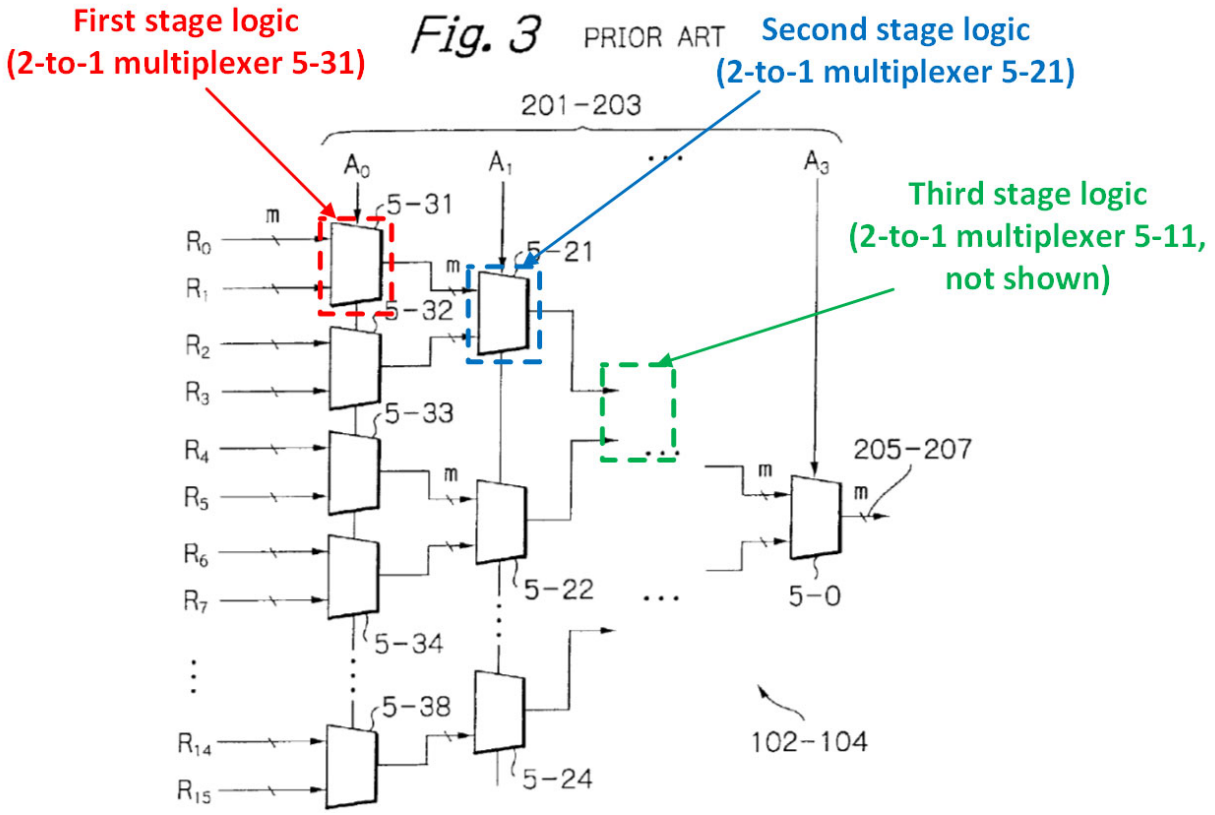


FIG.9

Pixley does not limit to where the output of the tri-state MUX 112 is transmitted. *See generally* EX1004, 7:7-8:3; EX1003, ¶82. As described with respect to Element [1.pre], *supra*, it was known that several m-bit 2-to-1 multiplexers could be nested, similar to the configuration shown in Pixley's FIG. 9. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037]. In one example of nested multiplexers described by Watanabe, the output of a second stage MUX (*e.g.*, 2-to-1 multiplexer 5-21) is transmitted to the input of a third stage MUX (*e.g.*, 2-to-1 multiplexer 5-

11). *See* EX1005, FIG. 3, [0036]-[0037]. This configuration was useful when the nested/cascading multiplexers were required to select between more than four data inputs. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037].



Therefore, a POSITA would have found obvious that, in Pixley-Watanabe's nested multiplexers of FIG. 9, ***the second stage logic*** [*e.g.*, multiplexer 112] ***is further configured to transmit, to a third stage logic*** [*e.g.*, a subsequent stage tri-state multiplexer in a larger nested multiplexer circuit with more than four data inputs]***, the data word selected for transmission by the second stage logic*** [*e.g.*, the output of tri-state multiplexer would have been connected to the input of the subsequent stage tri-state multiplexer], as recited in Claim [2]; EX1003, ¶83.

C. Claim 3

[3] Pixley-Watanabe renders obvious Claim [3].

As described with respect to [1.c.ii], *supra*, the tri-state MUX 112 is configured to output the data word received from either tri-state MUX 114 or tri-state MUX 116, depending on the state of the select signals output by terminal/PIN 128 and inverter 118. *See* EX1004, FIG. 9, 7:7-14, 3:14-22; EX1003, ¶85.

Further, as described with respect to [1.pre], *supra*, it was known that several m-bit 2-to-1 multiplexers could be nested, similar to the configuration shown in Pixley's FIG. 9. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037]. One known use case of such a configuration was the output of an operand from a selected register in a register bank for transmission to and use in an arithmetic and logical unit (ALU). *See* EX1005, FIG. 4, [0043]; EX1003, ¶86. In this example use case, "[t]he operand output . . . that has been readout is interconnected to be sent, for example, to the arithmetic and logical unit (ALU) via a system bus . . . ." EX1005, [0043]; *see also* EX1006, FIG. 9, [0021], [0028]-[0029], [0034] (illustrating and describing "4-to-1 Multiplexer (MUX) formed with cascaded buses" and tri-state drivers); EX1003, ¶86.

Accordingly, a POSITA would have at least found it obvious that, in Pixley-Watanabe's nested multiplexers of FIG. 9, ***the second stage logic*** [*e.g.*, tri-state MUX 112] ***is further configured to transmit, to a system bus*** [*e.g.*, a system bus

connecting the output OUT of tri-state MUX 112 to an arithmetic and logical unit (ALU)]***, the data word selected for transmission by the second stage logic*** [*e.g.*, either the data word output by tri-state MUX 114 or the data word output by tri-state MUX 116, depending on the state of the select signals output by terminal/PIN 128 and inverter 118], as recited in Claim [3]; EX1003, ¶87.

D. Claim 4

[4.pre] Pixley-Watanabe renders obvious Element [4.pre] for the same reasons described above with respect to Element [1.pre].

See Element [1.pre], *supra*; EX1003, ¶88.

[4.a] Pixley-Watanabe renders obvious Element [4.a] for the same reasons described above with respect to Element [1.a].

See Element [1.a], *supra*; EX1003, ¶89.

[4.b] Pixley-Watanabe renders obvious Element [4.b].

As discussed with respect to [1.b], "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶91-92.

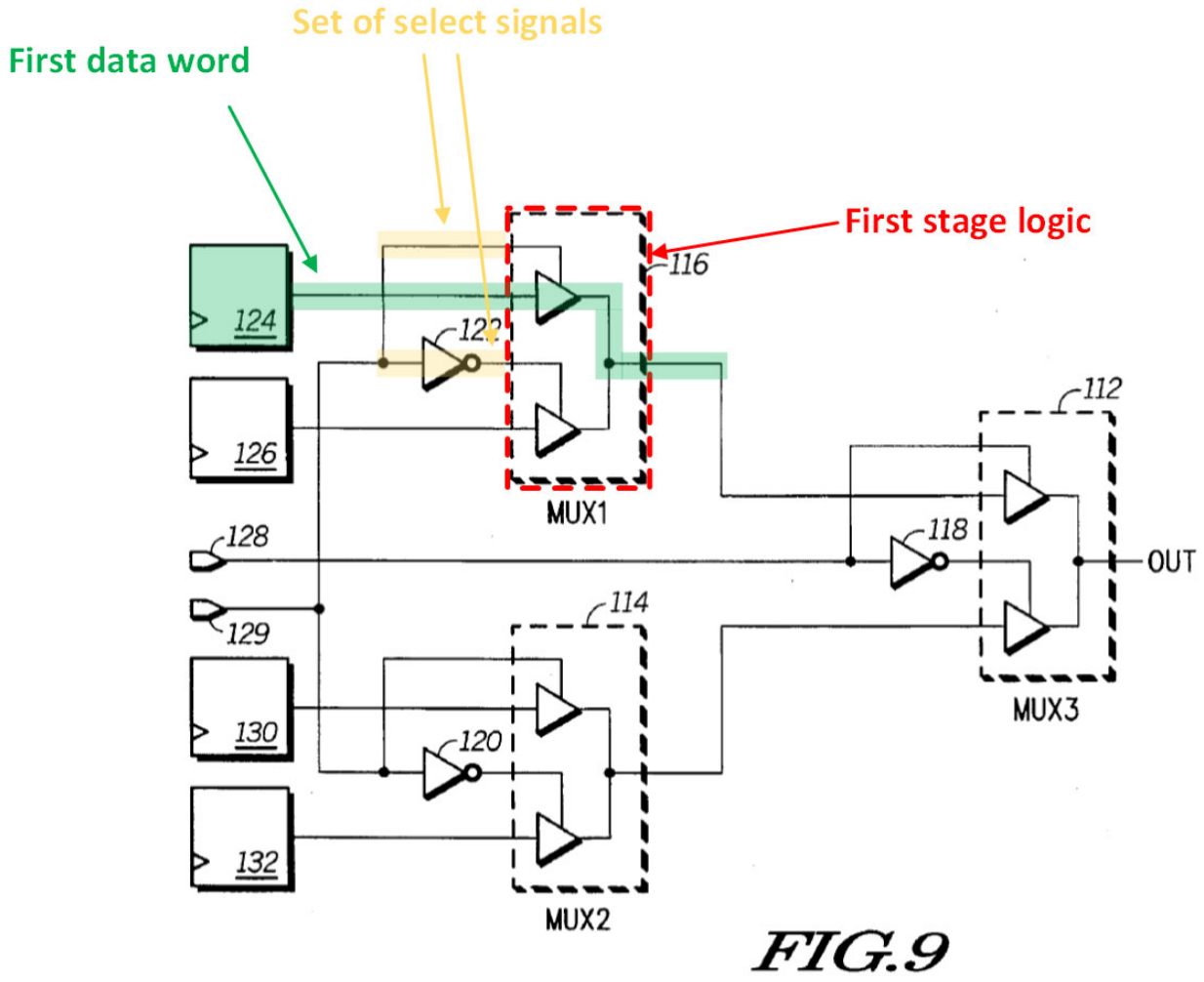


FIG.9

Therefore, a POSITA would have found obvious that Pixley-Watanabe's nested multiplexers of FIG. 9 included ***first stage logic*** [*e.g.*, tri-state MUX 116] ***configured to receive the first data word from one of the connections*** [*e.g.*, the m-bit data word received from the m D flip-flops 124] ***and to transmit the first data word received*** [*e.g.*, the upper tri-state driver transmits the m-bit data word received from the m D flip-flops 124 when the select signal input on terminal 129

is enabled] ***based on a set of select signals*** [*e.g.*, the select signal input on terminal 129 and the complement output by inverter 122], as recited in [1.b]. EX1003, ¶93.

[4.c.i] Pixley-Watanabe renders obvious Element [4.c.i].

As described with respect to Element [1.b], *supra*, each of the tri-state MUXs 112, 114, and 116 include two tri-state drivers. *See* EX1004, FIG. 9, 7:7-14, 3:14-22 (describing the operation of the tri-state drivers included in the described multiplexors). "When the select line labeled sel-N (wherein N is an integer between 0 and 2 for FIG. 3) is enabled then the [input] value is coupled to the output node OUT." EX1004, 3:19-22; EX1003, ¶95.

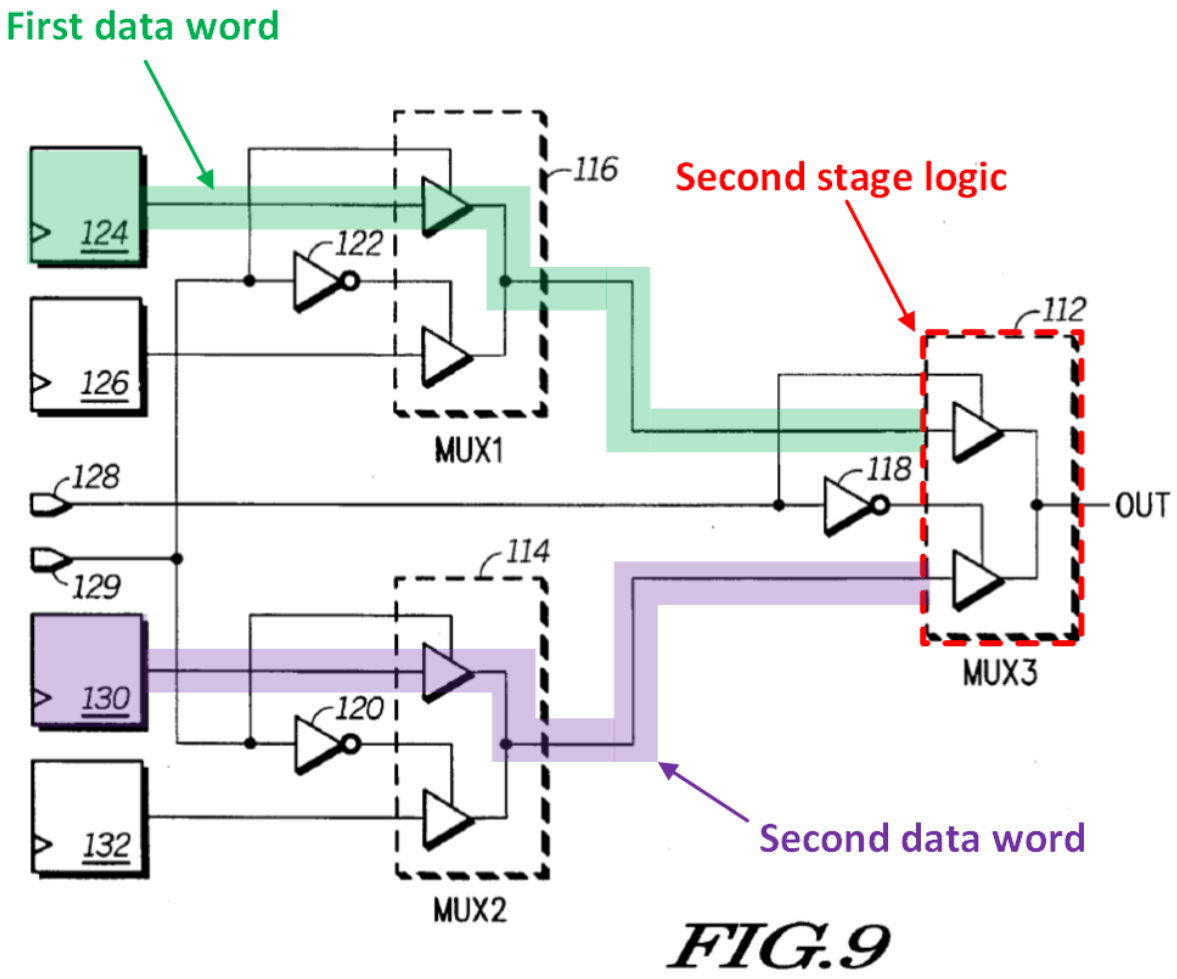


FIG.9

When the select signal input on terminal 129 is enabled (*i.e.*, a logic high), the upper tri-state driver of tri-state MUX 114 is enabled, and the second data word (highlighted in purple above) input to the upper tri-state driver is coupled to the output of tri-state MUX 114 and correspondingly to one of the inputs of tri-state MUX 112. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶96. And, as described with respect to Element [1.b], *supra*, when the select signal input on terminal 129 is enabled (*i.e.*, a logic high), the first/upper tri-state driver of tri-state MUX 116 is enabled, and the first data word (highlighted in green above) input to the

first/upper tri-state driver is coupled to the output of tri-state MUX 116 and correspondingly to the other input of tri-state MUX 112. *See id.*

Therefore, a POSITA would have found obvious that Pixley-Watanabe's nested multiplexers of FIG. 9 included ***second stage logic*** [*e.g.*, tri-state MUX 112] ***configured to receive the first data word from the first stage logic*** [*e.g.*, the tri-state MUX 112 receives the m-bit data word of the m D flip-flops 124 from the tri-state MUX 116 when select signal input on terminal 129 is enabled] ***and to select a selected data word between the first data word*** [*e.g.*, the m-bit data word received from the m D flip-flops 124 and output by tri-state MUX 116 when select signal s129 is enabled] ***and a second data word received from another of the plurality of data connections*** [*e.g.*, the tri-state MUX 112 receives the m-bit data word of the m D flip-flops 130 from the tri-state MUX 114 when select signal input on terminal 129 is enabled] ***based upon a set of select signals*** [*e.g.*, the tri-state MUX 112 selects between the data words output by each of tri-state MUX 114 and tri-state MUX 116 based on two select signals: the signal input on terminal/pin 128 input to the upper tri-state driver and the signal output by inverter 118 and input into the lower tristate driver], as recited in [1.c.i]. EX1003, ¶97.

[4.c.ii] Pixley-Watanabe renders obvious Element [4.c.ii].

As discussed with respect to [1.b]. "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that

are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶99.

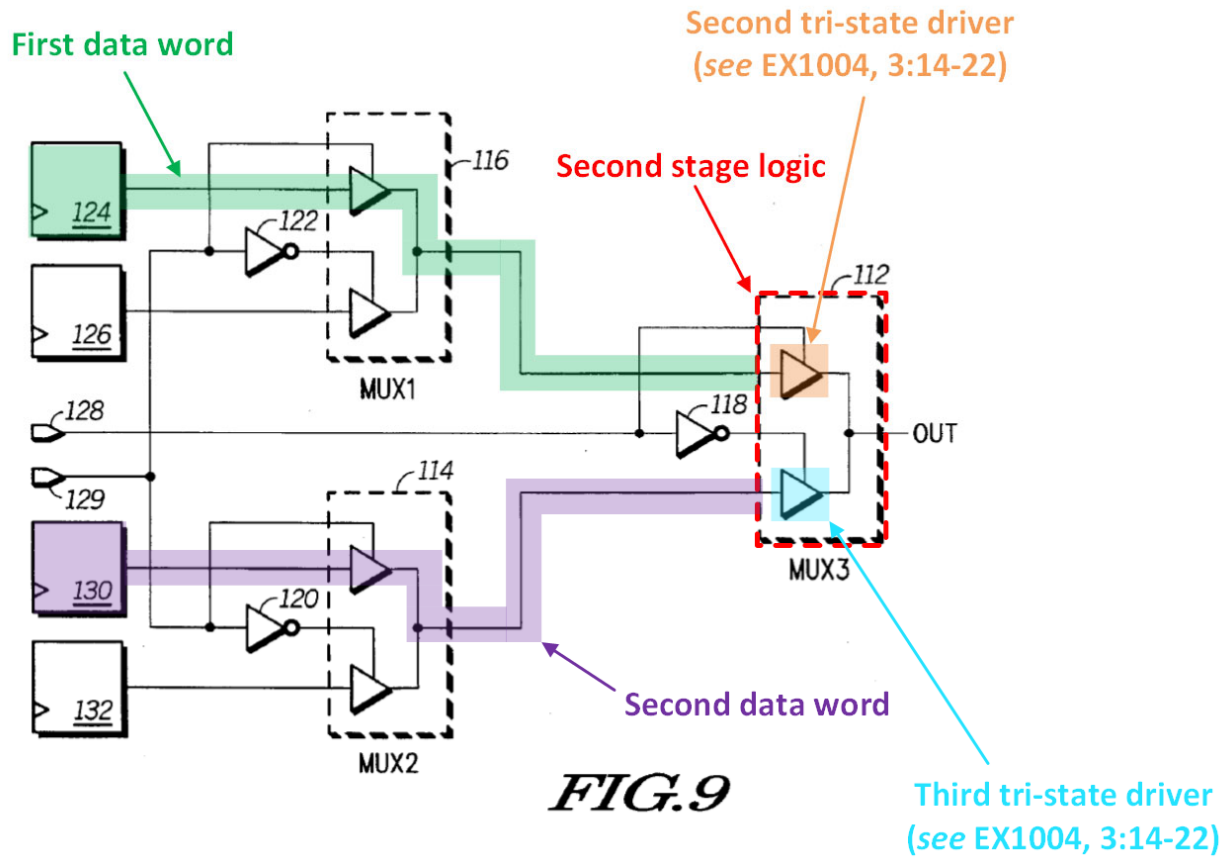


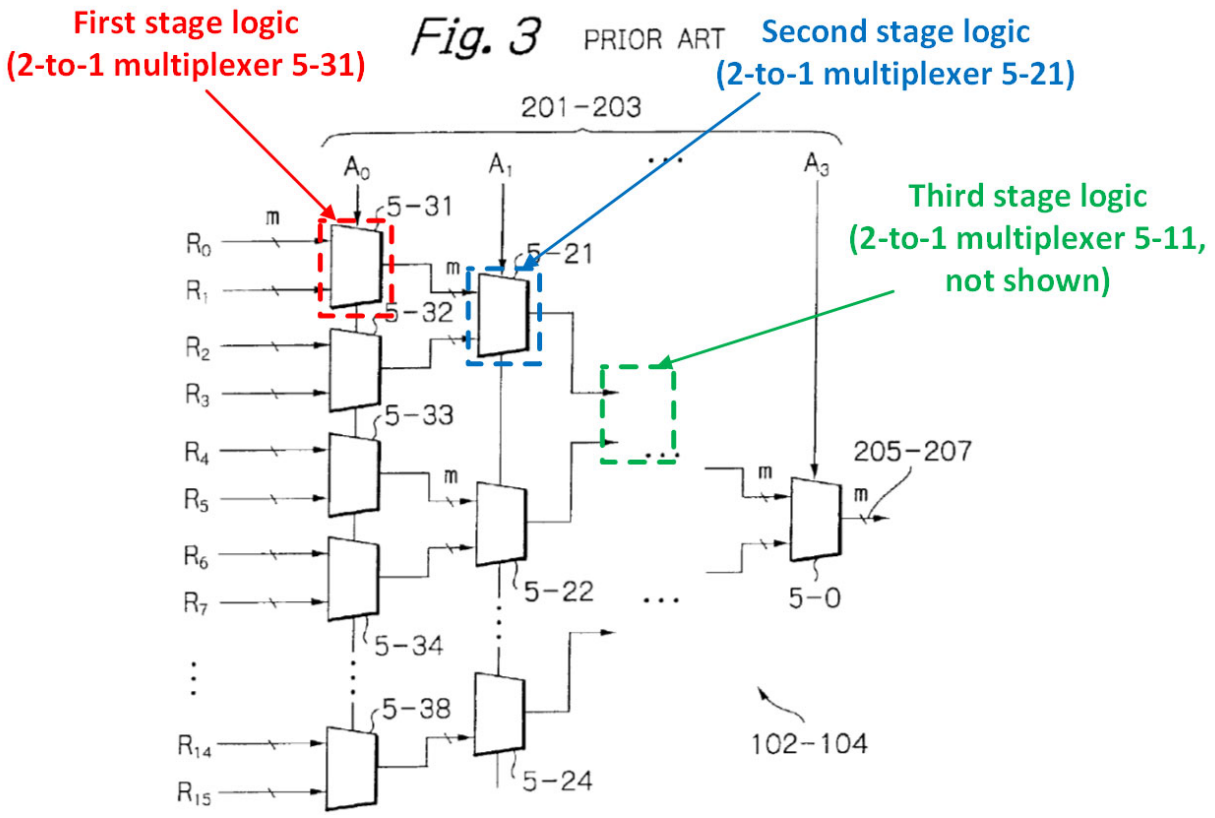
FIG.9

As described with respect to Element [1.c.i], *supra*, and shown in FIG. 9, the select signals for the tri-state MUX 112 are the input terminal/pin 128 and its complement as output by inverter 118. *See* EX1004, FIG. 9, 7:7-14; EX1003, ¶100. When the input terminal/pin 128 is enabled (*i.e.*, logic level high), the upper tri-state driver of MUX 112 is enabled, the lower tri-state driver of MUX 112 is disabled, and the MUX 112 passes the first data word from MUX 116 to output

OUT via the upper tri-state driver. *See* EX1004, FIG. 9, 3:14-22, 7:7-14; EX1003, ¶100. Conversely, when input terminal/pin 128 is disabled (*i.e.*, logic level low), the upper tri-state driver of MUX 112 is disabled, the lower tri-state driver of MUX 112 is enabled, and the MUX 112 passes the second data word from MUX 114 to output OUT via the lower tri-state driver. *See id.*

A POSITA would have understood or found obvious that the tri-state drivers described by Pixley would have increased a signal strength of a data word when they were enabled and coupled the data word to the output of the corresponding tri-state multiplexer. EX1003, ¶101. It was known that tri-state drivers were programmable "to be either off (high output impedence [sic]) or on (able to pass and amplify the applied data input signal)." EX1007, [0074]. Indeed, one of the primary purposes of a "driver" was generally known to be amplification for the purpose of signal transmission. *See, e.g.*, EX1008, 1:14-23 ("One of the circuit designs used in MOS LSI devices is a tristate driver circuit, i.e., a circuit which . . . interfaces with and functions to drive output loads, normally external to the MOS LSI, in response to low power signal sources within the MOS LSI"); EX1009, 1:64-2:5 (describing "an improved CMOS off-chip driver circuit which interfaces between a first circuit with a given supply voltage and a second circuit with a supply voltage having a magnitude greater than that of the given supply voltage").

Pixley does not limit to where the output of the tri-state MUX 112 is transmitted. *See generally* EX1004, 7:7-8:3; EX1003, ¶102. As described with respect to Element [1.pre] and Claim [3], *supra*, it was known that several m-bit 2-to-1 multiplexers could be nested, similar to the configuration shown in Pixley's FIG. 9. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037]. In one example of nested multiplexers described by Watanabe, the output of a second stage MUX (*e.g.*, 2-to-1 multiplexer 5-21) is transmitted to the input of a third stage MUX (*e.g.*, 2-to-1 multiplexer 5-11). *See* EX1005, FIG. 3, [0036]-[0037]. This configuration was useful when the nested/cascading multiplexers were required to select between more than four data inputs. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037]; EX1003, ¶102.



Therefore, a POSITA would have found obvious that, in Pixley-Watanabe's nested multiplexers of FIG. 9, ***the second stage logic*** [*e.g.*, the tri-state MUX 112] ***[was] configured to transmit the selected data word to a third stage logic*** [*e.g.*, in a larger nested multiplexer, the output of tri-state MUX 112 would be connected to a subsequent stage multiplexer] ***and to increase a signal strength of the first data word when the first data word is transmitted, if the first data word is selected*** [*e.g.*, when the first/upper tri-state driver is enabled and couples its input with the first data word to OUT, the tristate driver amplifies the first data word], as recited in Element [4.c.ii]. EX1003, ¶103.

E. Claim 5

[5.pre] Pixley-Watanabe renders obvious Element [5.pre] for the same reasons described above with respect to Element [1.pre].

See Element [1.pre], *supra*; EX1003, ¶104.

[5.a] Pixley-Watanabe renders obvious Element [5.a] for the same reasons described above with respect to Element [1.a].

See Element [1.a], *supra*; EX1003, ¶105.

[5.b] Pixley-Watanabe renders obvious Element [5.b] for the same reasons described above with respect to Element [4.b].

See Element [4.b], *supra*; EX1003, ¶106.

[5.c] Pixley-Watanabe renders obvious Element [5.c] for the same reasons described above with respect to Elements [4.c.i] and [4.c.ii].

See Elements [4.c.i], [4.c.ii], *supra*; EX1003, ¶107.

[5.d] Pixley-Watanabe renders obvious Element [5.d].

As described with respect to Element [1.b], *supra*, each of the tri-state MUXs 112, 114, and 116 include two tri-state drivers. *See* EX1004, FIG. 9, 7:7-14, 3:14-22 (describing the operation of the tri-state drivers included in the described multiplexors); EX1003, ¶109.

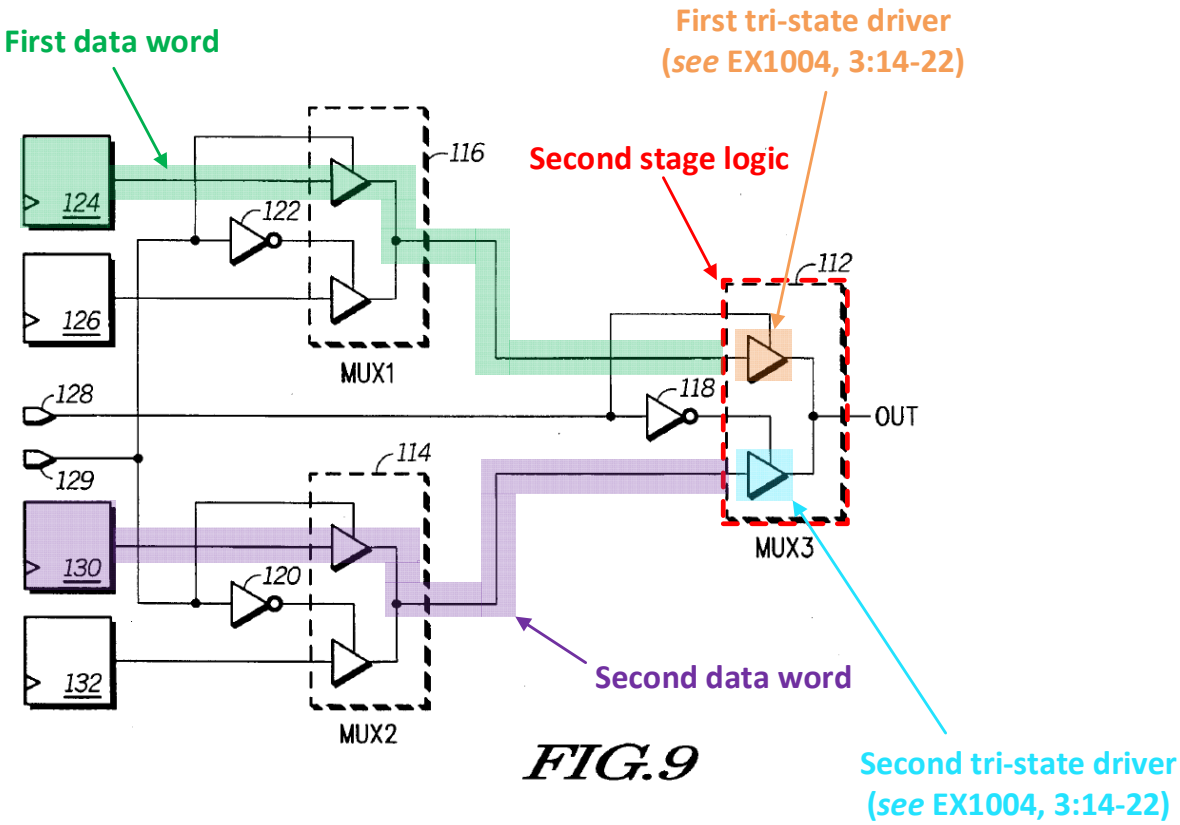


FIG.9

When the select signal input on terminal 128 is asserted (*i.e.*, a logic high), the first/upper tri-state driver of tri-state MUX 112 is enabled, and the first data word (highlighted in green above) input to the upper tri-state driver is coupled to the output OUT of tri-state MUX 112. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶110. Correspondingly, the second/lower tri-state driver of tri-state MUX 112 receives a complement of the select signal input on terminal 128 via inverter 118, such that when the select signal input on terminal 128 is asserted, the output of inverter 118 is deasserted (*i.e.*, a logic low) and the second/lower tri-state driver of tri-state MUX 112 is disabled. *See id.*

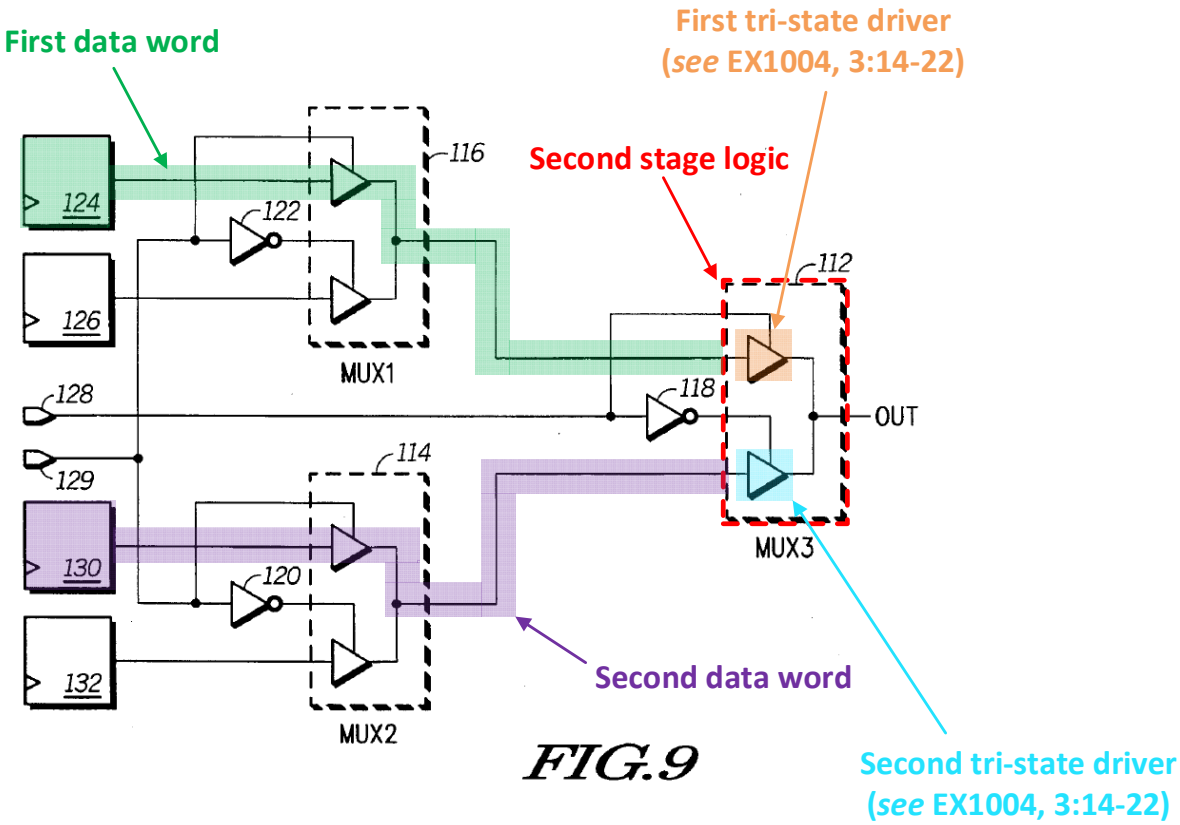


FIG.9

When the select signal output by the inverter 118 is asserted (*i.e.*, a logic high), the second/lower tri-state driver of tri-state MUX 112 is enabled, and the second data word (highlighted in purple above) input to the lower tri-state driver is coupled to the output OUT of tri-state MUX 112. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶¶112-113.

Therefore, a POSITA would have found obvious that Pixley-Watanabe's tri-state MUX 112 [the second stage logic] included ***a first tristate driver*** [*e.g.*, the first/upper tri-state driver of tri-state MUX 112] ***configured to drive a connection with the first data word from the first stage logic*** [*e.g.*, the connection of the

output of the tri-state MUX 116 to the input of the first/upper tri-state driver of tri-state MUX 112]***, the first tristate driver enabled if a data connection exclusion signal is asserted*** [*e.g.*, when the select signal input on terminal 128 is enabled/asserted, the first/upper tri-state driver couples its input with the first data word to the output OUT of the tri-state MUX 112] ***and disabled if the data connection exclusion signal is deasserted*** [e.g., when the select signal input on terminal 128 is disabled/deasserted, the first/upper tri-state driver is disabled]; and would further have found obvious that Pixley-Watanabe's tri-state MUX 112 [the second stage logic] included ***a second tristate driver*** [*e.g.*, the second/lower tri-state driver of tri-state MUX 112] ***configured to drive a connection with the second data word*** [*e.g.*, the connection of the output of the tri-state MUX 114 to the input of the second/lower tri-state driver of tri-state MUX 112]***, the second tristate driver enabled if a data connection select signal is asserted*** [*e.g.*, when the select signal output by inverter 118 is enabled/asserted, the second/lower tri-state driver couples its input with the second data word to the output OUT of the tri-state MUX 112] ***and disabled if the data connection select signal is deasserted*** [*e.g.*, when the select signal output by inverter 118 is disabled/deasserted, the second/lower tri-state driver is disabled], as recited in [5.d]. EX1003, ¶¶111, 114.

F. Claim 6

[6] Pixley-Watanabe renders obvious Claim [6].

As described with respect to Element [4.c.ii], *supra*, the tri-state drivers described by Pixley increase signal strength when they were enabled. EX1003, ¶116; Element [4.c.ii], *supra*. Therefore, a POSITA would have found obvious that, in Pixley-Watanabe's nested multiplexers of FIG. 9, ***the first tristate driver*** [*e.g.*, the first/upper tri-state driver of tri-state MUX 112] ***increases the signal strength of the first data word when the selected data word is the first data word*** [*e.g.*, when the first/upper tri-state driver is enabled and couples its input with the first data word to OUT, the tristate driver amplifies the first data word], as recited in Claim [6]. EX1003, ¶117

G. Claim 7

[7.a] Pixley-Watanabe renders obvious Element [7.a].

Pixley explicitly discloses multiplexing circuits that operate according to a system clock. *See* EX1004, Claim 7 ("The method of claim 1 wherein the circuit model uses a circuit clock signal wherein operations are performed in response to active edges of the circuit clock signal…"); *see also, e.g., id.* at 4:21-40 (discussing the system clock). Pixley's system therefore is both sequential (*i.e.*, it recites a machine that performs steps in a particular order) and synchronous (*i.e.*, a machine that performs those sequential steps according to a system clock). *See, e.g.*,

EX1011, 420 (explaining that machines that use a "system clock" are called "synchronous sequential machines," which are machines where "input data are introduced into the machine and are processed sequentially according to some algorithm, and outputs are generated—all regulated by a system clock"). At minimum, a POSITA would have understood that Pixley's system could be operated according to a system clock as so implementing it allows it to receive, process, and output data in an orderly sequential fashion so as to work with other components. EX1003, ¶119.

A POSITA would have further understood that, in order to operate a machine in a synchronous, sequential fashion, memory elements must be added to a circuit. EX1011, 419; EX1003, ¶120. This is because devices that "lack true memory . . . lack the ability to perform sequential operations." EX1011, 419. Such a memory element "will remember a logic 1 or a logic 0 indefinitely or until it is directed to change to the other value." EX1011, ¶428. Thus, these memory elements allow for synchronous and sequential operation of a circuit because, rather than operating whenever an input is received, these memory elements hold their value, allowing operations to be performed at a time specified by the system clock. EX1003, ¶120.

A POSITA would have understood "[a] digital latch is the simplest digital storage element." EX1010, 285. As such, absent other considerations, a POSITA

would have been strongly motivated to use a latch to avoid adding unnecessary complexity to a circuit. EX1003, ¶121. Alternatively, depending on design considerations, a POSITA may have also considered the use of a flip-flop—i.e. "the traditional storage element used to realize synchronous logic circuit." EX1010, 294. Flip-flops "save the state of the machine from one clock cycle to the next," and thus a POSITA would have also been strongly motivated to use a flip-flop in order to implement a synchronous sequential system. And, among the different type of flip-flops, "D flip-flops are the preferred type for integrated circuit applications"—as a POSITA would have also understood. EX1010, 295. A D flip-flop is comprised of two latches connected in a master-slave configuration. EX1010, 295-296; EX1003, ¶121.

In order to implement its disclosed multiplexors according to a system clock, Pixley discloses that "[d]ata inputs and control/select signals to the MUXes 112, 114, and 116 are provided via four D flip-flops 124, 126, 130, and 132..." EX1004, 7:10-13; *see also id.* Claim 10. As such, a POSITA would understand it obvious to use D flip-flops, each comprising two latches, for both the data inputs and the control/select signals. Even in the absence of this teaching, a POSITA would have understood that, in order to implement Pixley's multiplexor with a system clock, memory elements would have been required and would have been motivated to use the "preferred type" of memory element—a D flip-flop

comprising two latches—in order to accomplish that goal. EX1010, 295; EX1003, ¶122. Indeed, such implementation details well-known and easy to implement by a skilled artisan. EX1003, ¶122.

Accordingly, Pixley-Watanabe renders obvious a using a ***first latch circuit*** [*e.g.,* one of the latches in a D-flip flop] to ***receive*** and ***latch*** the value of the data connection exclusion signal, and ***output*** that value to the first tristate driver according to a system clock. EX1003, ¶123.

[7.b] Pixley-Watanabe renders obvious Element [7.b].

As discussed above, a POSITA would have found obvious that Pixley's clocked system uses latch memory elements to ensure synchronous and sequential operation. Element [7.a], *supra*. Accordingly, Pixley-Watanabe renders obvious using a ***second latch circuit*** [*e.g.*, one of the latches of a D-flip flop] to ***receive*** and ***latch*** the value of the data connection selection signal, and ***output*** that value to the second tristate driver according to a system clock. EX1003, ¶¶125.

[7.c] Pixley-Watanabe renders obvious Element [7.c].

As discussed above, a POSITA would have found obvious that Pixley's clocked system uses latch memory elements to ensure synchronous and sequential operation. Element [7.a], *supra*. Accordingly, Pixley-Watanabe renders obvious using a ***third latch circuit*** [*e.g.*, one of the latches of a D-flip flop] to ***receive*** and

latch the second data word, and ***output*** that data word to the second tristate driver according to a system clock. EX1003, ¶127.

[7.d] Pixley-Watanabe renders obvious Element [7.d].

As discussed above, Pixley teaches a synchronous and sequential system that operates according to a system clock. EX1004, Claim 7 ("The method of claim 1 wherein the circuit model uses a circuit clock signal wherein operations are performed in response to active edges of the circuit clock signal…"); *see also, e.g., id.* at 4:21-40 (discussing the system clock); *see also* Element [7.a], *supra*. Accordingly, Pixley-Watanabe renders obvious using a ***first clock configured to transmit a clock signal*** to each of the components of the system, including the three latches discussed above. EX1003, ¶129.

H. Claim 8

[8.pre] Pixley-Watanabe renders obvious Element [8.pre] for the same reasons described above with respect to Element [1.pre].

See Element [1.pre], *supra*; EX1003, ¶130.

[8.a] Pixley-Watanabe renders obvious Element [8.a] for the same reasons described above with respect to Element [1.a].

See Element [1.a], *supra*; EX1003, ¶131.

[8.b] Pixley-Watanabe renders obvious Element [8.b].

With respect to FIG. 9, Pixley describes that "[d]ata inputs and control/select signals to the MUXes 112, 114, and 116 are provided via four D flip-flops 124,

126, 130, and 132 . . . ." EX1004, 7:11-14. A POSITA would have understood that flip-flops are a form of "cyclic logic circuits," and are therefore a form of logic. EX1010, 5; EX1003, ¶133.

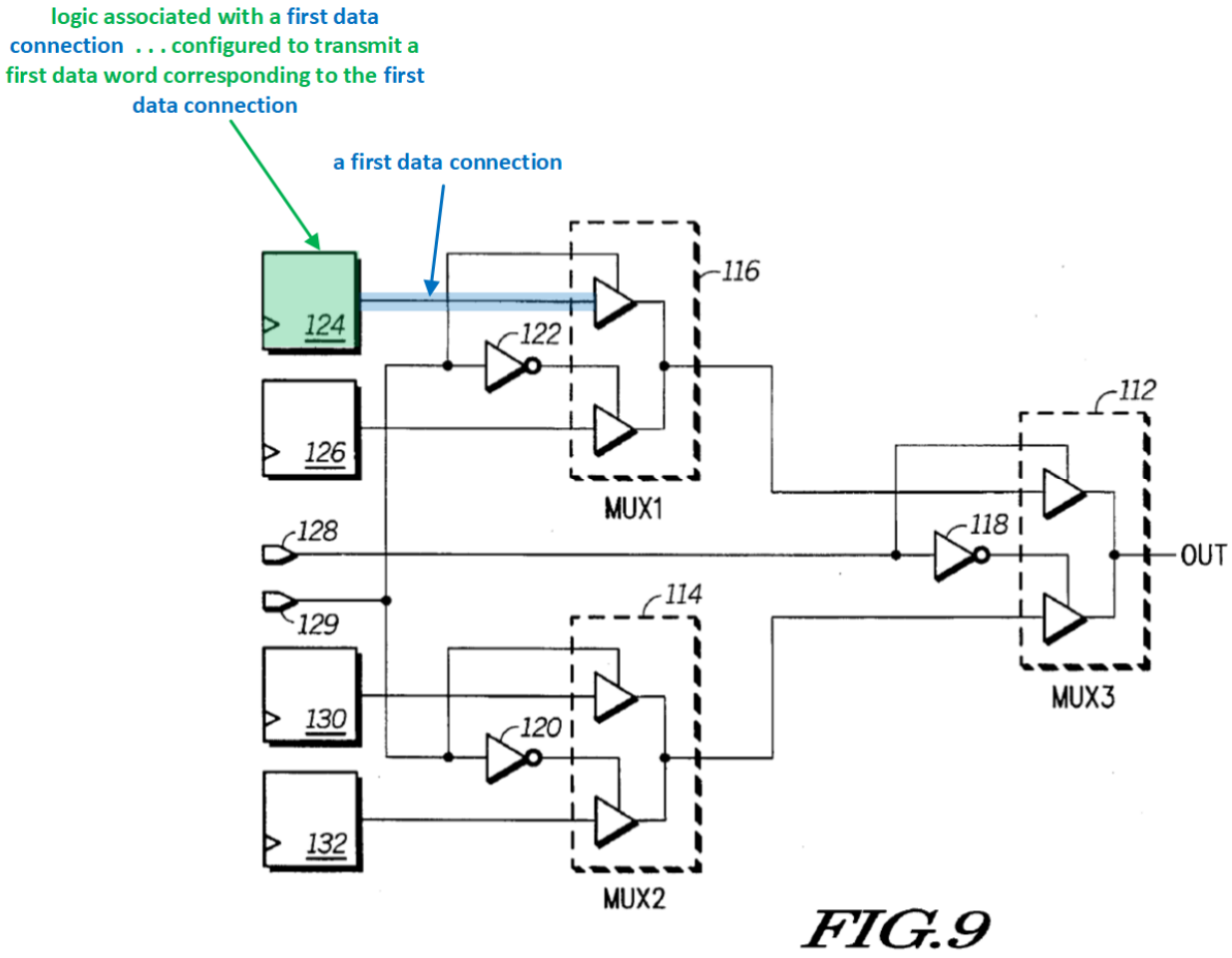


FIG.9

As described with respect to Element [1.pre], *supra*, a POSITA would have understood or at least found obvious that, for certain known use cases, the 2-to-1 multiplexers described by Pixler would have been configured to multiplex m-bit data words. Element [1.pre], *supra*; EX1003, ¶134. Thus, a POSITA would have understood or at least found obvious that, in m-bit processing applications in which

m-bit data must, for example, be read from registers or memory, each of Pixley's tri-state multiplexors 112, 114, and 116 would have been configured as an m-bit multiplexer composed of m one-bit multiplexers, one for each bit of data—effectively stacking a set of the multiplexer circuits illustrated in FIG. 9. EX1003, ¶134. In the context of Pixley's FIG. 9 circuit, the stack of one-bit multiplexer circuits would receive input from a corresponding set of flip-flops 124. *See* EX1004, 7:11-14. Indeed, a register may have been implemented with a set of flip-flops—one for each stored bit. EX1003, ¶134.

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 included ***logic associated with a first data connection of the plurality of data connections*** [*e.g.*, the set of flip-flops 124]***, the logic associated with the first data connection configured to transmit a first data word corresponding to the first data connection*** [*e.g.*, the set of flip-flops 124 transmits a first data word to the tri-state MUX 116], as recited in [8.b]. EX1003, ¶135.

[8.c] Pixley-Watanabe renders obvious Element [8.c].

As discussed with respect to [1.b], "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶¶137-138.

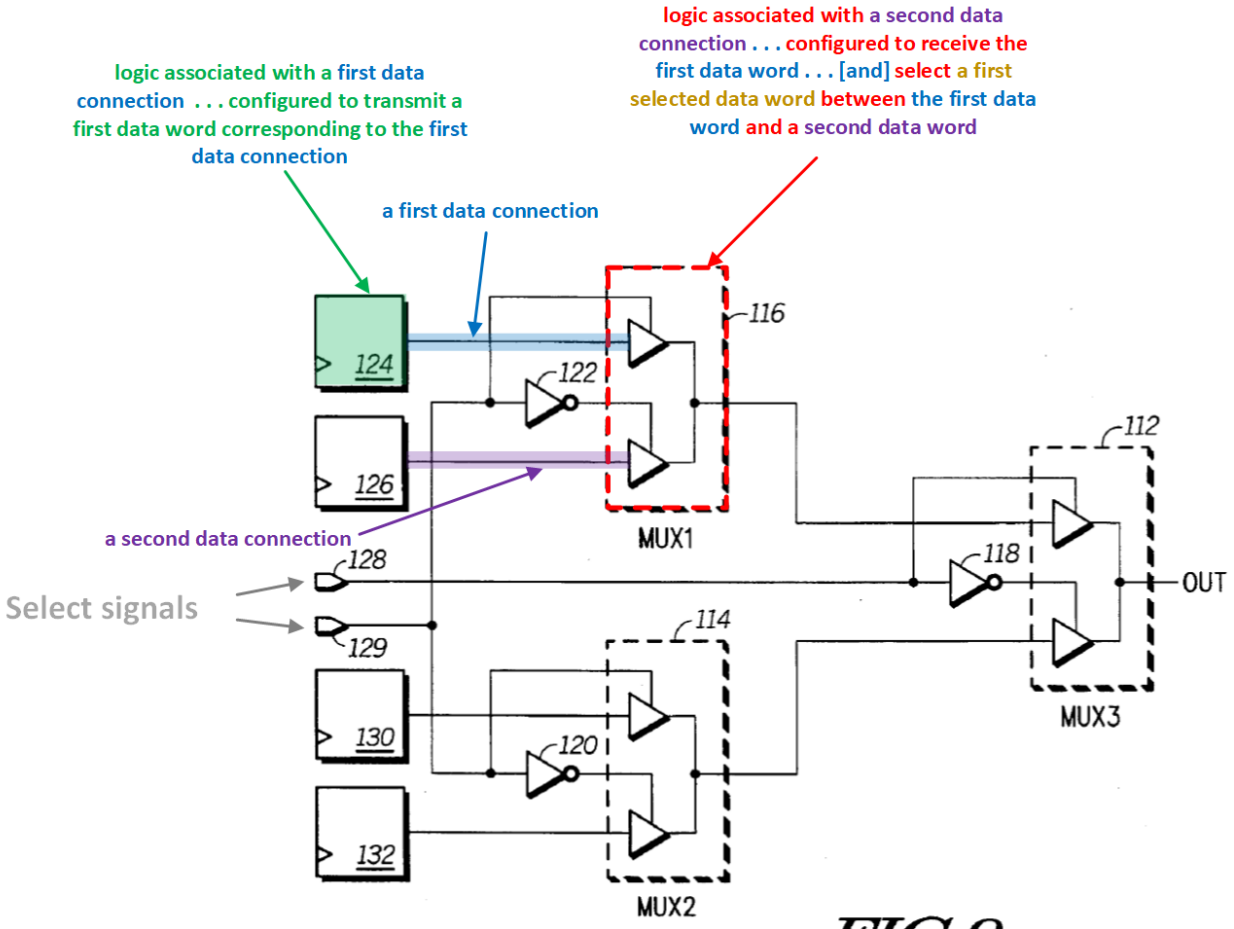


FIG.9

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 included ***logic associated with a second data connection of the plurality of data connections*** [*e.g.*, tri-state MUX 116, which is connected to a second data connection output by the set of flip-flops 126] ***configured to receive the first data word corresponding to the first data connection from the logic associated with the first of the plurality of data connections*** [*e.g.*, one input of tri-state MUX 116 is the output of the set of flip-flops 124, which transmit a first data word]***, the logic associated with the second data connection configured to select a***

first selected data word between the first data word and a second data word corresponding to the second data connection based upon a set of select signals

[*e.g.*, the tri-state MUX 116 selects between the first data word received from the set of flip-flops 124 and the second data word received from the set of flip-flops 126 based on the select signal of input terminal 129 and the select signal output by inverter 122], as recited in [8.c]. EX1003, ¶139.

[8.d] Pixley-Watanabe renders obvious Element [8.d].

As discussed with respect to [1.b]. "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶141.

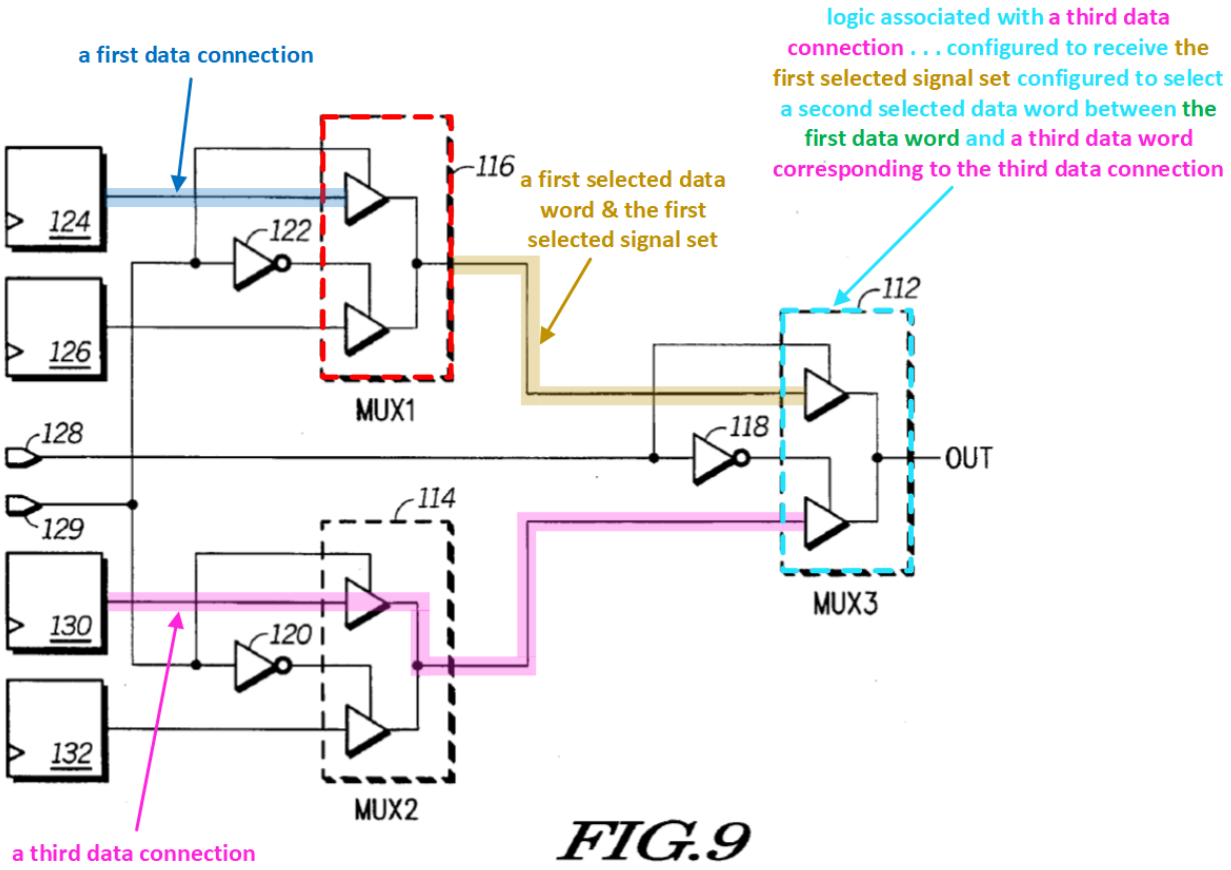


FIG.9

Further, as described with respect to [1.pre], *supra*, it was known that several m-bit 2-to-1 multiplexers could be nested, similar to the configuration shown in Pixley's FIG. 9. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037]. And, as discussed in Element [3], one known use case of such a configuration was the output of an operand from a selected register in a register bank for transmission to and use in an arithmetic and logical unit (ALU) via a system bus. *See* Element [3], EX1005, FIG. 4, [0043]; EX1003, ¶142-143.

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 included ***logic associated with a third data connection of***

the plurality of data connections [*e.g.*, tri-state MUX 112, which is connected to a third data connection output by the set of flip-flops 130 via tri-state MUX 114] ***configured to receive the first selected signal set*** [*e.g.*, the upper tri-state driver of tri-state MUX 112 receives the set of signals of the data word selected by tri-state MUX 116]***, the logic associated with the third data connection configured to select a second selected data word*** [*e.g.*, the data word output on OUT by tri-state MUX 112] ***between the first data word*** [*e.g.*, the data word associated with the set of flip-flops 124 received by tri-state MUX 112 via tri-state MUX 116] ***and a third data word corresponding to the third data connection*** [*e.g.*, the data word associated with the set of flip-flops 130 received by tri-state MUX 112 via tri-state MUX 114] ***based upon a set of select signals*** [*e.g.*, the select signal of input terminal 128 and the select signal output by inverter 118]***, the logic associated with the third data connection further configured transmit the second selected data word to a system bus*** [*e.g.*, a system bus connecting the output OUT of tri-state MUX 112 to an arithmetic and logical unit (ALU)], as recited in [8.d]. EX1003, ¶144.

I. Claim 9

[9.pre] Pixley-Watanabe renders obvious Element [9.pre] for the same reasons described above with respect to Element [1.pre].

See Element [1.pre], *supra*; EX1003, ¶145.

[9.a] Pixley-Watanabe renders obvious Element [9.a].

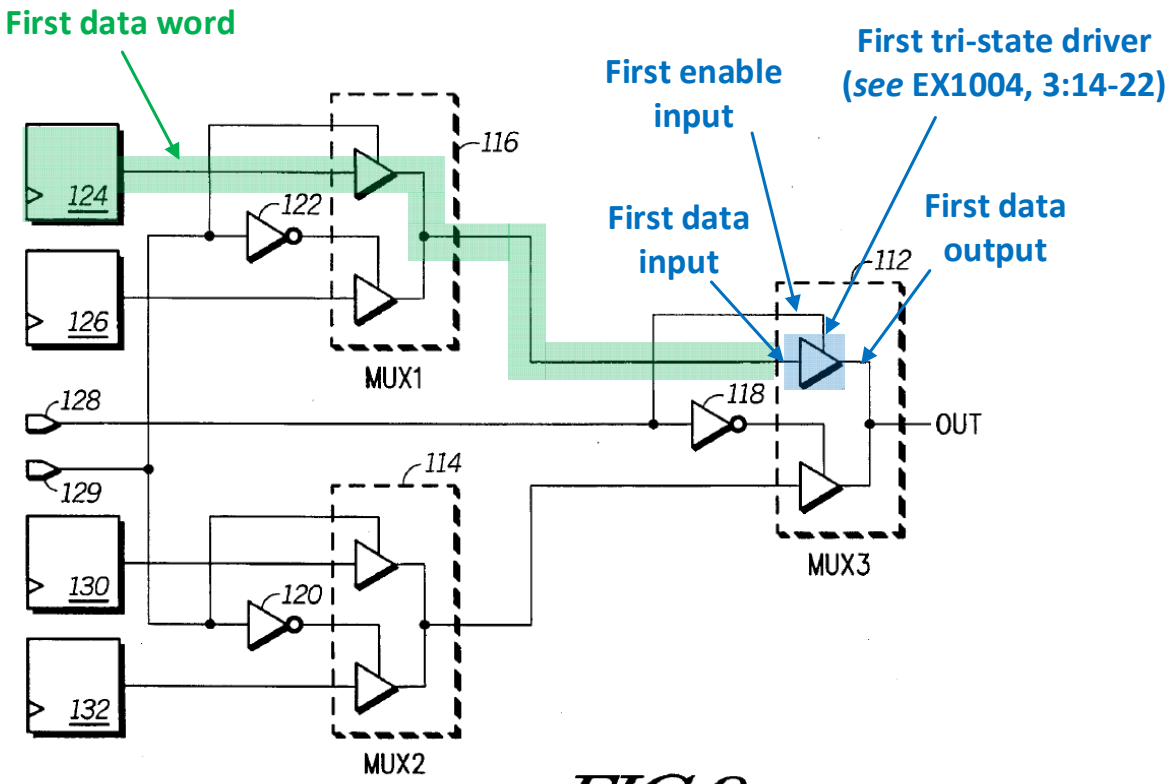


FIG.9

As described with respect to Element [1.pre], *supra*, a POSITA would have understood or at least found obvious that, for certain known use cases, the 2-to-1 multiplexers described by Pixler would have been configured to multiplex m-bit data words. *See* Element [1.pre], *supra*; EX1003, ¶147. One known use case of such a configuration was the output of an operand from a selected register in a register bank for transmission to and use in an arithmetic and logical unit (ALU). *See* EX1005, FIG. 4, [0043]; EX1003, ¶¶147-148. When the circuit of FIG. 9 was implemented in this way, the upper tristate driver of tri-state MUX 112 received

data input from the set of flip-flops 124 via the tri-state MUX 116. *See* EX1004, FIG. 9, 7:11-14; EX1003, ¶149. The upper tri-state driver of tri-state MUX 112 received a select signal from terminal 128 and coupled the input data to the output of tri-state MUX 112 when the select signal of terminal 128 was enabled. *See* EX1004, FIG. 9, 3:14-22, 7:7-14; EX1003, ¶149.

Therefore, a POSITA would have found obvious that Pixely's nested multiplexers of FIG. 9 included ***a first tristate driver comprising a first data input, a first data output, and a first enable input*** [*e.g.*, the upper tri-state driver of tri-state MUX 112]***, the first tristate driver adapted to receive a first data word via the first data input representative of a first data connection*** [*e.g.*, the upper tri-state driver of tri-state MUX 112 receiving the data word of flip-flops 124 via tri-state MUX 116], as recited in [9.a]. EX1003, ¶150.

[9.b] Pixley-Watanabe renders obvious Element [9.b].

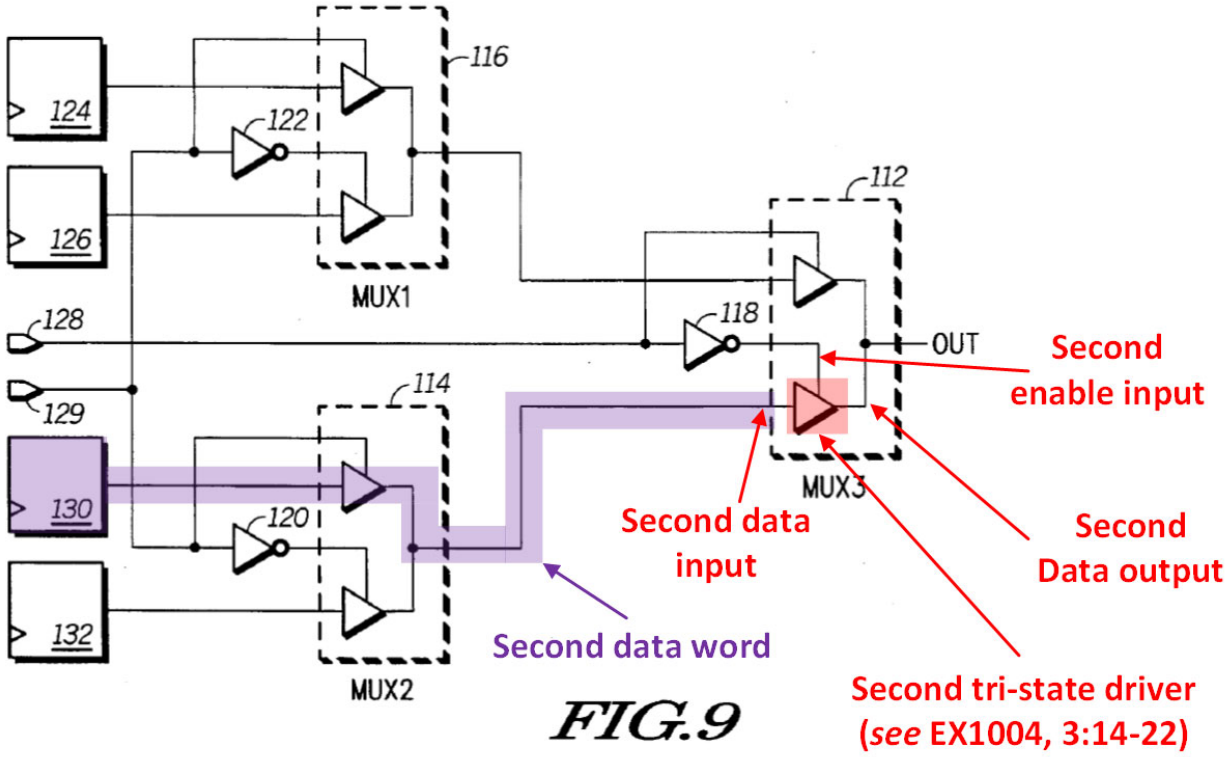


FIG.9

As described with respect to [9.a], each of Pixley's tri-state multiplexors 112, 114, and 116 would have been configured as an m-bit multiplexer composed of m one-bit multiplexers and these multiplexors would receive inputs from corresponding sets of m flip-flops 124, 126, 130, 132. *See, e.g.*, EX1005, FIGS. 3, 4, [0018], [0035]-[0037], [0043]; EX1004, 7:11-14; EX1003, ¶152. When the circuit of FIG. 9 was implemented in this way, the lower tristate driver of tri-state MUX 112 received data input from the set of flip-flops 130 via the tri-state MUX 114. *See* EX1004, FIG. 9, 7:11-14; EX1003, ¶153. The lower tri-state driver of tri-state MUX 112 received a select signal from inverter 118, and coupled the input

data to the output of tri-state MUX 112 when the select signal output by inverter 118 was enabled. *See* EX1004, FIG. 9, 3:14-22, 7:7-14; EX1003, ¶153.

Therefore, a POSITA would have found obvious that Pixely's nested multiplexers of FIG. 9 included ***a second tristate driver comprising a second data input, a second data output, and a second enable input*** [*e.g.*, the lower tri-state driver of tri-state MUX 112]***, the second tristate driver adapted to receive a second data word representative of a second data connection*** [*e.g.*, the lower tri-state driver of tri-state MUX 112 receiving the data word of flip-flops 130 via tri-state MUX 114], as recited in [9.b]. EX1003, ¶154.

[9.c] Pixley-Watanabe renders obvious Element [9.c].

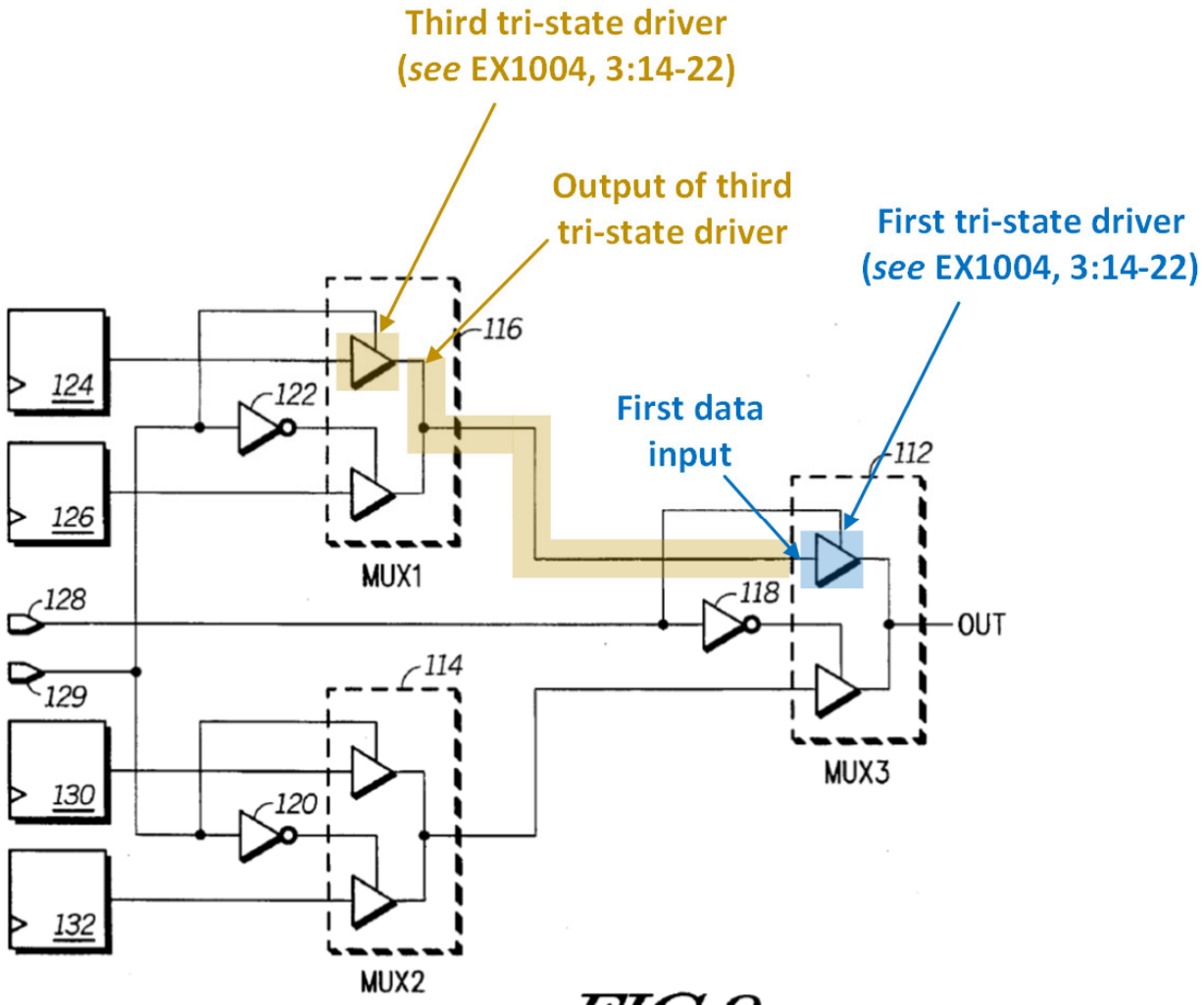


FIG.9

The upper tri-state driver of tri-state MUX 116 has an output connected to the data input of the upper tri-state driver of tri-state MUX 112. *See* EX1004, FIG. 9, 7:11-14; EX1003, ¶¶156-157. Therefore, a POSITA would have found obvious that Pixely's nested multiplexers of FIG. 9 included ***a third tristate driver*** [*e.g.*, the upper tri-state driver of tri-state MUX 116] ***having an output coupled to the first***

data input of the first tristate driver [*e.g.*, the upper tri-state driver of tri-state MUX 112], as recited in [9.c]. EX1003, ¶158.

[9.d] Pixley-Watanabe renders obvious Element [9.d].

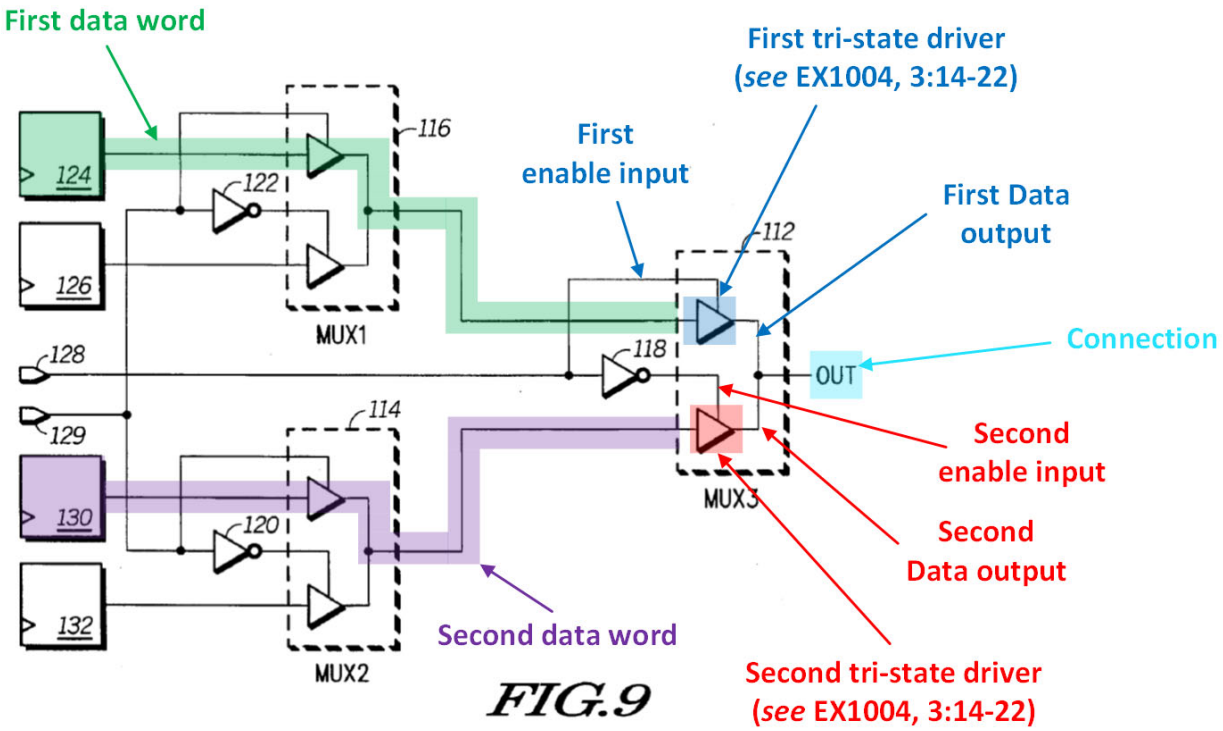


FIG.9

When the select signal of terminal 129 is enabled, the upper tri-state driver of each of tri-state multiplexers 114 and 116 is also enabled, connecting the first and second data words received from the sets of flip-flops 124 and 130 to be connected to the inputs of tri-state multiplexer 112. *See* EX1004, FIG. 9, 3:14-22, 7:7-14; EX1003, ¶¶160-161. The tri-state multiplexer 112 then selects between the first and second data words output by the tri-state multiplexers 114 and 116, respectively, based on the select signal of terminal 129 and the output of inverter 118. *See id.* When the select signal input on terminal 128 is enabled (*i.e.*, a logic

high), the upper tri-state driver of tri-state MUX 112 is enabled, and the first data word (highlighted in green above) input to the upper tri-state driver is coupled to the output OUT of tri-state MUX 112. *See id.* And when the select signal output by the inverter 118 is enabled (*i.e.*, a logic high), the second/lower tri-state driver of tri-state MUX 112 is enabled, and the second data word (highlighted in purple above) input to the lower tri-state driver is coupled to the output OUT of tri-state MUX 112. *See id.*; EX1003, ¶161.

Therefore, a POSITA would have found obvious that Pixely's nested multiplexers of FIG. 9 included ***a connection*** [*e.g.*, the output OUT of the tri-state multiplexer 112] ***adapted to receive, via the data output of the first tristate driver*** [*e.g.*, the upper tri-state driver of tri-state multiplexer 112]***, the first data word*** [*e.g.*, the data word input to the upper tri-state driver of the tri-state multiplexer 112 from the flip-flops 124 via tri-state multiplexer 116]***, if a first signal is asserted at the first enable input of the first tristate driver*** [*e.g.*, the input of the upper tri-state driver is coupled to the output OUT of the tri-state multiplexer 112 when the select signal of terminal 128 is enabled]***, the connection further adapted to receive, via the second data output of the second tristate driver*** [*e.g.*, the lower tri-state driver of tri-state multiplexer 112]***, the second data word*** [*e.g.*, the data word input to the lower tri-state driver of the tri-state multiplexer 112 from the flip-flops 130 via tri-state multiplexer 114]***, if a second signal is asserted at the***

enable input of the second tristate driver [*e.g.*, the input of the lower tri-state driver is coupled to the output OUT of the tri-state multiplexer 112 when the select signal output by inverter 118 is enabled], as recited in [9.d]. EX1003, ¶162.

J. Claim 10

[10] Pixley-Watanabe renders obvious Claim [10].

A POSITA would have understood or at least found obvious that the select signals asserted on input terminals/pins 128 and 129—which control which data words are selected by the tri-state multiplexers of FIG. 9—would have been asserted by select logic controlled by an application program. EX1003, ¶164. Pixley does not limit from where the signals asserted on input terminals/pins 128 and 129 are received. *See generally* EX1004, 7:7-8:3; EX1003, ¶165. As described with respect to Element [1.pre], *supra*, one known use case of a configuration of nested/cascading multiplexers like that shown in Pixley's FIG. 9 was the selection of an operand from a selected register in a register bank for transmission to and use in an arithmetic and logical unit (ALU). *See* EX1005, FIG. 4, [0043]; EX1003, ¶165. In this use case, it was further known that the select signal indicating the register number corresponding to the selected operand was received by logic (*e.g.*, an instruction register/decoder) controlled by an application program of a microprocessor. *See* EX1005, [0004]-[0006] (describing that a user "develop[s] program sequences" for a microprocessor that includes the

nested/cascading multiplexers used to read the registers), [0035]-[0037], [0040], [0043], [0050]; EX1003, ¶165.

Therefore, a POSITA would have found obvious that Pixely's nested multiplexers of FIG. 9 included ***select logic*** [e.g., an instruction register/decoder] ***configured to assert the first signal if an application program desires the first data word representative of the first data connection*** [*e.g.*, an application directing a microprocessor that includes the nested/cascading multiplexers of Pixley's FIG. 9 asserts the select signal of input terminal 128, enabling the upper tri-state driver] ***and configured to assert the second signal if the application program desires the second data word representative of the second data connection*** [*e.g.*, an application directing a microprocessor that includes the nested/cascading multiplexers of Pixley's FIG. 9 deasserts the select signal of input terminal 128, resulting in an assertion of the output of inverter 118, enabling the lower tri-state driver], as recited in Claim [10]. EX1003, ¶166.

K. Claim 11

[11] Pixley-Watanabe renders obvious Claim [11].

As described with respect to Claim [10], *supra*, a POSITA would have understood or at least found obvious that the select signals asserted on input terminals/pins 128 and 129—which control which data words are selected by the

tri-state multiplexers of FIG. 9—would have been asserted by select logic controlled by an application program. EX1003, ¶¶168-169.

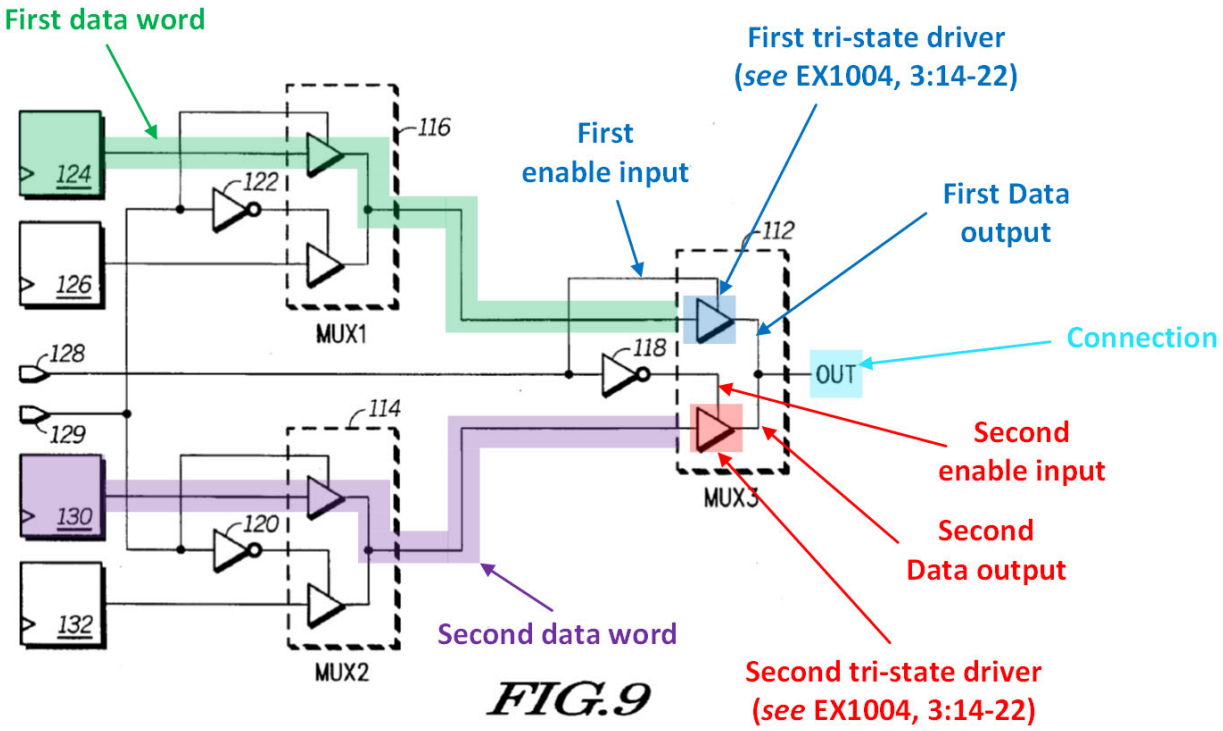


FIG.9

Therefore, a POSITA would have found obvious that, in Pixely's nested multiplexers of FIG. 9, ***the select logic deasserts the first signal if the application program does not desire the first data word*** [*e.g.*, the select logic deasserts the select signal input on terminal 128] ***and deasserts the second signal if the application program does not desire the second data word*** [*e.g.*, the select logic asserts the select signal input on terminal 128, which results in the output of inverter 118 being deasserted], as recited in Claim [11]. EX1003, ¶170.

L. Claim 12

[12] Pixley-Watanabe renders obvious Claim [12].

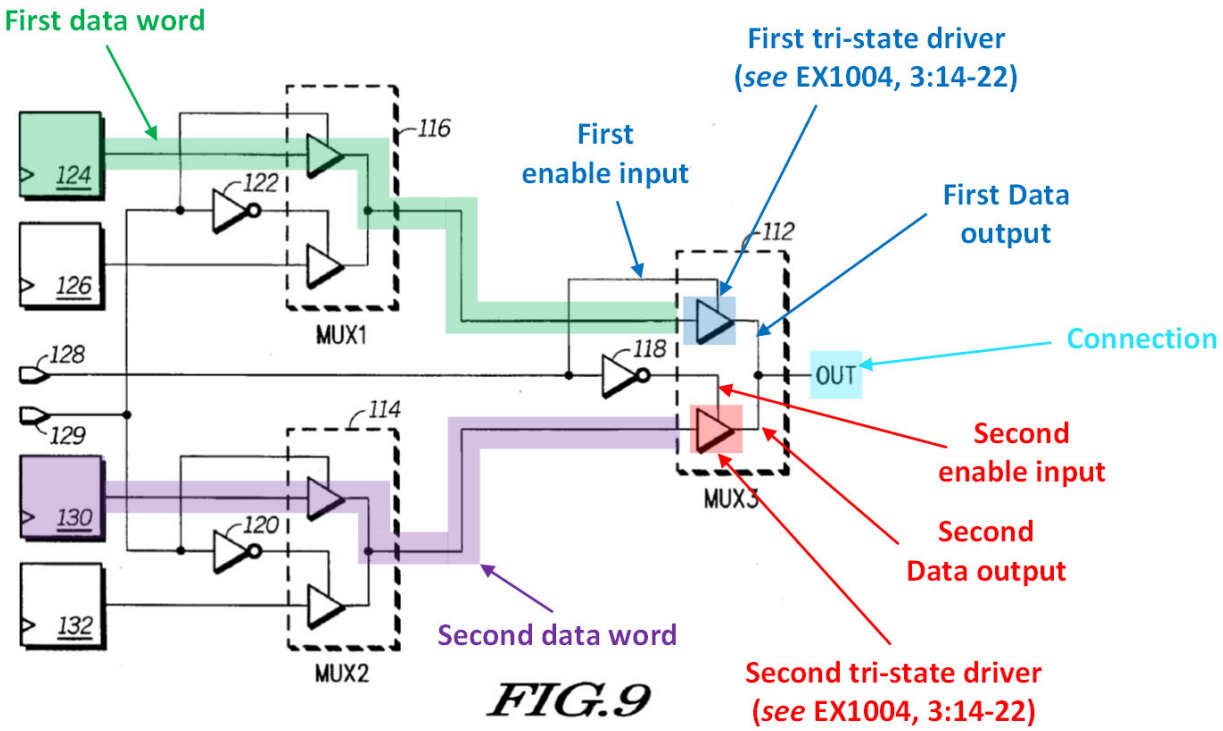


FIG.9

When the select signal of terminal 129 is enabled, the output of inverter 118 is disabled, because the select signal of terminal 129 is the input of inverter 118 and therefore the two select signals are complements of one another. *See* EX1004, FIG. 9, 7:7-14; EX1003, ¶¶172-173. As described by Pixley, "a tri-state multiplexer should be carefully checked during design to ensure: (1) that no two select lines which have different input logic values are enabled at or around a critical period of time; and (2) that at least one select line is enabled during all critical time periods." EX1004, 4:21-26. Pixley further teaches that the nested

multiplexer circuit illustrated in FIG. 9 meets these two conditions. *See* EX1004, 7:14-16; EX1003, ¶173.

Therefore, a POSITA would have found obvious that, in Pixely's nested multiplexers of FIG. 9, ***the first signal and the second signal enable and disable the first and second tristate drivers simultaneously*** [*e.g.*, when the select signal of input terminal/pin 128 is asserted, the output of inverter 118 is simultaneously deasserted, and when the select signal of input terminal/pin 128 is deasserted, the output of inverter 118 is simultaneously asserted], as recited in [12]. EX1003, ¶174.

M. Claim 13

See Claim 7, *supra*. EX1003, ¶¶175-176.

N. Claim 14

[14.pre] Pixley-Watanabe renders obvious Element [14.pre].

For example, Pixley "provides a method and apparatus to perform checking of tri-state multiplexers to ensure that the tri-state multiplexers are operating in a proper manner." EX1004, 2:60-63. Accordingly, a POSITA would have understood or at least found obvious that Pixley teaches a ***method for distributing multiplexing***, as recited in [14.pre]. EX1003, ¶¶178-179.

[14.a] Pixley-Watanabe renders obvious Element [14.a] for the same reasons described above with respect to Elements [1.b] and [1.c.ii].

See Elements [1.b], [1.c.ii], *supra*; EX1003, ¶¶180-183.

[14.b] Pixley-Watanabe renders obvious Element [14.b] for the same reasons described above with respect to Element [1.c.i].

See Element [1.c.i], *supra*; EX1003, ¶¶184-187.

[14.c] Pixley-Watanabe renders obvious Element [14.c] for the same reasons described above with respect to Element [1.c.i].

See Element [1.c.i], *supra*; EX1003, ¶¶188-191.

[14.d] Pixley-Watanabe renders obvious Element [14.d] for the same reasons described above with respect to Element [1.c.ii].

See Element [1.c.ii], *supra*; EX1003, ¶¶192-194.

[14.e] Pixley-Watanabe renders obvious Element [14.e] for the same reasons described above with respect to Element [1.c.ii].

See Element [1.c.ii], *supra*; EX1003, ¶¶195-197.

O. Claim 15

[15] Pixley-Watanabe renders obvious Claim 15.

As described with respect to [1.pre], *supra*, it was known that several m-bit 2-to-1 multiplexers could be nested, similar to the configuration shown in Pixley's FIG. 9. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037]. And, as discussed in Element [3], one known use case of such a configuration was the output of an operand from a selected register in a register bank for transmission to and use in an arithmetic and logical unit (ALU) via a system bus. *See* Element [3], EX1005, FIG. 4, [0043]; EX1003, ¶199.

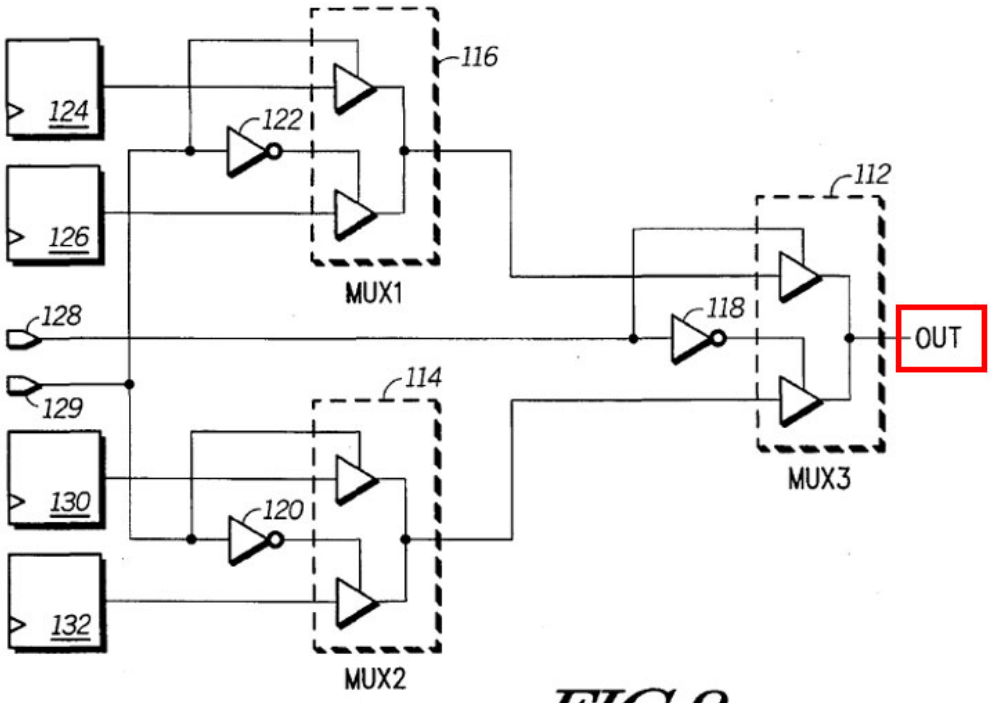


FIG.9

Applying the MUX circuit shown in FIG. 9 to the example use case described by Watanabe, a POSITA would have at least found it obvious that the output OUT of tri-state MUX 112 would have been connected to a system bus to provide data words read out from memory, such as registers, for use in an integrated circuit (IC) component, such as an ALU. *See* EX1005, FIGS. 3, 9, [0021], [0028]-[0029], [0034]-[0037], [0043]; EX1003, ¶200.

Moreover, the '448 Patent equates transmitting to a discrete IC component to generic outputting. *See* EX1001, 2:44-48 ("select logic then indicates which data word from the multiple data connections is to be output (e.g. transmitted to a discrete IC component"). As illustrated in Figure 9, excerpted above, the data

word is output (i.e. "OUT), which, as explained by the '448 Patent, equates to transmission to a discrete IC component. EX1003, ¶201.

Therefore, a POSITA would have found obvious that the output of FIG. 9 [*e.g.*, ***the selected data word***] is transmitted to a discrete integrated circuit component on the CPU. EX1003, ¶202.

P. Claim 16

[16] Pixley-Watanabe renders Claim 16 obvious for the same reasons discussed above in Elements [5.d.i] and [5.d.ii].

See Element [5.d.i], [5.di.ii], *supra*; EX1003, ¶203.

Q. Claim 17

[17.pre] Pixley-Watanabe renders Element [17.pre] obvious for the same reasons discussed above in Element [14.pre].

See Element [14.pre], *supra*; EX1003, ¶204.

[17.a][2] Pixley-Watanabe renders Element [17.a] obvious.

With respect to FIG. 9, Pixley describes that "[d]ata inputs and control/select signals to the MUXes 112, 114, and 116 are provided via four D flip-flops 124, 126, 130, and 132 . . . ." EX1004, 7:11-14.

[2] Though Claim 17 uses the same terminology as earlier claims, the "first" data word and similar numbered terminology of Claim 17 does not correspond to the "first" data word claimed in other claims—as is apparent from context of the

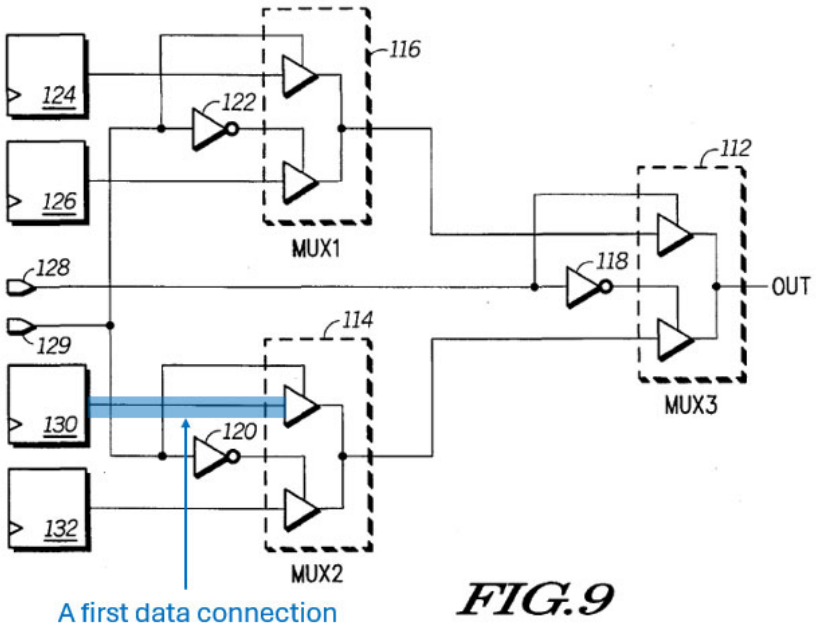


FIG.9

As described with respect to Element [1.pre], *supra*, a POSITA would have understood or at least found obvious that, in m-bit processing applications in which m-bit data must, for example, be read from registers or memory, each of Pixley's

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claim. For example, in Claim 1, a "second" stage logic selects between a "first" data word received from the "first" stage logic and another data word received from another of the plurality of data connections. In Claim 17, a "first data word" is transmitted by "a" tristate driver to a "first logic," and is driven by a "first" tristate driver—i.e. not "a" tristate driver. EX1003, ¶206. While confusing, Infineon does not assert, solely for the purposes of this IPR, that this confusion renders Claim 17 indefinite.

tri-state multiplexors 112, 114, and 116 would have been configured as an m-bit multiplexer composed of m one-bit multiplexers, effectively stacking a set of the multiplexer circuits illustrated in FIG. 9. EX1003, ¶¶207-208.

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 included ***receives a first data word corresponding to a first data connection*** [*e.g.*, the connection between the set of flip-flops 130 and tri-state MUX 114, where MUX 114 receives a first data word from flip-flops 130], as recited in [17.a]. EX1003, ¶209.

[17.b] Pixley-Watanabe renders obvious Element [17.b].

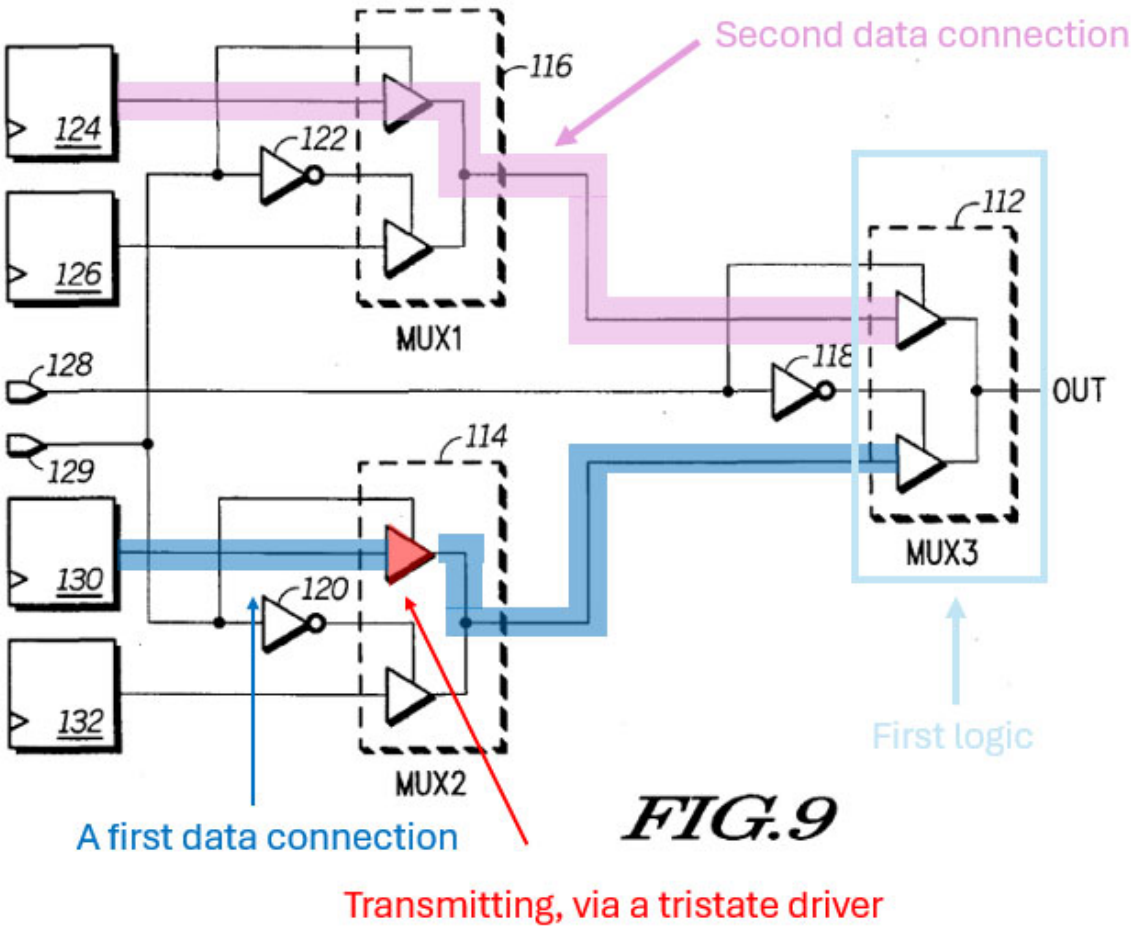


FIG.9

As described with respect to Element [17.a], MUX1 114 receives a first word via the first data connection. Next, upper tri-state driver of MUX2 114 (annotated in red above) transmits the first word. *See* 1004, 7:7-14, FIG. 9; EX1003, ¶211. When MUX1 114 receives an enable signal via input signal 129, the upper tri-state driver is coupled to the output OUT of MUX2 114, and the first data word (highlighted in blue above) is sent [e.g., transmitted] to MUX3 112. *See*

id. A POSITA would have recognized or found obvious that MUX3 112 is logic. EX1003, ¶212.

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 ***transmit, via a tristate driver*** [*e.g.,* the upper tri-state driver of MUX1 114], ***the first data word*** [*e.g.*, the data word associated with the set of flip-flops 130 received by tri-state MUX 112 via tri-state MUX 114] ***to first logic associated with a second data connection*** [*e.g.,* tri-state MUX 112, which is connected to a second data connection through its lower tri-state driver], as recited in [17.b]. EX1003, ¶213.

[17.c]. Pixley-Watanabe renders obvious Element [17.c].

As discussed with respect to [1.b]. "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶¶215-217.

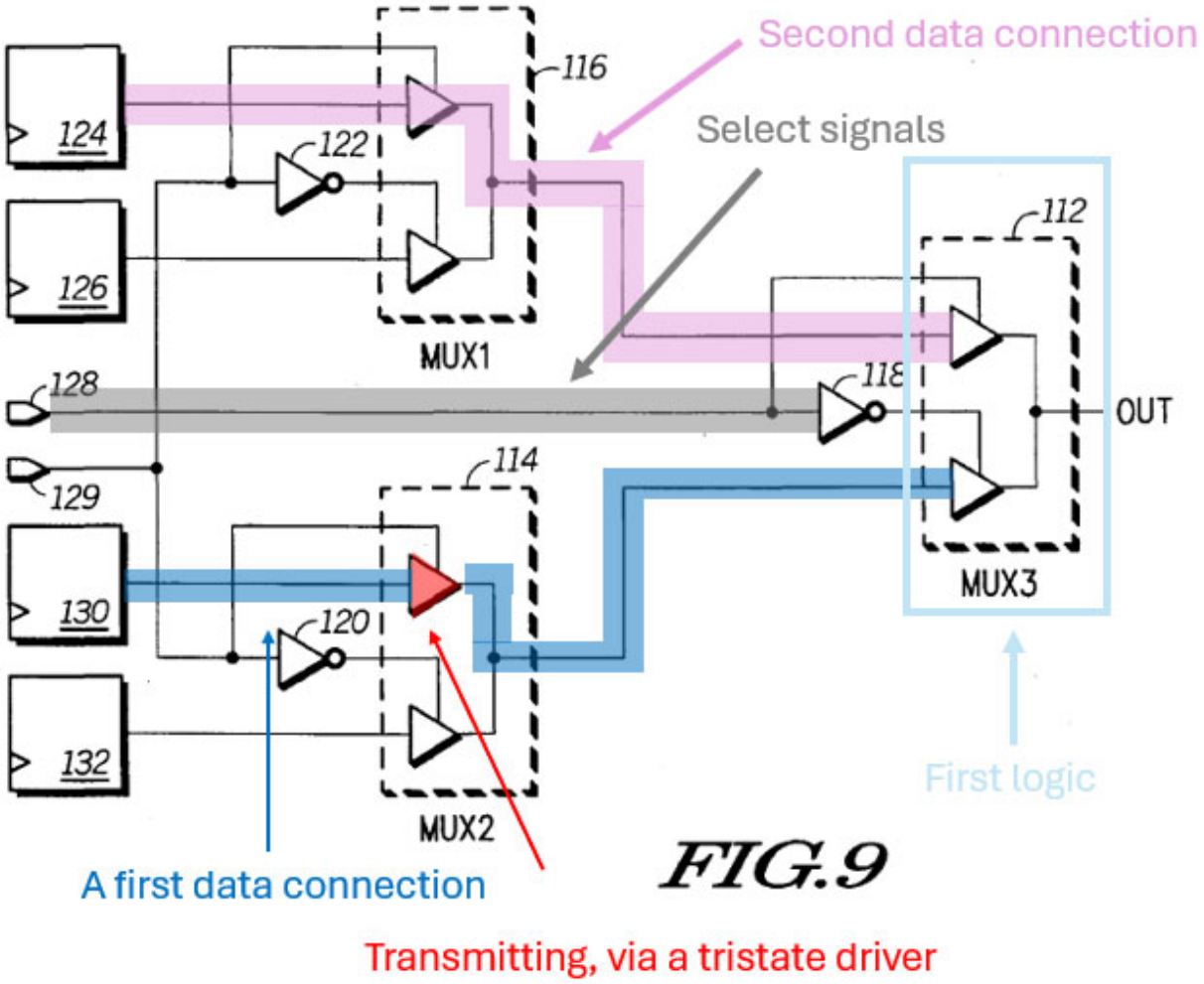


FIG.9

A POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 ***selects a selected data word via the first logic between the first data word and a second data word transmitted from the second data connection based upon a set of select signals*** [*e.g.*, the tri-state MUX 112 selects between the first data word received from the set of flip-flops 130 and the second data word received from the set of flip-flops 124 based on the select signal of input terminal 128 and the select signal output by inverter 118], as recited in [17.c]. EX1003, ¶218.

[17.d] Pixley-Watanabe renders obvious Element [17.d].

As described with respect to [1.pre], supra, it was known that several m-bit 2-to-1 multiplexers could be nested, similar to the configuration shown in Pixley's FIG. 9. *See, e.g.*, EX1005, FIG. 3, [0035]-[0037]. And, as discussed in Element [3], one known use case of such a configuration was the output of an operand from a selected register in a register bank for transmission to and use in an arithmetic and logical unit (ALU) via a system bus. *See* Element [3], EX1005, FIG. 4, [0043]; EX1003, ¶220.

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 ***transmits the selected data word*** [*e.g.*, a system bus connecting the output OUT of tri-state MUX 112 to an arithmetic and logical unit (ALU)], as recited in [17.d]. EX1003, ¶221.

[17.e] Pixley-Watanabe renders obvious Element [17.e].

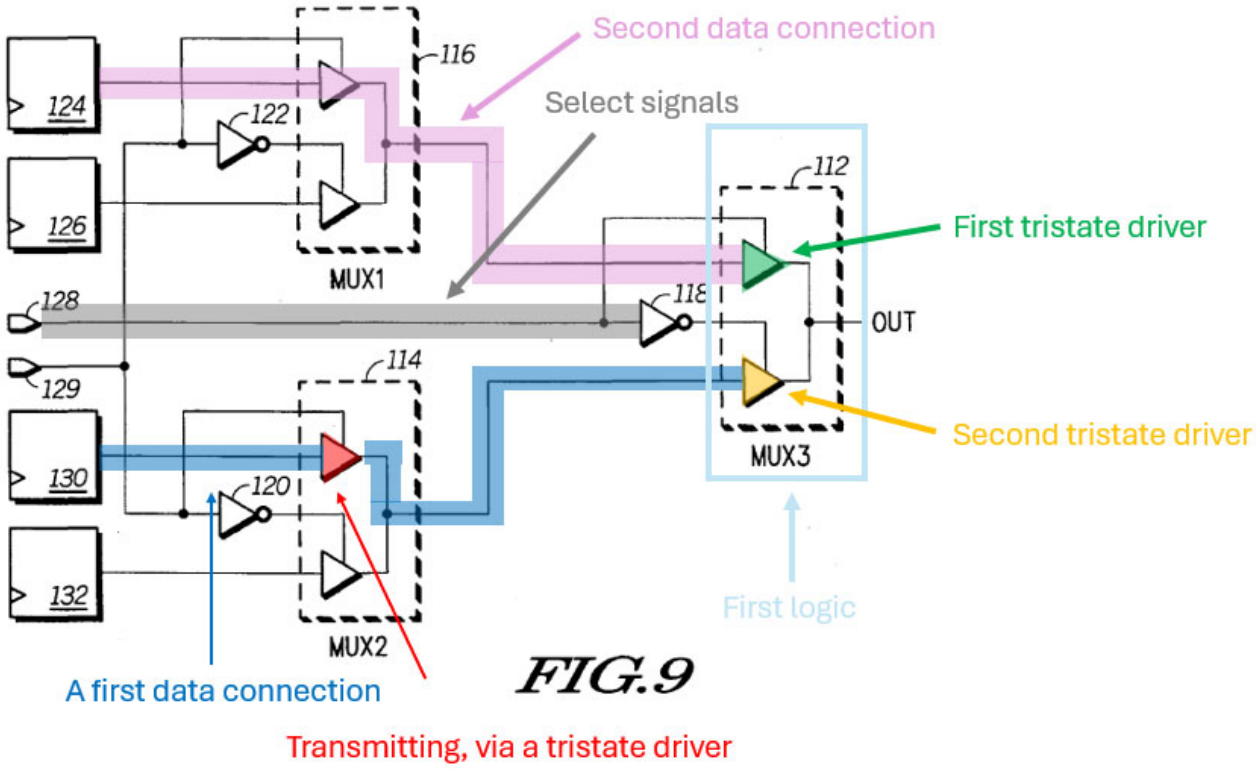


FIG.9

When the select signal input on terminal 128 is enabled (*i.e.*, a logic high), the first/upper tri-state driver of tri-state MUX 112 is enabled, and the second data word (highlighted in pink above) input to the upper tri-state driver is coupled to the output OUT of tri-state MUX 112. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶¶223-224. Correspondingly, the second/lower tri-state driver of tri-state MUX 112 receives a complement of the select signal input on terminal 128 via inverter 118, such that when the select signal input on terminal 128 is enabled, the output of inverter 118 is disabled (*i.e.*, a logic low) and the second/lower tri-state driver of tri-state MUX 112 is disabled. *See id.*; EX1003, ¶¶226-227.

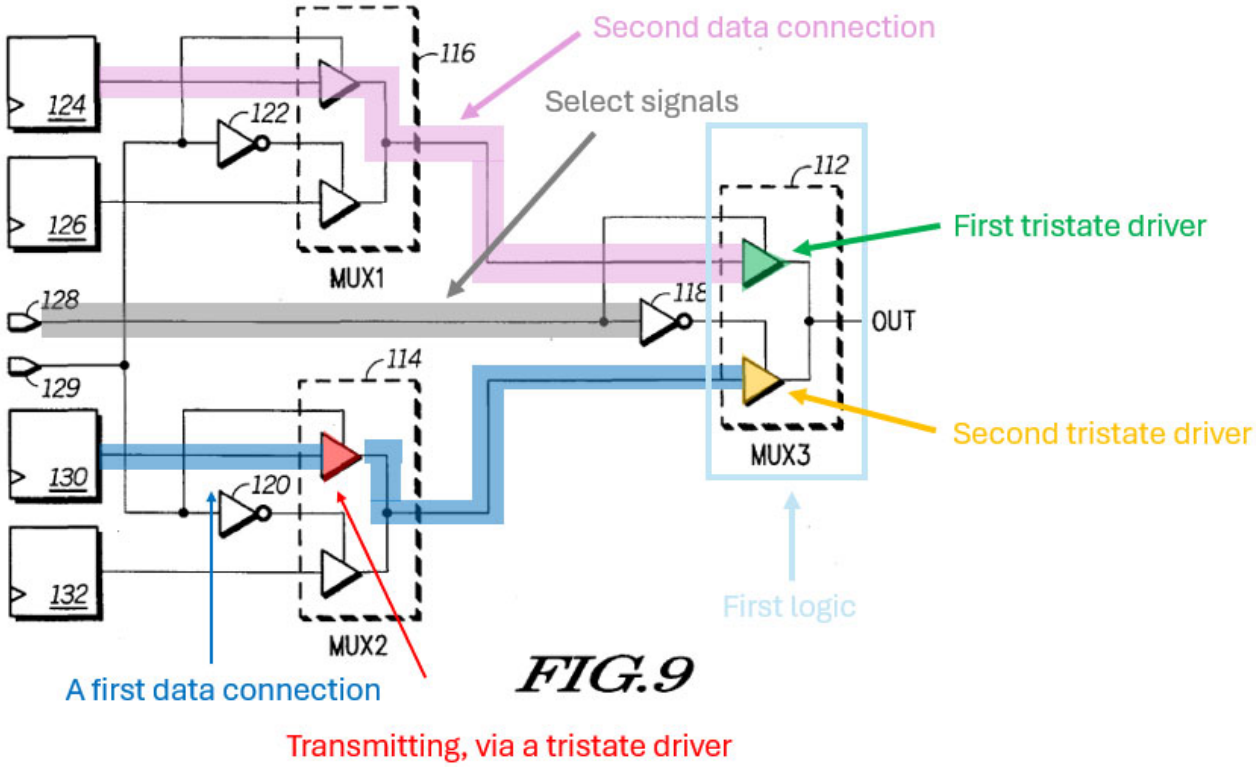


FIG.9

When the select signal input on terminal 128 is enabled (*i.e.*, a logic high), the first/upper tri-state driver of tri-state MUX 112 is enabled, and the second data word (highlighted in pink above) input to the upper tri-state driver is coupled to the output OUT of tri-state MUX 112. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶224. Correspondingly, the second/lower tri-state driver of tri-state MUX 112 receives a complement of the select signal input on terminal 128 via inverter 118, such that when the select signal input on terminal 128 is enabled, the output of inverter 118 is disabled (*i.e.*, a logic low) and the second/lower tri-state driver of tri-state MUX 112 is disabled. *See id.*; EX1003, ¶¶226-227.

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 ***drives the second data word to a connection via a first tri-state driver if the data connection selection signal is asserted*** [*e.g.*, when the select signal input on terminal 128 is enabled/asserted, the first/upper tri-state driver couples its input with the second data word to the output OUT of the tri-state MUX 112], and that Pixley's nested multiplexers of FIG. 9 ***disables a second tristate driver configured to receive the first data word*** [*e.g.*, when the select signal input on terminal 128 is enabled/asserted, the second/lower tri-state driver is disabled]***, and configured to drive the first data word to the connection if the data connection exclusion signal is asserted*** [*e.g.*, when the select signal input on terminal 128 is disabled/deasserted, the second/lower tri-state driver couples its input with the first data word to the output OUT of the tri-state MUX 112], as recited in [17.e]. EX1003, ¶225, ¶228.

R. Claim 18

[18] Pixley-Watanabe renders obvious Element Claim 18.

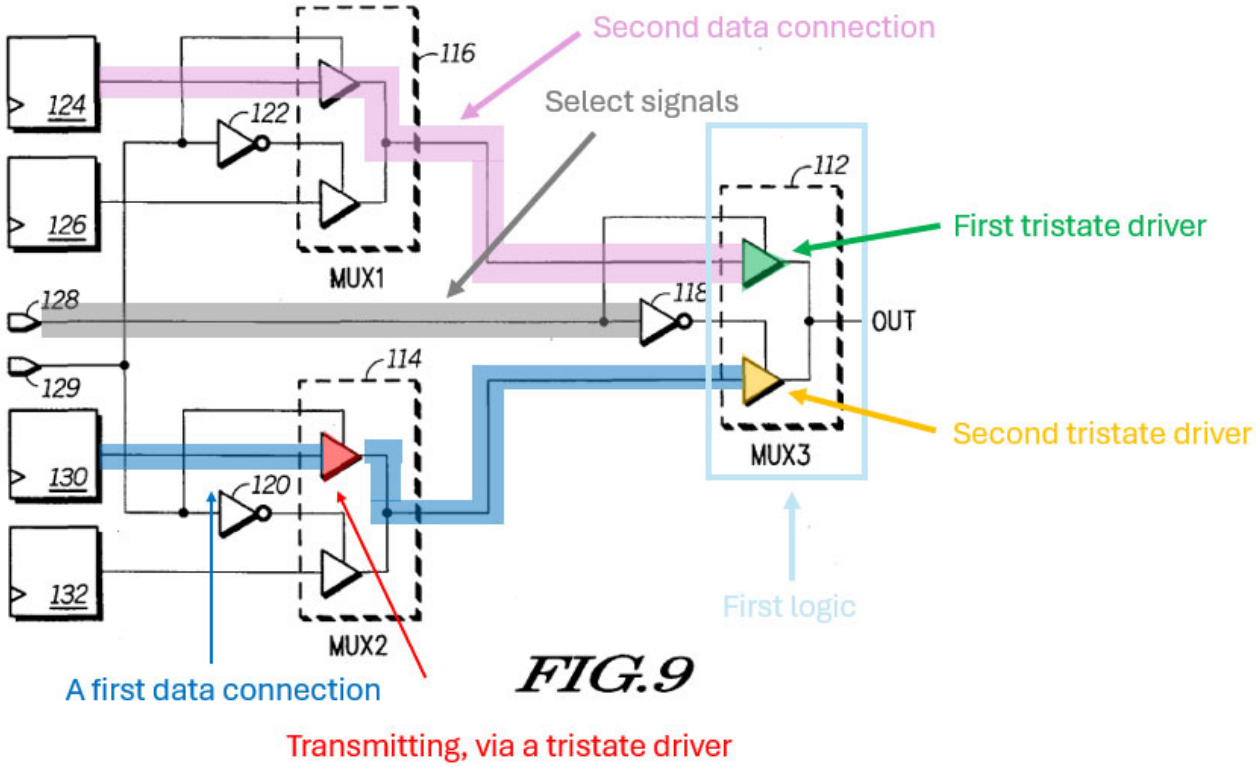


FIG.9

When the select signal input on terminal 128 is enabled (*i.e.*, a logic high), the first/upper tri-state driver of tri-state MUX 112 is enabled, and the second data word (highlighted in pink above) input to the upper tri-state driver is coupled to the output OUT of tri-state MUX 112. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶¶230-231. Correspondingly, the second/lower tri-state driver of tri-state MUX 112 receives a complement of the select signal input on terminal 128 via inverter 118, such that when the select signal input on terminal 128 is enabled, the output of

inverter 118 is disabled (*i.e.*, a logic low) and the second/lower tri-state driver of tri-state MUX 112 is disabled. *See id.*

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 ***drives the first data word to the connection via the second tristate driver if the data connection exclusion signal is asserted*** [*e.g.*, when the select signal input on terminal 128 is disabled/deasserted, the second/lower tri-state driver couples its input with the first data word to the output OUT of the tri-state MUX 112], ***and disables the first tristate driver if the data connection selection signal is deasserted*** [*e.g.*, when the select signal input on terminal 128 is disabled/deasserted, the first/upper tristate driver is disabled], as recited in [17.d]. EX1003, ¶232.

S. Claim 19

[19] Pixley-Watanabe renders Claim 19 obvious for the same reasons discussed above in Claim 6.

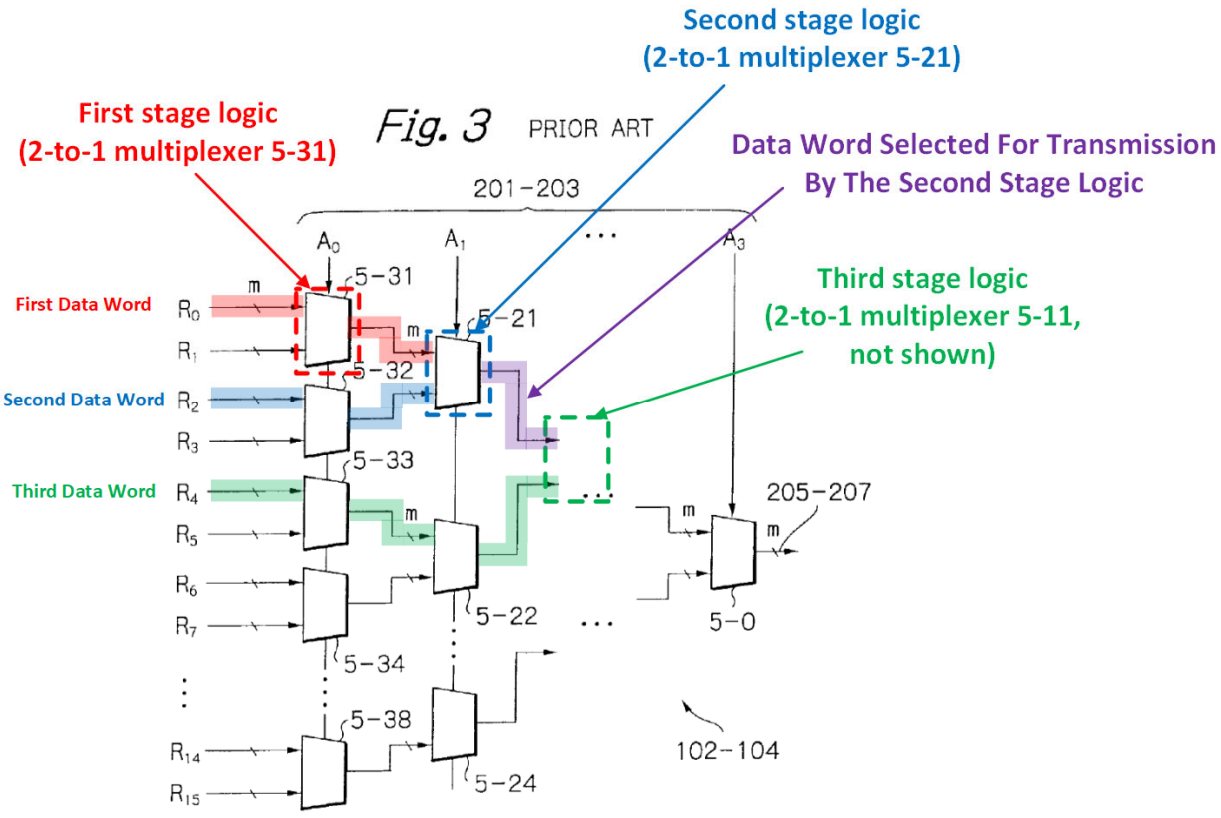
See Claim 6, *supra*; EX1003, ¶233.

T. Claim 20

[20.a] Pixley-Watanabe renders Element [20.a] obvious.

As described with respect to Element [1.pre] and Claim [3], *supra*, it was known that several m-bit 2-to-1 multiplexers could be nested, similar to the configuration shown in Pixley's FIG. 9. *See* Elements [1.pre] and [3]. This configuration was useful when the nested/cascading multiplexers were required to

select between more than four data inputs, as shown in Figure 3 from Watanabe (below). *See, e.g.*, EX1005, FIG. 3, [0035]-[0037].

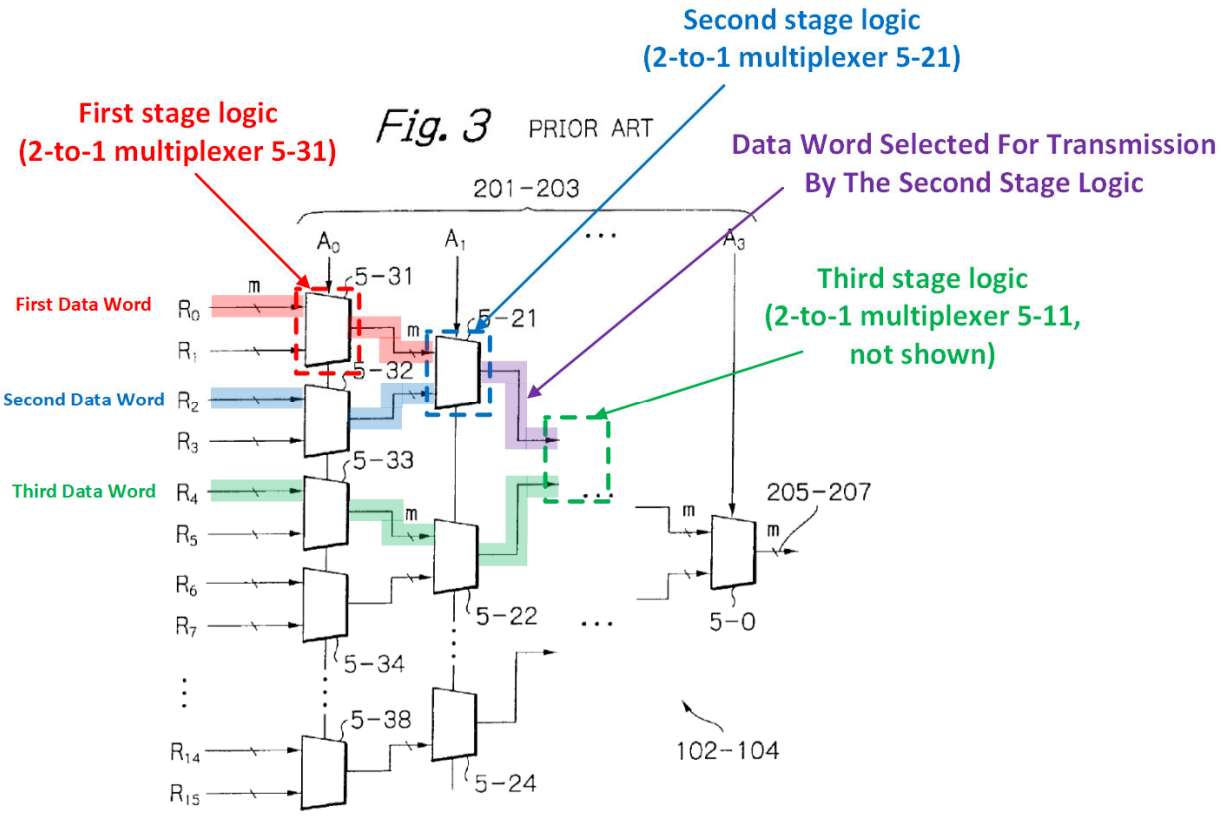


A POSITA would have found obvious that, in Pixley-Watanabe, the plurality of data words includes a third data word [*e.g.*, the m-bit data word received from the m D flip-flops, highlighted in green above] as recited in Element [20.a]. EX1003, ¶¶235-237.

[20.b] Pixley-Watanabe renders Element [20.b] obvious.

In one example of nested multiplexers described by Watanabe, for example as shown in Figure 3 (below), the output of a second stage MUX *(e.g.*, 2-to-1

multiplexer 5-21) is transmitted to the input of a third stage MUX (*e.g.*, 2-to-1 multiplexer 5-11). *See* EX1005, FIG. 3, [0036]-[0037].



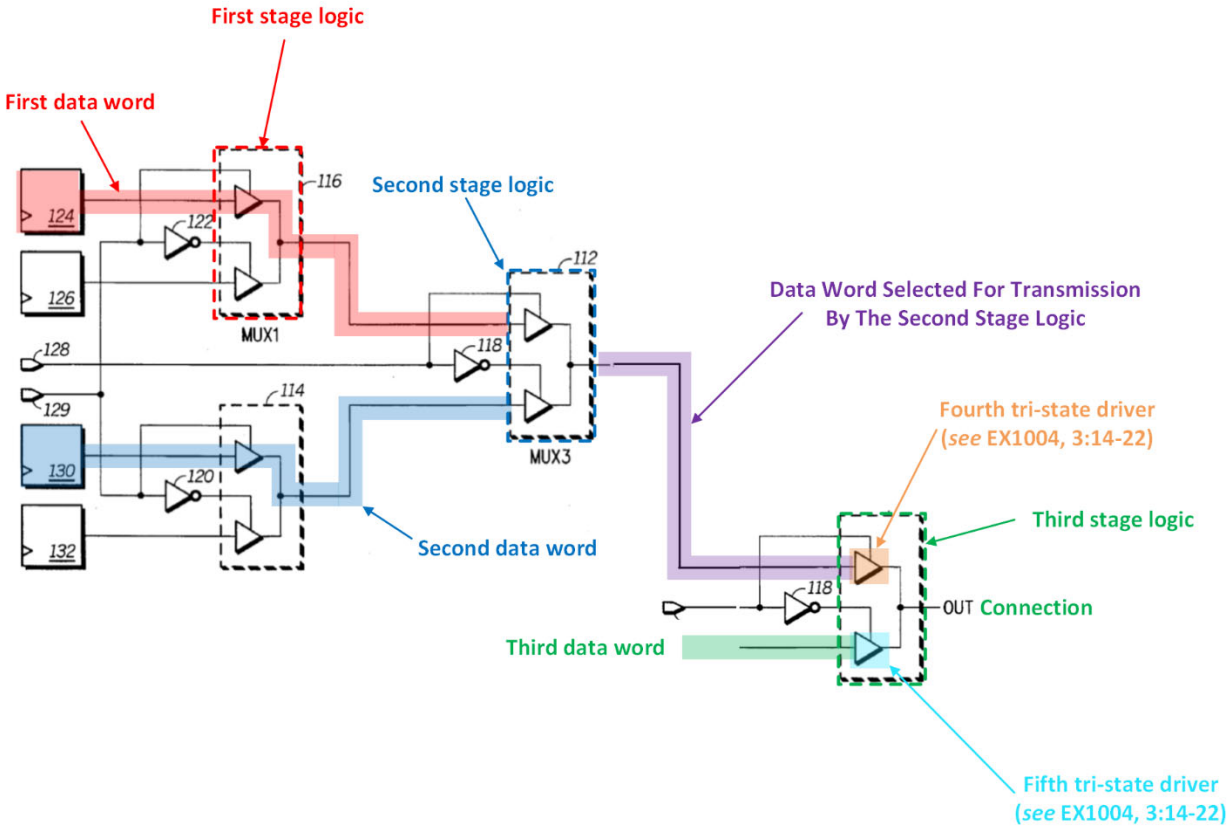
The third stage logic receives the third data word (highlighted in green above) and the data word selected for transmission by the second stage logic (highlighted in purple above). EX1003, ¶239.

As discussed with respect to [1.b]. Pixley teaches MUX circuits, each of which includes two tri-state drivers that are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶240.

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of FIG. 9 further comprises ***third stage logic*** [*e.g.*, a subsequent stage tri-state multiplexer in a larger nested multiplexer circuit with more than four data inputs, shown in green above], ***configured to receive the third data word*** [*e.g.*, the output of tri-state multiplexer would have been connected to the input of the subsequent stage tri-state multiplexer]***and the data word selected for transmission by the second stage logic*** [*e.g.*, the output of tri-state multiplexer would have been connected to the input of the subsequent stage tri-state multiplexer], as recited in [20.b]. EX1003, ¶241.

[20.c] Pixley-Watanabe renders Element [20.c] obvious.

As shown below, a POSITA would have recognized that the third stage logic would have the same structure as the other MUXes in FIG. 9 of Pixley, including the tri-state driver structure and selection signals. EX1003, ¶243.



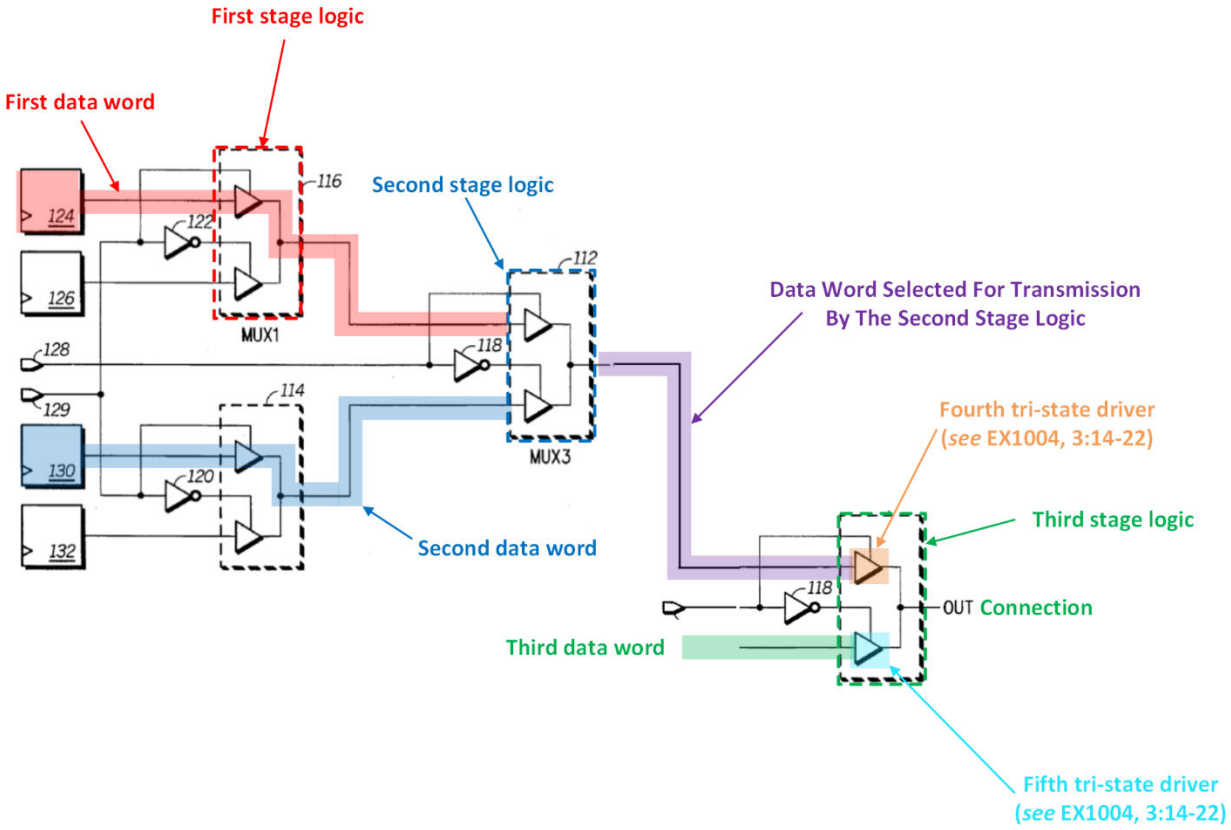
In the example of modified FIG. 9, a third logic (outlined by a green box) selects between the third data word and the data word selected for transmission by the second stage logic based on a select signal (received in the same manner as the other logics) and the output of inverter (inverted in the same manner as the other logics). *See* EX1003, ¶¶244-245.

Therefore, a POSITA would have found obvious that Pixley's nested multiplexers of modified FIG. 9 included ***the third stage logic*** [*e.g.*, tri-state MUX outlined in green, which is connected to the third data word and the data word selected for transmission by the second stage logic] ***configured to select for***

transmission one of the third data word [*e.g.*, the data output by tri-state MUX] ***and the data word selected for transmission by the second stage logic*** [*e.g.*, the data word highlighted in green above] ***based on a set of select signal*** [*e.g.*, the select signal of input terminal and the select signal output by the inverter], as recited in [20.c]. EX1003, ¶246.

[20.d] Pixley-Watanabe renders obvious Element [20.d].

As discussed with respect to [1.b]. "FIG. 9 illustrates a circuit having tri-state MUXes 112, 114, and 116," each of which includes two tri-state drivers that are enabled only if the corresponding select line is enabled and which couple the input line to the output when enabled. Element [1.b], *supra*; EX1004, FIG. 9, 3:14-22; 7:7-14; EX1003, ¶248. A POSITA would have recognized and found obvious that the third stage logic had the same structure as the prior stages. EX1003, ¶¶248-250.



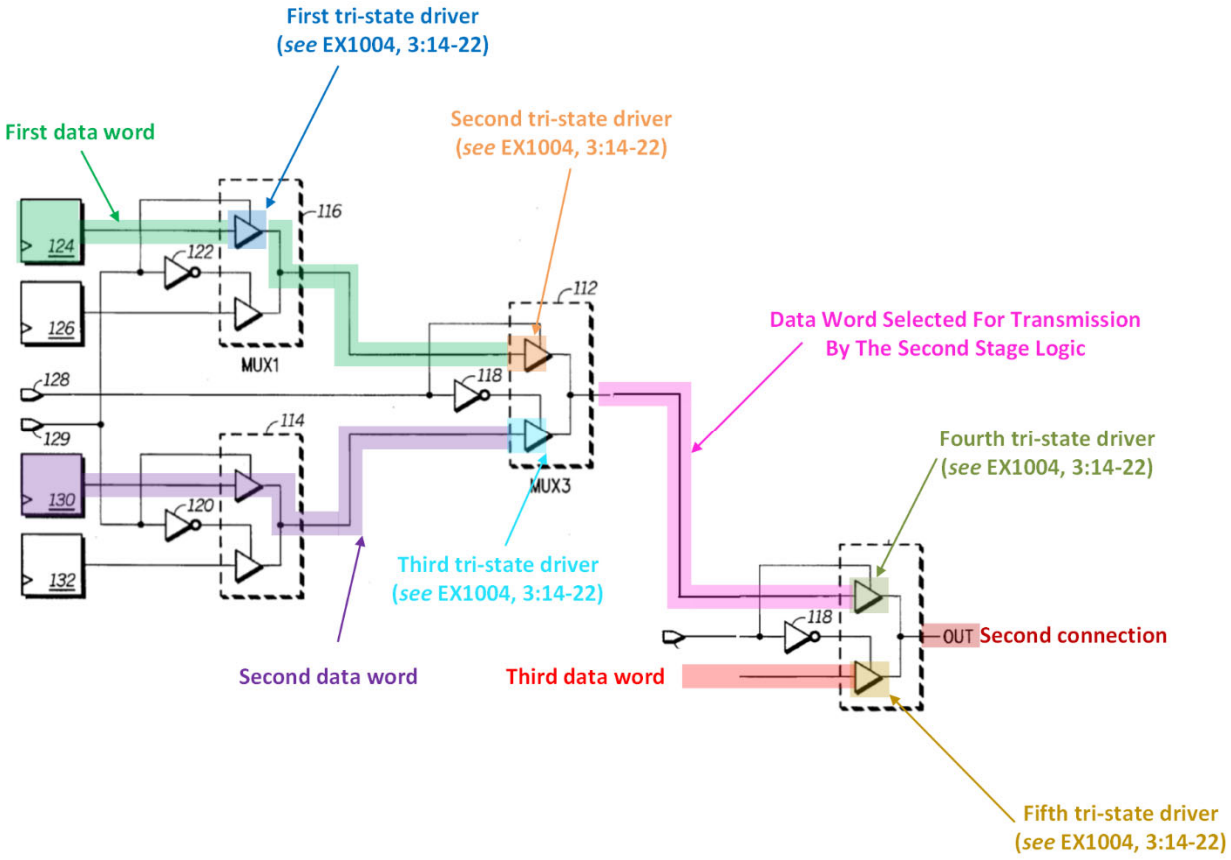
Therefore, a POSITA would have found obvious that Pixely's tri-state MUX [the third stage logic] in modified FIG. 9 included ***a connection*** [*e.g.*, output OUT of tri-state MUX], ***a fourth tristate driver*** [*e.g.*, the upper tri-state driver, highlighted in orange above], ***and a fifth tristate driver*** [*e.g.*, the lower tri-state driver, highlighted in light blue above], ***the fourth tristate driver having an output electrically coupled to an output of the fifth tristate driver*** [*e.g.*, the output of the upper and lower tri-state drivers of tri-state MUX are coupled together at OUT], ***the fourth tristate driver configured to receive the data word selected for transmission by the second stage logic and*** [*e.g.*, the upper tri-state driver (orange)

receives the data word selected from tri-state MUX 112] ***and to drive the connection of the third stage logic with the data word selected for transmission by the second stage logic if the data word selected for transmission by the second stage logic is selected for transmission by the third stage logic*** [*e.g.*, the data word received from the tri-state MUX 112 to the upper tri-state driver (orange) is coupled to OUT for transmission when the select signal input is enabled]***, the fifth tristate driver configured to receive the third data word and to drive the connection of the second stage logic with the third data word if the second data word is selected for transmission by the third stage logic*** [*e.g.*, lower tri-state driver (light blue) is coupled to OUT for transmission when the select signal output is enabled, which is when the select signal input is disabled], as recited in [20.d]. EX1003, ¶251.

U. Claim 21

[21] Pixley-Watanabe renders obvious Claim [21].

A POSITA would have recognized and found obvious that the third stage logic had the same structure as the prior stages. EX1003, ¶¶253-254.



In the example of modified FIG. 9, the fourth/upper tri-state driver (olive green) receives a data word selected for transmission by the second stage logic. *See* Element [1.c.ii]. Additionally, the second stage logic selects which input to send based upon selection signal 128. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶255. However, when the select signal input is enabled (*i.e.*, a logic high), the fourth/upper tri-state driver (olive green) is enabled, and the data word received from the second stage logic (highlighted in pink above) input to the upper tri-state driver is coupled to the output OUT, or second connection, and subsequently transmitted. *See* EX1004, FIG. 9, 3:14-22; EX1003, ¶255. Correspondingly, the

fifth/lower tri-state driver (gold) receives a complement of the select signal input via an inverter, such that when the select signal input is enabled, the output of the inverter is disabled (*i.e.*, a logic low) and the fifth/lower tri-state driver (gold) is disabled. *See id.* On the other hand, when the select signal input is disabled (*i.e.*, a logic low), the fourth/upper tri-state driver (olive gren) is disabled. *See id.* And, correspondingly, the fifth/lower tri-state driver (gold) receives a complement of the select signal input via an inverter, so when the select signal input is disabled, the output of the inverter is enabled (*i.e.*, a logic high) and the fifth/lower tri-state driver (gold) is enabled such that the third data word (highlighted in red above) input to the lower tri-state driver is coupled to the output OUT and transmitted. *See id.*

Therefore, a POSITA would have found obvious Pixley's nested multiplexers of modified FIG. 9 ***receives at a fourth tristate driver the data word selected by the selecting*** [*e.g.*, the fourth/upper tri-state driver (olive green) receives a first or second data word from the second tri-state MUX 112 depending on selection signal 128], ***selects for transmission between the received data word and a third data word based upon a set of select signals;*** [*e.g.*, selects between the data word received from tri-state MUX 112 (shown in pink above) and the third data word (shown in red above) based on the selection signal], ***drives a second connection with the received data word via the fourth tristate driver if the***

received data word is selected by the selecting for transmission between the received data word and the third data word [*e.g.*, the data word received from the tri-state MUX 112 to the upper tri-state driver (olive green) is coupled to OUT (second connection) and transmitted when the select signal input is enabled], ***and drives the second connection with the third data word if the third data word is selected by the selecting for transmission between the received data word and the third data word.*** [*e.g.*, the third data word from the tri-state MUX 112 to the lower tri-state driver (gold) is coupled to OUT (second connection) and transmitted when the select signal output from the inverter is enabled, which is when the select signal input is disabled], as recited in [21]. EX1003, ¶256.

V. PAYMENT OF FEES—37 C.F.R. §42.103

The Challenged Claims are unpatentable. Petitioner authorizes charge of fees to Deposit Account 06-1050.

VI. MANDATORY NOTICES—37 C.F.R. §42.8(a)(1)

A. Real Party-In-Interest—37 C.F.R. § 42.8(b)(1)

Infineon Technologies Americas Corp. is the Petitioner, and Infineon Technologies AG and Cypress Semiconductor Corporation are real parties-in-interest. No other parties had access to or control over the present Petition, and no other parties funded the present Petition.

B. Related Matters—37 C.F.R. § 42.8(b)(2)

To Petitioner's knowledge, the '448 Patent is only the subject of *MOSAID Technologies Inc. v. Infineon Technologies AG et al*, Case No. 1:25-cv-00358 (WDTX). Petitioner is not aware of any disclaimers, reexamination certificates, or current IPR petitions addressing the '448 Patent.

C. Lead And Back-Up Counsel—37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above. Petitioner consents to electronic service by email IPR60246-0005IP1@fr.com.

Respectfully submitted,

Dated: August 29, 2025

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(Control No. IPR2025-01489)

Attorneys for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,439 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: August 29, 2025

/Kenneth Wayne Darby Jr./

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Attorneys for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on August 29, 2025, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, to the Patent Owner, by serving the correspondence address of record as follows:

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