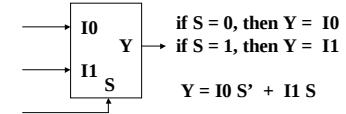
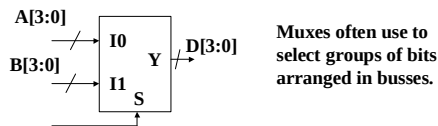


Combinational Building Blocks

2/1 Multiplexor (MUX)

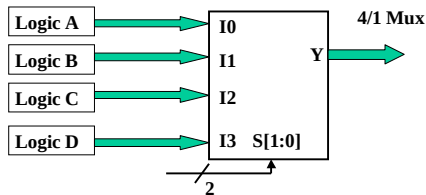


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1

What Good are Muxes ??

Sometimes want to have a bus be driven from multiple blocks, where only one block is driving the bus at a time.

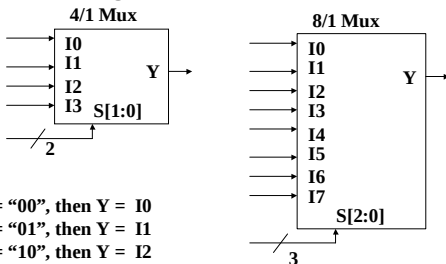


N to 1 mux will select 1 source; Select bus needs to be $\log_2(N)$. Note that only ONE input can be selected at a time!

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2

Higher Order Muxes



$$Y = I_0 S_1' S_0' + I_1 S_1' S_0 + I_2 S_1 S_0' + I_3 S_1 S_0$$

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3

Logic for 2/1, 4/1 Muxes

$Y = I_0 S' + I_1 S$

$Y = I_0 S_1' S_0' + I_1 S_1' S_0 + I_2 S_1 S_0' + I_3 S_1 S_0$

These are called **COMBINATIONAL** muxes.

BR 8/99 4

Tri State Buffer

There is another way to drive a line or bus from multiple sources. Use a TRISTATE buffer.

When $EN = 1$, then $Y = A$.

When $EN = 0$, then $Y = \text{?????}$
 Y is *undriven*, this is called the **high impedance state**.

Designate high impedance by a 'Z'.

When $EN = 0$, then $Y = 'Z'$ (high impedance)

BR 8/99 5

Using TriState Buffers

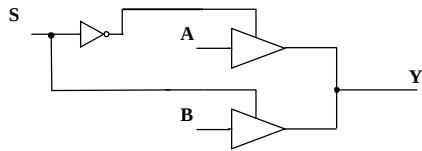
Can use tristate buffers instead of a combinational 2/1 mux

Must make sure that ENA , ENB are not both '1' at same time, or Y will be driven from multiple sources

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Using TriState Buffers (cont)

Only A or B is enabled at a time.



Implements 2/1 Mux function

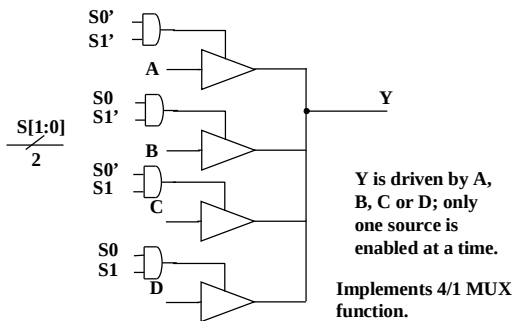
If $S=0$ then $Y = A$

If $S=1$ then $Y = B$

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7

Using TriState Buffers (cont)



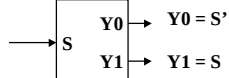
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8

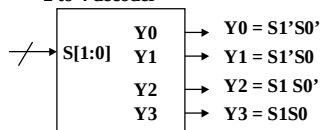
Decoders

Logic common to both of the previous mux implementations was the *decoder* function.

1 to 2 decoder

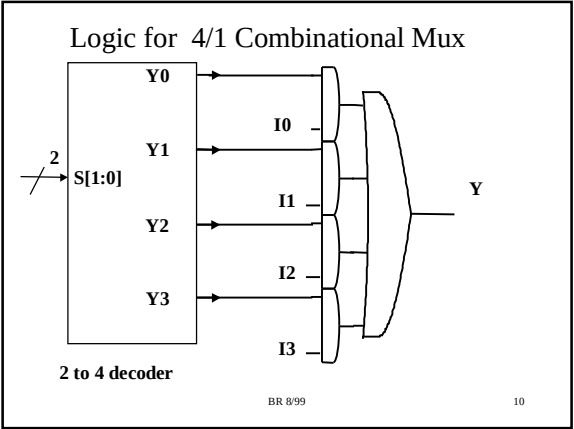


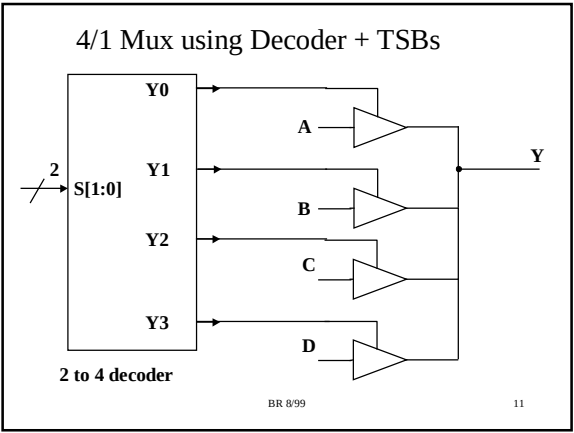
2 to 4 decoder

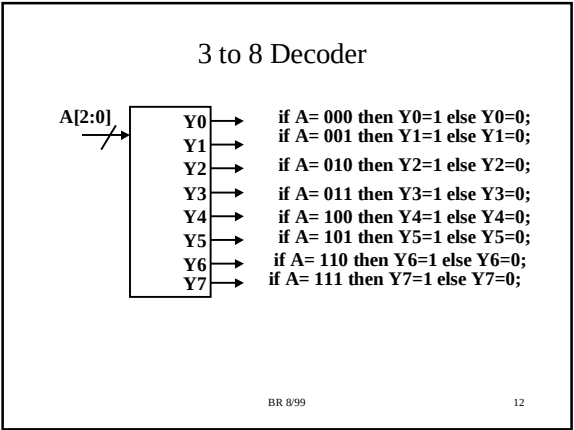


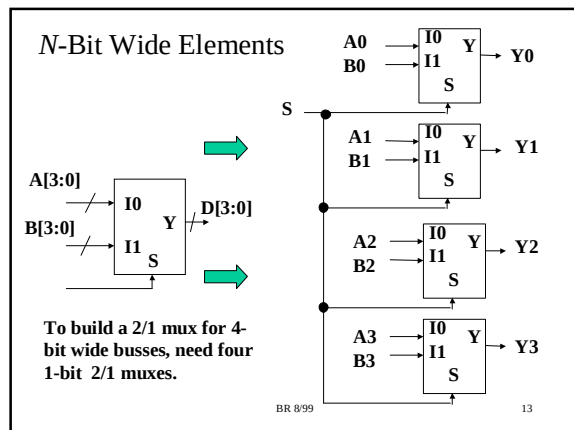
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9









Review of Memory example

$F(A,B,C) = A \text{ xor } B \text{ xor } C$ $G = AB + AC + BC$

A	B	C	F	G
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Recall that Exclusive OR (xor) is

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

$Y = A \oplus B$
 $= A \text{ xor } B$

8 x 2 Memory

LookUp Table (LUT)

A[2:0] is 3 bit address bus, D[1:0] is 2 bit output bus.
 Location 0 has "00",
 Location 1 has "10",
 Location 2 has "10",
 etc....

BR 8/99 14

Binary Adder

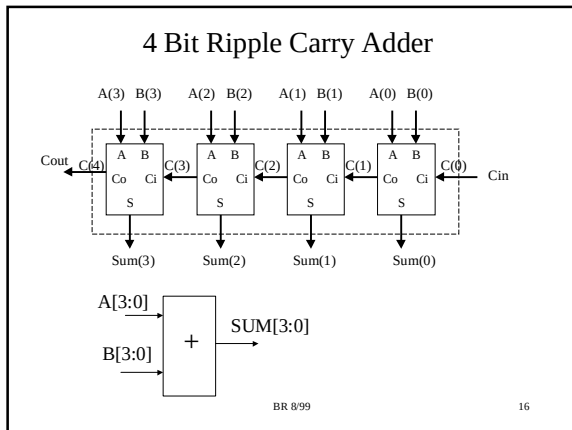
$F(A,B,C) = A \text{ xor } B \text{ xor } C$ $G = AB + AC + BC$

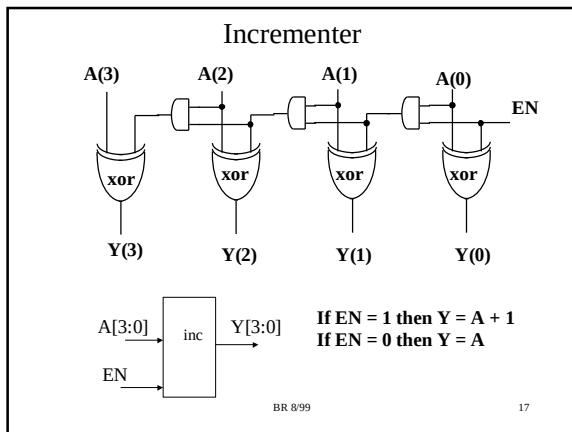
These equations look familiar. These define a **Binary Full Adder**:

Sum = $A \text{ xor } B \text{ xor } C_{in}$
 Cout = $AB + C_{in}A + C_{in}B$
 $= AB + C_{in}(A + B)$

Full Adder (FA)

BR 8/99 15





What do You have to know?

- Structures for Muxes, Decoders, Ripple Carry adder, Incrementer
- What a tristate buffer is
- How to build muxes from all combinational logic or from combinational logic + tristate buffers
- Bus naming convention
- How to build N-bit wide elements from 1-bit wide elements

BR 8/99 18
