

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INFINEON TECHNOLOGIES AMERICAS CORP.,
Petitioner,

v.

MOSAID TECHNOLOGIES INC.,
Patent Owner.

Case IPR2025-01489
Patent No. 7,349,448

PATENT OWNER'S PRELIMINARY RESPONSE

TABLE OF CONTENTS

	Page
I. INTRODUCTION	1
II. PETITIONER FAILS TO DEMONSTRATE OBVIOUSNESS OVER ITS LONE PIXLEY/WATANABE GROUND (ALL CLAIMS).	2
A. The Petition Is Deficient Because It Does Not Disclose, Reconcile, Or Apply Its District Court Claim Constructions.	2
1. Petitioner’s Means-Plus-Function Arguments For The “Logic” Terms Are Not Disclosed Or Reconciled.	4
a. Petitioner Fails To Disclose Its Means-Plus-Function Arguments From The District Court.	4
b. Petitioner Fails To Demonstrate That Pixley/Watanabe Teach The “Logic” Terms Under Petitioner’s Own District Court Construction.	7
2. Petitioner’s Indefiniteness Argument For “The First Selected Signal Set” Is Not Disclosed Or Reconciled.....	13
B. Petitioner Fails To Demonstrate That Pixley/Watanabe Teach Multiplexing “Data Words” (All Claims).	15
1. Pixley Alone Does Not Teach Multiplexing “Data Word[s].”	16
a. Petitioner Fails To Prove A Single Bit Can Be A “Data Word.”	16
b. Pixley Only Discloses Multiplexing One Bit At A Time.....	21
2. Petitioner Fails To Demonstrate That A POSITA Would Be Motivated To Combine Pixley And Watanabe.....	24
III. CONCLUSION	30

TABLE OF AUTHORITIES

Page(s)

COURT DECISIONS

<i>InTouch Techs., Inc. v. VGo Commc'ns., Inc.</i> , 751 F.3d 1327 (Fed. Cir. 2014)	29
<i>In re Kahn</i> , 441 F.3d 977 (Fed. Cir. 2006)	17
<i>KSR Int'l Co. v. Teleflex Inc.</i> , 550 U.S. 398 (2007).....	17
<i>In re Magnum Oil Tools Int'l, Ltd.</i> , 829 F.3d 1364 (Fed. Cir. 2016)	17
<i>Ruiz v. A.B. Chance Co.</i> , 357 F.3d 1270 (Fed. Cir. 2004)	29
<i>Univ. of Strathclyde v. Clear-Vu Lighting LLC</i> , 17 F.4th 155 (Fed. Cir. 2021)	29
<i>Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.</i> , 97 F.4th 882 (Fed. Cir. 2024)	18, 28

AGENCY DECISIONS

<i>10x Genomics, Inc. v. Pres. and Fellows of Harvard Coll.</i> , IPR2023-01299, Paper 15 (Mar. 7, 2024)	7
<i>Cambridge Mobile Telematics, Inc. v. Sfara, Inc.</i> , IPR2024-00952, Paper 12 (Dec. 13, 2024) (informative)	3, 6

<i>Orthopediatrics Corp. v. K2M, Inc.</i> , IPR2018-01546, Paper 10 (Feb. 14, 2019).....	7
<i>Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.</i> , IPR2025-00632, Paper 20 (Nov. 3, 2025) (precedential)	3, 9
<i>RPX Corp. v. Parity Networks, LLC</i> , IPR2018-00097, Paper 7 (Apr. 24, 2018).....	29
<i>Sportsradar AG v. Sportscaster Inc.</i> , IPR2025-00313, Paper 19 (July 16, 2025)	5
<i>Sun Pharm. Indus. Ltd. v. Nivagen Pharm., Inc.</i> , IPR2025-00893, Paper 18 (Sept. 19, 2025).....	4
<i>Tesla, Inc. v. Intellectual Ventures II LLC</i> , IPR2025-00340, Paper 18 (Nov. 5, 2025) (informative)	4, 15
<i>Xerox Corp. v. Bytemark, Inc.</i> , IPR2022-00624, Paper 9 (Aug. 24, 2022) (precedential)	19

STATUTES

35 U.S.C. § 112(f).....	6, 7
35 U.S.C. § 314(a)	30

REGULATIONS

37 C.F.R. § 42.104(b)(3).....	3, 6, 7
37 C.F.R. § 42.104(b)(4).....	6

37 C.F.R. § 42.65(a).....	18
---------------------------	----

EXHIBIT LIST	
2001	Lowenstein Declaration In Support of Notice of Intent
2002	Woo Declaration In Support of Notice of Intent
2003	Courtney Declaration In Support of Notice of Intent
2004	Complaint in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00358 (W.D. Tex.), Dkt. 1 (Mar. 25, 2025) [Complaint]
2005	November 3, 2017 Notice Letter to Cypress Semiconductor Corporation [11/03/17 Letter] (CONFIDENTIAL)
2006	First Amended Scheduling Order in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00358 (W.D. Tex.), Dkt. 43 (Oct. 17, 2025) [Amended-Scheduling-Order]
2007	Defendant's Opening Claim Construction Brief in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00358 (W.D. Tex.), Dkt. 44 (Oct. 27, 2025) [Opening-Claim-Construction-Brief]
2008	Defendants' Election of Asserted Prior Art Grounds in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00358 (W.D. Tex.) (served Nov. 3, 2025) [Election-of-Grounds]
2009-2011	Reserved
2012	Declaration of Boris Teksler [Teksler-Decl.] (CONFIDENTIAL)
2013	Press Release, Infineon Technologies AG completes acquisition of Cypress Semiconductor Corporation (Apr. 16, 2020) [Press-Release-Cypress]
2014	Letter from Cypress (May 5, 2019) [05/05/19 Letter] (CONFIDENTIAL)

2015	Response Presentation (April 2018) [04/18 Presentation] (CONFIDENTIAL)
2016	Cypress Chart (Aug. 1, 2018) [8/1/18 Chart] (CONFIDENTIAL)
2017	Response Presentation (Sept. 26, 2018) [09/26/18 Conversant Presentation] (CONFIDENTIAL)
2018	Conversant Response Presentation (June 21, 2019) [06/21/19 Conversant Response Presentation] (CONFIDENTIAL)
2019	Conversant Response Presentation (Dec. 4, 2019) [12/04/19 Conversant Response Presentation] (CONFIDENTIAL)
2020-2021	Reserved
2022	MOSAID – Infineon/Cypress Presentation (February 28, 2023) [02/28/23 MOSAID-Infineon/Cypress Presentation] (CONFIDENTIAL)
2023	Email chain (April 14, 2023) [4/14/23 Email] (CONFIDENTIAL)
2024	Reserved
2025	Infineon’s Preliminary Invalidity Contentions in <i>MOSAID Technologies Inc. v. Infineon Technologies AG, et al.</i> , No. 1:25-cv-00358 (W.D. Tex.) (served Aug. 15, 2025) [Invalidity-Contentions]
2026	Declaration and CV of Sunil P. Khatri, Ph.D.
2027	Excerpts from Microsoft Computer Dictionary (5th ed. 2002) [Microsoft-Computer-Dictionary]
2028	Excerpts from PAUL HOROWITZ & WINFIELD HILL, THE ART OF ELECTRONICS (3d ed. 2015) [Horowitz]
2029	Excerpts from PATRICK JUOLA, PRINCIPLES OF COMPUTER ORGANIZATION AND ASSEMBLY LANGUAGE (2007) [Juola]

2030	Rahul Awati, <i>What is bit (binary digit) in computing?</i> , TECHTARGET.COM/WHATIS (Jun. 6, 2025), https://www.techtarget.com/whatis/definition/bit-binary-digit [TechTarget]
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All emphases in quotations are added unless otherwise stated.

I. INTRODUCTION

The Petition should be denied as it fails to demonstrate a reasonable likelihood of prevailing on any challenged claim.

Petitioner's sole asserted ground, Pixley/Watanabe, should be rejected for multiple reasons. In contravention of recent precedential and informative Director Decisions, Petitioner fails to disclose or explain its different claim construction positions. In the district court, Petitioner insists that the "logic" terms "*must* be construed as means-plus-function limitations," further offering an alternative construction if they are not construed as means-plus-function limitations. Ex. 2007 [Opening-Claim-Construction-Brief] 22–29. Additionally, Petitioner argues that "the first selected signal set" limitation is indefinite. *Id.*, 29–30. By contrast, in the Petition, Petitioner does not mention these constructions and argues that "[n]o formal claim constructions are necessary." Pet., 8. This unexplained inconsistency is sufficient reason to deny institution. *See* Section II.A.

Further, Petitioner fails to demonstrate that Pixley/Watanabe teaches multiplexing a "data word." *See* Section II.B. Petitioner argues that because the '448 patent allegedly "does not preclude a 'data word' from being one bit," Pixley—which multiplexes one bit at a time—alone teaches these limitations. But Petitioner fails to substantiate its implicit claim construction and thus fails to demonstrate that Pixley teaches these limitations. *See* Section II.B.1. Recognizing

Pixley's shortcoming, Petitioner also argues that "a POSITA would have at least found it obvious that Pixley's multiplexer would operate with respect to multi-bit data words" per Watanabe's teachings. Petitioner, however, fails to demonstrate that a POSITA would have been motivated to combine Pixley and Watanabe. *See* Section II.B.2.

The Petition never reaches the threshold showing of a reasonable likelihood of success on any claim. For each of these reasons, institution should be denied.

II. PETITIONER FAILS TO DEMONSTRATE OBVIOUSNESS OVER ITS LONE PIXLEY/WATANABE GROUND (ALL CLAIMS).

A. The Petition Is Deficient Because It Does Not Disclose, Reconcile, Or Apply Its District Court Claim Constructions.

In the Petition, Petitioner maintains that "[n]o formal claim constructions are necessary." Pet., 8. In the District Court Action, however, Petitioner takes the opposite approach, insisting that multiple claim terms of the '448 patent (i) should be construed as means-plus-function or (ii) are indefinite.

The '448 patent is currently asserted in *MOSAID Technologies Inc. v. Infineon Technologies AG, et al.*, No. 1:25-cv-00358 (W.D. Tex.) (the "District Court Action"). There, Petitioner argues that the "first," "second," and "third" "stage logic[s]" recited in asserted claims (4 and 8) "*must* be construed as means-plus-function limitations." Ex. 2007 [Opening-Claim-Construction-Brief] 22. Alternatively, Petitioner argues that the District Court "should construe 'second

stage logic *configured to receive the first data word from the first stage logic...*

[and the associated language from claim 8] to mean that the second stage logic has an input configured to receive a data word from the output of a first stage logic.”

Id., 28–29 (emphasis in original). Petitioner also contends that the limitation “the first selected signal set” is indefinite. *Id.*, 29–30. Petitioner does not disclose these positions to the Board, does not attempt to reconcile them with its no-construction-necessary position here, and does not show that its sole Pixley/Watanabe ground renders the claims obvious even under its own proposed constructions.

Under recent Director decisions, that combination of nondisclosure, inconsistency, and substantive failure warrants denial of institution. In *Revvo*, the Director explained that while “the Board’s rules do not necessarily prohibit petitioners from taking inconsistent claim construction positions before the Board and a district court,” a petitioner that advances different positions “should, at a minimum, explain why alternative positions are warranted.” in order to comply with 37 C.F.R. § 42.104(b)(3)’s requirement that the petition must set forth a statement of “[h]ow the challenged claim is to be construed” *Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20, 3–5 (Nov. 3, 2025) (precedential) (quoting *Cambridge Mobile Telematics, Inc. v. Sfara, Inc.*, IPR2024-00952, Paper 12, 8–9 (Dec. 13, 2024) (informative)); *see also Sun Pharm. Indus.*

Ltd. v. Nivagen Pharm., Inc., IPR2025-00893, Paper 18, 2–3 (Sept. 19, 2025)

(denying institution where petitioner advanced narrow construction in district court and a broader “plain and ordinary meaning” in petition without sufficient explanation, noting that unexplained differences undermine Office’s goal of “uniformity and predictability” in claim construction). In *Tesla*, the Director denied institution where the petitioner argued indefiniteness of a term in district court while telling the Board that “no claim terms presently require a formal construction,” holding that the mere fact that indefiniteness cannot be raised in an IPR “is not a sufficient explanation” for the divergent positions and that, at a minimum, the petitioner had to either justify the difference or show that, even assuming definiteness, the prior art still met the limitation. *Tesla, Inc. v.*

Intellectual Ventures II LLC, IPR2025-00340, Paper 18, 3–4 (Nov. 5, 2025)

(informative).

1. Petitioner’s Means-Plus-Function Arguments For The “Logic” Terms Are Not Disclosed Or Reconciled.
 - a. *Petitioner Fails To Disclose Its Means-Plus-Function Arguments From The District Court.*

In the District Court Action, Petitioner argues that the “first,” “second,” and “third” “stage logic[s]” recited in asserted claims 4 and 8—the only asserted

claims—“*must* be construed as means-plus-function limitations.”¹ Ex. 2007 [Opening-Claim-Construction-Brief] 22. According to Petitioner, “logic” is a “well-known nonce term from which a POSITA would discern no structure” and thus “should be construed pursuant to § 112 ¶ 6,” with the corresponding structure for each “logic” term being the distributed multiplexer logic (“DML”) stages 204, 205, and 206 shown in Figure 4 of the ’448 patent. *Id.*, 22–25, 26–28. In other words, Petitioner’s district court position is that the “logic” terms can only be met by the DML stages disclosed in Figure 4, not by generic “logic” in the abstract.

Here, by contrast, Petitioner tells the Board that “[n]o formal claim constructions are necessary.” Pet., 8. Petitioner does not disclose its district court means-plus-function position, does not identify the DML stages as corresponding structure, and does not attempt to reconcile its “plain meaning” position here with

¹ Claims 4 and 8 are the only asserted claims. Consequently, Petitioner’s failure to reconcile its district court means-plus-function position still warrants denying institution because claims 4 and 8 are the only claims in dispute between the parties in the district court. *Cf. Sportsradar AG v. Sportscaster Inc.*, IPR2025-00313, Paper 19, 2 (July 16, 2025) (denying institution because “it is an inefficient use of Board resources to review claims of a patent that are no longer being asserted in district court.”).

its § 112 ¶ 6 position in court. This omission violates the Office’s rules, which require a petitioner to set forth “[h]ow the challenged claim is to be construed” and “[h]ow the construed claim is unpatentable.” 37 C.F.R. §§ 42.104(b)(3)–(4) . Moreover, “[w]here the claim to be construed contains a means-plus-function ... limitation ... the construction of the claim **must** identify the specific portions of the specification that describe the structure, material, or acts corresponding to each function.” *Id.* And as the CTPG makes clear, even “[w]here the claim language **may be** construed according to 35 U.S.C. § 112(f), a petitioner **must** provide a construction.” CTPG, 45 (“A petitioner who chooses not to address construction under § 112(f) risks failing to satisfy the requirement of 37 C.F.R. § 42.104(b)(3).”).

For good reason, the Director and the Board have rejected Petitioner’s approach. Indeed, the facts here echo those present in *Cambridge Mobile Telematics, Inc. v. Sfara, Inc.*, IPR2024-00952, Paper 12, 5–9 (Dec. 13, 2024) (informative). There, as here, the petitioner “emphasized the importance of resolving whether the ‘component’ terms are means-plus-function terms” and “clearly and emphatically stated that whether the ‘component’ terms are means-plus-function limitations is a dispositive issue for the litigation,” confirming the petitioner’s “belie[f] that the claims contain a means-plus-function limitation, thereby implicating 37 C.F.R. § 42.104(b)(3),” while “not address[ing] the issue”

in the petition, “merely provid[ing] a footnote to state its litigation position.” *Id.*, 7–8. The only difference here is that no such footnote disclosure was present in the Petition.

There, the Board found that the Petition “failed” to comply with 37 C.F.R. § 42.104(b)(3), stating that “[a]t a minimum, the Petition should have explained why the plain and ordinary meaning of the ‘component’ terms should apply in this proceeding (why the inconsistent positions are warranted) or set forth an alternative means-plus-function claim construction.” *Id.*, 8; *see 10x Genomics, Inc. v. Pres. and Fellows of Harvard Coll.*, IPR2023-01299, Paper 15, 11–13 (Mar. 7, 2024) (similar, holding “Petitioner is now left with the consequences of its strategic choice to not address § 112(f) in the Petition”); *Orthopediatrics Corp. v. K2M, Inc.*, IPR2018-01546, Paper 10, 10–11 (Feb. 14, 2019). Here too, Petitioner failed to comply with its bare minimum obligation and is left with the “consequences of its strategic choice not to address § 112(f) in the Petition.” This is reason enough to deny institution.

b. *Petitioner Fails To Demonstrate That Pixley/Watanabe Teach The “Logic” Terms Under Petitioner’s Own District Court Construction.*

Petitioner not only does not disclose its means-plus-function constructions, it also does not attempt to show that they are met. Petitioner fails to identify the “DML stage[s]” it contends that the “logic” terms require in claims 4 and 8. For

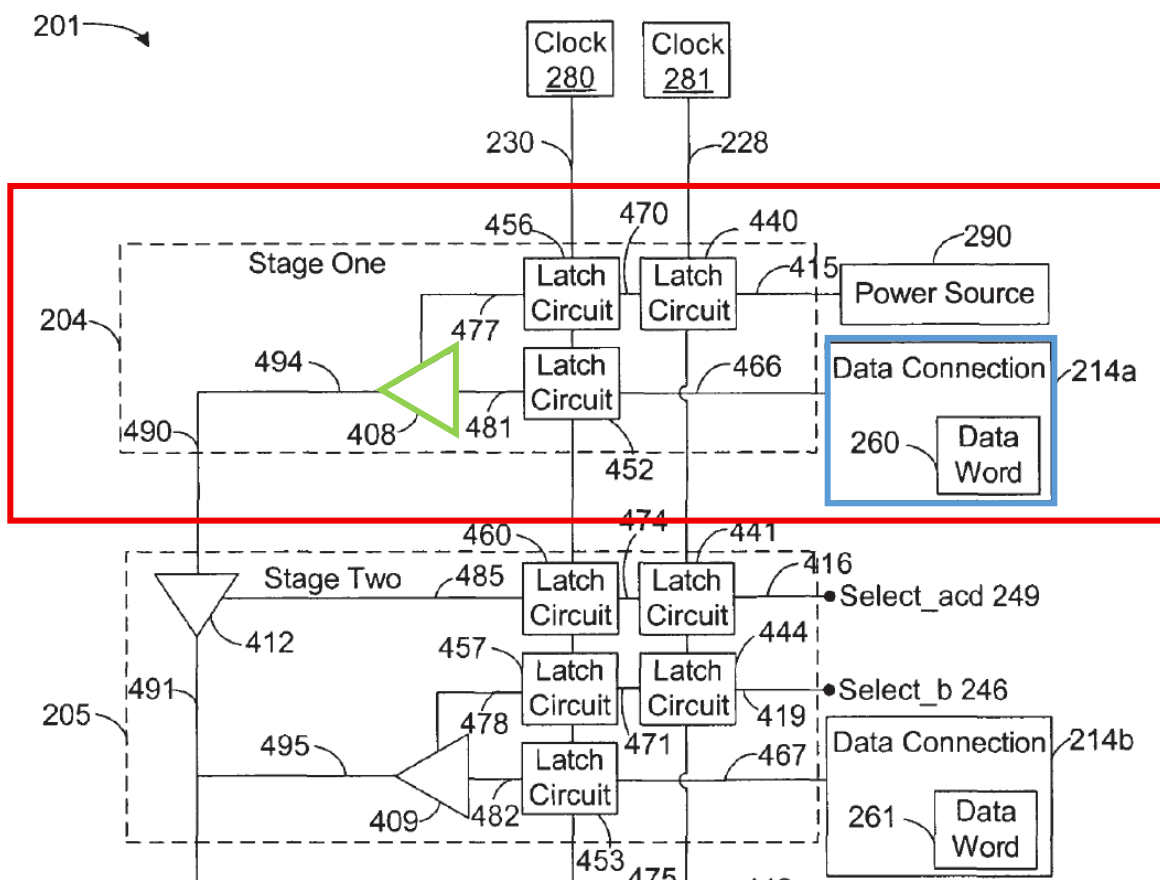
example, in claim 8, Petitioner contends that “logic associated with a first data connection ... configured to transmit a first data word corresponding to the first data connection” is taught by Pixley’s alleged “set of flip-flops 124.”² Pet., 44–46 (“A POSITA would have understood that flip-flops are a form of ‘cyclic logic circuits,’ and are therefore a form of logic.”). Petitioner’s district court position, however, is in no uncertain terms that the “logic” limitations require the “DML stage[s]” depicted in the ’448 patent’s Figure 4. Petitioner does not even mention let alone attempt to prove that Pixley’s “set of flip-flops 124” teaches a “DML stage.”³ *See id.*

² Pixley only depicts one flip-flop as element 124. Ex. 1004 [Pixley] Fig. 9, 7:11-14. Petitioner proposes modifying flip-flop 124 to be a “set of flip-flops 124” in order to multiplex more than one bit a time. Pet., 45-46. As further explained below, however, Petitioner fails to demonstrate that a POSITA would have been motivated to modify Pixley as proposed. *See* Section II.B.

³ To be sure, Patent Owner disputes Petitioner’s district court position that the “logic” terms of claims 4 and 8 require the tristate drivers depicted in the ’448 patent’s Figure 4. But, as the Director has made clear, a petitioner may not advance a disputed claim construction position in the district court while failing to

Moreover, there is no reason to believe that the “set of flip-flops 124” is a “DML stage” as depicted in Figure 4 that Petitioner insists in the District Court Action is required by the “logic associated with a first data connection.” Figure 4 depicts **DML stage 204** as the stage associated with the **first data connection**

214a:



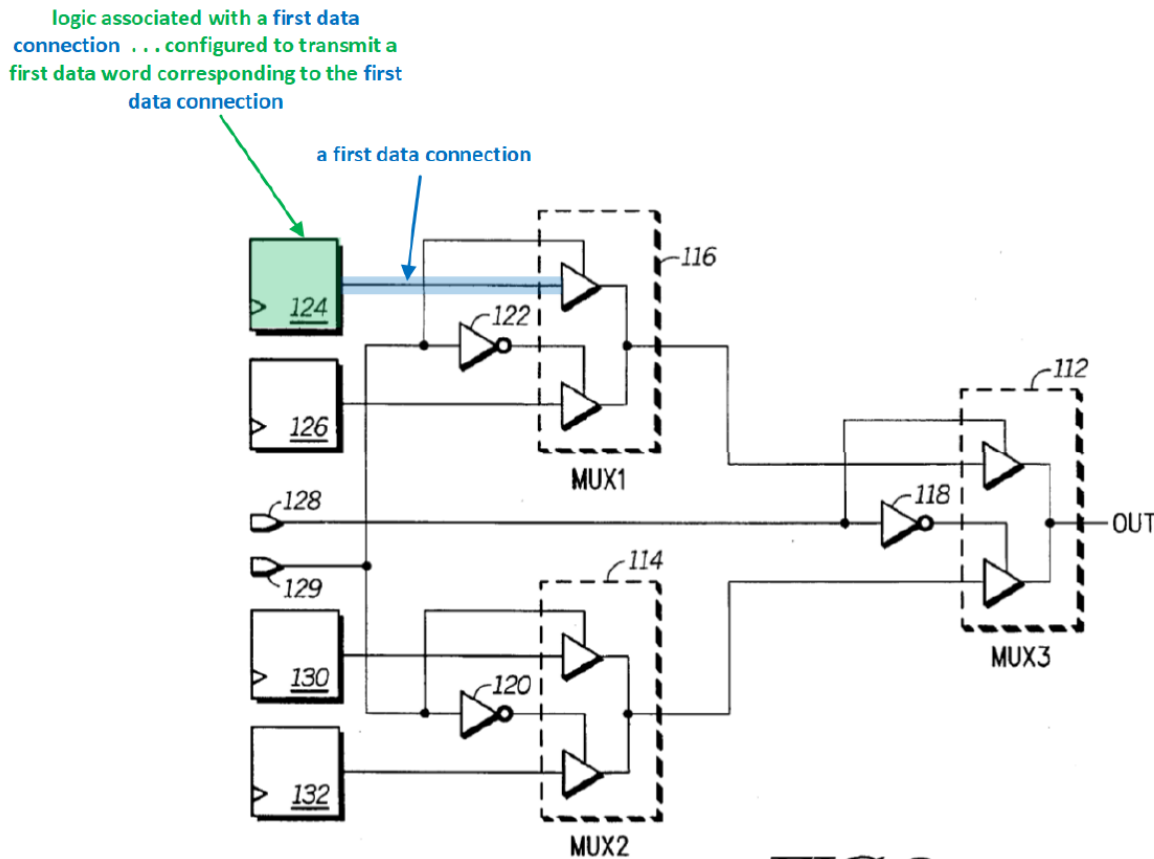
Ex. 1001 ['448] Fig. 4 (annotated).

reconcile that stance with its IPR position. *See Revvo Techs., Inc. v. Cerebrum Sensor Techs., Inc.*, IPR2025-00632, Paper 20, 3–5 (Nov. 3, 2025).

As can be seen above, DML stage 204 includes “**data connection tristate driver[] 408[]**, ... which receives and outputs its associated data word...” *Id.*, 7:15-20. In accord, in the District Court Action, Petitioner repeatedly emphasizes that the structure of the DML stages illustrated in Figure 4 includes a tristate driver in each stage. *E.g.*, Ex. 2007 [Opening-Claim-Construction-Brief] 21 (“As illustrated in Figure 4, ‘[e]ach DML stage 204-207, preferably **comprises data connection selection tristate drivers 408-411...**’”); 26–27 (similar); 21 (“When the select logic is driven to select a data word corresponding to a DML stage, **that DML stage’s data connection selection tristate driver** is activated”); 25 (“MOSAID then agreed in its response, contending that the amended claims it submitted were allowable because the prior art ‘fail[ed] to disclose at least an arrangement of ‘tristate drivers.’”). Thus, per Petitioner’s district court view, claim 8’s “logic associated with a first data connection” requires a tri-state driver.

Here, however, Petitioner never points to any tristate driver (per its District Court Action position) when mapping claim 8’s “logic associated with a first data connection,” as Dr. Khatri explains:

Again, in the Petition, Petitioner relies upon Pixley’s “set of flip-flops 124” as the “logic associated with a first data connection,” as depicted below:

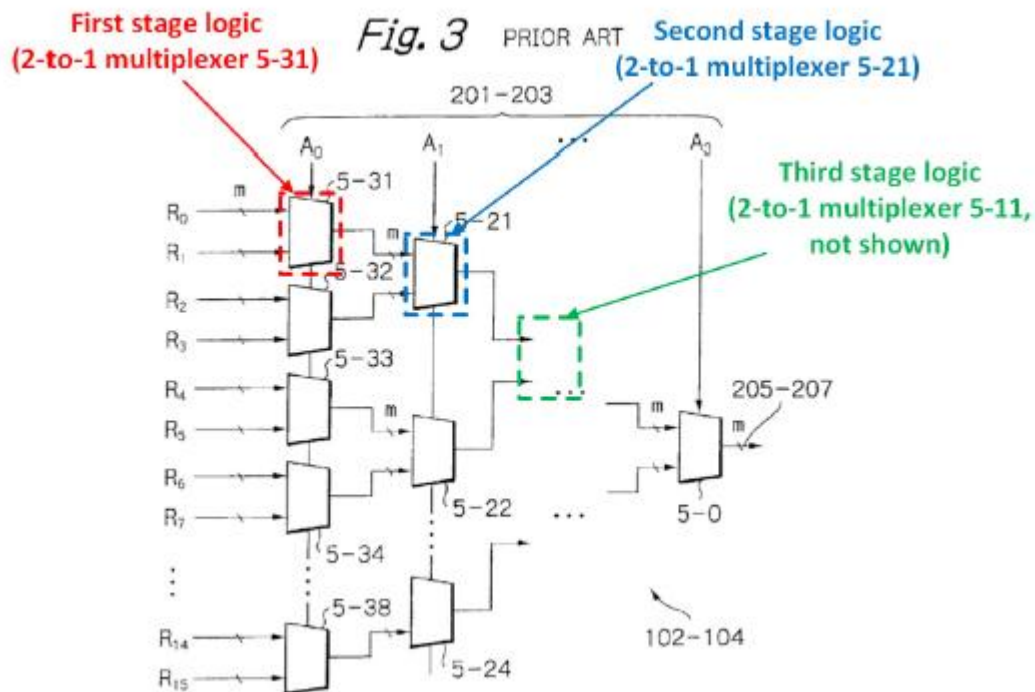


Pet., 45 (Petitioner’s annotation of Pixley’s Fig. 9); *id.* (“A POSITA would have understood that flip-flops are a form of ‘cyclic logic circuits,’ and are therefore a form of logic.”). As can be seen above, Petitioner does not identify any tri-state driver as being part of “logic associated with a first data connection.” Nor does Petitioner allege that the “set of flip-flops 124” is or somehow includes a tri-state driver. Indeed, as their names would imply, flip-flops are entirely different circuit elements from tri-state drivers. *Compare* Ex. 2027 [Microsoft-Computer-Dictionary] 218 (“flip-flop n. A circuit that alternates between *two possible states* when a pulse is received at the input.”) with

Ex. 2028 [Horowitz] 720 (three-state logic is an “ordinary logic, *with a third output state*: open circuit”).

Ex. 2026 [Khatri-Decl.] ¶ 36. Petitioner, thus, entirely ignores its district court argument that the “logic” terms require a tri-state driver. The Petition’s arguments, therefore, fails to show any “logic associated with a first data connection” that satisfies Petitioner’s proposed construction before the district court.

As to claim 4, Petitioner similarly fails to identify any tristate driver in the recited “third stage logic” in the Petition. Petitioner does not dispute that Pixley does not depict a “third stage logic.” *See* Pet., 34–35. Rather, Petitioner argues that “Pixley does not limit to where the output of the tri-state MUX 112 is transmitted” and that “a POSITA would have found obvious that, in Pixley-Watanabe’s nested multiplexers of FIG. 9, the second stage logic [*e.g.*, the tri-state MUX 112] [was] configured to transmit the selected data word to a third stage logic [*e.g.*, in a larger nested multiplexer, the output of tri-state MUX 112 would be connected *to a subsequent stage multiplexer*].” *Id.* Petitioner, however, never identifies any tristate driver in this hypothetical third stage logic, as can be seen in its annotated figure:



Id., 35. Thus, Petitioner also fails to demonstrate that the alleged “third stage logic” in Pixley has the structure Petitioner insists is necessary in the District Court Action.

Consequently, Petitioner not only fails to disclose its means-plus-function constructions, but it also does not attempt to show that they are met by the Pixley/Watanabe combination.

2. Petitioner’s Indefiniteness Argument For “The First Selected Signal Set” Is Not Disclosed Or Reconciled.

In the District Court Action, Petitioner urges the court to find “the first selected signal set” to be indefinite. Petitioner contends before the district court:

Here, claim 8 recites that a “logic associated with a third data connection of the plurality of data connections configured to receive *the first selected signal set*...” Despite the use of the article “the” before “first selected signal set,” this term appears nowhere else in the claim. Thus, just as in the example with “the lever” from the MPEP, the use of the article the renders this claim unclear and indefinite.

Ex. 2007 [Opening-Claim-Construction-Brief] 29–30 (emphasis in original).

Petitioner’s district court position thus is that “the first selected signal set” is so unclear that it cannot be applied at all.

Here, by contrast, Petitioner tells the Board that “[n]o formal claim constructions are necessary” and never discloses any indefiniteness challenge. Pet., 8. Petitioner offers no explanation of how a term it contends is indefinite in district court can be applied here without construction, and does not separately show that Pixley/Watanabe satisfies “the first selected signal set” under any definite construction.

Under *Tesla*, it is not enough for Petitioner to respond that indefiniteness is not an IPR ground. The Director has already held that this “is not a sufficient explanation” for taking inconsistent positions, and that a petitioner must either justify the difference or show that, even assuming definiteness, a POSITA would still understand the asserted art to meet the limitation. *Tesla*, IPR2025-00340,

Paper 18 at 3–4. Petitioner does neither here. Thus, under *Revvo*, *Tesla*, and *Sun*, that omission alone weighs against institution.

B. Petitioner Fails To Demonstrate That Pixley/Watanabe Teach Multiplexing “Data Words” (All Claims).

Each of the claims concerns multiplexing “data word[s.]”⁴ Petitioner presents two theories as to how Pixley/Watanabe teach these limitations. First, Petitioner argues that because the ’448 patent allegedly “does not preclude a ‘data word’ from being one bit,” Pixley—which multiplexes one bit at a time—teaches these limitations alone. *See* Pet., 12–14. But Petitioner fails to demonstrate that a single bit is a “data word,” and thus, its Pixley theory fails. *See* Section II.B.1. Recognizing Pixley’s shortcoming, Petitioner also argues that “a POSITA would have at least found it obvious that Pixley’s multiplexer would operate with respect

⁴ *E.g.*, Ex. 1001 [’448] cls. 1 (“A circuit for multiplexing a plurality of data words”); 4 (“A multiplexor circuit, comprising ... a second stage logic configured to ... select a selected data word between the first data word and a second data word”); 5 (similar); 8 (similar); 9 (“A multiplexor circuit, comprising ... a connection adapted to receive ... the first data word” or “the second data word”); 14 (“A method for distributing multiplexing, comprising ... selecting for transmission between the first data word and the second data word”); 17 (similar).

to multi-bit data words” per Watanabe’s teachings. Pet., 13-15. But Petitioner fails to demonstrate that a POSITA would have been motivated to combine Pixley and Watanabe. *See* Section II.B.2.

1. Pixley Alone Does Not Teach Multiplexing “Data Word[s].”

Again, each of the claims require “data word[s].” A “data word,” however, is more than one bit. *See* Section II.B.1(a). Pixley only discloses multiplexing one bit, not a data word. *See* Section II.B.1(b).

a. *Petitioner Fails To Prove A Single Bit Can Be A “Data Word.”*

Again, each of the claims concerns multiplexing “data word[s].” Petitioner argues that the “’448 Patent does not preclude a ‘data word’ from being one bit”:

The ’448 Patent describes that “[e]ach data connection is preferably capable of transmitting an n-bit data word, where ‘n’ refers to the number of bits within the data word.” EX1001, 2:36-38. The ’448 Patent goes on to state that “[a] set of bits, e.g. 128 bits simultaneously transmitted from the same data connection, is hereinafter referred to as a ‘data word.’” EX1001, 2:41-43. ***The ’448 Patent does not preclude a “data word” from being one bit.*** EX1003, ¶59.

Pet., 13. As can be seen above, Petitioner offers no evidence demonstrating that a single bit would be a “data word.” It cites paragraph 59 of Dr. Wolfe’s declaration, but he only repeats the same conclusory statement that “[t]he ’448

Patent does not preclude a ‘data word’ from being one bit.” *See* Ex. 1003 [Wolfe-Decl.] ¶ 59. Notably, Dr. Wolfe dodges offering his own opinion that a “word” of data can be a single bit.

Merely because the ’448 patent allows the number of bits in a data word to vary does not convert a data word into something it is not—a single data bit. First, Petitioner presents no evidence that a POSITA would consider a single bit to be a “data word.” Dr. Wolfe likewise provides nothing, and avoids providing his own opinion, instead stating that the ’448 patent itself “does not preclude” this non-credible definition. That is not surprising—patents (nor any document) cannot be expected to “preclude” non-credible assertions.

And the assertion is entirely without credibility. Petitioner presents no evidence of any single-bit data words in the art. At best, Petitioner’s assertion is conclusory and does not satisfy its burden of proof. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)) (“[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.”); *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements. The

petitioner must instead articulate specific reasoning, based on evidence of record, to support the legal conclusion of obviousness.”).

Second, to the extent Dr. Wolfe’s “does not preclude” statement has any meaning, it is a paradigmatic unsupported *ipse dixit* statement. It is well-settled that an expert’s conclusory statements are insufficient to establish invalidity. *See* 37 C.F.R. § 42.65(a) (unsupported expert testimony entitled to “little or no weight”); *see also Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887 n.2 (Fed. Cir. 2024) (“the conclusory assertions in Dr. Mohazzab’s declaration do not provide substantial evidence for finding a motivation to combine.”).

Indeed, Dr. Wolfe’s *ipse dixit* assertion that “[t]he ’448 Patent does not preclude a ‘data word’ from being one bit” is precisely the sort of conclusory testimony rejected in *Xerox*:

Petitioner’s only evidence in support of its assertion that blocking the purchaser would require recording the blocking in a record in the user’s account is the opinion of its Declarant, Dr. Jones. ... Dr. Jones does not cite to any additional supporting evidence or provide any technical reasoning to support his statement. Thus, the cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is offered to support, and is entitled to little weight.

Xerox Corp. v. Bytemark, Inc., IPR2022-00624, Paper 9, 15 (Aug. 24, 2022)
(precedential).

Fourth, both the usage in the art and the '448 patent itself suggest that a single bit is not a data word in the context of the claims. As Dr. Khatri explains, multiple sources indicate that a single bit would not be considered a “data word”:

Although Petitioner and Dr. Wolfe seem to implicitly construe “data word” to include a single bit, they tellingly cite no evidence supporting that construction. Contrary to that position, numerous textbooks and dictionaries make clear that a single bit is not a “data word.” Indeed, even a byte (8 bits) may not qualify as a word. For example, *Principles of Computer Organization and Assembly Language* explains that words are larger than bytes:

For convenience, 8 bits are usually grouped into a single block, conventionally called a byte. ...

The next-largest named block of bits is a word. The definition and size of a word are not absolute, but vary from computer to computer. A word is the size of the most convenient block of data for the computer to deal with.

Ex. 2029 [Juola] 13–14, 39 (“values ... are stored as binary digits of bits. These are grouped ... into larger units such as bytes and words”); *see also* Ex. 2030 [TechTarget] (“the term word is often used to describe two or more consecutive bytes. A word is usually 16, 32 or 64 bits long.”); Ex. 2027 [Microsoft Computer Dictionary] 573 (“**word** *n.*

The native unit of storage on a particular machine. A word is the largest amount of data that can be handled by the microprocessor in one operation Word sizes of 16 bits and 32 bits are the most common. Compare byte, octet.”).

Ex. 2026 [Khatri-Decl.] ¶ 44.

This usage, wherein a “data word” is more than one bit, is reflected in the ’448 patent itself. As Dr. Khatri explains:

Throughout its disclosure, the ’448 patent discusses a data word as being a “set of bits,” not a single bit. For example, the ’448 patent refers to a data word as a “*set* of bits,” not a single bit. Ex. 1001 [’448] 2:41–43 (“A set of bits, e.g. **128 bits** simultaneously transmitted from the same data connection, is hereinafter referred to as a ‘data word.’”); *see also id.*, 2:38–41 (“The n-bit data word is transmitted via a connection that comprises at least n routing wires wherein **each different bit of the n-bit word is** transmitted via a different routing wire.”). Moreover, the ’448 patent repeatedly uses an exemplary 128-bit word when describing both the background and the inventions. *E.g.*, *id.*, 1:9–15 (“For example, a MUX circuit within an IC may comprise eight data connections that transmit **128-bit data words**. Typically, each of the **128-bit data words** may be routed to multiplexor logic on the IC via a connection that comprises 128 routing wires, e.g., a wire for each bit that is transmitted.”); 1:17–19 (“The multiplexor logic selects and outputs one of the **128 bit words** received by the multiplexor logic.”); 3:25–29 (“For example, if data connection 214a transmits **a data word that is 128 bits wide**, then the connection 240 is preferably

comprised of 128 routing wires through which each of the 128 bits of the data word 260 is transmitted.”). The ’448 patent simply gives no reason to believe that the claimed “data word” (a “set of bits”) would be satisfied by a single bit.

Ex. 2026 [Khatri-Decl.] ¶ 46.

In summary, Petitioner not only fails to substantiate its position that a single bit is a “data word,” the only evidence clearly refutes the position. Petitioner is forced into an absurd claim construction because Pixley entirely lacks disclosure of multiplexing data words.

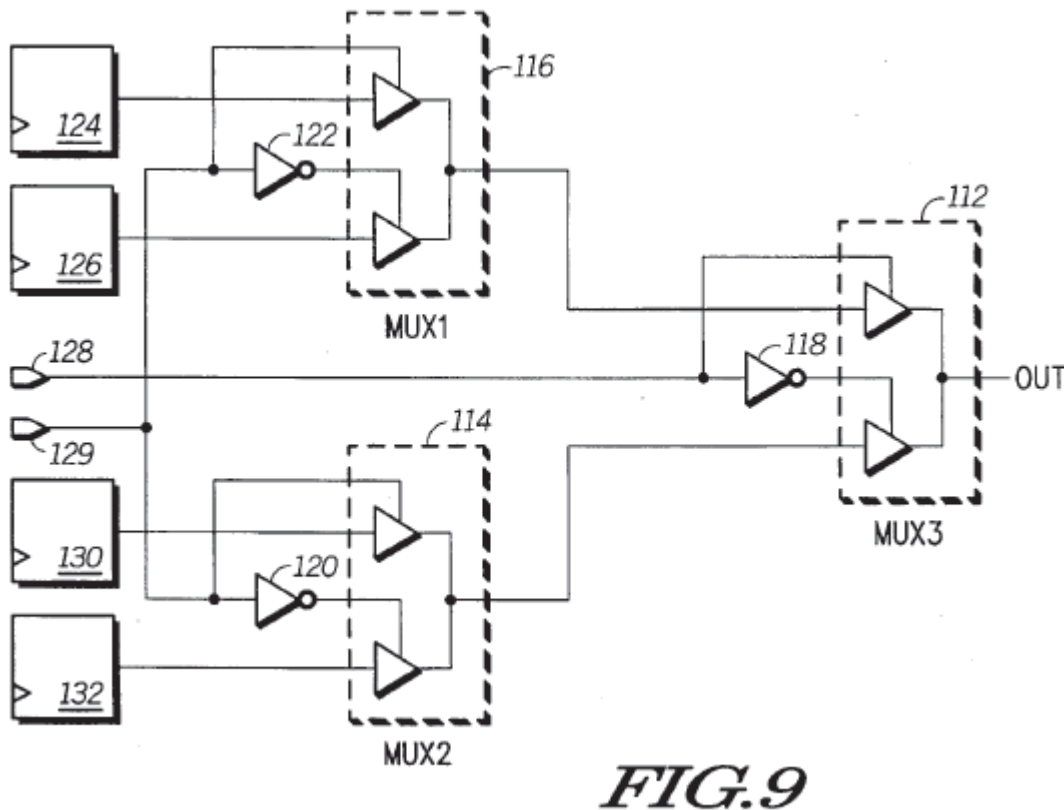
b. *Pixley Only Discloses Multiplexing One Bit At A Time.*

As just discussed, Petitioner has failed to demonstrate that multiplexing a single bit qualifies as multiplexing a “data word.” For this reason, Petitioner’s reliance upon Pixley—which only multiplexes a single bit—fails.

Indeed, Petitioner implicitly recognizes that Pixley only discloses multiplexing one bit at a time rather than a “data word.” That is the reason Petitioner argues that “a POSITA would have at least found it obvious that Pixley’s multiplexer would operate with respect to multi-bit data words,” relying upon Watanabe’s “known use case” of “the selection and transmission of an operand.” Pet., 13–14.

And as Petitioner implies, Pixley only multiplexes one bit at a time.

Petitioner's obviousness theory centers upon Pixley's Figure 9 (below) and its accompanying description:



E.g., Pet., 12–23 (citing Pixley's Figure 9 for every limitation of claim 1). Pixley's Figure 9, however, is only configured to multiplex a single bit at a time. As Dr. Khatri explains:

Pixley's Figure 9 exclusively describes and illustrates tri-state multiplexers processing single bit-wide inputs. As seen below, Figure 9, which includes MUXes 114, and 116, shows each multiplexer receiving only one single-bit data input from a corresponding **flip-flop**

(e.g., flip-flops 124/126 and 130/132, respectively), while MUX 112 receives single-bit data input from MUXes 116 and 114 respectively:

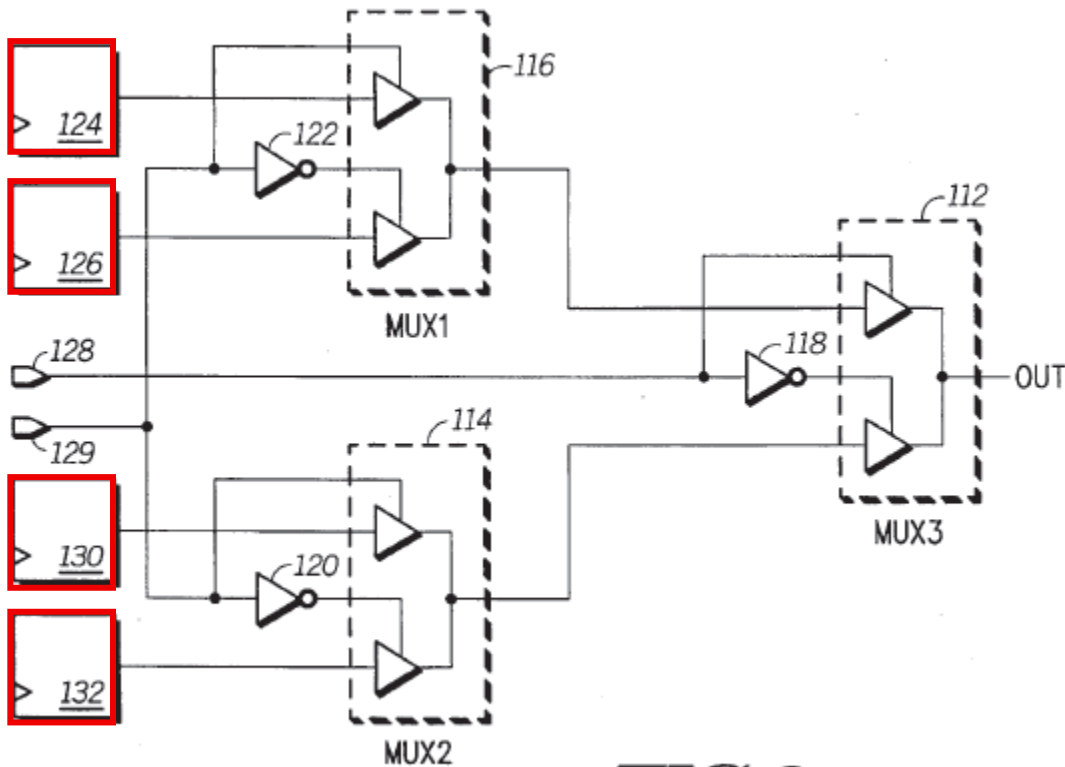


FIG. 9

Ex. 1004 [Pixley] Fig. 9 (annotated). Flip-flops are circuit elements that hold a single bit. Ex. 2029 [Juola] 246–247 (flip-flops “can be used as a 1-bit memory”). Each input and output line, moreover, are single wires and not labeled as buses, which are capable of carrying more than one bit at a time. Thus, Pixley’s Figure 9 only depicts multiplexing a single bit at a time.

Ex. 2026 [Khatri-Decl.] ¶ 51.

2. Petitioner Fails To Demonstrate That A POSITA Would Be Motivated To Combine Pixley And Watanabe.

Recognizing that the '448 patent does not in fact suggest that a single bit is a data word and that Pixley's Figure 9 only discloses multiplexing a single bit at time, Petitioner alternatively argues that "a POSITA would have at least found it obvious that Pixley's multiplexer would operate with respect to multi-bit data words," relying upon Watanabe's "known use case" of "the selection and transmission of an operand." Pet., 13–14. Even assuming, *arguendo*, that Watanabe is directed towards multiplexing "data words," Petitioner never explains why a POSITA would have been motivated to modify Pixley's Figure 9 in light of Watanabe with a reasonable likelihood of success.

Petitioner never grapples with what Pixley's Figure 9 is and how it relates to Pixley's actual invention, the checker. Pixley is directed to checking if tri-state multiplexers are properly operating. Pixley teaches that "if a tri-state MUX is incorrectly used, undesirable situations like erroneous/unpredictable functional behavior, excessive power consumption, and/or irreparable physical damage to the chip may arise." Ex. 1004 [Pixley] 1:14–18. Pixley further teaches that prior methods of avoiding these "undesirable situations" such as using a priority encoder or simulation come with their own drawbacks. *Id.*, 1:33–2:10. Consequently, Pixley teaches "a method and apparatus to perform checking of tri-state

multiplexers to ensure that the tri-state multiplexers are operating in a proper manner.” *Id.*, 2:60–63.

It is in this context that Pixley’s Figure 9 arises. Figure 9 is not an actual part of Pixley’s invention that Pixley (or anyone else) seeks to optimize. Figure 9 is merely an illustrative tristate MUX-based circuit intended to show how Pixley’s checker operates. Ex. 1004 [Pixley] 7:7–8 (“FIG. 9 ... illustrate[s] how nested multiplexers are processed”). As Dr. Khatri explains:

Pixley’s Figure 9 does not depict Pixley’s invention itself. Rather, Figure 9 is an illustration of an example “nested multiplexer” circuit and is presented to illustrate how Pixley’s “checker” method and apparatus work. Pixley teaches that its Figures 9 and 10 “illustrate how nested multiplexers are processed” according to Pixley’s “method and apparatus to perform checking of tri-state multiplexers to ensure that the tri-state multiplexers are operating in a proper manner.” Ex. 1004 [Pixley] 7:7–8, 2:60–63; *see also id.*, 2:36–42. Pixley teaches that Figure 9 “illustrates a circuit having tri-state MUXes 112, 114, and 116” and Figure 10 “illustrates the circuit of FIG. 9 *after MUXes 116 and 114 have been tested/verified* and achieved a passing state.” *Id.*, 7:8–16.

Thus, Pixley’s Figure 9 is simply an illustrative circuit which serves no other purpose or application to Pixley’s actual invention other than to illustrate along with Figure 10 how Pixley’s “checker” invention operates. A POSITA would understand that Pixley’s actual invention

is the checker logic and method, while Figure 9 is merely an example of a circuit that Pixley's checker invention may be illustratively applied to. Pixley does not convey or suggest any particular approach or improvement to Figure 9. Figure 9's circuit is thus **not** part of Pixley's invention and **not** something that Pixley seeks to optimize or improve upon.

Ex. 2026 [Khatri-Decl.] ¶¶ 54–55.

Petitioner's proposed modification (Pet., 13–15) does not change Pixley's checker at all. It instead modifies only the illustrative example in Figure 9. Petitioner asserts that “in m-bit processing applications in which m-bit data must, for example, be read from registers or memory, each of Pixley's tri-state multiplexors 112, 114, and 116 would have been configured as an m-bit multiplexer composed of m one-bit multiplexers, one for each bit of data—effectively stacking a set of the multiplexer circuits illustrated in FIG. 9,” and that “[a] POSITA would have been motivated to use m-bit multiplexors in m-bit processing applications as such applications demand the ability to process m-bit data words.” Pet., 13–15 (citing Ex. 1003 ¶¶ 61–62). As Dr. Khatri explained above, a POSITA would see no benefit to Pixley's actual invention—the checker—from such a change and no reason to recreate an illustrative design that Pixley uses solely as a teaching example to show how the actual invention (Pixley's checker) operates. Ex. 2026 [Khatri-Decl.] ¶¶ 54–55.

Not surprisingly, Petitioner does not identify any concrete “m-bit processing applications” in which the modified Figure 9 example is supposedly used or explain why that example would even be performing m-bit processing in the first place. In fact, Pixley’s illustrative circuit in Figure 9 is not used in any specific application, but is rather merely used to illustrate how “nested multiplexers are processed” in Pixley’s checker. Petitioner never says what processor, subsystem, or function Figure 9 belongs to, what problem in Pixley’s checker Watanabe’s “selection and transmission of an operand” is supposed to solve, or how adding Watanabe’s alleged m-bit multiplexing into this didactic example would improve anything Pixley cares about. *See* Pet., 14. In fact, the figure in Pixley’s Figure 9 is simply an exemplary circuit, and does not belong to any particular processor, subsystem of function, and therefore has no problem that needs to be solved. Fundamentally, as Dr. Khatri explains, Petitioner’s failure to grapple with the fact that Pixley’s Figure 9 is just an illustrative example meant to demonstrate how Pixley’s checker invention—which can generally apply to any circuit with tri-state multiplexers—works:

Again, the circuit illustrated in Pixley’s Figure 9 serves no purpose for Pixley’s invention other than to illustrate how Pixley’s checker invention works. In other words, Figure 9 simply represents a possible use case “nested multiplexer[]” circuit to illustrate how Pixley’s checker invention operates. Pixley does not remotely suggest

that its Figure 9 is meant to be used by any application—let alone some unspecified “m-bit processing application[]”—or is even part of a processor that would run these applications. *See* Ex. 1004 [Pixley] 7:7-8. Pixley’s invention is its checker which can be used on circuits with tri-state multiplexers. Consequently, there is nothing to improve upon or that needs modification in Pixley’s Figure 9. “Configur[ing]” Pixley’s Figure 9 to process m-bit words as Petitioner proposes (Pet., 13-15) does not affect, let alone improve, how it illustrates the operation of Pixley’s checker invention. There simply is no reason for a POSITA to modify Pixley’s Figure 9 or combine it with Watanabe as proposed.

Even if a POSITA were motivated for some reason to modify Pixley’s Figure 9, Petitioner additionally does not explain why he or she would care about Watanabe’s teaching of “selection ... of an operand,” how adding m-bit multiplexing into Pixley’s illustrative circuit would improve Pixley’s checker, or what “m-bit processing application” Pixley’s Figure 9 is supposedly performing. There is no articulated reason that would motivate a POSITA modify Pixley’s Figure 9 as proposed. *See* Pet., 13-15.

Ex. 2026 [Khatri-Decl.] ¶¶ 58–59.

At bottom, Petitioner’s argument amounts to arguing that a POSITA would have modified Pixley to process m-bit words because it was known. But the Federal Circuit has rejected such failures to provide a motivation to combine. *Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 886–87 (Fed. Cir. 2024) (“It does not suffice to meet the motivation to combine

requirement to recognize that two alternative arrangements ... were both known in the art.”); *RPX Corp. v. Parity Networks, LLC*, IPR2018-00097, Paper 7, 14 (Apr. 24, 2018) (“knowledge in the art does not . . . show a motivation to combine existing components in the manner claimed free of hindsight motivation.”).

Nor may Petitioner rely on the ’448 patent itself as a roadmap for this modification. Its proposal to “configur[e]” Pixley’s Figure 9 to process m-bit data words is driven not by any benefit to Pixley’s checker or anything else in Pixley, but by the claims’ recitation of distributed multiplexing of data words. That is classic hindsight. *Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 1275 (Fed. Cir. 2004). Petitioner’s invocation of “configur[ing]” Pixley’s Figure 9 to process m-bit words is hindsight-driven, merely following the ’448 patent’s inventive concept of distributed multiplexing of data words. But “[t]he inventor’s own path itself never leads to a conclusion of obviousness; that is hindsight.” *Univ. of Strathclyde v. Clear-Vu Lighting LLC*, 17 F.4th 155, 165 (Fed. Cir. 2021); *InTouch Techs., Inc. v. VGo Commc’ns., Inc.*, 751 F.3d 1327, 1351 (Fed. Cir. 2014) (rejecting obviousness theory that “relied on the [] patent itself as her roadmap for putting what she referred to as pieces of a ‘jigsaw puzzle’ together.”).

Because Petitioner identifies no problem in Pixley that Watanabe solves, no benefit to Pixley’s checker from the proposed changes, and no reason a POSITA would modify an illustrative circuit that Pixley uses only to demonstrate its

checker, Petitioner fails to articulate a legally sufficient motivation to combine Pixley and Watanabe.

III. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that institution be denied under 35 U.S.C. § 314(a).

Respectfully submitted,

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LOWENSTEIN & WEATHERWAX LLP

Date: December 9, 2025

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITS

This Patent Owner Preliminary Response (the “POPR”) consists of 6,271 words, excluding table of contents, table of authorities, certificate of service, this certificate, or table of exhibits. The POPR complies with the type-volume limitation of 14,000 words as mandated in 37 C.F.R. § 42.24. In preparing this certificate, counsel has relied on the word count of the word-processing system used to prepare the paper (Microsoft Word).

Respectfully submitted,

/ Abbie Neufeld /

Date: December 9, 2025

CERTIFICATE OF SERVICE

The undersigned hereby certifies that the following documents were served
by electronic service, by agreement between the parties, on the date below:

PATENT OWNER PRELIMINARY RESPONSE

EXHIBITS 2026-2030

The names and addresses of the parties being served are as follows:

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Respectfully submitted,

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