

David J.R. Cristaldi · Salvatore Pennisi · Francesco Pulvirenti
Liquid Crystal Display Drivers
Techniques and Circuits

Liquid Crystal Display Drivers deals with Liquid Crystal Displays from the electronic engineering point of view and is the first expressly focused on their driving circuits. After introducing the physical-chemical properties of the LC substances, their evolution and application to LCDs, the book converges to the examination and in-depth explanation of those reliable techniques, architectures, and design solutions amenable to efficiently design drivers for passive-matrix and active-matrix LCDs, both for small size and large size panels. Practical approaches regularly adopted for mass production but also emerging ones are discussed. The topics treated have in many cases general validity and found application also in alternative display technologies (OLEDs, Electrophoretic Displays, etc.).

Liquid Crystal Display Drivers is not only a reference for engineers and system integrators, but it is written also for scientific researchers, educators and students. It is a valuable resource for advanced undergraduate and graduate students attending display systems courses, and it may prove attractive even for a non-expert in the field, as it is reasonably simply written and reach of illustrations and many interesting details (the men and the ideas behind the things they produced were also put in evidence).

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David J.R. Cristaldi
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by

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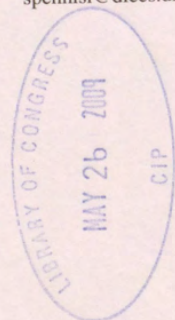
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Forewords

The origins of this book can be found in the scientific collaboration (officially started in March 2003) between Francesco Pulvirenti and me. Besides its obvious technical aim, this collaboration has produced eighteen theses for second-level laurea degree in electronic engineering and fifteen theses for first level laurea degree in electronic engineering. It has given many students the possibility to work within a skilled and experienced design team in a friendly environment, while measuring their strengths against advanced and exciting microelectronic issues. Many of these students are now appreciated designers working all over the world. One of these graduate students was David Joseph Roger Cristaldi, who has just completed his Ph.D. course program.

This book has been written also to leave the marks of this hard work, commitment, respect, and friendship.

Salvatore Pennisi

The activity on Display Drivers started in 1999 when the former CEO of STMicroelectronics, Pasquale Pistorio, and the General Manager of TECDIS (a company of passive displays based in Chatillon, Italy), Ettore Morezzi, decided to create a joint-venture, called DORA, with the purpose to design display drivers. At the beginning this activity was managed by Roberto Gariboldi, today site manager of DORA design center, now based in Aosta (Italy) and by Giuseppe Collé, today quality assurance manager in EM Microelectronics based in Marin (Switzerland).

Starting from January 2001, Pietro Menniti, General Manager of the Industrial and Power Supply Division, now called Industrial and Power Conversion Division, involved me in the design activity. At the beginning I had a team of about 15 people, shared between the DORA design center, originally based in Chatillon, and the STMicroelectronics Catania (Italy) site.

This new challenging adventure started with the contribution and thrust of all the main actors: Roberto, Giuseppe and Pietro. A huge support to my activity came also from Maria Rosa Borghi, Design Director of the Industrial and Power Supply Division, based in Castelletto (Italy) and Mario Paparo, Director of the TPA (Telecommunication, Peripheral and Automotive) R&D team based in Catania. Today Maria Rosa is still covering the same position, while Mario is managing the Automotive R&D team in Shenzen (China).

My traveling from Catania to Agrate (Italy) and Chatillon became more and more frequent, and I used to spend at least one week a month in Chatillon. During my staying in Chatillon I felt very comfortable there thanks to Giuseppe support and his frequent invitations to dinner with his family.

Chapter 4

Drivers for Passive-Matrix LCDs

This chapter is devoted to the description of reliable architectures and circuit solutions suitable to efficiently implement *drivers* for passive-matrix LCDs. Since passive-matrix LCDs have a limited number of rows and columns (the present maximum resolution for hand-held devices adopting passive-matrix LCDs is the Quarter-VGA having 320 rows×240 columns), the driver is commonly a single-chip¹ mixed-signal integrated circuit (**driver IC**). It includes as main functionalities: microprocessor interface, control logic, display memory, temperature compensation, voltage-level generation/regulation, and drive (row and column) outputs.

It is worth noting that research has continuously produced new materials suitable for display applications, even substantially different from LCs (see Appendix A for alternative flat panel technologies). These materials need driving circuits with somewhat different requirements than those treated here [L2001]. Nevertheless, the architecture discussed here is conceptually of broad application and many of the building blocks presented are of general significance.

In this chapter the typical driver IC architecture is introduced in section 4.1. A discussion of the constituting blocks is performed in Sections 4.2–4.6. The features required to the IC fabrication technology suitable for the application are described in Section 4.7. Finally, a survey on the chip assembling methods is given in Section 4.8.

4.1 Driver Architecture

It was described in Section 3.2 that single line or multiple line addressing approaches are possible in PMLCDs. CSTN LCDs often adopt the MLA technique which offers the best performance. For this reason, unless otherwise stated, we will consider this driving approach in this chapter.

¹Because of the greater number of rows and columns, large-area (active-matrix) LCDs cannot be driven by a single chip which would require an unfeasible number of pins. As we will see in Chapter 6, they adopt a different architecture made up of a controller board and several row and column driver ICs.

The generic block diagram of a passive-matrix LCD driver² is illustrated in Fig. 4.1. Other than the LCD panel, that is represented for reference as it does not belong to the driver, we have indicated as main blocks the **Host Interface**, **LUT (Look-up Table)/Dither**, **Display Data RAM**, **Color Processing**, **MLA and Grey Generation**, **Control Logic**, **Timing Controller**, **OTP (One Time Programmable) Memory**, **Oscillator**, **Temperature Sensor**, **Temperature Compensation**, **DC/DC Converter**, and finally **Column and Row Drivers**. It is worth mentioning that some block functions have distributed allocation when actually implemented, but are here described as concentrated for the sake of clarity. Also, the diagram does not include the power supply, but two external supplies are usually required: one for the host interface and the other for the DC/DC converter and analog blocks. The value of the former is related to the voltage levels adopted by the standardized signalling approach (usually, it is equal to 1.8 V), the latter depends on the silicon process utilized and is somewhat higher (e.g., 2.8 V). Today there is a certain tendency to adopt only a single supply, but this trend has not produced standardization yet.

Some of the blocks included in Fig. 4.1 perform functions already explained in the previous chapter and should be familiar to the reader, other blocks and their related functions will be explained in the following.

Data coming from a micro controller unit (MCU host) can represent either commands or video information. They are initially interfaced and prepared to be respectively interpreted (by the Control Logic section) or stored (into the RAM). Video data are also optimized through Color Processing techniques (e.g., Gamma Correction). On-chip oscillators and stabilized DC voltage generators are also necessary for synchronization and generation of accurate reference voltages. Proper biasing with high-voltage boosting circuits is also required to generate pixel voltage levels greater than the supply one. Column and row voltages are finally provided as outputs through the Column and Row Drivers.

The implementation of all these functions should be optimized to contain chip size and cost,³ as well as the required number of external components, such as capacitors used by the voltage multipliers (pumping capacitors) or needed to absorb large current spikes (bypass capacitors). Reduction of power consumption⁴ and crosstalk with enhanced protection to electrostatic damage (ESD) are also important issues. Lastly, easily programmable display features are often desirable from the end user. As a result, both the utilized silicon process with its minimum lithographic resolution (0.18–0.25 μm are common) and the adopted circuit design techniques play an important role in the driver economy considering that, owing to the great number of output channels, the aspect ratio of the die is usually high (e.g., 20 mm×1 mm). However, unlike one could be induced to think by the large number of output pads, an IC driver for small-area LCDs is not PAD limited for two main reasons:

²Another electrical section, the backlight inverter (a DC/AC converter) is present in an LCD, but it is implemented as a separate circuit.

³Given the strong competition in the flat-panel display market, the cost is perhaps the most crucial parameter. Thanks to the scaling-up and technological simplification the price of mobile devices has been steadily decreasing by approximately 30% a year.

⁴Power consumption of PMLCD drivers for mobile applications is usually around 2 mW.

(1) With the evolution of the market and technologies, the display manufacturers have reduced the assembly pitch to follow the lithographic scaling of silicon driver technologies.

(2) High-performance AMLCDs are potentially PAD-limited, but they may adopt LTPS technologies that allow the PAD number to be reduced thanks to the implementation of multiplexers directly on the glass. At this purpose, a single column line instead of three for the RGB subpixels is typically adopted; and some manufacturers have succeeded in implementing a 12-to-1 MUX.

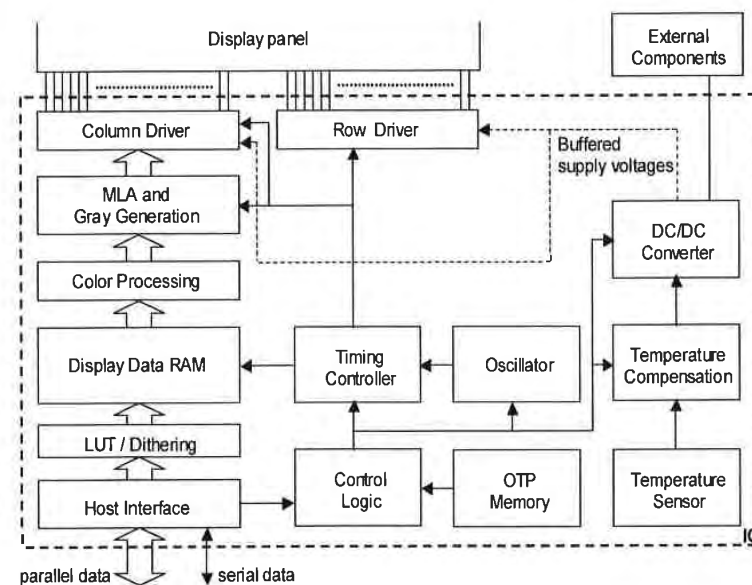


Fig. 4.1 Block diagram of a PM-LCD driver IC (within dashed box)

In the following sections we will explain in detail the behavior of a PMLCD driver by grouping its functions into 5 main categories, namely: (1) Host Interface, (2) Power Manager, (3) Driver Manager, (4) Image Processing and (5) Output Drivers.

4.2 Host Interface

4.2.1 Interfaces

Image data and commands are transferred from the MCU host to the driver, whereas diagnostic data and state information (e.g., driver ON/OFF condition) are transferred from the driver to the host. A bidirectional data link between the MCU and the driver is hence required. At this purpose, either parallel type or serial type communication interfaces have been exploited. In presence of multiple standards, to maximize flexibility and easy of use, a general driver IC is equipped with the most

popular industry standard host bus interfaces such as the (parallel type) **68 000** and **8080** and (serial type) **3 lines 9 bit** and **4 lines SPI** (Serial Peripheral Interface).

The two well-known parallel-type interfaces (introduced by Motorola and Intel, respectively) were the first exploited. A detailed description of these interfaces is beyond the scopes of this book. Here it is sufficient to say that they adopt CMOS standard signalling levels (that have progressively reduced from 3.3 V, 1.8 V, and in the next generation products to 1.2 V) and provide maximum speed rates up to 20 MHz for each channel.

Note that from the physical point of view, speed is ultimately limited by the RC time constant of the connection lines. However, the transfer rate between the host and the driver has significantly increased over the last years, to support the progressive migration of displayed data from text, to images, video, and full color compatibility. At this purpose, parallel-type interfaces were the first adopted for their higher transfer rates obtained by transmitting more bits in parallel. The main drawbacks of parallel connections are related to their cost and high exposure to mechanical breaks (of bus lines and connector contacts), which obviously may harm the whole system. The aforementioned problems are considerably reduced by adopting serial type interfaces, as they require a limited number of physical lines and are thus cheaper and more reliable.

We have mentioned two serial-type interfaces. These are briefly described below:

– 3 lines 9 bit from Nokia

the three lines are used for *enable*, *clock*, and *data*, the latter being in the 8-bit format plus 1 additional bit for datum/command discrimination.

– 4 lines Serial Peripheral Interface (SPI)

the function of the first three lines is the same as above, the fourth line is used for datum/command discrimination. Data are in the 8-bit format.

It should be observed that these are just two examples, since new interfaces are continuously developed. For example, Motorola adopts another interface type that uses 16 bit. The first 8 bit are used to code the command and the remaining 8 bit represent the data. It simplifies the subsequent elaboration task but can be less efficient for long data series transfer.

In conclusion, it is worth noting that these “low-speed” serial interfaces are typical of PMLCDs, owing to the limited data-transmission rate required. High-speed serial interfaces, required by AMLCDs, will be discussed in Section 6.2.

4.2.2 LUT/Dithering

Before being stored into the RAM, data at the output of the host interface may be remapped to fit the RAM word length. Two techniques may be needed: *insertion of additional bits* and *rounding*.

The former approach is required if the data length is smaller than the RAM word length. In this case, we need extending a reduced data color depth into the maximum one dictated by the RAM through a **Look-Up Table (LUT)** that is an associative array giving an output value for each of a range of index values. The LUT is also called *color map* or *palette*.

For example, consider a 18-bit RAM and 8-bit video data (as in the first case illustrated in Fig. 4.2). Assume that a number of 3 bit are used for Red and Green colors and 2 bit for Blue (3R 3G 2B). Data can be hence remapped to employ all 18 bit (6R 6G 6B). Other examples are included in Fig. 4.2.

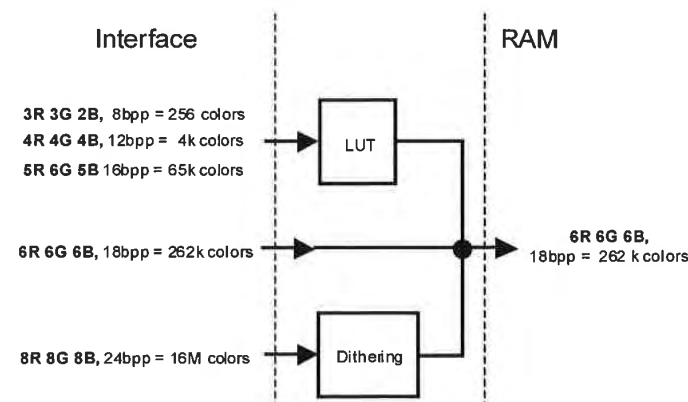


Fig. 4.2 Example of LUT/Dithering operation required in the case of a 18-bit video RAM

On the contrary, when the incoming data word length is greater than that allowed by the RAM we need to reduce the color depth, as illustrated in the last case of Fig. 4.2. At this purpose, the easiest solution is to truncate some bits. However, truncation may cause a significant error in the displayed image, like the generation of false contours. To limit this problem, several rounding (**dithering**) techniques have been developed such as conventional rounding, error feedback rounding, and dynamic rounding [J2001]. For example, error feedback rounding is performed by storing the residue of a truncation and adding it to the next addressed pixel. It substitutes less visible noise-like quantizing errors instead of contouring artefacts of simple truncation. An implementation scheme is shown in Fig. 4.3 where data word length is reduced from 16 to 8 bit. Note that the register included in the feedback path produces 16-bit output word in which the eight most significant bits are “0” and the remaining 8 bit are the 8 LSB of the previous output word.

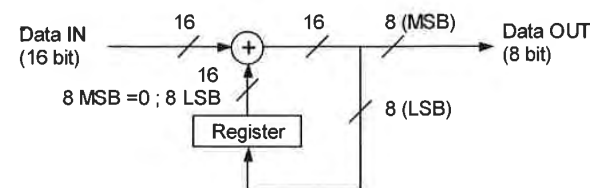


Fig. 4.3 Example of dithering algorithm using error feedback

4.3 Power Manager

The Power Manager section is devoted to the generation of all the bias and reference voltages (and currents) required by the driver circuits. Especially for hand-held devices, that can be subjected to dramatic temperature excursions during normal operation, it is essential that the reference voltages are temperature stabilized. The use of color graphics also worsens this problem since the color quality heavily depends on the absolute value of the LC threshold voltage and on the accuracy of the driving voltage level.

4.3.1 Temperature-Compensated Voltage Generator

All the internal reference voltages are generated from a reference bias circuit that is temperature compensated. A DC voltage, independent of temperature, is obtained through well-established circuits called *bandgap references*.⁵

A **bandgap** reference voltage has nominal zero temperature dependence as it is obtained by summing two voltages with proper weighting that have respectively negative and positive temperature coefficients. These voltages rely on the exponential voltage-to-current law of bipolar devices, for both positive (thermal voltage, V_T) and negative (base-emitter voltage, V_{BE}) temperature coefficients [W1971, K1973, B1974, BSU1999, MMF2001, GPC2003].

A bandgap reference circuit can be implemented in CMOS technologies by exploiting the inherent parasitic bipolar devices. Two examples of bandgap voltage generators are illustrated below.

The voltage reference in Fig. 4.4 is based on a differential amplifier. The bias currents, I_{C1} and I_{C2} , are set equal by imposing equal voltage drops across both the resistors R_3 and R_4 exploiting the virtual ground of the OpAmp.

Design equations are

$$I_{C1,2} = \frac{V_{BE1} - V_{BE2}}{R_2} = \frac{V_T}{R_2} \ln \left(\frac{A_{E2}}{A_{E1}} \right) \quad (4.1)$$

$$V_{REF} = V_{BE1} + 2R_1 I_{C1,2} = V_{BE1} + 2V_T \frac{R_1}{R_2} \ln \left(\frac{A_{E2}}{A_{E1}} \right) \quad (4.2)$$

This circuit requires that npn BJTs are available in the adopted CMOS technology.

⁵As known, this terminology is due to the fact that limit for $T \rightarrow 0$ K of the obtained reference voltage is the *bandgap* voltage of silicon.

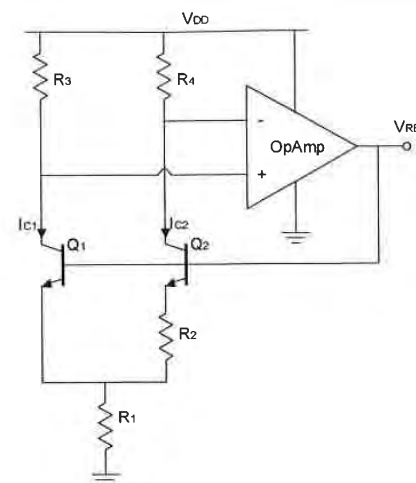


Fig. 4.4 Bandgap voltage reference with bipolar transistors

The circuit topology shown in Fig. 4.5 is fully compatible with a CMOS technology, because the npn transistors can be replaced by pnp or even simple pn junctions. Assuming the circuit properly biased, voltage V_{REF} is set to $V_{BE1} + (R_1 + R_3)I_{C1}$. Considering the virtual ground of the OpAmp, current I_{C1} can be found by inspection and results in

$$I_{C1} = \frac{V_T}{R_3} \ln \left(\frac{A_{E1}}{A_{E2}} \frac{I_{C2}}{I_{C1}} \right) \quad (4.3)$$

The virtual ground also forces the voltage drops across R_1 and R_2 to be equal, that is $I_{C1}/I_{C2} = R_2/R_1$. Substituting this expression in (4.3), V_{REF} results to be

$$V_{REF} = V_{BE1} + V_T \left(1 + \frac{R_1}{R_3} \right) \ln \left(\frac{A_{E1}}{A_{E2}} \frac{R_1}{R_2} \right) \quad (4.4)$$

Generally, transistors Q_1 and Q_2 are equal so that their emitter ratio is unitary and the output voltage mainly depends on resistive ratios.

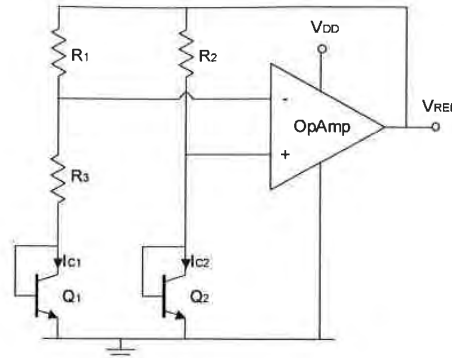


Fig. 4.5 Bandgap voltage reference circuit compatible with CMOS technologies

Figure 4.6 shows a typical behavior of the voltage versus temperature obtained by such circuits. They provide a temperature drift performance in the range of about 20–100 ppm/°C.

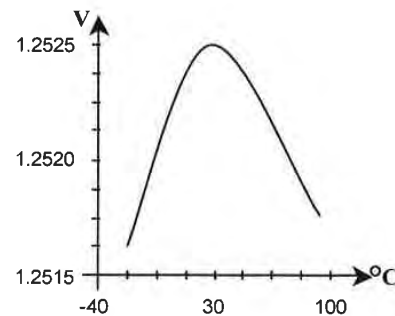


Fig. 4.6 Typical behavior of bandgap reference voltage versus temperature

4.3.2 Temperature Sensor

It was explained in Section 2.2.2 that the electro-optic (T/V) characteristic is dependent on the temperature. This problem is illustrated in Fig. 4.7a, where three curves are plotted for different temperatures $T_1 > T_A > T_2$, where T_A is the ambient temperature (be careful that letter T is used for both Transmittance and Temperature). From the figure it is seen that V_{TH} (and also V_{SAT}) decreases with the temperature, this is because the viscosity of the LC mixture decreases with the temperature and hence a reduced energy is required for the realignment. More specifically, the typical curve of V_{TH} versus temperature for STN LCDs is illustrated with solid curve in Fig. 4.7b.

As described in (3.18) and (3.19), V_{LCD} is proportional to V_{TH} , therefore in order to avoid that display contrast is affected by temperature variations, V_{LCD} must follow the same V_{TH} temperature behaviour. At the system level, V_{LCD} can be reconstructed by a piece-wise curve. This allows a simplification of the design and the minimization of data stored in the OTP. For example, the dashed curve in Fig. 4.7b represents one of the possible implementations of the curve into three segments having two intersections at temperatures T_L and T_H . T_L and T_H as well as the slopes of the three segments can be fine-tuned by the module maker according to the adopted LCD mixture and then stored in the OTP.

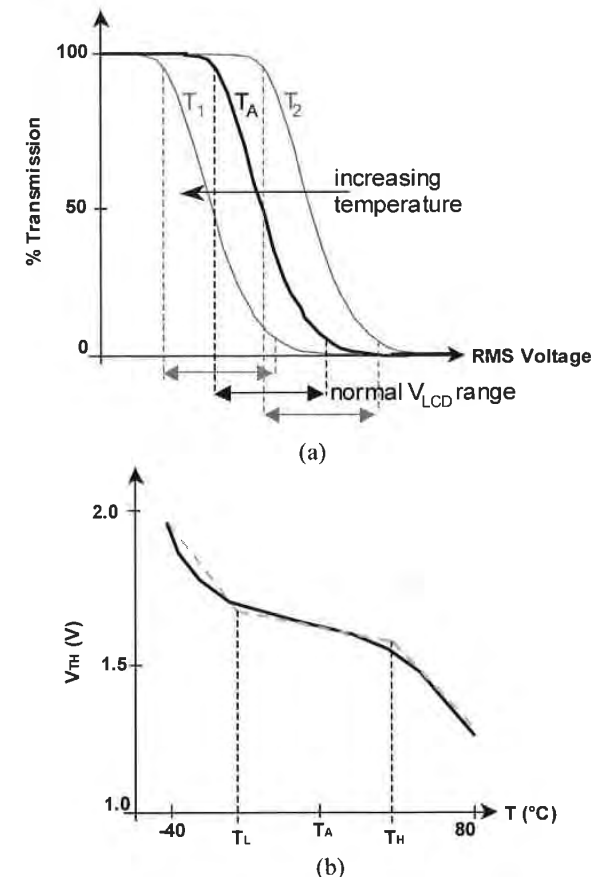


Fig. 4.7 (a) Electro-optic transfer function for three different temperatures, $T_1 > T_A > T_2$, highlighting the associated V_{LCD} ranges. (b) Threshold voltage versus temperature (solid line), and a possible segmentation (dashed line)

A temperature sensor is used to monitor the junction temperature of the driver, which is supposed to be very close to the display temperature. This information is

used not only in the block that generates the temperature segmentation of V_{LCD} , but also to change the frame frequency adapting it to the operating conditions of the LCD mixture. A possible block diagram of a temperature sensor is shown in Fig. 4.8.

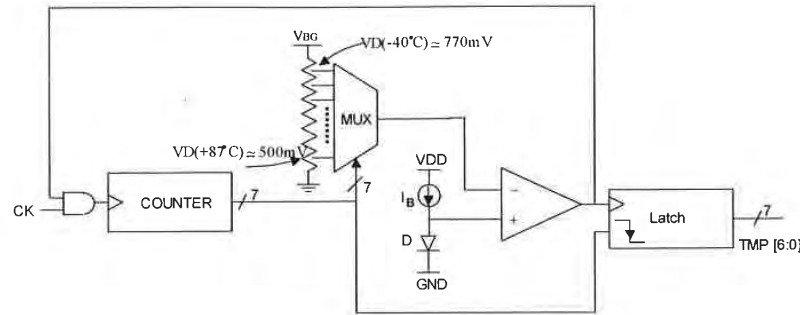


Fig. 4.8 Block scheme of the Temperature Sensor

CK is a synchronization signal coming from the Local Oscillator and feeding the 7-bit Counter. If the input feedback voltage at the AND gate is high, then the Counter output is increased by 1 bit at each clock pulse. The Counter output is then converted to an analog voltage through the resistor-string DAC and compared with the junction voltage of diode, D. The diode is forward biased through a constant current I_B and its useful voltage range is comprised between $V_D(-40^\circ\text{C}) = 770\text{ mV}$ and $V_D(+87^\circ\text{C}) = 500\text{ mV}$ with a slope of $-2\text{ mV}/^\circ\text{C}$. As far as the DAC output voltage is higher than the diode voltage, the counter will increase its output. The count up is stopped as soon as the output comparator switches down and the counter result is transferred to the Latch Register.

Observe that the DAC output corresponds to 770 mV for the lowest input word, 00HEX (i.e., the output voltage decreases for increasing input word).

A digital low pass filter can be inserted after the Latch Register to average the temperature value over a few (e.g., 4) acquisitions.

With a 7-bit variable TMP[6:0], the temperature ranging from the minimum value, -40°C , to the maximum 87°C can be detected with a resolution of 1°C .

Finally, the expression of the segmented V_{LCD} as a function of the temperature is given by

$$V_{LCD} = \begin{cases} V_{LCD,TA} + (T_L - T_A)S_{TA} + (T - T_L)S_{TL} & \text{for } T < T_L \\ V_{LCD,TA} + (T - T_A)S_{TA} & \text{for } T_L < T < T_H \\ V_{LCD,TA} + (T_H - T_A)S_{TA} + (T - T_H)S_{TH} & \text{for } T > T_H \end{cases} \quad (4.5)$$

in which $V_{LCD,TA}$ is the nominal V_{LCD} voltage at ambient temperature, whereas S_{TA} , S_{TL} , and S_{TH} are the slopes of the segments defined by the module maker and stored in the OTP. Figure 4.9 illustrates an example of the segmented V_{LCD} . In the figure

are also included V_{LCD,TA_MAX} and V_{LCD,TA_MIN} , that are the boundaries of the range in which V_{LCD} may vary as a function of the threshold voltage and the number of display rows. In general, for a color STN LCD with 128 rows the maximum V_{LCD} variation at ambient temperature is comprised between 5 V and 15 V.

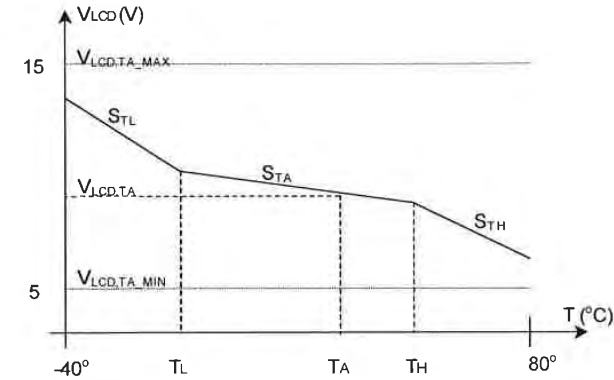


Fig. 4.9 Example of a segmented temperature programmable V_{LCD} voltage. The temperature range is split into three segments. Parameters $V_{LCD,TA}$, S_{TL} , S_{TA} and S_{TH} are the only stored into the OTP

4.3.3 DC/DC Converter

For battery-operated portable devices, the external supply is kept low to contain power consumption, therefore integer multiplication factors ($\times 2$, $\times 3$, $\times 4$ and even more) in both positive and negative amplitudes are required to generate the row and column voltages. A DC/DC converter that uses only switches (diodes originally) and capacitors is referred to as charge pump [D1976]. This inductorless architecture is amenable for integration and causes relatively low electromagnetic interferences (EMI). It is popular in low noise applications such as EEPROM, implantable pacemakers and, of course, small-size (up to around 8 in.) LCDs [GP1996, M1997, WW1998, YKC2003, SK2008].

The simplified scheme of a voltage multiplier ideally providing an output voltage, V_{out} , equal to $3V_{DD}$ is depicted in Fig. 4.10. The circuit includes three stages, each made up of a diode and a capacitor. C_{IN} models the input generator capacitance, while C_{P1} and C_{P2} are the **pumping capacitors** and C_B is the **bulk capacitor** with function of storage and filtering, acting as a voltage generator for the load. A square-wave oscillator provides two phases that drive one terminal of the pumping capacitors. After a certain transient, dictated by the charging time of the generator-diode-capacitor system and the frequency of the oscillator, C_{P1} is charged to $V_{DD} - V_D$, and C_{P2} to $2V_{DD} - 2V_D$ and C_{OUT} to $3V_{DD} - 3V_D$, in which V_D is the diode voltage drop. The typical behavior of V_{OUT} is depicted in Fig. 4.11. More details on charge pumps can be found in Chapter 7.

Fully integrated multipliers (i.e., without requiring external components) are of course preferred. But this depends on the current drive capability required. Indeed, to obtain large output currents we need large out-of-chip capacitors to avoid fast discharging.

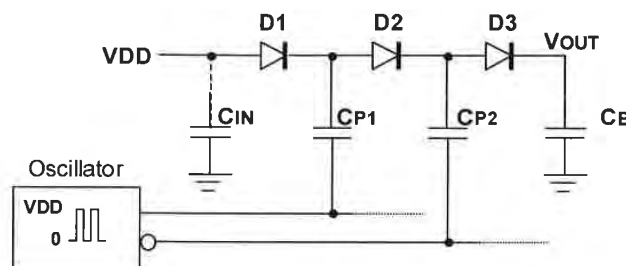


Fig. 4.10 Simplified scheme of a $\times 3$ charge pump

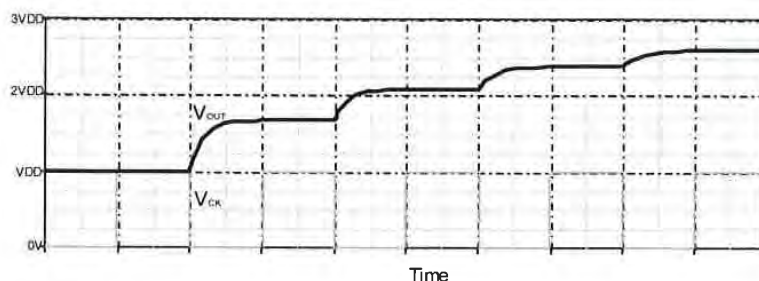


Fig. 4.11 Typical behavior of charge pump output voltage, V_{OUT} , and square wave, V_{CK}

Observe that owing to the high-valued bulk capacitor, a buffer amplifier is not needed to drive the row/column loads. This is instead required for voltages that are obtained by resistive partition. At this purpose, see Fig. 4.12 that illustrates a possible way to generate the voltages for a MLA-4 LCD.

The scheme generates the six required supply voltages $\pm V_R$, $\pm V_C$, and $\pm V_C/2$ (V_{COM} is the common voltage externally connected to ground). Four of them, $\pm V_R$ and $\pm V_C$, are obtained from charge pumps configured in closed loop, CP1, CP2, CP3, CP4, respectively. Each loop being constituted by an error amplifier, a voltage-controlled oscillator (VCO), and a charge pump. The loop works as follows. Consider for instance the loop generating V_R , and assume that it tends to decrease because of the load current demand. Then, also V'_R decreases, the output voltage of the error amplifier EA1 increases as well as the VCO1 frequency and, as a result, CP1 pumps more charges to its bulk capacitor, increasing (regulating) V_R .

The other two voltages, $\pm V_C/2$, are obtained from simple resistive partitioning (resistors R_1 – R_2) followed by a Linear Drop-Out Regulator (LDO) buffer. Buffer B1 is supplied between $+V_C$ and V_{COM} , whereas buffer B2 is supplied between V_{COM} and

$-V_C$. Two de-multiplexers and resistive dividers are also embedded into the above mentioned feedback loops. Their role is to set proper row, $+V_R$, and Bias Ratio, defined in (3.10), through coded words $V_{LCD}[\dots]$ and $BR[\dots]$. The last resistor divider (R_5 – R_5) is used to generate $-V_R$ from $+V_R$.

It is important to observe, in conclusion, that this architecture adopts a *centralized* driving voltages buffering, as opposite to the *distributed* buffering approach that is usually followed in AMLCDs (see Section 6.3.1).

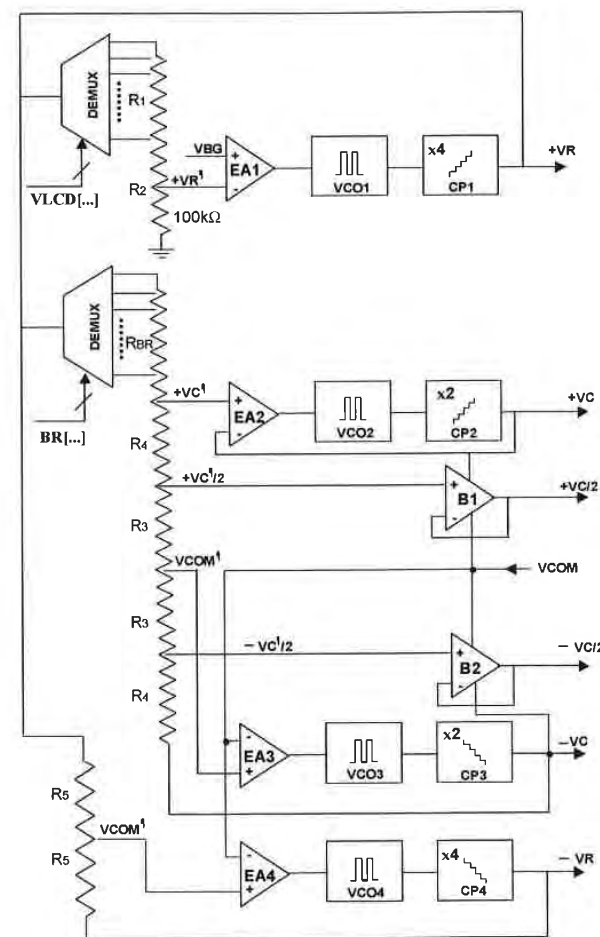


Fig. 4.12 Power Supply for LCD driver using MLA-4 technique

4.4 Driver Manager

4.4.1 One Time Programmable Memory

We have seen that the effectiveness of the LCD matrix in color reproduction depends mainly on the absolute values of parameters such as the LC threshold voltage and on the accuracy of the driving voltage levels. Any tolerance of these values must be hence compensated for. This task is performed by recording permanently in a dedicated non-volatile memory block the value of critical parameters, such as characteristics of the LC mixture, gamma curve data (see Section 4.5.2), the values of the reference voltages, etc., as well as configuration parameters. At this purpose, it is used a Memory called OTP (One Time Programmable) memory which can be implemented in a poly-fuse or anti-fuse technology.

The values of the aforementioned parameters are first measured by the module makers, for each production lot of LC mixture, as these may change from one lot to another one, and then written in the OTP. For instance an OTP word can be 22 bit long: 16 are used to code effective data and 6 are used to implement an Error Correction Code (ECC).

After each system reset or power on, the OTP is automatically initialized. Parameters stored in the non-volatile memory are read and latched in a volatile register situated in the Control Logic section (discussed in Section 4.4.3) and then the OTP is switched off to avoid current consumption. In the end-user application there is the possibility to upgrade the parameters stored in the OTP. This depends on the status of a "Protection Mode" bit present in the OTP. If it is low, said parameters can be upgraded, if it is high, the parameters cannot be upgraded.

4.4.2 Oscillator (Internal Clock Generator)

An internal oscillator, preferably fully integrated (without requiring external components) is included in the driver IC. It generates the master clock signal (at the maximum frequency), from which all the other synchronization signals are derived by frequency division.

A possible scheme of a relaxation oscillator is shown in Fig. 4.13 [P2002]. It is made up of two capacitors C_1 and C_2 alternatively fed by two constant current sources, I_{OSC} , or discharged by MOS transistors, M_1 and M_2 , acting as switches. Assuming one of the switches (e.g., M_1) be OFF, then the voltage across the associated capacitor increases linearly with the law $(I_{OSC}/C_1)t$ and when it reaches the threshold, V_{TH} , of M_{1A} the drain voltage of M_{1A} goes to "0" as well as the outputs of NOT_3 and NOT_5 (output). Hence, M_1 is switched ON and C_1 is discharged, while M_2 is switched OFF and capacitor C_2 starts to charge with the same law as C_1 . Assuming a duty cycle of 50%, $C_1=C_2=C$, and the oscillation frequency is given by

$$f_{OSC} = \frac{I_{OSC}}{2CV_{TH}} \quad (4.6)$$

and is electrically controlled by I_{OSC} . For instance, assuming $V_{TH}=0.8$ V, a 5-MHz oscillation frequency is obtained with $I_{OSC}=8$ μ A and $C=1$ pF.

Observe that M_{1A} and M_{2A} perform logically as NOT gates, but they are in common source configuration in order to provide a threshold voltage independent of V_{DD} and to limit the cross-conduction current to I_B .

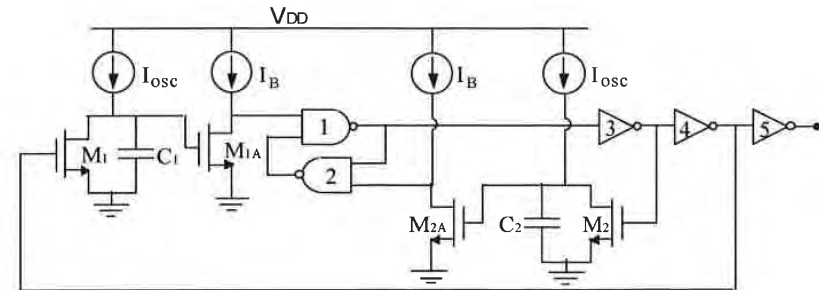


Fig. 4.13 Schematic of a relaxation oscillator [P2002]

Current I_{OSC} must be accurately set starting from the bandgap voltage, V_{BG} , an adjustable resistor and current mirrors, as illustrated in Fig. 4.14. Voltage V_{REF} is derived from V_{BG} by resistive partition and replicated across R_{ADJ} , where I_{REF} is generated ($I_{REF}=V_{REF}/R_{ADJ}$). R_{ADJ} is a resistor tuned during testing procedure to compensate for process variations in mass production.

The multiplexer, MUX, is usually implemented through a binary-tree selector (a three-bit version is depicted in Fig. 4.15).

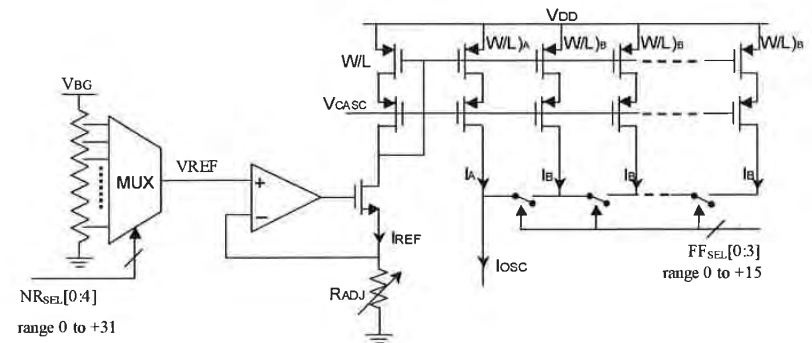


Fig. 4.14 Scheme for the generation of I_{OSC}

Referring to Fig. 4.14, if $I_A=k_1I_{REF}$ and $I_B=k_2I_{REF}$ we write the expression of I_{OSC}

$$I_{OSC} = I_A + FF_{SEL} \cdot I_B = I_{REF} (k_1 + k_2 \cdot FF_{SEL}) \quad (4.7)$$

$$= \frac{NR_{SEL}}{N} \frac{V_{BG}}{R_{ADJ}} (k_1 + k_2 \cdot FF_{SEL})$$

where N is the number of display rows, NR_{SEL} is a 5-bit control word that represents the subset of addressable rows (the user may operate only a portion of the display rows, this mode is usually referred to as *partial display mode*). FF_{SEL} is a 4-bit control word that represents the preferred frame frequency (required for instance to set the idle mode, or to allow frequency change with the temperature and LC mixture). Both are stored in the OTP and tuned by the module maker.

In conclusion, the above equation shows that the oscillation frequency can be set according to the addressable rows and frame frequency selected.

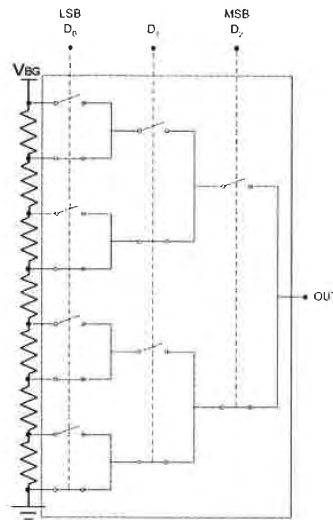


Fig. 4.15 String resistor DAC with three-bit multiplexer (MUX) scheme

4.4.3 Control Logic

The principal task of the Control Logic section is to decode the incoming command (Instruction Decoder) and to take the appropriate actions. It supervises the initialization phase of Timing Controller, Oscillator, DC/DC Converter and Temperature Compensation blocks. It also contains a (volatile) register where OTP parameters are latched at power on.

Advanced tasks offered by this section may include 2D graphic acceleration features to reduce the required processing power from the MCU and leaving it free

for other features. For instance, graphic functions are implemented that facilitate the user with simple instructions to draw lines, rectangles, copy or move objects and even define pop-up windows, while speeding up the application system.

4.5 Image Processing

The incoming pixel dataflow is stored into the RAM and subsequently goes through a data elaboration pipeline that performs color processing.

4.5.1 Display Data RAM

The column data of each frame, before being displayed, are stored into a static random access memory, Video SRAM, that is included into the driver. In practice, each pixel of the display is mapped into the RAM. To display color images, each RAM location must be a C -word, where C is the number of color bits. For instance, a 262k-color display requires 18 bit to code the column data. For a 132×162 display the required RAM dimension is $N \cdot M \cdot C$ bit = $132 \cdot 162 \cdot 18 = 384,912$ bit.

The RAM is essential for power saving when displaying the same image for a long time (like in PMLCD applications). In this case the image data are stored into the RAM and are no longer transmitted by the host processor.

Usually, when data are written in the RAM several displaying modes are possible such as for instance: *normal horizontal*, *normal vertical*, *horizontally mirrored* and *vertically mirrored*.

It is worth noting that CMOS processes with progressively reduced channel lengths are needed to implement single-chip drivers able to manage 4k, 65k, 262k color data, due to the RAM requirements in terms of area occupation. However, finer processes tolerate reduced voltages and hence a trade-off between required performance and suitable technology may arise, which is solved by the development of specific processes, as discussed in Section 4.7.

4.5.2 Color Processing

Color processing includes gamma expansion, correction of nonlinear electro-optical transfer function and, in principle, color space conversion with black/white points adjustment, all performed in the digital domain.

(a) **Gamma correction** ensures accurate reproduction of color and image detail over a wide range of luminance. To fully understand the subject, we must refer first to the CRT performance, because gamma correction was originally applied to this class of displays. As illustrated in Fig. 4.16a, curve 1, a CRT does not respond to an input voltage linearly, its luminance is approximately proportional to the input voltage raised to the 2.5 power. This number is known as **gamma** (γ) [P1993]. In general any kind of display has a nonlinear T/V characteristic, so that the normalized luminance, L , is proportional to some power of the normalized signal amplitude, x , according to $L = x^\gamma$ where $L, x \in [0 \dots 1]$ and $\gamma > 1$.

As a result, in a CRT, linear RGB data must be predistorted (gamma corrected) before being displayed to compensate for the nonlinearity of electro-optic transfer.

This correction effectively accomplishes a compression of the video signal through the inverse electro-optic transferfunction of the display, $x^{1/\gamma}$ (see curve 2 in Fig. 4.16a), so that the whole system (gamma-correction plus CRT display) response approaches the ideal straight line (see curve 3 in Fig. 4.16a). The input voltage is hence raised to the 0.4 power (i.e., $1/2.5$). In reality, since also the human visual system (eyes to brain transferfunction) is nonlinear, such exponent is changed into 0.45 and video standards assume accordingly a display gamma of about 2.2 for CRT displays.⁶

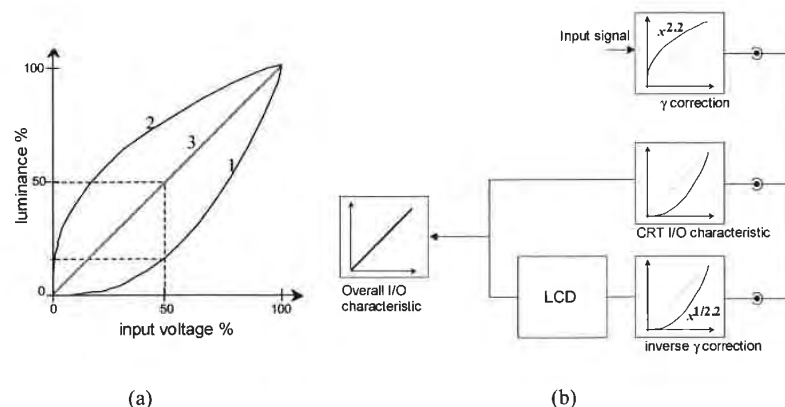


Fig. 4.16 (a) CRT luminance versus input voltage: (1) actual curve, x^γ , (2) gamma correction curve, $x^{1/\gamma}$ and (3) ideal (linear) response, x . (b) TV broadcasting system. LCD is assumed linear but requires its own γ correction

In the early period of CRT TVs, it was decided to apply the correction directly at the video cameras; a less expensive solution than having to provide gamma correction to every TV set, see Fig. 4.16b.

This means that nowadays, if we want to display TV-coded (and also MPEG-coded) video on an LCD, we must take the gamma correction into account and introduce a transfer function that raises the associated data voltages to the power of 2.2 (x^γ , gamma expansion, or inverse gamma correction). This scenario is further complicated by the fact that there are several standards defining different gamma compression functions with slightly different γ values, such as ITU Rec. 709 (TV), CIE L*, sRGB (WEB), etc. [IEC1998, IEC1999].

Of course, gamma expansion must be matched with the standard used to encode incoming images or video.⁷ As a consequence, an LCD driver IC cannot operate with a fixed gamma value.

Besides, an adjustable γ is needed for other two main reasons detailed below.

⁶Besides, human eyes are more sensitive to luminance changes in dark areas than to similar-sized changes in bright areas. Therefore, the compression should be reduced in low gray levels because that becomes much significant in dark areas. The solution is to use $\gamma = 1.8$ for $0 \leq x \leq 0.35$ and $\gamma = 2.2$ for $0.35 < x \leq 1$.

⁷In addition, most commercial digital cameras dynamically vary the amount of gamma.

First, a specific gamma correction for the electro-optic nonlinearity of the LCD itself must be devised. This nonlinear behavior depends on variations in manufacturing and process parameters from a production line (LC mixture, polarizers, backlight, etc.). Thus, different panels have different T/V curves and require different gamma values (otherwise, different panels next to each other will have slightly different color response). It should be observed at this purpose that the T/V curves are not exact analytical functions but they are expressed as approximated interpolation of experimental data.

Second, factors such as ambient illumination can play an important role in our perception of gray scale and color. Without the ability to adjust gamma, the reproduced image will suffer from lack of detail in shadow areas (black crush) or oversaturated whites.

Considering a normally white LCD and its T/V nonlinearity, we represent in Fig. 4.17 the gamma correction curve required to display equally distributed gray levels, GL , by applying non-equally distributed voltage levels V_{GL} . A curve for positive and negative values is needed by polarity inversion driving techniques.

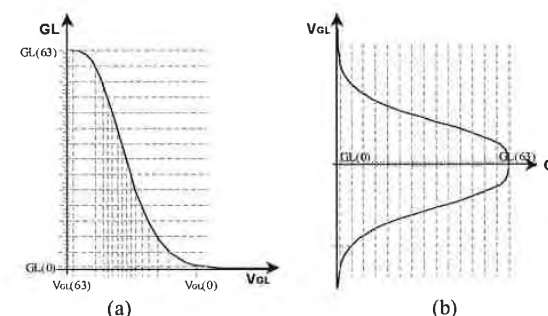


Fig. 4.17 LCD Gamma Correction curve: (a) nonlinear characteristic, (b) for positive and negative voltages

(b) **Color space conversion** (see also the Appendix D) can be used to translate RGB components from color space used to code still picture or video data, such as PAL, Rec. 709 (TV) or sRGB (WEB), etc., to color space that have as tristimulus base those that are *physically* reproduced by the particular display device. Indeed, if the RGB primaries of the display device have different chromaticities with respect to either interchange or transmission primaries, then an accurate color reproduction cannot be achieved. A 3×3 matrix is used to transform the color space from the interchange primaries to the display device primaries. This 3×3 matrix takes place in linear-light (tristimulus) space, after gamma expansion. The 3×3 matrix is unambiguously defined by primaries and white reference chromaticities of both interchange and display device color spaces. Hence, by suitably changing the matrix it is possible to change the white reference maintaining the same color primaries. Black and white points are the optical outputs of the display device when RGB

inputs are respectively $[0, 0, 0]$ and $[255, 255, 255]$ (considering 24-bit RGB, that uses 8 bit per color component). But the color characteristics of these points depend on characteristics of display components such as backlight, liquid crystal cell, color filters, etc. It is then possible to adjust these two points by adjusting electrical minimum and maximum values for each RGB component.

Actually, in passive displays, in which color quality is not the main concern, this task is heavily simplified and $T_{1 \rightarrow 2}$ is a straightforward diagonal matrix.

From the above considerations it emerges that the **pixel elaboration flow** has to be adaptable to different ambient conditions, to different encoding standards and to a wide range of display devices, and this has to be done by using a limited storage medium such as the OTP Memory previously described.

Figure 4.18 shows the three elaboration steps performed by a typical Driver IC. The incoming pixel data flow (R' , G' , B') is described in perceptual domain. The first operation is gamma expansion; typical values of γ are 1.0, 1.8, 2.2 and 2.5. It is possible to store in the OTP memory a custom γ value. After gamma expansion, the pixel data flow (R_1 , G_1 , B_1) is described in physical (intensity) domain. Now it is possible to transform color tristimulus from source space (R_1 , G_1 , B_1) to destination space (R_2 , G_2 , B_2) by using the 3×3 conversion matrix $T_{1 \rightarrow 2}$. In this step it is possible to adjust black point voltages by adding constants (c_R , c_G , c_B) to color components. White point voltages can be adjusted by proper choosing $T_{1 \rightarrow 2}$ matrix. The last step is to correct the nonlinearity of the electro-optical transfer function (EOTF) of LCD. To do this a Look Up Table (**Gamma LUT**) is used. In this LUT the inverse LCD T-V function is stored. It is possible to use different inverse T-V functions for each color component ($EOTF_R^{-1}$, $EOTF_G^{-1}$, $EOTF_B^{-1}$). The outputs are the voltages of elaborated pixel data flow (V_R , V_G , V_B), that is the RMS value driving the columns of the LCD allowing the desired pixel luminance (L_R , L_G , L_B).

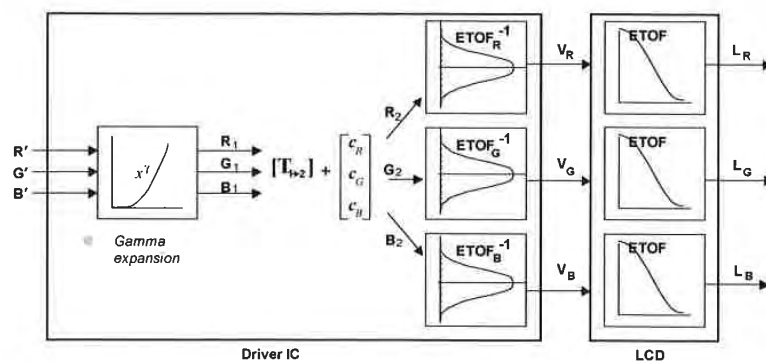


Fig. 4.18 Pixel elaboration steps

4.5.3 MLA and Gray Generation

Purpose of this block is to implement a **Column Logic** in order to latch Video RAM output, generate PWM/FRC control signals, calculate MLA waveforms and provide them to analog column drivers. Since these functions are tightly connected to the column (and row) drivers, their implementation issues will be discussed in Section 4.6.

4.5.4 Timing Controller (TCON)

This block generates the clock signals for (1) RAM access, (2) MLA and PWM/FRC elaboration and (3) n-line inversion. It synchronizes the column and row operations by selecting the proper rows with associated RAM data. These synchronization signals are all derived by division from the on-chip oscillator signal (described in Section 4.4.2). In the case of MLA, the orthogonal functions could be in principle memorized into a dedicated ROM. However, due to the small number of matrix elements usually needed (up to MLA-4 approach, at least), they are managed within the Timing Controller.

4.6 Output Drivers

The output drivers have the role to interface the driver IC with the LCD rows and the columns. These lines offer relatively large capacitive loads and should hence be driven with a sufficient current drive capability. This task is obtained by the analog buffers, directly connected at the output of the voltage generation section (DC/DC converters). Therefore, the architecture of the output drivers simplifies considerably and, ultimately, reduces to a multiplexer.

4.6.1 Row Drivers

It was described in Section 3.2 that both *single line* and *multiple line addressing* approaches are possible in PMLCDs.

In the former case, considering first the A&P approach, the row drivers are simple multiplexers designed to select one out of three voltages. As already illustrated in Fig. 3.9, the row voltage of a selected row can be $+V_R$ (or $-V_R$, for frames with reversed polarity), while unselected rows are addressed by a mid voltage (0 V).

The row driver for the IA&P technique must select one out of four voltages, i.e., $V_R + V_C$ for the selected row and V_C for unselected rows in positive-polarity frames (and respectively 0 and V_R in negative-polarity frames). Note that the above voltages are those depicted in Fig. 3.10, but shifted of $+V_C$ to exploit positive values only.

A possible row driver architecture for IA&P is depicted in Fig. 4.19. The N -stage shift register (see Section 6.4 for shift register architectures) selects one row at a time through the bank of (row select) switches S_{RS} . For illustration, row 1 is the selected one. The voltages with the proper frame polarity are obtained through switches S_{FP} .

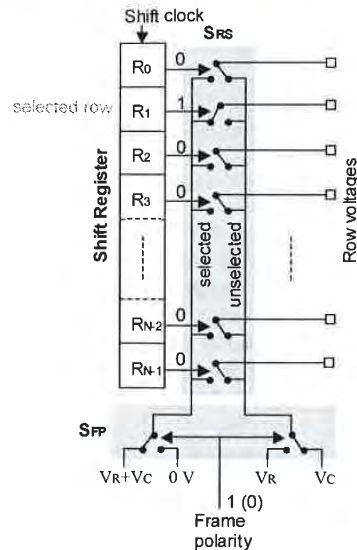


Fig. 4.19 Row driver block diagram for Improved Alt and Pleshko approach

Consider now the case of MLA- p addressing. We have seen in Section 3.2.2 that in this approach p lines at a time are addressed and the row signals are derived from orthogonal matrices, whose elements have just two values. Hardware complexity of the row (and column) driver depends on the number of voltage levels in the addressing waveforms, therefore those matrices minimizing the number of voltage levels in the scanning waveforms are preferred.

Also in this case, the row drivers are multiplexers that are designed to select one out of the three voltages i.e., $+V_R$ or $-V_R$, corresponding to elements $+1$ or -1 of matrix column (select pattern), and a mid voltage (0) corresponding to the unselected rows. The block diagram is very simple and can be deduced from that of a column driver for MLA described in the next section.

4.6.2 Column Drivers

Again, let us first consider single line addressing. In the A&P approach, the **column drivers** are multiplexers designed to select one of the two voltages i.e., $+V_C$ or $-V_C$, for ON and OFF pixels, respectively (the voltages are the same but with reversed meaning, for frames with reversed polarity). The column drivers used in the IA&P approach must instead select one out of four voltages, i.e., 0 or $2V_C$ for ON and OFF pixels, in positive frames, and V_R or V_R-2V_C for ON and OFF pixels, in negative frames (see Fig. 3.10 after shifting all waveforms by $+V_C$).

Consider now the case of MLA- p . The column signal is given by the *dot product* between the row select pattern and the data pattern in the selected subgroup of rows (as explained in Section 3.2). Assume that p is the number of grouped lines and that $p+1$ is the number of voltage levels in the column waveforms. The number of data

bits x must be consequently not lower than $\log_2(p+1)$. If M are the columns, there are hence M stages of shift register and latch and every stage has x bit each. After serially shifting the data corresponding to all column lines, the content of the shift registers are transferred in parallel to the latches and can be applied simultaneously to the column electrodes even though the dot products are computed sequentially. The schematic diagram of a column driver following this strategy is illustrated in Fig. 4.20 [RS2005].

This solution has the advantage of small area occupation, but requires high power consumption because the shift registers must work at the highest frequency (which hence coincides with f_{OSC} of the local oscillator) given by $f_f \cdot N \cdot M \cdot p = f_{OSC}$. For instance, if $f_f = 60$ Hz, $N=160$, $M=128$ and $p=4$, we get that the required local oscillator frequency is approximately $f_{OSC} = 5$ MHz.

An alternative low-power column driver scheme is depicted in Fig. 4.21.

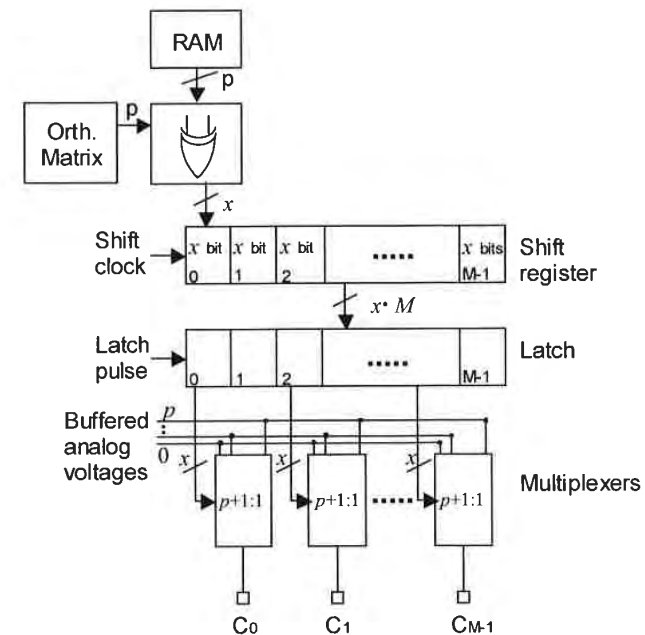


Fig. 4.20 Block diagram of a column driver used for MLA. (The operation performed by the XOR block is detailed in Fig. 4.21)

The column data patterns for each MLA row sub-group are stored into the Frame Buffer Memory and the XOR gates followed by the summer function perform the required product with the proper column of the orthogonal matrix. For instance, in Fig. 4.21 a MLA-4 approach is considered. The associated matrix is the 4×4 unity matrix shown at the left and the product with the first matrix column is performed. It is important to observe that to allow binary-logic computation, each -1 matrix entry is replaced by 0. In the figure it is also assumed that the data pattern for the

considered row subgroup is 1011 (meaning that in the considered row subgroup the first, third and fourth pixels are ON while the second pixel is OFF). The result of the XOR and subsequent summing computation is associated (through multiplexers) with the analog voltage that will be applied to the column. More precisely, the values 000, 001, 010, 011 and 100 are respectively associated with $-V_C$, $-V_C/2$, 0, $+V_C/2$ and $+V_C$. In the case exemplified the computation gives 010 that means 0 V. Compared to the previous solution, this one requires a lower clock frequency expressed by $f_F \cdot N \cdot p$, i.e., M times lower. Indeed, with the same data of the previous example this one works with a frequency equal to 38.4 kHz. The lower consumption allows high-resolution PWM (up to 64 levels) to be implemented. Actually, the above considered column driver schemes are all for black and white displays. Gray levels through the PWM approach can be obtained with a modification of the scheme in Fig. 4.21, as illustrated in Fig. 4.22, where a 64-PWM technique is considered. Now, each cell of the frame buffer memory contains the number of bits encoding the gray levels (6 in our example). Besides, PWM generator blocks (implemented through comparators) are inserted at the output of the buffer. They compare the output of a 6-bit counter with the incoming 6-bit data word. The comparator output goes high only if the gray-level-encoding word is greater than the counter word.

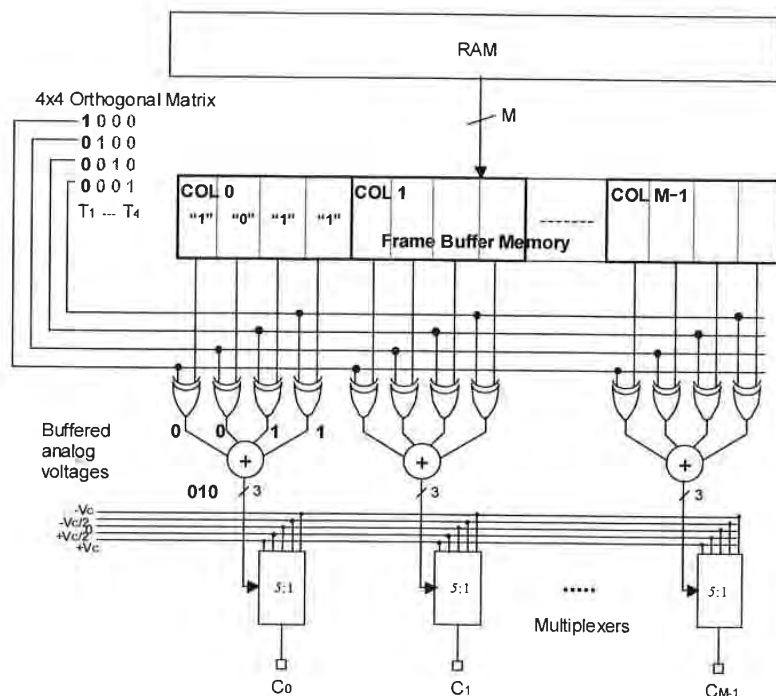


Fig. 4.21 Block diagram of another column-driver scheme for MLA-4

Considering again $f_F = 60$ Hz, $N=160$, $M=128$, $p=4$, $n_{GL}=64(=2^6)$, we get approximately that the required maximum frequency of the local oscillator is $f_{OSC} = f_F \cdot N \cdot p \cdot n_{GL} = 2.46$ MHz which is practical for mobile applications owing to the associated relatively low power dissipation.

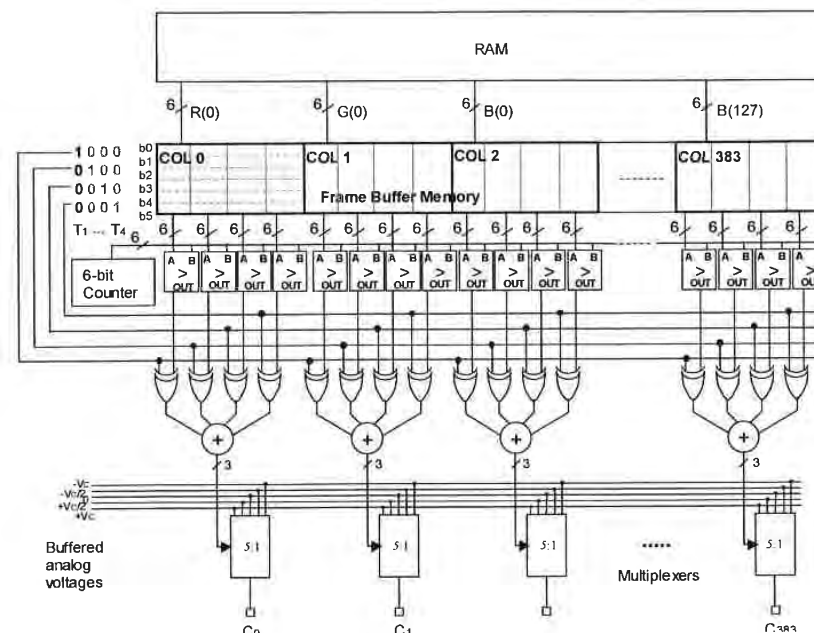


Fig. 4.22 Block diagram of column driver for color LCD adopting MLA-4 and PWM

4.7 Silicon Processes for Display Drivers

The silicon process required to implement single-chip driver ICs is quite challenging. Other than providing mixed-signal functionalities and allowing the integration of SRAM banks, it must possess also high-voltage capability (from 20 to 40 V).⁸ In addition, the demand for increased resolution and number of colors mandates for high gate density. Therefore, special technologies compatible with advanced CMOS families, but based on High Voltage Gate (HVG) CMOS devices have been developed.

Considering the specific case of mobile devices for consumer electronics, the market is very competitive and products have very short life (from 1 to 3 years).

⁸A process with these behaviors is of course developed by silicon foundries not only to cover passive-matrix and active-matrix LCDs (see Chapters 5 and 6) but also emissive (OLED) displays.

Keeping low the cost is thereby mandatory. This issue is addressed through the use of mature CMOS technologies ($0.35\text{ }\mu\text{m}$ – $0.13\text{ }\mu\text{m}$), reduction of available process steps (e.g., limited number of metal layers) and efforts on IO area reduction including either *Circuit Under PAD* (CUP)⁹ or *Bond over Active* (BOA)¹⁰ approaches.

This section is largely based on [ABC2005], a paper describing the BCD-HVG8 (Bipolar, CMOS and DMOS) process family developed by STMicroelectronics. The HVG8 process exploits a $0.18\text{-}\mu\text{m}$ standard CMOS technology with several enhancements such as:

- (1) Shallow Trench Isolation (STI) for CMOS isolation;
- (2) Borderless Contacts;
- (3) Dual Gate Oxide for 1.8-V/5-V CMOS devices (whose main electrical characteristics are summarized in Table 4.1). The low leakage current of the 1.8-V devices allows also the realization of compact SRAM banks based on the 6T cell (bit size $4.45\text{ }\mu\text{m}^2$, in line with all available advanced $0.18\text{-}\mu\text{m}$ CMOS processes). Figure 4.22a shows the schematic of a SRAM cell and the micrograph of a SRAM bank is depicted in Fig. 4.23a. The vertical geometries are diffusions (transistor source/drain terminals) and the horizontal ones are polysilicon layers (transistor gate terminal). Metal contacts and paths are not shown in the photograph 4.22b. Symbol X means to row decoder;
- (4) A number of 5 Al-Cu metal levels are allowed with the last one realized by either Al-Cu or pure Cu thick layer (though only three metal levels are utilized for LCD driver implementations, to keep fabrication costs low). The higher thickness of the upper metal allows long low-voltage-drop lines realization. This feature is very useful in display drivers because of their typical high aspect ratio.

The high voltage options offered by the HVG8 process are several and include:

- (1) 20-V/32-V/40-V HVG MOS transistors through thick gate oxide;
- (2) High voltage MOS transistors with low voltage (1.8/5 V) thin gate oxides (Drift MOS) for Antifuse One Time Programmable (OTP) memory blocks (OTP bit density in the range of 1 kbit/mm^2 has been achieved);
- (3) LDMOS transistors for OLED drivers where large currents are needed.

⁹To save chip space, active circuitry is placed underneath the bonding pads. The CUP technique, which violates the rule of conventional layout for a chip, uses a variety of support structures that contain metals, dielectrics and their combinations designed to protect device components and to minimize damage caused by probe testing and subsequent assembly.

¹⁰Typical wirebond pad designs consist of a top-level metal that does not include any circuitry beneath the bonding region. The BOA technique was developed to utilize this region beneath wirebond pads in order to minimize die area.

Table 4.1 Main electrical parameters of HVG8 1.8-V and 5-V CMOS

	Parameter	1.8 V ($L_{\min}=0.18\text{ }\mu\text{m}$)	5 V ($L_{\min}=0.6\text{ }\mu\text{m}$)
nMOS	V_T (mV)	680	850
	I_{on} ($\mu\text{A}/\mu\text{m}$)	510	500
	I_{off} (pA/ μm)	2	<1
pMOS	V_T (mV)	–770	–775
	I_{on} ($\mu\text{A}/\mu\text{m}$)	–220	–290
	I_{off} (pA/ μm)	–3	–1

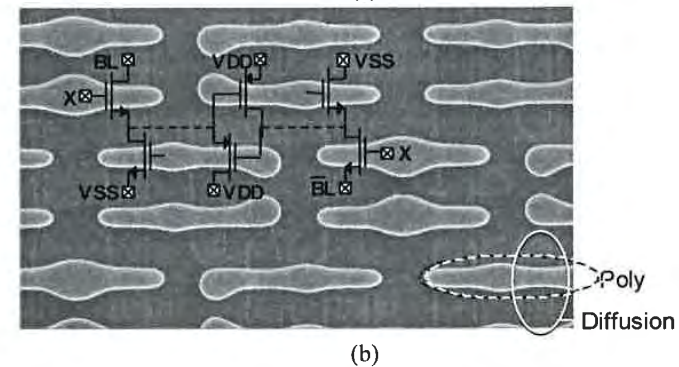
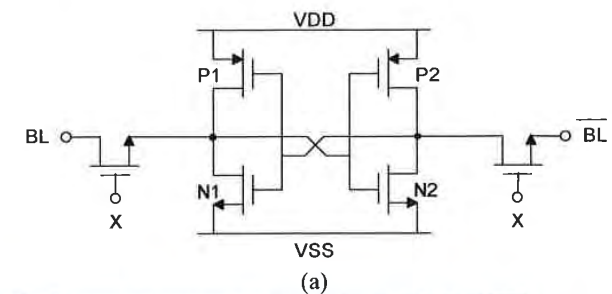


Fig. 4.22 (a) SRAM cell schematic, (b) micrograph of a SRAM bank in HVG8 technology

4.8 Packaging and Assembling Techniques

In this section we will describe the two main technologies that allow the electrical connection of the display to the driving circuits and of the driving circuits to the PCB. The same techniques described are not restricted to PMLCDs but are used also for Active Matrix LCDs.

Due to the great number of connections and the near impossibility of soldering ITO, both **Chip on Flex (COF)** and **Chip on Glass (COG)** approaches are widely used for driver IC attachment.

Anisotropically Conductive Adhesive Films (ACFs) are usually exploited to as an interconnection material for COG and COF [YP1998, S2004]. ACFs are composite materials consisting of polymer matrix, i.e., the adhesive and conductive particles, as illustrated in Fig. 4.23.

The fraction of conductive particles varies between 0.5 and 5% of the volume. The particle types vary from solid metal particles to polymer spheres coated with metal, the latter being most popular for high-density display applications [WT1999].

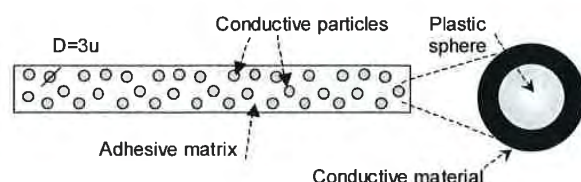


Fig. 4.23 Anisotropically Conductive Adhesive Films (ACFs) are used to electrically connect the Driver ICs to either the track on glass or tape automated bonding

4.8.1 Chip on Flex

In the original approach (first used by SHARP in 1985), the driver IC is packaged in a flexible **Tape Carrier Package (TCP)** and attached to the glass with **Tape Automated Bonding (TAB)** as illustrated in Fig. 4.24.

To allow flexibility the TCP has slits at regular distances (see Fig. 4.25a), and the tape can be bent only in a position corresponding to a slit. To improve performance and reduce costs, a new approach was developed called Chip on Film (1998).

The appearance of TCP or COF is similar, as both techniques rely in mounting the IC on a tape (see Fig. 4.25a, b). However, COF offers some substantial advantages: (1) it is free of slits and can be flexed in any position and with a greater freedom (oblique bend is possible), (2) it allows a finer bonding pitch ($< 35 \mu\text{m}$), (3) it allows high density packaging. Figure 4.26a shows the micrograph of a gold bump, while Fig. 4.26b shows the connections between the inner leads and bumps (in this case ACF is not used, but instead a gold-tin eutectic between the bump and the tin of the inner leads is formed [ML1986]).

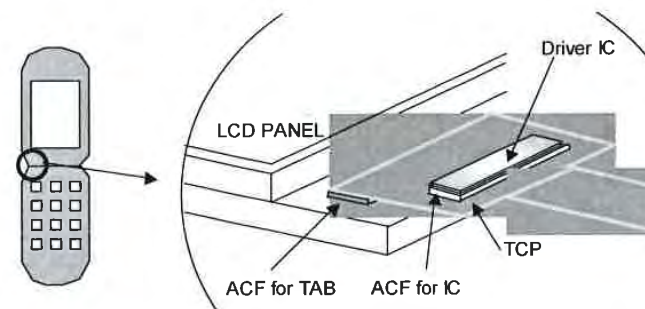


Fig. 4.24 TCP approach

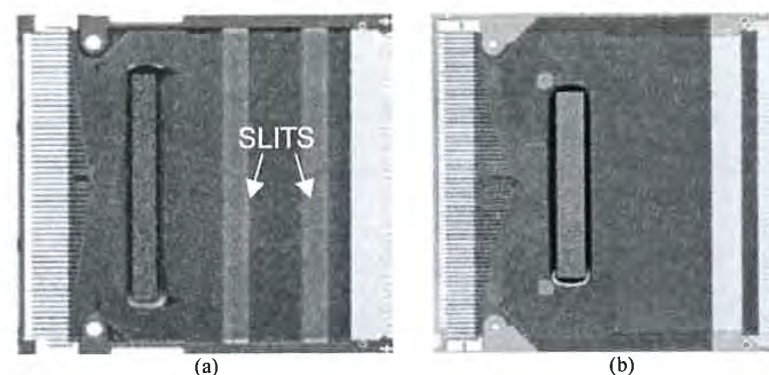


Fig. 4.25 Examples of (a) COF and (b) TCP [TNF2003]

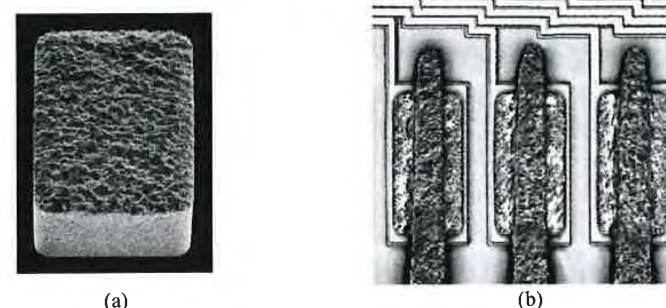


Fig. 4.26 Micrographs of (a) a gold bump and (b) connection between bumps and inner leads in COF via gold-tin eutectic bonding [TNF2003]

4.8.2 Chip on Glass

COG was first introduced in 1983 by Citizen and since then the method diffused significantly [KL1999]. In this approach the IC is mounted directly on the glass substrate, avoiding the use of the flex and reducing costs. Figure 4.27 depicts an LCD panel with Driver IC connected via COG approach. The drive lines of an LCD are typically brought to a single glass bonding ledge, and routed along the inactive sides of the display to their intended destinations.

As illustrated in Fig. 4.28, conventional IC wire bonding is here replaced by the formation of gold bumps. After prebonding the ACF to the glass with mild heat and low pressure, the driver IC is aligned in such a way that its bump pattern matches the pad pattern on the glass. Then, the IC is pressed against the ACF and glass applying heat through the bonding tool. Conductive particles should be trapped between each bump-pad pair in order to ensure conductivity. The adhesive allows anisotropic conduction, only in the vertical direction. Extra polymer should be pressed out from under the IC.

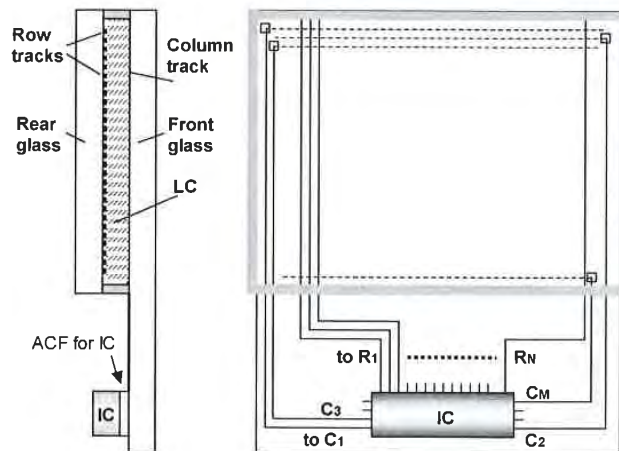


Fig. 4.27 LC panel with COG driver IC

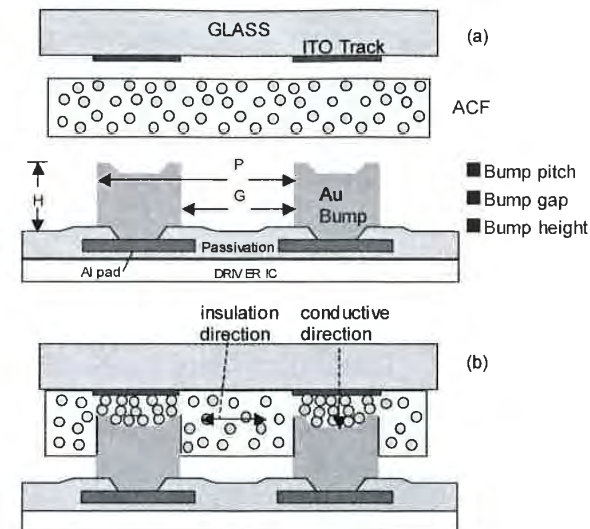


Fig. 4.28 COG technique. Cross section of a driver IC, Bumps, ACF, and Glass with typical dimensions: (a) before and (b) after electrical connection is formed

4.9 Concluding Remarks

We conclude this chapter by presenting an example of CSTN LCD ('C' stands for color) driver IC developed by STMicroelectronics, called the STE2028. It is designed for a 162×132-RGB LCD with 262k colors. It adopts the HVG technology and provides fully integrated booster (with the exception of the bulk capacitors), a 385-kbit SRAM and a 0.8-kbit OTP memory. It exploits MLA-4, n-line inversion and both PWM and FRC algorithms. It allows also partial display mode, enabling screen saver controls for power consumption reduction. The chip size is around 17 mm². Figure 4.29 shows the complete layout. Figure 4.30 illustrates the percentage of analog and digital component sections of the driver.

The complete block diagram is illustrated in Fig. 4.31. The reader will recognize many of the blocks although indicated with somewhat slightly different nomenclature (eg., MLS instead of MLA).

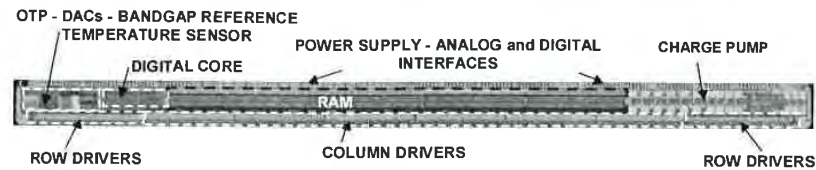


Fig. 4.29 Layout of the STE2028 LCD driver

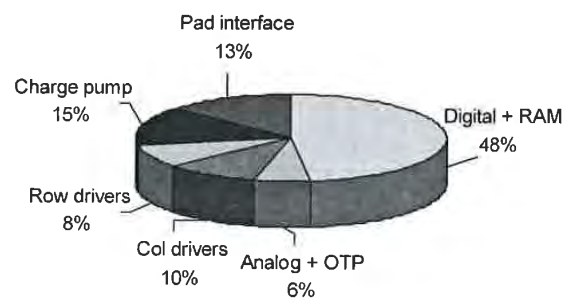


Fig. 4.30 Block partitioning of the STE2028 LCD driver

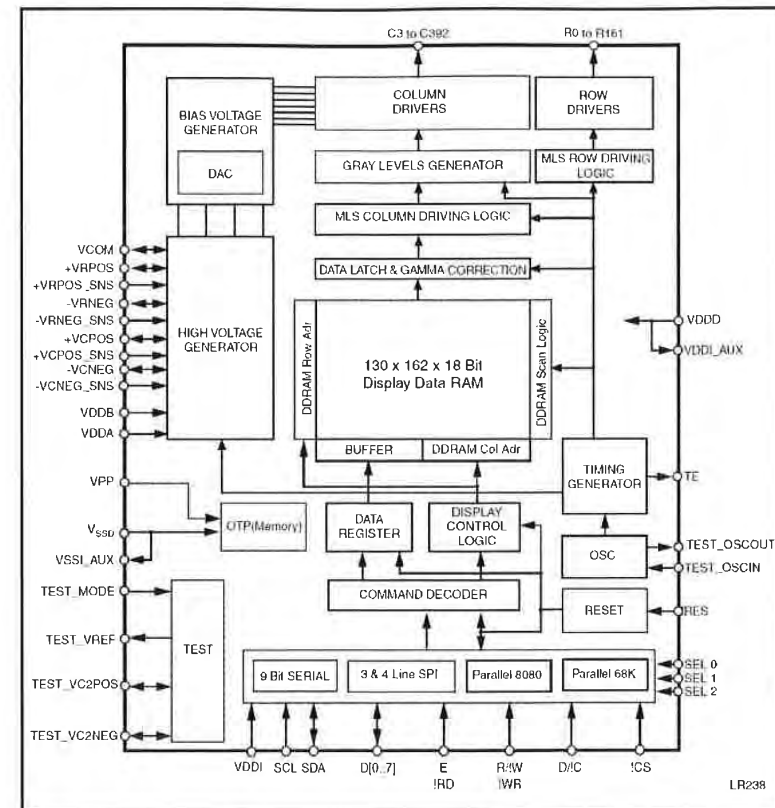


Fig. 4.31 Block diagram of the STE2028 LCD driver IC (Courtesy of STMicroelectronics)

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Chapter 5

Active Matrix LCDs and Their Addressing Techniques

We have seen that in PMLCDs the display contrast depends on the drive margin, but this parameter is in turn a function of the number of rows so that the more rows are added, the less contrast is obtained. **Active matrix LCDs (AMLCDs, also called TFT LCDs)** remove these multiplexing limitations by exploiting a switching element and a storage capacitor at every pixel of the display. These switches are usually implemented through transistors made up of deposited thin films, and are therefore called thin-film transistors,¹ TFTs. A TFT at each pixel allows the column voltages to be applied only to the row that is being addressed, while the storage capacitor maintains the pixel information for the whole frame also when the addressing signal is removed. Therefore, a high contrast is possible and a fast LC mixture can be used, since the pixel no longer has to respond to the average voltage over a whole frame period, as in PMLCDs. For the same reason the phenomenon of crosstalk is also minimized.

AMLCDs are hence suitable for full-motion video, requiring time responses below 20 ms. As main drawbacks, the TFT process increases production costs (at this purpose, a limit in the number of masks of the TFT process is from 4 to 6), reduces the yield and decreases the aperture ratio of the pixel: thus, to maintain an acceptable display luminance a brighter backlight is needed (by increasing power consumption).

In this chapter, after briefly describing the principal TFT devices and the structure of an AMLCD panel, addressing techniques for AMLCDs will be discussed. Related driver ICs and their implementation issues will be treated in Chapter 6.

¹The majority of AMLCDs use TFTs as switching devices. An alternative commercially exploited solution is constituted by the Metal-Insulator-Metal (MIM) diode. The MIM low fabrication temperature is compatible with plastic substrates.

5.1 Thin Film Transistors

In this section we will discuss the main characteristics of TFTs. Compared to conventional Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) implemented in a crystalline Si substrate, TFTs have similar model equations but, due to the reduced carrier mobility, μ , they exhibit poorer performance both in terms of conductance and switching speed. Being implemented on an insulating substrate, TFTs lack the substrate electrode (called Body or Bulk in conventional MOSFET devices), and have thus only three terminals named **Drain** (D), **Gate** (G), and **Source** (S). The presence of the insulating substrate provides ideal isolation of each device and negligible parasitic capacitances [LLB1992].

Figure 5.1 shows the cross section and top view of a basic² TFT (with the layers materials typically adopted) along with the circuit symbol. The gate-source voltage, v_{GS} , determines the TFT ON/OFF condition as it causes the formation of the conducting **channel** between the source and the drain (i.e., charges are induced in the semiconductor layer).

One type of TFT, the *n*-channel TFT, operates similarly to the *n*-channel MOSFET. In particular, we define the threshold voltage (whose typical value is about 1–4 V) as

$$V_{TH} = -qn_0d_{CH} / C_{ox} \quad (5.1)$$

where q is the charge of the electron, n_0 is the charge density in the channel, d_{CH} is the channel thickness and C_{ox} is the capacitance of the gate dielectric per unit area ($C_{ox} = \epsilon_0\epsilon_f/t_g$, where t_g is the thickness of the gate dielectric, see Fig. 5.1). The channel is formed if $v_{GS} > V_{TH}$, in this case the TFT is turned on and a current, i_D , can flow through the source and drain terminals, provided that a drain-source voltage, v_{DS} , is applied. Conversely, $i_D = 0$ if $v_{GS} \leq V_{TH}$.

Assume now $v_{GS} > V_{TH}$. Denoting as W and L the channel width and length, respectively (as shown in Fig. 5.1), we can write the expression of the drain current as a function of the gate-source and drain-source voltages both in the triode and saturation operating conditions [S2006, MK2003].

The **triode region** (also termed the **linear region**) is characterized by $v_{DS} \leq v_{GS} - V_{TH}$ and the drain current expression is

$$i_D = \mu C_{ox} \frac{W}{L} \left[(v_{GS} - V_{TH})v_{DS} - \frac{v_{DS}^2}{2} \right] \quad (5.2)$$

In this region, one of the most important parameters is the ON resistance offered by the TFT between the source and drain (when used as a switch), whose expression is

²The device depicted in Fig. 5.1 is a “bottom-gate” (or inverted staggered) TFT implemented in either amorphous silicon or polysilicon. Other alternatives are possible; see for instance [B2005, K2004].

$$R_{ON} = \left(\frac{\partial i_D}{\partial v_{DS}} \right)^{-1} = \frac{1}{\mu C_{ox} \frac{W}{L} (v_{GS} - V_{TH})} \quad (5.3)$$

The above relation shows that the TFT conductivity is increased by increasing the **aspect ratio**, W/L , and/or the **overdrive voltage** $v_{GS} - V_{TH}$.

In the **saturation region** we have $v_{DS} > v_{GS} - V_{TH}$ and the drain current is dependent to a first approximation only on v_{GS} (we will see that this assumption is not accurate in polysilicon TFTs, due to the so called *kink* effect)

$$i_D = \frac{\mu C_{ox} W}{2 L} (v_{GS} - V_{TH})^2 \quad (5.4)$$

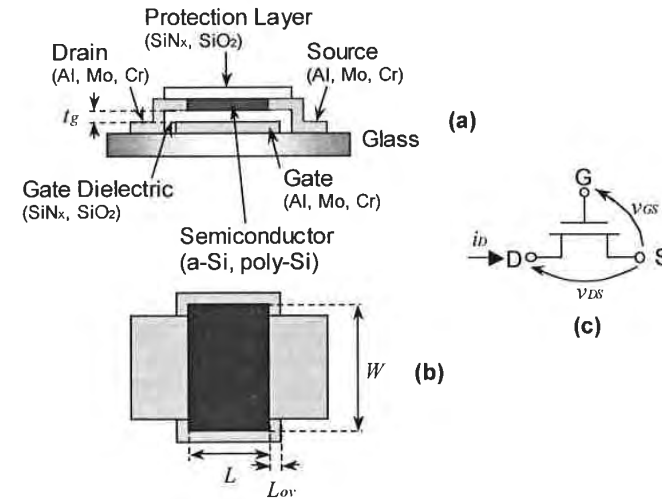


Fig. 5.1 Basic TFT: cross section (a), top view (b) and circuit symbol (c)

The output characteristics derived from (5.2) and (5.4) with v_{GS} as a parameter (and normalized to the factor $\mu C_{ox} W/L$), are plotted in Fig. 5.2. The transition region between the triode and saturation region (for $v_{DS} = v_{GS} - V_{TH}$) is represented by the dashed portion of a parabola whose equation is

$$i_D = \frac{\mu C_{ox} W}{2 L} v_{DS}^2 \quad (5.5)$$

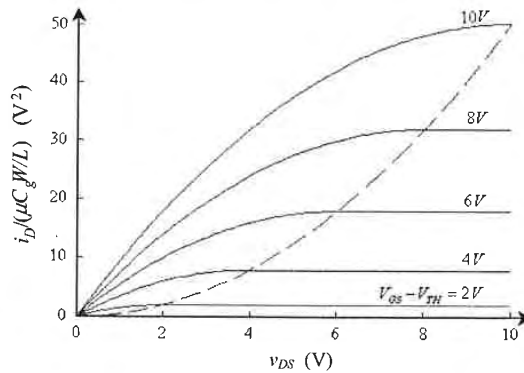


Fig. 5.2 Output characteristics (drain current versus drain-source voltage) of a generic TFT for $V_{GS} - V_{TH} = 2, 4, 6, 8, 10$ V

Ideally, i_D is equal to zero when $v_{GS} < V_{TH}$, in reality a **leakage conduction** is always present. Therefore, an important aspect regarding TFT addressing is the proper minimization of this current. Indeed, when the pixel is not selected, a high leakage current discharging the storage capacitor leads to a loss of information, but a larger storage capacitor results in a lower aperture-ratio and in a slowdown of the charging time.

Other important parameters for the dynamic behavior of a TFT are the **parasitic capacitances** between couples of terminals, C_{GS} , C_{GD} and C_{DS} . In particular, the gate-drain capacitance (or equivalently the gate-source capacitance, because these capacitances are equal in a transistor operating in triode) has two main contributions: one is due to the channel capacitance, the other is caused by the overlap region between the gate and drain. Assuming v_{DS} small in triode region, about half of the channel capacitance contributes to C_{GD} and the other half to C_{GS} . If the length of the overlap is labeled as L_{OV} (see Fig. 5.1) the expressions of maximum and minimum (when the TFT is near the cutoff region) of C_{GD} are

$$C_{GD,max} = W(L/2 + L_{OV})C_{ox} \quad (5.6a)$$

$$C_{GD,min} = WL_{OV}C_{ox} \quad (5.6b)$$

We will show in Section 5.3 that C_{GD} is the origin of performance degradation as it causes unwanted charge redistribution effects.

The above equations are useful for pencil-and-paper calculations. Circuit designers need more accurate but efficient models (time-domain simulations of a complete panel may be an onerous task in terms of required CPU time) to be used in their simulators (SPICE-like models are the most popular) [HS1989, SSJ1997].

5.1.1 a-Si TFT

The most common semiconductor layer used for the integration of TFTs on glass substrates is realized with hydrogenated **amorphous silicon** (a-Si:H, in the following a-Si for simplicity). It allows large-area fabrication in a low-temperature process (300°C–400°C) and is the dominant technology in computer and television LCDs. The main difference between a-Si TFT and a conventional Si MOSFET is the lower electron mobility (in the range of 0.2–1.5 cm²/Vs, while it is greater than 1800 cm²/Vs in crystalline Si), due to the presence of electron traps in amorphous silicon. Hence, a-Si TFTs are inadequate to be used in analog and high-speed digital processing directly on glass, but they are instead suitable for the implementation of ON/OFF pixel switches with refresh frequencies around 60 Hz. However, even for this simple scope, the low mobility would require extremely large aspect ratios, thereby reducing the **aperture-ratio** (i.e., only a portion of the pixel's area is transparent to light when the pixel is ON) and ultimately decreasing the display's brightness and contrast. To mitigate this problem, since the transconductance depends also on the gate-source overdrive, the gate of a TFT is driven by a high voltage, typically around 20 V.

Because a-Si materials exhibit poor stability and their structure can be modified by strong illumination and charge carrier injections (in particular its OFF current increases with incident light), the a-Si TFT must be shielded from light. Besides, this technology allows only *n*-channel TFTs to be realized. The conductivity of a-Si *p*-channel TFTs would not be sufficiently high, even as switches for LCDs.

Another disadvantage of a-Si TFTs is the **threshold voltage shift** (by several volts over a few hours with a DC voltage stress [GW2001, KNH2004]). It can be expressed by $\Delta V_{TH}(t) = A(V_{G,ST} - V_{TH,i})t^\beta$, where A and β are two temperature dependent parameters, $V_{G,ST}$ is the stress gate voltage and $V_{TH,i}$ is the threshold voltage before stress which has duration t [PBH1989]. It is caused by two mechanisms. At higher gate electric fields, electrons are injected into the gate dielectric [P1983, PD1993]; at lower electric fields, charges are trapped in the interface a-Si and gates [HMM1986]. The threshold voltage increase is larger for lower temperature processes [GW2001]. The shift is not a severe problem for switch operations, but the function of digital circuits is impaired when the static noise margin decreases considerably (becoming zero when V_{TH} increases to $V_{DD}/2$) [LVS2006]. The shift has different polarity for ON and OFF state, therefore a partial cancellation occurs. In any case, a practical driving scheme must take into account a threshold tolerance in the TFTs.

5.1.2 Poly-Si TFT

Polysilicon represents an alternative material appropriate to realize the TFT silicon layer, adopted in recent years for small-area displays. It is a silicon-based material, which contains numerous Si grains with sizes ranging from 0.1 to several microns. In semiconductor manufacturing, polysilicon is usually deposited as amorphous films by LPCVD (Low Pressure Chemical Vapor Deposition) and then crystallized by laser annealing above 900°C. This technology requires also expensive quartz substrates. The same approach cannot be exploited by the LCD industry since the strain temperature of glass is only about 650°C. **Low Temperature Polysilicon**

(LTPS) technologies, built on low-cost glass, were then developed based on either excimer laser annealing or by combined solid state phase crystallization [H1986, TDM1999, MS1999, JSH1996].

The preparation of LTPS film is more complicated than a-Si, and LTPS is more exposed to process variations over the substrate area. However, LTPS TFTs have a higher mobility than a-Si TFT (up to two orders of magnitude for electrons, 30 to 400 cm^2/Vs , and up to 150 cm^2/Vs for holes) and the implementation of both *n*-channel and *p*-channel transistors is possible, therefore they allow to increase the pixel aperture ratio (higher mobility means smaller TFT area for a given transconductance) and are suitable for the integration of CMOS-like circuits directly on the glass substrate (ultimately leading to a complete System on Glass, SOG). The latter is a remarkable advantage that allows the number of electrical connections on the LCD panel to be drastically reduced, thereby increasing reliability and compactness. The connections are made in the thin film technology using a mask which is in any case needed for processing the display.

A schematic cross section of a poly-Si TFT is shown in Fig. 5.3a. For high drain-source voltages, poly-Si TFTs exhibit the so called **kink** effect consisting in an anomalous increase of the drain current, as illustrated in Fig. 5.3b. This effect is mainly originated by the high voltage at the drain end of the channel that accelerates charges causing in turn an avalanche current (impact ionization). This current is able to flow to ground in monocrystalline Si ICs, being the body electrically connected to a bias voltage. For TFTs the substrate is insulating glass, therefore this current increases the drain current. Of course, to contrast this problem, low supply voltages should be adopted. A Lateral Body Terminal (i.e., the extension of the channel area serving as collector of the charges) was also employed [Y1999].

Recently, Sharp in conjunction with Semiconductor Energy Laboratory Co. Ltd., has developed a process called **Continuous Grain Silicon (CG Silicon)**, a further evolution of the LTPS technology, leading to the commercial introduction of high-resolution, high-definition system LCDs for mobile terminal devices in 2002. A complete CPU on a glass substrate is shown in Fig. 5.4 [N2003].

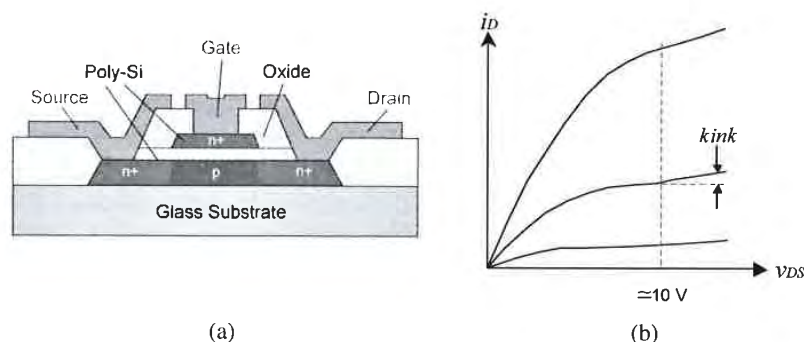


Fig. 5.3 Poly-Si TFT, (a) cross section and (b) drain current versus drain-source voltage putting in evidence the kink effect

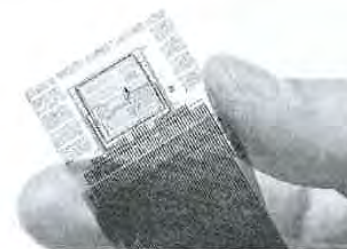


Fig. 5.4 CG Silicon CPU formed on a glass substrate (Semiconductor Energy Laboratory) [N2003]

5.1.3 Further Comparison of a-Si and Poly-Si TFT Performance

Figure 5.5 shows the a-Si and poly-Si TFT characteristics for $V_{DS} = 5$ V. The poly-Si TFT size is only 1/10 of its a-Si counterpart, to provide the same drain current corresponding to $V_{GS} = 20$ V. The smaller size of transistors (in consequence of the greater mobility electron) can increase both resolution (pixels per inch) and aperture-ratio improving the image definition. For this reason and for the large process tolerances of poly-Si, displays with a high pixel density and pixel size of $15 \mu\text{m} \times 15 \mu\text{m}$ are best addressed by poly-Si TFTs. Application of this kind are small high-definition displays for view finders in camcorder, or projection displays [B2005].

Compared to a-Si TFTs, poly-Si TFTs exhibit higher OFF currents, caused by the electric field at the highly doped drain and the imperfect crystalline structure of the poly-Si material. Methods currently adopted against this limitation are the dual gate structure or adding another process step to realize a lightly doped drain (LDD) [L2001].

From the driving voltage point of view, a negative gate-source voltage around -5 to -8 V (not just 0 V) is adopted for a minimum leakage condition below 10 pA. On the other hand, to compensate for the low electron mobility the gate-source voltage is set at around 20 V for switch-on, to provide a drain current in the order of 100 μA .

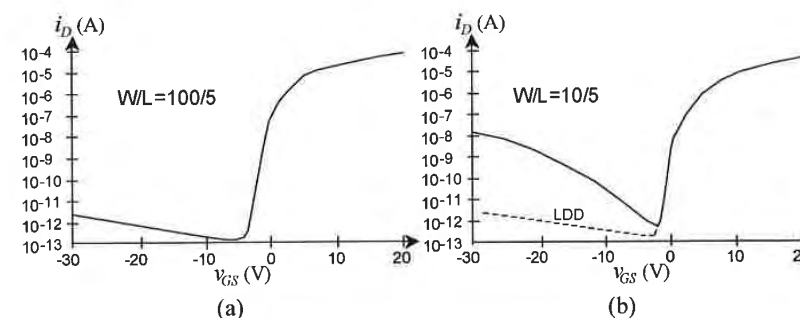


Fig. 5.5 Drain current versus gate-source voltage for an n-channel TFT: (a) a-Si TFT with $W/L = 100 \mu\text{m}/5 \mu\text{m}$ and (b) poly-Si with $W/L = 10 \mu\text{m}/5 \mu\text{m}$. Voltage V_{DS} is 5 V in both cases. The dashed curve in (b) represents the OFF current obtained with lightly doped drain (LDD) technology

5.2 Structure of an AMLCD Panel

Like a passive-matrix color LCD, an AMLCD has a sandwich-like structure with liquid crystal filled between two glass plates kept to a controlled distance by spacers and exploits backlight, polarizers and color filters (the latter fitting the upper substrate). The cross section of an AMLCD is shown in Fig. 5.6.

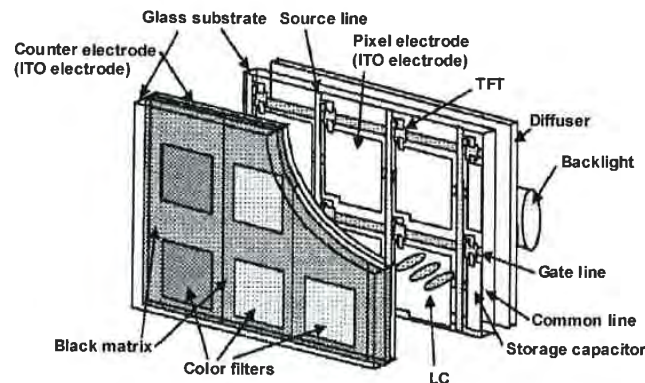


Fig. 5.6 Cross section of an AMLCD [U2006]

Each pixel of a color panel is subdivided into three RGB subpixels. TFTs are integrated on the back glass substrate, along with storage capacitors, ITO electrodes and interconnect wiring, as shown in Fig. 5.7a. In an AMLCD panel, the row and column electrodes are called gate and source electrodes (with reference to the associated TFT terminals). By scanning the gate lines sequentially, and by applying signal voltages to all source lines in parallel, we can address all pixels. As a result, the addressing of an AMLCD is very simple and performed line by line. Unlike passive-matrix addressing which required orthogonal row and column signals, the use of TFTs in AMLCDs makes each row independent from the others. Indeed, the thin-film storage capacitor (C_S), accessed through the associated TFT, memorizes the source (pixel data) voltage and maintains it even after the gate (selection) signal is removed. Note that C_S is added in parallel to the intrinsic LC capacitor, as the value of C_{LC} is too low for adequate charge retention. Between the color filters is placed a **black matrix**, made of an opaque metal, such as chromium (Cr), which shields the (a-Si) TFTs from room light and prevents light leakage between pixels to minimize photo-generated leakage currents in the TFTs. A double layer of Cr and CrOx is used to minimize reflection from the black matrix.

Figure 5.7b shows the electrical model of a subpixel with the storage capacitor C_S in parallel to C_{LC} connected as a load of the TFT. It is worth noting that C_S can be connected either to an adjacent gate line (**Cap-on-Gate**) or to a dedicated common storage bus (**Cap-on-Common**), see Fig. 5.7b, c. As main drawbacks, the former solution increases the capacitive load seen by the gate drivers while the latter

reduces the pixel aperture.³ The former approach is thus unsuitable for panels with a diagonal size larger than about 20 in.

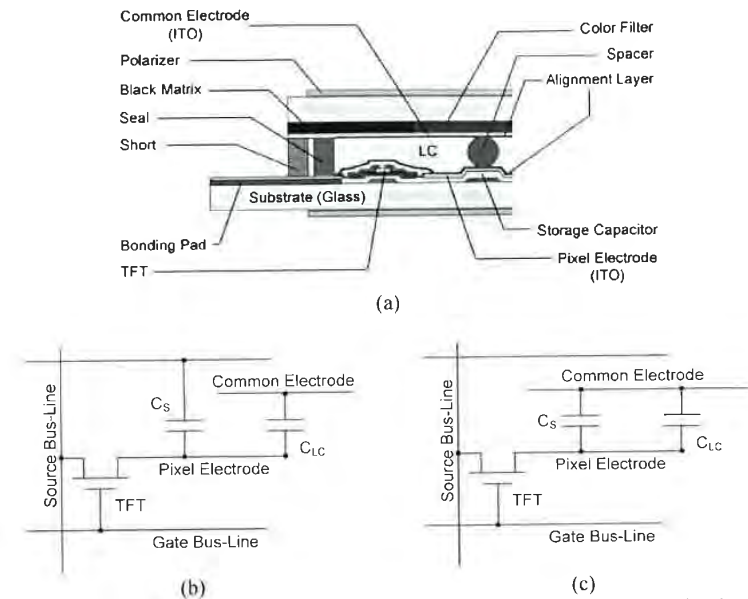


Fig. 5.7 Cross section of a subpixel in an AMLCD panel (a) equivalent circuits in Cap-on-Gate structure and (b) in Cap-on-Common structure (c)

In the unit cell, as shown in Fig. 5.8, TFT electrodes, storage-capacitor electrodes, signal bus-lines, and the black-matrix material constitute opaque areas. The combined areas of these elements, along with the area of the pixel aperture through which light can pass, determine the **aperture ratio** of the pixel: the aperture ratio is given by the area of the pixel aperture divided by the total pixel area (aperture area plus the area of the opaque elements). To increase this value as much as possible, the size of the opaque elements must be made as small as possible, while maintaining a design that maximizes the size of the pixel-electrode area. The Source Line (ITO) overlaps the bottom plate of the storage capacitor and the Gate Line at each pixel in the same column. These overlapping areas cause coupling capacitances.

A complete view of the TFT, C_S and C_{LC} is provided in Fig. 5.9a. The relative areas of C_S and C_{LC} are clearly evidenced. A top view showing the RGB color filters is depicted in Fig. 5.9b.

³To increase the pixel luminance for outdoor use, the opaque electrode of C_S can be covered with a reflective material, as suggested in [FNK2003].

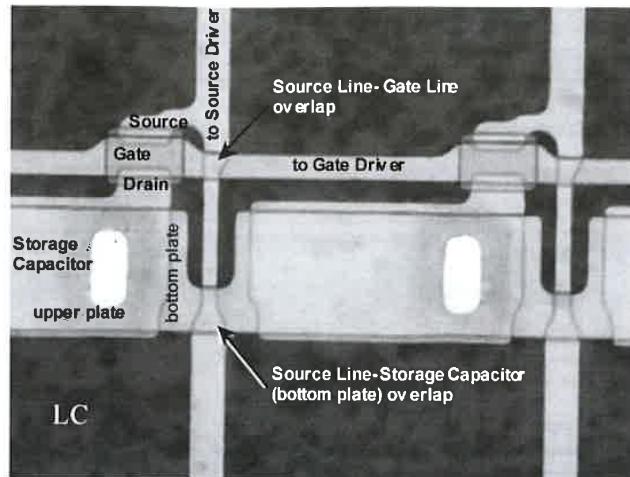


Fig. 5.8 Micrograph of an AMLCD panel showing the TFT, Storage Capacitor and interconnections

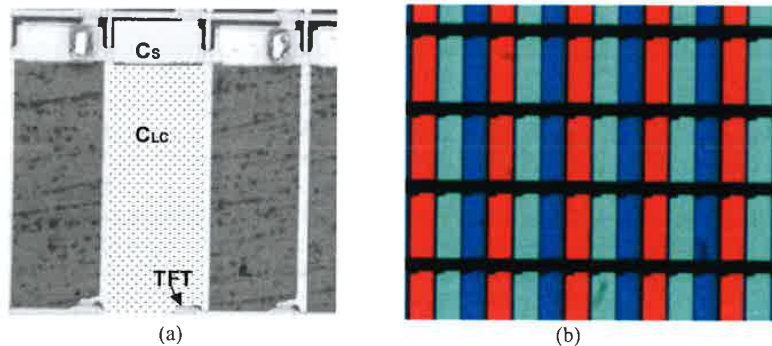


Fig. 5.9 AMLCD panel micrographs: (a) detail of the pixel capacitances (bottom view); Fig. 5.8 is a magnified version of this figure. (b) detail of the RGB color filters (top view)

5.3 General Considerations

In contrast to PMLCDs that need some form of elaboration technique (such as PWM and/or FRC) for gray level generation, AMLCDs are inherently designed to produce gray levels depending on the voltage magnitude applied to the pixel from the source line. With reference to Fig. 5.7, applying a suitable positive pulse voltage through a specific gate line has the effect of turning on all the TFTs whose gates are connected to that bus line. Capacitors C_{LC} and C_S are then charged at the voltage level applied through the (data) source line. This charged state (and consequently the pixel voltage

level) can be maintained as the gate voltage goes to a negative value, at which time the TFTs nominally turn off. The main function of C_S is then to maintain the voltage on the pixel electrode until the next source voltage is applied. An example of AMLCD addressing waveforms is illustrated in Fig. 5.10.

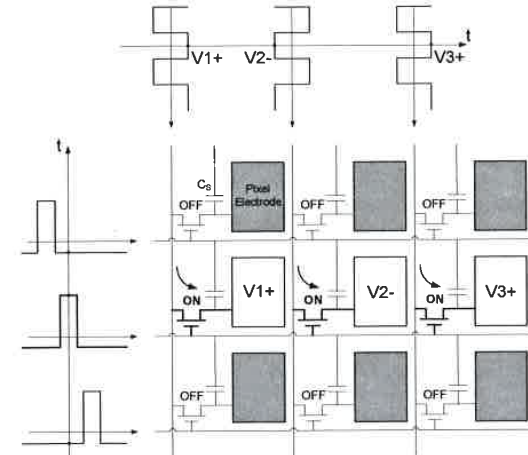


Fig. 5.10 Addressing example of an Active Matrix LCD

As already discussed, the scanning frequency should be at least 30 Hz to avoid flickering. A refresh frequency of 60 Hz is the result of a trade-off between elimination of flicker and low power dissipation. If $f_F = 1/T_F$ is the frame (scanning) frequency and N is the number of rows of display, the maximum access time to pixel (row time), T_R , will be:

$$T_R = \frac{T_F}{N} \quad (5.7)$$

When switched on, the resistance offered by the TFT, R_{ON} , should be adequate to charge the pixel capacitance at the maximum source line voltage within the row time. The ON time constant guaranteeing that, within $0.5T_R$, the voltage stored on C_S is only 1% below the desired value is given by (we consider that the source line voltage polarity is inverted in two consecutive addressing of the same pixel):

$$R_{ON}(C_S + C_{LC}) \leq \frac{T_R}{2 \ln(2 \cdot 100)} = \frac{T_R}{10.6} \quad (5.8)$$

On the other hand, from (5.3), the expression of R_{ON} is

$$R_{ON} = \frac{1}{\mu C_g \frac{W}{L} (v_G - v_{DATA} - V_{TH})} \quad (5.9)$$

where the TFT is assumed in the triode region. To ensure this, voltage v_G is made quite high, and v_{DS} is small, being zero at the steady state (i.e., no current flows in the TFT at the steady state). Hence, from (5.8) and (5.9) we find the minimum aspect ratio W/L of the TFT

$$\frac{W}{L} \geq \frac{1}{\mu C_g (v_G - v_{DATA} - V_{TH}) R_{ON}} = \frac{10.6(C_s + C_{LC})}{\mu C_g (v_G - v_{DATA} - V_{TH}) T_R} \quad (5.10)$$

When the TFT is OFF, several causes concur to discharge the pixel capacitance, modifying gray scale uniformity. The TFT leakage current is the most relevant one, but also resistive leakage through the LC material (R_{LC}) should be considered. Considering only the TFT leakage, I_{OFF} , this should be low enough to retain the charge on the pixel capacitance during the frame time. Assuming the parallel of C_s and C_{LC} be discharged by the constant current I_{OFF} during T_F , we get

$$I_{OFF} \leq \frac{C_s + C_{LC}}{T_F} \Delta V_{LK} \quad (5.11)$$

where ΔV_{LK} is limited by the maximum acceptable voltage loss (referred to one gray level).

Tables 5.1 and 5.2 show some technology and display parameters for a very large (56.3-in.) monolithic a-Si AMLCD [KSG2002].

Table 5.1 Technology parameters of a 56.3-in. a-Si AMLCD [KSG2002]

AMLCD Technology Parameter	Value	Unit	Symbol
Row (Gate) Bus Resistance (Width 30 μm)	18.8	Ω/mm	R_R
Row Bus Capacitance (Width 30 μm)	226	fF/mm	C_R
Column (Source) Bus Resistance (Width 10 μm)	45.0	Ω/mm	R_C
Column (Source) Bus Capacitance (Width 10 μm)	82.4	fF/mm	C_C
Row-to-Column Bus Overlap Capacitance	15.3	fF	C_{XC}
Column-to-Row Bus Overlap Capacitance	15.3	fF	C_{XR}
Sub-Pixel Liquid Crystal Capacitance	8.24	pF/mm ²	C_{LC}/A
Sub-Pixel Storage Capacitance	204	pF/mm ²	C_S/A
TFT Channel On-Resistance (Width/Length 100 $\mu\text{m}/4.5 \mu\text{m}$)	0.0634	M Ω -mm	R_{TFT}^{On}
TFT Channel Off-Resistance (Width/Length 100 $\mu\text{m}/4.5 \mu\text{m}$)	0.607	T Ω -mm	R_{TFT}^{Off}
TFT Gate-to-Source Capacitance	689	fF/mm	C_{GS}/W
TFT Gate-to-Drain Capacitance	919	fF/mm	C_{GD}/W
Row Driver Resistance	1.00	k Ω	R_{RS}
Row Driver Capacitance	1.00	pF	C_{RS}
Column Driver Resistance	1.40	k Ω	R_{CS}
Column Driver Capacitance	1.40	pF	C_{CS}

Table 5.2 Display parameters of a 56.3-in. a-Si AMLCD [KSG2002]

AMLCD Display Parameters	Value	Unit
Number of Horizontal Pixel	1280	1
Number of Vertical Pixel	720	1
Number of Column Lines	3840	1
Number of Row Lines	720	1
Aspect Ratio	16 x 9	1
Horizontal Pixel Pitch	0.974	mm
Vertical Pixel Pitch	0.974	mm
Pixel Array Width	1,246	mm
Pixel Array Height	701	mm
Display Size	1,429 (56.3)	mm (in)
Worst Case Sub-Pixel Charging Time	26.8	μs

As a numerical example, consider an XGA display with 768 rows and 60-Hz frame frequency ($N=768$, $T_F=16.6$ ms and $T_R=21 \mu\text{s}$) in which 256 gray levels are generated by a voltage swing (v_{DATA}) of 8 V (typical for large size panels). Thus, 31.2 mV defines one gray level. Assume also that $C_{LC,min}=150$ fF, $C_{LC,max}=300$ fF, $C_s=400$ fF, $V_{ROW}=v_G=20$ V, $C_g=1.06 \cdot 10^{-8}$ F/cm, $\mu=0.45$ cm²/V·s, $V_{TH}=3.5$ V. From (5.8) we get that $R_{ON} \leq 2.83$ M Ω , yielding $W/L \geq 7.4$ from (5.10). Assuming also as tolerable a ΔV_{LK} lower than 1/6 one gray level (about 5 mV), we get from (5.11) $I_{OFF} \leq 0.16$ pA. The values of W/L and I_{OFF} we have found are compatible with usual TFT technologies.

5.3.1 Kickback

The gate-drain parasitic capacitor C_{GD} is also the cause of charge redistribution with the pixel capacitor C_s . This phenomenon is referred to as the **kickback effect** (it is the same effect known as the clock-feedthrough experienced by designers of digital and switched-capacitor circuits) and causes a decrement, ΔV_{KB} , in the LC voltage when the TFT is turned OFF at the end of a select period (the same effect holds also when the TFT is turned ON, but it is not cause of error since it occurs at the beginning of a select period). Considering Fig. 5.11, if ΔV_G is the voltage change at the TFT gate when the row is deselected and assuming V_{COM} constant, the voltage shift of V_{LC} is expressed by

$$\Delta V_{KB} = \frac{C_{GD}}{C_{GD} + C_s + C_{LC}} \Delta V_G \quad (5.12)$$

As a result of both kickback and leakage effects, the behavior of a typical V_{LC} waveform appears as qualitatively illustrated in Fig. 5.12. The kickback causes a modification of the data voltage and the generation of an unwanted DC component (if the common electrode is held at the middle of data signal voltage swing). It is thus the cause of gray-scale errors [KTK1982], shadings [KKN1990] and flickering [K1989].

From (5.12) we see that the error is nullified for C_{GD} ideally equal to zero. Besides, ΔV_{KB} decreases by increasing $C_S + C_{LC}$, but this decreases also the ON charging time constant. We recall that C_{GD} for a TFT in triode is not a constant as it depends on V_{GS} . A conservative choice in order to evaluate (5.12) is to take the maximum value (5.6). Also C_{LC} is not a constant, as already discussed in Section 2.2.3. Referring to Fig. 2.12, we can take the minimum value $C_{LC,min}$.

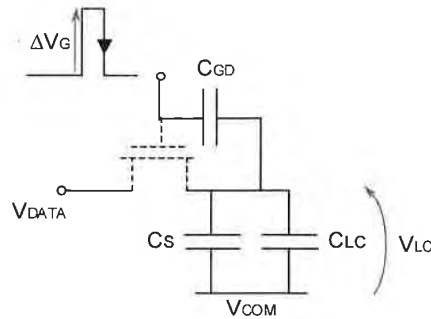


Fig. 5.11 Pixel electrical model for evaluating the kickback effect

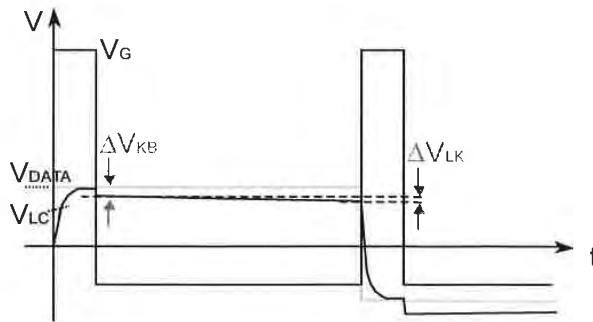


Fig. 5.12 Qualitative behavior of the pixel voltage due to kickback and leakage

As a numerical example, with the same data given before, assuming $\Delta V_G = 20 - (-5) = 25$ V, $C_{GD,max} = 50$ fF and again $C_S + C_{LC,min} = 550$ fF, we get the maximum $\Delta V_{KB} = 2.08$ V, corresponding to about 67 gray levels. In addition, since the voltage shift is always negative, a DC component is added to V_{LC} that, as said in many occasions, must be avoided (limited to below 100 mV). This demonstrates that a compensation of the kickback is mandatory. To be more precise, we can write

$$C_{LC} = C_{LC,min} + \Delta C_{LC} \quad (5.13)$$

where ΔC_{LC} depends on V_{LC} . Since also C_{GD} is dependent on the applied voltage, we can rewrite (5.12) as follows

$$\Delta V_{KB} = \Delta V_G \cdot \left[\frac{C_{GD,max}}{C_{GD,max} + C_S + C_{LC,min}} \right] \quad (5.14)$$

$$- \frac{C_{GD,max} \cdot \Delta C_{LC}}{(C_{GD,max} + C_S + C_{LC,min}) \cdot (C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC})}$$

STATIC
DYNAMIC

We recognize a first static term, independent of the LC polarization, and a second dynamic term which depends on the LC capacitance variation (function of the gray level) and the TFT gate-drain capacitance variation. The sign of the dynamic term is opposite to that of the static term.

We will describe techniques for kickback compensation in Section 5.5.

5.3.2 RC Delay and Pre-emphasis Driving Method

As the size and resolution of AMLCD panels increase, the large RC delay introduced by the rows and columns causes a smoothing of the ideal square waveforms and may cause an incomplete settling of the gate and column voltages. In other words, the rate of transferring the analog video signal voltage to the pixel in one row time becomes insufficient. The effect is illustrated in Fig. 5.13a. This limitation is particularly evident when driving large voltage increments onto pixel located at the farthest end of a column and of a row (with respect to the driving ends) and is particularly critical for moving pictures causing motion blur (leading to the appearance of a smear behind any moving image) [M2004]. Besides, the delay of the gate pulse waveforms produces also different kickback moving from the nearest driver end to the farthest end. To alleviate these problems, various approaches have been developed. One is technological, through the adoption of materials with low resistance for gate and source lines: for example, copper [TLT2006] or aluminium alloy [AIH1998, TCC1998]. The other approaches rely on modifying the driving method.

Source and gate drivers can be assembled at both ends of columns and rows for simultaneous driving in **Both-Side Drive** or **Dual Driving** (see Fig. 5.14). In this case the worst-case driving occurs at the center of the panel. Compared to the single-side drive, this method reduces the RC delay time up to a factor of 4, but doubles the number of gate and source drivers, thereby increasing fabrication costs. Source drivers are more critical in terms of area and power dissipation, therefore this approach is used only for the gate drivers.

A fast single-side drive technique exploits **Pre Emphasis (or Overdrive)**. Here the row time interval is divided into a “pre-emphasising sub-period” and a “source-follower sub-period”, as illustrated in Fig. 5.13b. During the former interval, the source data waveforms use pre-emphasis amplitudes that, as we will see, vary according to the magnitude of the gray-level shift to be driven [KSK2003]. During the source-follower period, the image data voltage is presented to the source line. Figure 5.13b illustrates qualitatively the improvement offered by this technique compared to the conventional one [NIM2007].

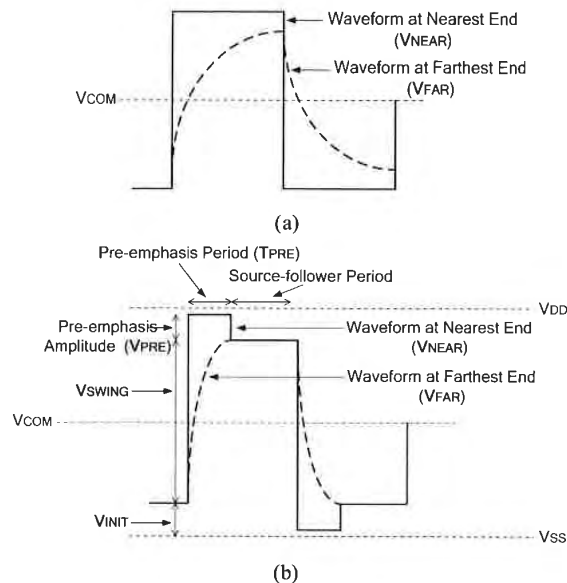


Fig. 5.13 Waveforms for: (a) conventional single side and (b) Pre-Emphasis driving. The curves in solid (dashed) line represent the waveform near (far from) the driver end

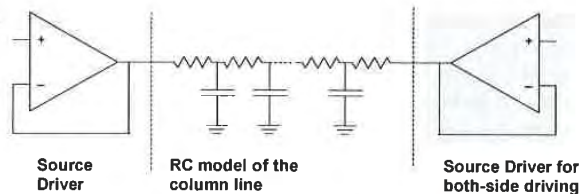


Fig. 5.14 Illustration of the Both-side Drive approach with RC-chain model of the source line and unity-gain amplifier(s) of the source driver

Let us evaluate analytically the required pre-emphasis voltage according to the data voltage swing and allowed pre-emphasis time T_{PRE} . During this time interval, the nearest end of the source line is driven at the voltage swing that is the sum of the target (nominal) voltage swing and the pre-emphasis voltage swing expressed by

$$V'_{SWING} = V_{SWING} + V_{PRE} \quad (5.15)$$

The farthest end source line voltage is expressed by

$$V_{FAR} = V_{INIT} + V'_{SWING} \left(1 - e^{-\frac{t}{R_{DATA} C_{DATA}}} \right) \quad (5.16)$$

where V_{INIT} is the initial pixel data voltage. The product $R_{DATA} C_{DATA}$ can be evaluated through the Elmore's delay model [E1948] and, for an M -length RC-chain, it is

$$R_{DATA} C_{DATA} = \sum_{i=1}^M \left(C_i \sum_{j=1}^i R_j \right) \quad (5.17)$$

After imposing that at time T_{PRE} the far-end voltage of the source line must have settled to the target voltage level, $V_{INIT} + V_{SWING}$, we get [SK2007]

$$V_{PRE} = \frac{e^{-\frac{T_{PRE}}{R_{DATA} C_{DATA}}} V_{SWING}}{1 - e^{-\frac{T_{PRE}}{R_{DATA} C_{DATA}}}} \quad (5.18)$$

The above relation shows that the pre-emphasis voltage must be proportional to the required voltage swing. Observe that to maintain the advantages deriving from the method, pre-emphasis voltages need to change according to T_{PRE} and the display panel load conditions. Besides, to manage the overdrive voltages required by the approach, a higher-voltage IC fabrication process than that used for conventional source drivers must be adopted (i.e., V'_{SWING} may result higher than the ordinary supply).

Based on the fact that extremely white or black regions have insignificant effects on image quality, a modification of the approach that varies the duration of the pre-emphasis period, rather than its amplitude (this last can be maintained only in the mid-swing regions) was proposed in [YHY2007]. This method does not require higher-voltage IC processes.

5.4 Crosstalk Reduction and Polarity Inversion Techniques

5.4.1 Crosstalk in AMLCDs

As explained in Section 3.3.3 crosstalk is mainly due to capacitive coupling effects. These effects worsen with the scaling of lithographic dimensions and increasing number of gray levels. In addition, crosstalk in AMLCDs can be caused by the following mechanisms [LL1998]:

(1) incomplete pixel charging (due to high TFT ON resistance, unequal data driver loading, line delay);

(2) leakage current from the pixel through the TFT.

Remedies to these problems are based on material selection, fabrication processes, device design and layout. For our scopes, we will address only the capacitive coupling effects.

Consider the layout of a pixel and his crosstalk capacitance shown in Fig. 5.15.

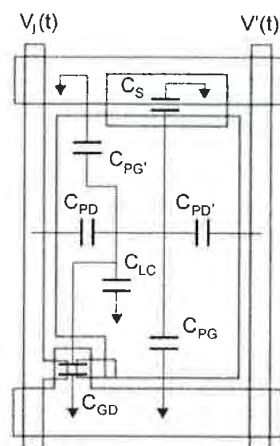


Fig. 5.15 Top view of a typical pixel layout showing the data-line-to-LC-electrode parasitic capacitance regions

The ratio of parasitic capacitances coupling the pixel-to-data line (α) and pixel-to-adjacent-data line (β) can be expressed as

$$\alpha = \frac{C_{PD}}{C_{LC} + C_S + C_{PG} + C_{PG'} + C_{GD} + C_{PD} + C_{PD'}} \quad (5.19a)$$

$$\beta = \frac{C_{PD'}}{C_{LC} + C_S + C_{PG} + C_{PG'} + C_{GD} + C_{PD} + C_{PD'}} \quad (5.19b)$$

where C_{PD} and $C_{PD'}$ are the data-line- and adjacent-data-line-to-pixel-electrode coupling capacitances, respectively, while C_{PG} and $C_{PG'}$ are the gate-line- and adjacent-gate-line-to-pixel-electrode coupling capacitances, respectively.

Note that all capacitances except C_S in (1) and (2) are functions of the liquid crystal dielectric constant. Both parameters α and β must be minimized to minimize the effects of crosstalk.⁴ One method relies on increasing C_S . Another one requires a ground-plane shielding beneath the data line. Both methods need added pixel area, at the expense of a smaller aperture ratio and larger gate-line delay.⁵ A third method is based on an appropriate data-driving scheme. It leaves unaltered the pixel layout and fabrication technology, thereby providing the least expensive and most straightforward approach to further pixel scaling. Note that this approach does not change α and β , but relies on incorporating some form of positive and negative data-line pulse-coupling cancellation. As a drawback, higher voltage drivers and/or higher driver power consumption may result.

We recall that any driving method must provide a nominally zero DC component of the pixel voltage. Actually a DC residual always exists and to avoid LC mixture damage, all present driving methods include some signal voltage polarity inversion in a time scale shorter than that needed for the mobile LC ions to move substantially.

According to the type of polarity inversion (in which the signs of both the row and column signals are periodically inverted) there are four possible driving methods. These are illustrated in Fig. 5.16 and are called **Frame Inversion**, **Column (Data-Line) Inversion**, **Row (Gate-Line) Inversion** and **Dot Inversion**.

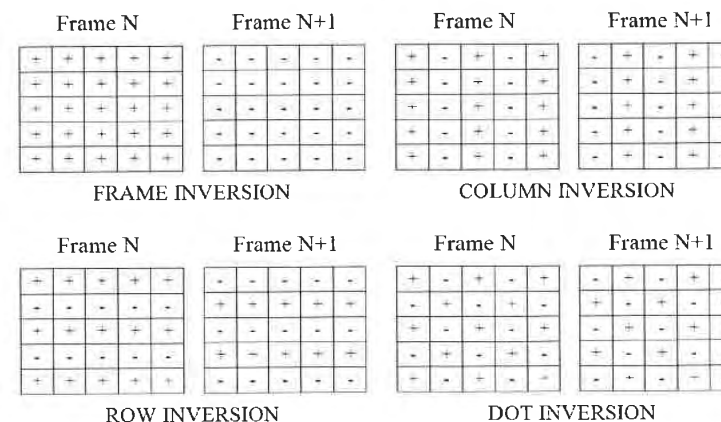


Fig. 5.16 Polarity inversion methods

⁴ $\alpha = 0.08$ and $\beta = 0.03$ were extracted for a VGA display in [LL1998].

⁵The IPS-Pro pixel structure has large C_S capacitance without reducing the aperture ratio because the common electrode is made of transparent material under the pixel electrodes [EOO2006].

The principal trade-off among the four mentioned driving methods is the degree of crosstalk cancellation versus driver chip power dissipation, and sensitivity to flicker.

In the **Frame Inversion** method, each source signal has the same data polarity and the data polarity is inverted once per frame time. The value of the instantaneous voltage across the liquid crystal capacitor in the i th row position is given by:

$$V_{pi}(t) = V_i + \alpha \cdot [V_j(t) - V_i] + \beta \cdot [V'_j(t) - V'_i] \quad (5.20)$$

where V_i and V'_i are the data voltages initially written onto the pixel and the adjacent pixel through pixel selection, respectively, through their corresponding TFTs. $V_j(t)$ and $V'_j(t)$ are the data-line and adjacent-data-line voltages with their respective parasitic coupling factors to the pixel, α and β .

In the Frame Inversion method, the RMS voltage at the i th row position in a N -row display can be derived from (5.20) as

$$\begin{aligned} \bar{V}_{pi}^2 = \frac{1}{N} \left\{ V_i^2 + \sum_{j>i}^N [V_i + \alpha(V_j - V_i) + \beta(V'_j - V'_i)]^2 \right. \\ \left. + \sum_{j=1}^{i-1} [-V_i + \alpha(V_j - (-V_i)) + \beta(V'_j - (-V'_i))]^2 \right\} \end{aligned} \quad (5.21)$$

where the first term (V_i^2) represents the value of voltage pixel during the TFT switching-on (line i -th selected), the second term represents the value of voltage pixel during the switching-on of all subsequent rows, while the third is the voltage pixel during the switching-on of the previous rows (reversed polarity).

The simplified expression, obtained by neglecting the second-order crosstalk terms (proportional to α^2 , β^2 , and $\alpha\beta$) in (5.21), is

$$\bar{V}_{pi}^2 \cong (V_i - \alpha V_i + \beta V'_i)^2 + \frac{2}{N} V_i \left[\sum_{j \geq i}^N (\alpha V_j + \beta V'_j) - \sum_{j=1}^{i-1} (\alpha V_j + \beta V'_j) \right] \quad (5.22a)$$

then

$$\bar{V}_{pi}^2 \cong (V_i - \alpha V_i + \beta V'_i)^2 + \frac{2}{N} \alpha V_i \left[\sum_{j \geq i}^N V_j - \sum_{j=1}^{i-1} V_j \right] + \frac{2}{N} \beta V_i \left[\sum_{j \geq i}^N V'_j - \sum_{j=1}^{i-1} V'_j \right] \quad (5.22b)$$

Since each pixel is made up of three (RGB) sub-pixels, in general it is $V_j(t) \neq V'_j(t)$. This condition guarantees that the first-order term in (5.22b) (linear in α and β) is dependent on the data-line voltage for one frame. The Frame Inversion is sensitive to flickering due to the absence of spatial averaging.

In a similar way, a general expression can be written for the case of the **Column Inversion** method, for which each consecutive signal line has alternating positive and negative data polarity and the data polarity is inverted once per frame time. By neglecting the second-order crosstalk terms, we obtain:

$$\bar{V}_{pi}^2 \cong (V_i - \alpha V_i + \beta V'_i)^2 + \frac{2}{N} \alpha V_i \left[\sum_{j \geq i}^N V_j - \sum_{j=1}^{i-1} V_j \right] - \frac{2}{N} \beta V_i \left[\sum_{j \geq i}^N V'_j - \sum_{j=1}^{i-1} V'_j \right] \quad (5.23)$$

Note that although $V_j(t) \neq V'_j(t)$, the Column Inversion method provides a better crosstalk compensation compared to the Frame Inversion owing to the polarity inversion between two adjacent columns that gives a *negative* contribution in the expression of RMS pixel voltage. This method is less sensitive to horizontal crosstalk caused by capacitive coupling between adjacent columns and can produce better crosstalk compensation to a larger number of pattern images compared to Frame Inversion. It is also less exposed to flicker due to the presence of spatial averaging.

For the **Row Inversion** driving method, where each signal line has the same data polarity and the data polarity is inverted once per scan line time, we obtain the expression in (5.24a) and by neglecting the second-order crosstalk terms we obtain the simplified expression in (5.24b).

$$\begin{aligned} \bar{V}_{pi}^2 = \frac{1}{N} \left\{ V_i^2 + \sum_{j(\text{even}) > i}^N [-V_i + \alpha(V_j - (-V_i)) + \beta(V'_j - (-V'_i))]^2 \right. \\ + \sum_{j(\text{even})=2}^{i-1} [V_i + \alpha(V_j - V_i) + \beta(V'_j - V'_i)]^2 \\ + \sum_{j(\text{odd}) > i}^N [V_i + \alpha(V_j - V_i) + \beta(V'_j - V'_i)]^2 \\ \left. + \sum_{j(\text{odd})=1}^{i-1} [-V_i + \alpha(V_j - (-V_i)) + \beta(V'_j - (-V'_i))]^2 \right\} \end{aligned} \quad (5.24a)$$

$$\begin{aligned} \bar{V}_{pi}^2 \cong & (V_i - \alpha V_i + \beta V_i')^2 \\ & + \frac{2}{N} \alpha V_i \left[\sum_{j(\text{odd}) \geq i}^N V_j - \sum_{j(\text{odd})=1}^{i-1} V_j - \sum_{j(\text{even}) > i}^N V_j + \sum_{j(\text{even}) > 1}^i V_j \right] \\ & + \frac{2}{N} \beta V_i' \left[\sum_{j(\text{odd}) \geq i}^N V_j' - \sum_{j(\text{odd})=1}^{i-1} V_j' - \sum_{j(\text{even}) > i}^N V_j' + \sum_{j(\text{even}) > 1}^i V_j' \right] \end{aligned} \quad (5.24b)$$

Compared to the Frame Inversion driving method described by (5.23), the Row Inversion one contains an additional polarity reversal, as it is evident from the separation of even and odd data-line values (V_j) and adjacent data-line (V_j') values. For this reason, the Row Inversion driving method, in general, provides better crosstalk compensation than the Frame Inversion driving method, but this is not guaranteed, because the magnitude of crosstalk is dependent upon the screen image pattern. For instance, if an alternating image pattern of black to white on the spatial periodicity of a scan line were present, the result is a worst-case adding of all coefficients of α and β for the case of the Row Inversion method. In general, image patterns tend to be uniform over a screen area of at least several gate-line spatial dimensions [LL1998]. In contrast to the Column Inversion method, this one provides a better compensation of the vertical crosstalk produced by capacitive coupling between the rows, but it is more sensitive to the horizontal crosstalk. As the Column Inversion, it is also less exposed to flicker. As above, a general expression can be written for the RMS pixel voltage in the case of the **Dot Inversion** method, where the column and the row inversion approaches are both applied to the data so that each consecutive signal line (column), as well as each consecutive gate line (row), has an alternating positive and negative data polarity, and the data polarity is inverted once per frame time. By neglecting the second-order crosstalk terms, the resulting expression is expressed in (5.25) and includes an additional polarity reversal compared to (5.24b).

$$\begin{aligned} \bar{V}_{pi}^2 \cong & (V_i - \alpha V_i + \beta V_i')^2 \\ & + \frac{2}{N} \alpha V_i \left[\sum_{j(\text{odd}) \geq i}^N V_j - \sum_{j(\text{odd})=1}^{i-1} V_j - \sum_{j(\text{even}) > i}^N V_j + \sum_{j(\text{even}) > 1}^i V_j \right] \\ & - \frac{2}{N} \beta V_i' \left[\sum_{j(\text{odd}) \geq i}^N V_j' - \sum_{j(\text{odd})=1}^{i-1} V_j' - \sum_{j(\text{even}) > i}^N V_j' + \sum_{j(\text{even}) > 1}^i V_j' \right] \end{aligned} \quad (5.25)$$

This method has virtually no flicker.

Equations (5.22b), (5.23), (5.24b), and (5.25) describing all four crosstalk-reduction driving methods show a gain-correction term $(V_i - \alpha V_i + \beta V_i')^2$ as the first term. For a simplified case, if $V_i = V_i'$, the gain correction is $(1 - \alpha + \beta)^2$, and the effect is only a parallel shift in the T/V curve which depends on the values of α and β . Any DC gain in the required RMS operation of the LC can easily be offset. In general, however, $V_i \neq V_i'$, which makes the gain term data dependent on the voltage or image pattern, and it cannot be easily offset.

Among the previous techniques, the Dot Inversion gives the best quality. Row and Column Inversion are suitable for the reduction of vertical and horizontal crosstalk effects, respectively. Since Column and Dot inversion needs source drivers with high voltage swings, a good trade-off between area/power consumption and image quality is given by the Row Inversion. Another approach that was not discussed and that is a further simplification of the Row Inversion is called **n-Line Inversion**. In this case polarity of the addressing waveforms is reversed at every n rows, where n is an integer less than the number N of matrix rows. Recently, **Vertical n-dot Inversion** has been adopted as a polarity reversal method to reduce power consumption while maintaining image quality [SKC2007]. The Vertical 2-dot Inversion is exemplified in Fig. 5.17.

Frame N					Frame N+1				
+	-	+	-	+	-	+	-	+	-
-	+	-	+	-	+	-	+	-	+
-	+	-	+	-	+	-	+	-	+
+	-	+	-	+	-	+	-	+	-
+	-	+	-	+	-	+	-	+	-

Fig. 5.17 Vertical 2-Dot Inversion driving method

In another technique, referred to as **Data Complement**, the row addressing time is partitioned into two intervals. During the first interval the data is applied to the source line, as usual. During the second interval all the row TFTs are turned OFF and the data complement (voltages with opposite sign) is applied to the source lines. If the two time intervals are equal, it can be easily shown that first-order crosstalk is eliminated [HAW1989]. The simplest case of equal subperiods halves however the net row time (it is now $T/2N$ instead of T/N) and hence requires an LC mixture with doubled switching speed. To avoid this drawback, the compensation interval can be a fraction $\delta T/N$ of the row time (with $\delta < 0.5$), and the amplitude of the complement voltage must be increased by a $\sqrt{\delta/(1-\delta)}$ factor.

5.4.2 Power Analysis of Polarity-Inversion Techniques

In this section we will evaluate the power consumption of the above polarity inversion methods. We will consider a display with N rows and M columns and

assume that the load capacitance of each source driver is constant and that the common electrode voltage V_{COM} is 0 V.

(a) Frame Inversion. In this case the lowest power consumption is obtained when all the pixel voltages of the same column are equal during a given frame time (white pixels are considered, otherwise for all black pixels the power consumption is theoretically zero). Indeed, in this case the Source Drivers have the minimum number of commutations. The power dissipated by a single column is hence:

$$P_{COL} = \frac{1}{2} \cdot C_{TOT} \cdot [V_{SAT} - (-V_{SAT})]^2 \cdot f_F = 2 \cdot C_{TOT} \cdot V_{SAT}^2 \cdot f_F \quad (5.25)$$

where C_{TOT} is the total capacitance seen by the Source Drivers, whose largest output voltages in the positive and negative frames are $+V_{SAT}$ and $-V_{SAT}$, respectively and f_F is the frame frequency.

The overall power consumption in this best-case condition is

$$P_{min} = 2 \cdot M \cdot C_{TOT} \cdot V_{SAT}^2 \cdot f_F \quad (5.26)$$

The worst case occurs when we have an alternating succession of black and white rows. In this case each Source Driver must provide N commutations in each frame.

$$P_{max} = \frac{1}{2} \cdot N \cdot M \cdot C_{TOT} \cdot V_{SAT}^2 \cdot f_F \quad (5.27)$$

P_{max} is $N/4$ times greater than P_{min} and then power consumption in Frame Inversion is limited by

$$P_{min} \leq P_{FI} \leq \frac{M}{4} \cdot P_{min} \quad (5.28)$$

(b) Column Inversion. The power consumption is exactly the same as in the previous case, because the pixels of the same column are subject to the same voltage. Hence, P_{CI} equals P_{FI} .

(c) Row and Dot Inversion. Dually to the previous approaches, here the maximum power consumption occurs when all the pixel voltages of the same column are equal during a given frame time. Indeed, in this case the Source Drivers have the maximum number of commutations.

$$P_{max} = 2 \cdot N \cdot M \cdot C_{TOT} \cdot V_{SAT}^2 \cdot f_F \quad (5.29)$$

and is 4 times greater than P_{MAX} of Frame e Column Inversion approaches. Besides from (5.26) it is N times greater than P_{MIN} obtained with Frame and Column Inversion. Therefore, we get

$$P_{min} \leq P_{RI} = P_{DI} \leq M \cdot P_{min} \quad (5.30)$$

The power consumption is greater in those driving methods where row polarity is switched from frame to frame.

For simplicity, we have assumed V_{COM} equal to 0 V. Actually, V_{COM} can be different from 0 and even a variable voltage (V_{COM} switching) in order to meet the constraints set by the adopted CMOS technology, area occupation, and/or low voltage demand. The V_{COM} switching approach increases the power dissipation and causes additional charge injection effects through parasitic capacitances. We will see in Section 5.5.2 that V_{COM} switching requires the same polarity for pixel of the same row and therefore cannot be adopted in both Column and Dot Inversion techniques.

5.5 Kickback Compensation Methods

We have seen in (5.14) that the error due to the kickback includes two contributions: a static one, independent of the gray level, and a dynamic one

$$\Delta V_{KB} = \Delta V_{KB,ST} + \Delta V_{KB,DYN} \quad (5.31)$$

The dynamic contribution, being dependent on the actual data, must be compensated by the source driver. The static part may be compensated through different approaches: we can shift V_{COM} (as illustrated in Fig. 5.18), or through the subsequent gate voltage for Cap-on-Common architectures or other techniques that will be described in the following.

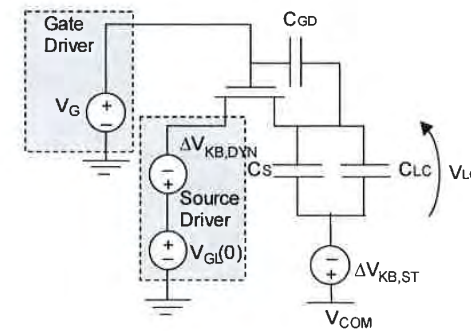


Fig. 5.18 Kickback compensation through the Source Driver (dynamic part) and V_{COM} (static part). The static part can be also compensated via the subsequent gate line, for cap-on-gate architectures

The gray-level voltage, V_{GL} , that through the source drivers must be applied to each pixel is hence

$$V_{GL} = V_{GL}(0) - \Delta V_{KB,DYN} \quad (5.32)$$

where $V_{GL}(0)$ represents the nominal gray-level voltage without kickback correction ("0" stands for zero kickback). Using (5.14), (5.32) can be rewritten as

$$V_{GL} = V_{GL}(0) + \frac{C_{GD,max} \cdot \Delta C_{LC}}{(C_{GD,max} + C_S + C_{LC,min}) \cdot (C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC})} \quad (5.33)$$

In practice, the nonlinear compensation required by (5.33) is implemented in the same circuit block that operates the Gamma Correction. Considering only the nonlinearity of the electrooptic T/V behavior, the Gamma Correction curve should be symmetrical in both positive and negative values, as already described in Section 4.5.2. This symmetry is lost if we introduce also the compensation of the dynamic part of kickback, as illustrated in Fig. 5.19. Note that due to the nonlinear dependence of C_{LC} on the applied voltage, curve (b) is not obtained by a simple shifting of curve (a). This implies that two different gamma curves must be constructed for both positive and negative polarity.

The kickback compensation for both the static and dynamic contributions is closely related to the driving scheme adopted [N1986, YKK1986, S1987, T1989, TNM1990]. In the following we will examine this issue with reference to the four polarity inversion techniques discussed before.

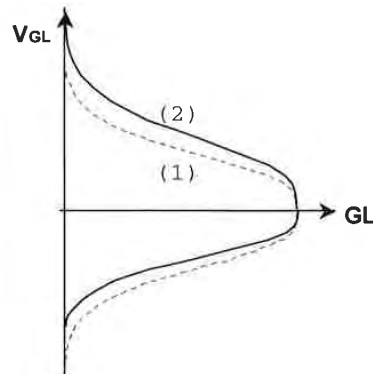


Fig. 5.19 Gamma correction curves: ideal symmetrical (1) and asymmetrical including dynamic kickback compensation (2)

5.5.1 2-Level Driving

In this scheme the Gate Driver provides a two-level output voltage, V_{ON} and V_{OFF} , for selected and unselected rows, as illustrated in Fig. 5.20. Voltage V_{COM} is held constant and consequently the Source Drivers signal swing must be $2V_{SAT}$ ($\approx 10V$) to

allow polarity inversion and thus covering the maximum excursion range given by $V_{COM} - V_{SAT}$ to $V_{COM} + V_{SAT}$. Nominally, V_{COM} can be either equal to 0 V or to V_{SAT} .

The dynamic kickback contribution is compensated via the asymmetrical Gamma Correction curve described before. Considering the static contribution and (5.14), its compensation is achieved by shifting the nominal value of V_{COM} by a quantity ΔV_{COM}

$$\Delta V_{COM} = \Delta V_{ST} = (V_{OFF} - V_{ON}) \cdot \frac{C_{GD,max}}{C_{GD,max} + C_S + C_{LC,min}} \quad (5.34)$$

Figure 5.21 illustrates the driving voltages in the case of 2-Level Driving for a Cap-on-Common LCD panel structure. The compensation effect is apparent. After the charge injection, the magnitude of the V_{LC} voltages in both positive and negative polarity are equal.

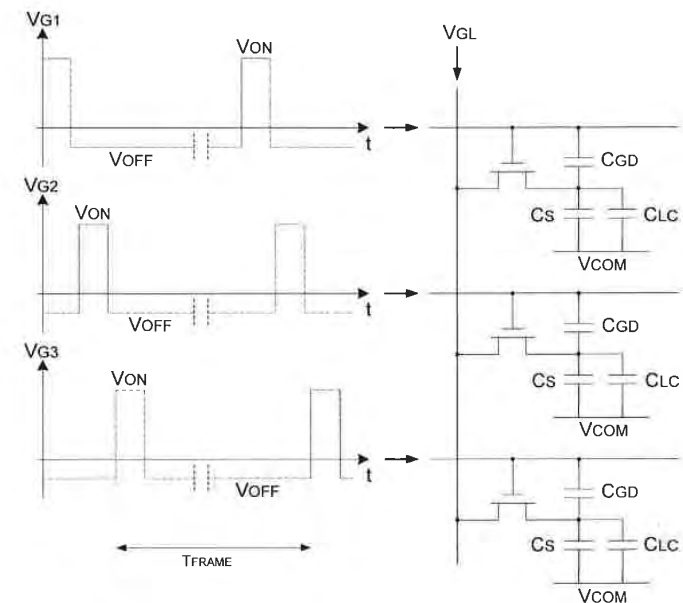


Fig. 5.20 Gate driver waveforms for three subsequent gate lines in the case of the 2-Level driving scheme

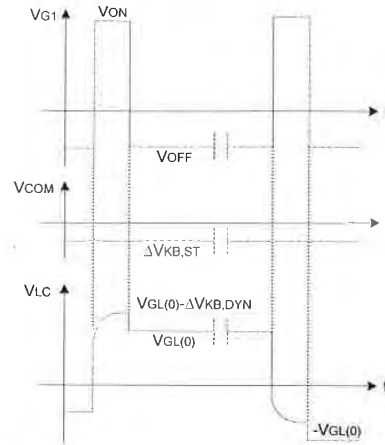


Fig. 5.21 Driving voltages in the case of 2-Level approach for a Cap-on-Common LCD panel structure

5.5.2 V_{COM} Switching

This technique operates the inversion polarity through the modulation of voltage V_{COM} , as illustrated in Fig. 5.22, where V_{GL} is the data voltage to be applied (in both polarities) to the LC pixel and V_{SD} is the output voltage of the Source Driver. Compared to the two-level approach, a Source Driver with a halved output swing is required. The approach is thereby suitable to be employed with low-voltage CMOS technologies.

Unfortunately, an additional error is introduced due to the charge injection from the common electrode when the TFT is OFF and V_{COM} is switching from 0 V to V_{SAT} , in order to allow the polarity inversion of the other rows (see Fig. 5.23). This problem is simply eliminated by introducing the same voltage change onto the gate voltage. Therefore, voltage V_{OFF} at the output of the Gate Driver can be either $V_{OFF,H}$ or $V_{OFF,L}$ so that

$$V_{OFF,H} - V_{OFF,L} = V_{COM,H} - V_{COM,L} \quad (5.35)$$

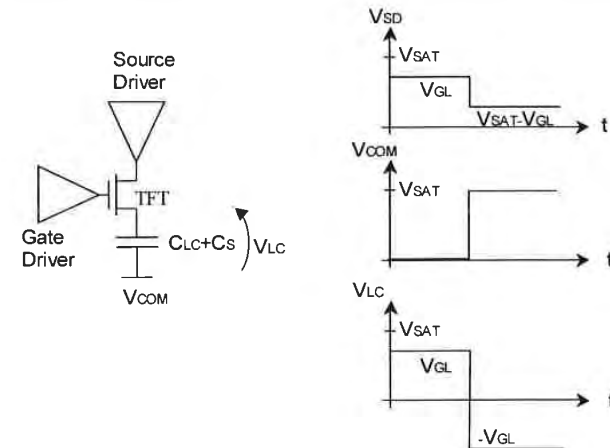


Fig. 5.22 Source Driver and V_{COM} waveforms for V_{COM} -switching driving scheme

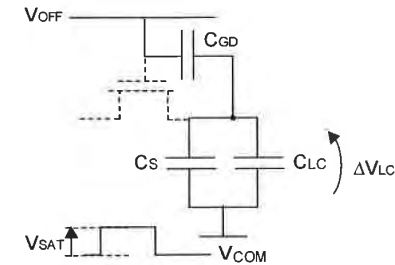


Fig. 5.23 Illustration of the error voltage (ΔV_{LC}) caused by the switching of V_{COM} when the row is unselected

The gate driving waveforms required in the V_{COM} -switching technique are exemplified in Fig. 5.24. To better illustrate the behavior, a Row Inversion method is assumed.

As far as the kickback is concerned, in this case the amount of kickback differs from positive to negative polarity, owing to the different C_{LC} and C_{GD} and also to the different step amplitude, that is $V_{ON} - V_{OFF,L}$ for negative polarity and $V_{ON} - V_{OFF,H}$ for positive polarity.

Consequently, the kickback amount is

$$\Delta V_{KB}^+ = (V_{ON} - V_{OFF,H}) \cdot \left[\frac{C_{GD,max}}{C_{GD,max} + C_S + C_{LC,min}} + \frac{C_{GD,max} \cdot \Delta C_{LC}}{(C_{GD,max} + C_S + C_{LC,min}) \cdot (C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC})} \right] \quad (5.36a)$$

$$= \Delta V_{KB,ST}^+ + \Delta V_{KB,DYN}^+$$

$$\Delta V_{KB}^- = (V_{ON} - V_{OFF,L}) \cdot \left[\frac{C_{GD,max}}{C_{GD,max} + C_S + C_{LC,max}} - \frac{C_{GD,max} \cdot \Delta C_{LC}}{(C_{GD,max} + C_S + C_{LC,min}) \cdot (C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC})} \right] \quad (5.36b)$$

$$= \Delta V_{KB,ST}^- + \Delta V_{KB,DYN}^-$$

The compensation of the static contribution is performed by shifting the value of V_{COM} by $\Delta V_{KB,ST}^+$ and $\Delta V_{KB,ST}^-$ and in turn the values $V_{OFF,H}$ and $V_{OFF,L}$. The expression of the pixel voltages in both polarities are

$$V_{LC}^+ = V_{GL}^+ + \Delta V_{KB}^+ - \Delta V_{COM,L} \quad (5.37a)$$

$$V_{LC}^- = V_{GL}^- + \Delta V_{KB}^- - (V_{SAT} + \Delta V_{COM,H}) \quad (5.37b)$$

where $\Delta V_{COM,L}$ and $\Delta V_{COM,H}$ are the correction values of the low and high V_{COM} level, respectively. As stated before, 0 and V_{SAT} are the low and high V_{COM} ideal levels (neglecting any kickback).

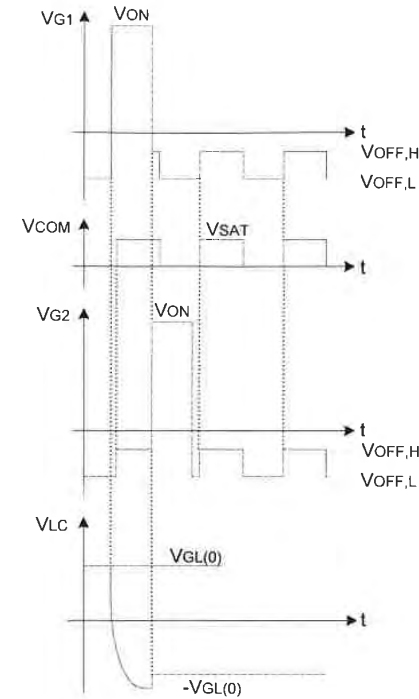


Fig. 5.24 Waveforms of two adjacent gate lines, common electrode, and pixel for V_{COM} -switching driving scheme

The dynamic contribution is compensated as usual via the Gamma Correction curve. Observe that for negative polarity the Gamma curve extends to negative voltage values. This should be avoided if source drivers with positive output swing are to be adopted. To obtain a completely positive Gamma curve it must be shifted by a constant value equal to the dynamic kickback of a *black* pixel. Rearranging (5.37) we get:

$$V_{LC}^+ = V_{GL}^+(0) + \Delta V_{KB,ST}^+ - (0 + \Delta V_{COM,L}) \quad (5.38a)$$

$$V_{LC}^- = V_{GL}^-(0) + \Delta V_{KB,DYN}^-(\text{Black}) + \Delta V_{KB,ST}^- - (V_{SAT} + \Delta V_{COM,H}) \quad (5.38b)$$

To obtain the correct pixel voltages $V_{LC}^+ = V_{GL}^+(0)$ and $V_{LC}^- = V_{GL}^-(0) - V_{SAT}$, the required $\Delta V_{COM,L}$ and $\Delta V_{COM,H}$ are:

$$\Delta V_{COM,H} = \Delta V_{KB,ST}^- + \Delta V_{KB,DYN}^-(\text{Black}) \quad (5.39a)$$

$$\Delta V_{COM,L} = \Delta V_{KB,ST}^+ \quad (5.39b)$$

Finally, from (5.35) and (5.39) we get:

$$V_{COM,H} = V_{SAT} + (V_1 - V_{OFF,H}) \cdot \frac{-C_{GD,max}}{C_{GD,max} + C_S + C_{LC,max}} \quad (5.40)$$

$$V_{COM,L} = \frac{-C_{GD,max} \cdot [C_{GD,max} \cdot V_{SAT} + (C_{LC,max} + C_S) \cdot (V_1 - V_{OFF,H} + V_{SAT})]}{(C_{LC,min} + C_S) \cdot (C_{GD,max} + C_{LC,max} + C_S)} \quad (5.41)$$

$$V_{OFF,L} = V_{OFF,H} - V_{SAT} - \Delta V_{COM,H} + \Delta V_{COM,L} \quad (5.42)$$

Considering the negative polarity, the gamma correction amount is

$$V_{GL}^- = V_{GL}^-(0) - \Delta V_{KB,DYN}^- + \Delta V_{KB,DYN}^- \text{ (Black)} \quad (5.43)$$

It should also be observed that the numerous commutations of the common electrode and Gate Lines, increase, in the case of Row Inversion, the power consumption. This is a clear limit of this approach for mobile applications. Besides, owing to the commutation of V_{COM} , techniques such as Column e Dot Inversion cannot be implemented. This scheme is however compatible with both Cap-on-Common and Cap-on-Gate structures.

As a numerical example, consider the typical values listed below:

$$V_{SAT} = 5 \text{ V}, V_1 = 18 \text{ V}, V_{OFF,H} = -8 \text{ V}, C_{GD,max} = 50 \text{ fF}, C_{LC,min} = 150 \text{ fF}, \\ C_{LC,max} = 300 \text{ fF}, C_S = 400 \text{ fF}$$

Using (5.40)–(5.42) we get the following voltages:

$$V_{COM,H} = 3.267 \text{ V}, V_{COM,L} = -2.661 \text{ V}, V_{OFF,L} = -13.928 \text{ V}$$

5.5.3 3-Level Driving

Like in the 2-Level approach, a constant V_{COM} is here employed (a high-voltage Source Driver is hence needed). This approach exploits the Cap-on-Gate panel structure, where the storage capacitor C_S is connected to the adjacent Gate Line, as depicted in Fig. 5.25, showing also the driving waveforms. V_1 is the TFT ON voltage, V_3 is the OFF voltage, and V_2 is called a pre-pulse voltage.

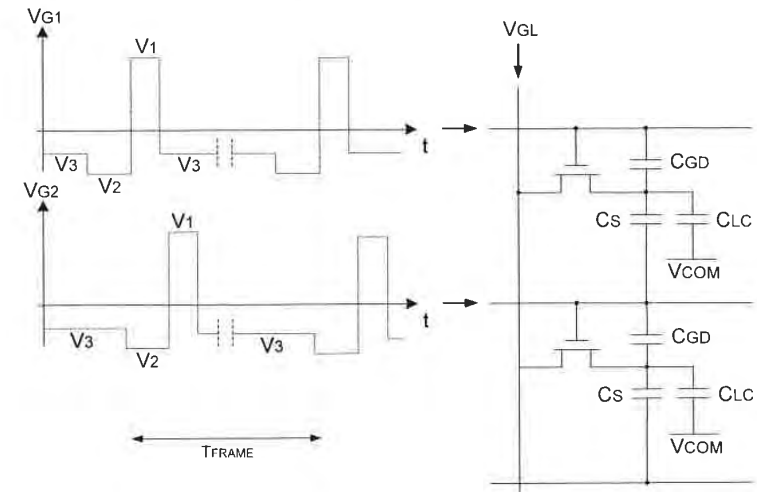


Fig. 5.25 Gate voltages in the case of 3-Level driving scheme

Separating the static and dynamic kickback contributions we get:

$$\Delta V_{KB,ST} = (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_{GD,max} + C_{LC,min} + C_S} - (V_3 - V_2) \cdot \frac{C_S}{C_{GD,min} + C_{LC,min} + C_S} \quad (5.44a)$$

$$\Delta V_{KB,DYN} = (V_3 - V_1) \cdot \frac{-C_{GD,max} \cdot \Delta C_{LC}}{(C_{GD,max} + C_S + C_{LC,min})(C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC})} \\ + (V_3 - V_2) \cdot \frac{C_S \cdot \Delta C_{LC}}{(C_{GD,min} + C_{LC,min} + C_S)(C_{GD,min} + C_{LC,min} + C_S + \Delta C_{LC})} \quad (5.44b)$$

After setting $\Delta V_{KB,ST} = 0$ we get

$$V_2 = V_3 + (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_S} \cdot \frac{C_{GD,min} + C_{LC,min} + C_S}{C_{GD,max} + C_{LC,min} + C_S} \\ \approx V_3 + (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_S} \quad (5.45)$$

Substituting (5.45) into (5.44b) we get the dynamic kickback component

$$\Delta V_{KB,DYN} \approx (V_3 - V_1) \cdot \frac{-C_{GD,max} \cdot \Delta C_{LC}}{C_{GD,max} + C_S + C_{LC,min}} \cdot \left(\frac{1}{C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC}} - \frac{1}{C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC}} \right) = 0 \quad (5.46)$$

As an important result, we see that with the aid of a pre-pulse voltage both static and dynamic kickback components are ideally eliminated, without requiring the use of Gamma correction. The Gamma curve can be therefore symmetrical, with an advantage both for circuit complexity and calibration task. Actually, due to the fact that C_{GD} is not constant, we cannot achieve a perfect cancellation of kickback. The driving voltages are illustrated in Fig. 5.26.

Assuming $V_1=18$ V, $V_3=-8$ V, $C_{GD,max}=50$ fF, $C_{GD,min}=30$ fF and $C_S=400$ fF, we get from (5.45) $V_2=-11.142$ V (and with the approximation -11.250 V).

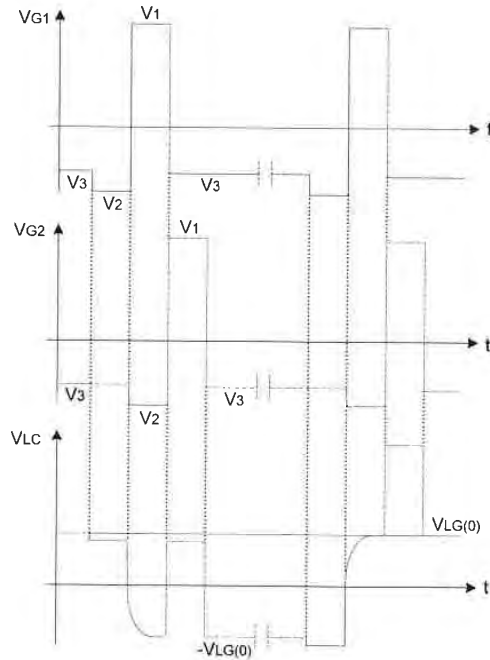


Fig. 5.26 Driving and pixel voltages in the case of 3-Level driving scheme

5.5.4 4-Level Driving

As for the 3-Level approach, also this driving scheme exploits the Cap-on-Gate structure. However, in this case the aim is to use a low-voltage source driver and a constant V_{COM} . The polarity inversion is here obtained by using four voltage levels in the gate line. These waveforms are shown in Fig. 5.27 (Frame Inversion is assumed).

Denoting as ΔV_{KB}^+ and ΔV_{KB}^- the kickback in a positive and negative frame polarity, respectively, and separating the static and dynamic components we get:

$$\Delta V_{KB,ST}^+ = (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_{GD,max} + C_S + C_{LC,min}} + (V_3 - V_4) \cdot \frac{C_S}{C_{GD,min} + C_S + C_{LC,min}} \quad (5.47a)$$

$$\Delta V_{KB,ST}^- = (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_{GD,max} + C_S + C_{LC,min}} + (V_3 - V_2) \cdot \frac{C_S}{C_{GD,min} + C_S + C_{LC,min}} \quad (5.47b)$$

$$\Delta V_{KB,DYN}^+ = (V_3 - V_1) \cdot \frac{-C_{GD,max} \cdot \Delta C_{LC}}{(C_{GD,max} + C_S + C_{LC,min})(C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC})} + (V_3 - V_4) \cdot \frac{C_S \cdot \Delta C_{LC}}{(C_{GD,min} + C_S + C_{LC,min})(C_{GD,min} + C_S + C_{LC,min} + \Delta C_{LC})} \quad (5.48a)$$

$$\Delta V_{KB,DYN}^- = (V_3 - V_1) \cdot \frac{-C_{GD,max} \cdot \Delta C_{LC}}{(C_{GD,max} + C_S + C_{LC,min})(C_{GD,max} + C_S + C_{LC,min} + \Delta C_{LC})} + (V_3 - V_2) \cdot \frac{C_S \cdot \Delta C_{LC}}{(C_{GD,min} + C_S + C_{LC,min})(C_{GD,min} + C_S + C_{LC,min} + \Delta C_{LC})} \quad (5.48b)$$

The pixel voltage is hence

$$V_{LC}^+ = V_{GL}^+ + \Delta V_{KB,ST}^+ + \Delta V_{KB,DYN}^+ - V_{COM} \quad (5.49a)$$

$$V_{LC}^- = V_{GL}^- + \Delta V_{KB,ST}^- + \Delta V_{KB,DYN}^- - V_{COM} \quad (5.49b)$$

where:

$$V_{GL}^+ = V_{GL}^+(0) + \Delta V_{GAMMA}^+, \quad V_{GL}^- = [V_{SAT} - V_{GL}^+(0)] + \Delta V_{GAMMA}^-, \quad V_{LC}^+ = -V_{LC}^-$$

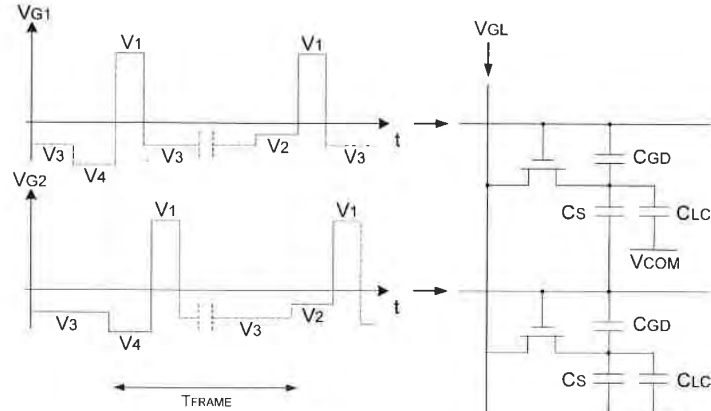


Fig. 5.27 Gate voltages in the case of 4-Level driving scheme (Frame Inversion is assumed)

Similarly to the previous case of V_{COM} modulation, in order to have a positive gamma voltage for both polarities we must set:

$$\Delta V_{GAMMA}^+ = -\Delta V_{KB,DYN}^+ \text{ and } \Delta V_{GAMMA}^- = -\Delta V_{KB,DYN}^- + \Delta V_{KB,DYN}^- (\text{Black})$$

$$\Delta V_{KB,ST}^+ = V_{COM} \text{ and } \Delta V_{KB,ST}^- = V_{COM} - V_{SAT} - |\Delta V_{KB,DYN}^- (\text{Black})|$$

After setting $V_{COM} = V_{SAT}/2$, we get the prepulse voltages:

$$\begin{aligned} V_2 &= V_3 + (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_S} \cdot \frac{C_{GD,min} + C_{LC,max} + C_S}{C_{GD,max} + C_{LC,max} + C_S} \\ &\quad + \frac{V_{SAT}}{2} \cdot \frac{C_{GD,min} + C_{LC,max} + C_S}{C_S} \\ &\approx V_3 + (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_S} + \frac{V_{SAT}}{2} \cdot \frac{C_{GD,min} + C_{LC,max} + C_S}{C_S} \end{aligned} \quad (5.50a)$$

$$\begin{aligned} V_4 &= V_3 + (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_S} \cdot \frac{C_{GD,min} + C_{LC,min} + C_S}{C_{GD,max} + C_{LC,min} + C_S} \\ &\quad - \frac{V_{SAT}}{2} \cdot \frac{C_{GD,min} + C_{LC,min} + C_S}{C_S} \\ &\approx V_3 + (V_3 - V_1) \cdot \frac{C_{GD,max}}{C_S} - \frac{V_{SAT}}{2} \cdot \frac{C_{GD,min} + C_{LC,min} + C_S}{C_S} \end{aligned} \quad (5.50b)$$

We show in Fig. 5.28 the driving and pixel voltages in the case of Frame Inversion.

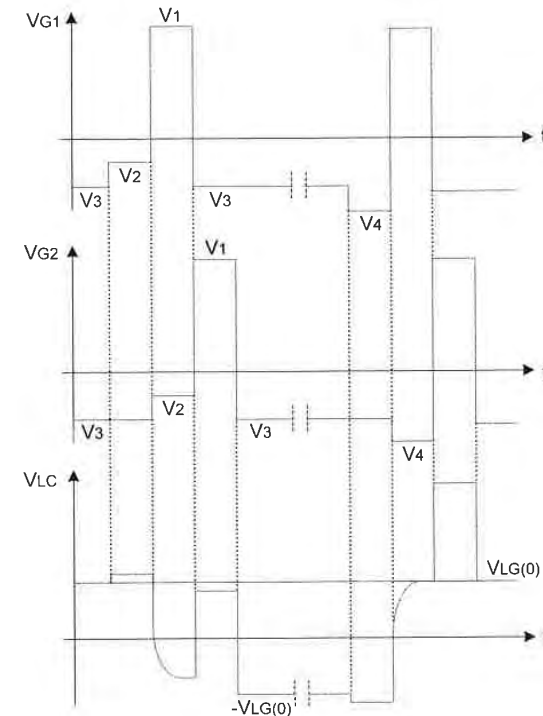


Fig. 5.28 Driving and pixel voltages in the case of 4-level driving scheme. Frame Inversion is considered

The advantage of the 4-level approach derives from the use of a low-voltage source driver and a constant V_{COM} , but a complex gamma correction to eliminate the kickback dynamic component. The approach is compatible only with Cap-on-Gate panels. Finally, either by increasing (for positive-polarity frames) or decreasing (for

negative-polarity frames) by the same amount all the ON pixels, it is possible to implement only those inversion methods in which the pixels of a given row have the same polarity, that is Row and Frame Inversion.

5.6 Concluding Remarks

The AMLCD industry has rapidly attracted a great interest by producers and originated a vast excitement in the consumers, so that now it has become an upstream dominant industry. As first investments were made in Japan and subsequently in Korea, Taiwan and recently in China, virtually all AMLCD panel fabrication lines are located in Asia. At the time of writing AMLCDs have penetrated completely the PC notebook market and by more than 50% that of PC monitors, while the TV sector represents the greatest potential of growth (in 2007, the number of LCD-TVs sold worldwide overcome that of CRT-TVs). This impressive and successful expansion has been possible thanks to the efforts of all divisions of the industry, from the manufacturers to component and equipment suppliers.

In this chapter we summarized the a-Si and poly-Si TFT electrical behaviors, we described the AMLCD panel structure and focused our attention on the dominant driving approaches. Conventional inversion polarity techniques were analyzed in detail with their related power consumption issues. Pre-emphasis and kickback compensation methods were addressed as well.

Based on these considerations, we can anticipate the first main differences between drivers for PMLCDs and AMLCDs:

- (1) The pixels do not respond to average voltages, frame response effect is absent and MLA techniques are no longer required;
- (2) Gray levels are generated by means of the sole source voltage (and not on both row and column voltages, as for PMLCDs), therefore an accurate Digital-to-Analog conversion is mandatory to obtain a source voltage from a digital RGB information. PWM techniques are no longer required;
- (3) Due to the higher data transfer rates, low-speed serial interfaces cannot be used because are too slow.

To conclude the discussion, we briefly describe some further methods that have been devised to improve AMLCD picture quality. They are based on the human vision perception system⁶ [YW2000, SAK2006, SL2007]. Of course, most of these techniques are meant for LCD TVs, but it is expected that they will be rapidly transferred to high-performance portable multimedia devices as well.

The first two approaches we treat are driving methods aimed to reduce the *motion blur* and in general to improve the quality of moving pictures [M2004].

⁶It is now recognized that optimized display performance can be only achieved by the understanding of the human color perception (see Appendix D), preferences, perceptible maximum contrast level (in general viewing circumstances and not only in dark rooms), and so on.

Studies on the human visual system show that the conventional display-and-hold driving method of LCDs, which maintains the previous frame image information for about 16.7 ms (=1/60 Hz) until the subsequent frame image, is the cause of *afterimage formation* on the retina and, in turn, the origin of motion blur perception [K2001, IYT2003]. This drawback is absent in CRTs with their inherent impulsive driving behaviour. Note that motion blur cannot be eliminated even if the LC response time approaches zero. This explains why, despite the use of progressively faster LCs and pre-emphasis techniques, we have now reached a limit in reducing motion blurring. The amount of afterimage on the human retina can be further reduced only by decreasing the frame time duration.

Fast Frame Rate (FFR) driving (i.e., the use of a frame frequency of 120 Hz) is at this purpose the most straightforward method [LSP2005, OIM2005], though there are issues to resolve in order to contrast the temperature increase in the data driver ICs without affecting the system cost.

Impulsive Driving is an attempt to recreate the CRT behavior through either *Black Data Insertion* [YKI2005, YTI2006] or *Backlight Blinking* [FNC2001, HST2001]. The former is based on the insertion of black data subframes between two consecutive video frames and is implemented via software. It takes advantage of the fast gray to black response of recent LC mixtures. For slower LCs the same effect can be simulated by pulsing the backlight. The technique is implemented via hardware through the backlight inverter and was proposed already in 1998 by a group of Japan Broadcasting Corporation (NHK) headed by Taichiro Kurita [KSY1998]. To be effective, residual light leakage during the backlight turning OFF must be minimized. As a main drawback, both approaches reduce the overall display luminance.

Research has been carried out to improve also contrast and color reproduction.

LCDs provide reduced contrast when displaying very bright or very dark images. **Dynamic gamma** can be used to overcome this drawback. In this approach the gamma curve is adjusted on a frame by frame basis depending on the image content.

Another promising approach for contrast improvement is the **Backlight Dimming**, [SHS2004, SKT2005, SM2006], in which the whole screen is divided into some areas and LEDs are assembled on each one with independent brightness control function. The backlight intensity of different areas is hence separately controlled based on input video signal levels. A 100 000:1 contrast ratio was reported using this method [SHS2004], which takes advantage of the LEDs fast response. This approach allows reducing the power dissipation of the backlight as well. The better LED color property⁷ will also improve color gamut in LCD TVs. To be completely exploited, this would require the introduction of an additional primary color (most probably Yellow) together with the traditional three RGB primaries (**Multi-Primary** color displays) [ELS2005, SL2007].

⁷A typical CCFL backlight will enable an LCD display to reproduce 60% of the colors that can be transmitted using an NTSC signal (see Appendix D). RGB LED backlight has the better color coverage spectrum (color gamut), which is about 110% NTSC (that of White LED is about 70–80% NTSC). Unfortunately, RGB LED backlight has the highest power consumption [CCC2007].

All these techniques are very important for the rapidly growing markets of LCD-TVs and home PC multi-media stations, where image quality is going to become a key factor. On the other side, the market pressure to reduce cost for mainstream desktop monitors (adopted massively by business companies for text and graphics usage) will cause a limited adoption of the above techniques into low-end displays. However, several improvements are foreseen also in the area of mobile AMLCD drivers. For example, Solomon Systech Ltd. (Hong-Kong), outlined the coming advances summarized in Table 5.3 already at the end of 2006.

Table 5.3 Some improvements expected in mobile LCD driver ICs [S2006a]

Features	Present	Coming advance
Resolution	QVGA	VGA
DAC	6-bit gray scale	8-bit gray scale
Motion	Pre-emphasis	Pre-emphasis and Black Data Insertion
Interface	Parallel and SPI	Custom parallel and high-speed serial*
Backlight	No control	LED Backlight Dimming
Contrast	No adjustment	Automatic adjustment according to ambient light level.
Touch panel	High-end feature	Popular feature

*High-speed serial interfaces are discussed in the next chapter.

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Chapter 6

Drivers for Active-Matrix LCDs

AMLCDs were originally conceived for *large*-screen full-motion applications, but the demand for multimedia handheld equipments with embedded high-quality (*small*-screen) displays has recently pushed their utilization also in this market segment.¹ Nevertheless, the driver circuits for these two LCD panel categories are subject to different trade-offs:

(1) Small-area LCDs are typically battery operated and are cost driven and area driven. Thus, the evolution of the driver architecture has been aimed to the reduction of the number of IC components ultimately converging to a monolithic IC (single chip, or *combo* chip), conceptually similar to that studied in Chapter 4 for PMLCDs.

(2) Owing to the greater number of rows and columns, large-area high-resolution panels cannot be driven by a single chip, which would require an unfeasible number of pins. Besides, large-area LCDs are not strictly focused on reducing power consumption and dimensions. Their main concern is on performance. Their driver design is hence characterized by a multichip architecture where the main functionalities are implemented by separate specialized ICs.

(3) As already discussed in the previous chapter, small-area AMLCDs can be realized either in a-Si and LTPS technologies, whereas large-area AMLCDs exploit only a-Si because of the inherent wide process variations of LTPS over the substrate area. Research is however performed to overcome this limitation.

(4) Column voltages of small-area AMLCDs must have a reduced voltage swing (of about 5 V and V_{COM} -switching is adopted) to employ thin-gate-oxide transistors in the implementation of the Source Drivers, choice driven by size and cost reduction. In contrast, Source Drivers for large-size AMLCDs require a higher voltage swing in the range of 16 V, because this supports the increasing number of gray levels required (10 bit per RGB color, at least). Therefore, 20-V thick-gate transistors are adopted. In this case V_{COM} is held constant to $V_{LCP}/2 (\approx 8 \text{ V})$ and V_{COM} -switching is not exploited. Dot Inversion or column and n-Line inversion is generally used in large-area AMLCDs for its better performance.

¹The demarcation between small-area and large-area AMLCDs can be roughly set to 5 in., despite this value is dependent on the application (e.g., mobile phones, smart phones, MP3/MP4 players, PDAs, etc.). This differentiation is becoming less and less evident with the increasing of the resolution.