

(51) Int. Cl. ⁵	Ident. Code	Internal Ref. No.	FI	Basis for Classification
G02F	1/1345	9018-2K		
	1/133 550	7820-2K		

Examination Request: Not Yet Total No. of Claims: 5 (Total 12 pages)

(21) Application No.	JP H3-147084	(71) Applicant	000005108 Hitachi, Ltd. 4-6 Kanda Surugadai, Chiyoda-ku, Tokyo-to
(22) Date of Filing	June 19, 1991 (Heisei 3)	(72) Inventor	Hideaki Yamamoto c/o Hitachi, Ltd. 3300 Hayano, Mobara-shi, Chiba-ken
		(72) Inventor	Toshiyuki Komiza c/o Hitachi, Ltd. 3300 Hayano, Mobara-shi, Chiba-ken
		(72) Inventor	Takao Tanabe c/o Hitachi, Ltd. 3300 Hayano, Mobara-shi, Chiba-ken
		(74) Agent	Junnosuke Nakamura, Patent Attorney (and one other)

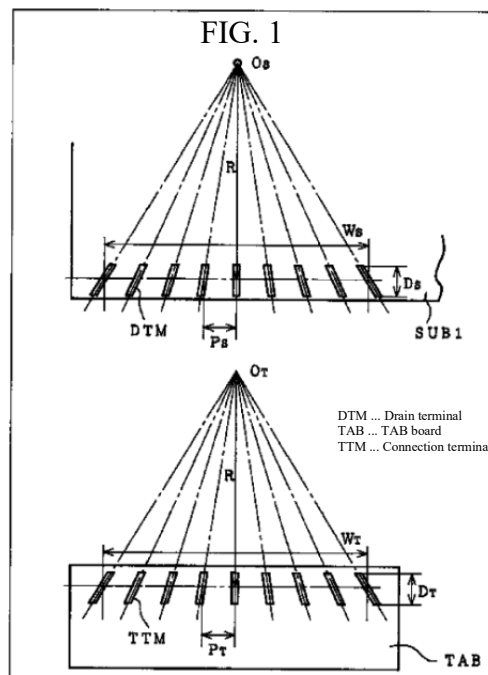
Continued on Last Page

(54) [Title of Invention] LIQUID CRYSTAL DISPLAY BOARD, LIQUID CRYSTAL DISPLAY PANEL, AND LIQUID CRYSTAL DISPLAY DEVICE

(57) [Abstract]

[Purpose] To prevent connection defects between a connection terminal of a TAB board and a signal line terminal from occurring.

[Configuration] A drain terminal DTM is divided into a plurality of drain terminal DTM areas, an extension line of each drain terminal DTM of the drain terminal DTM area converges to one point O_s , and extension lines of each connection terminal TTM of a connection terminal TTM area formed on a TAB board TAB and connected to the drain terminal DTM area converge to one point O_T .



[Scope of Patent Claims]

[Claim 1] A liquid crystal display board, wherein extension lines of each signal line terminal in a signal line terminal area converge at one point.

[Claim 2] A liquid crystal display panel, wherein the extension line of each signal line terminal of the signal line terminal area has a liquid crystal display board converging at one point.

[Claim 3] A liquid crystal display device, comprising: a liquid crystal display panel having a liquid crystal display board in which an extension line of each signal line terminal of a signal line terminal area converge at one point; an image signal drive circuit for giving an image signal to the liquid crystal display panel; a scan circuit for giving a scan signal to the liquid crystal display panel; and a control circuit for giving information for the liquid crystal display panel to the image signal drive circuit and the scan circuit.

[Claim 4] The liquid crystal display device according to claim 3, wherein the circuit elements of the image signal drive circuit and the scan circuit are mounted on the circuit board, and the extension lines of each connection terminal in the connection terminal area formed on the circuit board and connected to the signal line terminal area converge at one point.

[Claim 5] The liquid crystal display device according to claim 4, wherein a length of the connection terminal is shorter than a length of the signal line terminal.

[Detailed Description of Invention]

[0001]

[Industrial Applicability] The present invention relates to a liquid crystal display board, a liquid crystal display panel, and a liquid crystal display device, particularly an active matrix liquid crystal display board using a thin film transistor or the like, a liquid crystal display panel, and a liquid crystal display device.

[0002]

[Conventional Art] An active matrix liquid crystal display device is provided with a non-linear element (switching element) corresponding to each of a plurality of pixel electrodes arranged in a matrix. The liquid crystal in each pixel is theoretically constantly driven (1.0 duty ratio), and thus the active form has good contrast compared to the so-called simple matrix form, which uses a time-division drive method, and is becoming an indispensable technology, particularly in color liquid crystal display devices. Thin film transistors (TFTs) are typical switching elements.

[0003] FIG. 15 is a schematic exploded view illustrating a conventional active matrix liquid crystal display device (Nikkei Electronics No. 495 (1990), pages 122 to 136). In the figure, SUB1 is a lower transparent glass board, GL is a scan signal line formed on the lower transparent glass board SUB1, DL is a video signal line formed via an insulating film on the scan signal line GL, GTM1 is a gate terminal connected to the scan signal line GL, DTM1 is a drain terminal connected to the video signal line DL, TAB is a TAB board, DCE is a drive circuit element mounted on the TAB board TAB, CTM is a connection terminal connected to the drive circuit element DCE, TTM1 is a connection terminal connected to the drive circuit element DCE, the pitch P_T and the length D_T of the connection terminal TTM1 is equal to the pitch P_S and length D_S of the drain terminal

DMT1, the pitches P_T and P_S are 0.2 mm, the lengths D_T and D_S are 2 to 3 mm, furthermore, the number of connection terminals TTM1 is 160, and the distance W_T between connection terminals TTM1 at both ends is 32 mm. Then, the connection terminal TTM1 is connected to the drain terminal DTM1 via an anisotropic conductive film.

[0004]

[Problem to Be Solved by Invention] In such a liquid crystal display device, because the TAB board TAB is composed of an organic film such as a polyimide resin film, it is easy to expand and contract in the manufacturing process of the TAB board TAB, and the error of the distance W_T is ± 0.1 mm or more, and thus the pitches of the connection terminal TTM1 and the drain terminal DTM1 do not match, and a connection defect between the connection terminal TTM1 and the drain terminal DTM1 occurs.

[0005] The present invention has been configured to solve the problems described above, and an object thereof is to provide a liquid crystal display board, a liquid crystal display panel, and a liquid crystal display device, wherein connection defects between connection terminals of circuit boards and signal line terminals do not occur.

[0006]

[Means for Solving Problem] In order to achieve this object, in the present invention, extension lines of each signal line terminal in a signal line terminal area are converged to one point on a liquid crystal display board.

[0007] Furthermore, the liquid crystal display board is provided in which the extension lines of each signal line terminal of the signal line terminal area are converged at one point in a liquid crystal display panel.

[0008] Furthermore, the liquid crystal display device is provided with: a liquid crystal display panel having a liquid crystal display board in which an extension line of each signal line terminal of a signal line terminal area converge at one point; an image signal drive circuit for giving an image signal to the liquid crystal display panel; a scan circuit for giving a scan signal to the liquid crystal display panel; and a control circuit for giving information for the liquid crystal display panel to the image signal drive circuit and the scan circuit.

[0009] In this case, the circuit elements of the image signal drive circuit and the scan circuit are mounted on the circuit board, and the extension line of each connection terminal in the connection terminal area formed on the circuit board and connected to the signal line terminal area converge at one point.

[0010] In this case, the length of the connection terminal is made shorter than the length of the signal line terminal.

[0011]

[Effect] In the liquid crystal display board, the liquid crystal display panel, and the liquid crystal display device, even when an error in the distance between the connection terminals at both ends occurs, all of the connection terminals can be positioned on the signal line terminal when the circuit board is shifted in the direction of the signal line connected to the signal line terminal when the signal line terminal and the connection terminal are connected.

[0012] Furthermore, when the length of the connection terminal is shorter than the length of the signal line terminal,

the end portion of the circuit board does not go atop the protective film even when the circuit board is shifted toward the signal line side.

[0013]

[Examples] The configuration of the present invention will be described below along with examples in which the present invention is applied to a liquid crystal display board and liquid crystal display panel of an active matrix color liquid crystal display device.

[0014] Note that in all figures for describing examples, those having the same function are labelled using the same reference numerals, and repeated descriptions thereof are omitted.

[0015] FIG. 2 is a plan view illustrating one pixel and the surroundings of an active matrix color liquid crystal display device to which the present invention is applied, FIG. 3 is a diagram illustrating a cross section along a cut line 3-3 in FIG. 2 and a cross section near a seal portion of a display panel, and FIG. 4 is a cross section view along a cut line 4-4 in FIG. 2. Furthermore, FIG. 7 (main plan view) illustrates a plan view when a plurality of pixels illustrated in FIG. 2 are arranged.

[0016] (Pixel arrangement) As illustrated in FIG. 2, each pixel is arranged within an intersection region (within a region surrounded by four signal lines) between two adjacent scan signal lines (gate signal lines or horizontal signal lines) GL and two adjacent video signal lines (drain signal lines or vertical signal lines) DL. Each pixel includes a thin film transistor TFT, a transparent pixel electrode ITO1, and a holding capacitance element Cadd. The scan signal lines GL extend in the column direction and are disposed in a plurality of row directions. The video signal lines DL extend in the row direction and are disposed in a plurality of column directions.

[0017] (Overall display unit cross-sectional structure) As illustrated in FIG. 3, a thin film transistor TFT and a transparent pixel electrode ITO1 are formed on the side of a lower transparent glass board SUB1 based on a liquid crystal LC, and a color filter FIL and a light-shielding film BM that forms a black matrix pattern for light-shielding are formed on the side of an upper transparent glass board SUB2. The lower transparent glass board SUB1 is configured to be, for example, about 1.1 mm thick. Furthermore, a silicon oxide film SIO formed by a dip treatment or the like is provided on both surfaces of the transparent glass boards SUB1 and SUB2. Therefore, even when there are sharp scratches on the surfaces of the transparent glass boards SUB1 and SUB2, the sharp scratches can be covered by the silicon oxide film SIO, and thus it is possible to effectively prevent the scan signal line GL and the color filter FIL from being damaged.

[0018] The central part of FIG. 3 illustrates a cross section of one pixel portion, but the left side illustrates a cross section of a left edge portion of the transparent glass boards SUB1 and SUB2 where an external pull-out wiring exists, and the right side illustrates a cross section of a right edge portion of the transparent glass boards SUB1 and SUB2 where an external pull-out wiring does not exist.

[0019] Sealants SL illustrated on the left and right sides of FIG. 3 are configured to encapsulate the liquid crystal LC and are formed along the entire periphery of the transparent glass boards SUB1 and SUB2 excluding the liquid crystal seal entrance (not illustrated). The sealants SL are formed

from, for example, epoxy resins.

[0020] A common transparent pixel electrode ITO2 on the upper transparent glass board SUB2 side is connected to an external pull-out wiring formed on the lower transparent glass board SUB1 side by a silver paste material SIL in at least one place. This external pull-out wiring is formed by the same manufacturing process as each of a gate electrode GT, a source electrode SD1, and a drain electrode SD2.

10 [0021] The respective layers of oriented films ORI1, ORI2, a transparent pixel electrode ITO1, a common transparent pixel electrode ITO2, protective films PSV1, PSV2, and an insulating film GI are formed inside the sealant SL. Polarizing plates POL1 and POL2 are formed on the outer surface of the lower transparent glass board SUB1 and the upper transparent glass board SUB2, respectively.

[0022] The liquid crystal LC is sealed between the lower oriented film ORI1 and the upper oriented film ORI2 for setting the orientation of a liquid crystal molecule and is sealed by the sealant SL.

[0023] The lower oriented film ORI1 is formed on the upper part of the protective film PSV1 on the lower transparent glass board SUB1 side.

20 [0024] A light-shielding film BM, the color filter FIL, the protective film PSV2, the common transparent pixel electrode ITO2 (COM), and the upper oriented film ORI2 are sequentially laminated on the surface of the upper transparent glass board SUB2 (liquid crystal LC side).

[0025] This liquid crystal display device is assembled by separately forming respective layers on the lower transparent glass board SUB1 side and the upper transparent glass board SUB2 side, then superimposing the upper and lower transparent glass boards SUB1 and SUB2, and enclosing the liquid crystal LC between them.

30 [0026] (Thin film transistor TFT) The thin film transistor TFT operates such that when a positive bias is applied to the gate electrode GT, the channel resistance between the source and the drain decreases, and when the bias is set to zero, the channel resistance increases.

[0027] The thin film transistor TFT of each pixel is divided into two (plurality) within the pixel and is composed of thin film transistors (split thin film transistors) TFT1 and TFT2. Each of the thin film transistors TFT1 and TFT2 is configured to be substantially the same size (the same channel length and width). Each of the divided thin film transistors TFT1 and TFT2 is mainly composed of a gate electrode GT, a gate insulating film GI, an i-type semiconductor layer AS composed of an amorphous silicon (Si) having an i-type (intrinsic, intrinsic, not doped with conductive impurities), and a pair of a source electrode SD1 and a drain electrode SD2. Note that it should be understood that the source drain is originally determined by the bias polarity therebetween, and in the circuit of this liquid crystal display device, the polarity is inverted during operation, and thus the source drain is replaced during operation. However, in the following description, one is expressed as a source and the other as a drain for convenience.

50 [0028] (Gate electrode GT) As illustrated in detail in FIG. 8 (plan view depicting only the second conductive film g2 and

the i-type semiconductor layer AS in FIG. 2), the gate electrode GT is configured to protrude in a vertical direction (upward in FIG. 2 and FIG. 8) from the scan signal line GL (branched into a T shape). The gate electrode GT is configured to protrude to the respective forming regions of the thin film transistors TFT1 and TFT2. Each gate electrode GT of the thin film transistors TFT1 and TFT2 is integrally configured (as a common gate electrode) and is continuously formed on the scan signal line GL. The gate electrode GT is constituted of a second conductive film g2 of a single layer. The second conductive film g2 is formed using, for example, an aluminum film formed by sputtering at a film thickness of about 1,000 to 5,500 Å. Furthermore, an anodized aluminum oxide film AOF is provided on the gate electrode GT.

[0029] As illustrated in FIG. 2, FIG. 3, and FIG. 8, the gate electrode GT is formed to be larger, so as to completely cover the i-type semiconductor layer AS (when viewed from below). Therefore, when a backlight BL such as a fluorescent lamp or the like is attached below the lower transparent glass board SUB1, the gate electrode GT composed of opaque aluminum is shadowed, and the i-type semiconductor layer AS does not receive backlight light, making conductive phenomena due to light irradiation, that is, off-characteristic deterioration of the thin film transistor TFT, occur less readily. Note that the original size of the gate electrode GT has a minimum required width between the source electrode SD1 and the drain electrode SD2 (including an alignment margin between the gate electrode GT and the source electrode SD1 and the drain electrode SD2), and the depth length thereof for determining the channel width W is determined by the ratio of the distance (channel length) L between the source electrode SD1 and the drain electrode SD2, that is, the factor W/L for determining the mutual conductance gm.

[0030] The size of the gate electrode GT in the liquid crystal display device is made to be larger than the original size described above.

[0031] (Scan signal line GL) The scan signal line GL is configured by a second conductive film g2. The second conductive film g2 of the scan signal line GL is formed by the same manufacturing process as the second conductive film g2 of the gate electrode GT and is configured integrally. Furthermore, an anodized aluminum oxide film AOF is provided on the scan signal line GL.

[0032] (Insulating film GI) The insulating film GI is used as the respective gate insulating film of the thin film transistors TFT1 and TFT2. The insulating film GI is formed on the upper layer of the gate electrode GT and the scan signal line GL. Insulating film GI is formed using, for example, a silicon nitride film formed by plasma CVD at a film thickness of about 3,000 Å.

[0033] (i-type semiconductor layer AS) The i-type semiconductor layer AS is used as a channel forming region of each of the plurality of divided thin film transistors TFT1 and TFT2, as illustrated in FIG. 8. The i-type semiconductor layer AS is formed by an amorphous silicon film or a polycrystalline silicon film, and is formed at a film thickness

of about 1,800 Å.

[0034] The i-type semiconductor layer AS is formed continuously in the same plasma CVD device and without being exposed to the outside from the plasma CVD device, by changing the component of the supplied gas and forming an insulating film GI used as a gate insulating film composed of Si₃N₄. Furthermore, a N(+)-type semiconductor layer d0 (FIG. 3) doped with 2.5% phosphorus (P) for ohmic contact is similarly formed continuously to a thickness of about 400 Å. Thereafter, the lower transparent glass board SUB1 is taken out from the CVD device, and the N(+)-type semiconductor layer d0 and the i-type semiconductor layer AS are patterned into independent islands as illustrated in FIG. 2, FIG. 3, and FIG. 8 by photographic processing technology.

[0035] As illustrated in detail in FIG. 2 and FIG. 8, the i-type semiconductor layer AS is also provided between both intersection portions (crossover portions) of the scan signal line GL and the video signal line DL. The i-type semiconductor layer AS at the intersection is configured to reduce short-circuiting between the scan signal line GL and the video signal line DL at the intersection.

[0036] (Source electrode SD1, drain electrode SD2) The respective source electrode SD1 and drain electrode SD2 of the plurality of divided thin film transistors TFT1 and TFT2 are provided separately on the i-type semiconductor layer AS, as illustrated in detail in FIG. 2, FIG. 3, and FIG. 9 (planar views depicting only first to third conductive films d1 to d3 in FIG. 2).

[0037] The source electrode SD1 and the drain electrode SD2 are each configured by sequentially overlapping the first conductive film d1, the second conductive film d2, and the third conductive film d3 from a lower layer side in contact with the N(+)-type semiconductor layer d0. The first conductive film d1, the second conductive film d2, and the third conductive film d3 of the source electrode SD1 are formed in the same manufacturing process as the first conductive film d1, the second conductive film d2, and the third conductive film d3 of the drain electrode SD2.

[0038] The first conductive film d1 is formed using a chromium film formed by sputtering at a film thickness of 500 to 1,000 Å (a film thickness of about 600 Å in the liquid crystal display device). When a chromium film is formed thick, the stress increases, so the chromium film is formed within a range not exceeding the film thickness of about 2000 Å. The chromium film has good contact with the N(+)-type semiconductor layer d0. The chromium film constitutes a so-called barrier layer that prevents aluminum of the second conductive film d2, which will be described later, from spreading to the N(+)-type semiconductor layer d0. In addition to the chromium film, the first conductive film d1 may be formed from a high melting point metal (Mo, Ti, Ta, W) film or a high melting point metal silicide (MoSi₂, TiSi₂, TaSi₂, WSi₂) film.

[0039] After the first conductive film d1 is patterned by photographic processing, the N(+)-type semiconductor layer d0 is removed using the same photographic processing mask

or using the first conductive film d1 as a mask. In other words, a portion of the N(+)-type semiconductor layer d0 remaining on the i-type semiconductor layer AS other than the first conductive film d1 is removed by self-alignment. At this time, the N(+)-type semiconductor layer d0 is etched so that all of its thickness is removed, and thus the i-type semiconductor layer AS is also etched slightly on the surface portion thereof, but the extent thereof can be controlled by the etch time.

[0040] Thereafter, the second conductive film d2 is formed by sputtering aluminum to a film thickness of 3,000 to 5,500 Å (a film thickness of about 3,500 Å in this liquid crystal display device). The aluminum film is less stressed than the chromium film and can be formed to a thick film thickness, and is configured to reduce the resistance values of the source electrode SD1, the drain electrode SD2, and the video signal line DL. The second conductive film d2 may be formed by an aluminum film containing silicon or copper (Cu) as an additive in addition to an aluminum film.

[0041] After patterning of the second conductive film d2 using a photographic processing technique, the third conductive film d3 is formed. This third conductive film d3 is composed of a transparent conductive film (Indium-Tin-Oxide ITO: NESA film) formed by sputtering, and is formed at a film thickness of 1,000 to 2,000 Å (a film thickness of about 1,200 Å in the liquid crystal display device). The third conductive film d3 constitutes the source electrode SD1, the drain electrode SD2, and the video signal line DL and also constitutes the transparent pixel electrode ITO1.

[0042] The first conductive film d1 of the source electrode SD1 and the first conductive film d1 of the drain electrode SD2 respectively penetrate inwardly (into the channel region) compared to the second conductive film d2 and the third conductive film d3 of the upper layer. In other words, the first conductive film d1 in these portions is configured to define a channel length L of the thin film transistor TFT independent of the second conductive film d2 and the third conductive film d3.

[0043] The source electrode SD1 is connected to the transparent pixel electrode ITO1. The source electrode SD1 is configured along a stepped shape of the i-type semiconductor layer AS (a stepped corresponding to a film thickness obtained by adding a film thickness of the first conductive film g1, a film thickness of the N(+)-type semiconductor layer d0, and a film thickness of the i-type semiconductor layer AS). Specifically, the source electrode SD1 is composed of a first conductive film d1 formed along a stepped shape of the i-type semiconductor layer AS, a second conductive film d2 formed on an upper part of the first conductive film d1 having a side connected to the transparent pixel electrode ITO1 at a smaller size than that, and a third conductive film d3 connected to the first conductive film d1 exposed from the second conductive film d2. The second conductive film d2 of the source electrode SD1 is configured to overcome the i-type semiconductor layer AS because the chromium film of the first conductive film d1 cannot be formed to be thick due to increased stress and cannot overcome the stepped shape of the i-type semiconductor layer AS. In other words, the second conductive film d2 is formed to be thick to improve step coverage. The second conductive film d2 can be formed to be thick, which contributes greatly to the reduction of the resistance value of the source electrode SD1 (the same is true for the drain electrode SD2 and the video signal line DL).

The third conductive film d3 cannot go over the stepped shape caused by the i-type semiconductor layer AS of the second conductive film d2, and thus the structure is configured to connect to the exposed first conductive film d1 by reducing the size of the second conductive film d2. Not only are the first conductive film d1 and the third conductive film d3 excellent in adhesion, but the difference in stepped shape of the connection portion between the two is small, and thus the source electrode SD1 and the transparent pixel electrode ITO1 can be reliably connected.

[0044] (Transparent pixel electrode ITO1) The transparent pixel electrode ITO1 constitutes one of the pixel electrodes of the liquid crystal display unit.

[0045] The transparent pixel electrode ITO1 is connected to the source electrode SD1 of the thin film transistor TFT1 and the source electrode SD1 of the thin film transistor TFT2. Therefore, when a defect occurs in one of the thin film transistors TFT1 and TFT2, for example, the thin film transistor TFT1, the thin film transistor TFT1 and the video signal line DL are separated by laser light or the like in the manufacturing process, and when the thin film transistor TFT1 and the transparent pixel electrode ITO1 are cut apart, there are substantially no point defects or line defects, and even the probability of a point defect occurring in the two thin film transistors TFT1 and TFT2 at the same time is extremely small.

[0046] (Protective film PSV1) The protective film PSV1 is provided on the thin film transistor TFT and the transparent pixel electrode ITO1. The protective film PSV1 is mainly formed to protect the thin film transistor TFT from moisture and the like and is made of a highly transparent film having good moisture resistance. The protective film PSV1 is formed from, for example, a silicon oxide film or a silicon nitride film formed in a plasma CVD device, and is formed at a film thickness of about 8,000 Å.

[0047] (Gate terminal GTM, drain terminal DTM) As illustrated in FIG. 5, a gate terminal GTM is configured from a first conductive film g1 and a third conductive film d3.

[0048] Furthermore, as illustrated in FIG. 6, a drain terminal DTM is configured from a first conductive film g1 and a third conductive film d3.

[0049] The first conductive film g1 uses, for example, a chromium (Cr) film formed by sputtering and is formed at a film thickness of about 1,000 Å.

[0050] As illustrated in FIG. 1 and FIG. 14, the gate terminal GTM and the drain terminal DTM are divided into a plurality of signal line terminal areas, and for example, the extension lines of each drain terminal DTM in the drain terminal DTM area converge to a single point Os. Furthermore, the respective extension lines of the connection terminal TTM of the connection terminal TTM area formed in the TAB board TAB and connected to the drain terminal DTM area converge to one point Ot. Therefore, even were an error to occur in the distance W_T between the connection terminals TTM at both ends, when the TAB board TAB is shifted in the direction of the video signal line DL connected to the drain terminal DTM when connecting the drain terminal DTM and the connection terminal DTM, all the connection terminals TTM can be positioned on the drain

terminal DTM, and thus no connection defect between the connection terminal TTM and the drain terminal DTM occurs. In this case, when defining the distance between the drain terminals DTM at both ends of the drain terminal DTM area as W_S and the distance between the points O_S and O_T and the center of the drain terminal DTM and the center of the connection terminal TTM of the drain terminal DTM area and the connection terminal TTM area as R , all the connection terminals TTM can be positioned on the drain terminal DTM by shifting the TAB board TAB as long as the W_T/W_S is within the range indicated by the following formula.

$$[0051] \quad 1 - (D_S - D_T)/2R < W_T/W_S < 1 + (D_S - D_T)/2R$$

For example, when the length D_T is 2 mm, the length D_S is 3 mm, the distance R is 10 mm, and the distance W_S is 32 mm, when the error of the distance W_T is within ± 0.16 mm, all the connection terminals TTM can be positioned on the drain terminal DTM by shifting the TAB board TAB.

[0052] Furthermore, because the length D_T is shorter than the length D_S , the end portion of the TAB board TAB does not go atop the protective film PSV1 even when the TAB board TAB is shifted to the video signal line DL side, and thus the drain terminal DTM and the connection terminal TTM can be reliably connected.

[0053] Note that the configuration of the other drain terminal DTM area portion and the gate terminal GTM area portion is also the same as the configuration of the drain terminal DTM area portion described above. (Light-shielding film BM) On the upper transparent glass board SUB2 side, a light-shielding film BM is provided so that external light (light from above in FIG. 3) does not become incident on the i-type semiconductor layer AS used as a channel forming region, and the light-shielding film BM has a pattern as illustrated in hatching in FIG. 10. Note that FIG. 10 is a plan view illustrating only the third conductive film d3 composed of the ITO film, the color filter FIL, and the light-shielding film BM in FIG. 2. The light-shielding film BM is formed from, for example, an aluminum film, a chromium film having high light shielding, or the like, and in this liquid crystal display device, a chromium film is formed by sputtering to a film thickness of about 1,300 Å.

[0054] Therefore, the i-type semiconductor layer AS of the thin film transistors TFT1 and TFT2 is sandwiched by the light-shielding film BM above and below and the large gate electrode GT, and the portion thereof is prevented from being hit by external natural light or backlight light. As illustrated in the hatched portion in FIG. 10, the light-shielding film BM is formed around the pixels, that is, the light-shielding film BM is formed in a grid shape (black matrix), and this grid divides an effective display region of one pixel. Therefore, the outline of each pixel is clearly defined by the light-shielding film BM, and contrast is improved. That is, the light-shielding film BM has two functions, namely light shielding for the i-type semiconductor layer AS, and a black matrix.

[0055] Furthermore, a portion facing the edge portion on the root side of the rubbing direction of the transparent pixel electrode ITO1 (the lower right portion of FIG. 2) is blocked by the light-shielding film BM, and thus even when a

domain occurs in the above portion, the domain is not visible, and thus display characteristics do not degrade.

[0056] Note that the backlight may also be attached to the upper transparent glass board SUB2 side, and the lower transparent glass board SUB1 may be used as the observation side (external exposed side).

[0057] (Common transparent pixel electrode ITO2) The common transparent pixel electrode ITO2 faces the transparent pixel electrode ITO1 provided for each pixel on the lower transparent glass board SUB1 side, and the optical state of the liquid crystal LC changes in response to a potential difference (electric field) between each pixel electrode ITO1 and the common transparent pixel electrode ITO2. A common voltage V_{com} is configured to be applied to the common transparent pixel electrode ITO2. The common voltage V_{com} is an intermediate potential between a low-level driving voltage V_{dmin} applied to the video signal line DL and a high-level driving voltage V_{dmax} .

[0058] (Color filter FIL) The color filter FIL is configured by coloring a dyeing substrate formed from a resin material such as acrylic resin. The color filter FIL is formed in a stripe shape at a position facing the pixel (FIG. 11) and dyed separately (FIG. 11 depicts only the third conductive film layer d3, the light-shielding film BM, and the color filter FIL of FIG. 7, and the color filter FILs of B, R, and G are hatched 45°, 135°, and perpendicular, respectively). As illustrated in FIG. 10, the color filter FIL is formed to be large enough to cover all of the transparent pixel electrode ITO1, and the light-shielding film BM is formed inside the periphery of the transparent pixel electrode ITO1 so as to overlap the edge portion of the color filter FIL and the transparent pixel electrode ITO1.

[0059] The color filter FIL can be formed as follows. First, a dyeing substrate is formed on the surface of the upper transparent glass board SUB2, and the dyeing substrate other than in the red filter forming region is removed by a photolithography technique. Thereafter, the dyeing substrate is dyed with a red dye and subjected to a fixation treatment to form a red filter R. Next, a green filter G and a blue filter B are sequentially formed by applying the same process.

[0060] (Protective film PSV2) The protective film PSV2 is provided to prevent dyes having their color filters FIL dyed different colors from leaking into the liquid crystal LC. The protective film PSV2 is formed from, for example, a transparent resin material such as acrylic resin or epoxy resin.

[0061] A wiring diagram of an equivalent circuit and a peripheral circuit of a display matrix part (overall equivalent circuit of the display device) is illustrated in FIG. 12. Although this drawing is a circuit diagram, it is drawn corresponding to an actual geometric arrangement. AR is a matrix array in which a plurality of pixels are disposed in two dimensions.

[0062] In the drawing, X means a video signal line DL, and the indices G, B, and R are added corresponding to green, blue, and red pixels, respectively. Y means a scan signal line GL, and indices 1, 2, 3, ..., and end are added according to

the order of scanning timing.

[0063] The video signal line X (index omitted) is alternately connected to an upper (or odd) video signal drive circuit He and a lower (or even) video signal drive circuit Ho.

[0064] The scan signal line Y (index omitted) is connected to the vertical scan circuit V.

[0065] SUP is a circuit including a power supply circuit for obtaining a plurality of divided and stabilized voltage sources from one voltage source and a circuit for exchanging information for a CRT (cathode ray tube) from a host (higher order processing unit) with information for a TFT liquid crystal display device.

[0066] (Structure of holding capacitance element Cadd) The transparent pixel electrode ITO1 is formed so as to overlap a neighboring scan signal line GL at an end portion opposite an end portion connected to the thin film transistor TFT. This superimposition, as is clear in light of FIG. 4, constitutes a holding capacitance element (electrostatic capacitance element) Cadd in which the transparent pixel electrode ITO1 is one electrode PL2 and a neighboring scan signal line GL is the other electrode PL1. The dielectric film of the holding capacitance element Cadd is composed of an insulating film GI and an anodized oxide film AOF used as a gate insulating film of a thin film transistor TFT.

[0067] As is clear in light of FIG. 8, the holding capacitance element Cadd is formed on a portion of the scan signal line GL where the width of the second conductive film g2 is expanded. Note that the second conductive film g2 of the portion that intersects the video signal line DL is made thinner to reduce the probability of a short circuit with the video signal line DL.

[0068] Similarly to the source electrode SD1, an island region configured from the first conductive film d1 and the second conductive film d2 is provided in a portion between the transparent pixel electrode ITO1 and the electrode PL1 superimposed to constitute the holding capacitance element Cadd, such that the transparent pixel electrode ITO1 is not disconnected upon going over the stepped shape. This island region is configured as small as possible so as not to reduce the area (opening ratio) of the transparent pixel electrode ITO1. (Equivalent circuit of holding capacitance element Cadd and operation thereof) An equivalent circuit of the pixel illustrated in FIG. 2 is illustrated in FIG. 13. In FIG. 13, Cgs is a parasitic capacitance formed between the gate electrode GT of the thin film transistor TFT and the source electrode SD1. The dielectric film of the parasitic capacitance Cgs is an insulating film GI. Cpix is a liquid crystal capacitance formed between the transparent pixel electrode ITO1 (PIX) and the common transparent pixel electrode ITO2 (COM). The dielectric film of the liquid crystal capacity Cpix is the liquid crystal LC, the protective film PSV1, and the oriented films ORI1 and ORI2. Vlc is a midpoint potential.

[0069] The holding capacitance element Cadd acts to reduce the effect of the gate potential change ΔV_g on the midpoint potential (pixel electrode potential) Vlc when the thin film transistor TFT is switched. This can be expressed by the following formula.

[0070]

$$\Delta V_{lc} = \{C_{gs}/(C_{gs} + C_{add} + C_{pix})\} \times \Delta V_g$$

Here, ΔV_{lc} represents change in the midpoint potential due to ΔV_g . This change in ΔV_{lc} causes a DC component to be applied to the liquid crystal LC, but the larger the holding capacitance Cadd, the smaller the value thereof can be made. Furthermore, the holding capacitance element Cadd also has the effect of extending the discharge time, and accumulates video information for a long time after the thin film transistor TFT is turned off. Reducing the DC component applied to the liquid crystal LC improves the life of the liquid crystal LC and reduces a so-called seizure that remains in the previous image when the liquid crystal display screen is switched.

[0071] As described above, the larger the gate electrode GT is so as to completely cover the i-type semiconductor layer AS, the greater the overlap area with the source electrode SD1 and the drain electrode SD2, and thus the larger the parasitic capacitance Cgs, and the more susceptible the midpoint potential Vlc is to the gate (scan) signal Vg. However, this disadvantage can also be eliminated by providing a holding capacitance element Cadd.

[0072] The holding capacitance of the holding capacitance element Cadd is set to a value of about 4 to 8 times ($4 \cdot C_{pix} < C_{add} < 8 \cdot C_{pix}$) the liquid crystal capacity Cpix and 8 to 32 times ($8 \cdot C_{gs} < C_{add} < 32 \cdot C_{gs}$) the parasitic capacitance Cgs, based on writing characteristics of the pixels.

[0073] (Wiring method of holding capacitance element Cadd electrode wire) The first stage scan signal line GL (Y_0) used only as the holding capacitance electrode line is connected to the common transparent pixel electrode ITO2 (Vcom), as illustrated in FIG. 12. As illustrated in FIG. 3, the common transparent pixel electrode ITO2 is connected to external pull-out wiring by a silver paste material SL at the periphery of the liquid crystal display device. Moreover, a portion of the conductive film (g1 and g2) of this external pull-out wiring is configured by the same manufacturing process as the scan signal line GL. As a result, the holding capacitance electrode line GL of the last stage can be easily connected to the common transparent pixel electrode ITO2.

[0074] The first stage holding capacitance electrode line Y_0 may be connected to the last stage scan signal line Yend, connected to a DC potential point (AC ground point) other than Vcom, or connected so as to receive one extra scan pulse Y_0 from the vertical scan circuit V.

[0075] Next, a manufacturing method of the liquid crystal display device according to the present invention will be described. First, a silicon oxide film SIO is provided on both surfaces of a lower transparent glass board SUB1 composed of 7059 glass (trade name), which is then baked at 500°C for 60 minutes. Next, a first conductive film g1 composed of chromium having a film thickness of 1,100 Å is provided on the lower transparent glass board SUB1 by sputtering. Next, the first conductive film g1 is selectively etched using a photographic etching technique using the second cerium ammonium nitrate solution as the etching solution to form a gate terminal GTM and a drain terminal DTM, and an

anodizing bus line (not illustrated) connecting the gate terminal GTM and an anodizing pad (not illustrated) connected to the anodizing bus line. Next, after the resist is removed using the detachment solution S502 (trade name), O₂ ashing is performed for one minute. Next, a second conductive film g2 composed of aluminum-palladium, aluminum-silicon, aluminum-silicon-titanium, aluminum-silicon-copper, and the like having a film thickness of 2,800 Å is provided by sputtering. Next, an electrode PL1 of a scan signal line GL, a gate electrode GT, and a holding capacitance element Cadd is formed by selectively etching the second conductive film g2 using the photographic etching technique using a mixture of phosphoric acid, nitric acid, and acetic acid as the etching solution. Next, SF₆ gas is introduced into a dry etching device to remove residues such as silicon, and then the resist is removed. Next, a resist for anodizing is provided. Next, an anodizing portion of the lower transparent glass board SUB1 to be anodized is immersed in an anodic oxide solution consisting of a solution in which 3% tartaric acid is adjusted to a pH of 7.0 ± 0.5 by ammonia and diluted 1:9 with ethylene glycol, and an anodic oxide voltage is applied to the anodizing pad to anodize the second conductive film g2, thereby providing an anode oxide film AOF having a film thickness of about 1,800 Å on the scan signal line GL and on the gate electrode GT. Next, ammonia gas, silane gas, and nitrogen gas are introduced into a plasma CVD device to provide a silicon nitride film having a film thickness of 2,000 Å, silane gas and hydrogen gas are introduced into the plasma CVD device to provide an i-type amorphous silicon film having a film thickness of 2,000 Å, and hydrogen gas and phosphine gas are introduced into the plasma CVD device to provide an N(+)-type amorphous silicon film having a film thickness of 300 Å. Next, the i-type semiconductor layer AS is formed by selectively etching an N(+)-type amorphous silicon film and an i-type amorphous silicon film using the photographic etching technique using SF₆ and CCl₄ as dry etching gasses. Next, after removing the resist, an insulating film GI is formed by selectively etching a silicon nitride film using SF₆ as a dry etching gas using the photographic etching technique. Next, after removing the resist, a first conductive film d1 composed of chromium and having a film thickness of 1,000 Å is provided by sputtering. Next, a first layer of the video signal line DL, the source electrode SD1, and the drain electrode SD2 is formed by selectively etching the first conductive film d1 using the photographic etching technique. Next, before removing the resist, CCl₄ and SF₆ are introduced into the dry etching device to selectively etch the N(+)-type amorphous silicon film, thereby forming an N(+)-type semiconductor layer d0. Next, after removing the resist, O₂ ashing is performed for one minute. Next, a second conductive film d2 composed of aluminum-palladium, aluminum-silicon, aluminum-silicon-titanium, aluminum-silicon-copper, and the like having a film thickness of 3,500 Å is provided by sputtering. Next, a second layer of the video signal line DL, the source electrode SD1, and the drain

electrode SD2 is formed by selectively etching the second conductive film d2 using the photographic etching technique. Next, after removing the resist, O₂ ashing is performed for one minute. Next, a third conductive film d3 composed of an ITO film having a film thickness of 1,000 Å is provided by sputtering. Next, the third conductive film d3 is selectively etched using the photographic etching technique using a mixture of hydrochloric acid and nitric acid as an etching solution to form a third layer of the video signal line DL, the source electrode SD1, and the drain electrode SD2, an uppermost layer of the gate terminal GTM and the drain terminal DTM, and the transparent pixel electrode ITO1. Next, after removing the resist, ammonia gas, silane gas, and nitrogen gas are introduced into the plasma CVD device to provide a silicon nitride film having a film thickness of 1 µm. Next, the protective film PSV1 is formed by selectively etching a silicon nitride film using the photographic etching technique, using SF₆ as a dry etching gas.

[0076] Although the invention configured by the present inventor above is specifically described based on the example above, it is needless to say that the present invention is not limited to the example above, and various modifications can be made within a scope that does not deviate from the essence thereof.

[0077] For example, in the example described above, a reverse stagger structure of gate electrode formation → gate insulating film formation → semiconductor layer formation → source and drain electrode formation is indicated, but the present invention is also valid even when the vertical relationship or the order of making this is reversed. In addition, in the above embodiment, the first and second conductive films d1 and d2 composed of chromium and aluminum were formed, and then the third conductive film d3 composed of ITO was formed, but the chromium film and aluminum film may be formed after the ITO film is formed.

[0078]

[Effects of Invention] As described above, in the liquid crystal display board, liquid crystal display panel, and liquid crystal display device according to the present invention, all connection terminals can be positioned on the signal line terminal even when an error occurs in the distance between the connection terminals at both ends, and thus connection defects between the connection terminal of the circuit board and the signal line terminal do not occur.

[0079] Furthermore, when the length of the connection terminal is shorter than the length of the signal line terminal, even when the circuit board is shifted to the signal line side, the end portion of the circuit board does not go atop the protective film, and thus the signal line terminal and the connection terminal can be reliably connected.

[0080] Thus, the effect of the present invention is remarkable.

[Brief Description of Drawings]

[FIG. 1] A schematic diagram illustrating a drain terminal portion of the liquid crystal display device illustrated in FIG. 2.

[FIG. 2] A main plan view illustrating one pixel of the liquid crystal display unit of the active matrix color liquid crystal display device to which the present invention is applied.

[FIG. 3] A cross-sectional view of a portion formed by

cutting along the cutting line 3-3 in FIG. 2, and a peripheral portion of the seal portion.

[FIG. 4] A cross-sectional view along the cutting line 4-4 in FIG. 2.

[FIG. 5] A cross-sectional view illustrating a gate terminal portion of the liquid crystal display device illustrated in FIG. 2.

[FIG. 6] A cross-sectional view illustrating a drain terminal portion of the liquid crystal display device illustrated in FIG. 2.

[FIG. 7] A main portion plan view of a liquid crystal display unit in which a plurality of pixels illustrated in FIG. 2 are disposed.

[FIG. 8] A plan view depicting only a predetermined layer of pixels illustrated in FIG. 2.

[FIG. 9] A plan view depicting only a predetermined layer of pixels illustrated in FIG. 2.

[FIG. 10] A plan view depicting only a predetermined layer of pixels illustrated in FIG. 7.

[FIG. 11] A main portion plan view illustrating only the pixel electrode layer, light-shielding film, and color filter layer illustrated in FIG. 7.

[FIG. 12] An equivalent circuit diagram illustrating a liquid crystal display unit of an active matrix color liquid crystal display device.

[FIG. 13] An equivalent circuit diagram of the pixel illustrated in FIG. 2.

[FIG. 14] A schematic diagram illustrating a liquid crystal display board of the liquid crystal display device illustrated in FIG. 2.

[FIG. 15] A schematic exploded view illustrating a portion of a

conventional active matrix liquid crystal display device.

[Description of Reference Numerals]

SUB ... Transparent glass board

GL ... Scan signal line

DL ... Video signal line

GI ... Insulating film

GT ... Gate electrode

AS ... i-type semiconductor layer

SD ... Source electrode or drain electrode

PSV ... Protective film

BM ... Light-shielding film

LC ... Liquid crystal

TFT ... Thin film transistor

ITO ... Transparent pixel electrode

g, d ... Conductive films

Cadd ... Holding capacitance element

Cgs ... Parasitic capacitance

Cpix ... Liquid crystal capacitance

AOF ... Anodized oxide film

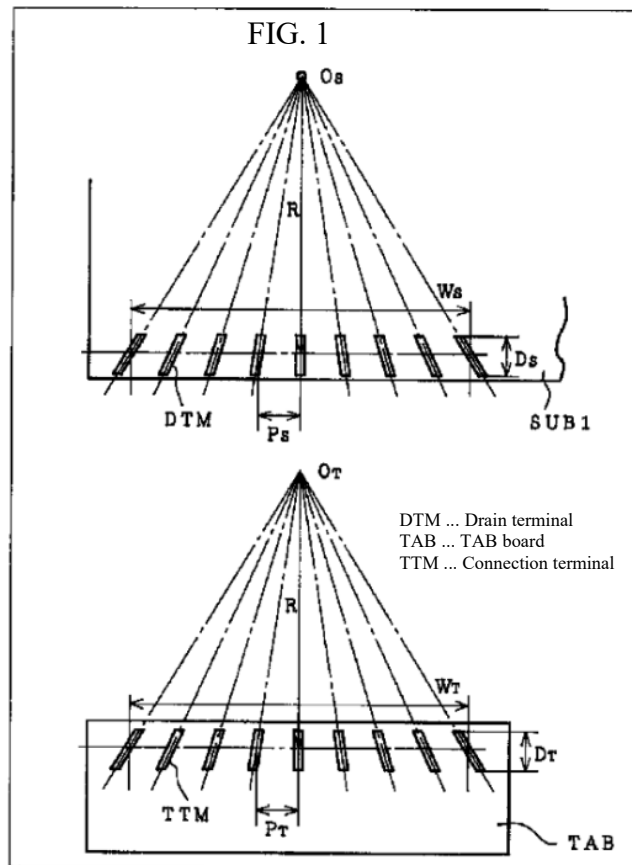
GTM ... Gate terminal

DTM ... Drain terminal

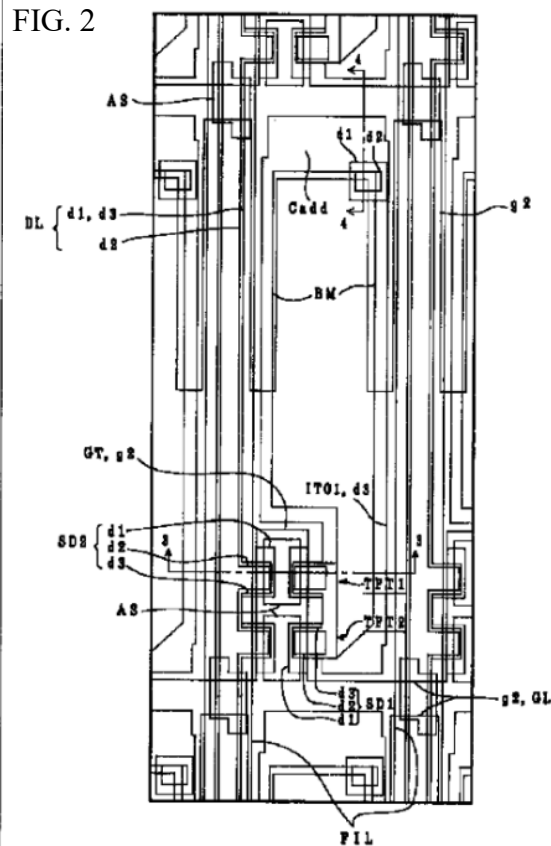
TAB ... TAB board

TTM ... Connection terminal

[FIG. 1]

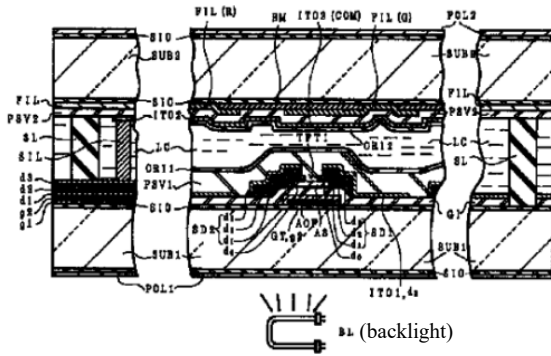


[FIG. 2]



[FIG. 3]

FIG. 3

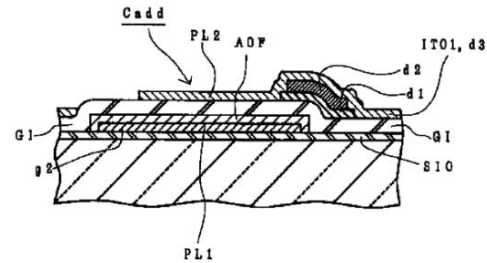


POL1, POL2 ... Polarizing board
 SUB2 ... Upper glass board
 FIL ... Color filter
 PSV2 ... Protective film of color filter
 ITO2 ... Common transparent pixel electrode
 ORI2 ... Upper oriented film
 LC ... Liquid crystal
 ORI1 ... Lower oriented film
 BM ... Black matrix
 PSV1 ... Protective film of TFT

ITO1 (layer d3) ... Transparent pixel electrode
 SD ... Source drain electrode (layers d1 to d3)
 AS ... i-Type semiconductor layer
 GI ... Gate insulating film
 GT ... Gate electrode (layer g1, g2)
 SUB1 ... Lower glass board
 BL ... Backlight
 SIO ... Silicon oxide film

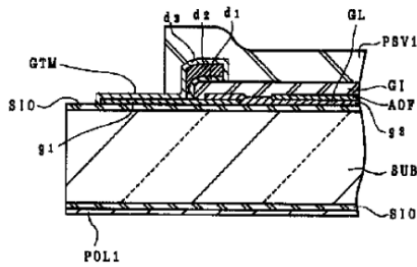
[FIG. 4]

FIG. 4



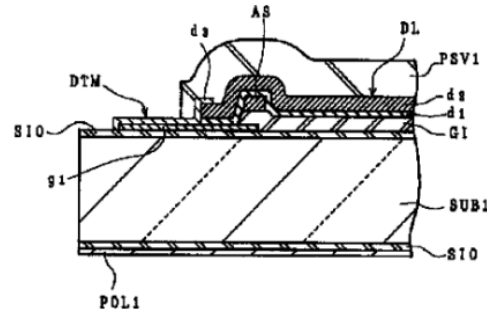
[FIG. 5]

FIG. 5



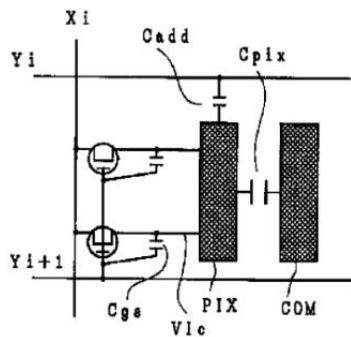
[FIG. 6]

FIG. 6



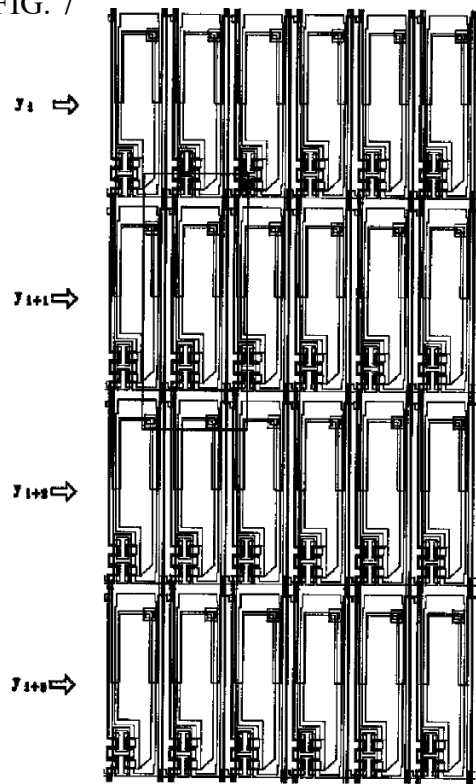
[FIG. 13]

FIG. 13



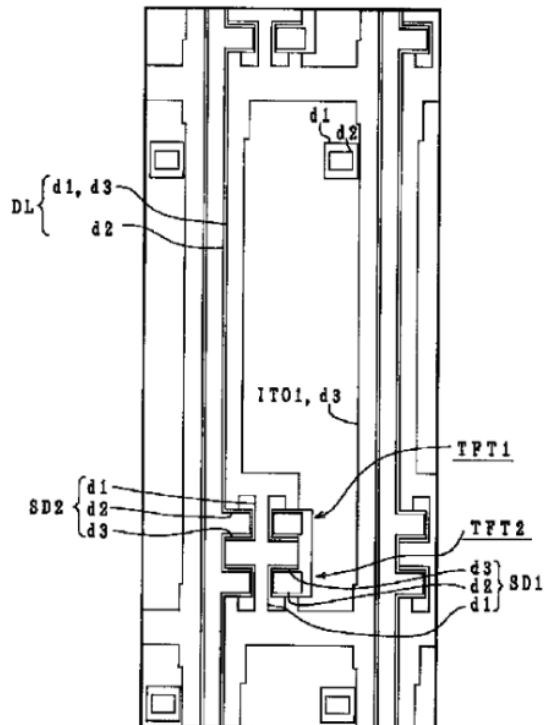
[FIG. 7]

FIG. 7



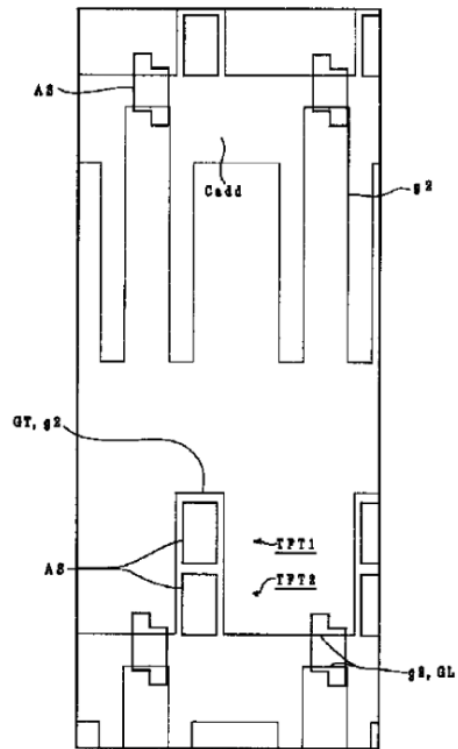
[FIG. 9]

FIG. 9



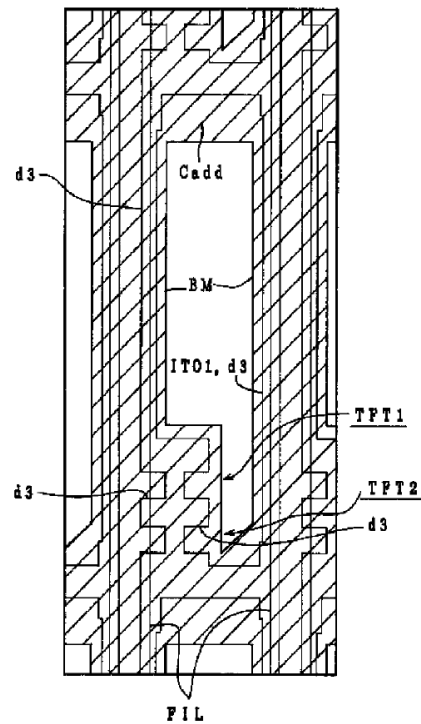
[FIG. 8]

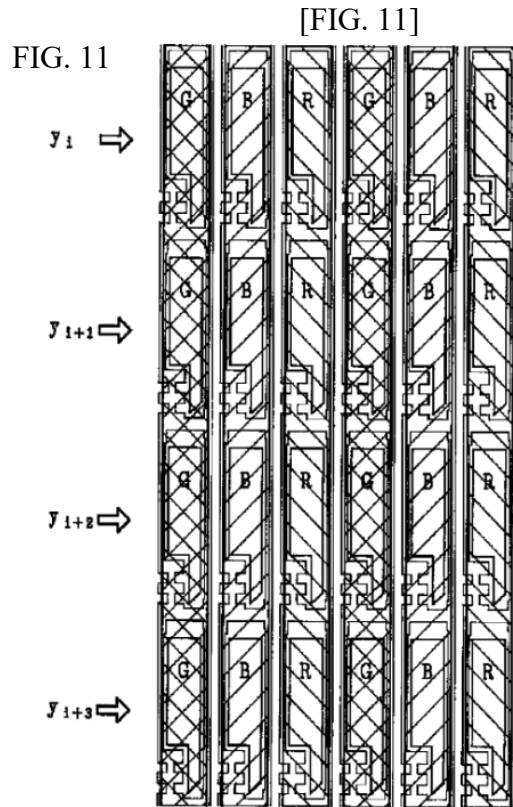
FIG. 8



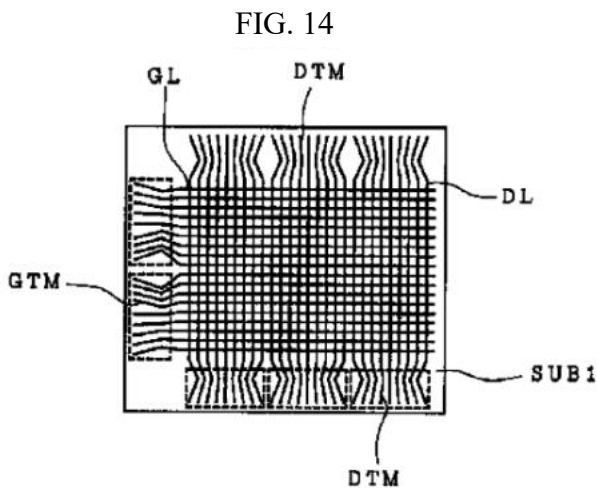
[FIG. 10]

FIG. 10

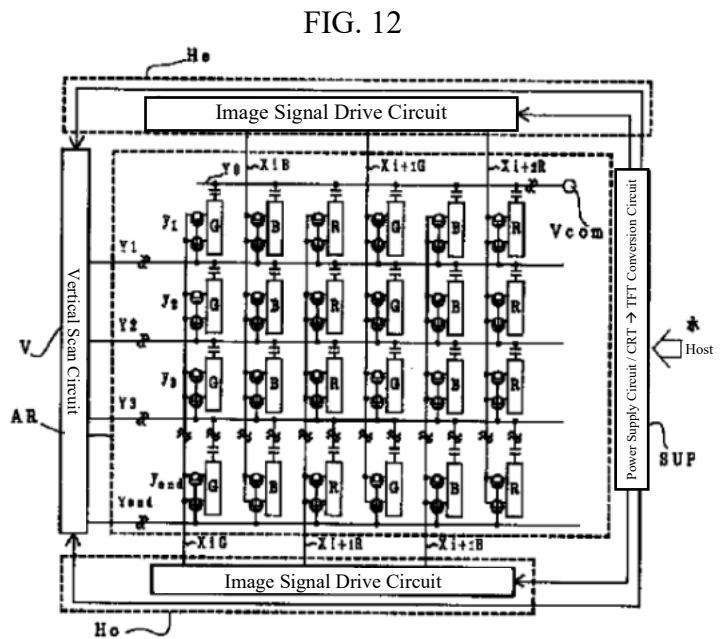




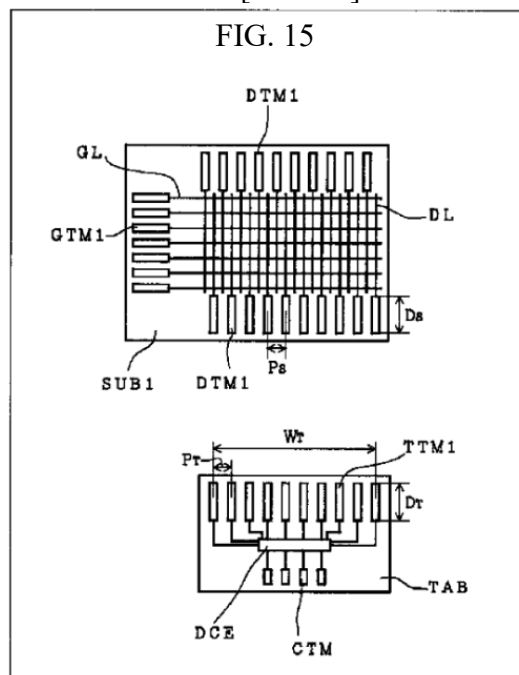
[FIG. 14]



[FIG. 12]



[FIG. 15]



Continued from Front Page
 (72) Inventor Toshio Futami
 c/o Hitachi, Ltd.
 3300 Hayano, Mobara-shi, Chiba-ken