

Third Edition

Wire Bonding

IN MICROELECTRONICS

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George Harman

The Industry Standard to Wire Bonding—Fully Updated

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The definitive resource on the critical process of connecting semiconductors with their packages, *Wire Bonding in Microelectronics*, Third Edition, has been thoroughly revised to help you meet the challenges of today's small-scale and fine-pitch microelectronics. This authoritative guide covers every aspect of designing, manufacturing, and evaluating wire bonds engineered with cutting-edge techniques. In addition to gaining a full grasp of bonding technology, you'll learn how to create reliable bonds at exceedingly high yields, test wire bonds, solve common bonding problems, implement molecular cleaning methods, and much more.

COVERAGE INCLUDES:

- Ultrasonic bonding systems and technologies, including high-frequency systems
- Bonding wire metallurgy and characteristics, including copper wire
- Wire bond testing
- Gold-aluminum intermetallic compounds and other interface reactions
- Gold and nickel-based bond pad plating materials and problems
- Cleaning to improve bondability and reliability
- Mechanical problems in wire bonding
- High-yield, fine-pitch, specialized-looping, soft-substrate, and extreme-temperature wire bonds
- Copper, low-dielectric-constant (Cu/Lo-k) technology and problems
- Wire bonding process modeling and simulation



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Wire Bonding in Microelectronics

George Harman

Third Edition



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CHAPTER 9

Advanced and Specialized Wire Bonding Technologies

(Including High Yield, Fine
Pitch, PCBs, Soft Substrates,
Extreme Temperature Wire
Bonding and Specialized
Looping)

9.1 The Technology and Problems of High Yield and Ever-Finer Pitch Wire Bonding, and Specialized Looping

9.1.1 Introduction to High Yield in Modern Wire Bonding

Forty years ago, wire bonding yield was considered acceptable if it was around 98%, a figure that could not be tolerated today. At that time, most ICs had only 8 or 10 I/Os, the bonders were manual, and rework for missed bonds took place before the package was removed from the bonder. Today (2008), we have thousands of I/Os per chip, high-speed autobonders (operating 12 wires/second or

greater),* and worldwide competitive pressures. Thus, the current manufacturing thrust assumes high yield for cost-driven as well as performance-driven devices. In assembly and packaging, this usually refers to achieving high yields in each specific operation (e.g., sawing, die attach, wire bonding, plastic encapsulation, surface mounting). Of all chip-assembly steps, wire bonding (and other interconnection methods) can have the greatest assembly impact on device yield because of the large numbers of I/Os on each chip with two bonds per wire. In addition, if the interconnection failure damages the chip (as in cratering), it often results in loss of the package or requires difficult rework, which is prohibitive in current production rates and economics. Thus, to improve device packaging yield, efforts should logically be concentrated on improving interconnection yield.

Bonds can be made with some autobonders at 30 μm pitch, but currently such chips are not available. As the pitch decreases, so does the wire diameter, and 15 μm Au wire is available with finer diameters expected, as demand requires. Thus, fine pitch wire bonding has arrived. Almost every aspect of fine-pitch bonding requires more planning and is more expensive to achieve than bonding at earlier accepted pitches. (We note that many chips are still being made at $\geq 100 \mu\text{m}$ pad pitch and will continue for many years.)

Currently (2008), the world semiconductor industry is making about 12 to 14 trillion wire interconnections per year (two bonds and wire loop). The infrastructure to achieve this is so large that no new interconnection method can replace them in the foreseeable future. Thus, we will continue to use wire-bond interconnections for a majority of chips. Flip-chip (C-4) and as yet unknown technologies such as photonic interconnections will be used for the most advanced device production and increase their market share. Today, wire-bonding yield losses in volume production typically range from about 100 to 25 ppm, with some less than 20 ppm. In order to achieve the lower numbers, one must understand all of the conditions that affect both bond yield and reliability (because they are interrelated).

In order to discuss the details of high-yield and fine-pitch bonding, we must assume that the reader understands the normal elements of bonding technology as described elsewhere in this book. These include: bond pad and wire metallurgy (Chap. 3), testing (Chap. 4), but special fine pitch changes are discussed below, intermetallic compound formation (Chap. 5), plating (Chap. 6, Secs. A and B), cleaning

*Defining the bonding speed (number of wires/s) of a high-speed autobonder is complex. The simple straight out, minimum-loop bonding-speed can be much higher than realistic production speeds; even bonding around a chip is slower than a simple straight-out run. Long wires take longer. Complex looping will slow the process considerably—see App. 9A. The cassette loading of chips into bonding position slows the average speed. Thus, a bonder manufacturer could honestly state a very high speed that in real-world usage might never be achieved.

(Chap. 7), and mechanical issues (Chap. 8) such as cratering. In addition, the bonder must be set up by valid statistical design methods [See App. 8B (DOE), by Lee Levine.] Without such understanding and control of the bonding process, it is not possible to even approach high yields and fine-pitch wire bonding. Also, to achieve these ends, everything must be done correctly, and the solution to every solved production problem must be understood! A quick fix (change something and it works), without understanding why it failed, usually results in the problem recurring at a later time.

9.1.2 The Requirements for High-Yield Bonding (Metallization Surface, Hardness, Cleanliness)

The requirements for high-yield bonding are summarized in outline form in Table 9-1. Each of these was discussed in detail in earlier chapters and is summarized below. Also, some of these concepts were described earlier in [9-1].

Bond-Pad Metallization, Aluminum

The first requirement for high-yield bonding is that the metallization on both the chip and the package be bondable. Unfortunately, the characteristics of the chip metallization may be determined by other

1. Good bondable metallization on chip and package
 - Uniform, reproducible characteristics
 - Soft—approximately same hardness as wire
 - Most additives decrease yield (Cu, Ti, etc.)
 - Thickness: 1 to 1.2 μm , pure Al pad caps (0.3 μm thick) can be added at Fab level for bondability and cratering protection
 - Free of organic and inorganic contamination (plasma clean as final Fab process)
2. Uniform wire
 - Close dimensional tolerances (<1.25 μm diameter variation for 25- μm gold ball bonding)
 - Consistent metallurgy (elongation, breaking load)
3. Controllable, consistent bonding machine (force, US energy, etc.)
 - Accurate placement on bonding pad
 - Reproducible, fast, ball formation
4. Package designed around the characteristics and limitations of the specific autobonder
5. Bonding machine package clamping designed for the specific package
6. Accurate and flat (horizontal) die-attach

TABLE 9-1 High Yield and Fine Pitch Bonding Requirements

considerations. For example, adequate electromigration performance often requires that additives be incorporated in or under the Al metallization. Titanium nitride or Ti-W layers are sometimes sandwiched within or under the pad and occasionally (process dependent) the Ti may diffuse to the surface [9-2] and oxidize, lowering bondability. Copper is often added to the Al variously from about 0.5 to 2% by weight. Generally, if the amount of Cu exceeds ~2%, the bondability decreases. In most cases, 1% Cu is adequate for electromigration purposes, this low percentage may result in the growth of theta phase (Al_2Cu) hillocks/aggregates during various wafer heat treatments [9-3]. This level of copper doping increases the metallization's susceptibility to corrosion [9-1, 9-4] and may result in copper oxide on the surface, which requires the bonding engineers to deal with the resulting poorly bondable metal. The metallurgical part of this problem was discussed in Chap. 5, Sec. 5.3.2. A solution to this can be to apply approximately 3000 Å of pure Al on top of the Cu doped metallization as shown in Fig. 9-1. This does add another step to fabrication but increases the bonding yield, which should pay for that process. (Also, there are other ways to avoid Cu, TiN, or other additives, and some devices use special underlayers, sandwiches of metals, etc., which can leave pure Al on top in the process.)

The effect of bond pad hardness on bondability is shown in Fig. 9-2 [9-5, 9-6]. (Note: these experiments are difficult to perform and should be repeated with modern equipment.) In general, for the highest bondability between Au and Al, the hardness of both the wire

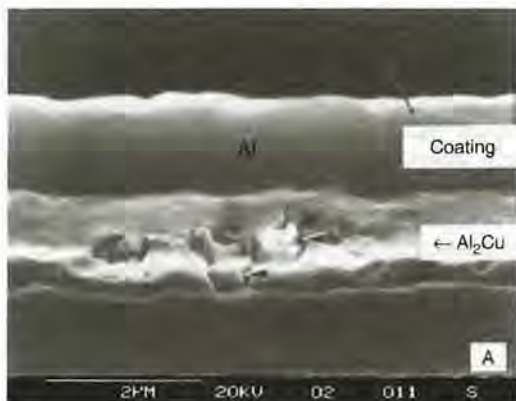


FIGURE 9-1 A bond pad containing 1.5% Cu with Al-Cu intermetallic compounds which decreases bondability. A 3000 Å cap of pure Al was deposited over the layer of Al-Cu which will increase the bondability [9-1]. (Composite figure showing an Al-1.5% Cu-bond pad metallization including Al-Cu intermetallics, with a cap which can be pure Al or Al-1%Si [9-1]; © IEEE.)

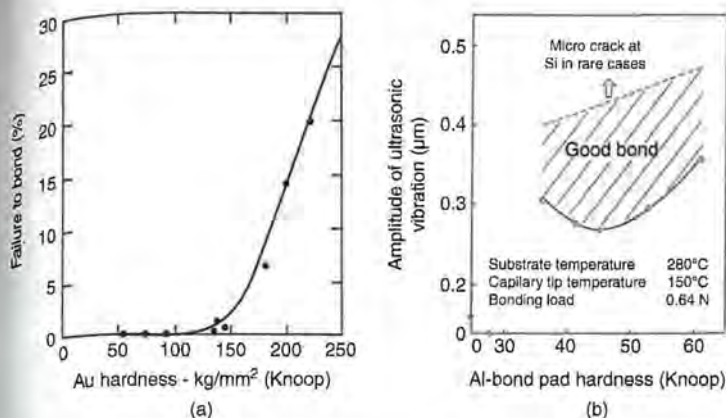


FIGURE 9-2 (a) The effect of a gold film hardness versus gold bond lifts (bondability) [9-5]. (b) Ultrasonic energy to bond versus hardness of aluminum bond pad, for Cu ball bonding [9-6]. In (a), a minima should be reached below the ball hardness (~40 HK). For Cu balls (hardness ~55 HK), it occurs on (hardened) Al pads near 45 HK (© IEEE).

and the bond pad should be approximately matched [9-6, 9-7]. Titanium has also been alloyed into Al in concentrations of about 0.2% for electromigration protection. No increased corrosion has been reported for this additive; however, some Ti may diffuse to the surface of the pad, lowering bond yields. Also, it will increase the hardness to over 100 HK (Knoop hardness), requiring an increase of the thermosonic energy or bonding temperature to ~320°C in order to achieve a high yield. This, in turn, requires a high-temperature die-attach epoxy which, if not already in use, necessitates expensive qualification tests. In general, any dopant (except silicon) added to pure Al will reduce its bondability to some degree.

A solution to many bondability problems that could eliminate bond yield loss from Fab-metallurgical bond-pad conditions has been known for some time. This requires capping (or coating) the Cu-doped bond-pad metallization with ~0.3 μm of pure aluminum as indicated in Fig. 9-2. Fortunately, today, many IC Fabs have design rules that are intended to produce high-bondability chip pads. Some of this has been a result of Cu/Lo-k chips that were originally impossible to bond at high yield. (See above and in Chap. 10.)

Metallization Cleanliness

Regardless of the specific metal(s) making up the pad, its surface must be clean in the assembly area if high-bond yields are expected. There have been numerous studies on cleaning methods and procedures, and many of these are reviewed in Chap. 7. One recent study

was oriented specifically toward cleaning/bonding to the Ni-based metallizations that are used for wire bonding on PCBs, PBGAs, etc., [9-8] (also see Sec. 6B). Oxygen/argon plasma and UV/ozone are the best cleaning methods, but one must be aware that any silver, copper, or nickel in the package or chip may oxidize and lower the yield for bonds made on these metals. Such cleaning is economically mandatory for low-volume, high-reliability hybrids, MCMs, SIPs, sensors, and the like, and large single-chip packages but not, in general, for high-volume IC production (although automatic, in-line plasma cleaners are available). Investigations of bond-pad cleanliness on wafers have shown that several significant contaminants may be left by the wafer processing steps [9-5, 9-7]. These may include S, Cl, F, TiN, fluoropolymers, glass, and carbonaceous materials. Some of these are shown in the Auger spectra of a bond pad on a wafer (see Fig. 9-3). This figure also demonstrates how effective oxygen plasma is in removing most residual Fab contamination. However, oxygen plasma will not remove glass or other inorganics from the pad, except by sputtering, so it is imperative that they be removed earlier during processing. Wafers may be shipped to packaging foundries (often continents away) with the processing contaminants remaining on the bond pads. These will not be removed by washing accompanying

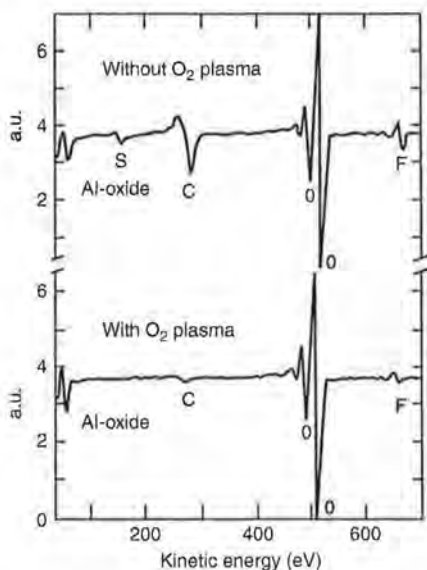


FIGURE 9-3 The effect of O_2 plasma cleaning on an Al-bond pad surface. This Auger cleaning was done at the wafer level in order to remove wafer processing contamination. (After Klein [9-5]; © IEEE.)

saw-separation and can, therefore, reduce bondability. It is a simple matter for the wafer Fab to plasma clean the wafers, in oxygen (or oxygen-argon), before shipment or storage. Then, Fab-induced contaminants will not contribute to bond-yield or reliability problems as in the past!

After the wafers are cleaned, they must be properly packaged for storage or shipment to avoid recontamination. The effect of wafer storage on contamination was studied [9-9]. It was found that storage and shipment of wafers should take place in sealed aluminum cans having aluminum wafer holders. Storage in plastic will eventually result in a buildup of organic contamination. As an alternative, if wafers must be shipped and stored in plastic then the wafers should be plasma or UV-ozone cleaned before saw-separation at the packaging facility. Cleaning whole wafers is quick and economical.

Advanced, High-Performance Devices now Use Cu (Rather than Al) On-chip Interconnects

These Cu-bond-pad areas on the chip are protected by a diffusion barrier and have $\sim 1 \mu\text{m}$ of pure Al deposited on top as the actual bond pad. Thus recent Cu/Lo-k devices do not have the same bond-pad problems as many traditional Al interconnected devices. However, they must be cleaned as described above. See Chap. 10 for a description of that technology. At the present time, the vast majority of devices are still based on Al interconnects, but this will change in the future.

The Package Metallization

The off-chip metallization, be it on a leadframe, ceramic, laminated plastic substrate for a BGA, etc., can result in as serious a bond-yield problem as the chip metallization. Gold, Ag, Pd, and Ni are the most frequently used off-chip metallizations, see Chap. 6 (A and B). Cleaning is equally as important as for the chip pads (discussed in Chap. 7). This problem is complicated because of the variety of different metals used for bond pads in the many types of packages. Each metal usually requires different cleaning and storage conditions. Metals that oxidize (i.e., Ni, Cu) cannot be removed with UV/ozone or oxygen plasma, but rather by sputtering/reduction with Ar or H_2 + Ar. Electroplated metal films may vary in hardness, crystal structure, impurity, and gas content, all of which can affect bondability. Appropriate quality evaluation tests must be run for each bonding method (pull test for wedge and shear test for ball bonds).

9.1.3 The Bonding Machine and Its Control

As indicated above, the characteristics and setup procedures of individual bonding machines are beyond the scope of this book, since these vary greatly and will continue to change as newer models are

introduced. Specific information for each bonder is available from the manufacturers, who usually offer training courses in their use. All bonders for production use, must be set up for the intended chip and package metallization using appropriate experimental design methods, DOE (see Chap. 8, App. 8B). However, the set up and control of bonders to produce high-bond yields in hybrids, SIPs, stacked chips with overhanging pad areas, etc., are much more difficult than for the high-volume production of ICs. The latter have been discussed earlier in this chapter. Most sensors, hybrids, and MCMs are produced in relatively low volume, but stacked chips, SIPs, etc. can be very high. These all may include a number of chips from different manufacturers, and each chip can have different metallizations or at least have undergone different heat treatments. The contamination left on bond pads by different wafer fabs and subsequent handling is apt to be different. As production progresses, chips ordered later from the same vendors can be from different wafer lots/designs, and the metallization and residual contamination may vary. Thus, cleaning with UV-ozone or O_2 plasma, after polymer die-attach (which produces its own contamination) and within several hours of bonding becomes important in order to obtain the highest bond yields. Following these procedures, the highest yields have been achieved when bonding to chips in ceramic packages [9-5]. The choice of specific bonding technology, in addition to all other factors, can have an impact on the yield in a given situation. Numerous other machine conditions and factors can affect yield in the 10 to 100 ppm region (e.g., design of the bonding tool, as well as maintaining the vertical position with respect to the bonding pad).

9.1.4 Reliability for Small Numbers of Bonds (Small Sample Statistics)

Bondability, as well as reliability data for set up on low-volume chip and substrate metallizations, is often obtained by bonding across metallization pads on electrical reject substrates and chips. However, the main high-yield problem is less than 100 ppm yield production control when using small sample sizes. One approach to achieve bond-production control with small sample sizes used the deformed width of wedge bonds (which fitted a normal distribution as determined by the Chi-square statistic) in conjunction with reliability test data. This was used to predict bond reliability (lifetime) of chip-on-board (COB) devices on PC boards [9-10]. While not a generic solution, this concept may be used as a starting point to develop a more universal small sample bond-process control. An example of fine-pitch bond-yield prediction was used by Shu [9-11] who measured the gaps between adjacent ball bonds on fine-pitch bonding test die, assumed that they were normally distributed, and used that assumption to calculate the probability of shorting between adjacent balls in a variety of fine-pitch wire-bonding situations. Based on these

examples, one possible approach to small sample yield or reliability control would be to study the failure modes, establish and then combine the distributions of the most likely failures, and use the results to predict yield or reliability. As production continues, confidence in the method would increase based on cumulative production control charts. In the above examples, the predictions based on a measurable bond parameter would apply to a wide variety of products so that in time a large amount of yield or reliability data could be obtained, even though low-volume production runs are small. Discussions, including cause-and-effect (fishbone) diagrams, of the procedures necessary to bring low-volume wire bonding under statistical process control have been published [9-12]. The process can be improved using DOE setup of bonders in the beginning (see Chap. 8, App. 8B, by Lee Levine).

The generic *reliability* prediction (defects per thousand device hours) for wire bonds is often requested by designers of low-volume systems, such as SIPs, MCMs, specialized devices/systems, as well as small-volume IC production. While such a value would be desirable, it is not realistic to expect that any definitive numbers will emerge. There are so many variables in the manufacture and long-term environment of devices that such a hypothetical value, if used to predict bond life, would be equivalent to the computer jargon of "garbage in, garbage out." Some variables that make such general prediction almost impossible are: type of bond and metallurgy (Au-ball-wedge, Al- and Au-wedge-wedge, Al, Au, Ag, Ni, Pd, etc., pads), quality of bond set up (DOE or other), any cleaning procedures used before bonding (plasma, UV-ozone, solvent, other, or none), loop heights (if open cavity), plastic molded (if so then which resin), fine pitch or not, cratering probability, and chip metallization structure, environment (temperature, power, or temperature cycle-number), range, dwell time, duration, and humidity. However, the reliability of a specific known type of device can be determined by performing stress tests on appropriate numbers and evaluating the results by statistical methods. If all chips from different vendors had pure, uniform aluminum metallization caps, as described in Fig. 9-1, then high-yield low-volume bonding set up and control would be greatly simplified, and such reliability predictions could be more valid. The same admonition for manufacturing low-volume systems as for high-yield bonding is appropriate. To achieve these ends, everything must be done correctly, and the solution to every solved production problem must be understood (or the problem may reappear)!

9.1.5 Package Related Bond-Yield Issues

The effect of different package types on bonding yield as well as its dependence on leadframe clamping has been studied by Klein [9-5]. In general, he found that the rigid ceramic packages are best, and that small packages (perhaps because they are difficult to clamp) are worse.

Leadframe and package clamping have long been known to affect bond yield. A poorly clamped package results in the dissipation of ultrasonic energy by resonating (vibrating) rather than concentrating that energy in the bond interface area.* The observable symptom of poor clamping is a large variation of bond deformation across the sample/substrate. Ceramic packages, because of their rigidity, generally result in higher bond yields than bare leadframes. Also, thin, small-outline, and also fine-pitch leadframes, have lower bond yields than large leadframes. Thus, the choice of package, as well as its clamping, can have a significant impact on wire-bond yield.

9.1.6 Possible Yield Problems and Solutions

Wire Diameter Variations

It has been shown that variations in the diameter of gold bonding wire (within the currently allowed ASTM specifications of $\pm 3\%$, or a 6% maximum diameter variation) for 25 μm wire, ASTM F 72-06 in Chap. 3, App. 3A, can result in variations of ball-formation diameter for ball bonding [9-13]. If the wire diameter is slightly larger, then more of the thermal energy from the EFO is conducted away from the melt zone, and the resulting ball is smaller. The maximum difference in the unbonded, free air-ball diameter is only about 5 μm for a typical 25 μm diameter wire ball. However, this can combine with other variables of the EFO wire-machine system increasing the difference. Different ball sizes require slightly different optimum bonding machine set ups, so this may affect yield in the high-yield range. To achieve the very highest bond yields (e.g., <25 ppm defects, wire should be purchased under a tighter diameter control of ± 1 to 2%). Similar variations in wire for wedge bonding should not affect bonding, since thermal conductivity does not play a role as it does with ball bonding. (A ball size shift, with constant wire diameter, can be experimentally simulated by varying the EFO setting in a designed experiment.)

Probe-Mark Damage

Probe-mark damage left on the pads is an example of a problem that chip packaging personnel cannot avoid, if left during wafer test. However, they can be observed, and could be a reason to reject a wafer lot, if bonding problems occur. Such probe marks only became a problem when fine pitch was implemented [9-14, 9-15, 9-16]. It was found that

*This resonance can be easily demonstrated by spreading *lycopodium* powder (or equivalent) over the package before the bonding-clamping experiments. Poorly clamped packages will show powder accumulations at resonance nodes and clean areas on maxima. Such resonant patterns are very prominent in large-diameter wire bonding experiments. (Note: this very fine powder tends to get all over the bonder workstage, so it should be handled with care. Such experiments are usually run on manual bonders.) All such large wire experiments show some resonances, but it is still helpful.

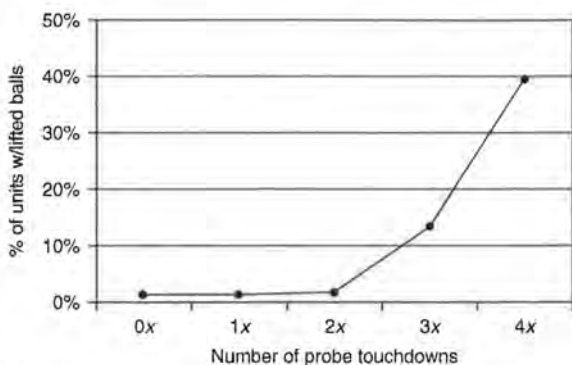


FIGURE 9-4 The number of lifted balls versus probe touchdowns for $\sim 60\ \mu\text{m}$ pitch pads [9-14] (© IEEE).

probe damage was acceptable for $60\ \mu\text{m}$ pitch pads, only if the probe touchdowns exceeded 2/pad, as shown in Fig. 9-4. However, the finer the pitch, the more lifts occurred. For $35\ \mu\text{m}$ pitch, the ratio of non-stick-on-pads (NSOP) due to probe marks could be as high as 84%, with only *one probe touchdown* [9-16]. Although several solutions for pad design have been investigated (hardened, laminated, and corrugated pads, etc.), it was found by several studies that the most practical solution was to off-set the probe testing part from the bonding area, as shown in Fig. 9-5. In those cases the extended pads can overlap into active areas that would not be damaged by the probe stress. This design would not require larger chip size. It would, however, require different visual inspection criteria which could require changes in such documents.

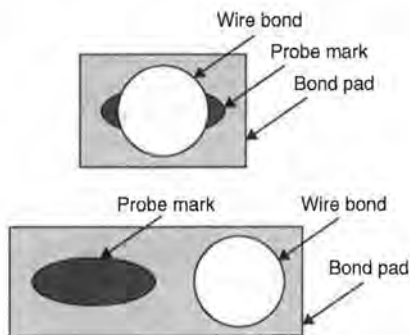


FIGURE 9-5 Top, normal fine-pitch pad. Bottom, pad is elongated to avoid damage during probing. (This configuration may require different visual inspection criteria.) [9-16] (© IEEE).

9.1.7 Other Considerations That May Affect Overall Device Yield

The Ultrasonic Systems

The ultrasonic systems of wire bonders in the past used 60 kHz ultrasonic energy. However, starting in the 1990s the bonding frequency has been increased to ~120 kHz. Publications of that period indicated that the bond yield could be improved by increasing the ultrasonic frequency. This work offered a new parameter that may increase the bond yield. High-frequency systems currently have been universally adopted by production autobonder manufacturers. See Chap. 2, Sec. 2.4, for a more detailed discussion of high-frequency bonding technology including additional references.

Wire Sweep

Wire sweep refers to the movement of the wire-bond loops during the transfer-molding process. In worst cases, adjacent wires will touch and short one another. Technically, wire sweep is not a part of wire bonding, but it can affect the yield of plastic devices. As such, it must be considered in designing such wire-bonding process.

During the molding process, enough hydrostatic force is generated by the hot plastic to deform and occasionally push the wires into one another, leading to short circuits. The latter seldom occurs, but some deformation of the wire loops is common. Many industry specifications permit up to a 5% (permanent) displacement or deformation of the loop. However, this is an arbitrary value that is not appropriate for long fine-pitch wires in molded devices. Course pitch can normally safely accept an even greater displacement. The smaller the wire diameter, the higher and longer the loop, the more rejects will be encountered due to wire sweep. Fine-pitch packages have less fanout and often longer wires for higher lead count, resulting in greater possibility of wire shorting from minimal wire sweep. The looping shapes can also affect the shorting possibility. Additional complications can result from area array bonding.

Wire sweep is a complex subject and depends on the wire diameter, its stiffness (Cu stiffer than Au), the shape of the loop, its orientation with respect to the plastic flow (position and size of the mold gates), the height and position of the chip, and the mold design. In addition, it is affected by the viscosity and other parameters of the mold compound [9-17, 9-18, 9-19]. Although many experiments have been run using x rays and/or plastic removal, most current work consists of finite element modeling to design the mold, gates, and plastic flow, in order to minimize the effect. The dynamic flow properties of the hot filled resin must often be estimated, and FEA results that are not confirmed with experiments may not be accurate. Wire sweep modeling is often done with large, general, FEA software packages, and these can be adapted to wire sweep design [9-20].

9.1.8 Wire Looping

Appendix 9A by Lee Levine has a specialized discussion on wire looping, illustrated with many examples of long wires, shapes, etc. As with wire sweep, looping is not directly a bonding issue. It is controlled by the machine and its looping software. However, looping can affect the reliability and yield of a ball bonded package, so such capabilities should be understood by the user. Often packages require very low loops only about 50 to 75 μm (2 to 3 mil), such as in stacked chips, CSPs, BGAs, etc. Other packages require long flat loops or ones with special shapes to avoid contacting part of the chip or package. The simplest and oldest of these looping techniques moves the wire initially in a reverse (opposite) direction from the second bond position before moving toward it. This forms a smooth loop that does not sag. More recently, bonder manufacturers have learned to form very special loop shapes by a series of tool motions (back and forth, up and down, etc.) during loop formation. There have been patents and papers describing these complex loop-forming motions [9-21 to 9-23]. These motions can produce long flat loops, as well as loops with kinks and discrete bends. Some variations of these are named "worked loops," "smart loops," etc. Without such loop control it would not be possible to wire bond many of the special packages used today as fully described in App. 9A. We note, however, that any special loop shaping slows the bonder throughput significantly. Unusual loop shapes have been designed for special purposes. One, for especially low stable loops, is shown in Fig. 9-6.

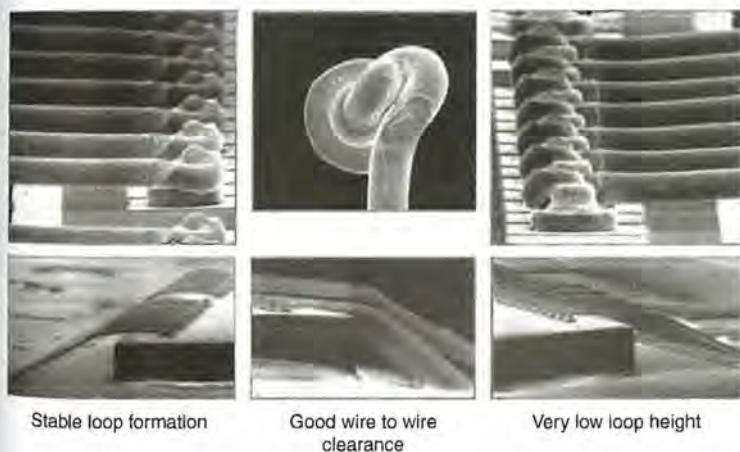
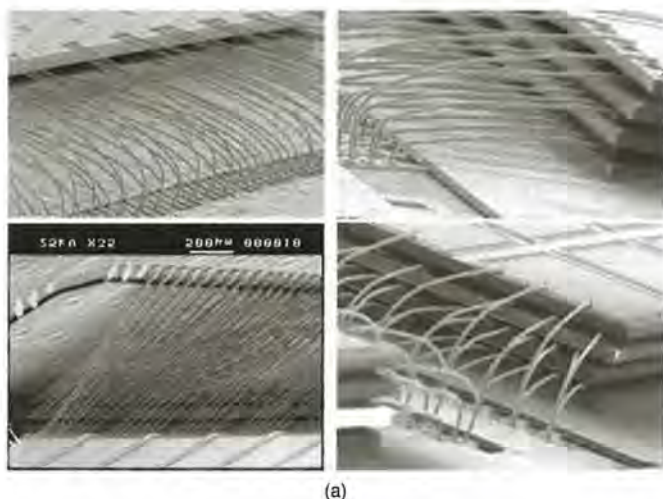


FIGURE 9-6 Ultralow "Escargot" loops that are less than 40 μm high. (Courtesy of ASM, Singapore)

Stacked Chips

Another area that requires very special looping and other unusual wire bonding techniques is that of stacked chips. These chips are first thinned to 50 to 200 μm and bonding often takes place to overhanging chips. This leads to very special bonders/programming for that unique purpose. There is a glue layer, or interposer, between offset chips. These stacks are built in layers, with bonding as each layer is applied. Normally, memory chips are used because of their low thermal dissipation. However, when power chips are used, they are placed at the bottom of the stack for heat-sinking. Currently, most of these stacks are used in very high volume for portable devices, such as cell phones. Although stacks have been demonstrated as high as 25 or 30, most have less than 10 layers. Several such stacks are shown in Fig. 9-7a. This is a specialized subject and interested persons should



(a)

Maximum numbers of dies stacked (and in volume production)									
Year	2008	2009	2010	2011	2012	2013	2014	2015	2018
Wire bonded	8	10	10	12	12	12	14	14	16

(b)

FIGURE 9-7 (a) Examples of stacked dies connected with wire bonds. (Stud bumps are first bonded to dies and the crescent of a ball bond to-the-package is bonded to it. Then the next layer is applied, etc.) In this case 4-stacked dies are shown on the right. The wire bond complexity is obvious (*Courtesy of Amkor*). (b) An excerpted section of the 2008 ITRS A&P roadmap for wire-bonded stacked chips predicting the years that the number of stacked dies will be entering high-volume production, somewhere in the world.

start with the ITRS 2008 A&P Roadmap, and the ITRS "SIP white paper 2008," manufacturers' literature, etc. A section of the 2008 A&P Roadmap predicting the future number of dies stacked is given in Fig. 9-7b. Note that the roadmap also discusses another stacking technology (e.g., "Through Silicon vias"-TSV), which is predicted to have only 5 chips/stack by 2018, but its performance would be much higher than wire bonded ones. We note that some totally different method of increasing active chip density could be invented by that date.

9.1.9 Fine-Pitch Ball and Wedge Bonding

Fine-pitch bonding is evolving faster than a book can possibly follow. It is the leading edge of wire bonding. Although the author believes that the current state of the art (2008) is reasonably represented below, the situation will probably change (improve) even before this book is published. Most of the advances result from improvements in auto-bonders, capillary design, wire doping, and associated equipment, rather than user-based improvements. Currently, advanced auto-bonders for IC production are capable of 30 to 35 μm pitch, and some might go still finer, but implementation is delayed by the availability of appropriate chips/infrastructure. There are many papers/articles on this subject each year, in conferences, as well as from the bonding machine manufacturers. The reader should obtain these and contact those companies to assess the state-of-the-art at any given time. Fine-pitch bonding requires special capillaries that are generally called bottleneck capillaries, because of their shape. These avoid hitting adjacent wires, as shown in Fig. 9-8.

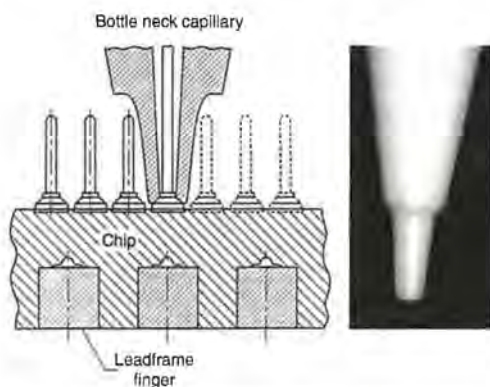


FIGURE 9-8 Left: drawing of a bottleneck capillary, bonding from the left to right direction. It is designed to avoid contacting the last-made-bond (on the left). These capillaries are fragile and break easily. Right: a photograph of the constricted tip. For very fine pitch, the tip is much more constricted and more fragile.

It should be noted that as the pitch decreases, more interface reliability and other problems have appeared. Some will be described below. The introduction of new dopants for Au wires is the major change related to reliability of the Au-Al interface. As a reality check, one should realize that most chips and packages are not (in 2008) classified as fine pitch. These are usually the most advanced or specialized chips. Later as new Fabs are built, and the feature size shrinks, finer pitch moves to more conventional chips.

Fine-Pitch Ball Bonding

A majority of devices made in 2008 still have low pin-counts (<100), and the bonding-pad-pitch for such ball bonds is still in the 80 to 100 μm range. However, 40 μm pitch is currently in production for high-end devices. An example of ball-bonds made with a similar fine pitch is given in Fig 9-12, and 35 μm ball bond pitch devices are nearing volume production in 2008. Figure 9-7 gives an example of 70 μm pitch ball bonds made with 25 μm diameter Au wire. Such bonds are made with bottleneck capillaries to avoid displacing adjacent bond wires. See Fig. 9-8 for an example of such capillaries. Very fine-pitch ball bonds can be visually different from the familiar coarser pitch ones, as shown in Chap. 4, Fig. 4-18 in which the bonded ball is only a little larger than the wire.

Some wires in use are only 15 μm in diameter, and 12 μm has been tested. These wires will be more subject to wire-sweep failures during plastic molding unless a solution to that problem is achieved. In time, insulated wire, lower viscosity molding compounds, or improved mold gates may extend the limit somewhat. Finer pitch-ball bond pitch ($<30 \mu\text{m}$) has been achieved in experiments but may not be used until chips having such pitch are available.

Typical bond parameters for fine-pitch ball bonding are given in Table 9-2. Note that the bonded ball size for this 70 μm process is about 47 μm , less than twice the wire diameter. For 50 μm pitch the bonded ball is only $\sim 40 \mu\text{m}$ diameter and having $\sim 12 \text{ gf}$ shear, with a shear force of $\sim 7.5 \text{ gf}$. Below $\sim 60 \mu\text{m}$ pitch, the bond-pull test would adequately evaluate the weld strength of ball bonds, and the shear test would be used only for set up purposes. This is desirable since shear testing of fine pitch balls is slow, difficult, and error prone. See Chap. 4, Sec. 4.7 for a discussion of this alternative. A caveat of such testing is that for long-term reliability of Au-Al ball bonds, the bond shear force should be more than 5.5 gf/mil^2 (also see Ref. [9-24] and Chap. 4, Fig. 4-23).

Fine-Pitch Wedge Bonding

Currently, wedge bonds can be made at 25 μm pitch using wires of 18 to 20 μm diameter, and bonding with high frequency ($\sim 120 \text{ kHz}$) US energy. This results in very low bond deformation (see Chap. 2, Sec. 2.4). It is not clear if this is in actual production, but if not, it certainly will be in the near future.

Machine or Test Parameter	100 μm Process	90 μm Process	80 μm Process	70 μm Process	50 μm Process	40 μm Process	35 μm Process
Free-air ball diameter (μm)	50	—	43.2	40.6	32.4	31	29.5
Bonded ball diameter (μm)	74	61.3	55.8	47	~40	32	27
Bonded ball height (μm)	16.1	13.5	12.5	5.9	~6	~7	~7

^aValues are typical and were collected from the literature, since the ball diameter can be changed during setup, it may not result in a consistent table.

^bWire diameter <25 μm , for fine pitch (from K&S [9-25]), as low as 17 and 15 μm diameter.

TABLE 9-2 Four Fine-Pitch Ball Bonding Parameters for Processes Using 25 μm Diameter Gold Wire^a

Fine-Pitch Capillaries (Caps) and Wedge-Bonding Tools

Everything must undergo a change for fine pitch, and the capillaries and bonding tools are no exception. In order to avoid deforming the already formed loops, the tools must be reduced in diameter. Examples for both ball-bonding capillaries and wedge-bonding tools are given in Figs. 9-8 and 9-9. Note that these shapes are typical, but for instance, caps can also be long and finely tapered, rather than bottle-neck shaped.

9.1.10 Reliability and Testing Problems of Fine-Pitch Bonding

The bond pitch is the distance between wire bond centers (also the distance between the center of one bond pad to the next). However, part of this space must be used to separate (insulate) the pads; thus, the bondable area on the pad itself is further reduced by the overlapping passivation. One of the concerns expressed about very fine-pitch bonding is that bonder inaccuracy can place the bond on that passivation. It may not be far enough off-pad to be rejected, but it can crack the passivation, and the cracks sometimes propagate outside the pad. There have been no documented reports that this presents a reliability problem in hermetic packages. The primary concern is for devices in moisture permeable plastic molded packages where leakage paths may develop. Also, some bonds can overlap and short with



FIGURE 9-9 Fine-pitch wedge bonding tools. The left is an older design. (Courtesy of Microminiature Tech.) On the right is a recent design that is stronger (less fragile). This tool has a cross-groove in its foot, and is intended for fine-pitch wedge bonding with gold wire. (Courtesy of Fraunhofer IZM.)

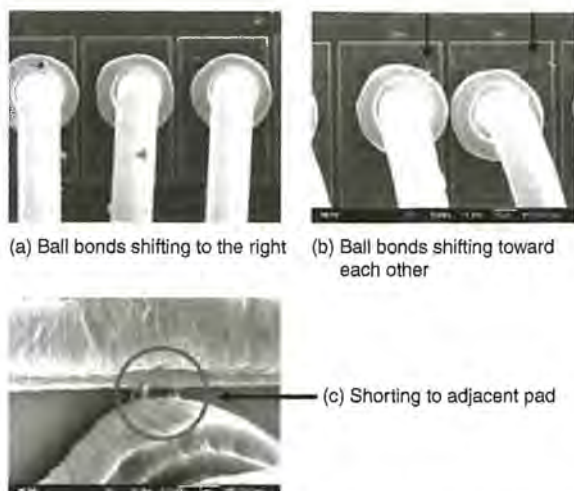


FIGURE 9-10 Three possible shorting problems of 47 μm fine-pitch (and finer) ball bond placement [9-24] (© IEEE).

adjacent pads or ball bonds. Ruston [9-24] gave examples of several possible placement problems with 47 μm pitch ball bonds. These are shown in Figure 9-10. Solutions included finer diameter wire (which could lead to more wire sweep), but produced smaller balls, and new machines with closer placement tolerance. Ultimately, the balls passed the ball shear strength and maintained the minimum industry-standard value of 5.5 gf/mil² after extended thermal aging. It should be noted that similar problems can arise with each new *finer pitch chip* generation!

The New Mechanical Testing Problems for Fine Pitch Ball Bonds

Table 9-3 shows the predictions of the ITRS roadmap for wire-bonding pitch until 2016. Ball-bonding pitch reduces to its minimum of 25 μm by 2015, and the wedge-bonding minimum is expected to be reached sometime in 2009 (see the table footnote). (All such ITRS predictions are subject to modification each year and assume that high-volume production at such pitch will exist somewhere in the world by that date.)

The decreasing pitch indicates possible future wire-bond problems or at least changes in manufacturing and testing (see Fig. 9-11). Both pull testing and shear testing are affected by finer pitch bonds.

The ball-shear test has been described as indispensable to evaluation of ball bonds (see Chap. 4, Sec. 4.3). However, as the pitch decreases to below $\sim 50 \mu\text{m}$, it is harder to position the ever smaller

Year of Production	2007	2008	2009	2010	2012	2014	2016
Wire bond, ball, single in-line (μm)	40	35	35	35	30	30	25
Two-row staggered pitch (μm)	55	50	45	45	40	40	35
Three-tier pitch (μm)	60	60	60	55	55	45	45
Wire bond—wedge bond pitch (μm)	25	25	20 ^a	20 ^a	20 ^a	20 ^a	20 ^a

Excerpted from ITRS 2008 A&P roadmap, Table AP3.
These values are proposed and may be postponed or never reach production. The bonders could, but other factors may prevent or slow implementation.

TABLE 9-3 Chip-to-Package Substrate Technology Requirements—Near-Term Years

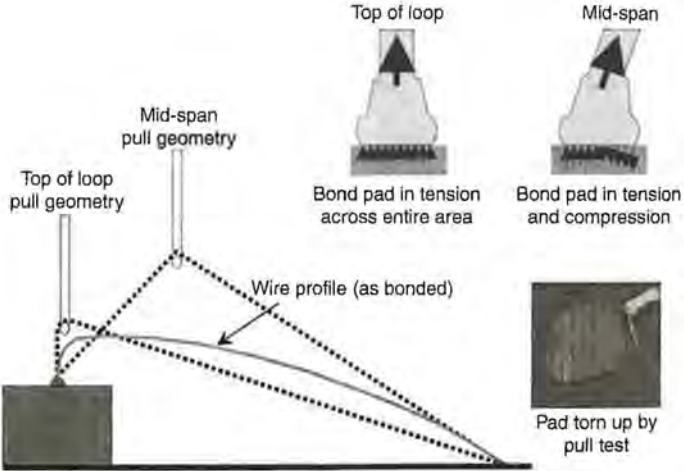


FIGURE 9-11 A merged figure showing two pulling geometries. The Top of loop (left) vertical pull (will never be perfectly straight up) will minimize pad tearing. An example of a pad, torn up during a pull test is shown on the lower right. (Courtesy of Jon Brunner, K&S.)

shear probe without hitting the adjacent ball bond, resulting in inaccurate data. (Accurate placement takes longer and requires more operator skill. At some point even this is not possible.)

The first work to have investigated the pull test to replace the shear test for fine-pitch ball bonds was done by Sundararaman [9-26]. He found that when a fine-pitch ball bond is made over a probe mark, the pull-test stress at the normal center-pull angle is large enough to lift-peel that ball. This starts in the probe mark area, which is poorly bonded and serves as a stress raiser, and the ball lifts before the wire can break normally at the HAZ. The results from such a lift/peel test should be interpreted with caution. A bond pull should be considered a failure only if the ball lifts and examination shows that there was poor intermetallic formation.

This test is mostly used on Cu/Lo-k chips, which often have low pad or sublayer to pad adhesion and the pad may lift or tear, even without a probe mark-stress raiser. Other work found that if the angle of pull is vertical, then the "tear" component is minimized and more normal HAZ (wire) breaks occur. An example of the desired (vertical) configuration is shown in Fig. 9-11. Note that even for "attempted" top-of-loop pulling, some tear stress still exists and tearing may be occasionally observed since the angle is not exactly vertical. For some very fine-pitch bonds with balls shaped as in Fig. 4-18 (Chap. 4), this tearing problem can occur if the pull force exceeds the tensile adhesion of the pad to SiO_2 in normal (non-Cu/Lo-k) structures.

Almost every aspect of fine-pitch bonding requires more planning and is more expensive to achieve than bonding at relatively coarse pitch. The shape, size, and placement of the bond pads must be coordinated with the selection of the autobonder and die-attach machine (with their known positioning accuracy and repeatability), as well as the specific package layout. For vertically integrated companies this is done during the early chip-design phase. Problems can exist for packaging foundries, but they often work closely with high-volume chip designers. The finest pitch wedge bonding is achieved with narrow (rectangular or parallelogram shaped) bond pads, but these would not be amenable to ball bonding even if there were compelling reasons for doing it at a later time. Because of these limitations such pad designs are not often used except in vertically integrated companies, or as a help in testing fine-pitch pads using displaced probes (in Fig. 9-5). The throughput from an auto-wedge bonder is less than that from an equivalent ball bonder (2 to 4 wires/s vs. >10/s, respectively). Thus, wedge bonds cost more than ball bonds, and as a result, only represent about 5% of the total number of bonds made.

Some packages have bonding pads on two or more vertical shelves (tiers). It is possible for bond wires to cross over one another, particularly when bonding around corners of the package where the wires fan out. Shorting between rows is a possibility, and it is necessary to

carefully design and control the bond loops to meet minimum clearance requirements (see App. 9A). This is both a high-yield and a fine-pitch bonding problem. Proprietary spreadsheet programs for tolerance analysis have been designed for this purpose, which includes bond-loop and wire-spacing prediction, as well as all package tolerances. Software with some modern autobonders has some of this capability. However, the bonding machine will operate faster, the positioning will be more accurate, bond loops more highly controlled, and the yield higher if all wires are bonded straight out from the chip (no fanout). This requires complete coordination between the chip and the package designer. Bonding straight out in fine-pitch ceramic packages is usually achieved by bonding to two or more tiers. However, some modern high-density SIPs, MCMs, etc., can have bond pads with pitches approaching those on chips, simplifying bonding and improving the yield.

Area Array Wire Bonding

As autobonders have increased in capability and chips have more I/Os, the concept of area-array wire bonding became both possible and essential for high leadcount devices. This has pushed the limits on all aspects of wire-bonding technology. These bonders have fine-pitch, extremely precise, long loops, with minimum possible sag of the loop. It is thus possible to have a greater number of wire bond I/Os than area-array flip chips in the same chip area. (Cross-talk, inductance, and other electrical problems can be improved by design, but of course, will still not have the high-frequency performance of flip chips.) An example of area-array chip bonding is shown in Fig. 9-12.

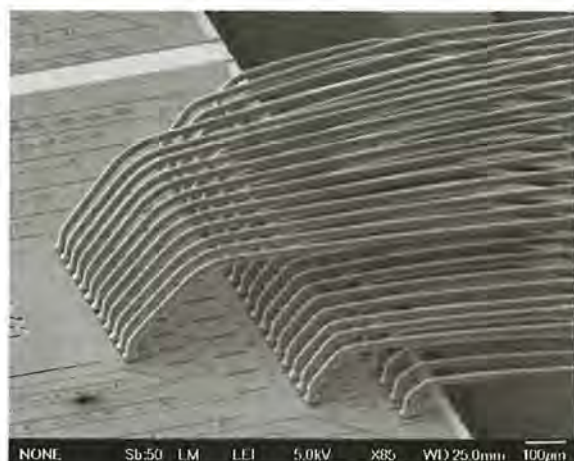


FIGURE 9-12 An example of fine-pitch area-array wire bonding. These bonded balls are 40 μm in diameter. (Courtesy of ASM, Singapore.)

9.1.11 Conclusions of High Yield and Fine Pitch

1. To even hope to approach high-yield and fine-pitch wire bonding, you have to do everything right and understand everything you do!
2. If vertically integrated, you should *cooperatively* design the chip, the package, and choose the bonding and die-attach process as well as the actual equipment before chip production can begin.
3. You have to understand both the wafer Fab's metallurgical processes (what's under the pad) as well as all assembly processes (e.g., die attach) that affect bonding.
4. You must remove contamination from the bond pads, including those remaining from the wafer Fab and assembly processes. (However, it should be the responsibility of the wafer Fab to deliver wafers that have clean, bondable metal.)
5. You have to understand both your wire bonder's limitations and the bonding process, and control them as well as your incoming materials. (Form keiretsu-like relationships with your suppliers.)
6. For fine pitch you must upgrade your equipment (bonders, caps, cleanliness, etc.) continually.
7. Your management must be completely committed to the fine-pitch and high-yield process.
8. If you are manufacturing SIPs, hybrids, MCMs, MEMS or other complex, low-volume products, you start with two strikes against you. You will have to work twice as hard as the IC industry to even approach high-yield bonding, but fine pitch can be achieved with the same effort.

9.2 Wire Bonding to PC boards, Flex, BGAs, MCMs, SIPs, and Various Soft Substrate Devices and High-Performance Systems

9.2.1 Introduction

The classical thick-film hybrid uses a ceramic substrate. Bond pads are of thick-film Au or Ag (alloy) applied directly over that ceramic. This poses no more special problems than bonding to a ceramic package [9-27]. As such, high yields (≤ 50 ppm defective) are attainable if the best metallurgy and bonding procedures are followed. However, other plastic-based substrates (PC boards, BGAs, SIPs, etc.) can pose significant bonding problems. These are normally epoxy-like

polymers laminated with fiberglass or other fillers and may bond well above their glass transition. In some cases, a layer of thin-film dielectric and metallization is deposited on the surface of a ceramic- or laminate-based substrate to improve the high-frequency signal characteristics (build-up layers). In other cases, plastics without lamination (such as flex substrates) may be used. Some complex IC chips have multilevel polymer-insulated metallization or special Low- k dielectrics such as SiOC (see Chap. 10). If pads are placed on top of these polymers rather than on the traditional Si/SiO₂, then bonding can be similar to bonding on soft substrates. Microwave hybrids are often made on polytetrafluoroethylene (PTFE) "soft" substrates and require special knowledge and bonding machine set up. These plastic substrates may be laminated or have fillers similar to PC boards. Some are hard and easily bonded.

The discussion that follows describes all aspects of soft-substrate wire bonding, including the polymer and bond-pad metal material properties, the bonding-machine requirements, as well as the considerations for using wire bonds in high-clock-rate systems. The important point is that if one expects to wire bond to multilayer polymer substrates, or other soft substrates, then one must design the system (both polymer and metallization) with that objective in mind. Otherwise, the wire-bond yield may be unacceptable and the redesign time consuming and costly [9-28].

9.2.2 Bonding to Thin-Film Dielectric Substrates

Bond pads usually consist of gold-plated thin-film Cu, or Al, placed on top of one or more layers of relatively soft polyimide (PI) or other plastics. But the first soft substrates were microwave hybrids that used laminated or filled PTFE (soft) substrates. One of the first solutions to bonding over PTFE was to solder thick gold-plated Cu disks to the thin-metal bond pads, which produced a rigid platform for bonding [9-29]. Most of the later work on soft substrates has followed equivalent solutions, although often without realizing it. As an example, when using Cu conductors, Ni films are often applied as diffusion barriers between the Au surface plating (for high bondability) and the Cu to prevent Au-Cu interdiffusion. But, fortuitously, this Ni layer also stiffened the bond pads, improving their bondability.

Other approaches that improved thermosonic (TS) ball bonding yields onto pads over PI are to add hard 0.5 μm thick Ti or Ti/W layers under Al-bonding pads on PI (over Si chips) [9-30, 9-31, 9-32, 9-33]. (Such hard metal layers have long been used under Al and GaAs IC chip pads to prevent cratering.) In addition, it was reported that greater ball deformation resulted with the same bonding machine parameters, a normal indication of improved bondability. Various reliability tests used in both studies verified the improved bond quality.

As with PI-coated chips, hard underlayers of Ti, Cr, etc., are also used to stiffen Cu-bond pads on thin-film high-performance substrates. (These hard metals are often required for adhesion, as well as corrosion protection on PI substrates, but because these metal films are lossy, they must be thin, $\leq 1000 \text{ \AA}$, for high clock-rate systems; see Sec. 9.2.6.) To improve Au-plated Cu bond pads, a thick layer of Ni (~ 3 to $8 \text{ \mu m}$) can be plated on top of the Cu pad and then overplate it with $\sim 1 \text{ \mu m}$ of soft, bondable Au. All of these hard layers can reduce the pad deformation during bonding, increasing the bonding yield. Although the terms cupping, bending, copper-trace sag, and pad deformation of the bond pads have been used in the field for several years, it remained for Takeda [9-34] to actually measure this effect on bond pads over flexible polyimide PCBs. He wedge bonded to $18 \text{ \mu m}$ thick Cu-bond pads (overplated with $2 \text{ \mu m}$ of Au) using $35 \text{ \mu m}$ diameter gold-plated Cu wire. (Since this is much harder than Au or Al wire, it easily demonstrated the cupping phenomena.) The bonding process left a significant pad indentation (measured with a profilometer), as shown in Fig. 9-13. The indentation depth was shown to be dependent on both the ultrasonic energy and the bonding force. They also found that the larger the bond-pad area, the higher the wire-bond yield. The fact that the Cu-bonding wire was harder than the usual Au or Al wires presumably made the indentation more prominent and, thus, easier to measure. The cupping was accompanied by poor bonding yield. After plating $3 \text{ \mu m}$ of Ni between the Cu base and the top bondable Au, the

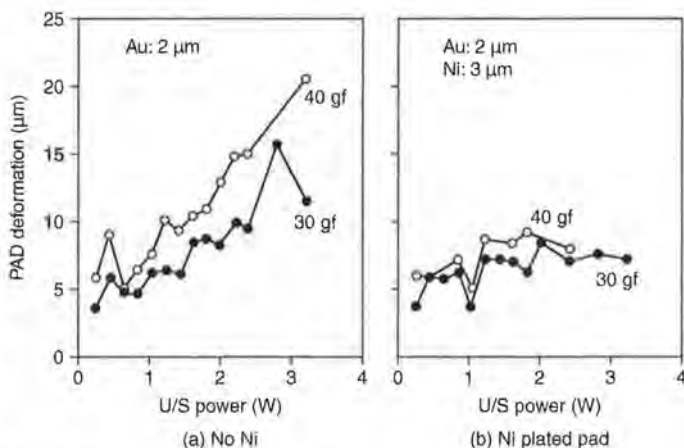


FIGURE 9-13 The depth of bond-pad indentation (cupping) on polyimide flex substrates as a function of ultrasonic energy and bond force. (a) with only $2 \text{ \mu m}$ thick Au over $18 \text{ \mu m}$ thick Cu; (b) with a $3\text{-}\mu\text{m}$ thick Ni layer between the Cu and Au layers [9-34] (© IMAPS).

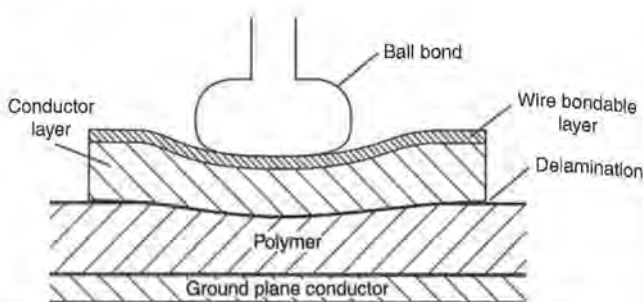


FIGURE 9-14 Deformed bond pad and polymer structure after wire bonding. This illustrates the bond-pad cupping phenomena (metal and polymer yielding) that occurs during wire bonding to copper-gold metallization deposited over a soft polymer. The edge of the metal pad may delaminate (as shown) from the polymer due to high-vertical stress. The figure is drawn from the results of a finite element model [9-30] (© IMAPS).

cupping decreased, and the bonding yield increased enough for volume manufacturing. Figure 9-14 illustrates the cupping phenomena. The edge of the metal pad may delaminate (rupture) from the polymer due to high-vertical stress. In such cases, the addition of an adhesion layer (usually Cr or Ti) will prevent separation [9-32].

Some workers in the past have developed bonding parameters for Au-TS bonding with the substrate maintained at room temperature using a heated capillary. This was intended to minimize the thermal softening of the flex-PI film and allow a low bonding force. The combination could help to prevent bond-pad cupping, but a hard Ni layer (platform) appears to be the better solution. In addition, heated capillaries are unavailable on modern autobonders; therefore, hard Ni layers or bond-pad support structures (similar to those used in Cu/Lo-k, see Chap. 10) have become a necessity under the bond pad.

Bonding at temperatures above the T_g for glass-laminated substrates is often possible if the bond-pad metallization is rigid (e.g., having adequate hard metal top layers or underlayers and covers a large area to inhibit sinking). Once a sufficiently rigid, non-cupping platform is achieved, then lowering the bonding temperature (to decrease softening of the polymer) has less effect on bonding. Nevertheless, because of changing expansion coefficient, the effect on any metal adhesives, and in some cases elastic compression of the entire rigid bond pad into the soft plastic, bonding above the substrate's T_g is not recommended.

Several investigators have presumed that it is the soft plastic under the bond pad that absorbs the ultrasonic energy, reducing wire-bonding yield, but this has never been proven. However, if cupping can be minimized by hard-metal layers, bonding will take place

over the softest of substrates, PTFE and polyethylene, implying that the cupping (metal yielding) is more detrimental than the soft plastic in dissipating the ultrasonic energy (assuming that the pad dimensions are large enough to prevent the pad from dynamically sinking into the soft substrate during US application and bonding). Also, for the best bond yield, the application of US energy should be delayed until all mechanical cupping and sinking has stabilized.

The design solution for dynamic sinking and cupping is to apply a hard metal layer, such as Ti, Ti/W, or Ni, directly under the bond pad or between the metallization and the polymer. This reduces or prevents cupping and results in reliable bonding. An example of a structure (with all variations) that achieves this is shown in Fig. 9-15.

9.2.3 Bonding to Laminate Substrates, Such as PCBs, BGAs, SIPs, and Buildup Layers

The wire bonding on most laminate substrates (plastic-ball grid-arrays, system in packages, etc.), which are generally made of glass-epoxy laminates, resembles bonding to PCBs. The metal pads are relatively thick and are often designated in "ounces" of Cu ("1 oz Cu" is 36 μm or 1.4 mil thick) from PCB industry usage. The most common thickness for laminate board Cu conductors is 18 μm (0.5 oz). The epoxy-fiberglass substrate (other polymers and fibers may also be used) is hard and rigid below its glass transition temperature (T_g). This technology offers few problems when bonding at low to moderate temperatures. Aluminum-wedge bonding at 25°C is done with little concern for rigidized bond pads (using $\leq 2 \mu\text{m}$ of Ni under a Cu pad). Chip-on-board (COB) devices using similar substrates have been used for many years, and watch-modules are made on them. BGAs, SIPs, etc. on single or multilayer substrates are also similar. These types of substrates can be bonded with both Au-TS (heated work-stage-below T_g) and cold Al-US methods.

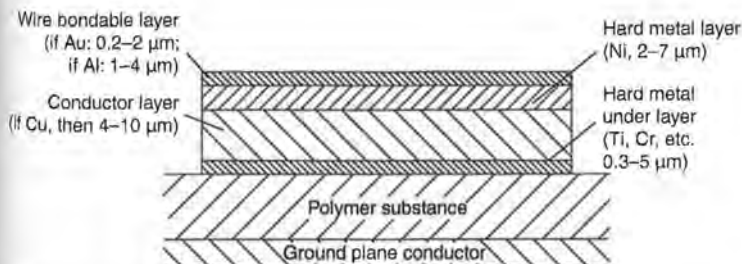


FIGURE 9-15 Structure of a generic, stiffened-metal bond pad and polymer substrate for wire bonding to high-performance substrates/systems [9-30]. The ground plane is included for discussion in Sec. 9.2.6. (© IMAPS).

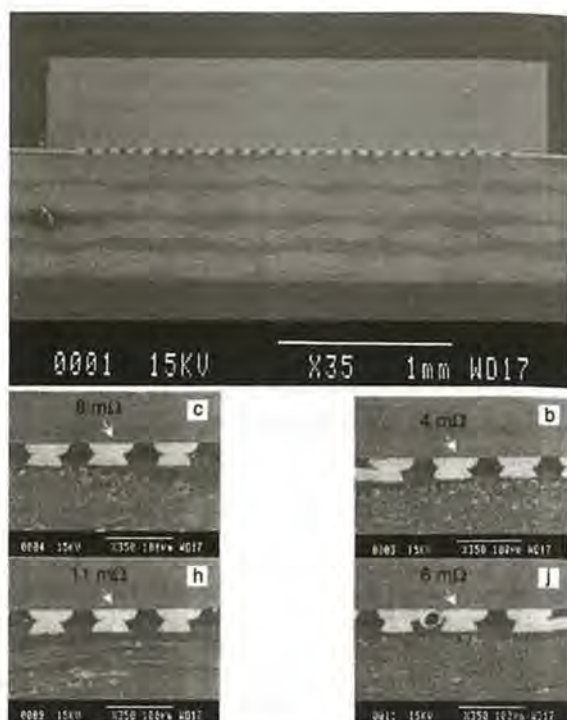


FIGURE 9-16 A cross-section of a glass-fiber-filled printed circuit board, showing how the existence/absence of glass fibers, depending on position, either can or cannot mechanically support any bond pads on the surface. As the temperature approaches T_g the plastic becomes soft. Sinking (and low-bond yield) during the bonding process will more easily occur over areas with no fiber support on the left. (After Liu [9-35].)

The problem of bonding to any type of fiberglass-laminated polymer substrate is illustrated in a PC board cross-section with conductive epoxy flip-chip connections in Fig. 9-16. This provides limited support in specific areas under some of the bond pads. It should be pointed out that some boards use a nonwoven polymer "paper" for support. If its T_g is high (such as aramid), then it uniformly supports all bond pads, even above the epoxy board's T_g .

In some cases, the polymer (being above T_g or because of applied US) may become soft enough so that an entire rigid bond pad literally sinks into the soft plastic during bonding. Dynamic bond-pad sinking changes (lowers) the effective bond force over the first few milliseconds after the capillary (tool) drops (normally during the time that US energy is applied) leading to a changing bond force and lowering

the bond quality/yield. This was first observed when bonding to a polymer substrate above its T_g [9-30] but can also occur with low modulus substrates at room temperature.

9.2.4 Buildup Layers

These are pure polymer (usually epoxy) films without any reinforcing glass fiber (as was shown in Fig. 9-16). They are deposited on top of a normal PC board, and thin, fine-line metallization is applied on top. This can then be laser drilled, and fine vias applied through the layer. The fine vias/metallization lines permit much higher frequencies to be used on a normal low-frequency board/substrate. Often many such layers are built up in this way resulting in high-density, high-performance systems at a nominal cost. They are often used for cell phone boards and other high-density/high-frequency, but cost-driven, applications. If the board or buildup layer has a T_g near the bonding temperature, then wire bonds (but not flip chips), are subject to sinking and low yield. An example of such dynamic sinking during gold crescent-bonding to an Au plating on a *buildup layer* is given in Fig. 9-17.

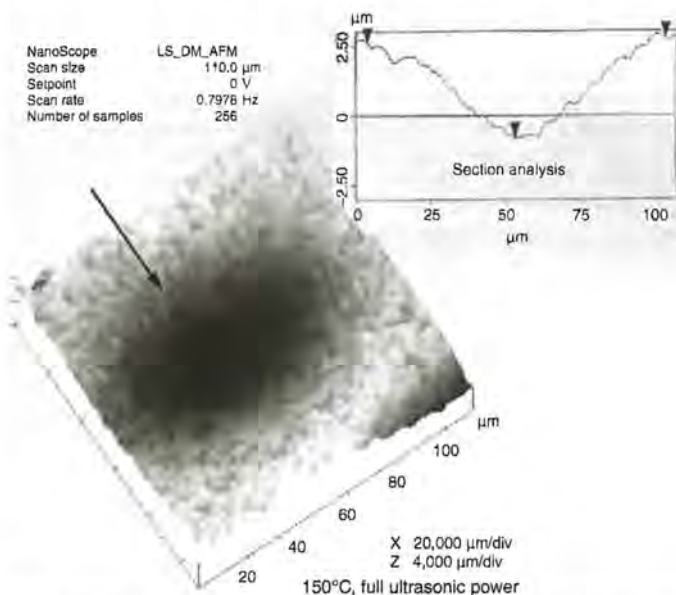


FIGURE 9-17 The sinking phenomena (indicated by arrow) of a 25- μm Au crescent (wedge) bond into an Au-plated pad on an epoxy buildup layer over a PC board (the wire did not weld to the Au plating). The bonding temperature was 150°C, which was near the buildup layers' T_g . The measured depth of the sinking as indicated in the AFM section analysis was about 2.5 μm . (The AFM measurement was made by J. Kopanski, NIST.)

Dynamic bond-pad sinking changes (lowers) the effective bond-to-pad force over the first ~10 to 100 ms after the capillary (tool) drops. This sinking occurs during the time that US energy is normally applied and the bond weld is forming (optimum delay experimentally determined). The dynamically changing bond force requires more US energy or the welding will be incomplete. (The solution is to delay application of US energy.) Thus, bonding near or above the substrate or buildup layer's T_g is not recommended for production unless the bond pad is both rigid and large enough to prevent sinking, or (*experimentally determined*) delay application of US energy until the dynamic sinking stabilizes [9-36]. The effectiveness of such a delay has been verified informally many times. The sinking phenomenon can also occur in PTFE, PI, and other soft substrates at room temperature, if the bond pad is small. A similar delay usually improves bonding.

In general, large PCB panels (typically made of FR-4, $T_g \sim 120^\circ\text{C}$) having bare chips (COB) are usually bonded with Al wire by cold US methods to prevent heat warping of the board and possible softness complications that might result from exceeding the material's T_g . TS bonding at moderate temperatures ($\leq 110^\circ\text{C}$) is often possible, and using a heated tip tool also helps. Special resins with higher T_g (170 to 190°C) are used to permit higher temperature thermosonic bonding (and soldering) to PBGAs and equivalent. If these are processed as large panels, then special substrate clamps (often assisted by vacuum) to hold the structure firmly against the workstage are required and can be a design challenge. Even small, thin-laminate module substrates must be firmly clamped for TS ball bonding to avoid warping, which will lower the bonding yield. However, in some cases, vacuum hold-down has proven adequate for individual BGA-sized substrates. The thicker the PCB/BGA substrate, the less important special clamping becomes. Thermosonic bonding over an unsupported center was successfully achieved on two sides of a small, 28 mm square, 1 mm thick, glass fiber-reinforced BT-resin module [9-37]. When bonding problems are encountered in such substrates, they can usually be solved by methods described above, using bond-pad structures illustrated in Fig. 10-11 (Chap. 10) and delaying application of US energy, if necessary.

9.2.5 The Effect of a Polymer Substrate's Material Properties on Wire Bonding

The best polyimide for thermosonic bonding over active areas on IC chips was found to have the highest elastic modulus, E (stress divided by the strain, below the elastic limit) [9-33]. This material property is related to the stiffness of the polymer and, therefore, should be correlated with cupping, or indentation, of the material during bonding. (The compression modulus in an anisotropic material should give a better indication of softness, but the tensile modulus is often the only

modulus property measured.) The total deformation of an unsupported pad and the polymer during the bonding process was shown in Fig. 9-14 results in the absorption of considerable ultrasonic energy. Such deformation can also result in delamination/rupture of the bond-pad metal from the polymer [9-32]. Elastic modulus data for several substrate polymers are given in Table 9-4. These values range from about 0.5 to 30 GPa. Values on the high end come from harder materials, which will better support a bond pad and, therefore, inhibit cupping during bonding. Polymers having low-modulus values require thicker layers of hard metal (e.g., 4 to 12 μm of Ni) and possibly larger area bond pads to prevent them from sinking into the soft polymer under the bonding load.

Material	Elastic modulus (E) GPa @ (25°C)	E, GPa @ (T°C)	Glass Trans. (T_g) T°C	Reference
FR-4	23, varies by mfg. and meas. direction, range 11-25	21 (100); 15.4 (150)	115-125	Fu, Brown, Ume Ref. [9-38]
Epoxy-glass (BT)	17	—	>170	Manufacturer
Epoxy-Aramid-Paper filler	30	—	194	Sanyu Rec Co., Ltd, Osaka,
Polyimide (unfilled films)	2.5 (flex, films) 7-13 (used as Si chip coatings)	2.0 (200)	-350	E. I. Dupont, Various Mfg., and Ref. [9-33]
BCB	~2-2.5	~1.4-1.8 (200) cure-dependent	>350	Dow Chemical, Midland, MI and Ref. [9-39]
PTFE composite (filled)	0.5-0.9 (ceramic) 1-1.3 (glass micro)	0.45-0.49 (100)	>300, if any, minor trans. ≈ 75	Rogers Corp., Chandler, AZ, others

*Some E values depend on the type of filler and the axis chosen for measurement. Values, therefore, are considered typical. Polyimides and BCB may change properties with different cures. Values obtained from manufacturers' literature, except as noted.

TABLE 9-4 Modulus for Several Electronic Packaging Polymers*

For comparison with polymers, Table 9-5 gives the properties of the metals often used (in combination) for bond pads on them. Note that the modulus of Ti is too low to explain its successful use in supporting Al pads on polyimide over Si chips [9-6, 9-7]. However, both the yield strength and the hardness appear to be good indicators of the bond pad's ability to prevent plastic deformation (cupping) during bonding. The yield strength has been used in a finite-element model with general agreement to observations of cupping, that was illustrated in Fig. 9-14. From Table 9-5 it is apparent that both electroplated and electroless Ni and Cu can have a wide range of yield strengths and hardness. The consequences are that the extent of cupping, for a given metal thickness, will depend upon the specific properties of the metal films in use. As an example, electroless Ni with 1 to 3% P will have much higher yield strength than with 8 to 12% P. The quantitative effect of ultrasonic energy on the softening of both the polymers and the metal layers is a major unknown. Little information is available on this subject. Aluminum, Cu, and Au soften significantly with ultrasonic energy (see Chap. 2) and bond (weld) readily. Nickel, Ti, and W do not soften at normal ultrasonic bonding energy densities and therefore should make good rigid platforms during

Metal	Modulus GPa	Yield Str. MPa	Micro-hardness (Films) kg/mm ²	Brinell hardness (Bulk) kg/mm ²
Al, 1% Si	70	35 (anneal dependant)	50-120	30
Au	80	low, 1-3 (dopant and anneal dependant)	40-100	30
Cu	130	27-40	140-170	35
Ni	207	60-130+	450-800 EL 150-800 EP	75
Ti	110	140		200
W	410	140	460	365

^aEL is electroless and EP is electroplated (films). Most values are for bulk samples at room temperature and are considered indicative only. (For example, Ti values are sensitive to oxygen and nitrogen content; electroless Ni is sensitive to P content, etc.) Values from *Mechanical Behavior of Materials*, by McClintock and Argon, Addison-Wesley, 1966, and *ASM Metals Handbook*, Vol. 2, 9th ed. Also Safranek, W. H., *The properties of Electrodeposited Metals and Alloys*, 2d ed., ASEE, 1986.

TABLE 9-5 Selected Properties of Metals Used on PC Boards and "Soft Substrates"^a

bonding. Nickel has much lower yield strength and hardness than Ti and W, but is higher than copper. As such, Ni should require thicker layers to stiffen a bond pad, which has been observed (3 to 8 μm Ni vs. 0.3 to 0.5 μm Ti or Ti-W). (Note: very thick Ni-plated layers on fine-pitch pads may produce nodular or rounded bonding surfaces that can lower autobonder yield.)

Many HPS substrate materials have anisotropic (directional) characteristics and/or ones that vary with the type of filler or lamination [e.g., some PTFE substrates may have compressive moduli of ~ 1 GPa at 23°C for microparticle fills (either ceramic or glass), but ~ 10 GPa for woven glass fills]. The latter should be better for wire bonding. In some cases (e.g., flex PI, some filled polymer substrates), the metal films have been bonded to the substrate by a different polymer (i.e., acrylic, T_g ~ 45 to 55°C), and this layer can be of significant thickness (~ 25 μm). The various polymer-based glues often have relatively low values of thermo-mechanical properties (i.e., T_g and melting point, modulus $< 50\%$ of PI films, etc.), and these can limit the wire-bonding temperature and affect other bonding characteristics as much or more than the known substrate properties. (Note also that any tiny air bubbles remaining in the glue layer under the pad that do not otherwise present problems may inhibit wire bonding [9-40].) Often, the material characteristics of the glue layer are not readily available to polymer-substrate assembly personnel and, in fact, may not be considered by them when purchasing the substrate. High- T_g glues are available, but direct-bonded Cu is better for wire bonding than gluing with a different polymer on flex substrates.

The temperature characteristics of the substrate must also be taken into consideration when TS bonding at high temperatures. As the polymer's T_g is approached, the modulus decreases (the material becomes softer), and this can affect bonding by offering less resistance to dynamic sinking by a relatively soft- or thin-metal pad. An example of this ($> T_g$) softening on the most frequently used PC board material, a low-temperature FR-4, is given in Fig. 9-17 [9-38]. Equivalent data were not available for other epoxy-based board materials, but they should have similar shaped curves, being displaced toward higher temperatures for higher T_g . Note that the modulus value of the FR-4 board (above) at 150°C is ~ 15.5 GPa, which is still considerably higher than PTFE boards and PI (on flex or as-deposited films). We note, however, that the imbedded glass fiber limits the lowest value on the right of the curve. Without its support, the modulus would be only a few GPa (see Fig. 9-16 for a cross-section of typical PC boards).

A new measurement is needed that would better reflect the resistance to bond-pad cupping. The compressive modulus of anisotropic materials is better than the tensile elastic modulus but, even when available, is not the optimum measurement. If a small bond pad happens to be located over an area of voids between the woven-glass fiber bundles in Fig. 9-16, the board will be locally softer above the T_g .

and no general modulus measurement will reveal a problem. A better measurement could be made by recording the depth of depression, of a ball-type probe, into the bond pad, the glue film (if any), and the polymer substrate, by a given force. It should be measured as a function of temperature and would reflect the overall material properties related to wire bonding much better than a modulus measurement of the polymer substrate alone.

Bonding Optimization

Other actions that can improve bonding over polymers are using *finer diameter wire* (e.g., 18 μm vs. 25 μm diameter), and making *smaller balls* if ball bonding. These permit bonding with *lower machine parameters* (force/power) and thus reduce dynamic cupping, everything else being equal. If using US Al wedge bonding, then the same result will follow from using a softer wire (12 to 14 gm vs. 16 to 18 gm breaking load for 25 μm diameter wire) and/or smaller diameter wire. In general, it is easier to wedge bond with Al wire at room temperature than to use Au wire (wedge or ball) at high temperatures because of the polymers' softening, especially if any glue layers are under the metalization. It is also slow and difficult to conduct heat from the heat-stage through a relatively thick glass-filled polymer and obtain even temperature distribution over an area. However, the specific material properties of the polymer(s) in question should be considered before making such decisions. Often, Al wedge bonding at 25°C can be accomplished on epoxy-laminate substrates (e.g., FR-4) without special thick or hard bond-pad structures. Because the problem in bonding to small-bond pads is related to sinking, which dynamically changes the bond-interface force until it stabilizes, some improvement should be realized by delaying application of US power as discussed above. This delay time should be empirically determined for each type of substrate at its bonding temperature, while approaching its T_g .

Wedge-bond machine parameters for bonding to pads over polyimide-type substrates have been compared to those for bonding to pads over ceramics. If all machine variables were held constant, then bond-pull strengths will be lower (particularly low-modulus ones), compared to normal ceramic bonding. In other examples [9-32, 9-33], when ball bonding to Al IC chip pads over PI, even with 0.5 μm of Ti under the pad, a higher bonding force was found to be necessary (≈ 110 versus 80 gf). In addition, it was found that bonding to Au/Cu (with no hard Ni) pads on 90 μm thick PI required 350 ms versus 50 ms compared to bonding over ceramic [9-41]. Also, more power was required. The long bonding time may have delayed most of the welding until sinking and any load-induced cupping had stabilized. This is another option if the bonder has no adjustable delay in applying the US energy after tool touchdown.

High-volume, high-yield wire bonding on very soft substrates may require the combined use of high-frequency energy, pad metallurgy

optimized for bonding (i.e., soft bondable gold), DOE-machine set up, delayed application of US energy, and plasma or UV-ozone cleaning before bonding. Certainly, a full understanding of all normal bond reliability and yield issues is required, as discussed in this chapter and elsewhere in this book.

9.2.6 Additional Considerations When Using Wire Bonds in Packages Running at High Clock Rates in High-Performance Systems (HPS)

Inductance of Wire Bonds

Flipchips have the lowest inductance of any chip-interconnection method. However, short wire bonds have long been used in circuits operating over 1 GHz. A simple calculation, based on classical formulas for the self-inductance of a straight wire, can easily be made and gives a *quick estimate* that is adequate for many computations. (FEA modeling can be used for an exact solution.) Such an equation was given years ago by Terman [9-42] and is in modern electrical engineering handbooks as well.

$$L = 2 \times 10^{-4} \times \ell \times (\ln [4\ell/d] - 1 + \mu\epsilon) \quad (9-1)$$

where L is inductance in nanohenries, ℓ is the wire length, d is its diameter (both in μm), and μ is the permeability (assumed to be 1). The skin-effect correction factor, E , is a function of wire diameter and frequency. For 25 μm and 33 μm diameter Au wires at 1 GHz, its value is approximately 0.07 and can be neglected. For low frequencies, <100 kHz, E is 0.25. Larger diameter wires produce slightly smaller values of inductance. From Eq. (9-1), it can be seen that a wire bond has an inductance of approximately 1 nH/mm. A graph of measured values of bond inductance and mutual inductance is shown in Fig. 9-18 [9-43]. This figure includes values of both self- and mutual-inductance from nearby wires. Parallel signal wires were also shown to reduce the inductance somewhat. Another technique is to use special interspaced ground and signal wire structures with 50 Ω terminations to achieve performance at 2.4 GHz or higher [9-44].

The most important consideration in using wire bonds for high clock-rate packages is to design them as short as possible (~1 mm long). This can be accomplished by thinning the chips, recessing the chips, and placing the pads on the package-/board-substrate as near to the chip as practical, which usually means no long diagonal bonds.

9.2.7 Skin-Effect in Typical Package/Board Conductor Metal Structures

In most wire-bonded systems, it is necessary to have metallization structures consisting of two or more metal layers, as described above

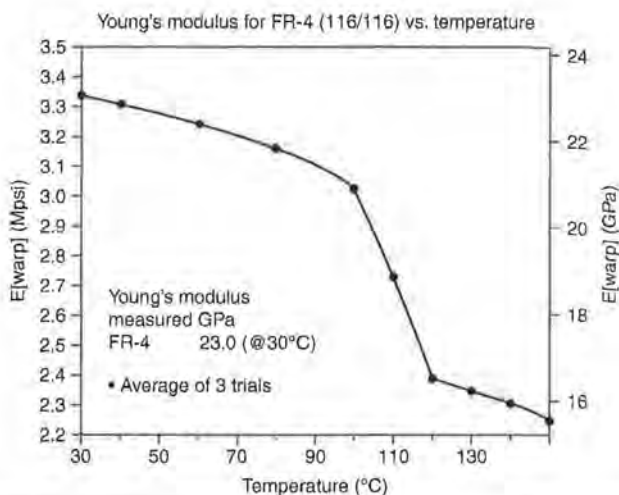


FIGURE 9-18 A typical plot of Young's modulus as a function of temperature for FR-4 glass-laminated epoxy printed-circuit boards. This particular board had a T_g of $\sim 110^\circ\text{C}$, but different manufacturers' FR-4 boards T_g can vary up to approximately 140°C [9-38] (© IEEE).

and shown in Fig. 9-15. The primary conductor is typically Cu or Al, but the structures may include a layer(s) of resistive (lossy) conductor(s) such as Cr, Ti, Pd, W, and/or Ni, the latter being both lossy and magnetic. These lossy layers are applied to serve several purposes in high-performance boards. These purposes may be to improve adhesion of the primary conductor to the polymer, to provide corrosion protection, and, in some cases, to act as a diffusion barrier. If thick enough, they also improve bondability by providing a rigid, noncupping bonding platform as discussed above.

The resistive layer or film can result in skin-effect losses at high frequencies, assuming that the same metal structure is used to conduct the signals. The extent of these losses will depend upon both the metal-film properties, its thickness, and its position with respect to any ground plane. From Fig. 9-15, if the resistive metal film lies between the primary conductor and the ground plane, the current will concentrate in that film, and losses will occur in the gigahertz-frequency range. See Table 9-6 for a listing of skin depths for metals used in high clock-rate conductors. These will depend upon the film-resistivity thickness and magnetic properties. Adhesion and corrosion-prevention layers can be quite thin ($\sim 1000 \text{ \AA}$) and, if so, will introduce negligible losses [9-45]. However, the layer must be relatively thick (3000 to 4000 $\text{\AA}$ for Ti) to act as a rigid platform for bonding on a soft substrate. At some combination of thickness and frequency, the skin effect will result in significant

Metal	Resistivity ($\mu\Omega\text{-cm}$)	Skin depth, δ (μm) at Frequency			
		1 GHz	10 GHz	20 GHz	40 GHz
Aluminum	2.65	2.59	0.82	0.58	0.41
Chromium	12.9	5.71	1.81	1.28	0.91
Copper	1.67	2.05	0.65	0.46	0.33
Gold	2.35	2.43	0.77	0.55	0.39
Nickel ^b	6.84(60)	0.59(12.3)	0.19(3.9)	0.13(2.8)	0.093(1.9)
Titanium	42.0	10.3	3.26	2.31	1.63

^aValues from Ref. 45 but with Ni corrected for (permeability) and all metals recalculated for 40 GHz (© IEEE).

^b $\delta = (\rho / f \times \mu \times \pi)^{1/2}$ where ρ = resistivity, f = frequency, $\mu = 4 \times \pi \times 10^{-7}$.

^cRange for Ni is calculated with a permeability of (50), first number for bulk Ni, and second number (in parenthesis) for high-phosphorus electroless Ni. Lower phosphorus content gives intermediate permeability values. All electroless Ni resistivity values are much higher than bulk Ni values and resistivity must be changed for calculations, due to P and other impurities.

TABLE 9-6 Skin-Effect Depth for Typical MCM Metallizations as a Function of Frequency^a

electrical losses! These losses can be avoided entirely if the hard-lossy metal layer is confined to the bond-pad region. To do this, the bond pads must be processed separately from the rest of the signal conductors, with some cost penalty. Alternatively, the signal could pass through a via to a good-quality conductor below the surface.

Most PCBs have the hard-resistive layer (usually Ni) on top of the primary conductor (usually Cu). Assuming that a ground plane lies below, as shown in Fig. 9-15 (without the hard under-layer), this will not cause skin-effect losses at high frequencies. The skin effect and other high-frequency losses in HPS have been extensively studied [9-45, 9-46, 9-47].

9.2.8 Conclusions

The solutions to increased wire-bond yields on pads over soft substrates are to increase the bond-pad metal thickness and area and apply a hard-metal underlayer (e.g., $\sim 0.3 \mu\text{m}$ thick Ti), a hard-metal top layer (e.g., 3 to $8 \mu\text{m}$ thick Ni), or some combination of these, capped with a highly bondable metal (e.g., Al or Au). This converts the pad into a rigid platform that does not "cup" or "sag" during bonding. Most workers using stiffened pads report that essentially "normal," or with ~ 10 to 20% higher than normal, bonding parameters are required for various soft substrate bonding. The material properties of the polymer were discussed, and bonding was generally correlated to the elastic modulus of the polymer or

laminate and to the yield strength of the metal bond-pad layers. The higher these values, the more rigid the material and the less cupping during bonding for a given pad structure. If the polymer has a low modulus (or is bonded near its T_g), then the pad must be larger to prevent it from dynamically sinking into the soft material or the application of the US energy should be delayed (5 to 10 ms) until the pad sinking has stabilized. Sinking, as well as cupping, can lower the bond yield. Thus, the material properties are at least as important as the actual bonding-machine set up in achieving high-yield bonding on soft substrates. Even when using the above solutions, high-yield bonding will occur only if the best metallurgical, bonding, and cleaning (UV-ozone or plasma) procedures are followed, as given in Chaps. 5, 6, and 7.

9.3 Wire Bonds in Extreme Temperatures/Environments*

9.3.1 Introduction

This is a brief introduction to the materials and requirements for wire bond interconnections that can be used in packaging chips for extreme high- and low-temperature (HTE and LTE, respectively) environments. Devices capable of operating in these environments are needed for future space probes on other solar system planets, well-logging, geothermal measurements, sensors near rocket and jet engines, automobile engines, etc. Modern SiC and other high-temperature devices are capable of operation up to 500°C, although packaging materials/technology for such high temperatures can be both challenging and expensive! The normal metallurgy used for Si chip interconnections, Au-Al (wire bonds, aluminum metallization) fail in HTE, but generally can be used in LTE. The required material changes, such as Au-Au, (or other noble and monometallic interfaces), substrate/chip CTE matching, etc., are necessary for systems to survive in these thermal and changing-temperature environments. Some of the concepts/problems below are described in Chaps. 2 and 5, and in the literature [9-48, 9-49, 9-50, 9-51, 9-52]. Reference [9-48] is a comprehensive overview of materials, and wire bonding for extreme environment devices.

9.3.2 High Temperature Interconnection Requirements

The most commonly used Au-Al wire bonds should be avoided in the HTE range, along with any other metallurgical interfaces that form brittle intermetallics and/or Kirkendall voids. Gold-gold bonds can improve with time and temperature rather than degrade (see Chap. 5,

*Part of this material is from a chapter in: Suhir, E., Lee, Y. C., and Wong, C. P., *Micro-and Opto-Electronic Materials and Structures*, Springer, 2007, Vol. 2, Chapter 4, Harman, G. G., *Metallurgical Interconnections for Extreme High and Low Temperature Environments*, pp. 121-133.

Fig. 5-16). Therefore, a clear preference is given for high-melting point monometallic interfaces or metals that form solid solutions—gold (or other noble metals) in the HTE environments for both wire and flip-chip bonds. Gold bumps/balls can be used in place of the normal solder-ball flip-chip interconnections. Such chips can be ball-bumped or stud-bumped to Au pads, and the entire chip thermocompression/thermosonic bonded to gold metallization on (matched CTE) ceramic substrates. This results in reliable HTE flip-chip interconnections (provided the chip and substrate have approximately matched TCEs, with the substrate a little higher than the chip).

Metallurgical fatigue damage to wires can occur during large ΔT temperature/power-cycling in both HTE and LTE. Also, deep well-logging, and sensor applications can be cycled through wide temperature ranges. McClusky [9-50, 9-51] has reported that high-temperature-annealed Al wires have decreased fatigue life as well as the wire interconnection integrity, even if the bonded interface (the bond nugget) remains strong. In this case temp-cycling went up to 200°C. No data exist for higher temperature cycling of large (or any) diameter Al round and ribbon wires. One could assume that large ribbon wire, since it is flexible in the plane of the bond loop, will have a longer fatigue life at high temperature than equivalent cross-section/metallurgy round wire. An example of large-diameter Al wire fatigue was shown in Chap. 8, Fig. 8-19. Large-diameter

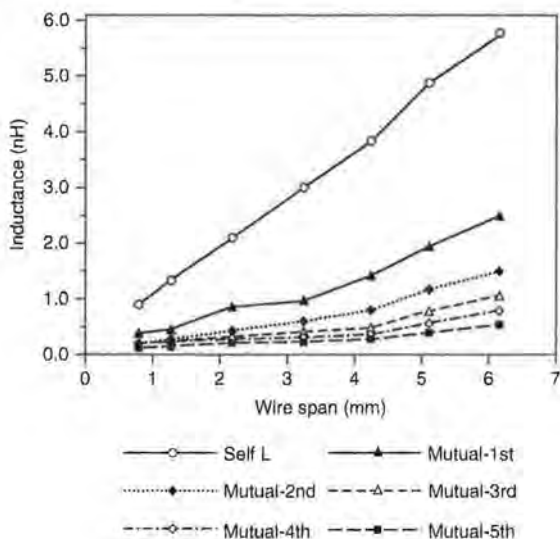


FIGURE 9-19 Gives plots of both self- and mutual-inductance of wire bonds as a function of wire span [9-43] (© IMAPS).

round wires are stiff, and stress is concentrated at all bends and at the weld attachment (bond heel), where the fatigue failures usually occur. Small-diameter wire (e.g., 25 μm) is flexible, and most fatigue stress is applied to the heels of the bonds, where the failures occur. A variety of factors (wire diameter, shape, loop height, metallurgy, including additives/dopants, and strain-rate) determine the fatigue susceptibility and life of a wire bond (high, smooth loops and low-bond deformation give best protection against fatigue, for fine-diameter wires). Gold wire is more fatigue resistant than Al wire at typical thermal cycle, low-strain-rates, and temperatures up to 125°C [9-53]. No equivalent data are available for higher temperatures.

In HTE (but not LTE), the current carrying capacity of wire bonds must be appropriately derated to avoid burnout. Al wire (with its 660°C melting point) must be derated more than Au (melting point 1064°C). HTE will result in annealing *small-diameter* Al wires causing the breaking load and bond-pull strength to decrease to less than 30% of their initial values. *Large-diameter* Al wire ($\geq 100 \mu\text{m}$) is normally annealed when produced, so its breaking load will decrease only slightly. Aluminum-aluminum or Al-Ni welded bond interfaces will remain strong at high temperatures, so any annealing of the wire (tensile strength decrease) is not normally considered a reliability problem. However, its temperature-cycle fatigue-life may be shortened, as above [9-51], and this must be determined before implementation. Gold wire for ball bonding is already annealed, and its strength will change minimally. However, the strength of small-diameter gold wire used for wedge bonding will anneal (soften), but less than equivalent Al wire. Little work has been done to determine the effect of high-temperature cycling on fine-diameter Au and Al wire fatigue. Temperature studies, up to 125°C, have shown a general decrease in fatigue lifetime with temperature, and also a significant dependence on strain rate [9-53]. (See comments in Chap. 3.) Modern gold wires have special stabilizing impurities, and it is assumed that these improve the high-temperature fatigue life from the past studies; however, typical aluminum wires are unchanged from the past.

Platinum wire is used in HTE, but it requires high-bonding force and work-hardens significantly during US wedge bonding, similar to Cu (Chap. 3). Wedge bonding with it can crater SiC, one of the hardest known materials [9-49]. Pt and Pd have much lower electrical conductivity, only ~20% of Au or Al, as well. In general, Pt and Pd wedge bond best at high temperatures ($\geq 300^\circ\text{C}$) (thermosonic bonding). Both can be ball bonded, but little information has been published on that. Sometimes Pt and Pd are used in LTE systems *because of their low thermal conductivity* (~20% of Au). In the 75 to 150 μm (~3 to 6 mil) diameter range, Pt and Pd may be welded to substrates and packages by electrical discharge methods, if appropriate for an application (see Chap. 2).

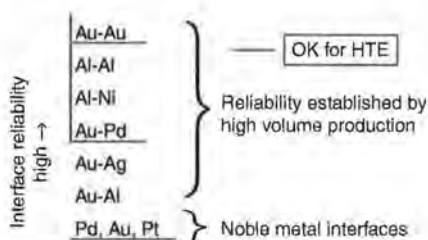


FIGURE 9-20 Metallurgical interfaces that can be used reliably in both extreme environments. All are acceptable for LTE. However, only the underlined/boxed ones are acceptable for HTE.

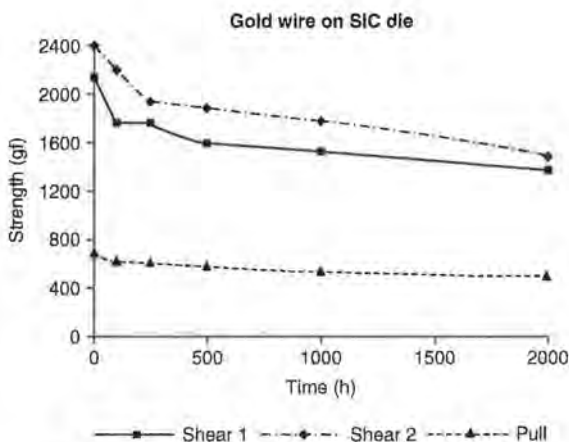


FIGURE 9-21 Average pull/shear strength of 250 μm diameter Au wire, wedge bonded at 225°C to Ti/Ti:W/Au die metallization (Au plating was 3 μm thick), as a function of storage time at 300°C [9-49] (© IEEE).

An overview of metallurgical interface (bonding) reliability for both HTE and LTE is shown in Fig. 9-20.

Examples of gold bond interface lifetimes, stored at 300°C, were given by Johnson as shown in Fig. 9-21. This stable life is in agreement with discussions in Chap. 5 for Au-Au bonds.

9.3.3 Low-Temperature Environment Interconnection Requirements

For LTE and intermediate temperature ranges, up to about 125°C, conventional interconnections (Au and Al wire bonds) to Al chip metallization (bond pads) are acceptable. One would not use a normal

Component	Material	CTE (ppm/°C)	Thermal Cond. (W/cm·°C)
Chip	Si	2.6	1.57
	SiC	1–3 (T-dep)	~5 (>T dep)
	GaN	~3	1.3
	GaAs	5.7	0.48
Substrate	SiC	1–3	0.8–2
	Si ₃ N ₄	2.5–3.3	0.3–0.6
	AlN	4.6	1.75
	Al ₂ O ₃	~6	0.35
	BeO	~6–7	~3

Components should be chosen to minimize thermal expansion differences. In the table, similar color chip and materials are appropriate matches.

(Color distinctions wash out in B & W and should be checked in the color CD.)

Note: thermal-conductivity values can/will change at low temperatures and exact data may not be available. (Data from SRC-CINDAS.)

TABLE 9-7 Some Material Properties of Chips and Substrates for Use in both High and Low Temperature

laminate substrate, but rather a ceramic one. See Table 9-7 for some material property choices in designing packages. Components should be chosen to minimize the expansion differences for temperatures down to about 55°C.

9.3.4 Packaging Effects at Extreme Temperatures

The packages for HTE will usually be made of metal/glass/ceramic (classical hermetic hybrid packages). Package reliability problems from hysteresis, creep, and/or cracking of normal glass-metal seals (Kovar-glass) in hermetic packages can cause failure during temperature cycling in both HTE and especially in LTE. The glass-metal seals undergo expansion/contraction hysteresis possibly resulting in cracking or delamination in the range starting below ~100°C. In HTE, any leads extending through the softened glass seals, at ~300°C, will yield under mechanical stress resulting in possible damage to any wire bonds connected to them. Diffusion processes generally follow the Arrhenius equation and will be greatly accelerated in HTE. Possible failure of metal adhesion layers between gold metallization and ceramic, as well as any diffusion barriers under/over the chip metallization, must be considered as potential reliability hazards that could weaken wire bonds attached to them.

Although chips used in LTE can be Si based, those used in HTE will not be. Most likely they will be SiC or possibly GaP, GaAs, with Si-Ge being used in the low HTE range. Their metallization will most

likely be complex layers with noble metals and diffusion barriers between the chip and the conductors. The die attach for HTE will have to be metallurgical rather than polymer (epoxy), as currently used on normal devices. In some intermediate temperature ranges, silver-glass (maximum $T \sim 350^\circ\text{C}$) may be an acceptable die-attach material. For SiC chip die attach, some possibilities could be Ni/Ti/TaSi₂, Ti/TaSi₂/Pt, Ni/Ti/Pt/Au, or Au-Sn. Currently, neither these nor any other die-attach materials have been qualified for HTE (up to 500°C). Thus high-temperature wire-bond development is far more advanced than die attach and other packaging materials/technologies.

9.3.5 Summary

The material properties and requirements for wire bond and Au ball-bumped flip-chip interconnections that can be used in packaging chips for extreme high- and low-temperature environments [from $\sim 500^\circ\text{C}$ (HTE) down to about -100°C (LTE)] have been described. The most commonly used Au-Al wire bond interfaces should be avoided in the HTE range, along with any other metallurgical interfaces that form brittle intermetallics and/or Kirkendall voids. Gold-gold bonds (and other noble metals) are stable or improve with time and temperature (see Chap. 5); thus a clear preference is given for gold (or other noble metals) in the HTE environment for both wire and flip-chip bonds. Monometallic interfaces, such as Al-Al are also reliable. For LTE, and in intermediate temperature ranges, conventional interconnections (Au-Al wire bonds) to Al-chip metallization (bond pads) are acceptable. (Also, normal flip-chip solder bumps are acceptable, without plastic under-fill.) Information on other materials, such as CTE matching between chip and substrate, was given. It is concluded that, with the proper selection of materials, interconnections can be reliable over a wide range of extreme temperature environments. For an overview of the entire high-temperature electronics field see Kirschman [9-54].

Appendix 9A Wire Bonder Looping

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By Lee Levine

9A.1 Introduction

In its simplest form a wire bond is a segment of wire interconnected (bonded) at each end to allow completion of an electrical circuit. The segment of wire between the bonds is called the loop. Historically ball-bond loops were 10 to 15 mil in height with a smooth, unstressed shape. As wire-bonding machines were automated, producing

low-stress loop shapes without stretching the heat affected zone (HAZ) directly above the ball became more difficult because the dynamics of automated machines were different from manual, operator-controlled machines. The HAZ is the region above the ball that was heated by the melting of the wire that formed the ball. Its properties are significantly different from the bulk wire because the heat recrystallizes the grain structure and recrystallized grains are weaker than the cold worked grains in the wire. Controlling the chemistry of the 99.99% (100 ppm residual trace elements) became necessary to both refine the grain size in the recrystallized HAZ and provide additional strength. The addition of Beryllium in the 7 to 10 ppm range provided these properties and allowed the development of high-speed automated wire bonders. Today all 99.99% gold bonding wire is alloyed within the 100 ppm residual impurities range. However, some special purpose wires can have a higher level of dopant than this (not 99.99/Au). Each wire manufacturer has a variety of alloys with different properties tailored to provide optimized performance for difficult applications. Specialized machine motions were developed to mimic the behavior of manual machine operators. Observations that manual machine operators often made a motion away from second bond after forming the first bond lead to the development of the reverse bond motion. Bending the wire in the HAZ cold works the wire, changing its mechanical properties. Specific bending motions, such as reverse motion bending (bending first away from and then toward second bond), are used to control final loop height and shape and to reduce sag near second bond. Pulling the wire just before bonding the second bond straightens the wire and reduces the final loop height.

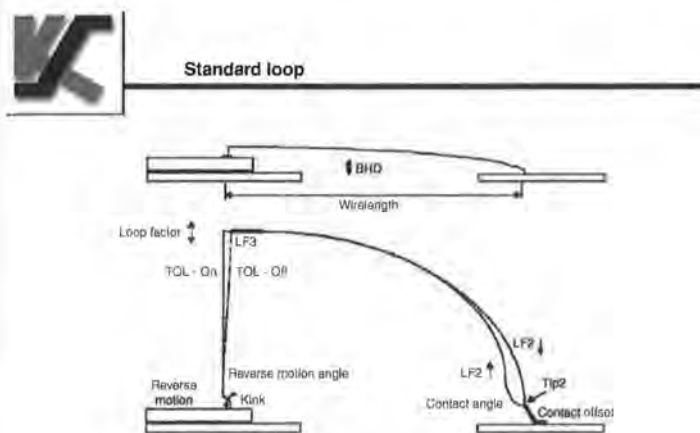
Currently state-of-the-art packages have wire pitch (the distance between adjacent wires) of 30 μm . The demands of fine-pitch bonding in turn drive the requirements for longer wire length, smaller wire diameter, smaller capillary tip diameter, straighter wire loops with less sagging, and better machine motion control. Because fine-pitch devices typically have more wire interconnections they require faster bonding motions and higher acceleration to maintain productivity and profitability. These demands have been met by continuously studying the wire-bonding process; wire, tools, hardware, and software. All have been continuously improved through the use of designed experiments and advanced analytical tools that have enabled improved process controls and enhanced capabilities.

9A.2 Machine Motions and Trajectories

Wire bonders move in smooth, continuous, coordinated motions, with all three axes (X, Y, and Z) moving simultaneously. Wire is fed through the capillary and bent by the machine motion to provide the required shape. Motions are calculated on the fly and adjusted so that each machine axis travels along a precisely calculated trajectory.

Motion trajectories must be controlled and coordinated to within only a few microns of tracking error. A variation of a few microns can significantly affect loop shape and repeatability. Wire payouts and bends need to be adjusted on the fly to account for changing wire lengths caused by die placement variation. All this needs to be accomplished while bonding up to 16 wires/s, with acceleration rates exceeding 12Gs in XY and 150Gs in Z. The latest wire-bonding equipment employs new, faster, and more accurate servo controls, which enable more repeatable looping and more complex shapes. The simplest standard wire-bond loop employs four separate motions from the ball bond to second bond. The formation of more complex loop shapes may employ more than 12 motions. Kinks, bends, flat segments, and smooth curved portions are all formed by programmable loop parameters within the software. Wire lengths are controlled and adjusted based on both the modeled loop shape and actual calculated distances between the ball and second bond. As each die is indexed to the bond site, the machine vision system uses pattern recognition to locate the die and leads. Machine intelligence, then, corrects the location of each bond and adjusts the metered wire length for repeatable loop shape and height.

Accurate servo controls enable more repeatable looping and more complex shapes. The simplest standard wire-bond loop employs four separate motions from the ball bond to second bond as shown in Fig. 9A-1. The formation of more complex loop shapes may employ



Packages: QFP (<170 mil wire), discrete
 Status: Common basic loop shape
 Motions: 4 XYZ between first and second

FIGURE 9A-1 The formation of a standard loop.

more than 12 motions. Kinks, bends, flat segments, and smooth curved portions are all formed by programmable loop parameters within the software. Wire lengths are controlled and adjusted based on both the modeled loop shape and actual calculated distances between the ball and second bond. As each die is indexed to the bond site, the machine vision system uses pattern recognition to locate the die and leads. Machine intelligence, then, corrects the location of each bond and adjusts the metered wire length for repeatable loop shape and height.

9A.3 Loop Shaping

The main reasons for shaping a wire loop are to provide clearance and avoid interference (electrical short circuits) from adjacent wires as well as from the die or substrate. Some wedge-bonding applications demand controlled impedance where the wire length, height, and shape are controlled to tight tolerances. The shape and features of the wire, the wire "loop," have changed significantly over time as machine capabilities and device requirements have evolved and package density has increased.

9A.4 Prebending, Cold Work During Looping Trajectory

Bonder motions within the HAZ can be used for cold working and bending functions. Standard wire-bond loops use a reverse motion in the HAZ to bend the wire away from second bond initially, cold working the HAZ. When the looping trajectory bends the wire in the



FIGURE 9A-2 Examples of long low loops. (Courtesy of Oerlikon.)

HAZ back into a vertical position, the cold worked HAZ will be stiffer and the wire loop will be more erect with less sagging than it would have been without the cold work from the reverse motion. Other motions can be used to provide additional bends in the wire, providing useful shapes. These shapes can provide additional standoff near second bond, as required in ball grid array (BGA) packages, with power and ground rings in the vicinity of second bond. They can also provide flat (parallel to the die surface) portions of the loop with sharp bends descending to the second bond, as in the chip scale packages (CSP) or worked loop. Wire stiffness needs to be optimized so that these bends can be produced uniformly. New wire types are being developed to provide both a high stiffness above the HAZ and a soft ball for improved bondability.

9A.5 CSP and BGA Looping

The ability to shape a wire-bond loop, with well-controlled bends and kinks, has been in continuous development for over 12 years [9A-1, 9A-2]. The first worked loop shape patents were granted in 1993 [9A-3]. These shapes enabled the development of the CSP loop. The CSP loop, with additional wire bends designed to provide buss bar clearance near second bond, evolved into BGA looping. Now, the demand for thin-profile, *stacked-die*, and *multichip packages* is pushing development of even lower loop height levels. Today's state-of-the-art wire bonders may offer the capabilities to support a library of as many as 20 loop shapes. Additional new loop shapes are continually being developed to accommodate packaging design requirements. Loop shapes within the bonder library have programmable



FIGURE 9A-3 Stacked die looping. (Courtesy of K&S.)

parameters that enable formation of the desired shape but also provide flexible controls for the large variety of packages that are encountered.

9A.6 Stacked Die and Multi-Chip Packages

The advent of stacked die packages has also placed new demands on wire bonders. More die layers need to be integrated into thinner and thinner packages. Production dice, commonly thinned to 100 μm thickness, are now down to 75 μm . Even 50 μm dice are being introduced into mass production. Stacked thin cantilever dice, with cantilever exposure of up to 5 mm, deflect significantly during bonding. This deflection effects bonding. Differences in deflection between bond pads located in the corner of the die and those located in the center of the die edge are large; therefore, bonding variability as a function of pad location has to be taken into consideration. In addition, finite element modeling (FEM) and high-speed video photography of the die deflection have enabled good understanding of this process and provided good working solutions to this problem. Time delays required for the die to deflect and recover are significant and reduce throughput.

Multichip packages often require several different type loops, at different second bond elevations (Z axis) within the same package. Often they require chip-to-chip bonding. Chip-to-chip bonding has a whole range of additional requirements because the capillary cannot touch the die face without damaging sensitive components on the die. The stand-off-stitch bond (SSB) is a sequence of three bonds that addresses this application. First a ball bump is bonded on Die 1 and terminated forming a new ball under the capillary. The second ball is then bonded to Die 2 as a standard wire bond. The second bond is then bonded on top of the bump bond on Die 1 completing the 3-bond sequence. The SSB is called a reverse bond because the ball bond is

The issue is that the lower and longer the loop is, the lower is the productivity—require more motions



FIGURE 9A-4 Loop height reduction using the capillary. (Courtesy of K&S.)

normally on the lead and the second bond/bump are on the upper die. This avoids placement of a second bond directly on the die surface, which would be a reliability risk. SSB height is very low because the second bond and bump are normally on the upper die. However, bond speed for the 3-bond sequence is slower than standard bonding because of the additional process steps.

9A.6 Capillary Forming for Lower Loops

Recently, new forward bonded loop shapes have been introduced that can produce heights of less than 75 μm without sacrificing throughput. Achieving these ultra-low loop shapes is very important for the lowest die of a stacked dice package, especially when the wires are underneath an overhanging cantilever die. In this loop profile the ball bond is produced and as the capillary is moving from reverse bond position the capillary descends to the ball-bond surface, compressing the wire against the ball bond. The capillary then moves to second bond position and completes the second bond. This loop profile can achieve loop heights less than 50 μm with only a small throughput cost.

9A.7 Capillary Shape and Its Effect on Drag/Friction

Capillaries transfer ultrasonic energy to the bond and control weld size and shape. Their internal and external shapes and dimensions provide the necessary features that form the bond. They also are a source of friction during wire feed. Friction and drag are necessary to control the flow of wire and provide tension, but too much friction can break bonds and wire, stretch the ball neck in the HAZ, result in deformed loop shape, and scrape and tear the wire surface.

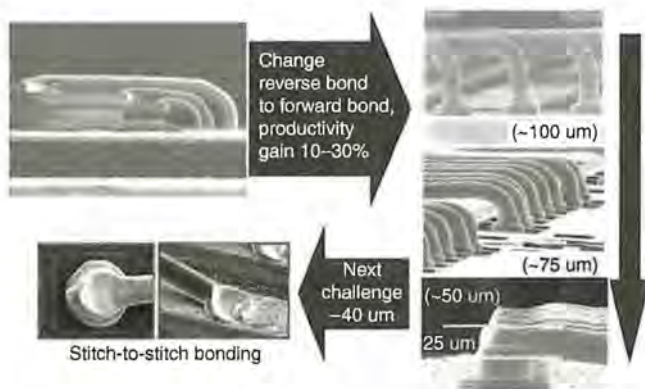


FIGURE 9A-5 Ultralow loops. (Courtesy of K&S.)



FIGURE 9A-6 Wire bond loop defects. (Courtesy of Oerlikon.)

Controlled low-drag capillaries, with design features optimized for long capillary life, can add value to the process. When implemented in the wire-bonding process, these unique bonding tools provide greater loop height control and shape stability, significantly reducing looping failures typically found on wires formed with a conventional capillary.

9A.8 Role of Wire

Wire properties play a significant role in a wire bonder's ability to produce accurate, repeatable loops. Over the years these properties have undergone continuous improvements to enable the production of the longer, lower, straighter loops required by today's packages. Gold bonding wire is normally specified as 99.99% (four 9s) purity, while chemistry within the residual 100 ppm impurities is carefully controlled to provide the required mechanical and electrical properties. New alloys that have recently been introduced to the market are in the high three-9s range to provide improved long-term reliability in very fine pitch (<50 μm ball diameter) applications without significantly sacrificing electrical properties.

9A.9 Ball and Stud Bumping

Ball and stud bumping can be classified as looping variants because the bonder terminates the wire above the ball without making a loop. There are three varieties of stud bumps. Normal ball bumps terminate within the HAZ because this region is the weakest region of the

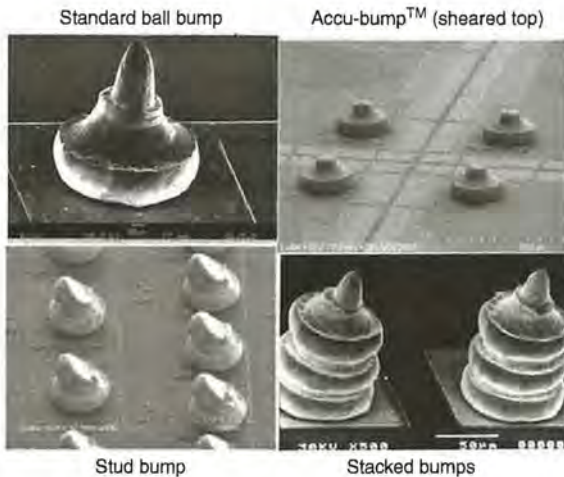


FIGURE 9A-7 Variants of bump bonding. (Courtesy of K&S.)

wire and the wire preferentially breaks in the weakest region. The bonder forms the ball bond and then rises to the correct height for a new ball, the wire clamps close, and the bond head again ascends to the EFO firing position. The wire breaks within the HAZ during this motion. Wire alloying can significantly affect the wire recrystallization temperature and have a large effect on the height and variability of the broken wire tip. An alloy with a higher recrystallization temperature will have shorter tails and less variability.

Newer bonders, with better Z axis control, are capable of forming the ball, rising a controlled distance of only a few microns, and then moving horizontally to shear the wire above the ball bond and produce a flattened bump. The additional motions require additional time but the process is still very fast (>20 bumps/second). Planarity is adequate for many applications.

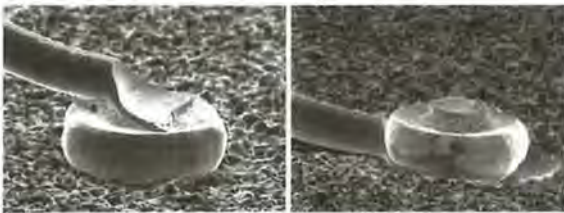


FIGURE 9A-8 Bumps for improved reliability. (Courtesy of K&S.)



FIGURE 9A-9 Heavy wire wedge and ribbon bonding. (Courtesy of Orthodyne.)

Stud bumps are produced by first forming the ball bond; the head rises a short distance then descends and forms a second bond on the edge of the ball. The wire/loop has the appearance of a cotter pin with a total loop height of approximately 3 to 5 mil. In most cases stud bumps are dipped in a conductive adhesive for interconnection of the bump to the substrate.

Wedge bonding has required an additional machine motion axis in order to align the wedge tool, which is directional during bonding. This additional axis resulted in the wedge-bonding process being significantly slower and it also had less bond placement accuracy. Historically, both fine and heavy wire-wedge bonding had simpler motions, "H" or "trapezoidal" motions were most common. In an "H" motion the tool lifted straight up off first bond, moved to top of loop, moved horizontally toward second bond and then down. In a trapezoidal motion loop the tool lifted off at an angle, usually close to the angle of the tool feed hole, reached top of loop and moved towards second bond. At a programmed point the tool began an angled descent toward second bond. Recently more complex loop shapes, with pull-out motions near second bond and better axis controls, have become available. Bond shift is now available so that first and second bonds do not have to be as closely aligned as previously required.

Because of its low inductance and high current carrying capacity, ribbon wire is often required. Often in microwave, Rf devices design



FIGURE 9A-10 Heavy wire wedge bonded modules. (Courtesy of Orthodyne.)

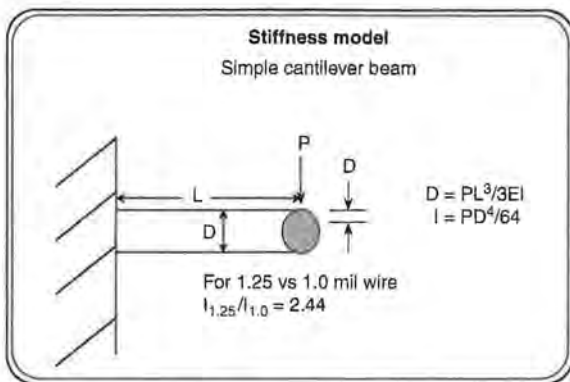


FIGURE 9A-11. Wire stiffness model.

criteria requires ribbon bonds that are nearly horizontal, the shortest length between first and second bonds.

Ribbon bonding is a variant of wedge bonding. Ribbon wire is normally produced by roll forming round wire to flatten it.

9A.10 Stiffness—Young's Modulus

Even though wire is thin, it should be understood as a structural element. The simplest model of a round cantilever beam provides adequate understanding of the relationships between the significant variables (deflection, length, diameter, material). Stiffness, defined as the resistance to deflection under a load, has a cubic relationship with length and a quartic relationship with diameter (a 10% increase in length will have a 33% increase in deflection and a 10% decrease in diameter will have a 46% increase in deflection). Wire chemistry and treatments can have a smaller effect on Young's modulus (E), but the effect is linear.

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