UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Patent No. 11,081,503

Inter Partes Review No. IPR2025-01494

PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.*

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c. 1[b]: "a pad portion disposed on the array substrate; and" 60

d. 1[c]: "an integrated circuit disposed on the pad portion and comprising a bump portion;" 61

e. 1[d]: "wherein: the pad portion comprises a first sub-pad unit comprising an inclined first pad and a second sub-pad unit comprising an inclined second pad;" 63

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h. 1[g]: "the bump portion comprises a first sub-bump unit comprising an inclined first bump and a second sub-bump unit comprising an inclined second bump;" 64

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e. 1[d]: "wherein: the pad portion comprises a first sub-pad unit comprising an inclined first pad and a second sub-pad unit comprising an inclined second pad;" 86

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g. 1[f]: "the pad portion is electrically connected with the bump portion;" 93

h. 1[g]: "the bump portion comprises a first sub-bump unit comprising an inclined first bump and a second sub-bump unit comprising an inclined second bump;" 94

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Petitioner BOE Technology Group Co., Ltd. ("Petitioner" or "BOE") petitions for *inter partes* review of claims 1-10 of U.S. Patent No. 11,081,503 ("the '503 patent" (Ex. 1001)) in accordance with 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq*.

I. INTRODUCTION

The '503 patent relates to mounting an integrated circuit to an array substrate. (EX1001, Title.) Normally, the array substrate has connection pads that are aligned with corresponding bumps on the integrated circuit. (EX1002, ¶11.) But if the substrate array expands or contracts, misalignment may occur between the pads and bumps. (*See* EX1001, 1:50-56.)

The '503 patent discloses techniques for preventing misalignment. The pads and bumps are "inclined" (e.g., parallelograms) rather than straight. (*See* EX1001, claim 1.) This way, misalignment between the pads and bumps, shown in FIG. 4, can be mitigated by shifting the integrated circuit in the Y-direction (i.e., up or down) as shown in FIG. 5. (*See* EX1001, FIGs. 4-5.)

Fig.4

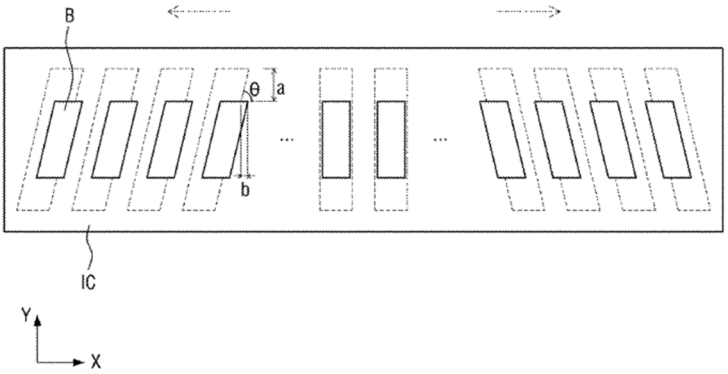
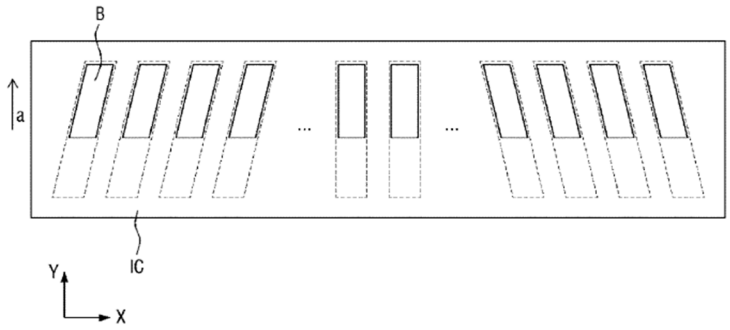


Fig.5



Using inclined pads and bumps to prevent misalignment was not new at the time of the '503 patent in 2014. For example, Wildes discloses "connection pads are formed in ***fanout arrays*** . . . ***allowing significant variations in the dimensions of the respective substrates being electrically connected to be accommodated***." (EX1004, 2:10-15 (emphasis added)[1].) Likewise, Lieshout "provide[s] a connection device wherein ***misalignment problems for IC chips***, notably in a flip-

[1] All emphasis and annotations, such as highlighting and coloring, are added unless otherwise stated.

chip bonding area, are counteracted." (EX1005, 2:21-23.) Similarly, Imaoka discloses "***radially*** arranged" terminals for mounting a chip component in a display device. (*See*, *e.g.*, EX1006, claim 17, FIGs. 2A-B.)

Petitioner submits that the challenged claims are unpatentable for the reasons set forth in this Petition, as supported by Dr. Chen. (EX1002.)

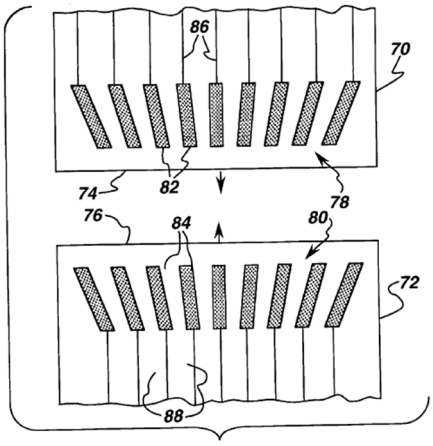
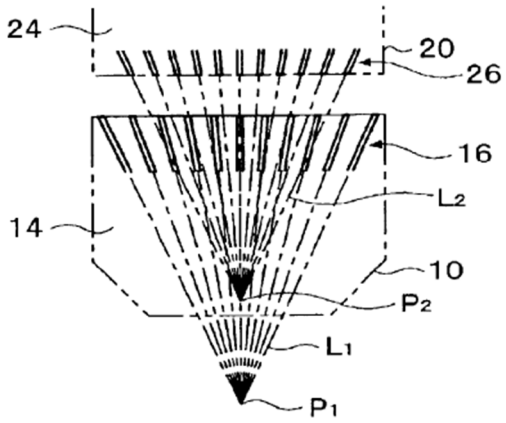
II. OVERVIEW OF THE TECHNOLOGY

A display can have an integrated circuit that provides electrical signals to control the pixels. (EX1002, ¶11.) The integrated circuit can be mounted onto an array substrate of the display using conventional techniques. (*Id*.) Dating back to the 1980s, chip-on-glass ("COG") technology involves mounting the integrated circuit (specifically, its bumps) onto a glass substrate, for example. (EX1007, 138.) Flexible substrates were also common. (*See* EX1005, 5:25-6:1, 8:27-9:7; *see also* EX1036, Abstract.) Further, elongated bumps (as opposed to square or circle bumps) on integrated circuits were known to be beneficial in as early as 1990. (EX1002, ¶11; *see also* EX1029-1033.)

It was well-known that misalignment can occur between the integrated circuit and the array substrate, for example, due to stress during manufacturing. (EX1002, ¶12; EX1005, 1:11-2:6.) The deformed substrate may cause the connection pads on the substrate to offset from the bumps on the integrated circuit. This can happen to either flexible or normally rigid substrates (e.g., plastic, glass).

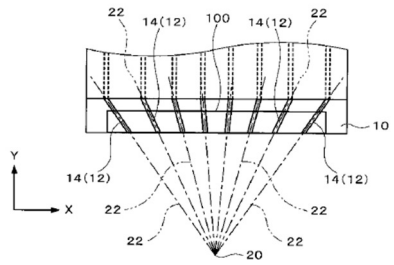
(*Id*., 5:25-6:7)

At the time of the invention, engineers regularly used diagonal, or inclined, layouts for precision electrical alignment for displays. It was a cheap, effective, and well-known design. (EX1002, ¶13.) Misalignment was fixed by simply shifting the substrate or the integrated circuit in the Y-direction. Such designs were prevalent in the industry, as shown by examples below.

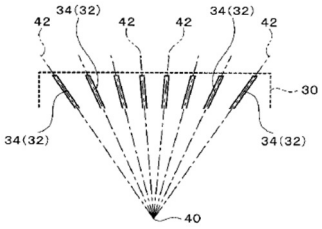
Wildes (EX1004) –Published in 1999	**Imaoka (EX1006) – Published in 2003**
 *fig. 6*	 FIG. 2A

Ishida (EX1016-1018) – Published in 2006

【図３】



【図４】



FIGs. 3-4

Yamamoto (EX1019-1021) – Published in 1992

図1

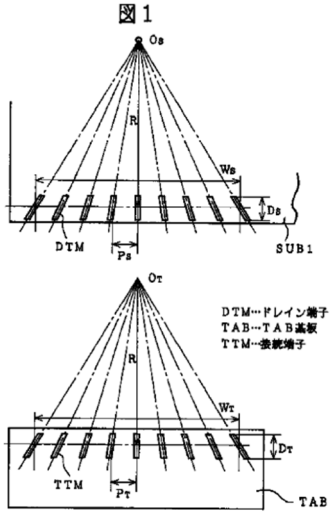


FIG. 1

Mochida (EX1025-1027) – Published in 2010

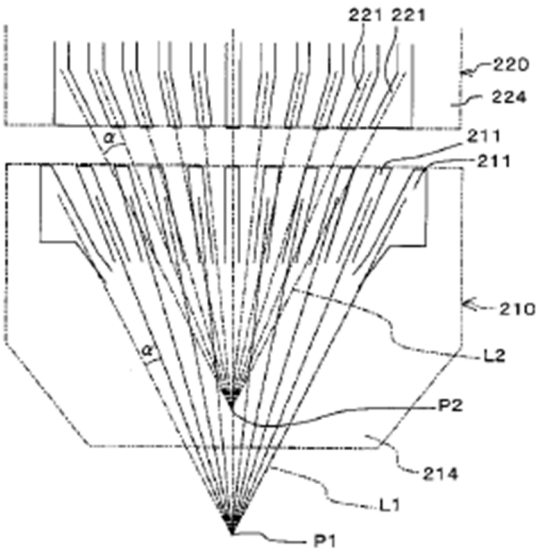


FIG. 23

Yamada (EX1015) – Published in 2007

FIG. 2

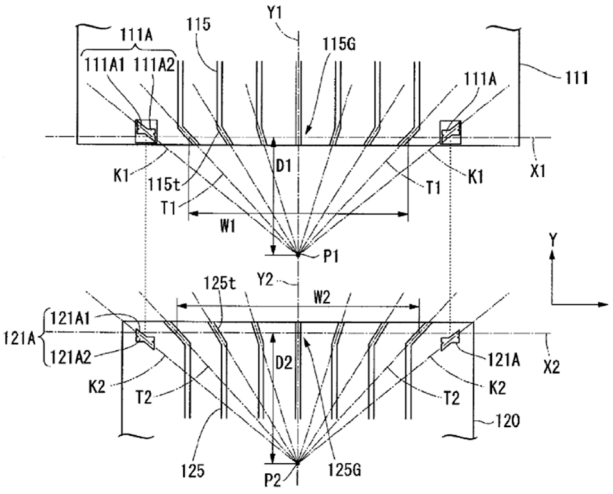


FIG. 2

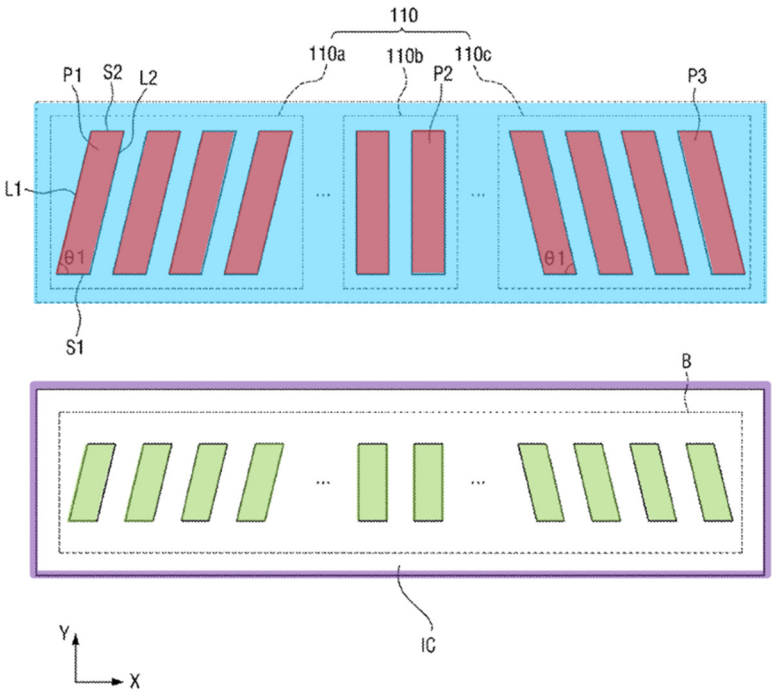
Numerous patent and patent publications, including those discussed herein, disclose this idea before the earliest priority date of the '503 patent. (EX1002, ¶13.)

III. THE '503 PATENT

A. Summary

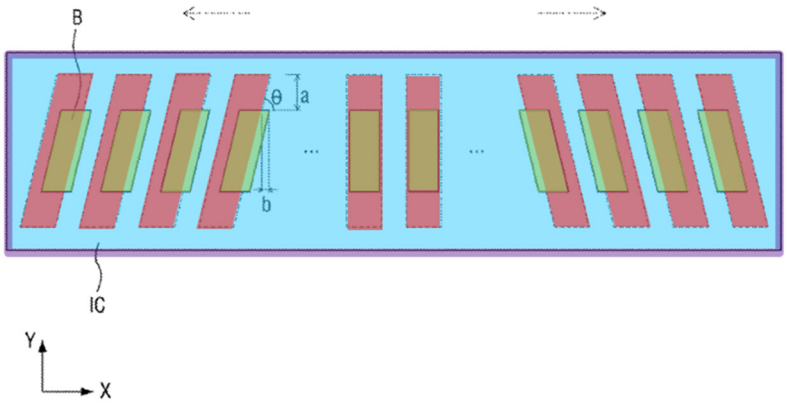
The '503 patent is directed to mounting an integrated circuit to an array substrate. The '503 patent provides "an ***array substrate*** capable of preventing misalignment between the bumps of a driving ***integrated circuit*** and the pads of a pad unit. . . ." (EX1001, 1:66-2:2.) For example, in FIG. 2, the ***pad portion 110*** on the array substrate comprises inclined pads such as P1 and P3. Similarly, the data driving ***integrated circuit IC*** comprises inclined ***bumps B***.

Fig.2



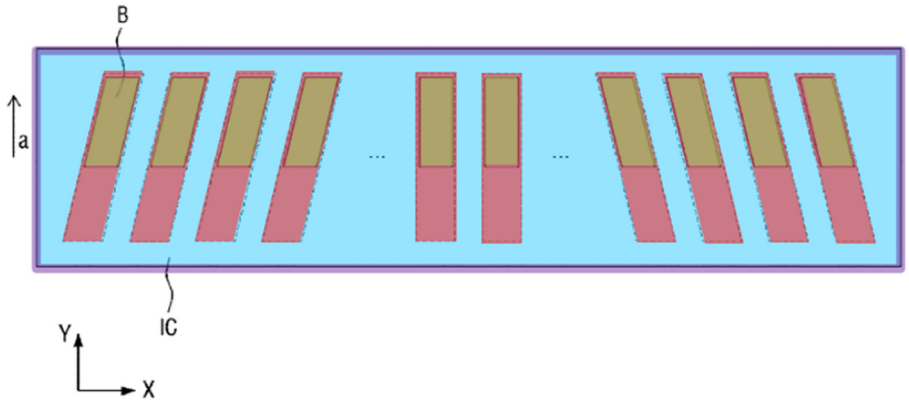
Misalignment may occur if the array substrate expands or contracts. An exemplary misalignment between the ***pad portion 110*** and the bumps ***B*** is shown in FIG. 4. (EX1001, 6:48-60.)

Fig.4

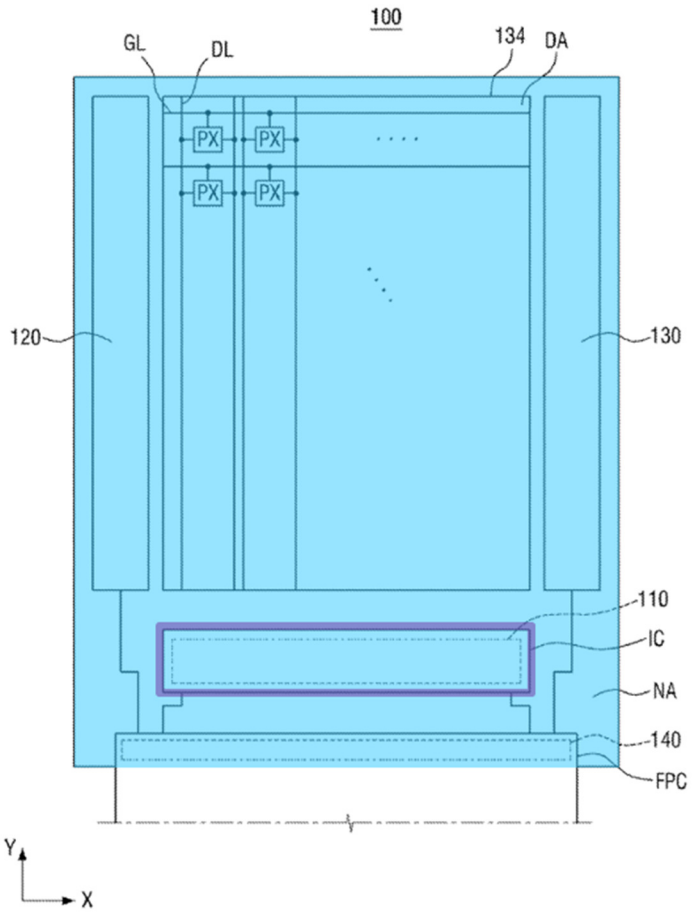


The "inclined" pad portion and bumps mitigate the misalignment problem. Alignment can be achieved "by moving the data driving integrated circuit IC toward the positive second direction +Y by a distance a, as illustrated in FIG. 5." (EX1001, 6:67-7:6.)

Fig.5



The techniques above can be applied in a conventional electronic device, as shown in FIG. 1. (EX1002, ¶20.) As shown, "data driving ***integrated circuit IC***" is mounted on the pad portion 110 of ***array substrate*** 100. (EX1001, 4:19-49.) The '503 patent states that the pad portion may be a "Chip-on-Glass (COG)" pad unit or a "Chip-on-Plastic (COP)" pad unit. (*Id.*) Both COP and COG were well-known at the time of invention. (EX1002, ¶21; *see also* EX1005, 1:11-21, 5:25-6:7; EX1007, 138.)



B. Effective Filing Date

The '503 patent was filed on July 12, 2019, issued on August 3, 2021, and

claims priority to a Korean application filed on June 17, 2014. For purposes of this Petition only, Petitioner relies on June 17, 2014, as the earliest effective filing date. (EX1002, ¶14.)

C. Prosecution History

The '503 examination was not robust. (EX1002, ¶¶26-28.) The Examiner did not issue any prior art-based Office Action during prosecution.

The application that matured into the '503 patent was filed on July 12, 2019. The Examiner issued one Office Action containing double-patenting rejections only. (EX1003, 66-74.) The applicants submitted a terminal disclaimer form in response. (*Id.*, 83.) The Examiner then allowed the claims on April 1, 2021, citing the entirety of claim 1 as the reason for allowance. (*Id.*, 30, 33-34.)

Almost a month after the Notice of Allowance was issued, the applicant submitted an Information Disclosure Statement ("IDS") on April 29, 2021, citing several references including Wildes. (*Id.*, 18-19.) The Examiner initialed the IDS and placed it in the file on June 10, 2022, without any comments. (*Id.*, 14-15.)

A. Level of Ordinary Skill in the Art

A person of ordinary skill in the art (POSITA) in the field of the '503 patent would have a bachelor's degree in electrical engineering, computer engineering, materials science, or equivalent field, and two years of experience working on integrated circuits and packaging. Alternatively, a POSITA would have four years

of experience working on integrated circuits and packaging. An advanced graduate degree in the disciplines cited above may make up for the work experience indicated above. (EX1002, ¶¶34-36.)

IV. CLAIM CONSTRUCTION

For purposes of this Petition only, Petitioner does not believe any terms require a formal construction. Each of the terms carries its "ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question" at the time of the invention. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007); EX1002, ¶¶37-38.)

V. PRECISE REASONS FOR RELIEF REQUESTED

Pursuant to 37 C.F.R. § 42.104(b), Petitioner requests cancellation of the challenged claims based on the following references (EX1002, ¶¶39-43):

Prior Art Reference	Abbreviation (Exhibit No.)
U.S. Patent No. 5,951,304	"Wildes" (EX1004)
David J.R. Cristaldi *et al*., "Liquid Crystal Display Drivers: Techniques and Circuits" (Springer Science+Business Media B.V., 2009).	"Cristaldi" (EX1007-1008)
International Publication No. WO 2007/145522	"Lieshout" (EX1005)
U.S. Patent No. 6,872,081	"Imaoka" (EX1006)
Japanese Patent Pub. No. 2003-68795	"Shioda" (EX1037-EX1039)

The statutory grounds for the challenge of each claim are set forth below. All of the statutory citations are AIA.

Ground	35 U.S.C. §	Claims	Prior Art Reference(s)
1	103	1-10	Wildes
2	103	1-10	Wildes, Cristaldi
3	103	1-10	Lieshout, Imaoka
4	103	1-10	Wildes, Lieshout
5	103	6	Wildes, Shioda
6	103	6	Wildes, Cristaldi, Shioda
7	103	6	Lieshout, Imaoka, Shioda
8	103	6	Wildes, Lieshout, Shioda

Below, Petitioner discusses why the challenged claims are unpatentable under the statutory grounds raised, including how and where the prior art satisfies each element of each challenged claim, as required by 37 C.F.R. § 42.104(b)(4).[2] Petitioner's showing establishes that there is a reasonable likelihood that it will prevail on each ground of unpatentability to each challenged claim.

[2] Petitioner also shows how each claim preamble is satisfied, but does not concede that any preamble is limiting for any ground in the Petition.

A. Ground 1: Wildes Renders Obvious Claims 1-10

1. Summary of Wildes

Wildes was filed on May 21, 1997, and issued on September 14, 1999, qualifying as prior art at least under §§ 102(a)(1) and 102(a)(2).

Wildes is generally directed to "providing multiple-conductor circuit interconnections where there is a lack of precise dimensional control . . . ." (EX1004, Abstract.) Wildes states that its techniques can be widely applied, such as "***flat panel (LCD) displays*** for appliances, computers, and aircraft" and "the ***mounting of integrated circuit packages*** to a circuit board substrate employing surface mount technology." (EX1004, 1:48-56.)

FIGs. 1 and 2 illustrate a prior art system having misalignment issue due to "manufacturing variations." (EX1004, 4:4-6.) The connection pads ***30*** and ***32*** are straight in FIG. 1. (*See also* EX1004, 3:52-64.)

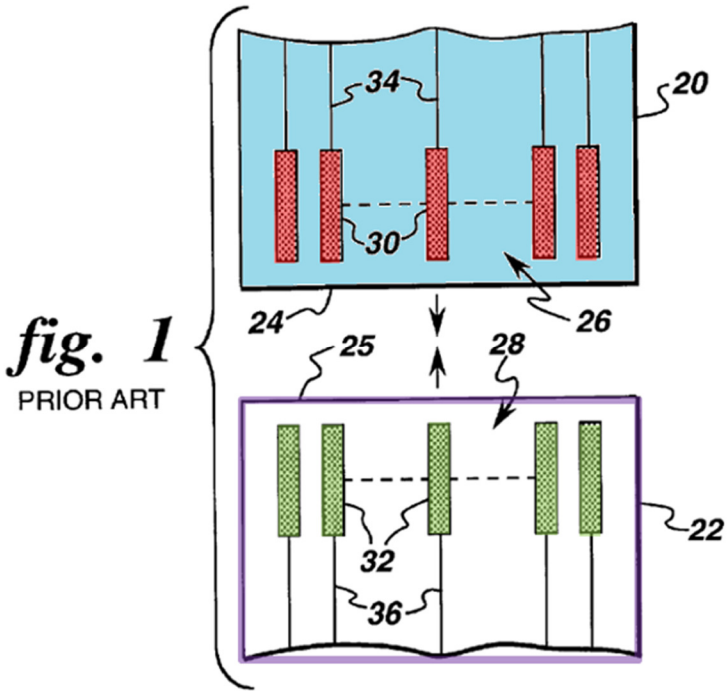


fig. 1
PRIOR ART

The straight connection pads can cause misalignment. For example, "***upper printed circuit board substrate 20***, as a result of manufacturing processing, is relatively wider than ***lower substrate 22***, and ***individual connection pads 30*** of array 26 are spaced farther apart than ***individual connection pads 32*** of array 28." (EX1004, 3:60-64.) FIGs. 2 and 4 illustrate the misalignment below.

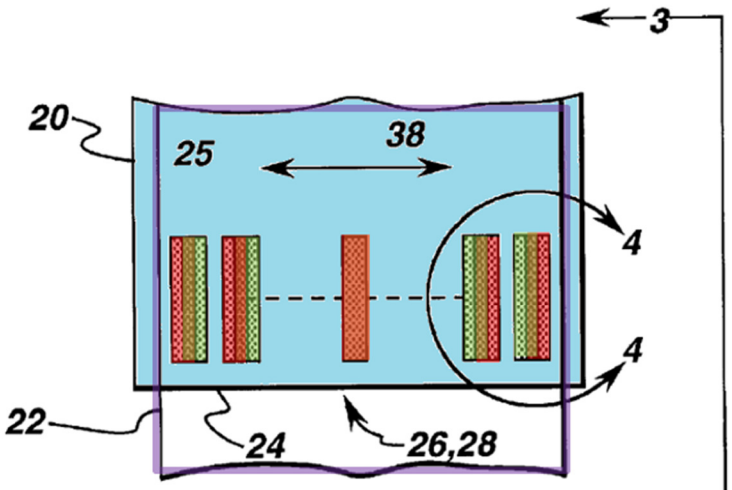


fig. 2
PRIOR ART

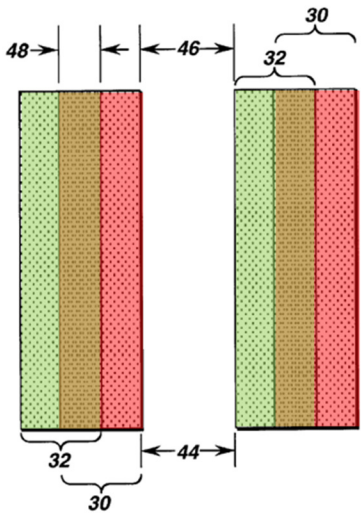


fig. 4
PRIOR ART

To overcome the misalignment problem, Wildes discloses inclined connection pads, as shown in FIG. 5.

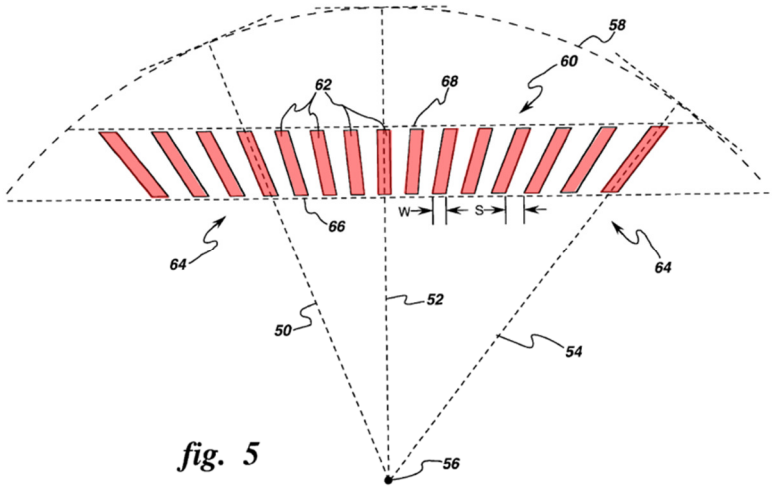


fig. 5

An exemplary application of fanout array 60 is represented in FIGs. 6 and 7. FIG. 6 shows two fanout arrays including inclined connection pads. (*See also* EX1004, 4:56-5:11.)

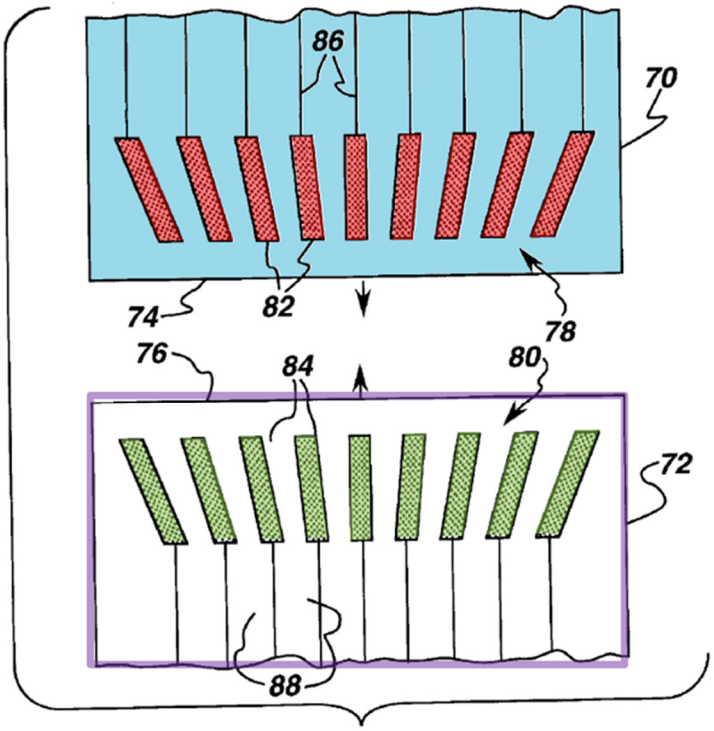


fig. 6

"When the printed circuits of FIG. 6 are joined as shown in FIGs. 7 and 8, two alignment axes are available, i.e., lateral and longitudinal, ***enabling 100% overlap of corresponding pads across the widths of the connection pads***." (EX1004, 5:4-7; *see also id*., FIG. 9.) This "allow[s] significant variations in the dimensions of the respective substrates being electrically connected to be accommodated." (EX1004, 2:10-15.)

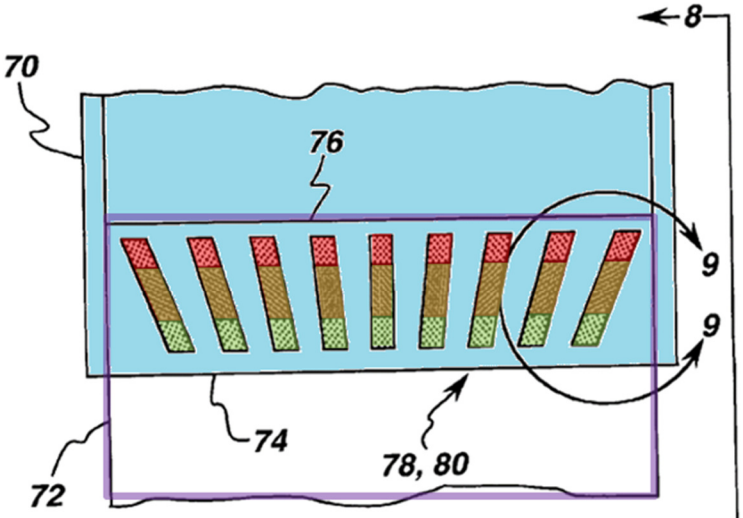


fig. 7

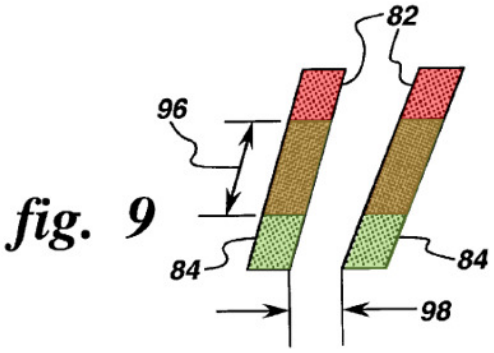


fig. 9

As another example, FIG. 13 of Wildes provides a "multi-row version 90 of the fanout pad array[.]" (EX1004, 6:44-45.) An annotated version of FIG. 13 is provided herein for better readability.

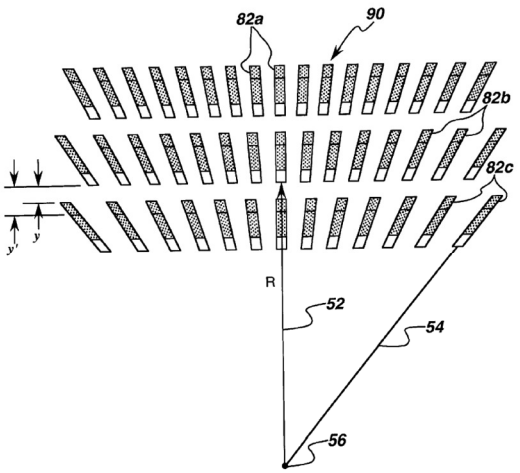


fig. 13

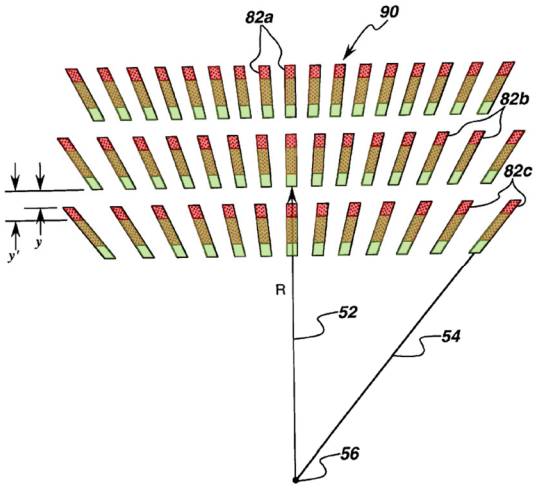


fig. 13

FIG. 14 depicts another form of multiple-row connection pad array. Importantly, Wildes states that "[t]he FIG. 14 arrangement is ***particularly advantageous for connecting integrated circuit packages to underlying printed circuit substrates*** employing surface mount techniques. Advantageously, conventional circuit routing techniques are still applicable." (EX1004, 7:22-26.) It would have been obvious to a POSITA that the structure shown in FIG. 14 is identical or at least analogous to the structure of an LC mounted to an array substrate. (EX1002, ¶54.) In each case, an integrated circuit is bonded to a substrate (e.g., an array substrate or an underlying substrate) to establish electrical connections and provide driving signals.

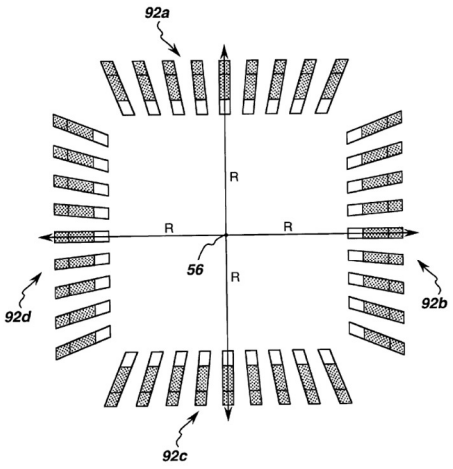


fig. 14

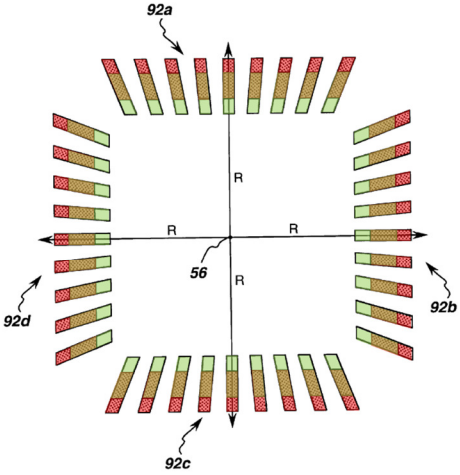


fig. 14

2. Claim 1

a. Preamble: "An electronic device, comprising:"

Wildes discloses an electronic device. "A major application is electrical connection to ***flat panel (LCD) displays*** for appliances, computers, and aircraft." (EX1004, 1:48-50.) A POSITA would have understood that such a multiple-conductor interconnect system is part of an electronic device. (EX1002, ¶¶56-57.)

b. 1[a]: "an array substrate;"

Wildes discloses a "multiple-conductor interconnect system includ[ing] a pair of ***substrates*** with respective circuits and respective corresponding connection pad arrays for electrically connecting the respective circuits when joined." (EX1004, 2:60-64.)

FIG. 6 depicts a "pair of substrates 70 and 72." (EX1004, 4:57.) Either substrate 70 or substrate 72 can be mapped to the "array substrate." For illustrative purposes, ***substrate 70*** is mapped to the "array substrate" but it should be obvious

to a POSITA that, in an alternative mapping, substrate 72 may be mapped to the "array substrate." (EX1002, ¶¶58-67.)

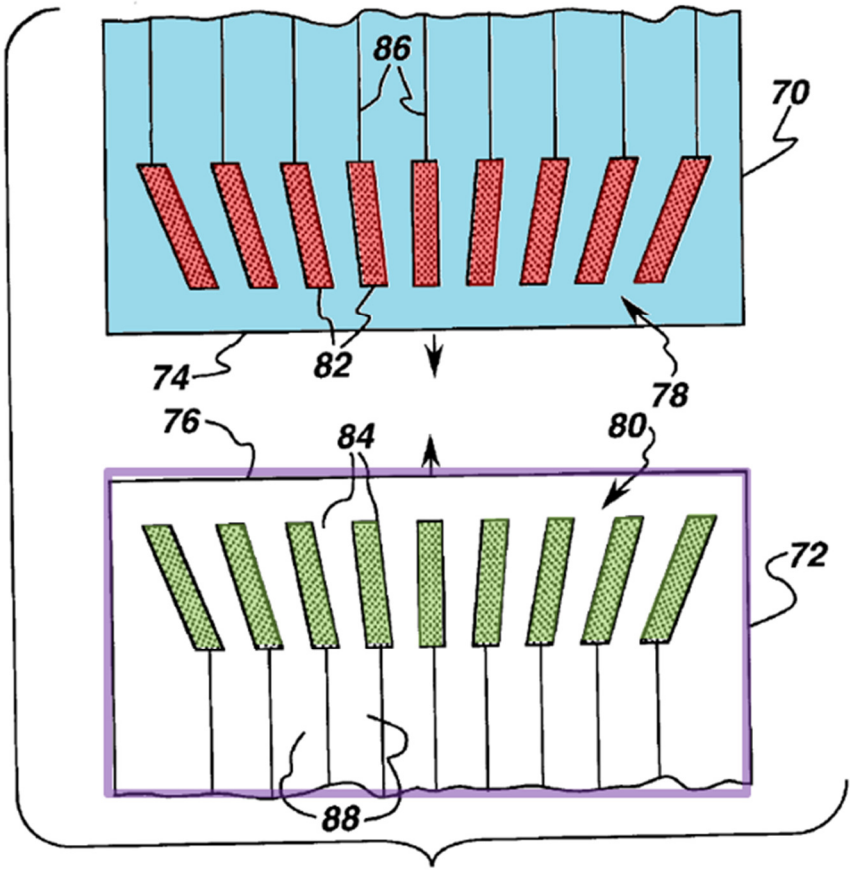


fig. 6

Wildes discloses that substrate 70 can be an "array substrate." Wildes states that "[a] major application [of the multiple-conductor interconnect system] is ***electrical connection to flat panel (LCD) displays*** for appliances, computers, and aircraft." (EX1004, 1:48-50.) A POSITA would understand that this teaches applying Wildes to provide electrical connection between an integrated circuit and

the array substrate to provide driving signal to the array substrate. (EX1002, ¶¶61-62.)

As background, a textbook titled "Liquid Crystal Display Drivers: Techniques and Circuits" by Cristaldi *et al*. discloses well-known technologies for mounting the IC onto an array substrate, including the chip-on-glass ("COG") technology. It explains that "COG was first introduced in 1983" and "[i]n this [i.e., COG] approach the ***IC is mounted directly on the glass substrate***[.]" (EX1007, 138.) The glass substrate is an array substrate. (EX1002, ¶62.) Plastic substrates were also commonly used as array substrates. (EX1002, ¶63; *see* EX1005, 5:25-6:1, 8:27-9:7; EX1036, Abstract.)

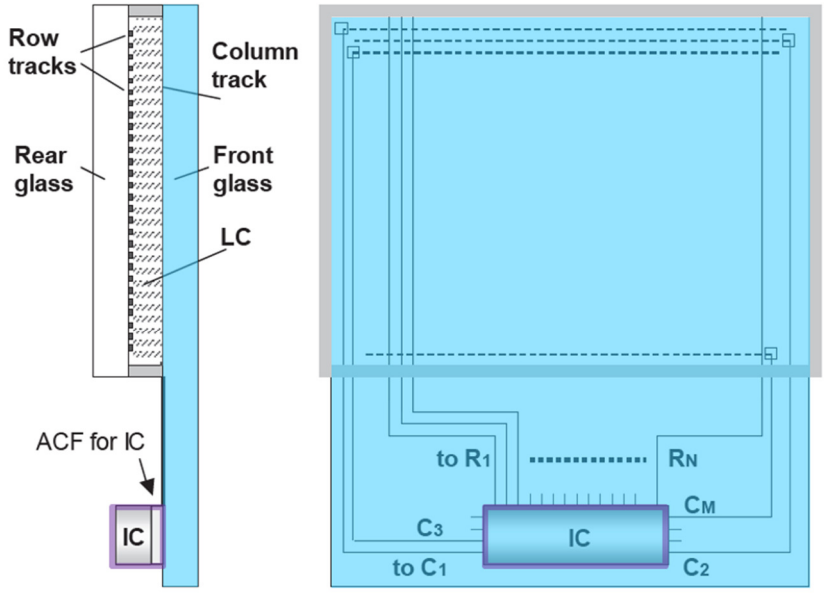


Fig. 4.27 LC panel with COG driver IC

EX. 1008

Potential misalignment between the pads on the array substrate and the IC bumps was well-known. (EX1002, ¶64.) For example, Cristaldi teaches that "the IC is pressed against the ACF and glass applying heat through the bonding tool" during manufacturing. (EX1007, 138.) Heat and stress can cause the glass substrate to deform, leading to misalignment. (EX1002, ¶64.) Lieshout, a patent publication in 2007, states that "[u]ncertainties in dimensions between the IC chips and substrates cause ***misalignment*** of connections, and unintended open and shorted connections." (EX1005, 1:7-8.) It was known that potential misalignment can occur for different types of substrates, including "a plastic substrate, a flexible circuit board, a rigid circuit board, and a glass substrate." (EX1005, claim 2; *see also id*. at 6:3-7.)

Wildes addresses this exact problem: "providing multiple-conductor circuit interconnections where ***there is a lack of precise dimensional control*** . . . ." (EX1004, Abstract.) Wildes contemplates a variety of potential applications, including "***flat panel (LCD) displays*** for appliances, computers, and aircraft" and "the mounting of ***integrated circuit packages*** to a circuit board substrate[.]" (EX1004, 1:48-55.) Although Wildes describes "flexible" substrates in some embodiments, Wildes does not limit its application as such. (EX1002, ¶66.) A POSITA would understand that the common materials (e.g., glass, plastic) for

array substrates may deform (e.g., due to heat or stress) and thus can benefit from the teachings of Wildes. (EX1002, ¶¶66-67.)

Thus, it would have been obvious to a POSITA to apply Wildes to provide electrical connection between an array substrate of a display and an integrated circuit that drives the display in COG or COP, which are well-known LCD technologies. One of the substrates in FIG. 6, such as substrate 70, would be an array substrate. The other one of the substrates, such as substrate 72, would be the integrated circuit that is mounted onto the array substrate to drive the display. (EX1002, ¶67.)

c. 1[b]: "a pad portion disposed on the array substrate; and"

Wildes discloses a pad portion. In FIG. 6, "***substrates 70*** and 72 . . . have respective ends 74 and 76 and support respective arrays 78 and 80 of ***individual connection pads 82*** and 84 for establishing electrical connections[.]" (EX1004, 4:57-64.) The ***individual connection pads 82*** are the "pad portion." (EX1002, ¶68-70.)

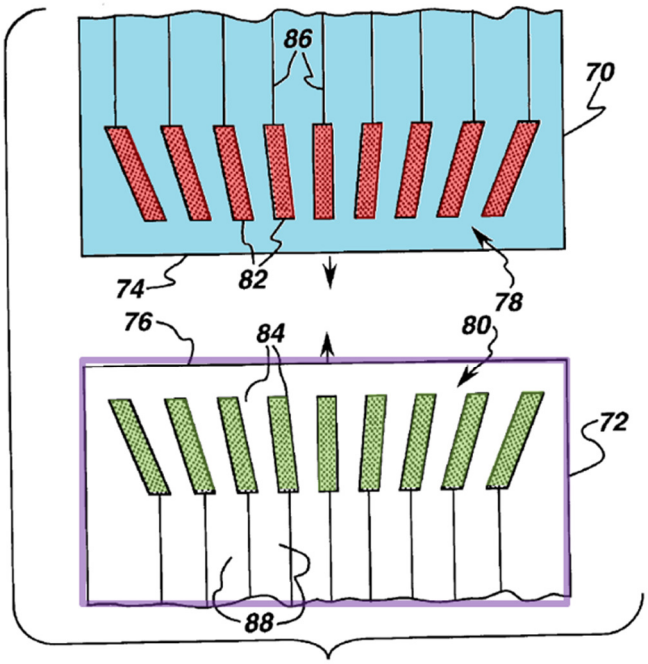


fig. 6

FIG. 8 provides a side view depicting the ***individual connection pads 82*** disposed on the ***substrate 70***. (EX1004, 4:57-64.)

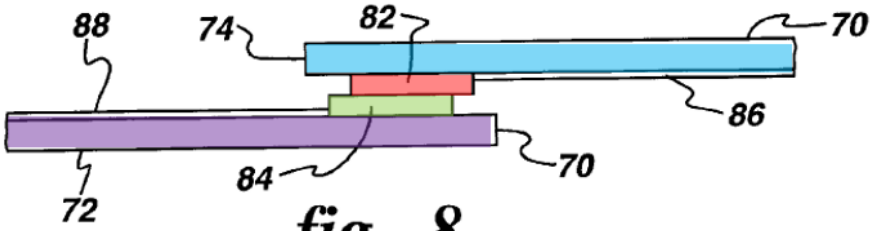


fig. 8

FIG. 5 shows how the layout of the pads is designed, specifically that "the connection pads of each array are ***longitudinally aligned along radial lines***[.]" (EX1004, 4:32-34.)

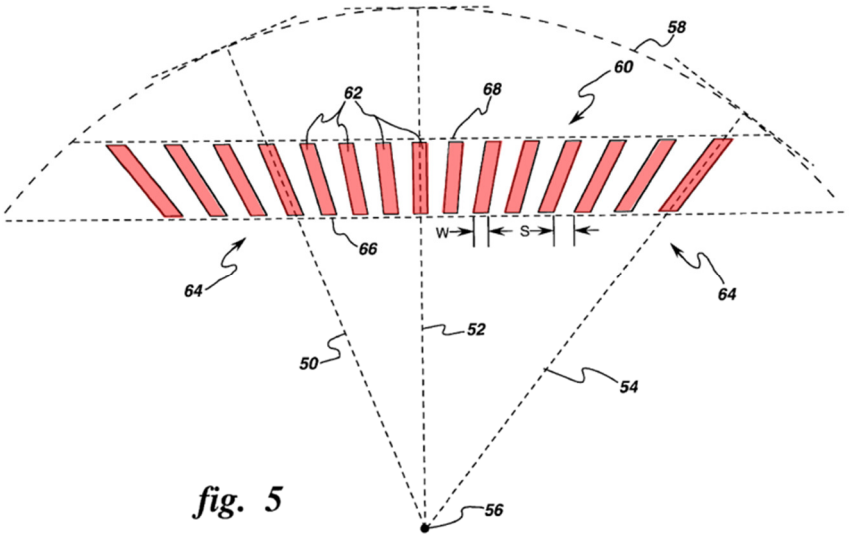


fig. 5

As additional examples, FIG. 13 depicts "a multiple-row connection pad array[.]" (EX1004, 3:42-43.) "FIG. 14 depicts another form of multiple-row connection pad array where the pads of respective fanout arrays ***92a, 92b, 92c, and 92d*** are arranged around, and positioned at, equal distances from a center 56, generally forming a square, rectangle or other polygon." (EX1004, 7:18-22.) A POSITA would understand that these pads would be disposed on a substrate such as ***substrate 70*** in FIG. 6 and operate in a similar manner. (EX1002, ¶¶68-70.)

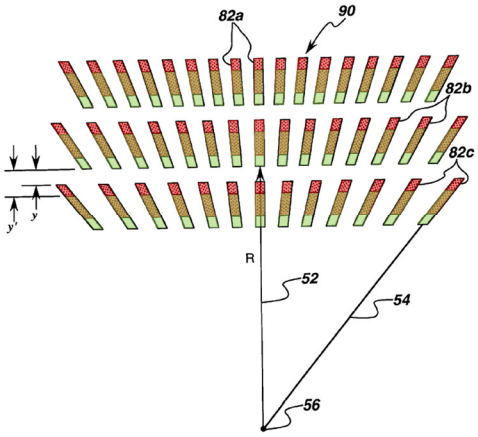


fig. 13

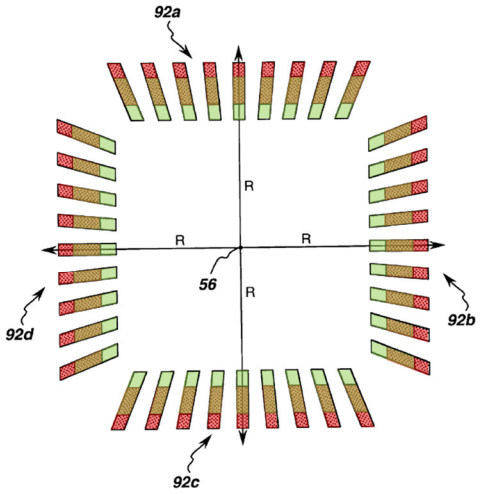


fig. 14

d. 1[c]: "an integrated circuit disposed on the pad portion and comprising a bump portion;"

As discussed above, in FIG. 6, ***substrate 70*** would be the array substrate and ***substrate 72*** would be the integrated circuit comprising bumps for electrical connection. (*Supra* V.A.2.b; *see also* EX1004, 4:56-64, 5:4-11.) The ***substrate 72*** provides ***individual connection pads 84***. (EX1002, ¶¶71-72.) It would be obvious to a POSITA that the ***individual connection pads 84*** are the "bump portion" of the integrated circuit package for establishing electrical connection. (*Id.*)

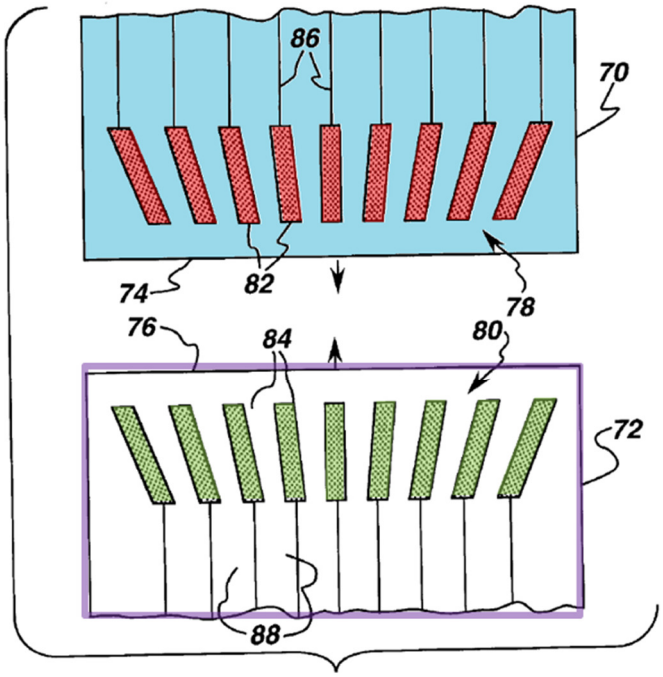


fig. 6

FIG. 8 shows that the ***individual connection pads 84*** are raised connection bumps. (EX1002, ¶73; *see also* EX1004, 5:4-11.)

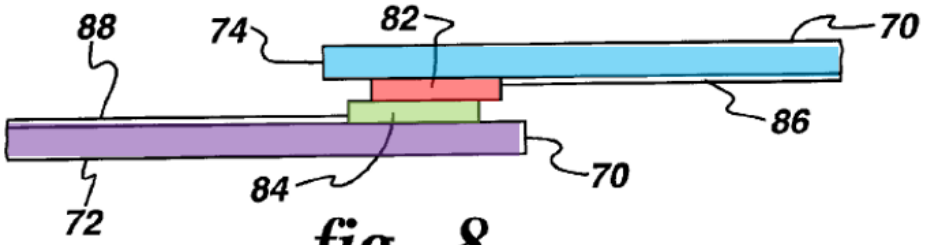


fig. 8

Wildes discloses that the integrated circuit is disposed on the pad portion. FIG. 7 shows that the ***integrated circuit*** (i.e., 72) comprising ***individual connection pads 84*** is disposed on the ***individual connection pads 82*** (i.e., the pad portion) on the ***substrate 70***. (EX1002, ¶74; *see also* EX1004, 5:4-11.)

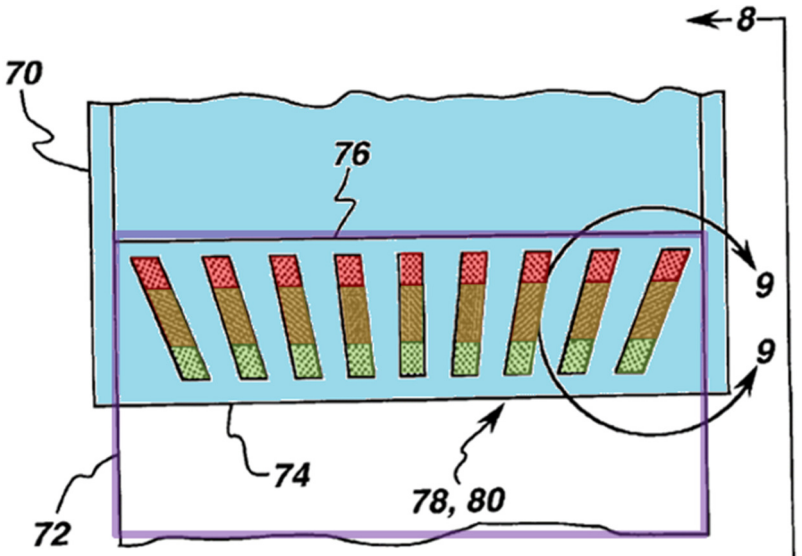


fig. 7

In addition to FIG. 6, Wildes states that "[t]he FIG. 14 arrangement is particularly advantageous for connecting ***integrated circuit packages*** to underlying printed circuit substrates employing surface mount techniques." (EX1004, 7:22-25.) It would have been obvious to a POSITA that the structure shown in FIG. 14 is identical or at least analogous to the structure of LC amounted to an array substrate. (EX1002, ¶75.) In each case, an integrated circuit is bonded to a substrate (e.g., an array substrate in a display or an underlying substrate) to establish electrical connections and provide driving signals.

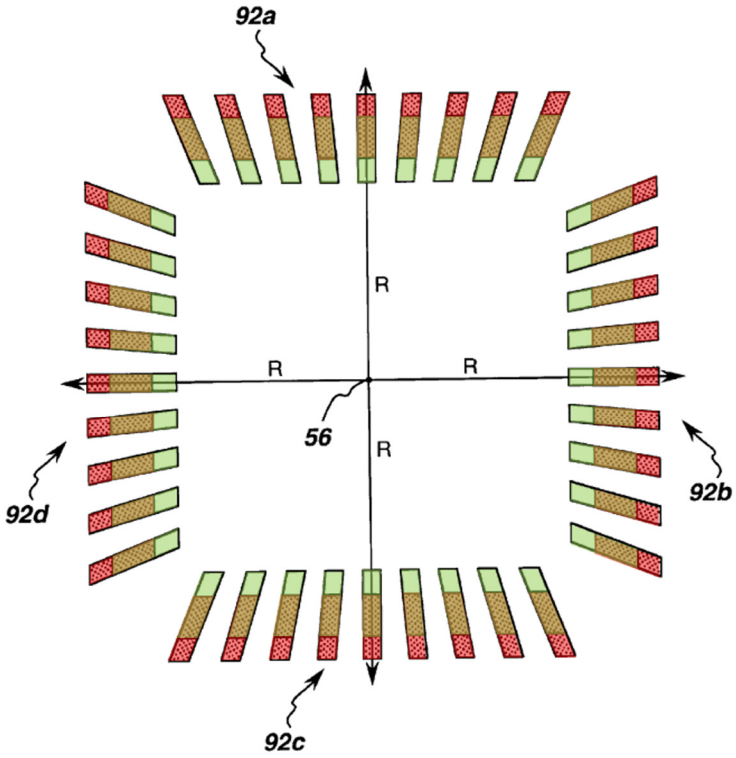


fig. 14

The integrated circuit in FIG. 14, as shown, has inclined parallelogram ***bumps*** disposed on inclined parallelogram ***pads of respective fanout arrays 92a, 92b, 92c, and 92d***. (EX1002, ¶75.) Thus, Wildes itself makes it clear, and it would have been obvious to a POSITA that an integrated circuit having inclined, parallelogram bumps (such as FIG. 14) can be mounted onto the array substrate with corresponding inclined, parallelogram pads. (*Id.*)

FIG. 13 shows that these ***pads 82a, 82b, 82c*** are each connected to a corresponding connection pad in green, which can be bumps of an integrated circuit package. (EX1004, 6:44-45; EX1002, ¶76.)

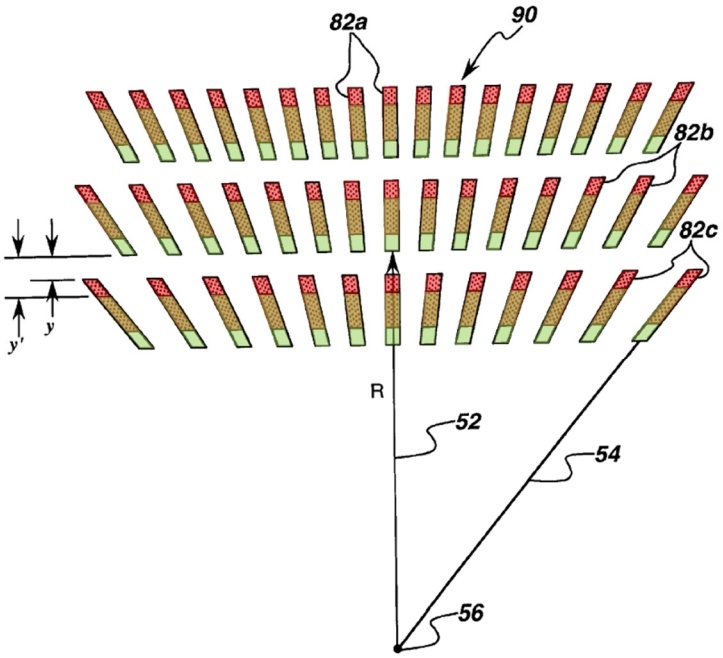


fig. 13

As explained by Dr. Chen, it was common knowledge that an integrated circuit provides "bumps" for electrical connection at the time of the invention. (EX1002, ¶77.) Well before the invention, integrated circuits had bumps of various shapes to provide electrical connection with other devices. (*Id.*) Wildes itself discloses an integrated circuit with inclined bumps (e.g., FIG. 14) for electrical connection. As another example, a patent publication dated 2007 stated that "[t]he external shape of the bump [] is not particularly limited. The external shape of the bump [] may be a quadrilateral (including ***square*** and ***rectangle***) or a ***circle***." (EX1035, [0118].) In particular, elongated bumps were known to be preferrable compared to non-elongated bumps such as square bumps at least since 1990. (EX1002, ¶77; *see also* EX1029-1031 and 1032-1033.)

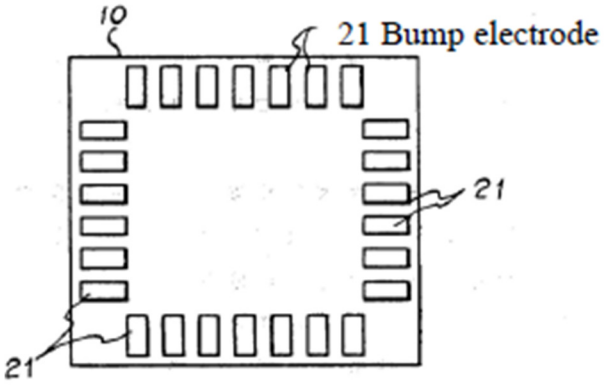
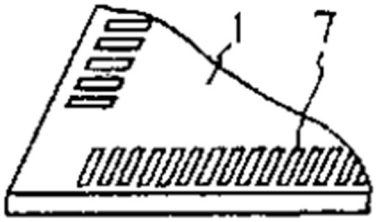


FIG. 2

(EX1030.)

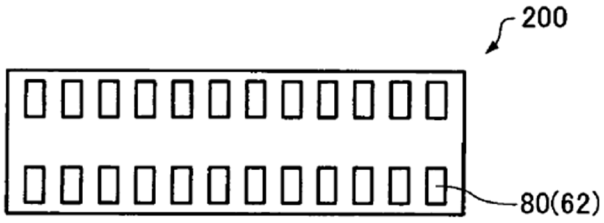


A schematic diagram illustrating an embodiment of a semiconductor device bump according to the present invention

FIG. 1

(EX1033.)

FIG.12



(EX1035.)

Below are exemplary microscopic images of "gold bumps" of an IC for providing electrical connection to a display from a textbook dated 2009. (EX1007, 137.) While figure (b) mentions COF, Cristaldi states that COG also provides "gold bumps" and a POSITA would understand that the gold bumps in the figure below are the same as gold bumps in COG (or for that matter, COP) in purpose and shape. (EX1007, 138; EX1002, ¶78.)

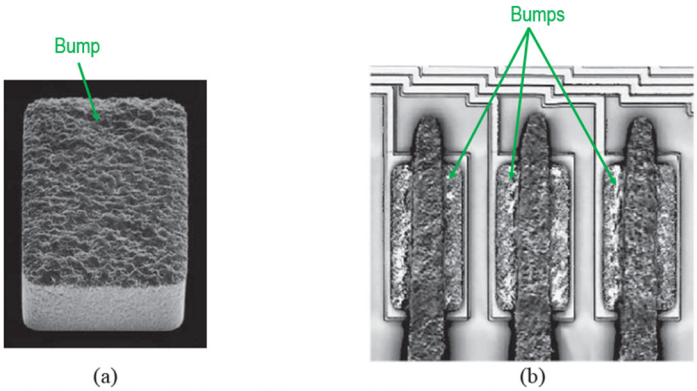
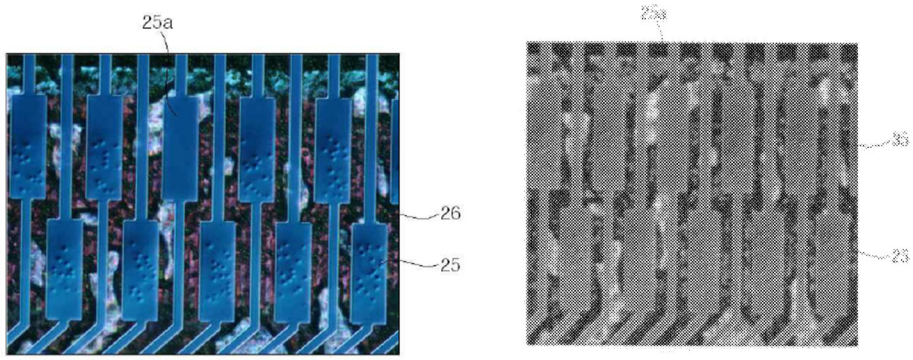


Fig. 4.26 Micrographs of (**a**) a gold bump and (**b**) connection between bumps and inner leads in COF via gold-tin eutectic bonding [TNF2003]

(EX1008, 137.)

Below are photomicrographs showing rectangular bumps 25 of an integrated circuit in patent literature dated before the invention. (EX1012, FIG. 3, [0035]; EX1013, FIG. 3; EX1002, ¶79.)



Below are illustrations of inclined parallelogram IC bumps in patent literature dated before the invention. "A bump 10 is provided on each of electrode pads of a semiconductor chip 9." (EX1014, [0052]; EX1002, ¶80.)

FIG.18A

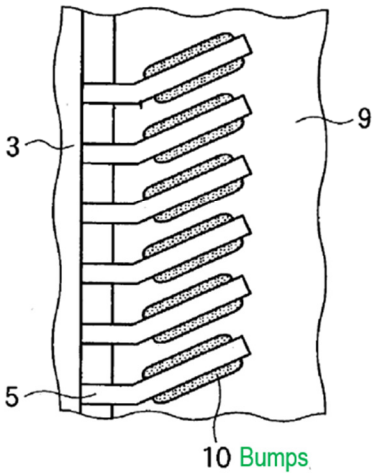
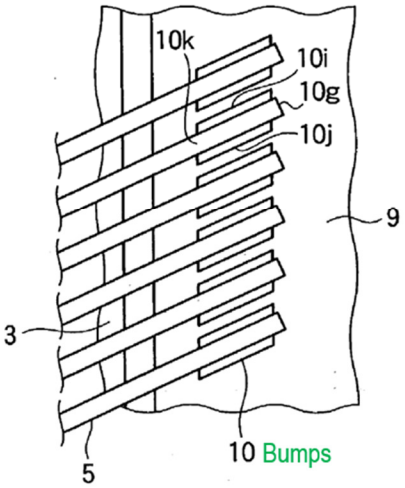
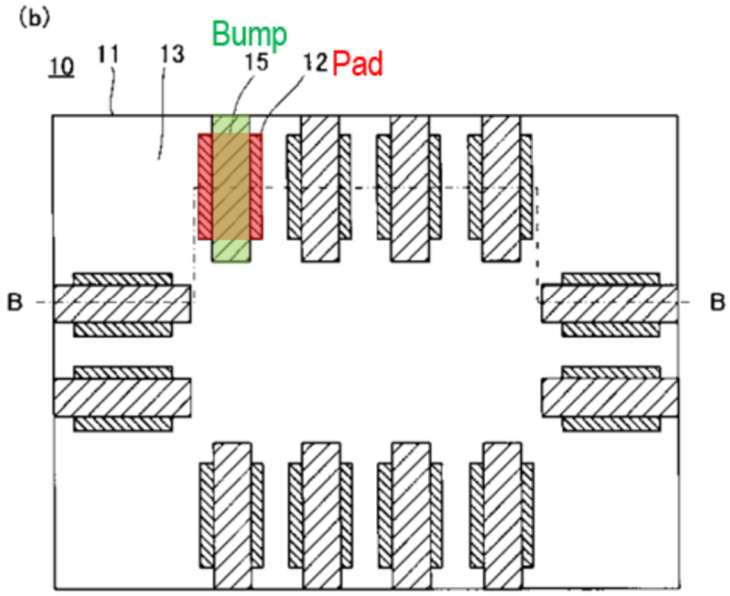


FIG.22A



Below is another illustration of flip-chip mounting involving rectangular ***bumps 15*** in patent literature dated before the invention. (EX1022-1024, FIG. 1(b), Abstract; EX1002, ¶81.)



e. 1[d]: "wherein: the pad portion comprises a first sub-pad unit comprising an inclined first pad and a second sub-pad unit comprising an inclined second pad;"

The ***individual connection pads 82*** in Wildes include four inclined pads on the left – one or more of these four inclined pads on the left can be mapped a "first sub-pad unit." Likewise, the ***individual connection pads 82*** include four inclined pads on the right – one or more of these four inclined pads on the right can be mapped a "second sub-pad unit." (EX1002, ¶82; *see also* EX1004, 4:32-5:11.)

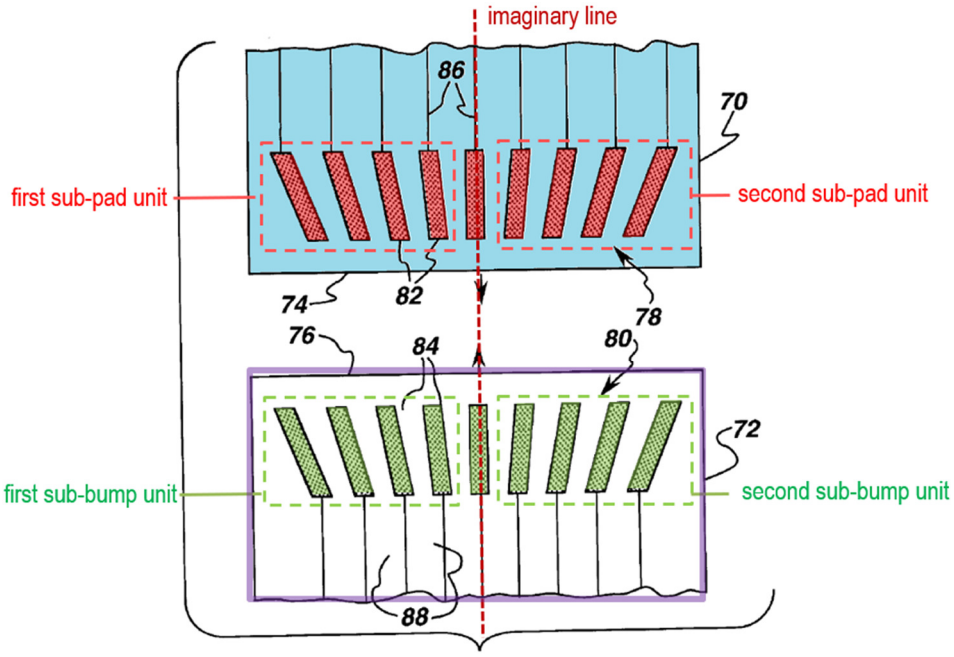


fig. 6

An exemplary mapping of "inclined first pad" and "inclined second pad" is provided below. (EX1002, ¶83; *see also* EX1004, 4:32-5:11.)

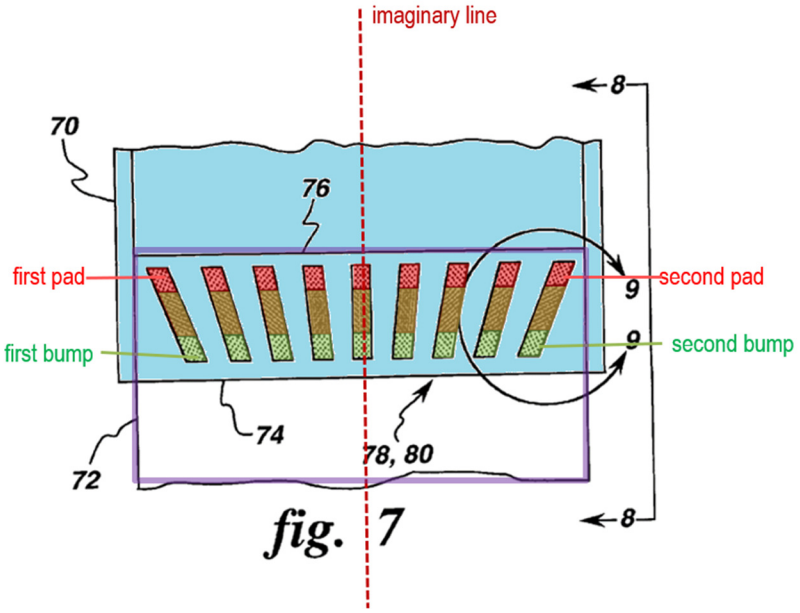


fig. 7

FIG. 5 discloses the limitation. (*See* EX1004, 4:32-34; EX1002, ¶83.)

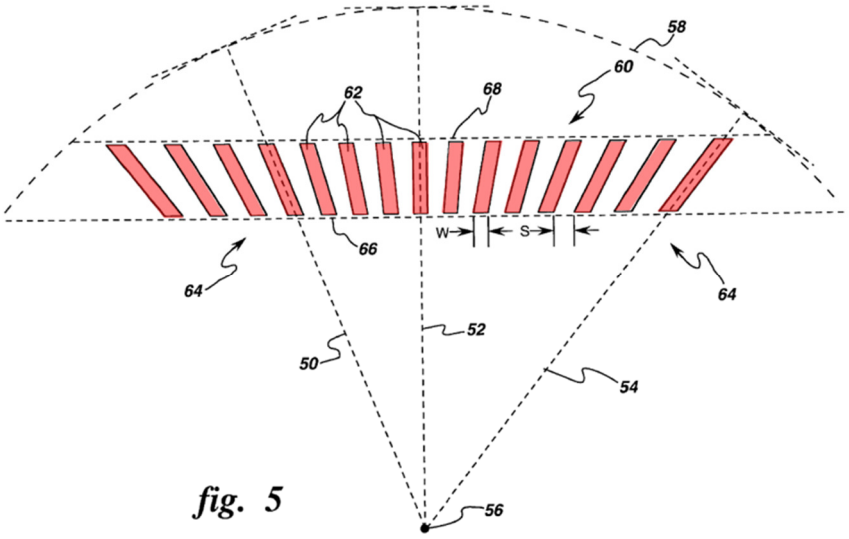


fig. 5

In FIG. 13, one or more of the inclined pads to the left of the line 52 disclose a "first sub-pad unit." One or more of the inclined pads to the right of the line 52 can be mapped a "second sub-pad unit." (EX1002, ¶84; *see also* EX1004, 6:44-45.) An exemplary mapping is shown below. Each row of the three rows discloses the limitation. (*Id.*)

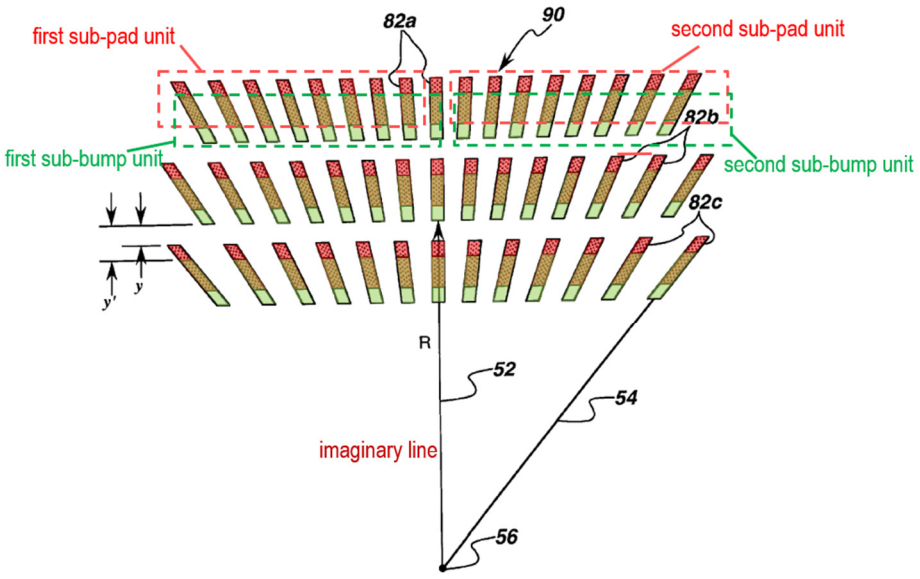


fig. 13

FIG. 14 also discloses the limitation. (EX1002, ¶85; *see also* EX1004, 7:18-26.)

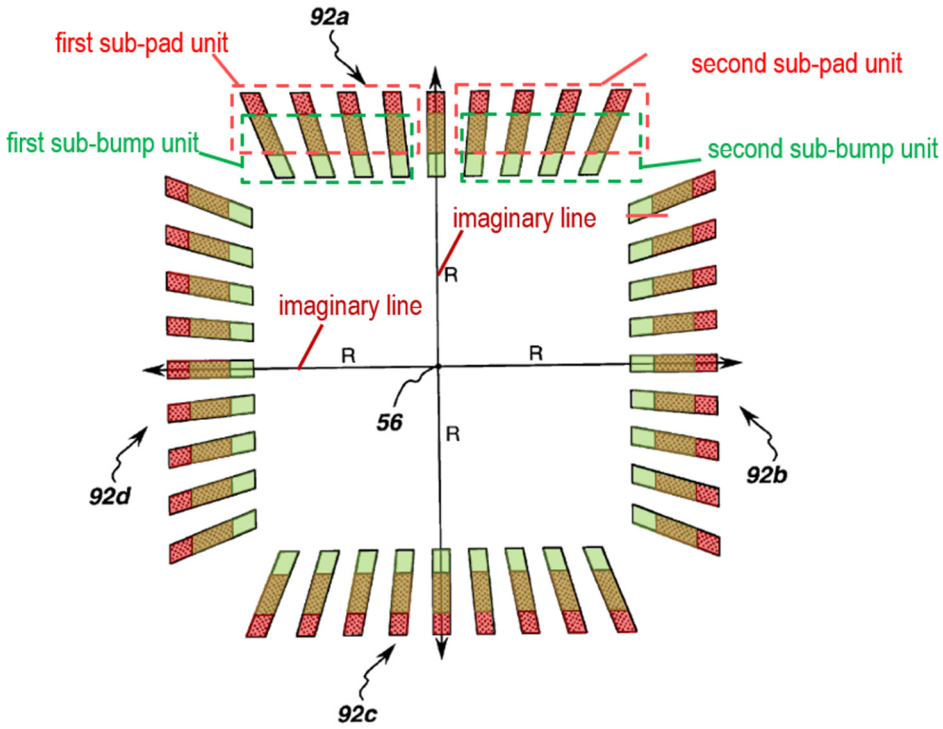


fig. 14

f. 1[e]: "the first pad and the second pad are inclined in different directions symmetrically about an imaginary line that divides the pad portion; and;"

Wildes discloses this limitation. For example, Wildes states that "the fanout array is ***symmetrical about a midpoint line***." (EX1004, 2:28-29; *see also id*. at 2:52-55; 4:48-55; claims 2, 5, 9, 14, and 18.) This is shown in FIGs. 6 and 7. (*See also* EX1004, 4:56-5:11; EX1002, ¶86.)

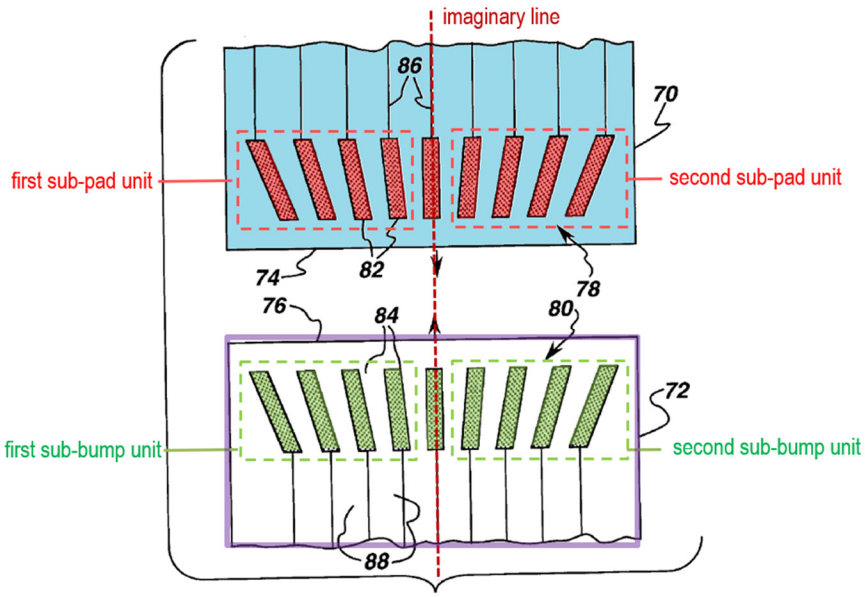


fig. 6

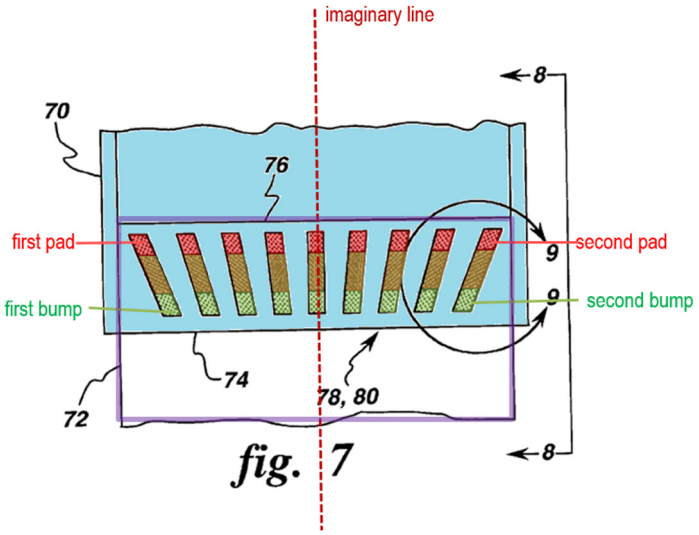


fig. 7

In FIG. 13, line 52 is the ***imaginary line***. (EX1002, ¶87; *see also* EX1004, 6:44-46.)

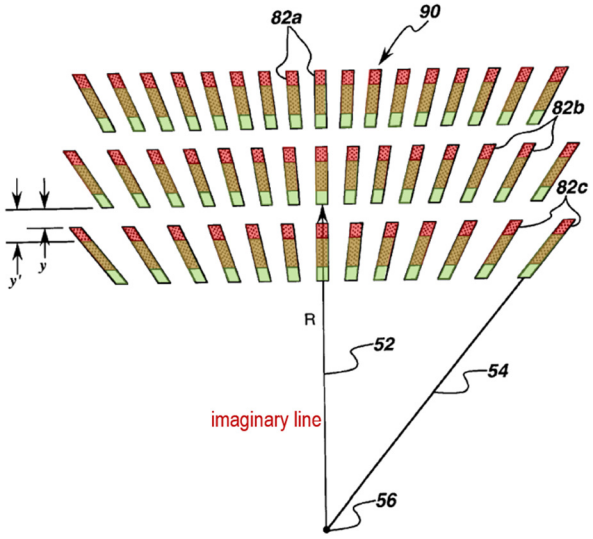


fig. 13

In FIG. 14, each of the pad portions 92a, 92b, 92c, and 92d has an imaginary line in the middle. (EX1002, ¶88; *see also* EX1004, 7:18-26.)

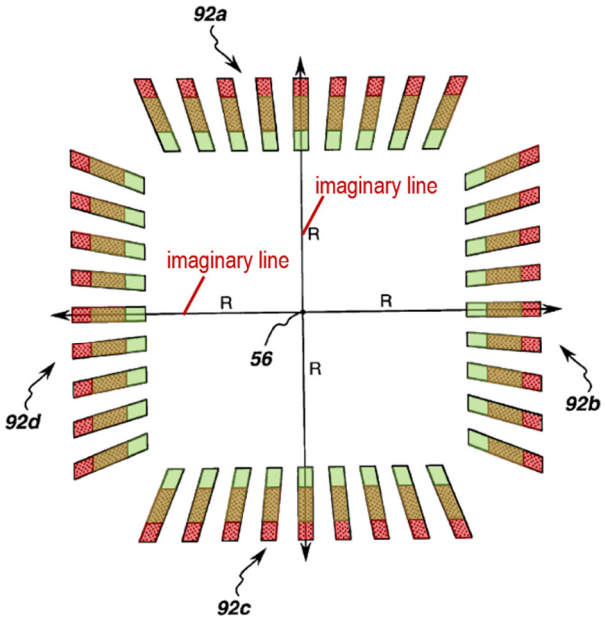


fig. 14

FIG. 5 shows that the "fanout array 60 is ***symmetrical about a midpoint line which, in FIG. 5, is radial line 52***". (EX1004, 4:48-51; EX1002, ¶89.)

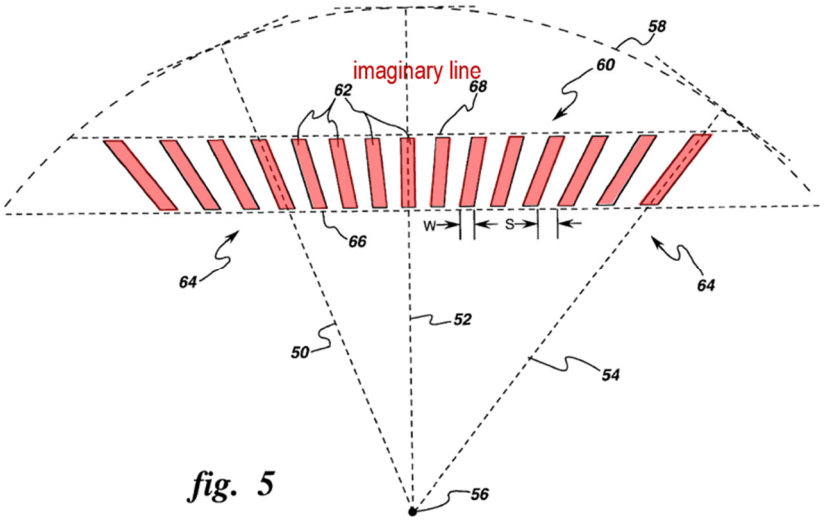


fig. 5

g. 1[f]: "the pad portion is electrically connected with the bump portion;"

All of the pad portions discussed above are "elongated ***electrical connection*** pads." (EX1004, 2:19; EX1002, ¶¶90-91.) FIG. 6 is "a plan view depicting a pair of substrates supporting respective fanout connection pad arrays for ***electrically connecting*** respective circuits on the substrates . . . ." (EX1004, 3:16-19.)

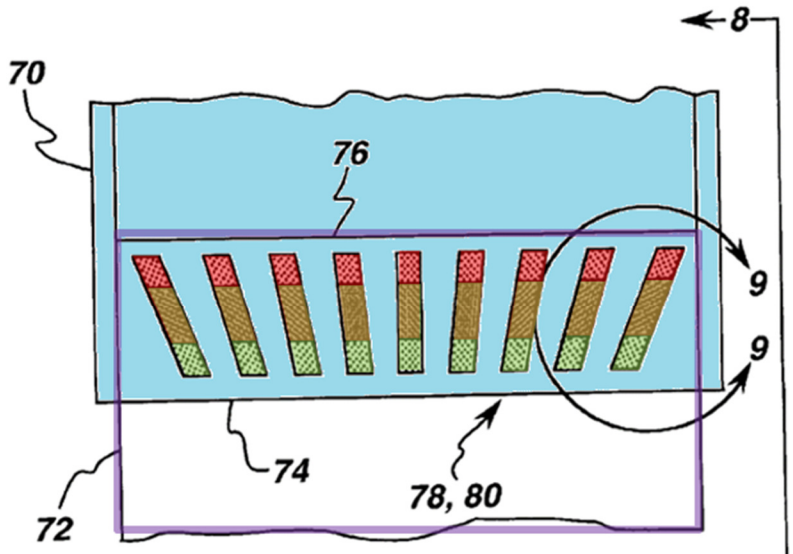


fig. 7

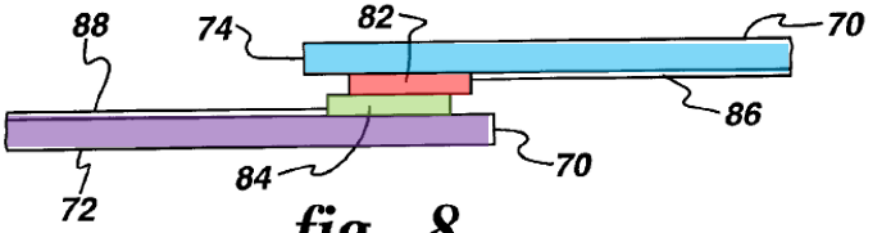


fig. 8

h. 1[g]: "the bump portion comprises a first sub-bump unit comprising an inclined first bump and a second sub-bump unit comprising an inclined second bump;"

As discussed above, Wildes' substrate 72 would be an integrated circuit. (*Supra* V.A.2.db, V.A.2.d.) In ***individual connection pads 84*** shown in FIG. 6, any of the four inclined pads on the left can be mapped a "first sub-bump unit" and any of the four inclined pads on the right can be mapped a "second sub-bump unit". (EX1002, ¶92; *see also* EX1004, 4:56-5:11.)

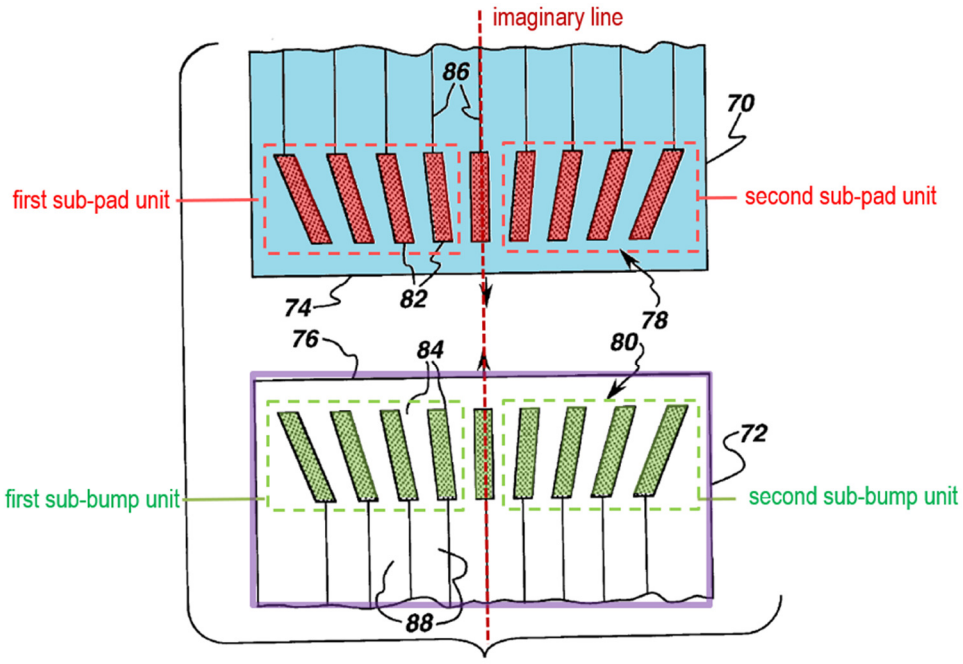


fig. 6

An exemplary mapping of "first bump" and "second bump" is shown below. (EX1002, ¶93.)

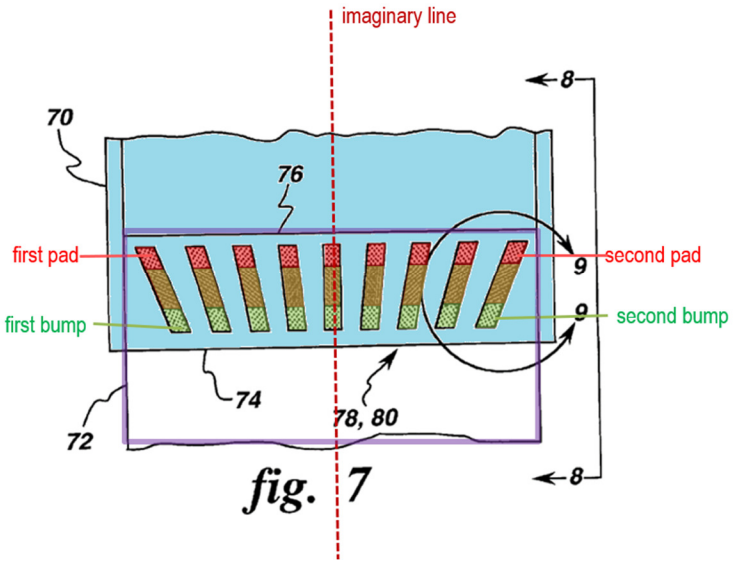


fig. 7

The embodiment in FIG. 13 also discloses such a bump portion. (EX1002, ¶94; *see also* EX1004, 6:44-46.)

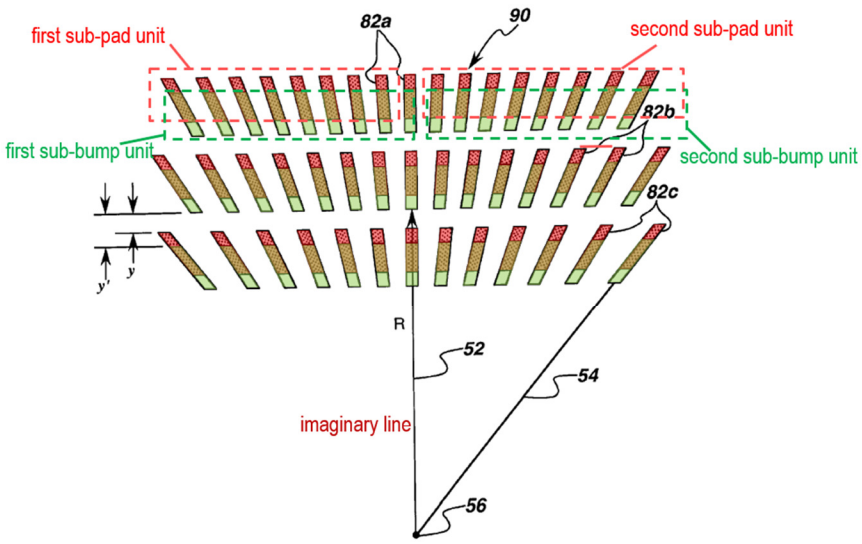


fig. 13

The embodiment in FIG. 14 also discloses such a bump portion. (EX1002, ¶95; *see also* EX1004, 7:17-26.)

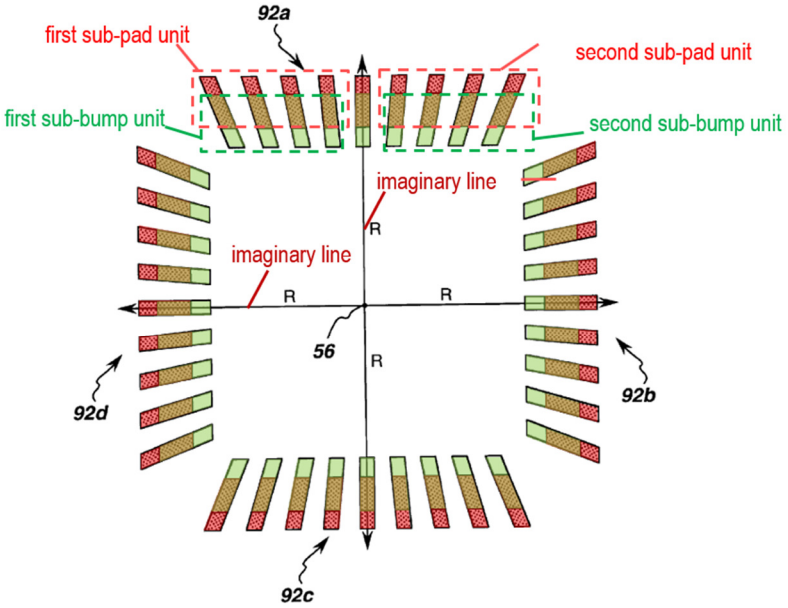


fig. 14

FIG. 5 shows an exemplary layout of pads. A POSITA would understand that the corresponding bump portion is similarly designed. (EX1002, ¶95.)

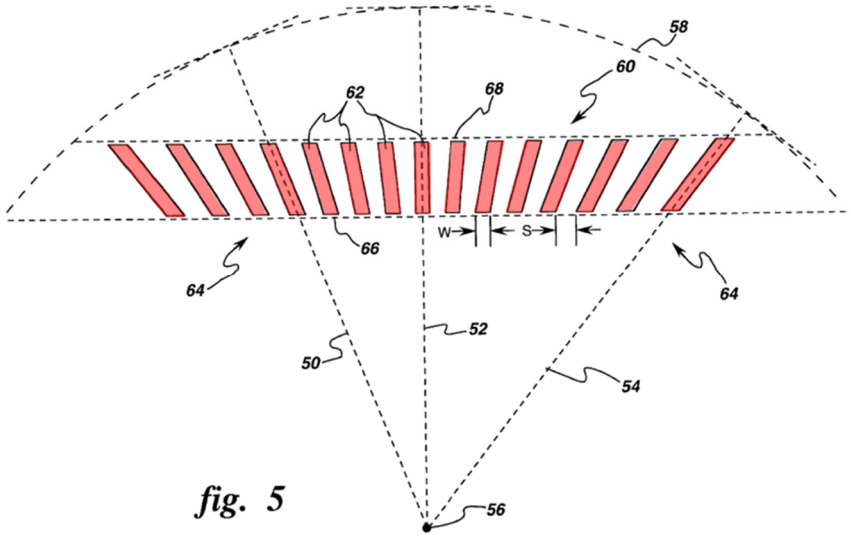


fig. 5

As discussed above, IC bumps were commonly made in elongated shapes in LCD displays at the time of the invention. (*Supra* V.A.2.d.) Wildes itself discloses parallelogram IC bumps in FIG. 14 bonded to a circuit substrate with parallelogram pads in a structure identical or at least analogous to IC bonded to an array substrate. Furthermore, as early as 1990, elongated IC bumps were known to be advantageous comparing to square IC bumps because they allow for higher density and a larger contact area. (*See, e.g.*, EX1030, 114; EX1033, 167; EX1002, ¶75.) Elongated IC bumps were widely used in LCD displays well before the invention. (*See, e.g.*, EX1007, 138; EX1012, FIG. 3; EX1013, FIG. 3; EX1014, [0052], EX1022, FIG. 1(b); EX1002, ¶93.) Making them inclined in Wildes' layout would be obvious to a POSITA, as the shape and the manufacturing methods were known and practiced at the time, and doing so would provide the benefit of preventing misalignment and "achiev[ing] a high connection density when making these electrical interconnections" as taught by Wildes. (EX1004, 2:8-9; EX1002, ¶93.)

i. 1[h]: "the first bump and the second bump are inclined in different directions symmetrically about the imaginary line that divides the pad portion."

As discussed above, Wildes discloses the imaginary line. (*Supra* V.A.2.f.) FIG. 6 discloses this limitation, as shown by the exemplary mapping below. (EX1002, ¶96.)

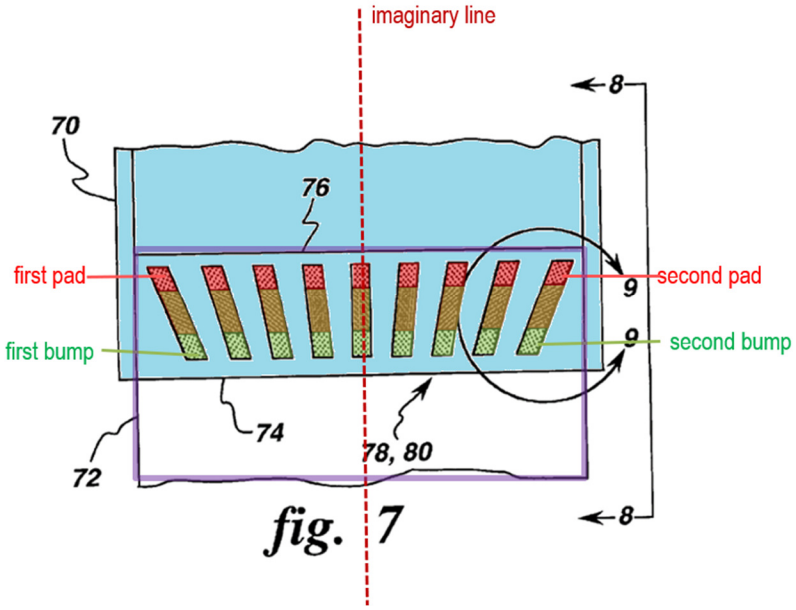


fig. 7

The examples in FIGs. 13 and 14 also disclose this limitation. (EX1002, ¶97; *see also* EX1004, 6:44-46, 7:18-26.)

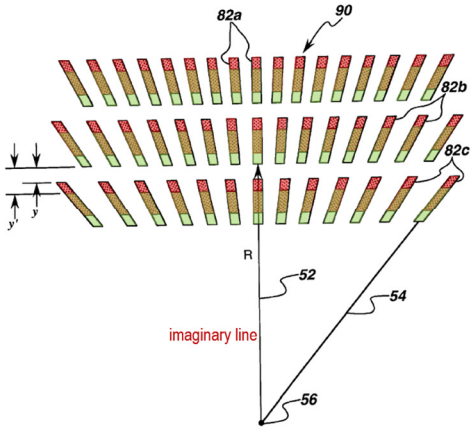


fig. 13

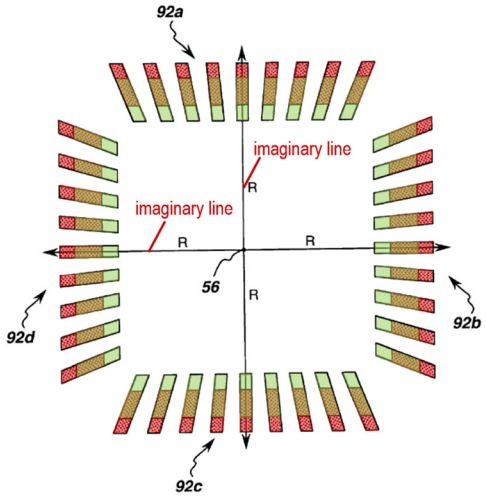


fig. 14

3. Claim 2: "The electronic device of claim 1, wherein at least one of the first pad and the second pad has a parallelogram shape."

Wildes discloses this limitation. In Fig. 6, at least one of the ***individual connection pads 82*** has a parallelogram shape. (EX1002, ¶98; *see also* EX1004, 4:32-5:18.)

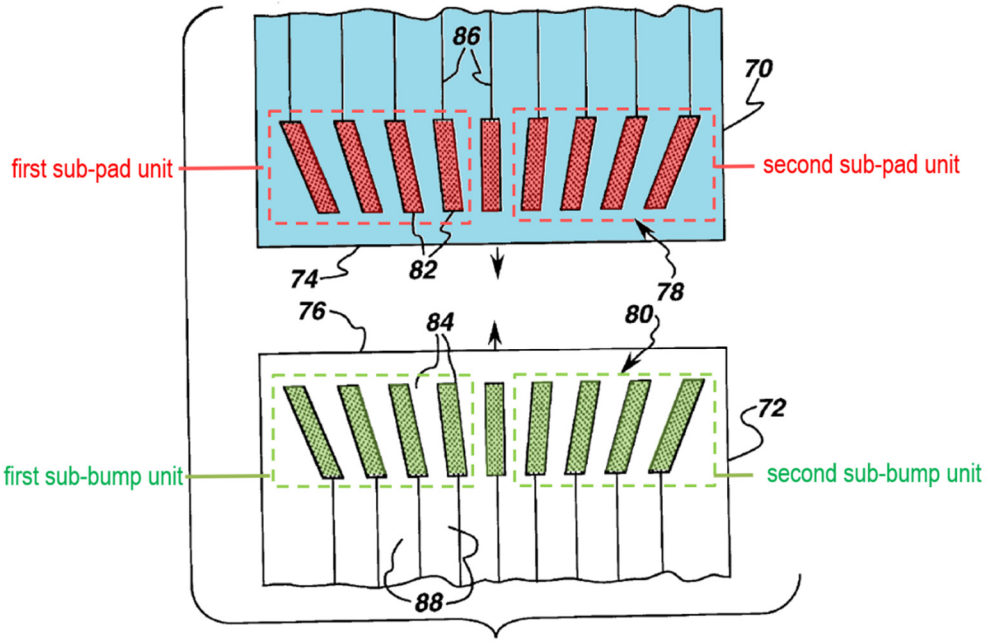


fig. 6

FIGs 13 and 14 each discloses this limitation. (EX1002, ¶99; *see* EX1004, 6:44-46; 7:18-26.)

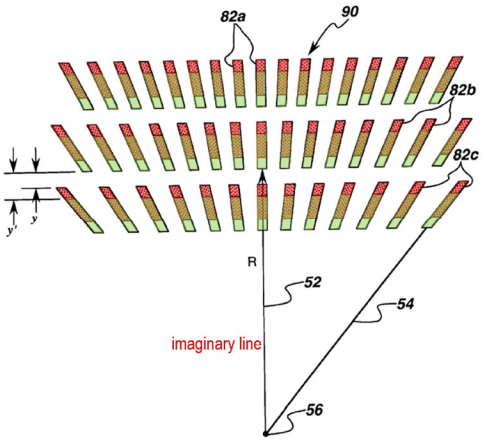


fig. 13

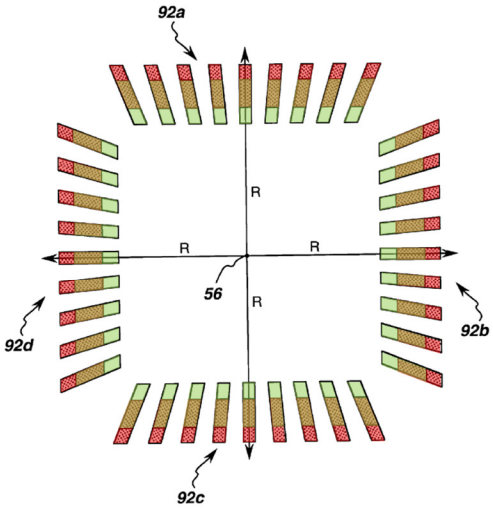


fig. 14

4. Claim 3: "The electronic device of claim 1, wherein: the first bump has a same inclination angle as the first pad; and the second bump has a same inclination angle as the second pad."

As shown in the exemplary mapping in FIG. 7, the first bump has a same inclination angle as the first pad; and the second bump has a same inclination angle as the second pad. (EX1002, ¶100; *see also* EX1004, 4:32-5:11.)

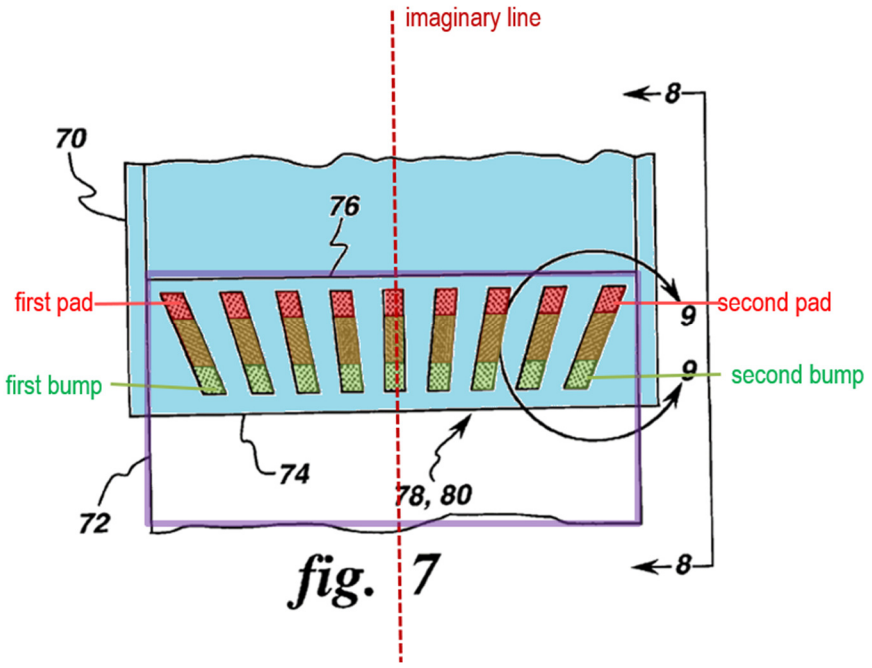


fig. 7

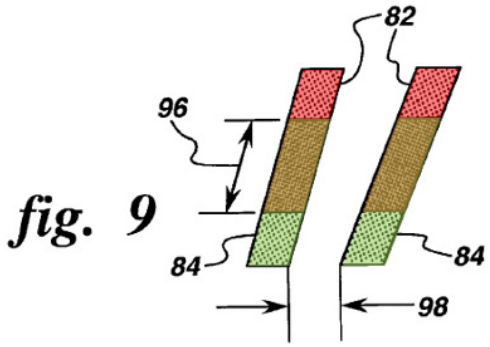


fig. 9

FIGs. 13 and 14 each discloses this limitation. (EX1002, ¶101; *see also* EX1004, 6:44-46, 7:18-26.)

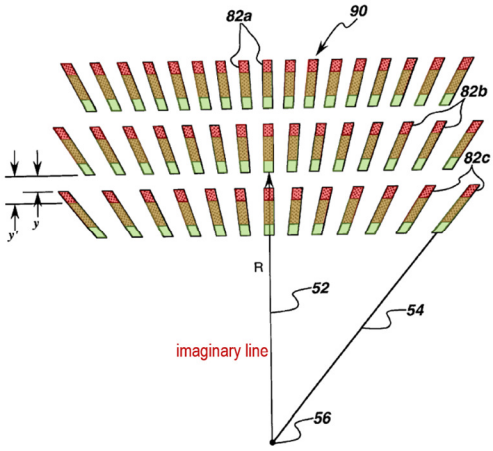


fig. 13

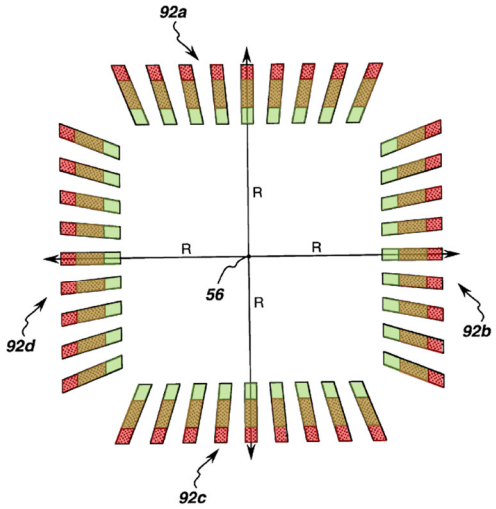


fig. 14

5. Claim 4: "The electronic device of claim 1, wherein a shape of the first bump corresponds to a shape of the first pad, and a shape of the second bump corresponds to a shape of the second pad."

Wildes discloses the shapes of its bumps correspond to the shapes of the corresponding pads. In the example shown in FIG. 7, the first bump and the first

pad have the same shape; the second bump and the second pad have the same shape. (EX1002, ¶102; *see also* EX1004, 4:56-5:11.)

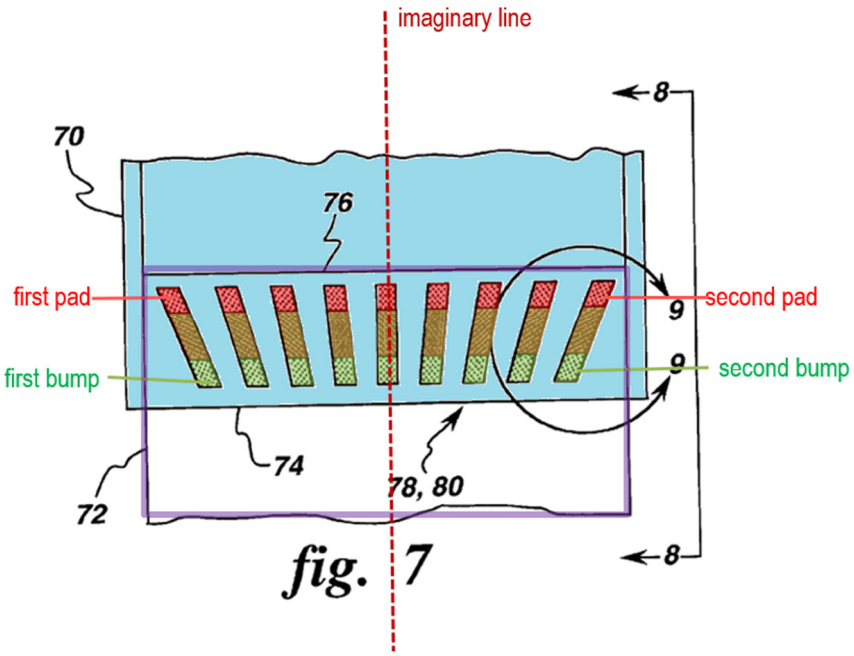


fig. 7

FIGs. 13 and 14 each discloses this limitation. (EX1002, ¶103; *see also* EX1004, 6:44-46, 7:18-26.)

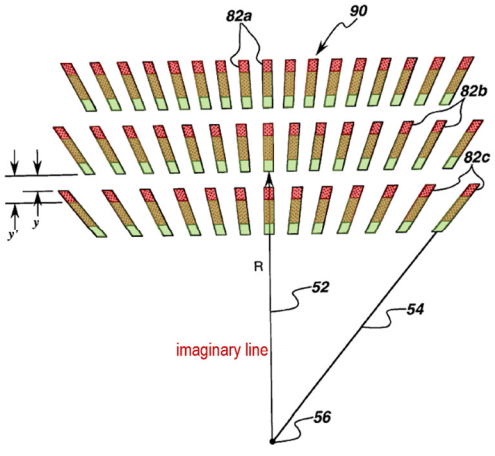


fig. 13

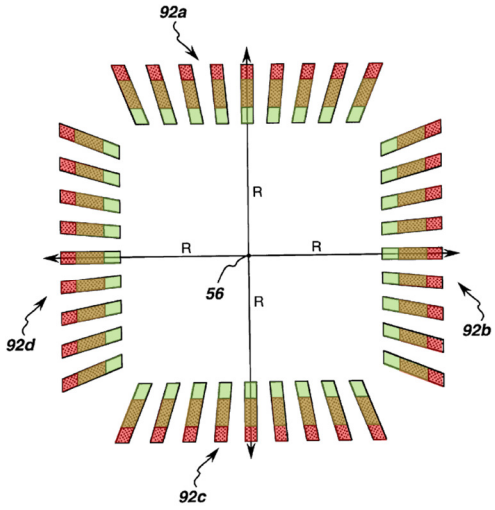


fig. 14

6. Claim 5: "The electronic device of claim 1, wherein the first pad is electrically connected with the first bump and the second pad is electrically connected with the second bump."

FIG. 7 shows that the first pad is electrically connected with the first bump and the second pad is electrically connected with the second bump. (EX1002, ¶104.)

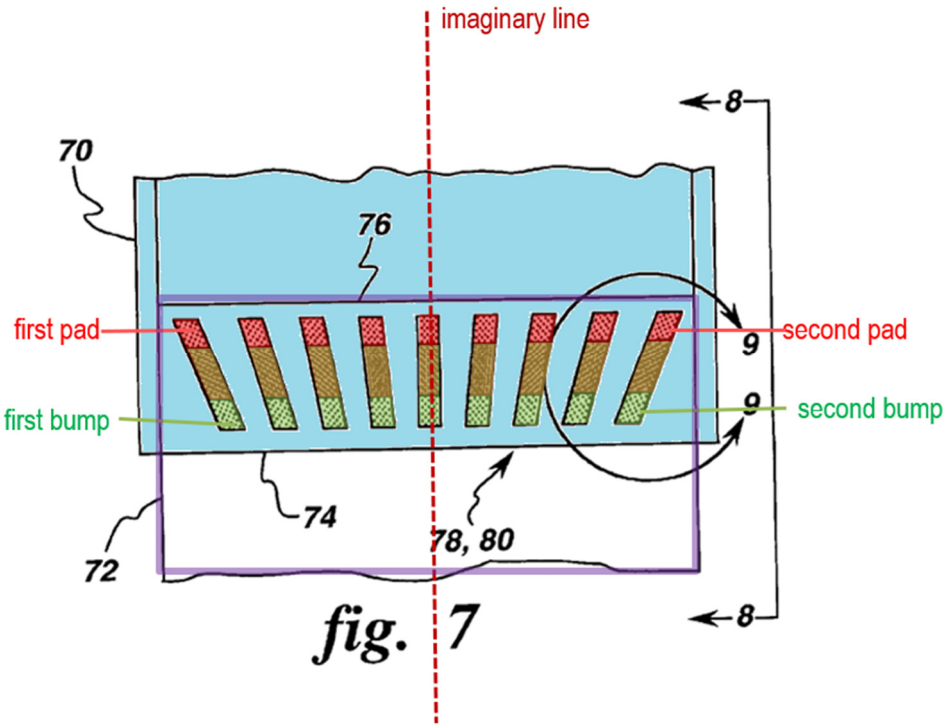


fig. 7

In FIGs. 13 and 14, each ***pad*** and each corresponding ***bump*** are electrically connected. (EX1002, ¶105; *see also* EX1004, 6:44-46, 7:18-26.)

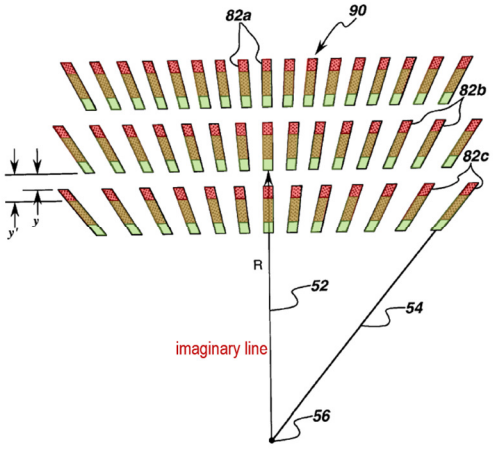


fig. 13

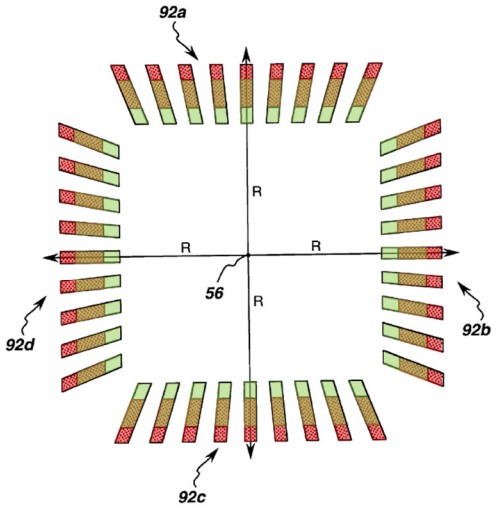


fig. 14

7. Claim 6: "The electronic device of claim 1, wherein an area of the first pad is greater than an area of the first bump."

Wildes discloses that the connection pads may experience "shrinkage or ***swelling*** of the parts during manufacturing." (EX1004, 1:58-61.) The swelling would cause a connection pad on the array substrate to have a greater area than a corresponding bump on the integrated circuit. (EX1002, ¶106.) An example of such swelling is shown with reference to FIG. 12. The swelling of the substrate causes the connection pads to expand in width and/or length, thus resulting in a greater area. (EX1002, ¶107-109.)

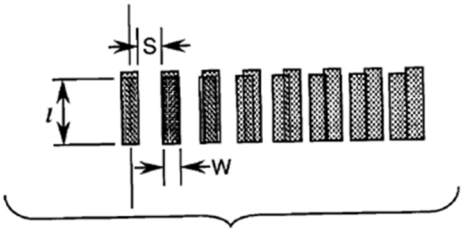


fig. 11

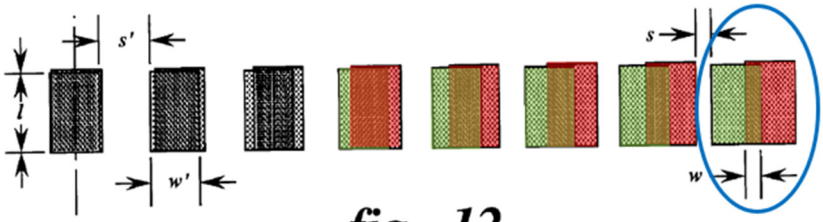


fig. 12

8. Claim 7: "The electronic device of claim 1, wherein: the first bump comprises a first region and a second region; and the first region overlaps the first pad and the second region does not overlap the first pad."

Wildes discloses this limitation. In the exemplary mapping in FIG. 9, each bump has an upper half that overlaps with the corresponding pad and a lower half that does not overlap with the corresponding pad. (EX1002, ¶110; *see also* EX1004, 5:4-11.)

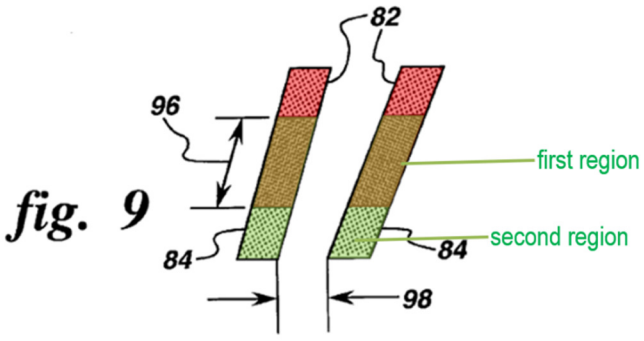


fig. 9

Each of FIGs. 6, 13, and 14 discloses this limitation. (EX1002, ¶111.)

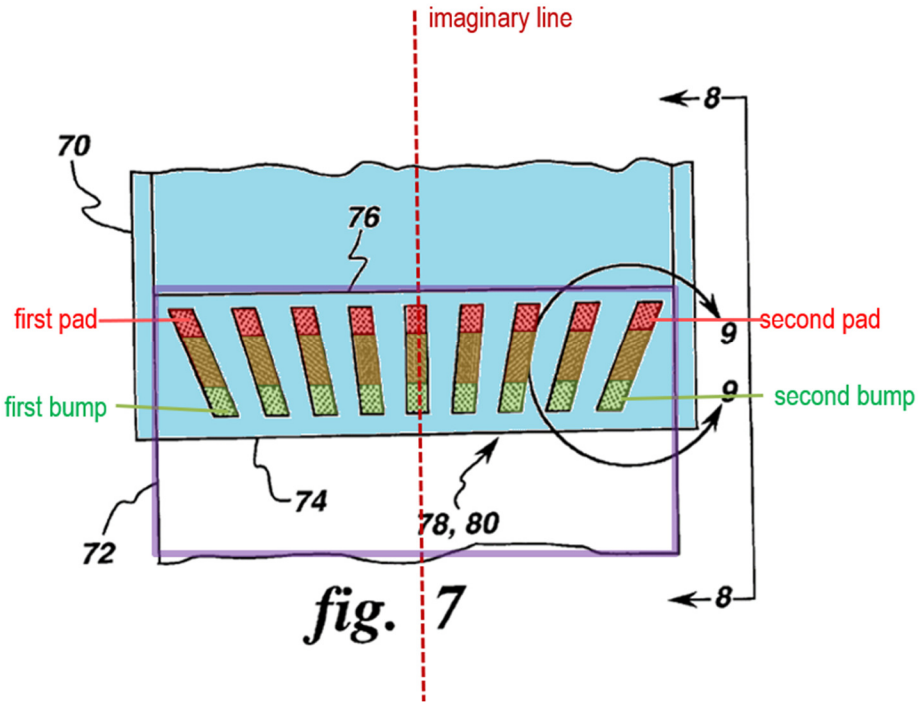


fig. 7

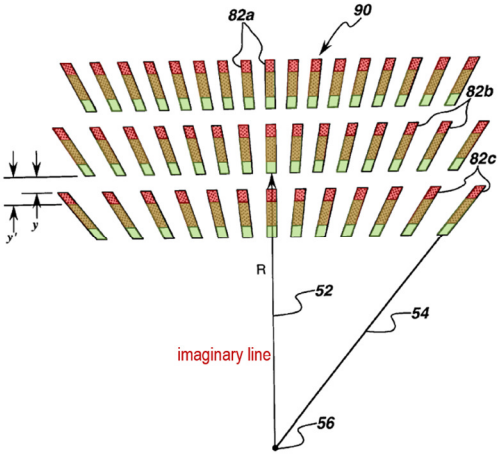


fig. 13

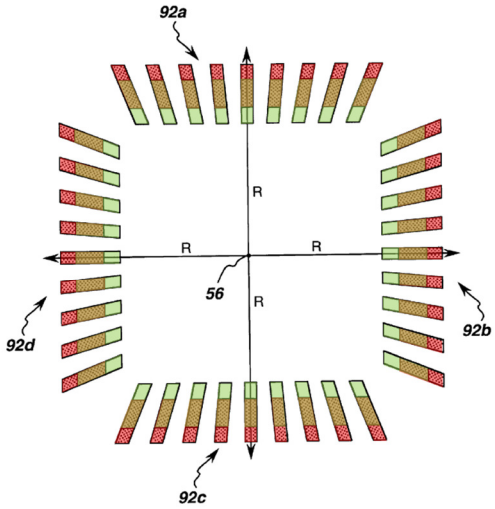


fig. 14

9. Claim 8: "The electronic device of claim 1, wherein at least one of the first pad and the second pad has a quadrangle shape."

In Fig. 6, each of the ***individual connection pads 82*** has a quadrangle shape. (EX1002, ¶112; *see also* EX1004, 4:56-5:11.) Each of the ***individual connection pads 82*** is a four-sided plane figure. (*Id.*)

FIGs. 13 and 14 also disclose this limitation. (*Id.*, ¶113; *see also* EX1004, 6:44-46, 7:18-26.)

10. Claim 9: "The electronic device of claim 2, wherein the pad portion further comprises a third sub-pad unit comprising a third pad having a rectangular shape and disposed between the first sub-pad unit and the second sub-pad unit."

Wildes discloses this limitation. FIG. 6 shows that the ***individual connection pads 82*** (i.e., the pad portion) comprises a ***center rectangular pad*** disposed between the first sub-pad unit and the second sub-pad unit. The ***center rectangular pad*** forms the "third sub-pad unit." (EX1002, ¶114; *see also* EX1004, 4:56-5:11.)

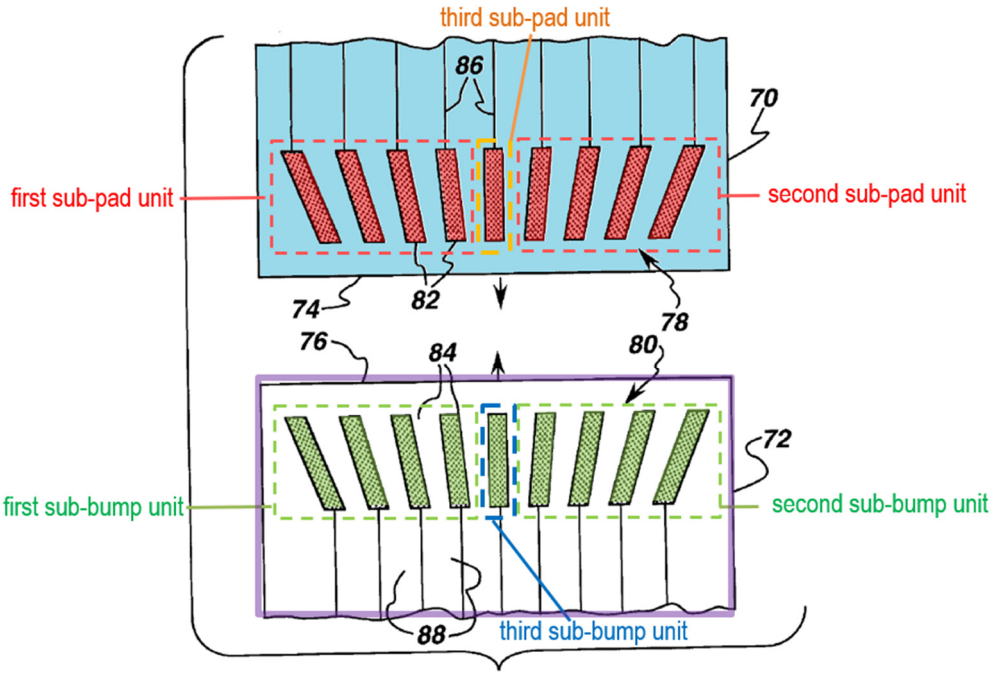


fig. 6

FIGs. 13 and 14 also disclose this limitation. (EX1002, ¶115; *see also* EX1004, 6:44-46, 7:18-26.)

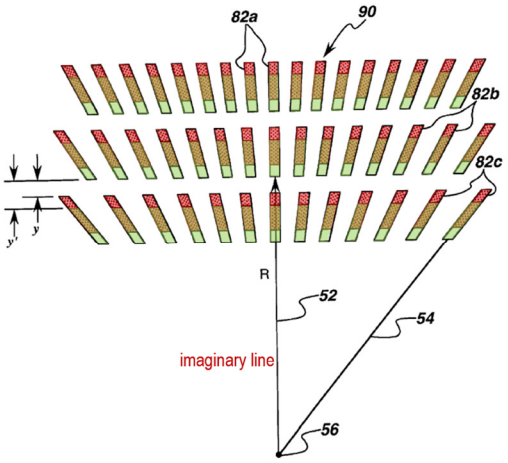


fig. 13

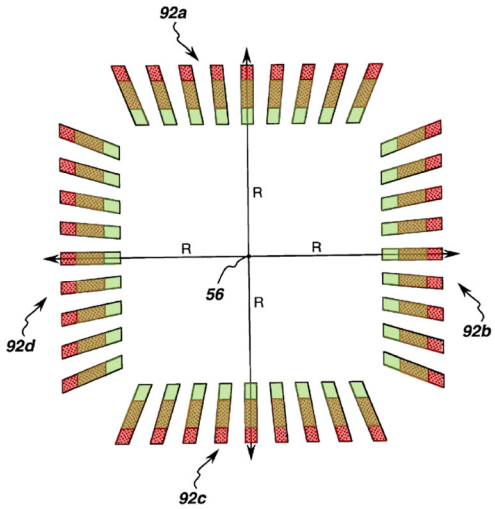


fig. 14

11. Claim 10: "The electronic device of claim 9, wherein the bump portion further comprises a third sub-bump unit comprising a third bump having a rectangular shape and disposed between the first sub-bump unit and the second sub-bump unit."

Wildes discloses this limitation. FIG. 6 shows that the ***individual connection pads 84*** (i.e., the pad portion) comprises a ***center rectangular pad***. The ***center rectangular pad*** forms the "third sub-bump unit." (EX1002, ¶116; *see also* EX1004, 4:56-5:11.) Exemplary annotations are shown in FIG. 6 below.

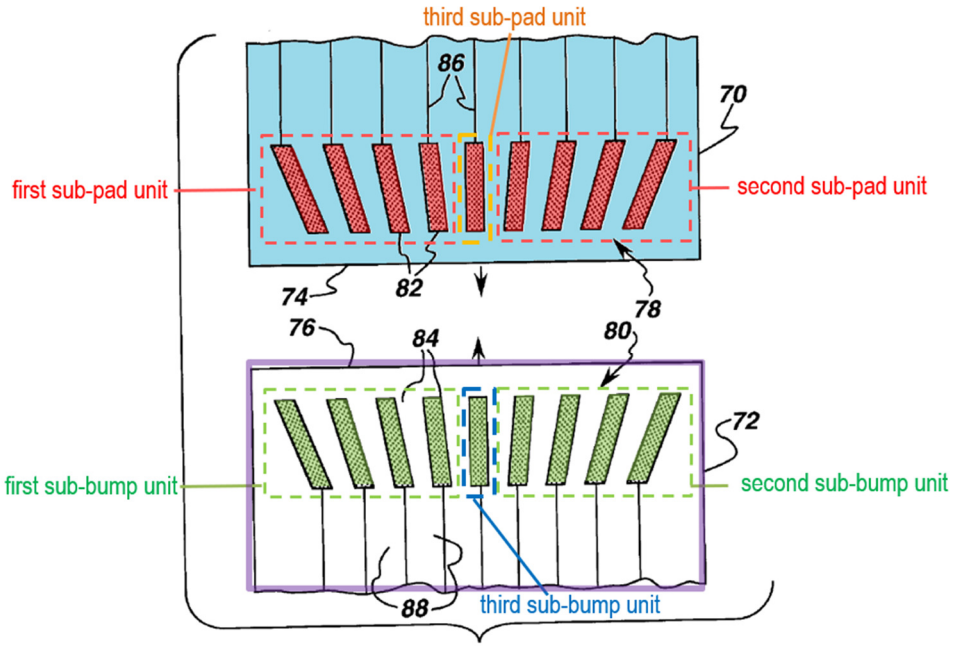


fig. 6

FIGs. 13 and 14 also disclose this limitation. Each row of the ***individual connection pads*** has a center rectangular pad. (EX1002, ¶117; *see also* EX1004, 6:44-46, 7:18-26.)

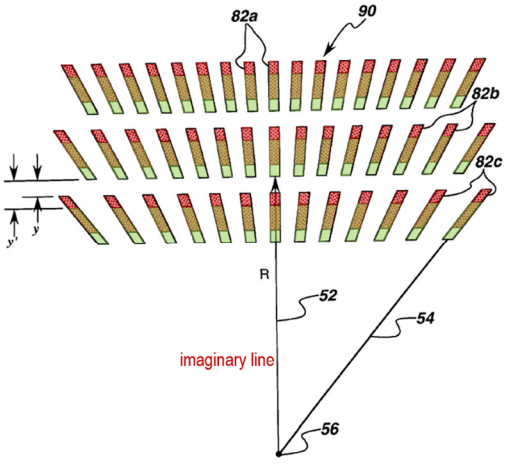


fig. 13

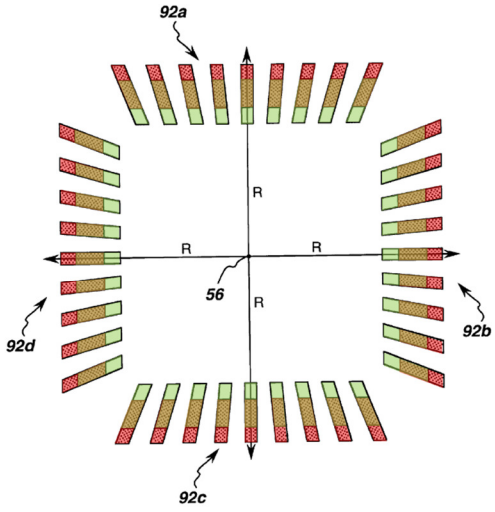


fig. 14

B. Ground 2: Wildes and Cristaldi Render Obvious Claims 1-10

1. Summary of Cristaldi

Cristaldi is a textbook published in 2009, qualifying as prior art at least under §§ 102(a)(1). The Examiner never found, and Applicant never cited, Cristaldi during prosecution.

Cristaldi states, "COG was first introduced in 1983 by Citizen[.]" (EX1007, 138; EX1002, ¶¶118-119.) "In this [Chip on Glass or COG] approach the ***IC*** is mounted directly on the ***glass substrate***, avoiding the use of the flex and reducing costs." (*Id.*)

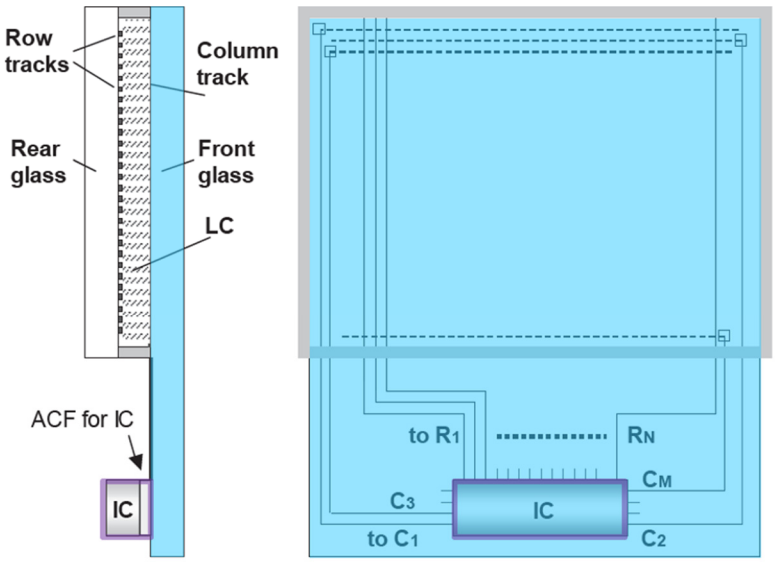


Fig. 4.27 LC panel with COG driver IC

(EX1008, 138.)

Cristaldi provides microscopic images of the "***gold bumps***" of an ***IC*** below, which apply to COG and COF equally. (EX1007, 138; EX1002, ¶120-121.)

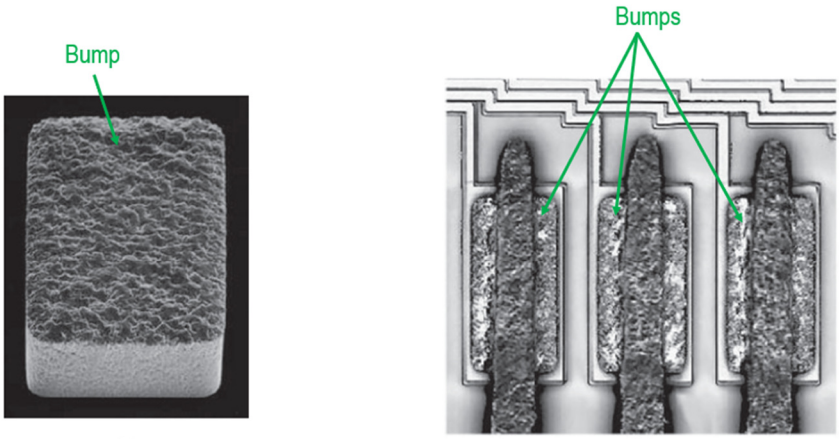


Fig. 4.26 Micrographs of (**a**) a gold bump and (**b**) connection between bumps and inner leads in COF via gold-tin eutectic bonding [TNF2003]

(EX1008, 137.)

"After prebonding the ACF to the glass with mild heat and low pressure, the ***driver IC*** is aligned in such a way that its ***bump pattern*** matches the ***pad pattern*** on the ***glass***." (EX1007, 138; EX1002, ¶122-123.)

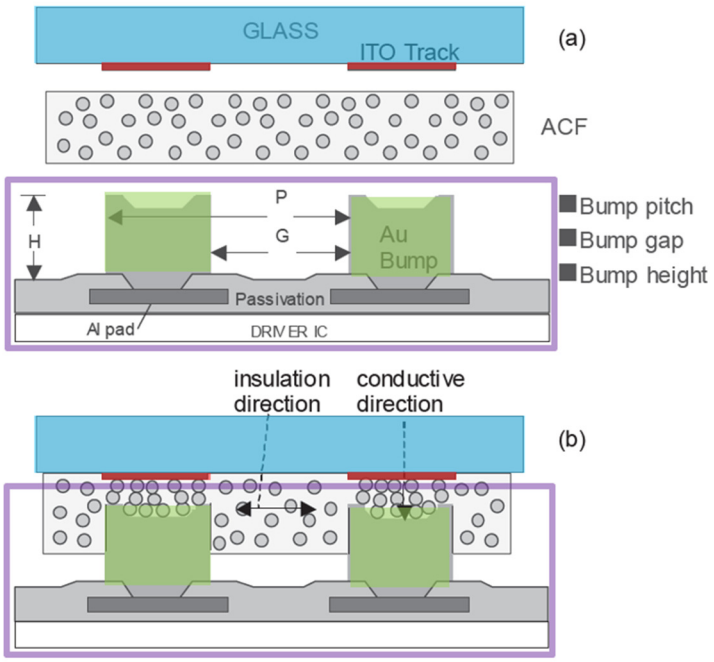


Fig. 4.28 COG technique. Cross section of a driver IC, Bumps, ACF, and Glass with typical dimensions: (**a**) before and (**b**) after electrical connection is formed

2. Claim 1

a. Preamble: "An electronic device, comprising:"

Wildes discloses the preamble. (*Supra* V.A.2.a.)

Cristaldi is titled "Liquid Crystal Display Drivers: Techniques and Circuits." (EX1007, Title.) A POSITA would understand that the liquid crystal display is or can be a part of an electronic device. (EX1002, ¶124-25.)

b. 1[a]: "an array substrate;"

Wildes discloses element 1[a]. (*Supra* V.A.2.b.)

Cristaldi discloses that "[i]n this [Chip on Glass or COG] approach the IC is mounted directly on the ***glass substrate***, avoiding the use of the flex and reducing costs." (EX1007, 138.) Figure 4.27 of Cristaldi "depicts an LCD panel with Driver IC connected via COG approach." (EX1007, 138.) The "***front glass***" of the LCD panel is an "array substrate." (*Id.*; EX1002, ¶126-128)

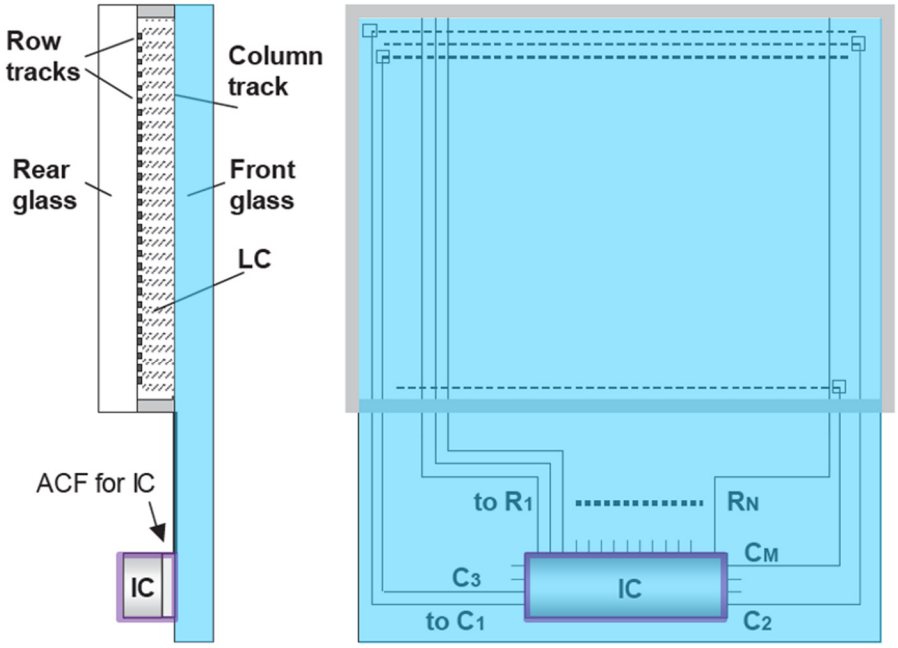


Fig. 4.27 LC panel with COG driver IC

(EX. 1008.)

c. 1[b]: "a pad portion disposed on the array substrate; and"

Wildes discloses element 1[b]. (*Supra* V.A.2.c; EX1002, ¶129.)

Cristaldi also discloses a "pad portion disposed on the array substrate." (EX1007, 138.) In FIG. 4.28, two electrodes, each marked as "***ITO Track***," are disposed on the array substrate. (EX1007, 138-139.) An ITO Track can refer to an electrode made of indium oxide and tin oxide ("ITO"). (EX1002, ¶130.) ITO Tracks are commonly applied on glass substrates and act as connection pads that conduct electricity. (*Id.*; *see also* EX1007, Fig. 5.7.)

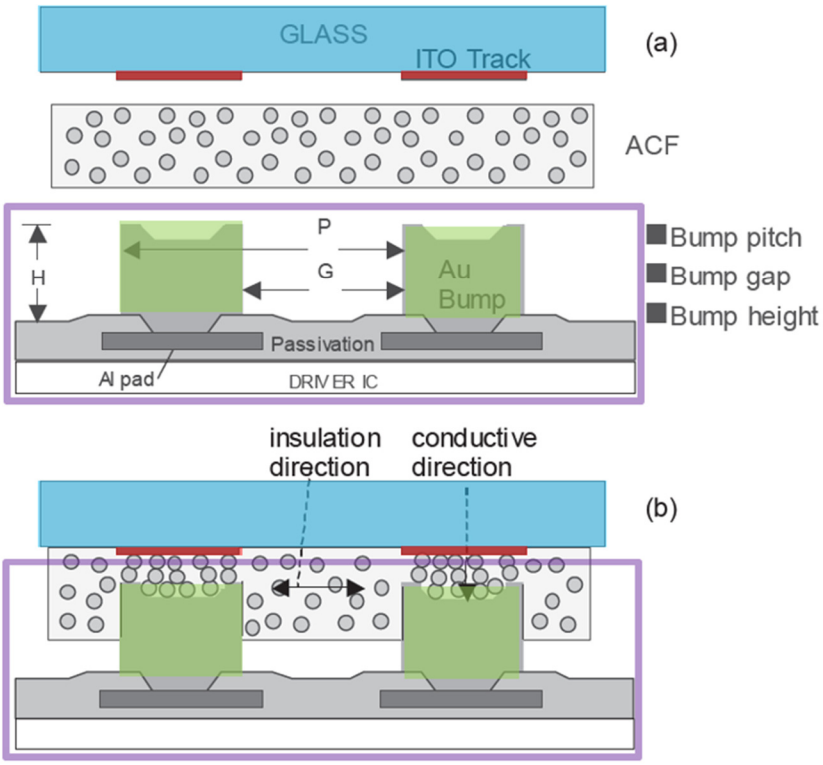


Fig. 4.28 COG technique. Cross section of a driver IC, Bumps, ACF, and Glass with typical dimensions: **(a)** before and **(b)** after electrical connection is formed

(EX1008, 139.)

d. 1[c]: "an integrated circuit disposed on the pad portion and comprising a bump portion;"

Wildes discloses element 1[c]. (*Supra* V.A.2.d.)

Figure 4.27 of Cristaldi "depicts an LCD panel with ***Driver IC*** connected via COG approach." (EX1007, 138; EX1002, 131-134.)

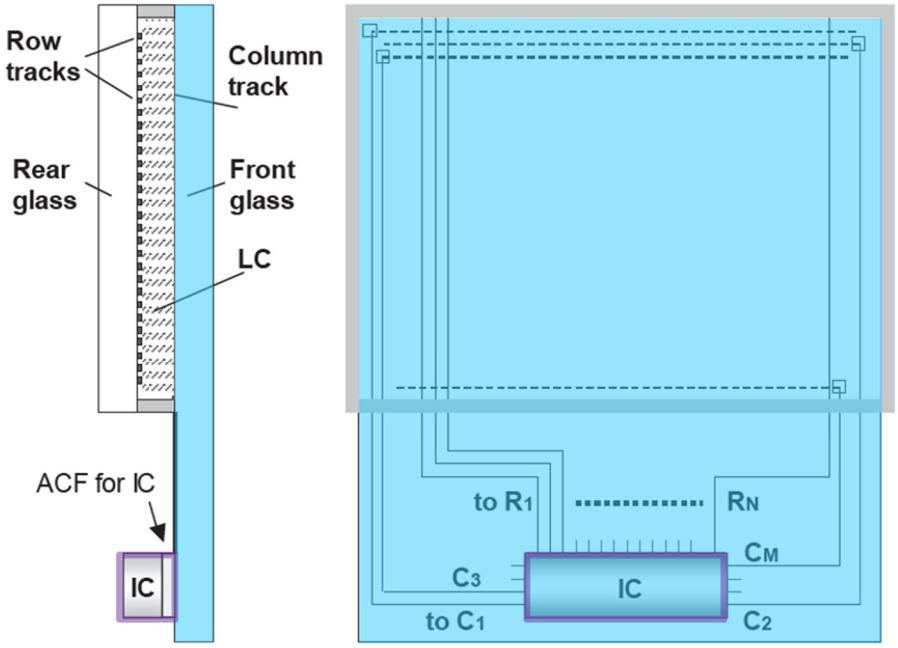


Fig. 4.27 LC panel with COG driver IC

(EX. 1008.)

Cristaldi discloses that the integrated circuit comprises "***gold bumps***."

(EX1007, 138.)

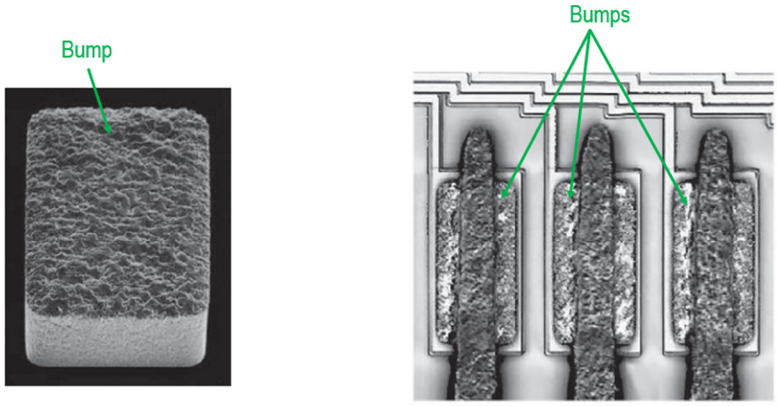


Fig. 4.26 Micrographs of (**a**) a gold bump and (**b**) connection between bumps and inner leads in COF via gold-tin eutectic bonding [TNF2003]

The bumps on the integrated circuit are disposed on the pad portion. "After prebonding the ACF to the glass with mild heat and low pressure, the ***driver IC*** is aligned in such a way that its ***bump pattern*** matches the ***pad pattern*** on the ***glass***." (EX1007, 138.)

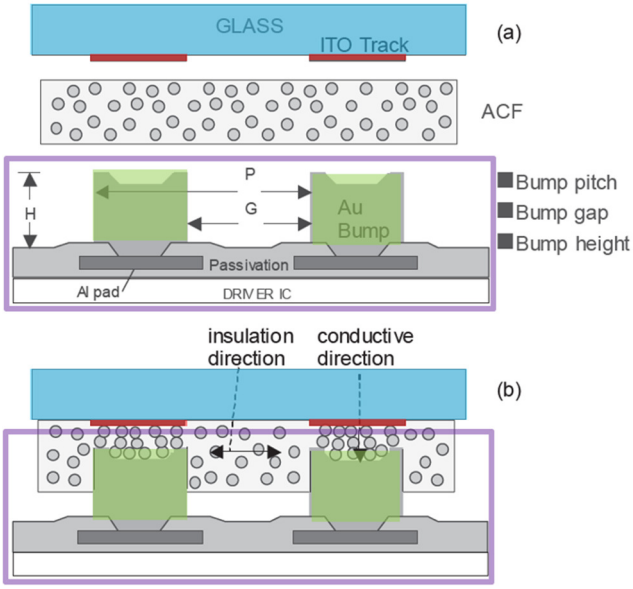


Fig. 4.28 COG technique. Cross section of a driver IC, Bumps, ACF, and Glass with typical dimensions: (**a**) before and (**b**) after electrical connection is formed

(EX1008, 139.)

e. 1[d]: "wherein: the pad portion comprises a first sub-pad unit comprising an inclined first pad and a second sub-pad unit comprising an inclined second pad;"

Wildes discloses element 1[d]. (*Supra* V.A.2.e.)

f. 1[e]: "the first pad and the second pad are inclined in different directions symmetrically about an imaginary line that divides the pad portion; and;"

Wildes discloses element 1[e]. (*Supra* V.A.2.f.)

g. 1[f]: "the pad portion is electrically connected with the bump portion;"

Wildes discloses element 1[f]. (*Supra* V.A.2.g.)

Cristaldi discloses element 1[f]. (*See* EX1007, 138; EX1002, ¶138)

h. 1[g]: "the bump portion comprises a first sub-bump unit comprising an inclined first bump and a second sub-bump unit comprising an inclined second bump;"

Wildes discloses element 1[g]. (*Supra* V.A.2.h.)

i. 1[h]: "the first bump and the second bump are inclined in different directions symmetrically about the imaginary line that divides the pad portion."

Wildes discloses element 1[h]. (*Supra* V.A.2.i.)

3. Claim 2: "The electronic device of claim 1, wherein at least one of the first pad and the second pad has a parallelogram shape."

Wildes discloses claim 2. (*Supra* V.A.3.) Cristaldi discloses claim 2 as it discloses rectangular bumps and "matching" pad patterns. (EX1002, ¶141.)

4. Claim 3: "The electronic device of claim 1, wherein: the first bump has a same inclination angle as the first pad; and the second bump has a same inclination angle as the second pad."

Wildes discloses claim 3. (*Supra* V.A.4.)

5. Claim 4: "The electronic device of claim 1, wherein a shape of the first bump corresponds to a shape of the first pad, and a shape of the second bump corresponds to a shape of the second pad."

Wildes discloses claim 4. (*Supra* V.A.5.) Cristaldi discloses that "[a]fter prebonding the ACF to the glass with mild heat and low pressure, the ***driver IC*** is

aligned in such a way that its ***bump pattern*** matches the ***pad pattern*** on the ***glass***."

(EX1007, 138.)

6. Claim 5: "The electronic device of claim 1, wherein the first pad is electrically connected with the first bump and the second pad is electrically connected with the second bump."

Wildes discloses claim 5. (*Supra* V.A.7.) Cristaldi discloses claim 5.

(*Supra* V.B.2.g.)

7. Claim 6: "The electronic device of claim 1, wherein an area of the first pad is greater than an area of the first bump."

Wildes discloses claim 6. (*Supra* V.A.6.)

8. Claim 7: "The electronic device of claim 1, wherein: the first bump comprises a first region and a second region; and the first region overlaps the first pad and the second region does not overlap the first pad."

Wildes discloses claim 7. (*Supra* V.A.8.)

9. Claim 8: "The electronic device of claim 1, wherein at least one of the first pad and the second pad has a quadrangle shape."

Wildes discloses claim 8. (*Supra* V.A.9.) Cristaldi discloses claim 8 as it

discloses rectangular bumps and "matching" pad patterns.

10. Claim 9: "The electronic device of claim 2, wherein the pad portion further comprises a third sub-pad unit comprising a third pad having a rectangular shape and disposed between the first sub-pad unit and the second sub-pad unit."

Wildes discloses claim 9. (*Supra* V.A.10.)

11. Claim 10: "The electronic device of claim 9, wherein the bump portion further comprises a third sub-bump unit comprising a third

bump having a rectangular shape and disposed between the first sub-bump unit and the second sub-bump unit."

Wildes discloses claim 10. (*Supra* V.A.11.)

12. A POSITA would have been motivated to combine Wildes and Cristaldi.

At the time of the invention, it would have been obvious to apply Wildes' techniques to an LCD device in Cristaldi. (EX1002, ¶150.) Wildes solves potential misalignment in the electrical connection between connection pads on two substrates, one or both of which may deform. (*Id.*) Wildes teaches that a "major application is electrical connection to flat panel (LCD) displays . . . ." (EX1004, 1:48-50.) Cristaldi describes a well-known LCD technique for connecting an LCD substrate with a driving integrated circuit. (EX1002, ¶150.) As discussed above, both flexible and rigid substrate arrays were common. (*Supra V.A.2.b*.) Thus, Wildes and Cristaldi are from the same field of endeavor and reasonably pertinent to the same technical problems of providing electrical connection between an array substrate and its driving circuit in an LCD device. (*Id*.)

The Wildes-Cristaldi combination can result in a system in which Wildes' techniques are applied in LCD displays. For example, Cristaldi's ITO Tracks (i.e., pads) on the glass substrate and the bumps on the IC can adopt Wildes' fanout array configuration to address misalignment. Cristaldi already teaches that the two

components should be aligned "in such a way that its ***bump pattern matches the pad pattern on the glass***." (EX1007, 138.) The simple modification of making them inclined as taught by Wildes does not involve any extensive re-design and would be easy to manufacture. (EX1002, ¶151; *Supra V.A.2.d*.) Additionally or alternatively, the Wildes-Cristaldi combination can result in a system in which one of the two substrates (e.g., substrate 70 in FIG. 6) in Wildes is an array substrate and the other substrate (e.g., substrate 72 in FIG. 6) in Wildes is an integrated circuit as taught by Cristaldi. This system is obvious in light of Wildes by itself; for example, FIG. 14 itself discloses mounting an integrated circuit with inclined bumps for electrical connection in a structure identical or at least analogous to IC bonded to array substrate of LCD display. (*Supra V.A.2.b*.) A POSITA would further be motivated to implement Wildes in this manner in light of the teaching of Cristaldi, because Wildes states that its "major application is electrical connection to flat panel (LCD) displays" and Cristaldi teaches a common LCD technology. (EX1004, 1:48-50; EX1002, ¶151.)

The combination gains significant benefits. In COG technology, the glass substrate may deform during manufacturing. (EX1002, ¶152.) Cristaldi discloses that heat and stress are involved during manufacturing, which can cause deformation of glass. (EX1007, 138.) And even relatively small deformation can be significant due to the density of the pads. (EX1002, ¶152; *see also* EX1005,

1:11-2:6.) For COP, the misalignment between IC and array substrate can be more severe. (EX1002, ¶152.) Misalignment issue is precisely what Wildes solves. The Wildes-Cristaldi system would ensure that the resulting display can provide reliable electrical connection, thus providing reliable graphics and preventing short circuits. (*Id.*)

Combining Cristaldi with Wildes would improve the capabilities of Cristaldi in the same way, because the Wildes-Cristaldi combination would ensure pad-bump alignment despite potential deformation. (EX1002, ¶153.) The combination would yield predictable results of effectively ensuring electrical connection between the array substrate and the integrated circuit. (*Id*.) Further, it would have been obvious to try combining Cristaldi with Wildes, as there is a finite number of identified, predictable solutions, without requiring much effort and with a reasonable expectation of success. (*Id*.) There was a finite number of potential pad/bumps shapes, such as rectangle, square, and circle, that were commonly seen in the industry at the time of the invention. (*Id*.; *see also* EX1010, 313.) The known benefits of Wildes would prompt the application of Wildes in the same field based on design incentives and other market forces to produce reliable displays that have high tolerance for various manufacturing and use conditions. (*Id*.)

C. Ground 3: Imaoka and Lieshout Render Obvious Claims 1-10

1. Summary of Lieshout

Lieshout was filed on June 15, 2007, and published on December 21, 2007, qualifying as prior art at least under §§ 102(a)(1) and 102(a)(2). (EX1007-1009.) The Examiner never found, and Applicant never cited, Lieshout during prosecution.

Lieshout is directed to "varied pitch connection devices for integrated circuit (IC) bonding." (EX1005, 1:1-3; EX1002, ¶154-161.) Lieshout "provide[s] a connection device wherein ***misalignment problems for IC chips***, notably in a flip-chip bonding area, are counteracted." (EX1005, 2:21-23.) Misalignment can occur because the "substrate can change size due to manufacturing stresses." (EX1005, 1:15-16.) To address potential misalignment, in FIG. 5, an array substrate includes "continuous ***bond pads***" that "provide a smooth transition to adjust and attach the connection bumps of the connection bump devices." (EX1005, 8:2-3.) In FIG. 6, "the two parallel ***bond pad sets*** provide connections for two parallel connection bump sets on a connection bump device." (EX1005, 8:15-17.) As shown, these bond pads are inclined.

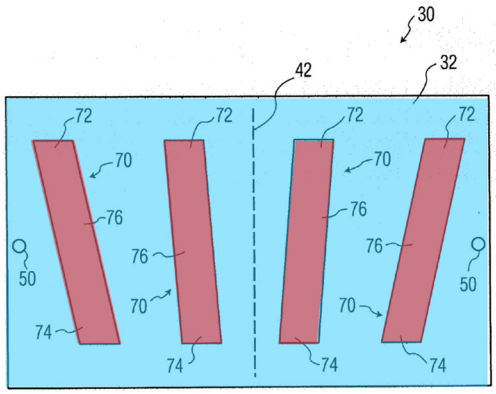


FIG. 5

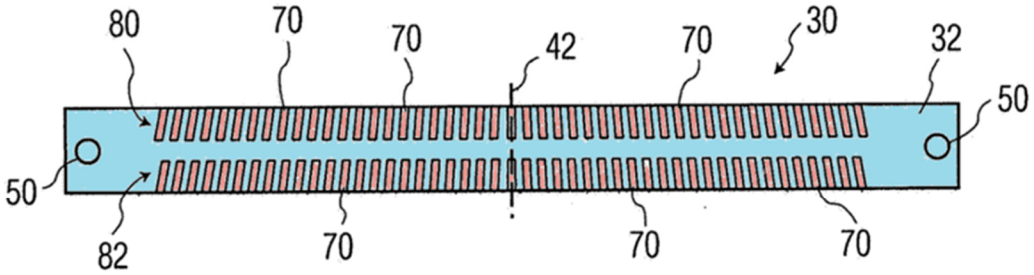


FIG. 6

In FIG. 7, Lieshout provides "an alignment system" that "adjusts the position of a connection bump device with connection bumps relative to a varied pitch connection device with bond pads ***so that the connection bumps and the bond pads align***." (EX1005, 9:9-13.) In FIG. 7, the system includes ***bond pads 120*** and ***connection bumps 106***.

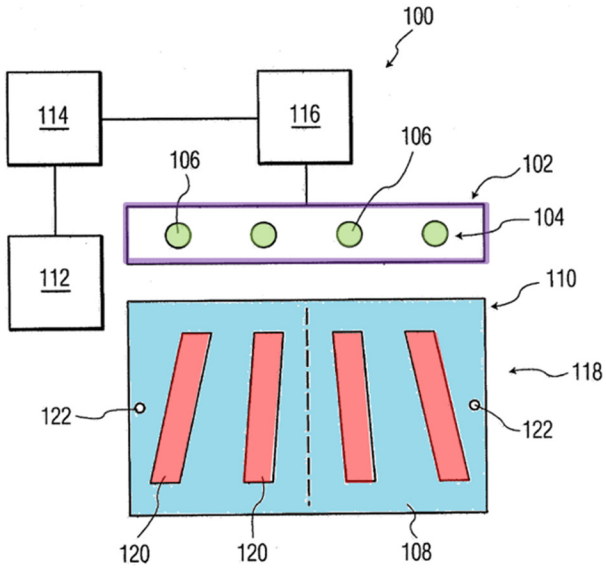


FIG. 7

Lieshout can "move the connection bump device 102 relative to the varied pitch connection device 110 ***by the y-displacement to align*** the ***connection bumps 106*** with the ***bond pads 120***." (EX1005, 10:18-21.)

While ***the connection bumps 106*** are illustrated as circles in FIG. 7, Lieshout emphasizes that "[t]he pattern and spacing of bond pad locations on the photo masks used during TFT processing are ***the same as the pattern and spacing of connection IC bumps*** on the IC chips, so the structures on the substrate on the rigid support have the same pattern and spacing as on the photo masks." (EX1005, 1:24-28.) Thus, it would have been obvious to a POSITA that Lieshout's ***connection bumps 106*** can be in the same pattern (i.e., inclined parallelograms) for coupling with the ***bond pads 120***. (EX1002, ¶¶154-161.)

2. Summary of Imaoka

Imaoka was filed on July 25, 2002, and published on January 30, 2003, qualifying as prior art at least under §§ 102(a)(1) and 102(a)(2). The Examiner never found, and Applicant never cited, Imaoka during prosecution.

Imaoka is directed to solving potential misalignment in the electrical connection between an array substrate of a display and an integrated circuit that drives the array substrate. (EX1002, ¶162-173.) Imaoka teaches that the first terminals are inclined terminals disposed along lines "radially arranged passing through the first point" and similar second terminals. (EX1006, 5:28-32, claim 17.) When the first and second points are aligned, the first terminals and the second terminals are "overlapped and electrically connected with one another[.]" (*See*, *e.g.*, EX1006, 3:22-48.)

For example, FIG. 2A shows the ***terminals 26*** before they are electrically connected to the ***terminals 16***, and FIG. 2B shows how the ***terminals 26*** and the ***terminals 16*** are electrically connected to one another. (*See also* EX1006, 3:22-9:40.)

FIG. 2A

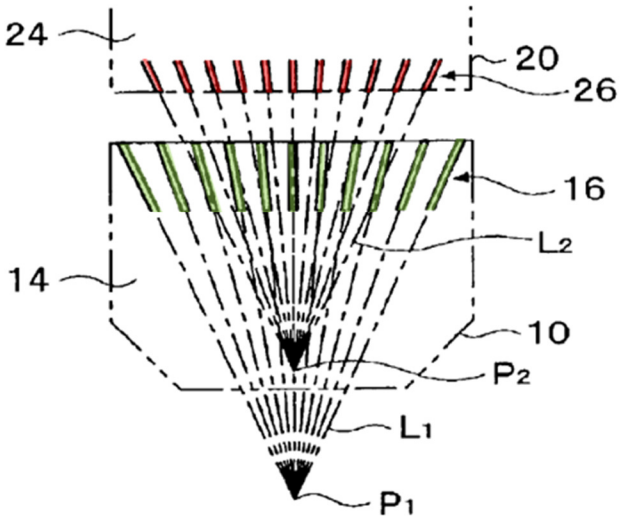


FIG. 2B

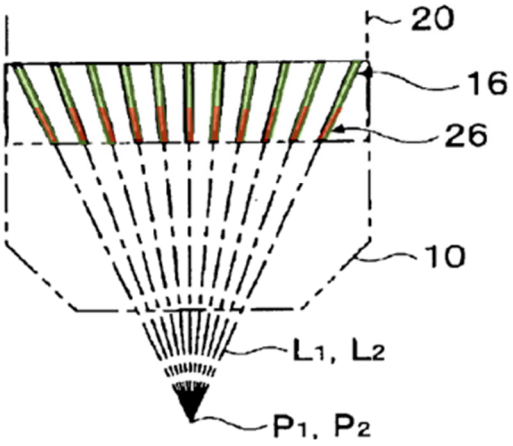
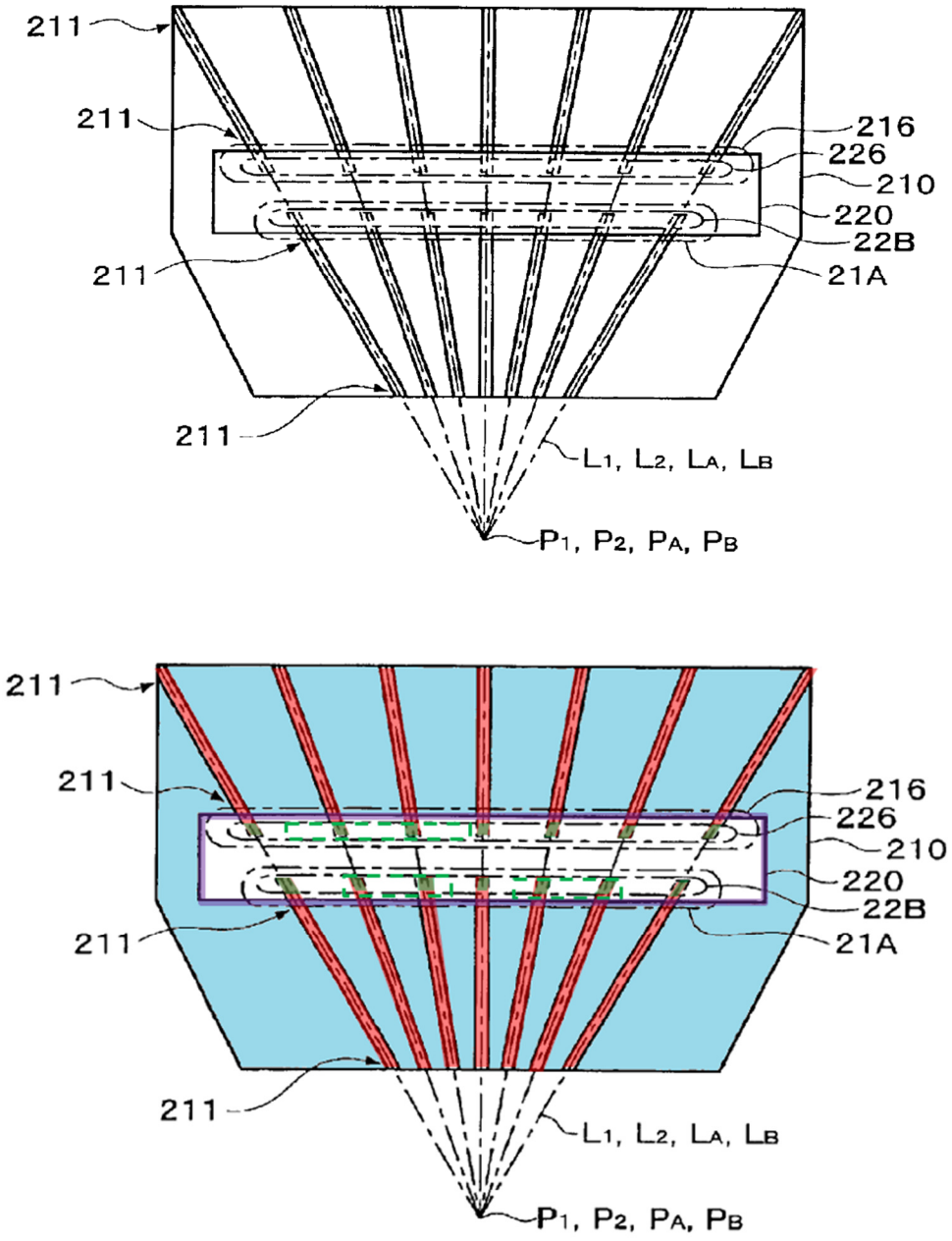


FIG. 11 is an exemplary application of Imaoka's techniques above. In FIG. 11, a first electronic component 210 includes ***terminals 216*** and ***terminals 21A***. Both are pad portions. (EX1002, ¶169.) The original version of FIG. 11 and an annotated version are provided below.



The electronic component 220 is "a ***chip component (for example, a semiconductor chip)***" and "***mounted on the first electronic component 210***." (EX1006, 17:64-67.) The integrated circuit 220 in FIG. 11 comprises a bump portion comprising "bumps." "The ***terminals 226*** of the second group may be any

of electrodes, pads or ***bumps***." (EX1006, 18:31-32.) Further, the integrated circuit 220 also comprises a B-group of ***terminals 22B***. Both ***terminals 226*** and ***terminals 22B*** are bump portions. (EX1002, ¶170.)

Imaoka teaches that potential misalignment is mitigated by the inclined terminals. (*See* EX1006, 11:26-36.)

3. Claim 1

a. Preamble: "An electronic device, comprising:"

Lieshout discloses its connection device can be arranged on "a display or a flexible display", which in turn can be "arranged in a portable device, like a mobile phone, a palmtop computer, an organizer, or the like." (EX1005, 9:2-4.) A POSITA would understand that these are examples of electronic devices. (EX1002, ¶174.)

b. 1[a]: "an array substrate;"

Lieshout discloses that "the display unit or the flexible display unit compris[es] at least one electronic component electrically connected to a ***substrate*** by means of a flip-chip bonding . . . ." (EX1005, 9:4-7.) Lieshout discloses "[f]lip-chip bonding provides a convenient way to make a large number of electrical connections between a silicon IC chip and a ***large substrate, such as a display backplane***." (EX1005, 1:12-14.)

FIG. 5 depicts an exemplary array substrate 32. "***The bond pad surface 32*** can be any surface capable of supporting bond pads for making connections." Lieshout discloses that ***bond pad surface 32*** may be "a plastic substrate," "a flexible or rigid circuit board," "a glass substrate." (*See* EX1005, 5:25-6:1.)

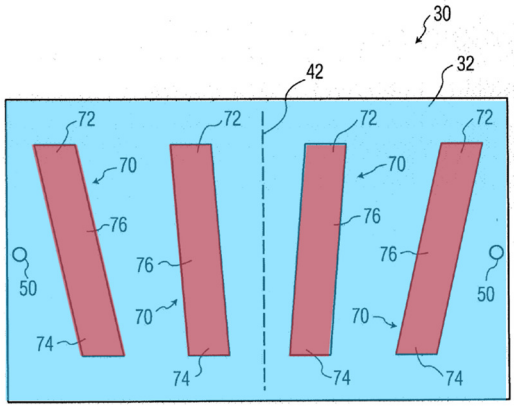


FIG. 5

FIGs. 6 and 7 each discloses an array substrate. (EX1002, ¶¶175-178; *see also* EX1005, 8:13-9:27.)

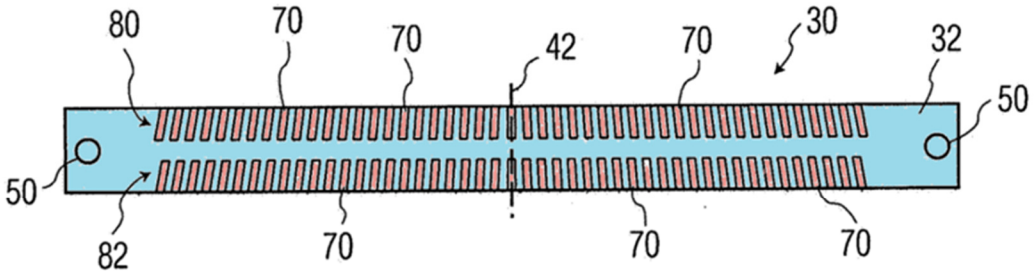


FIG. 6

c. 1[b]: "a pad portion disposed on the array substrate; and"

FIG. 5 provides "a front view of a varied pitch connection device with ***continuous bond pads*** made in accordance with the present invention. . . The varied pitch connection device 30 includes a number of ***continuous bond pads 70***. The continuous bond pads 70 are disposed on the ***bond pad surface 32***." (EX1005, 4:9-10, 8:3-5; EX1002, ¶¶179-182.)

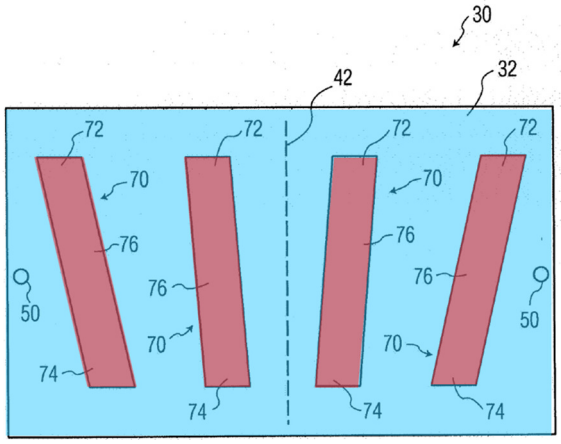


FIG. 5

FIG. 6 shows "a ***first bond pad set 80*** and a ***second bond pad set 82***. Each of the bond pad sets includes a number of continuous bond pads 70. Those skilled in the art will appreciate that any number of bond pad sets can be used as desired for a particular application, as required to ***match connection bump sets on a connection bump device***." (EX1005, 8:17-22 (emphasis added).)

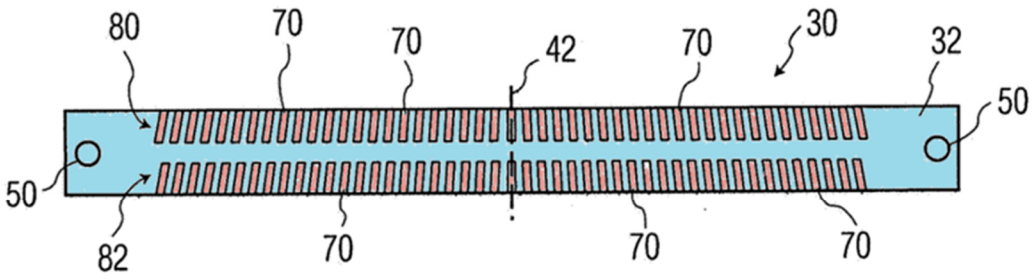


FIG. 6

Similarly, FIG. 7 depicts an "exemplary varied pitch connection alignment system 100" having "***a substrate 108*** having at least one varied pitch connection device 110[.]" (EX1005, 9:14-20.) "The varied pitch connection device 110 includes at least one ***bond pad set 118 with bond pads 120*** and alignment marks 122." (EX1005, 9:21-23.)

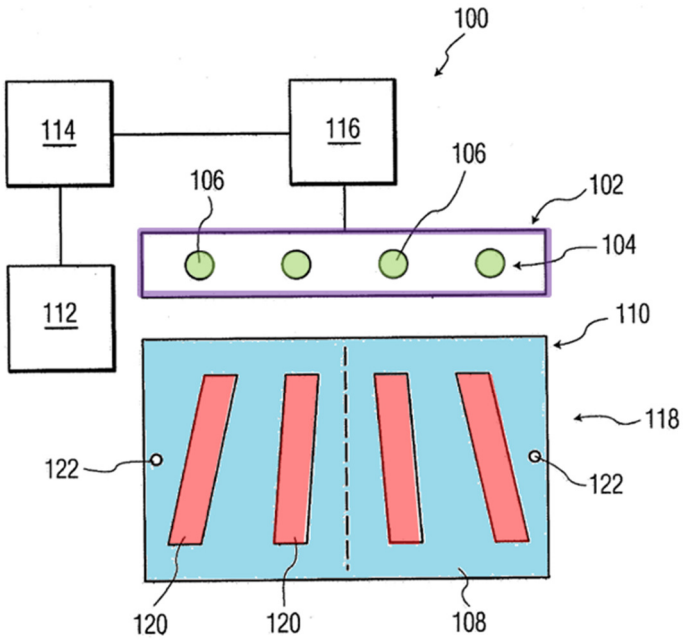


FIG. 7

Imaoka also discloses a pad portion disposed on the array substrate. For example, Imaoka states that FIG. 2A shows the ***terminals 26*** before they are electrically connected to the ***terminals 16***, and FIG. 2B shows how the terminals are electrically connected to one another. ***Terminals 26*** disclose the "pad portion." (EX1002, ¶183.)

FIG. 2A

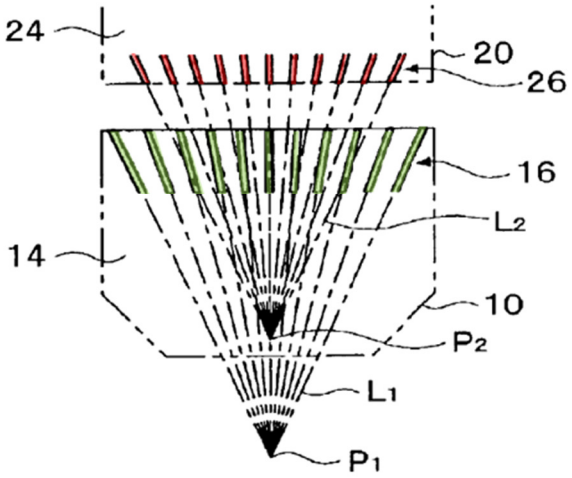
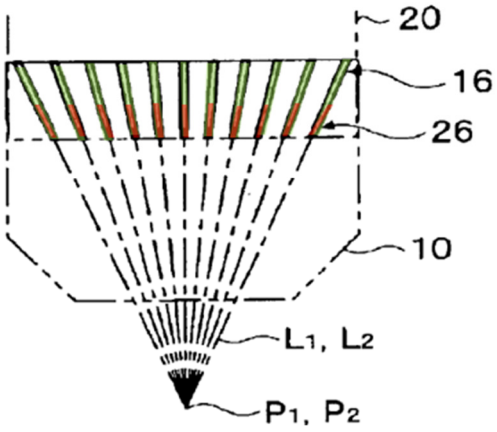
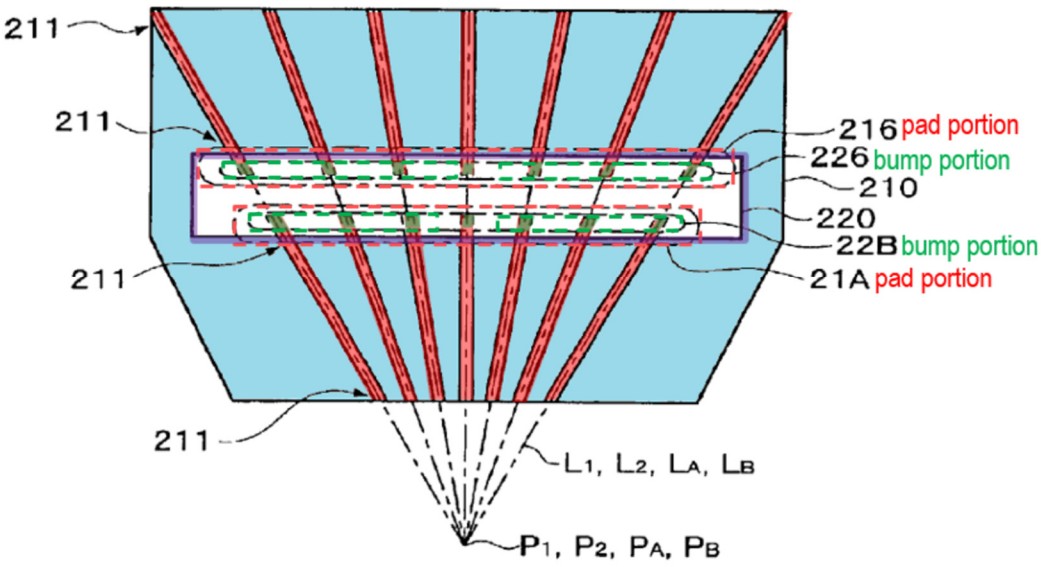


FIG. 2B



In FIG. 11, the substrate of the first electronic component 210 "includes a plurality of first terminals 211. (*See* EX1006, 17:60-18:59.) The ***terminals 216*** and the ***terminals 21A*** disclose a pad portion. (EX1002, ¶184.)



d. 1[c]: "an integrated circuit disposed on the pad portion and comprising a bump portion;"

Lieshout discloses that an integrated circuit is disposed on the ***pad portion*** and comprises a ***bump portion***. Lieshout states that "[t]he pattern and spacing of the ***connection IC bumps*** on the ***IC chip*** is fixed at manufacture. The substrate can change size due to manufacturing stresses. The ***connection IC bumps*** on the ***IC chip*** and ***bond pads*** on the ***substrate*** have to be accurately matched to provide good electrical connections." (EX1005, 1:14-18; EX1002, ¶¶185-191.)

Lieshout discloses that bumps of an integrated circuit is disposed on the bond pads in FIG. 5, although bumps are not depicted in FIG. 5. "The ***continuous bond pads*** provide a smooth transition to adjust and attach the ***connection bumps*** of the connection bump devices." (EX1005, 8:2-3.) Lieshout discloses that the

continuous bond pads "provide area for attachment of the ***connection bumps*** of the connection bump devices." (EX1005, 8:8-12.)

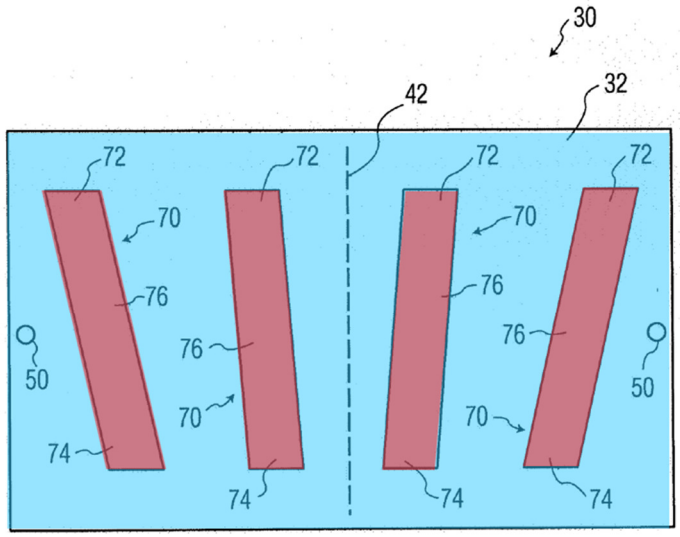


FIG. 5

FIG. 6 of Lieshout also discloses this limitation. "In this example, the two parallel ***bond pad sets*** provide connections for two parallel ***connection bump sets*** on a connection bump device. . . Those skilled in the art will appreciate that any number of ***bond pad sets*** can be used as desired for a particular application, as required to ***match connection bump sets on a connection bump device***." (EX1005, 8:15-22.)

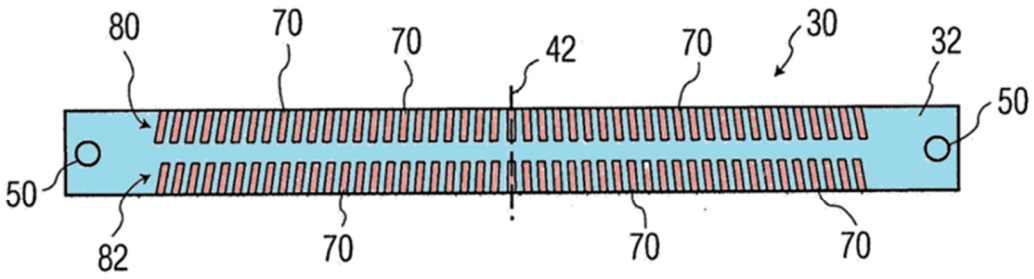


FIG. 6

"Referring to FIG. 7, the exemplary varied pitch connection alignment system 100 includes a connection bump device 102 with at least ***one connection bump set 104*** . . . ." (EX1005, 9:14-20.) "The connection bump set 104 includes ***connection bumps 106***." (EX1005, 9:20-21.)

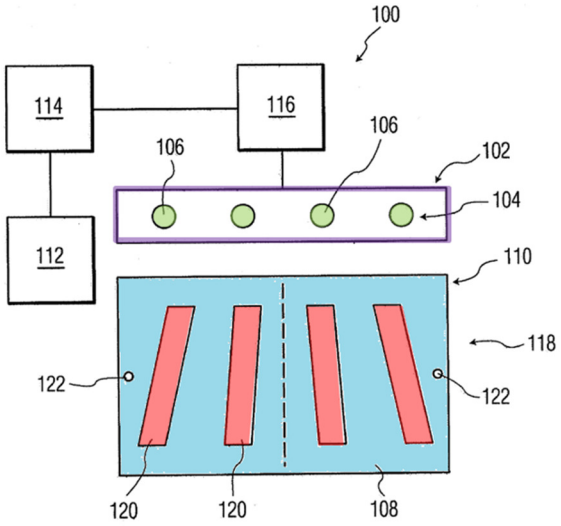


FIG. 7

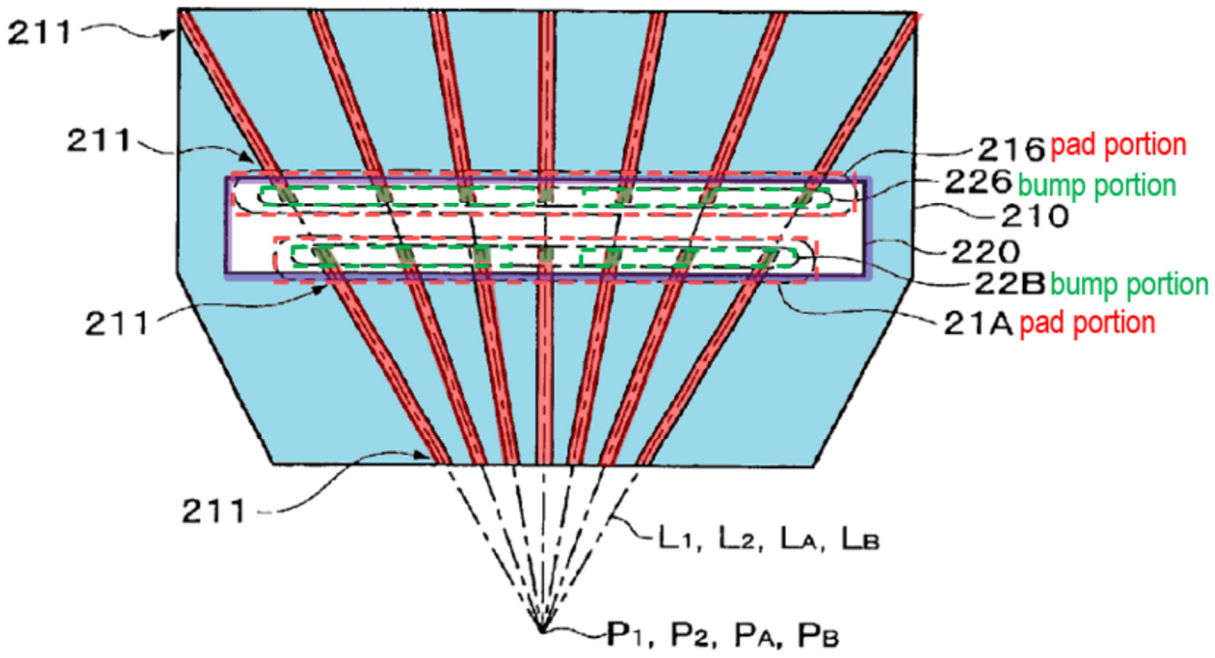
Importantly, although ***the connection bumps 106*** are illustrated as circles in FIG. 7, Lieshout emphasizes that "[t]he pattern and spacing of bond pad locations

on the photo masks used during TFT processing are ***the same as the pattern and spacing of connection IC bumps*** on the IC chips[.]" (EX1005, 1:24-28.) Thus, it would have been obvious to a POSITA that Lieshout's ***connection bumps 106*** can be in the same pattern (i.e., inclined parallelograms) for coupling with the ***bond pads 120***. (EX1002, ¶190.)

Lieshout discloses that the integrated circuit is disposed on the pad portion. Lieshout states that "[a] connection bump device 20 with ***connection bumps 24***, such as an IC chip with IC bumps, can be ***bonded*** to the ***bond pads*** on the ***substrate*** before or after the substrate is delaminated from the rigid support." (EX1005, 6:1-3.)

The purpose of Imaoka (e.g., FIGs. 2A-B, FIG. 11) includes providing driving signals to an LCD display via aligned electrical connections. (*See* EX1006, 10:21-26.) A POSITA would have understood that terminals 16 in FIGs. 2A-B provide electrical connection to an array substrate, which are analogous to IC bumps of Lieshout bonded to pads. (EX1002, 192.) Imaoka discloses an integrated circuit disposed on the pad portion and comprising a bump portion. In FIG. 11, the second electronic component 220 is "a ***chip component (for example, a semiconductor chip)***" and "***mounted on the first electronic component 210***." (EX1006, 17:64-67.) The ***integrated circuit 220*** in FIG. 11 comprises a bump portion. "The ***terminals 226*** of the second group may be any of electrodes, pads or

bumps." (EX1006, 18:28-33.) The ***terminals 226*** disclose a "bump portion." Imaoka teaches that the details of electrical connection shown in FIGs. 2A-B for preventing misalignment can be applied to the connection between the ***terminals 216*** and the ***terminals 226*** in FIG. 11. (*See* EX1006, 18:9-12, 18:17-20, 18:40-43, 18:56-59, 9:46-48.) FIG. 11 of Imaoka shows IC bumps bonded to a substrate, which is analogous to IC bumps bonded to an array substrate in Lieshout. (EX1002, 193; 245-248.)



The ***terminals 22B*** disclose another bump portion. (EX1002, ¶193-194.)

Imaoka teaches that the inclined terminals address potential misalignment if either substrate expands or shrinks. "When the member (substrate 14 or 26) that supports the terminals 16 or 26 of the first group or the second group expands or

contracts, ***the terminals 16 or 26 move along the first lines L_1 or the second lines L_2. . . the electrical connection between the terminals 16 and 26 of the first and second groups are secured***." (EX1006, 11:63-12:11.)

e. 1[d]: "wherein: the pad portion comprises a first sub-pad unit comprising an inclined first pad and a second sub-pad unit comprising an inclined second pad;"

FIG. 5 discloses this limitation. (EX1002, ¶195; *see also* EX1005, 7:28-8:12.)

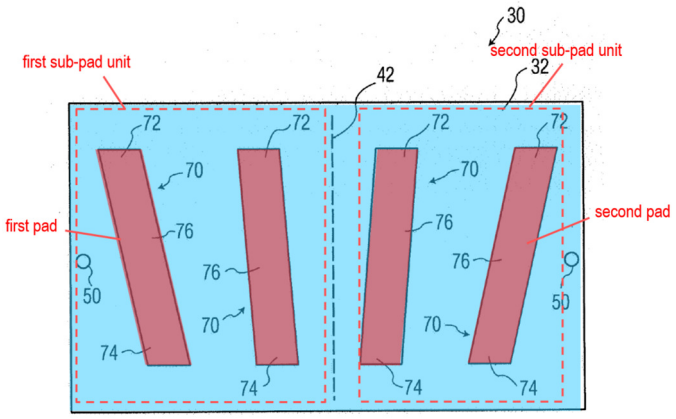


FIG. 5

FIG. 6 discloses this limitation. In FIG. 6, one or more of the inclined pads to the left of the line 42 disclose a "first sub-pad unit comprising an inclined first pad." One or more of the inclined pads to the right of the line 42 can be mapped a "second sub-pad unit comprising an inclined second pad." (EX1002, ¶196; *see also* EX1005, 8:13-9:7.)

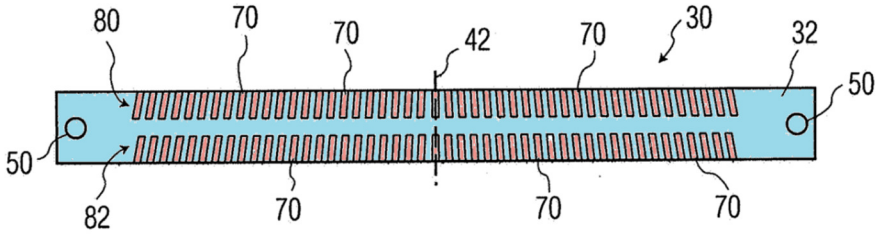


FIG. 6

FIG. 7 discloses this limitation. (EX1002, ¶197; *see also* EX1005, 9:9-27.)

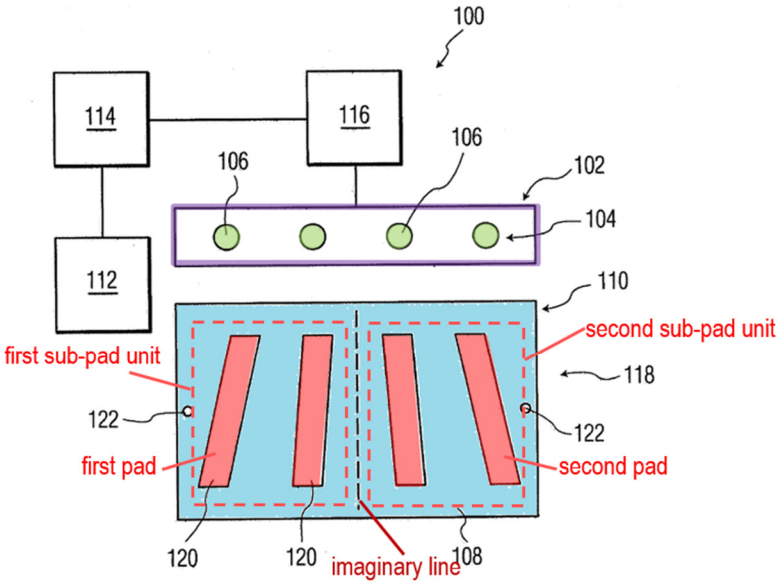
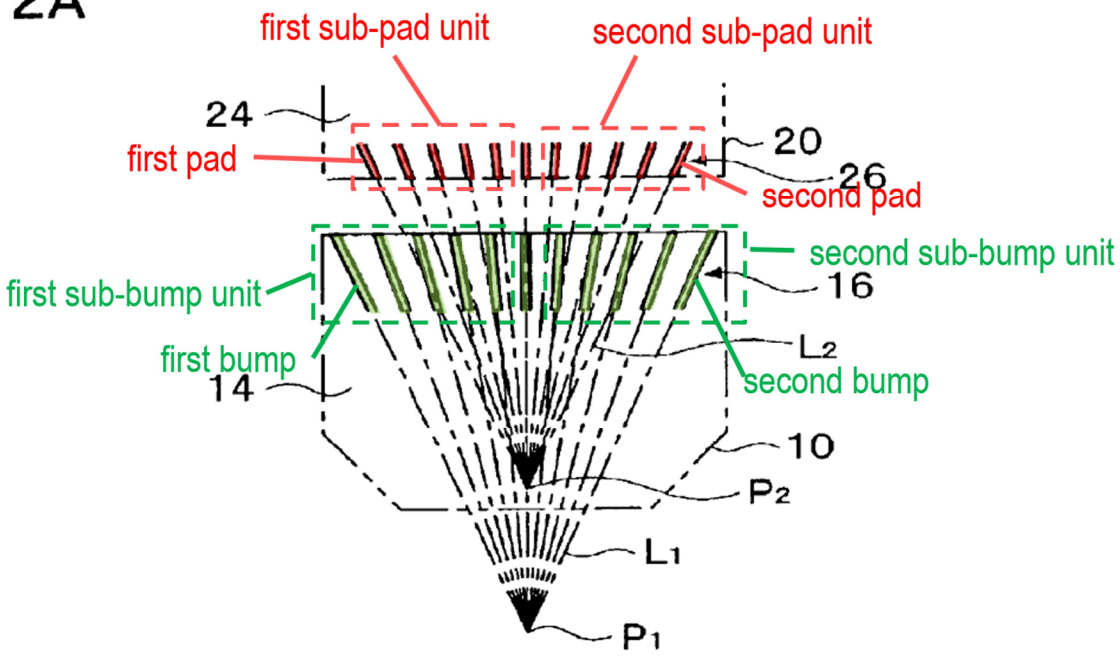


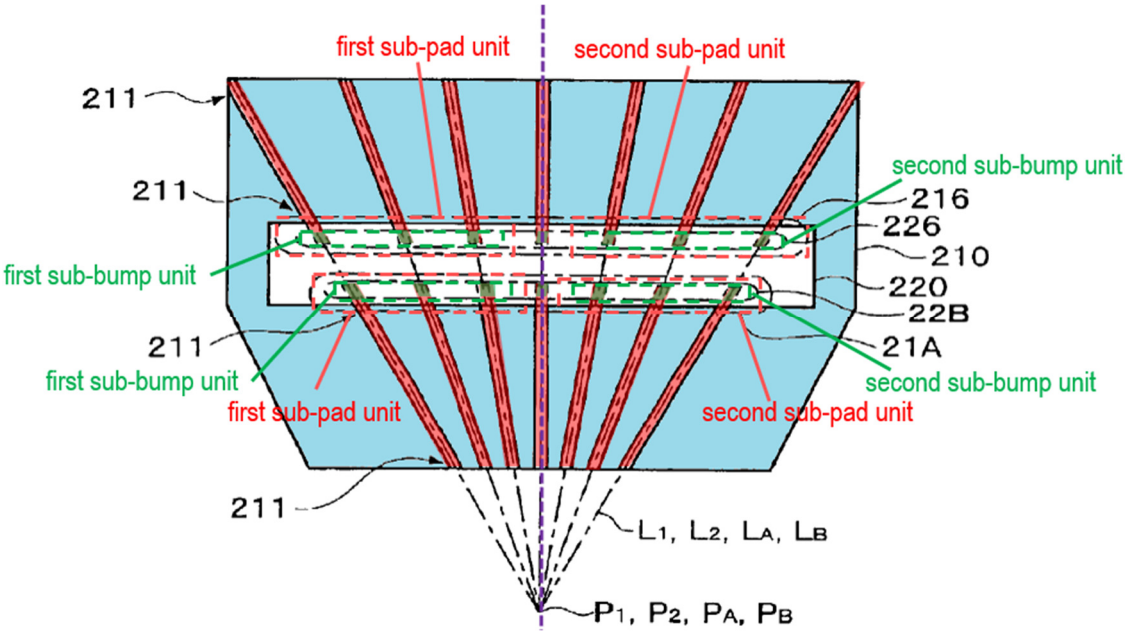
FIG. 7

Imaoka also discloses this limitation. In FIG. 2A, all of the ***terminals 26*** other than the one terminal in the middle are inclined. (EX1002, ¶¶198-199; *see also* EX1006, 10:63-12:11.)

FIG. 2A



In FIG. 11, in the top half of the electronic device, the ***terminals 216*** (i.e., the "pad portion") comprises three inclined pads on the left (i.e., "first sub-pad unit") and three inclined pads on the right (i.e., "second sub-pad unit"). Additionally or alternatively, the ***terminals 21A*** also disclose this limitation. (EX1002, ¶200.)



f. 1[e]: "the first pad and the second pad are inclined in different directions symmetrically about an imaginary line that divides the pad portion; and;"

In Lieshout, FIG. 5 and FIG. 6 each depicts a ***reference line 42***. (EX1002, ¶201; *see also* EX1005, 7:28-9:7.) As shown by the exemplary annotations below in FIG. 5, a first pad and a second pad are inclined in different directions symmetrically about the reference line 42 that divides the pad portion.

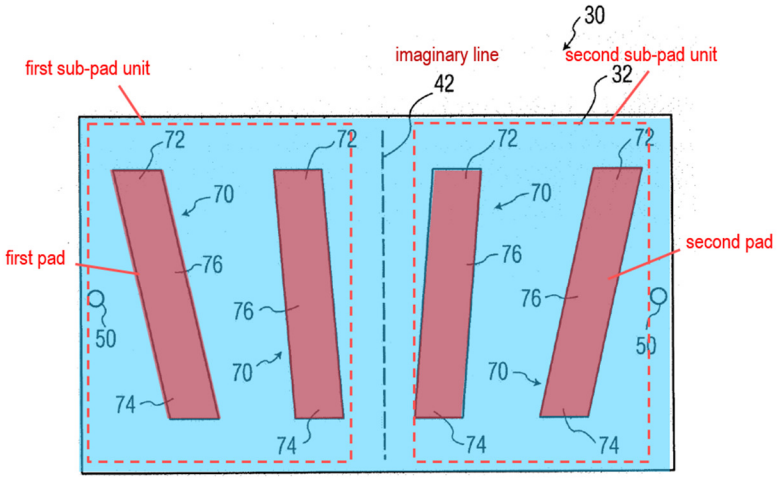


FIG. 5

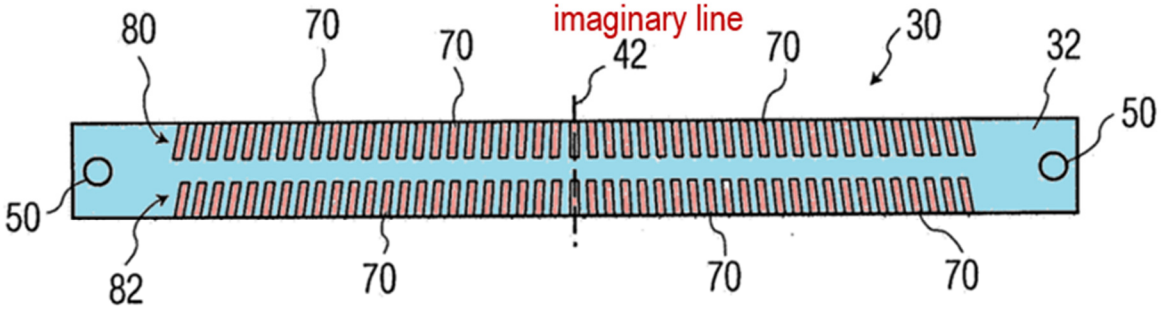


FIG. 6

FIG. 7 depicts a similar reference line. (EX1002, ¶202; *see also* EX1005, 9:9-27.)

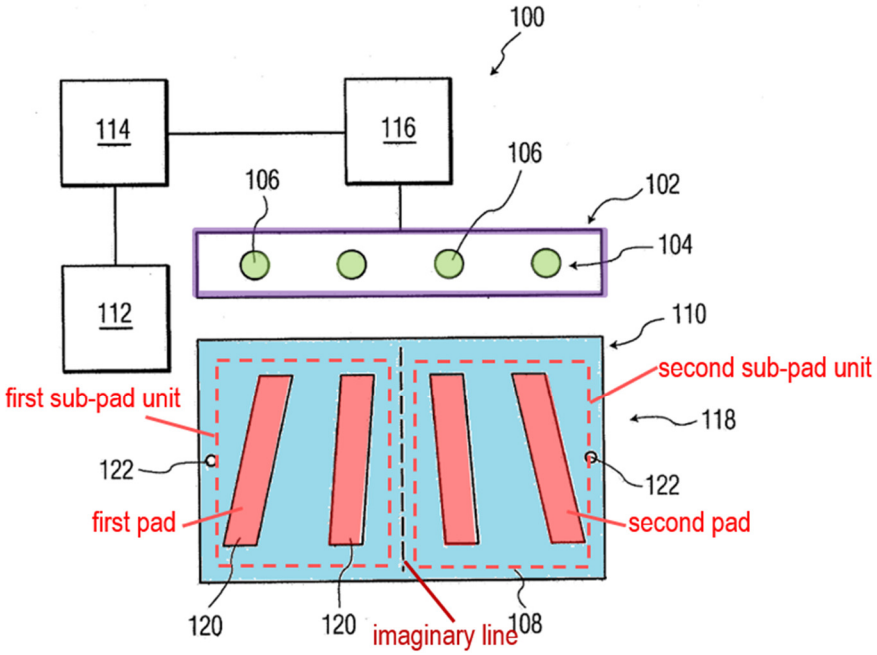
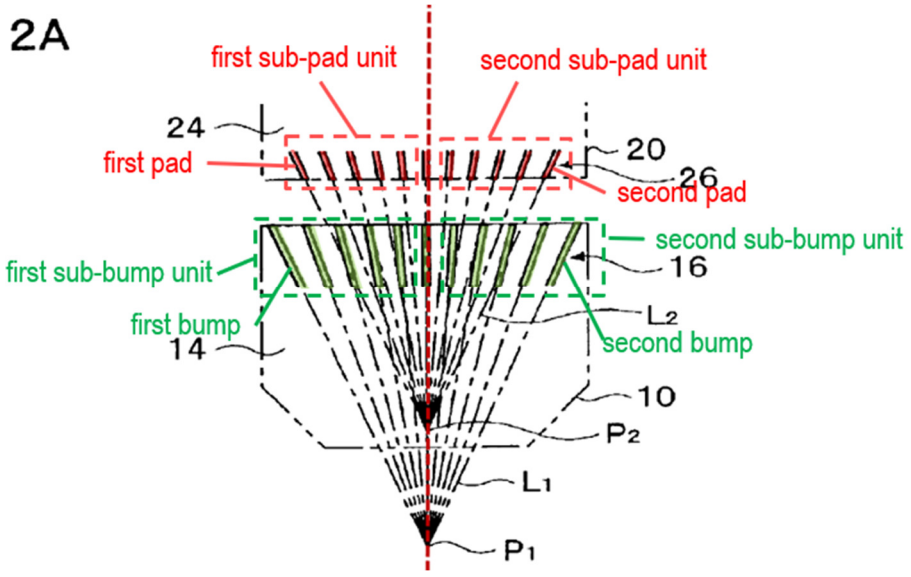


FIG. 7

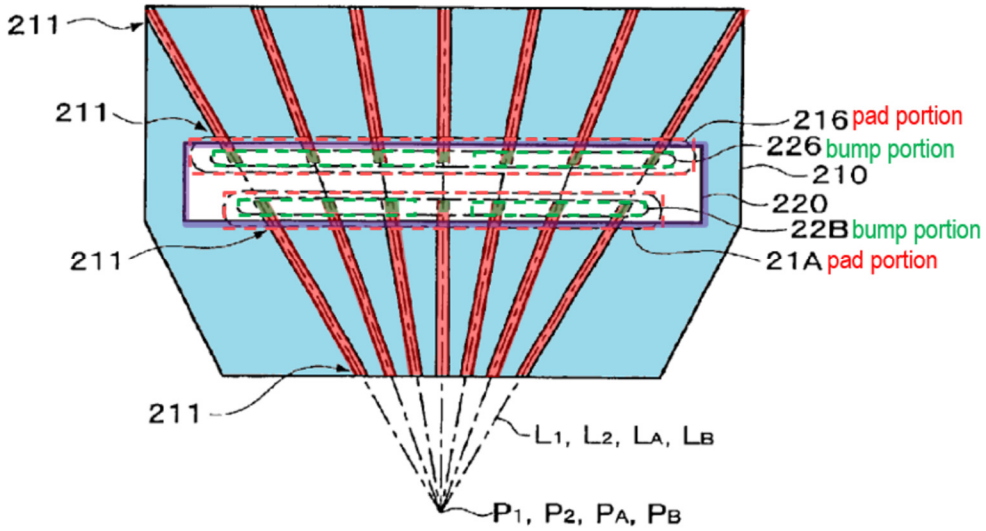
Imaoka discloses an imaginary line that divides the pad portion. For example, Imaoka states, "right and left portions of the plural terminals 16 of the first group are ***symmetrically arranged***" and that there is "an ***imaginary line***". (*See* EX1006, 12:13-21; EX1002, ¶203.)

In FIG. 2A, the ***terminals 26*** are symmetrical about a ***central vertical line***. An exemplary first pad and an exemplary second pad are inclined in different directions symmetrically about the ***central vertical line***. (EX1002, ¶204; *see also* EX1006, 10:63-12:11.)

FIG. 2A



Similarly, as shown in FIG. 11, the electronic device is symmetrical about a ***central vertical line***. The first pad (e.g., the leftmost terminal of ***terminals 226***) and the second pad (e.g., the rightmost terminal of ***terminals 226***) are inclined in different directions symmetrically about the ***central vertical line*** that divides the ***terminals 226***. (EX1002, ¶205; *see also* EX1006, 17:60-18:59.)

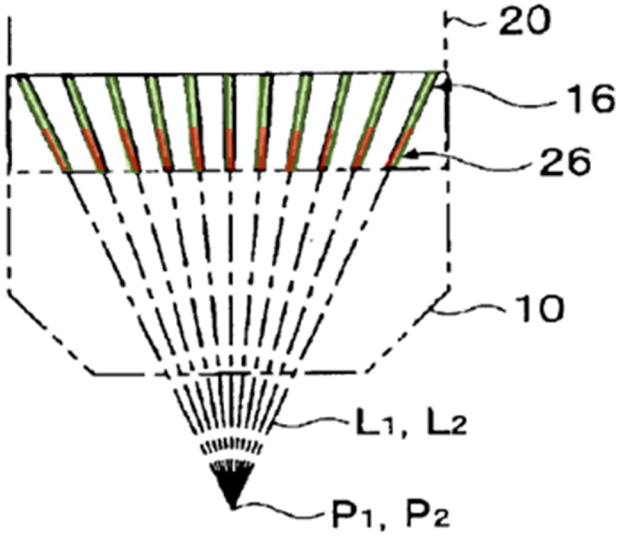


g. 1[f]: "the pad portion is electrically connected with the bump portion;"

Lieshout states that "[t]he ***connection IC bumps*** on the IC chip and ***bond pads*** on the substrate have to be accurately matched to provide good ***electrical connections***." (EX1005, 1:16-18.)

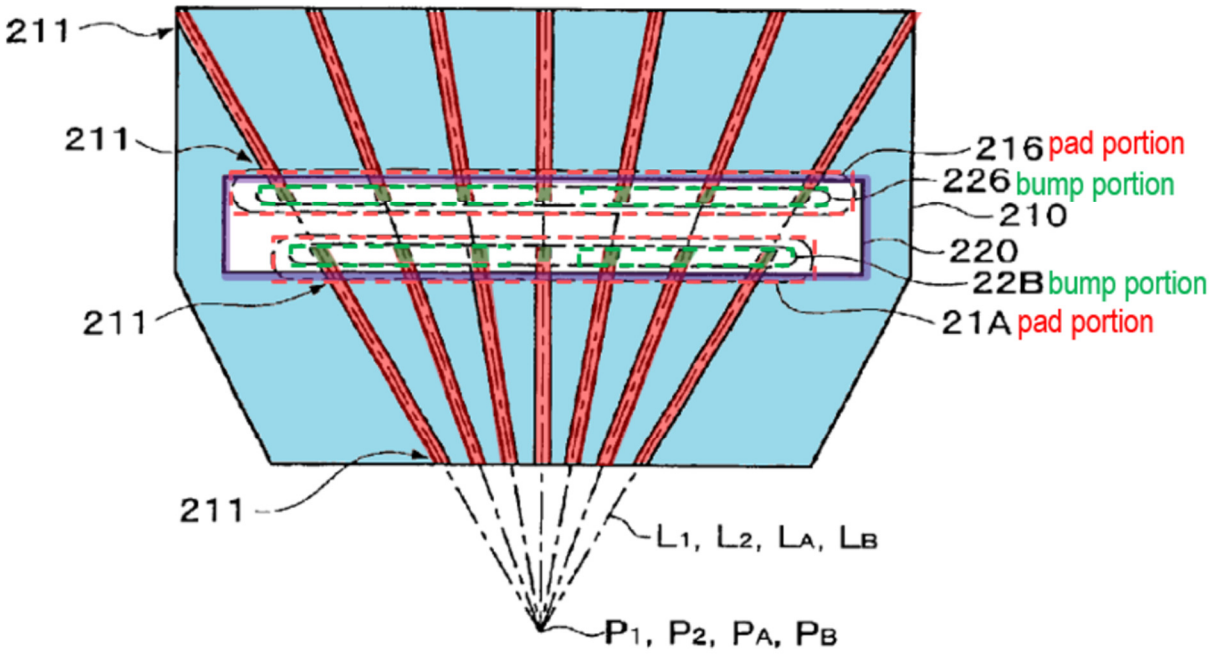
In Imaoka, "FIG. 2B is a drawing showing the terminals of the first and second groups after they are ***electrically connected*** to one another." (EX1006, 10:65-11:2.) The ***terminals 26*** and the ***terminals 16*** are aligned in the same manner as the '503 patent. "In this manner, ***even when the substrate 16 expands, the terminals 16 and 26 of the first and second groups can be electrically connected one another***." (EX1006, 11:48-50.)

FIG. 2B



Imaoka discloses that the details of FIGs. 2A-B can be applied to the terminals in FIG. 11. (*See* EX1006, 18:9-12, 18:15-20.) "Positions of

the terminals 21A and 22B of the A-group and B-group are overlapped by making the A-lines L_A and B-lines L_B overlap." (EX1006, 19:3-5.) (EX1002, ¶¶206-211.)



h. 1[g]: "the bump portion comprises a first sub-bump unit comprising an inclined first bump and a second sub-bump unit comprising an inclined second bump;"

Lieshout discloses that bumps of an integrated circuit are disposed on the bond pads in FIG. 6, although they are not depicted. "Those skilled in the art will appreciate that any number of ***bond pad sets*** can be used as desired for a particular application, as required to ***match connection bump sets on a connection bump device***." (EX1005, 8:19-22.) Lieshout also discloses that "[t]he pattern and spacing of bond pad locations on the photo masks used during TFT processing are ***the same as the pattern and spacing of connection IC bumps*** on the IC chips, so

the structures on the substrate on the rigid support have the same pattern and spacing as on the photo masks." (EX1005, 1:24-28.) Thus, a POSITA would understand that the bump portion meets the limitation. (EX1002, ¶¶212-213.)

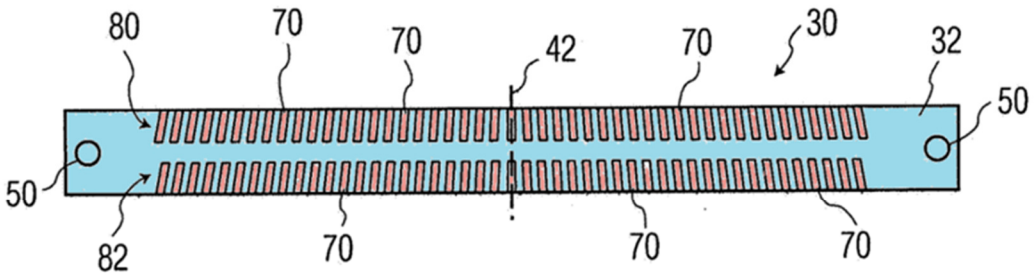
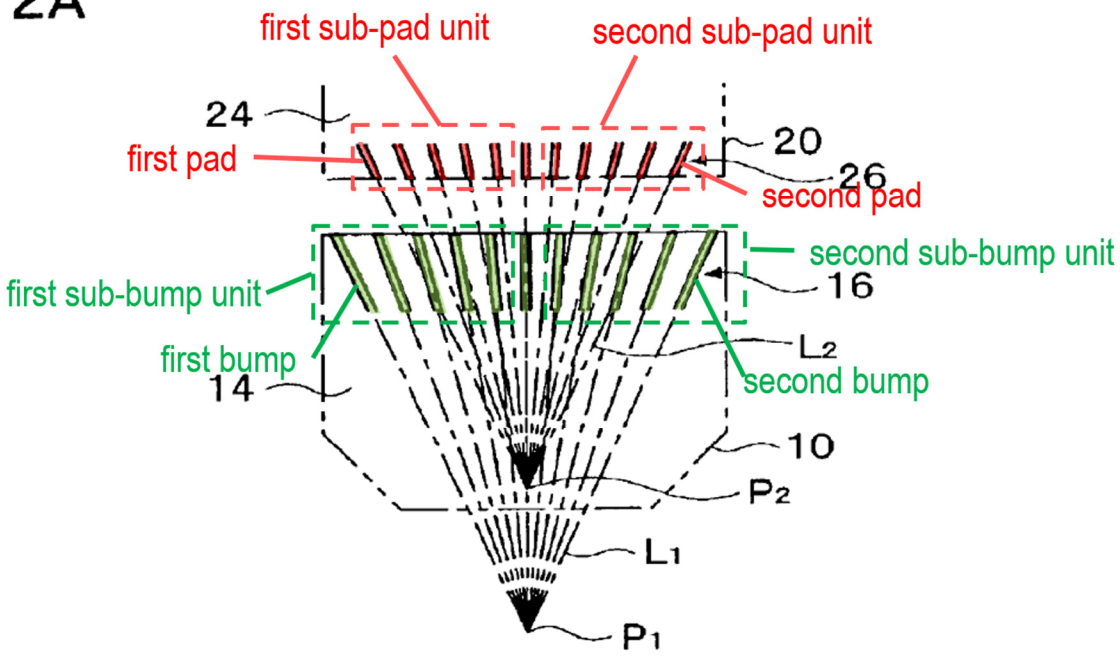


FIG. 6

In Imaoka, the ***terminals 16*** other than the one terminal in the middle are inclined. The terminals 16 in FIGs. 2A-B of Imaoka, which are for providing electrical connection to an array substrate, are analogous to the IC bumps of Lieshout bonded to pads, which have the same purpose. (EX1002, ¶246.)

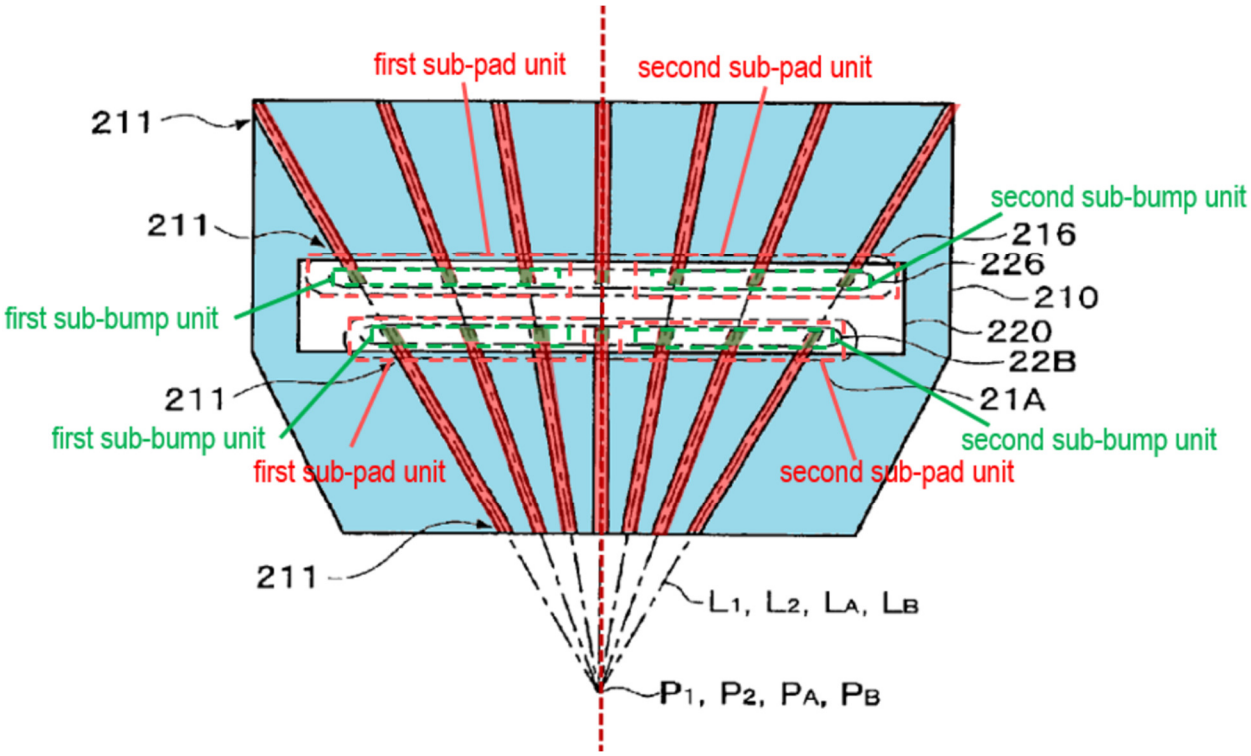
FIG. 2A



In FIG. 2A, the ***terminals 16*** include five inclined bumps on the left, one or more of which can be mapped a "first sub-bump unit." The ***terminals 16*** include five inclined bumps on the right, one or more of which can be mapped a "second sub-bump unit." (EX1002, ¶¶214-215; *see also* EX1006, 10:63-12:11.) As discussed above, the purpose of FIGs. 2A-B is to provide driving signals to an LCD display via aligned electrical connections. (*See* EX1006, 10:21-26.)

In FIG. 11, in the top half of the electronic device, the ***terminals 226*** (i.e., the "bump portion") comprises three inclined bumps on the left (i.e., "first sub-bump unit") and three inclined bumps on the right (i.e., "second sub-bump unit"). Additionally or alternatively, in the bottom half of the electronic device, the ***terminals 22B*** (i.e., the "bump portion") comprises three inclined bumps on the

left (i.e., "first sub-bump unit") and three inclined bumps on the right (i.e., "second sub-bump unit"). (EX1002, ¶¶216-217; *see also* EX1006, 17:60-18:59.) Imaoka teaches that the details of electrical connection shown in FIGs. 2A-B for preventing misalignment can be applied to the connection between the ***terminals 216*** and the ***terminals 226*** in FIG. 11. (*See* EX1006, 18:9-12, 18:17-20, 18:40-43, 18:56-59, 9:46-48.) Like FIGs. 2A-B, the bump portions in FIG. 11 are shown to include inclined parallelogram bumps and the pad portions in FIG. 11 are shown to include inclined parallelogram pads.



i. 1[h]: "the first bump and the second bump are inclined in different directions symmetrically about the imaginary line that divides the pad portion."

Lieshout discloses that "[t]he pattern and spacing of bond pad locations on the photo masks used during TFT processing are ***the same as the pattern and spacing of connection IC bumps*** on the IC chips . . . ." (EX1005, 1:24-27.) Thus, it would have been obvious to a POSITA that Lieshout's connection bumps are similarly arranged as the pads, thus disclosing this limitation. (EX1002, ¶218.)

In Imaoka, in FIG. 2A, the ***terminals 16*** are symmetrical about a ***central vertical line***. As shown below, an exemplary first pad and an exemplary second pad are inclined in different directions symmetrically about the ***central vertical line.*** (EX1002, ¶¶219-220; *see also* EX1006, 10:63-12:11.)

FIG. 2A

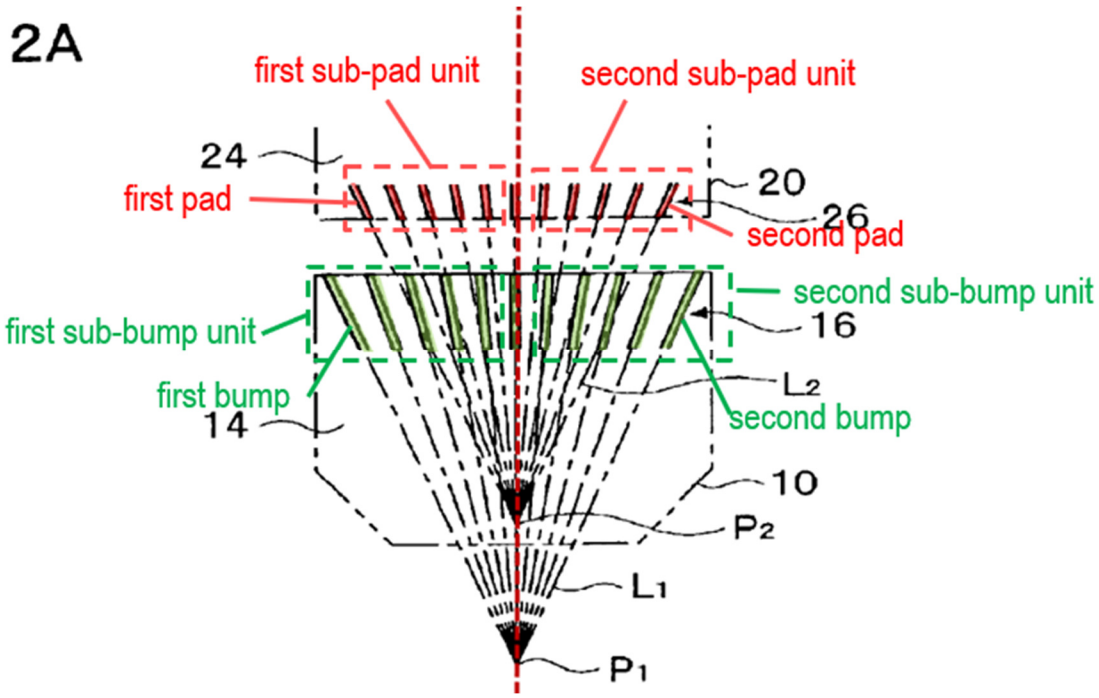
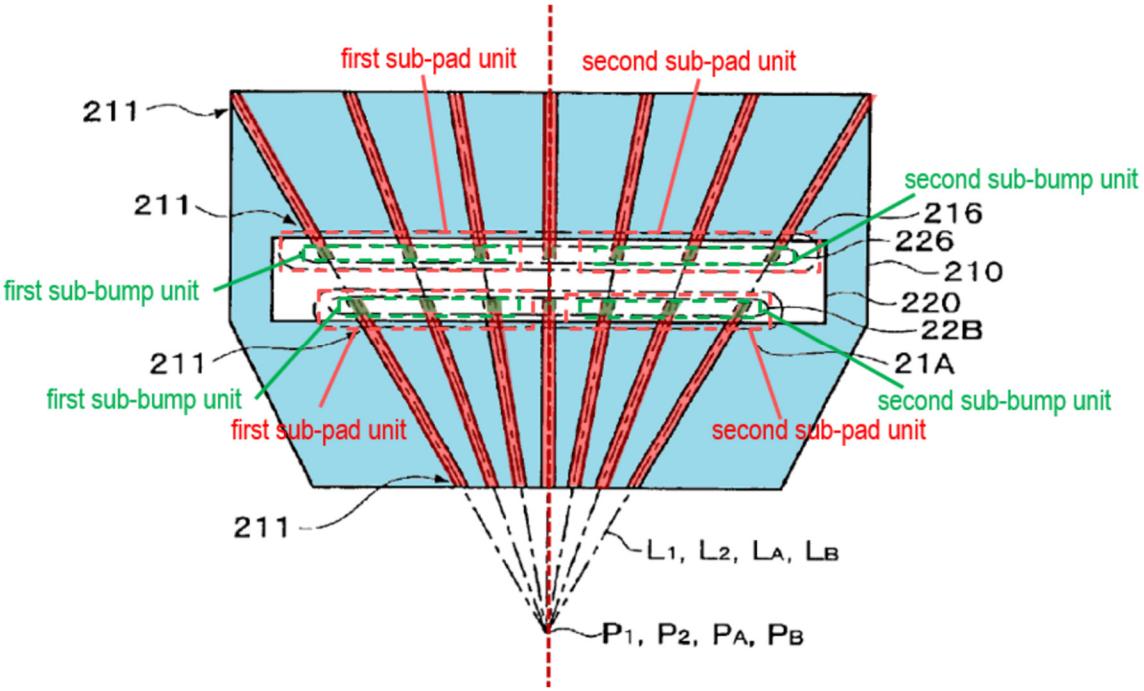


FIG. 11 also discloses this limitation. In FIG. 11, the electronic device is symmetrical about a ***central vertical line***. The first bump (e.g., the leftmost terminal of ***terminals 226***) and the second bump (e.g., the rightmost terminal of ***terminals 226***) are inclined in different directions symmetrically about the ***central vertical line*** that divides the ***terminals 226***. (EX1002, ¶221; *see also* EX1006, 17:60-18:59; *supra V.C.3.h.*)



4. Claim 2: "The electronic device of claim 1, wherein at least one of the first pad and the second pad has a parallelogram shape."

In Lieshout, each bond pad in FIGs. 5, 6, and 7 has a parallelogram shape. (EX1002, ¶222; *see also* EX1005, 7:28-8:12, 8:13-9:7, 9:9-27.) In Imaoka, in each of FIGs. 1, 2A-B and 11, each terminal has a parallelogram shape. (EX1002, ¶222; *see also* EX1006, 10:63-12:11.)

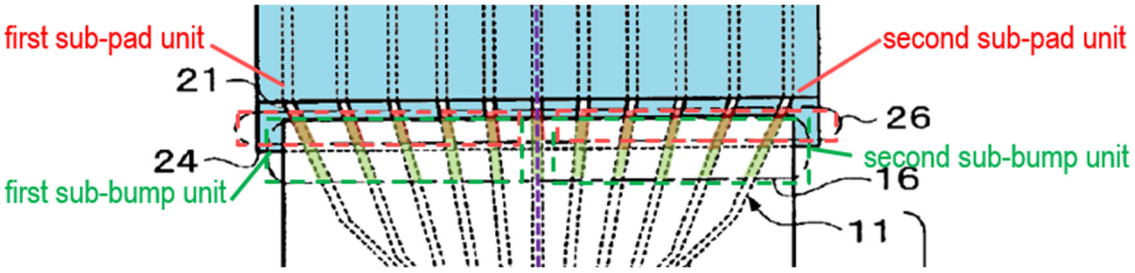
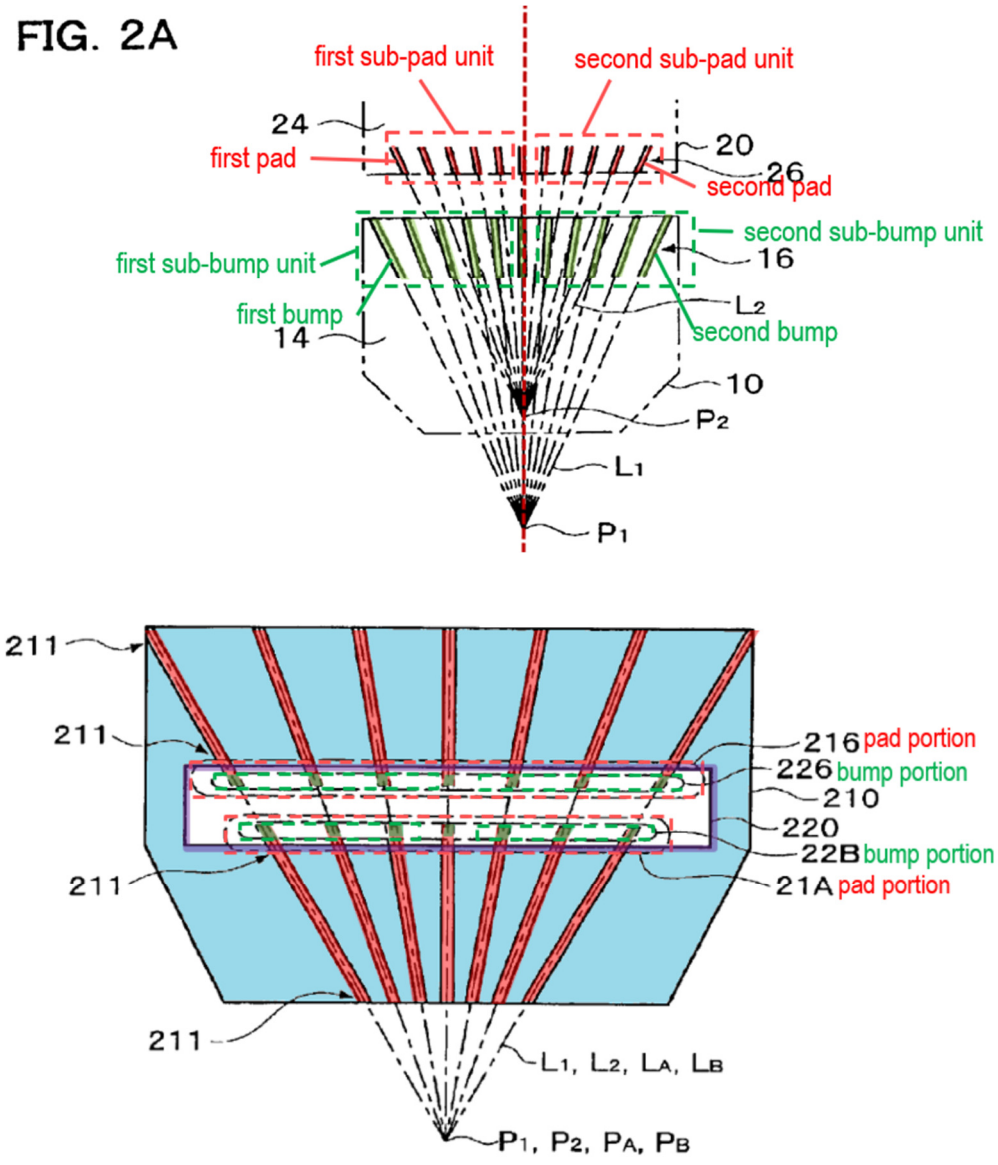


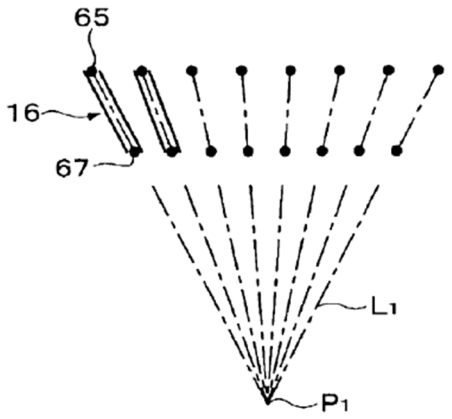
FIG. 1 (EX1006)

FIG. 2A



Further, in Imaoka, FIG. 7B discloses how the ***terminals 16*** of the first embodiment (i.e., FIGs. 1 and 2A-B) are designed. (EX1006, 14:29-56.) Each terminal has a parallelogram shape. (EX1002, ¶223.) Imaoka also states that "[s]imilarly, the ***terminals 26*** of the second group are designed." (EX1006, 14:1-2.)

FIG. 7B



5. Claim 3: "The electronic device of claim 1, wherein: the first bump has a same inclination angle as the first pad; and the second bump has a same inclination angle as the second pad."

In FIG. 2A of Imaoka, an exemplary first bump has a same inclination angle as an exemplary first pad and an exemplary second bump has a same inclination angle as an exemplary second pad. (EX1002, ¶224; *see also* EX1006, 10:63-12:11.)

FIG. 2A

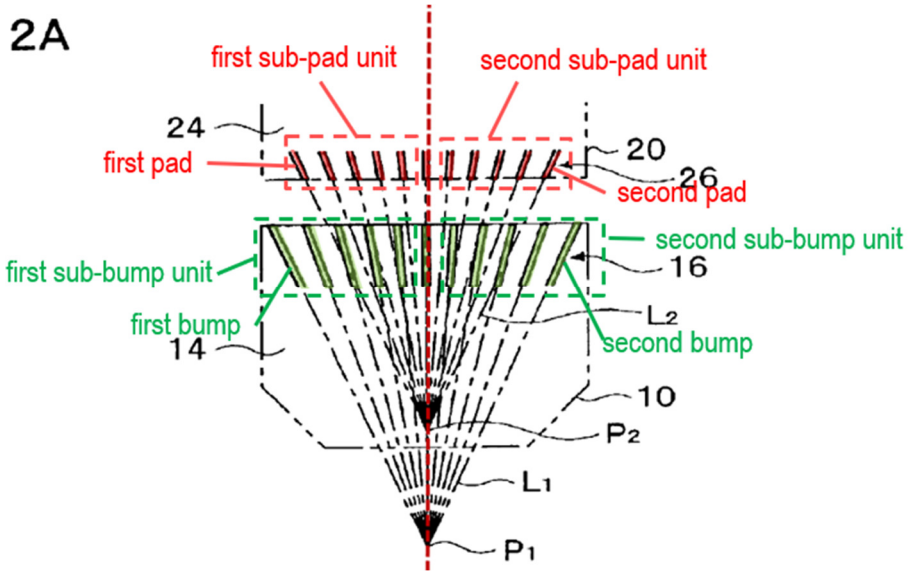
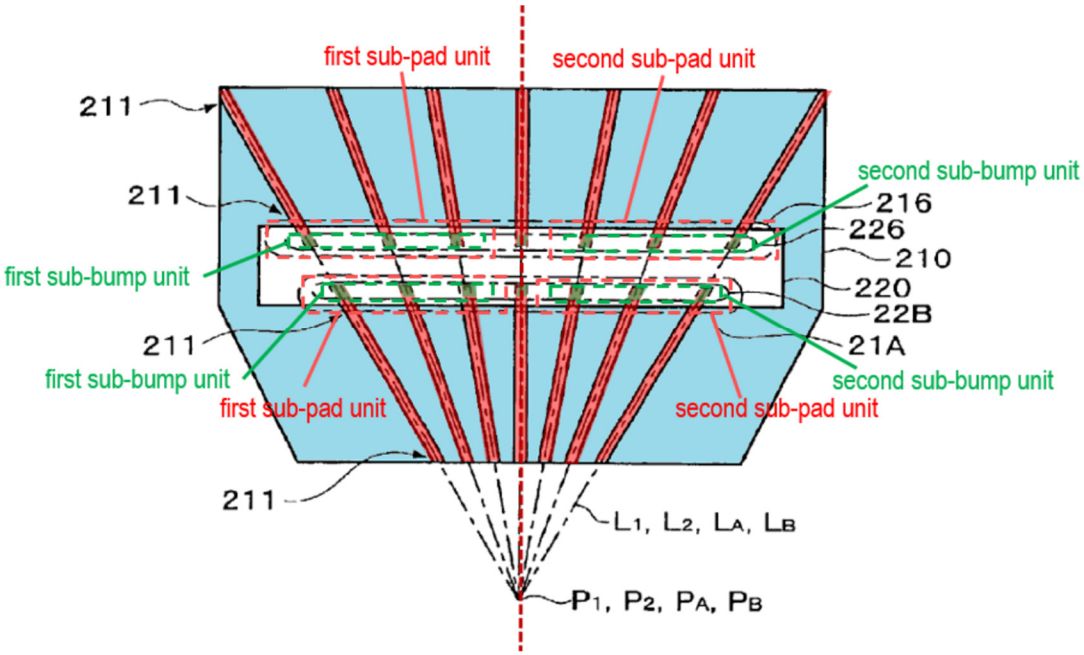


FIG. 11 also discloses this limitation. (EX1002, ¶¶225-226; *see also* EX1006, 17:60-18:59.)

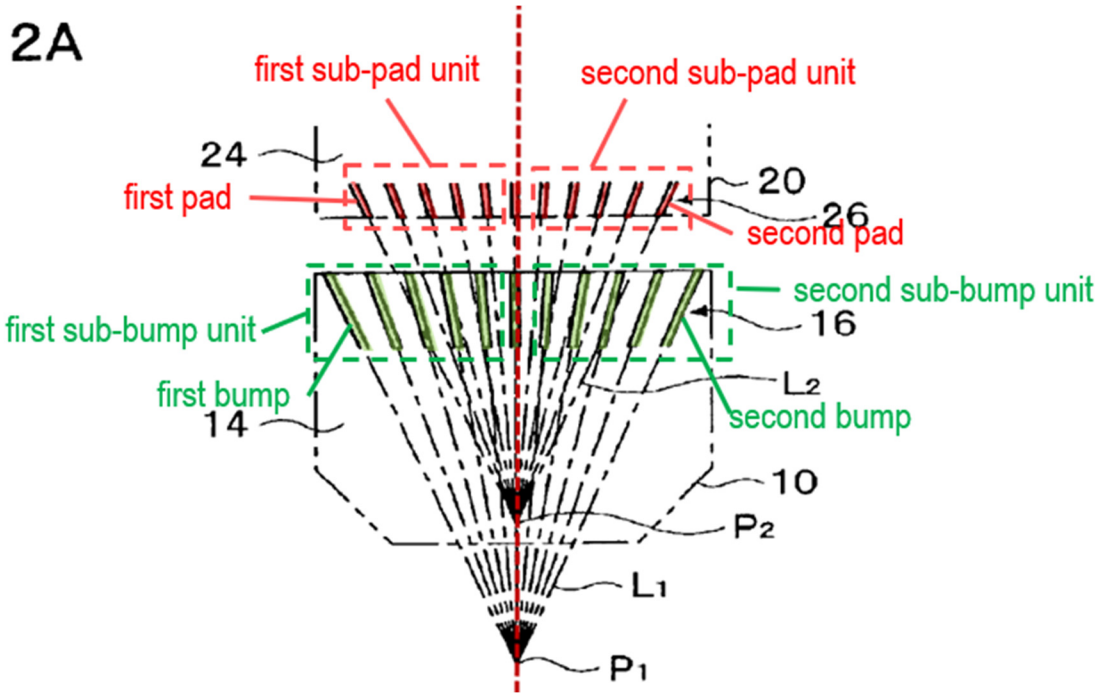


6. Claim 4: "The electronic device of claim 1, wherein a shape of the first bump corresponds to a shape of the first pad, and a shape of the second bump corresponds to a shape of the second pad."

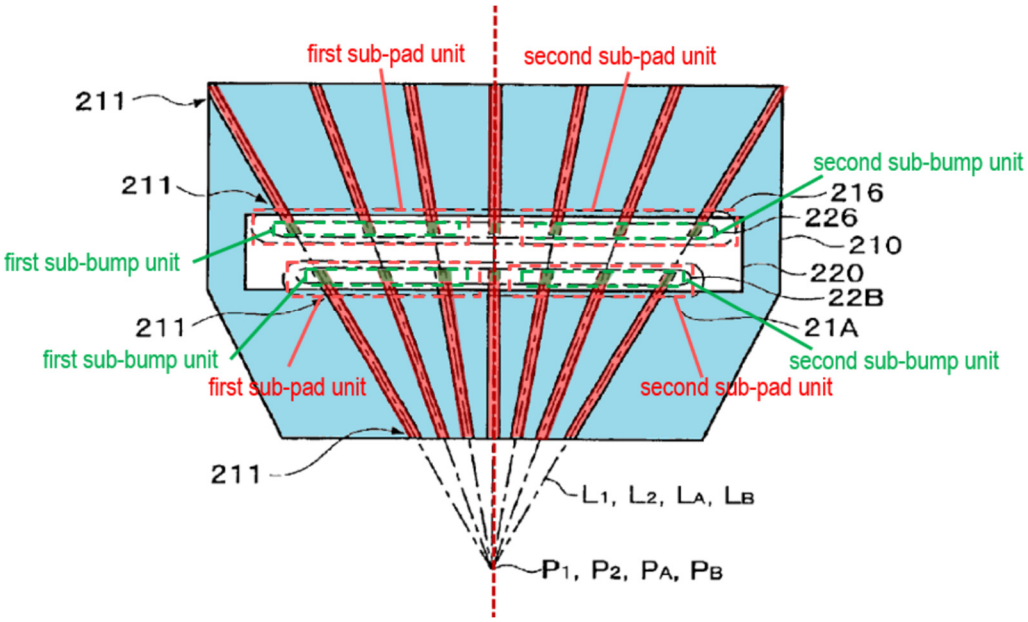
Lieshout discloses that "[t]he pattern and spacing of bond pad locations on the photo masks used during TFT processing are ***the same as the pattern and spacing of connection IC bumps*** on the IC chips. . . ." (EX1005, 1:24-27.) Thus, it would have been obvious to a POSITA that the shape of a bump on the integrated circuit would correspond to a shape of a corresponding bond pad. (EX1002, ¶227.)

In Imaoka, as shown in FIGs. 2A-B, the first exemplary bump and the first exemplary pad have the same shape. Similarly, the second exemplary bump and the second exemplary pad have the same shape. (EX1002, ¶228; *see also* EX1006, 10:63-12:11.)

FIG. 2A



The embodiment in FIG. 11 also discloses this limitation. As shown below, any bump and the corresponding pad have the same shape. (EX1002, ¶229; *see also* EX1006, 17:60-18:59.)



7. Claim 5: "The electronic device of claim 1, wherein the first pad is electrically connected with the first bump and the second pad is electrically connected with the second bump."

Lieshout states that "[t]he ***connection IC bumps*** on the IC chip and ***bond pads*** on the substrate have to be accurately matched to provide good ***electrical connections***." (EX1005, 1:16-18.) A POSITA would have understood that the bond pads in each of the examples in FIGs. 5, 6, and 7 are electrically connected with corresponding IC bumps of an integrated circuit. (*See, e.g.,* EX1005, 10:30-11:2; EX1002, ¶230-231.)

In FIGs. 2A-B of Imaoka, the first exemplary pad is electrically connected with the first exemplary bump and the second exemplary pad is electrically connected with the second exemplary bump. (EX1002, ¶232; *see also* EX1006, 10:63-12:11.)

FIG. 2A

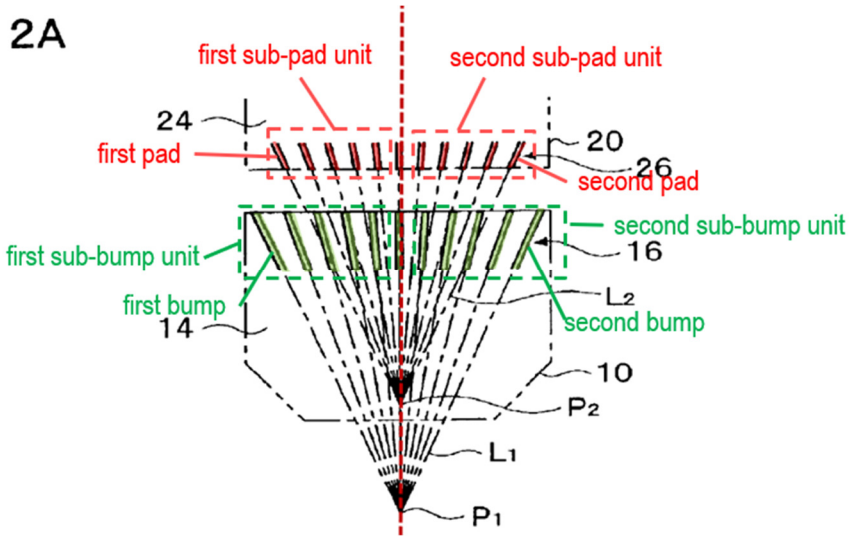
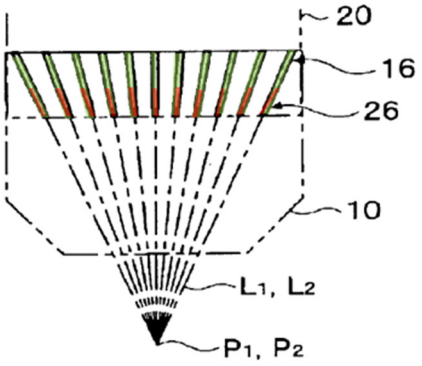
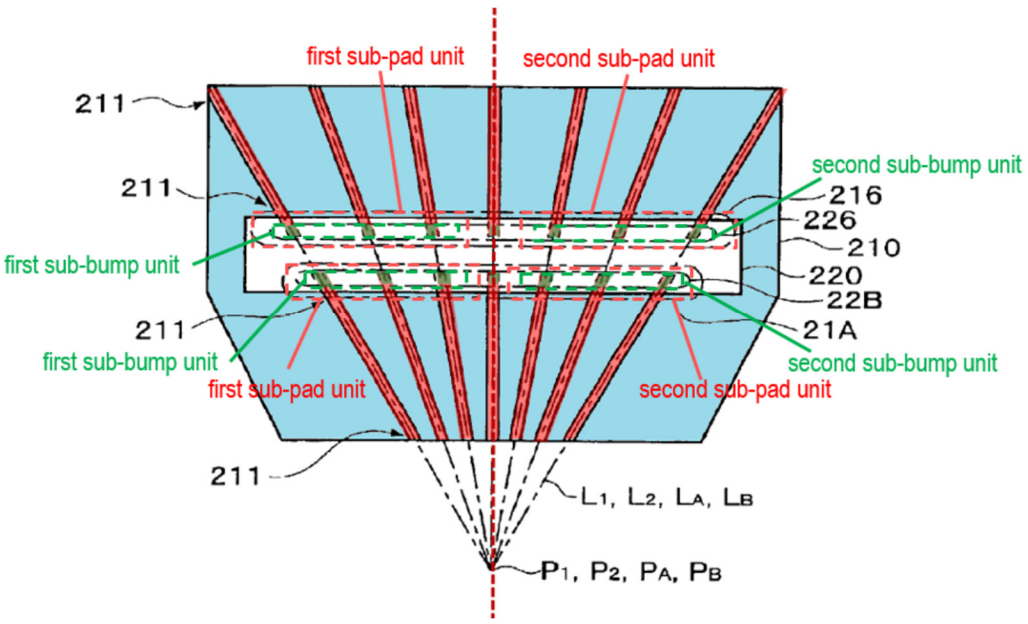


FIG. 2B

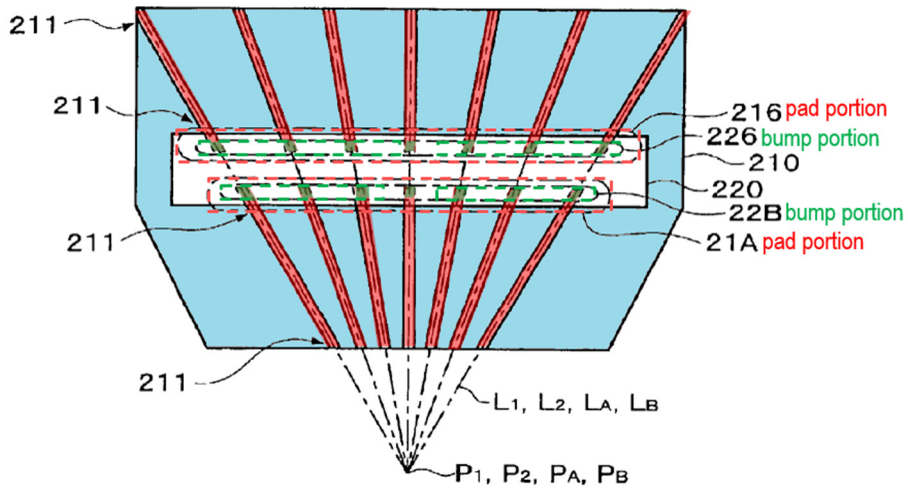


The embodiment in FIG. 11 also shows that each pad is electrically connected with a corresponding bump. (EX1002, ¶233; *see also* EX1006, 17:60-18:59.)



8. Claim 6: "The electronic device of claim 1, wherein an area of the first pad is greater than an area of the first bump."

For example, FIG. 11 of Imaoka shows that each ***pad*** (e.g., 216) is greater in area than the corresponding ***bump*** (e.g., 226). (*See* EX1006, 17:60-18:59; EX1002, ¶¶234-235.)



9. Claim 7: "The electronic device of claim 1, wherein: the first bump comprises a first region and a second region; and the first region overlaps the first pad and the second region does not overlap the first pad."

In FIGs. 2A-B of Imaoka, each bump has a region that overlaps the corresponding pad and another region that does not overlap the corresponding pad. (EX1002, ¶236.) It would also be obvious to a POSITA that any embodiment of Imaoka, including FIG. 11, can be designed such that each bump partially overlaps with the corresponding pad in this manner as shown in FIGs. 1 and 2A-B. (*Id.*)

FIG. 2A

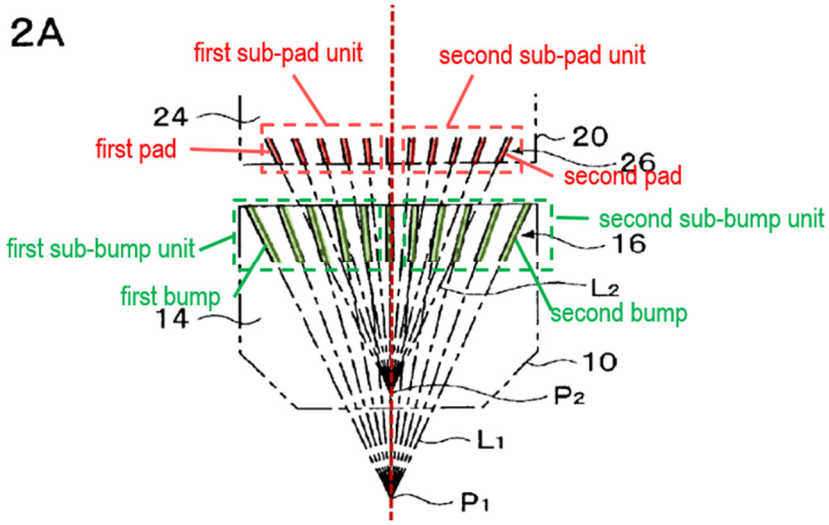
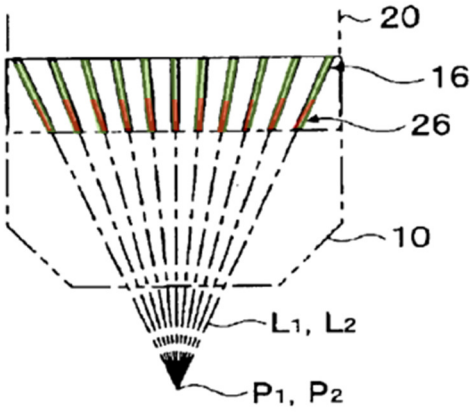


FIG. 2B



10. Claim 8: "The electronic device of claim 1, wherein at least one of the first pad and the second pad has a quadrangle shape."

In Lieshout, each bond pad in FIGs. 5, 6, and 7 has a quadrangle shape. Imaoka also teaches this limitation in FIGs. 2A-B. (EX1002, ¶237; *see also* EX1005, 7:28-8:12, 8:13-9:7, 9:9-27; EX1006, 10:63-12:11.)

11. Claim 9: "The electronic device of claim 2, wherein the pad portion further comprises a third sub-pad unit comprising a third pad having a rectangular shape and disposed between the first sub-pad unit and the second sub-pad unit."

In FIG. 6 of Lieshout, the continuous bond pads 70 comprise two rectangular bond pads at the center between the first sub-pad unit and the second sub-pad unit. (EX1002, ¶238; *see also* EX1005, 8:13-9:7.)

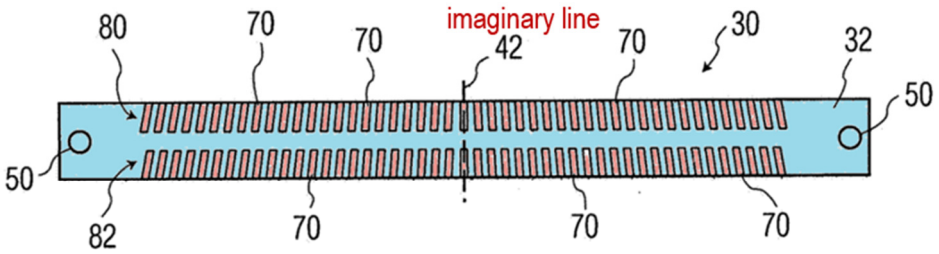


FIG. 6

FIGs. 2A-B of Imaoka disclose this limitation. The ***terminals 26*** comprises a rectangular terminal in the middle disposed between the first sub-pad unit and the second sub-pad unit. (EX1002, ¶239; *see also* EX1006, 10:63-12:11.)

FIG. 2A

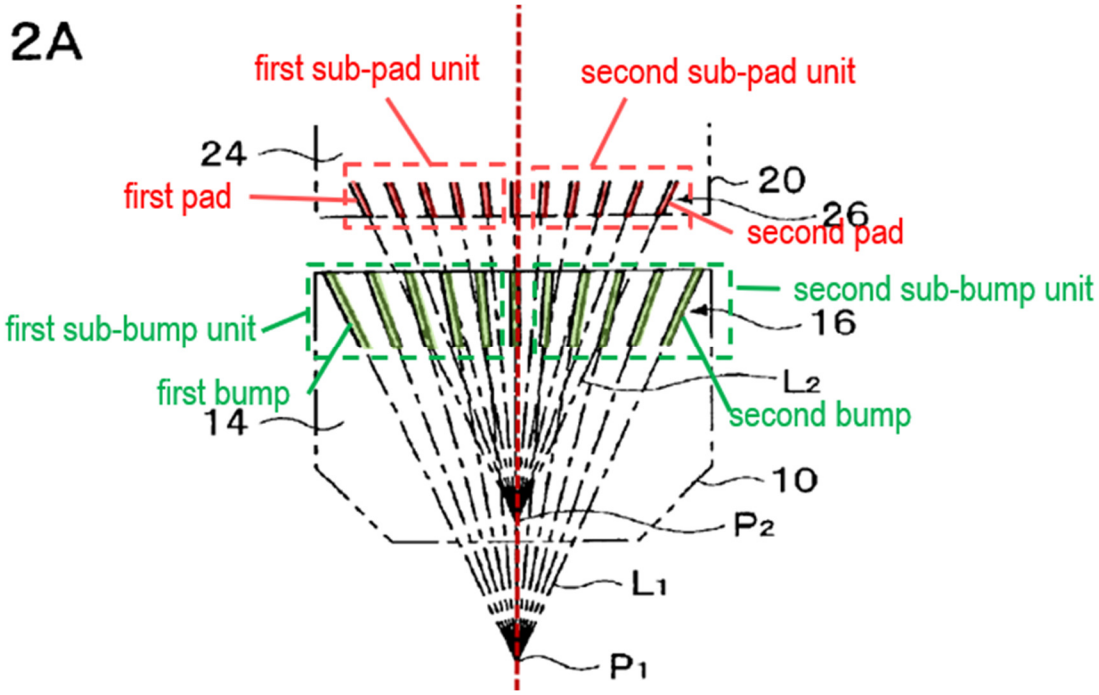


FIG. 2B

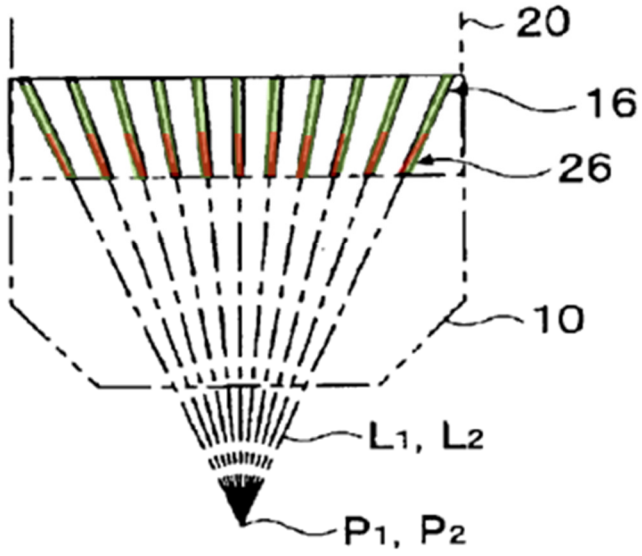
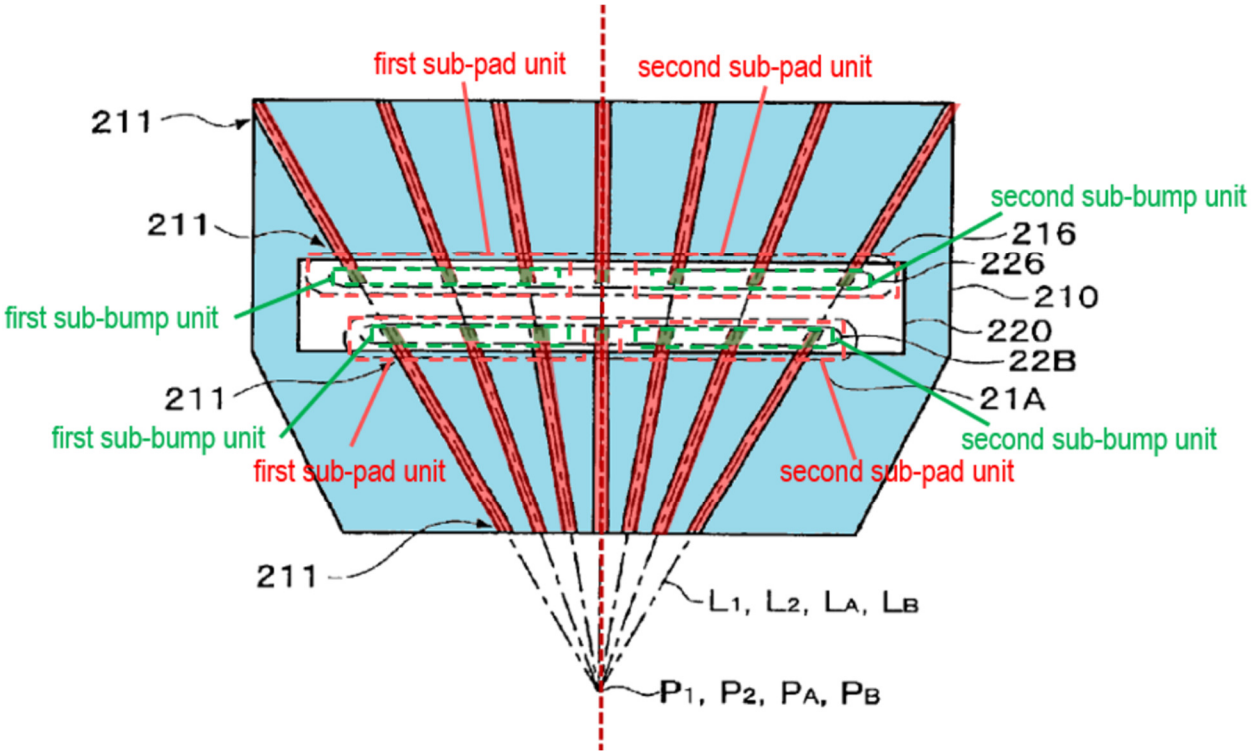


FIG. 11 also discloses this limitation. As shown below, ***terminals 216*** comprise a rectangular terminal in the middle disposed between the first sub-pad unit and the second sub-pad unit. So do ***terminals 21A***. (EX1002, ¶¶240-241; *see also* EX1006, 17:60-18:59.)



12. Claim 10: "The electronic device of claim 9, wherein the bump portion further comprises a third sub-bump unit comprising a third bump having a rectangular shape and disposed between the first sub-bump unit and the second sub-bump unit."

Lieshout discloses that "[t]he pattern and spacing of bond pad locations on the photo masks used during TFT processing are ***the same as the pattern and spacing of connection IC bumps*** on the IC chips . . . ." (EX1005, 1:24-27.) Thus, it would have been obvious to a POSITA that, like the pad portion, Lieshout's bump portion would comprise rectangular bumps disposed between the first sub-bump unit and the second sub-bump unit, similar to the pad portion. (EX1002, ¶242.) At the time of the invention, it was common knowledge that an integrated circuit provides elongated bumps for electrical connection. (*Supra* V.A.2.d.) It

was also common knowledge that the shape of these bumps need to correspond to the respective pads. (*Id.*)

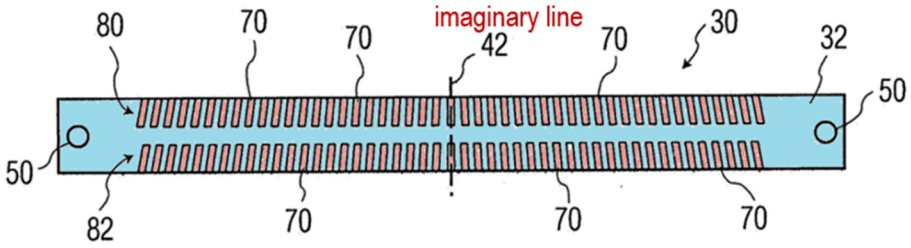


FIG. 6

In Imaoka, as shown in FIGs. 2A-B, the ***terminals 16*** comprises a rectangular terminal in the middle disposed between the first sub-bump unit and the second sub- ump unit. (EX1002, ¶243; *see also* EX1006, 17:60-18:59.)

FIG. 2A

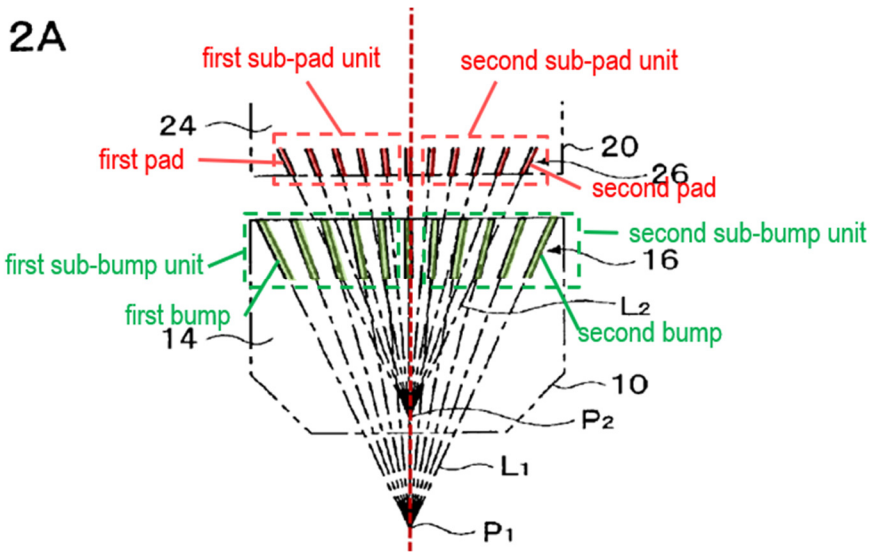


FIG. 2B

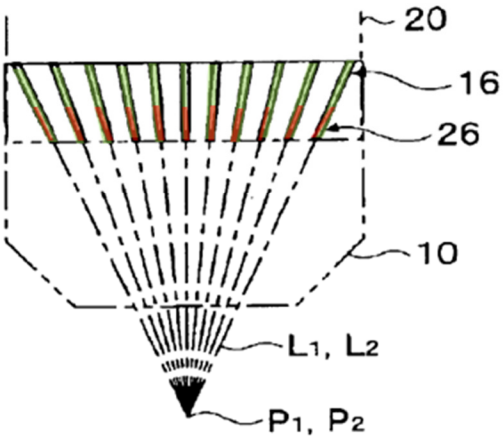
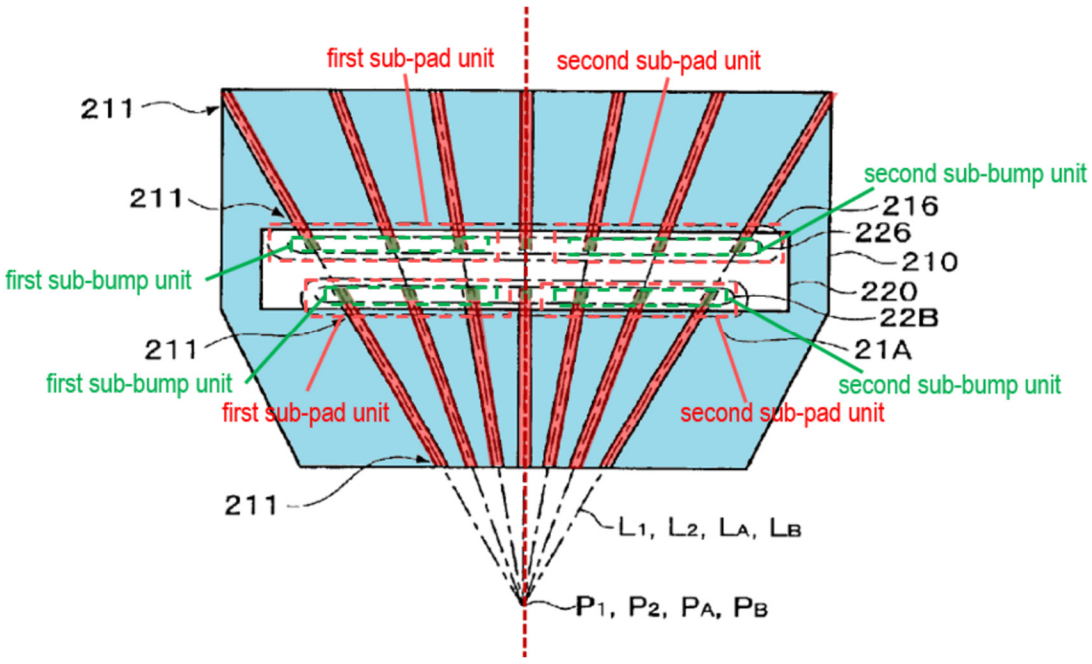


FIG. 11 also discloses this limitation. The ***terminals 226*** comprise a rectangular terminal in the middle between the first sub- bump unit and the second sub-bump unit. So do the ***terminals 22B***. (EX1002, ¶244; *see also* EX1006, 17:60-18:59.)



13. A POSITA would have been motivated to combine Lieshout and Imaoka.

It would have been obvious to combine the teachings of Lieshout and Imaoka. Both Lieshout and Imaoka are directed to solving misalignment between an array substrate and a driving circuit that provides driving signals. (EX1005, 1:4-2:5, 2:21-23; EX1006, 5:28-32, 3:22-48; EX1002, ¶245.) And their solutions are similar – both discloses providing ***inclined*** pads in a symmetrical manner on the array substrate, which achieves alignment by adjusting the y-displacement between pad portion and the connection portion. (*See, e.g.,* EX1005, FIGs. 5-7; EX1006, FIGs. 2A-B and 11.) Thus, Lieshout and Imaoka are from the same field of endeavor and reasonably pertinent to the same technical problems of improving electrical connection between an array substrate and a driving circuit. (EX1002, ¶245.)

The Lieshout-Imaoka combination results in a system in which the IC bumps in Lieshout are ***inclined parallelogram bumps*** as taught by, for example, FIGs. 2A-B of Imaoka for reducing misalignment, to the extent they are not already. (EX1002, ¶246.) The terminals 16 in FIGs. 2A-B of Imaoka, which are for providing electrical connection to an array substrate, are analogous to the IC bumps of Lieshout bonded to pads, which has the same purpose. Thus, Lieshout's IC bumps can adopt the structure of terminals 16 to reduce misalignment. (*Id.*) At

the time of the invention, elongated bumps on an integrated circuit were commonplace for providing electrical connection with an array substrate. (*Id*.; *see also* EX1035, [0118].) Elongated bumps (as opposed to square and circle bumps) were known to be preferrable in as early as 1990. (EX1002, ¶77; *see also* EX1029-1031 and 1032-1034.) The simple modification of making the bumps elongated and inclined as taught by Imaoka (e.g., terminals 16 in FIGs. 2A-B, which are analogous to IC bumps in Lieshout) does not involve any extensive re-design and would be easy to manufacture. (EX1002, ¶246.)

Alternatively or additionally, the Lieshout-Imaoka combination results in a system in which the integrated circuit chip with inclined bumps (as taught by Imaoka such as FIG. 11) is mounted or designed to be mounted to the array substrate as taught by Lieshout. (*Id*.) Imaoka's FIG. 11 already shows an integrated circuit bonded to an underlying substrate via inclined bumps and corresponding inclined pads to provide driving signals. (*See, e.g.,* EX1006, FIG. 11.) It is structurally and functionally identical or at least analogous to Lieshout, where an integrated circuit is bonded to an array substrate via bumps and corresponding pads on its array substrate. Thus, it would have been obvious to combine the structure of FIG. 11 of Imaoka with Lieshout to reduce misalignment. This again amounts to a simple modification that does not involve any extensive re-design and would be easy to manufacture. (*Id*.)

The combination of Lieshout and Imaoka gains significant benefits. (EX1002, ¶247.) The parallelogram-shaped bumps, which match the shape of the pads, result a larger contact area than, for example, coupling a circular bump and a parallelogram pad, and thus can maximize overlap. (*Id*.) The elongated shape was known to be beneficial over a non-elongated shape (e.g., square, circle), for example, because it can "reduc[e] the area of the semiconductor device without reducing the bonding strength." (EX1030, 114; *see also* EX1033, 167.) This is particularly important for high-resolution displays, which require a greater number of bumps within a limited area. (EX1002, ¶247.) Lieshout itself recognizes that "[t]olerances for bonding IC chips on substrates have become increasingly important with the increase in the number of components on circuit boards and the increase in the number of connections per IC." (EX1005, 1:4-6.) Lieshout's process for aligning the bumps and pads (e.g., using its alignment monitoring device 112) is unaffected in the modified system and achieves better alignment. (EX1002, ¶247.)

Further, the Lieshout-Imaoka system provides greater alignment tolerance. (EX1002, ¶247.) In Lieshout, the integrated circuit chip and the array substrate (e.g., "glass substrate", "plastic substrate") may expand differently and Imaoka's radial elongation ensures continuity of electrical connection despite this. (*See*, *e.g.*, EX1005, 12:25-26; EX1002, ¶247)

Combining the technical features of Imaoka with the teachings of Lieshout would improve the capabilities of Lieshout in the same way, because the Lieshout-Imaoka combination ensures a parallelogram-shaped bonding area is achieved between a pad and a corresponding bump. (EX1002, ¶248.) Combining the teachings of Lieshout and Imaoka as such would yield predictable results of effectively ensure electrical connection despite potential deformation of component(s). (*Id*.) Further, it would have been obvious to try as there is a finite number of identified, predictable solutions (e.g., potential bumps shapes), without requiring much effort and with a reasonable expectation of success. The known benefits of Imaoka would prompt the application of Imaoka in the same field based on design incentives and other market forces to produce reliable displays that have high tolerance for various manufacturing and use conditions. (*Id*.)

D. Ground 4: Wildes and Lieshout Render Obvious Claims 1-10

1. Claim 1

a. Preamble: "An electronic device, comprising:"

Wildes and Lieshout both disclose the preamble. (*Supra* §V.A.2.a, V.C.3.a.)

b. 1[a]: "an array substrate;"

Wildes and Lieshout both disclose element 1[a]. (*Supra* §.) It would have been obvious to combine them. (*Supra* § V.A.2.b, V.B.2.b.)

c. 1[b]: "a pad portion disposed on the array substrate; and"

Wildes and Lieshout both disclose element 1[b]. (*Supra* §V.A.2.c, V.B.2.c.)

d. 1[c]: "an integrated circuit disposed on the pad portion and comprising a bump portion;"

Wildes and Lieshout both disclose element 1[c]. (*Supra* § V.A.2.d, V.B.2.d.)

e. 1[d]: "wherein: the pad portion comprises a first sub-pad unit comprising an inclined first pad and a second sub-pad unit comprising an inclined second pad;"

Wildes and Lieshout both disclose element 1[d]. (*Supra* § V.A.2.e, V.B.2.e.)

f. 1[e]: "the first pad and the second pad are inclined in different directions symmetrically about an imaginary line that divides the pad portion; and;"

Wildes and Lieshout both disclose element 1[e]. (*Supra* § V.A.2.f, V.B.2.f.)

g. 1[f]: "the pad portion is electrically connected with the bump portion;"

Wildes and Lieshout both disclose element 1[f]. (*Supra* § V.A.2.g, V.B.2.g.)

h. 1[g]: "the bump portion comprises a first sub-bump unit comprising an inclined first bump and a second sub-bump unit comprising an inclined second bump;"

Wildes and Lieshout both disclose element 1[g]. (*Supra* § V.A.2.h, V.B.2.h.)

i. 1[h]: "the first bump and the second bump are inclined in different directions symmetrically about the imaginary line that divides the pad portion."

Wildes and Lieshout both disclose element 1[h]. (*Supra* § V.A.2.i, V.B.2.i.)

2. Claim 2: "The electronic device of claim 1, wherein at least one of the first pad and the second pad has a parallelogram shape."

Wildes and Lieshout both disclose claim 2. (*Supra* § V.A.3, V.C.4.)

3. Claim 3: "The electronic device of claim 1, wherein: the first bump has a same inclination angle as the first pad; and the second bump has a same inclination angle as the second pad."

Wildes and Lieshout both disclose claim 3. (*Supra* § V.A.4, V.B.4.)

4. Claim 4: "The electronic device of claim 1, wherein a shape of the first bump corresponds to a shape of the first pad, and a shape of the second bump corresponds to a shape of the second pad."

Wildes and Lieshout both disclose claim 4. (*Supra* § V.A.5, V.C.6.)

5. Claim 5: "The electronic device of claim 1, wherein the first pad is electrically connected with the first bump and the second pad is electrically connected with the second bump."

Wildes and Lieshout both disclose claim 5. (*Supra* §V.A.6, V.C.7.)

6. Claim 6: "The electronic device of claim 1, wherein an area of the first pad is greater than an area of the first bump."

Wildes and Lieshout both disclose claim 6. (*Supra* § V.A.6, V.C.8.)

7. Claim 7: "The electronic device of claim 1, wherein: the first bump comprises a first region and a second region; and the first region overlaps the first pad and the second region does not overlap the first pad."

Wildes discloses claim 7. (*Supra* § V.A.7, V.C.9.)

8. Claim 8: "The electronic device of claim 1, wherein at least one of the first pad and the second pad has a quadrangle shape."

Wildes and Lieshout both disclose claim 8. (*Supra* § V.A.9, V.C.10.)

9. Claim 9: "The electronic device of claim 2, wherein the pad portion further comprises a third sub-pad unit comprising a third pad having a rectangular shape and disposed between the first sub-pad unit and the second sub-pad unit."

Wildes and Lieshout both disclose claim 9. (*Supra* §V.A.9, V.C.11.)

10. Claim 10: "The electronic device of claim 9, wherein the bump portion further comprises a third sub-bump unit comprising a third bump having a rectangular shape and disposed between the first sub-bump unit and the second sub-bump unit."

Wildes and Lieshout both disclose claim 10. (*Supra* § V.A.11, V.C.12.)

11. A POSITA would be motivated to combine Wildes and Lieshout.

It would have been obvious to combine the teachings of Wildes and Lieshout. (EX1002, ¶267.) Both Wildes and Lieshout are directed to solving potential misalignment in the electrical connection between an array substrate and a driving circuit. And their solutions are similar – both discloses providing inclined pads in a symmetrical manner on the array substrate, which achieves alignment by adjusting the y-displacement between pad portion and the connection portion of the driving circuit. Thus, Wildes and Lieshout are from the same field of endeavor and reasonably pertinent to the same technical problems of improving

electrical connection between an array substrate and a driving circuit in a display. (EX1002, ¶268.)

The Wildes-Lieshout combination can result in a system in which Lieshout's IC bumps are ***inclined parallelogram bumps*** as taught by, for example, pads 84 of Wildes for reducing misalignment, to the extent they are not already. (EX1002, ¶269.) As discussed, Wildes' substrate 72 is or is analogous to an integrated circuit and thus Wildes' connection pads 84 are IC bumps. (*Supra V.A.2.d.*) Wildes' design of connection pads 84 can be adopted to IC bumps of Lieshout, which can be mounted to various array substrates (e.g., "glass substrate", "plastic substrate"). (*See*, *e.g.*, EX1005, 12:25-26.) Lieshout already teaches that "[t]he pattern and spacing" of pads and IC bumps should match. (*See* EX1005, 1:24-28.) Making the IC bumps inclined as taught by Wildes (e.g., connection pads 84) does not involve any extensive re-design and would be easy to manufacture as they were well-known and can be easily made. (EX1002, ¶269.) At the time of the invention, elongated bumps on an integrated circuit were commonplace. (*Id.*; *see also* EX1035, [0118].) Elongated bumps (as opposed to square and circle bumps) were also known to be preferrable in as early as 1990. (EX1002, ¶77; *see also* EX1029-1031 and 1032-1033.)

Alternatively or additionally, the Wildes-Lieshout combination can result in a system in which the integrated circuit chip with inclined bumps (as taught by

Wildes such as FIG. 14) is mounted or designed to be mounted to the array substrate of Lieshout. (EX1002, ¶269.) FIG. 14 of Wildes already discloses an integrated circuit with inclined bumps in a structure identical or at least analogous to Lieshout and can be combined with Lieshout, where IC is bonded to the array substrate. (*Id*.) It is structurally and functionally identical or at least analogous to Lieshout. Thus, it would have been obvious to combine the structure of FIG. 14 of Wildes with Lieshout to reduce misalignment. This again amounts to a simple modification that does not involve any extensive re-design and would be easy to manufacture. (*Id*.)

The combination gains significant benefits, for example, similar to the Lieshout-Imaoka system. (*Supra V.C.13*.) Wildes-Lieshout system would ensure that the resulting display can provide reliable electrical connection, thus providing reliable graphics and preventing short circuits. (EX1002, ¶270.)

The combination would ensure an intended overlap area is achieved between a pad and a corresponding bump despite deformation. (EX1002, ¶271.) Combining the teachings of Wildes and Lieshout as such would yield predictable results of ensuring electrical connection. For example, Lieshout's process for aligning the bumps and pads (e.g., using its alignment monitoring device 112) is unaffected in the modified system and achieves better alignment. (*Id*.) Further, it would have been obvious to try combining Lieshout with Wildes, as there is a

finite number of identified, predictable solutions for connecting an array substrate with a driving circuit (e.g., chip-on-glass, chip-on-plastic, chip-on-film), without requiring much effort and with a reasonable expectation of success. (*Id*.) For example, there are a finite number of potential bumps shapes that were commonly seen in the industry and are easy to manufacture at the time of the invention. (*Id*.) The known benefits of Wildes would prompt the application of Wildes in the same field based on design incentives and other market forces to produce reliable displays that have high tolerance for various manufacturing and use conditions. (*Id*.)

E. Ground 5: Wildes and Shioda Render Obvious Claim 6

1. Summary of Shioda

Shioda was published on March 7, 2003, qualifying as prior art at least under § 102(a)(2). The Examiner never found, and Applicant never cited, Shioda during prosecution.

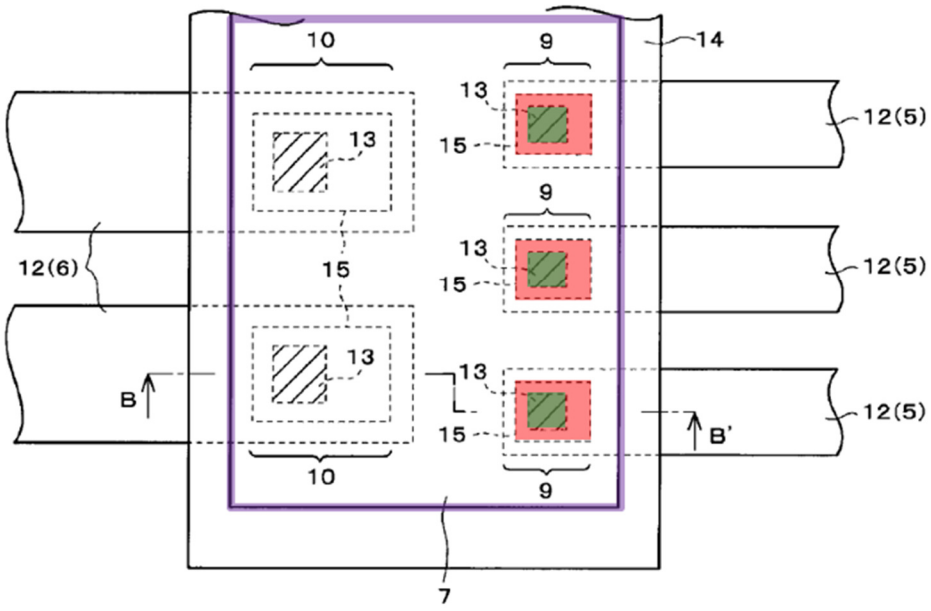
Shioda is directed to "a display device . . . wherein various drive ICs can be mounted at low cost." (EX1038, Abstract.) Shioda states that "drive ICs of various sizes have been commercially available" and thus "changing the design such as the position of the contact pad to mount a drive IC . . . may lead to increased manufacturing costs." (EX1038, [0036]-[0037].) To solve this problem, Shioda teaches "an opening having an ***area larger than that of the bump***

electrode." (*Id*., [0038]; EX1002, ¶¶272-273.)

2. Claim 6: "The electronic device of claim 1, wherein an area of the first pad is greater than an area of the first bump."

For example, Shioda teaches "an opening having an ***area larger than that of the bump electrode***." (EX1038, [0038].) FIG. 4 shows a ***liquid crystal drive IC 7*** providing ***bump electrodes 13***. (*Id*., [0070].) Further, ***openings 15*** are "are formed in the protective film 12." (*Id*., [0073].) Each opening 15 serves as a conductive pad. (EX1002, ¶274.) The openings 15 "are formed in a rectangular shape ***slightly larger*** than the ***bump electrode 13***." (*Id*., [0074]; *see also id*., [0075].)

[FIG. 4]



At the time of the invention, it would have been obvious to apply Shioda's techniques to Wildes to make a connection pad larger than the corresponding bump

in one or both directions. Wildes and Shioda are from the same field of endeavor and reasonably pertinent to the same technical problems of preventing misalignment between an array substrate and a driving circuit. (EX1002, ¶¶274-275.) The simple modification of making a pad larger than the bump does not involve any extensive re-design and would be easy to manufacture. Combining the technical features of Shioda with Wildes would improve the capabilities of Wildes in the same way, because the Wildes-Shioda combination would ensure that the pad provides extra margin to form a reliable connection. Standardizing larger pads can make the substrate design more versatile. The combination would yield predictable results of effectively ensure electrical connection. (*Id*.) Further, it would have been obvious to try, as there is a finite number of identified, predictable solutions (e.g., making the pad longer, making the pad wider), without requiring much effort and with a reasonable expectation of success. (*Id*.) The known benefits of Shioda would prompt the application of Shioda in the same field based on design incentives and other market forces to produce reliable displays that have high tolerance for various manufacturing and use conditions. (*Id*.)

F. Ground 6: Wildes, Cristaldi, and Shioda Render Obvious Claim 6

Shioda discloses claim 6. (*Supra V.E.2*.) At the time of the invention, it would have been obvious to apply Shioda to the Wildes-Cristaldi system for

similar reasons discussed above. (*Id.*; EX1002, ¶¶276-277.)

G. Ground 7: Lieshout, Imaoka, and Shioda Render Obvious Claim 6

Shioda discloses claim 6. (*Supra V.E.2.*) At the time of the invention, it would have been obvious to apply Shioda to the Lieshout-Imaoka system for similar reasons. (*Id.*; EX1002, ¶¶278-279.)

H. Ground 8: Wildes, Lieshout, and Shioda Render Obvious Claim 6

Shioda discloses claim 6. (*Supra V.E.2.*) At the time of the invention, it would have been obvious to apply Shioda to the Wildes-Lieshout system for similar reasons discussed above. (*Id.*; EX1002, ¶¶280-281.)

VI. SECTION 325(D) IS INAPPLICABLE

Section 325(d) is inapplicable to this proceeding because the Petition does not raise substantially the same art or arguments in the same way as the examination of the '503 patent and, to the extent the Petition does, the Office erred in a material manner. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7-11 (P.T.A.B. Feb. 13, 2020) (precedential).[3]

[3] Petitioner is not addressing discretionary issues in the Petition. *See FAQs for Interim Processes for PTAB Workload Management*, USPTO,

The ’503 examination was not robust. The Examiner’s sole Office Action contained only double-patenting rejections based on the ’503 patent’s parent. His Notice of Allowance was conclusory, citing the entire claim 1 as the reason for allowance. (EX1003, 33-34.) Not a single pertinent reference was mentioned or discussed in the Notice of Allowance. (EX1003, 32-35.) About a month ***after the allowance***, the applicant submitted Wildes in an IDS. (EX1003, 18.) The Examiner simply initialed and placed the IDS in the file without applying or even discussing Wildes. (EX1003, 15.)

Cristaldi, Lieshout, and Imaoka were not considered during the prosecution of the ’503 patent. The Examiner did not raise any prior art rejections at all. “The Board has consistently declined exercising its discretion under Section 325(d) when the only fact a Patent Owner can point to is that a reference was disclosed to the Examiner during the prosecution.” *Amgen Inc. v. Alexion Pharms., Inc.*, IPR2019-00740, Paper 15 at 65-66 (P.T.A.B. Aug. 30, 2019).

Furthermore, the Examiner never considered the Wildes-Cristaldi, Wildes-Lieshout, or Lieshout-Imaoka combinations. Both Lieshout and Imaoka address potential misalignment between an array substrate and a driving circuit. Cristaldi

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https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management (last visited Aug. 28, 2025).

discloses COG technology for mounting IC bumps onto pads of an array substrate. Thus each asserted ground is materially different and not cumulative of the art applied during examination.

Even if the Board were to conclude otherwise, the Office erred in a material manner. The Examiner allowed the claims without considering Cristaldi, Lieshout, and Imaoka. While the Examiner may have considered Wildes in an IDS, the touchstone is "the extent of such consideration" and whether there is "evidence of record indicating why the Examiner" did not reject the claims. *William Hill US Holdco, Inc. v. CG Tech. Dev., LLC*, IPR2019-00317, Paper 14 at 35 (P.T.A.B. May 30, 2019). Accordingly, "[t]he Board frequently holds that a reference that was neither applied against the claims nor discussed by the Examiner does not weigh in favor of exercising the Board's discretion under § 325(d) to deny a petition." *Amazon.com, Inc. v. M2M Sols. LLC*, IPR2019-01204, Paper 14 at 16 (P.T.A.B. Jan. 23, 2020) (internal quotations omitted). Wildes was neither applied against the claims nor discussed by the Examiner, because it was provided after the Notice of Allowance.

Where the examination record is not well developed, as here, it may indicate that the Examiner erred by "overlook[ing] something persuasive." *Advanced Bionics*, IPR2019-01469, Paper 6 at 10. This Petition confirms the Examiner's error because Lieshout —which the Examiner did not consider—and Wildes—

which the Examiner may have considered but without providing any explanation—each in combination with Imaoka, Cristaldi, and each other renders the claims obvious. *See William Hill*, IPR2019-00317, Paper 14 at 35 (reasonable likelihood that claims are obvious in view of unaddressed art "weighs heavily" in instituting). Moreover, the obviousness arguments here are supported by the testimony of Mr. Chen (Ex. 1002) that the Examiner did not have.

For all the foregoing reasons, the Board should decline to deny the Petition under § 325(d).

VII. NOTICES AND STATEMENTS

Pursuant to 37 C.F.R. § 42.8(b)(1), BOE Technology Group Co., Ltd., is the real party-in-interest for Petitioner.

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner identifies the following related matters.

Samsung Display Co., Ltd., v. BOE Technology Group Co., Ltd., et al., No. 2:25-cv-00430 (E.D. Tex.)

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioner identifies the following counsel (and a power of attorney accompanies this Petition).

Lead Counsel	First Backup Counsel
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Pursuant to 37 C.F.R. § 42.8(b)(4), service information for lead and back-up counsel is provided above. Petitioner consents to electronic service by email to BOE-Samsung-IPR@mofo.com.

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '503 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

The USPTO is authorized to charge any required fees, including the fee as set forth in 37 C.F.R. § 42.15(a) and any excess claim fees, to Deposit Account

No. **03-1952** referencing Docket No. **37294-00000.04**

Dated: August 29, 2025

Respectfully submitted,

By */s/ Alex S. Yap*

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Certification of Word Count (37 C.F.R. § 42.24)

I hereby certify that this Petition for *Inter Partes* Review has 13,999 words (as counted by the "Word Count" feature of the Microsoft Word™ word-processing system), exclusive of "a table of contents, a table of authorities, mandatory notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing."

Dated: August 29, 2025

By */s/ Alex S. Yap*
Alex S. Yap

Certificate of Service (37 C.F.R. § 42.6(e)(4) and 42.205(a))

I hereby certify that the attached Petition for *Inter Partes* Review and supporting materials were served as of the below date by UPS, which a means as fast and reliable as U.S. Express Mail on the Patent Owner at the correspondence address indicated for U.S. Patent No. 11,081,503.

CANTOR COLBURN LLP
20 Church Street
22nd Floor
Hartford, CT 06103

Dated: August 29, 2025

By */s/ Alex S. Yap*
Alex S. Yap