

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Patent No. 10,720,483

Inter Partes Review No. IPR2025-01498

DECLARATION OF THOMAS CREDELLE

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Exhibit List

Exhibit Description	Exhibit #
U.S. Patent No. 10,720,483	1001
Expert Declaration of Mr. Thomas Credelle	1002
Prosecution History of U.S. Patent No. 10,720,483	1003
U.S. Publication No. 2007/0058100 to Ishii	1004
U.S. Publication No. 2003/0141811 to Park	1005
U.S. Publication No. 2002/0118150 to Kwon	1006
U.S. Publication No. 2012/0313100 to Liu	1007
U.S. Publication No. 2011/0128211 to Ono	1008
U.S. Patent No. 6,674,245 to Ko	1009
U.S. Publication No. 2004/0012028 to Park et al.	1010
U.S. Publication No. 2011/0297941 to Zhan et al.	1011
U.S. Publication No. 2012/0007080 to Liu	1012
U.S. Patent No. 8,664,662 to Ono et al.	1013
U.S. Publication No. 2003/0222589 to Osame	1014
U.S. Publication No. 2012/0211750 to Kakinuma	1015

I, Thomas Credelle, make this declaration in connection with the proceeding identified above.

I. INTRODUCTION

1. I have been retained as an expert witness on behalf of BOE Technology Group Co., Ltd. (“Petitioner” or “BOE”) to provide expert opinions on the patentability of United States Patent No. 10,720,483 (“the ’483 patent”).

2. I am being compensated at my normal rate, plus reimbursement for expenses, for my analysis. My compensation does not depend on the content of my opinions or the outcome of this proceeding.

II. QUALIFICATIONS

3. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae, which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

4. As shown in my curriculum vitae, I have devoted my career to the research and development and product engineering of flat panel displays and materials/optics/electronics for flat panel displays and touch sensors. I have over 20 years of involvement in active-matrix LCD R&D, starting in 1983 at RCA Labs and continuing at GE. I led the product development of active matrix LCDs for notebook computers at Apple in the early 1990s and had close collaboration with

many LCD developers in Asia. Later in my career, I made significant contributions to the design and implementation of new pixel architectures for LCDs and OLEDs while at Clairvoyante; both efforts involved Thin Film Transistor (“TFT”) design modifications to achieve the desired goals of high pixel transmission and reduced circuit complexity.

5. After receiving my Masters in Electrical Engineering from MIT in 1970, I was employed by RCA at Sarnoff Labs in Princeton, NJ as a Member of the Technical Staff and later as a Group Manager in charge of all active matrix LCD research. During my time at RCA, I participated in research and development projects relating to optical materials and flat panel displays, including LCD devices. In 1983, I established the TFT LCD Program at Sarnoff Labs. As a Group Manager, I led a project that resulted in the development of the first poly silicon TFT LCD at Sarnoff Labs. I received the Sarnoff Outstanding Achievement Award for Large Area Flat Panel TV Developments.

6. From 1986 to 1991, I was employed by GE as the Manager of TFT LCD Research and Development at the GE Research and Development Center in Schenectady, NY. My duties included contributing to and managing research and development efforts relating to TFT and LCD technology. While employed by GE, I led the team that built the world’s first 1-million-pixel color LCD device. I

also led the development of numerous other optical devices utilizing LCD technology.

7. From 1991 to 1994, I was employed by Apple Computer as the Manager of Display Engineering. In my role at Apple, I supervised all TFT-LCD design (in-house and at vendors), engineering, and qualifications for the first PowerBook notebook computers introduced to market in the United States. A key part of my effort was the evaluation and development of active matrix LCDs with improved performance, such as viewing angle, contrast ratio, and uniformity.

8. From 1994 to 1996, I was employed as the Director of Advanced Product Marketing by Allied Signal, where I was involved with the design and engineering of optical films and custom focusing backlight designs for improving the viewing angle performance of LCD devices.

9. From 1996 to 1999, I was employed as the Director of Product Marketing for Motorola's Flat Panel Display Division, where I worked on the development of new flat panel technology. I also worked closely with Motorola groups responsible for integrating TFT-LCD technology into mobile phone products and materials development for OLED displays.

10. From 1999 to 2001, I served as the Vice President of Operations of Alien Technology Corporation. During my time at Alien Technology, I was

involved with the design and architecture of drive electronics packaging technology suitable for flexible display devices.

11. From 2001 to 2007, I served as the Vice President of Engineering for Clairvoyante, Inc. My responsibilities as the VP of Engineering included managing research, development, engineering, and marketing of technologies for improving the resolution and power consumption of color flat panel displays, which required significant changes to the active matrix layout. During my time at Clairvoyante, I was therefore heavily involved with the design of the active matrix array and the LCD or OLED pixel circuit and driving circuitry.

12. From 2007 to 2008, I served as the Senior VP of Engineering for Pureddepth, Inc. My responsibilities included the design of hardware and software to create 3D images on TFT-LCDs.

13. From 2012 through 2015, I served as the Vice President of Application Engineering and Device Performance for Innova Dynamics, Inc., a nanotechnology company developing materials to be used in LCDs and touch sensors. In that effort, I led the collaboration with major capacitive touch sensor makers to replace brittle Indium Tin Oxide (“ITO”) transparent conductors with transparent silver nanowire conductors, which are compatible with flexible touch sensors. We successfully fabricated flexible capacitive touch sensors that could be bent without breaking.

14. In 2008, I founded TLC Display Consulting, a company that provides technical consulting in the areas of flat panel displays, liquid crystal displays, OLED, touch sensors, LEDs, and related electronics. I currently serve as the President of TLC Display Consulting.

15. I have been an active member of the Society for Information Display (“SID”) for over 40 years, and am currently a Life Member. I was a member of the Society for Information Display’s Program Committee for 15 years, and the Director of the Society for Information Display’s Symposium Committee for 10 years. In 1984, I was awarded the title of Fellow of the Society for Information Display in recognition of my achievements and contributions to flat panel display technology.

16. My curriculum vitae contains further details regarding my experience, education, publications, and other qualifications that allow me to render expert opinions in connection with this proceeding.

III. MATERIALS CONSIDERED

17. In preparing this declaration, I have reviewed, among other things, the ’483 patent and file history. I have also considered each of the documents cited in this Declaration and the documents specifically identified in the Exhibit List. In formulating my opinions, I have further relied upon my extensive experience in the relevant fields.

IV. SUMMARY OF THE '483 PATENT

A. Filing And Priority Dates

18. The '483 patent was filed on September 18, 2017, and issued on July 21, 2020. The '483 patent is a continuation of Application No. 15/064,526, which became U.S. Patent No. 9,768,241, and a continuation of Application No. 13/801,937, which became U.S. Patent No. 9,299,730. The '483 patent claims priority to Korean Patent Application 10-2012-0104215, which was filed on September 19, 2012.

B. Specification And Claims

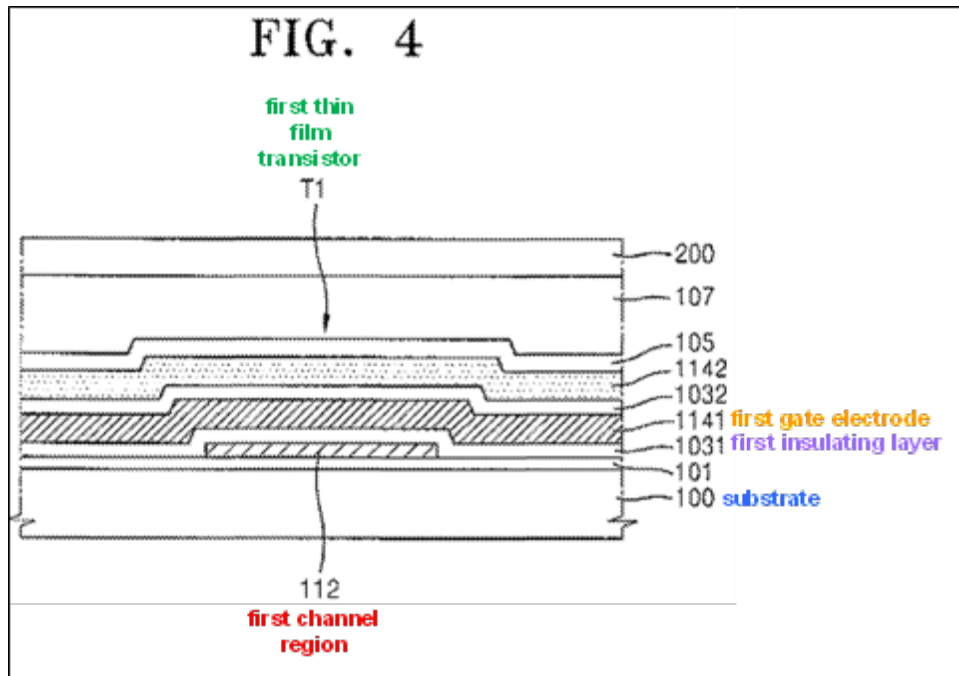
19. The '483 patent is titled “Thin Film Transistor Array Substrate and Organic Light-Emitting Diode Display.” The '483 patent discloses “[a] thin film transistor (TFT) array substrate” including a plurality of layers and materials. (EX1001, Abstract.) The TFT array substrate may include a plurality of TFTs such as a driving TFT T1, a compensation TFT T3, and an initialization TFT T4. (EX1001, 2:14-32, Fig. 1.) The OLED display may also include a storage capacitor Cst comprising a lower electrode Cst1/1141 and an upper electrode Cst2/1142. (EX1001, 7:8-10.)

20. The '483 specification explains that misalignment between the substrate and a mask (for patterning the layers) may occur during processing of an OLED display. (EX1001, 1:39-46.) The misalignment may lead to a deviation in the amount of overlap (an overlay deviation) between the upper electrode 1141 and

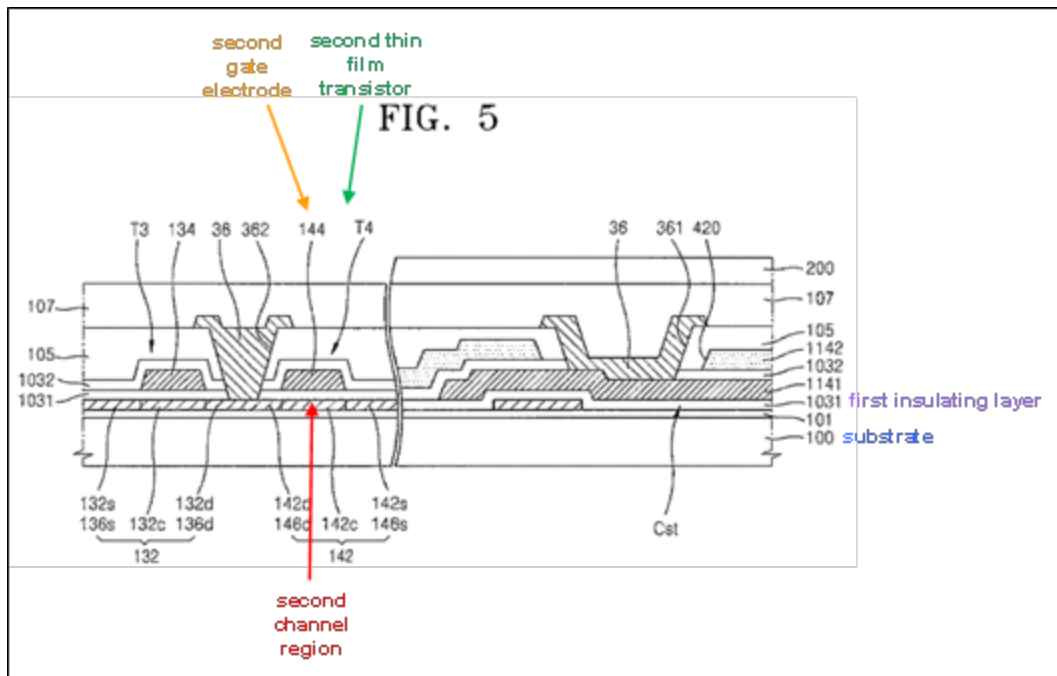
the lower electrode 1142 of the storage capacitor. (EX1001, 1:46-48.) The overlay deviation results in the actual capacitance differing from the target capacitance, thereby causing issues with the OLED display such as “low-gradation spots, abnormal colors, or the like.” (EX1001, 1:48-51.)

21. Figures 4 and 5 (annotated below) show a cross-sectional view of the TFT array substrate. Independent claim 1 is directed to the TFT array substrate, which comprises:

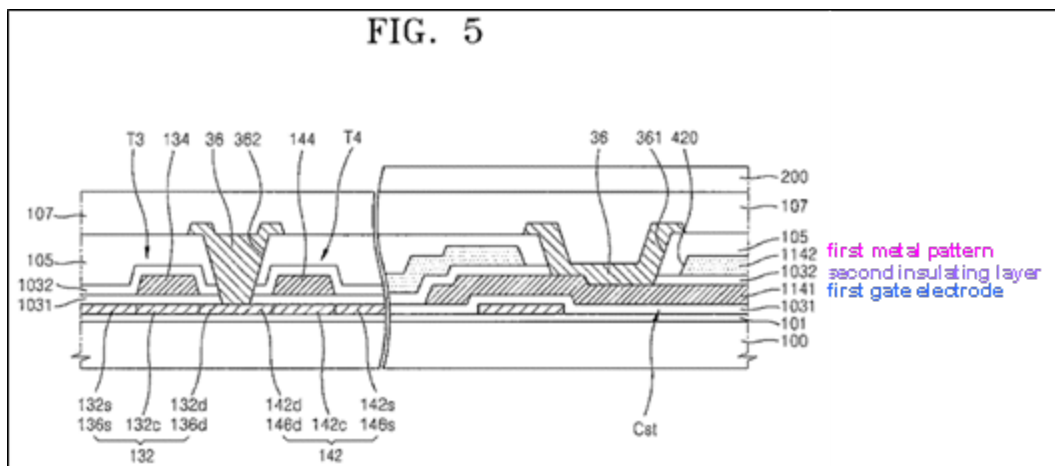
- **“a substrate”** 100 (EX1001, 9:5-7)
- **“a first thin film transistor”** (driving TFT T1) including **“a first channel region”** (driving channel region of driving semiconductor layer 112 (EX1001, 9:21-24)) and **“a first gate electrode”** (driving gate electrode 1141 (EX1001, 6:65-66)) overlapping the first channel region (EX1001, 7:5-7), the first gate electrode 1141 and the first channel region being spaced apart from each other with **“a first insulating layer”** (first gate insulation film 1031) therebetween (EX1001, Figure 4);



- “a second thin film transistor” (compensation TFT T3, or alternatively, initialization T4) including “a second channel region” (compensation channel region 132c, or alternatively, initialization channel region 142c (EX1001, 9:24-6, 9:29-30)) and “a second gate electrode” (compensation gate electrode 134, or alternatively, initialization gate electrode 144 (EX1001, 7:57-59, 8:4-5)) overlapping the second channel region 132c/142c (EX1001, 9:51-57), the second gate electrode 134/144 and the second channel region 132c/142c being spaced apart from each other with the first insulating layer 1031 therebetween (EX1001, Figure 5);

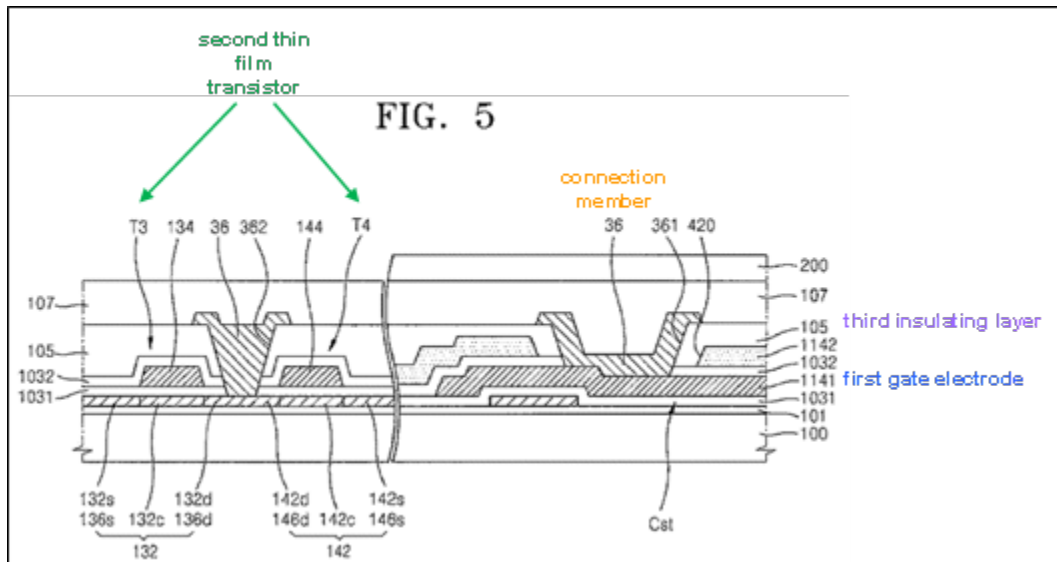


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- **“a third insulating layer”** (inter-layer insulation film 105) disposed on the first metal pattern 1142 (EX1001, Figure 5); and

- **“a connection member”** (connection node 36) disposed on the third insulating layer 105 (EX1001, Figure 5) and electrically connecting the first gate electrode 1141 and the second thin film transistor T3/T4 (EX1001, 2:18-20, 2:25-27).



22. Independent claim 22 recites limitations similar to independent claim 1. Claim 22 further requires “the connection member overlapping a portion of the first channel region in a plan view.” (EX1001, Figure 2.)

23. Claims 2-21 and 23-29 are dependent claims. Claims 2-6, 23, and 24 are directed to an opening in the first metal pattern 1142. Claims 7-10, 25, and 26 are directed to the first channel region including bent portion(s). Claims 11-13 and 27-29 are directed to a driving voltage line and a first contact hole of the first metal pattern. Claims 14-21 relate to a first gate line, a second gate line, and an initialization voltage line.

C. Prosecution History

24. I understand that during prosecution of the '483 patent, the Examiner issued a Restriction Requirement on February 21, 2019 requiring restriction between Group I (claims 1-21, drawn to a TFT array substrate) and Group 2 (claims 22-40, drawn to a display device). (EX1003, 96-98.) On April 16, 2019, Applicant responding by electing Group I, claims 1-21. (EX1003, 58.)

25. On October 17, 2019, the Examiner issued a Non-Final Office Action that rejected claims 1-21 for failing to comply with the written description requirement, and then provided suggestions for amending the claims to address the rejections. (EX1003, 50.) The Examiner did not issue any rejections based on prior art, anticipation, or obviousness. (EX1003, 48-51.)

26. On January 9, 2020, Applicant responded by amending the claims according to the Examiner's suggestions (from the October 17, 2019 Non-Final Office Action). (EX1003, 31-47.) Applicant also added claims 41-48, which later issued as claims 22-29 of the '483 patent.

27. On March 10, 2020, the Examiner issued a Notice of Allowance without stating the reasons why the claims were allowed. (EX1003, 20-25.)

V. RELEVANT LEGAL STANDARDS AND DEFINITIONS

A. Anticipation

28. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly

or inherently in a single prior art reference or system. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference and that it would have been so recognized by a POSITA. In addition, I understand that an enabling disclosure is a disclosure that allows a POSITA to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

B. Obviousness

29. I understand that a claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the claimed subject matter was made to a POSITA to which the subject matter pertains. I understand that a patent claim may be obvious to a POSITA in view of the prior art teachings of a single reference or a combination of references.

30. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the

level of ordinary skill in the art, and any secondary considerations to the extent they exist.

31. It is also my understanding that there are principles that may be used as further guidance in an obviousness analysis (especially when considering combinations of references), which include considering whether:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;
- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;
- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;
- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based

on design incentives or other market forces if the variations would have been predictable to a POSITA;

- there existed at the time of conception and reduction to practice a known problem for which there was an obvious solution encompassed by the patent's claims; and
- there is some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed subject matter.

32. I understand that there are secondary considerations that may tend to show that a claimed invention would not have been obvious to a POSITA. These include, for example, commercial success, long-felt but unsolved needs, failure of others, and unexpected results. I further understand that there must be a relationship, or nexus, between any secondary considerations and the novelty of the claimed invention.

VI. LEVEL OF ORDINARY SKILL IN THE ART FOR THE '483 PATENT

33. I am informed and understand that various factors can be considered in determining a person of ordinary skill in the art (POSITA). I am informed and understand that those factors include: (1) the educational level of the inventors; (2) the type of problems encountered in the art; (3) prior art solutions to those

problems; (4) the rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the field.

34. A person of ordinary skill in the art (POSITA) in the field of the '483 patent would have a bachelor's degree in electrical engineering or materials science, including OLED displays, or an equivalent level of skill, knowledge, and experience. This POSITA would have been aware of and generally knowledgeable about OLED materials, and display pixel design, layout, and operation.

35. I agree with this level of ordinary skill for the '483 patent. Based on my experience, I understand and know of the capabilities of a person of this skill level as of the time the '483 priority application was filed in 2012. I am familiar with how a POSITA would have understood and used the terminology found in the '483 patent at the time of the filing of the priority application, and with the state of the art at that time.

VII. CLAIM CONSTRUCTION

36. I have been informed that claim construction requires consideration of the words of the claims themselves, the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. I have also been informed that the specification is usually definitive, as it is the single best guide to the meaning of a disputed term.

37. I have been informed that, in the context of this proceeding, Petitioner did not propose any terms for construction. Instead, Petitioner believes each of the terms of the '483 patent carries its ordinary and customary meaning, which is the meaning that the term would have to a POSITA. I agree with Petitioner and apply the ordinary and customary meaning of the terms in my analysis below.

VIII. PRIOR ART

38. I understand that each of the references discussed herein qualifies as prior art against the '483 patent:

39. U.S. Publication No. 2003/0141811 ("Park," EX1005) was filed on December 27, 2002, claims priority to a Korean patent application filed on December 29, 2001, and published on July 31, 2003.

40. U.S. Publication No. 2011/0297941 ("Zhan," EX1011) was filed on February 17, 2011, claims priority to a Korean patent application filed on June 7, 2010, and published on December 8, 2011.

41. U.S. Publication No. 2003/0222589 ("Osame," EX1014) was filed on January 17, 2003, claims priority to Japanese patent applications filed on January 18, 2002 and February 1, 2002, and published on December 4, 2003.

42. U.S. Patent No. 6,674,245 ("Ko," EX1009) was filed on December 26, 2002, claims priority to a Korean patent application filed on December 29, 2001, published on July 3, 2003, and issued on January 6, 2004.

43. U.S. Publication No. 2002/0118150 (“Kwon,” EX1006) was filed on December 7, 2001, claims priority to a Korean application filed on December 29, 2000, and published on August 29, 2002.

44. U.S. Publication No. 2012/0313100 (“Liu100,” EX1007) was filed on February 2, 2012, claims priority to a foreign application filed on June 10, 2011, and published on December 13, 2012.

45. U.S. Publication No. 2011/0128211 (“Ono,” EX1008) was filed on January 24, 2011, claims priority to a PCT application filed on November 27, 2009, and published on June 2, 2011.

46. U.S. Publication No. 2012/0007080 (“Liu080,” EX1012) was filed on October 15, 2010, claims priority to a Taiwanese application filed on July 8, 2010, and published on January 12, 2012.

IX. ANALYSIS AND OPINION

A. Claims 1, 11, 14, And 15 Are Obvious Over Park

1. Summary of Park

47. Park relates “to an active matrix electro luminescence display (ELD) device having thin film transistors and [a] manufacturing method for the same.” (EX1005, [0003].) Park states that there are inorganic ELD devices and organic ELD devices. (EX1005, [0003].) Park explains that the organic ELD device “emits light by recombination of an electron and a hole and thus it is referred to as an organic light emitting diode (OLED).” (*Id.*) Park discloses that these OLED

devices have advantages including being “self-luminescent,” able to “display every color[] in the visible range,” and having “a high brightness and a low action voltage” that makes them “suitable for an ultra-thin type display device.” (*Id.*) For example, Park states: “[r]ecently, an active matrix type display in which a plurality of pixels is arranged in a matrix form and a thin film transistor is connected thereto has been widely applied to the flat panel display devices.” (*Id.*)

48. Referring to Figure 1, Park discloses that “a pixel of the active matrix organic electro luminescent display device” (prior art) “has a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7.” (EX1005, [0006].) Park explains that the storage capacitor 6 “is for keeping a gate driving voltage of the driving thin film transistor stable and is an important element for displaying high quality images by restraining a pixel voltage fluctuation that is induced by a kick-back voltage of the switching film transistor and a leakage current.” (EX1005, [0015].) The capacitance of the storage capacitor 6 is directly proportional to the area of the electrodes and inversely proportional to the thickness of the dielectric substance. (*Id.*) Therefore, there is a limit to reducing the thickness of the dielectric substance. (*Id.*) But “[i]f the area of the electrode of the storage capacitor is increased, it results in a decrease of an area of the pixel electrode, i.e., the anode electrode 60, and thus an aperture ratio is decreased.” (*Id.*)



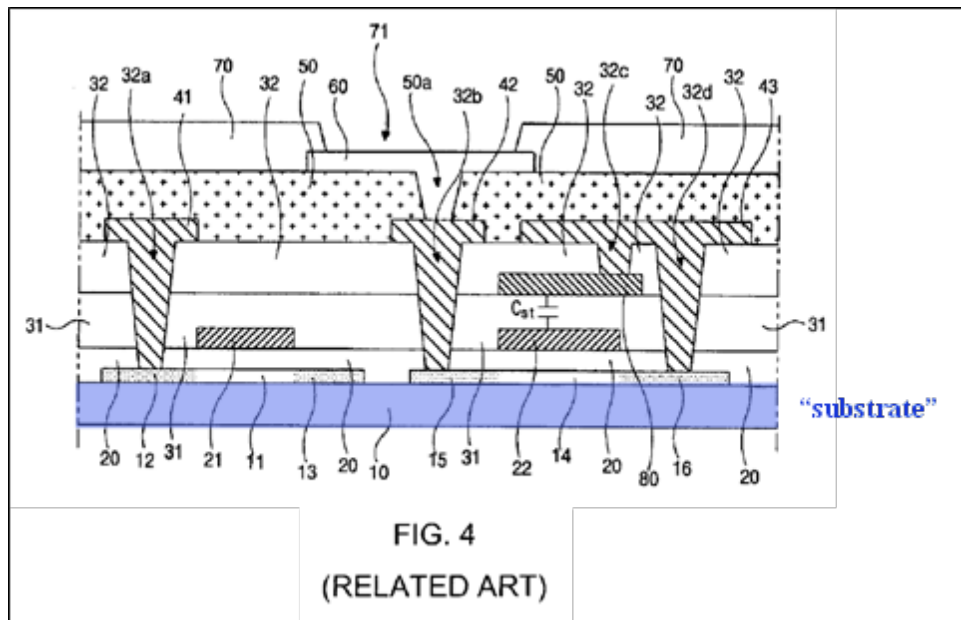
film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7.”

(EX1005, [0006] (emphases added), Fig. 1.)

54. Park describes the plurality of TFTs as part of “an *array substrate* of the active matrix organic electroluminescent display device.” (EX1005, [0014] (emphasis added).)

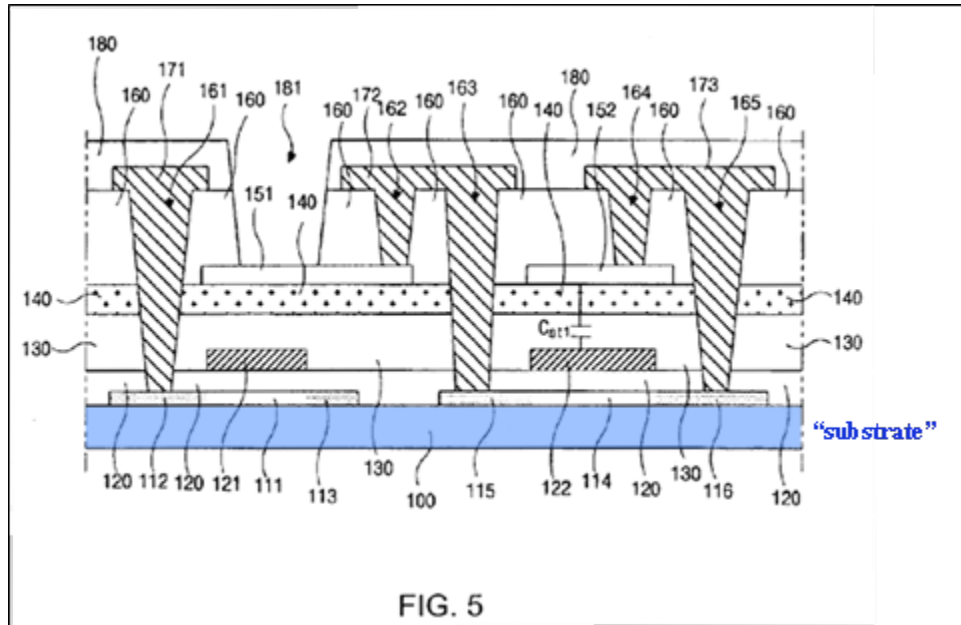
b. 1[a]: “a substrate;”

55. Park discloses “a substrate.” For example, Park’s active matrix organic electro luminescent display device “is formed on a transparent insulating substrate.” (EX1005, [0034]; *see also* [0007] (“display device . . . is formed on a substrate 10”).) Figure 4 (annotated below) shows Park’s substrate 10.



56. As shown in Figure 5 (annotated below), Park discloses “a transparent *substrate 100*.” (EX1005, [0034]; *see also* [0008] (“In FIG. 3A, a semiconductor

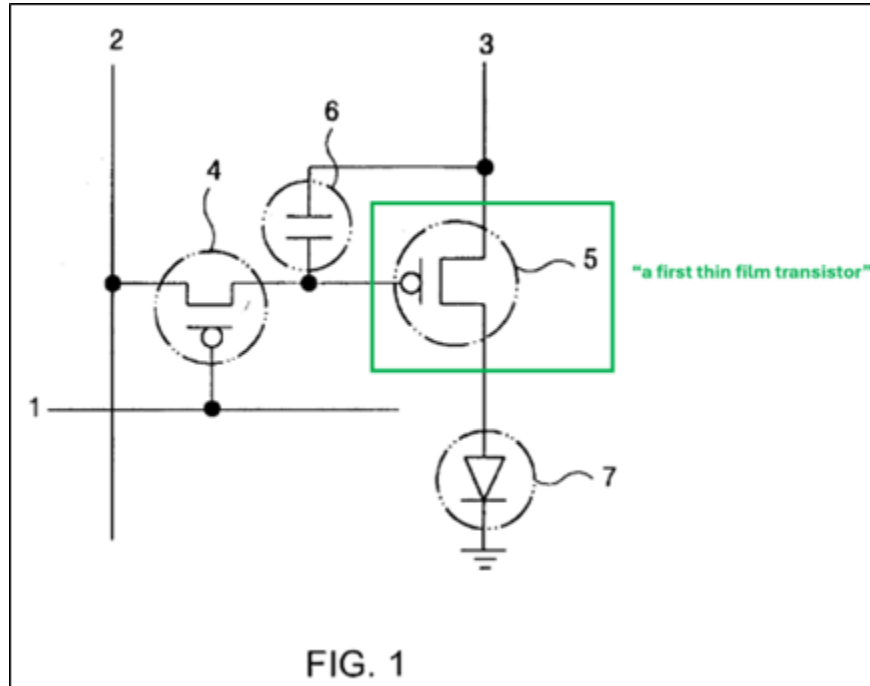
layer 17 and 18 are formed by forming a polycrystalline silicon layer and patterning it with a first mask on the substrate 10.”.)



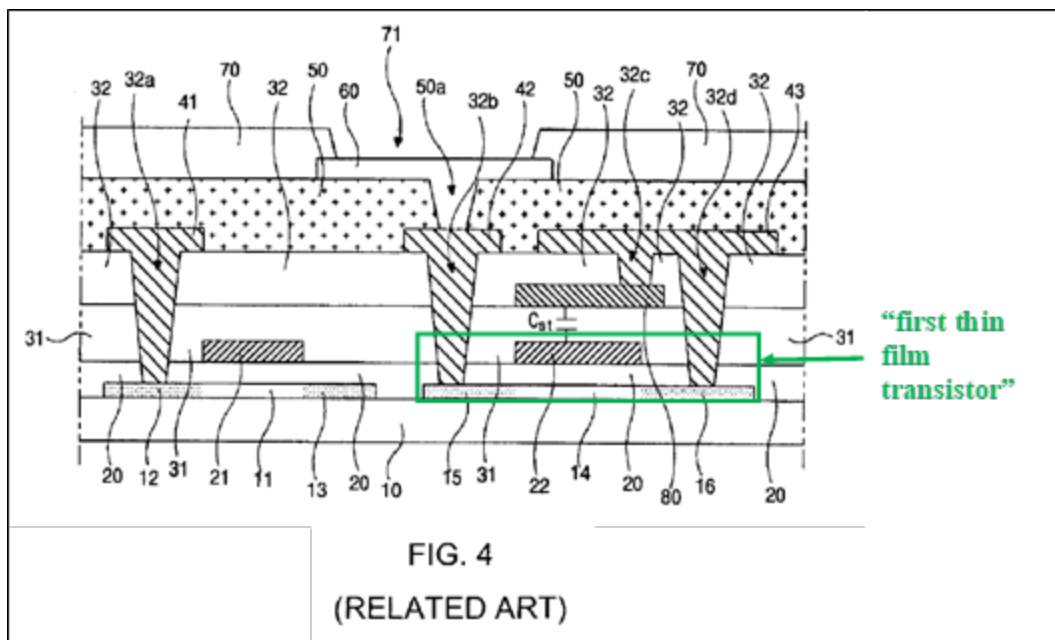
57. As another example, claim 1 of Park recites: “[a]n active matrix organic electro luminescent display (ELD) device, comprising: *a substrate.*” (EX1005, cl. 1 (emphasis added).)

- c. 1[b]: “a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”

58. Park discloses “a first thin film transistor.” For example, as shown below in annotated Figure 1, Park discloses “*a driving thin film transistor 5*” in an active matrix organic electro luminescent display device. (EX1005, [0006].)



59. Park's driving thin film transistor 5 is comprised of "the second gate electrode [22/]122, the second source electrode 173 and the second drain electrode 172." (EX1005, [0034]; *see also* [0007].) Figure 4 and 5 (annotated below) show the *driving thin film transistor 5*.

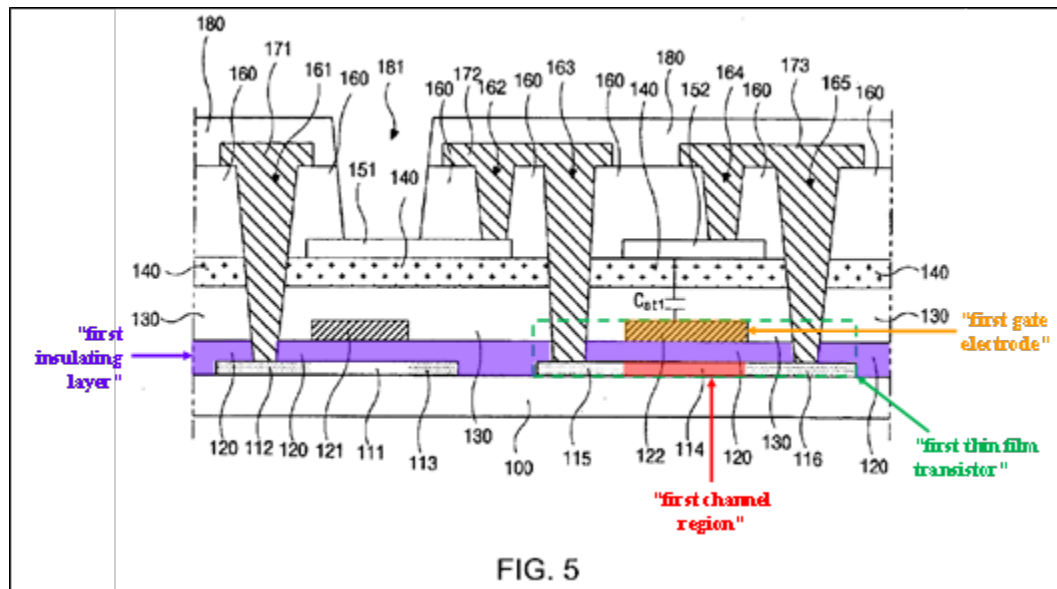
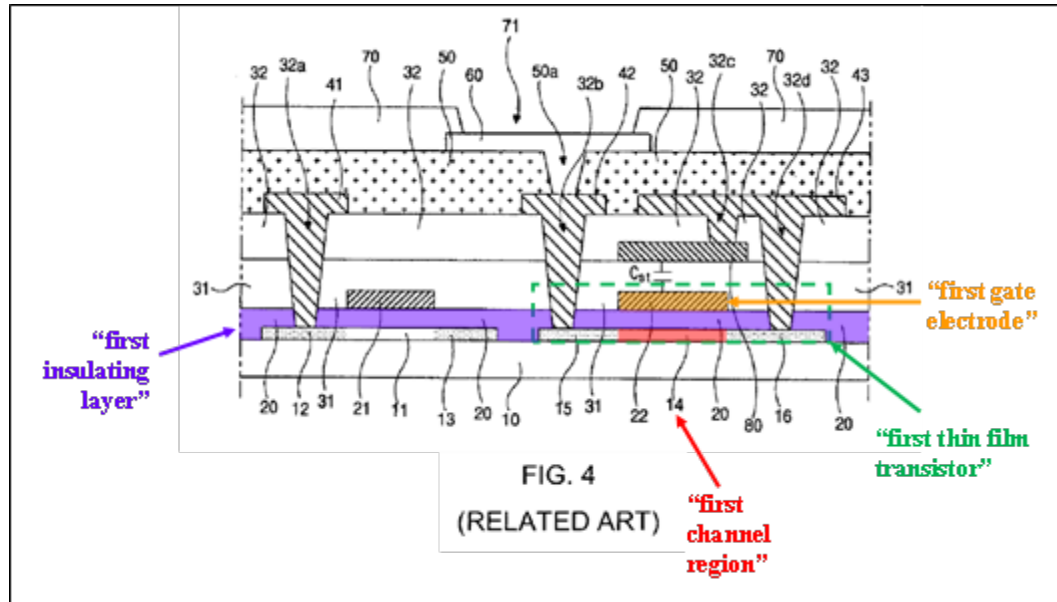




61. Figures 4 and 5 (annotated below) shows the active layer 14/114, the gate electrode 22/122, and the *insulating layer 20/120*. The figure also shows the *gate electrode 22/122* (“first gate electrode”) overlapping the *active layer 14/114*

(“first channel region”) allowing the gate electrode to shield the active layer

14/114 from being implanted with impurities. (EX1005, [0036].)



62. Park discloses the gate electrode 122 is “formed on the gate insulating layer 120 respectively over the active area 111 and 114.” (EX1005, [0034], [0007].) The gate electrode 122 is “formed by depositing material such as metal

on the *gate insulating layer 120* and patterning it with a second mask.” (EX1005, [0036] (emphasis added), [0007].) Further, as shown in Figures 4 and 5 (annotated above), the *gate electrode 22/122* and *active layer 14/114* are spaced apart from each other with the *insulating layer 20/120* (“first insulating layer”) therebetween.

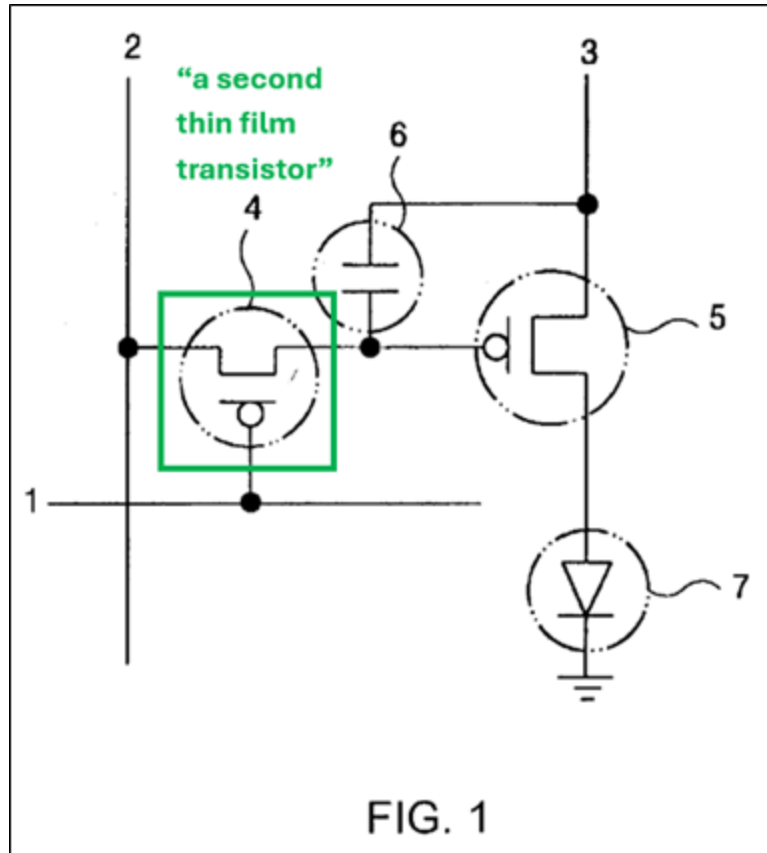
63. As another example, Park discloses in claim 1 that the active matrix organic electro luminescent display device comprises “first and second active layers formed of polycrystalline silicon on the substrate; . . . a gate insulating layer on the first and second active layers; first and second gate electrodes on the gate insulating layer.” (EX1005, cl. 1.) Similarly, claim 14 discloses a method to manufacture the active matrix organic electro luminescent display device includes “forming first and second semiconductor layers on a substrate with polycrystalline silicon; forming a gate insulating layer on the first and second semiconductor layers; forming first and second gate electrodes on the gate insulating layer” (EX1005, cl. 14.)

- d. **1[c]: “a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”**

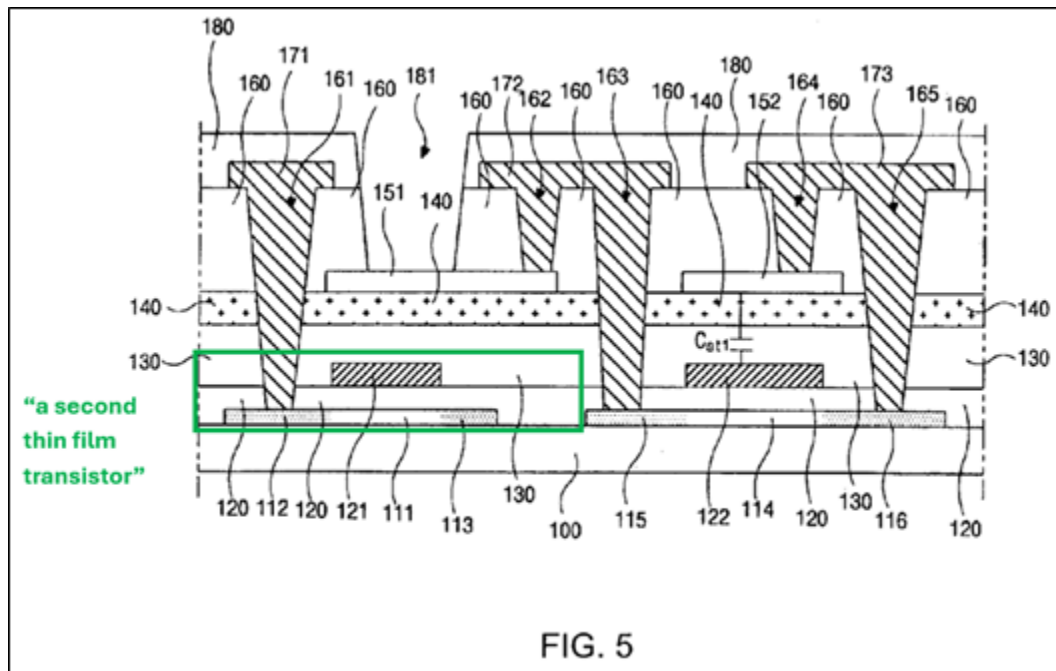
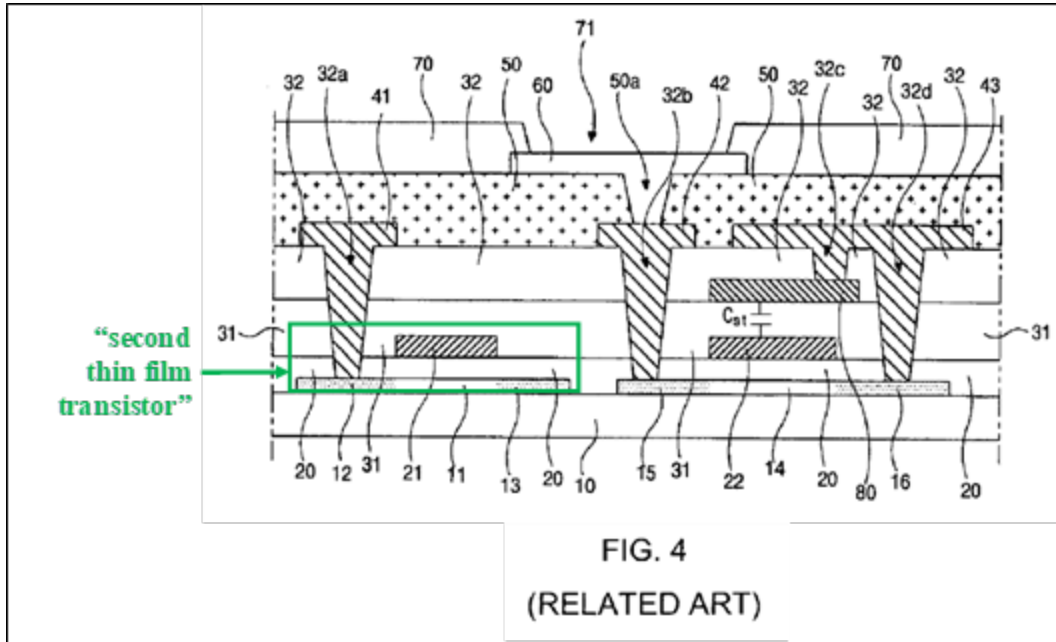
64. Park discloses “a second thin film transistor.” For example, as shown below in Figure 1 (annotated below), Park discloses *a switching thin film*

transistor 4 in an active matrix organic electro luminescent display device.

(EX1005, [0006].)



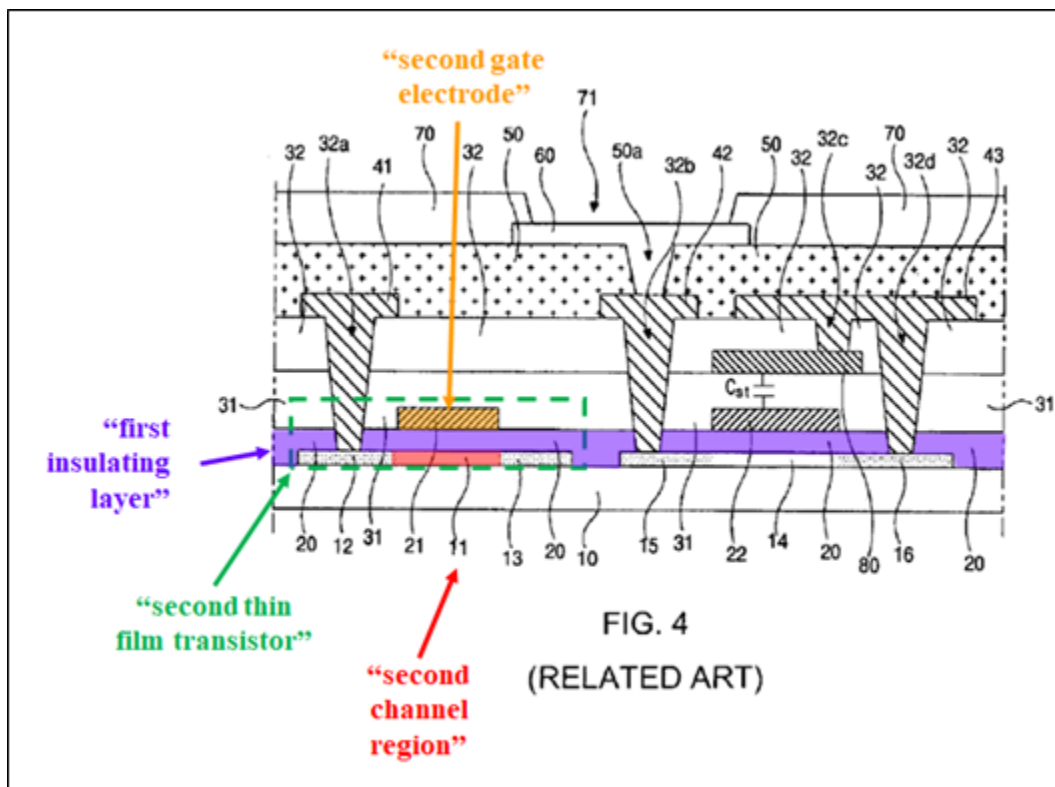
65. Park's switching thin film transistor 4 is comprised of "[t]he first gate electrode 121, the first source electrode 171 and the first drain electrode (not shown)." (EX1005, [0034], [0007].) Figures 4 and 5 (annotated below) show the switching thin film transistor 4.

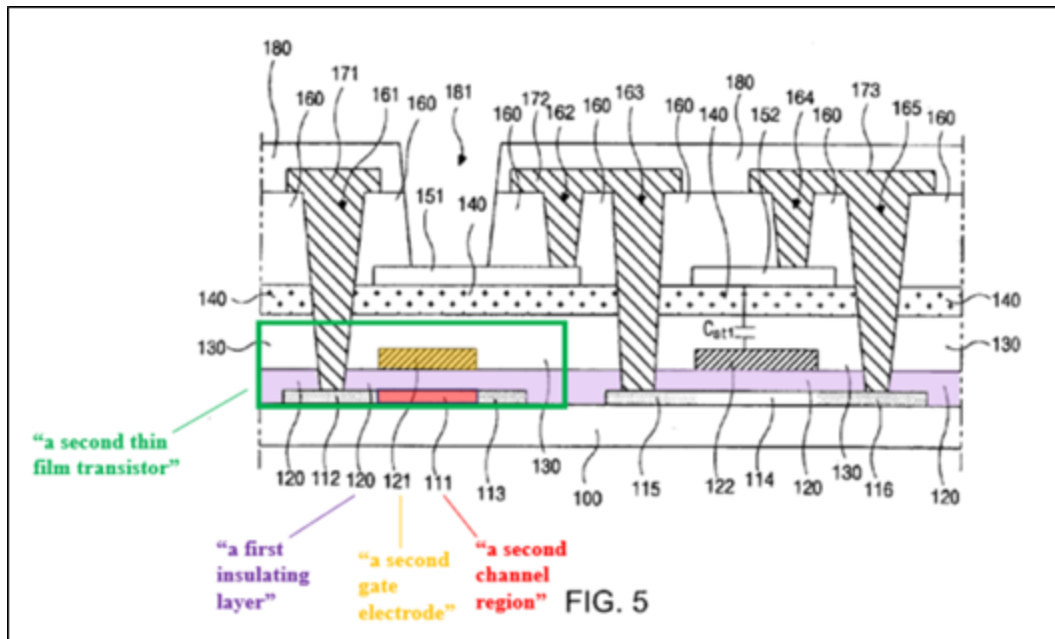


66. Park further discloses “a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween.” For example, Park

discloses the switching thin film transistor 4 including an active layer 11/111 (“second channel region”) and a gate electrode 21/121.

67. Figures 4 and 5 (annotated below) show the *active layer 11/111*, the *gate electrode 21/121*, and the *insulating layer 20/120*. The figures also show the gate electrode 21/121 (“second gate electrode”) overlapping the active layer 11/111 (“second channel region”).





68. Park discloses the gate electrode 121 is “formed on the gate insulating layer 120 respectively over the active area 111 and 114.” (EX1005, [0034]; *see also* [0007].) The gate electrode 21/121 is “formed by depositing material such as metal *on the gate insulating layer 120* and patterning it with a second mask.” (EX1005, [0036] (emphasis added), [0007].) Further, as shown in Figures 4 and 5 (annotated above), the gate electrode 21/121 and active layer 11/111 are spaced apart from each other with the *insulating layer 20/120* (“first insulating layer”) therebetween.

69. As another example, Park discloses in claim 1 that the active matrix organic electro luminescent display device comprises “first and second active layers formed of polycrystalline silicon on the substrate; . . . a gate insulating layer on the first and second active layers; first and second gate electrodes on the gate

insulating layer.” (EX1005, cl. 1.) Similarly, claim 14 discloses the method to manufacture the active matrix organic electro luminescent display device includes “forming first and second semiconductor layers on a substrate with polycrystalline silicon; forming a gate insulating layer on the first and second semiconductor layers; forming first and second gate electrodes on the gate insulating layer” (EX1005, cl. 14.)

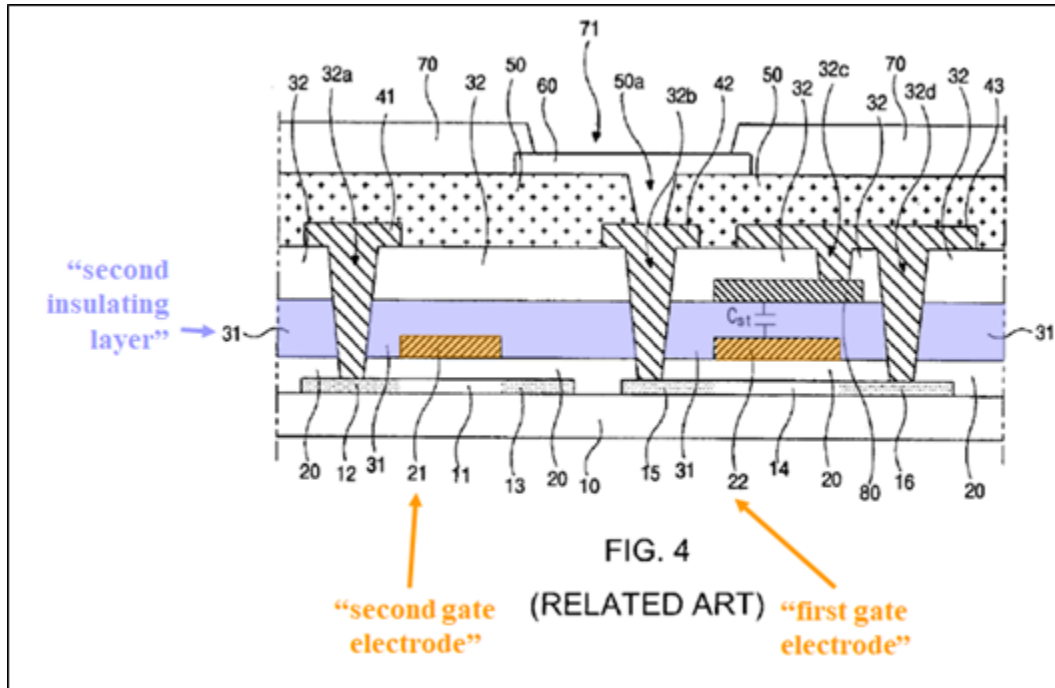
e. 1[d]: “a second insulating layer disposed on the first and second gate electrode;”

70. As shown for element 1[b], Park teaches a gate electrode 22/122 (“first gate electrode”). As shown for element 1[c], Park teaches a gate electrode 21/121 (“second gate electrode”).

71. Park discloses “a second insulating layer disposed on the first and second gate electrode.” For example, Park discloses an inter layer 31¹/130 and/or

¹ Park uses the reference number 30 to refer to the “inter layer” formed on the first and second gate electrodes 21 and 22 when describing Figure 2. (EX1005, [0007].) Park then uses the reference number 31 to refer to the “inter layer” formed on the first and second gate electrodes 21 and 22 when describing Figure 4. (EX1005, [0015].) A POSITA would have understood the inter layer 30 of Figure 2 is the same inter layer 31 of Figure 4 given that Park states “the active matrix

inter layer 140 that is “formed on the first and second gate electrodes 121 and 122.” (EX1005, [0034], [0007].) Park also discloses “the first and second inter layers 130 and 140 are sequentially formed on the first and second gate electrodes 121 and 122.” (EX1005, [0037], [0007].) Figures 4 and 5 (annotated below) show the *inter layer 31/130* and/or *inter layer 140* (“second insulating layer”) disposed on the *gate electrode 22/122* (“first gate electrode”) and *gate electrode 21/121* (“second gate electrode”).



organic electro luminescent display device of FIG. 4 has a similar structure with that of the above mentioned one of FIG. 2 except a storage capacitor portion.” (EX1005, [0015].)

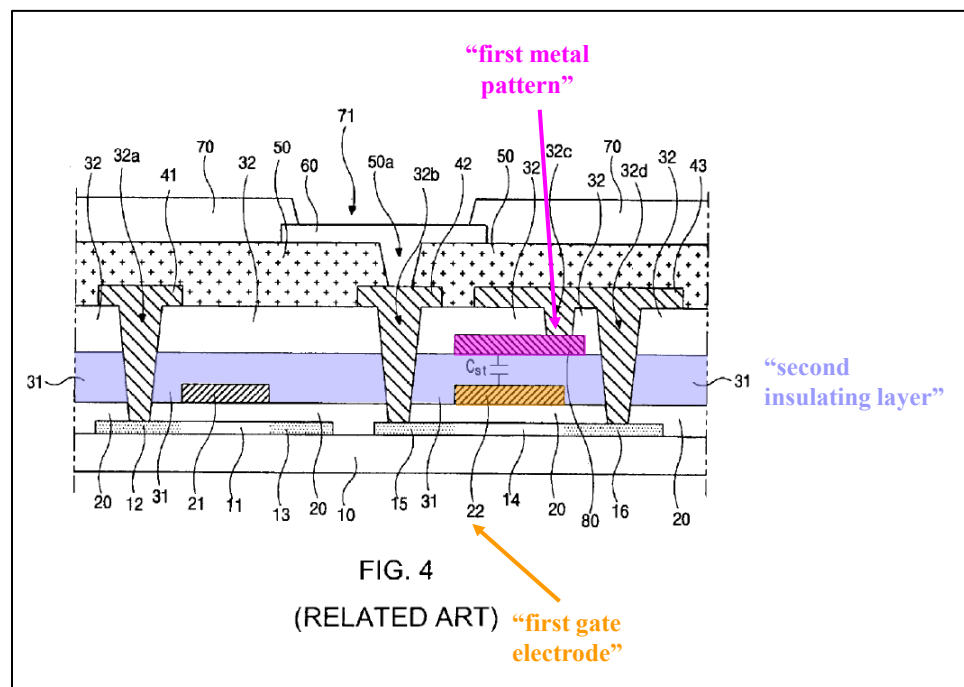


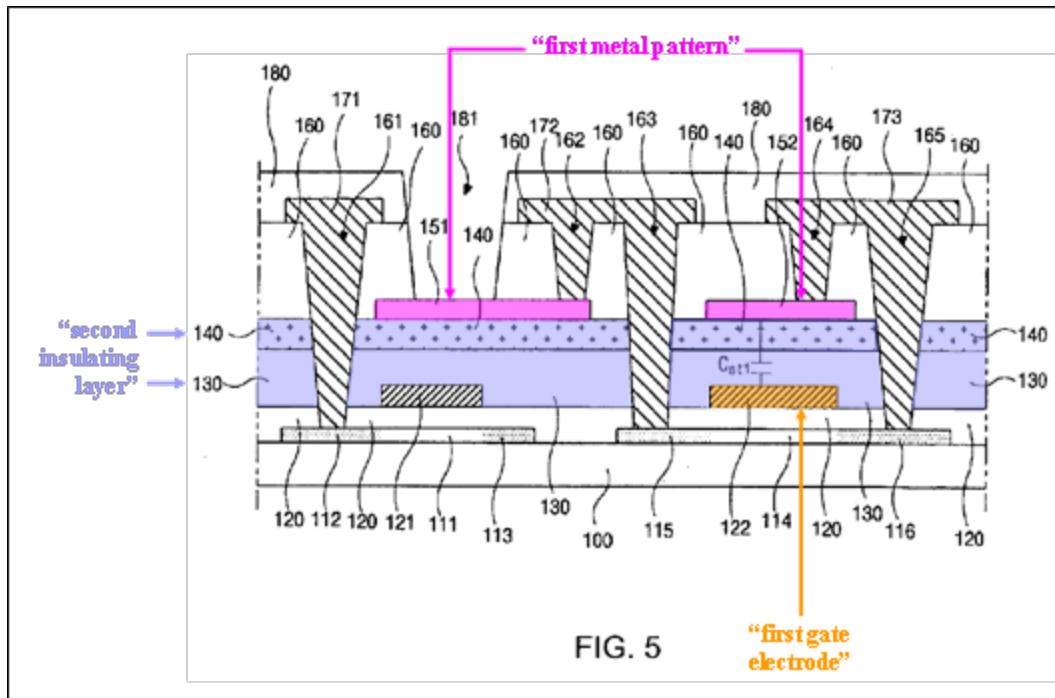
73. As shown for element 1[b], Park teaches a gate electrode 22/122 (“first gate electrode”). As shown for element 1[d], Park teaches an inter layer 31/130 and/or inter layer 140 (“second insulating layer”).

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EX1002 Pa

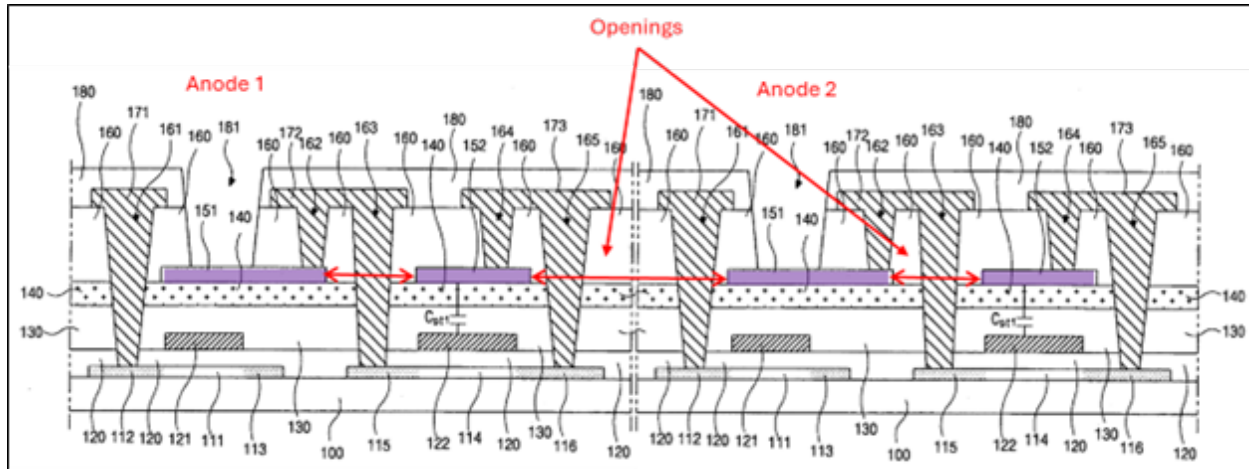
from each other with the second insulating layer therebetween.” For example, Park discloses the active matrix organic electro luminescent display device comprises an “*anode electrode 151 and a capacitor electrode 152* are formed of transparent conductive material such as indium tin oxide (ITO) on the second inter layer 140.” (EX1005, [0034] (emphasis added), [0015].) Figures 4 and 5 (annotated below) show the *anode electrode 151* and *capacitor electrode 80/152* (part of the “first metal pattern”) overlapping the *electrode 22/122* (“first gate electrode”).





75. As another example, in claim 1, Park discloses the active matrix organic electro luminescent display device comprises “an anode electrode and a capacitor electrode on the first inter layer.” (EX1005, cl. 1.) Further, in claim 2, Park discloses that “the capacitor electrode is overlapped with the second gate electrode and forms a storage capacitor together with the second gate electrode.” (EX1005, cl. 2.) To illustrate the relationship between the various layers and openings, Figure 5 has been reproduced twice below to show various components for two pixels. Anode 1 and anode 2 represent where two luminescent elements are located in relation to each other in the Park invention. The anodes are connected to the drain of the driving transistors through the contact holes 162/163 while the sources of the driving transistors are connected to the upper electrode of

the capacitor and to the power source through the contact holes 164/165. Between the anode electrode 151 and capacitor electrode 152 are openings as indicated.

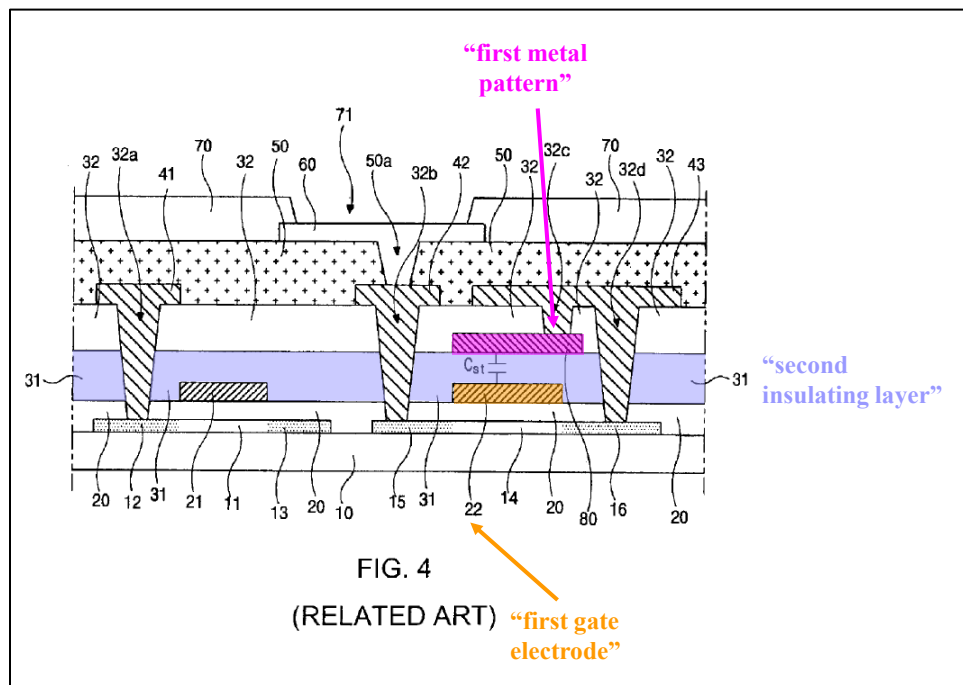


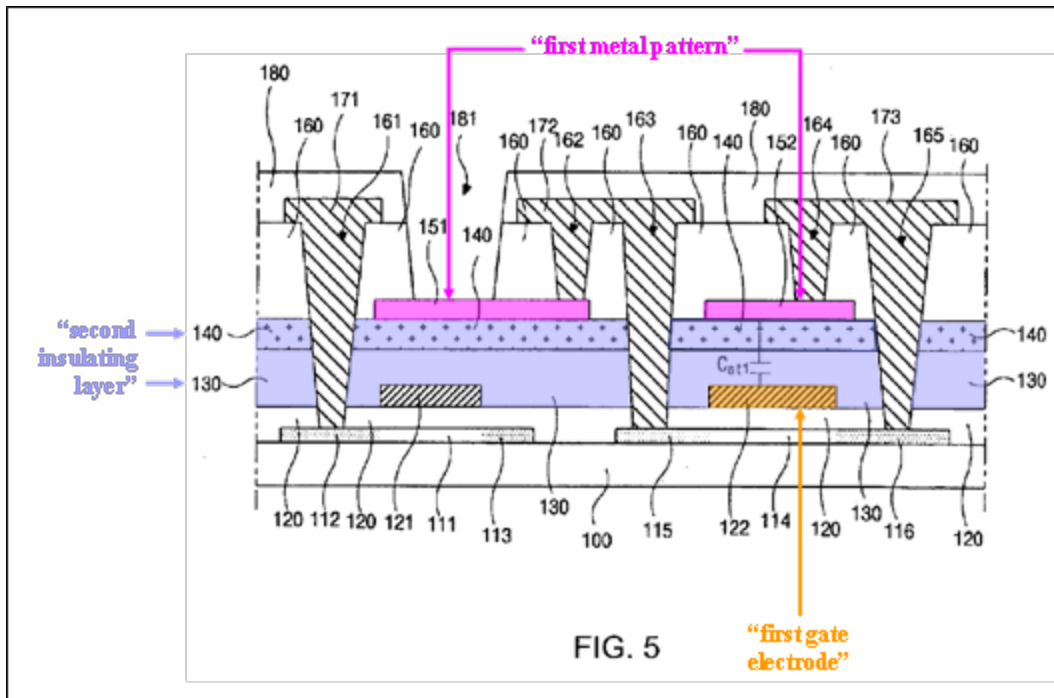
76. For Figure 4, Park discloses the “capacitor electrode 80 must be formed of metal material.” (EX1005, [0015].)

77. For Figure 5, it would have been obvious for the anode electrode 151 and capacitor electrode 152 to be a metal material, which is a conductive material since it carries current to the OLED or capacitor. Park discloses that these layers “are formed of a transparent conductive material *such as* indium tin oxide.” (EX1005, [0034] (emphasis added).) A POSITA would understand that another transparent conductive material is thin silver, for example. It was known to use metal materials for the anode electrode and/or capacitor electrode. Depending on the OLED configuration, it is sometimes advantageous to use a transparent conductive material such as low-conductivity Indium Tin Oxide or thin silver for the anode electrode 151 (EX1005, [0034]), e.g., bottom emitting OLED. In other

configurations, it is advantageous to use a reflective metal for the anode electrode 151, e.g., top-emitting OLED. In either case, the same material can be used for the capacitor electrode 152 because both are low-conductivity materials. For example, Park '028 teaches “[t]he cathode 134 is made of aluminum (Al) or Al alloy of high reflectance. For the organic EL device of top emission type, the materials of the anode and the cathode may be exchanged.” (EX1010, [0069], [0020].)

78. Figures 4 and 5 (annotated below) also show the anode electrode 151 and capacitor electrode 80/152 (part of the “first metal pattern”) and gate electrode 22/122 (“first gate electrode”) being spaced apart from each other with inter layer 31/130 and/or inter layer 140 (“second insulating layer”) therebetween.





79. Park provides additional disclosures that show that it teaches “the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween”:

- interlayer 130 “[is] sequentially formed on the first and second gate electrodes 121 and 122.” (EX1005, [0034]; *see also* [0015].)
- “[t]he anode electrode 151 and the capacitor electrode 152 are formed by depositing transparent conductive material *on the second inter layer 140* and patterning it with a third mask.” (EX1005, [0037] (emphasis added).)

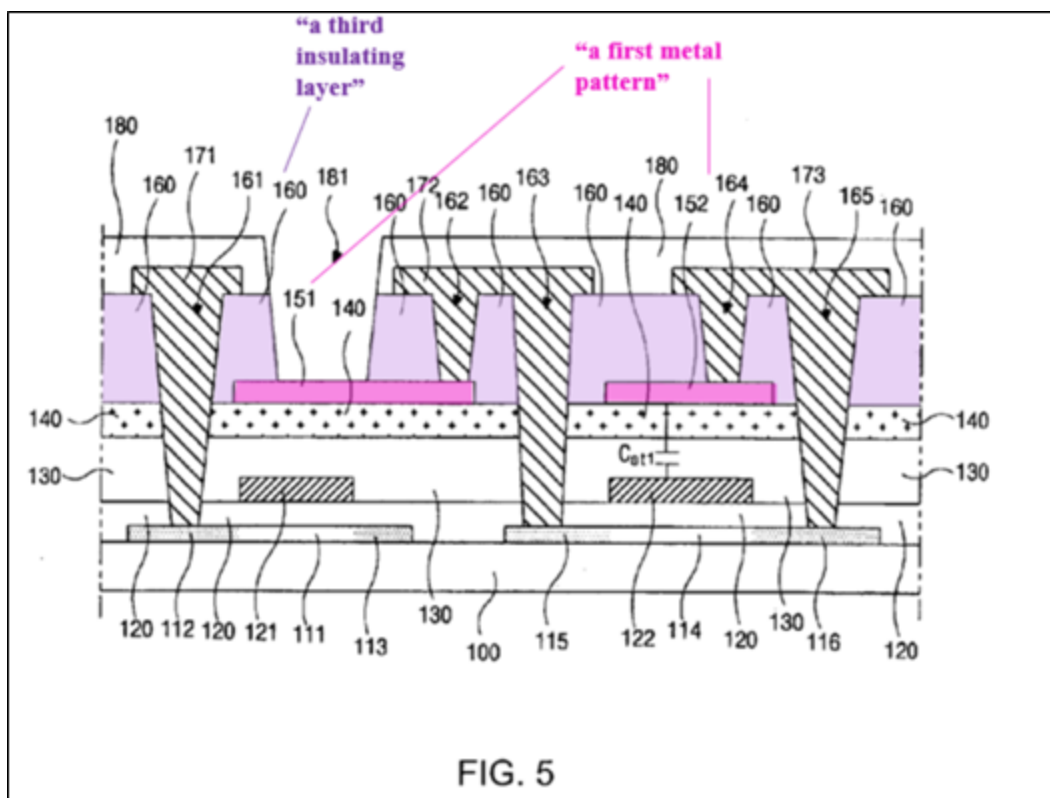
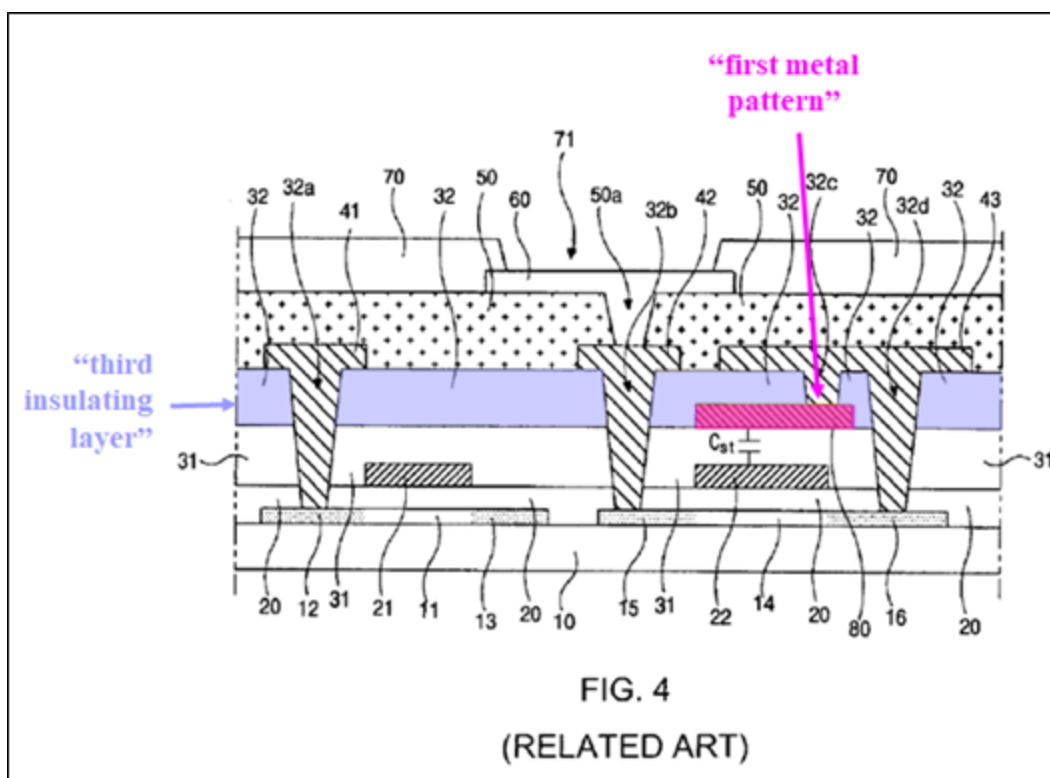
80. As another example, in claim 14, Park discloses the method of manufacturing the active matrix organic electro luminescent display device includes “forming an anode electrode on the first interlayer; forming a capacitor

electrode on the first inter layer.” (EX1005, cl. 14.) Further, in claims 15 and 16, Park discloses that “the capacitor electrode is overlapped with the second gate electrode . . .” and “the capacitor electrode forming is performed in a same process as a process for forming the anode electrode.” (EX1005, cls. 15, 16.)

g. 1[f]: “a third insulating layer disposed on the first metal pattern; and”

81. As shown for element 1[e], Park teaches an anode electrode 151 and a capacitor electrode 80/152 (part of the “first metal pattern”).

82. Park discloses “a third insulating layer disposed on the first metal pattern.” For example, Park discloses a “*first passivation layer 160 is formed of material such as silicon oxide (SiO₂) on the anode electrode 151 and the capacitor electrode 152.*” (EX1005, [0034] (emphasis added), [0015].) Park also discloses that “the first passivation layer 160 is then formed on the anode electrode 151 and the capacitor electrode 152 by depositing material such as silicon oxide (SiO₂).” (EX1005, [0038].) Figures 4 and 5 (annotated below) show the *inter layer 32/passivation layer 160* (“third insulating layer”) disposed on the *anode electrode 151* and the *capacitor electrode 80/152* (part of the “first metal pattern”).



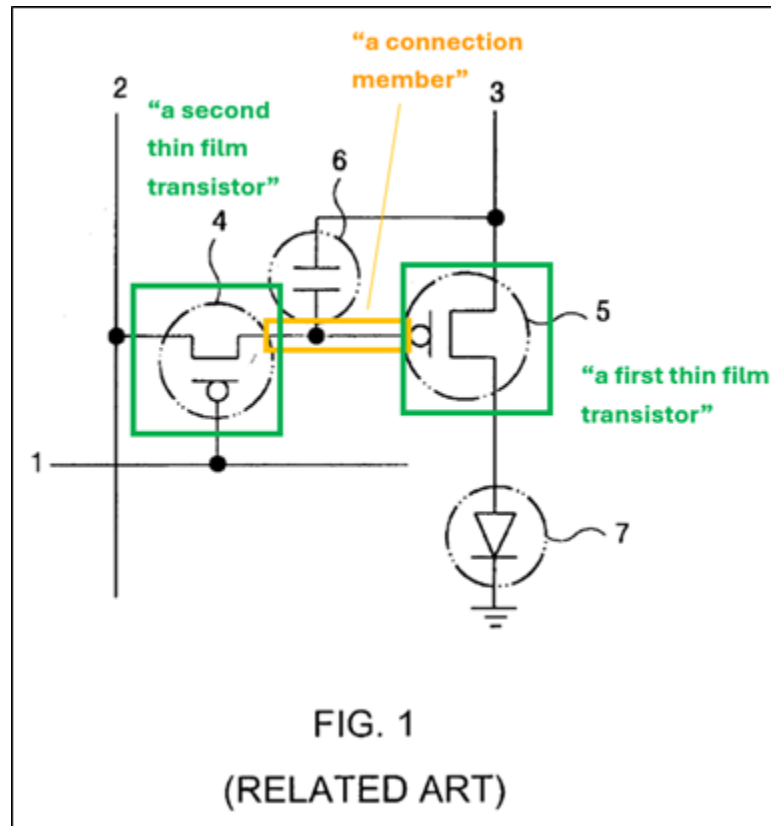
83. As another example, Park discloses in claim 1 that the active matrix organic electro luminescent display device comprises “a first passivation layer on the anode electrode and the capacitor electrode.” (EX1005, cl. 1.) Similarly, in claim 14, Park discloses “forming a first passivation layer on the anode electrode and the capacitor electrode, ...” (EX1005, cl. 14.)

h. 1[g]: “a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor.”

84. As shown for element 1[f], Park teaches an inter layer 32/passivation layer 160 (“third insulating layer”). As shown for element 1[b], Park teaches a gate electrode 22/122 (“first gate electrode”), which is the gate electrode of the driving thin film transistor 5 (“first thin film transistor”). As shown for element 1[c], Park teaches a switching thin film transistor 4 (“second thin film transistor”).

85. Park discloses a “connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor.” Figure 1 of Park (annotated below) shows a circuit. Park explains that the “drain electrode of the switching thin film transistor 4 *is connected to* a gate electrode of the thin, film transistor 5” and a “storage capacitor 6 *is connected to* the gate electrode and the source electrode of the driving thin film resistor 5.” (EX1005, [0006] (emphasis added).) The figure shows the drain of the *switching*

thin film transistor 4 and gate of electrode of the *driving thin film transistor 5* are electrically connected by a *connection member*.



86. Park's connection member is disposed on the inter layer 32/passivation layer 160 ("third insulating layer"). For example, Park discloses "*a first drain electrode (not shown), which is connected to the first drain region 113, and a power line (not shown), which is connected to the second source electrode 173, are also formed on the first passivation layer 160.*" (EX1005, [0034] (emphasis added); see also [0011].) Park provides additional disclosures that show that it teaches "a connection member disposed on the third insulating layer":

- “a first drain electrode (not shown), which is connected to the first drain region 113, and a power line (not shown), which is connected to the second source electrode 173, are also formed on the first passivation layer 116 (sic²).” (EX1005, [0039] (emphasis added).)
- “the drain region of the switching thin film transistor, i.e., the first drain region 113, which is electrically connected to the gate electrode of the driving thin film transistor.” (EX1005, [0041].)

87. Park discloses “the first passivation layer 160 is then formed on the anode electrode 151 and the capacitor electrode 152 by depositing material such as silicon oxide (SiO₂).” (EX1005, [0038].) A POSITA would have known that

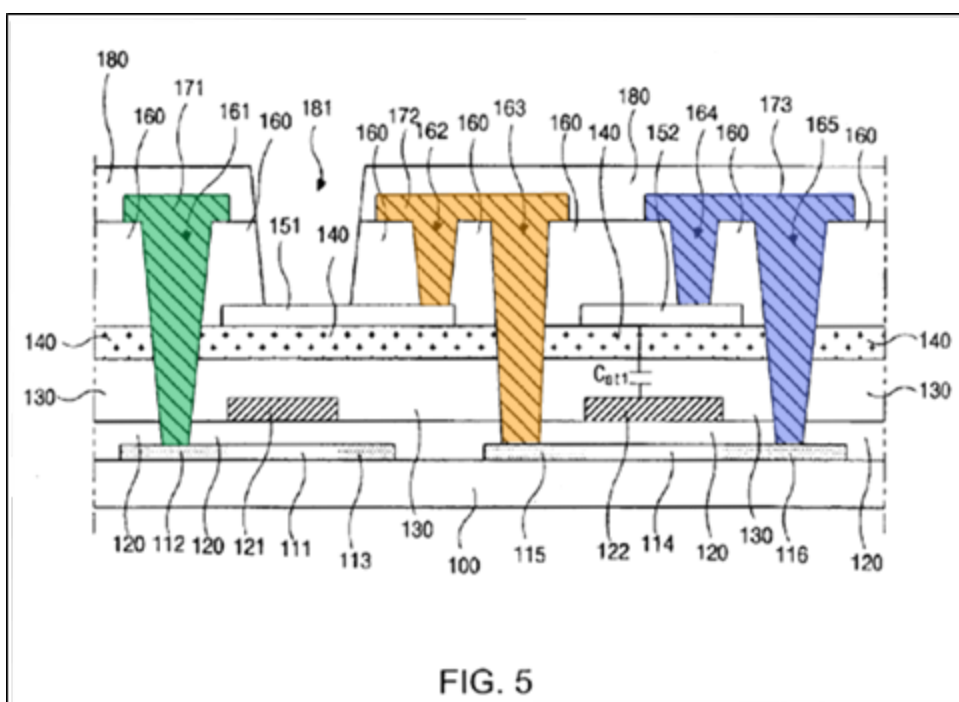
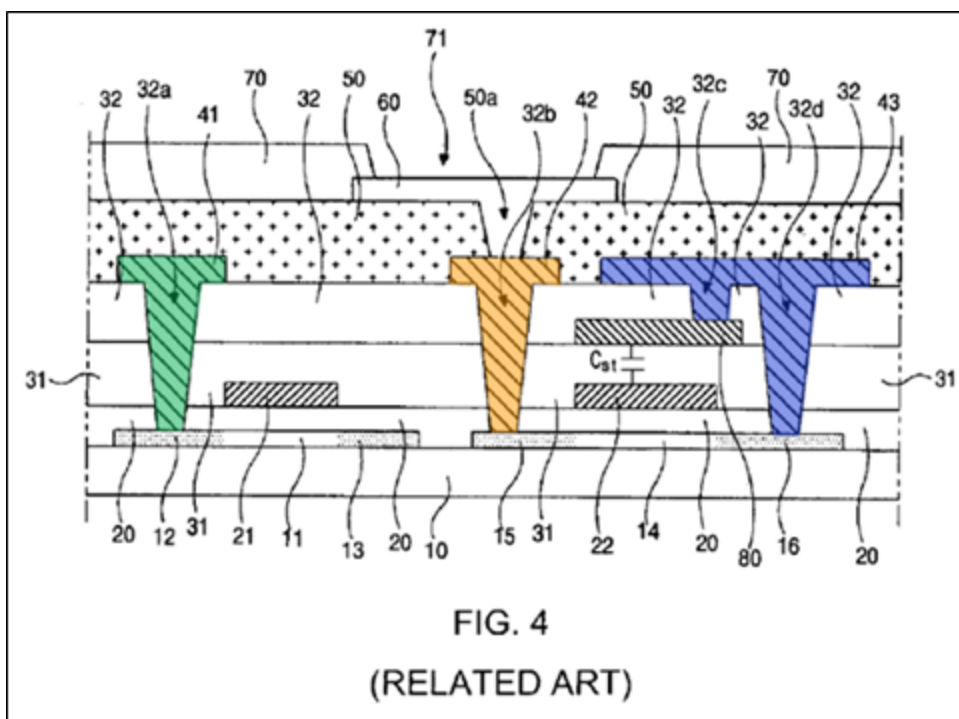
² A POSITA would have understood that “first passivation layer 116” in [0039] of Park should read “first passivation layer 160.” The paragraph discusses the “first source electrode 171, the second drain electrode 172 and the second source electrode 173 are formed by depositing conductive material such as metal on the first passivation layer.” (EX1010, [0039].) The next sentence that follows states: “[t]hough it is not shown in the figure, a first drain electrode (not shown) . . . *[is] also formed on the first passivation layer 116.*” (*Id.*) This shows that the second sentence references the same “first passivation layer 160.”

silicon oxide SiO₂ is an insulating layer, and thus, would have understood inter layer 32/passivation layer 160 is an insulating layer.

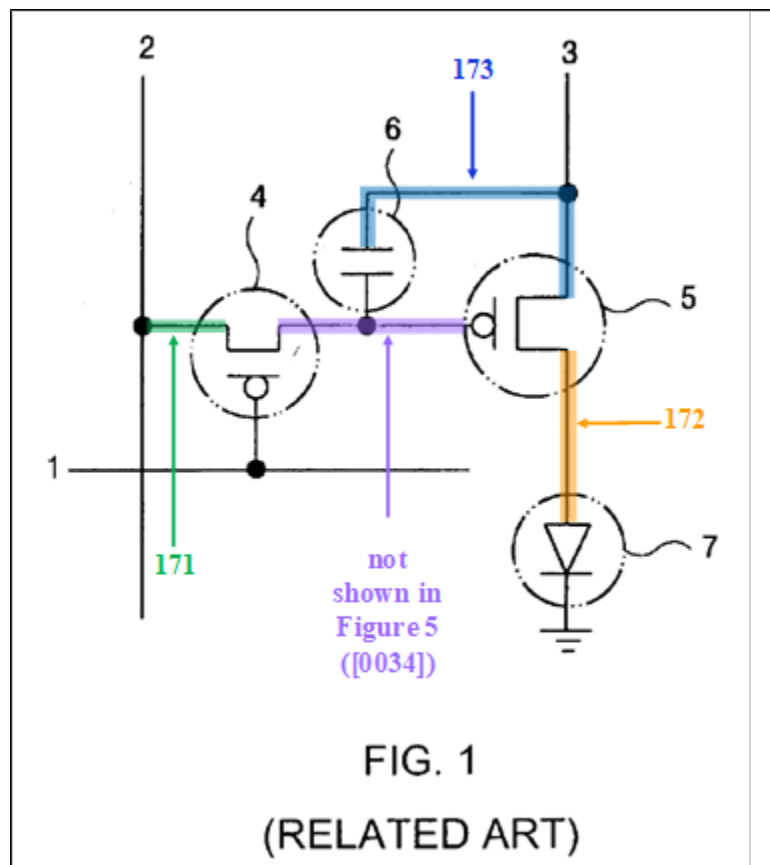
88. Park discloses describes the structure of the source and drain electrodes for Figure 5 (Figure 6E shows fabrication steps for Figure 5): “[i]n FIG. 6E, the first source electrode 171, the second drain electrode 172 and the second source electrode 173 are formed by depositing conductive material such as metal on the first passivation layer 160 and patterning it with a fifth mask.” (EX1005, [0039].) Then, Park states “[t]hough it is not shown in the figure, a first drain electrode (not shown), which is connected to the first drain region 113, and a power line (not shown), which is connected to the second source electrode 173, are also formed on the first passivation layer 116. The second source electrode 173 may be extended from the power line (not shown) or may be formed of a portion of the power line.” (EX1005, [0039].) A POSITA would have understood Park’s Figure 5 structure to represent the structure of the “first drain electrode” because it explains that it is not shown in the figure and then describes the connection and formation on the first passivation layer 160, which is like the drain electrodes shown in Figure 5. Further, the structure of the source/drain electrodes in Figure 4 is similar to the structure of the source/drain electrodes in Figure 5.

89. Figures 4 and 5 show (annotated below) and the passages in [0039] teach the source and drain electrodes, including the first drain electrode

(“connection member”) being disposed on the inter layer 32/passivation layer 160 (“third insulating layer”).



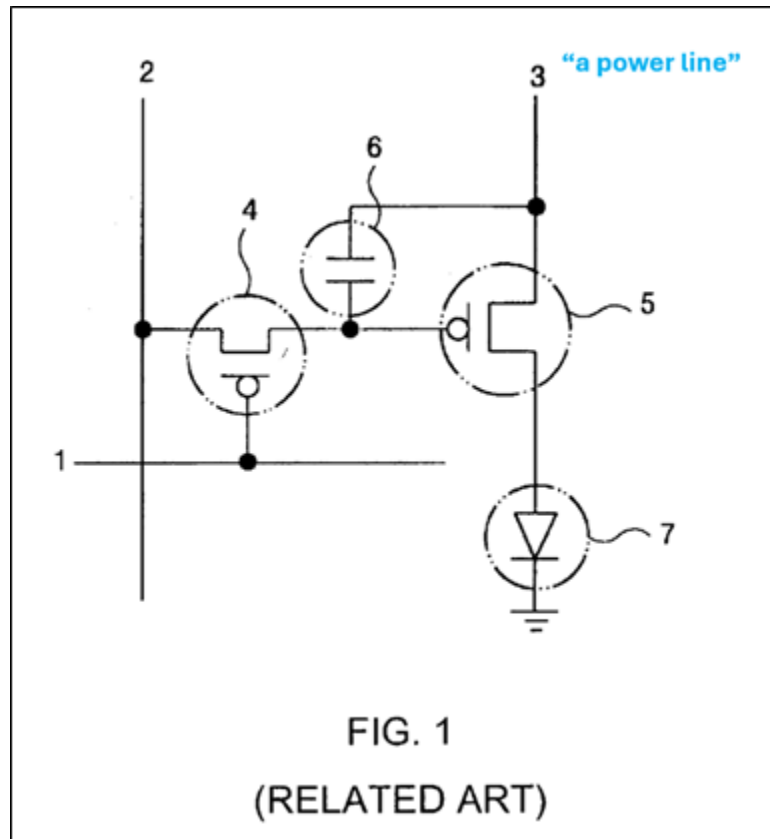
90. Figure 1 (annotated below) shows the connections of the pixel circuit that correspond to the source/drain electrodes 171, 172, and 173 of Figures 4 and 5 (above). As shown in the figures above, Park's source/drain electrodes 171, 173, and 175 are on the inter layer 32/passivation layer 160 ("third insulating layer"). Further, Figures 4 and 5 (annotated below) represent the structures of the first drain electrode that is indicated as "not shown."



3. Claim 11: “The TFT array substrate of claim 1, further comprising a driving voltage line on the third insulating layer, wherein the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer.”

91. Park teaches claim 1 as shown above. As shown for element 1[e], Park teaches an anode electrode 151 and a capacitor electrode 80/152 (part of the “first metal pattern”). As shown for element 1[f], Park teaches an inter layer 32/passivation layer 160 (“third insulating layer”).

92. Park teaches “a driving voltage line on the third insulating layer, wherein the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer.” For example, Figure 1 (annotated below) of Park shows a circuit comprising a “source electrode of the driving thin film transistor 5 [] connected to *a power line 3*.” (EX1005, [0006] (emphasis added).) A POSITA would have understood that a power line is a “driving voltage line” because it delivers a voltage to the light emitting diode (LED) 7. (EX1005, [0006].)



93. Park discloses the active matrix organic electro luminescent display device contains “a first drain electrode (not shown), which is connected to the first drain region 13/113, and *a power line (not shown), which is connected to the second source electrode [43/]173, are also formed on the [inter layer 32/]first passivation layer 160.* The second source electrode [43/]173 may be extended from the power line (not shown) or may be formed of a portion of the power line.” (EX1005, [0034] (emphasis added); *see also* [0007].)

94. Park provides additional disclosures that show that it teaches “a driving voltage line on the third insulating layer”:

- the active matrix organic electro luminescent display device comprises “a power line on the first passivation layer.” (EX1005, cl. 1.)
- “A manufacturing method for an active matrix organic electro luminescent display (ELD) device, comprising: . . . forming a power line on the first passivation layer.” (EX1005, cl. 14.)
- “a first drain electrode (not shown), which is connected to the first drain region 113, and a power line (not shown), which is connected to the second source electrode 173, are also formed on the first passivation layer 116³ (sic). The second source electrode 173 may be extended from the power line (not shown) or may be formed of a portion of the power line.” (EX1005, [0039] (emphasis added).)

95. Park further discloses, that “[t]he second source electrode 173 *is connected to the capacitor electrode 152* and the second source region 110⁴

³ As discussed for Footnote 1, a POSITA would have understood “first passivation layer 116” should instead read “first passivation layer 160.”

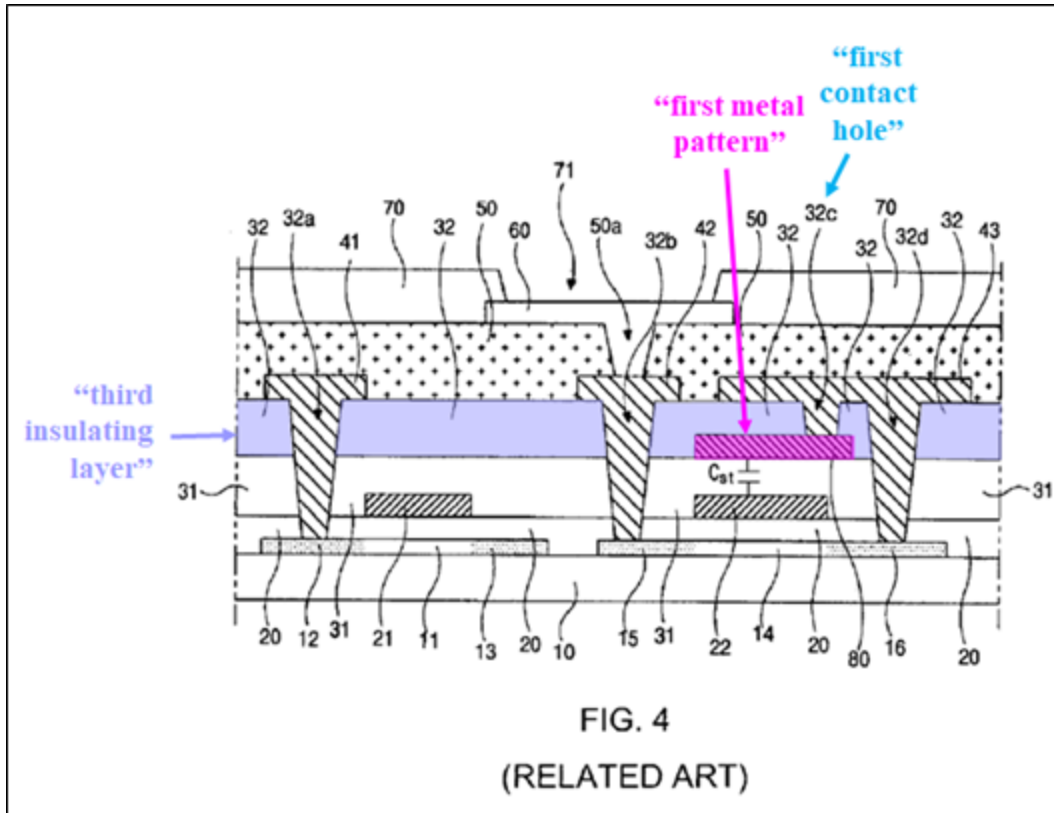
⁴ A POSITA would have understood that “second source region 110” in [0039] of Park should read “second source region 116.” The passage refers to Figure 6E, which shows a second source region 116. Further, [0034] uses “116” to refer the “second source region.”

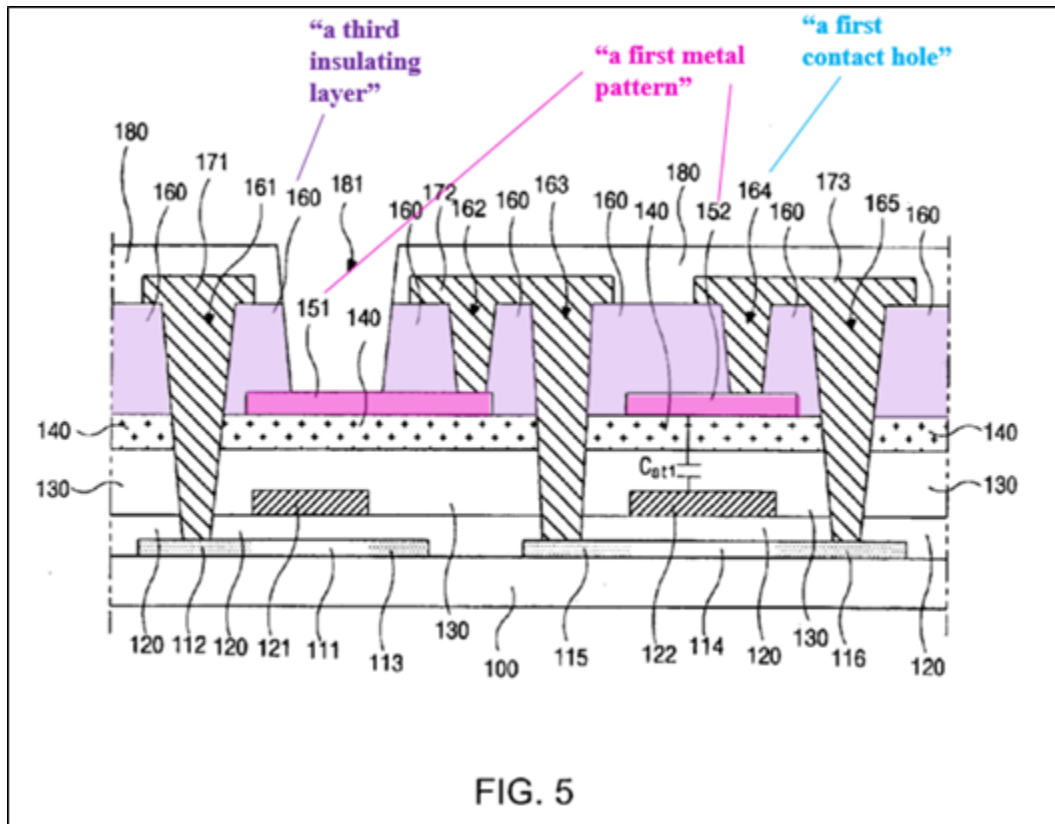
through the fourth and fifth *contact holes 164* and 165.” (EX1005, [0039]; *see also* [0015].) Referring to Figure 5, “[t]he second source electrode 173 is connected to the capacitor electrode 152 and the second source region 116 through the fourth and fifth contact holes 164 and 165.” (*Id.*) (EX1005, [0034]; *see also* [0038] (“The first, second., third, *fourth* and fifth *contact holes* 161, 162, 163, *164*, and 165 *are formed by patter[n]ing* the gate insulating layer 120, the first and second inter layers 130 and 140 and *the first passivation layer 160 with a fourth mask.*” (emphases added))); *see also* [0015].) A POSITA would have understood patterning a layer with a mask creates a contact hole of the layer.

96. As another example, Park discloses in claim 1 that “the power line and the capacitor electrode and the second drain electrode being connected to the second drain region and the anode electrode.” (EX1005, cl. 1; *see also* cl. 14 (“the power line and the capacitor electrode and the second drain electrode being connected to the second drain region and the anode electrode”).) Hence, Park teaches the power line 3 (“driving voltage line”) is connected to capacitor electrode 80/152 (part of the “first metal pattern”) through contact hole 164 (“first contact hole”) of the inter layer 32/passivation layer 160 (“third insulating layer”).

97. Figures 4 and 5 (annotated below) show the *contact hole 32c/164* (“first contact hole”) connecting to the *capacitor electrode 80/152* (part of the

“first metal pattern”) though the *inter layer 32/passivation layer 160* (“third insulating layer”).



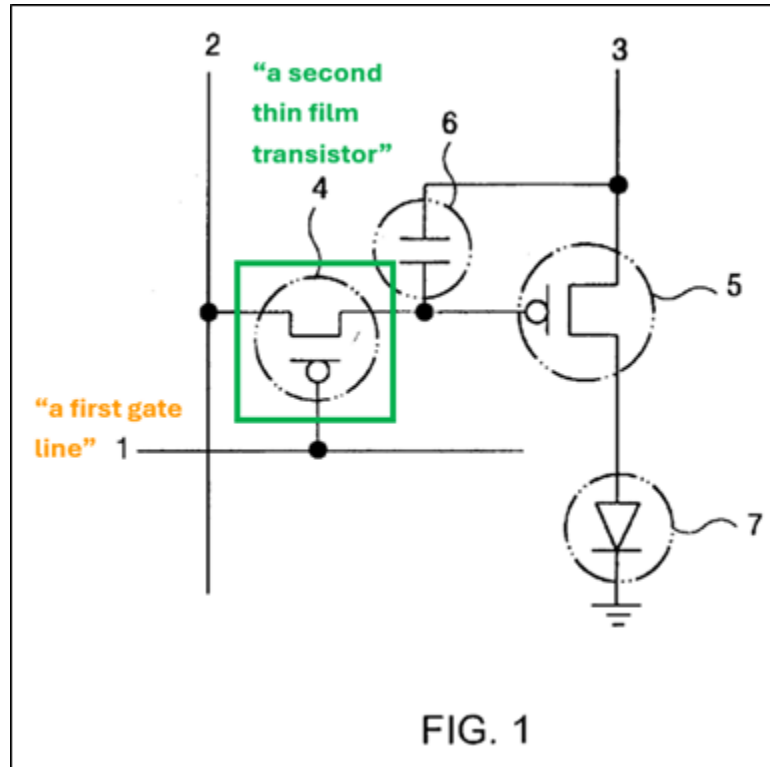


4. Claim 14: “The TFT array substrate of claim 1, further comprising a first gate line electrically connected to the second gate electrode.”

98. Park teaches claim 1 as shown above. As shown for element 1[c], Park teaches a gate electrode 21/121 (“second gate electrode”). The gate electrode 21/121 is of the switching thin film transistor 4. (EX1005, [0034]; *see also* [0007].)

99. Park teaches “a first gate line electrically connected to the second gate electrode.” For example, Park discloses that a “gate electrode of the switching thin film transistor 4 is connected to the gate lane [sic] 1.” (EX1005, [0006].) Figure 1

(annotated below) shows the *gate line 1* (“first gate line”) electrically connected to the gate electrode of the *switching thin film transistor 4*.

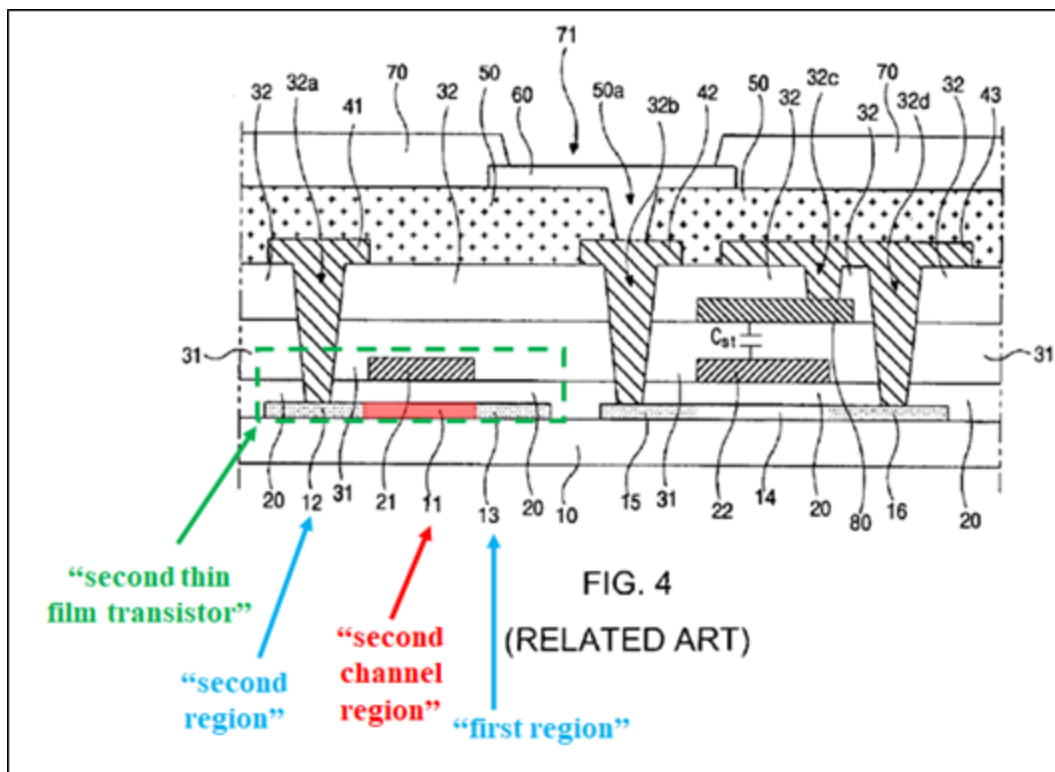


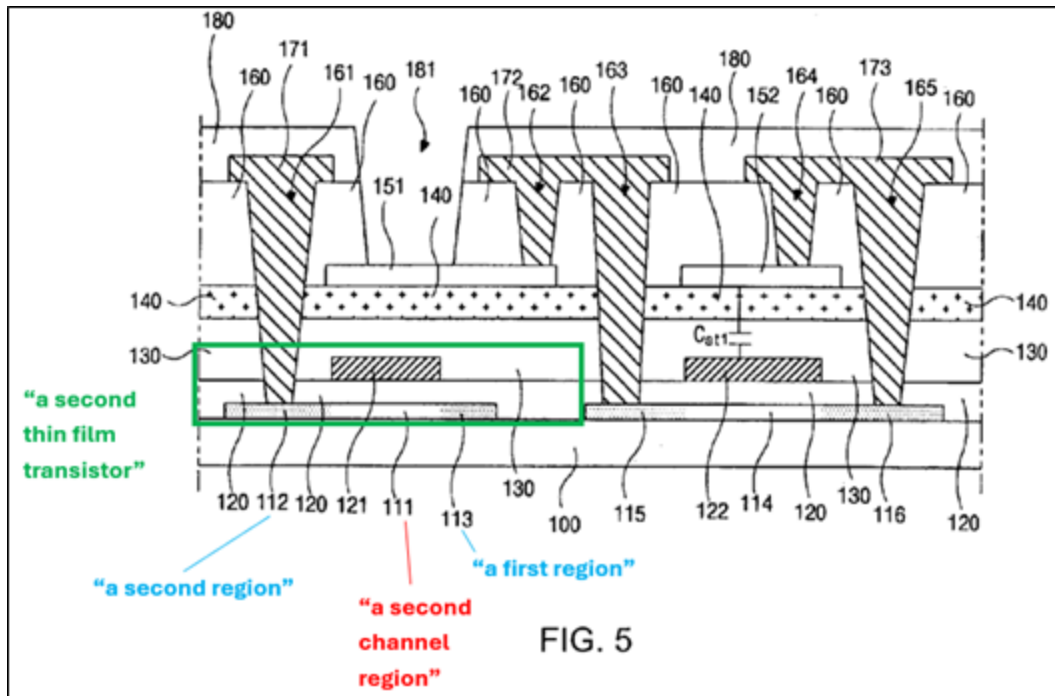
5. Claim 15

- a. 15[a]: “The TFT array substrate of claim 14, wherein the second thin film transistor further comprises a first region adjacent to a side of the second channel region and a second region adjacent to another side of the second channel region, and”

100. Park teaches claim 14 as shown above. As shown for element 1[c], Park teaches a switching thin film transistor 4 (“second thin film transistor”) comprising an active layer 11/111 (“second channel region”).

101. Park teaches “the second thin film transistor further comprises a first region adjacent to a side of the second channel region and a second region adjacent to another side of the second channel region.” For example, Park’s switching thin film transistor 4 comprises “a first source region [12/]112 and a first drain region [13/]113.” (EX1005, [0034]; *see also* [0007].) As shown in Figures 4 and 5 (annotated below), the *drain region 13/113* is adjacent to a side of the *active layer 11/111*. The figures also show the *source region 12/112* is adjacent to another side of the *active layer 11/111*. (EX1005, [0009], [0036].)





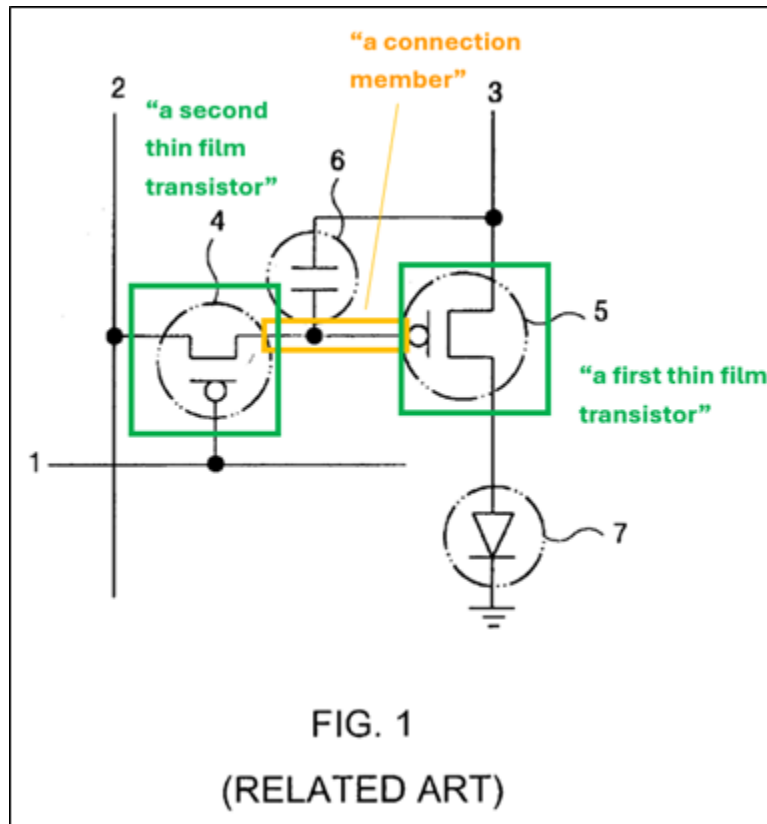
102. As another example, Park discloses the manufacturing method for an active matrix organic electro luminescent display device comprises the step of “forming first source and drain regions and second source and drain regions by inputting ions into the first and second semiconductor layer using the first and second gate electrodes as a mask.” (EX1005, cl. 14.) A POSITA would have understood the source region 12/112 and drain region 13/113 are adjacent to the active area 11/111 as they are defined by inputting ions into the uncovered semiconductor layer. (EX1005, [0036].)

- b. **15[b]: “the first region is electrically connected to the first gate electrode via the connection member.”**

103. As shown for element 15[a], Park teaches a drain region 13/113 (“first region”). As shown for element 1[b], Park teaches a gate electrode 22/122 (“first

gate electrode”). As shown for element 1[g], Park teaches a member connecting the drain of the switching thin film transistor 4 and the gate of electrode of the driving thin film transistor 5 (“connection member”).

104. Park discloses “the first region is electrically connected to the first gate electrode via the connection member.” For example, Park discloses that “[t]hough it is not shown in the figure, the second gate electrode [22/]122 is electrically connected to the first drain region [13/]113.” (EX1005, [0034]; *see also* [0007].) Park further discloses that the “first drain electrode (not shown), which is connected to the first drain region [13/]113, ... The second source electrode [43/]173 is connected to the capacitor electrode [80/]152 . . . The capacitor electrode [80/]152 forms a storage capacitor C_{st1} together with the second gate electrode [22/]122.” (*Id.*) Figure 1 (annotated below) shows the drain region 13/113 (“first region”) of the *switching thin film transistor 4* is electrically connected to the gate electrode (“first gate electrode”) of the *driving thin film transistor 5* via the *connection member*.



105. As another example, Park discloses that “[t]he drain region of the switching thin film transistor, i.e., the first drain region 113” “is electrically connected to the gate electrode of the driving thin film transistor.” (EX1005, [0041].) Park also discloses the manufacturing method for an active matrix organic electro luminescent display device comprises the step of “forming first source and drain regions and second source and drain regions by inputting ions into the first and second semiconductor layer using the first and second gate electrodes as a mask.” (EX1005, cl. 14.)

B. Claims 2-6, 22-24, And 27 Are Obvious Over Park And Zhan

1. Summary of Zhan

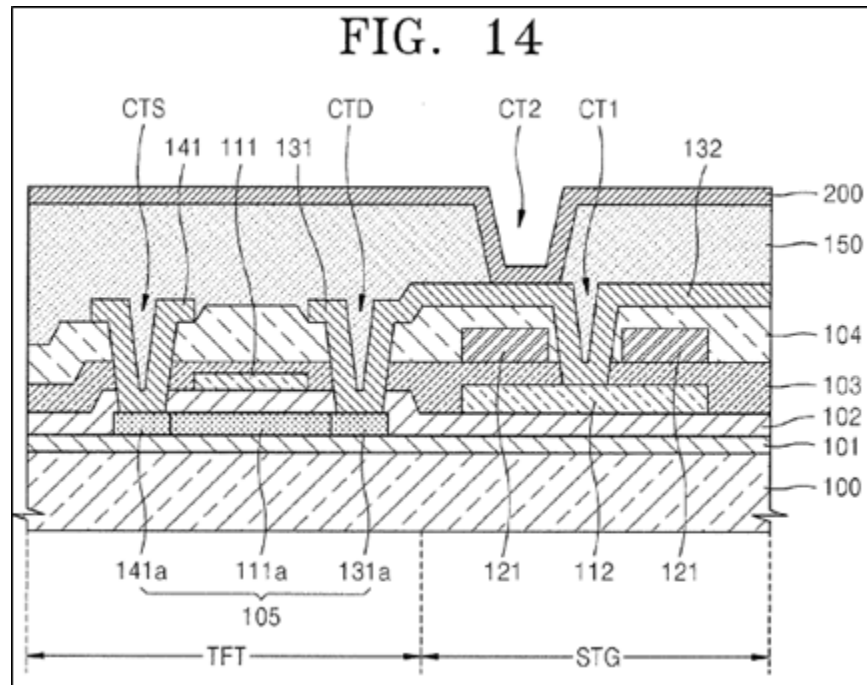
106. Zhan is directed to a “display device and a method of manufacturing the same.” (EX1011, [0003].) “The flat panel display device according to embodiments of the present invention may be an organic light-emitting display apparatus or a liquid crystal display apparatus.” (EX1011, [0041].) The display device has “increased capacitance arranging a storage capacitor in parallel through a first storage electrode located at a same level as a gate electrode, a second storage electrode from which a common voltage line is extended, and a third storage electrode from which a drain electrode is extended.” (EX1011, [0007].)

107. Zhan discloses increasing the capacitance of the capacitor without increasing the area, or reducing the area without negatively impacting the capacitance or aperture ratio: “the STG according to an embodiment of the present invention has a capacitance about 18% greater than that of the typical capacitor having the same area. In other words, if the STG of the present invention is designed to have the same capacitance as the typical capacitor, the STG may have an area of about 84% the size of the typical capacitor (based on $1/1.18=0.84$). Therefore, if the area occupied by a typical capacitor in the entire pixel is about 12% and the STG according to an embodiment is used in place of the typical

capacitor, the aperture ratio of the pixel will be increased by about 2%.” (EX1011, [0058].)

108. Zhan’s display device comprises a “second storage electrode 121 [that] is divided and the first contact hole CT1 is disposed between the divided second storage electrodes 121. In this case, at least two second storage electrodes 121 may be formed and in a plan view, a hole may be located in the center of the second storage electrode 121.” (EX1011, [0073].) “The second storage electrode 121 is formed in such a way that the common voltage line 120 extends from the second storage electrode 121, and partially overlaps with the first storage electrode 112.” (EX1011, [0045].)

109. Figure 14 (below) shows a cross-sectional view of Zhan’s display device. The Figure 14 embodiment of Zhan creates a direct connection from the transistor TFT 105 (via drain electrode contact opening (CTD)) to the pixel (via second contact hole CT2) and then to the capacitor (via first contact hole CT1).



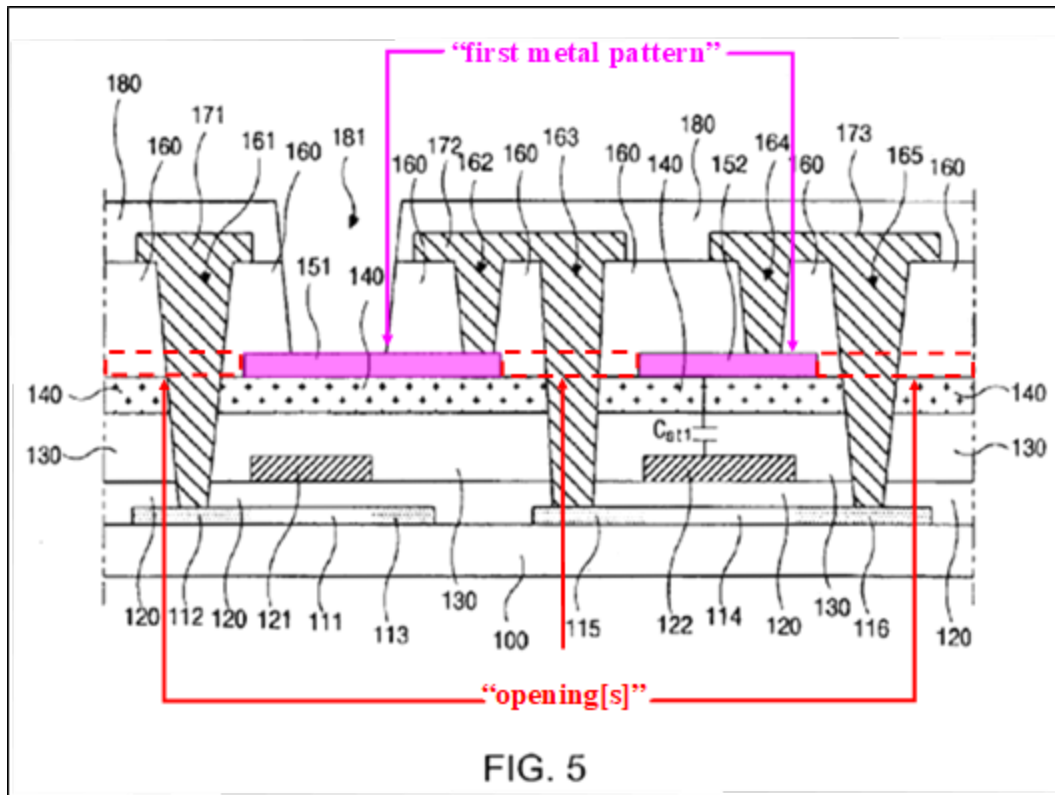
- 2. Claim 2: “The TFT array substrate of claim 1, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.”**

a. Park

110. Park teaches claim 1 as shown above. As shown for element 1[e], Park teaches an anode electrode 151 and a capacitor electrode 152 (“first metal pattern”). As shown for element 1[g], Park teaches a member connecting the drain of the switching thin film transistor 4 and the gate of electrode of the driving thin film transistor 5 (“connection member”).

111. Park discloses “wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.” For example, Figure 5 (annotated below) shows the *anode electrode 151* and the

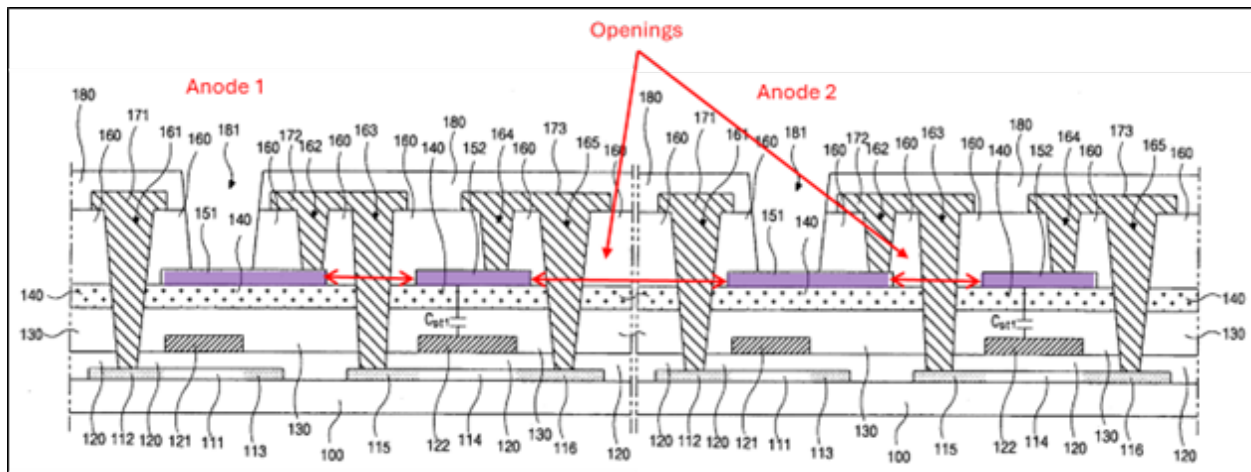
capacitor electrode 152 including an *opening*. (EX1005, [0034], [0015].) The figure shows that Park's source and drain electrodes overlap the openings of the layer of the anode electrode 151 and the capacitor electrode 152.



112. As discussed for element 1[g], a POSITA would have understood Park's Figure 5 as representing the structure of the "first drain electrode (not shown)." Thus, Park teaches the first drain electrode (part of the "connection member") overlapping the opening in a plan view.

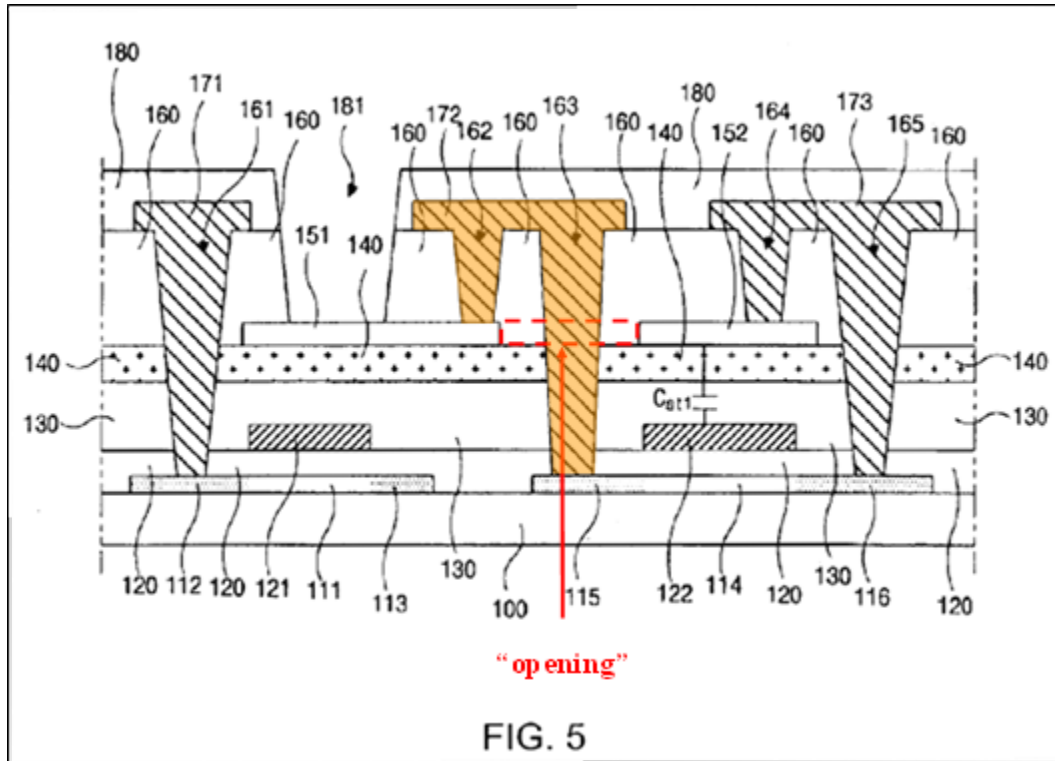
113. To illustrate more completely the relationship between the various layers and openings, Figure 5 has been reproduced twice below to show various components for *two* pixels. Anode 1 and anode 2 represent where two luminescent

elements are located in relation to each other in the Park invention. The anodes are connected to the drain of the driving transistors through connection 162/163 while the sources of the driving transistors are connected to the upper electrode of the capacitor and to the power source through connection 164/165. Between the metal layers 151 and 152 are openings as indicated.



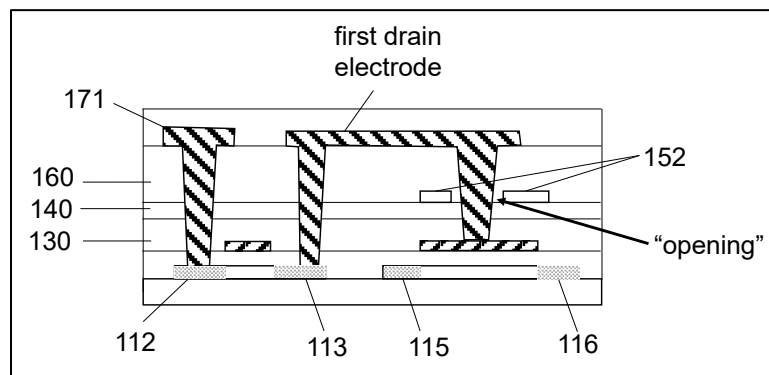
114. For example, Park discloses that “the first passivation layer 160 *is then formed on* the anode electrode 151 and the capacitor electrode 152.” (EX1005, [0038] (emphasis added).) Park discloses that “the first source electrode 171, the second drain electrode 172 and the second source electrode 173 are formed by depositing conductive material such as metal *on the* first passivation layer 160 and patterning it with a fifth mask.” (EX1005, [0039] (emphasis added).) Figure 5 (annotated below) shows a cross-sectional view with the source electrode 172 (orange) overlapping an opening (red) of the layer of the anode

electrode 151 and capacitor electrode 152, where the source electrode 172 is located closer to the top than the opening.



115. Park describes the drain of the switching thin film transistor 4 (part of the “connection member”) in relation to “a first drain electrode (not shown), which is connected to the first drain region 113 . . . are also formed on the first passivation layer 160” (EX1005, [0034]; *see also* [0007].) Before describing the drain electrode of the switching thin film transistor 4, it describes the source and drain electrodes shown in Figure 5. Hence, a POSITA would have understood that the drain electrode of the switching thin film transistor 4 would have a similar configuration as the source and drain electrodes shown in Figure 5. Because Park states that the drain electrode of the switching thin film transistor 4 is “not shown”

and “also formed on the first passivation layer 160,” a POSITA would have understood that the drain electrode of the switching thin film transistor (part of the “connection member”) overlaps the opening in a plan view. If the drain electrode did not overlap the opening in the first metal pattern, the drain electrode would be shorted to either the anode or capacitor electrodes 151 and 152. The figure below shows an example configuration of Park’s first drain electrode.



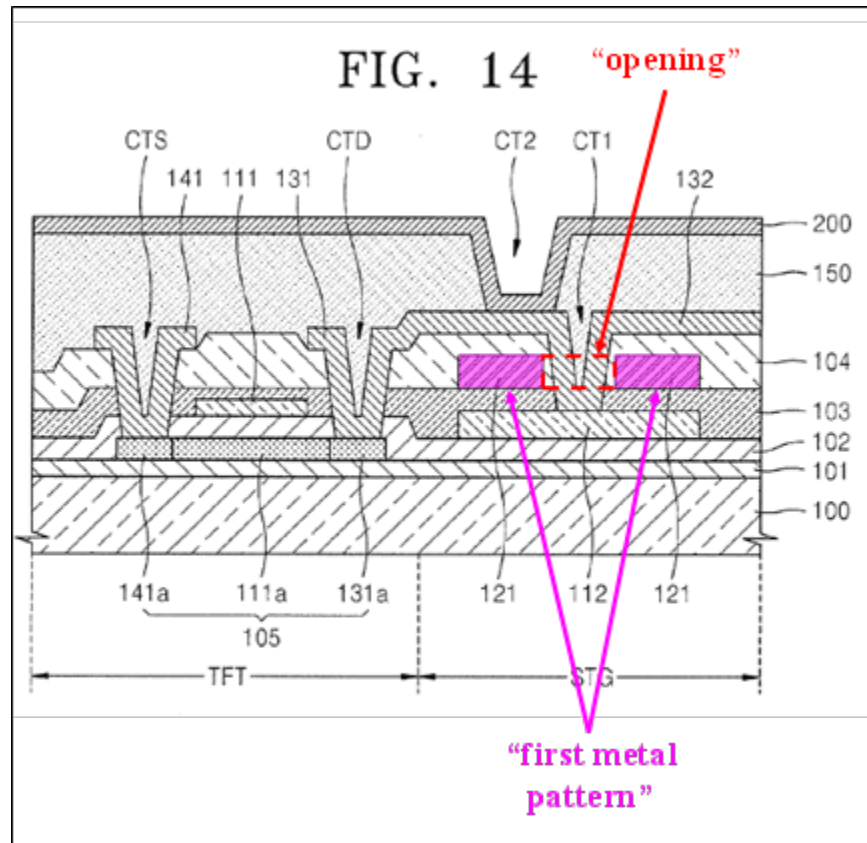
116. As shown for element 1[e], Park also discloses a capacitor electrode 80 (“first metal pattern”) of Figure 4.

b. Zhan

117. Zhan also teaches “the first metal pattern includes an opening.” For example, Zhan discloses a “second storage electrode 121 may be formed of a metal or indium tin oxide (ITO). If the second storage electrode 121 is formed of a metal, electrical conductivity thereof is great and thus a common electrode signal applied through the common voltage line 120 may be prevented from being delayed. If the second storage electrode 121 is formed of ITO, an aperture ratio

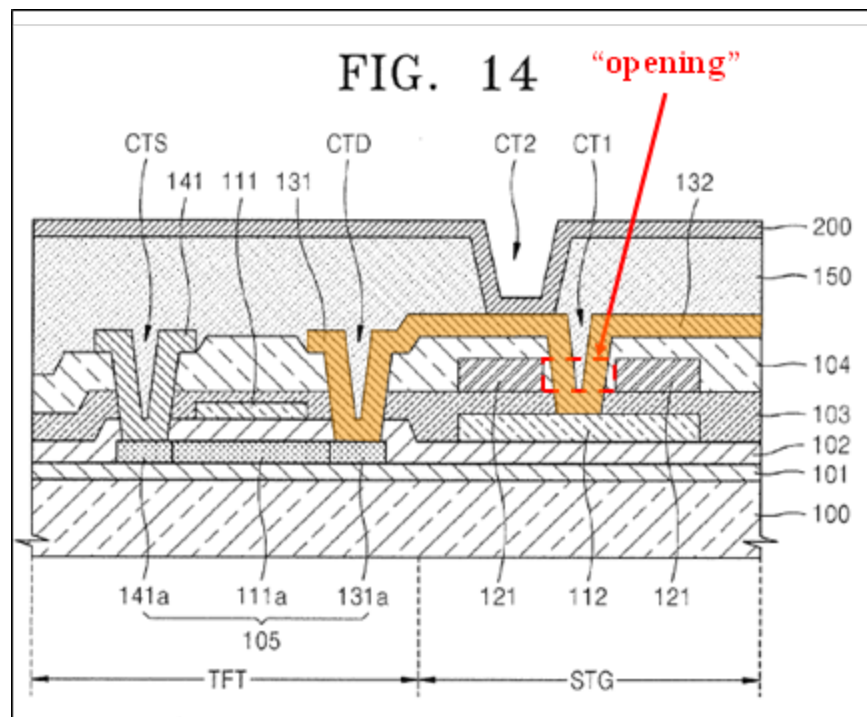
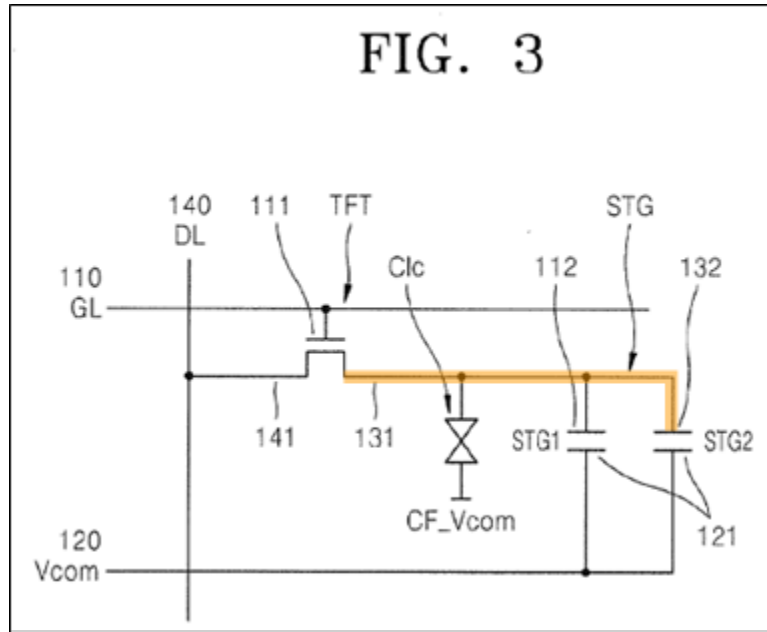
thereof is increased and may be excellent.” (EX1011, [0063].) Zhan discloses that “[r]eferring to FIG. 14, in one embodiment of the present invention, the second storage electrode 121 is divided and the first contact hole CT1 is disposed between the divided second storage electrodes 121. In this case, at least two second storage electrodes 121 may be formed and in a plan view, a hole may be located in the center of the second storage electrode 121.” (EX1011, [0073].) Figure 14 (annotated below) shows the *storage electrode 121* including a *hole* (“opening”).

“The second storage electrode 121 is formed in such a way that the common voltage line 120 extends from the second storage electrode 121, and partially overlaps with the first storage electrode 112.” (EX1011, [0045].) Thus, the storage electrode 121 is a “first metal pattern.”

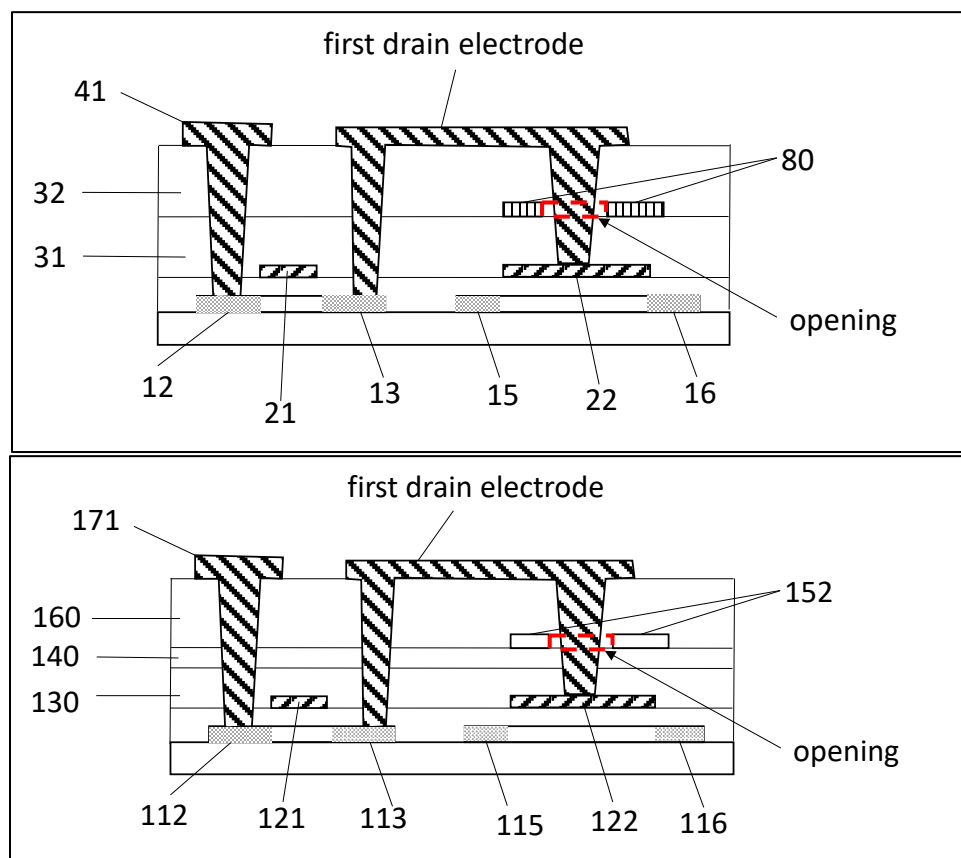


118. Zhan also teaches “a portion of the connection member overlaps the opening in a plan view.” For example, Zhan discloses a “third storage electrode 132 . . . contacts the first storage electrode 112 through a first contact hole (or first contact unit or opening) CT1 located in the first interlayer adjusting layer 103 and second interlayer adjusting layer 104. As described above, the third storage electrode 132 extends from the drain electrode 131 of the TFT.” (EX1011, [0048].) Figure 3 (annotated below) shows the storage electrode 132 electrically connecting TFT 131. Figure 14 (annotated below) shows that a portion of *storage electrode 132* overlaps the *hole* in the storage electrode 121 in a plan view. Thus,

Zhan teaches a “first metal pattern includ[ing] an opening, and a portion of the connection member overlaps the opening in a plan view.”



119. The figure below shows the first drain electrode in Park. A POSITA would be motivated to extend the drain electrode to connect it to the first storage electrode of the capacitor, and would have done so via a first contact hole CT1 and an opening, as shown in the figure below. The first drain electrode in Park is part of the connection member connected between the first drain region 13/113 and the second gate electrode 22/122.



c. Motivation to combine Park and Zhan

120. It would have been obvious to a POSITA at the time of the '483 patent to combine the teachings of Park and Zhan. Park and Zhan disclose light-emitting devices and structures. Both teach increasing the capacitance of the

storage capacitor. Park discloses “an active matrix organic electro luminescent display (ELD) device in which a storage capacitance of a storage capacitor is increased without reducing an aperture ratio and number of masks needed is reduced.” (EX1005, [0017].) Similarly, Zhan discloses increasing the capacitance of the capacitor without increasing the area, or reducing the area without negatively impacting the capacitance or aperture ratio. Zhan discloses “the STG according to an embodiment of the present invention has a capacitance about 18% greater than that of the typical capacitor having the same area. In other words, if the STG of the present invention is designed to have the same capacitance as the typical capacitor, the STG may have an area of about 84% the size of the typical capacitor (based on $1/1.18=0.84$). Therefore, if the area occupied by a typical capacitor in the entire pixel is about 12% and the STG according to an embodiment is used in place of the typical capacitor, the aperture ratio of the pixel will be increased by about 2%.” (EX1011, [0058], [0041].) Thus, Park and Zhan are from the same field of endeavor and reasonably pertinent to the same technical problems of improving the manufacturing and quality of light-emitting display devices, including with respect to structural configurations that promote increased capacitance of the storage capacitor.

121. Zhan discloses the “first storage capacitor STG1 includes the first storage electrode 112 and the second storage electrode 121, and the second storage

capacitor STG2 includes the second storage electrode 121 and the third storage electrode 132. Accordingly, the storage capacitor according to an embodiment of the present invention may have a greater capacitance than that of typical capacitors having the same area and structure due to the parallel structure.” (EX1011, [0052].) Zhan also discloses “the second storage electrode 121 is divided and the first contact hole CT1 is disposed between the divided second storage electrodes 121. In this case, at least two second storage electrodes 121 may be formed and in a plan view, a hole may be located in the center of the second storage electrode 121.” (EX1011, [0073].) Zhan’s technical features may be combined with Park’s teachings to result in an OLED with greater storage capacitance and reduced manufacturing deviations. There would have been a reasonable expectation of success because such techniques were known in the prior art and have been successfully demonstrated. Zhan further teaches a connection member that provides an electrode of the capacitor (storage electrode 112) through an opening in a metal pattern (storage electrode 132) in a similar manner to Park. Park teaches a connection member 163 that provides connection to drain region 115 through an opening in a metal pattern 151/152.

122. Park and Zhan teach increasing the storage capacitance in a light-emitting display device and using connection members for interconnections between layers. A POSITA would have been motivated to use Zhan’s techniques

to improve the similar device of Park in the same way. Prior art such as Zhan successfully demonstrated an OLED configuration that improved the storage capacitance, and thus, there would have been a reasonable expectation of success for combining Park and Zhan. As a result, it would have been obvious to a POSITA to combine the teachings of Park and Zhan.

3. Claim 3

- a. **3[a]: “The TFT array substrate of claim 2, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and”**

123. Park and/or Zhan teach claim 2 as shown above.

(i) Park

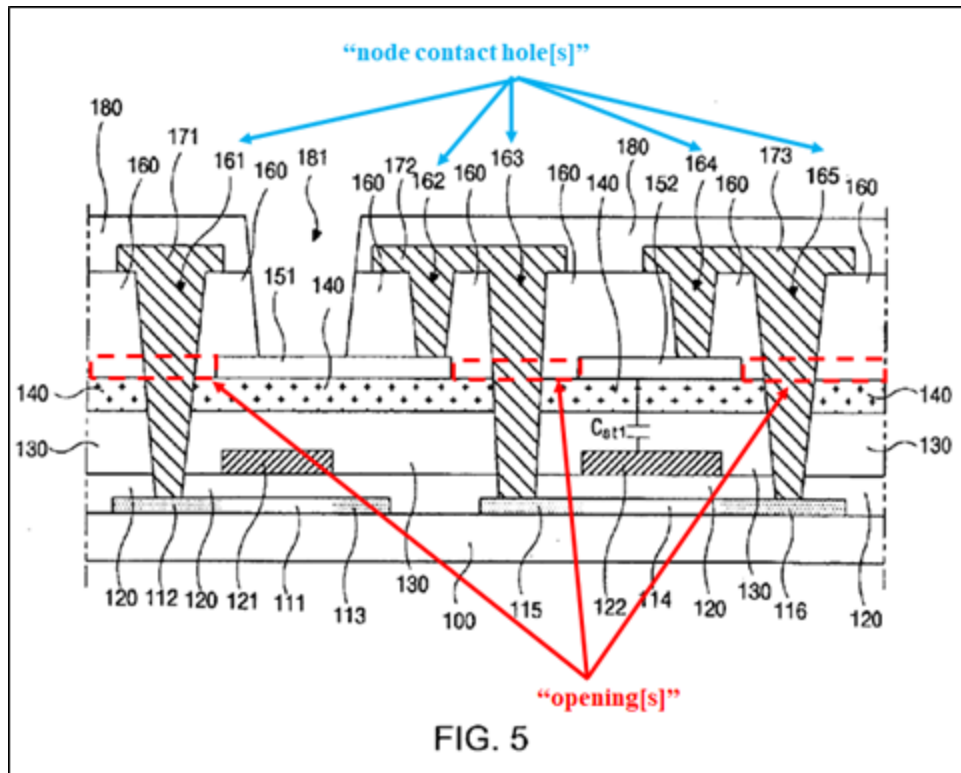
124. As shown for element 1[d], Park teaches an interlayer 31/130 (“second insulating layer”). As shown for element 1[f], Park teaches an inter layer 32/passivation layer 160 (“third insulating layer”).

125. Park teaches “wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening.” For example, Park teaches the interlayer 130 and passivation layer 160 including contact holes that overlap the openings of the layer of the anode electrode 151 and capacitor electrode 80/152. For example, Park discloses “[t]he first, third, and fifth contact holes 161, 163 and 165 are formed all the way to the gate insulating layer 120. The first contact hole 161 exposes a portion of the [first] source region 112, the

second contact hole 162 the anode electrode 151, the third contact hole 163 the second drain region 115, the fourth contact hole 164 the capacitor electrode 152 and the fifth contact hole 165 the second source region 116.” (EX1005, [0034]; *see also* [0015].)

126. Figure 5 (annotated below) shows the contact holes 161, 162, 163, 164, and 165 overlapping the openings. As discussed for element 15[b], a POSITA would have understood that the drain electrode of the switching thin film transistor 4 would have a similar configuration as the source and drain electrodes shown in Figure 5. Referring to the prior art in Figure 2, with a similar configuration for the source and drain electrodes, Park discloses: “[a] first drain electrode (not shown in the figure) is further formed of same material as the first source electrode 41 over the first drain region 13 and connected to the first drain region 13. The first drain electrode (not shown) is also connected to the second gate electrode 22.” (EX1005, [0007].) Since the first drain electrode is formed of the same material as the first source electrode 41 and is connected to the gate electrode 22, a POSITA would have understood that the drain of the first transistor 113 in Figure 5 is connected to the gate electrode 122 with the same metal as the connection member through a node contact hole in the second and third insulators. This would include the interlayer 130 and passivation layer 160 including a contact

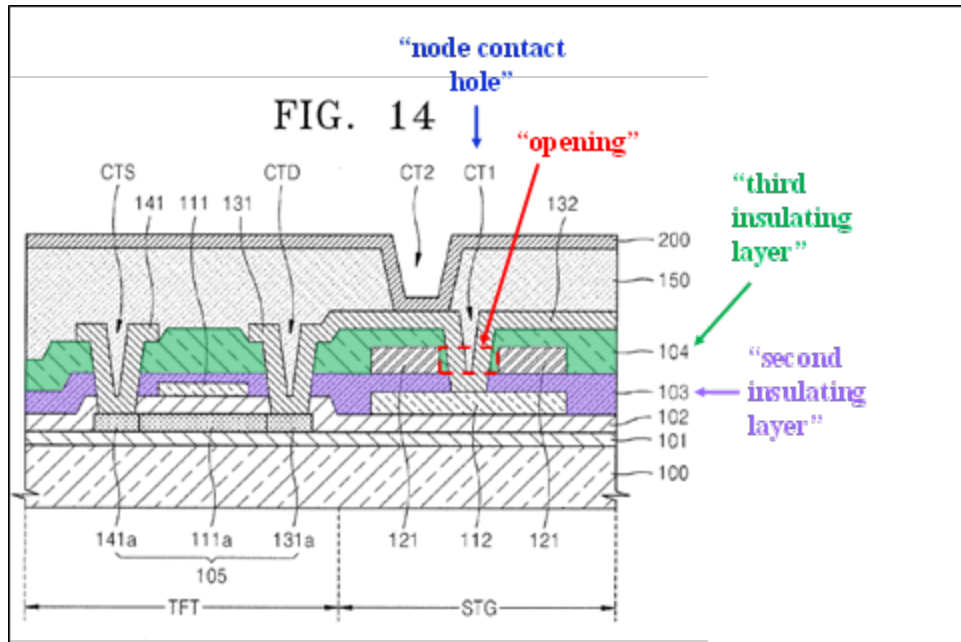
hole for the drain electrode of the switching thin film transistor 4 overlapping an opening.



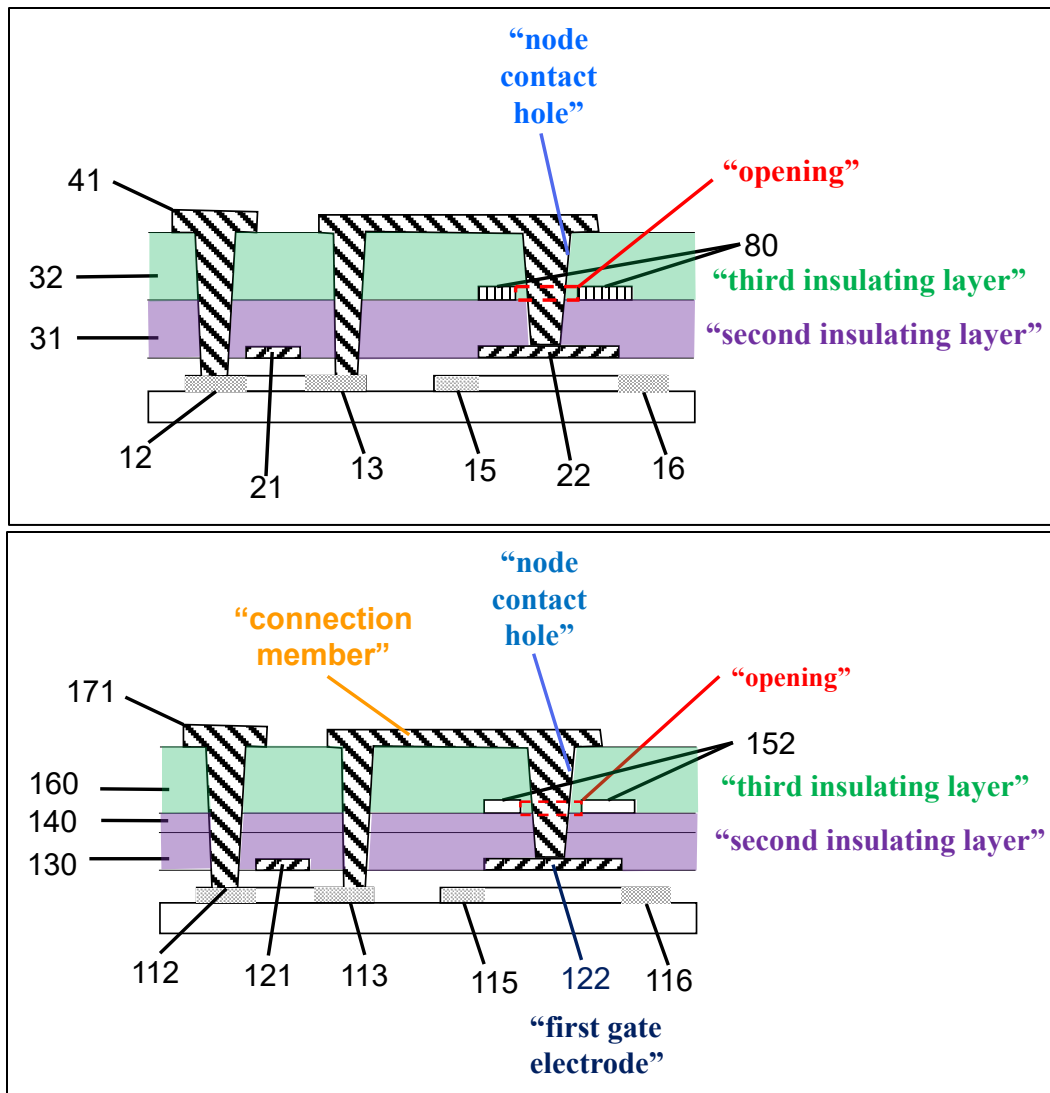
(ii) Zhan

127. Zhan teaches “wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening.” For example, Zhan discloses “first contact hole CT1 may be formed by penetrating (or through) the first and second interlayer adjusting layers 103 and 104 at locations corresponding to a part (or a location) where the second storage electrode 121 is not located.” (EX1011, [0050].) Zhan explains that “the first interlayer adjusting layer 103, and the second interlayer adjusting layer 104 may each be an insulator, may each have a single-layered or a multi-layered structure, and may each be formed of an organic

material, an inorganic material, or an organic/inorganic composition.” (EX1011, [0065].) Figure 14 (annotated below) shows *interlayer adjusting layer 103* and *interlayer adjusting layer 104* including *contact hole CT1* overlapping the *hole*. Thus, Zhan teaches element 3[a].



128. It would have been obvious to a POSITA to combine the teachings of Park and Zhan. (See Claim 2.) The figures below show the Park-Zhan combination including the *inter layer 31/130* and *inter layer 140* (“second insulating layer”) and *inter layer 32/passivation layer 160* (“third insulating layer”). The figures show the *node contact hole* overlapping the *opening*.



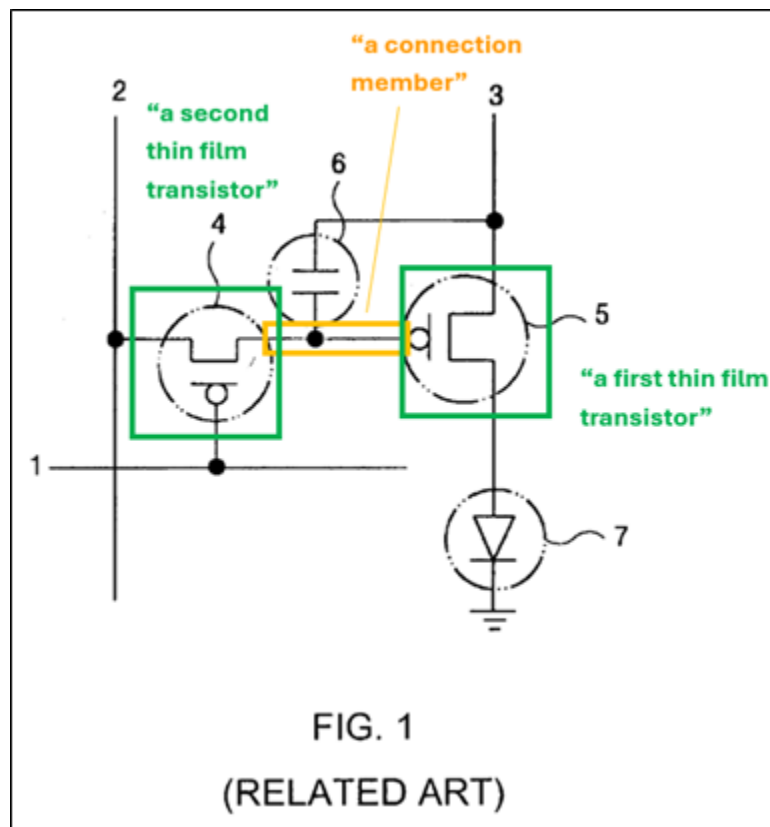
b. 3[b]: “the portion of the connection member is connected with the first gate electrode through the node contact hole.”

(i) Park

129. As shown for claim 2, Park teaches a “first drain electrode” of the switching thin film transistor 4 (“portion of the connection member”). As shown for element 1[b], Park teaches a gate electrode 22/122 (“first gate electrode”) of the driving thin film transistor 5. As shown for element 3[a], Park teaches a node

contact hole (“node contact hole”) for connecting the first drain electrode of the switching thin film transistor 4.

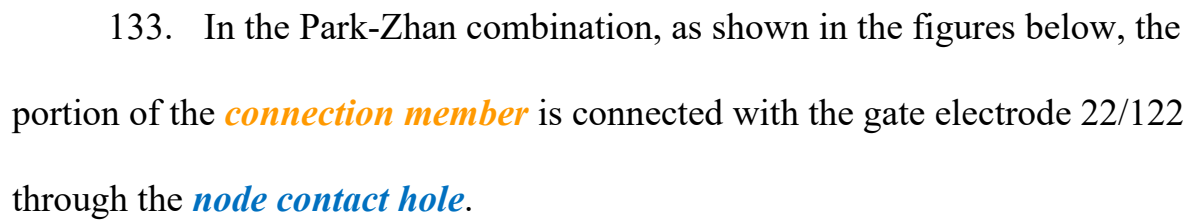
130. Figure 1 of Park (annotated below) shows the “drain electrode of the switching thin film transistor 4 *is connected to* a gate electrode of the thin, film transistor 5” and a “storage capacitor 6 *is connected to* the gate electrode and the source electrode of the driving thin film resistor 5.” (EX1005, [0006] (emphasis added).) Thus, Park teaches “the portion of the connection member is connected with the first gate electrode through the node contact hole.”

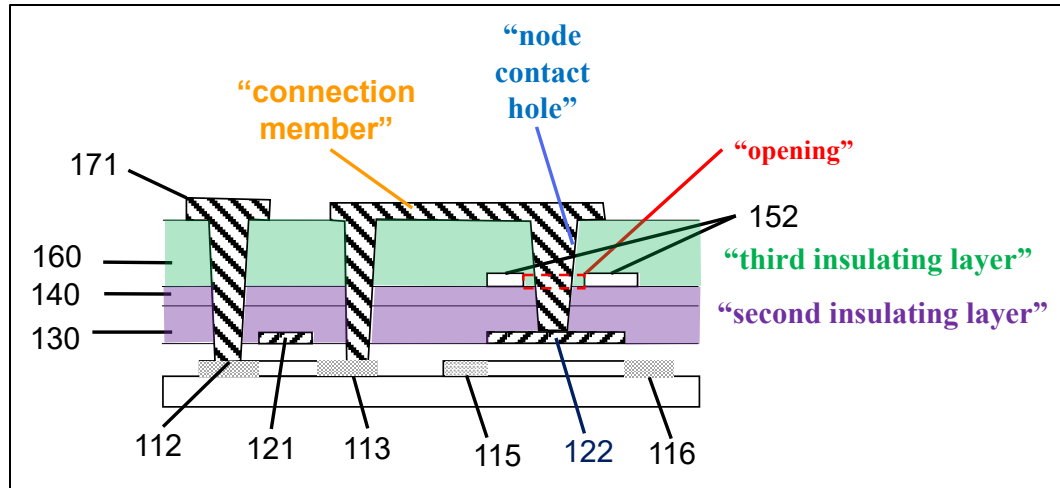


(ii) Zhan

131. As shown for claim 2, Zhan teaches a storage electrode 132 (“connection member”). As shown for element 3[a], Zhan teaches contact hole CT1 (“node contact hole”).

132. Zhan teaches “the portion of the connection member is connected with the [] electrode through the node contact hole.” For example, Zhan discloses “[t]he third storage electrode 132 is located on the second interlayer adjusting layer 104 and contacts the first storage electrode 112 through a first contact hole (or first contact unit or opening) CT1 located in the first interlayer adjusting layer 103 and second interlayer adjusting layer 104. As described above, the third storage electrode 132 extends from the drain electrode 131 of the TFT.” (EX1011, [0048].) Figure 14 (annotated below) shows the *storage electrode 132* connected to the *storage electrode 112* through the *contact hole CT1*.





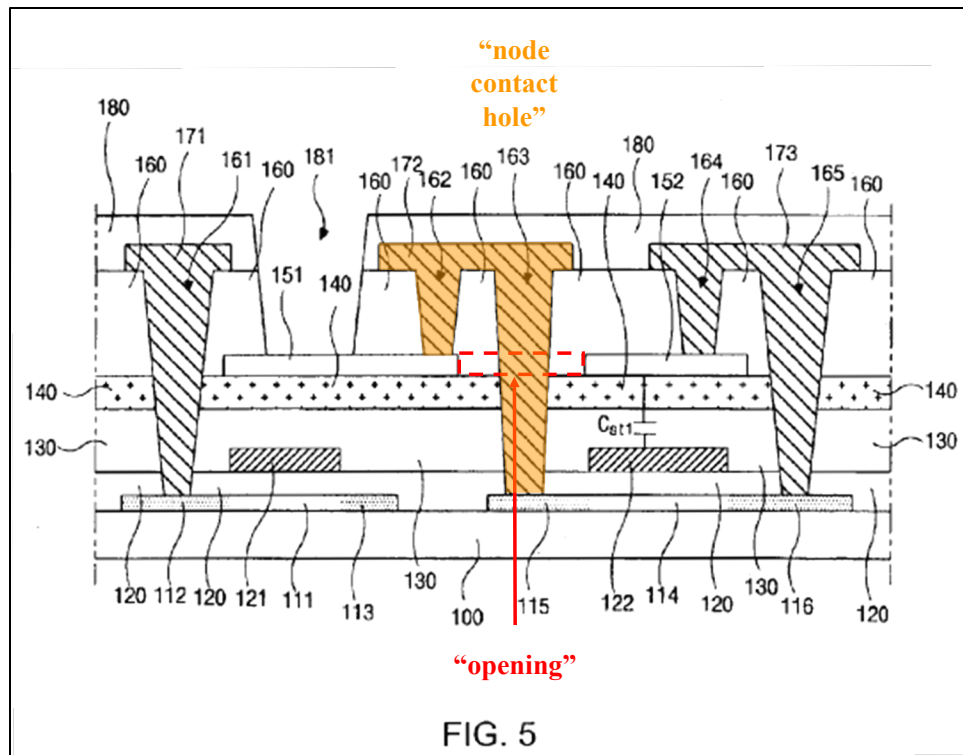
4. Claim 4: “The TFT array substrate of claim 3, wherein a size of the opening is greater than a size of the node contact hole in the plan view.”

134. Park and/or Zhan teach claim 3 as shown above in Section IX.B.3.

a. Park

135. As shown for claim 2, Park teaches an opening and a node contact hole for the “first drain electrode (not shown), which is connected to the first drain region 113 . . . are also formed on the first passivation layer 160.” (EX1005, [0034]; *see also* [0007].)

136. Park also teaches the size of the opening in the layer of the anode electrode 151 and capacitor electrode 152 being greater than a size of a contact hole. For example, Figure 5 (annotated below) shows the size of an *opening* being greater than the size of the *contact hole 163*.

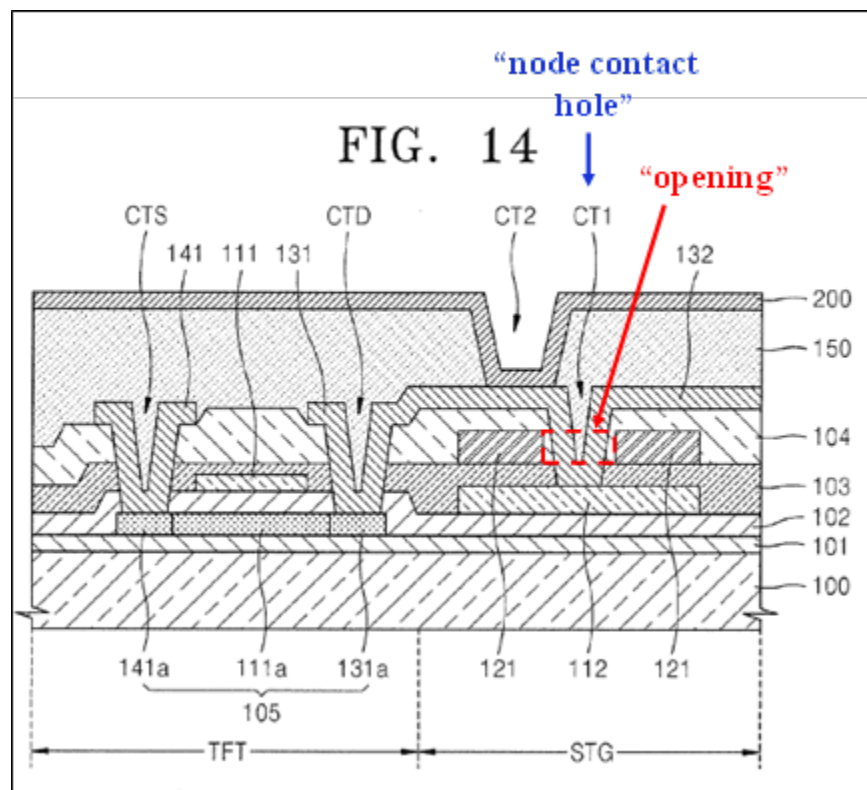


137. Park explains that “[t]hough it is not shown in the figure, the second gate electrode 122 is electrically connected to the first drain region 113.” (EX1005, [0034]; *see also* [0007].) As discussed for element 1[g], a POSITA would have understood that the drain electrode of the switching thin film transistor 4 would have a similar configuration as the source and drain electrodes shown in Figure 5. This includes the contact hole of the drain electrode of the switching thin film transistor 4 having a similar configuration (size of the opening being greater than the size of the contact hole) as the contact holes of the source and drain electrodes shown in Figure 5. Thus, Park teaches claim 4.

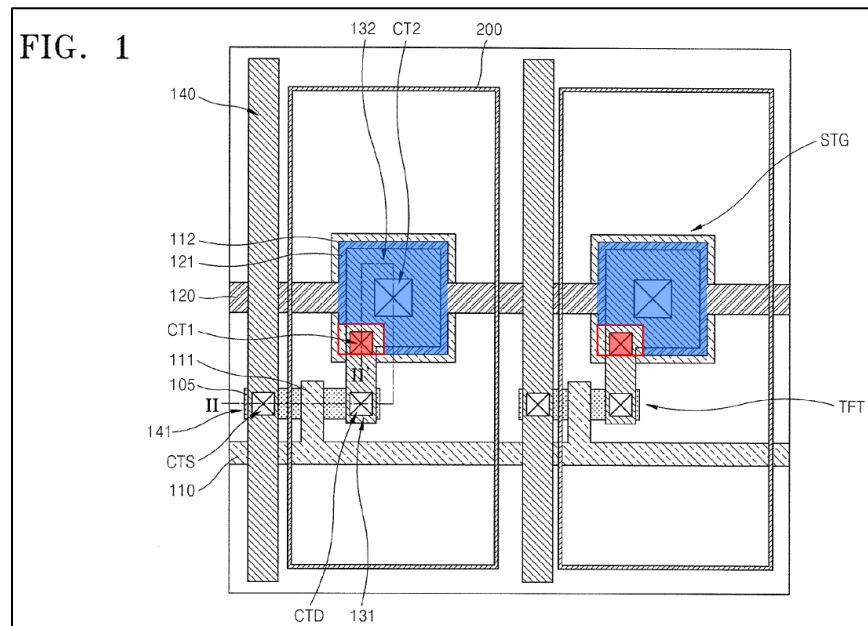
b. Zhan

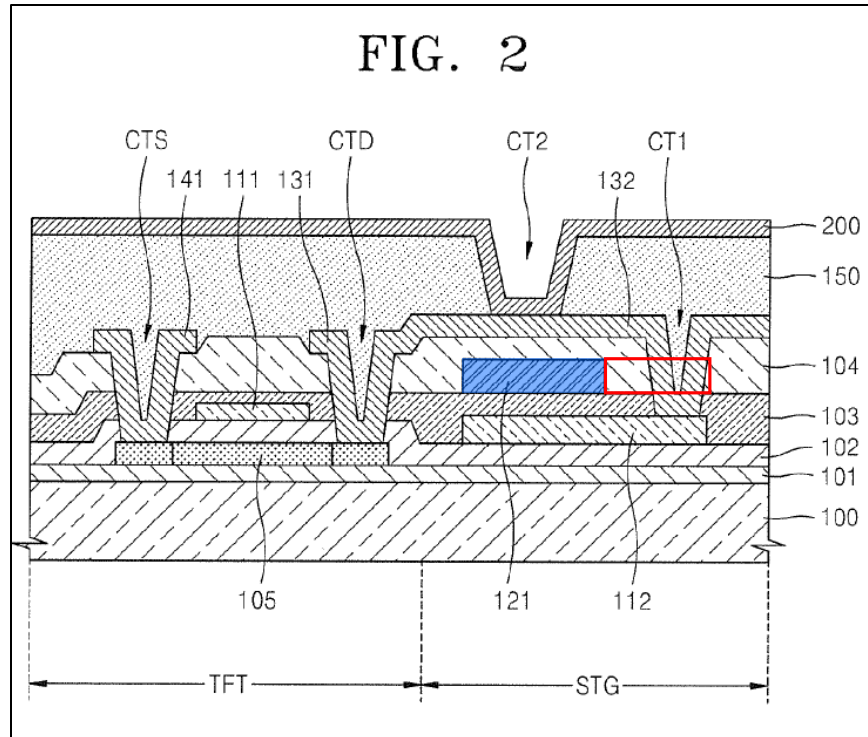
138. As shown for claim 2, Zhan teaches a hole (“opening”) in the storage electrode 121. As shown for element 3[a], Zhan teaches a contact hole CT1 (“node contact hole”).

139. Zhan teaches “a size of the opening is greater than a size of the node contact hole in the plan view.” For example, Figure 14 (annotated below) shows that the size of the **hole** is greater than a size of the **contact hole CT1**. Figure 14 is a cross-sectional view, but a POSITA would have understood that the size of the hole is greater than a size of the contact hole CT1 in a plan view because the width of hole is greater than the width of contact hole CT1. Thus, Zhan teaches claim 4.

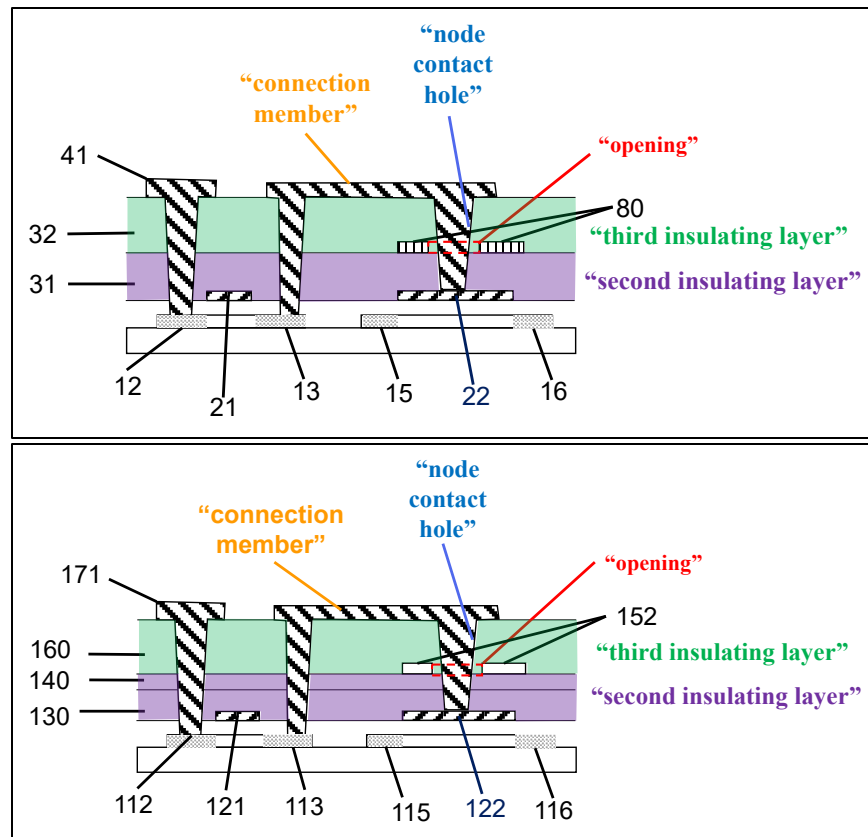


140. Figures 1 and 2 of Zhan (annotated below) show the contact hole CT1 penetrates through the interlayer adjusting layers 103 and 104 at locations where the second storage electrode 121 is not located. (EX1011, [0050].) Thus, Zhan teaches the size of the opening is greater than a size of the contact hole in the plan view.





141. It would have been obvious to a POSITA to combine the teachings of Park and Zhan. (*See* Section IX.B.2.) In the Park-Zhan combination, as shown in the figures below, the size of the opening is greater than a size of the node contact hole. Even though the figures below show cross-sectional views, it would have been obvious that the sizes of the openings are greater than the sizes of the contact holes in the plan view because the widths of the openings are greater than the widths of contact holes in the cross-section view.

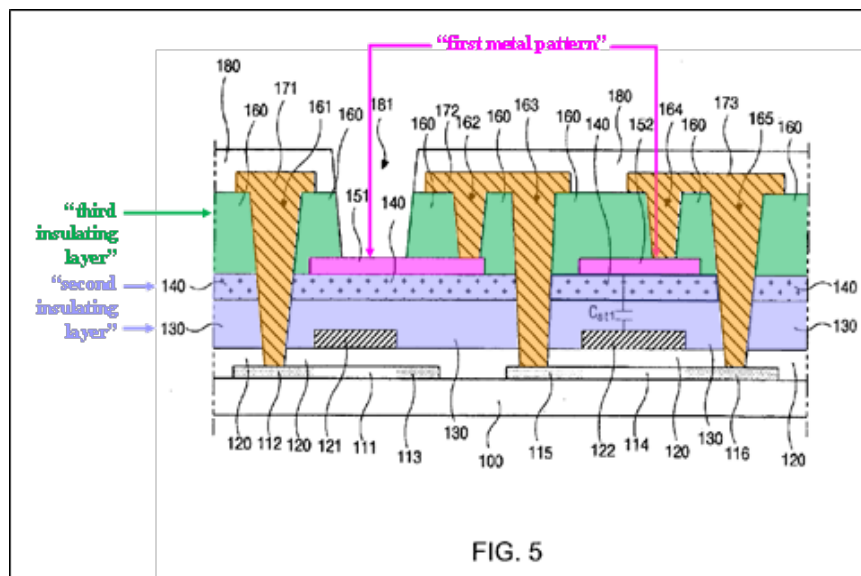


- 5. Claim 5: “The TFT array substrate of claim 4, wherein the second and third insulating layers contact each other in a region between the first metal pattern and the portion of the connection member in a cross-sectional view.”**

142. Park and/or Zhan teaches claim 4 as shown above in Section IX.B.4.

143. As discussed for element 1[g], Park teaches a first drain electrode (“connection member”). As shown for element 1[d], Park teaches an inter layer 130 and/or inter layer 140 (“second insulating layer”). As shown for element 1[f], Park teaches a passivation layer 160 (“third insulating layer”). As shown for element 1[f], Park teaches an anode electrode 151 and capacitor electrode 152 (“first metal pattern”).

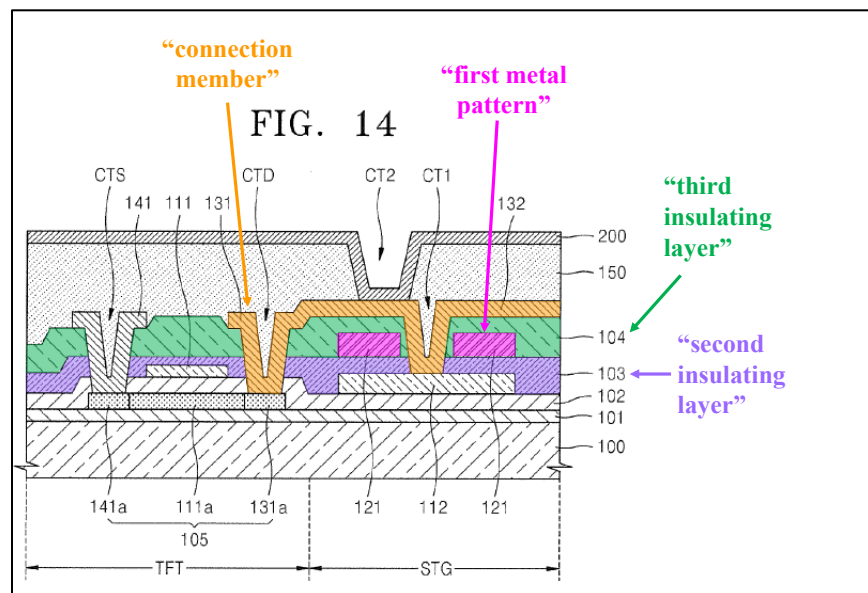
144. Park teaches “the second and third insulating layers contact each other in a region between the first metal pattern and the portion of the connection member in a cross-sectional view.” For example, Figure 5 (below) of Park shows *inter layer 130* and/or *inter layer 140* and *passivation layer 160* contacting each other (shown in red circles) between the *anode electrode 151* and *capacitor electrode 152* and the *source drain electrodes*.



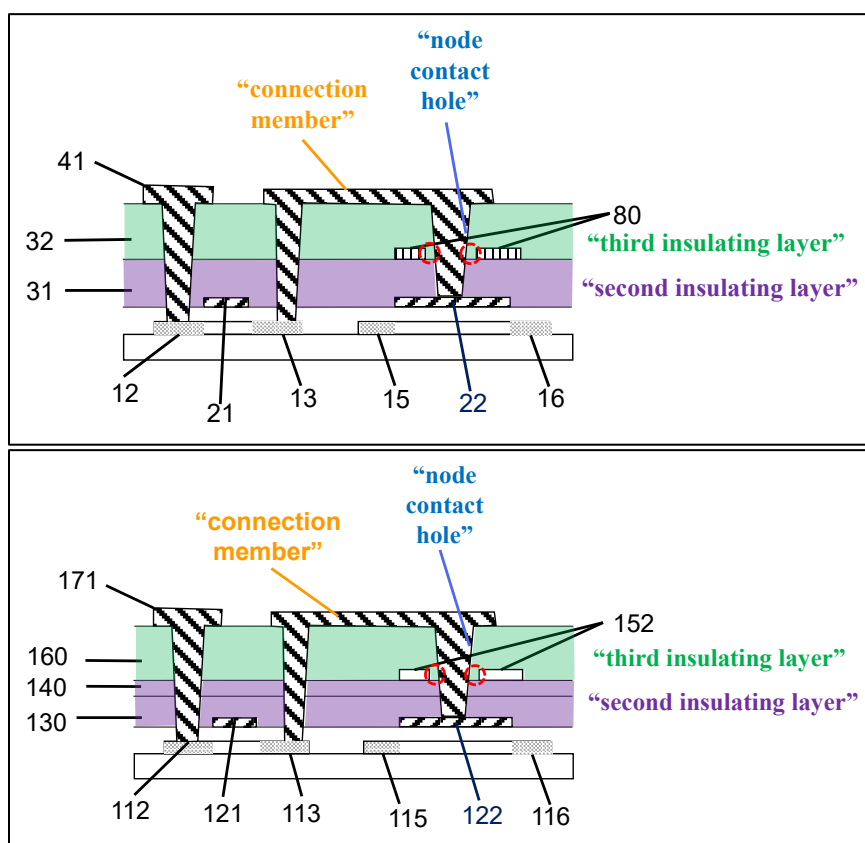
145. As shown for element 1[g], Figure 5 of Park shows the structure of the source and drain electrodes. The figure represents the structure of Park’s first drain electrode. (EX1005, [0039].) Thus, it would have been obvious that the inter layer 140 and inter layer 160 contact each other in a region between the anode electrode 151 and capacitor electrode 152 and the portion of the first drain electrode.

146. Zhan discloses a first contact hole CT1 “formed by penetrating (or through) the first and second interlayer adjusting layers 103 and 104 at locations corresponding to a part (or a location) where the second storage electrode 121 [(“first metal pattern”)] is not located.” (EX1011, [0050].) Zhan explains that “[i]f the second storage electrode 121 is formed of a metal, electrical conductivity thereof is great and thus a common electrode signal applied through the common voltage line 120 may be prevented from being delayed.” (EX1011, [0063].)

Figure 14 of Zhan (annotated below) shows the *interlayer adjusting layer 103* (“second insulating layer”) and the *interlayer adjusting layer 104* (“third insulating layer”) contact each other in a region (shown in red circles) between the second storage electrode 121 (“first metal pattern”) and the portion of the storage electrode 132 (“connection member”) in a cross-section view.



147. The figures below show examples of the combination of Park and Zhan, which teaches an *inter layer 31/130* and *inter layer 140* (“second insulating layer”) and an *inter layer 32/passivation layer 160* (“third insulating layer”) that contact each other in a region (shown in red circles) between the storage electrode 80/152 (part of the “first metal pattern”) and the part of connection member in a cross-section view.



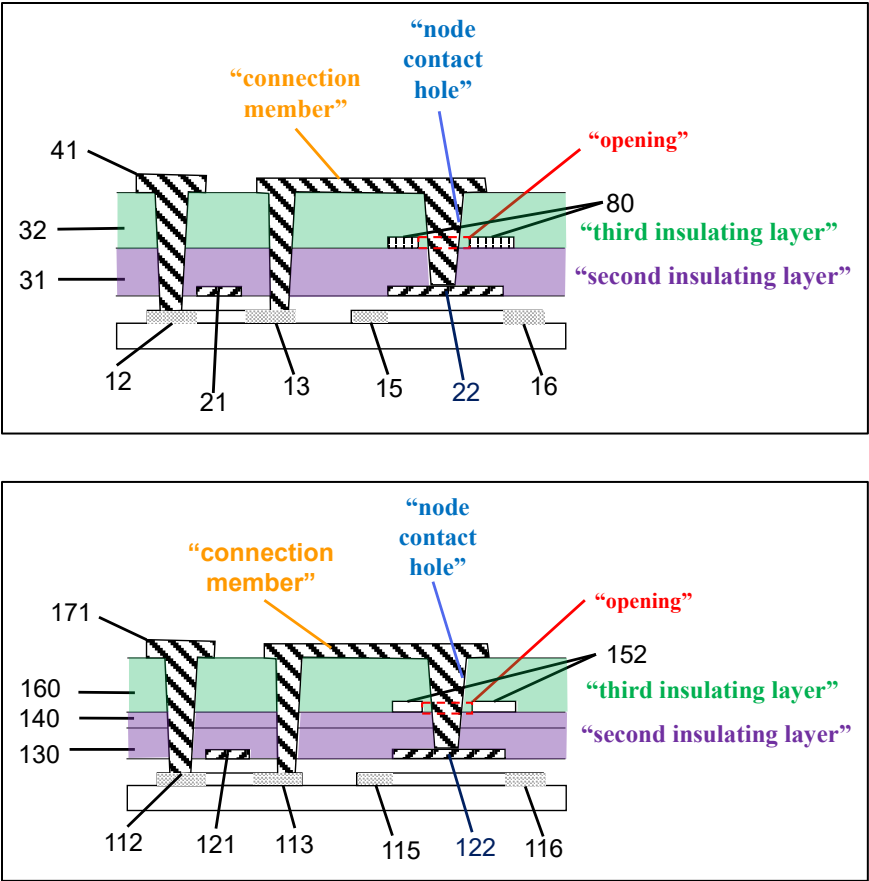
6. Claim 6: “The TFT array substrate of claim 2, wherein an entire area of the opening overlaps the first gate electrode in the plan view.”

148. Park and/or Zhan teaches claim 2 as shown above in Section IX.B.2.

As shown for claim 2, Park discloses a hole (“opening”) in the layer comprising the capacitor electrode 152.

149. Zhan teaches a “second storage electrode 121 is divided and the first contact hole CT1 is disposed between the divided second storage electrodes 121. In this case, at least two second storage electrodes 121 may be formed and in a plan view, a *hole may be located in the center of the second storage electrode 121.*” (EX1011, [0073] (emphasis added), Fig. 14.)

150. The figures below show the Park-Zhan combination. In the Park-Zhan combination, as shown in the figures, an entire area of the hole (“opening”) overlaps the gate electrode 22/122. Even though the below figures show cross-sectional views, it would have been obvious that the entire areas of the openings overlap the first gate electrode 22/122 in the plan view because the hole is located in the center of the capacitor electrode 80/152 (part of the “first metal pattern”) and has a width that is less than the width of the gate electrode 22/122.



7. Claim 22

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

151. The preamble of claim 22 is similar to the preamble of claim 1, which Park renders obvious. (See Section IX.A.2.a.) The table below shows the similarities.

Preamble of Claim 1	Preamble of Claim 22
“A thin film transistor (TFT) array substrate comprising:”	“A thin film transistor (TFT) array substrate comprising:”

b. 22[a]: “a substrate;”

152. Element 22[a] is similar to element 1[a], which Park renders obvious.

(See Section IX.A.2.b.) The table below shows the similarities.

Element 1[a]	Element 22[a]
“a substrate;”	“a substrate;”

c. 22[b]: “a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”

153. Element 22[b] is similar to element 1[b], which Park renders obvious.

(See Section IX.A.2.c.) The table below shows the similarities.

Element 1[b]	Element 22[b]
“a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”	“a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”

d. 22[c]: “a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”

154. Element 22[c] is similar to element 1[c], which Park renders obvious.

(See Section IX.A.2.d.) The table below shows the similarities.

Element 1[c]	Element 22[c]
“a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”	“a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”

e. 22[d]: “a second insulating layer disposed on the first and second gate electrode;”

155. Element 22[d] is similar to element 1[d], which Park renders obvious.

(See Section IX.A.2.e.) The table below shows the similarities.

Element 1[d]	Element 22[d]
“a second insulating layer disposed on the first and second gate electrode;”	“a second insulating layer disposed on the first and second gate electrode;”

f. 22[e]: “a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”

156. Element 22[e] is similar to element 1[e], which Park renders obvious.

(See Section IX.A.2.f.) The table below shows the similarities.

Element 1[e]	Element 22[e]
“a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”	“a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”

g. 22[f]: “a third insulating layer disposed on the first metal pattern; and”

157. Element 22[f] is similar to element 1[f], which Park renders obvious.

(See Section IX.A.2.g.) The table below shows the similarities.

Element 1[f]	Element 22[f]
“a third insulating layer disposed on the first metal pattern; and”	“a third insulating layer disposed on the first metal pattern; and”

h. 22[g]: “a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor,”

158. Element 22[g] is similar to element 1[g], which Park renders obvious.

(See Section IX.A.2.h.) The table below shows the similarities.

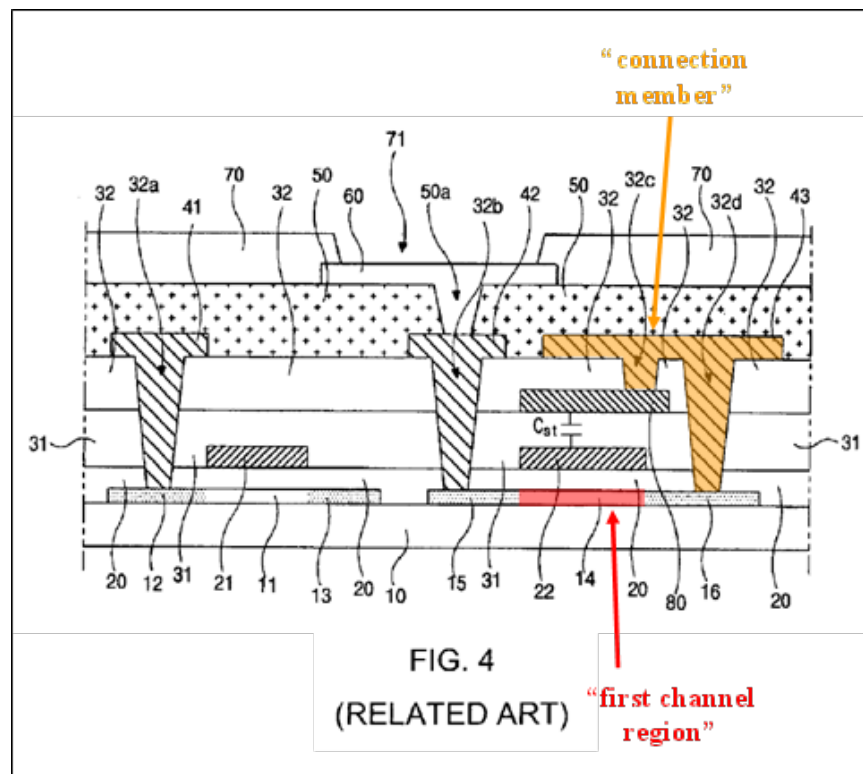
Element 1[g]	Element 22[g]
“a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor.”	“a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor,”

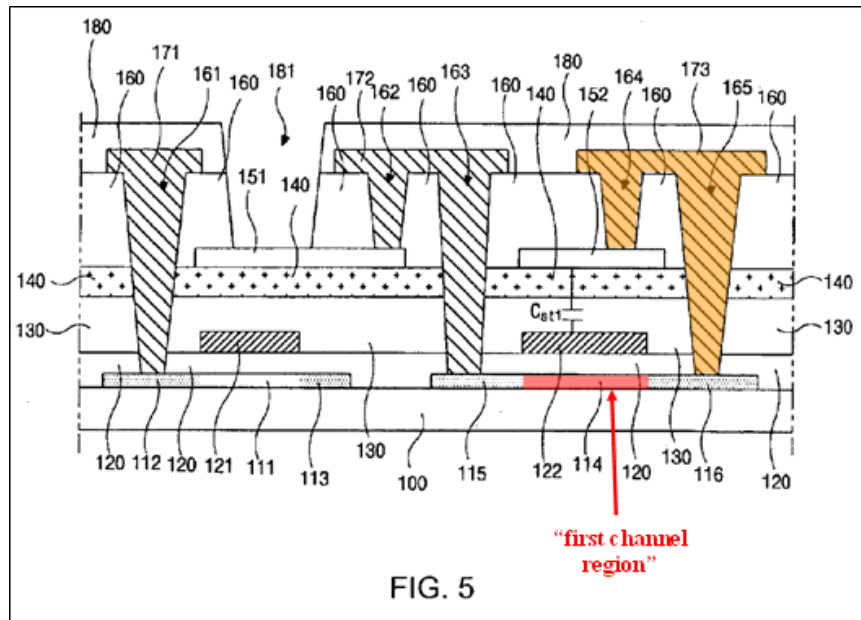
i. 22[h]: “the connection member overlapping a portion of the first channel region in a plan view.”

(i) Park

159. As shown for element 1[g], Park teaches a member connecting the drain of the switching thin film transistor 4 and the gate of electrode of the driving thin film transistor 5 (“connection member”). As shown for element 1[b], Park teaches an active layer 14/114 (“first channel region”).

160. Park discloses “the connection member overlapping a portion of the first channel region in a plan view.” For example, Park teaches source and drain electrodes overlapping with a portion of the active layer of the transistors. For example, Figures 4 and 5 (annotated below) of Park shows the *source electrode 43/173* overlaps a portion of *active layer 14/114* of the driving thin film transistor 5. These figures show cross-sectional views with the source electrode 173 located above the gate electrode, and therefore overlaps the first channel region in plan view. Because these figures show cross-sectional views through the first and second transistors, a POSITA would have understood that the plan view would show the source electrode 173 overlapping the first channel region (active layer 14/114).





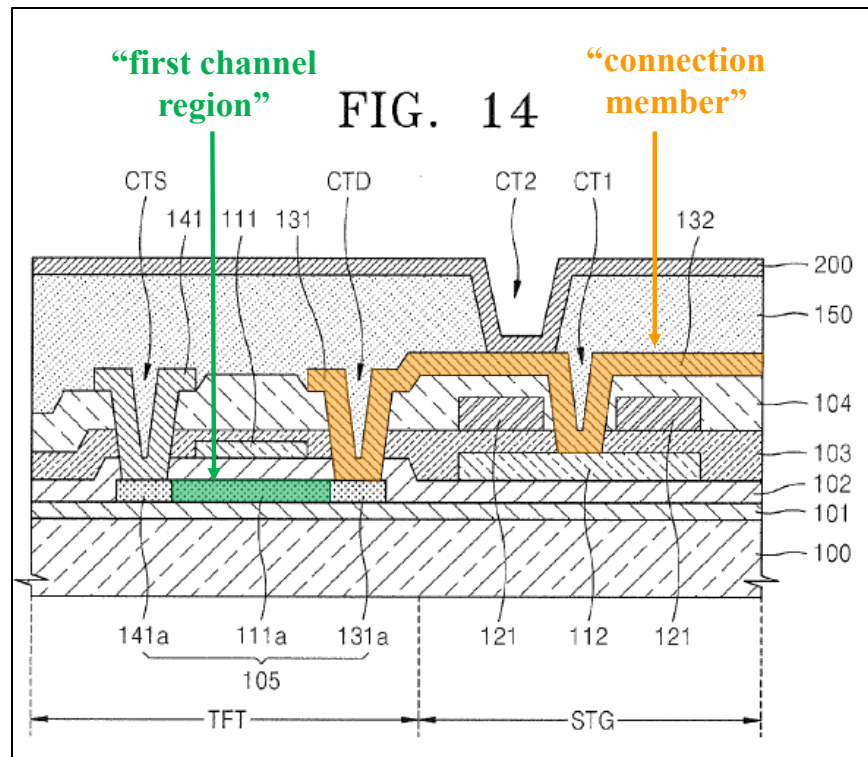
161. Park describes the drain of the switching thin film transistor 4 (part of the “connection member”) in relation to “a first drain electrode (not shown), which is connected to the first drain region 113 . . . are also formed on the first passivation layer 160.” (EX1005, [0034]; *see also* [0007] (“The first drain electrode (not shown) is also connected to the second gate electrode 22.”).) Before describing the drain electrode of the switching thin film transistor 4, it describes the source and drain electrodes shown in Figures 4 and 5. Hence, a POSITA would have understood that the drain electrode of the switching thin film transistor 4 would have a similar configuration as the source and drain electrodes shown in Figures 4 and 5. Because Park states that the drain electrode of the switching film thin transistor 4 is “not shown” and “also formed on the [inter layer 32/]first passivation layer 160,” a POSITA would have understood that the drain electrode

of the switching thin film transistor (part of the “connection member”) overlaps a portion of the corresponding active layer 14/114 (“first channel region”) in a plan view.

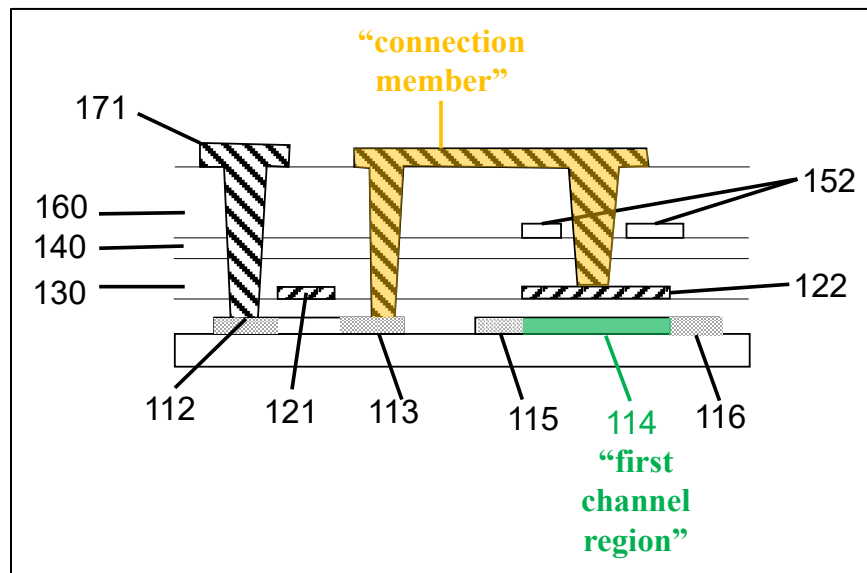
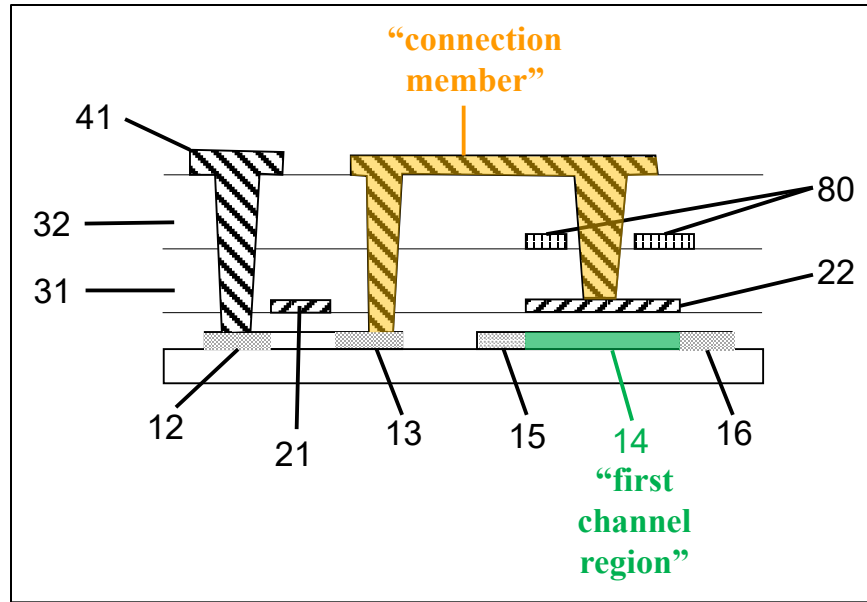
(ii) **Zhan**

162. Zhan teaches a storage electrode 132: “[t]he third storage electrode 132 ... contacts the first storage electrode 112 through a first contact hole (or first contact unit or opening) CT1 ... the third storage electrode 132 extends from the drain electrode 131 of the TFT.” (EX1011, [0048], [0067].) The storage electrode 132 connects the storage electrode 112 to the drain electrode 131a of the TFT, as shown in Figure 14 (below), thereby making it a connection member. Zhan also teaches “[t]he active layer 105 may be formed of an inorganic semiconductor material, such as amorphous silicon or polysilicon, or an organic semiconductor material and may include a source area 141a, a drain area 131a, and a channel area 111a interposed between the source area 141a and the drain area 131a.” (EX1011, [0061].)

163. Figure 14 (annotated below) shows the *storage electrode 132* overlapping a portion of the *channel area 111a*.



164. The figures below show the Park-Zhan combination. In the Park-Zhan combination, as shown in the figures, the *first drain electrode* (“connection member”) extends to the storage capacitor to connect with the first gate electrode 22/122 through a contact hole. The connection member extending to the storage capacitor thereby overlaps the *first channel region 14/114*. A POSITA would have understood that the gate electrode 22/122 overlaps the channel region 14/114 in plan view because in the cross-sectional view the gate electrode 22/122 is shown on top of the channel region 14/114.



8. **Claim 23: “The TFT array substrate of claim 22, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in the plan view.”**

165. Claim 23 is similar to claim 2, which Park and Zhan teach. (See Section IX.B.2.) The table below shows the similarities.

Claim 2	Claim 23
“The TFT array substrate of claim 1, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.”	“The TFT array substrate of claim 22, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in the plan view.”

9. **Claim 24: “The TFT array substrate of claim 23, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and the portion of the connection member is connected with the first gate electrode through the node contact hole.”**

166. Claim 24 is similar to claim 3, which Park and Zhan teach. (See Section IX.B.3.) The table below shows the similarities.

Claim 3	Claim 24
“The TFT array substrate of claim 2, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and the portion of the connection member is connected with the first gate electrode through the node contact hole.”	“The TFT array substrate of claim 23, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and the portion of the connection member is connected with the first gate electrode through the node contact hole.”

10. **Claim 27: “The TFT array substrate of claim 22, further comprising a driving voltage line on the third insulating layer, the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer.”**

167. Park teaches claim 22 as shown in Section IX.A.6.

168. Claim 27 is similar to Claim 11, which Park renders obvious. (See Section IX.A.3.) The table below shows the similarities.

Claim 11	Claim 27
“The TFT array substrate of claim 1, further comprising a driving voltage line on the third insulating layer, wherein the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer.”	“The TFT array substrate of claim 22, further comprising a driving voltage line on the third insulating layer, the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer.”

C. Claims 7-10 Are Obvious Over Park And Osame

1. Summary of Osame

169. Osame discloses an invention that “relates to an electroluminescence (EL) element, and to a method of driving an electronic display manufactured by forming thin-film transistors (hereinafter abbreviated as TFTs) on a substrate. Particularly, the invention relates to a light-emitting device which uses semiconductor elements (elements formed from a semiconductor thin film).” (EX1014, [0002].)

170. Osame recognized that in organic EL devices “the capacitance C_s tends to be large and the light-emitting area of organic EL tends to be small correspondingly. In addition to the capacity C_s , shapes, numbers, and arrangements of TFTs, wirings, contacts, partitioning walls, and the like constituting pixels become factors for decreasing the light-emitting areas. As the light-emitting area decreases, the current density increases and the reliability of the organic EL element decreases seriously.” (EX1014, [0007].) “Further, if an opening portion is formed in a complex shape in order to increase aperture ratio as

much as possible, a shrink of the organic EL portion may be promoted.” (*Id.*, [0010].) Osame explains that to promote constant current flow into the EL and avoid changes in brightness, “the channel lengths of the driving TFTs must be maintained long in the pixels. Further, the aperture ratio decreases as the size of the driving TFT increases.” (*Id.*, [0022]-[0029].)

171. Osame “provides a light-emitting device which realizes a high aperture ratio in which the quality of image is little affected by the variation in the characteristics of TFTs.” (EX1014, Abstract, [0030].) Osame explains “a large holding capacitor C_s is not provided in the pixel portion but, instead, the channel length and the channel width of the driving TFTs are increased, and the channel capacitance is utilized as C_s .” (EX1014, Abstract; *see also id.*, [0032].) “Therefore, the drain currents of the driving TFTs are little affected by the variation in the threshold voltage.” (*Id.*)

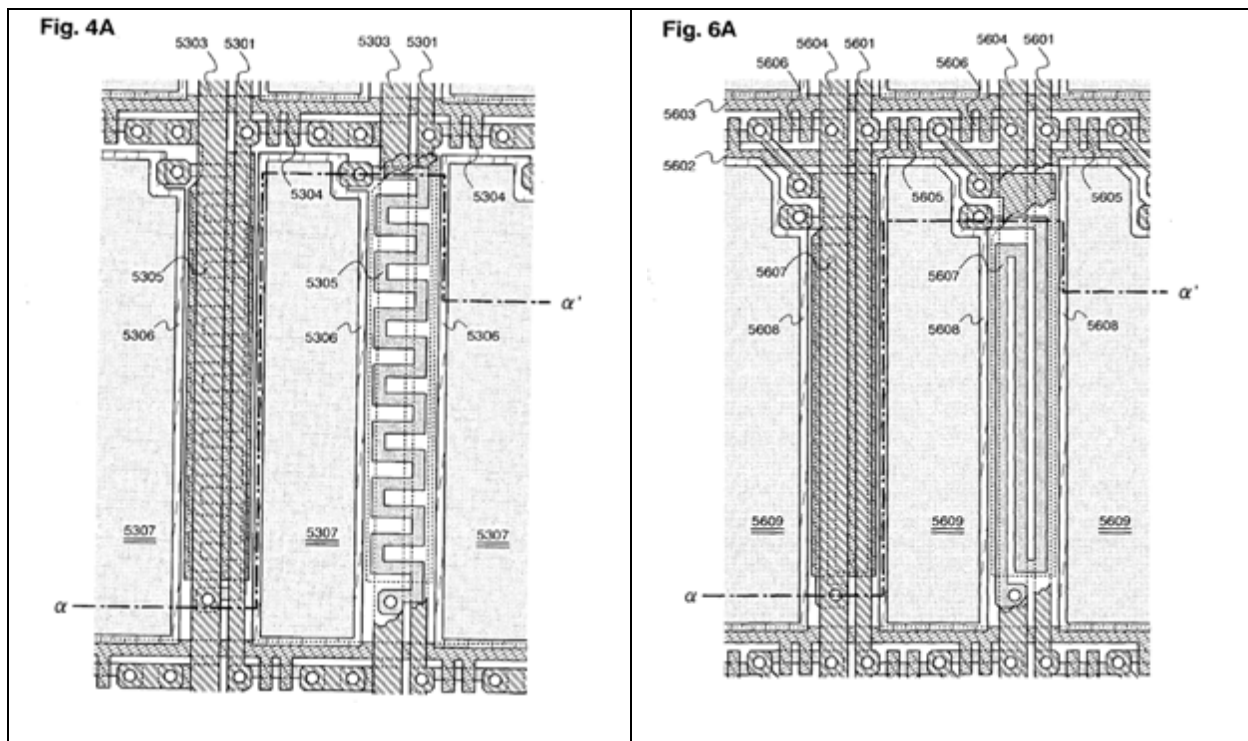
172. Referring to Figure 1, Osame discloses an embodiment of the invention with two transistors in a pixel where the “driving TFT 5005 has an increased channel length and an increased channel width so as to also work as a holding capacitor and, further, to suppress variation in the characteristics.” (EX1014, [0083].) Osame discloses the semiconductor layer can have different shapes. For example, “FIG. 4A illustrates an example of a semiconductor layer of

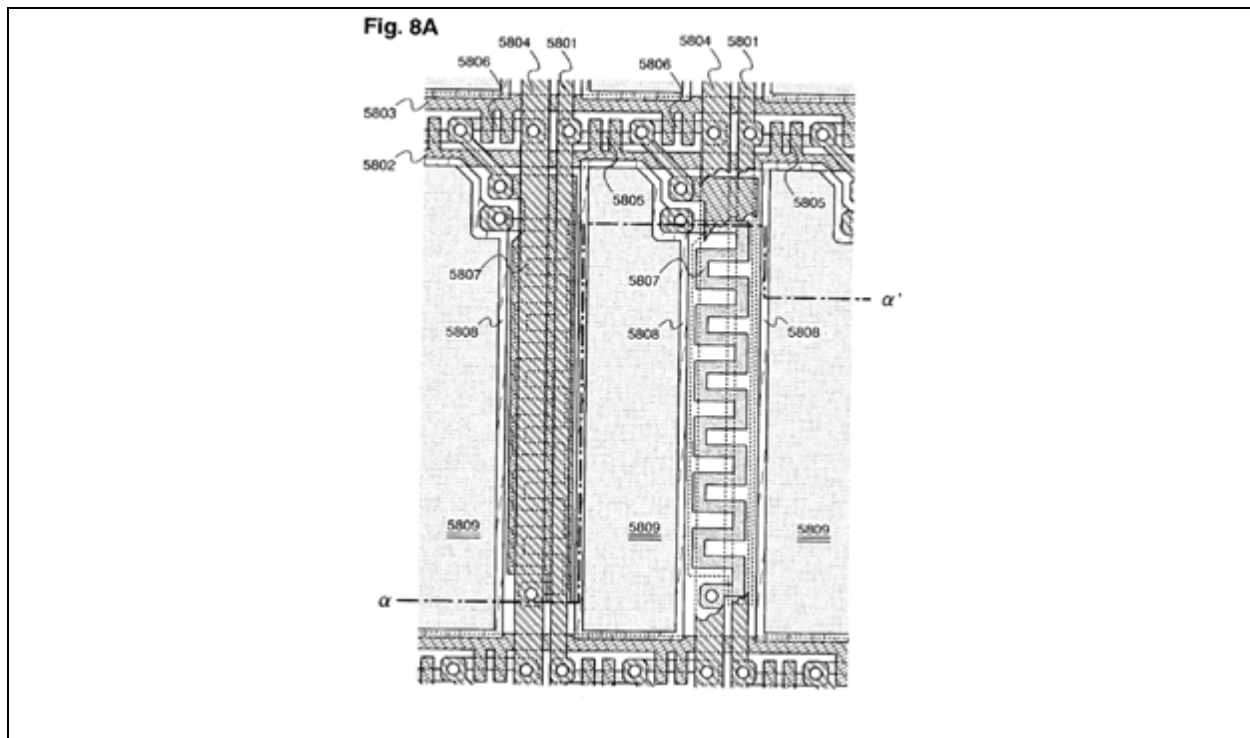
a different shape of pattern instead of the semiconductor layer of FIG. 1A.”

(EX1014, [0114]).

173. Referring to Figure 5, Osame discloses an embodiment of the invention with three transistors in a pixel. (EX1014, [0085], [0115]). Osame discloses this embodiment can also have semiconductor layers in different shapes. For example, FIGS. 6A and 8A each “illustrate[] an example of a semiconductor layer of a different shape of pattern instead of the semiconductor layer of FIG. 5A.” (EX1014, [0119], [0121]).

174. Figures 4A, 6A, and 8A (below) show different shapes disclosed in Osame for the semiconductor layers.

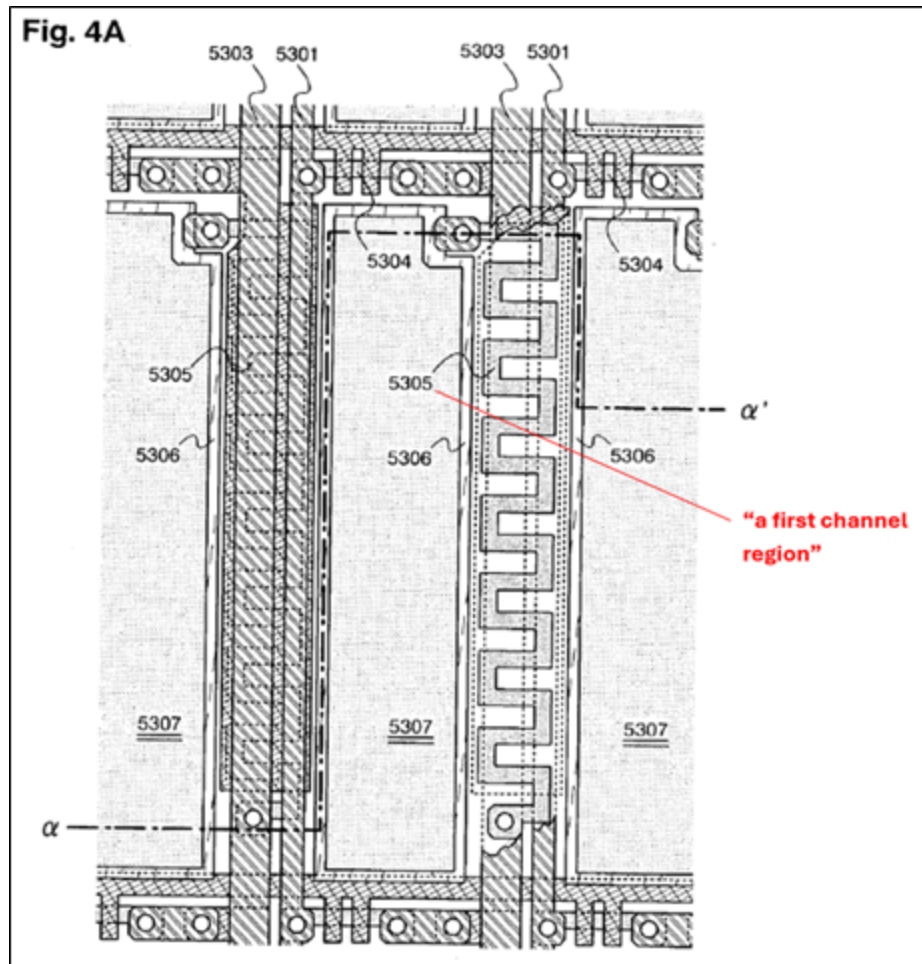




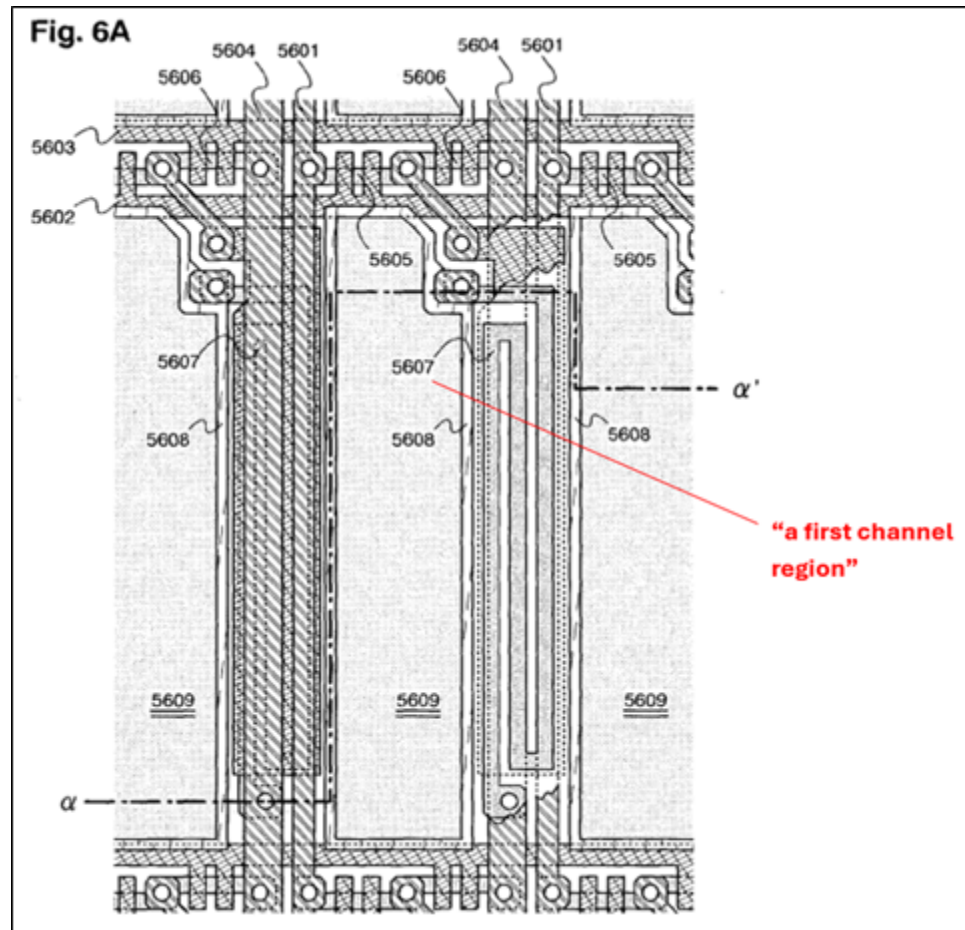
2. Claim 7: “The TFT array substrate of claim 1, wherein the first channel region includes a bent portion.”

175. Park teaches claim 1 as shown above in Section IX.A.2.

176. Osame further discloses “the first channel region includes a bent portion.” For example, as shown in Figure 4A (annotated below), Osame discloses that “[t]he semiconductor layer may be formed in a meandering shape in the horizontal direction as represented by the driving TFT 5305.” (EX1014, [0114].)

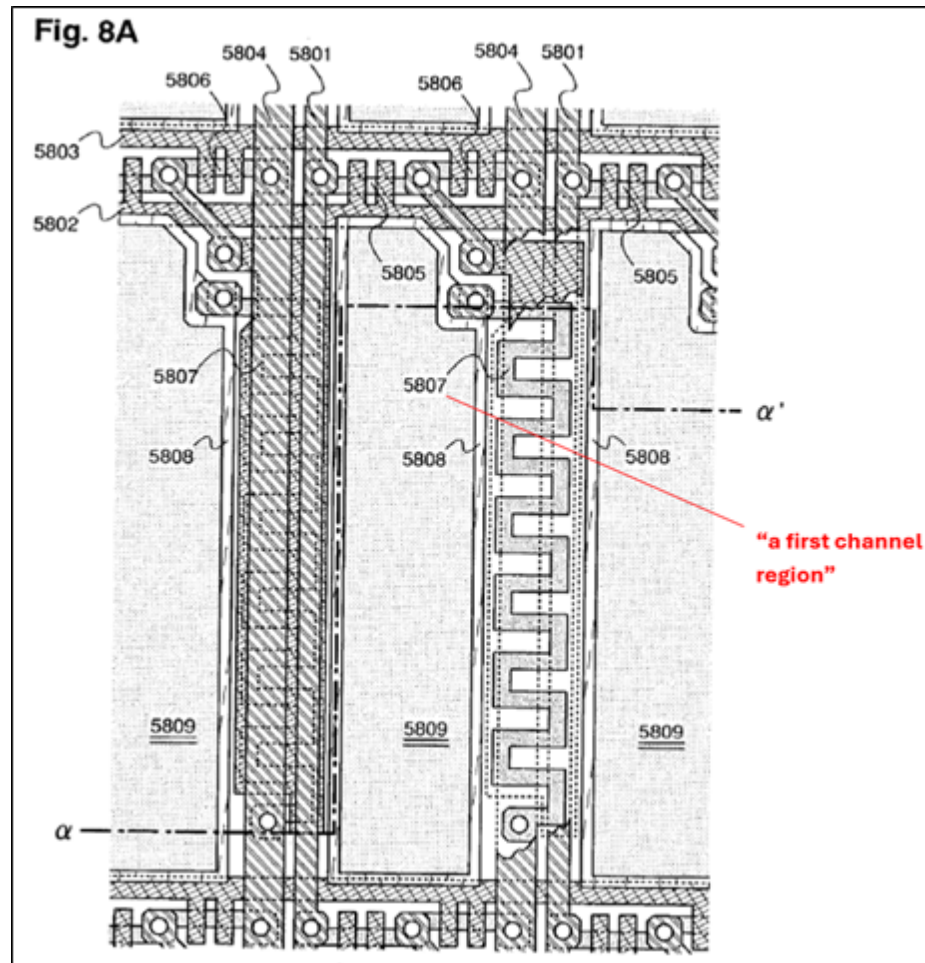


178. As another example, Figure 6A (annotated below) shows that Osame discloses that “[t]he semiconductor layer may be formed being meandered in the vertical direction as represented by a driving TFT 5607.” (EX1014, [0119].)



179. Osame further discloses the benefit of this configuration: “[w]ith the semiconductor layer being thus formed, the channel length of the driving TFT 5607 can be further increased without decreasing the aperture ratio.” (EX1014, [0119].)

180. As another example, Figure 8A (annotated below) shows that “[t]he semiconductor layer may be formed in a meandering shape as represented by a driving TFT 5807.” (EX1014, [0121].)



181. Osame further discloses the benefit of this configuration: “[w]ith the semiconductor layer being thus formed, the channel length of the driving TFT 5807 can be further increased and the channel width can be increased to some extent without decreasing the aperture ratio.” (EX1014, [0121].)

a. Motivation to combine Park and Osame

182. It would have been obvious to a POSITA at the time of the '483 patent to combine the teachings of Park and Osame. Park and Osame disclose light-emitting devices and configurations. Park discloses “an active matrix organic electro luminescent display (ELD) device in which a storage capacitance of a storage capacitor is increased without reducing an aperture ratio.” (EX1005, [0017].) Similarly, Osame discloses a “light-emitting device which realizes a high aperture ratio and in which the quality of image is little affected by the variation of the driving TFTs.” (EX1014, [0030].) Both use the same pixel circuit having two transistors and one storage capacitor. (EX1005, Fig. 1, [0006]; EX1014, Fig. 12, [0007].) Park’s storage capacitor is disposed above the transistor. Its gate electrode 22/122 forms the storage capacitor electrode, thereby increasing the storage capacitance without reducing the aperture ratio. (EX1005, [0007], [0011], [0015], [0034].) Osame’s capacitor is between the gate electrode and the current supply line of the driving TFT, which is utilized as part of the holding capacitor C_s and the channel capacitance is utilized as the capacitance between the gate electrode and the channel region, thereby achieving an increasing in aperture ratio. (EX1014, Abstract, [0082], [0083], [0089], [0097], [00105].) Thus, Park and Osame are from the same field of endeavor and reasonably pertinent to the same

technical problem of increasing aperture ratio without compromising image quality.

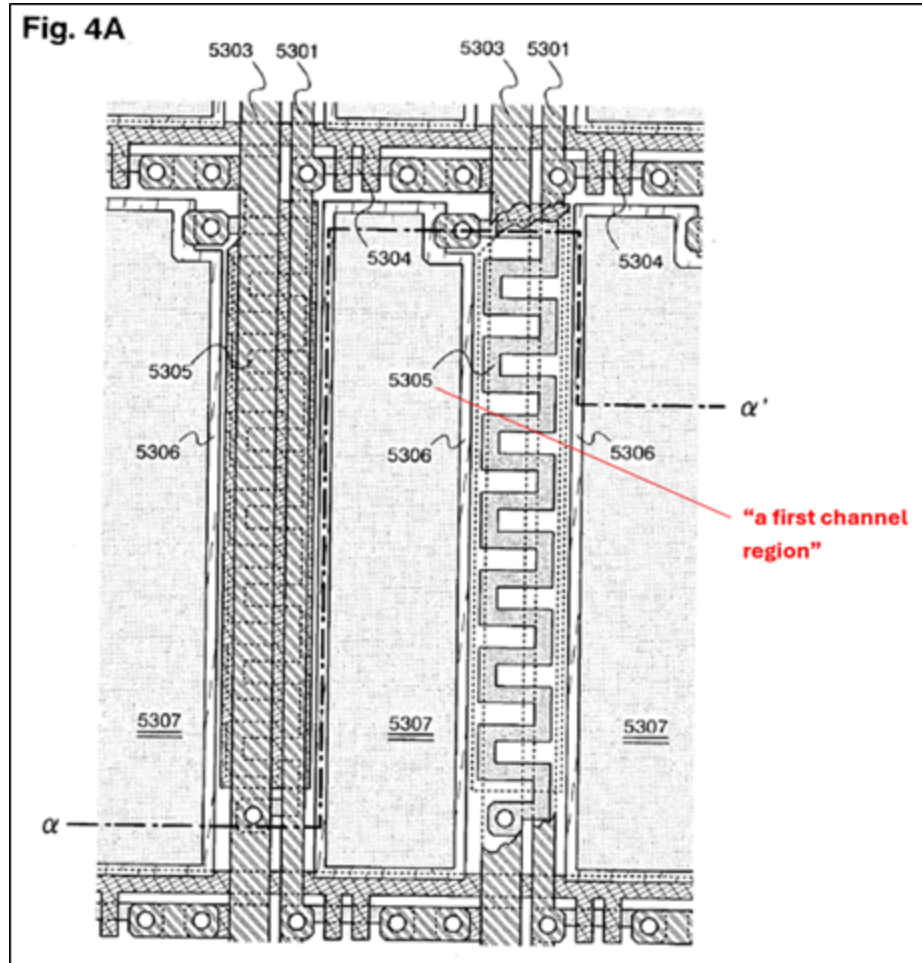
183. Osame discloses light-emitting devices including different shapes for increasing TFT channel length and channel width, without decreasing aperture ratio. Osame's technical features may be combined with the Park's teachings, and there would have been a reasonable expectation of success to generate a smaller light-emitting device where the storage capacitor has an increased capacitance, without decreasing the device's aperture ratio. Osame, among other prior art, has demonstrated this success, and combining with Park would still lead to a reasonable expectation of success given that the devices of Park and Osame are similar.

184. A POSITA would be motivated to use Osame's techniques to improve the similar device of Park in the same way. Further, it would have been obvious to try combining the teachings of Park and Osame because Osame teachings of changing the shape of the semiconductor layer's channel region is a simple substitution and offers a number of configurations to try. Thus, it would have been obvious to a POSITA to combine the teachings of Park and Osame.

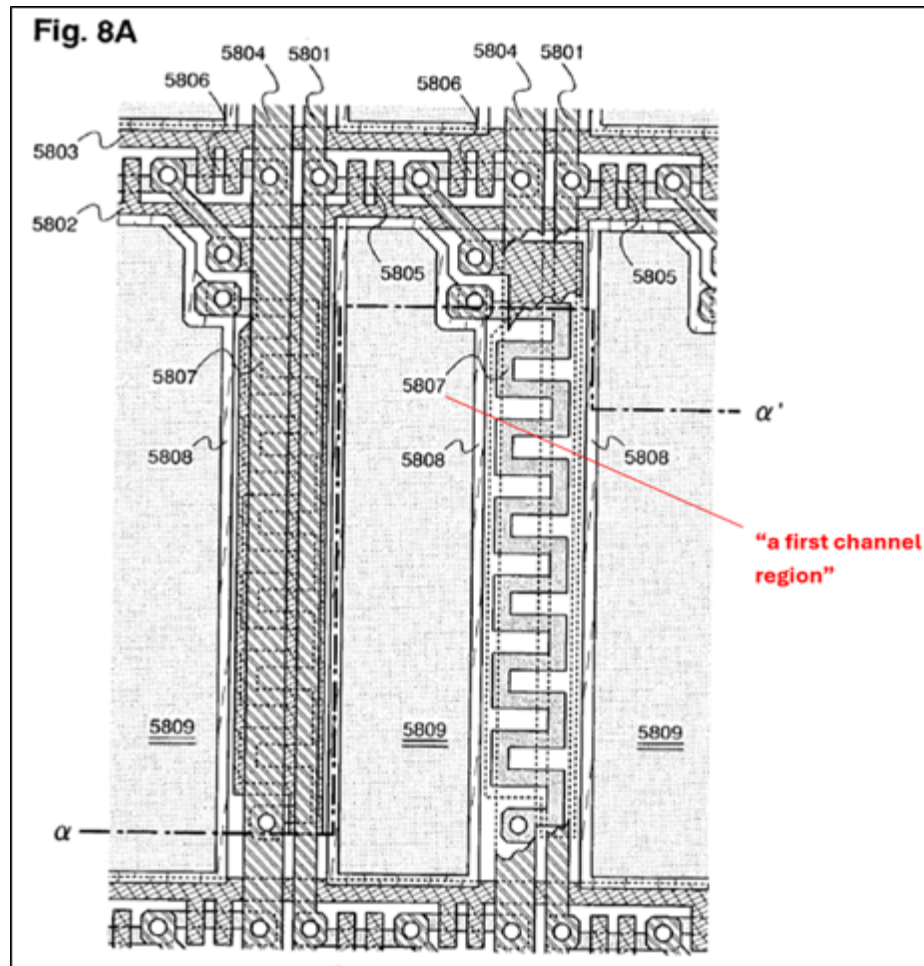
3. Claim 8: “The TFT array substrate of claim 7, wherein the first channel region includes at least two bent portions.”

185. Park and Osame teach claim 7 as shown above in Section IX.C.2. As shown for element 1[b], Park teaches a channel region of a driving transistor (“first channel region”).

186. Osame teaches “the first channel region includes at least two bent portions.” For example, Osame discloses that “[t]he semiconductor layer may be formed in a meandering shape in the horizontal direction as represented by the driving TFT 5305.” (EX1014, [0114].) As shown in Figure 4A (annotated below), there are at least two bent portions in the channel of the driving TFT 5305.



187. As another example, Figure 6A (annotated below) of Osame shows that “[t]he semiconductor layer may be formed being meandered in the vertical direction as represented by a driving TFT 5607.” (EX1014, [0119].)



189. It would have been obvious to a POSITA to combine the teachings of Park and Osame. (See Section IX.C.2.)

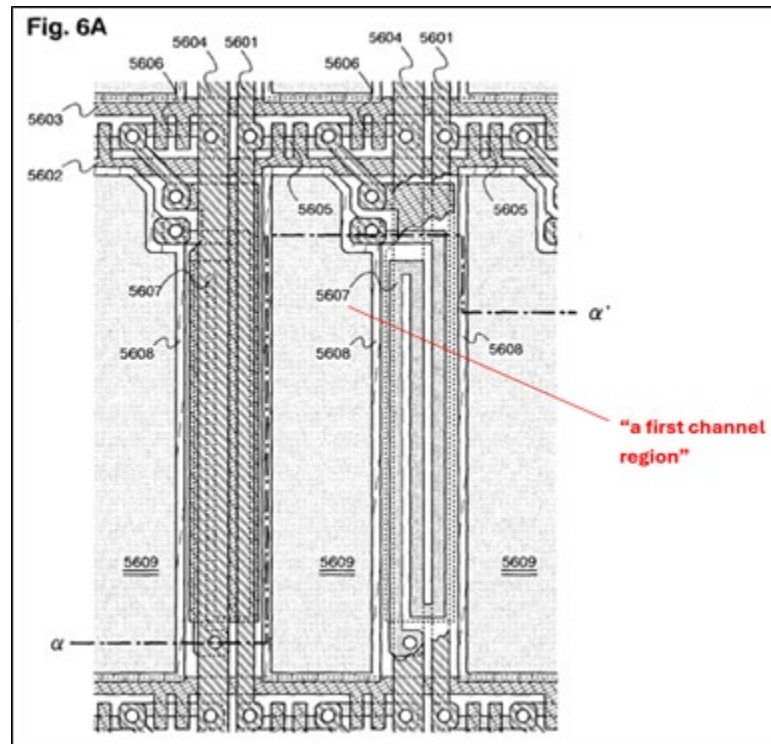
4. Claim 9: “The TFT array substrate of claim 7, wherein the first channel region is curved in an ‘S’ shape.”

190. Park and Osame teach claim 7 as shown above in Section IX.C.2.

191. Osame teaches “the first channel region is curved in an ‘S’ shape.”

For example, Osame discloses that “[t]he semiconductor layer may be formed being meandered in the vertical direction as represented by a driving TFT 5607.”

(EX1014, [0119].) As shown in Figure 6A (annotated below), the channel of the driving TFT 5807 is curved in an ‘S’ shape.



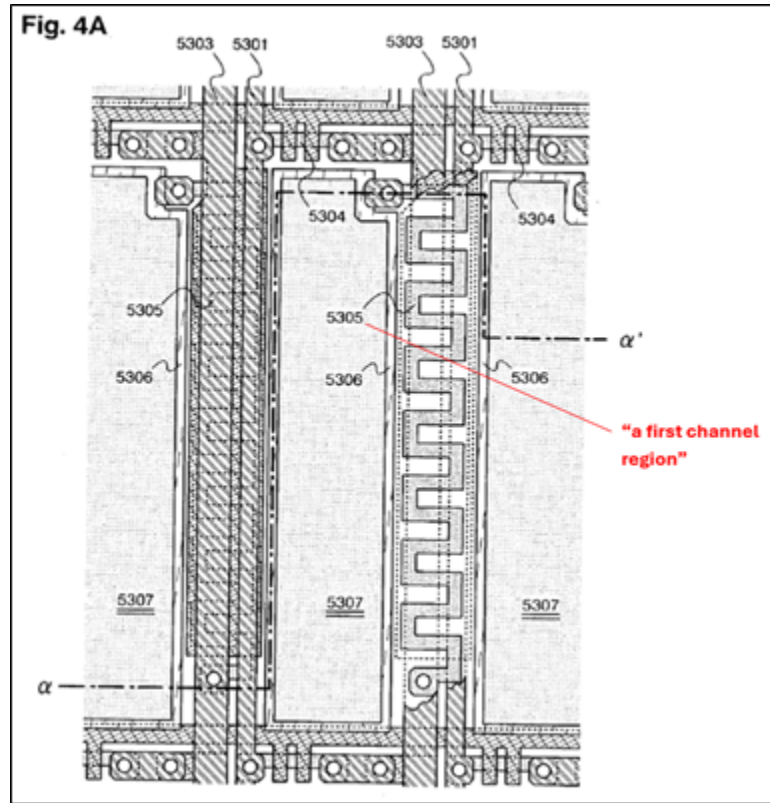
192. It would have been obvious to a POSITA to combine the teachings of Park and Osame. (See Section IX.C.2.)

5. Claim 10: “The TFT array substrate of claim 7, wherein the first channel region is curved in a zigzag shape.”

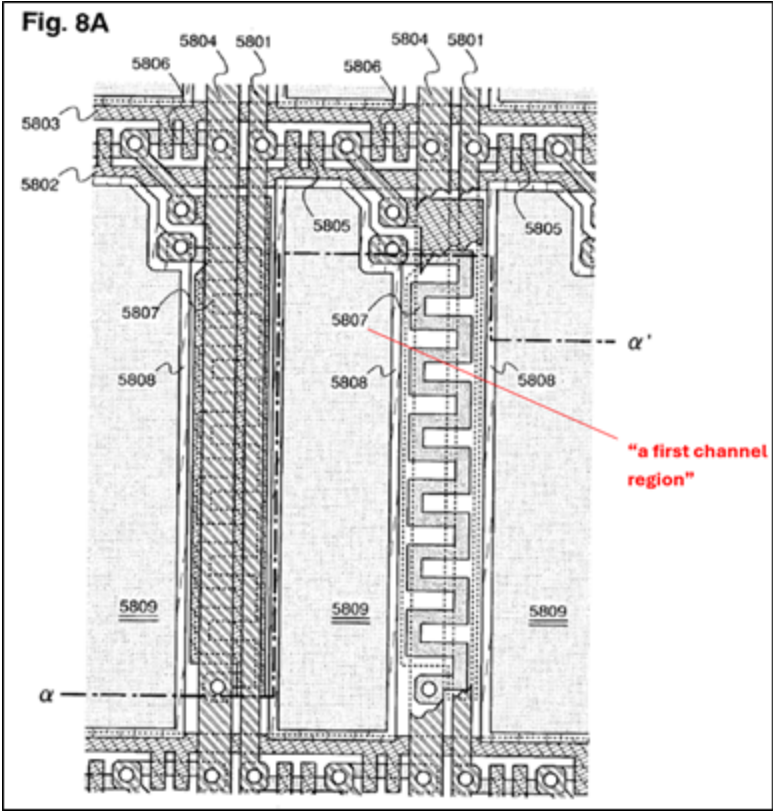
193. Park and Osame teach claim 7 as shown above in Section IX.C.2.

194. Osame teaches “the first channel region is curved in a zigzag shape.” For example, Osame discloses that “[t]he semiconductor layer may be formed in a meandering shape in the horizontal direction as represented by the driving TFT

5305.” (EX1014, [0114].) As shown in Figure 4A below, the channel of the driving TFT 5305 is curved in a zigzag shape.



195. As another example, referring to Figure 8A, Osame discloses that “[t]he semiconductor layer may be formed in a meandering shape as represented by a driving TFT 5807.” (EX1014, [0121].) As shown in Figure 8A below, the channel of the driving TFT 5807 is curved in a zigzag shape.



196. It would have been obvious to a POSITA to combine the teachings of Park and Osame. (See Section IX.C.2.)

D. Claims 25 And 26 Are Obvious Over Park, Zhan, And Osame

1. **Claim 25: “The TFT array substrate of claim 22, wherein the first channel region includes a bent portion.”**

197. Claim 25 is similar to claim 7, which Osame teaches. (See Section IX.C.2.) The table below shows the similarities.

Claim 7	Claim 25
“The TFT array substrate of claim 1, wherein the first channel region includes a bent portion.”	“The TFT array substrate of claim 22, wherein the first channel region includes a bent portion.”

2. Claim 26: “The TFT array substrate of claim 25, wherein the first channel region is curved in a zigzag shape.”

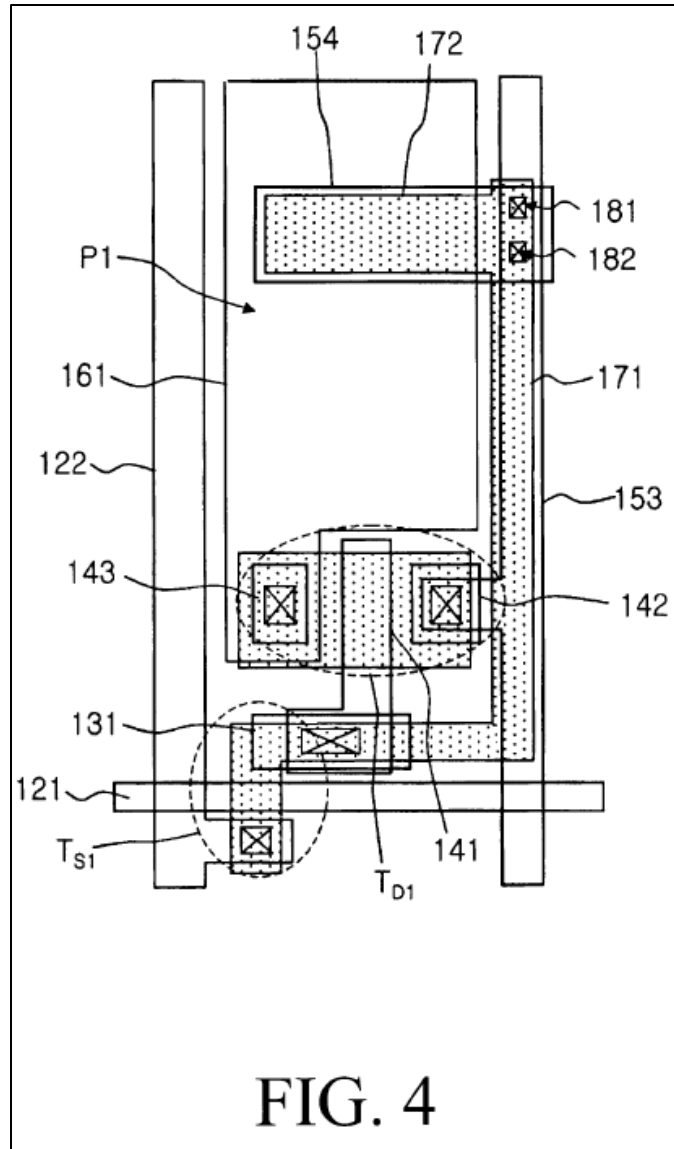
198. Claim 26 is similar to claim 10, which Osame teaches. (See Section IX.C.5.) The table below shows the similarities.

Claim 10	Claim 26
“The TFT array substrate of claim 7, wherein the first channel region is curved in a zigzag shape.”	“The TFT array substrate of claim 25, wherein the first channel region is curved in a zigzag shape.”

E. Claims 12 And 13 Are Obvious Over Park And Ko

1. Summary of Ko

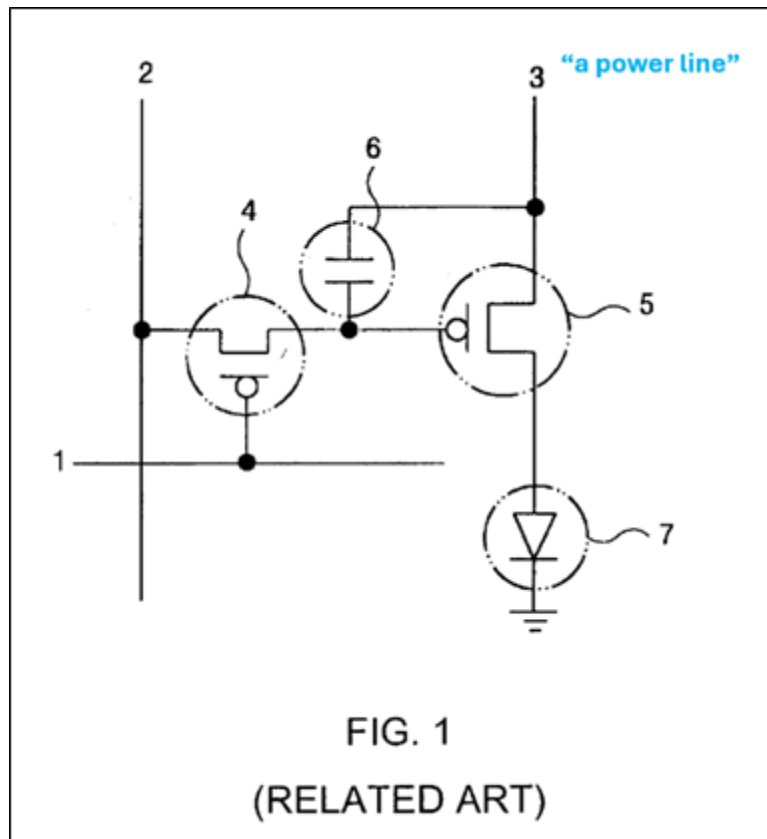
199. Ko discloses “active matrix organic electroluminescence display (ELD) device and a method of fabricating the same.” (EX1009, 1:12-15.) As Ko explains, “[b]ecause the power line 153 is formed of an opaque material, and the first capacitor electrode 154 is formed of transparent conductive material, in the active matrix organic electroluminescence display device according to the second embodiment, an electrical resistance of the power line is decreased and, an aperture ratio is increased at the same time.” (EX1009, 7:44-50.) Figure 4 (below) shows Ko’s active matrix organic ELD device comprising a power line 153, a first capacitor electrode 154, and first and second contact holes 182 and 182. The first capacitor electrode 154 and power line 153 connect to and overlap each other. (EX1009, 7:38-43.)



2. Claim 12: “The TFT array substrate of claim 11, wherein the first contact hole includes a plurality of first-sub contact holes.”

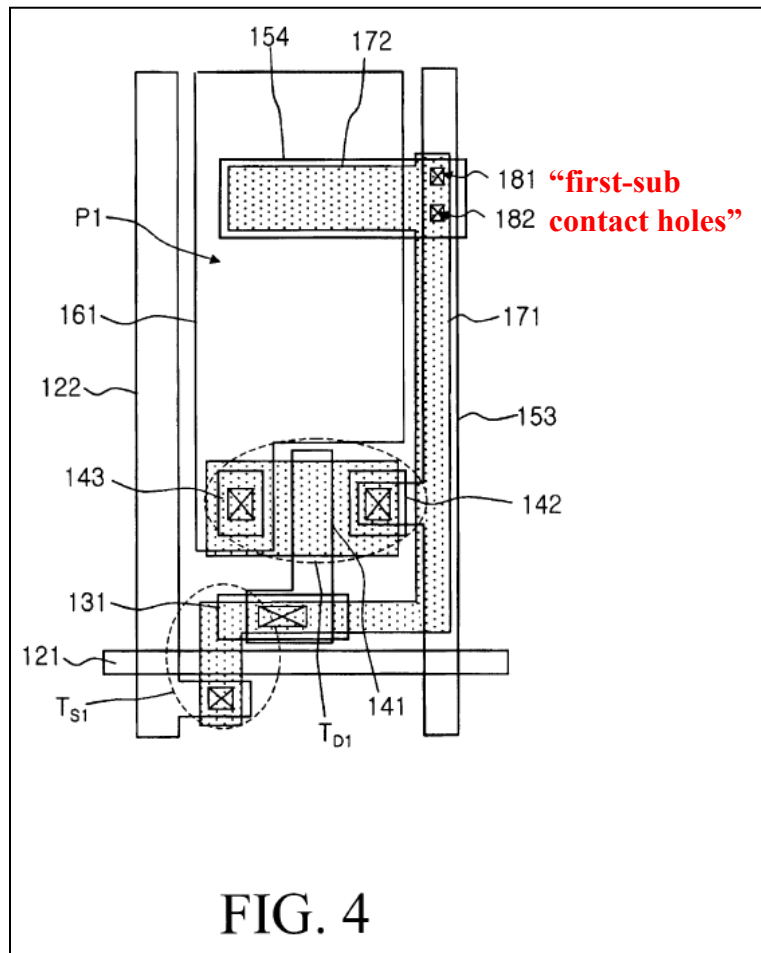
200. Park teaches claim 11 as shown above in Section IX.A.3. Park teaches a “driving voltage line” 3 in Figure 1, which is connected to the upper electrode of the capacitor and the source of the thin film transistor T5. Park describes “a power line (not shown), which is connected to the second source

electrode 173, are also formed on the first passivation layer 160. The second source electrode 173 may be *extended from the power line* (not shown) or may be formed of a portion of the power line.” (EX1005, [0034] (emphasis added).) Therefore, Park discloses a driving voltage line connected to a metal pattern. (See Section IX.A.3).



201. Ko teaches “the first contact hole includes a plurality of first-sub contact holes.” For example, Ko discloses “[f]irst and second contact holes 181 and 182 are formed at a portion where the first capacitor electrode 154 and the power line 153 overlap one another. The first capacitor electrode 154 is connected to the power line 153 through the first and second contact holes 181 and 182.”

(EX1009, 7:38-43.) Figure 4 (below) shows the *first and second contact holes 181 and 182*.



b. Motivation to combine Park and Ko

202. It would have been obvious to a POSITA at the time of the '483 patent to combine the teachings of Park and Ko. Park and Ko both teaches light-emitting devices comprising power lines, data lines, and gate lines, and contact holes. Park discloses “an active matrix organic electro luminescent display (ELD) device” that includes a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6, a light emitting diode (LED) 7, a power line 3, a

data line 2, and a gate line 1 and contact holes. (EX1005, [0006], [0007], [0034], Figs. 1, 4, and 5.) Ko discloses “an active matrix organic electro-luminescent display device” that includes a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6, a light emitting diode (LED) 7, a power line 3, a data line 2, a gate line 1, and contact holes 181 and 182. (EX1009, 2:1-20, 7:38-43.) Thus, Park and Ko are from the same field of endeavor.

203. Park teaches a display that displays high quality images by increasing the storage capacitance of the display without decreasing aperture ratio. (EX1005, [0015].) Ko teaches decreasing the electrical resistance of the power line and increasing the aperture ratio, resulting in improving the performance and quality of the light-emitting display devices. (EX1009, 7:44-50, 9:50-58.) Ko explains that “a picture quality of displayed images may be deteriorated due to an increased resistance of a wiring.” (EX1009, 7:18-20. Ko’s solution is to include a power line 153 formed of an opaque metal material and a first capacitor electrode 154 formed of a transparent conductive material. Ko configures the power line 153 and first capacitor electrode 154 such that they overlap one another and connect to each other through first and second contact holes 181 and 182. (EX1009, 7:33-43.)

204. Ko’s technical features may be combined with Park’s OLED to result in an OLED having improved performance and quality due to increased aperture ratio and decreased wiring resistance. A POSITA would have been able to easily

combine Park and Ko given the similarities of their circuits. Ko's circuit comprises a capacitor 6 including an upper electrode, and a lower electrode connected to the drain of a switching thin transistor 4 and the gate of a driving thin film transistor 5. (EX1009, 2:10-13, Fig. 1.) "A gate electrode of the switching thin film transistor 4 is connected to the gate line 1, and the source electrode is connected to the data line 2. A drain electrode of the switching thin film transistor 4 is connected to a gate electrode of the driving thin film transistor 5. A drain electrode of the driving thin film transistor 5 is connected to an anode electrode of the light emitting diode (LED) 7. A source electrode of the driving thin film transistor 5 is connected to a power line 3, and a cathode electrode of the light emitting diode (LED) 7 is grounded. A storage capacitor 6 is connected to the gate electrode and the source electrode of the driving thin film transistor 5." (EX1009, 2:9-20.) This is similar to Park's circuit, which also comprises a capacitor 6 including an upper electrode and a lower electrode connected to the drain of a switching thin film transistor 4 and a gate of a driving thin film transistor 5. (EX1005, [0006], Fig. 1.) And just like Ko, in Park, "[a] gate electrode of the switching thin film transistor 4 is connected to the gate lane 1 and a source electrode is connected to the data line 2. A drain electrode of the switching thin film transistor 4 is connected to a gate electrode of the driving thin, film transistor 5 and a drain electrode of the driving thin film transistor 5 is connected to an anode

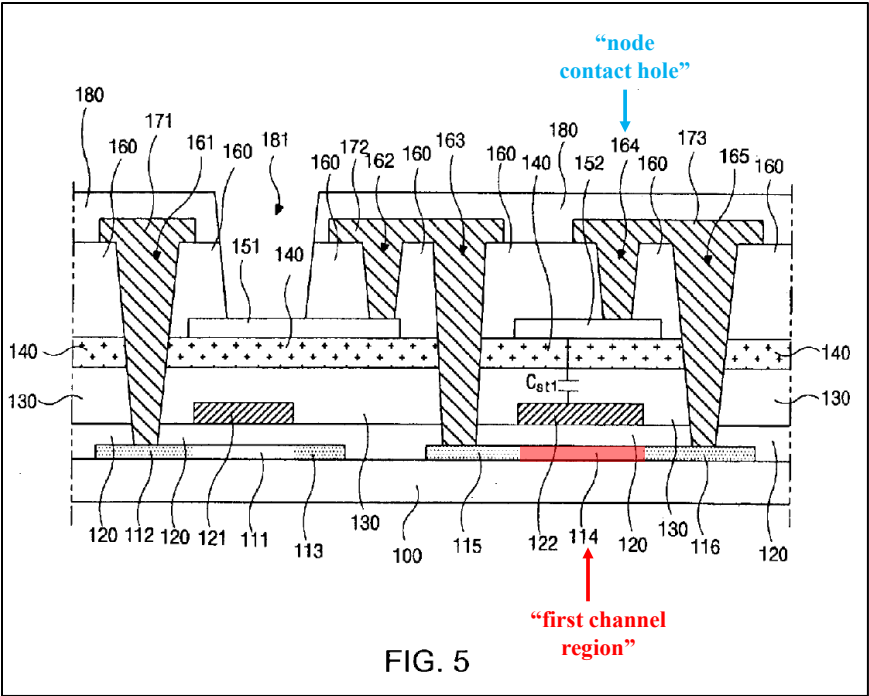
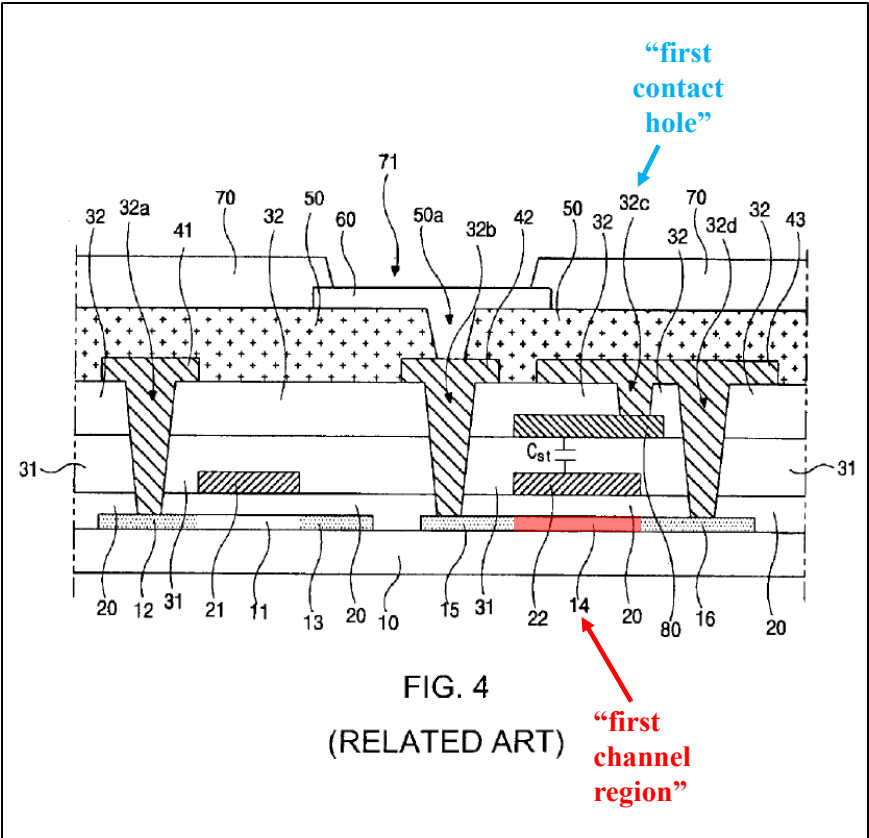
electrode of the light emitting diode (LED) 7. A source electrode of the driving thin film transistor 5 is connected to a power line 3 and a cathode electrode of the light emitting diode (LED) 7 is grounded to earth. A storage capacitor 6 is connected to the gate electrode and the source electrode of the driving thin film resistor 5.” (EX1005, [0006].) Given the overlap between Park and Ko, and that the prior art has already known and demonstrated such techniques with success, there would have been a reasonable expectation of success. Thus, it would have been obvious to a POSITA to combine the teachings of Park and Ko.

3. Claim 13: “The TFT array substrate of claim 12, wherein at least one of the plurality of first-sub contact holes overlaps the first channel region in a plan view.”

205. Park and Ko teach claim 12 as shown above in Section IX.D.2.

206. As shown for claim 11, Park discloses contact hole 32c/164 (“first contact hole”). As shown for element 1[b], Park discloses an active layer 14/114 (“first channel region”).

207. Park teaches a “contact hole[] overlaps the first channel region in a plan view.” Figures 4 and 5 (below) show that the *contact hole 32c/164* overlaps with the *active layer 14/114*. (EX1005, [0015].)



F. Claims 28 And 29 Are Obvious Over Park, Zhan, And Ko

1. Claim 28: “The TFT array substrate of claim 27, wherein the first contact hole includes a plurality of first-sub contact holes.”

208. Claim 28 depends from claim 22, which Park and Zhan teach. Claim 28 is similar to claim 12, which Ko teaches. (See Section IX.D.2.) The table below shows the similarities.

Claim 12	Claim 28
“The TFT array substrate of claim 11, wherein the first contact hole includes a plurality of first-sub contact holes.”	“The TFT array substrate of claim 27, wherein the first contact hole includes a plurality of first-sub contact holes.”

2. Claim 29: “The TFT array substrate of claim 28, wherein at least one of the plurality of first-sub contact holes overlaps the first channel region in the plan view.”

209. Claim 29 depends from claim 22, which Park and Zhan teach. Claim 29 is similar to claim 13, which Ko teaches. (See Section IX.D.3.) The table below shows the similarities.

Claim 13	Claim 29
“The TFT array substrate of claim 12, wherein at least one of the plurality of first-sub contact holes overlaps the first channel region in a plan view.”	“The TFT array substrate of claim 28, wherein at least one of the plurality of first-sub contact holes overlaps the first channel region in the plan view.”

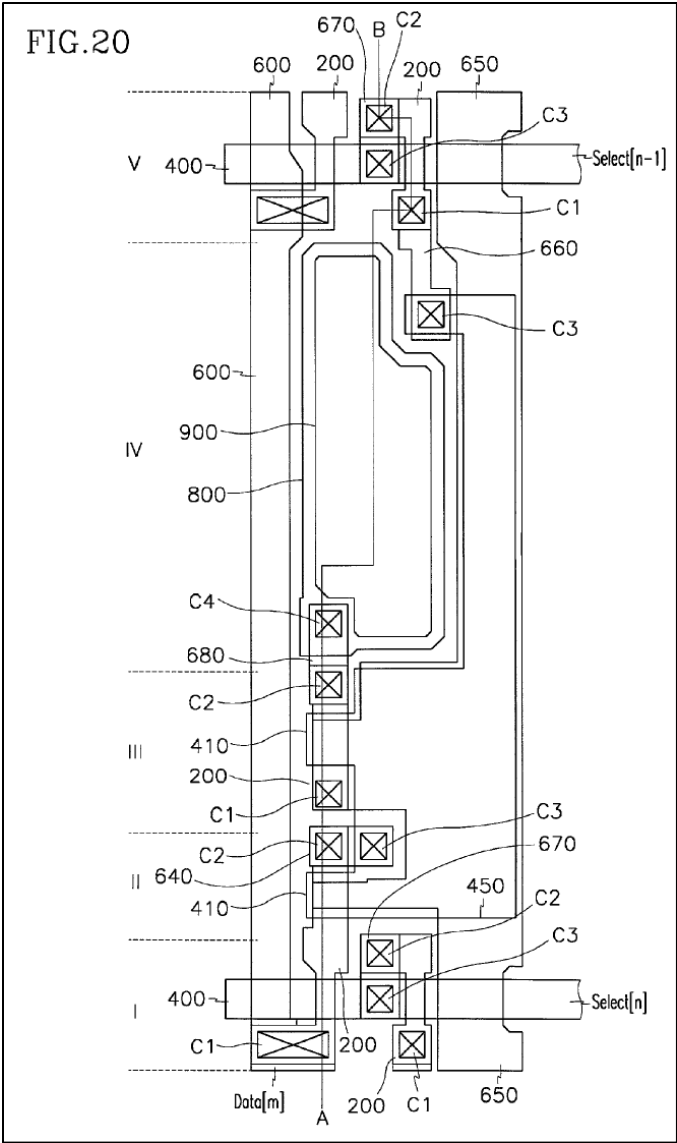
G. Claims 17-19 Are Obvious Over Park And Kwon

1. Summary of Kwon

210. Kwon discloses “an organic EL display (OELD), its driving methods and a pixel circuit that can compensate for deviation of the threshold voltage of a

211. Figure 7 (below) shows Kwon's pixel circuit. Figures 20 and 21 (below) show plan and cross-sectional views of Kwon's OLED.

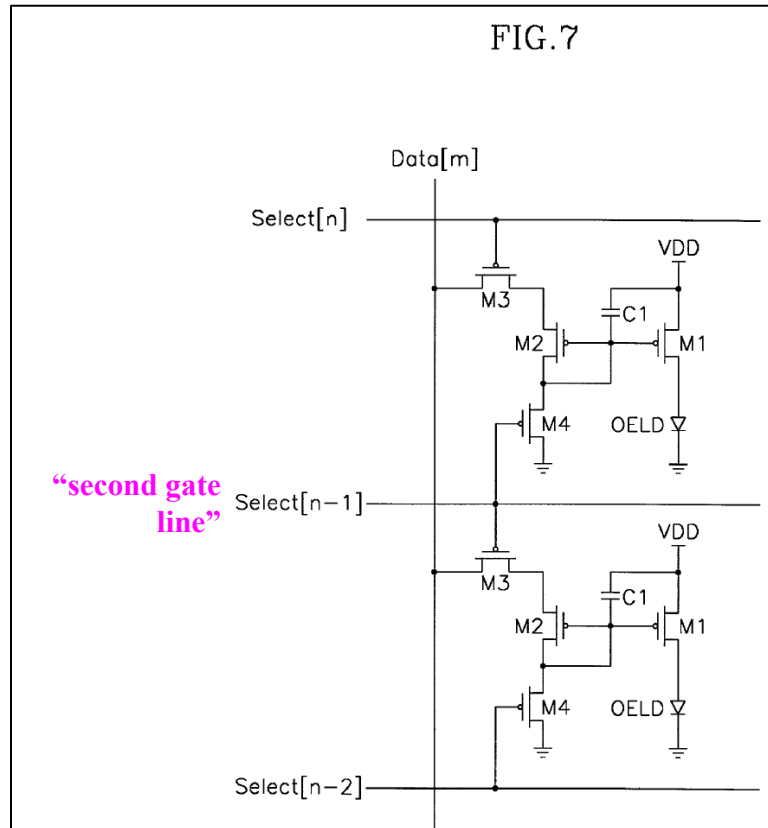




a. 17[a]: “The TFT array substrate of claim 14, further comprising a second gate line, and”

213. Kwon teaches “a second gate line.” For example, Kwon discloses “an external reset signal Reset is supplied to the gate of the transistor M4 to initialize the node A into a ground level.” (EX1006, [0060].) Figure 7 (annotated below) shows Kwon’s pixel circuit comprising a “Select Signal Select[n-1] of the previous Scan line instead of an additional external reset Signal Reset, [that] supplies the select signal Select[n-1] to the gate of the transistor M4.” (EX1006, [0063].) As shown in the figure, the gate of transistor M4 is coupled to the previous Select[n-1]

line, which turns on the transistor M4 in response to a previous signal on *Select[n-1]* line.



a. Motivation to combine Park and Kwon

214. It would have been obvious to a POSITA at the time of the '483 patent to combine the teachings of Park with Kwon. Park and Kwon disclose light emitting devices and pixel circuits to operate these light emitting devices. Park discloses “an active matrix organic electro luminescent display (ELD) device having thin film transistors.” (EX1005, [0017].) Kwon discloses “an organic electroluminescent (EL) display, a driving method of the EL display and a pixel circuit of the EL display.” (EX1006, [0002].) Park teaches a pixel circuit

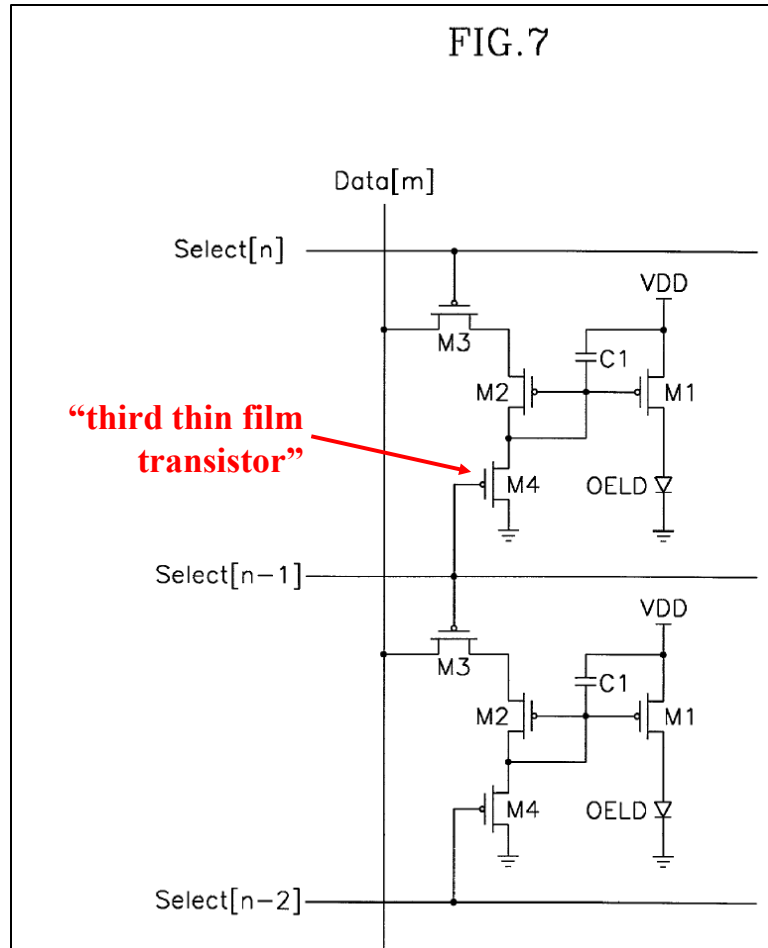
comprising “a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7.” (EX1005, [0006].) Kwon similarly teaches a “pixel circuit compris[ing] a current supplying transistor M1 and a threshold voltage compensation transistor M2 of PMOS transistors, and switches S1 and S2 of PMOS transistors M3 and M4.” (EX1006, [0056].) Thus, Park and Kwon are in the same field of endeavor.

215. Kwon explains that its teachings apply to a conventional pixel circuit: “it is difficult for the conventional pixel circuit to achieve high gray scale because the threshold voltage V of the TFT varies depending on the manufacturing process thereof.” (EX1006, [0011].) A POSITA would have understood that Park’s teachings similarly applies to a conventional pixel circuit. (EX1005, Fig. 1 (“Related Art”).) Kwon then teaches a “pixel circuit that can compensate for deviation of the threshold voltage of a thin film transistor (TFT) and achieve high gray scale display when driving the pixels of the OLED by using the TFT.” (EX1006, [0002].) The pixel circuit includes an additional transistor M4 that resets the gate voltage of the driving transistor M1 and a threshold voltage compensation transistor M1 to achieve high gray scale display. (EX1006, [0056]-[0057].) These technical features may be combined with the teachings of Park to generate a display device with high gray scale display. The display device may include circuitry in the pixel circuit that compensates for deviations in the

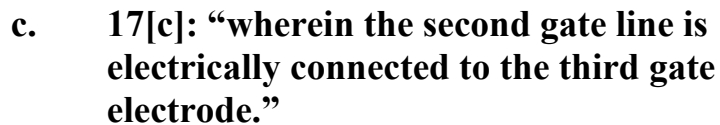
threshold voltage of the driving TFT, resulting in a display device with high gray scale display. There would have been a reasonable expectation of success because such techniques were known in the prior art and have been successfully demonstrated, and further there is an overlap among Park and Kwon including with their circuits and that they are used for active matrix display devices. Because Park and Kwon have similar circuits, a POSITA would have been motivated to use the technique disclosed in Kwon to improve the similar devices of Park in the same way. A POSITA would have been motivated to combine these technical features of Kwon with the teachings of Park and would have had a reasonable expectation of success.

- b. 17[b]: “a third thin film transistor, the third thin film transistor including a third gate electrode and a third channel region overlapping the third gate electrode, the third gate electrode and the third channel region being spaced apart from each other with the first insulating layer therebetween, and”**

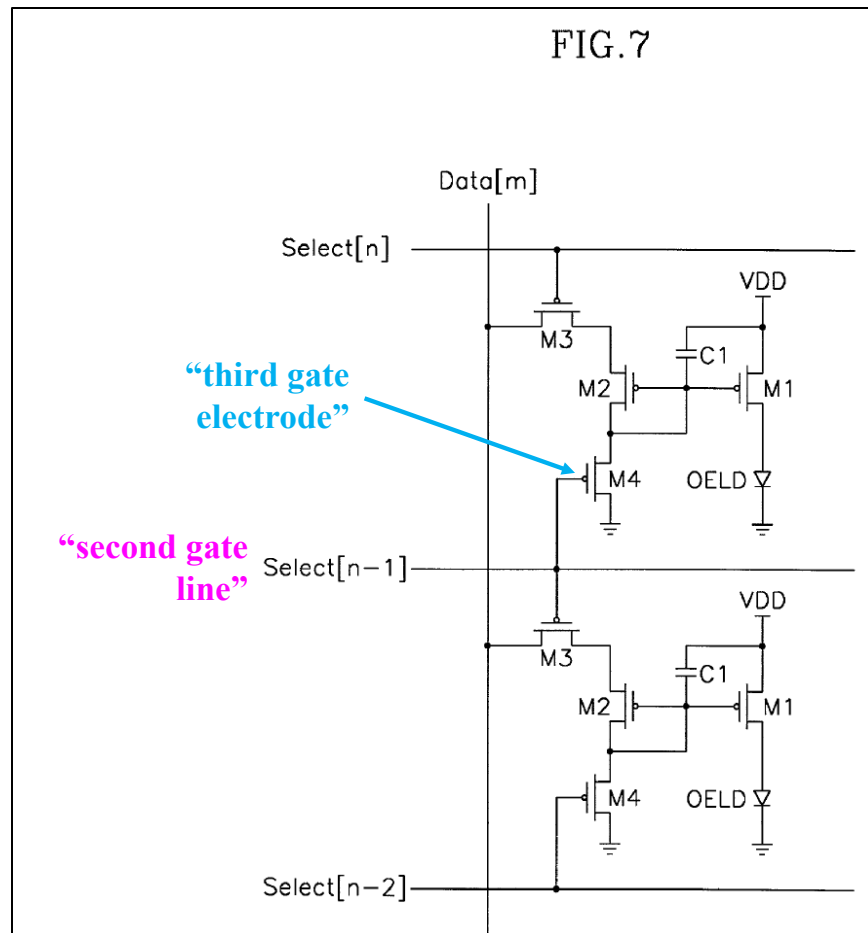
216. Kwon teaches “a third thin film transistor.” For example, Figure 7 (annotated below) of Kwon shows a pixel circuit comprising a *transistor M4*. (EX1006, [0063].)



217. Figure 21 (below) of Kwon shows a cross-sectional layout of the **transistor M4** including a **gate electrode 410** and a **channel region 220** in the region V. (EX1006, [0091], [0094].) The figure also shows the channel region 220 overlaps the gate electrode 410, and the gate electrode 410 and the channel region 220 are spaced apart from each other with the **gate insulation layer 300** therebetween.



219. Kwon teaches “the second gate line is electrically connected to the third gate electrode.” For example, Figure 7 (annotated below) of Kwon shows that the *Select[n-1] line* is electrically connected to the gate of *transistor M4*.



3. Claim 18

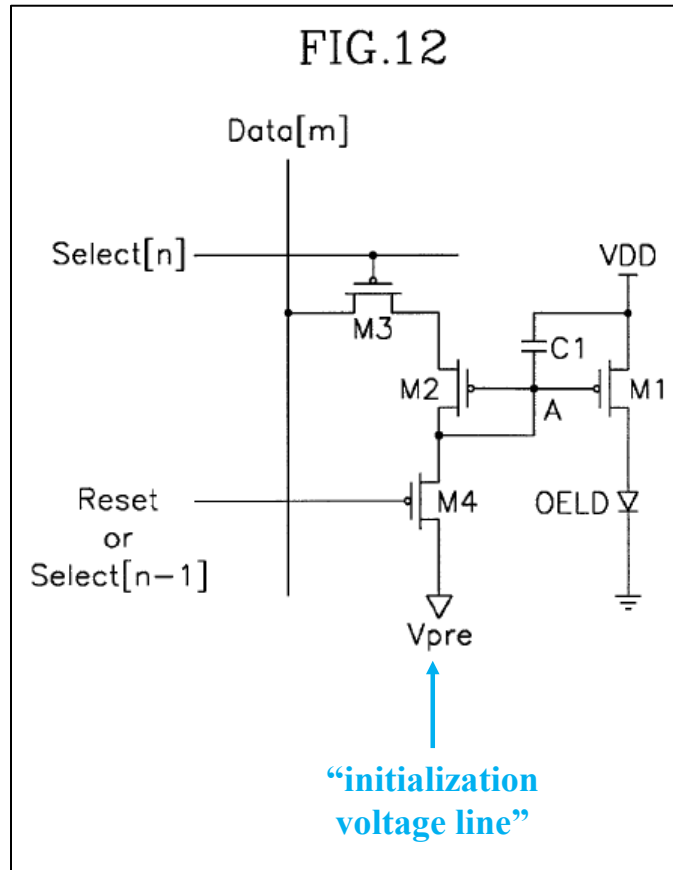
- a. **18[a]: “The TFT array substrate of claim 17, further comprising a[n] initialization voltage line,”**

220. Park teaches claim 17 as shown above in Section IX.B.8.

221. Kwon further discloses a TFT array substrate “comprising a[n] initialization voltage line.” For example, Kwon discloses a “current flowing to the ground or the pre-charge voltage [V_{pre}] from the node A via the transistor M4 is constant, and accordingly, the reset operation can be quickly performed.”

(EX1006, [0078].) Figure 12 (below) shows the *pre-charge voltage line V_{pre}*. A

POSITA would have understood that the pre-charge voltage line V_{pre} is an initialization voltage line because it pre-charges (initializes) node A.

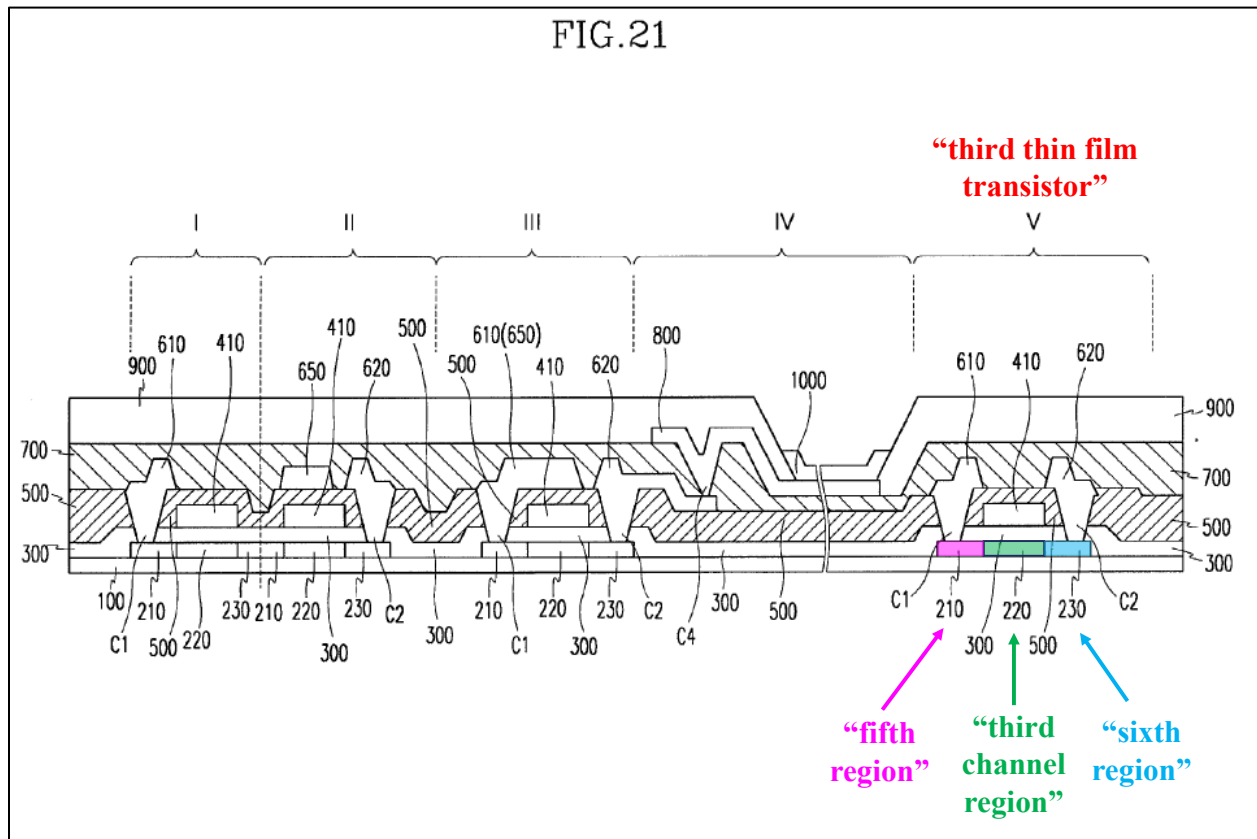


- b. 18[b]: “wherein the third thin film transistor further comprises a fifth region adjacent to a side of the third channel region and a sixth region adjacent to another side of the third channel region, and”

222. As shown for element 17[b], Kwon teaches a transistor $M4$ (“third thin film transistor”).

223. Kwon teaches “the third thin film transistor further comprises a fifth region adjacent to a side of the third channel region and a sixth region adjacent to another side of the third channel region.” For example, Figure 21 (below) shows

the **transistor M4** comprising a **source region 210** adjacent to a side of the **channel region 220** and a **drain region 230** adjacent to another side of the channel region 220. (EX1006, [0094], [0098].)

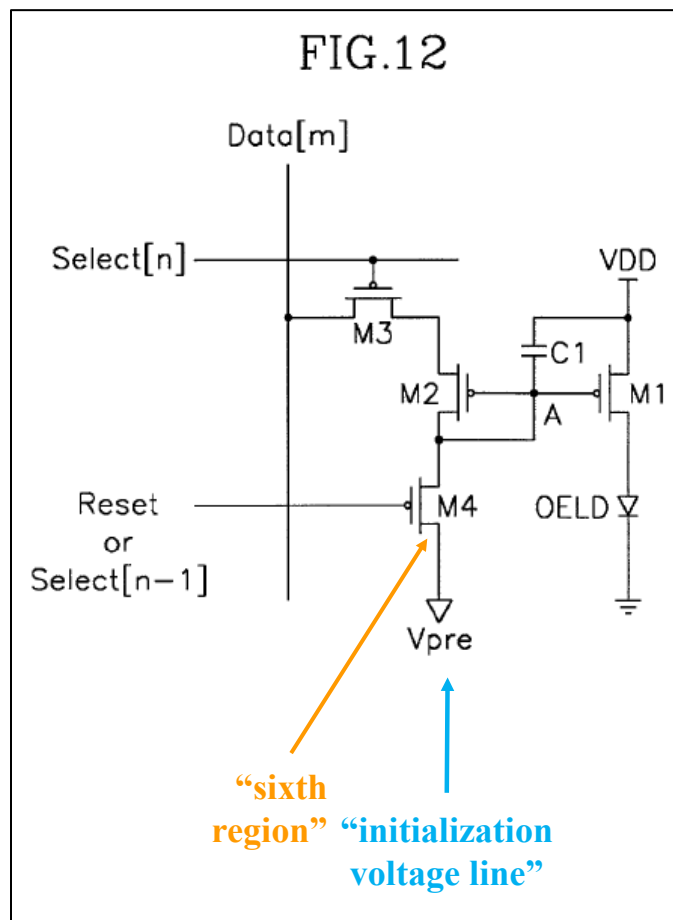


224. It would have been obvious to a POSITA to combine the teachings of Park and Kwon. (See Section IX.E.2.a.)

- c. **18[c]: “the sixth region is electrically connected to the initialization voltage line.”**

225. As shown for element 18[b], Kwon teaches a drain region 230 (“sixth region”) of a transistor M4. As shown for element 18[a], Kwon teaches a pre-charge voltage line V_{pre} (“initialization voltage line”).

226. Kwon discloses that “the sixth region is electrically connected to the initialization voltage line.” For example, Figure 12 (below) of Kwon shows the *drain* of transistor M4 is electrically connected to the *pre-charge voltage line*. (EX1006, [0076].) Kwon discloses “a pre-charge voltage V_{pre} instead of the ground voltage is supplied to the drain of the switching transistor M4.” (EX1006, [0071].)



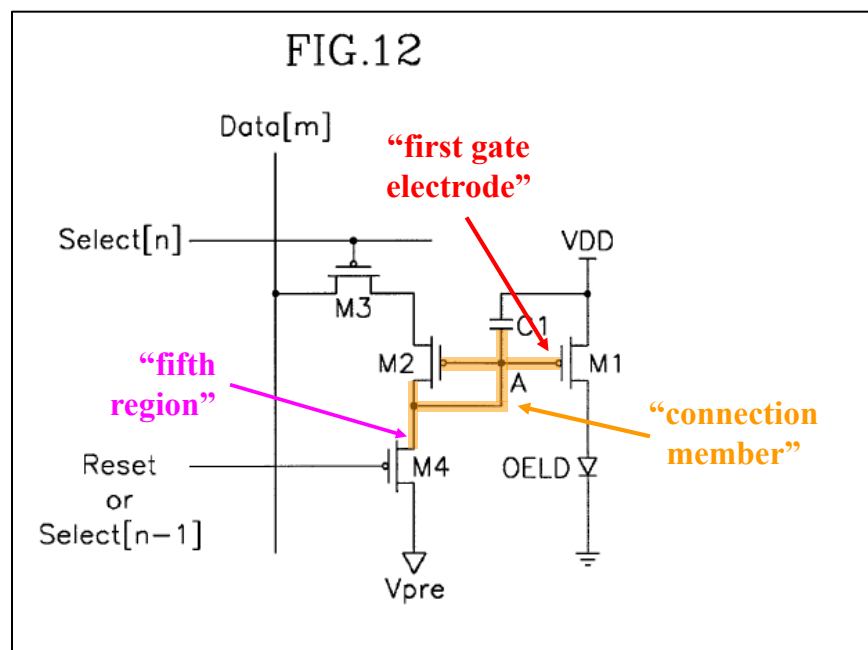
227. It would have been obvious to a POSITA to combine the teachings of Park and Kwon. (See Section IX.E.2.a.)

4. Claim 19: “The TFT array substrate of claim 18, wherein the fifth region is electrically connected to the first gate electrode via the connection member.”

228. Park with Kwon teach claim 18 as shown above in Section IX.E.2.

229. As shown for element 18[b], Kwon teaches a transistor M9 (“third thin film transistor”) and a gate electrode of a driving transistor M1 (“first gate electrode”).

230. Kwon discloses that “the fifth region is electrically connected to the first gate electrode via the connection member.” For example, Figure 12 (below) of Kwon shows the *source* of the transistor M9 is electrically connected to the *gate electrode of the driving transistor M1* via the *connection member*.



231. It would have been obvious to a POSITA to combine the teachings of Park and Kwon. (*See* Section IX.E.2.a.)

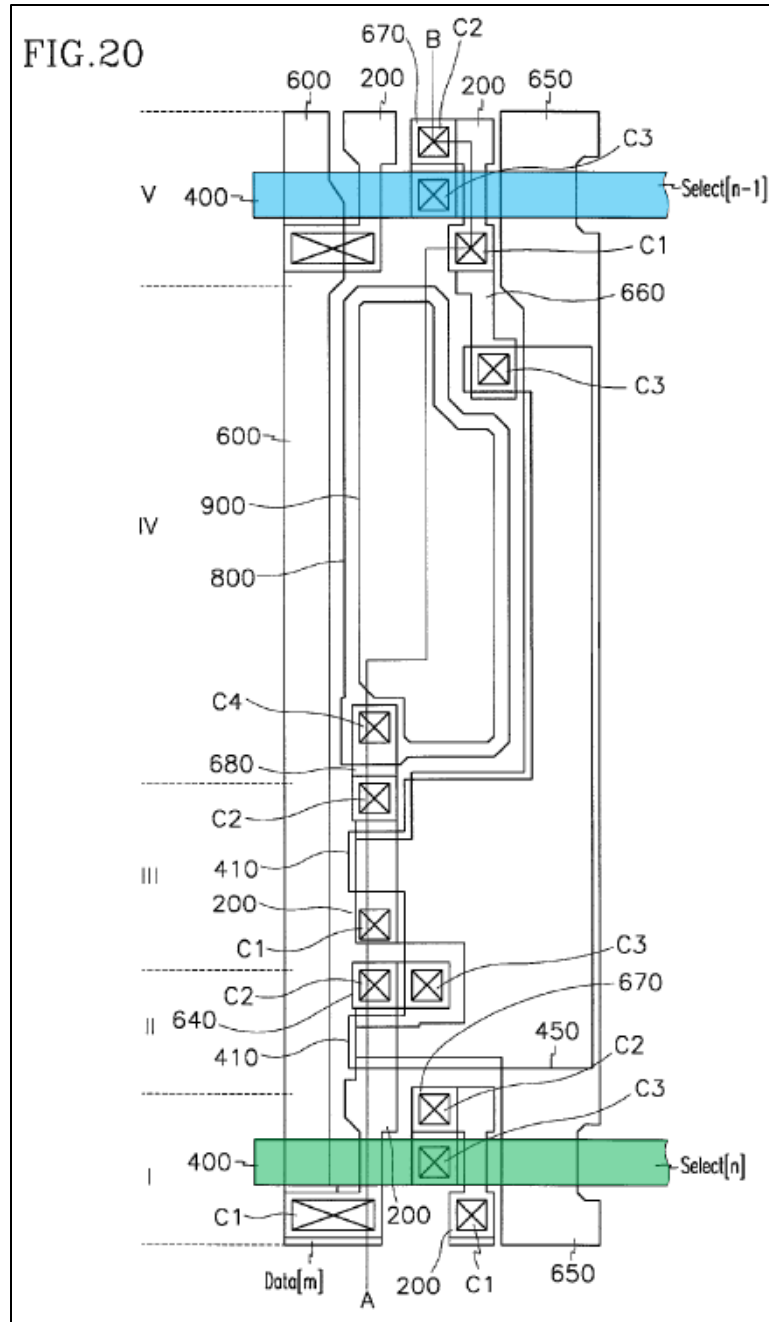
5. Claim 20: “The TFT array substrate of claim 18, wherein the initialization voltage line extends in the same direction as the first gate line.”

232. As shown for element 18[a], Kwon teaches a pre-charge voltage line V_{pre} (“initialization voltage line”).

233. Kwon teaches “wherein the initialization voltage line extends in the same direction as the first gate line.” For example, Kwon discloses “the previous select signal is used instead of the ground voltage or the pre-charge voltage.” (EX1006, [0074].) A POSITA would have understood this passage to mean the previous select signal would be used as the pre-charge voltage line V_{pre} .

234. Kwon also discloses “a select signal $Select[n]$ is supplied to the gate of the transistor M3 to activate the corresponding pixel. A data signal $Data[m]$ is supplied to the source of the activated transistor M3 to drive the current driving transistor M1.” (EX1006, [0060].) The select signal $Select[n]$ is a “first gate line” because it is a gate line to the gate electrode of the switching transistor M3.

235. Figure 20 (annotated below) shows the *previous select signal $Select[n-1]$* extends in the same direction as the *select signal $Select[n]$* .



H. Claims 1-4, 12-19, 22-24, 28, And 29 Are Obvious Over Liu100 And Ono

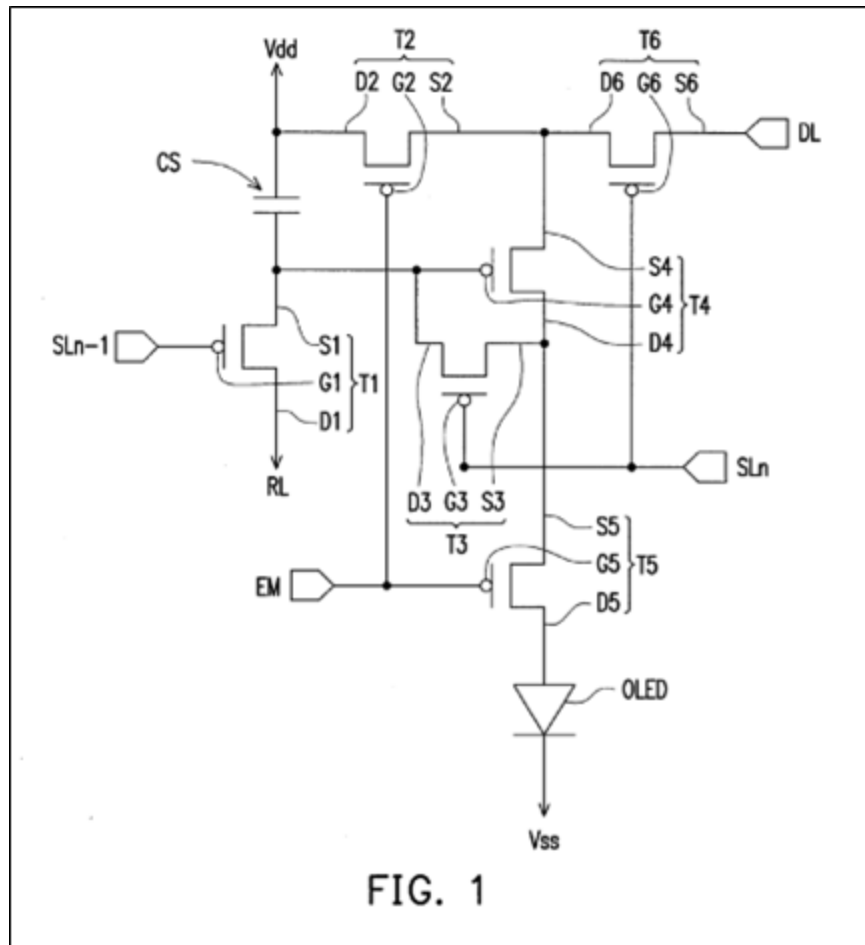
1. Summary of Liu100

236. Liu100 “relates to a semiconductor device,” including its pixel structure. (EX1007, [0003].) Liu100 teaches that “the pixel structure is applied to

an organic electro luminescence display device and has a structure comprising six thin film transistors and one capacitor.” (EX1007, [0032].)

237. Liu100 acknowledges that the “pixel structure of the organic light emitting device in the display is usually driven by the cooperation of a plurality of thin film transistors (TFTs) and a capacitor.” (EX1007, [0006].) The plurality of TFTs occupies much of the area in a pixel structure, leaving “no extra space for disposing other components.” (*Id.*) Additionally, “the pixel circuit structure can not be miniaturized easily and thus can not be applied in displays with high resolution.” (*Id.*)

238. Liu100 discloses a pixel structure therefore that is “capable of reducing an area occupied by components of the pixel structure.” (EX1007, [0007].) Figure 1 (below) is “a schematic circuit diagram of a pixel structure according to an embodiment of the invention.” (EX1007, [0013].) “[T]he pixel structure is applied to an organic electroluminescence display and has a structure comprising six thin film transistors and one capacitor.” (EX1007, [0032].)



239. Figure 8 (below) is a top view of Figure 1, and Figure 10 (below) is a cross section of a portion of Figure 1. Liu100 notes that “the cross-sectional diagram of FIG.10 is a cross-sectional view for the fifth thin film transistor in the 6T1C pixel structure. Since the six thin film transistors in the 6T1C pixel structure are substantially similar, the people skilled in the art may understand the cross-sectional structures of other five thin film transistors in accordance with the description for the fifth thin film transistor shown in FIG. 10.” (EX1007, [0058].)

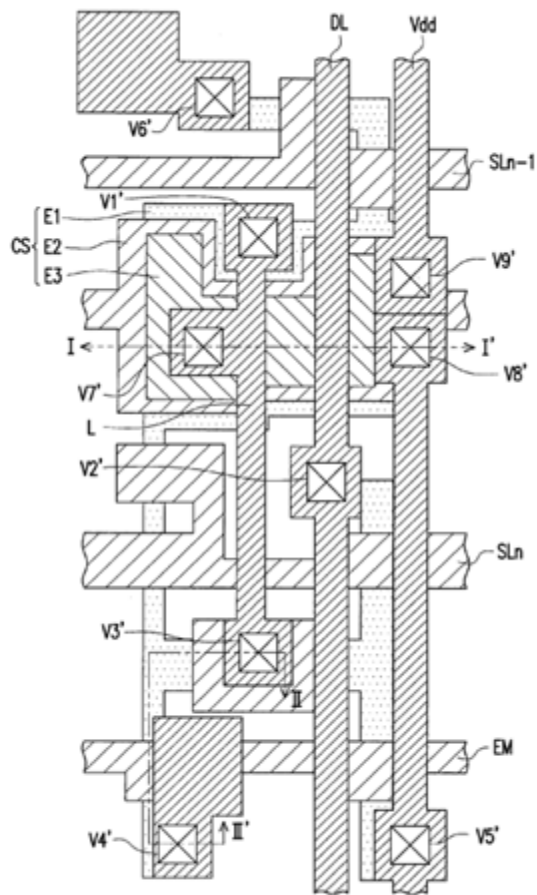


FIG. 8

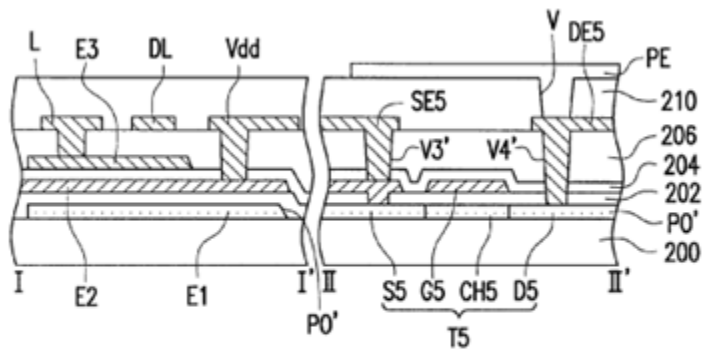


FIG. 10

2. Summary of Ono

240. Ono “relates to luminescent display devices, and particularly to an active-matrix luminescent display device which includes a luminescent element and a driving circuit having a capacitor and a thin-film transistor.” (EX1008, [0003].) Ono teaches that “the luminescent element may be an organic electroluminescent element.” (EX1008, [0046].)

241. Ono states that conventional active-matrix luminescent display devices arrange pixel circuits to include, “for each luminescent element, a driving circuit for driving the luminescent element.” (EX1008, [0005].) Ono explains: “[t]he driving circuit generally includes: a switching transistor which selects a pixel for producing luminescence; a driving transistor which drives a luminescent element; and a capacitor. The driving circuit includes, for example, a capacitor which holds a voltage for determining an amount of current passed by the driving transistor.” (EX1008, [0006].)

242. Ono recognizes, however, that this arrangement results in less design flexibility because it dedicates a region to the capacitor. (EX1008, [0008].) Therefore, “when the number of capacitors or the capacitor area increases, the region for forming other elements becomes smaller.” (*Id.*) Accordingly, Ono discloses “a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to

the capacitor.” (EX1008, [0010].) For example, Ono teaches forming a capacitor above the driving transistor, such as the gate electrode of the driving transistor. (EX1008, [0050], [0070], Fig. 3, Fig. 4, [0091], Fig. 6, Fig. 7, [0113], Fig. 8, Fig. 9, [0124], Figs. 10-12.)

3. Claim 1

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

243. Liu100 discloses “a thin film transistor (TFT) array substrate.” For example, Liu100 teaches the pixel structure of a semiconductor device includes “at least one thin film transistor.” (EX1007, [0008]-[0009].)

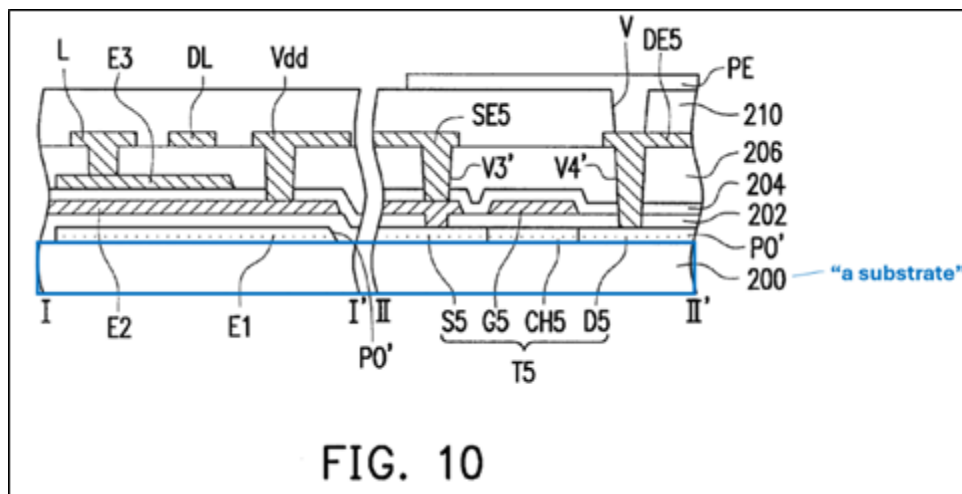
244. Referring to Figure 1, Liu100 teaches that “the pixel structure is applied to an organic electroluminescence display and has a structure comprising six thin film transistors” (EX1007, [0032].)

245. Liu100 provides additional disclosures that show that it teaches “a thin film transistor (TFT) array substrate:”

- “A pixel structure, comprising: . . . at least one thin film transistor.” (EX1007, cls. 1, 5.)
- “The pixel structure as claimed in claim 1, wherein the at least one thin film transistor comprises six thin film transistors.” (EX1007, cl. 4, cl. 8 (“The pixel structure as claimed in claim 5, wherein the at least one thin film transistor comprises six thin film transistors.”).)

b. 1[a]: “a substrate;”

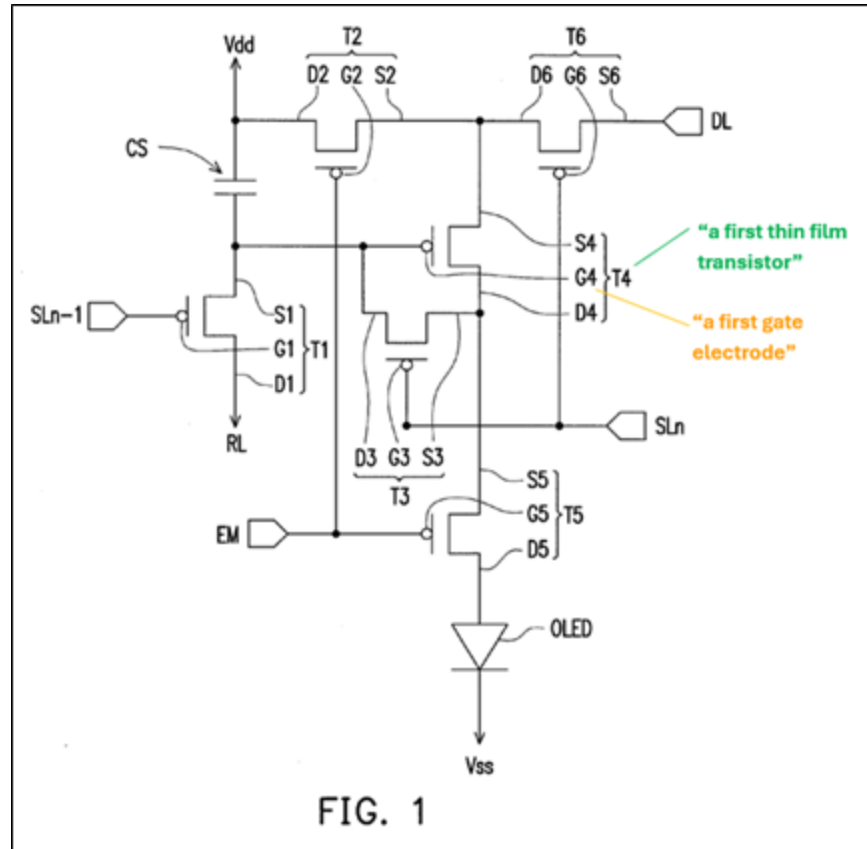
246. Liu100 discloses a pixel structure comprising “a substrate.” For example, Liu100 discloses “the pixel structure is disposed on a substrate 100.” (EX1007, [0032].) As another example, referring to Figure 10 (annotated below), Liu100 discloses “the pixel structure is disposed on a substrate 200.” (EX[Liu100]), [0058].)



c. 1[b]: “a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”

247. Liu100 discloses “a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween.” For example, referring to Figure 1 (annotated below), Liu100 teaches the pixel structure includes “*a channel region* (not shown)

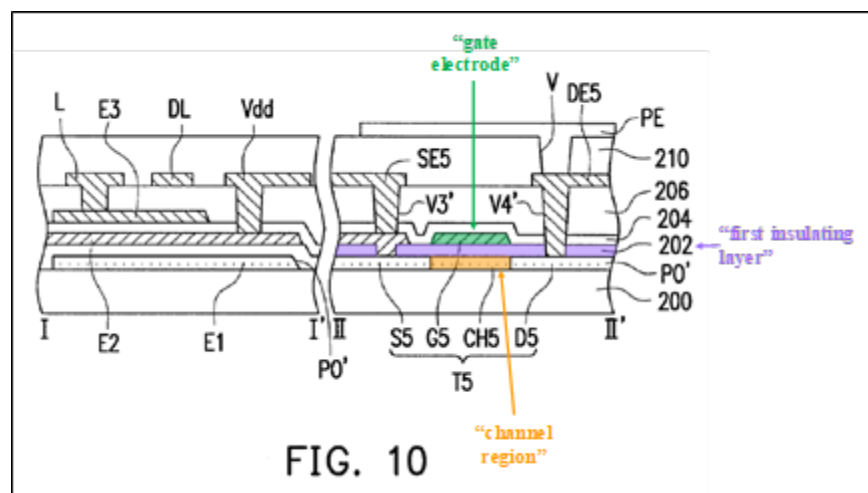
in a region predetermined for forming a fourth thin film transistor T4.” (EX1007, [0035] (emphasis added).)



248. Liu100 further discloses “[t]he third conductive layer M3 has a source electrode and a drain electrode (not shown) in the region predetermined for forming the fourth thin film transistor T4, the source electrode and the drain electrode are electrically connected to the source region S4 and the drain region D4 respectively, and the source region S4, the drain region D4, the source electrode, the drain electrode and the gate G4 form the third thin film transistor T4.” (EX1007, [0069].)

249. Figure 10 is a “schematic cross-sectional diagram” of the pixel structure shown in Figure 1. (EX1007, [0057].) Referring to Figure 10 (annotated below), Liu100 discloses “the pixel structure is disposed on a substrate 200 and comprises a semiconductor layer PO’.” (EX1007, [0058].) Liu100 discloses that “the semiconductor layer PO’ has a source region S5, a drain region D5 and a channel region CH5 in a region predetermined for forming a fifth thin film transistor T5.” (EX1007, [0060].) “The first insulating layer 202 covers the semiconductor layer PO’.” (EX1007, [0058].)

250. Liu100 discloses “[t]he first conductive layer M1’ is disposed on the first insulating layer 202,” where “the first conductive layer M1’ has a gate G5 in the region predetermined for forming the fifth thin film transistor T5.” (EX1007, [0063].)



251. As shown in Figure 10 (annotated above), the *gate electrode* overlaps the *channel region*. The figure also shows the gate electrode of a thin film

transistor and the channel region being spaced apart from each other with *insulating layer 202* therebetween. Liu100 discloses “[t]he gate G is disposed on the insulating layer 202 above the channel region CH of the semiconductor layer PO’.” (EX1007, [0077].)

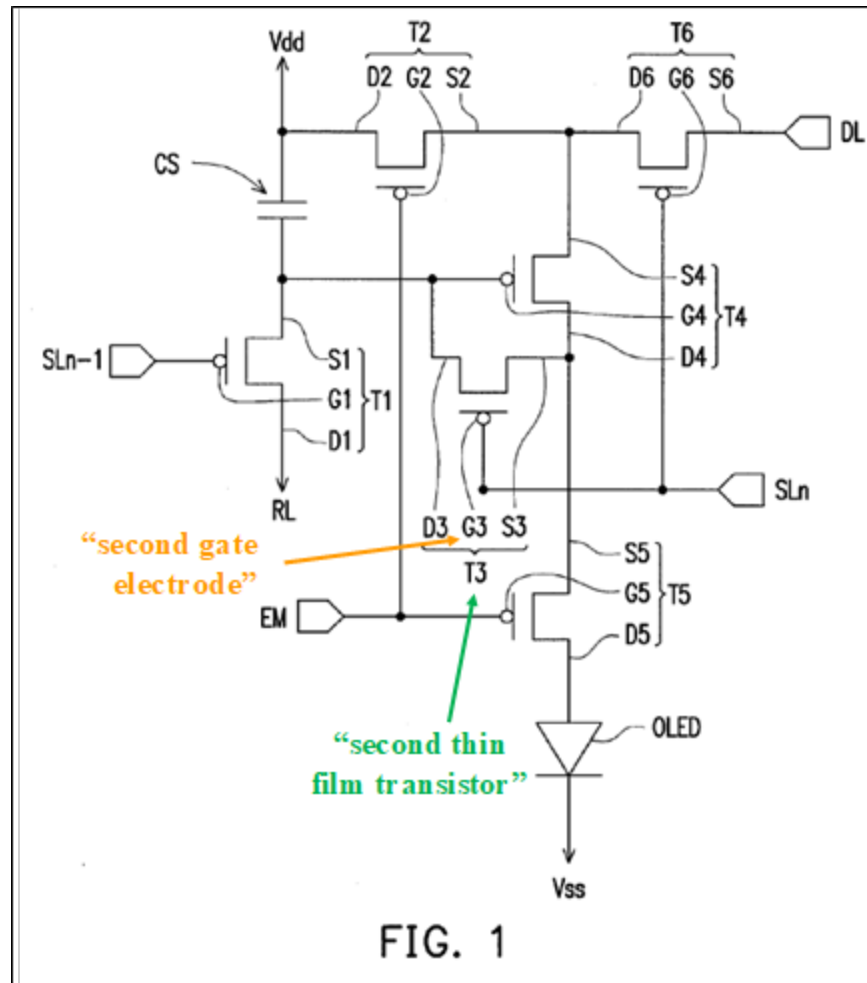
252. As Liu100 explains, “the cross-sectional diagram of FIG. 10 is a cross-sectional view for the fifth thin film transistor in the 6T1C pixel structure. Since the six thin film transistor in the 6T1C pixel structure are substantially similar, the people skilled in the art may understand the cross-sectional structures of other five thin film transistors in accordance with the description for the fifth thin film transistor shown in FIG. 10.” (EX1007, [0058].) Although Figure 10 shows the cross-sectional view and structure specifically for the fifth thin film transistor T5, a POSITA would have understood that this figure represents the structure of the other thin film transistors, such as the fourth thin film transistor T4.

253. Thus, Liu100 teaches element 1[b]: a fourth thin film transistor T4 including a channel region CH4 and a gate electrode G4 overlapping the channel region CH4, the gate electrode G4 and the channel region CH4 being spaced apart from each other with insulating layer 202 therebetween.

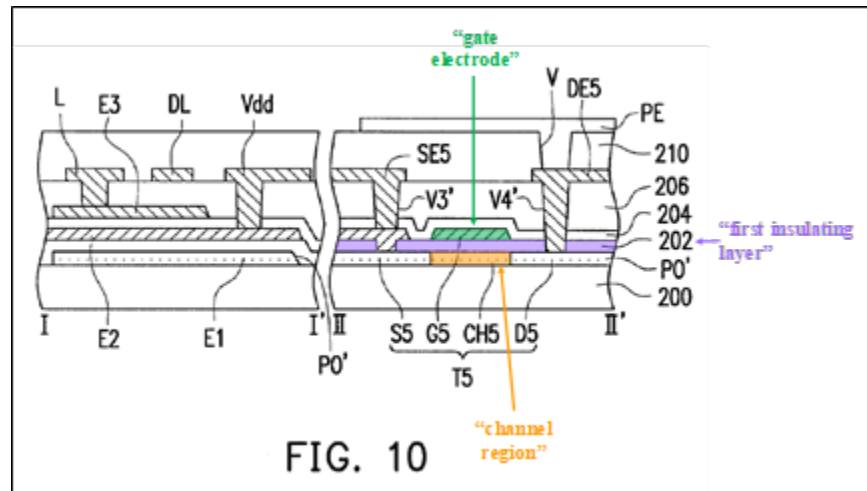
- d. **1[c]: “a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”**

254. Liu100 discloses “a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween.” For example, referring to Figure 1 (annotated below), Liu100 discloses a pixel structure “comprising six thin film transistors,” where the third thin film transistor T3 includes a semiconductor layer PO that “has a source region S3, a drain region D3 and a channel region (not shown).” (EX1007, [0032], [0035].)

255. Liu100 discloses “[t]he third conductive layer M3’ has a source electrode and a drain electrode (not shown) in the region predetermined for forming the third thin film transistor T3, the source electrode and the drain electrode are electrically connected to the source region S3 and the drain region D3 respectively, and the source region S3, the drain region D3, the source electrode, the drain electrode and the *gate G3* form the third *thin film transistor T3*.” (EX1007, [0069].)



256. As discussed for element 1[b], Liu100's Figure 10 (annotated below) shows a *gate electrode* overlaps the *channel region*. The figure also shows the gate electrode of a thin film transistor and the channel region being spaced apart from each other with *insulating layer 202* therebetween. Liu100 explains that Figure 10 represents the cross-sectional view and layers for other thin film transistors, such as the third thin film transistor T3, as shown for element 1[b]. (EX1007, [0058].)



257. Thus, Liu100 teaches element 1[c]: a third thin film transistor T3 including a channel region CH3 and a gate electrode G3 overlapping the channel region CH3, the gate electrode G3 and the channel region CH3 being spaced apart from each other with insulating layer 202 therebetween.

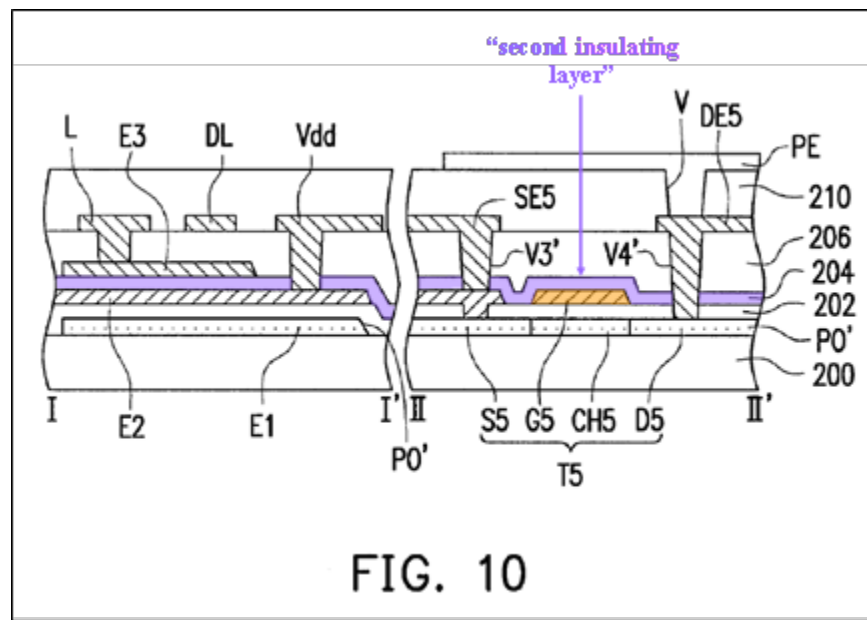
e. 1[d]: “a second insulating layer disposed on the first and second gate electrode;”

258. As shown for element 1[b], Liu100 teaches a gate electrode G4 (“first gate electrode”). As shown for element 1[c], Liu100 teaches a gate electrode G3 (“second gate electrode”).

259. Liu100 discloses “a second insulating layer disposed on the first and second gate electrode.” For example, Liu100 discloses “the first conductive layer M1’ has a gate G3 in the region predetermined for forming the third thin film transistor T3; the first conductive layer M1’ has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007, [0064].) Liu100 explains that “[t]he second insulating layer 204 covers the first conductive

layer M1' and has a material similar to or the same with the material of the second insulating layer 104 as described in the first embodiment.” (EX1007, [0065].)

260. Figure 10 (annotated below) shows the *insulating layer 204* disposed on the *gate electrode G5*. As explained for elements 1[b] and 1[c], the cross-sectional view in Figure 10 is representative of all the thin film transistors in the pixel structure. (EX1007, [0058].) Thus, Liu100 teaches element 1[d].

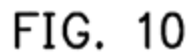


- f. 1[e]: “a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”

(i) **Liu100**

261. As shown for element 1[b], Liu100 teaches a gate electrode G4 (“first gate electrode”). As shown for element 1[d], Liu100 teaches an insulating layer 204 (“second insulating layer”).

262. Liu100 discloses “a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween.” For example, referring to Figure 10 (annotated below), Liu100 discloses the pixel structure includes “a *third electrode E3* of the second conductive layer M2” and the *layer M1*’ having the gates. (EX1007, [0063], [0066]). Liu100 teaches that, “[i]n consideration of electrical conductivity, the second conductive layer M2 is often made of metal materials. . . . The metal material includes, for example, an alloy, metal nitride, metal oxide, metal oxynitride, another appropriate material, or a layer in which the material and any other conductive material are stacked to each other.” (EX1007, [0040].) The second conductive layer M2’ “has a material similar to or the same with the material” of the second conductive layer M2. (EX1007, [0066].)



264. Liu100 explains that “the layout of the first conductive layer M1’ is shown in FIG. 9B, which mainly comprises gates of the six thin film transistors and a second electrode E2 of the capacitor CS.” (EX1007, [0063].) This means that the electrode E2 is formed on the same layer as the gates including gate G4.

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electrode E1 and the second electrode E2 and the second insulating layer 204 between the second electrode E2 and the third electrode E3 serve as capacitor dielectric layers of the capacitor CS.” (EX1007, [0078].) Figure 10 (annotated above) shows the *electrode E3* and the *electrode E2* being spaced apart from each other with *insulating layer 204* therebetween.

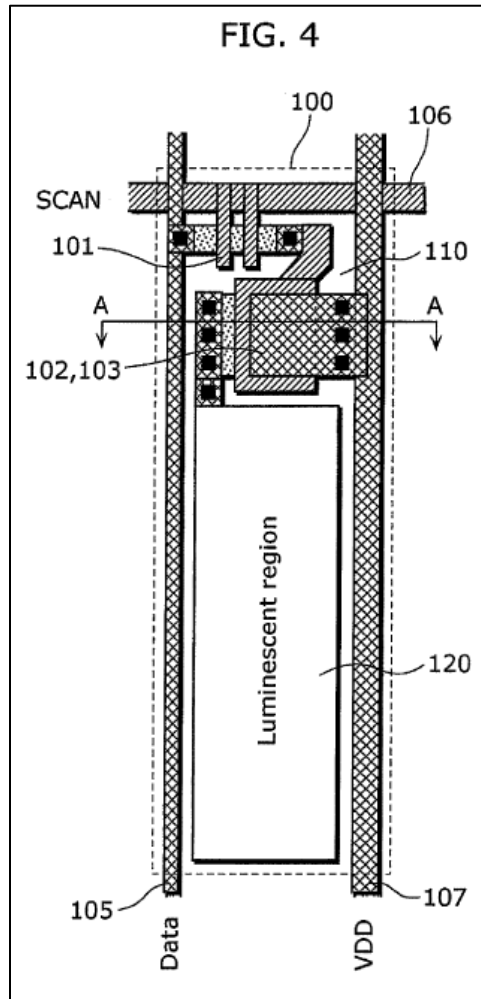
(ii) Ono

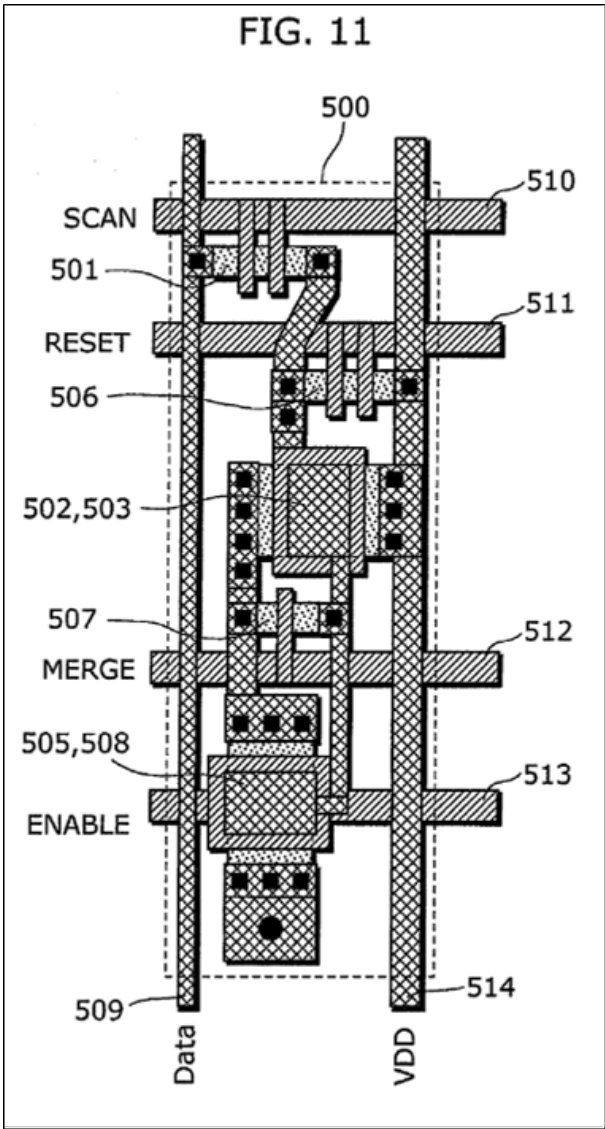
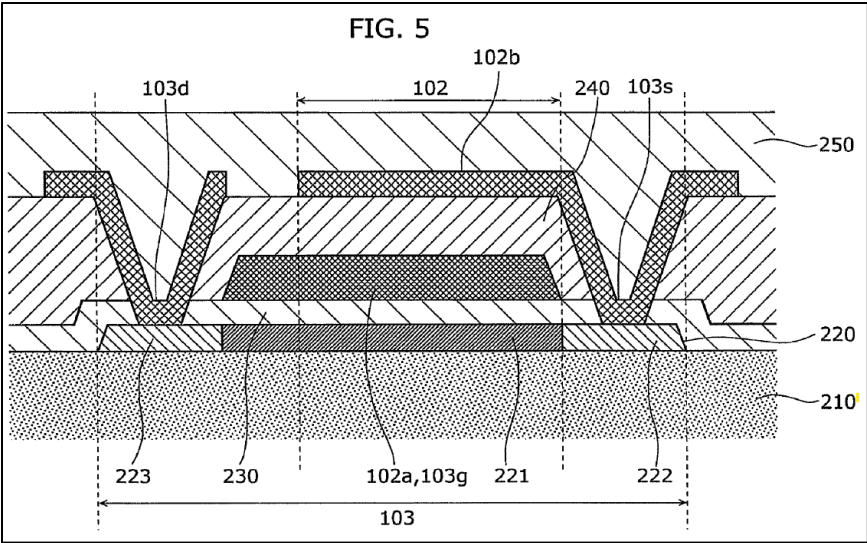
266. To the extent that Liu100 does not teach “a first metal pattern overlapping the first gate electrode,” Ono teaches it. For example, Ono teaches forming a capacitor in the region above the driving transistor, such as “the gate electrode of the thin-film transistor is used not only simply as the gate electrode but also as one of two electrodes constituting the capacitor.” (EX1008, [0029].)

267. For example, Figures 4 and 5 (below) show Ono’s capacitor 102 including a capacitor electrode 102b, an interlayer insulating film 240, and a capacitor electrode 102a. The capacitor electrode 102a functions also as the gate electrode 103g. As another example, Figure 11 (below) show Ono’s capacitor electrode 502 (“first metal pattern”) over the gate of driving thin film transistor 503 (“first gate electrode”). Ono discloses “the driving transistor 503 and the capacitor 502 are formed in the same region in the plane *to overlap each other*.” (EX1008, [0140] (emphasis added).) As another example, referring to Figure 7, Ono teaches

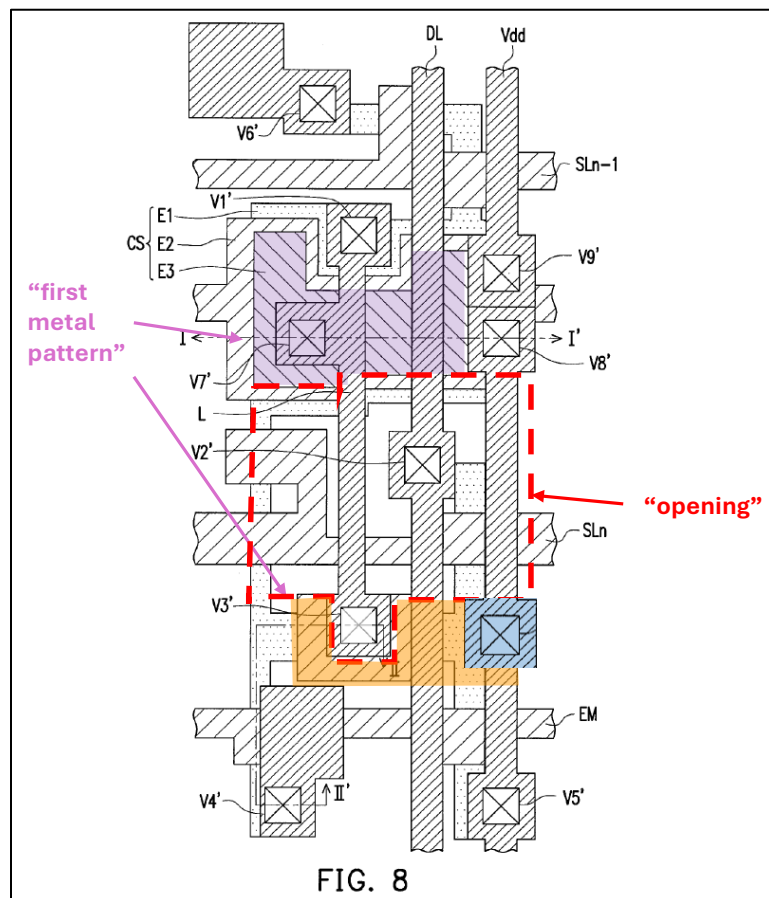
“the capacitor 311 [is] formed *on* the driving transistor 103.” (EX1008, [0107]

(emphasis added).)





268. The combination of Liu100 and Ono would result in adding an extension to Liu100's upper electrode E2 located on top of the driving transistor T4, as taught by Ono. Modified Figure 8 (annotated below) shows the extended upper *electrode E2* according to the Liu100-Ono combination. It would have been obvious to a POSITA to include an opening in the electrode of a capacitor. Liu100 discloses "the layout of the first conductive layer M1' is shown in FIG. 9B, which mainly comprises gates of the six thin film transistors." (EX1007, [0063].) "[T]he first conductive layer M1' has a gate G4 in the region predetermined for forming the fourth thin film transistor T4 ." (EX1007, [0064].)



g. Motivation to combine Liu100 and Ono

269. It would have been obvious to a POSITA at the time of the '483 patent to combine the teachings of Liu100 and Ono. Liu100 and Ono disclose organic light emitting display devices with transistors that efficiently use the spaces in the device's pixel structure to promote the miniaturization of OLED devices. Liu100 discloses a pixel structure of an OLED device that is "capable of reducing an area occupied by components of the pixel structure." (EX1007, [0007].) Similarly, Ono discloses "a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor." (EX1008, [0030].) Thus, Liu100 and Ono are in the same field of endeavor and reasonably pertinent to the same technical problem of decreasing the area of the pixel structure and/or increasing the capacitance of the storage capacitor in the OLED devices. Both references teach efficiently using the space to make the organic light-emitting devices smaller.

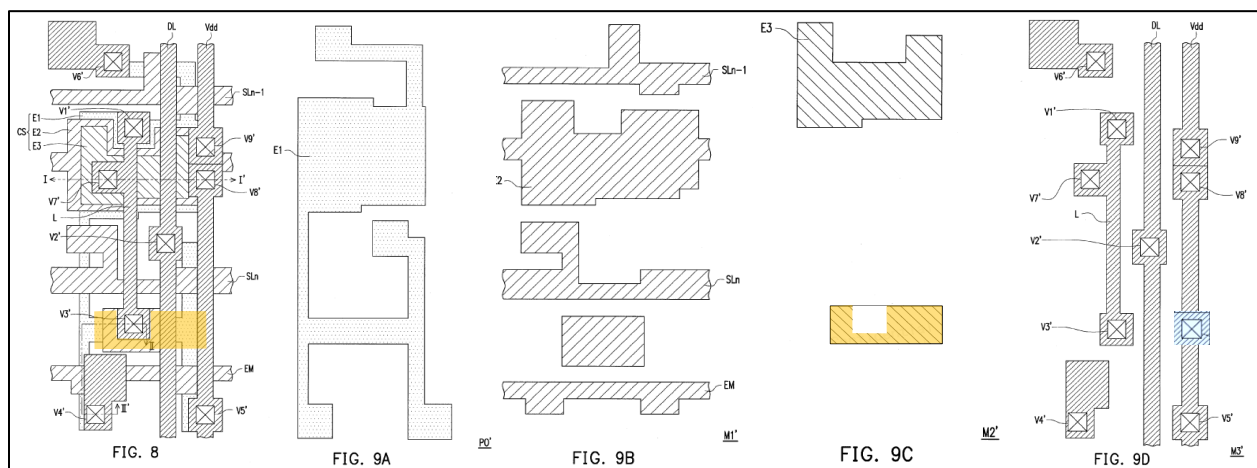
270. Ono teaches "the gate electrode of the thin-film transistor is used not only simply as the gate electrode but also as one of two electrodes constituting the capacitor." (EX1008, [0029].) "Thus, the capacitor can be formed above the thin-film transistor to overlap with the thin-film transistor, enabling efficient use of the pixel space." (*Id.*) Ono solves the problem "when the number of capacitors or the

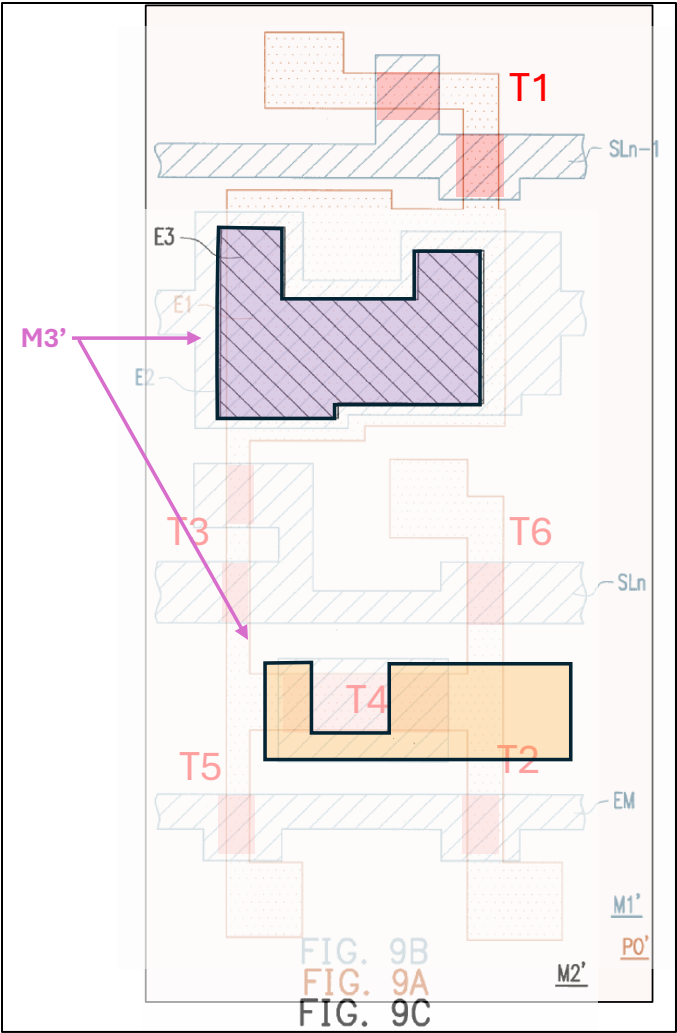
capacitor area increases, the region for forming other elements becomes smaller, resulting in less design flexibility.” (EX1008, [0008].) Ono also teaches using one of capacitor electrodes as the gate electrode of the driving transistor 103/503. (EX1008, [0070], Fig. 3, Fig. 4, [0091], Fig. 6, Fig. 7, [0113], Fig. 8, Fig. 9, [0124], Figs. 10-12.) Ono’s technical features may be combined with Liu100’s teachings with a reasonable expectation of success to generate a smaller light-emitting device with increased storage capacitor area without decreasing the device’s quality.

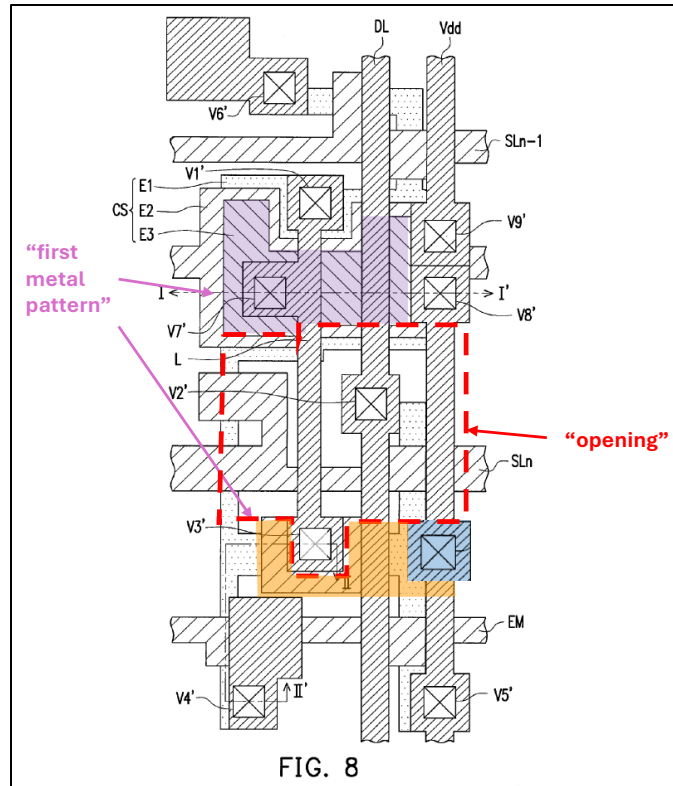
271. Liu100’s electrode E2 is on the same layer as the gates of the transistors, and Figure 9C shows that the space above the gate of the driving transistor T4 is not occupied. A POSITA would have been motivated to extend Liu100’s electrode E2 in the space above the gate of the transistor T4, as taught by Ono, to increase the total capacitance and capacitor area. It was known to a POSITA, such as taught in Kakinuma (EX1015, [0011], [0019]) that the display performance may be improved by increasing the capacitance of the pixel structure without occupying additional area. Because no extra layers are added, the space is unoccupied, and the change would not require a different mask for patterning the M2’ layer, a POSITA would have had a reasonable expectation of success combining the two references. A modification to the mask for patterning the M2’

layer would not create additional complexities or changes to the manufacturing process.

272. The Liu100-Ono combination includes an extended upper electrode E2, as shown in modified Figures 8 and 9A-9D (below). Below is a composite figure overlaying Figures 9A-9D of Liu100, showing the extended upper *electrode* according to the combination of Liu100 and Ono. Liu100 discloses “the layout of the first conductive layer M1' is shown in FIG. 9B, which mainly comprises gates of the six thin film transistors.” (EX1007, [0063].) “[T]he first conductive layer M1' has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007, [0064].) The electrode E2 extends to include a region (yellow) above the gate electrode of the thin-film transistor on the M2' layer, overlapping the power line Vdd, the two are connected through a via structure. (EX1008, [0030].)







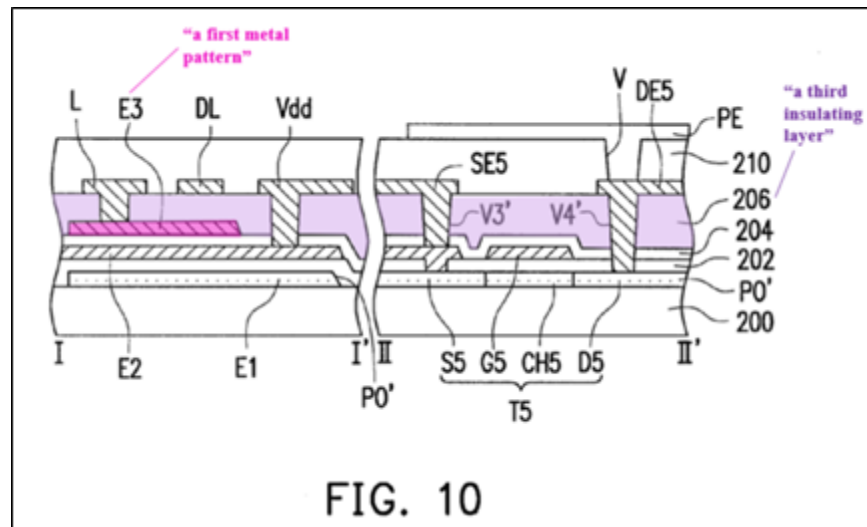
273. Liu100 and Ono both relate to efficiently using pixel space within organic light emitting display devices would motivate a POSITA to use the techniques disclosed in Ono to improve the similar device of Liu100 in the same way. Further, it would have been obvious to combine the teachings of Liu100 and Ono because Ono teaches placing a capacitor over a gate electrode of the driving transistor, which was known in the art, and Liu100's display device has space for the capacitor over the gate electrode of transistor T4. This technique increases the overall capacitance of the pixel structure resulting in improved display performance without requiring additional area. Prior art such as Ono successfully demonstrated an OLED display device configuration that shrinks the size of the

components within a pixel structure, and thereby there would have been a reasonable expectation of success for combining Liu100 and Ono. Thus, it would have been obvious to a POSITA to combine the teachings of Liu100 and Ono.

h. 1[f]: “a third insulating layer disposed on the first metal pattern; and”

274. As shown for element 1[e], Liu100 teaches an electrode E3 (“first metal pattern”).

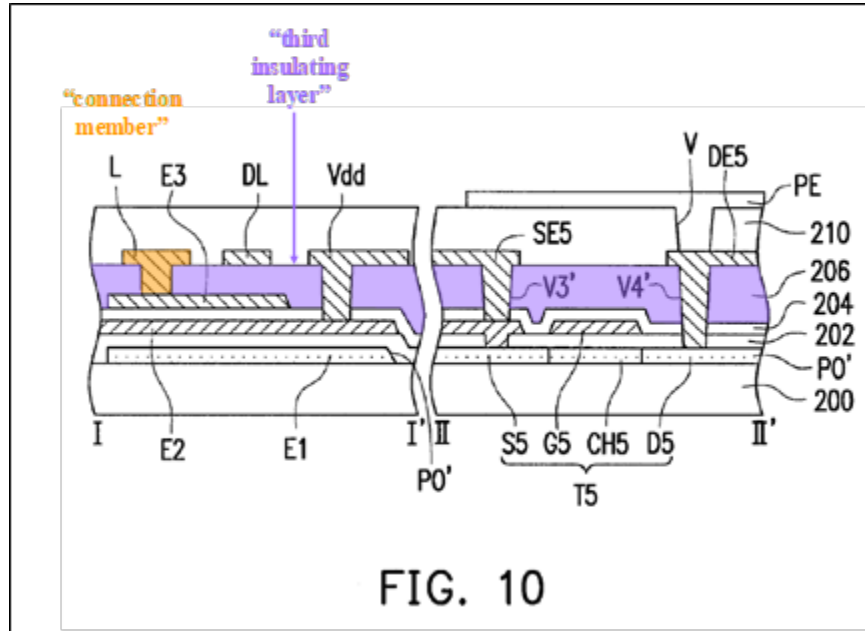
275. Liu100 discloses “a third insulating layer disposed on the first metal pattern.” For example, referring to Figure 10 (annotated below), Liu100 discloses a *third insulating layer 206*, where “[t]he third insulating layer 206 covers the second conductive layer M2’.” (EX1007, [0058], [0067].) Liu100 teaches that the third *electrode E3* is on the second conductive layer M2’. (EX1007, [0066].)



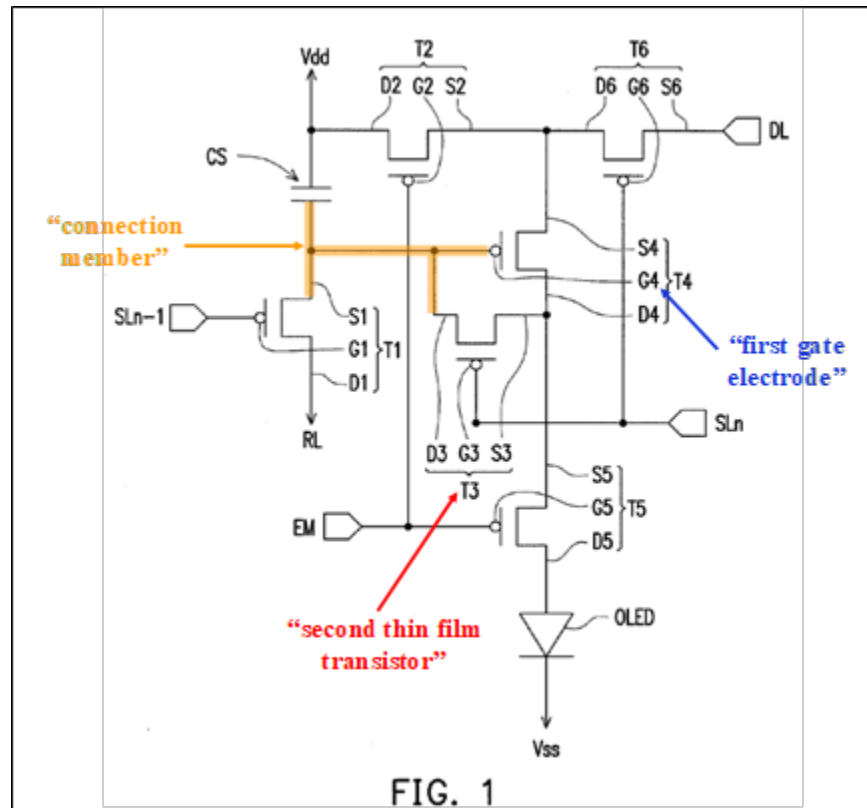
- i. **1[g]: “a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor.”**

276. As shown for element 1[f], Liu100 teaches an insulating layer 206 (“third insulating layer”). As shown for element 1[b], Liu100 teaches a gate electrode G4 (“first gate electrode”). As shown for element 1[c], Liu100 teaches a thin film transistor T3 (“second thin film transistor”).

277. Liu100 discloses “a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor.” For example, as shown below in annotated Figure 10, Liu100 discloses “[t]he third conductive layer M3’ may further comprise a signal line L, and the third electrode E3 of the capacitor CS is electrically connected to the signal line L through a contact via structure V7’.” (EX1007, [0070].) The figure below shows the *signal line L* disposed on *insulating layer 206*.



278. Figure 1 (annotated below) shows the *connection member* electrically connecting *gate electrode G4* ("first gate electrode") to the *transistor T3* ("second thin film transistor").

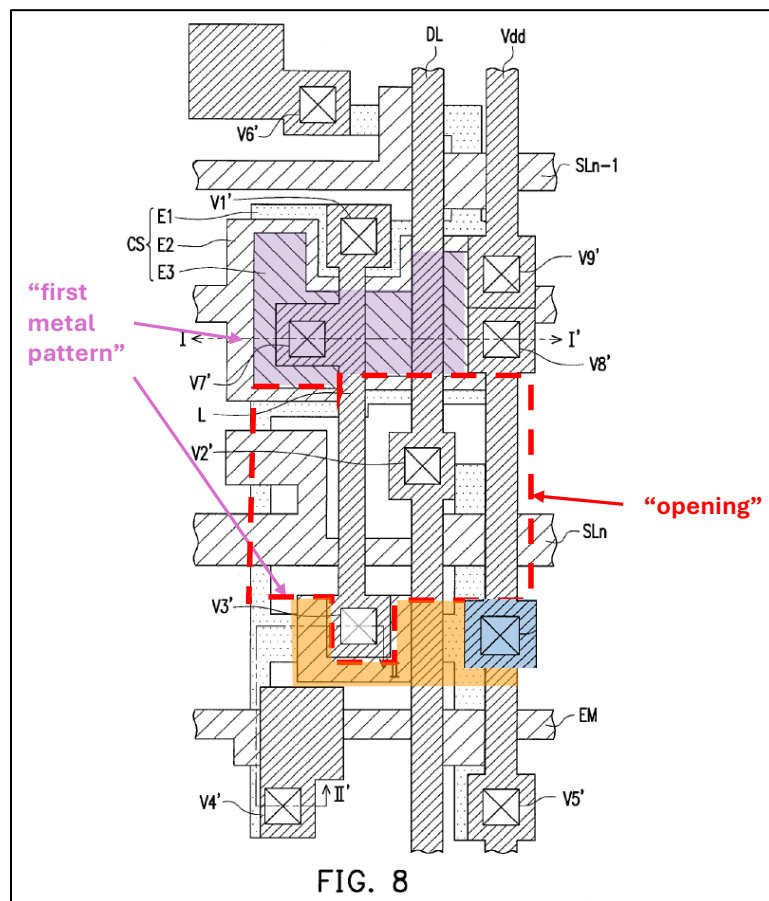


4. **Claim 2: “The TFT array substrate of claim 1, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.”**

279. Liu100 teaches claim 1 as shown above in Section IX.F.2. As shown for element 1[e], Liu100 teaches an electrode E3 (“first metal pattern”). As shown for element 1[g], Liu100 teaches a signal line L (“connection member”).

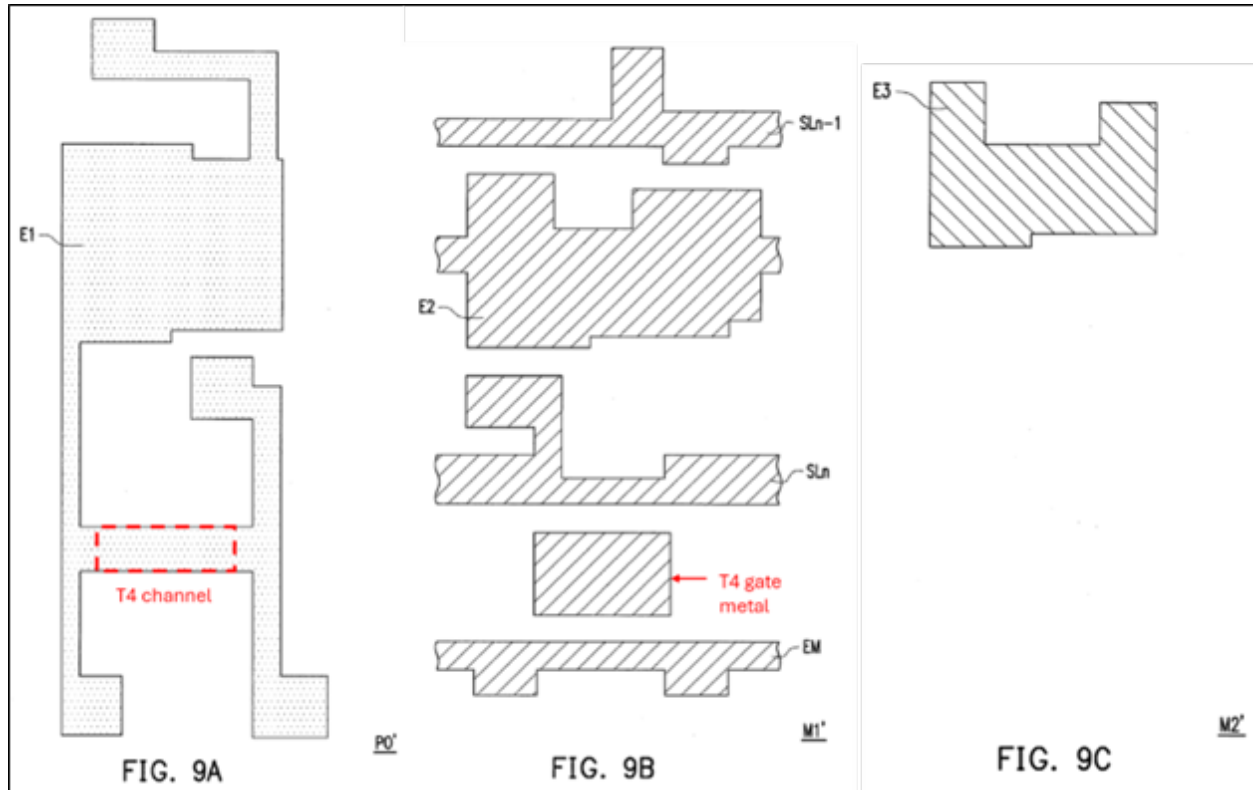
280. Liu100 teaches “the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.” For example, Liu100’s M2’ layer, shown in Figure 9C, “mainly comprises a third electrode E3 of the capacitor CS,” but also includes a large unoccupied space above the gate of the transistor T4. (EX1007, [0057], [0066].) Ono teaches

placing a capacitor electrode over a gate electrode, which was known in the art, to increase the overall capacitance of the pixel structure resulting in improved display performance without using additional space. (EX1008, [0030].) Modified Figure 8 (below) shows the extended upper electrode (yellow) of the Liu100 and Ono combination. In the Liu100-Ono combination, the M2' layer includes Liu100's electrode E3 and an extended upper electrode, which thereby leads to an opening.

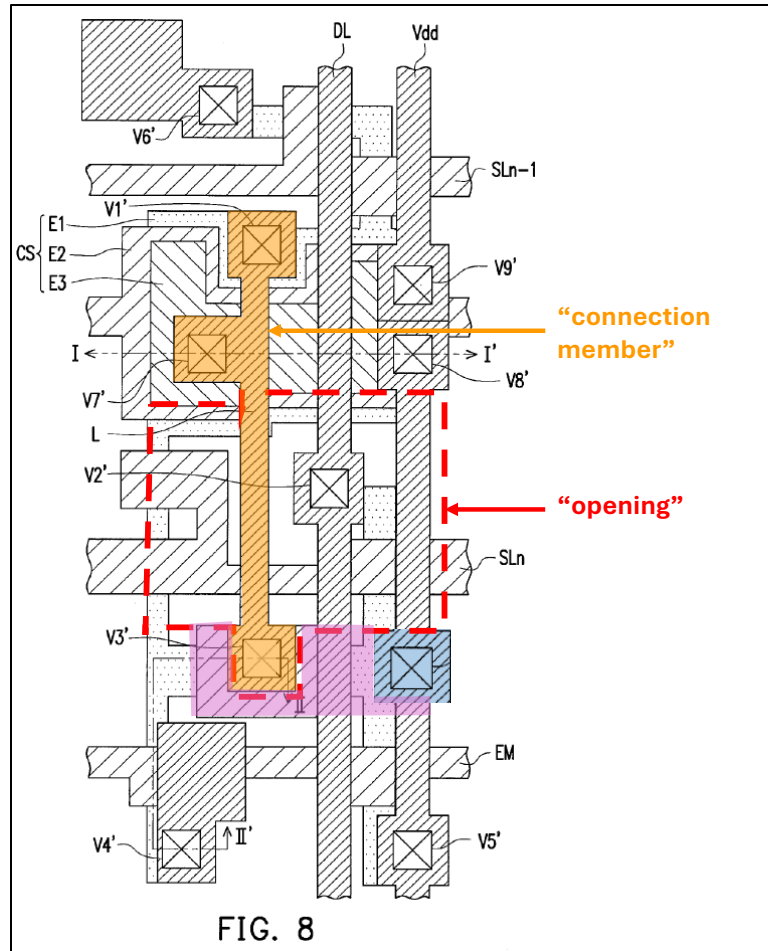


281. Liu100 explains that “the first conductive layer M1' has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007,

[0064].) The location of T4 is indicated (below) by red arrows and is located where the layer M1' metal gate crosses the PO' polySi semiconductor layer.



282. Modified Figure 8 (below) also shows that the *connection member* overlaps the *opening* of the Liu100-Ono combination in a plan view.



283. As discussed for element 1[e], it would have been obvious to combine Liu100 and Ono to extend upper electrode E2 in the space above the gate of the transistor T4 to increase the total capacitance. Liu100 discloses “the layout of the first conductive layer M1' is shown in FIG. 9B, which mainly comprises gates of the six thin film transistors.” (EX1007, [0063].) Liu100 explains that “the first conductive layer M1' has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007, [0064].)

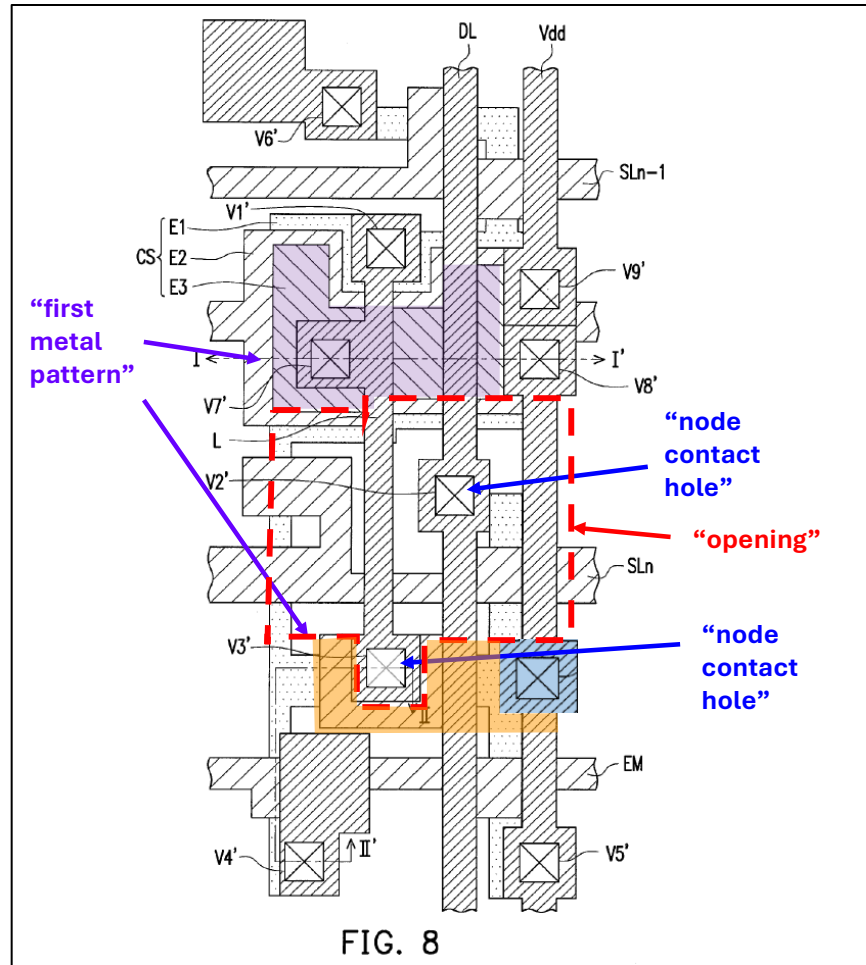
5. Claim 3

- a. **3[a]: “The TFT array substrate of claim 2, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and”**

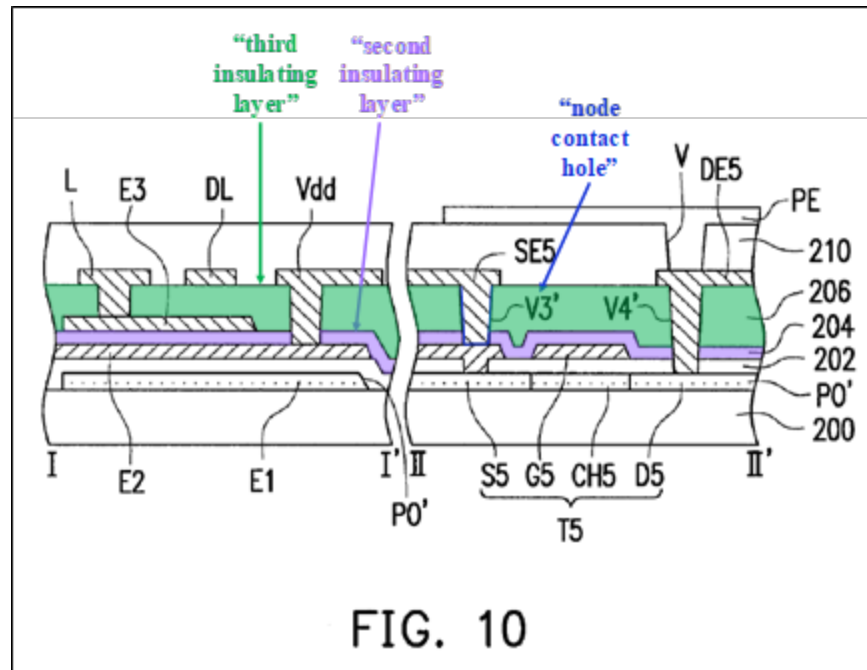
284. Liu100 teaches claim 2 as shown above in Section IX.F.3. As shown for elements 1[d] and 1[f], Liu100 teaches an insulating layer 204 (“second insulating layer”) and an insulating layer 206 (“third insulating layer”), respectively.

285. Liu100 discloses that “at least one of the second and third insulating layers includes a node contact hole overlapping the opening.” For example, Liu100 teaches that “the third insulating layer 206 covers the second conductive layer M2’” and “the third conductive layer M3’ is disposed on the third insulating layer 206.” (EX1007, [0067], [0068].) Liu100 teaches that the third conductive layer M3’ has source electrodes and drain electrodes that “are electrically connected to the source region and the drain regions through contact via structures V1’-V6’.” (EX1007, [0069].) A POSITA would have understood the contact via structures V1’-V6’ electrically connecting to the source and drain regions means they are node contact holes.

286. Modified Figure 8 (below) shows via structures including, for example, via structure V3’ (“a node contact hole”). As the figure shows, the *via structure V3’* overlaps the *opening*.



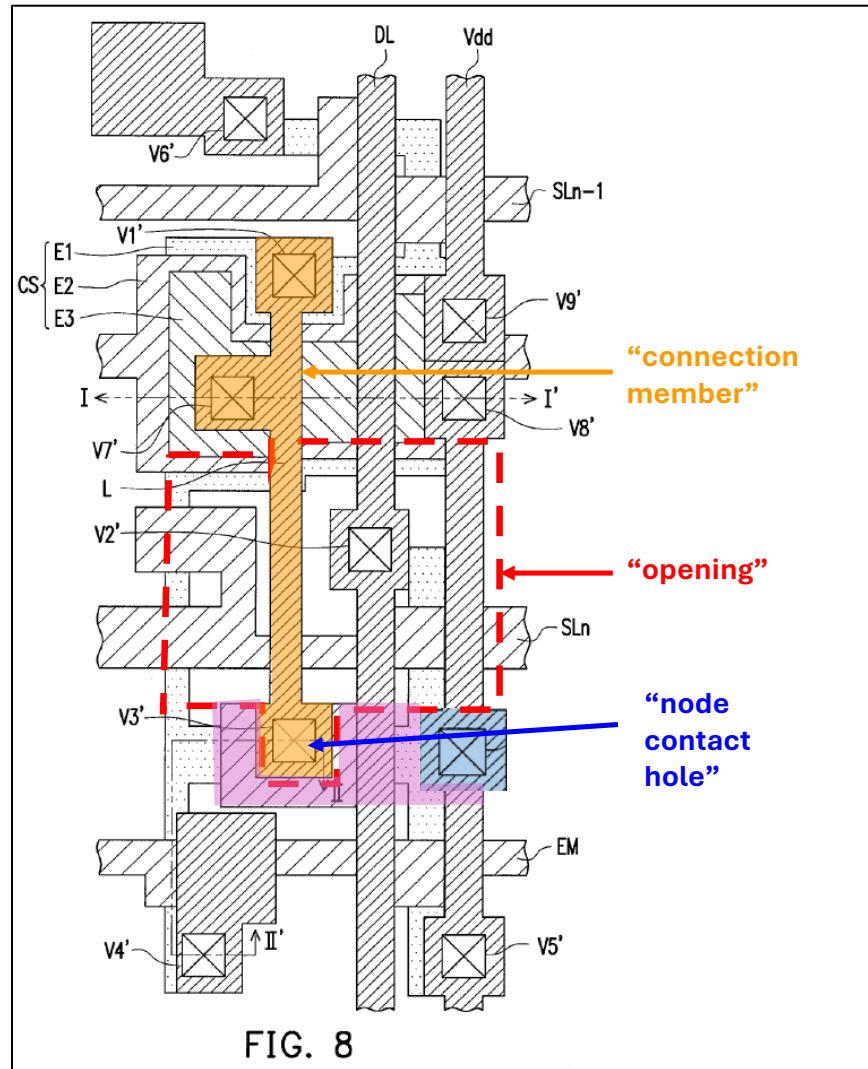
287. Figure 10 (annotated below) shows the *insulating layer 204* and *insulating layer 206* including a *via structure V3'* which is shown in modified Figure 8 as providing connection to the gate of transistor T4.



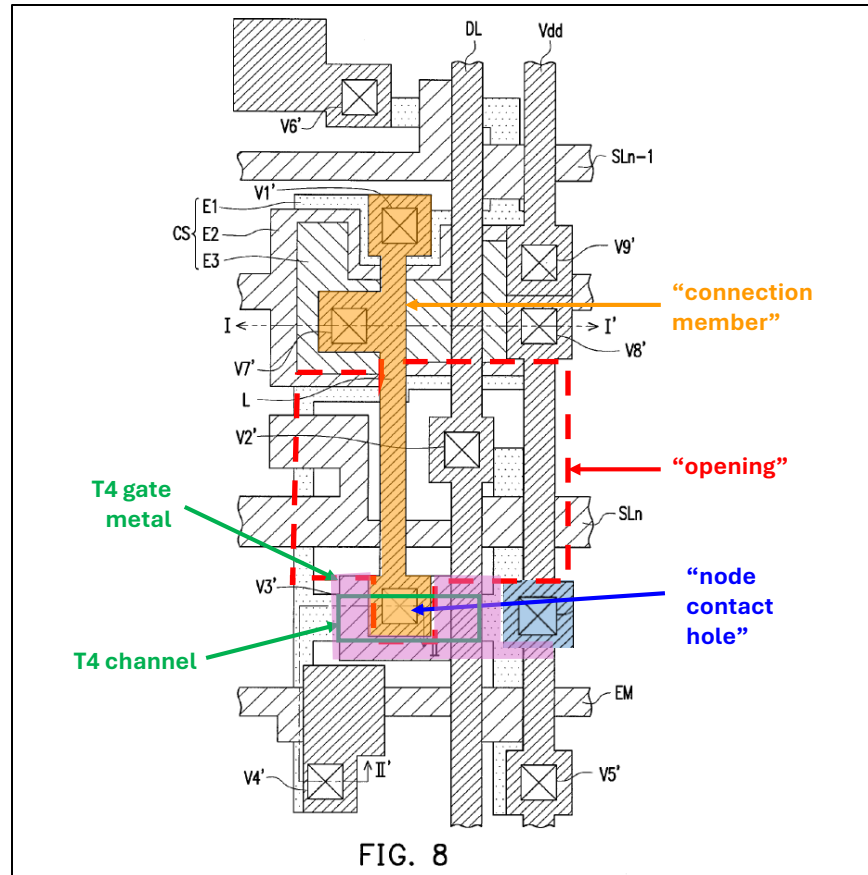
- b. 3[b]: “the portion of the connection member is connected with the first gate electrode through the node contact hole.”

288. As shown for claim 2, Liu100 teaches a portion of signal line L (“connection member”). As shown for element 1[a], Liu100 teaches a gate electrode G4 (“first gate electrode”) of transistor T4. As shown for element 3[a], Liu100 teaches a via structure V3’ (“node contact hole”). As shown for element 1[g], the signal line L is connected with the gate electrode G4 of transistor T4.

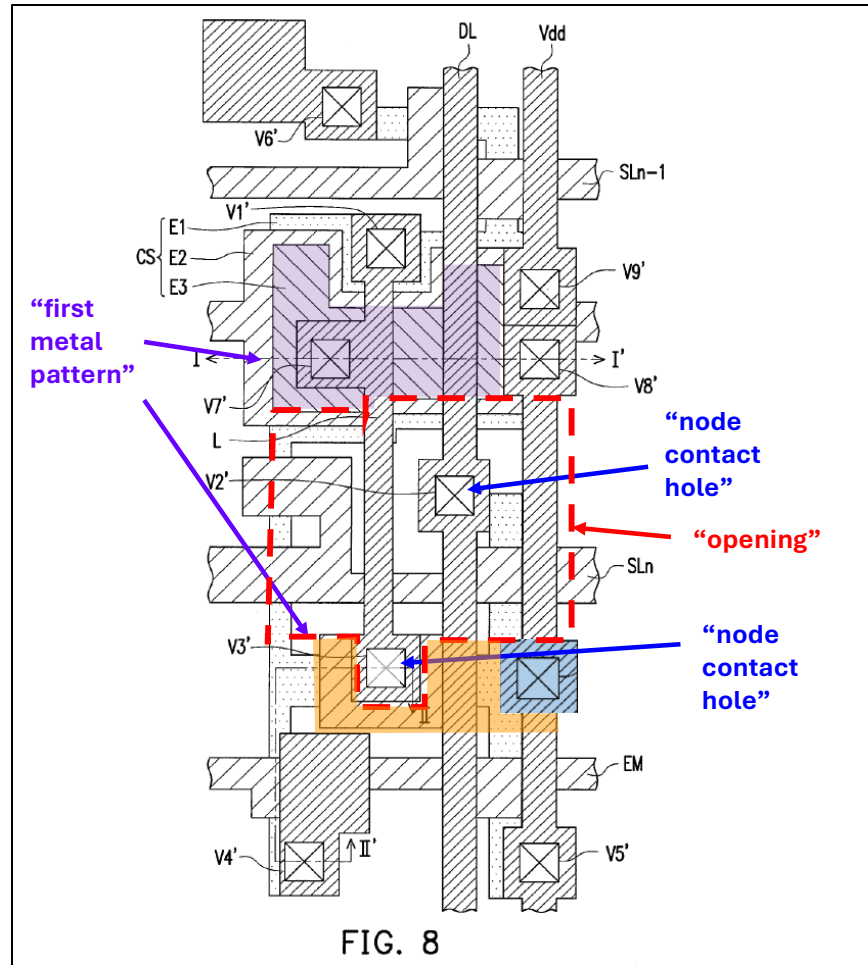
289. Modified Figure 8 (below) shows that the signal line L connects to the gate of transistor T4 through the via structure V3’. As previously shown, transistor T4 is located under via structure V3’. Because a via structure V3’ is a hole that electrically connects to a layer under it, the **signal line L** (“connecting member”) connects to the gate of transistor T4 through **via structure V3’**.



290. Figure 8 (annotated below) shows the gate of transistor T4 being located under (because Figure 8 is a plan view) the via structure V3'.



6. Claim 4: “The TFT array substrate of claim 3, wherein a size of the opening is greater than a size of the node contact hole in the plan view.”



293. It would have been obvious to a POSITA to combine the teachings of Liu100 and Ono. (See Section IX.F.2.g.)

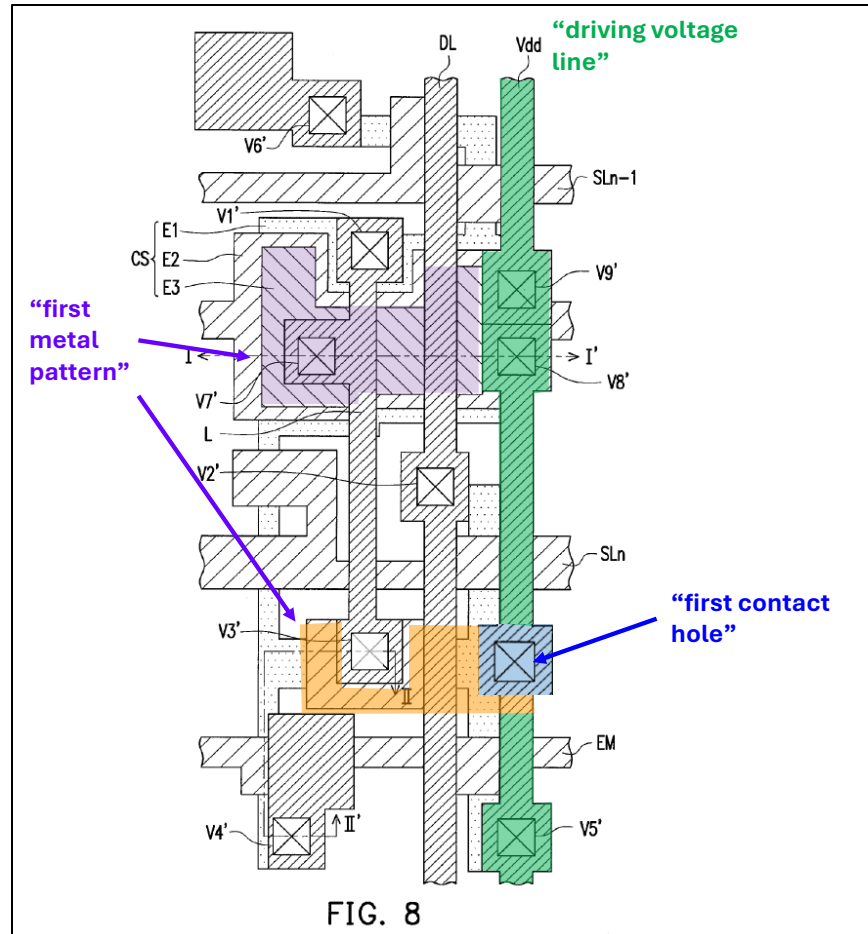
7. **Claim 11: “The TFT array substrate of claim 1, further comprising a driving voltage line on the third insulating layer, wherein the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer.”**

294. As shown for element 1[e], Liu-Ono teaches an extended upper electrode that is part of a “first metal pattern.” As shown for element 1[f], Liu100

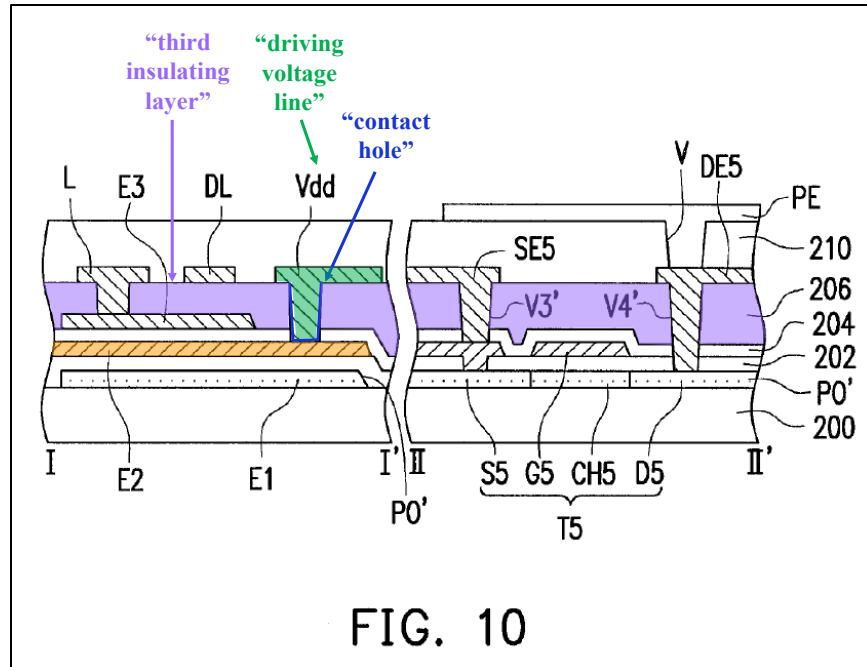
teaches insulating 206 (“third insulating layer”). As shown for element 3[a], Liu100 teaches via structures (“contact hole[s]”).

295. The combination of Liu100 and Ono teaches “a driving voltage line on the third insulating layer, wherein the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer.” For example, Liu100 discloses “the third conductive layer M3’ further comprises a data line DL and a power line Vdd. ... the power line Vdd is electrically connected to the second electrode E2 of the capacitor CS through contact via structures V8-V9’.” (EX1007, [0070].) A POSITA would have understood the power line Vdd is a “driving voltage line” because it delivers power. “[T]he power line Vdd is electrically connected to the drain region D2, as shown in FIG. 1.” (EX1007, [0042].)

296. As shown for element 1[e], the Liu100-Ono combination comprises an extended upper electrode E2 (“first metal pattern”) in the space above the gate of the transistor T4 to increase the total capacitance. The *extended upper electrode* would be electrically coupled to the *power line Vdd* through a *via structure*, as shown in modified Figure 8 (below) of the Liu100-Ono combination.



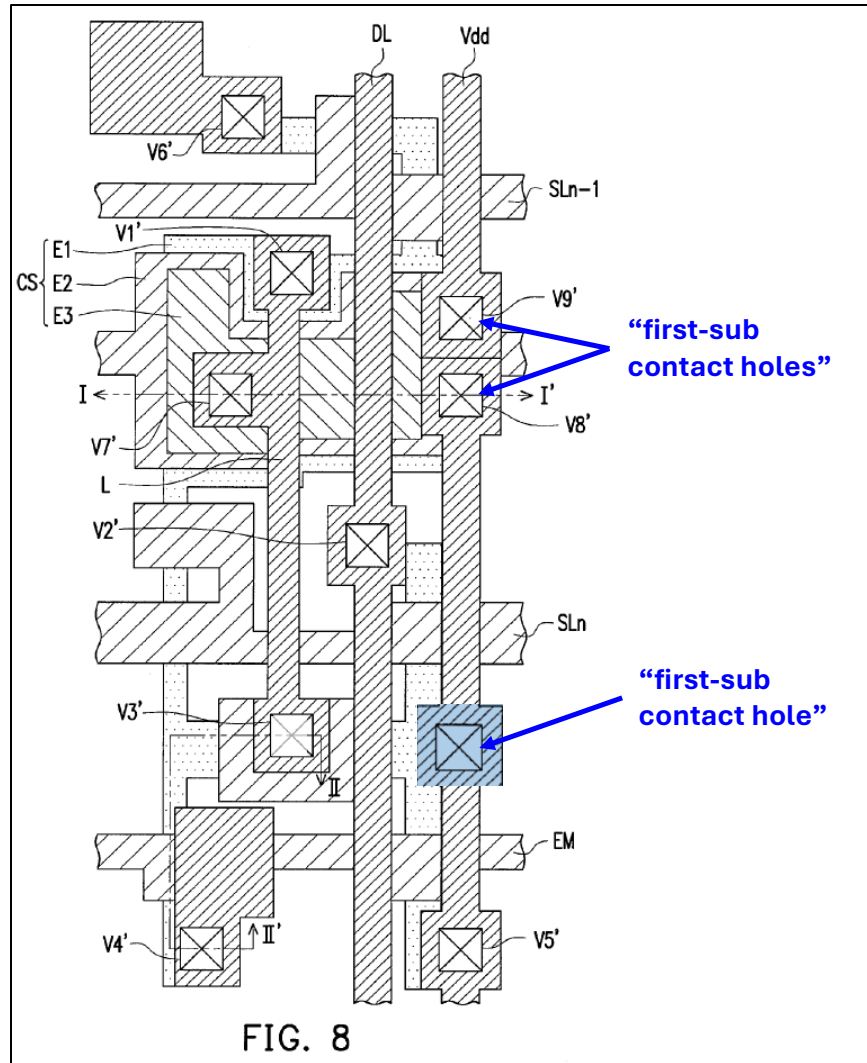
297. As shown for element 3[a], Liu100 teaches using via structures in the insulating layer 206 to make connections between layers. For example, Figure 10 (below) shows the **power line Vdd** on the M3' layer is connected to **electrode E2** on the M1' layer through a **via structure** of the **insulating layer 206**. A POSITA would have understood the power line Vdd on the M3' layer would be similarly be used to connect to the extended upper electrode on the M2' layer through a via structure of the insulating layer 206.



8. **Claim 12: “The TFT array substrate of claim 11, wherein the first contact hole includes a plurality of first-sub contact holes.”**

298. As shown for claim 11, Liu100 teaches via structures (“contact holes”).

299. Figure 8 (below) of the Liu100-Ono combination shows a plurality of via structures that make connections to the power line Vdd (“driving voltage line”).

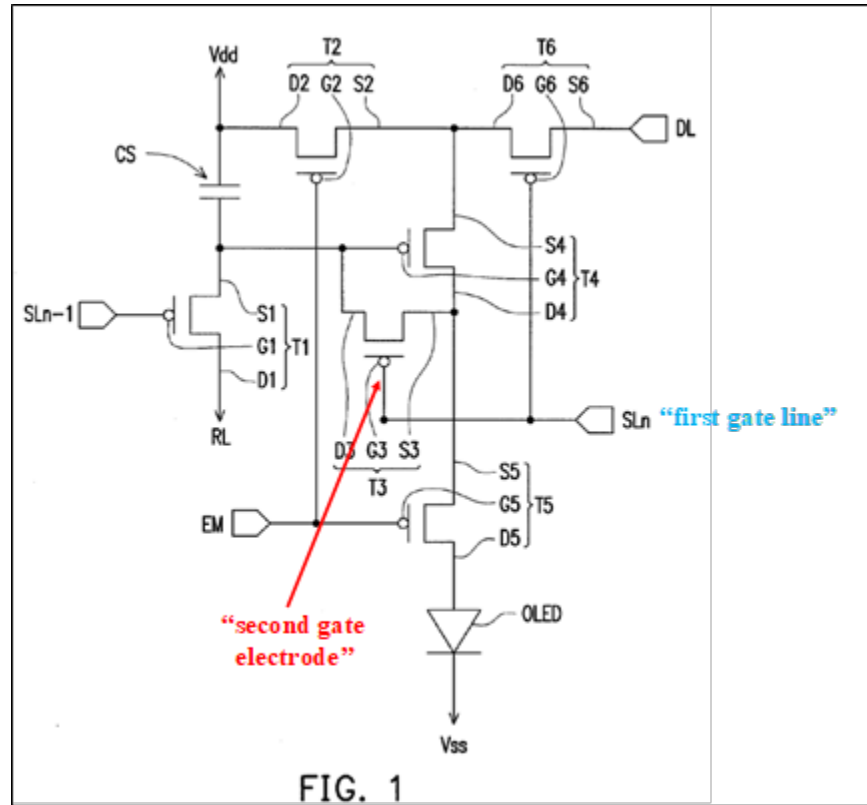


9. Claim 14: “The TFT array substrate of claim 1, further comprising a first gate line electrically connected to the second gate electrode.”

300. Liu100 teaches claim 1 as shown above in Section IX.F.2. As shown for element 1[c], Liu100 teaches a gate G3 (“second gate electrode”).

301. Liu100 teaches “a first gate line electrically connected to the second gate electrode.” For example, referring to Figure 1 (annotated below), Liu100 teaches “the first conductive layer M1 further comprises *a scan line SLn*, a scan

line SL_{n-1} and a light emitting signal line EM, wherein the *scan line SL_n is electrically connected to the gate G_3 *” (EX1007, [0038] (emphases added).)



302. Similarly, referring to Figure 10, Liu100 teaches “the first conductive layer M1’ further comprises a scan line SL_n , a scan line SL_{n-1} and a light emitting signal line EM, wherein the scan line SL_n is electrically connected to the gate G_3 ” (EX1007, [0064].)

10. Claim 15

- a. **15[a]: “The TFT array substrate of claim 14, wherein the second thin film transistor further comprises a first region adjacent to a side of the second channel region and a second region adjacent to another side of the second channel region, and”**

303. Liu100 teaches claim 14 as shown above in Section IX.F.6. As shown for element 1[c], Liu100 teaches a thin film transistor T3 (“second thin film transistor”) that includes a channel region (“second channel region”).

304. Liu100 teaches “the second thin film transistor further comprises a first region adjacent to a side of the second channel region and a second region adjacent to another side of the second channel region.” For example, referring to Figure 1 (annotated below), Liu100 teaches “the semiconductor layer PO has a source region S3, a drain region D3 and a channel region (not shown) in a region predetermined for forming a third film transistor T3.” (EX1007, [0035].) As shown in Figure 1 below, the source region S3 is adjacent to a side of the third film transistor T3 (including the channel region that is not shown), and the drain region D3 is adjacent to another side of the third film transistor T3 (including the channel region that is not shown).

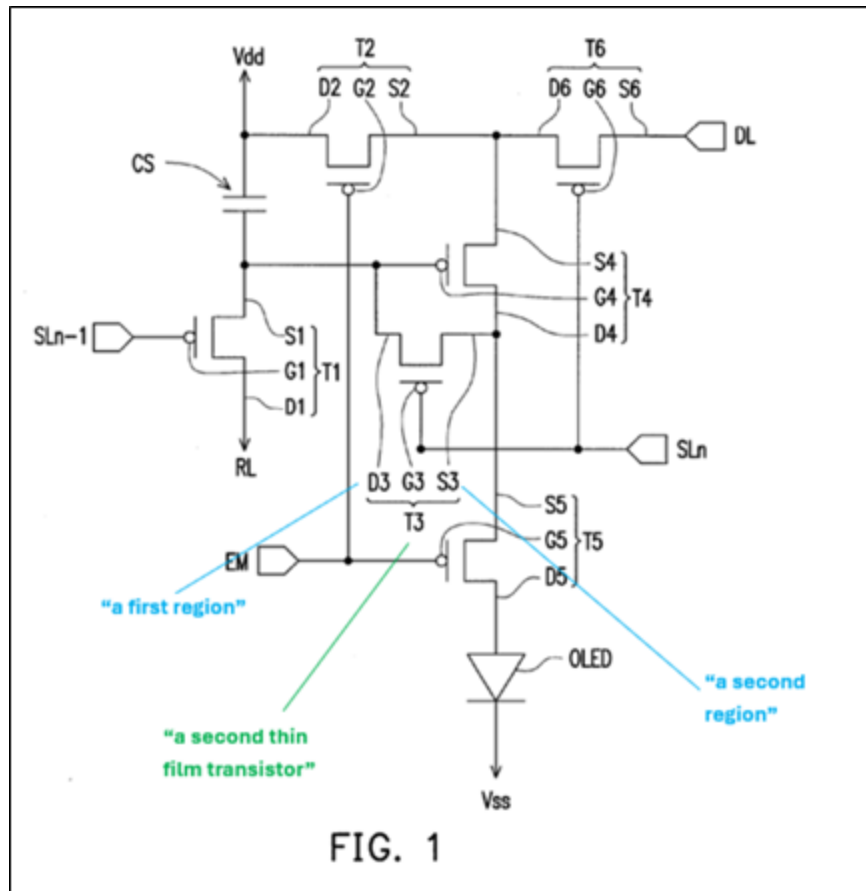


FIG. 1

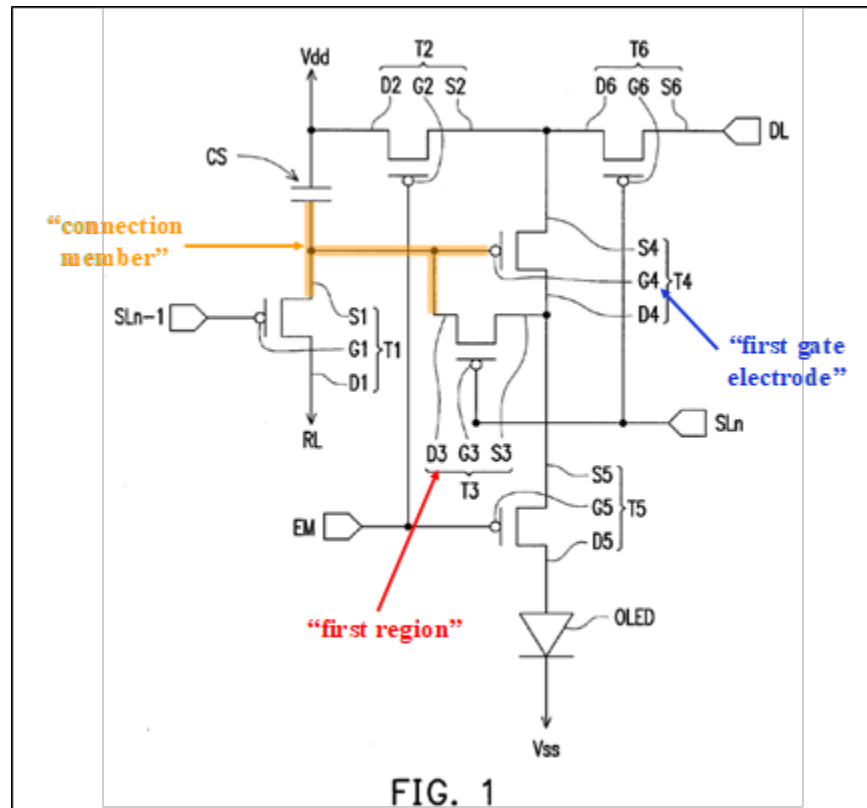
305. As another example, referring to Figure 10 (annotated below), Liu100 teaches the fifth thin film transistor T5 (which, as shown for element 1[c], is similarly configured as all other thin film transistors in the device, including the third thin film transistor T3) “has a source region S5, a drain region D5 and a channel region CH5.” (EX1007, [0060].) As shown in Figure 10 below, the *source region S5* is adjacent to a side of the *channel region CH5*, and the *drain region D5* is adjacent to another side of the channel region CH5. As explained for elements 1[b] and 1[c], the cross-sectional view in Figure 10 is representative of all

306. As shown for element 15[a], Liu100 teaches a drain region D3 (“first region”). As shown for element 1[b], Liu100 teaches a gate G4 (“first gate electrode”). As shown for element 1[g], Liu100 teaches a connection member.

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308. As another example, Liu100 teaches “the second conductive layer M2 further comprises as bottom electrode BE in a region predetermined for forming a capacitor CS, and *the bottom electrode BE is electrically connected to* the source region S1, *the drain region D3 and the gate G4*, as shown in FIG. 1.” (EX1007, [0042] (emphases added).) Figure 1 above shows that the bottom electrode BE is part of the connection member.

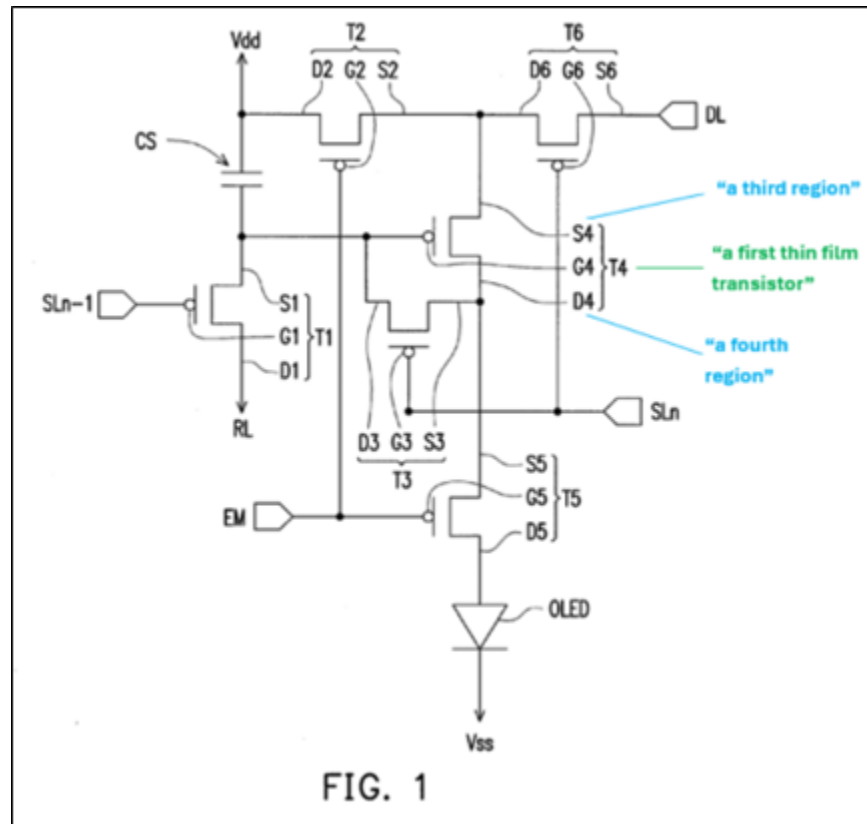
11. Claim 16

- a. **16[a]: “The TFT array substrate of claim 15, wherein the first thin film transistor further comprises a third region adjacent to a side of the first channel region and a fourth region adjacent to another side of the first channel region, and”**

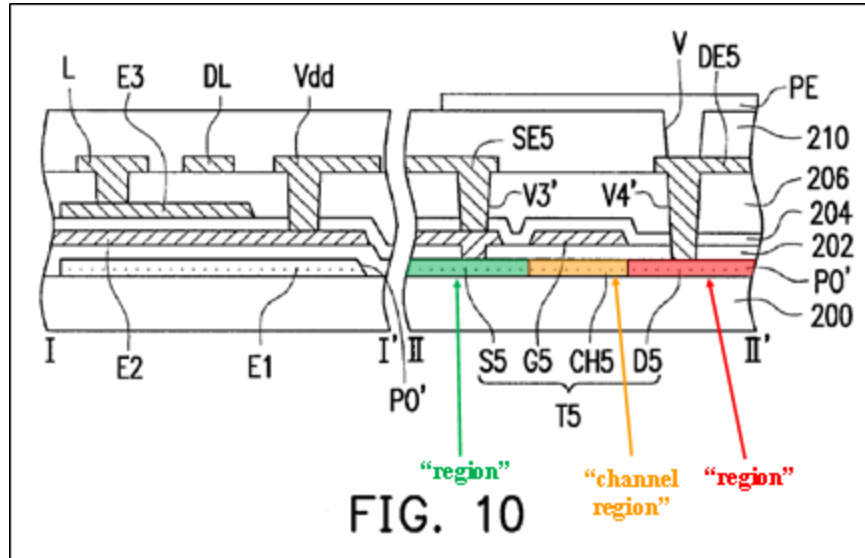
309. Liu100 teaches claim 15 as shown above in Section IX.F.7. As shown for element 1[b], Liu100 teaches a thin film transistor T4 (“first thin film transistor”) comprising channel region CH4 (“first channel region”).

310. Liu100 teaches “the first thin film transistor further comprises a third region adjacent to a side of the first channel region and a fourth region adjacent to another side of the first channel region.” For example, referring to Figure 1 (annotated below), Liu100 discloses “the semiconductor layer PO has a source region S4, a drain region D4 and a channel region (not shown) in a region predetermined for forming a fourth thin film transistor T4.” (EX1007, [0035].)

The annotated figure shows the *source region S4* is adjacent to a side of the *thin film transistor T4* (including the channel region that is not shown), and the *drain region D4* is adjacent to another side of the fourth thin film transistor T4 (including the channel region that is not shown).



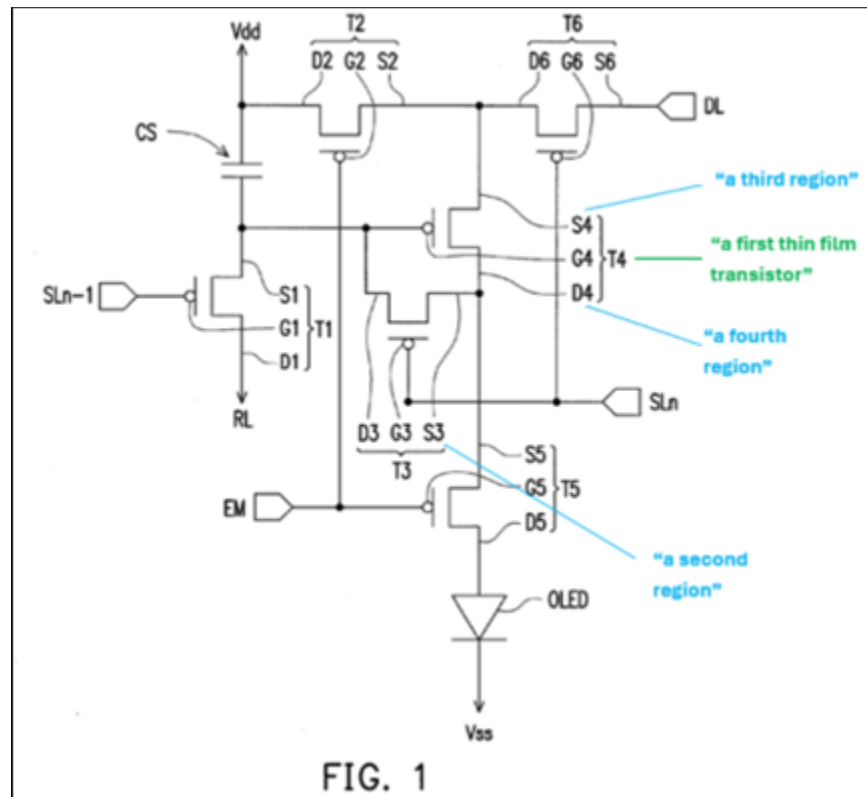
311. As another example, referring to Figure 10 (annotated below), Liu100 teaches the fifth thin film transistor T5 (which, as shown in element 1[c], is similarly configured as all other thin film transistors in the device, including the fourth thin film transistor T4) “has a source region S5, a drain region D5 and a channel region CH5.” (EX1007, [0060].) The figure below shows the *source region S5* is adjacent to a side of the *channel region CH5*, and the *drain region D5* is adjacent to another side of the channel region CH5. As explained for elements 1[b] and 1[c], the cross-sectional view in Figure 10 is representative of all the thin film transistors in the pixel structure. (EX1007, [0058].) Thus, Liu100 teaches element 16[a].



b. 16[b]: “the second region is electrically connected to the fourth region.”

312. As shown for element 15[a], Liu100 teaches a source region S3 (“second region”). As shown for element 16[a], Liu100 teaches a drain region D4 (“fourth region”).

313. Liu100 teaches “the second region is electrically connected to the fourth region.” For example, referring to Figure 1 (annotated below), the source region S3 (“second region”) is electrically connected to drain region D4 (“fourth region”).

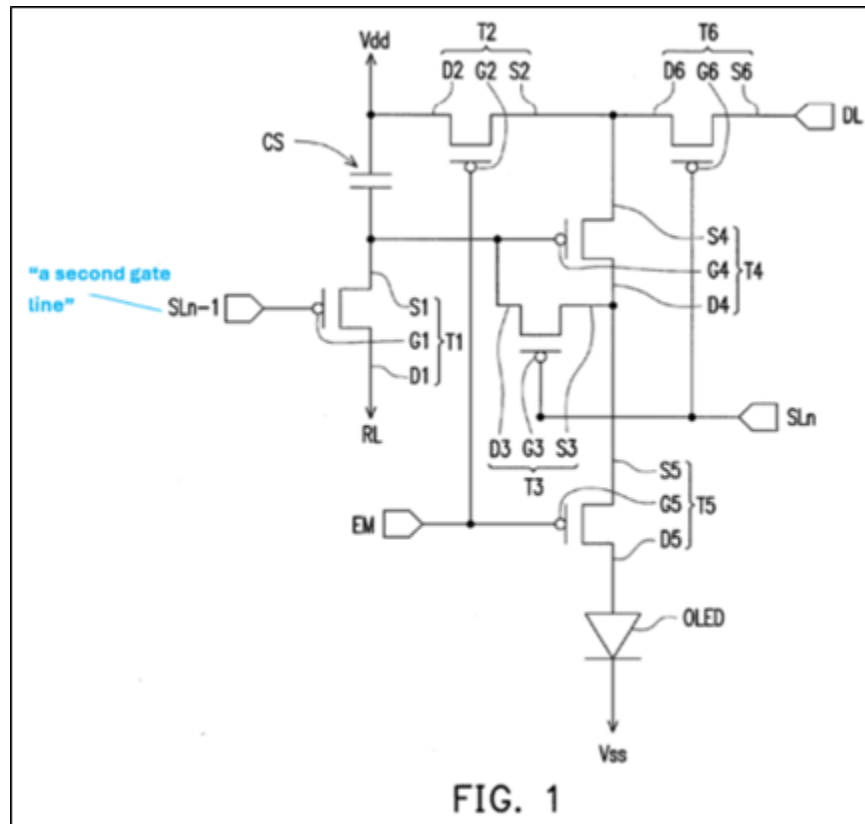


12. Claim 17

- a. 17[a]: “The TFT array substrate of claim 14, further comprising a second gate line, and”

314. Liu100 teaches claim 14 as shown above in Section IX.F.6.

315. Liu100 discloses “a second gate line.” For example, referring to Figure 1 (annotated below), Liu100 discloses “the first conductive layer M1 further comprises a scan line SL_n , a scan line SL_{n-1} and a light emitting signal line EM, wherein . . . the scan line SL_{n-1} is electrically connected to the gate $G1$ ” (EX1007, [0038] (emphases added).)

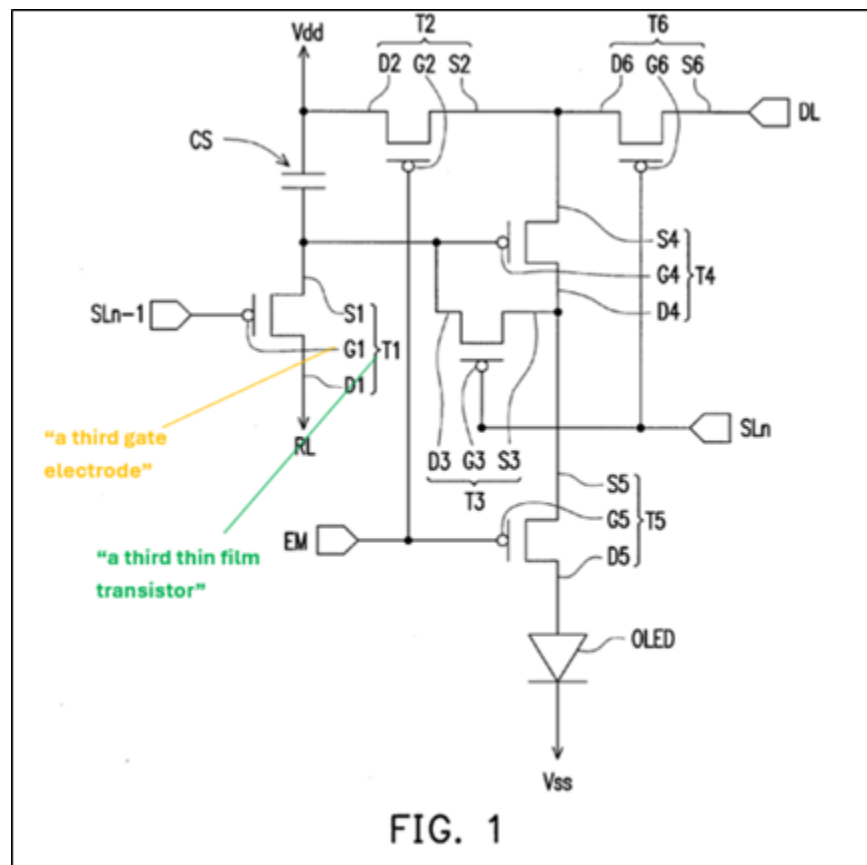


316. Similarly, referring to Figure 10, Liu100 teaches “the first conductive layer M1’ further comprises a scan line SL_n , *a scan line SL_{n-1}* and a light emitting signal line EM, wherein . . . *the scan line SL_{n-1} is electrically connected to the gate G1 . . .*” (EX1007, [0064] (emphases added).)

- b. 17[b]: “a third thin film transistor, the third thin film transistor including a third gate electrode and a third channel region overlapping the third gate electrode, the third gate electrode and the third channel region being spaced apart from each other with the first insulating layer therebetween, and”

317. As shown for element 1[b], Liu100 teaches an insulating layer 202 (“first insulating layer”).

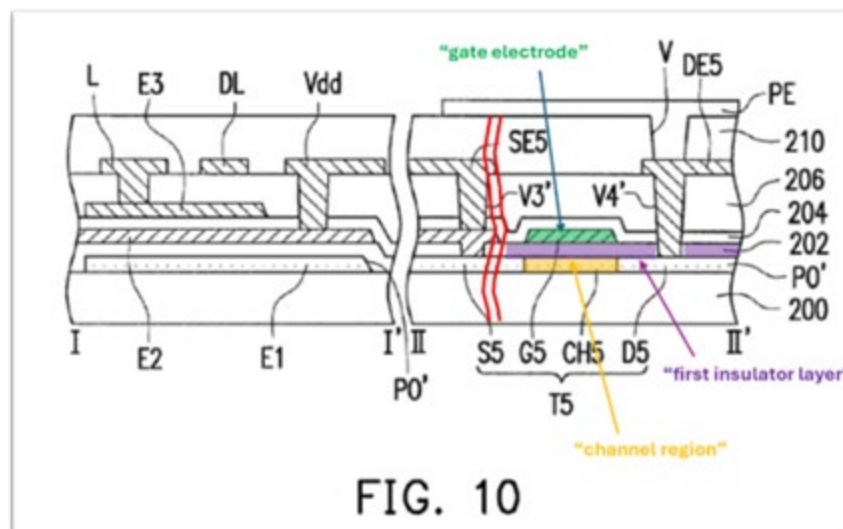
318. Liu100 discloses “a third thin film transistor, the third thin film transistor including a third gate electrode and a third channel region.” For example, referring to Figure 1 (annotated below), Liu100 discloses “the semiconductor layer PO has a source region S1, a drain region D1 and *a channel region (not shown)* in a region predetermined for forming *a first thin film transistor T1.*” (EX1007, [0035] (emphasis added).) Liu100 further discloses “the first conductive layer M1 has a *gate G1* in the region predetermined for forming the first *thin film transistor T1.*” (EX1007, [0038] (emphasis added).)



319. Referring to Figure 10 (annotated below), Liu100 teaches “the pixel structure is disposed on a substrate 200 and comprises a semiconductor layer PO’.”

(EX1007, [0058].) Liu100 discloses that the fifth thin film transistor T5 (which, as shown for element 1[c], is similarly configured as all other thin film transistors in the device, including the first thin film transistor T1) includes “the semiconductor layer PO’ [which] has a source region S5, a drain region D5 and a channel region CH5 in a region predetermined for forming a fifth thin film transistor T5.”

(EX1007, [0060].) “The first insulating layer 202 covers the semiconductor layer PO’.” (EX1007, [0058].) The annotated figure below shows that the *channel region* overlaps the *gate electrode*.



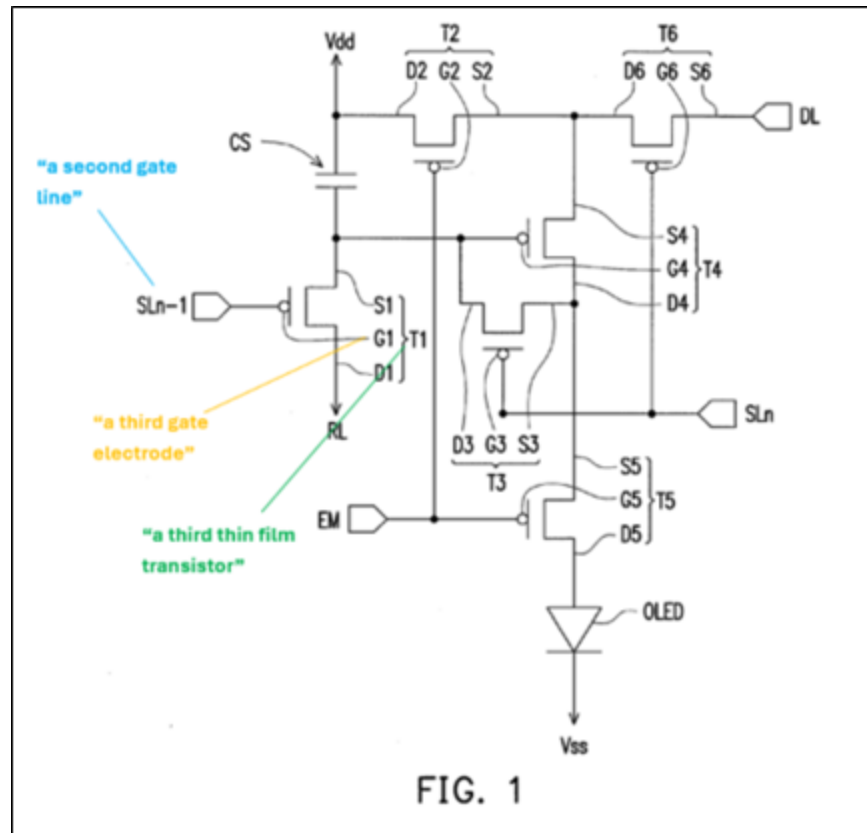
320. Also referring to Figure 10 (annotated above), Liu100 teaches “[t]he first conductive layer M1’ is disposed on the first insulating layer 202,” where “the first conductive layer M1’ has a gate G5 in the region predetermined for forming the fifth thin film transistor T5.” (EX1007, [0063].) The figure shows that the

gate electrode and the *channel region* are spaced apart from each other with *insulating layer 202* therebetween.

c. 17[c]: “wherein the second gate line is electrically connected to the third gate electrode.”

321. As shown for element 17[a], Liu100 teaches a scan line SL_{n-1} (“second gate line”). As shown for element 17[b], Liu100 teaches a gate G1 (“third gate electrode”).

322. Liu100 discloses “the second gate line is electrically connected to the third gate electrode.” For example, referring to Figure 1 (annotated below), Liu100 discloses “the scan line SL_{n-1} is electrically connected to gate G1.” (EX1007, [0038]; *see also* EX1007, [0064] (“In addition, the first conductive layer M1’ further comprises a scan line SL_n, a scan line SL_{n-1} and a light emitting signal line EM, wherein the scan line SL_n is electrically connected to the gate G3, *the scan line SL_{n-1} is electrically connected to the gate G1*, and the light emitting signal line EM is electrically connected to the gates G5, G2.”) (emphasis added).)



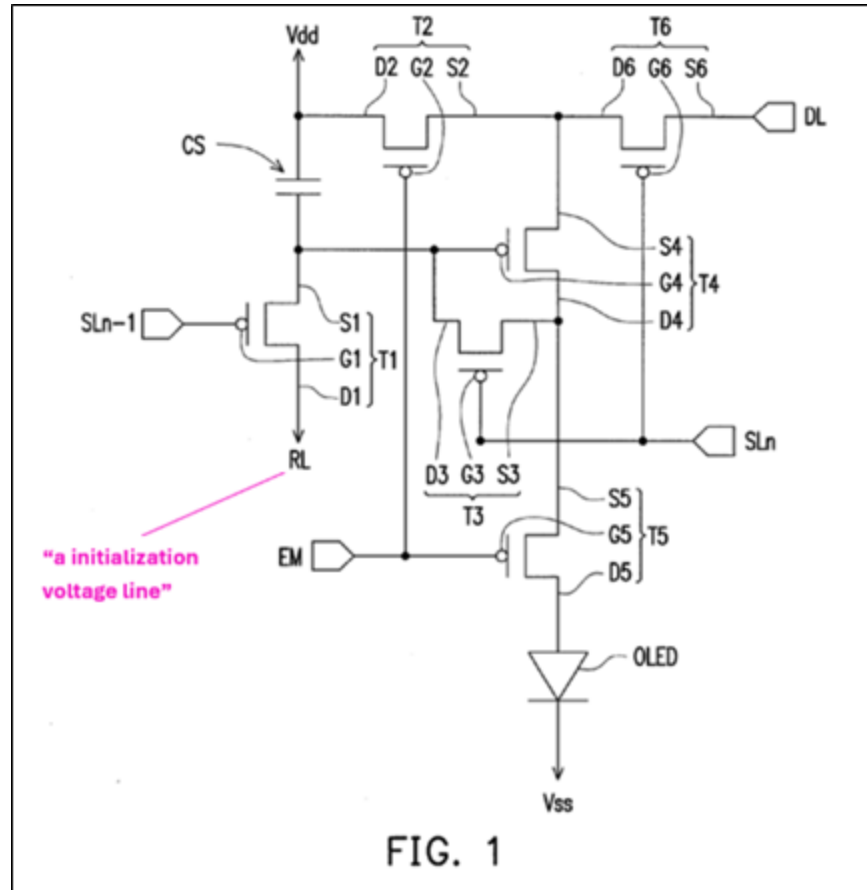
13. Claim 18

- a. 18[a]: “The TFT array substrate of claim 17, further comprising a[n] initialization voltage line,”

323. Liu100 teaches claim 17 as shown above in Section IX.F.9.

324. Liu100 teaches “a[n] initialization voltage line.” For example, referring to Figure 1 (annotated below), Liu100 discloses “the first conductive layer M1 may further comprise a *reference signal line RL*.” (EX1007, [0038] (emphasis added).) The transistor T1 is configured to provide the reference signal to the gate G4 of the transistor T4, which is a driving transistor. As such, transistor

T1 is an initialization transistor, and the reference signal line RL is an initialization voltage line.



- b. 18[b]: “wherein the third thin film transistor further comprises a fifth region adjacent to a side of the third channel region and a sixth region adjacent to another side of the third channel region, and”

325. As shown for element 17[b], Liu100 teaches a thin film transistor T1 (“third thin film transistor”) comprising a channel region CH1 (“third channel region”).

326. Liu100 teaches “the third thin film transistor further comprises a fifth region adjacent to a side of the third channel region and a sixth region adjacent to another side of the third channel region.” For example, referring to Figure 1 (annotated below), Liu100 discloses “the semiconductor layer PO has a source region S1, a drain region D1 and a channel region (not shown) in a region predetermined for forming a first thin film transistor T1.” (EX1007, [0035].) As shown in Figure 1 below, the *source region S1* is adjacent to a side of the *thin film transistor T1* (including the channel region that is not shown), and the *drain region D1* is adjacent to another side of the thin film transistor T1 (including the channel region that is not shown).



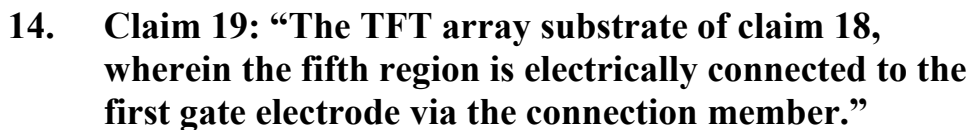
327. As another example, referring to Figure 10 (annotated below), Liu100 teaches the fifth thin film transistor T5 (which, as shown for element 1[c], is similarly configured as all other thin film transistors in the device, including the thin film transistor T1) “has a source region S5, a drain region D5 and a channel region CH5.” (EX1007, [0060].) As shown in Figure 10 below, the *source region S5* is adjacent to a side of the *channel region CH5*, and the *drain region D5* is adjacent to another side of the channel region CH5.



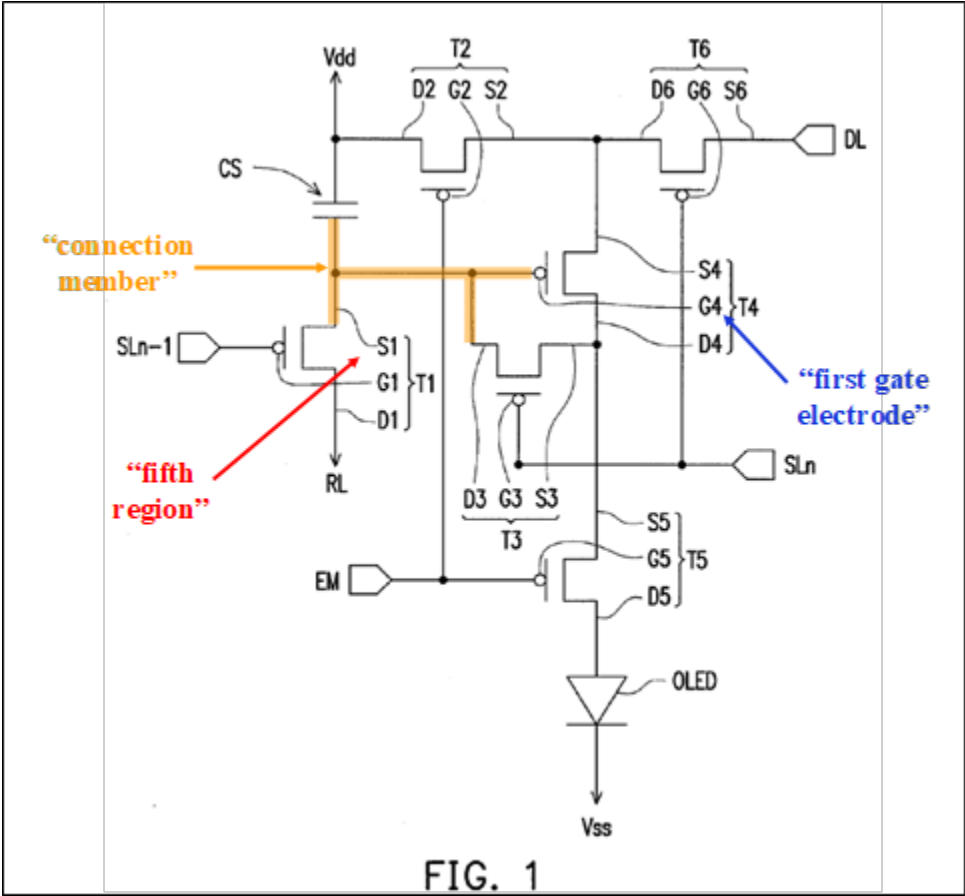
c. 18[c]: “the sixth region is electrically connected to the initialization voltage line.”

328. As shown for element 18[a], Liu100 teaches a reference signal line RL (“initialization voltage line”). As shown for element 18[b], Liu100 teaches a drain region D1 (“sixth region”).

329. Liu100 teaches “the sixth region is electrically connected to the initialization voltage line.” For example, as shown below on Figure 1 (annotated below), Liu100 teaches that the *drain* (“sixth region”) of transistor T1 is electrically connected to *reference signal line RL* (“initialization voltage line”).



331. Liu100 teaches “the fifth region is electrically connected to the first gate electrode via the connection member.” For example, as shown in Figure 1 (annotated below), Liu100 teaches that the *source region S1* is electrically connected to *gate G4* via the *connection member*.



15. Claim 22

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

332. The preamble of claim 22 is similar to the preamble of claim 1, which Liu100 and Ono teach. (See Section IX.F.2.a.) The table below shows the similarities.

Preamble of Claim 1	Preamble of Claim 22
“A thin film transistor (TFT) array substrate comprising:”	“A thin film transistor (TFT) array substrate comprising:”

b. 22[a]: “a substrate;”

333. Element 22[a] is similar to element 1[a], which Liu100 and Ono teach. (See Section IX.F.2.b.) The table below shows the similarities.

Element 1[a]	Element 22[a]
“a substrate;”	“a substrate;”

c. 22[b]: “a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”

334. Element 22[b] is similar to element 1[b], which Liu100 and Ono teach. (See Section IX.F.2.c.) The table below shows the similarities.

Element 1[b]	Element 22[b]
““a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”	“a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”

d. 22[c]: “a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”

335. Element 22[c] is similar to element 1[c], which Liu100 and Ono teach. (See Section IX.F.2.d.) The table below shows the similarities.

Element 1[c]	Element 22[c]
“a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”	“a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”

e. 22[d]: “a second insulating layer disposed on the first and second gate electrode;”

336. Element 22[d] is similar to element 1[d], which Liu100 and Ono teach. (See Section IX.F.2.e.) The table below shows the similarities.

Element 1[d]	Element 22[d]
“a second insulating layer disposed on the first and second gate electrode;”	“a second insulating layer disposed on the first and second gate electrode;”

f. 22[e]: “a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”

337. Element 22[e] is similar to element 1[e], which Liu100 and Ono teach. (See Section IX.F.2.f.) The table below shows the similarities.

Element 1[e]	Element 22[e]
“a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”	“a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”

g. 22[f]: “a third insulating layer disposed on the first metal pattern; and”

338. Element 22[f] is similar to element 1[f], which Liu100 and Ono render obvious. (See Section IX.F.2.g.) The table below shows the similarities.

Element 1[f]	Element 22[f]
“a third insulating layer disposed on the first metal pattern; and”	“a third insulating layer disposed on the first metal pattern; and”

h. 22[g]: “a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor,”

339. Element 22[g] is similar to element 1[g], which Liu100 and Ono render obvious. (See Section IX.F.2.h.) The table below shows the similarities.

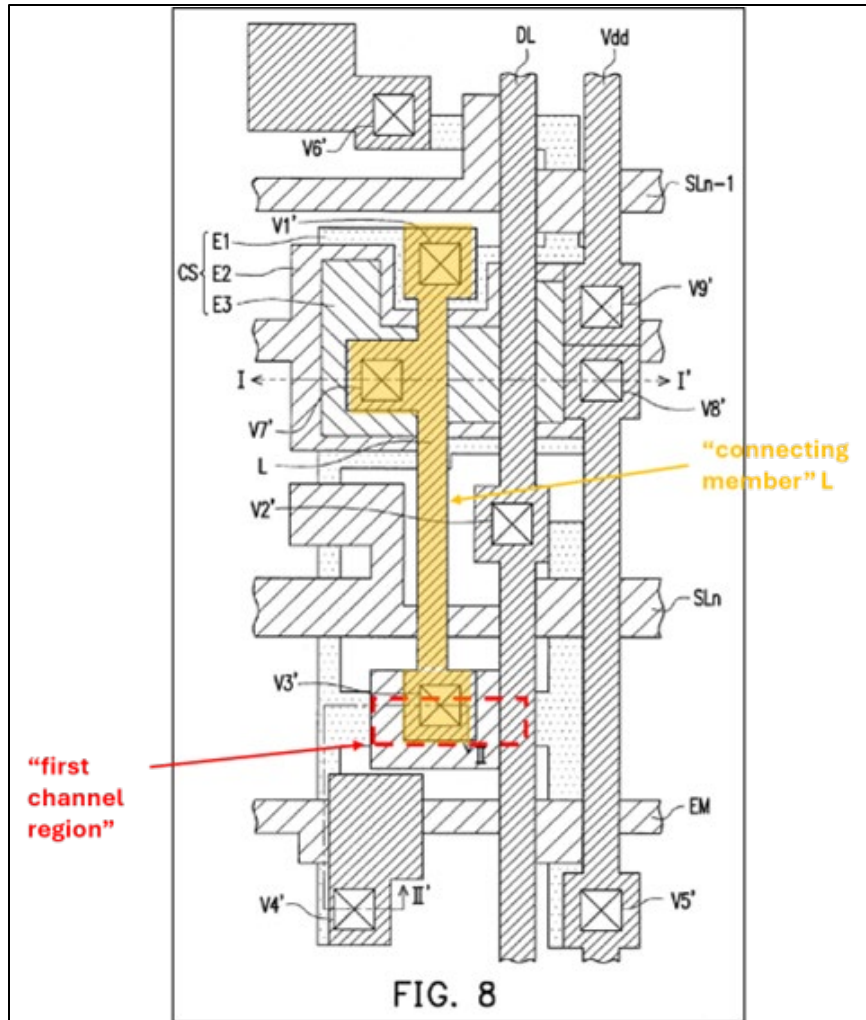
Element 1[g]	Element 22[g]
“a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor.”	“a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor,”

i. 22[h]: “the connection member overlapping a portion of the first channel region in a plan view.”

340. As shown in elements 1[b] and 1[g], Liu100 teaches channel region CH4 (“first channel region”) and a signal line L (“connection member”).

341. Liu100 teaches “the connection member overlapping a portion of the first channel region in a plan view.” For example, referring to Figure 1, Liu100 teaches the fourth thin film transistor T4 (“first thin film transistor”) “has a source region S4, a drain region D4 and a channel region (not shown).” (EX1007, [0035].) Liu100 explains that “[t]he semiconductor layer PO' includes a source region S, a drain region D and a channel region CH.” (EX1007, [0077].) Figure 8 (annotated below) shows the signal line L overlaps a portion of the channel region CH4 of the thin film transistor T4. Thus, Liu100 discloses element 22[h].

Additionally, it was known by a POSITA at the time for the connection member to overlap the channel region.



16. **Claim 23:** “The TFT array substrate of claim 22, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in the plan view.”

342. Claim 23 is similar to claim 2, which Liu100 and Ono render obvious.

(See Section IX.F.3.) The table below shows the similarities.

Claim 2	Claim 23
“The TFT array substrate of claim 1, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.”	“The TFT array substrate of claim 22, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in the plan view.”

17. **Claim 24: “The TFT array substrate of claim 23, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and the portion of the connection member is connected with the first gate electrode through the node contact hole.”**

343. Claim 24 is similar to claim 3, which Liu100 and Ono render obvious.

(See Section IX.F.4.) The table below shows the similarities.

Claim 3	Claim 24
“The TFT array substrate of claim 2, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and the portion of the connection member is connected with the first gate electrode through the node contact hole.”	“The TFT array substrate of claim 23, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and the portion of the connection member is connected with the first gate electrode through the node contact hole.”

18. **Claim 28: “The TFT array substrate of claim 27, wherein the first contact hole includes a plurality of first-sub contact holes.”**

344. Claim 28 is similar to claim 12, which Liu100 and Ono teach. (See Section IX.D.2.) The table below shows the similarities.

Claim 12	Claim 28
“The TFT array substrate of claim 11, wherein the first contact hole includes a plurality of first-sub contact holes.”	“The TFT array substrate of claim 27, wherein the first contact hole includes a plurality of first-sub contact holes.”

19. Claim 29: “The TFT array substrate of claim 28, wherein at least one of the plurality of first-sub contact holes overlaps the first channel region in the plan view.”

345. Claim 29 is similar to claim 13, which Liu100 and Ono teach. (See Section IX.D.3.) The table below shows the similarities.

Claim 13	Claim 29
“The TFT array substrate of claim 12, wherein at least one of the plurality of first-sub contact holes overlaps the first channel region in a plan view.”	“The TFT array substrate of claim 28, wherein at least one of the plurality of first-sub contact holes overlaps the first channel region in the plan view.”

I. Claims 7-10, 25, And 26 Are Obvious Over Liu100, Ono, And Osame

1. Claim 7: “The TFT array substrate of claim 1, wherein the first channel region includes a bent portion.”

346. Liu100 and Ono teach claim 1 as shown above in Section IX.F.2. As shown in Section IX.C.2, Osame teaches claim 7.

a. Motivation to combine Liu100, Ono, and Osame

347. It would have been obvious to a POSITA at the time of the ’483 patent to combine the teachings of Liu100, Ono, and Osame. Liu100, Ono, and Osame all relate to OLED devices with transistors that efficiently use space in the device’s pixel structure without compromising image quality. Liu100 discloses a pixel structure of an OLED device that is “capable of reducing an area occupied by components of the pixel structure.” (EX1007, [0007].) Ono discloses “a luminescent display device with higher design flexibility by forming a capacitor

without a region dedicated to the capacitor or a new region dedicated to the capacitor.” (EX1008, [0030].) Similarly, Osame discloses a “light-emitting device which realizes a high aperture ratio and in which the quality of image is little affected by the variation of the driving TFTs.” (EX1014, [0030].) Thus, Liu100, Ono, and Osame are from the same field of endeavor and reasonably pertinent to the same technical problem of efficiently using the space in the pixel structure of light-emitting devices.

348. Ono teaches a luminescent display device where “the gate electrode of the thin-film transistor is used not only simply as the gate electrode but also as one of two electrodes constituting the capacitor.” (EX1008, [0029].) “Thus, the capacitor can be formed above the thin-film transistor to overlap with the thin-film transistor, enabling efficient use of the pixel space.” (*Id.*) Ono solves the conventional problem “when the number of capacitors or the capacitor area increases, the region for forming other elements becomes smaller, resulting in less design flexibility.” (EX1008, [0008].) Ono’s technical features may be combined with Liu100’s teachings with a reasonable expectation of success to generate a smaller light-emitting device with increase storage capacitor area without decreasing the device’s quality.

349. Osame teaches light-emitting devices comprising different shapes for increasing TFT channel length and channel width without decreasing aperture

ratio. Osame's technical features may be further combined with the teachings of Liu100 and Ono with a reasonable expectation of success to generate a smaller light-emitting device with increased storage capacitance without decreasing the device's aperture ratio.

350. A POSITA would be motivated to use the techniques disclosed in Osame and Ono to improve the similar device of Liu100 in the same way. It would have been obvious to try combining the teachings of Liu100 and Ono because Ono teaches placing a capacitor over a gate electrode was known in the art. Ono's technique increases the overall capacitance of the pixel structure resulting in improved display performance without using additional area. Further, it would have been obvious to try combining the teachings of Liu100, Ono, and Osame because Osame teaches changing the shape of the semiconductor layer's channel region is a simple substitution and offers a number of configurations to try. Prior art such as Ono successfully demonstrated an OLED device configuration that shrinks the size of the components within a pixel structure. There would have been a reasonable expectation of success for combining Liu100 and Ono by modifying the configuration of the capacitor and gate electrode in Liu100. Moreover, prior art such as Osame successfully demonstrated an OLED configuration that with different shapes of the semiconductor layer's channel region increased the design flexibility without compromising on device quality,

and thus, there would have been a reasonable expectation of success for further combining Liu100, Ono, and Osame by modifying the configuration of the shape of the semiconductor layer's channel region. Thus, it would have been obvious to a POSITA to combine the teachings of Liu100, Ono, and Osame.

2. Claim 8: “The TFT array substrate of claim 7, wherein the first channel region includes at least two bent portions.”

351. Liu100 and Ono teach claim 7 as shown above in Section IX.G.1. As shown in Section IX.C.3, Osame teaches claim 8.

352. It would have been obvious to a POSITA to combine the teachings of Liu100, Ono, and Osame. (*See* Section IX.G.1.)

3. Claim 9: “The TFT array substrate of claim 7, wherein the first channel region is curved in an ‘S’ shape.”

353. Liu100 and Ono teach claim 7 as shown above in Section IX.G.1. As shown in Section IX.C.4, Osame teaches claim 9.

354. It would have been obvious to a POSITA to combine the teachings of Liu100, Ono, and Osame. (*See* Section IX.G.1.)

4. Claim 10: “The TFT array substrate of claim 7, wherein the first channel region is curved in a zigzag shape.”

355. Liu100 and Ono teach claim 7 as shown above in Section IX.G.1. As shown in Section IX.C.5, Osame teaches claim 10.

356. It would have been obvious to a POSITA to combine the teachings of Liu100, Ono, and Osame. (*See* Section IX.G.1.)

5. Claim 25: “The TFT array substrate of claim 22, wherein the first channel region includes a bent portion.”

357. Liu100 and Ono teach claim 22 as shown above in Section IX.F.12.

358. Claim 25 is similar to claim 7, which Liu100, Ono, and Osame render obvious. (*See* Section IX.G.1.) The table below shows the similarities.

Claim 7	Claim 25
“The TFT array substrate of claim 1, wherein the first channel region includes a bent portion.”	“The TFT array substrate of claim 22, wherein the first channel region includes a bent portion.”

6. Claim 26: “The TFT array substrate of claim 25, wherein the first channel region is curved in a zigzag shape.”

359. Claim 26 is similar to claim 10, which Liu100, Ono, and Osame render obvious. (*See* Section IX.G.1.) The table below shows the similarities.

Claim 10	Claim 26
“The TFT array substrate of claim 7, wherein the first channel region is curved in a zigzag shape.”	“The TFT array substrate of claim 25, wherein the first channel region is curved in a zigzag shape.”

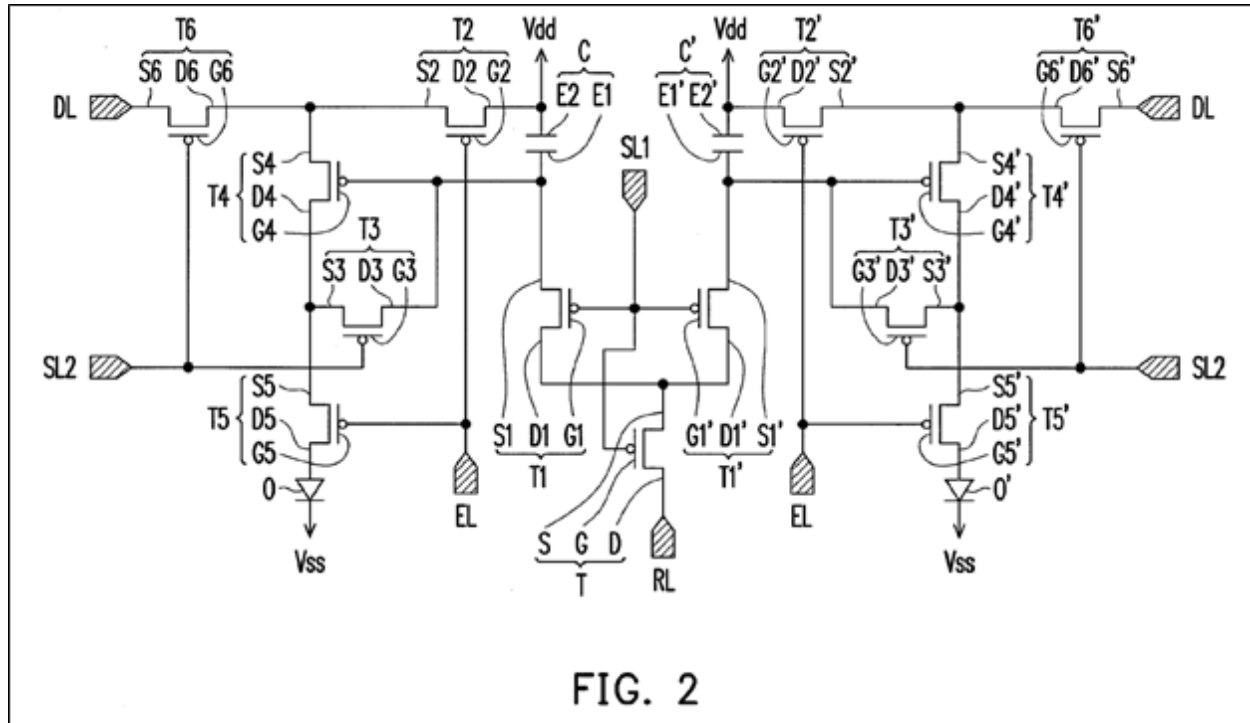
J. Claims 20 And 21 Are Obvious Over Liu100, Ono, And Liu080

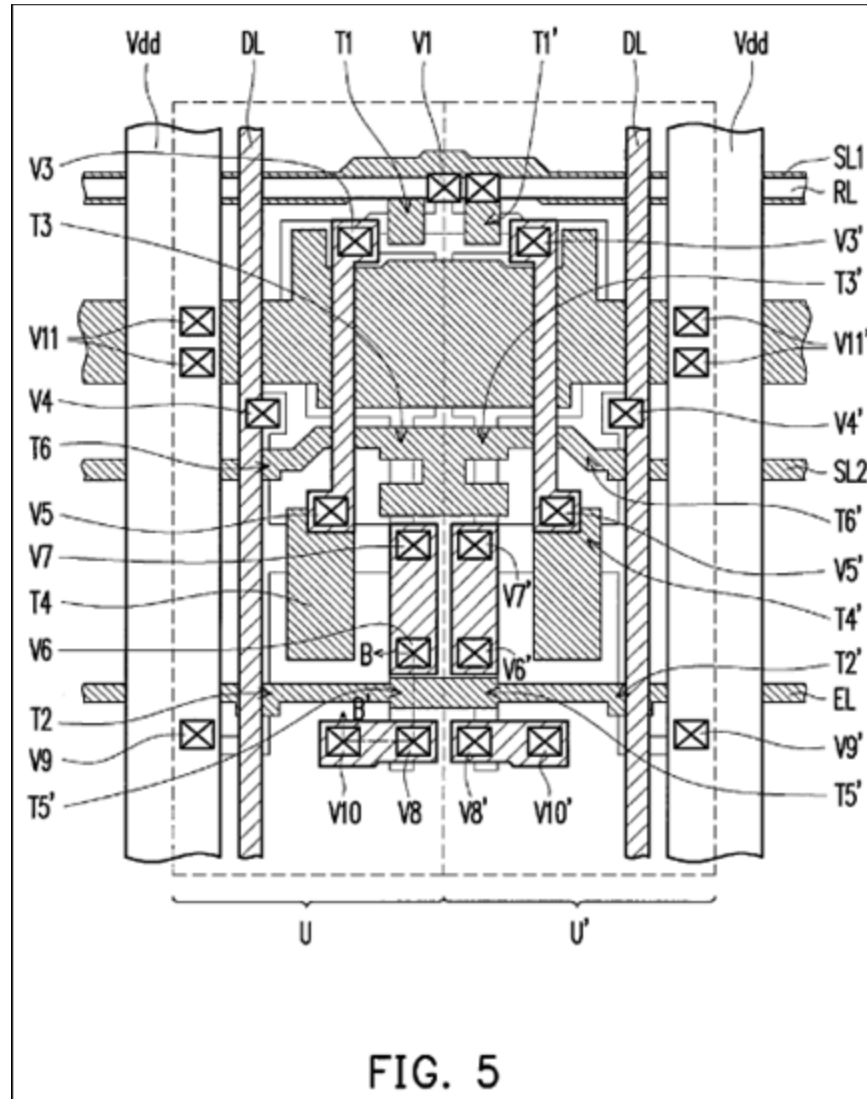
1. Summary of Liu080

360. Liu080 discloses “a pixel structure of an organic light emitting device, where the pixel structures each can reduce an area occupied by components of the

pixel structure.” (EX1012, [0007].) Liu080 reduces the area of the pixel structure by having “the first pixel unit and the second pixel unit of the pixel structure in the invention share the common TFT.” (EX1012, [0056].) This sharing of the common TFT saves space by reducing the number of transistors (and space occupied) in the overall OLED device.

361. Figures 2 and 5 (below) show the circuit and plan view, respectively, of Liu080’s OLED device.



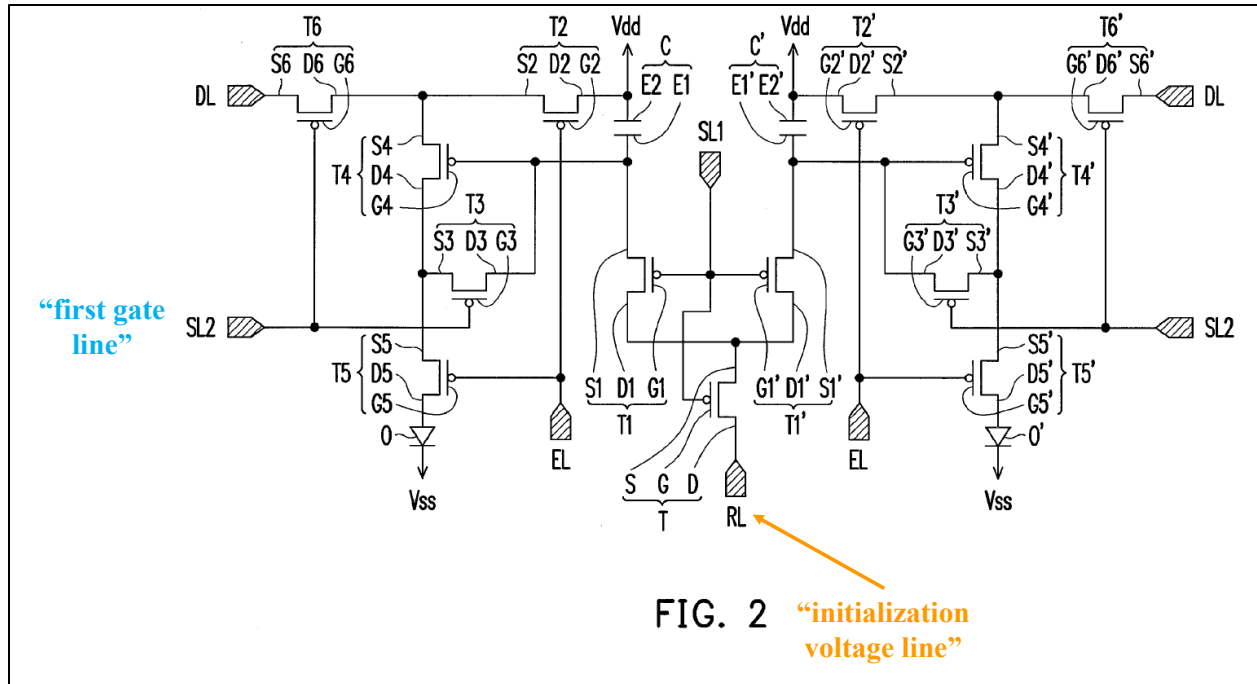


2. **Claim 20:** “The TFT array substrate of claim 18, wherein the initialization voltage line extends in the same direction as the first gate line.”

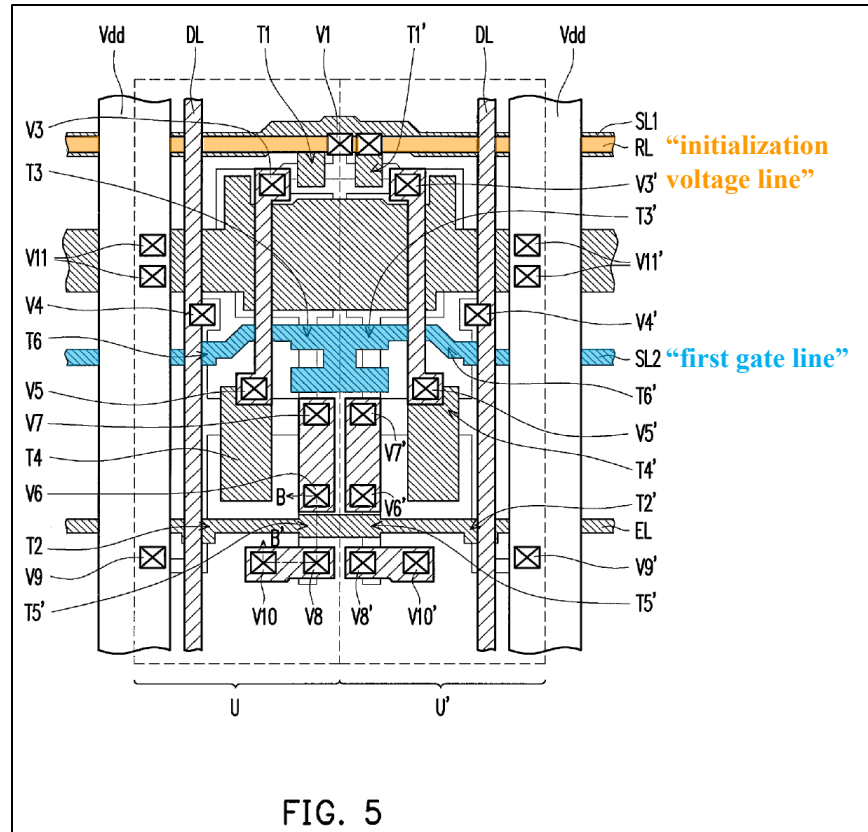
362. As shown for element 18[a], Liu100 teaches a reference signal line RL (“initialization voltage line”) electrically connected to the drain of an initialization transistor T1. As shown for claim 14, Liu100 teaches a scan line SLn (“first gate line”) electrically connected to the gate G3 of a transistor T3. The

transistor T3 has a drain D3 connected to the source of the initialization transistor T1. (EX1007, [0032], [0035], [0069], Fig. 1.)

363. Liu080 teaches “the initialization voltage line extends in the same direction as the first gate line.” For example, like Liu100, Liu080 teaches a reference signal line RL (“initialization voltage line”) electrically connected to the drain of a common thin film transistor T. Also like Liu100, Liu080 teaches a scan line SL2 (“first gate line”) electrically connected to the gate G1 of a transistor T6. “The common gate electrode G is electrically connected to the first scan line SL1, and the common drain electrode D is electrically connected to the reference signal line RL.” (EX1012, [0024].) The transistor T1 has a drain D1 connected to the source of the common thin transistor T. A POSITA would have understood the common thin film transistor T to be an initialization TFT because it sets the gate potential of transistor T1 to a reference voltage from the reference voltage line RL. Thus, both Liu100 and Liu080 teach similar circuits comprising initialization transistors, initialization voltage lines, and “first gate line[s].” Figure 2 (annotated below) shows Liu080’s circuit comprising the *reference signal line RL* and *scan line SL2*.



364. Liu080 further discloses “an extending direction of the reference signal line RL is parallel to an extending direction of the first scan line SL1 and the second scan line SL2.” (EX1012, [0022].) Figure 5 (annotated below) shows the *reference signal line RL* extending in the same direction as the *scan line SL2*. (See also EX1012, Fig. 1.) Thus, Liu080 teaches claim 20.



a. Motivation to combine Liu100, Ono, and Liu080

365. It would have been obvious to a POSITA at the time of the '483 patent to combine the teachings of Liu100 and Ono with Liu080. Liu100, Ono, and Liu080 relate to OLED devices with transistors that efficiently use the spaces in the device's pixel structure to promote the miniaturization of the OLED devices. Liu100 discloses a pixel structure of an OLED device that is "capable of reducing an area occupied by components of the pixel structure." (EX1007, [0007].) Ono discloses "a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor." (EX1008, [0030].) Liu080 discloses "a pixel structure of an

organic light emitting device, where the pixel structures each can reduce an area occupied by components of the pixel structure.” (EX1012, [0007].) Thus, Liu100, Ono, and Liu080 are in the same field of endeavor and reasonably pertinent to the same technical problem of decreasing the area of the pixel structure, thereby efficiently using the space to make the organic light-emitting devices smaller.

366. Liu080 teaches “the first pixel unit and the second pixel unit of the pixel structure in the invention share the common TFT, a pixel area occupied by the TFTs respectively in the first pixel unit and the second pixel unit of the pixel structure can be reduced. Hence, the area of the pixel structure is reduced for the pixel structure to be applied in high resolution product. The space saved in the pixel structure can also be used for disposing other devices or components when the pixel structure is not to be miniaturized.” (EX1012, [0056].) Liu080’s technical features may be combined with the teachings of Liu100 and Ono with a reasonable expectation of success to generate a smaller light-emitting device by sharing common TFTs among pixel units.

367. Liu100, Ono, and Liu080 relate to OLEDs and have the same objectives of miniaturizing OLED devices. A POSITA would have been motivated to use Liu080’s techniques of sharing common TFTs among pixel units to improve the similar devices of Liu100 and Ono (to reduce the pixel area occupied by the TFTs) in the same way. Further, Liu100 and Liu080 share the

same inventor, and also share many of the same circuit components. For example, the circuits of Liu100 and Liu080 both comprise transistors T1-T6 having similar connections, such as the source of transistor T1 connected to the bottom electrode of the capacitor, the drain of transistor T6 connected to the gate of transistor T4, the source and drain of transistor T3 connected to the drain of transistor T4 and the gate of transistor T4, respectively. (EX1007, [0042], Fig. 1; EX1012, [0029], [0031], [0034], Fig. 2.) Thus, it would have been obvious to combine the references and their teachings.

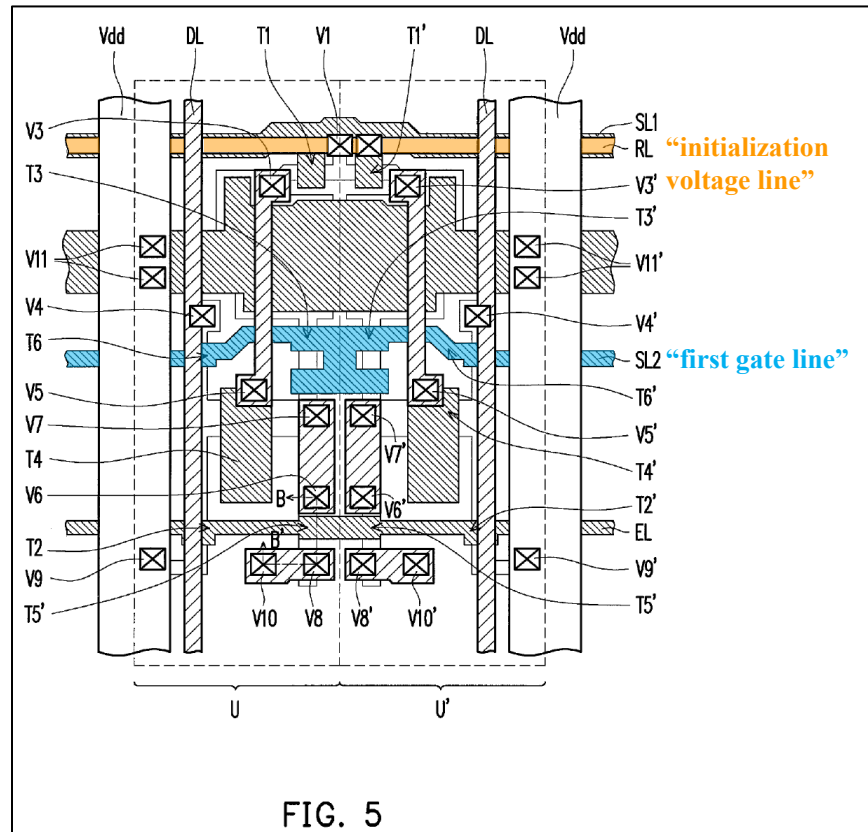
3. Claim 21: “The TFT array substrate of claim 18, wherein the initialization voltage line is formed of a different layer from the first gate line.”

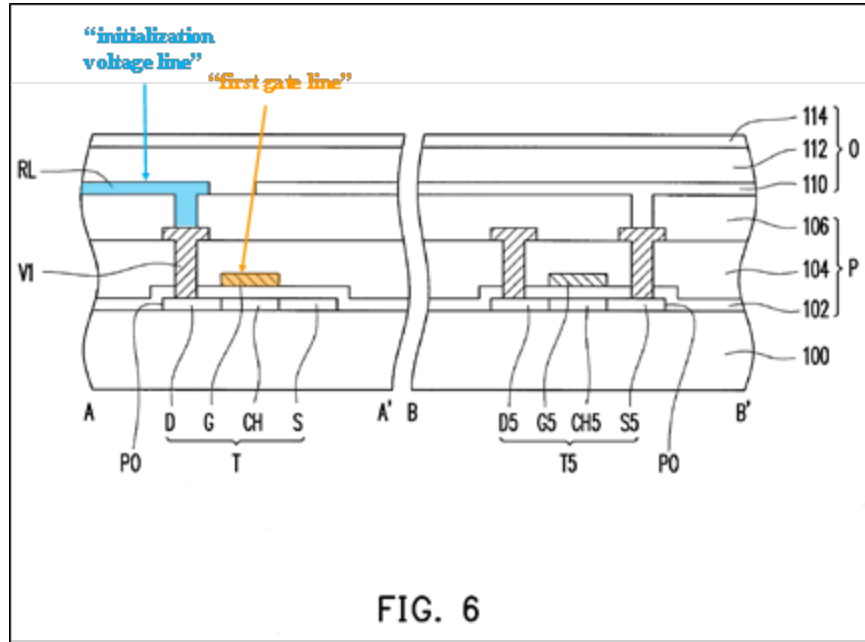
368. As shown for claim 20, Liu080 teaches a reference signal line (“initialization voltage line”) and a scan line SL1 (“first gate line”).

369. Liu080 teaches “the initialization voltage line is formed of a different layer from the first gate line.” For example, Liu080 discloses “since the reference signal line RL and the first electrode layer 110 of the emission device O are disposed in the same layer, the reference signal line RL can be disposed in overlap with the first scan line SL1. In other words, the reference signal line RL is disposed on top of the first scan line SL1. Thus, the space occupied by components or devices in the pixel structure can be further reduced.” (EX1012, [0055].)

Figure 5 (annotated below) shows the *reference signal line RL* disposed on top of

the *scan line SL2*, thereby the reference signal line RL is formed of a different layer from the scan line SL2. Figure 6 (annotated below) shows the reference line RL is formed of a different layer from the scan line SL2. Thus, Liu080 teaches claim 21.





370. It would have been obvious to a POSITA to combine the teachings of Liu100, Ono, and Liu080. (See Section IX.J.2.)

* * *

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: August 31, 2025


Thomas Credelle

Thomas L. Credelle Curriculum Vitae

Professional Summary

Mr. Credelle is a recognized expert in the flat panel/touch industry with over 40 years of expertise in all aspects of flat panel displays, LEDs, LED displays, and optics. He has made significant contributions in the areas of R&D, engineering, marketing, and senior management. He has served at an executive level at start-up businesses within major corporations and start-up companies in Silicon Valley and has had extensive interaction with flat panel producers and customers in Japan, Taiwan, Korea and China. Mr. Credelle holds 84 issued US patents in various flat-panel related technologies including display design, display electronics, materials, algorithms, systems, RFID, and optics, with additional pending.

Mr. Credelle is a Fellow of the Society for Information Display and currently consults regarding technology, business, and patent issues involving Flat Panel Display and LED Technology for various clients. He has written expert-analysis reports for private clients on patent portfolios of over 500 patents and has written numerous IPR ITC, and District Court Case reports and has given depositions on many. He has testified at four District Court cases and three ITC Hearings.

Expertise

- Flat Panel Display Technology
- LEDs and LED lighting
- Display electronics
- Electro-optics
- Patent analysis
- Expert witness (reports, testimony)
- TFT and Liquid Crystal Display R&D

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1970	Massachusetts Institute of Technology	M.S., Electrical Engineering Emphasis: Electro-optics and Solid State Physics Thesis: "Optical Properties of High Purity Stannic Oxide"
1969	Drexel University	B.S., Electrical Engineering (Honors Program)

Thomas L. Credelle Curriculum Vitae

Professional Experience

- From: 2008
To: Present
Organization: **TLC Display Consulting**
Title: President
Summary:
- Technical consulting in the field of flat panel displays, LEDs, and display electronics
 - Business/patent consulting in the fields of displays, LEDs, optics, new technology
- From: 2016
To: 2018
Organization: **RealD**
Title: Acting CEO, RealD Me (2016-2017), Strategic Advisor, RealD 2017-2019)
Summary:
- Business and technical advisor to RealD Intelligent Backlight Business Unit
- From: 2012
To: 2016
Organization: **Innova Dynamics, Inc.**, San Francisco, CA
Title: VP, Application Engineering and Device Performance
Summary:
- Primary interface between customer and product engineering
 - Testing and qualification of all products
 - Business development/technical contact for new opportunities
- From: 2008
To: 2018
Organization: **Display Engineering, Inc.** San Jose, CA
Title: Contractor
Summary:
- Design and testing of high-brightness LED backlights for outdoor signage
 - Circuit design and thermal analysis of LED light bars
 - Developed new methods for passive cooling of LED light sources

Thomas L. Credelle

Curriculum Vitae

From: 2007
To: 2008
Organization: **Puredepth, Inc.**, Redwood City, CA and Auckland, NZ
Title: Senior VP Engineering
Summary:

- Recruited to establish first senior management leadership position for hardware and software engineering related to Puredepth's Multi Layer Display (MLD) technology.
- Rapidly learned details of technology, established new development plans, and supported customer engagements in US, Korea, and Japan.
- Divided time between US and NZ offices, supporting sales/marketing and leading engineering effort.

From: 2001
To: 2007
Organization: **Clairvoyante, Inc.**, Cupertino, CA
Title: VP Engineering
Summary:

- Responsible for engineering, product development, product roadmap, marketing of technology that improves resolution and reduces power of color flat panel displays.
- Responsible for applied R&D, IC development, customer training and support for all technology integration programs.
- Creation of new intellectual property to advance adoption of Clairvoyante technology.
- Monthly interaction with leading LCD producers in Taiwan, Korea, Japan; management of all vendors relating to product development (8-10 on-site visits per year).

From: 1999
To: 2001
Organization: **Alien Technology Corporation**, Morgan Hill, CA
Title: VP of Operations
Summary:

- Key member of management team to develop novel technology for nanoblock-IC assembly using fluidic process. Responsible for facilities, manufacturing operations, IT, and HR; managed \$20M construction project for mfg.
- Key contributor to display-related use of Alien manufacturing processes.
- Contributed to patent portfolio for Alien with key inventions in Nanoblock™ IC manufacturing techniques for displays and RFID tags.

Thomas L. Credelle Curriculum Vitae

From: 1996
To: 1999
Organization: **Motorola**, Flat Panel Display Division, Tempe, AZ
Title: Director, Product Marketing
Summary:

- Responsible for establishing market direction and initial sales approach for new Field Emission Displays (FED) under development within the Division.
- Won potential business for initial small FEDs in industrial and automotive applications.
- Established and managed marketing communications department, creating new brand image for product as well as managing all trade show activities.
- Contributed to product development and spec generation. Generated patent disclosures aimed at solving customer-related issues.

From: 1994
To: 1996
Organization: **Allied Signal**, Los Gatos, CA
Title: Director, Advanced Product Marketing
Summary:

- Responsible for establishing product marketing direction and establishing customer contacts for newly-developed optical films for viewing angle enhancement for LCDs.
- Participated in product development, product improvement based on customer input.

From: 1991
To: 1994
Organization: **Apple Computer**, Cupertino, CA.
Title: Manager, Display Engineering
Summary:

- Responsible for all LCD engineering and qualification for first PowerBook notebook computers introduced to market.
- Extensive interaction with Asian suppliers.
- Generated patent disclosures related to LCD integration in notebook PCs

Thomas L. Credelle Curriculum Vitae

From: 1986
To: 1991
Organization: **GE** R&D Center, Schenectady, NY
Title: Manager, TFT LCD Research and Development
Summary:

- Managed R&D in TFT and LCD technology for avionics applications. Led the team that built the first 1 million pixel color LCD. Led development of various optical devices based on liquid crystal materials.
- Established photonics effort based on liquid crystal technology.

From: 1970
To: 1986
Organization: **RCA** Sarnoff Labs, Princeton, NJ
Title: Individual Contributor, then Group Manager
Summary:

- Increasing levels of responsibility in the R&D of optical materials and flat panel displays.
- Key contributor to novel methods for large screen flat panel TFT.
- Established TFT LCD Program at Sarnoff Labs in 1983.
- Led development of first polySi TFT LCDs at Sarnoff Labs.

Legal Consulting

Expert Engagement:

Type of Matter: Deposition on patent dispute
Client: Alien Technology
Case Name: Alien v. Avery, Case No. 08-cv-00795
Services Provided: Deposed as expert and inventor on behalf of Alien
Date: October 29, 2008

Expert Engagement:

Type of Matter: Patent Infringement, LCD Projection
Client: McKenna Long & Aldridge LLP
Case Name: Undisclosed
Services Provided: Non-testifying expert on ITC case
Date: November 2011

Thomas L. Credelle Curriculum Vitae

Expert Engagement:

Type of Matter: LCD backlight
Client: Steptoe and Johnson LLP on behalf of LG
Case Name: In the Matter of Certain Devices for Improving Uniformity Used in a Backlight Module and Products Containing the Same Inv. No. 337-TA-805
Services Provided: Non-testifying expert on ITC case (settled)
Date: November 2011

Expert Engagement:

Type of Matter: Display driving method for eBooks
Client: Klarquist Sparkman LLP on behalf of Amazon (v. Positive Technologies)
Case Name: 2:11-cv-2226, N.D. Calif.
Services Provided: Expert Reports, Testifying Expert (settled)
Date: October 2012 – April 2013

Expert Engagement:

Type of Matter: Display driving method for eBooks
Client: Alston and Bird LLP on behalf of Barnes and Noble (v. Positive Technologies)
Case Name: 3:11-cv-02226-SI
Services Provided: Testifying expert on District Court Case (settled) Non infringement and non-enablement reports written.
Date: March 2013 – July 2013

Expert Engagement:

Type of Matter: LCD driving method
Client: Kenyon and Kenyon LLP on behalf of Sony (v. Surpass)
Case Name: IPR2015-0863
Services Provided: IPR Reports and Deposition
Date: Jan 2015-Mar 2016

Expert Engagement:

Type of Matter: LCD Optics and TFT design
Client: Marc Labgold on behalf of Funai (v. Gold Charm Ltd.)
Case Name: IPR2015-01448
Services Provided: IPR Report
Date: Apr, 2015 – Jul, 2015

Expert Engagement:

Type of Matter: LCD Backlights using LEDs
Client: Shearman & Sterling LLP/Fried Frank LLP on behalf of Mercedes Benz (v. Innovative Display Technologies)
Case Name: IPR2015-01995, IPR2015-01115, IPR2015-01113 and 2: 14-cv-00535 TXEDC
Services Provided: IPR Expert Reports
Date: Mar 2015 – May 2015

Thomas L. Credelle Curriculum Vitae

Expert Engagement:

Type of Matter: TFT array and LCD panel interconnect
Client: Covington & Burling on behalf of Samsung Display Co. (v. MiiC & Partners)
Case Name: IPR205-01469, IPR2015-01499
Services provided: IPR Expert Reports
Date: May 2015- Mar 2016

Expert Engagement:

Type of Matter: LCD Backlights using LEDs
Client: Mayer Brown on behalf of KJ Pretech (v. Innovative Display Technologies)
Case Name: IPR2015-01866, IPR2015-01867, IPR2015-01868
Services Provided: IPR reports and depositions (3)
Date: Aug 2015-Jun 2016

Expert Engagement:

Type of Matter: LCD backlights using LEDs
Client: Gibson, Dunn, and Crutcher LLP on behalf of Vizio (v. Delaware Display Group LLC)
Case Name: Case No. 13-cv-2112
Services Provided: Non-infringement Report, Deposition, Testifying Expert (settled)
Date: Sep 2015-Mar 2017

Expert Engagement:

Type of Matter: LCD manufacturing, TFT array design
Client: Sughrue Mion PLLC on behalf of TCL
Case Name: Arbitration (Hong Kong) between AUO and TCL
Services Provided: Non-infringement analysis of TFT array design (settled)
Date: Jun 2017 – Sep 2017

Expert Engagement:

Type of Matter: LED display panels
Client: Adduci Mastriani & Schaumberg on behalf of Ultravision Technologies LLC (v. >20 Chinese companies)
Case Name: ITC Case 337-TA-1114
Services Provided: Expert Reports (Invalidity and Non-infringement) and Deposition (3 days)
Date: Jan 2018 – Feb, 2019

Expert Engagement:

Type of Matter: LCD gamma circuit
Client: K&L Gates on behalf of Wistron (v. plaintiff Phenix Longhorn)
Case Name: IPR2018-01255, 2:17 cv-00711 TXEDC
Services Provided: Expert report and Expert Testimony as needed (settled)
Date: May 2018 – Jun 2019

Thomas L. Credelle Curriculum Vitae

Expert Engagement:

Type of Matter: LED packaging
Client: Davidson, Berquist, Jackson & Gowdey, LLP on behalf of Document Security Systems (v. defendants Seoul Semiconductor, Nichia Corp, Cree, Inc., Everlight Electronics)
Case Name: IPR2018-00966, 2018-01165
Services Provided: Expert Reports, Depositions (2) and Expert Testimony at trial as needed
Date: June 2018 – May 2019

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: Vinson and Elkins on behalf of AUO (v. plaintiff Vista Park Ventures)
Case Name: 2:18 cv-00276, 00278, 00279 TXEDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Dec 2018 – Sep 2019

Expert Engagement:

Type of Matter: LED Display Panels
Client: Fabricant LLP on behalf of Plaintiff Ultravision (v. >10 companies)
Case Name: 2:18 cv-00112, 00118, 00150 TXEDC
Services Provided: Expert report and Expert Testimony as needed; two days deposition in 2020, two depositions in 2021. **Testified at trial May 2021**
Date: Jan 2019 – Present

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: McDermott, Will and Emery on behalf of TCL (v. plaintiff Vista Park Ventures)
Case Name: 2:19 cv-00188, 00189, 00190, 00191 TXEDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Aug 2019 – Oct 2019

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: McDermott, Will and Emery on behalf of GiantPlus (v. plaintiff Vista Park Ventures)
Case Name: 2:19 cv-00183, 00184, 00185, 00187 TXEDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Oct 2019 – Jan, 2020

Expert Engagement:

Thomas L. Credelle Curriculum Vitae

Type of Matter: TFT-LCD technology
Client: Vincent and Elkins on behalf of JDI (v. plaintiff Vista Park Ventures)
Case Name: 2:19 cv-00323, 00324, 00325 TXEDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Nov 2019 – Jun 2020

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: Sidley on behalf of LG Electronics (v. defendant Hisense)
Case Name: 2:19 cv-09474 CACDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Feb. 2020 – Jan. 2021

Expert Engagement:

Type of Matter: Quantum dot technology
Client: Murtha Law on behalf of RPI (v. defendant Samsung)
Case Name: 2:19 cv-20097 KM-ESK
Services Provided: Expert reports and Expert Testimony as needed
Date: Jan. 2020 – Jun 2021

Expert Engagement:

Type of Matter: OLED, touch panels
Client: RAK Law on behalf of Solas (v. defendant Samsung)
Case Name: 2:19-cv-00152-JRG (E.D. Tex)
Services Provided: Expert reports and Expert Testimony; two depositions in 2020.
Testified at trial Mar. 2021.
Date: Apr. 2020 – Mar. 2021

Expert Engagement:

Type of Matter: LCD technology
Client: Morgan Lewis on behalf of Fuji Film (v. plaintiff Vista Park Ventures)
Case Name: 2:20 cv-00064, 65, 66 E.D. Tex.
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Jul. 2020 – Oct 2020

Expert Engagement:

Type of Matter: Touch panels
Client: DLA Piper, Alston and Bird, on behalf of Microsoft, Dell (v. plaintiff Neodron)
Case Name: 2:19-cv-00318-ADA (W.D. Tex)
Services Provided: Expert Reports and Expert Testimony as needed (settled)
Date: Aug. 2020 – Nov. 2020

Thomas L. Credelle Curriculum Vitae

Expert Engagement:

Type of Matter: LCD
Client: Vincent and Elkins on behalf of Japan Display Inc (v. defendant Tianma)
Case Name: 2:20-CV-00283, 284, 285-JRG (E.D. Tex)
Services Provided: Expert Reports, depositions, and Expert Testimony as needed (settled)
Date: Jan 2021 – Jan 2022

Expert Engagement:

Type of Matter: LCD
Client: Perkins Coie on behalf of Truly Semiconductor, Hannstar (v. plaintiff Vista Park Ventures)
Case Name: 2:20-CV-250, 251, 252 (E.D. Tex)
Services Provided: Expert Reports and Expert Testimony as needed (settled)
Date: Jan 2021 – June 2021

Expert Engagement:

Type of Matter: Quantum dots
Client: Mintz on behalf of Nanoco (v. defendant Samsung)
Case Name: 2:20-CV-00038-JRG (E.D. Tex)
Services Provided: Expert Reports, depositions, case settled day before trial opening arguments
Date: Jan 2021 – Jan 2023

Expert Engagement:

Type of Matter: OLED circuits
Client: Morrison Forster on behalf of JOLED (v. defendant Samsung)
Case Name: Case No. 6:20cv559 (W.D. Tex.)
Services Provided: Expert Reports and Expert Testimony (settled)
Date: July 2020 – April 2021

Expert Engagement:

Type of Matter: OLED circuits
Client: Perkins Coie on behalf of AUO (v. defendant Samsung)
Case Name: TBD
Services Provided: Expert Reports and Testimony (settled)
Date: Feb. 2021 – May 2021

Expert Engagement:

Type of Matter: LED circuits
Client: Kim IP on behalf of CAST Lighting (v. Plaintiff WAC Lighting)
Case Name: ITC Inv. No. 337-TA-1261
Services Provided: Expert Reports and Testimony (settled)
Date: May 2021 – Oct 2021

Thomas L. Credelle Curriculum Vitae

Expert Engagement:

Type of Matter: OLED circuits
Client: RAKLaw on behalf of Solas, Ltd. (v. Defendant Samsung)
Case Name: ITC Inv. No. 337-TA-1243
Services Provided: Expert Reports and **Testified at Hearing Nov. 15-19, 2021**
Date: May 2021 – Dec 2021

Expert Engagement:

Type of Matter: OLED circuits
Client: PV Law on behalf of TCL (vs. Plaintiff SEL Co.)
Case Name: 8:21-cv-00554-JAK-ADS (CDCA)
Services Provided: Expert Reports and Depositions; case settled
Date: July 2021 – July 2023

Expert Engagement:

Type of Matter: LED circuits
Client: Carmichael IP on behalf of Lynk Labs (vs. defendant Samsung)
Case Name: IPR Proceedings
Services Provided: Expert Reports and Depositions, case settled.
Date: Jan 2022 – Jan 2023

Expert Engagement:

Type of Matter: OLED circuits
Client: Baker Botts on behalf of FujiFilm (vs. defendant ButterflyQ)
Case Name: C.A. No. 22-309-JPM
Services Provided: Expert Reports and Depositions, testify at trial if needed (settled Nov, 2023)
Date: Jul 2022 – Nov. 2023

Expert Engagement:

Type of Matter: Outdoor LCD signage
Client: Kilpatrick Townsend on behalf of MRI, Inc. (vs. defendants Samsung et al)
Case Name: ITC 337-TA-1331
Services Provided: Expert Reports, Depositions, **Testified at Hearing June 26-30, 2023**
Date: Oct 2022 – Aug 2023

Expert Engagement:

Type of Matter: OLED circuits and pixel arrangements
Client: Orrick Herrington & Sutcliffe LLP on behalf of BOE (vs. plaintiff Samsung et al)
Case Name: ITC 337-TA-1351
Services Provided: Expert Reports, Depositions. **Testified at Hearing July 16, 2024**
Date: Sep 2023 – Sept 2024

Thomas L. Credelle Curriculum Vitae

Expert Engagement:

Type of Matter: Light concentrators, LCD backlights
Client: Katz PLLC on behalf of SVV (vs. defendants Asus and Acer)
Case Name: WD Tex 6:22-cv-0311, 312, 313, 511, 512, 513, 639, 640, 641-ADA
Services Provided: Expert Reports, Depositions, **testified at trial (v. Acer), June, 2024; testified at trial (v. ASUS), Sept, 2024**
Date: Jan 2023- Oct 2024 (Plaintiff won in both trials)

Expert Engagement:

Type of Matter: LCD AMOLED circuits,
Client: Kramer Alberti on behalf of Polaris PowerLED Technologies, LLC (vs. defendant Samsung et al)
Case Name: EDTEX 2:22-cv-00469-JRG
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert (trial scheduled for Jan 2025)
Date: Mar 2023- Dec 2024 (settled)

Expert Engagement:

Type of Matter: LCD AMOLED circuits,
Client: Morrison & Forester LLP on behalf of Crystal Leap (vs. defendant HKC)
Case Name: No. 2:22-cv-00382 (EDTEX)
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert, settled Mar, 2024
Date: Jul 2023- Mar 2024 (settled)

Expert Engagement:

Type of Matter: LCD AMOLED circuits,
Client: Kramer Alberti on behalf of Polaris PowerLED Technologies, LLC (vs. various defendants)
Case Name: 2:23-cv-03478-GW-PD (CD CAL)
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert
Date: Dec 2023- present

Expert Engagement:

Type of Matter: Image sensor circuits,
Client: PVLaw on behalf of Keyence (vs. plaintiff AI Core Technologies, LLC)
Case Name: 2:24-cv-00438-RWS-RSP,
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert
Date: Dec 2023- Nov 2024 (settled)

Thomas L. Credelle Curriculum Vitae

Expert Engagement:

Type of Matter: AMOLED design, circuits
Client: Morrison & Forester LLP on behalf of BOE (vs. Plaintiff SDC)
Case Name: No. 2:25-cv-00430 (E.D. Tex.), *Samsung Display Co., Ltd. v. BOE Technology Group Co., Ltd. et al.*, No. 2:23-cv-00426 (E.D. Tex.)
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert
Date: Jun 2025 - present

Expert Engagement:

Type of Matter: AMOLED design, circuits
Client: Orrick on behalf of BOE
Case Name: Not yet assigned
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert
Date: May 2025 - present

Consulting Projects

Consulting Engagement:

Client: Tessera
Services Provided: Business case analysis for M&A department
Date: Mar 2008 to 2011

Consulting Engagement:

Client: Sipix Imaging
Services Provided: Technical consulting on display algorithms
Date: Mar 2008 to 2009

Consulting Engagement:

Client: Holox Technologies, Inc. (self-funded start up in holographic optics)
Services Provided: CEO; business leadership, fund raising, market analysis, optical design of advanced diffusers for LCD backlights, solar collectors, window films.
Date: Sept 2008 to June 2012

Consulting Engagement:

Client: Innova Dynamics, Inc.
Services Provided: Technical and business development consulting in touch screen technology
Date: October 2011 to November 2012

Technical and Patent Consulting:

Client: LG Display
Services Provided: Technical consulting on pixel processing algorithms, OLED displays; patent generation for advanced pixel concepts for OLED.

Thomas L. Credelle
Curriculum Vitae

Date: Aug 2009 to Dec 2011

Consulting Engagement:

Client: Scivax

Services Provided: Technical and business development consulting in nanoimprinting technology

Date: Feb 2018 to Jul 2018

Thomas L. Credelle Curriculum Vitae

Professional Affiliations, Achievements & Awards

- Fellow of the Society for Information Display (SID)
- Past Director, SID Symposium Committee (10 years)
- Conference and Program Chair, SID Symposium and IDRC
- Past Member, SID Program Committee (15 years)

US Patents & Publications

<u>Patent</u>	<u>Date</u>	<u>Description</u>
10,163,985	12/25/2018	Subpixel arrangement structure for a display device
9,583,034	02/28/2017	Subpixel arrangement structure for a display device
9,041,625	05/26/2015	Subpixel arrangement structure for a display device and display device
9,001,167	04/07/2015	Display panel having crossover connections effecting dot inversion
8,933,959	01/13/2015	Subpixel layouts and subpixel rendering methods for directional displays and systems
8,876,937	11/04/2014	Production of nanostructures
8,797,344	08/05/2015	Memory structures for image processing
8,754,913	06/17/2014	Subpixel arrangement structure of display device
8,704,744	04/22/2014	Systems and methods for temporal subpixel rendering of image data
8,633,886	01/21/2014	Display panel having crossover connections effecting dot inversion
8,519,910	08/27/2013	Image processing method and display device using the same
8,516,683	08/27/2013	Methods of making a radio frequency identification (RFID) tags
8,456,496	06/04/2013	Color flat panel display sub-pixel arrangements and layouts for sub-pixel rendering with split blue sub-pixels
8,456,414	06/04/2013	Gamma adjustment with error diffusion for electrophoretic displays
8,436,799	05/07/2013	Image degradation correction in novel liquid crystal displays with split blue subpixels
8,421,820	04/16/2013	Methods and systems for sub-pixel rendering with adaptive filtering
8,411,022	04/02/2013	Multiprimary color display with dynamic gamut mapping
8,405,692	03/26/2013	Color flat panel display arrangements and layouts with reduced blue luminance well visibility
8,378,947	02/19/2013	Systems and methods for temporal subpixel rendering of image data
8,294,741	10/23/2012	Four color arrangements of emitters for subpixel rendering
8,259,127	09/04/2012	Systems and methods for reducing desaturation of images rendered on high brightness displays
8,144,094	03/27/2012	Liquid crystal display backplane layouts and addressing for non-standard subpixel arrangements

Thomas L. Credelle Curriculum Vitae

8,134,583	03/13/2012	Two color flat panel display sub-pixel arrangements and layouts for sub-pixel rendering with split blue sub-pixels
8,035,599	10/11/2011	Display panel having crossover connections effecting dot inversion
8,018,476	09/13/2011	Subpixel layouts for high brightness displays and systems
8,013,867	09/06/2011	Systems and methods for implementing improved gamut mapping algorithms
7,969,456	06/28/2011	Methods and systems for sub-pixel rendering with adaptive filtering
7,876,341	06/25/2011	Subpixel layouts for high brightness displays and systems
7,864,194	01/04/2011	Systems and methods for motion adaptive filtering
7,791,679	09/07/2010	Alternative thin film transistors for liquid crystal displays
7,755,652	07/13/2010	Color flat panel display sub-pixel rendering and driver configuration for sub-pixel arrangements with split sub-pixels
7,701,476	04/20/2010	Four color arrangements of emitters for subpixel rendering
7,646,430	01/12/2010	Display system having improved multiple modes for displaying image data from multiple input source formats
7,592,996	09/22/2009	Multiprimary color display with dynamic gamut mapping
7,583,279	09/01/2009	Subpixel layouts and arrangements for high brightness displays
7,573,493	08/11/2009	Four color arrangements of emitters for subpixel rendering
7,573,448	08/11/2009	Dot inversion on novel display panel layouts with extra drivers
7,559,131	07/14/2009	Method of making a radio frequency identification (RFID) tag
7,505,053	03/17/2009	Subpixel layouts and arrangements for high brightness displays
7,492,379	02/17/2009	Color flat panel display sub-pixel arrangements and layouts for sub-pixel rendering with increased modulation transfer function response
7,417,648	08/26/2008	Color flat panel display sub-pixel arrangements and layouts for sub-pixel rendering with split blue sub-pixels
7,397,455	07/08/2008	Liquid crystal display backplane layouts and addressing for non-standard subpixel arrangements
7,283,142	10/16/2007	Color display having horizontal sub-pixel arrangements and layouts
7,260,882	08/28/2007	Methods for making electronic devices with small functional elements supported on a carriers
7,248,271	07/24/2007	Sub-pixel rendering system and method for improved display viewing angles
7,218,301	05/15/2007	System and method of performing dot inversion with standard drivers and backplane on novel display panel layouts
7,187,353	03/06/2007	Dot inversion on novel display panel layouts with extra drivers
7,184,066	02/27/2007	Methods and systems for sub-pixel rendering with adaptive filtering
7,167,186	01/23/2007	Systems and methods for motion adaptive filtering
7,084,923	08/01/2006	Display system having improved multiple modes for displaying image data from multiple input source formats
7,068,287	06/27/2006	Systems and methods of subpixel rendering implemented on display panels
7,046,256	05/16/2006	System and methods of subpixel rendering implemented on display panels
6,985,361	01/10/2006	Electronic devices with small functional elements supported on a carrier
6,917,368	07/12/2005	Sub-pixel rendering system and method for improved display viewing angles

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6,816,380	11/09/2004	Electronic devices with small functional elements supported on a carrier
6,731,353	05/04/2004	Method and apparatus for transferring blocks
6,693,384	02/17/2004	Interconnect structure for electronic devices
6,606,247	08/12/2003	Multi-feature-size electronic structures
5,961,362	10/05/1999	Method for in situ cleaning of electron emitters in a field emission device
5,883,467	03/16/1999	Field emission device having means for in situ feeding of hydrogen
5,477,350	12/19/1995	Interferometric spatial switch for polarized or unpolarized light using liquid crystal
5,373,393	12/13/1994	Optical interferometric device with spatial light modulators for switching substantially coherent light
5,363,228	11/08/1994	Optical device with spatial light modulators for switching arbitrarily polarized light
5,345,321	09/06/1994	Compact polarization dependent optical switching units
5,319,477	06/07/1994	Compact polarization independent optical switching units
5,317,445	05/31/1994	Optical device with spatial light modulators for switching polarized light
4,630,893	12/23/1986	LCD pixel incorporating segmented back-to-back diode
4,598,227	07/01/1986	Electron beam convergence and scanning structures for flat panel display device
4,517,489	05/14/1985	Modulator structure and method for flat panel display devices
4,484,103	11/20/1984	Color selection electron beam guide assembly for flat panel display devices
4,362,966	12/07/1982	Electron leakage reduction in flat panel display devices
4,335,332	06/15/1982	Focus mesh structure and biasing technique for flat panel display devices
4,316,118	02/16/1982	Guided beam display device
4,298,819	11/03/1981	Beam Clean up structure for flat panel display devices
4,234,815	11/18/1980	Flat display tube having shielding member between beam guide and screen
4,174,881	11/20/1979	Recording a synthetic focused-image hologram on a thermally deformable plastic
4,153,856	05/08/1979	Proximity focused element scale image display device
4,148,636	04/10/1979	Broadening the spatial frequency pass band of a thermoplastic layer
4,137,478	01/30/1979	Color flat panel television
4,137,077	01/30/1979	Broadening the spatial frequency pass band of a thermoplastic layer
4,131,823	12/26/1978	Modular flat display device with beam convergence
4,121,137	10/17/1978	System for achieving image uniformity in display devices
4,103,205	07/25/1978	Flat display device with beam guide
4,103,204	07/25/1978	Flat display device with beam guide
4,088,920	05/09/1978	Flat display device with beam guide

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Publications

1. "Thermoplastic Media for Holographic Recording," RCA Review: A Technical Journal (1972)
2. "Guided Beam Displays for Large Screen Flat-Panel Color TV," Information Display (1983)
3. "Recent trends in color avionic LCDs," Information Display (1987)
4. "Thin-film transistors for video applications," Inter. Display Research Conference Record (1988)
5. "TFT-LCD for video applications," Information Display (1989)
6. "LCDs," JTEC Panel Report on Display Technologies in Japan (1992)
7. "Viewing-Angle-Enhancement System for LCDs" SID Digest of Technical Papers (1995)
8. "SpectraVue™: A new system to enhance the viewing angle of LCDs," SID Journal (1997)
9. "The Business Case for Motorola's Flat-Panel-Display Division," Information Display (1997)
10. "MTF of high-resolution PenTile Matrix™ displays," Proc Eurodisplay (2002)
11. "Adding a White Subpixel," Information Display (2005)
12. "Low Power, High-Pixel-Density Mobile Displays Using PenTile RGBW™ Architectures," SID Mobile Displays Digest of Technical Papers (2006)
13. *"Invited Paper: High-Pixel-Density Mobile Displays: Challenges and Solutions,"* SID Digest of Technical Papers (2006)