

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Patent No. 10,720,483

Inter Partes Review No. IPR2025-01498

**PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §§ 311-319
AND 37 C.F.R. § 42.100 *et seq.***

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U.S. Patent No. 10,720,483	1001
Expert Declaration of Mr. Thomas Credelle	1002
Prosecution History of U.S. Patent No. 10,720,483	1003
U.S. Publication No. 2007/0058100 to Ishii	1004
U.S. Publication No. 2003/0141811 to Park	1005
U.S. Publication No. 2002/0118150 to Kwon	1006
U.S. Publication No. 2012/0313100 to Liu	1007
U.S. Publication No. 2011/0128211 to Ono	1008
U.S. Patent No. 6,674,245 to Ko	1009
U.S. Publication No. 2004/0012028 to Park et al.	1010
U.S. Publication No. 2011/0297941 to Zhan et al.	1011
U.S. Publication No. 2012/0007080 to Liu	1012
U.S. Patent No. 8,664,662 to Ono et al.	1013
U.S. Publication No. 2003/0222589 to Osame	1014
U.S. Publication No. 2012/0211750 to Kakinuma	1015

Petitioner BOE Technology Group Co., Ltd., (“Petitioner” or “BOE”) respectfully petitions for *inter partes* review of claims 1-29 of U.S. Patent No. 10,720,483 (“the ’483 patent” (EX1001)) in accordance with 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq.*

I. INTRODUCTION

The ’483 patent is directed to a TFT array substrate comprising transistors and a capacitor including lower and upper electrodes overlapping the gate of a transistor. This overlap accounts for an overlay deviation between the capacitor electrodes due to misalignment between masks during fabrication. (EX1001, 1:35-40.) If not accounted for, the actual capacitance differs from the target capacitance, causing “low-gradation spots, abnormal colors, or the like.” (EX1001, 1:40-45.)

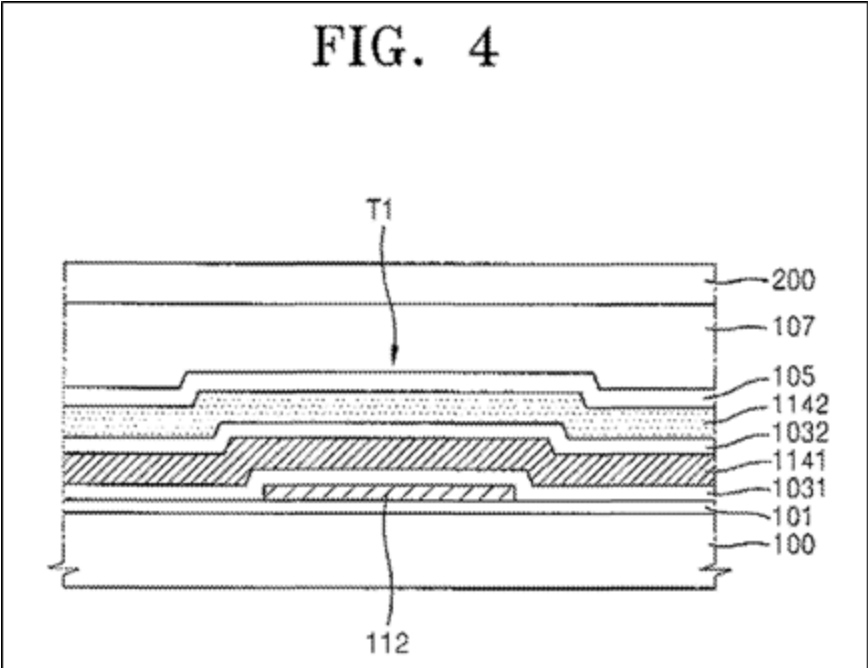
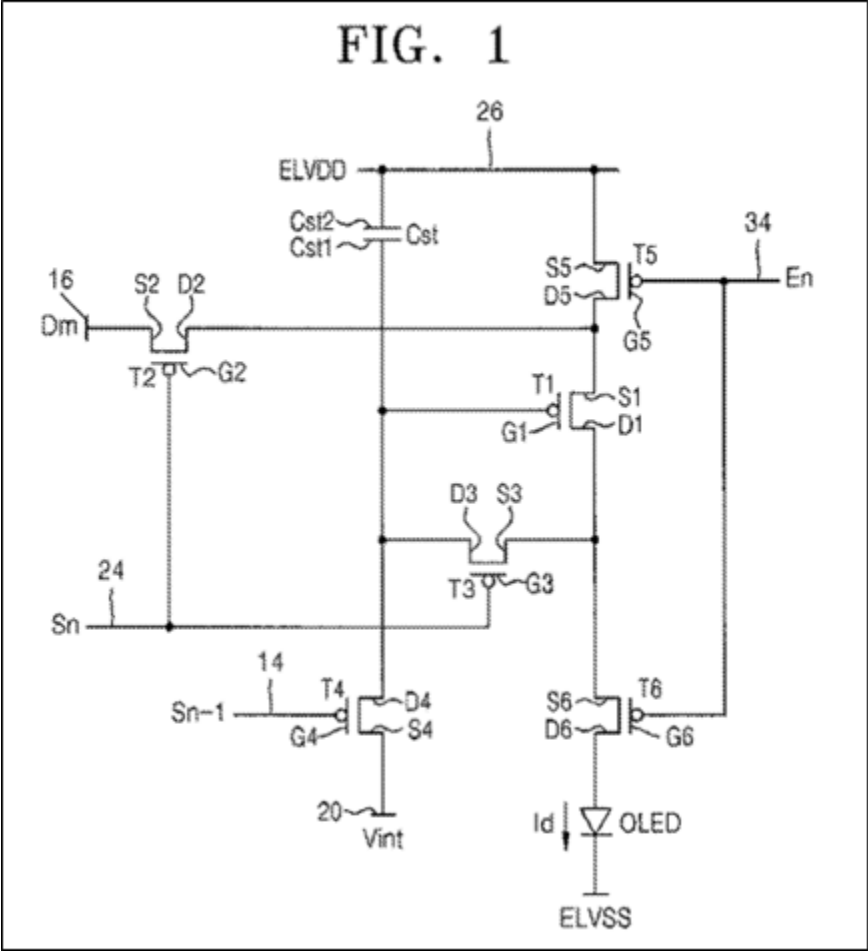
Display devices having overlay deviation issues and display devices having transistors and capacitors with electrodes overlapping the gate of a transistor were known before the ’483. Park and Ono each discloses display devices comprising transistors and capacitors with an electrode overlapping a gate. For example, Ono’s driving transistor and capacitor overlap each other, and the gate electrode of a transistor is one of the capacitor electrodes.

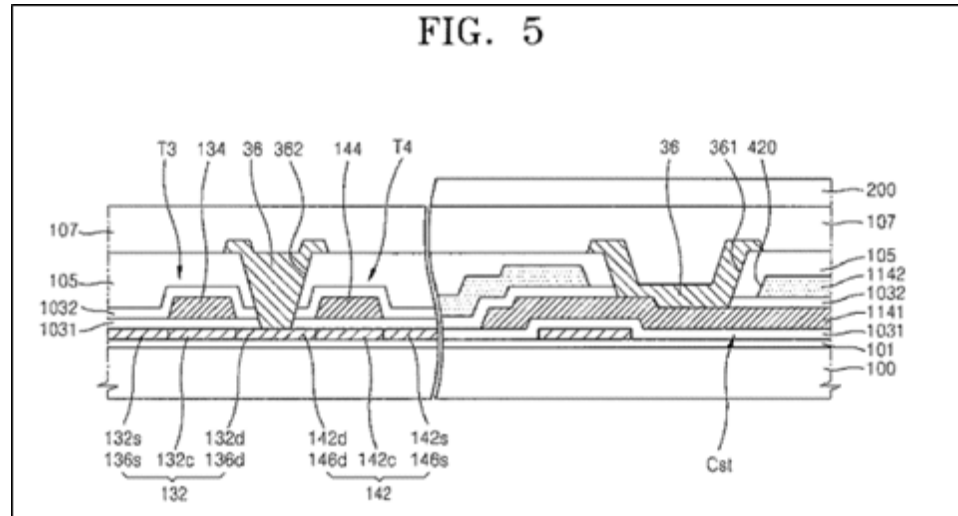
Petitioner submits the challenged claims are unpatentable for the reasons set forth in this Petition, as supported by Mr. Thomas Credelle (EX1002).

II. SUMMARY OF THE '483 PATENT

The '483 discloses “a thin film transistor (TFT) array substrate including at least one TFT and one storage capacitor, and an organic light-emitted (OLED) display.” (EX1001, 1:21–24.) The OLED display allegedly solves problems faced during manufacturing, including misalignment between masks (overlay deviation). (EX1001, 1:38–51.) The overlay deviation generates an actual capacitance different from the target capacitance, resulting in “low-gradation spots, abnormal colors, or the like.” (EX1001, 1:48–51.) The '483's OLED display therefore “includ[es] a storage capacitor structure for maintaining a capacitance to be substantially constant even though an overlay deviation occurs.” (EX1001, 1:56–60; EX1001, 1:42–51; EX1002, ¶¶19-20.)

Figures 1, 4, and 5 (below) show a pixel circuit and cross-sectional views of the OLED display. The circuit includes a driving TFT T1, a switching TFT T2, and an initialization TFT T4. (EX1001, 4:22–25.) The OLED display device includes a storage capacitor Cst comprising a lower electrode 1141 and an upper electrode 114. (EX1001, 4:14–19, 7:8–10; EX1002, ¶¶21-23.)





A. Effective Filing Date

The '483 is a continuation of Application Nos. 15/064,526 (U.S. Patent No. 9,768,241) and 13/801,937 (U.S. Patent No. 9,299,730) and has the following dates:

Filing	September 18, 2017
Published	January 4, 2018
Issued	July 21, 2020
Priority	September 19, 2012 ¹

(EX1002, ¶18.)

B. Prosecution History

During prosecution, the Examiner only issued rejections based on a Restriction Requirement and § 112. (EX1003, 48–51.) In the February 21, 2019

¹ For purposes of this Petition only, Petitioner relies on the priority date as the earliest effective filing date.

Restriction Requirement, the Examiner required election among claims drawn to a TFT array substrate and claims drawn to a display device, to which Applicant elected the TFT array substrate claims. (EX1003, 58, 96–98; EX1002, ¶24.)

In the October 17, 2019 Non-Final Office Action, the Examiner rejected claims 1-21 for failure to comply with the written description requirement. (EX1003, 50.) In response, Applicant implemented the Examiner’s suggested amendments. (EX1003, 31–47.) Applicant also added claims 41-48 (later issued as claims 22-29 of the ’483). (EX1002, ¶¶25-26.)

Without stating the reasons for the allowance, on March 10, 2020, the Examiner issued a Notice of Allowance. (EX1003, 20–25; EX1002, ¶27.)

C. Level Of Ordinary Skill In The Art

A person of ordinary skill in the art (“POSITA”) in the field of the ’483 patent would have bachelor’s degree in electrical engineering or materials science, including OLED displays, or an equivalent level of skill, knowledge, and experience. This POSITA would have been aware of and generally knowledgeable about OLED materials, and display pixel design, layout, and operation. (EX1002, ¶¶33-35.)

III. CLAIM CONSTRUCTION

For purposes of this petition only, Petitioner does not believe any terms require a formal construction. Each of the terms carries its “ordinary and

customary meaning.” *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (citation omitted); (EX1002, ¶¶36-37.)

IV. PRECISE REASONS FOR RELIEF REQUESTED

Pursuant to 37 C.F.R. § 42.104(b), Petitioner requests cancellation of the challenged claims based on the following references (EX1002, ¶¶38-46):

Prior Art	Abbreviation	Date	Prior Art Under §
U.S. 2003/0141811	Park (EX1005)	July 31, 2003 (published)	102(b)
U.S. 2011/0297941	Zhan (EX1011)	December 8, 2011 (published)	102(b)
U.S. 2003/0222589	Osame (EX1014)	December 4, 2003 (published)	102(b)
U.S. 6,674,245	Ko (EX1009)	July 3, 2003 (published)	102(b)
U.S. 2002/0118150	Kwon (EX1006)	August 29, 2002 (published)	102(b)
U.S. 2012/0313100	Liu100 (EX1007)	February 2, 2012 (filed)	102(e)
U.S. 2011/0128211	Ono (EX1008)	June 2, 2011 (published)	102(b)
U.S. 2012/0007080	Liu080 (EX1012)	January 12, 2012 (published)	102(a)

The statutory grounds (pre-AIA) for the challenge of each claim are:

Ground	35 U.S.C. §	Claim(s)	Prior Art Reference(s)
1	103	1, 11, 14, 15	Park
2	103	2-6, 22-24, 27	Park, Zhan
3	103	7-10	Park, Osame
4	103	25, 26	Park, Zhan, Osame
5	103	12, 13	Park, Ko
6	103	28, 29	Park, Zhan, Ko
7	103	17-20	Park, Kwon
8	103	1-4, 12-19, 22-24, 28, 29	Liu100, Ono
9	103	7-10, 25, 26	Liu100, Ono, Osame
10	103	20, 21	Liu100, Ono, Liu080

Below, Petitioner discusses why the challenged claims are unpatentable under the statutory grounds raised, including how and where the prior art satisfies each element of each challenged claim, as required by 37 C.F.R. § 42.104(b)(4). Petitioner's showing establishes a reasonable likelihood it will prevail on each ground of unpatentability to each challenged claim.

V. GROUND 1: PARK RENDERS OBVIOUS CLAIMS 1, 11, 14, AND 15

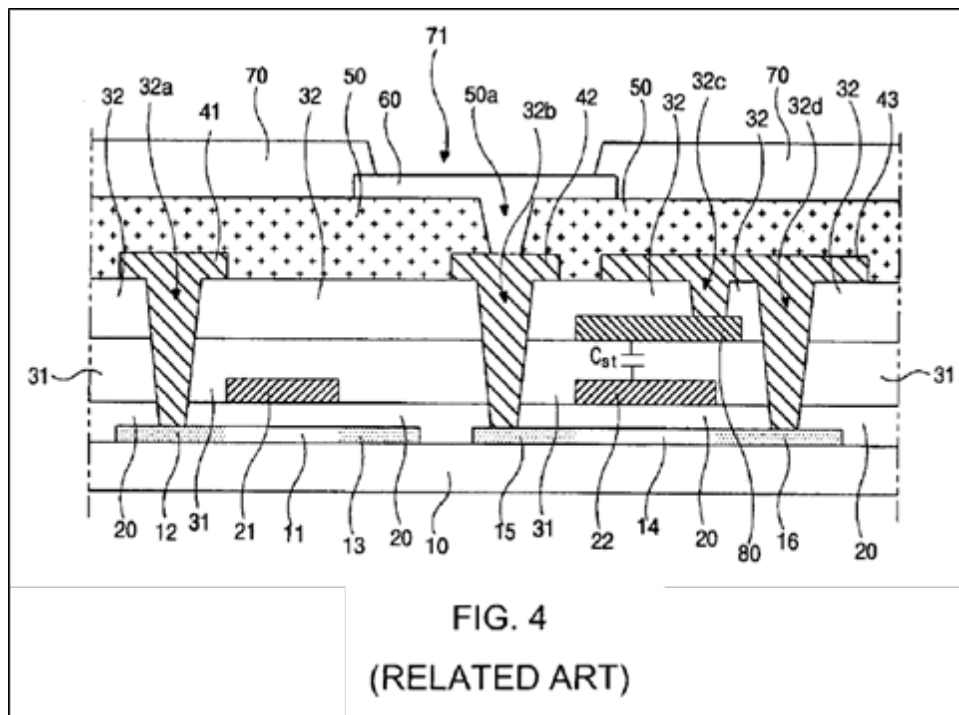
A. Summary Of Park

Park discloses an active matrix electro luminescence display (ELD) device. (EX1005, [0003].) A pixel has a switching transistor 4, a driving transistor 5, a

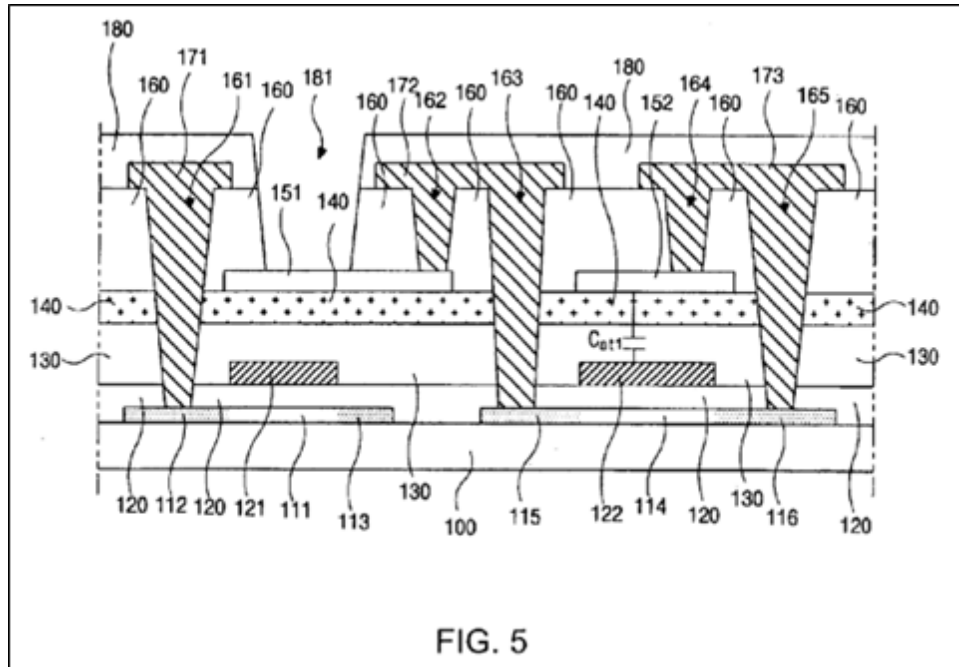
storage capacitor 6 and a light emitting diode (LED) 7. (EX1005, [0006]; EX1002, ¶¶47-48.)

Park explains it is desirable to increase the storage capacitance by increasing the area of the electrodes and/or decreasing the thickness of the dielectric between the electrodes, but doing so may “decrease of an area of the pixel electrode [], and thus an aperture ratio is decreased.” (EX1005, [0015]; EX1002, ¶48.)

Park’s display device (Figure 4 (below)) overcomes these problems by including a “capacitor electrode 80 that overlapped with the second gate electrode 22 [that] is formed on the first inter layer 31. A second inter layer 32 is formed on the capacitor electrode 80.” (EX1005, [0015].) “[T]hus the storage capacitance of the storage capacitor can be increased.” (*Id.*; EX1002, ¶¶49-51.)



Park discloses (Figure 5 (below)) an active matrix organic ELD device with increased storage capacitor without reducing the aperture ratio, and reduced manufacturing time and costs. (EX1005, [0017], [0007], [0034]; EX1002, ¶¶50-51.)



B. Claim 1

1. Preamble: “A thin film transistor (TFT) array substrate comprising:”

To the extent the preamble is limiting (which Petitioner does not concede), Park discloses the preamble.

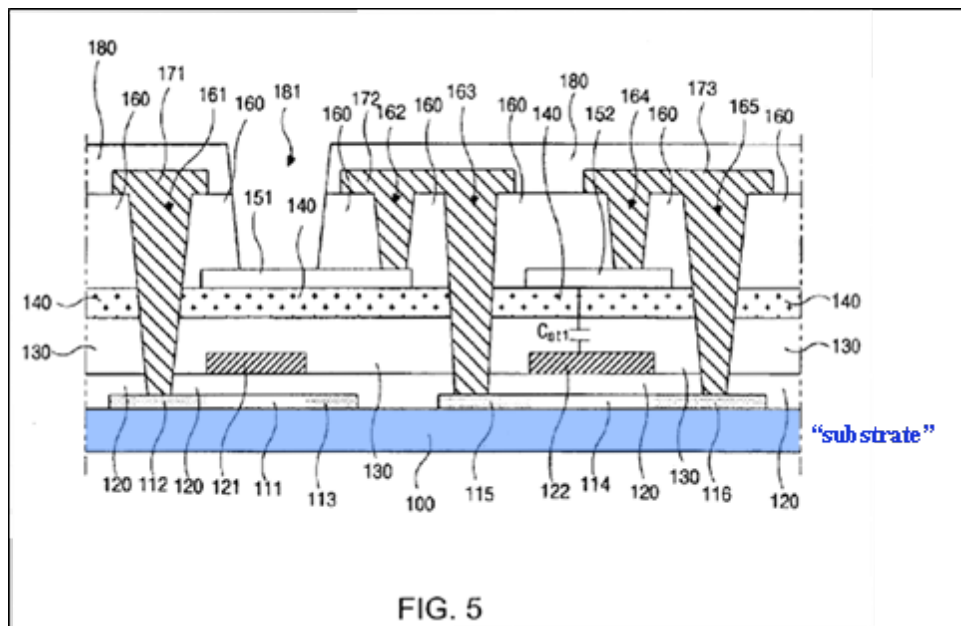
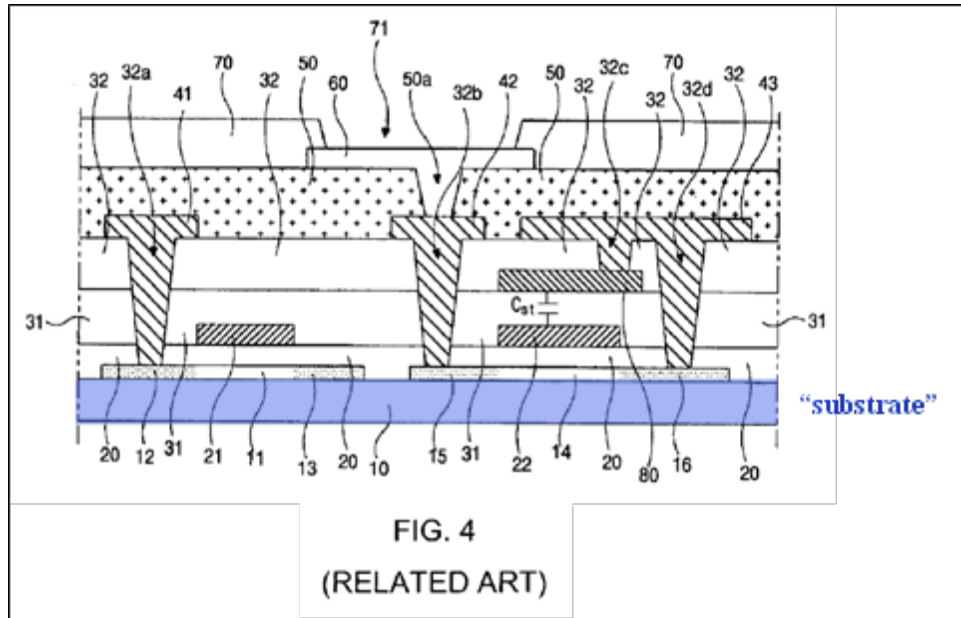
Park's device comprises TFTs part of "an *array substrate* of the active matrix organic electro luminescent display device." (EX1005, [0014]², [0006],

² All annotations in color and emphasis added, unless otherwise noted.

[0007], [0034], Fig. 1; EX1002, ¶¶52-54.)

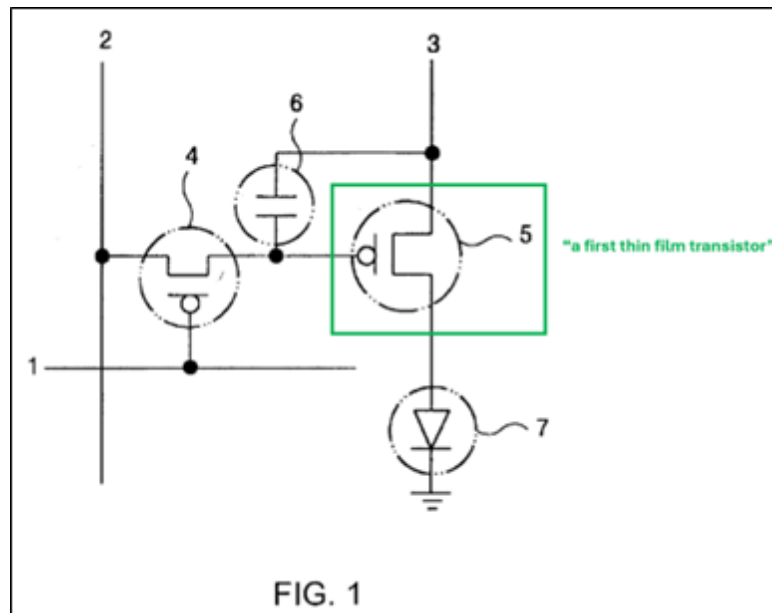
2. 1[a]: “a substrate;”

Park’s device “is formed on a transparent *substrate 100*” (Figures 4 and 5 (below)). (EX1005, [0034], [0007], [0008], [0034]; EX1002, ¶¶55-57.)

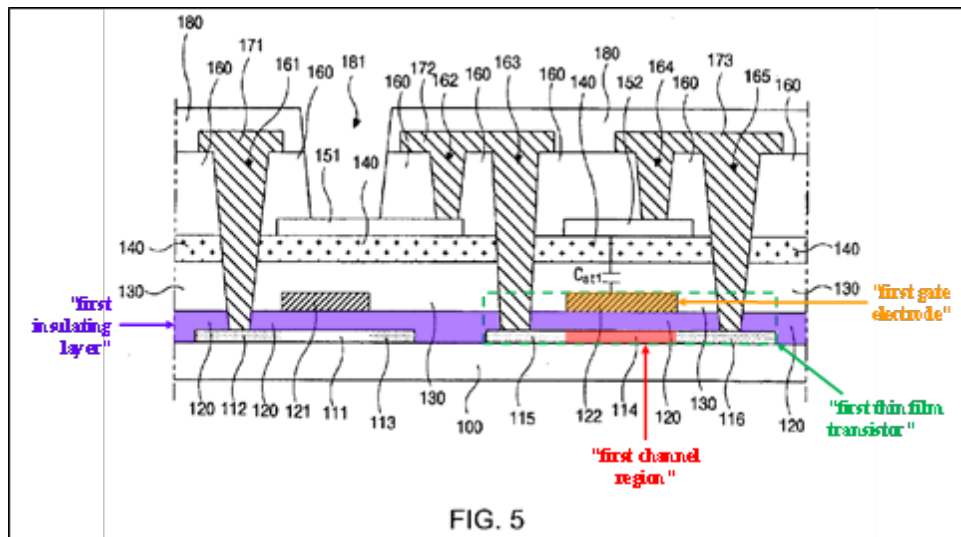
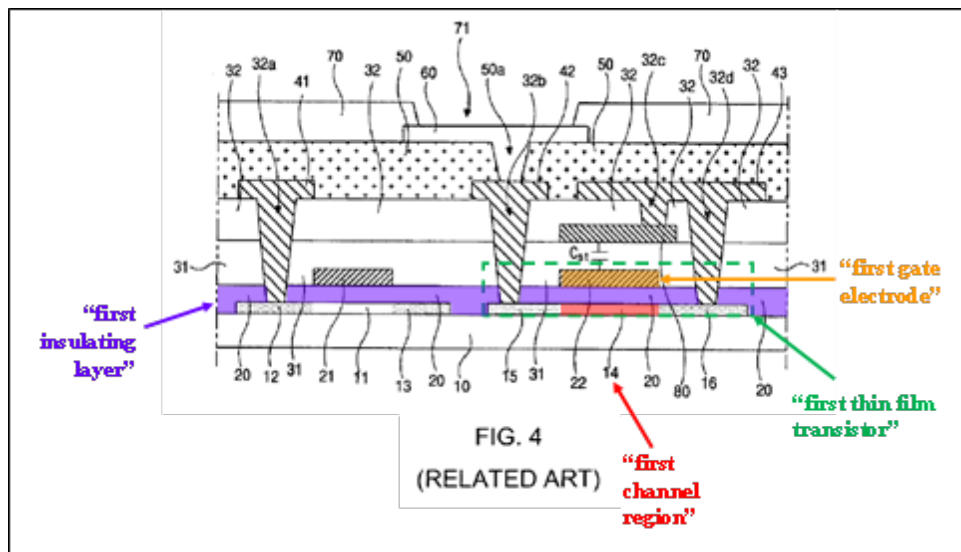


3. 1[b]: “a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”

Park’s *driving transistor 5* (Figure 1 (below)) comprises a gate electrode 22/122 (Figures 4 and 5 (below)) and an active layer 14/114. (EX1005, [0006], [0007], [0034]; EX1002, ¶¶58-60.)

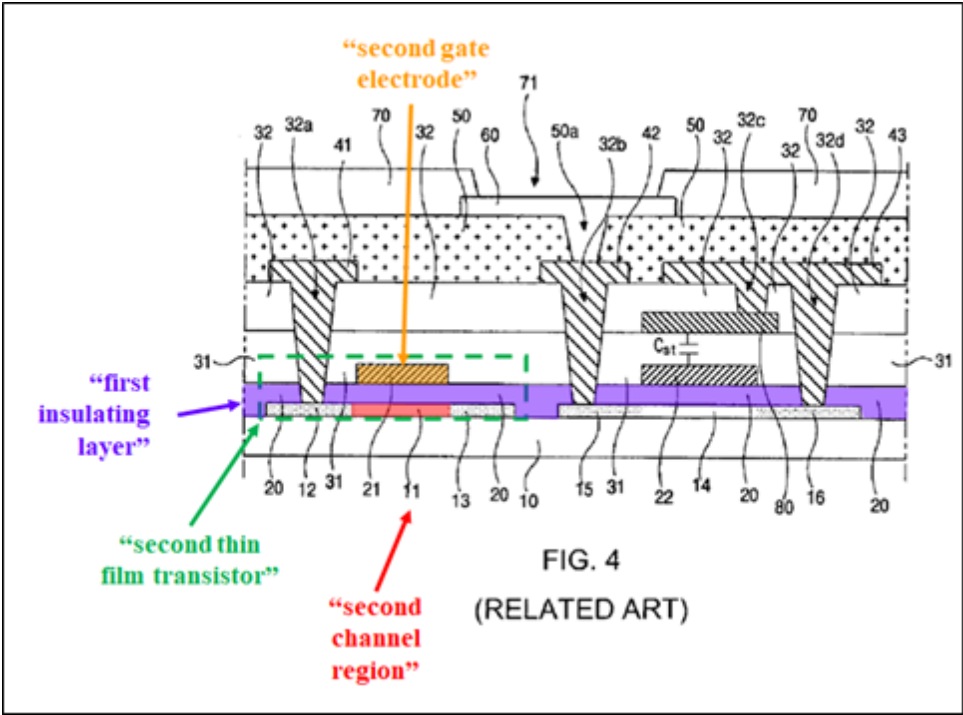
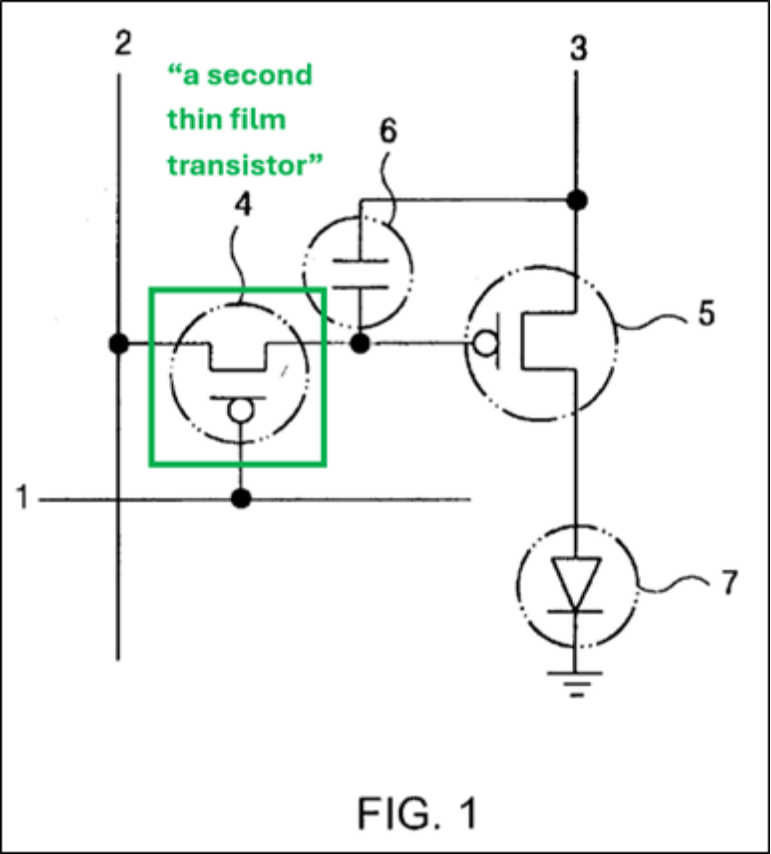


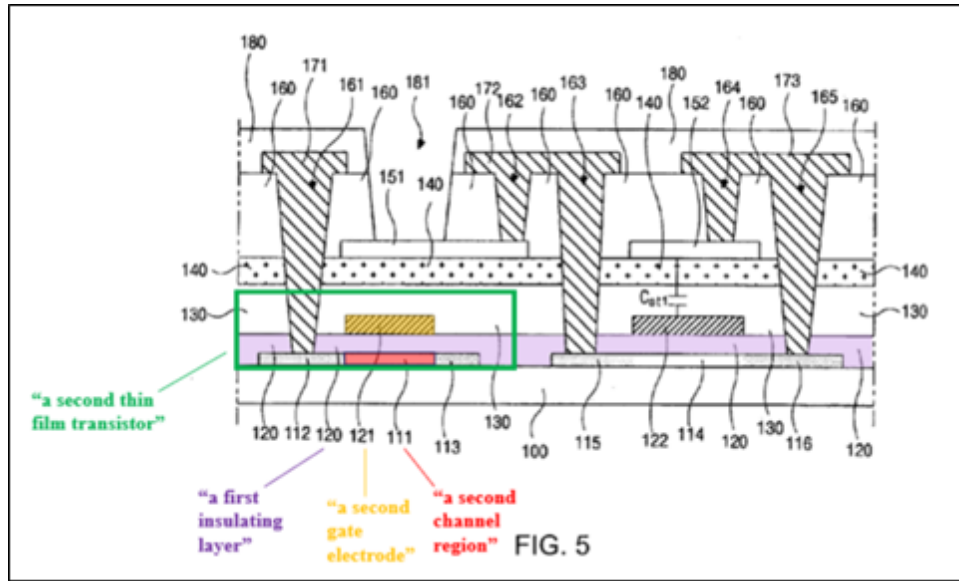
insulating layer 120 respectively over the active area 111 and 114.” (EX1005, [0034], [0007], [0036].) For Figure 4, “first and second gate electrodes 21 and 22 are formed on the gate insulating layer 20 over the active layer 11 and 14.” (EX1005, [0007], [0009]; EX1002, ¶¶61-63.)



4. 1[c]: “a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”

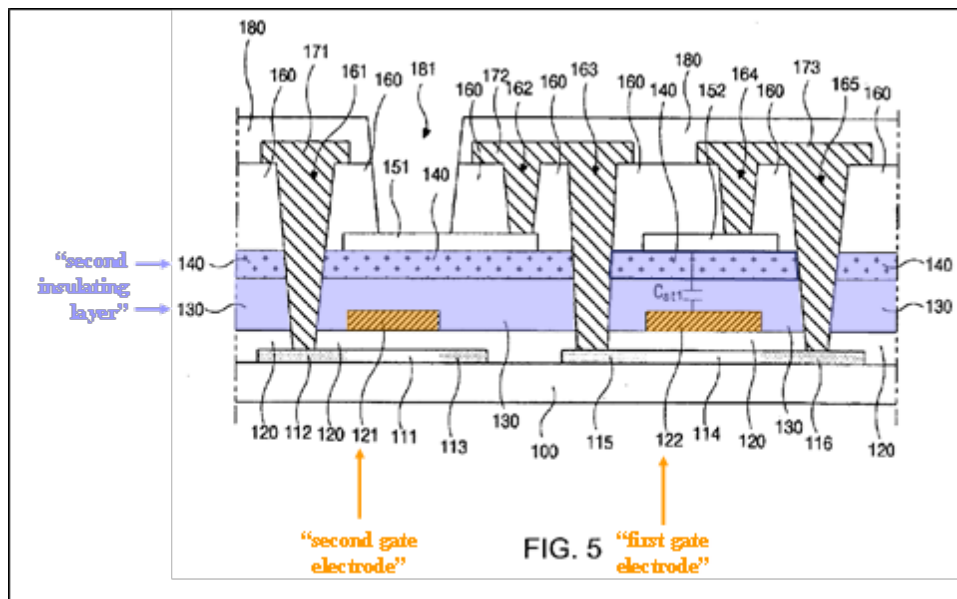
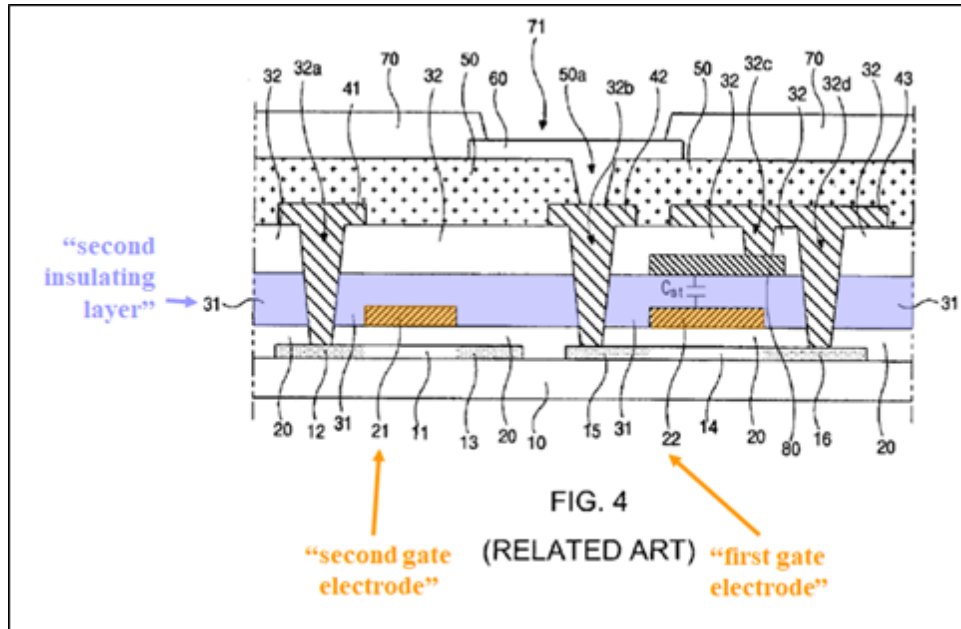
Park’s *switching transistor 4* (Figure 1 (below)) comprises a gate electrode 21/121 and an active layer 11/111 (Figures 4 and 5 (below)). (EX1005, [0034], [0007].) The *gate electrode 21/121* (“second gate electrode”) overlaps the *active layer 11/111* (“second channel region”). (EX1005, [0006].) The gate electrode 21/121 and active layer 11/111 are spaced apart from each other with the *insulating layer 20/120* (“first insulating layer” (1[b])) therebetween. Park’s gate electrode 121 is “formed on the gate insulating layer 120 respectively over the active area 111 and 114.” (EX1005, [0034], [0007]; EX1002, ¶¶64-69.)





5. 1[d]: “a second insulating layer disposed on the first and second gate electrode;”

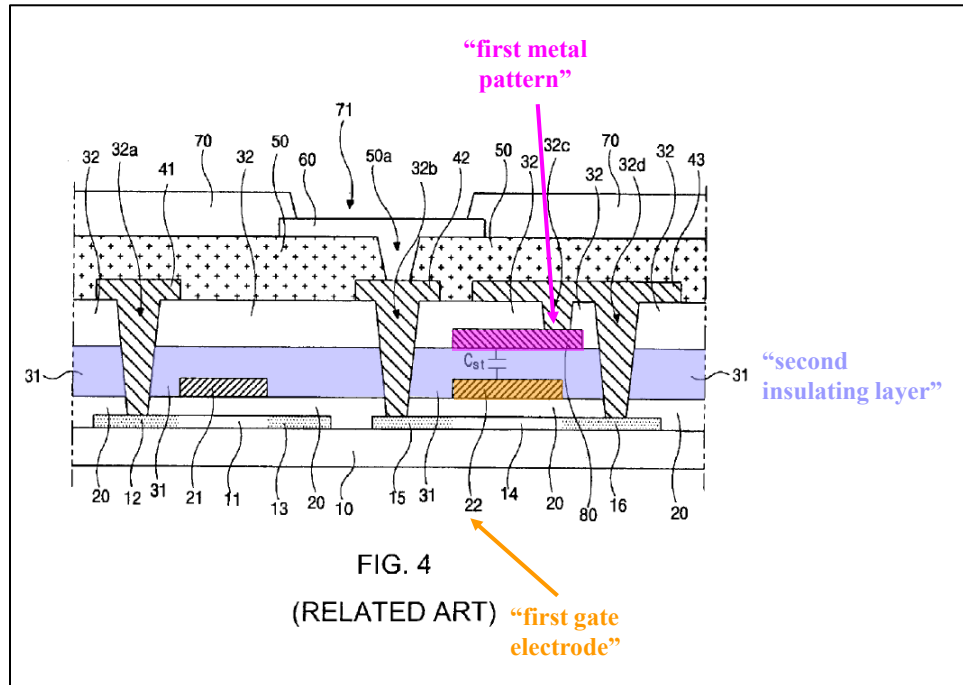
Park discloses *inter layer 31/130* and *inter layer 140* (“second insulating layer”) formed of silicon oxide (SiO₂) and disposed on the *gate electrode 22/122* (“first gate electrode” (1[b])) and *gate electrode 21/121* (“second gate electrode” (1[c])) (Figures 4 and 5 (below)). (EX1005, [0015], [0007], [0034]; EX1002, ¶¶70-72.)

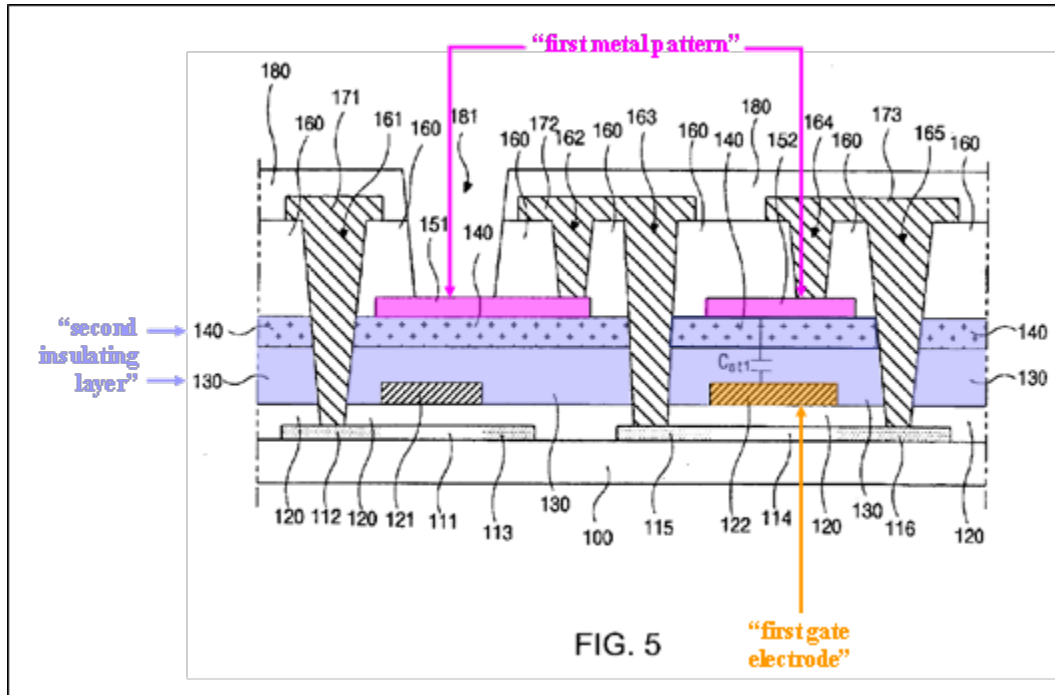


6. 1[e]: “a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”

Park’s device comprises an *anode electrode 151 and capacitor electrode 80/152* (part of the “first metal pattern”) (Figures 4 and 5 (below)) overlapping the

gate electrode 22/122 (“first gate electrode” (1[b])). The *anode electrode 151* and *capacitor electrode 80/152* and *gate electrode 22/122* are spaced apart from each other with *interlayer 31/130* and/or *inter layer 140* (“second insulating layer” (1[d])) therebetween. (EX1005, [0015], [0034], [0037]; EX1002, ¶¶73-75, 78-79.)



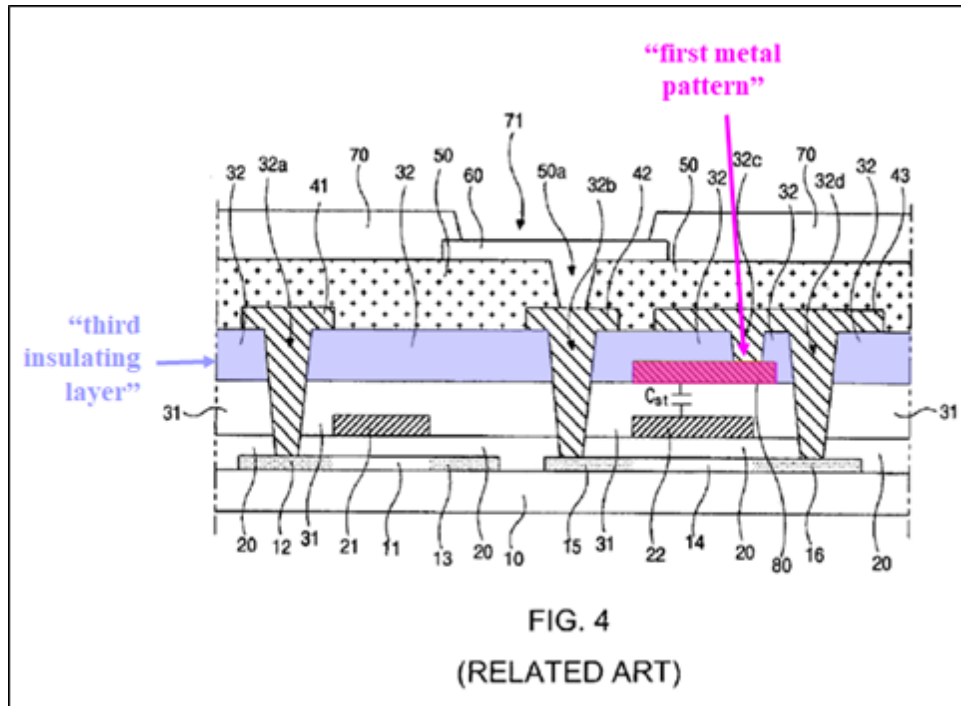


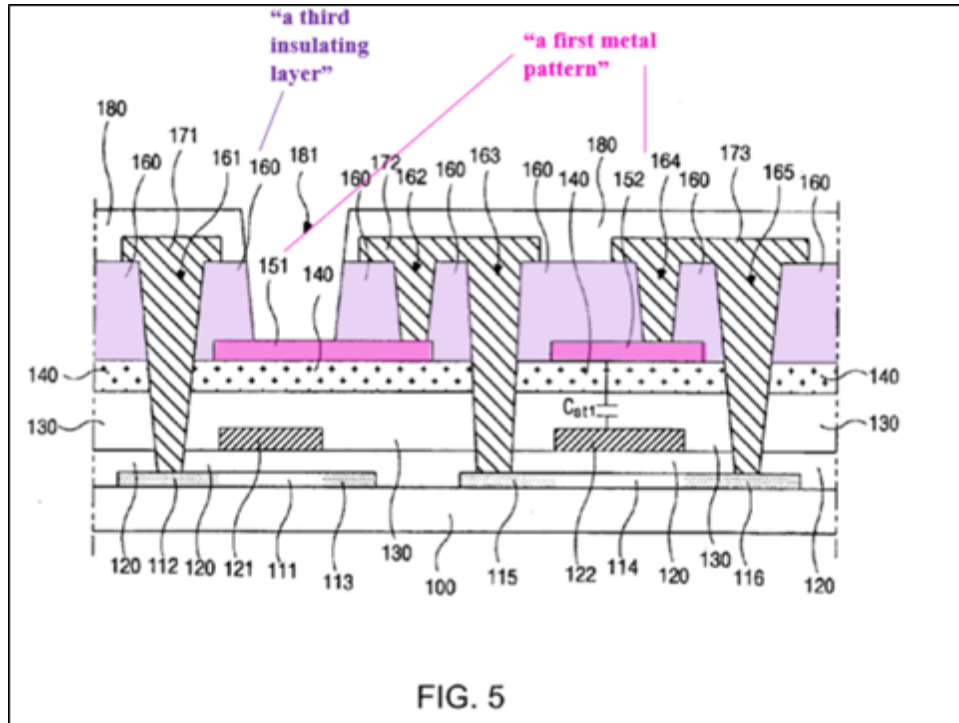
In Figure 4, the “capacitor electrode 80 must be formed of metal material.” (EX1005, [0015].) In Figure 5, the anode electrode 151 and capacitor electrode 152 “are formed of transparent conductive material *such as* indium tin oxide (ITO).” (EX1005, [0034].) It would have been obvious for the anode electrode 151 and capacitor electrode 152 to be a different material, such as a metal material because it was known that using a reflective metal for the electrodes for top-emitting OLEDs was advantageous. (See, e.g., EX1010, [0020], [0069]; EX1002, ¶¶76-77.)

7. 1[f]: “a third insulating layer disposed on the first metal pattern; and”

Park discloses an *inter layer 32/passivation layer 160* (“third insulating layer”) (Figures 4 and 5 (below)) “formed of a material such as silicon oxide

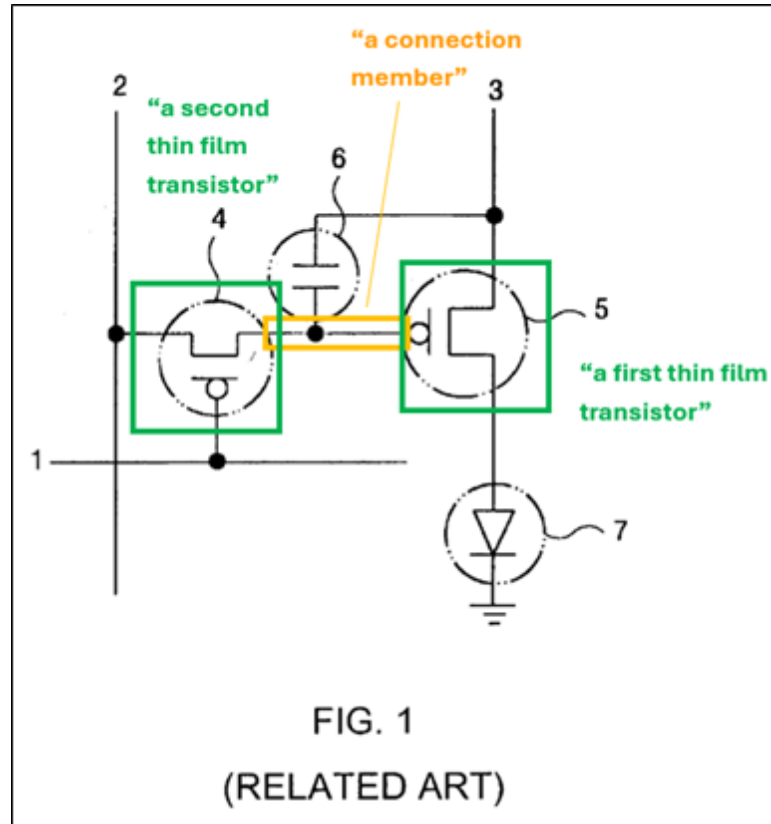
(SiO₂) and on the *anode electrode 151 and the capacitor electrode [80/152]*” (part of the “first metal pattern” (1[e])). (EX1005, [0034], [0015], [0038].) SiO₂ is an insulating layer. EX1002, ¶¶81-83.)





8. 1[g]: “a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor.”

Park’s circuit comprises a “drain electrode of the switching thin film transistor 4 [] *connected to* a gate electrode of the thin[] film transistor 5” and a “storage capacitor 6 [] *connected to* the gate electrode and the source electrode of the driving thin film resistor 5.” (EX1005, [0006].) Figure 1 (below) shows a *connection member* electrically connecting the gate electrode of the *driving transistor 5* (“first gate electrode” (1[b])) and the *switching transistor 4* (“second thin film transistor” (1[c])). (EX1002, ¶¶84-85.)

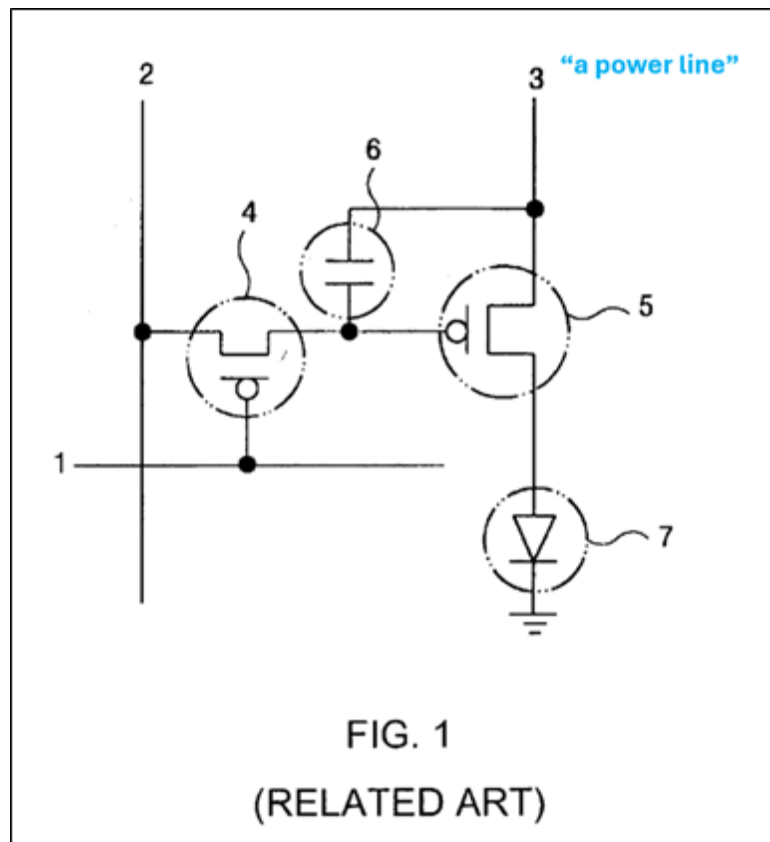


Park's connection member includes the "first drain electrode" disposed on the inter layer 32/passivation layer 160 ("third insulating layer" (1[f])). (EX1005, [0007], [0034], [0039], [0041].) The first drain electrode is connected to the first drain region 13/113 of the switching transistor 4 ("second thin film transistor") and connected to the second gate electrode 22/122. (*Id.*; EX1002, ¶¶86-90.)

C. Claim 11: "The TFT array substrate of claim 1, further comprising a driving voltage line on the third insulating layer, wherein the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer."

Park's Figure 1 circuit (below) shows a "source electrode of the driving thin film transistor 5 is connected to a *power line 3*." (EX1005, [0006].) The source

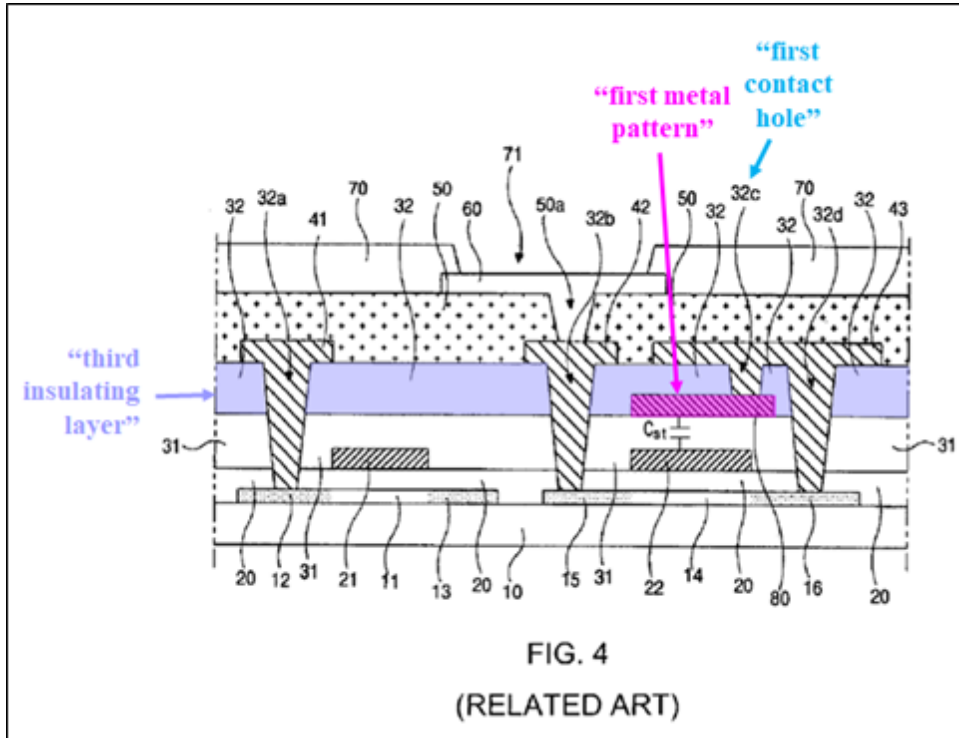
electrode 43/173 is connected to the power line 3 and extends from the power line 3 or may be a portion of the power line 3. (EX1005, [0007], [0034].) The “power line (not shown), which is connected to the second source electrode [43/]173, are also formed on the [inter layer 32/]first passivation layer 160” (“third insulating layer” (1[f])). (EX1005, [0020], [0021], [0034], [0039]; EX1002, ¶¶91-96.)

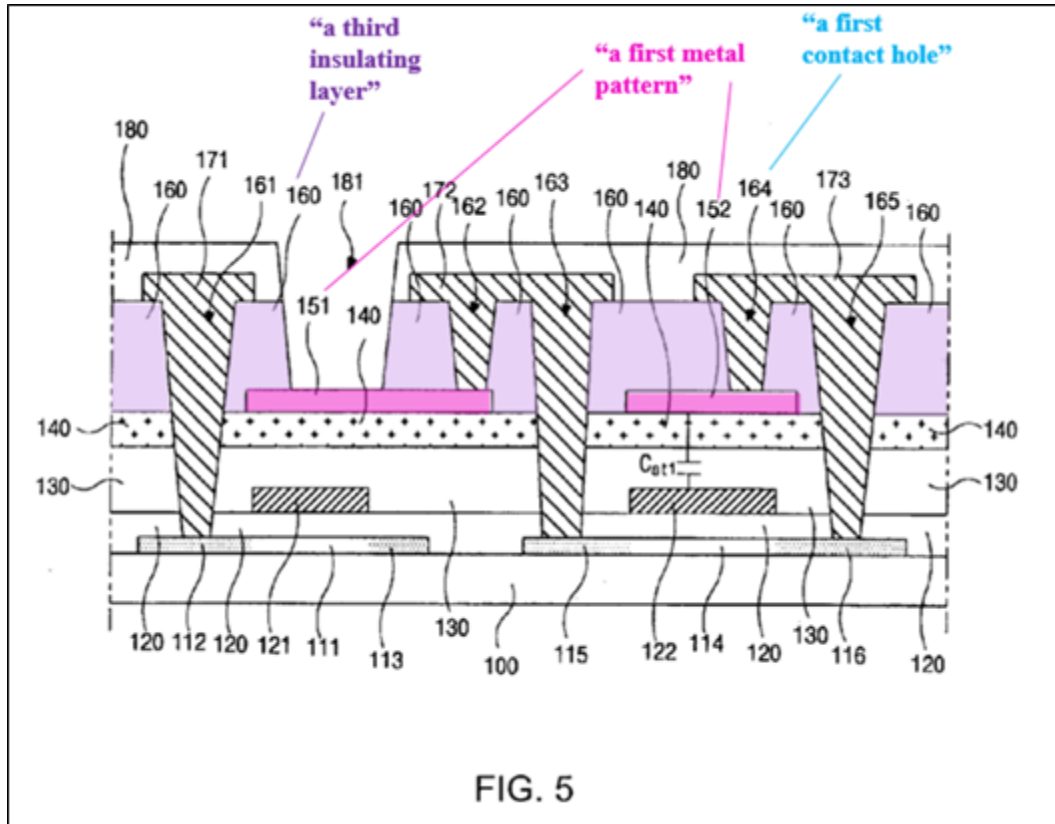


Figures 4 and 5 (below) show the *contact hole 32c/164* (“first contact hole”) connecting to the *capacitor electrode 80/152* (part of the “first metal pattern” (1[e])) through the *passivation layer 32/160* (“third insulating layer” (1[f])). “The second source electrode [43/]173 *is connected to the capacitor electrode [80/]152* and the second source region [16/]110 *through the fourth and fifth contact holes*

[32c]/164 and [32d]/165.” (EX1005, [0039], [0015], [0034], [0038]; EX1002,

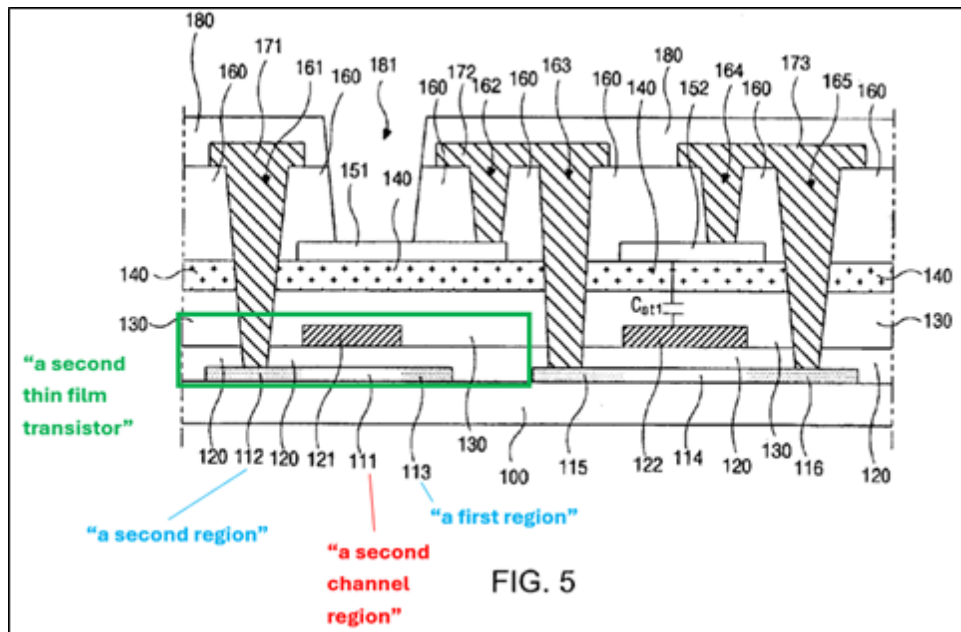
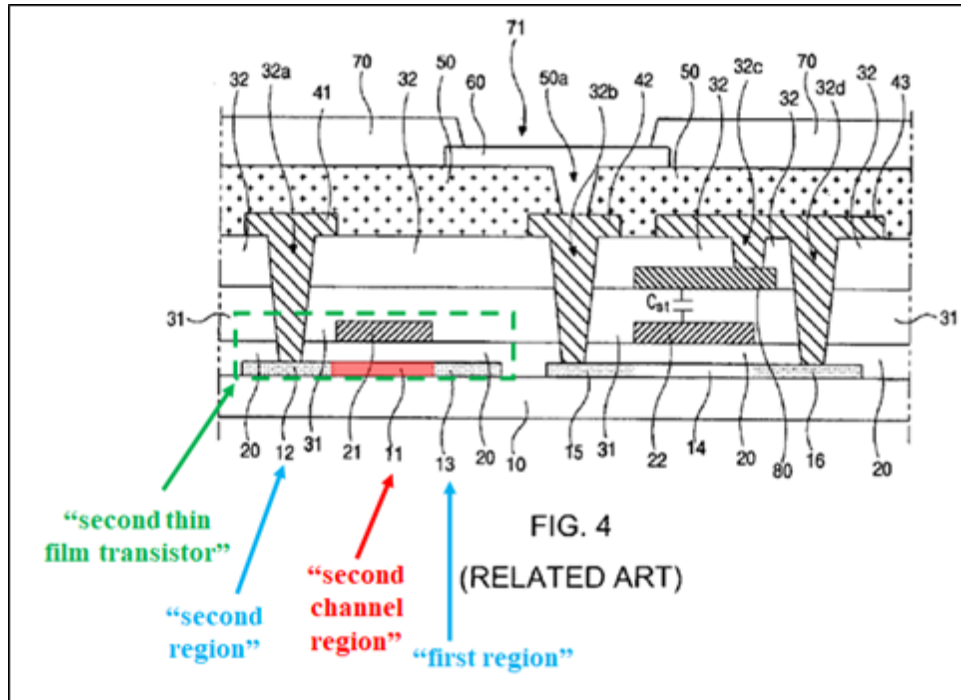
¶97.)





D. Claim 14: “The TFT array substrate of claim 1, further comprising a first gate line electrically connected to the second gate electrode.”

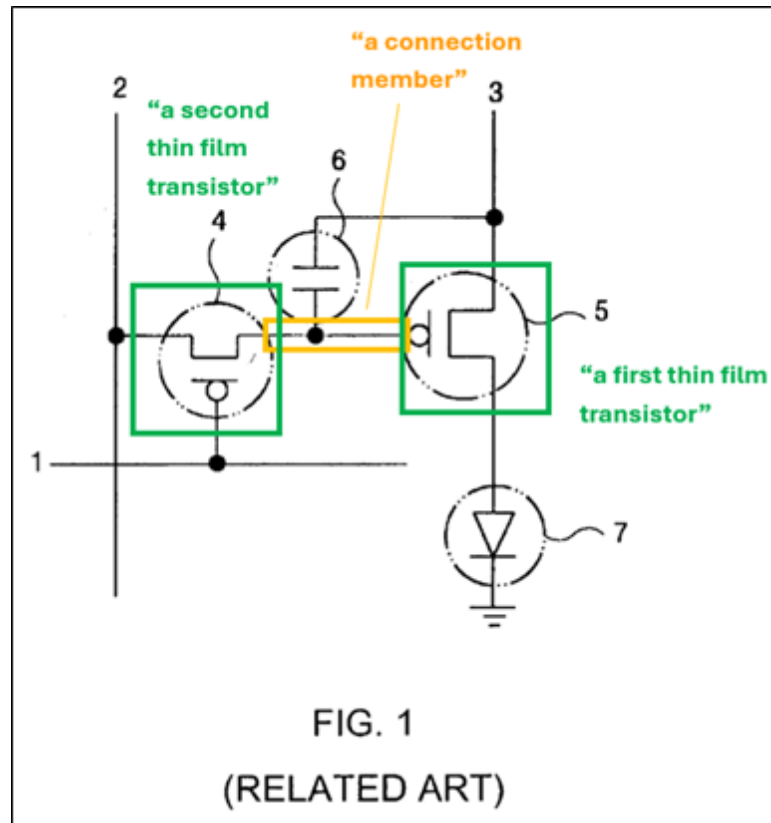
Park’s *gate line 1* (“first gate line”) is electrically connected to the gate electrode of the *switching transistor 4* (“second gate electrode” (1[c])) (Figure 1 (below)). (EX1005, [0006].) (EX1002, ¶¶98-99.)



2. 15[b]: “the first region is electrically connected to the first gate electrode via the connection member.”

Park's Figure 1 (below) shows the drain region 13/113 ("first region" (15[a])) of the *switching transistor 4* is electrically connected to the gate electrode

(“first gate electrode” (1[b])) of the *driving transistor 5* via the *connection member* (1[g]). The “second gate electrode [22/]122 is electrically connected to the first drain region [13/]113.” (EX1005, [0034], [0007], [0015].) The “first drain electrode (not shown) [] is connected to the first drain region [13/]113,” “[t]he second source electrode [43/]173 is connected to the capacitor electrode [80/]152,” and “[t]he capacitor electrode [80/]152 forms a storage capacitor C_{st1} together with the second gate electrode [22/]122.” (*Id.*; EX1002, ¶¶103-105.)



VI. GROUND 2: PARK AND ZHAN RENDER OBVIOUS CLAIMS 2-6, 22-24, AND 27

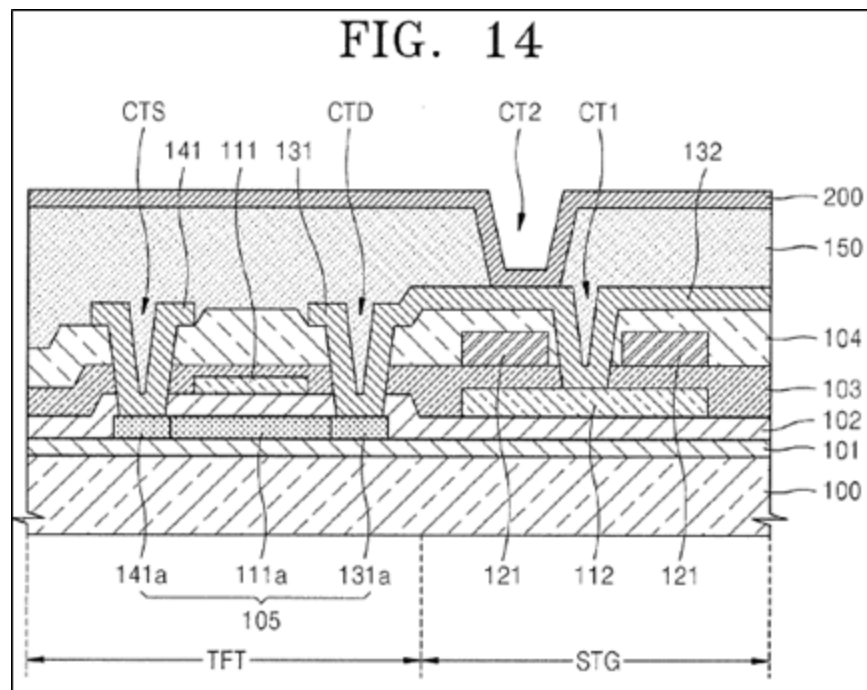
A. Summary Of Zhan

Zhan discloses a flat panel display device (*e.g.*, OLED or liquid crystal

display) having “increased capacitance arranging a storage capacitor in parallel through a first storage electrode located at a same level as a gate electrode.”

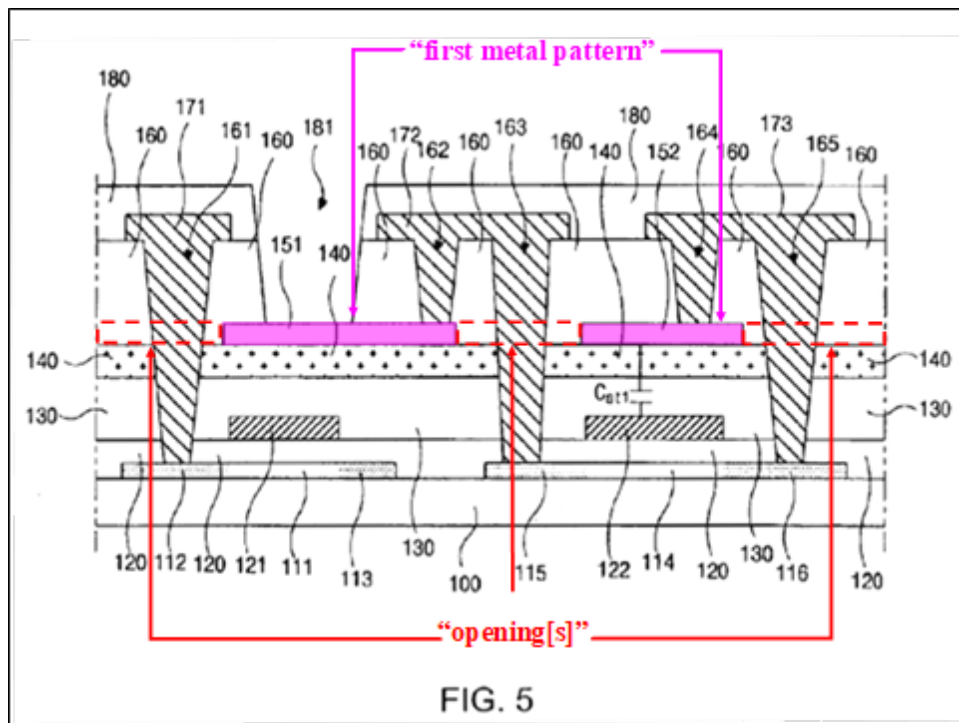
(EX1011, [0007], [0003], [0041].) The “second storage electrode 121 is divided and the first contact hole CT1 is disposed between the divided second storage electrodes 121. ... a hole may be located in the center of the second storage electrode 121.” (EX1011, [0073]; EX1002, ¶¶106-108.)

Figure 14 (below) shows a cross-sectional view of an embodiment that advantageously creates a direct connection from the transistor to the pixel and then to the capacitor. (EX1002, ¶109.)



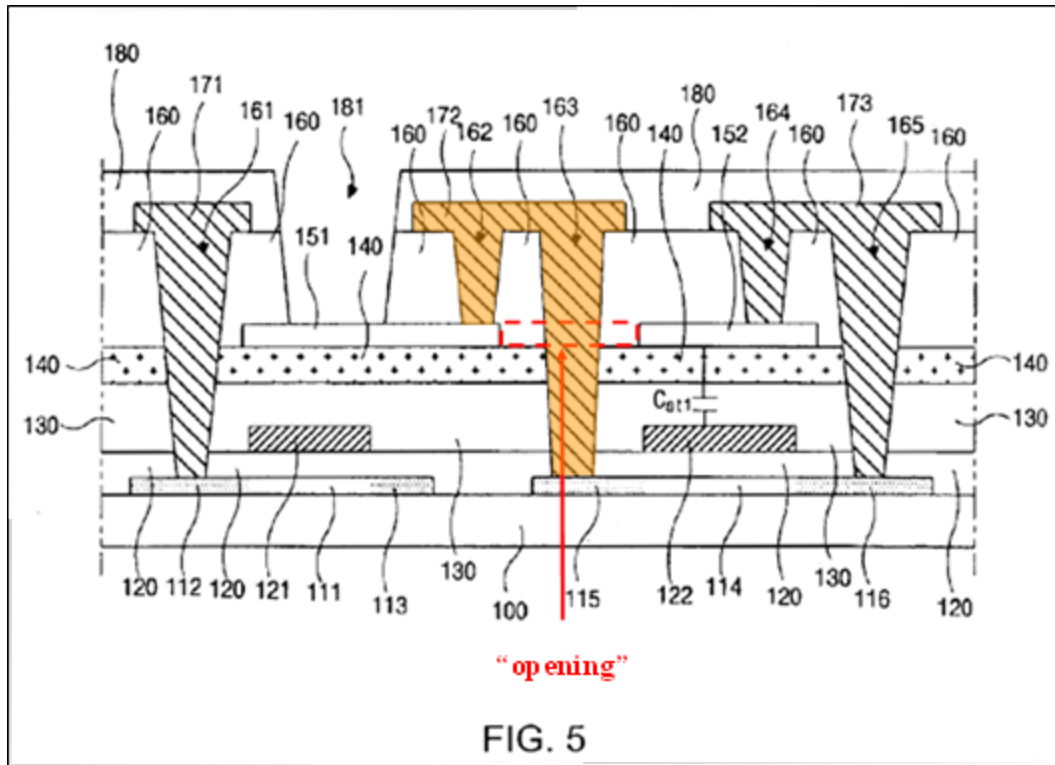
B. Claim 2: “The TFT array substrate of claim 1, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.”

Figure 5 (below) shows Park’s *anode electrode 151 and the capacitor electrode 152* (part of “first metal pattern” (1[e])) including an *opening*. (EX1005, [0015], [0034]; EX1002, ¶¶110-111.)



Park’s “first passivation layer 160 *is then formed on* the anode electrode 151 and the capacitor electrode 152.” (EX1005, [0038].) Park’s “first source electrode 171, the second drain electrode 172 and the second source electrode 173 are formed by depositing conductive material such as metal *on the* first passivation layer 160 and patterning it with a fifth mask.” (EX1005, [0039].) The *drain electrode 172* overlaps an *opening* of the layer of the anode electrode 151 and

capacitor electrode 152 in a plan view due to the drain electrode 172 being located closer to the top than the opening. (EX1002, ¶¶112-114.)

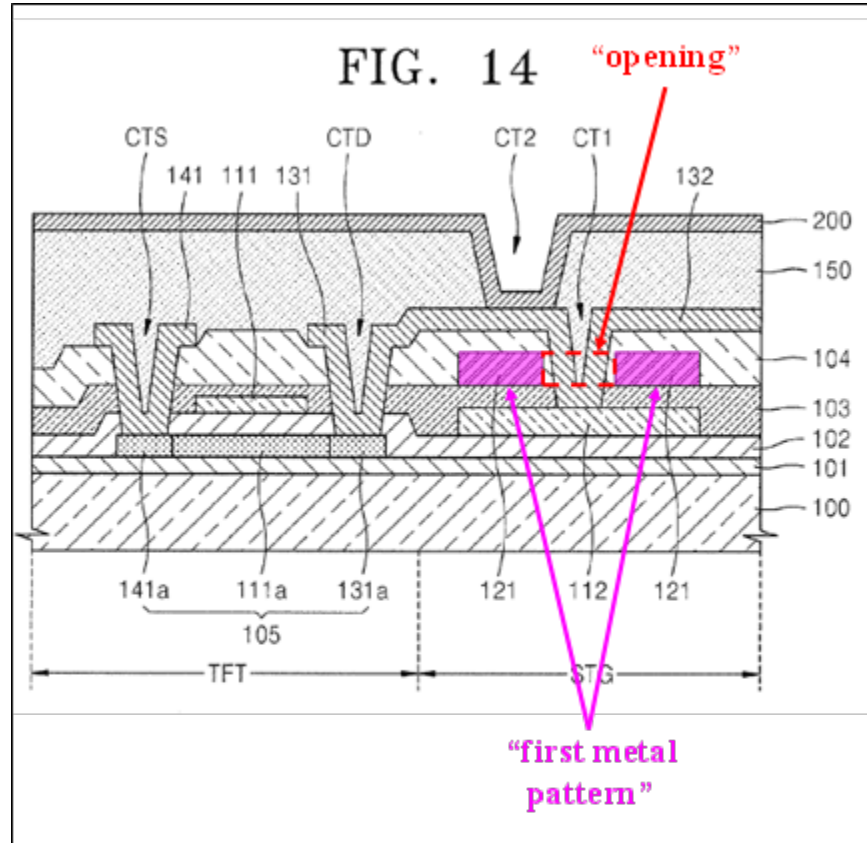


Although Figure 5 specifically shows the drain electrode 172, Park describes the first drain electrode of the switching transistor 4 (part of the “connection member”) as “not shown.” (EX1005, [0007], [0034].) A POSITA would have expected the figure to represent the structure of the other transistor electrodes, including the drain electrode of the switching transistor 4. (EX1002, ¶¶115-116.)

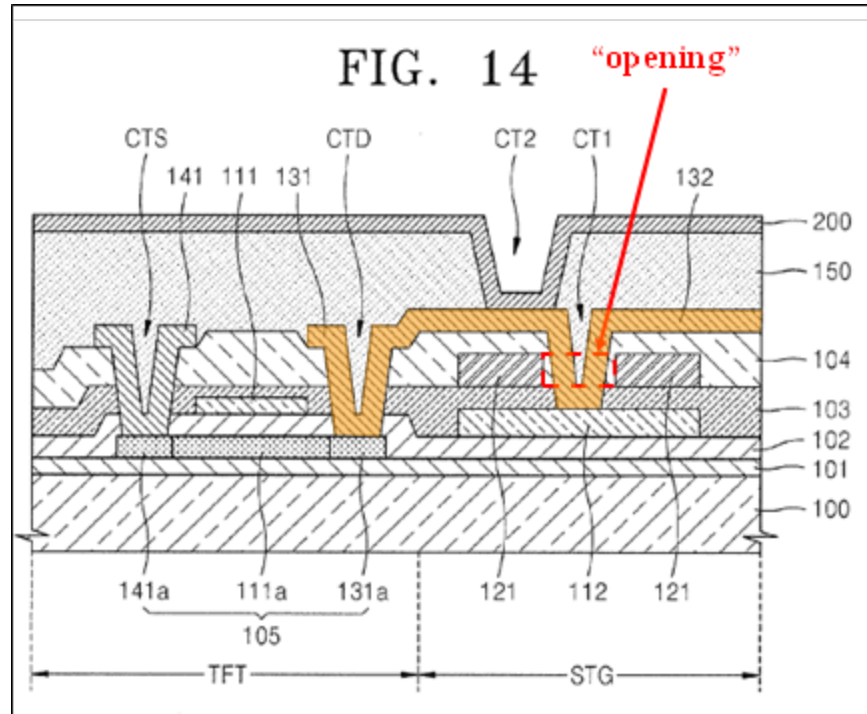
Zhan’s “second storage electrode 121 is divided and the first contact hole CT1 is disposed between the divided second storage electrodes 121 ... at least two second storage electrodes 121 may be formed and in a plan view, a *hole may be*

located in the center of the second storage electrode 121” (Figure 14 (below)).

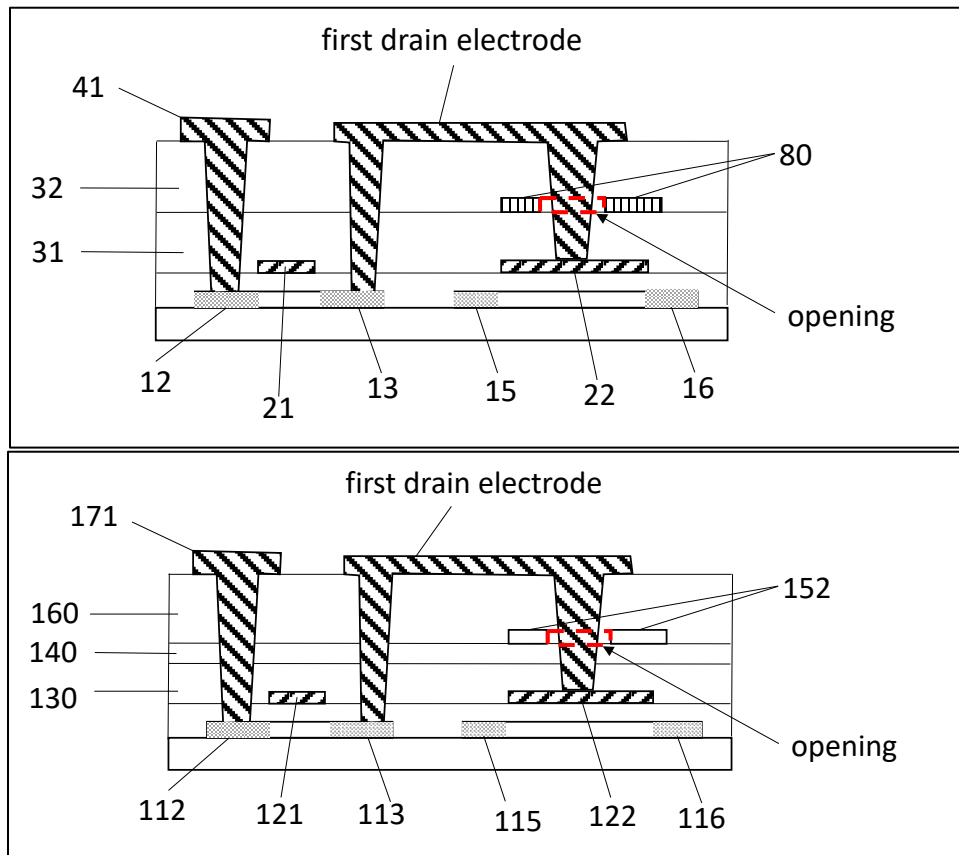
(EX1011, [0073]; EX1002, ¶117.)



Zhan’s *storage electrode 132* overlaps with the *hole* in a plan view (Figure 14 (below)). The “third storage electrode 132” is a connection member that “contacts the first storage electrode 112” and “extends from the drain electrode 131 of the TFT.” (EX1011, [0048]; EX1002, ¶118.)



A POSITA would be motivated to extend the drain electrode to connect with the first storage electrode under the second storage electrode through a first contact hole CT1 in the second electrode, as taught by Zhan, to improve the similar device of Park in the same way. The figures below show the configuration of Park's first drain electrode as part of the connection member connected between the first drain region 13/113 and the second gate electrode 22/122 based on the teachings of Zhan. (EX1002, ¶119.)



1. Motivation to combine Park and Zhan

It would have been obvious to a POSITA to combine the teachings of Park and Zhan. Park and Zhan are from the same field of endeavor, both disclosing light-emitting devices and structures for increasing the storage capacitance. Park discloses an active matrix organic ELD device “in which a storage capacitance of a storage capacitor is increased without reducing an aperture ratio.” (EX1005, [0017].) Zhan discloses increasing the capacitance without increasing area or reducing aperture ratio in an OLED apparatus. (EX1011, [0041], [0058].) Park

and Zhan are reasonably pertinent to the same technical problems of improving the manufacturing and quality of light-emitting display devices, including increasing the storage capacitance. (EX1002, ¶120.)

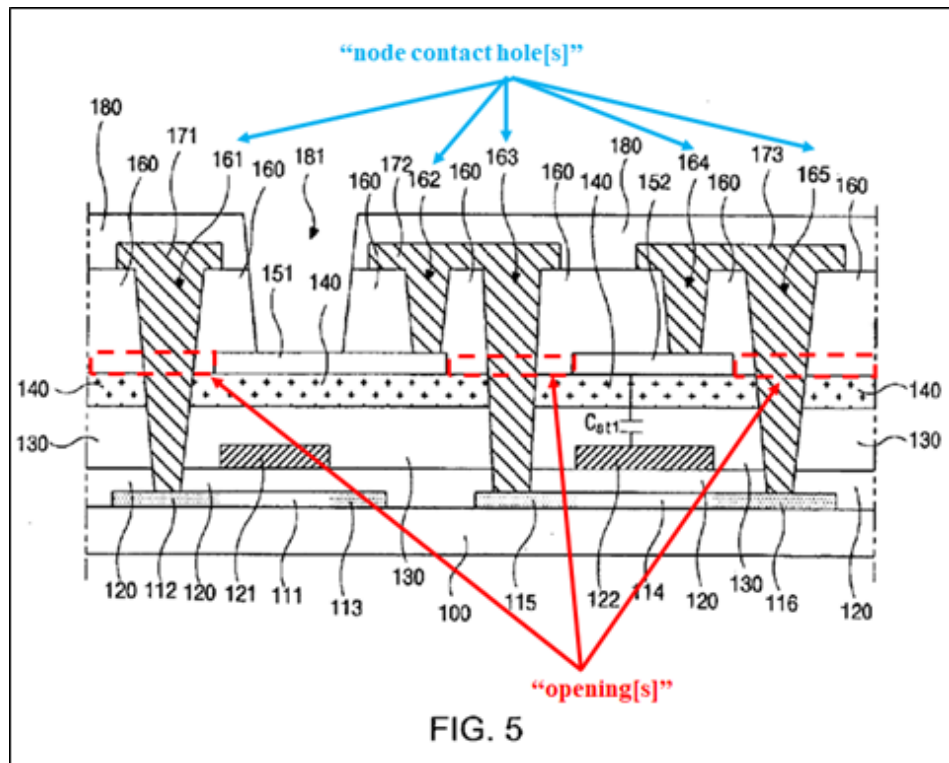
Zhan teaches using two storage capacitors sharing a storage electrode 121, resulting in greater capacitance due to the parallel structure. (EX1011, [0052].) The “second storage electrode 121 is divided and the first contact hole CT1 is disposed between the divided second storage electrodes 121 ... at least two second storage electrodes 121 may be formed and in a plan view, a hole may be located in the center of the second storage electrode 121.” (EX1011, [0073].) These technical features may be combined with the teachings of Park to generate an OLED with greater storage capacitance and reduced manufacturing deviations. Zhang improves upon Park. Given the overlap between Park and Zhang, and the prior art had already known and demonstrated such techniques with success, there would have been a reasonable expectation of success. (EX1002, ¶121.)

Because Park and Zhan both relate to increasing the storage capacitance and both use connection members to provide interconnections between layers, a POSITA would be motivated to use Zhan’s techniques to improve the similar device of Park in the same way. Zhan successfully demonstrated an OLED configuration that improved the storage capacitance. It would have been obvious to a POSITA to combine the teachings of Park and Zhan. (EX1002, ¶122.)

C. Claim 3

1. 3[a]: “The TFT array substrate of claim 2, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and”

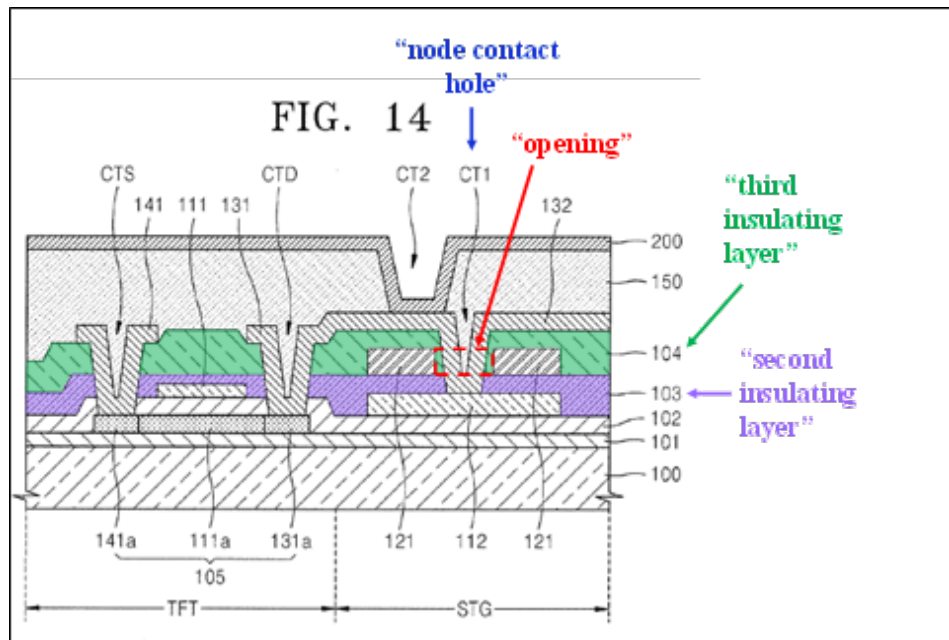
Park’s inter layer 130 and/or inter layer 140 (“second insulating layer” (1[d])) (Figure 5 (below)) and passivation layer 160 (“third insulating layer” (1[f])) include *contact holes 161, 163, and 165* overlapping the *openings* of the anode electrode 151 and capacitor electrode 152 layer. (EX1005, [0007], [0015], [0034]; EX1002, ¶¶123-126.)



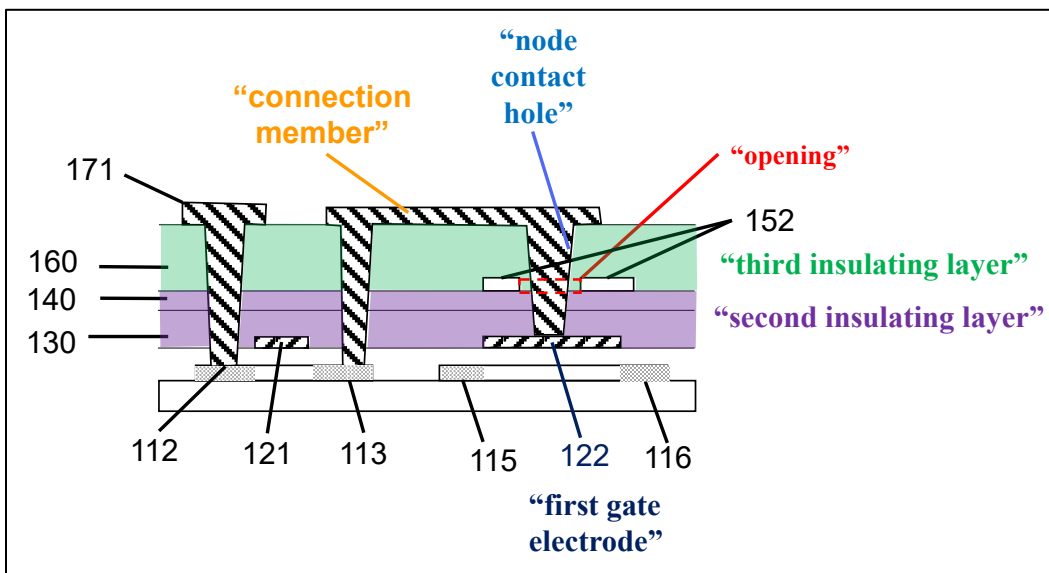
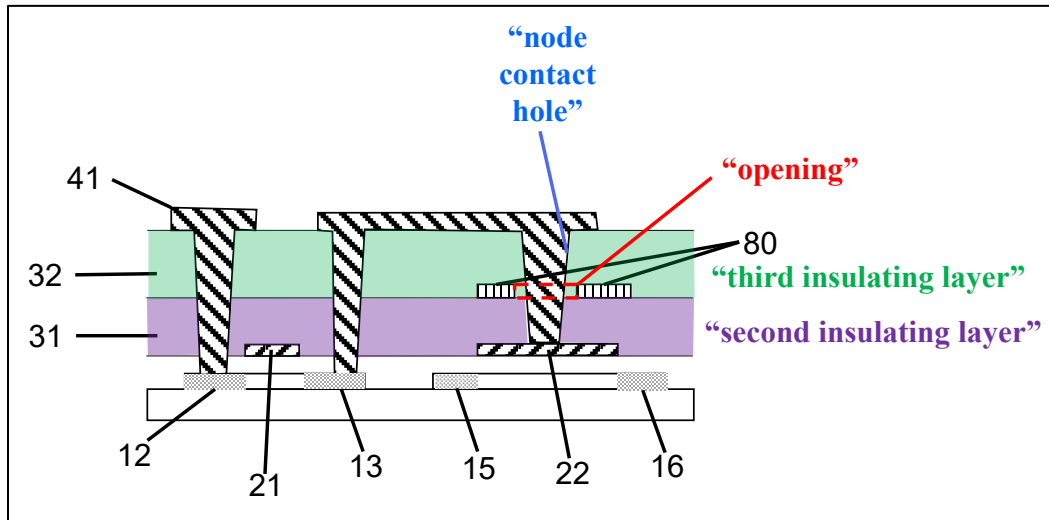
Park’s Figure 5 represents the structure for its “first drain electrode (not shown)” of the switching transistor 4 (part of the “connection member”). (See

claim 4.) Park teaches an inter layer 130 and passivation 160 including a contact hole overlapping an opening for the switching transistor 4. (EX1002, ¶126.)

Zhan discloses interlayer adjusting layer 103 and interlayer adjusting layer 104. (EX1004, [0050].) Its first contact hole CT1 is “formed by penetrating (or through) the first and second interlayer adjusting layers 103 and 104 at locations ... where the second storage electrode 121 is not located.” (EX1011, [0050].) The *interlayer adjusting layer 103* and *interlayer adjusting layer 104* (Figure 14 (below)) includes *contact hole CT1* overlapping the *hole*. (EX1002, ¶127.)



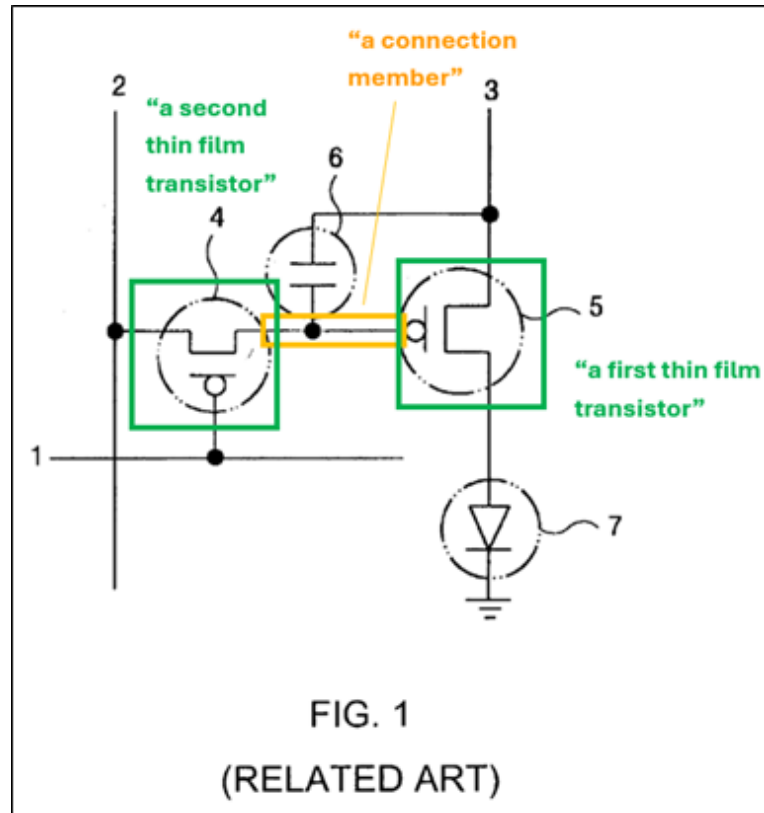
Park-Zhan teaches element 3[a]. The figures below show the *inter layer 31/130* and *inter layer 140* (“second insulating layer” (1[d])) and *inter layer 32/passivation layer 160* (“third insulating layer” (1[f])) including *node contact hole* overlapping the *opening*. (EX1002, ¶128.)



2. 3[b]: “the portion of the connection member is connected with the first gate electrode through the node contact hole.”

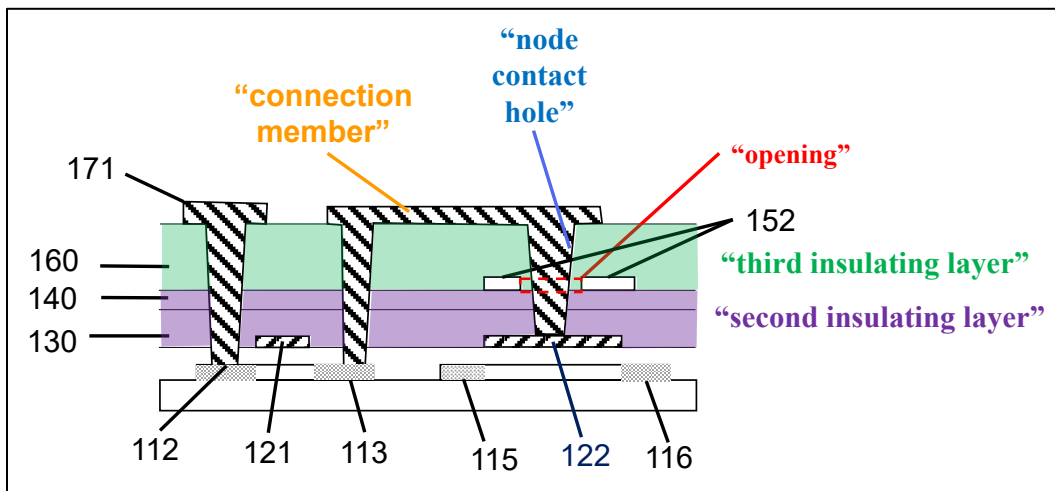
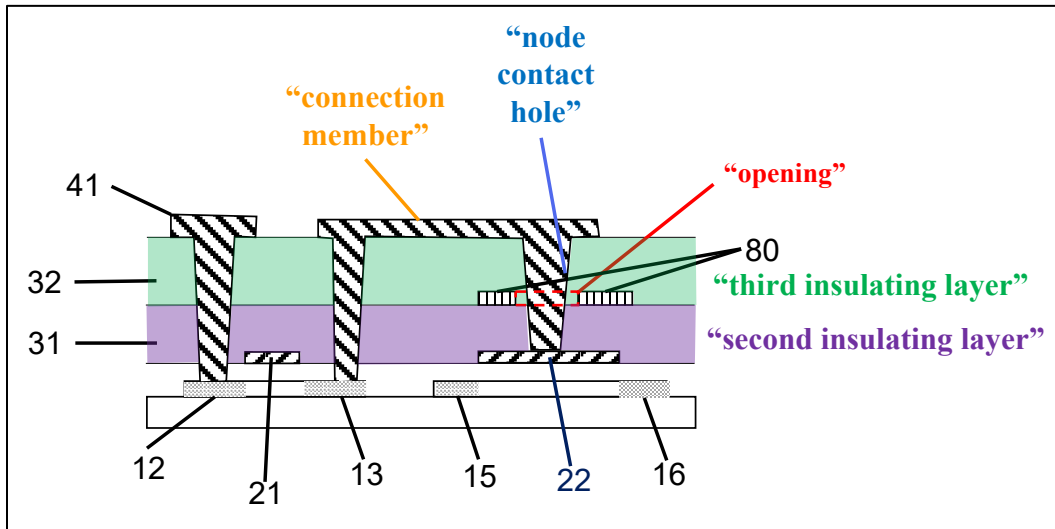
Park’s *connection member* is connected with the gate electrode 22/122 (“first gate electrode” (1[b])) of the driving transistor 5 and contact hole (“node contact hole” (3[a])). The drain electrode of the *switching transistor 4* is connected to a gate electrode of the driving transistor 5, and the storage capacitor 6

is connected to the gate electrode and the source electrode of the *driving transistor* 5 (Figure 1 (below)). (EX1005, [0006]; EX1002, ¶¶129-130.)



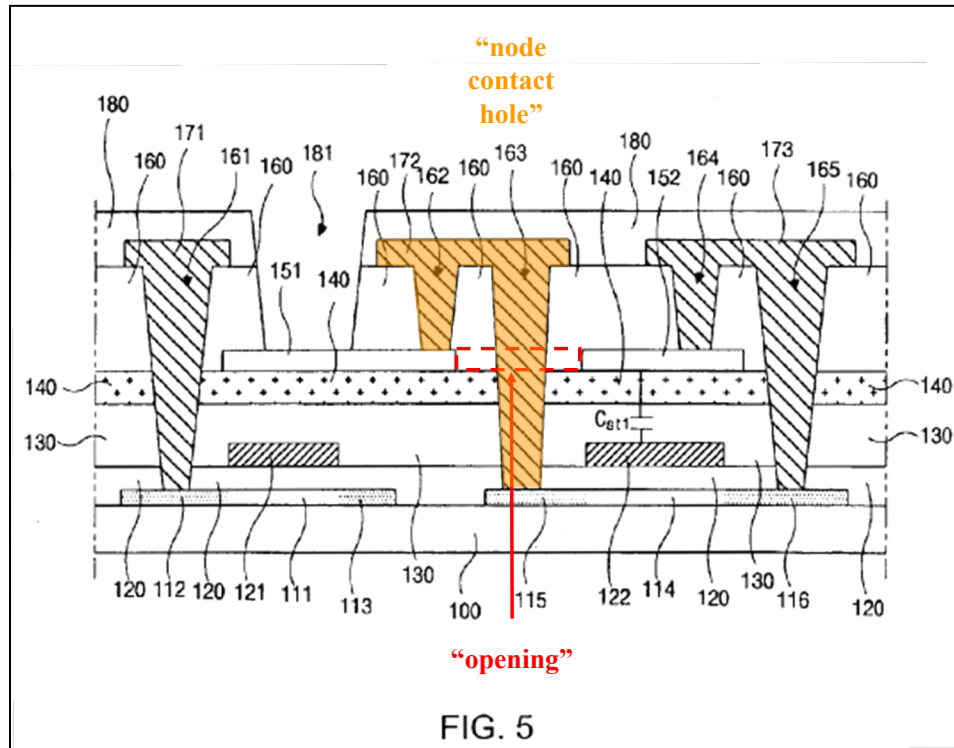
Zhan’s “third storage electrode 132 ... contacts the first storage electrode 112 through a first contact hole (or first contact unit or opening) CT1 ... the third storage electrode 132 extends from the drain electrode 131 of the TFT.” (EX1011, [0048].) The *storage electrode 132* (“connection member” (1[g])) is connected with the *storage electrode 112* through the *contact hole CT1* (“contact hole” (3[a])) (Figure 14). (EX1002, ¶¶131-132.)

Park-Zhan discloses the portion of the *connection member* is connected with the gate electrode 22/122 through the *node contact hole*. (EX1002, ¶131.)



D. Claim 4: “The TFT array substrate of claim 3, wherein a size of the opening is greater than a size of the node contact hole in the plan view.”

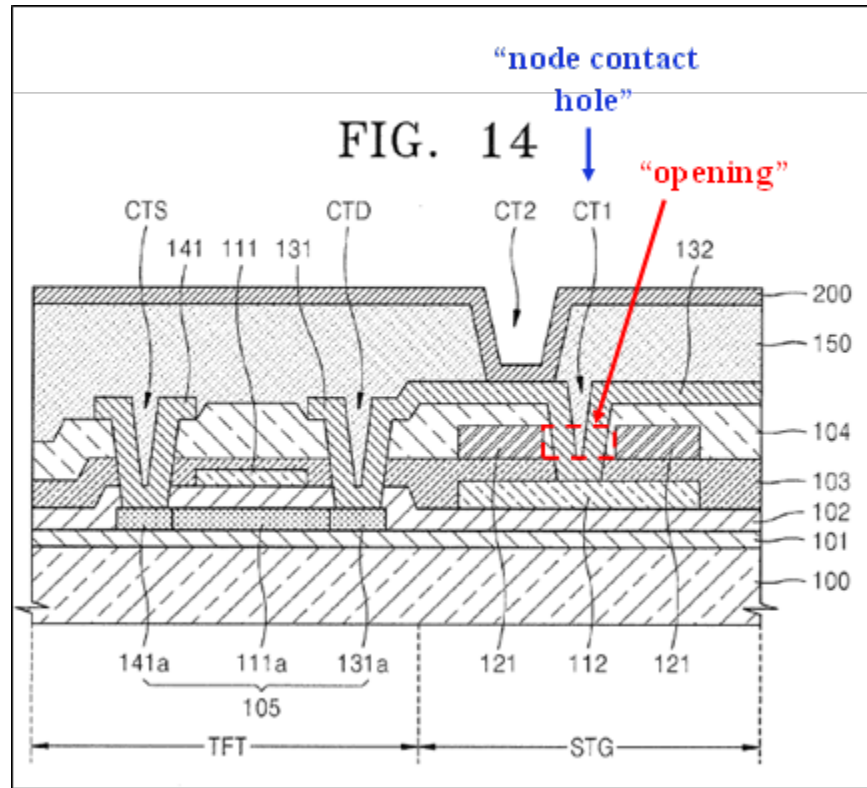
Figure 5 (below) shows the size of an *opening* is greater than a size of *contact hole 163*. (EX1005, [0007], [0034]; EX1002, ¶¶134-136.)



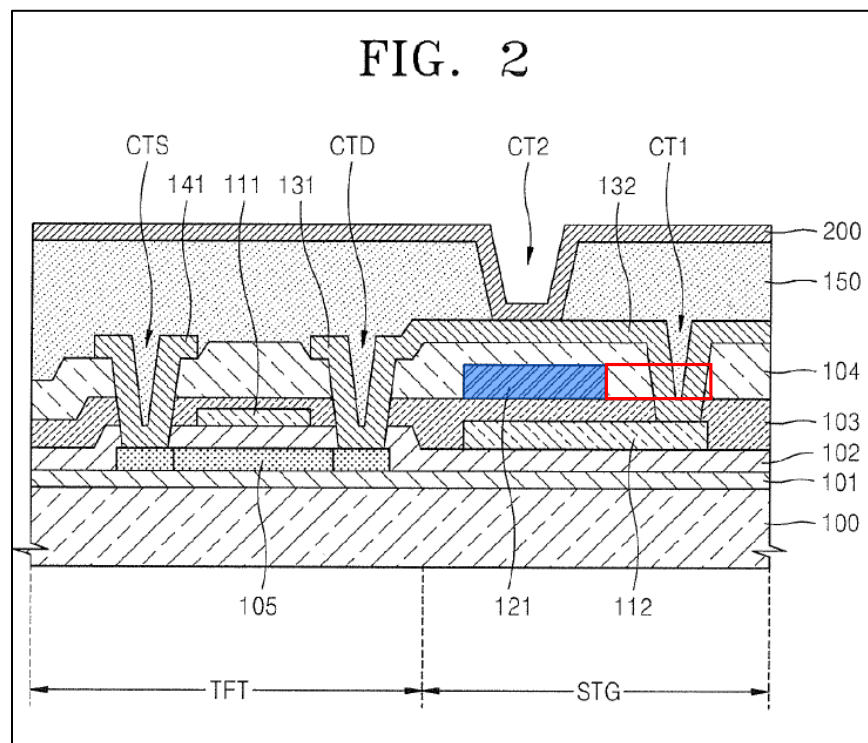
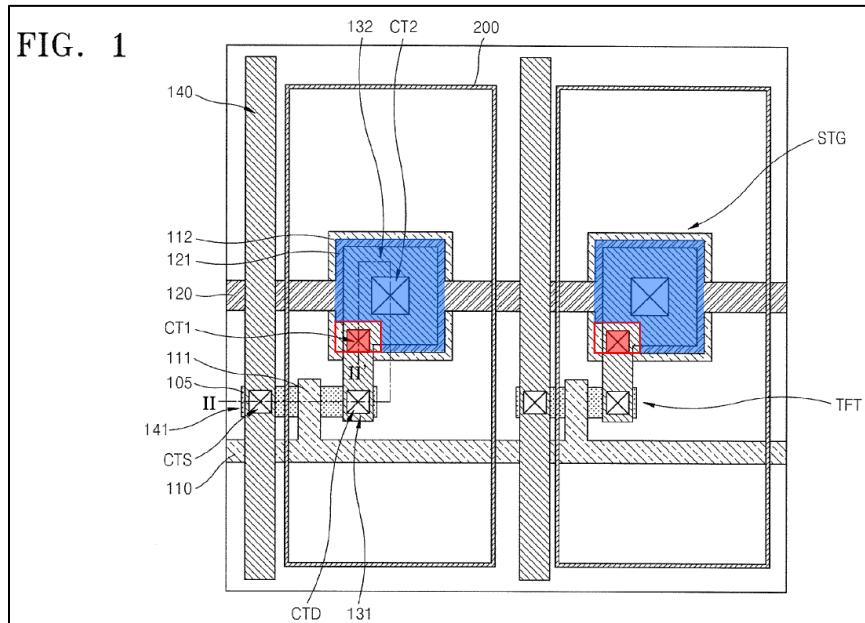
Park explains “[t]hough it is not shown in the figure, the second gate electrode 122 is electrically connected to the first drain region 113.” (EX1005, [0034], [0007].) A POSITA would have understood the drain electrode of the switching transistor 4 would have a similar configuration as the source and drain electrodes shown in Figure 5. (*See* claim 4.) This includes the contact hole of the drain electrode of the switching transistor 4 having a similar configuration (size of the opening greater than the size of the contact holes) as the contact holes of the source and drain electrodes shown in Figure 5. (EX1002, ¶137.)

Figure 14 (below) of Zhan shows the size of the *hole* is greater than a size of the *contact hole CT1* (“node contact hole” (3[a])). Even though Figure 14 is a cross-sectional view, it would have been obvious the size of the hole would be

greater than a size of the contact hole CT1 in a plan view because the width of the hole is greater than the width of contact hole CT1. (EX1002, ¶¶138-139.)

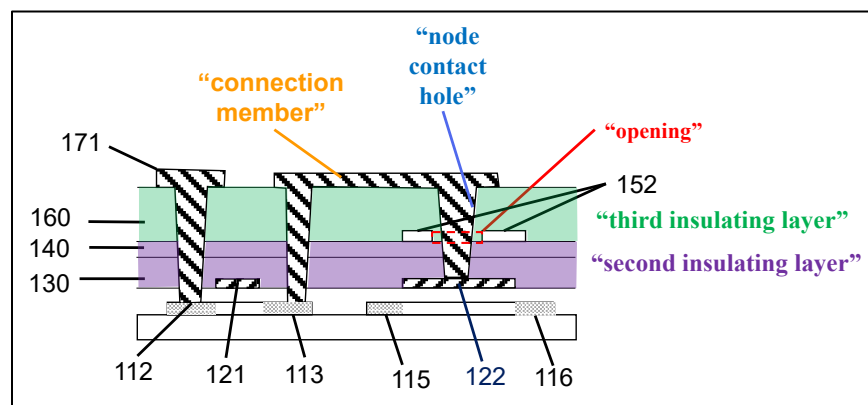
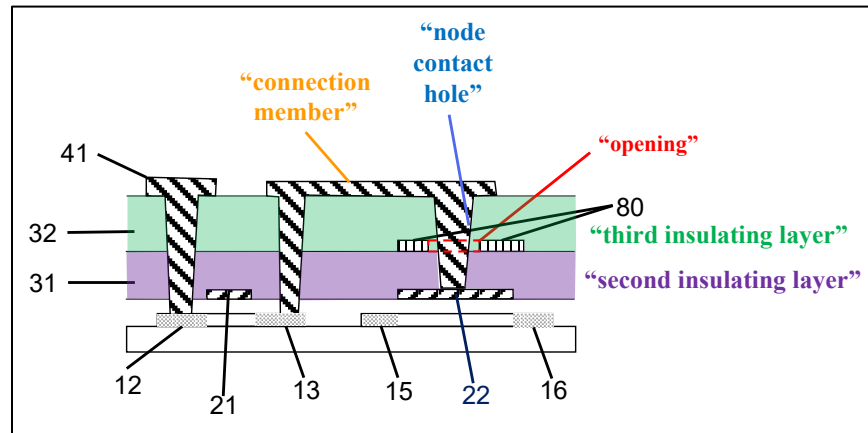


Figures 1 and 2 (below) are plan and cross-section views showing the contact hole CT1 formed by penetrating through the first and second interlayer adjusting layers 103 and 104 at locations where the second storage electrode 121 is not located. (EX1011, [0050]; EX1002, ¶140.)



Park-Zhan teaches the size of the opening is greater than the size of the node contact hole. Even though the figure below is a cross-sectional view, it would have been obvious the size of the opening would be greater than a size of the

contact hole in a plan view because the width of the opening is greater than the width of contact hole in a cross-section view. (EX1002, ¶141.)



E. Claim 5: “The TFT array substrate of claim 4, wherein the second and third insulating layers contact each other in a region between the first metal pattern and the portion of the connection member in a cross-sectional view.”

Park’s first drain electrode (“connection member” (1[g])) is disposed on the passivation layer 160. (See 1[g].) The *inter layer 130* and/or *inter layer 140* (“second insulating layer” (1[d])) and *passivation layer 160* (“third insulating layer” (1[f])) contact each other (Figure 5 (below) (shown in red circles)) between the *anode electrode 151 and capacitor electrode 152* (“first metal pattern”) and the

second drain electrode 172. It would have been obvious for the inter layer 140 and inter layer 160 contact each other in a region between the anode electrode 151 and capacitor electrode 152 and the portion of the first drain electrode in a cross-section view. (EX1002, ¶¶142-145.)

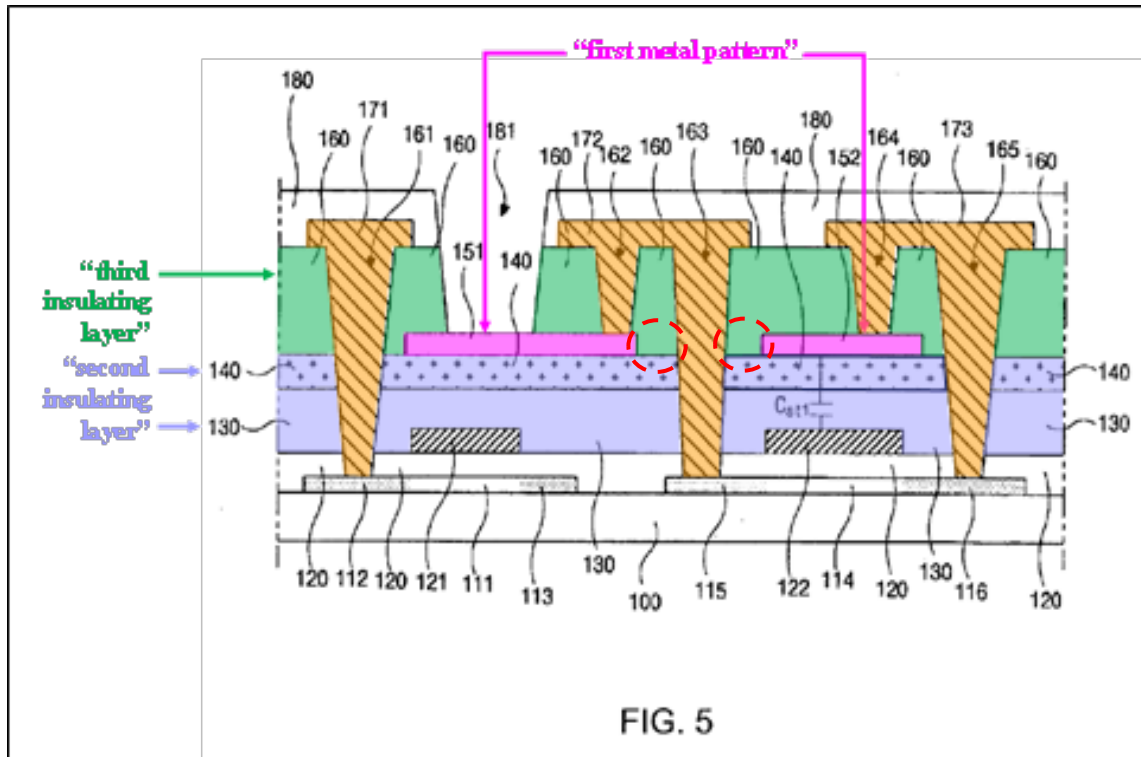
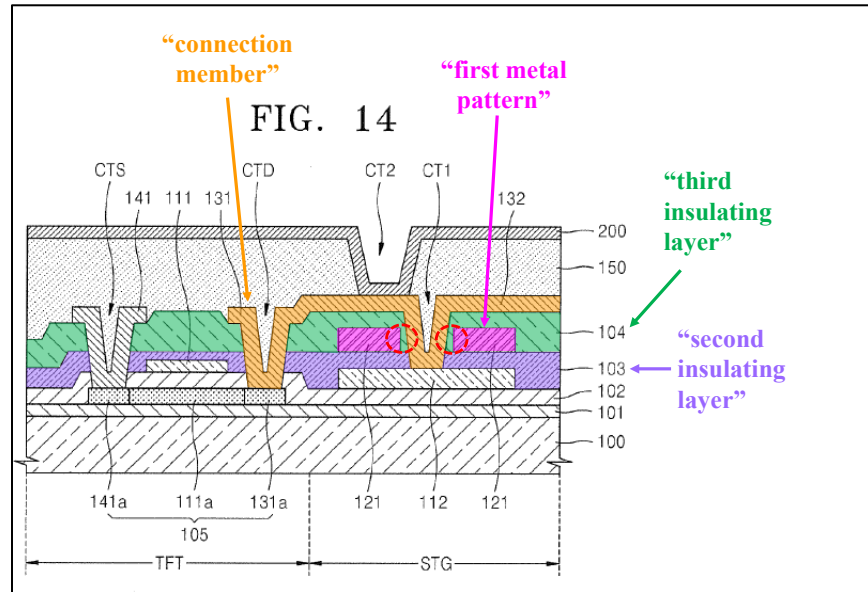
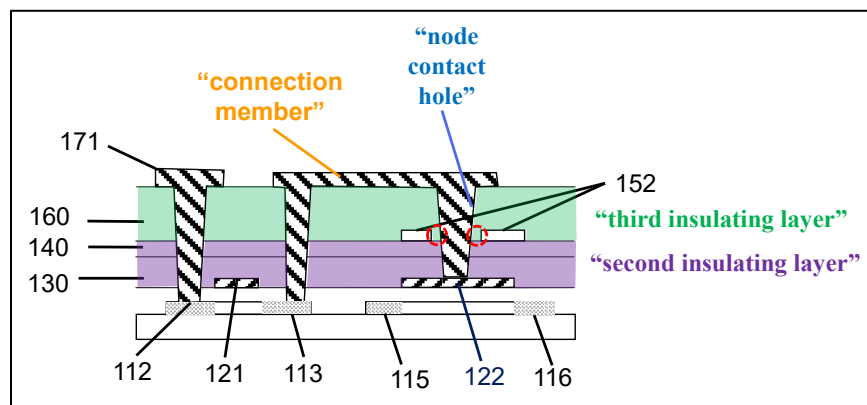
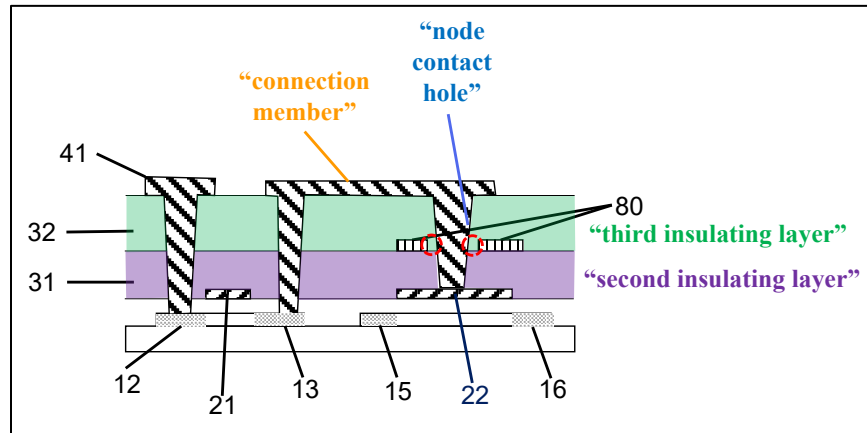


Figure 14 of Zhan (below) shows the **storage electrode 132** (“connection member” (1[g])) is connected with the **storage electrode 112** through the **contact hole CT1** (“contact hole” (3[a])). The first contact hole CT1 “penetrat[es] (or through) the first and second interlayer adjusting layers 103 and 104 at locations ... where the second storage electrode 121 (“first metal pattern”) is not located.” (EX1011, [0050], [0063].) Zhan discloses the first interlayer adjusting layer 103 (“second insulating layer” (1[d])) and the second interlayer adjusting layer 104

(“third insulating layer” (1[f])) contact each other in a region (shown red circles) between second storage electrode 121 (“first metal pattern”) and the *storage electrode 132* in a cross-section view (“connection member” (1[g])). (EX1002, ¶146.)



Park-Zhan discloses the *inter layer 31/130* and *inter layer 140* (“second insulating layer” (1[d])) and *inter layer 32/passivation layer 160* (“third insulating layer” (1[f])) contact each other in a region (position in red circles) between the storage electrode 80/152 (part of the “first metal pattern” (1[e])) and the part of the connection member in a cross-section view. (EX1002, ¶147.)

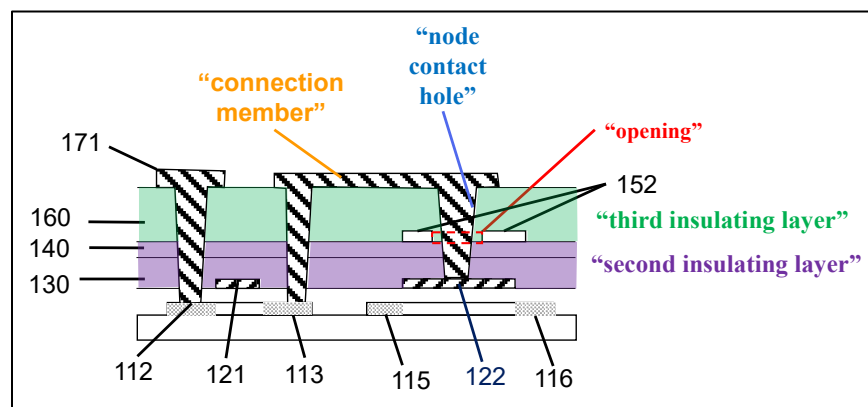
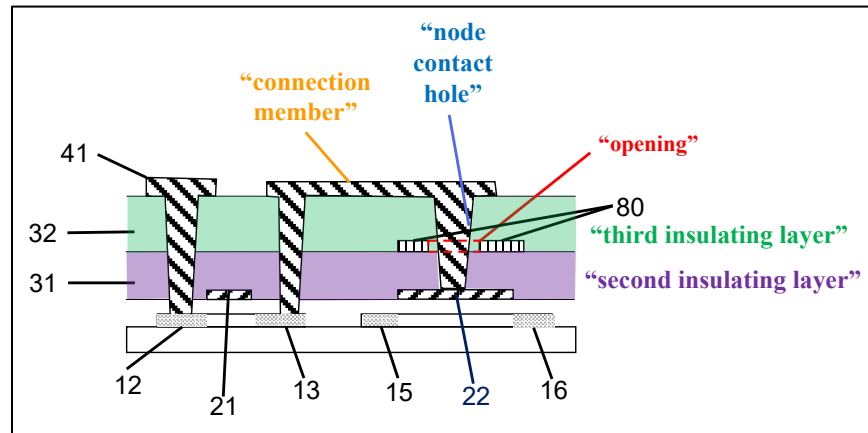


F. Claim 6: “The TFT array substrate of claim 2, wherein an entire area of the opening overlaps the first gate electrode in the plan view.”

Park-Zhan (below) shows an entire area of the hole (“opening” (claim 2)) overlaps the gate electrode 22/122. Zhan discloses (Figure 14 (below)) a “second storage electrode 121 is divided and the first contact hole CTI is disposed between the divided second storage electrodes 121. ... in a plan view, a *hole may be located in the center of the second storage electrode 121.*” (EX1011, [0073].) Even though the figures below show cross-sectional views, it would have been obvious an entire area of the opening overlaps the first gate electrode 22/122 in the

plan view because the hole is located in the center of the capacitor electrode

80/152 (part of the “first metal pattern”). (EX1002, ¶¶148-150.)



G. Claim 22

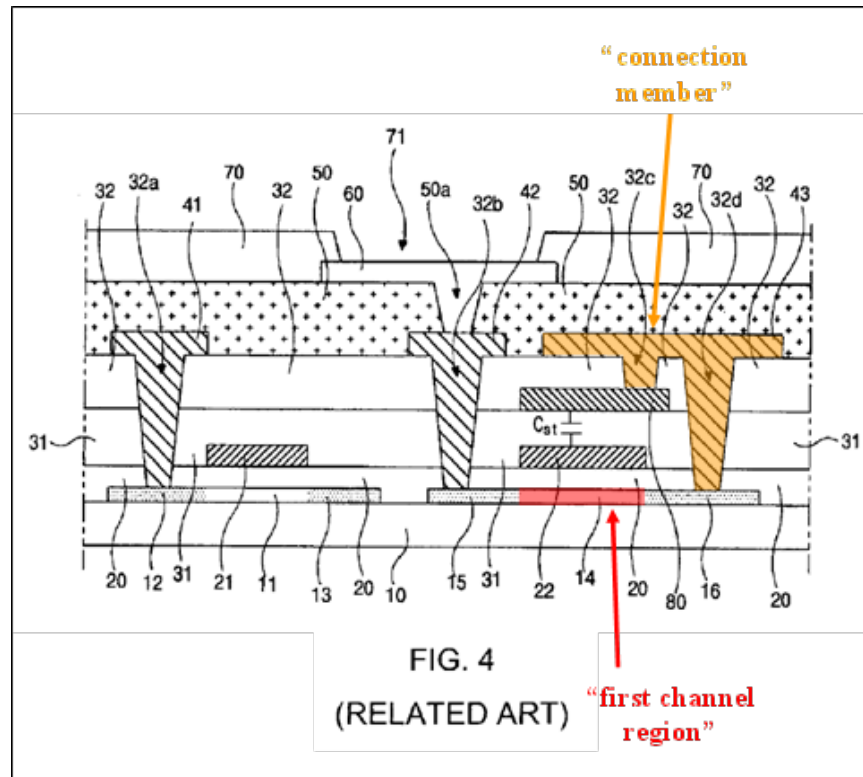
1. Elements 22[pre]-22[g]

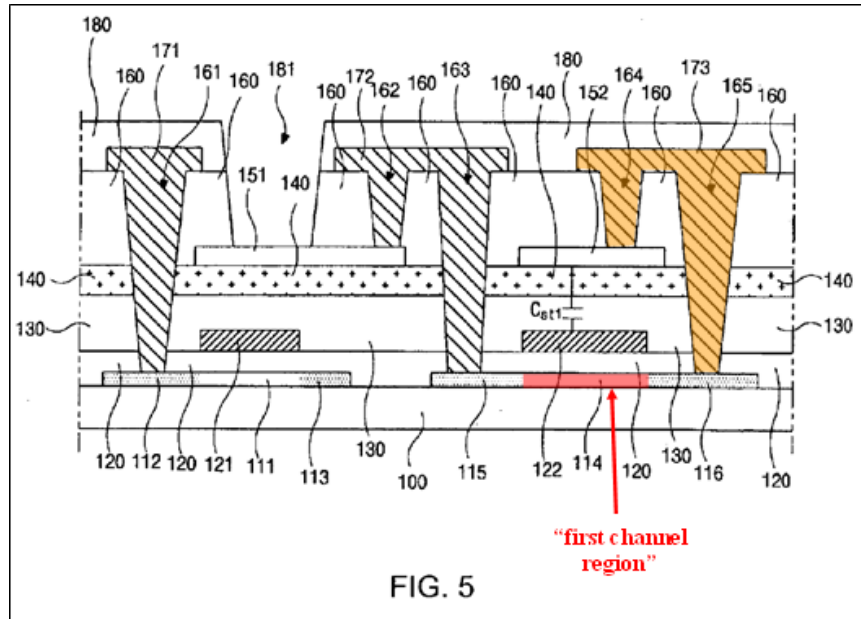
Elements 22[pre]-22[g] are similar to elements 1[pre]-1[g], which Park and/or Zhan teaches. (EX1002, ¶¶151-158.)

2. 22[h]: “the connection member overlapping a portion of the first channel region in a plan view.”

Park teaches a connection member electrically connects the drain of the switching transistor 4 and the gate of the driving transistor 5 (1[g]). Park teaches

source and drain electrodes overlapping with a portion the active layer of the transistors. For example, Figures 4 and 5 (below) show the *source electrode 43/173* located above the gate electrode, overlapping a portion of *active layer 14/114* of the driving transistor 5 in the cross-sectional view. A POSITA would have expected the gate electrode overlaps the channel region in plan view. It was known by a POSITA at the time for the connection member to overlap the channel region. (EX1002, ¶¶159-160.)

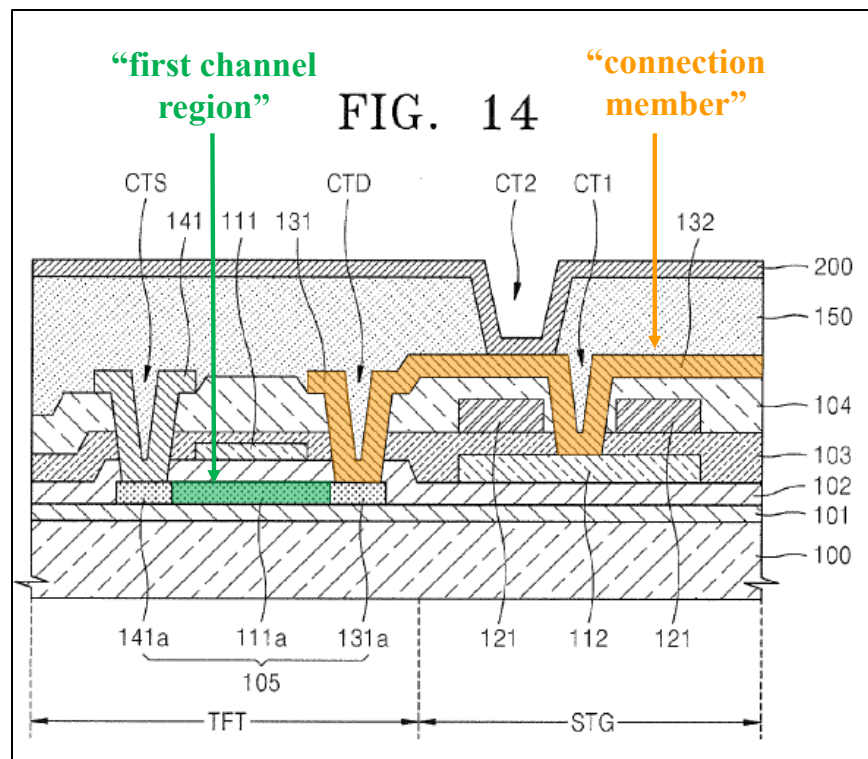




Park describes the structure of the source and drain electrodes with reference to Figure 4 and 5. Then Park refers to the drain of the switching transistor 4 (part of the “connection member”) as “a first drain electrode (not shown), which is connected to the first drain region 113 . . . are also formed on the first passivation layer 160.” (EX1005, [0034], [0007].) This means Figure 4 or 5 represents the structure of the first drain electrode. Because Park states the drain electrode of the switching transistor 4 is “not shown” and “also formed on the inter layer 32/first passivation layer 160,” a POSITA would have understood the drain electrode of the switching transistor 4 (part of the “connection member”) overlaps a portion of the corresponding active layer 114 (“first channel region”) in a plan view. (EX1002, ¶161.)

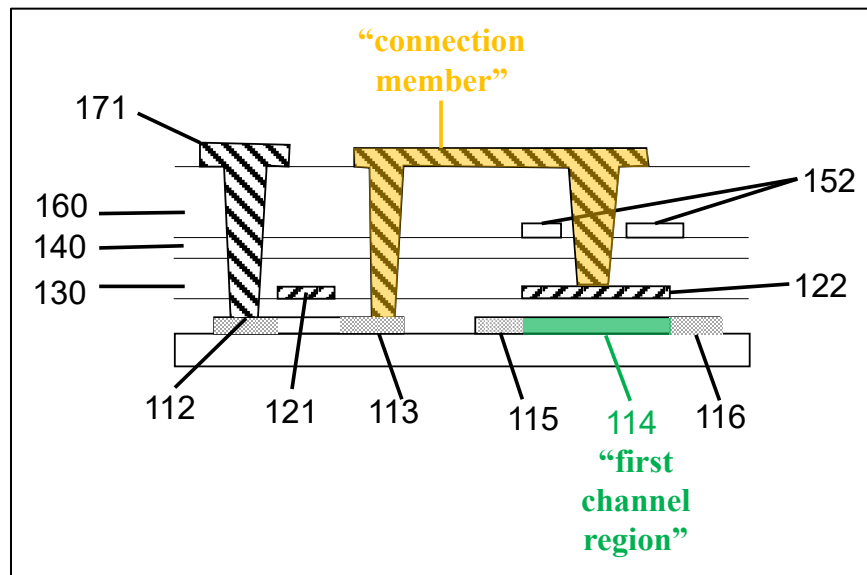
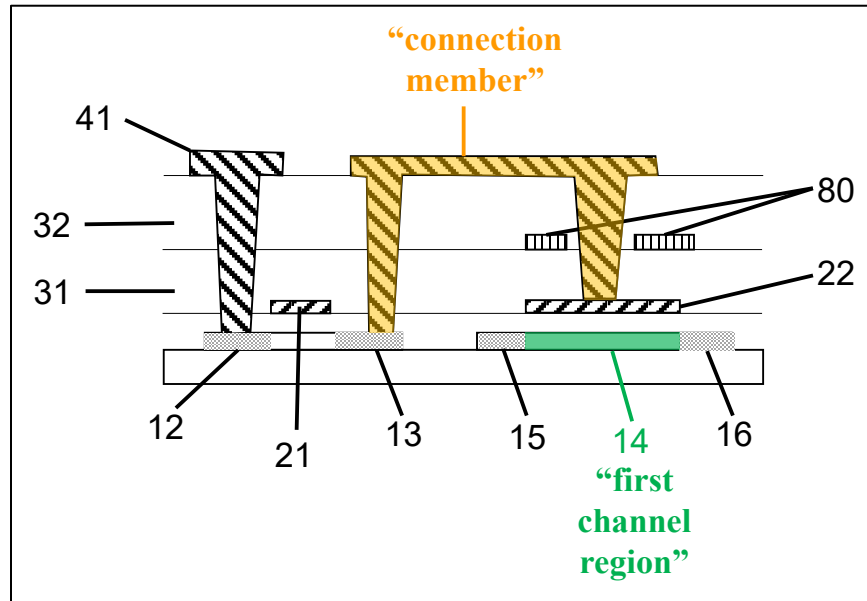
Zhan’s “third storage electrode 132 . . . contacts the first storage electrode

112 through a first contact hole (or first contact unit or opening) CT1 ... the third storage electrode 132 extends from the drain electrode 131 of the TFT.” (EX1011, [0048].) Figure 14 (below) shows the *storage electrode 132* is a connection member that connects the electrode 112 to the *drain electrode 131* of the TFT and overlaps a portion of the *channel area 111a* in a plan view. (EX1011, [0061]; (EX1002, ¶¶162-163.)



Park-Zhan discloses the first drain electrode extends to the storage capacitor to connect with the first gate electrode 22/122, thereby the connection member overlaps the first channel region 14/114 (shown in the figures below). A POSITA would have expected the gate electrode overlaps the channel region in plan view. It was known by a POSITA the connection member overlaps the first channel

region in a plan view. (EX1002, ¶164.)



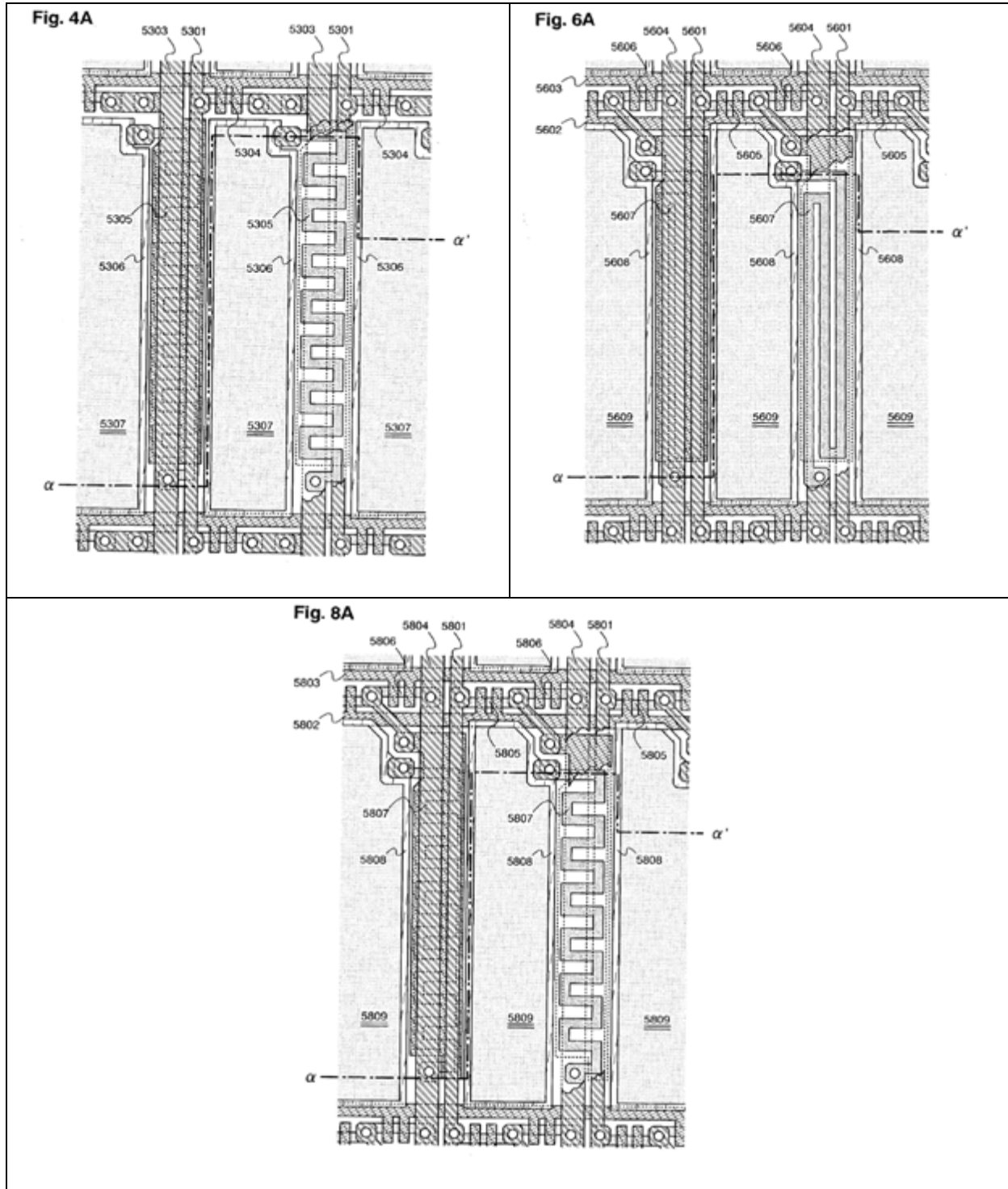
H. Claims 23, 24, And 27

Claims 23, 24, and 27 are similar to claims 2, 3, and 27, which Park and/or Zhan teach. (EX1002, ¶¶165-168.)

VII. GROUND 3: PARK AND OSAME RENDER OBVIOUS CLAIMS 7-10

A. Summary Of Osame

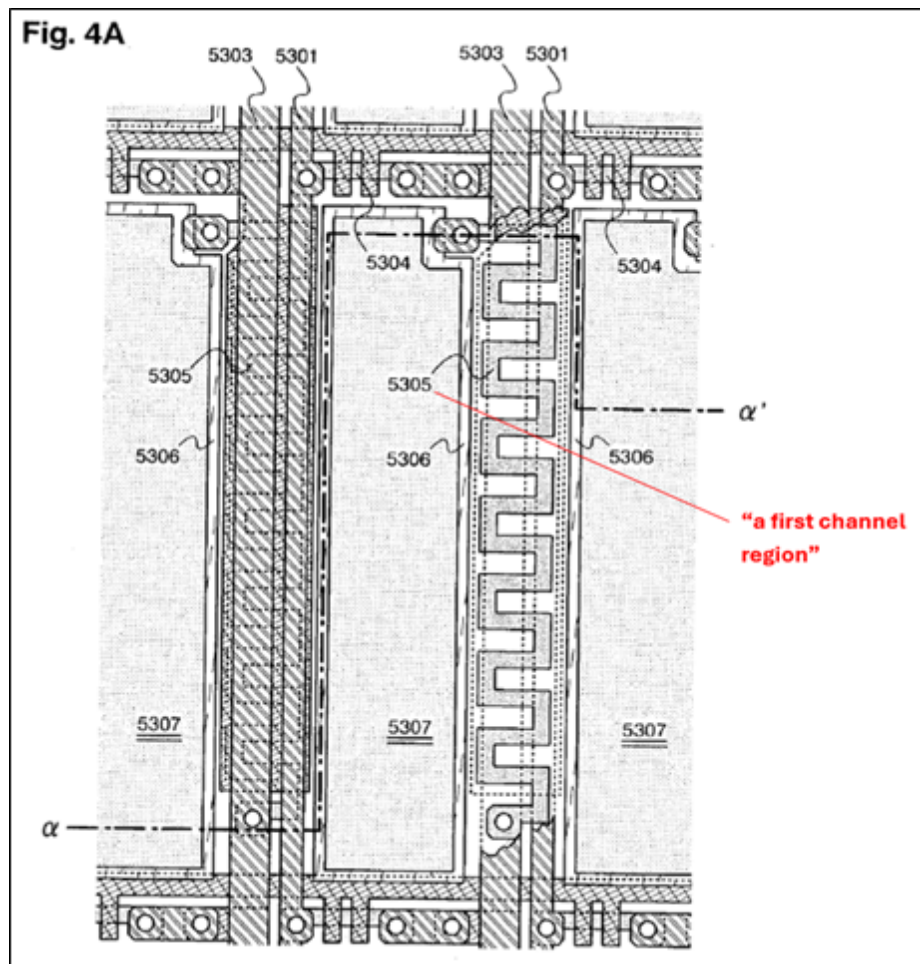
Osame discloses a light-emitting device comprising “a high aperture ratio in which the quality of image is little affected by the variation in the characteristics of TFTs.” (EX1014, Abstract, [0030].) Osame teaches increasing the channel length and the channel width of the driving TFTs to increase the channel capacitance. (EX1014, Abstract, [0007], [0030], [0032].) “[T]he channel lengths of the driving TFTs must be maintained long in the pixels” to promote constant current flow into the EL and avoid changes in brightness. (*Id.*, [0022]-[0029], [0083].) “[T]he aperture ratio decreases as the size of the driving TFT increases.” (*Id.*) Figures 4A, 6A, and 8A (below) show Osame’s shapes. (EX1014, [0114], [0119], [0121]; EX1002, ¶¶169-174.)



B. Claim 7: “The TFT array substrate of claim 1, wherein the first channel region includes a bent portion.”

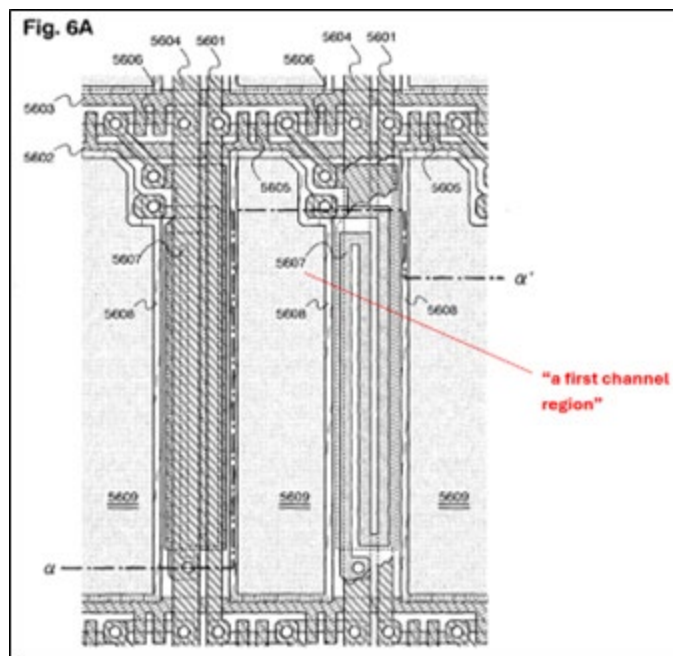
Osame’s “semiconductor layer may be formed in a meandering shape in the

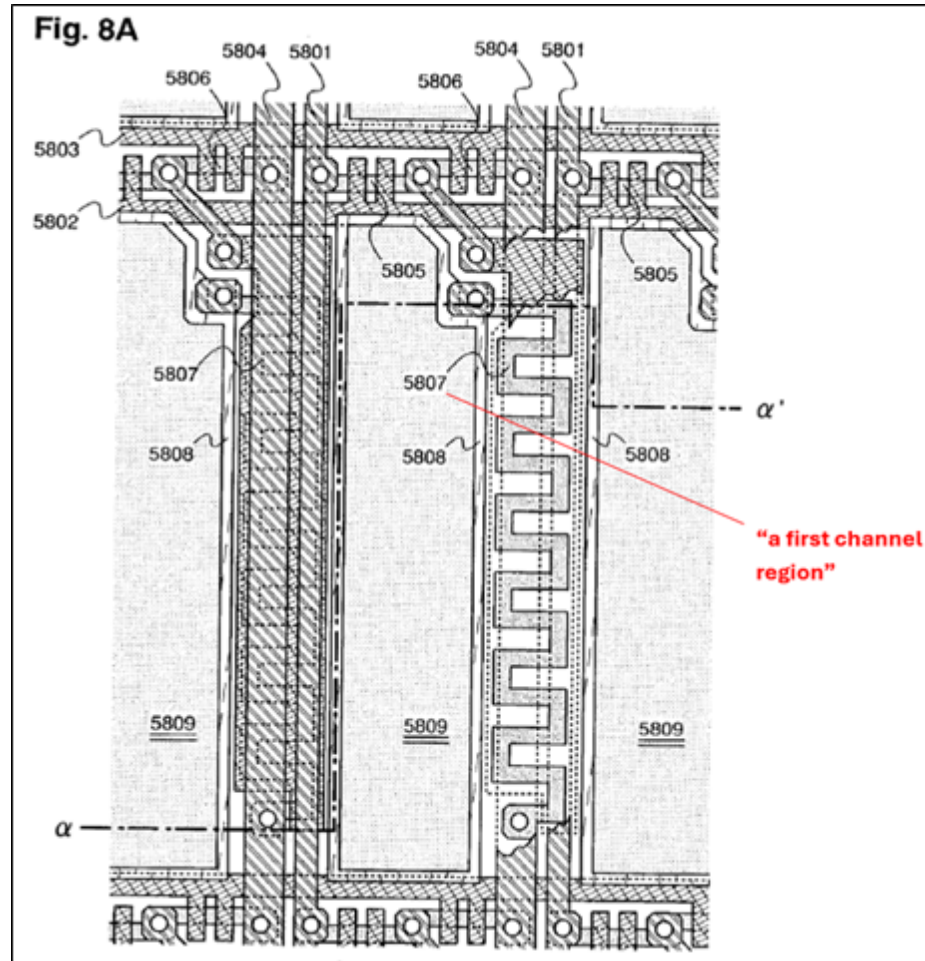
horizontal direction as represented by the driving TFT 5305” (Figure 4A (below)). (EX1014, [0114].) “[T]he meandering has a meaning of ‘flowing in a winding manner’, and the meandering shape stands for that the shape of the semiconductor layer is meandering.” (EX1014, [0114].) “[T]he channel length of the driving TFT 5305 can be further increased and the channel width can be further increased and the channel width can be increased to some extent without decreasing the aperture ratio.” (*Id.*; EX1002, ¶¶175-177.)



Figures 6A and 8A (below) have meandering shapes and configurations.

(EX1014, [0119], [0121]; EX1002, ¶¶178-181.)





1. Motivation to combine Park and Osame

It would have been obvious to a POSITA to combine the teachings of Park and Osame. Park and Osame are from the same field of endeavor because they both relate to light-emitting devices and associated configurations. Park and Osame are pertinent to the same technical problem of increasing aperture ratio without compromising image quality based on the same pixel circuit having two transistors and one storage capacitor. (EX1005, Fig.1, [0006]; EX1014, Fig.12, [0007].) Park discloses an ELD device “in which a storage capacitance of a

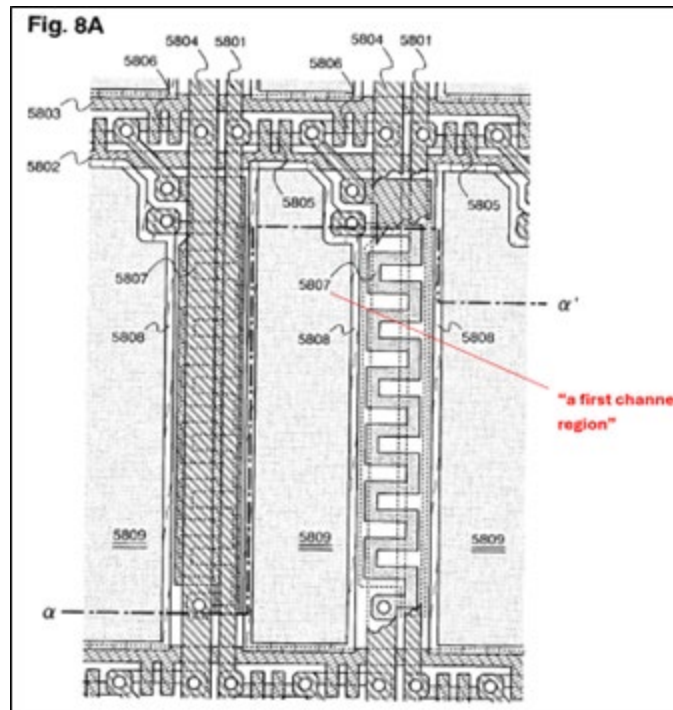
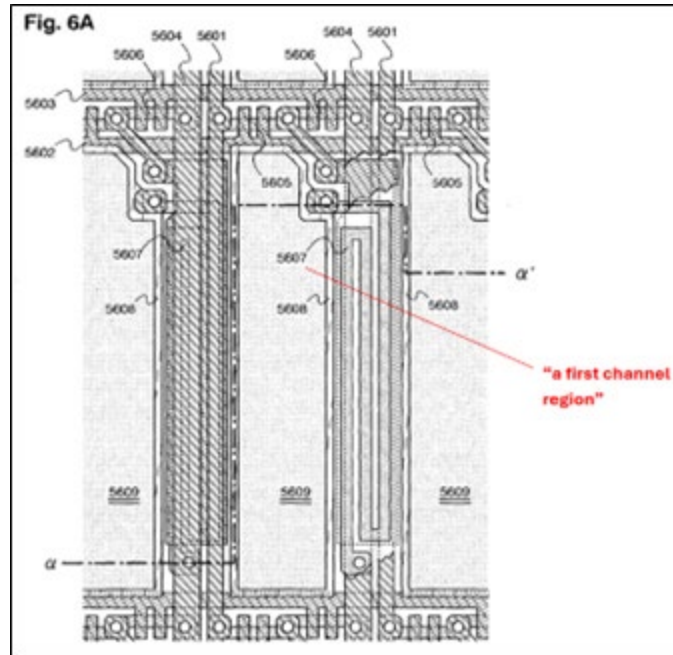
storage capacitor is increased without reducing an aperture ratio and number of masks needed is reduced.” (EX1005, [0017].) The storage capacitor is disposed above the transistor and the gate electrode 22/122 forms the storage capacitor electrode to increase the storage capacitance without reducing an aperture ratio. (EX1005, [0007], [0011], [0015], [0034].) Osame discloses a “light-emitting device which realizes a high aperture ratio and in which the quality of image is little affected by the variation of the driving TFTs.” (EX1014, [0030].) The capacitance between the gate electrode and the current supply line of the driving TFT can be utilized as part of the holding capacitor C_s and the channel capacitance is utilized as C_s between the gate electrode and the channel region to realize a high aperture ratio. (EX1014, Abstract, [0082], [0083], [0089], [0097], [00105].) Park and Osame disclose similar devices. (EX1002, ¶182.)

Osame teaches using semiconductor layers of different shapes in light-emitting devices to increase TFT channel length and width without decreasing aperture ratio. Increasing the TFT channel length “improve[s] current characteristics in the saturated region, and a high V_s is applied to the driving TFTS to obtain a desired drain current. Therefore, the drain currents of the driving TFTs are little affected by the variation in the threshold voltage.” (EX1014, Abstract, [0087].) Variation in the driving TFT may negatively affect the brightness of the EL elements, and increasing the channel length improves the performance of the

light-emitting device. (EX1014, [0088].) The Park-Osame combination involves use of a known technique (increasing the TFT channel length as taught by Osame) to improve a similar device (Park) in the same way. A POSITA would have a reasonable expectation of success in combining Osame's features with the teachings of Park to generate an improved display device with driving TFTs having little to no variation in the drain current. It would have been obvious because Osame's teaching is a simple substitution of a known element (a channel length with a meandering shape (*see, e.g.*, EX1015, Fig. 9)) to obtain the predictable result of increasing the channel length without decreasing the aperture ratio. (EX1002, ¶¶183-184.)

C. Claim 8: "The TFT array substrate of claim 7, wherein the first channel region includes at least two bent portions."

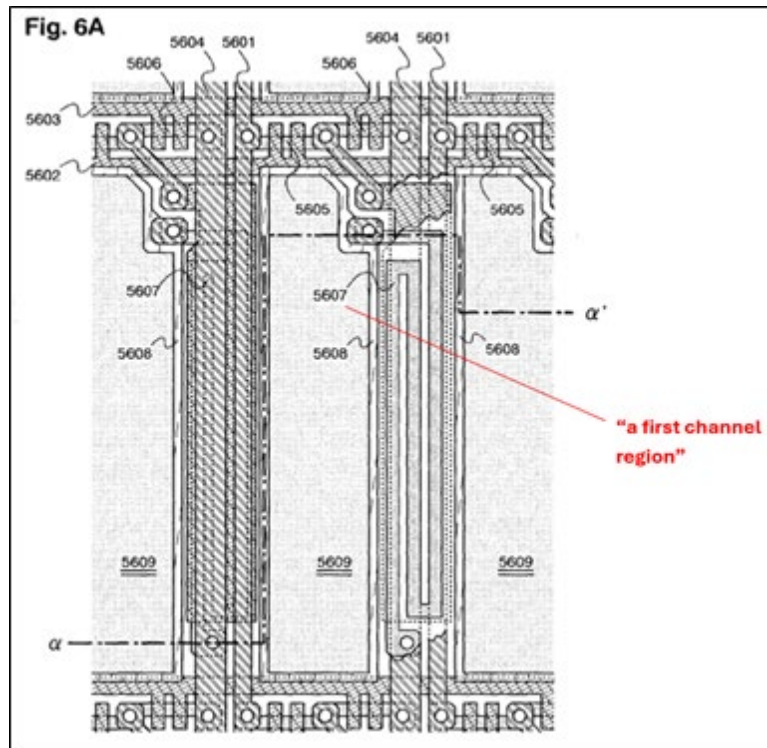
Osame discloses at least two bent portions in the channel of the driving TFTs (Figures 4A, 6A, and 8A (below)). (EX1014, [0114], [0119], [0121]; EX1002, ¶¶185-189.) Park's first channel region is similarly the channel of the driving transistor. (*See* 1[b].)



It would have been obvious to a POSITA to combine the teachings of Park and Osame. (See claim 7.)

D. Claim 9: “The TFT array substrate of claim 7, wherein the first channel region is curved in an ‘S’ shape.”

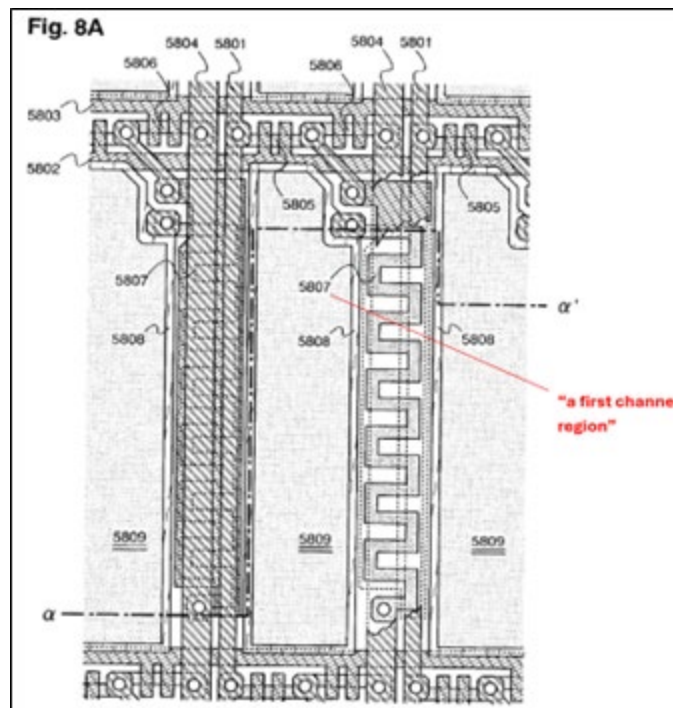
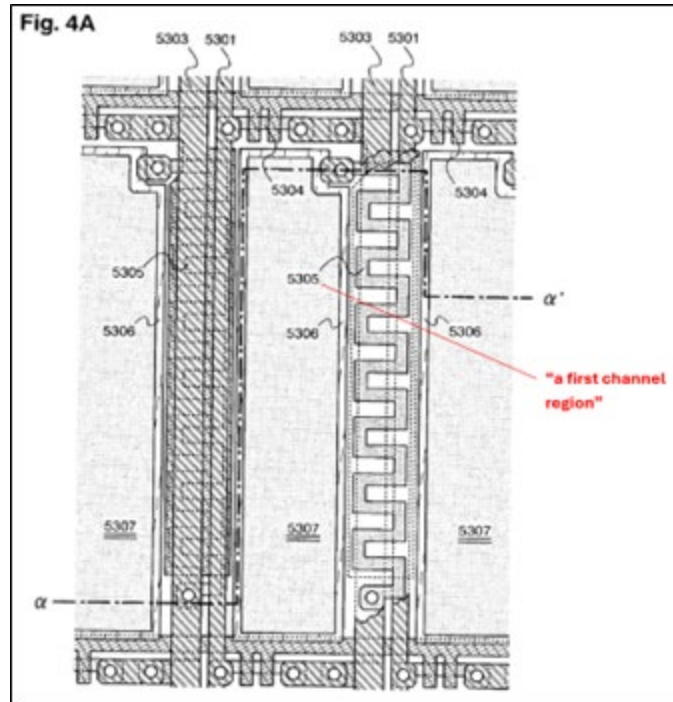
Osame’s Figure 6A (below) shows the channel of the driving TFT 5807 is curved in an ‘S’ shape. (EX1014, [0119]; EX1002, ¶¶190-192.)



It would have been obvious to a POSITA to combine the teachings of Park and Osame. (See claim 7 .)

E. Claim 10: “The TFT array substrate of claim 7, wherein the first channel region is curved in a zigzag shape.”

Osame’s Figures 4A and 8A (below) show the channel of the driving TFTs are curved in a zigzag shape. (EX1014, [0114], [0121]; EX1002, ¶¶193-196.)



It would have been obvious to a POSITA to combine the teachings of Park and Osame. (See claim 7.)

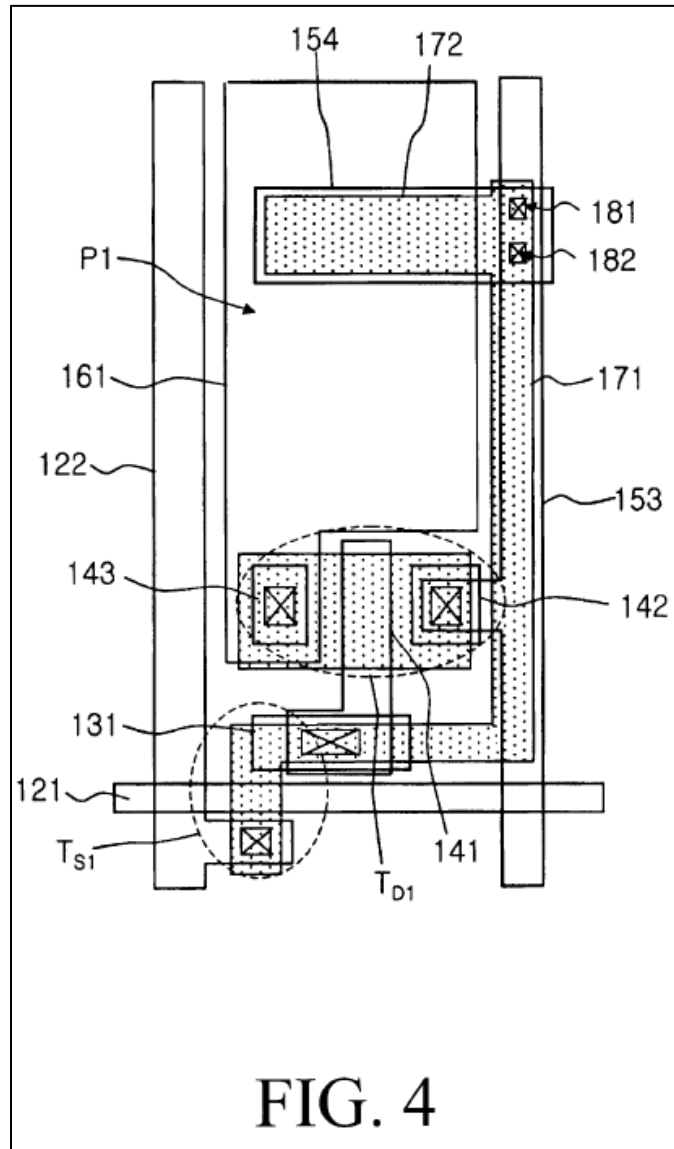
VIII. GROUND 4: PARK, ZHAN, AND OSAME RENDER OBVIOUS CLAIMS 25 AND 26

Claims 25 and 26 are similar to claims 7 and 10, which Osame teaches. (EX1002, ¶¶197-198.) The combination of Park, Zhan, and Osame teach claims 25 and 26.

IX. GROUND 5: PARK AND KO RENDER OBVIOUS CLAIMS 12 AND 13

A. Summary Of Ko

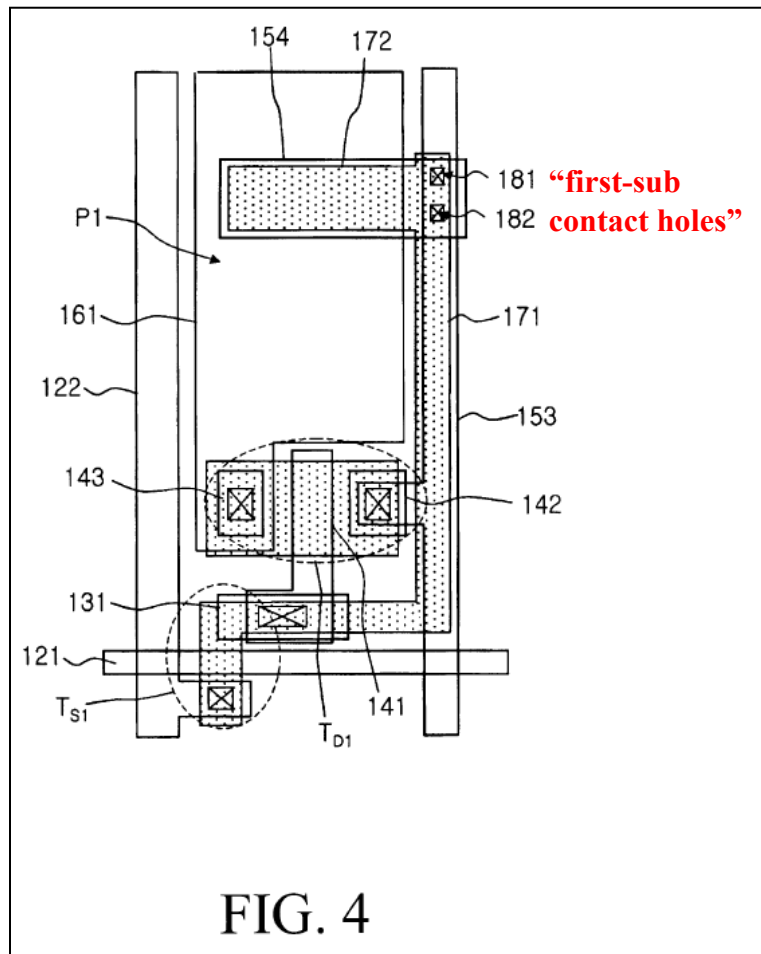
Ko discloses an active matrix organic ELD device. (EX1009, 1:12-15.) “Because the power line 153 is formed of an opaque material, and the first capacitor electrode 154 is formed of transparent conductive material, in the active matrix organic electroluminescence display device ..., an electrical resistance of the power line is decreased and, an aperture ratio is increased at the same time.” (EX1009, 7:44-50.) Figure 4 (below) shows the power line 153, first capacitor electrode 514, and first and second contact holes 182 and 182 formed and connecting where the first capacitor electrode 154 and power line 153 overlap each other. (EX1009, 7:38-43; EX1002, ¶199.)



B. Claim 12: “The TFT array substrate of claim 11, wherein the first contact hole includes a plurality of first-sub contact holes.”

Figure 4 (below) of Ko show “*first and second contact holes 181 and 182* [] formed at a portion where the first capacitor electrode 154 and the power line 153 overlap one another. The first capacitor electrode 154 is connected to the power line 153 through the first and second contact holes 181 and 182.” (EX1009,

7:38-43; EX1002, ¶¶200-201.)



It would have been obvious to a POSITA to combine the teachings of Park and Ko. Park and Ko are from the same field of endeavor, both relating to light-emitting devices comprising lines such as power, data, and gate lines. Park and Ko disclose “an active matrix organic electro luminescent display [] device” including a switching transistor 4, driving transistor 5, storage capacitor 6, LED 7, power line 3, data line 2, gate line 1, and contact holes. (EX1005, [0006], [0007], [0034], Figs. 1, 4, and 5; EX1009, 2:1-20, 7:38-43; EX1002, ¶202.)

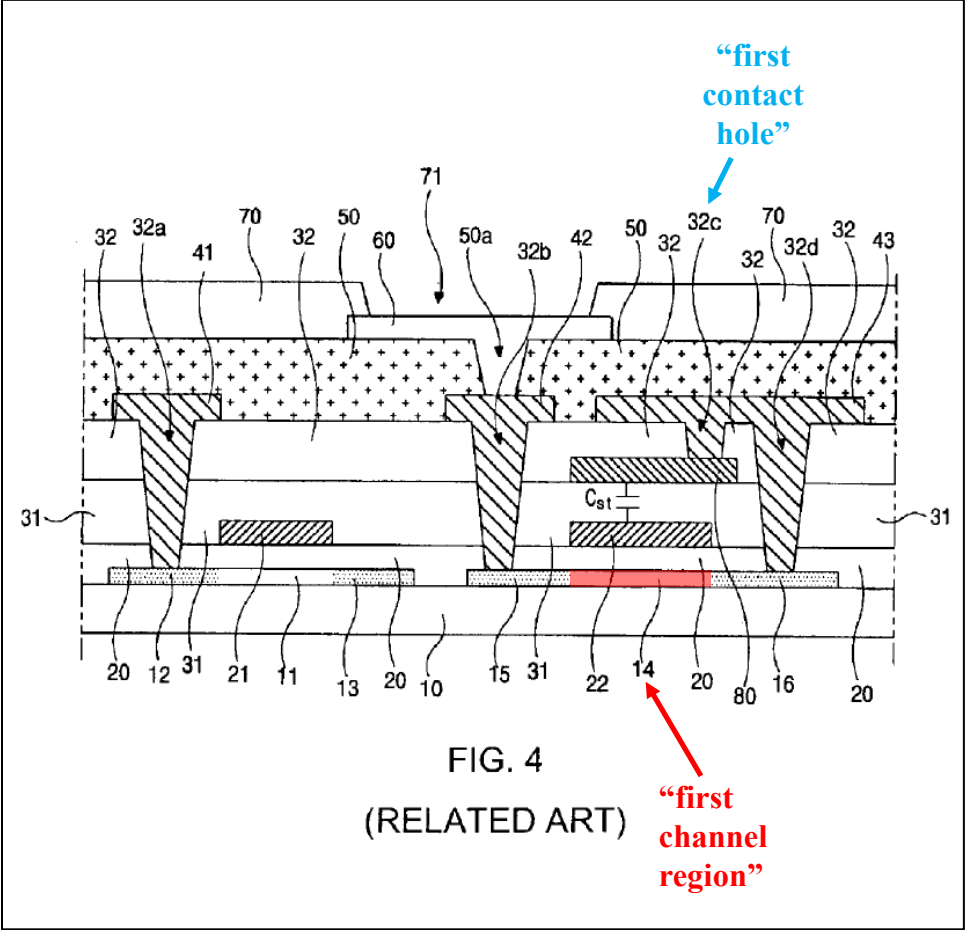
Park teaches displaying high quality images by increasing the storage capacitance without decreasing aperture ratio. (EX1005, [0015].) Ko teaches decreasing the electrical resistance of the power line and increasing the aperture ratio to improve the picture quality of the displayed images. (EX1009, 7:44-50, 9:50-58.) Ko explains “a picture quality of displayed images may be deteriorated due to an increased resistance of a wiring.” (EX1009, 7:18-20.) Ko’s ELD device improves upon the performance and quality of the light-emitting display devices by comprising a power line 153 formed of an opaque metal material and a first capacitor electrode 154 formed of a transparent conductive material. The power line 153 and first capacitor electrode 154 overlap one another and connect to each other through first and second contact holes 181 and 182. (EX1009, 7:33-43; EX1002, ¶203.)

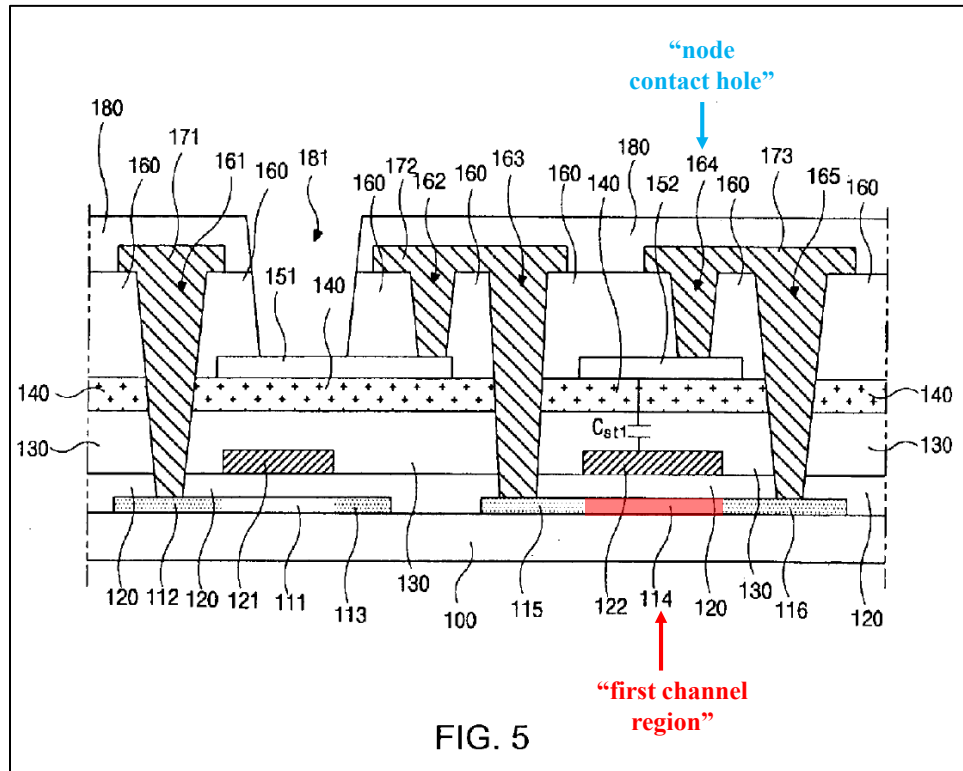
Ko’s technical features may be combined with the teachings of Park to generate an OLED with improved performance and quality by increasing aperture ratio and decreasing the resistance of the wiring. Ko and Park have similar circuits. Ko’s circuit comprises a capacitor 6 including an upper electrode and a lower electrode connected to the drain of a switching transistor 4 and the gate of a driving transistor 5. (EX1009, 2:10-13, Fig. 1.) The circuits of both Ko and Park include: the gate of the switching transistor 4 is connected to the gate line 1, and the source is connected to the data line 2. The drain of the switching transistor 4 is

connected to the gate of the driving transistor 5. The drain of the driving transistor 5 is connected to an anode electrode of the LED 7. The source electrode of the driving transistor 5 is connected to a power line 3, and a cathode electrode of the LED 7 is grounded. A storage capacitor 6 is connected to the gate and the source of the driving transistor 5. (EX1009, 2:9-20; EX1005, [0006], Fig. 1.) Given the overlap between Park and Ko, and the prior art had already known and demonstrated such techniques with success, there would have been a reasonable expectation of success. (EX1002, ¶204.)

C. Claim 13: “The TFT array substrate of claim 12, wherein at least one of the plurality of first-sub contact holes overlaps the first channel region in a plan view.”

Park’s contact hole 32c/164 (“first contact hole” (claim 11)) overlaps with the active layer 14/114 (“first channel region” (1[b])) (Figures 4 and 5 (below)). (EX1005, [0015]; EX1002, ¶¶205-207.)





X. GROUND 6: PARK, ZHAN, AND KO RENDER OBVIOUS CLAIMS 28, AND 29

Claims 28 and 29 are similar to claims 12 and 13, which Ko teaches. The combination of Park, Zhan, and Ko teach claims 28 and 29. (EX1002, ¶¶208-209.)

XI. GROUND 7: PARK AND KWON RENDER OBVIOUS CLAIMS 17-20

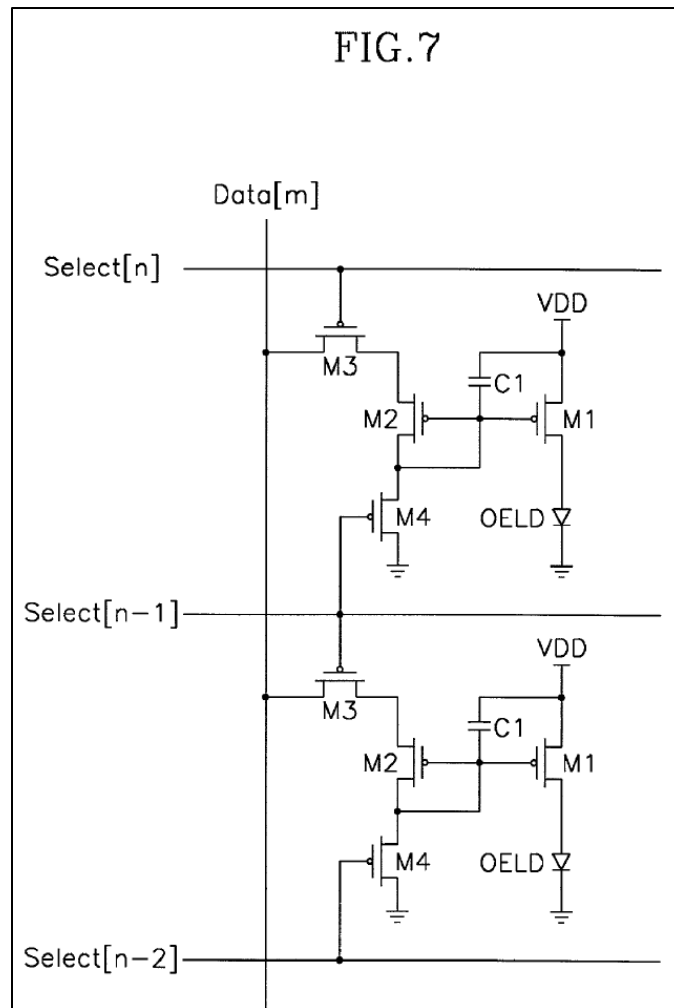
A. Summary Of Kwon

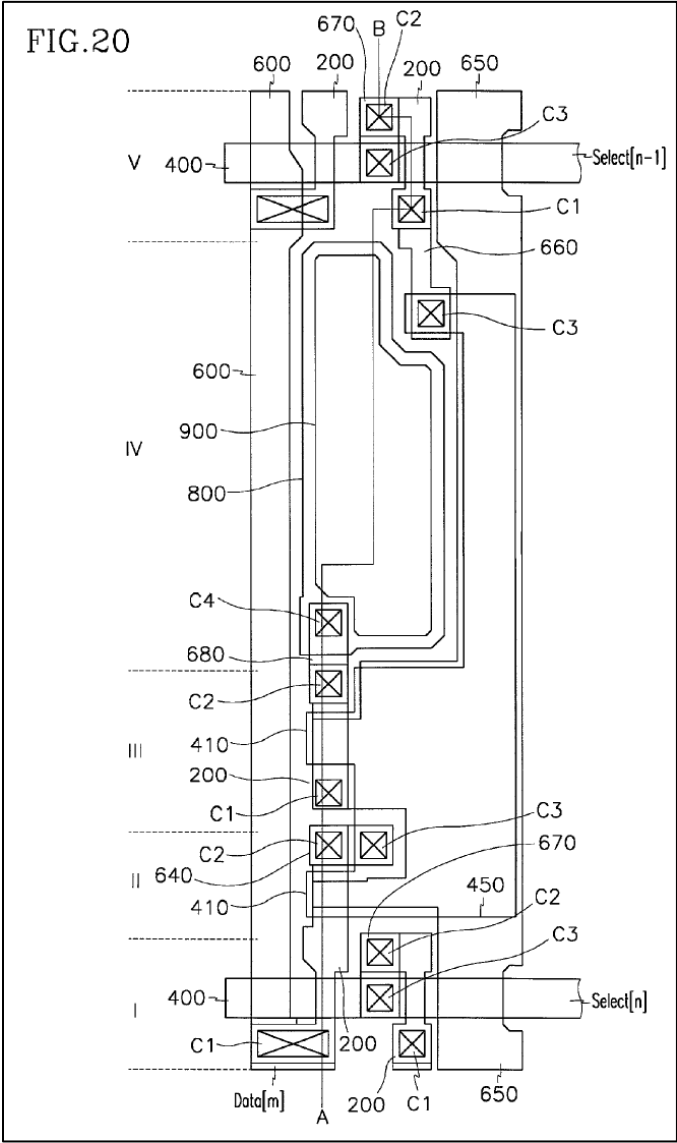
Kwon discloses “an organic EL display (OELD) ... and a pixel circuit that can compensate for deviation of the threshold voltage of a thin film transistor (TFT) and achieve high gray scale display when driving the pixels of the OELD using the TFT.” (EX1006, [0002].) Kwon explains “it is difficult for the conventional pixel circuit to achieve high gray scale because the threshold voltage

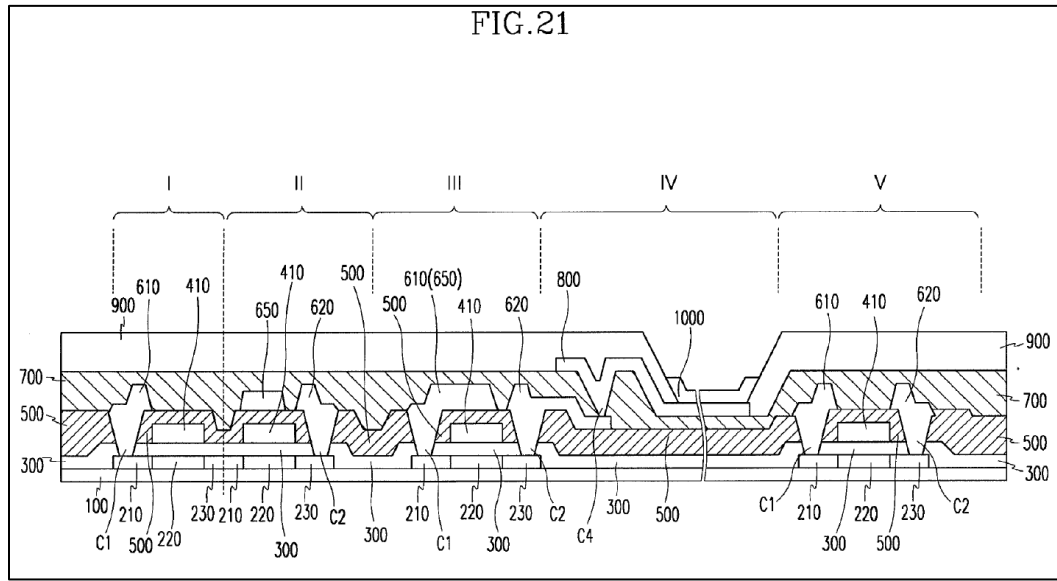
V_{TH} of the TFT varies depending on the manufacturing process thereof.”

(EX1006, [0011].) Kwon “provide[s] an OLED for compensating for deviations of the threshold voltage of the TFT and displaying high gray scale.” (EX1006, [0012]; EX1002, ¶210.)

Figures 7, 20, and 21 (below) show the pixel circuit, and plan and cross-sectional views of the OLED of Kwon. (EX1002, ¶211.)



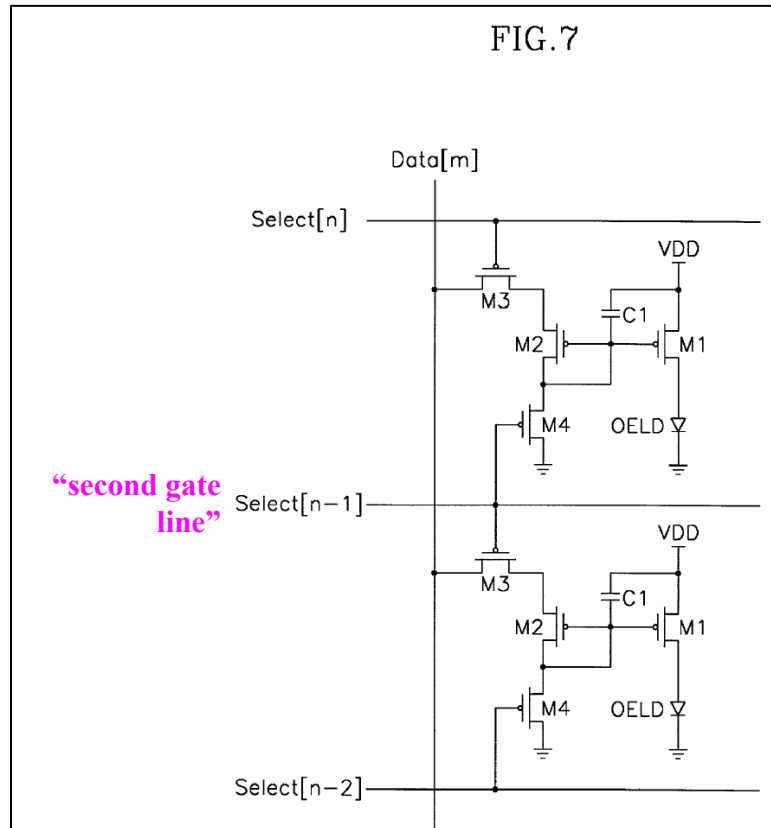




A. Claim 17

1. 17[a]: “The TFT array substrate of claim 14, further comprising a second gate line, and”

Park’s gate line 1 electrically connects to the gate electrode of the switching transistor 4. (EX1005, [0006].) To the extent that Park does not teach the claimed “second gate line,” Kwon discloses “an external reset signal Reset is supplied to the gate of the transistor M4 to initialize the node A into a ground level.” (EX1006, [0060].) Kwon’s pixel circuit (Figure 7 (below)) comprises a “Select Signal Select[n-1] of the previous Scan line instead of an additional external reset Signal Reset, [that] supplies the select signal Select[n-1] to the gate of the transistor M4,” thereby turning the transistor M4 on in response to a previous signal on *Select[n-1] line* (“second gate line”). (EX1006, [0063]; EX1002, ¶¶212-213.)



It would have been obvious to a POSITA to combine the teachings of Park with Kwon. Both disclose EL display devices and pixel circuits having transistors for operating such devices. (EX1005, [0017]; EX1006, [0002].) Park and Kwon are in the same field of endeavor. (EX1002, ¶214.)

Park’s pixel circuit comprises “a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a [] (LED) 7.” (EX1005, [0006].) Kwon’s “pixel circuit comprises a current supplying transistor M1 and a threshold voltage compensation transistor M2 of PMOS transistors, and switches S1 and S2 of PMOS transistors M3 and M4.” (EX1006, [0056]; EX1002, ¶214.)

Kwon explains “it is difficult for the conventional pixel circuit to achieve high gray scale because the threshold voltage V of the TFT varies depending on the manufacturing process thereof.” (EX1006, [0011].) A POSITA would have understood Park’s teachings similarly apply to a conventional pixel circuit. (EX1005, Fig. 1 (“Related Art”).) Kwon’s “pixel circuit [] can compensate for deviation of the threshold voltage of a thin film transistor (TFT) and achieve high gray scale display when driving the pixels of the OLED by using the TFT.” (EX1006, [0002].) It comprises an additional transistor M4 that resets the gate voltage of the driving transistor M1 and a threshold voltage compensation transistor M1 to achieve high gray scale display. (EX1006, [0056]-[0057].) Kwon’s technical features may be combined with the teachings of Park to generate a display device with high gray scale display by including circuitry in the pixel circuit to compensate for any deviations in the threshold voltage of the driving TFT. The Park-Kwon combination results in a display device with high gray scale display. There would have been a reasonable expectation of success because such techniques were known in the prior art, have been successfully demonstrated, and because there is an overlap between Park and Kwon including with their circuits and use for active matrix display devices. (EX1002, ¶215.)

Because Park and Kwon have similar circuits, a POSITA would have been motivated to use the technique disclosed in Kwon to improve the similar devices of

Park in the same way. It would have been obvious to a POSITA to combine Park and Kwon. (EX1002, ¶215.)

- a. 17[b]: “a third thin film transistor, the third thin film transistor including a third gate electrode and a third channel region overlapping the third gate electrode, the third gate electrode and the third channel region being spaced apart from each other with the first insulating layer therebetween, and”

Kwon’s pixel circuit of Figure 7 (below) comprises a *transistor M4*.

(EX1006, [0063]; EX1002, ¶216.)

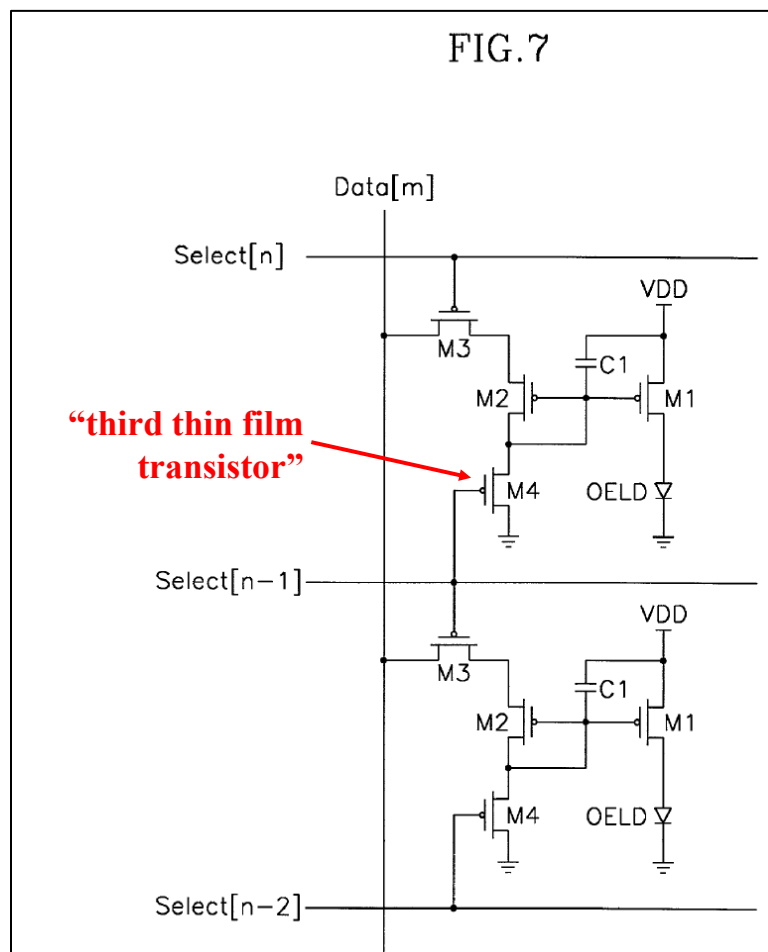
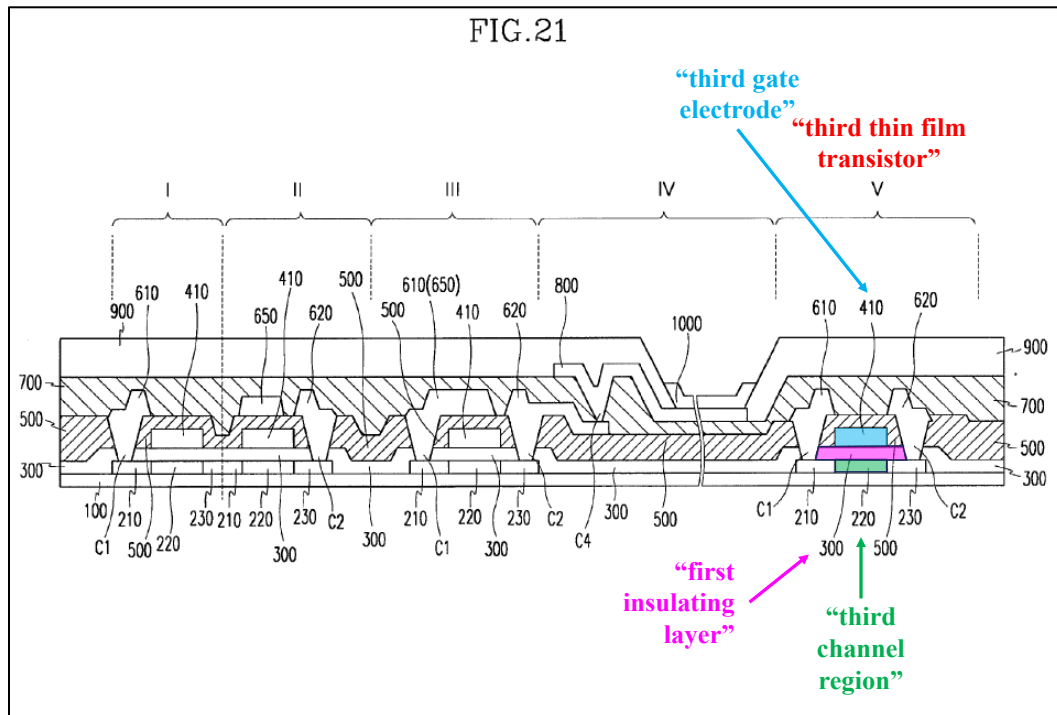


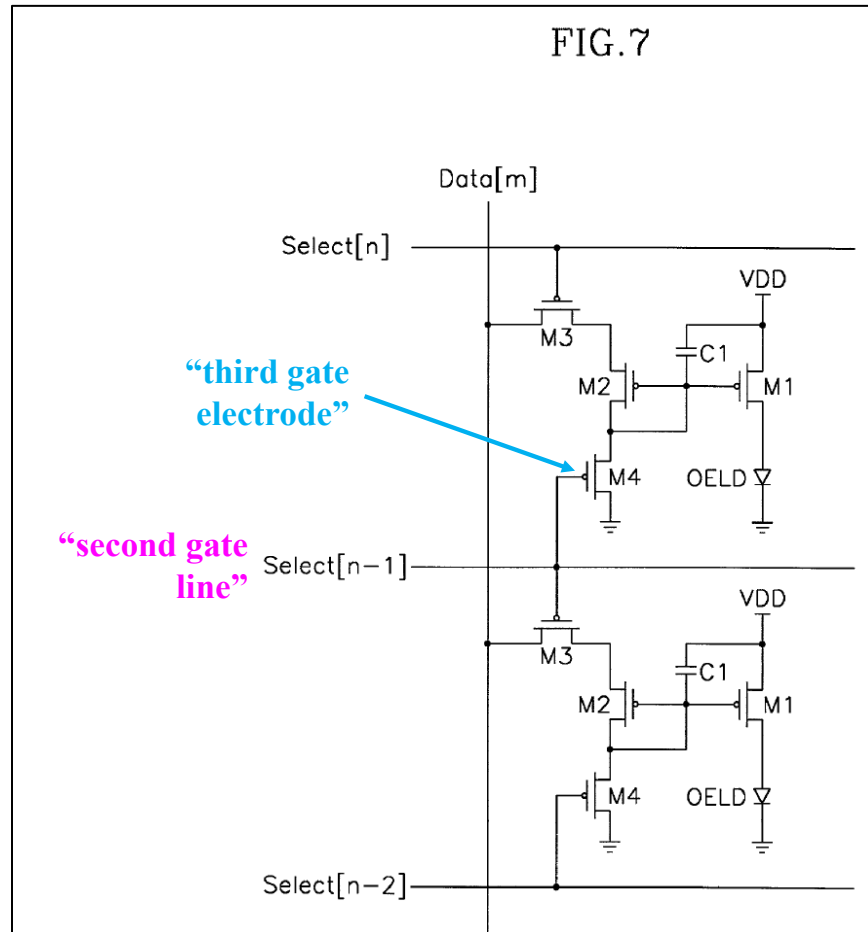
Figure 21 (below) of Kwon shows a cross-sectional layout of *transistor M4*

including a *gate electrode 410* and a *channel region 220* in region V. (EX1006, [0091], [0094].) The channel region 220 overlaps the gate electrode 410, and the gate electrode 410 and the channel region 220 are spaced apart from each other with the *gate insulation layer 300* therebetween. (EX1002, ¶217.)



2. 17[c]: “wherein the second gate line is electrically connected to the third gate electrode.”

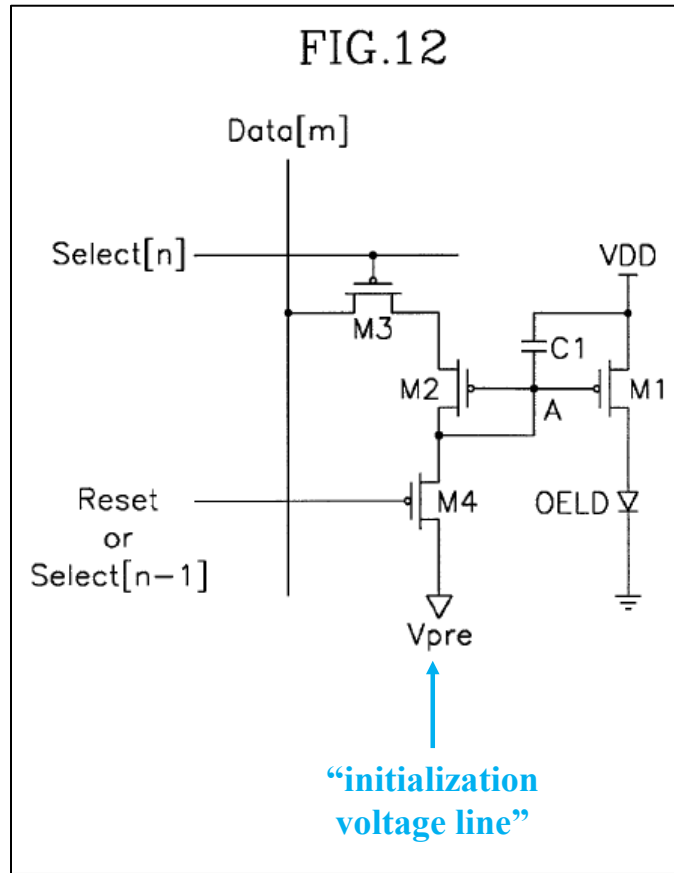
Figure 7 (below) shows the *Select[n-1] line* (“second gate line” (17[a])) is electrically connected to the gate of *transistor M4* (“third gate electrode” (17[b])). (EX1002, ¶¶218-220.)



A. Claim 18

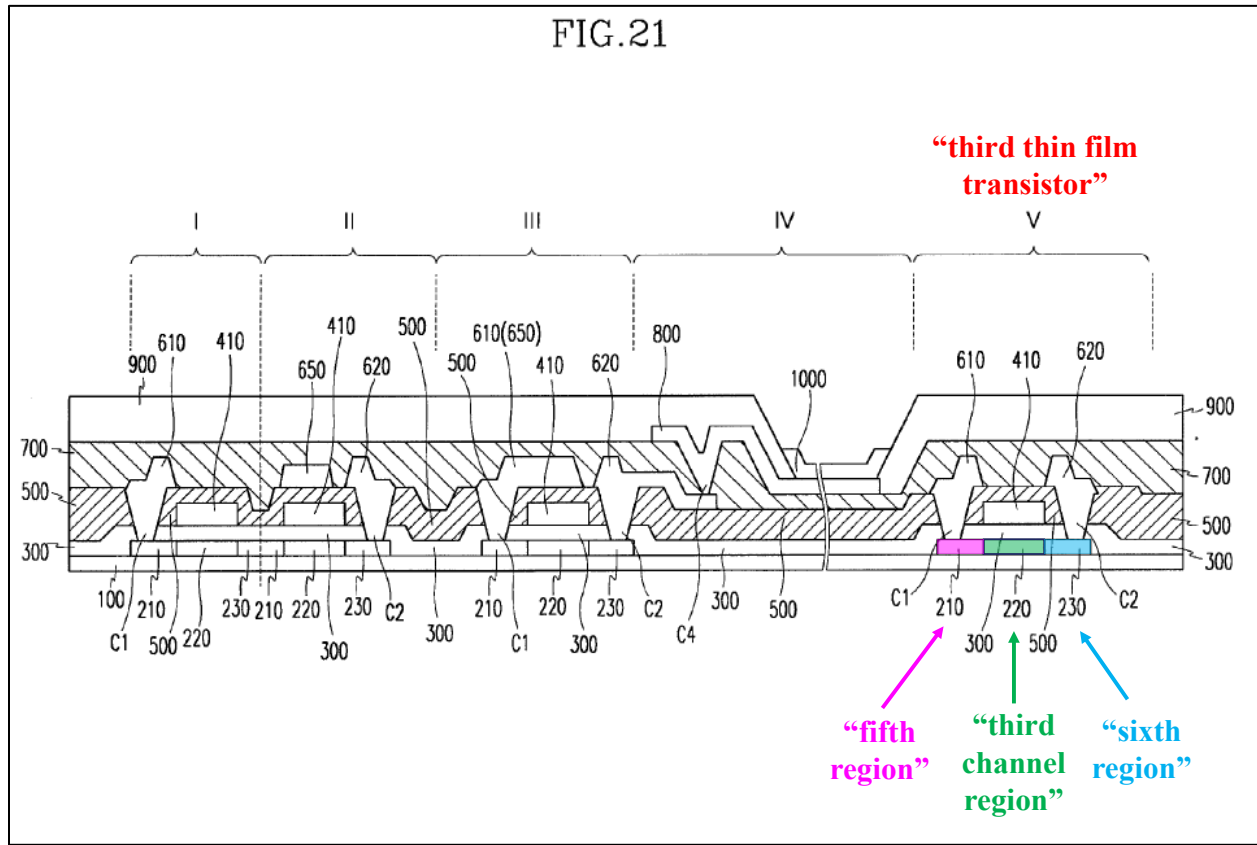
1. 18[a]: "The TFT array substrate of claim 17, further comprising a[n] initialization voltage line,"

Kwon discloses a "current flowing to ... the *pre-charge voltage [Vpre]* from the node A via the transistor M4 is constant, and accordingly, the reset operation can be quickly performed" (Figure 12 (below)). (EX1006, [0078]; EX1002, ¶¶220-221.)



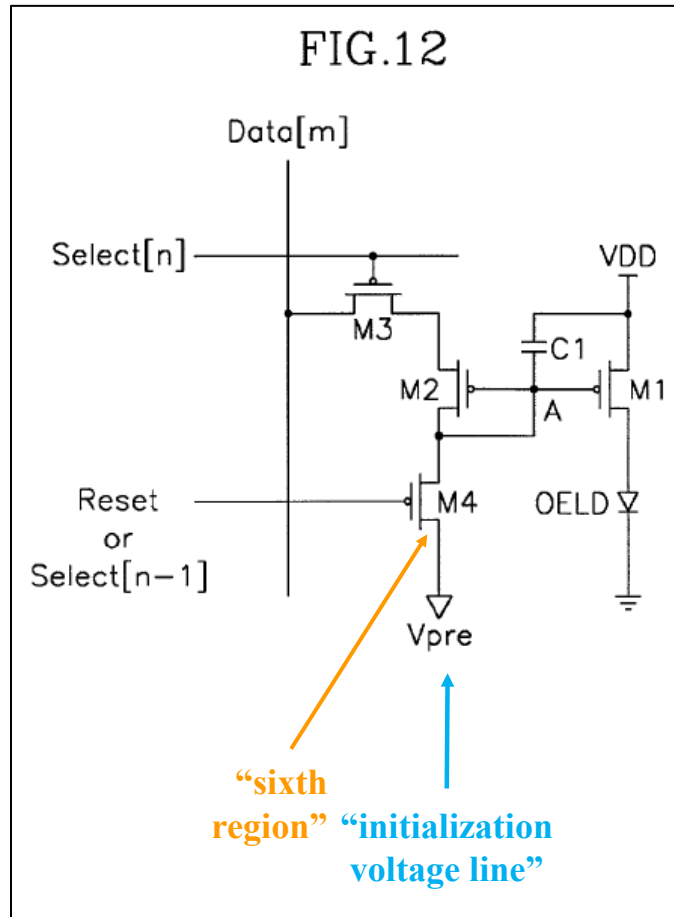
- a. 18[b]: “wherein the third thin film transistor further comprises a fifth region adjacent to a side of the third channel region and a sixth region adjacent to another side of the third channel region, and”

Figure 21 (below) of Kwon shows *transistor M4* (“third thin film transistor” (17[b])) comprising a *source region 210* adjacent to a side of the *channel region 220* and a *drain region 230* adjacent to another side of the channel region 220. (EX1006, [0094], [0098]; EX1002, ¶¶222-224.)



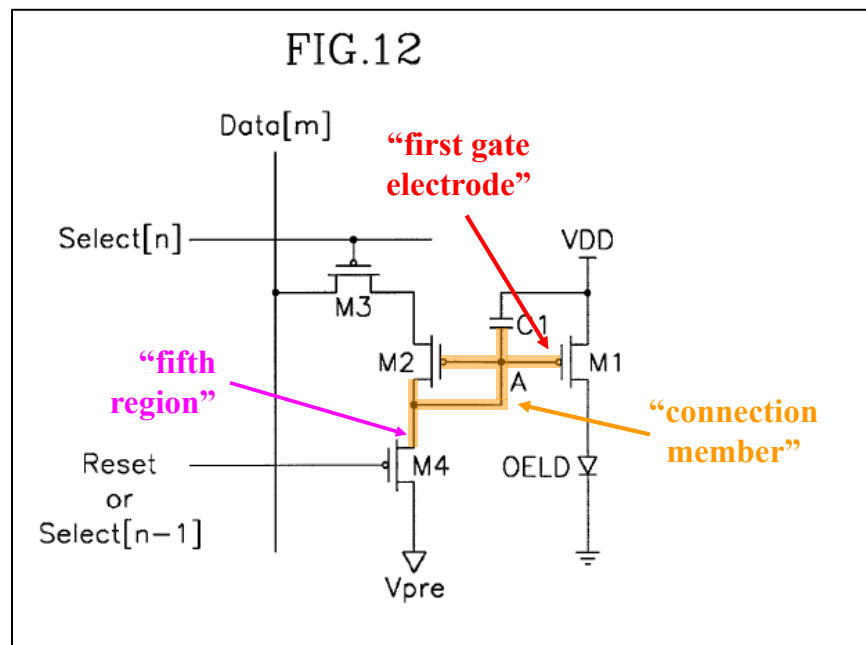
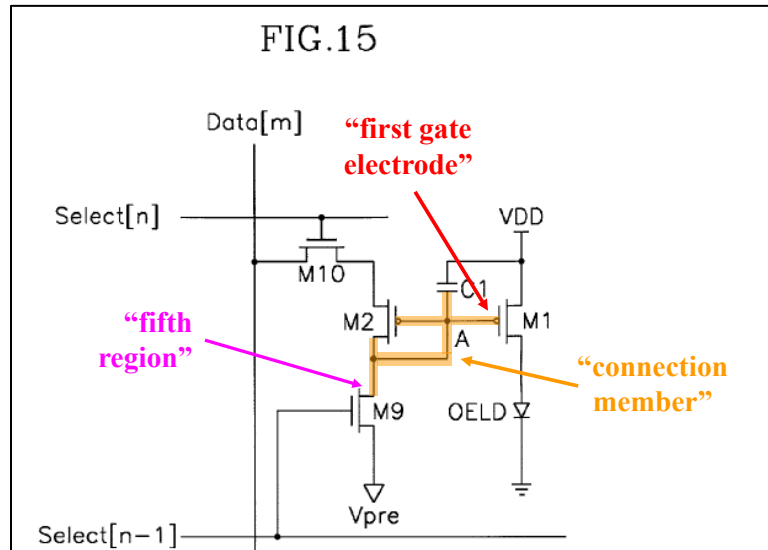
b. 18[c]: “the sixth region is electrically connected to the initialization voltage line.”

Figure 12 (below) shows the *drain* of transistor M4 is electrically connected to the *pre-charge voltage line* (“initialization voltage line” (18[a])). (EX1006, [0076].) Kwon discloses “a pre-charge voltage V_{pre} instead of the ground voltage is supplied to the drain of the switching transistor M4.” (EX1006, [0071]; EX1002, ¶¶225-227.)



- B. Claim 19: “The TFT array substrate of claim 18, wherein the fifth region is electrically connected to the first gate electrode via the connection member.”**

Figure 12 (below) shows the *source* of the transistor M9 (“third thin film transistor” (18[b])) is electrically connected to the *gate electrode of the driving transistor M1* (“first gate electrode”) via the *connection member*. (EX1002, ¶¶228-231.)

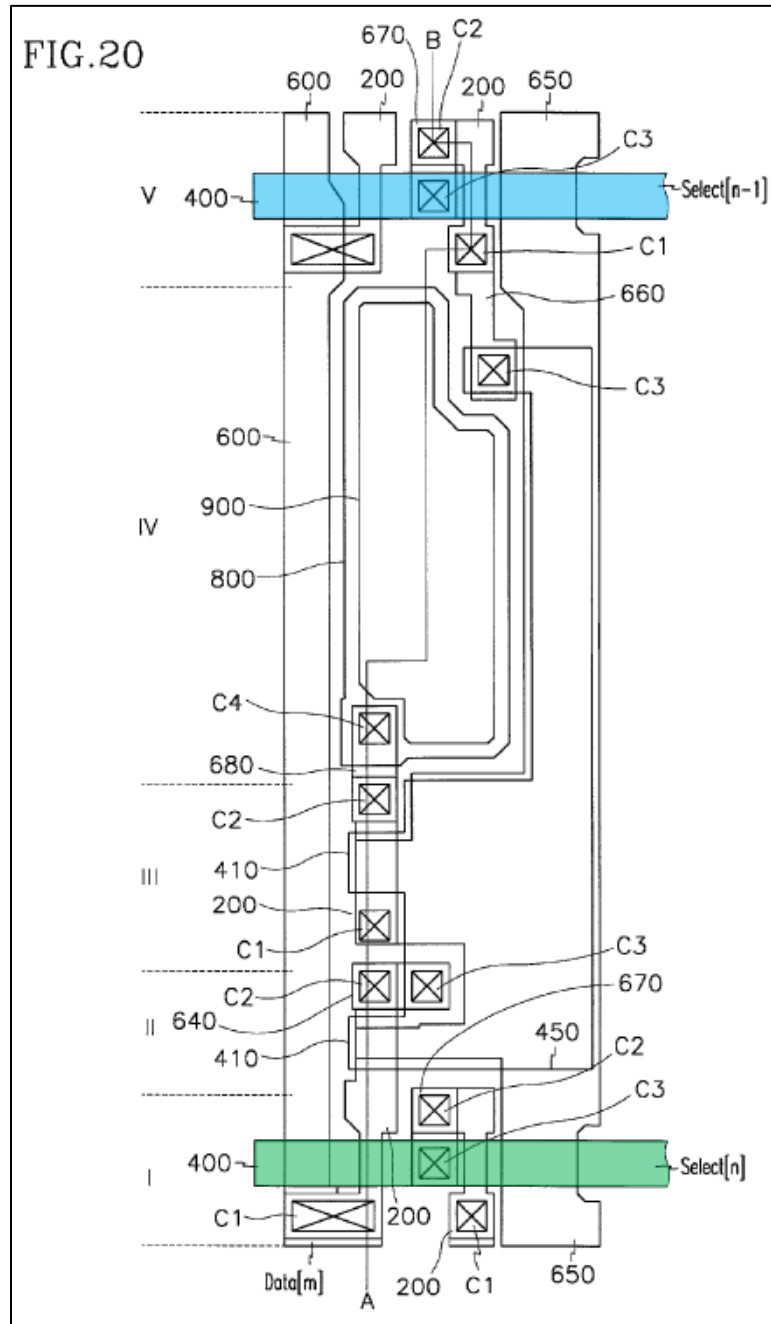


C. Claim 20: “The TFT array substrate of claim 18, wherein the initialization voltage line extends in the same direction as the first gate line.”

Kwon discloses using the previous select signal instead of the pre-charge voltage (“initialization voltage line” (18[a])). (EX1006, [0074].) Kwon discloses “first gate line”: “a select signal Select[n] is supplied to the gate of the [switching]

transistor M3 to activate the corresponding pixel. A data signal Data[m] is supplied to the source of the activated transistor M3 to drive the current driving transistor M1.” (EX1006, [0060]; EX1002, ¶¶232-234.)

Figure 20 (below) shows the *previous select signal Select[n-1]* extends in the same direction as the *select signal Select[n]*. (EX1002, ¶235.)



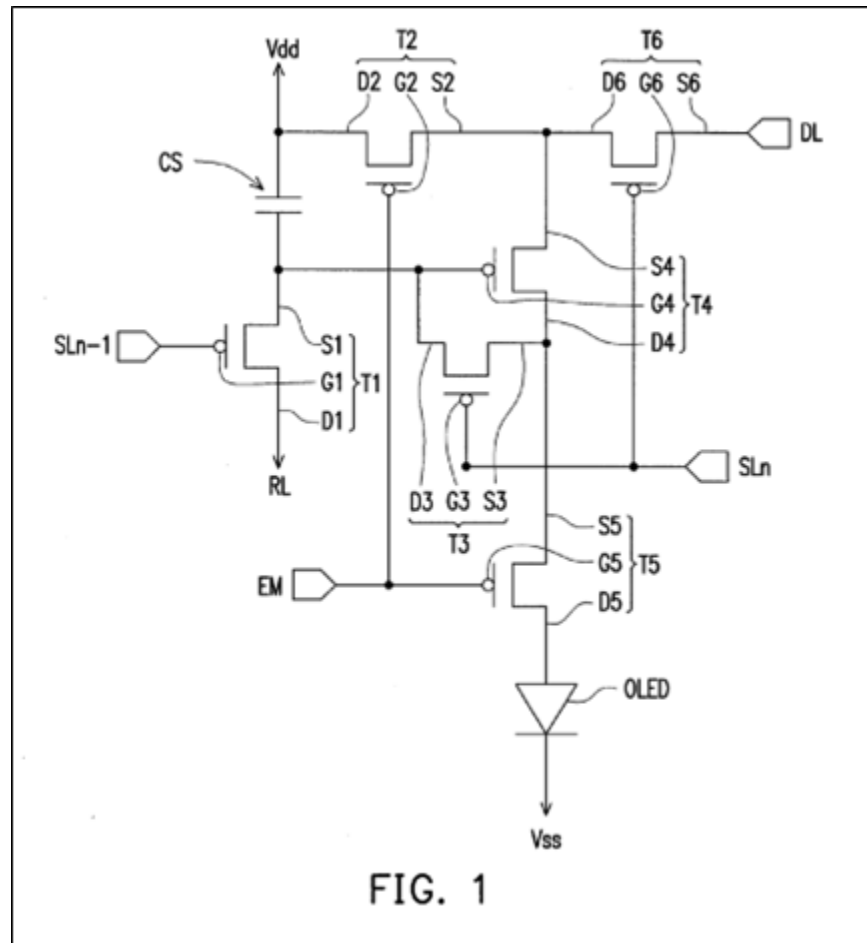
XII. GROUND 8: CLAIMS 1-4, 12-19, 22-24, 28, AND 29 ARE OBVIOUS OVER LIU100 AND ONO

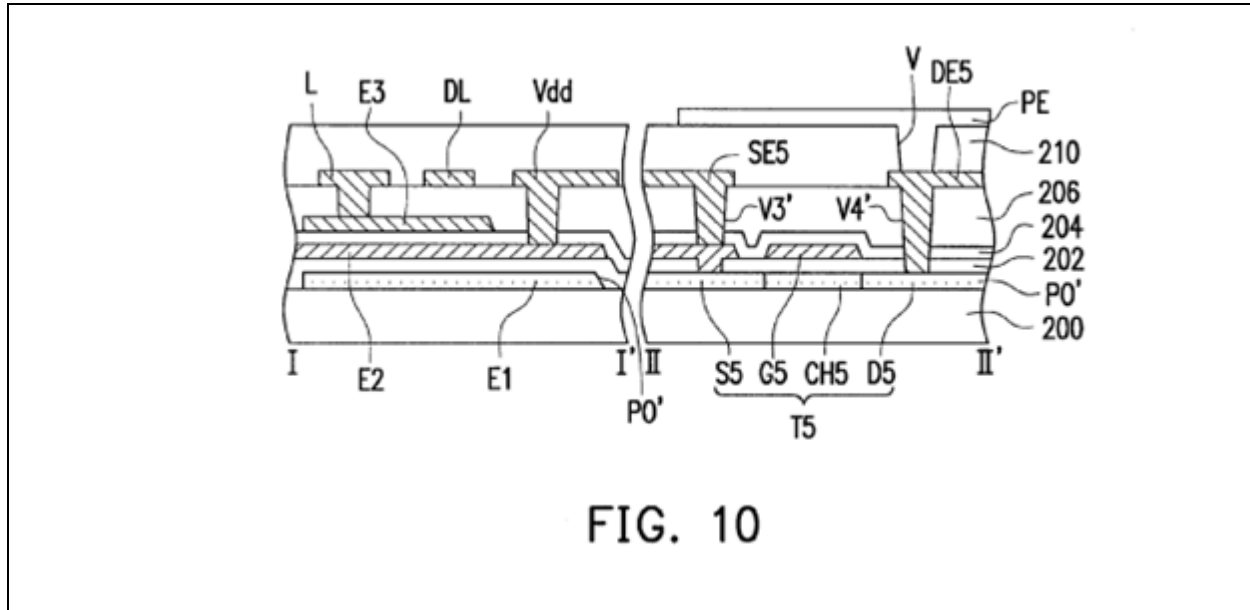
A. Summary Of Liu100

Liu100 discloses a pixel structure for an OLED device “comprising six thin film transistors and one capacitor.” (EX1007, [0032], [0003], [0006].) Liu100

explains that the TFTs typically occupies much of the area in a pixel structure, leaving “no extra space for disposing other components.” (*Id.*; EX1002, ¶¶236-237.)

Liu100 teaches “reducing an area occupied by components of the pixel structure.” (EX1007, [0007].) Figures 1, 8, and 10 (below) shows a circuit schematic, and top and cross-sectional views, respectively, of the pixel circuit and structure of Liu. (EX1007, [0013], [0032], [0058]; EX1002, ¶¶238-239.)





B. Summary Of Ono

Ono discloses “an active-matrix luminescent display device which includes a luminescent element and a driving circuit having a capacitor and a thin-film transistor.” (EX1008, [0003], [0046]; EX1002, ¶240.)

Ono recognizes that conventional active-matrix luminescent display devices have less design flexibility because they dedicate a region to the capacitor. (EX1008, [0005], [0006], [0008].) “[W]hen the number of capacitors or the capacitor area increases, the region for forming other elements becomes smaller.” (*Id.*) Ono teaches a “higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor.” (EX1008, [0010].) Ono forms the capacitor in a region above the driving transistor and includes the gate electrode of the driving transistor for different pixel circuits. (EX1008, [0050], [0070], Fig. 3, Fig. 4, [0091], Fig. 6, Fig. 7, [0113], Fig. 8, Fig.

9, [0124], Figs. 10-12; EX1002, ¶¶241-242.)

C. Claim 1

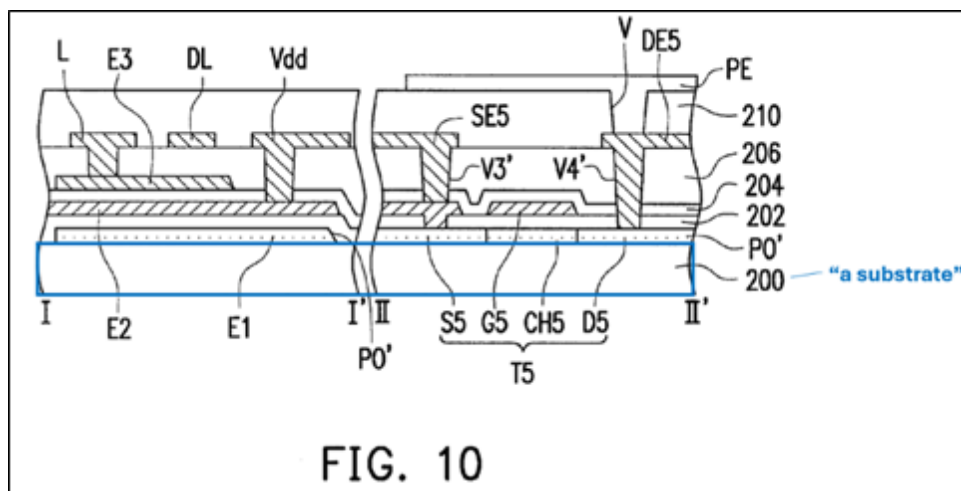
1. Preamble: “A thin film transistor (TFT) array substrate comprising:”

To the extent the preamble is limiting (which Petitioner does not concede), Liu100 teaches the preamble.

Liu100 teaches “the pixel structure is applied to an organic electroluminescence display and has a structure comprising six thin film transistors” (EX1007, [0032], [0008], [0009]; EX1002, ¶¶243-245.)

a. 1[a]: “a substrate;”

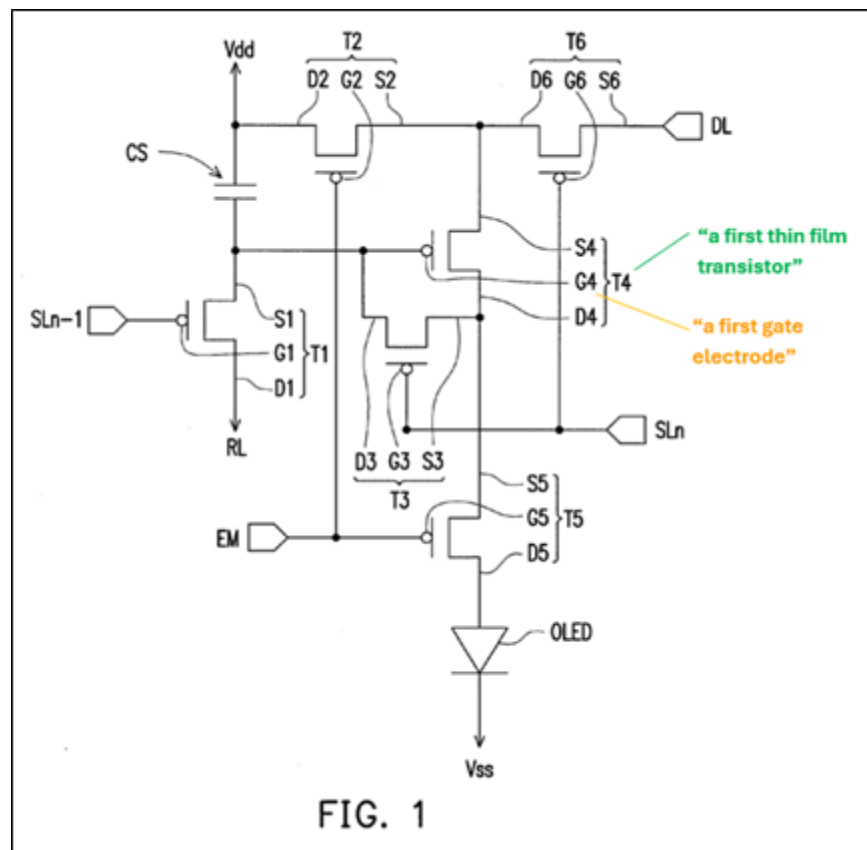
Liu100’s “pixel structure is disposed on a *substrate 200*” (Figure 10 (below)). (EX1007), [0058], [0032]; EX1002, ¶246.)



- b. 1[b]: “a first thin film transistor including a first channel region and a first gate electrode overlapping the first channel region, the first gate electrode and the first channel region being spaced apart from each other with a first insulating layer therebetween;”

Liu100’s pixel structure includes “a channel region (not shown) in a region predetermined for forming a fourth thin film transistor T4.” (EX1007, [0035].)

The “third conductive layer M3 ... in the region [is] predetermined for forming the fourth thin film transistor T4, ... *the gate G4 form the third thin film transistor T4*” (Figure 1 (below)). (EX1007, [0069]; EX1002, ¶¶247-250.)



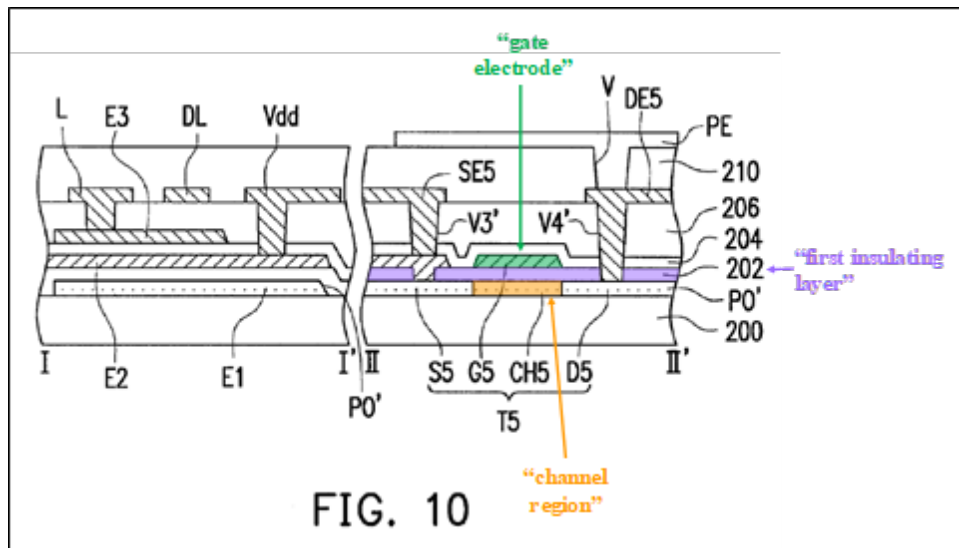
Liu100’s “first insulating layer 202 covers the semiconductor layer PO’.”

(EX1007, [0058].) “The first conductive layer M1’ is disposed on the first

insulating layer 202,” where “the first conductive layer M1’ has a gate G5.”

(EX1007, [0063].) “The gate G is disposed on the insulating layer 202 above the channel region CH of the semiconductor layer PO’.” (EX1007, [0077], [0058].)

The *gate electrode* (Figure 10 (below)) overlaps the *channel region*, and are spaced apart from each other with *insulating layer 202* therebetween. (EX1002, ¶¶249-251.)

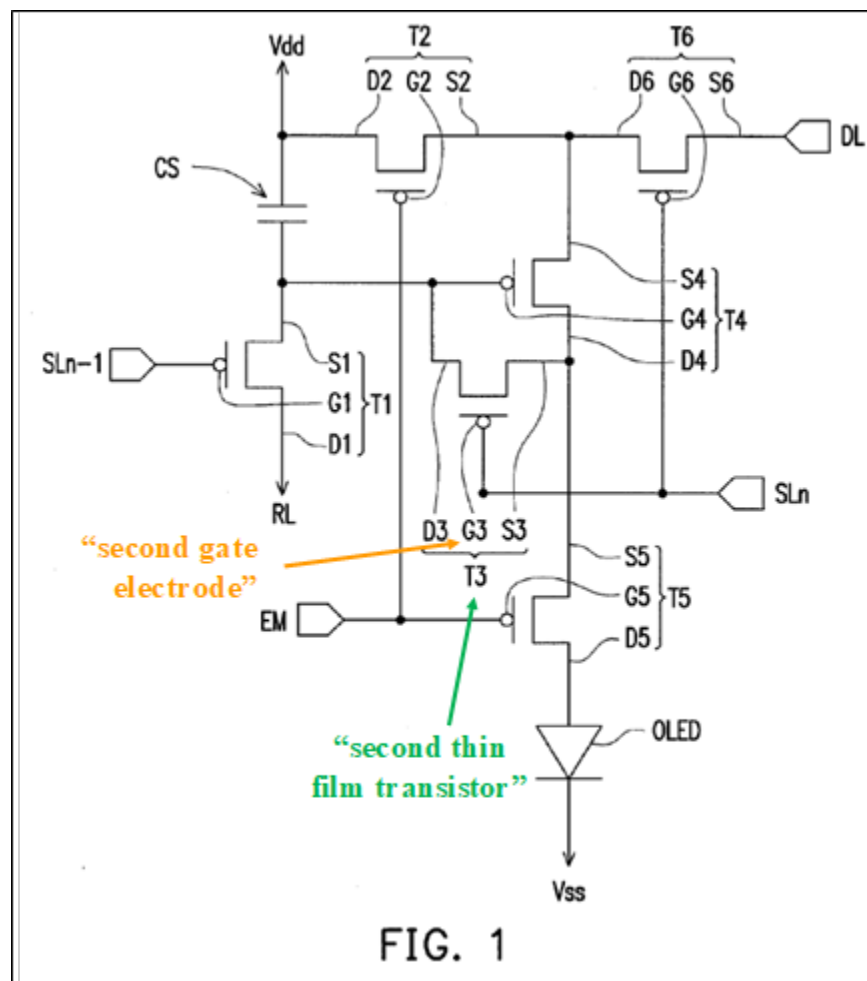


As Liu100 explains, “the cross-sectional diagram of FIG. 10 is a cross-sectional view for the fifth thin film transistor in the 6T1C pixel structure. Since the six thin film transistor in the 6T1C pixel structure are substantially similar, the people skilled in the art may understand the cross-sectional structures of other five thin film transistors in accordance with the description for the fifth thin film transistor shown in FIG. 10.” (EX1007, [0058].) Although Figure 10 shows the cross-sectional view and structure specifically for the transistor T5, a POSITA

would have understood this figure represents the layers and structures for the other transistors including transistor T4. (EX1002, ¶¶252-253.)

- c. 1[c]: “a second thin film transistor including a second channel region and a second gate electrode overlapping the second channel region, the second gate electrode and the second channel region being spaced apart from each other with the first insulating layer therebetween;”

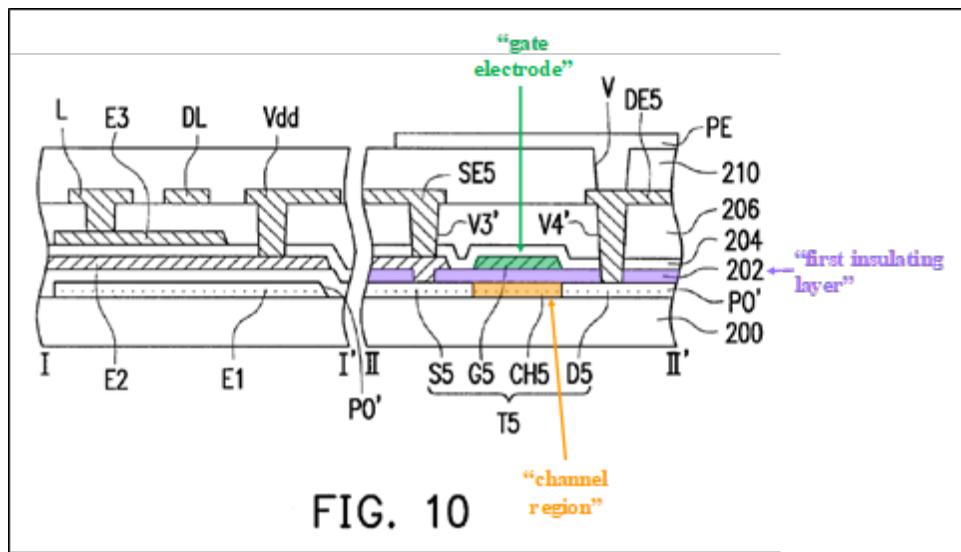
Liu100’s pixel structure comprises *transistor T3* including “a channel region (not shown)” and *gate G3* (Figure 1 (below)). (EX1007, [0032], [0035], [0069]; EX1002, ¶¶254-255.)



Liu100's "first insulating layer 202 covers the semiconductor layer PO'."

(EX1007, [0058].) "The first conductive layer M1' is disposed on the first insulating layer 202," where "the first conductive layer M1' has a gate G5."

(EX1007, [0063].) "The gate G is disposed on the insulating layer 202 above the channel region CH of the semiconductor layer PO'." (EX1007, [0077].) Figure 10 (below) shows the **gate electrode** overlapping the **channel region**, and being spaced apart from each other with **insulating layer 202** therebetween. Liu100 explains Figure 10 represents the cross-sectional view and layers for other transistors, including transistor T4. (See 1[b]; EX1007, [0058]; EX1002, ¶¶256-257.)



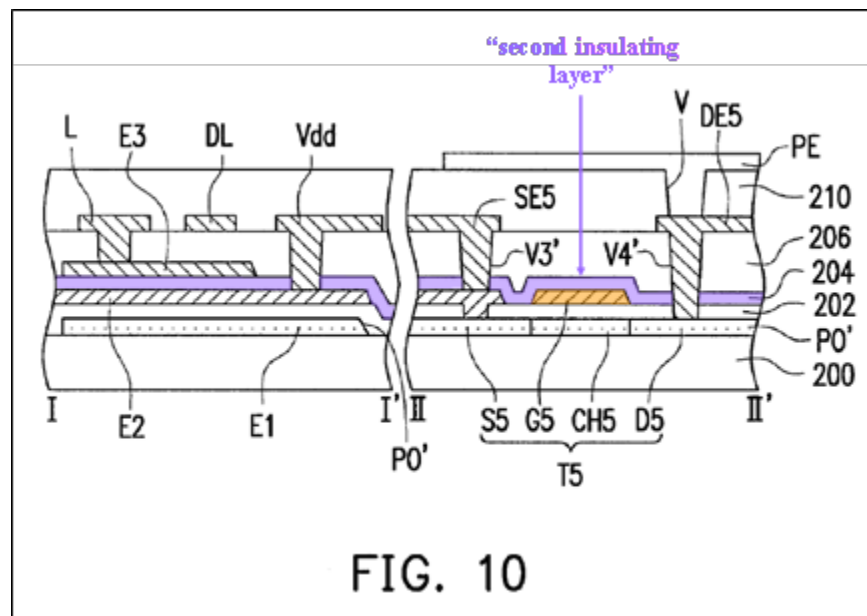
d. 1[d]: "a second insulating layer disposed on the first and second gate electrode;"

Liu100's first conductive layer M1' comprises gate G3 of the third transistor T3 and gate G4 of the fourth transistor T4. (EX1007, [0064].) Liu100's "second

insulating layer 204 covers the first conductive layer M1'." (EX1007, [0065].)

The insulating layer 204 covering the conductive layer M1', comprising gate G4 ("first gate electrode" (1[b])) and gate G3 ("second gate electrode" (XII.C.1.c)), means the insulating layer 204 is disposed on the gates G4 and G3. (EX1002, ¶¶258-259.)

Figure 10 (below) shows the *insulating layer 204* disposed on the *gate electrode G5*. Figure 10 is representative of all the transistors in the pixel structure, including the transistors T4 and T3. (See 1[b]; EX1007, [0058]; EX1002, ¶260.)

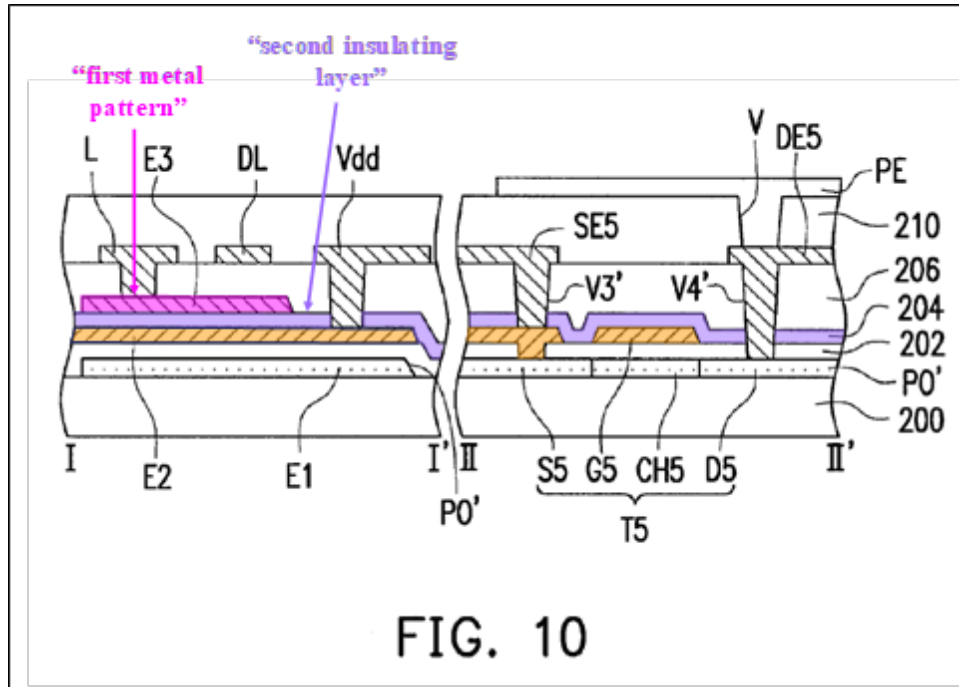


- e. **1[e]: “a first metal pattern overlapping the first gate electrode, the first metal pattern and the first gate electrode being spaced apart from each other with the second insulating layer therebetween;”**

(i) Liu100

Liu100 discloses “a third electrode E3 of the second conductive layer M2’.” (EX1007, [0066]). Liu100’s layer M2’ “has a material similar to or the same with the material” of the second conductive layer M2, which is often made of metal materials.” (EX1007, [0063], [0066], [0040].) The third electrode E3 is part of the capacitor CS and “is disposed above the second electrode E2 of the first conductive layer M1’.” (EX1007, [0066].) “[T]he first conductive layer M1’ has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007, [0063].) “[T]he third electrode E3 is disposed on the second insulating layer 204. The first insulating layer 202 between the first electrode E1 and the second electrode E2 and the second insulating layer 204 between the second electrode E2 and the third electrode E3 serve as capacitor dielectric layers of the capacitor CS.” (EX1007, [0078]; EX1002, ¶¶261-264.)

Figure 10 (below) shows the *electrode E3* (“first metal pattern”) and the *layer M1’* having a gate being spaced apart from each other with *insulating layer 204* (“second insulating layer” (1[d])) therebetween. (EX1007, [0063], [0066]). Figure 10 is representative of all the transistors in the pixel structure, including the transistor T4 having gate G4 (“first gate electrode” (1[b])). (See 1[b]; EX1007, [0058]; EX1002, ¶¶264-265.)



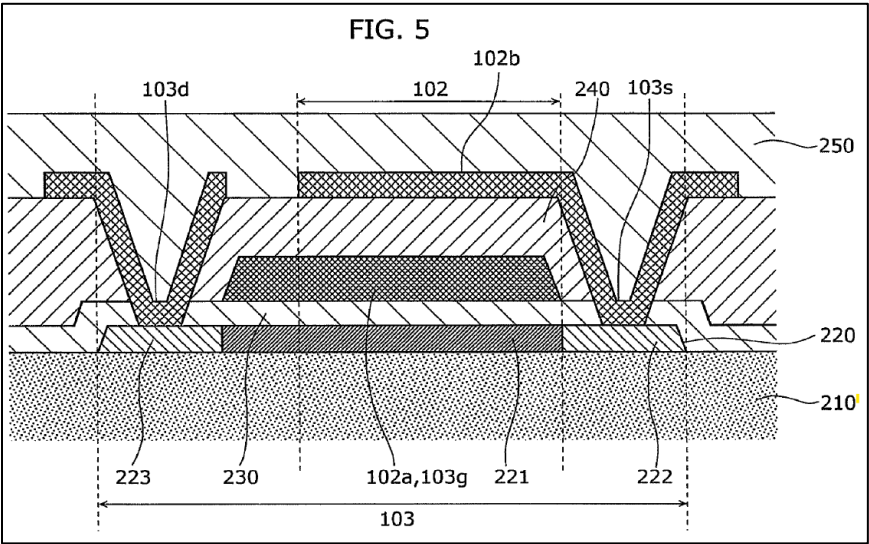
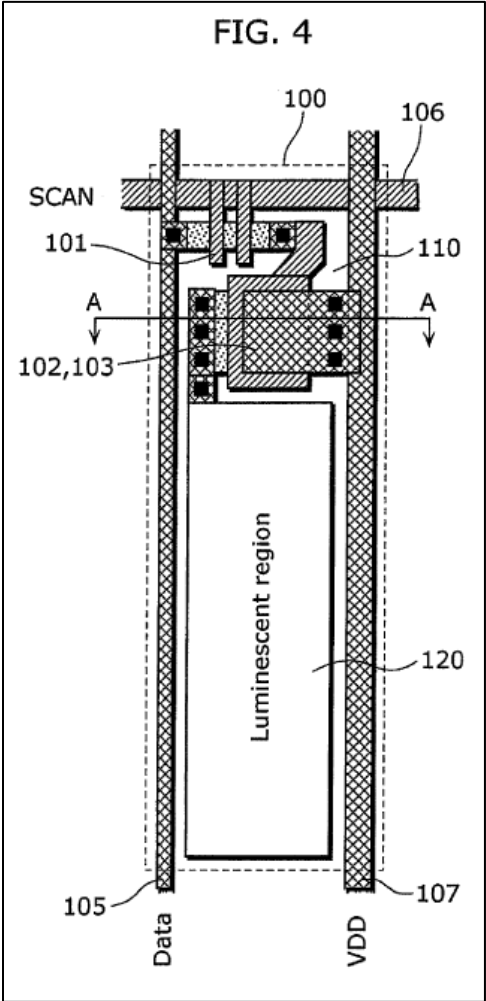
(ii) Ono

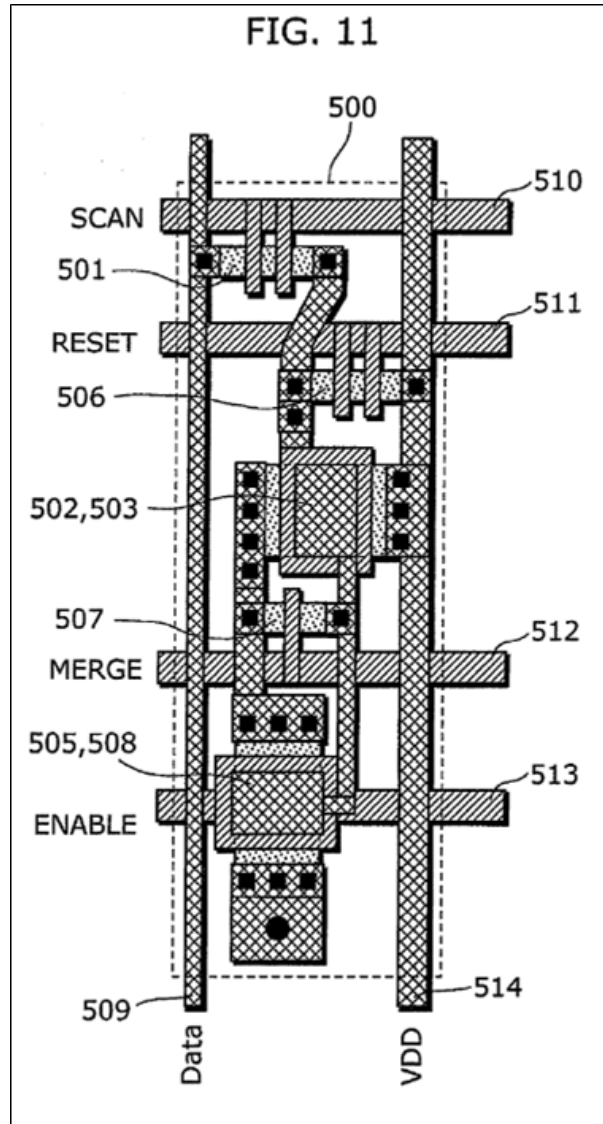
To the extent that Liu100 does not teach this claim element, Ono teaches it.

Ono discloses forming the capacitor in a region above the driving transistor including the gate electrode of the driving transistor for different pixel circuits.

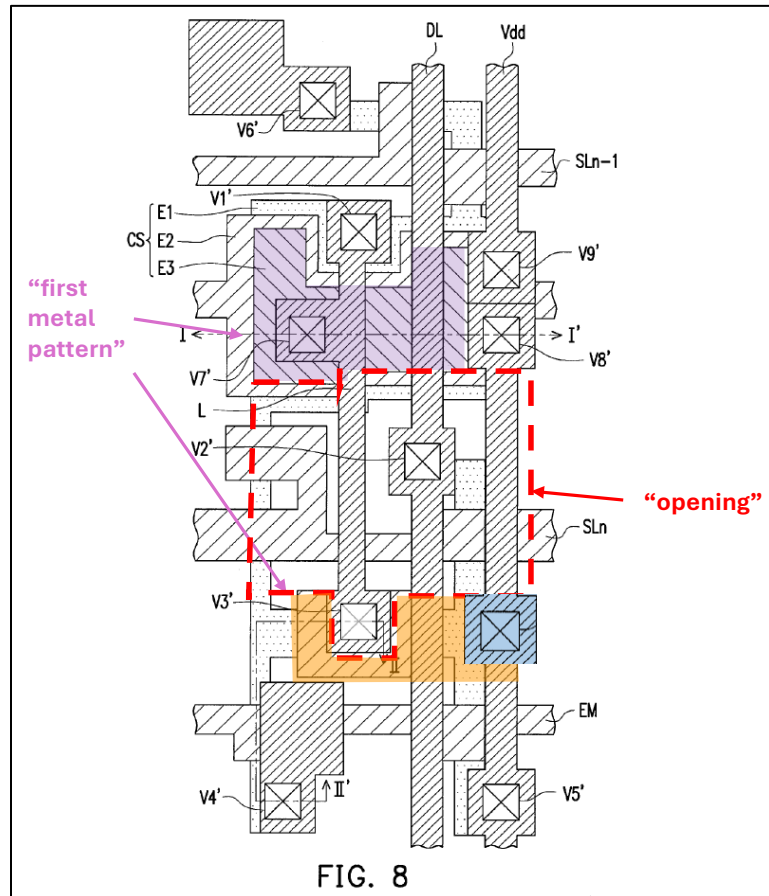
(EX1008, [0050], [0070], [0091], [0113], [0124], Figs. 3, 4, 6-12; (EX1002, ¶266.)

Ono teaches using the capacitor electrode 102a as the gate electrode 103g (Figures 4 and 5 (below)), and putting a capacitor electrode 502 (“first metal pattern”) over the gate of driving transistor 503 (“first gate electrode”) (Figure 11 (below)). (EX1008, [0140] (“the driving transistor 503 and the capacitor 502 are formed in the same region in the plane to overlap each other.”), [0107].) (EX1002, ¶267.)





The Liu100-Ono combination results in extending Liu100's upper electrode to be on top of the driving transistor T4, as taught by Ono. Modified Figure 8 (below) shows the extended *upper electrode* according to the Liu100-Ono combination and an *opening*. It would have been obvious to a POSITA to include an opening in the electrode of a capacitor. (EX1002, ¶268.)



(iii) Motivation to combine Liu100 and Ono

It would have been obvious to combine Liu100 and Ono to extend Liu100's upper electrode in the space above the gate of the transistor T4 to increase the total capacitance. Both disclose OLED devices with an array of transistors, and both address efficiently using the space in the device's pixel structure to promote the miniaturization of OLED devices. Liu100 teaches "reducing an area occupied by components of the pixel structure." (EX1007, [0007].) Ono teaches "a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the

capacitor.” (EX1008, [0030].) Liu100 and Ono are in the same field of endeavor and directed to efficiently using the space to decrease the area of the pixel structure and/or increasing the capacitance of the storage capacitor in the OLED devices. (EX1002, ¶269.)

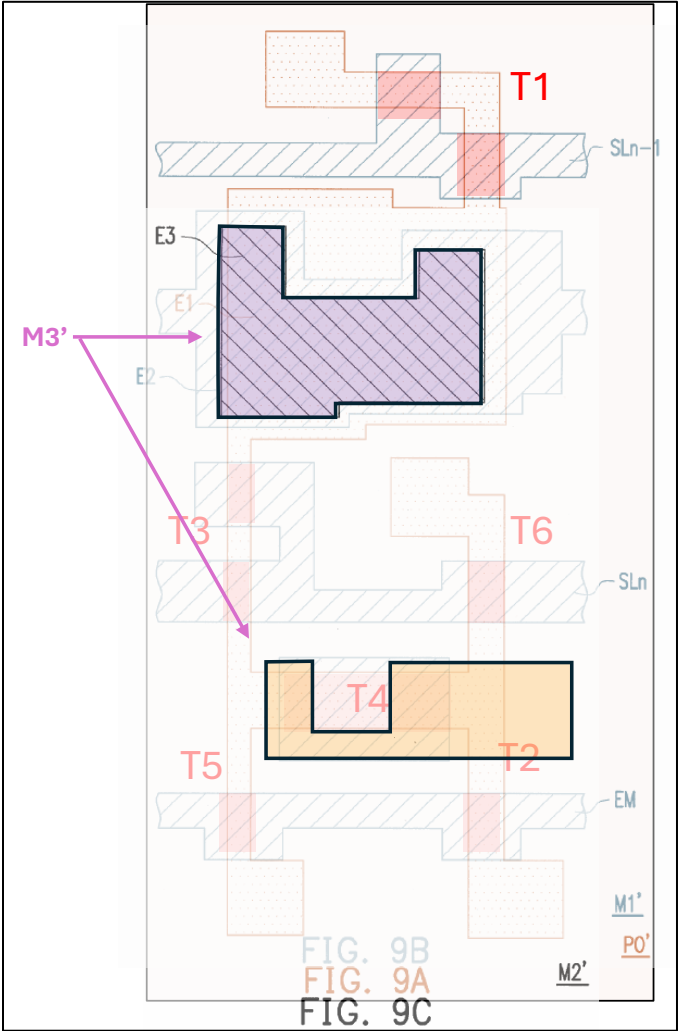
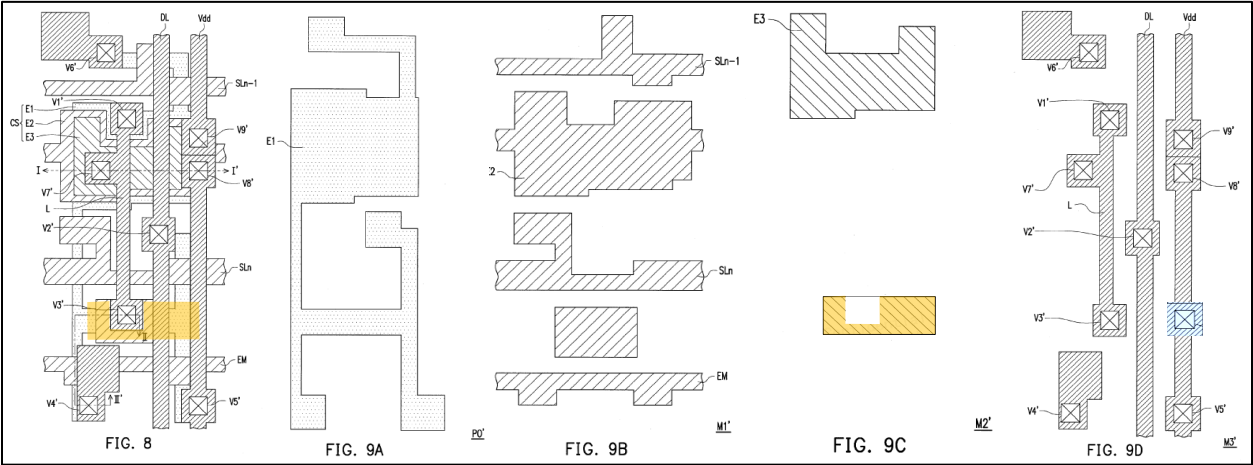
Ono teaches “the gate electrode of the thin-film transistor is used not only simply as the gate electrode but as one of two electrodes constituting the capacitor.” (EX1008, [0029].) “[T]he capacitor can be formed above the thin-film transistor to overlap with the thin-film transistor, enabling efficient use of the pixel space.” (*Id.*) Ono explains “when the number of capacitors or the capacitor area increases, the region for forming other elements becomes smaller, resulting in less design flexibility.” (EX1008, [0008].) Ono teaches the gate electrode of the driving thin-film transistor in different pixel circuits is used as one of the capacitor electrode formed above the driving thin-film-transistor. (EX1008, [0070], [0091], [0113], [0124], Figs. 3, 4, 6-12; EX1002, ¶270.)

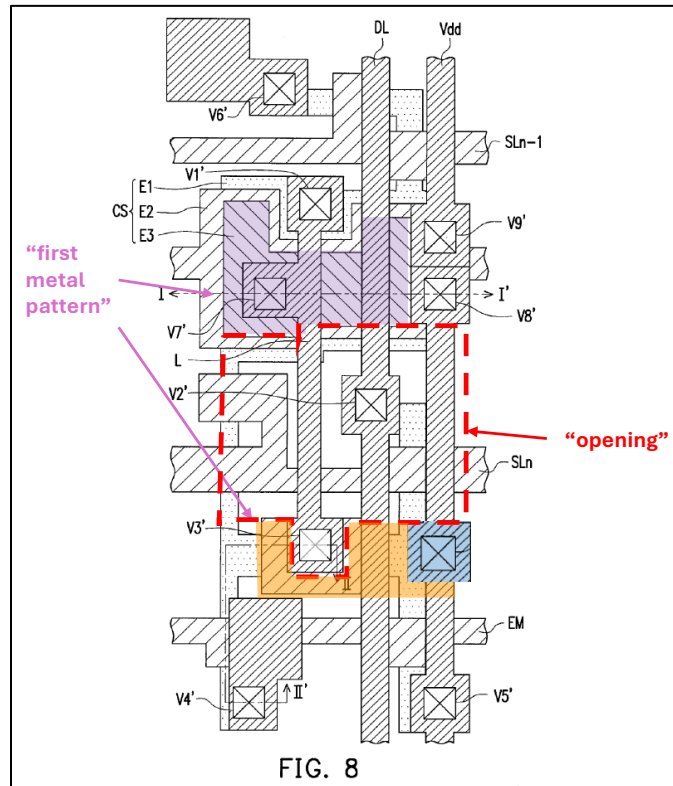
The Liu100-Ono combination results in an OLED with smaller area for the pixel structure and higher design flexibility. The combination results in a smaller OLED device with increased capacitor area for the storage capacitor due to efficiently using unoccupied space, without decreasing the device’s quality. (EX1002, ¶270.)

Liu100’s M2’ layer has a large amount of unoccupied space above the gate

of the driving transistor T4 (Figure 9C). Ono teaches “forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor.” (EX1008, [0030].) A POSITA would have been motivated to extend Liu100’s upper electrode in the space above the gate of the driving transistor T4, as taught by Ono and other prior art (*e.g.*, EX1015, [0011], [0019]), to increase the capacitor area, increasing the overall capacitance and improving display performance without using additional area. Because no extra layers are added and the space is unoccupied, a POSITA would have had a reasonable expectation of success combining the two references. All that is required is a different mask for patterning the M2’ layer. (EX1002, ¶271.)

Figures 8 and 9A-9D (below) are modified according to the Liu100-Ono combination, showing the extended *upper electrode*. The composite Figures 9A-9D (below) shows the extended *upper electrode* according to the Liu100-Ono combination. The extended upper electrode extends to overlap with and connect to the power line Vdd to a via structure. Liu100 discloses “the layout of the first conductive layer M1' is shown in FIG. 9B, which mainly comprises gates of the six thin film transistors.” (EX1007, [0063].) “[T]he first conductive layer M1’ has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007, [0064]; EX1002, ¶272.)

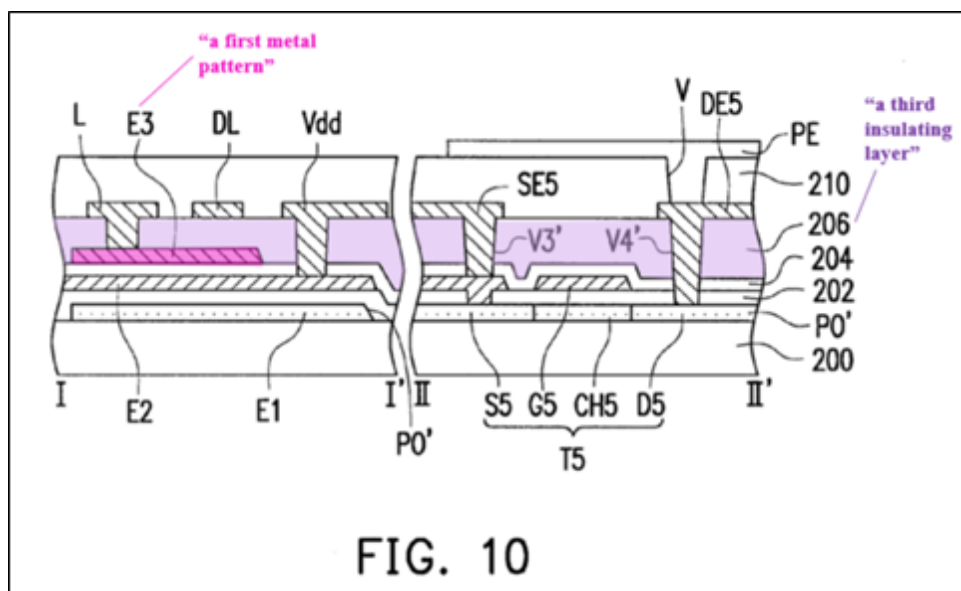




Because Liu100 and Ono both relate to efficiently using pixel space within organic light emitting display devices, a POSITA would be motivated to use Ono's techniques to improve the similar device of Liu100 in the same way. Ono's teaching of placing a capacitor electrode over a gate electrode of the driving transistor was known in the art. Liu100's device including unoccupied space on its layer M2' above the gate electrode of driving transistor T4 makes it easy to extend the upper electrode to include more capacitor area. Ono has successfully demonstrated OLED device configurations that shrink the size of the components within a pixel structure, and it would have been obvious to a POSITA to combine Liu100 and Ono. (EX1002, ¶273.)

2. 1[f]: “a third insulating layer disposed on the first metal pattern; and”

Liu100’s “*third insulating layer 206* covers the second conductive layer M2” (Figure 10 (below)). (EX1007, [0058], [0067].) Liu100’s third *electrode E3* (part of the “first metal pattern” (1[e])) is in the second conductive layer M2’. (EX1007, [0066]; EX1002, ¶¶274-275.)



3. 1[g]: “a connection member disposed on the third insulating layer and electrically connecting the first gate electrode and the second thin film transistor.”

Liu100 discloses a *signal line L* (“connection member”) (Figure 10 (below)) disposed on *insulating layer 206* (“third insulating layer” (1[f])). (EX1002, ¶¶276-277.)

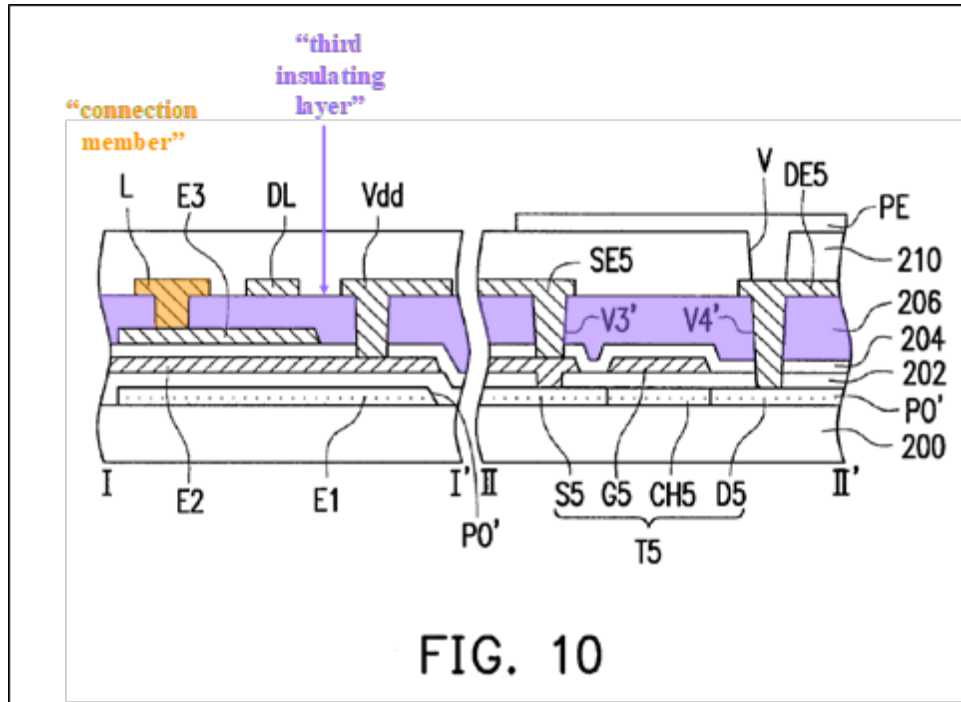
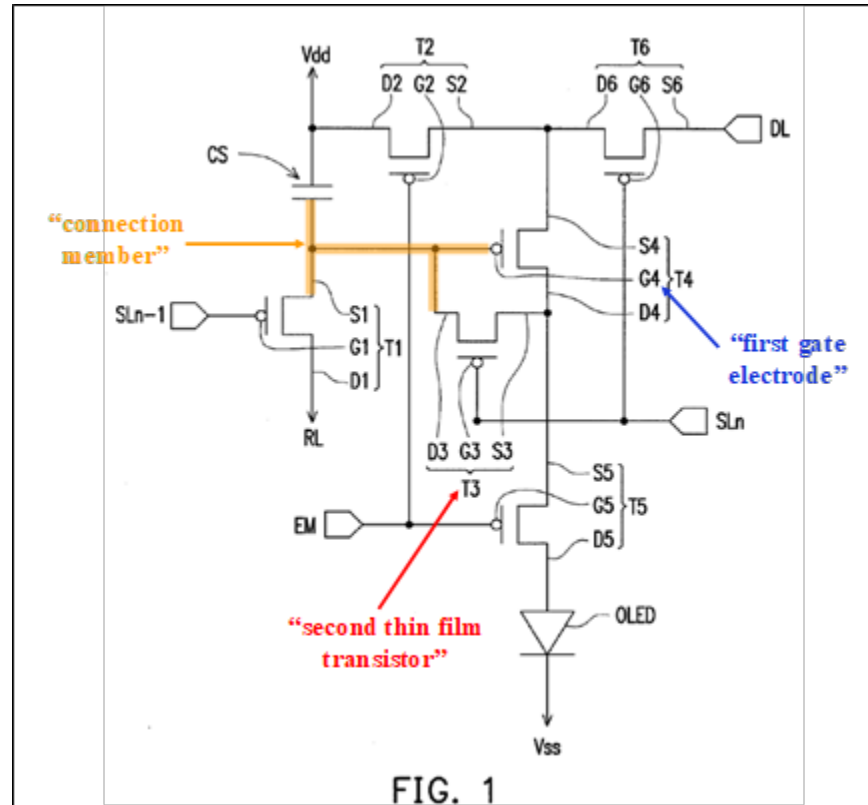


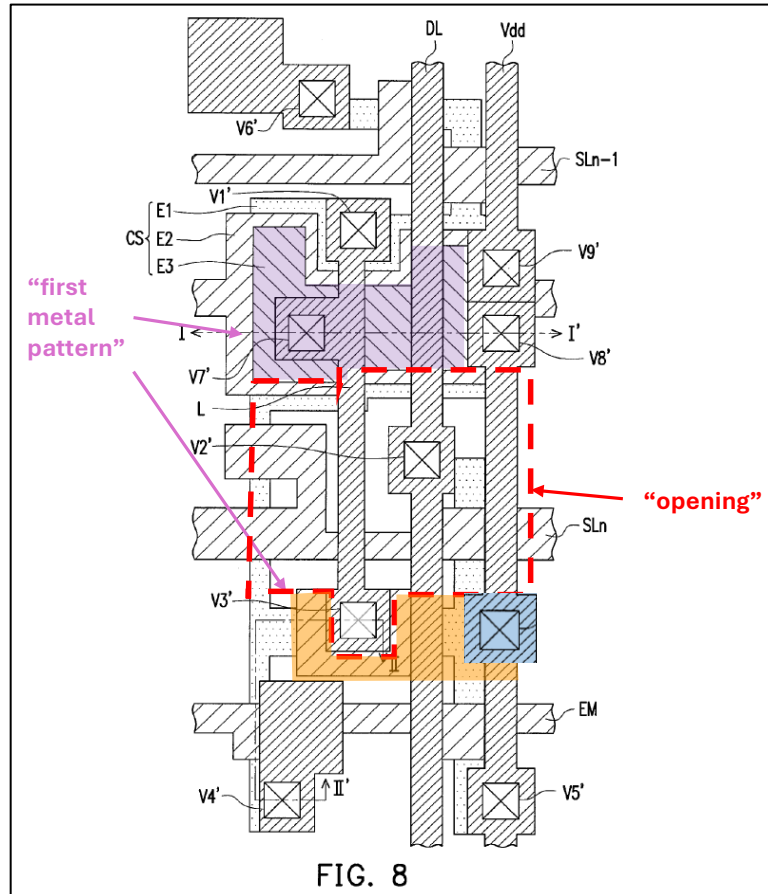
Figure 1 (below) shows the *connection member* electrically connecting *gate electrode G4* ("first gate electrode" (1[b])) to the *transistor T3* ("second thin film transistor" (1[c])). (EX1002, ¶278.)



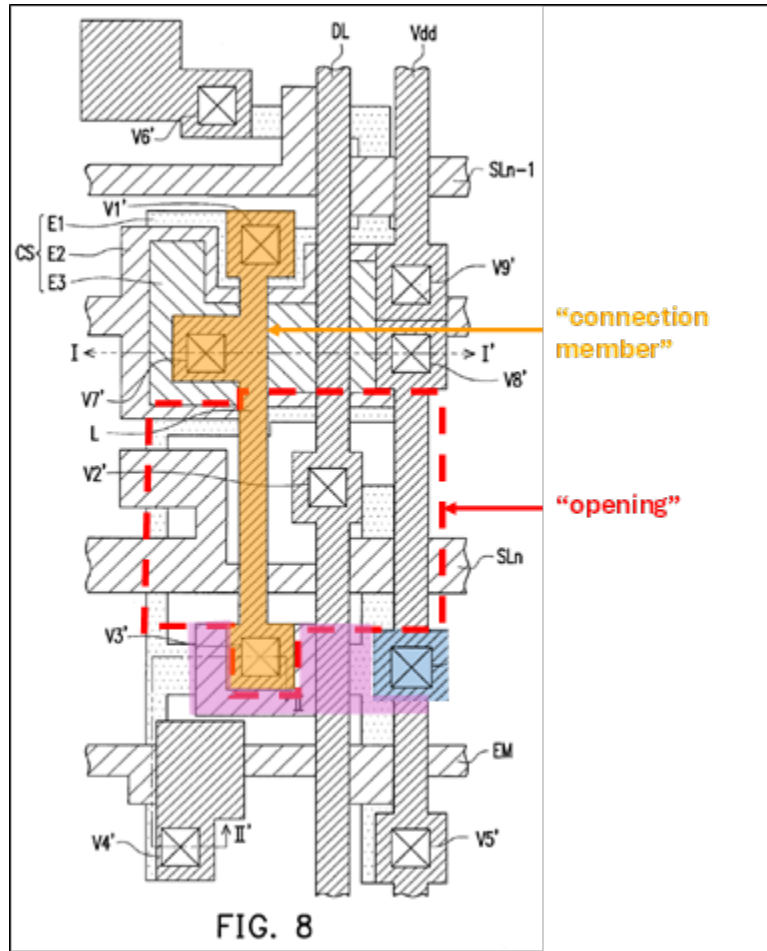
D. Claim 2: “The TFT array substrate of claim 1, wherein the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.”

The Liu100-Ono combination teaches forming an extended upper electrode (“first metal pattern”) in the space above the gate of the transistor T4 to increase the total capacitance. (EX1007, [0063], [0064]; *see* 1[e].) Figure 9C shows the M2’ layer comprising a large unoccupied space above the gate of the transistor T4. (EX1007, [0057], [0066].) Figure 8 (below) has been modified to include the extended upper electrode of the Liu100-Ono combination. The figure shows the M2’ layer including the *electrode E3* and the extended *upper electrode* of the Liu100-Ono combination including an *opening*. It was known to a POSITA for a

connection member to connect to a lower capacitor electrode using an opening in the upper electrode. (EX1002, ¶¶279-281.)



Modified Figure 8 (below) shows the *connection member* overlapping the *opening* of the Liu100-Ono combination in a plan view. (EX1002, ¶¶282-283.)



E. Claim 3

1. 3[a]: “The TFT array substrate of claim 2, wherein at least one of the second and third insulating layers includes a node contact hole overlapping the opening, and”

Liu100’s “third insulating layer 206 covers the second conductive layer M2” and “third conductive layer M3’ is disposed on the third insulating layer 206.” (EX1007, [0067], [0068].) The third conductive layer M3’ has source electrodes and drain electrodes “electrically connected to the source region and the drain regions through contact via structures V1’-V6’.” (EX1007, [0069]; EX1002,

¶¶284-285.)

Modified Figure 8 (below) shows the *via structure V3'* overlaps the *opening*. (EX1002, ¶286.)

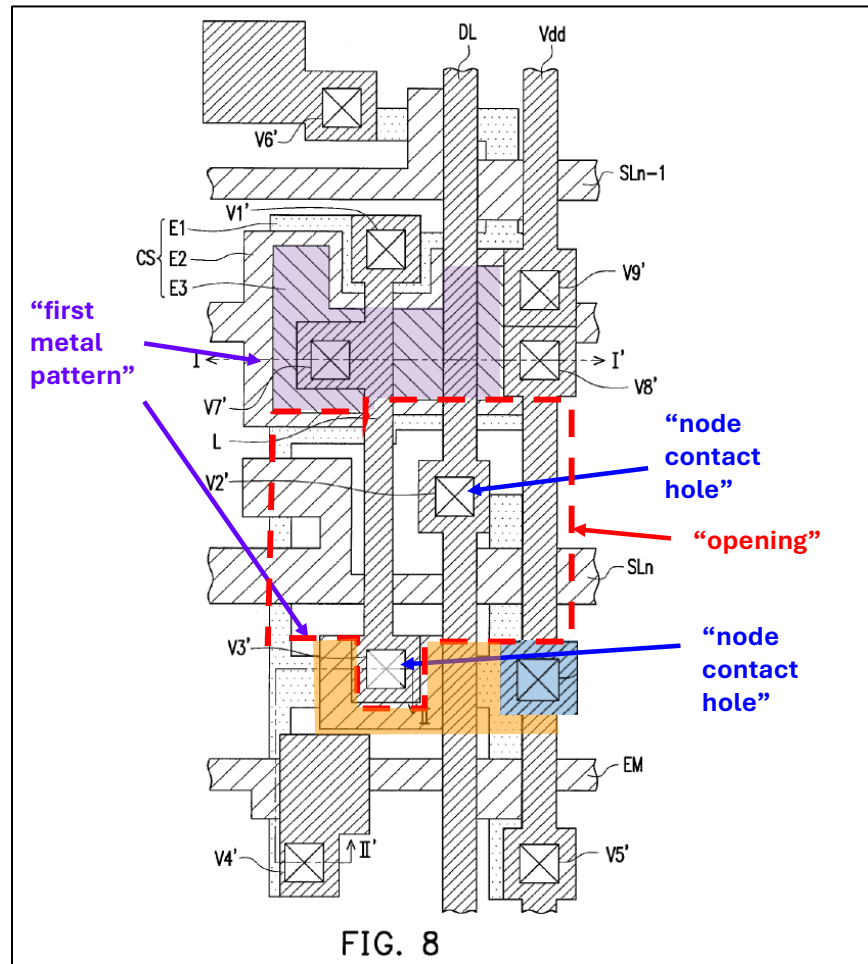
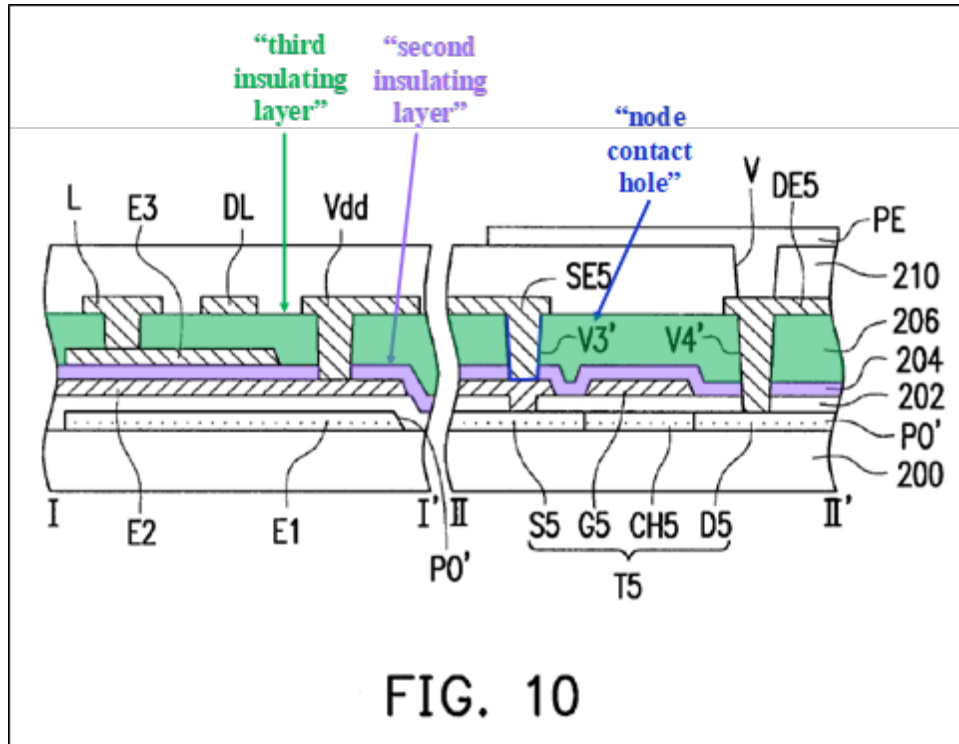


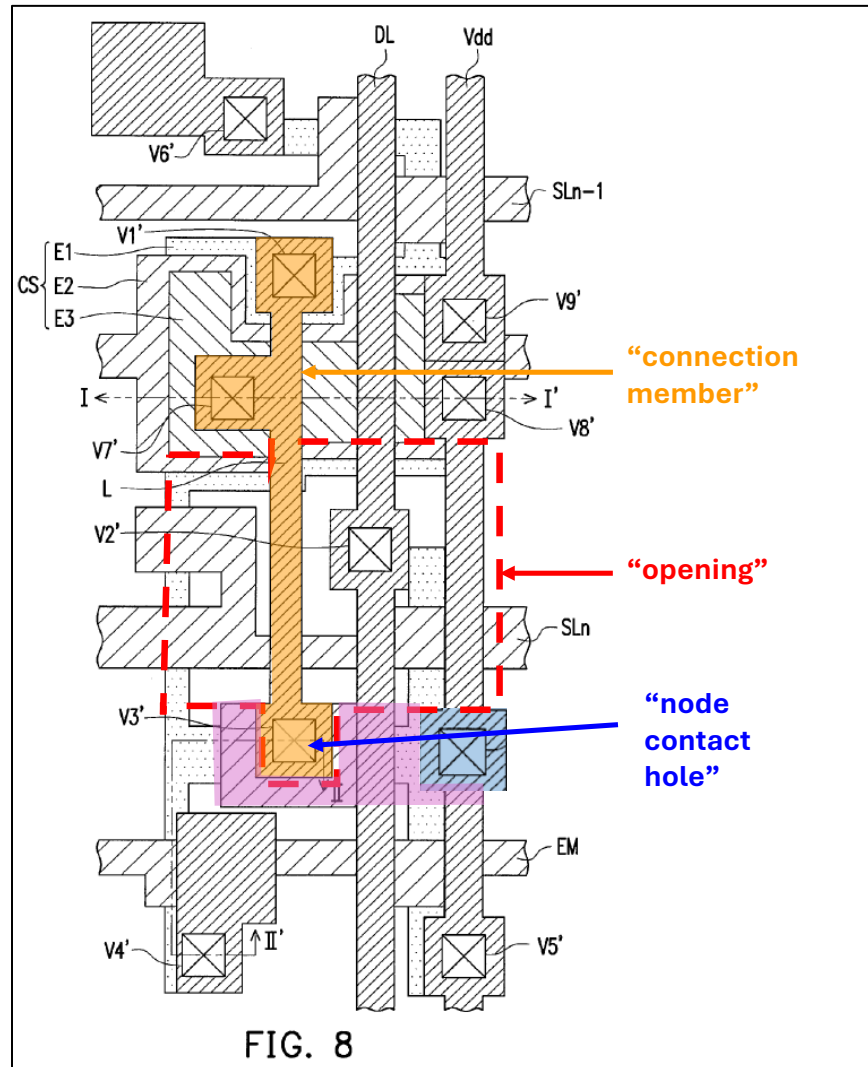
Figure 10 (below) shows the *insulating layer 204* (“second insulating layer” (1[d])) and *insulating layer 206* (“third insulating layer” (1[f])) including a *via structure V3'*. (EX1002, ¶287.)



2. 3[b]: “the portion of the connection member is connected with the first gate electrode through the node contact hole.”

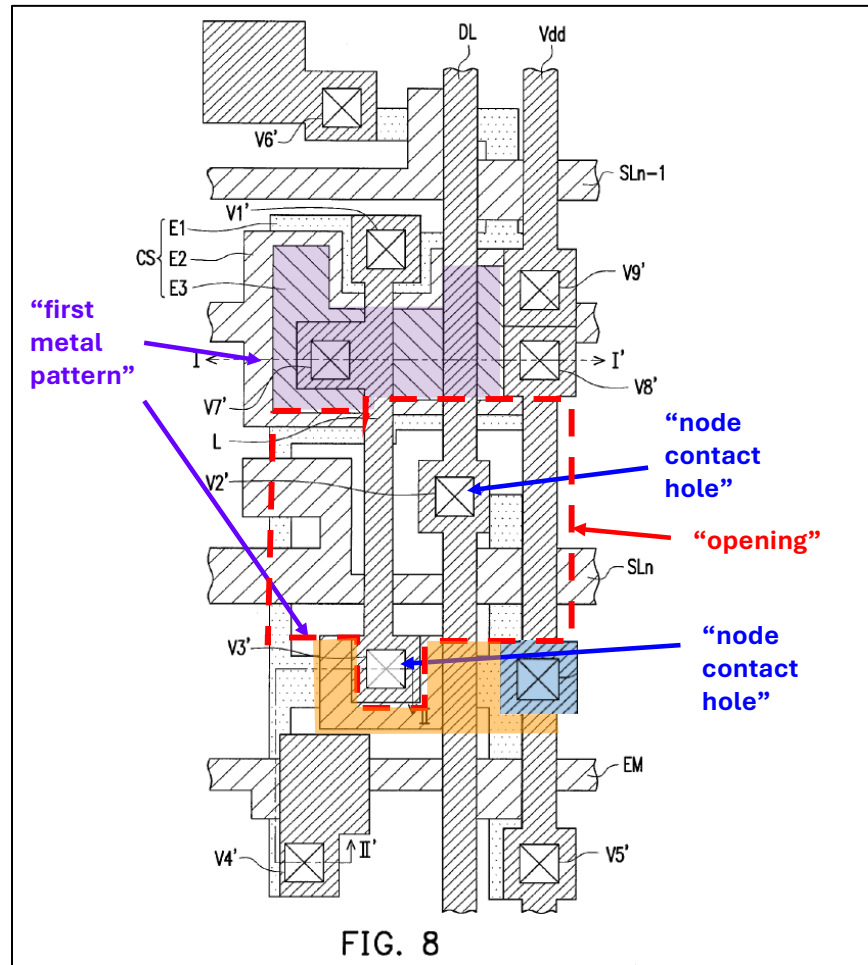
Liu100 teaches a portion of signal line L (“connection member”) overlapping with the opening. (See claim 2.) The signal line L is connected with the gate of transistor T4. Liu100’s third conductive layer M3’ has source electrodes and drain electrodes “electrically connected to the source region and the drain regions through contact via structures V1’-V6’.” (EX1007, [0069].)

Modified Figure 8 (below) shows a portion of the **signal line L** is located on top of, and thus connected with, the gate electrode of transistor T4 through the **via structure V3’**. (EX1002, ¶¶288-290.)



F. Claim 4: “The TFT array substrate of claim 3, wherein a size of the opening is greater than a size of the node contact hole in the plan view.”

Modified Figure 8 (below) of the Liu100-Ono combination shows the size of the *opening* in the M2' layer is greater than a size of a *via structure V3'* (“node contact hole” (3[a])) in the plan view. (EX1002, ¶¶290-293.)

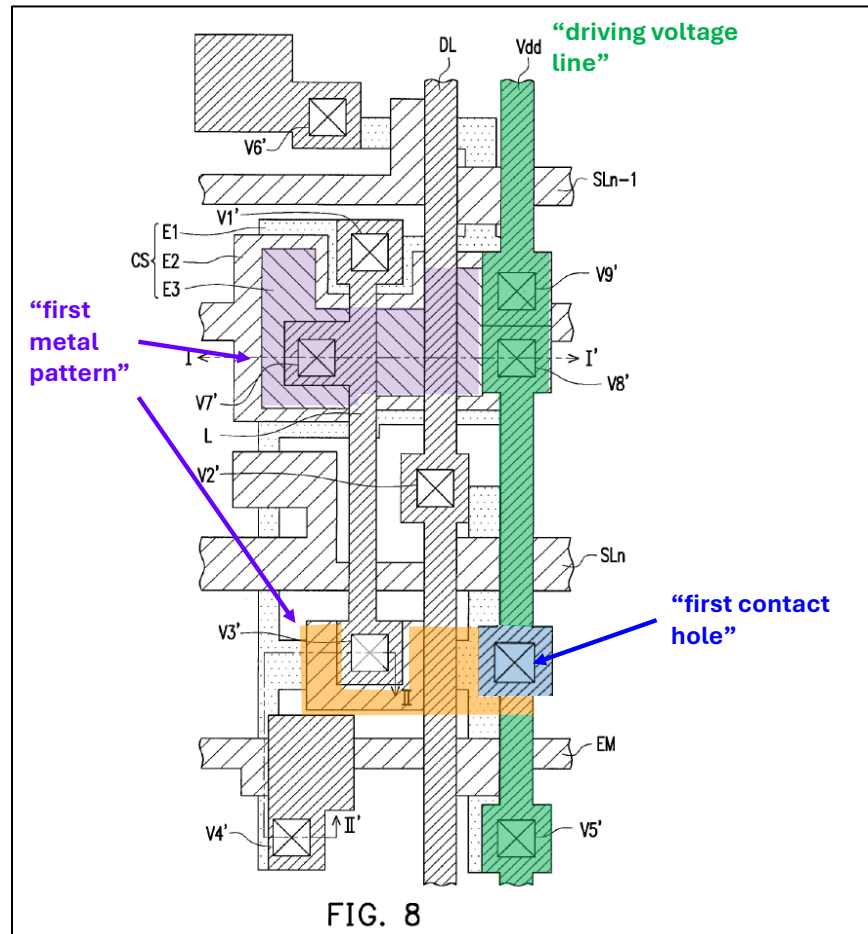


G. Claim 11: “The TFT array substrate of claim 1, further comprising a driving voltage line on the third insulating layer, wherein the driving voltage line is connected to the first metal pattern through a first contact hole of the third insulating layer.”

Liu100’s “third conductive layer M3” further comprises ... the power line Vdd is electrically connected to the second electrode E2 of the capacitor CS through contact via structures V8-V9’.” (EX1007, [0070]; EX1002, ¶¶294-295.)

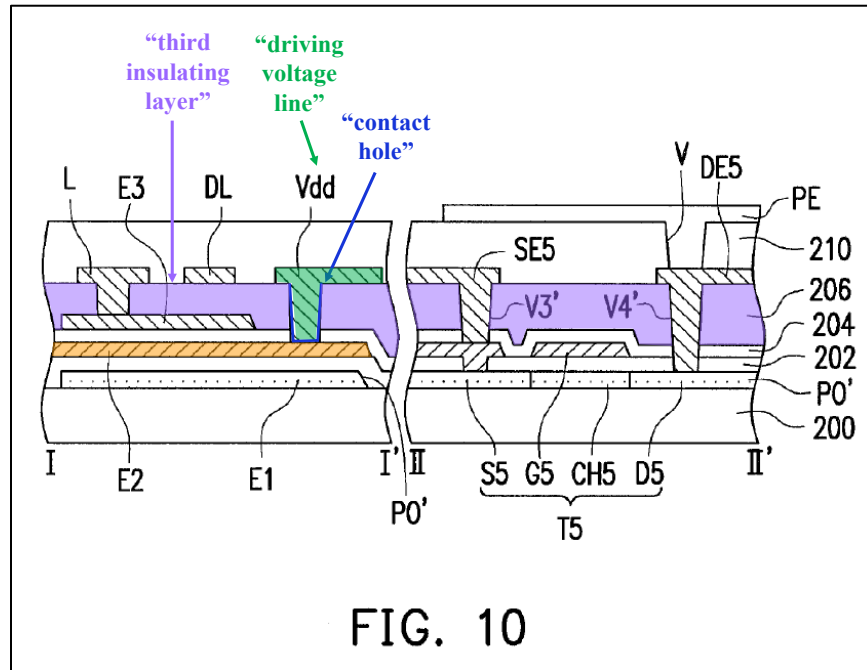
The Liu100-Ono combination comprises an extended upper electrode (“first metal pattern”) in the space above the gate of the transistor T4 to increase the total

capacitance. (See 1[e].) The extended *upper electrode* is electrically coupled to the *power line Vdd* through a *via structure* (modified Figure 8 (below)) of the Liu100-Ono combination. (EX1002, ¶296.)



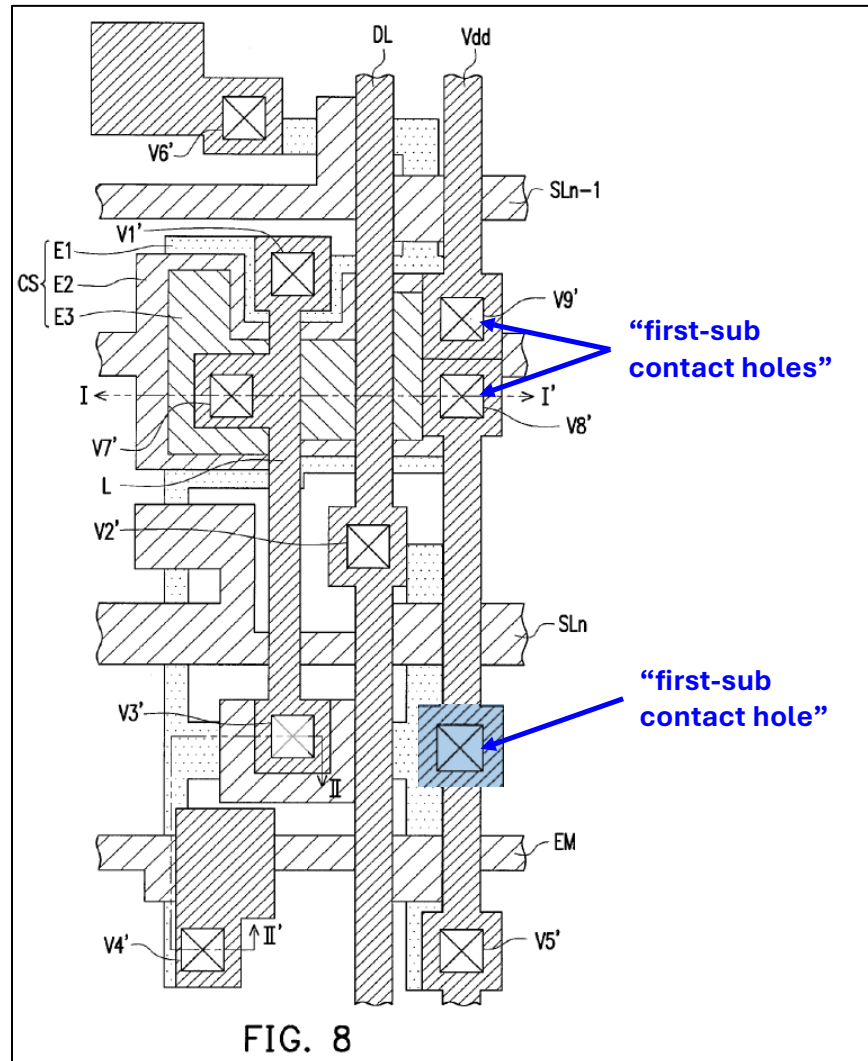
Liu100's via structures ("contact hole[s]") are of the insulating layer 206 ("third insulating layer"). (See 3[a].) Figure 10 (below) shows the *power line Vdd* is connected to *electrode E2* through a *via structure* of the *insulating layer 206*. A POSITA would have understood the power line Vdd would be similarly connected to the extended upper electrode through a via structure of the insulating layer 206.

(EX1002, ¶297.)



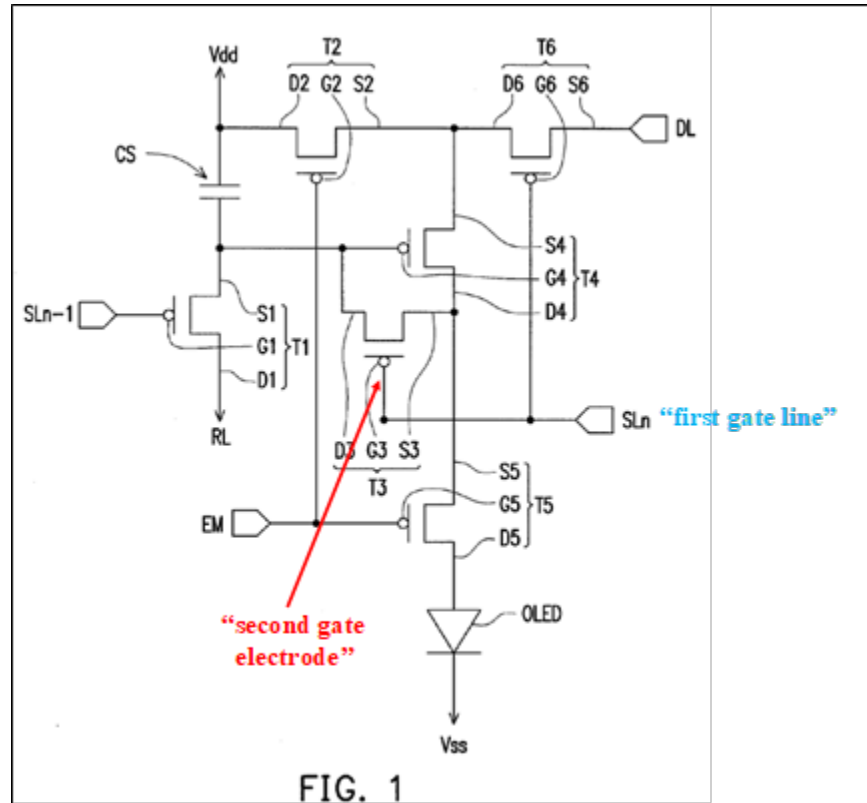
H. Claim 12: “The TFT array substrate of claim 11, wherein the first contact hole includes a plurality of first-sub contact holes.”

Figure 8 (below) of the Liu100-Ono combination shows a plurality of *via structures* (“first contact hole” (claim 11)) making connections to the power line Vdd (“driving voltage line”). (EX1002, ¶¶298-299.)



- I. **Claim 14:** “The TFT array substrate of claim 1, further comprising a first gate line electrically connected to the second gate electrode.”

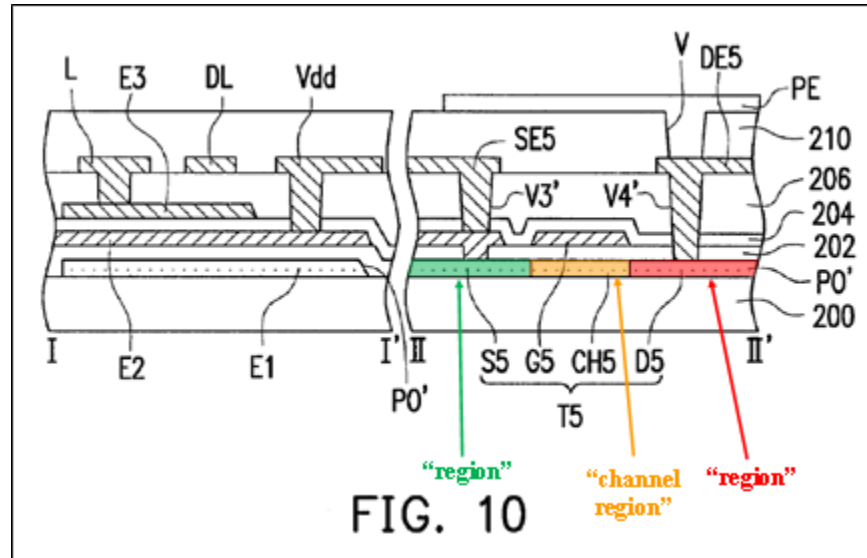
Liu100’s “*scan line SLn* is electrically connected to the *gate G3*” (“second gate electrode” (1[c])) (Figures 1 and 8 (below)). (EX1007, [0038], [0064]; EX1002, ¶¶300-302.)



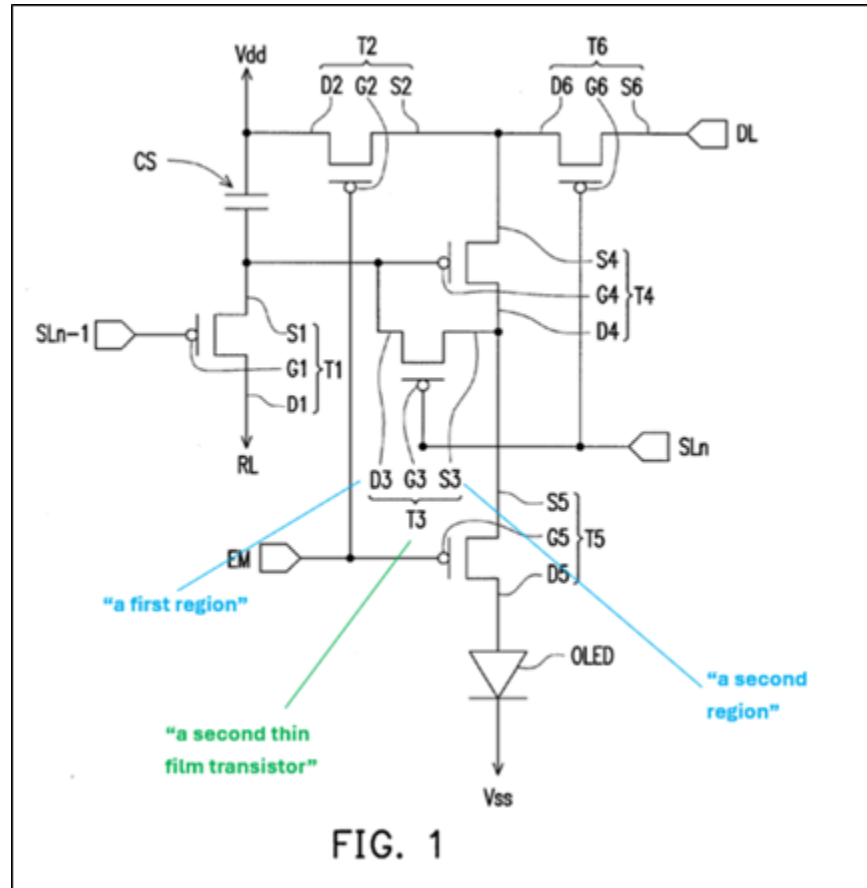
J. Claim 15

1. 15[a]: “The TFT array substrate of claim 14, wherein the second thin film transistor further comprises a first region adjacent to a side of the second channel region and a second region adjacent to another side of the second channel region, and”

Figure 10 (below) shows Liu100’s transistor comprising a *source region* adjacent to a side of the *channel region* and a *drain region* adjacent to another side of the channel region. (EX1007, [0060].) Liu100 explains Figure 10 represents the cross-sectional view and structure for other transistors, such as transistor T3. (See 1[c]; EX1007, [0058], [0060]; EX1002, ¶¶303-304.)



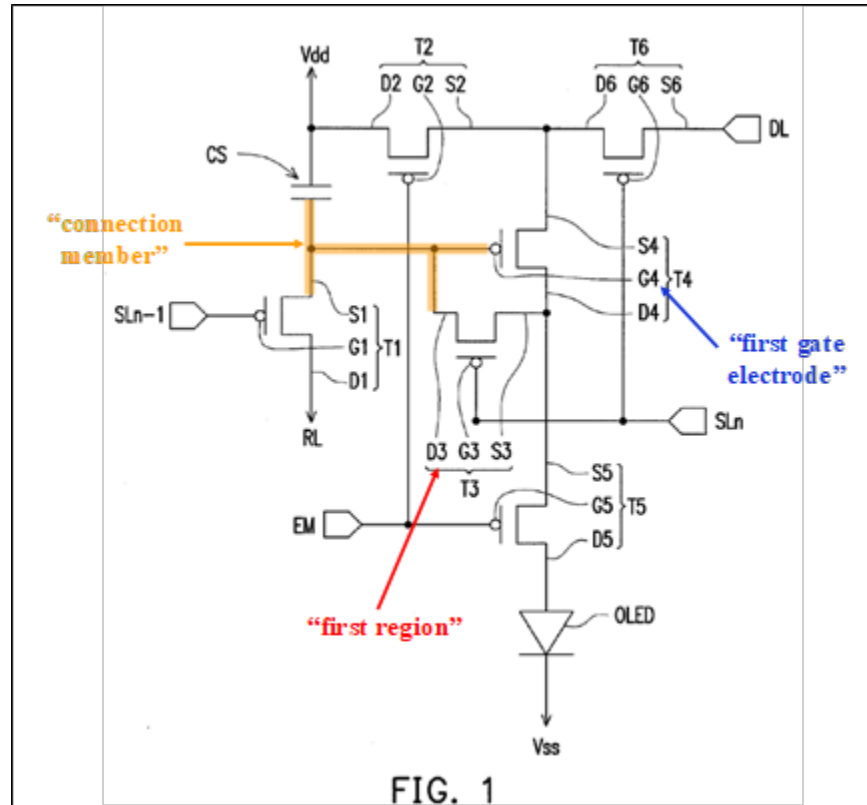
Liu100's "semiconductor layer PO has a source region S3, a drain region D3 and a channel region (not shown) in a region predetermined for forming a third film transistor T3." (EX1007, [0035].) Figure 1 (below) shows the *source region S3* is adjacent to a side of the *transistor T3* (including the channel region), and the *drain region D3* is adjacent to another side of the transistor T3 (including the channel region). (EX1002, ¶305.)



2. 15[b]: “the first region is electrically connected to the first gate electrode via the connection member.”

Liu100’s “bottom electrode BE is electrically connected to the source region S1, the drain region D3 and the gate G4, as shown in FIG. 1.” (EX1007, [0042].)

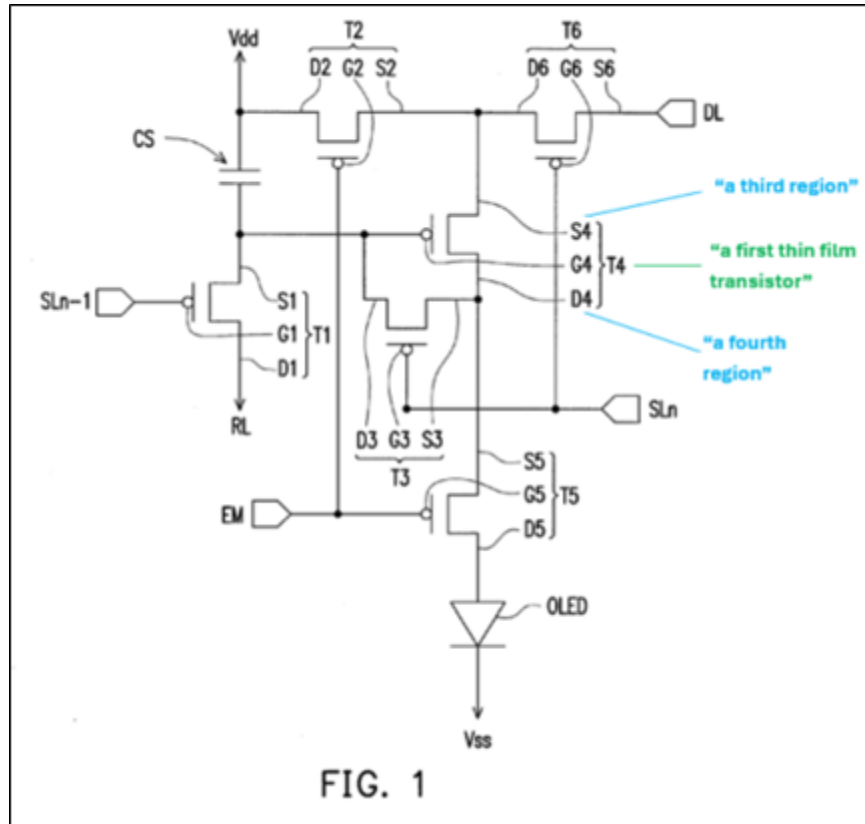
Figure 1 (below) shows the *drain region D3* (“first region” (15[a])) is electrically connected to *gate G4* (“first gate electrode” (1[b])) via the *signal line L*. (EX1002, ¶¶306-308.)



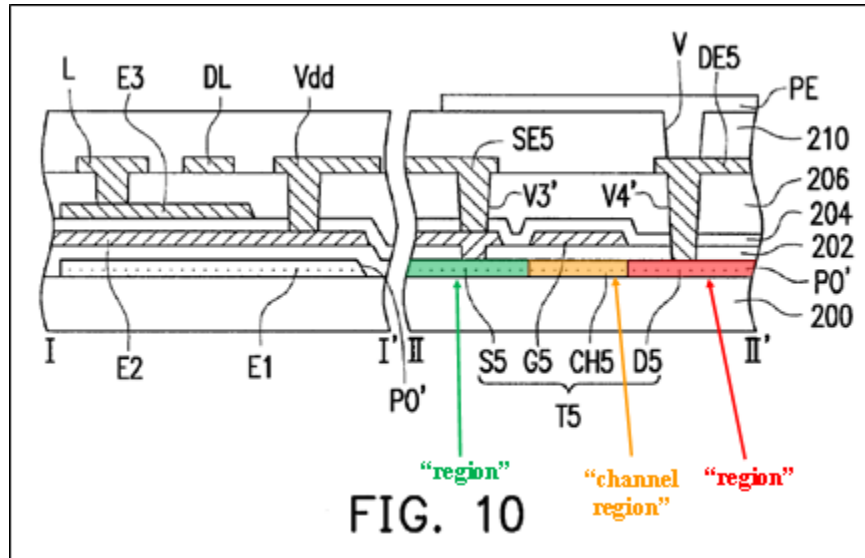
K. Claim 16

1. 16[a]: “The TFT array substrate of claim 15, wherein the first thin film transistor further comprises a third region adjacent to a side of the first channel region and a fourth region adjacent to another side of the first channel region, and”

Liu100 discloses “a channel region (not shown) in a region predetermined for forming a fourth thin film transistor T4.” (EX1007, [0035].) The *transistor T4* (“first thin film transistor” (1[b])) (Figure 1 (below)) comprises a *source region S4* adjacent to a side of the transistor T4 (including the channel region (not shown)), and a *drain region D4* adjacent to another side of the transistor T4 (including the channel region (not shown)). (EX1007, [0035]; EX1002, ¶¶309-310.)

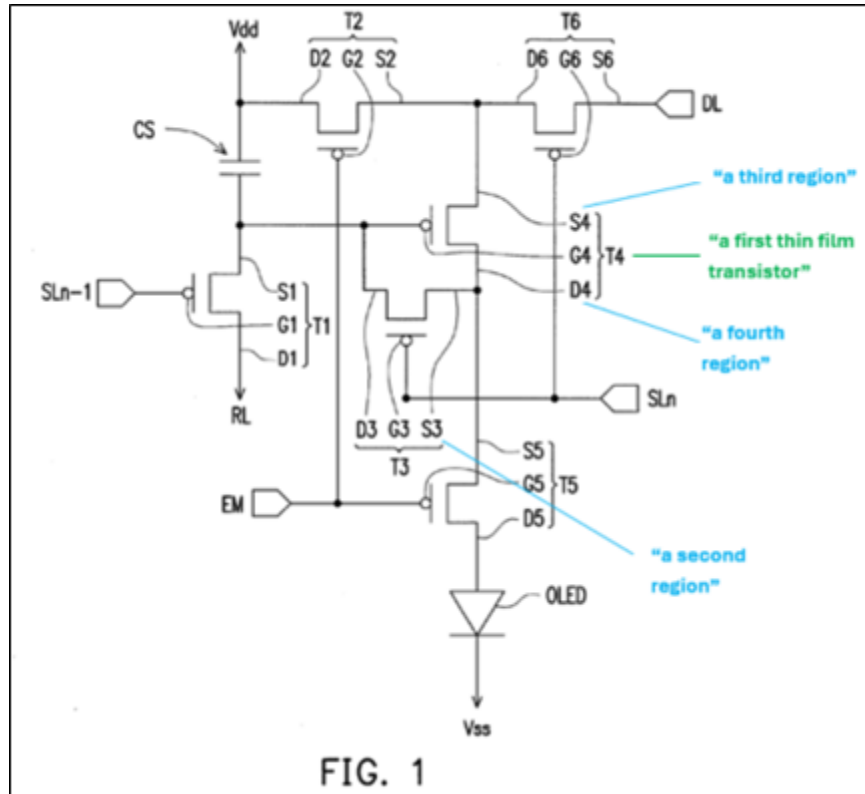


Liu100's transistors comprise a *source region* adjacent to a side of the *channel region* and a *drain region* adjacent to another side of the channel region, the structure of Figure 10 (below) being representative of all transistors, such as transistor T4. (1[c]; EX1007, [0058], [0060]; EX1002, ¶311.)



2. 16[b]: “the second region is electrically connected to the fourth region.”

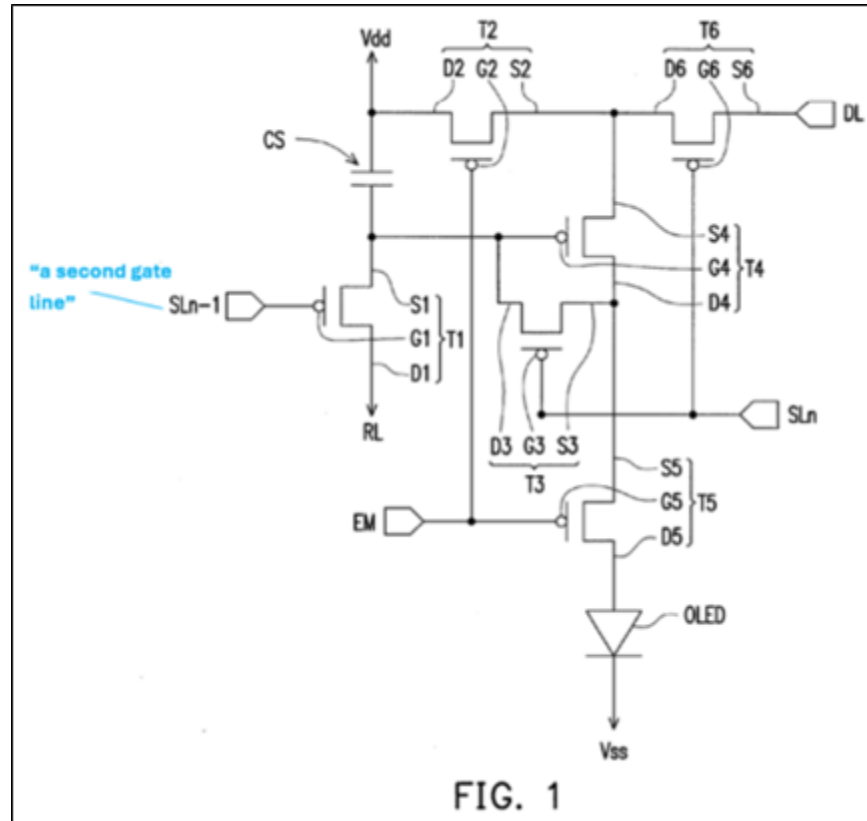
Figure 1 (below) shows Liu100’s *source region S3* (“second region” (16[a])) is electrically connected to *drain region D4* (“fourth region” (16[a])). (EX1002, ¶¶312-313.)



L. Claim 17

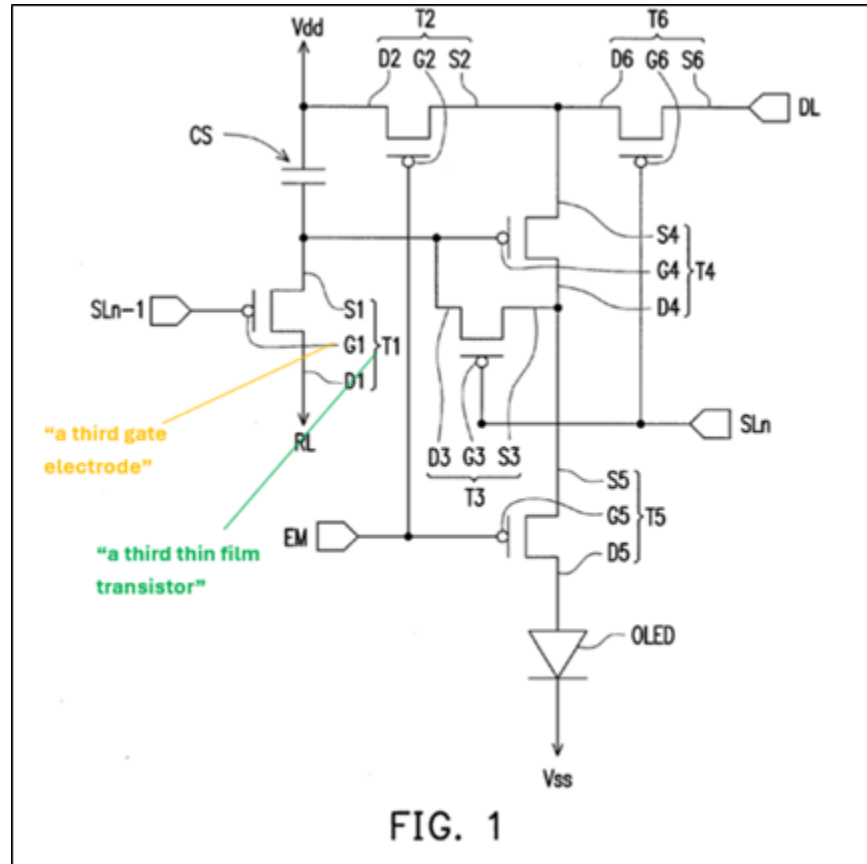
1. 17[a]: “The TFT array substrate of claim 14, further comprising a second gate line, and”

Liu100’s “*scan line SLn-1* is electrically connected to the gate G1” (Figure 1 (below)). (EX1007, [0038], [0064]; EX1002, ¶¶314-316.)



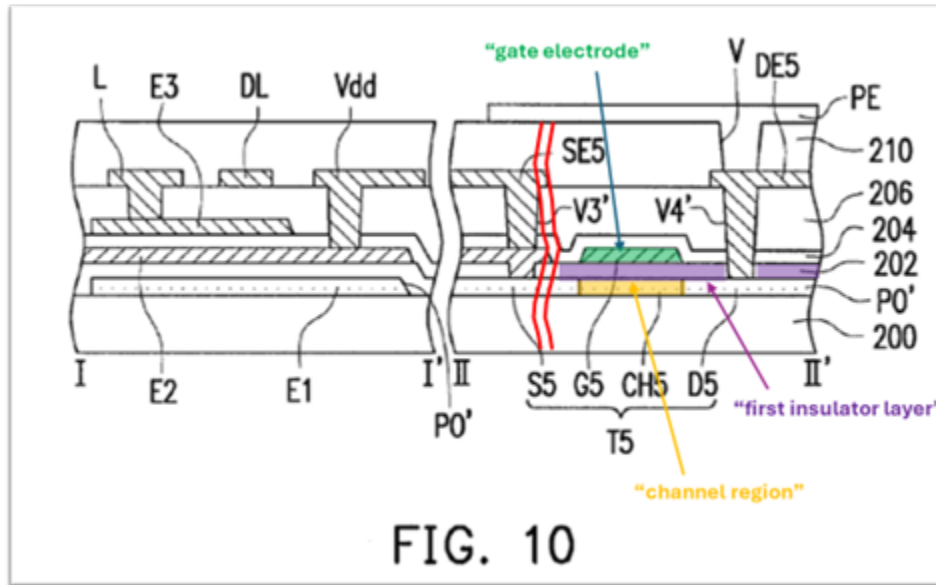
2. 17[b]: “a third thin film transistor, the third thin film transistor including a third gate electrode and a third channel region overlapping the third gate electrode, the third gate electrode and the third channel region being spaced apart from each other with the first insulating layer therebetween, and”

Liu100’s “first conductive layer M1 has a *gate G1* in the region predetermined for forming the first *thin film transistor T1*” and “a *channel region (not shown)* in a region predetermined for forming a *first thin film transistor T1*” (Figure 1 (below)). (EX1007, [0038], [0035]; EX1002, ¶¶317-318.)



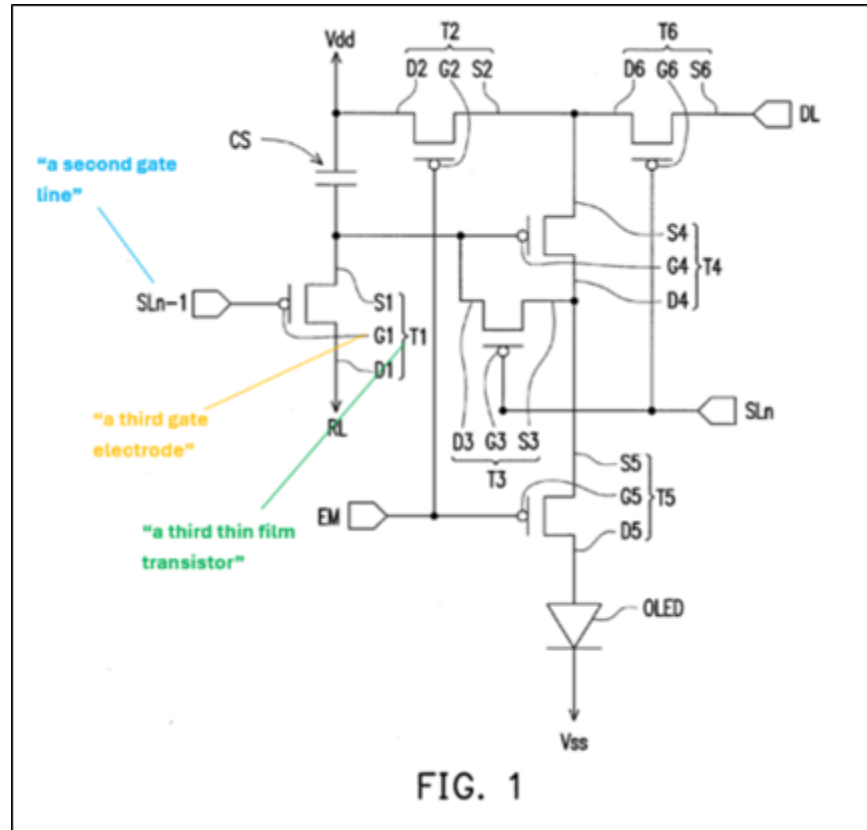
Liul00's Figure 10 (below) shows a "semiconductor layer PO' has a source region S5, a drain region D5 and a channel region CH5 in a region predetermined for forming a fifth thin film transistor T5." (EX1007, [0060].) "The first insulating layer 202 covers the semiconductor layer PO'." (EX1007, [0058].) "The first conductive layer M1' is disposed on the first insulating layer 202," where "the first conductive layer M1' has a gate G5 in the region predetermined for forming the fifth thin film transistor T5." (EX1007, [0063].) The *channel region* overlaps the *gate electrode*, and are spaced apart from each other with *insulating layer 202* ("first insulating layer" (1[b])) therebetween. Figure 10

specifically shows a cross-sectional view and structure for transistor T5, but it also represents the cross-sectional view and structure for the other transistors, including transistor T1. (See 1[c]; EX1002, ¶¶319-320.)



3. 17[c]: “wherein the second gate line is electrically connected to the third gate electrode.”

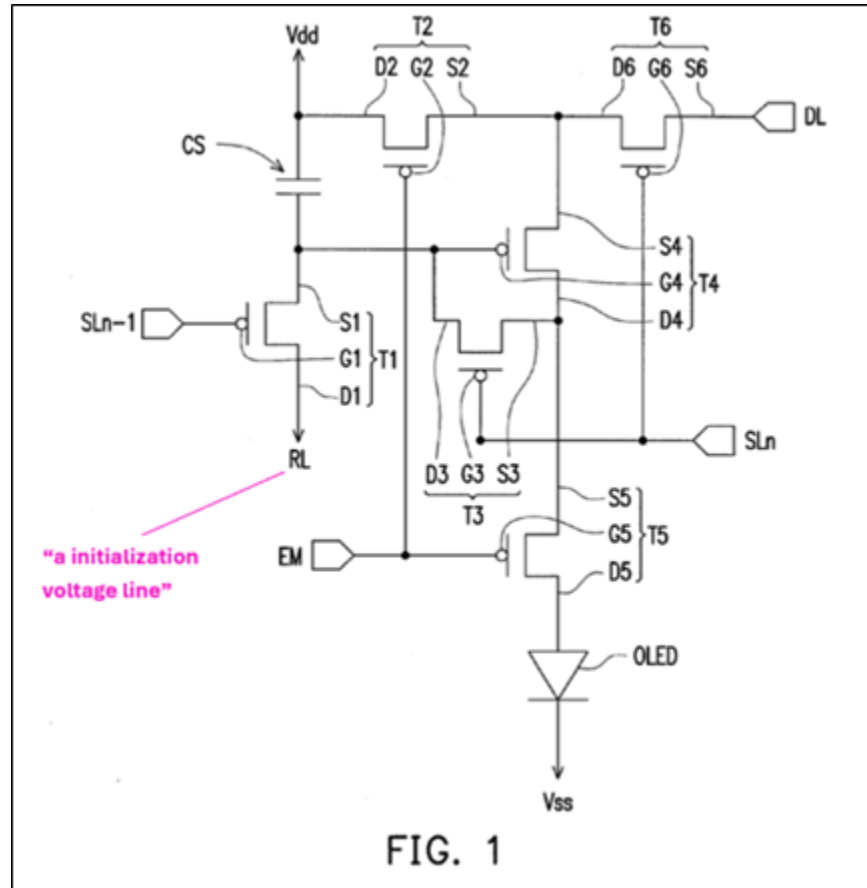
Liu100’s “*scan line SLn-1* is electrically connected to *gate G1*” (Figure 1 (below)). (EX1007, [0038], [0064]; EX1002, ¶¶321-322.)



M. Claim 18

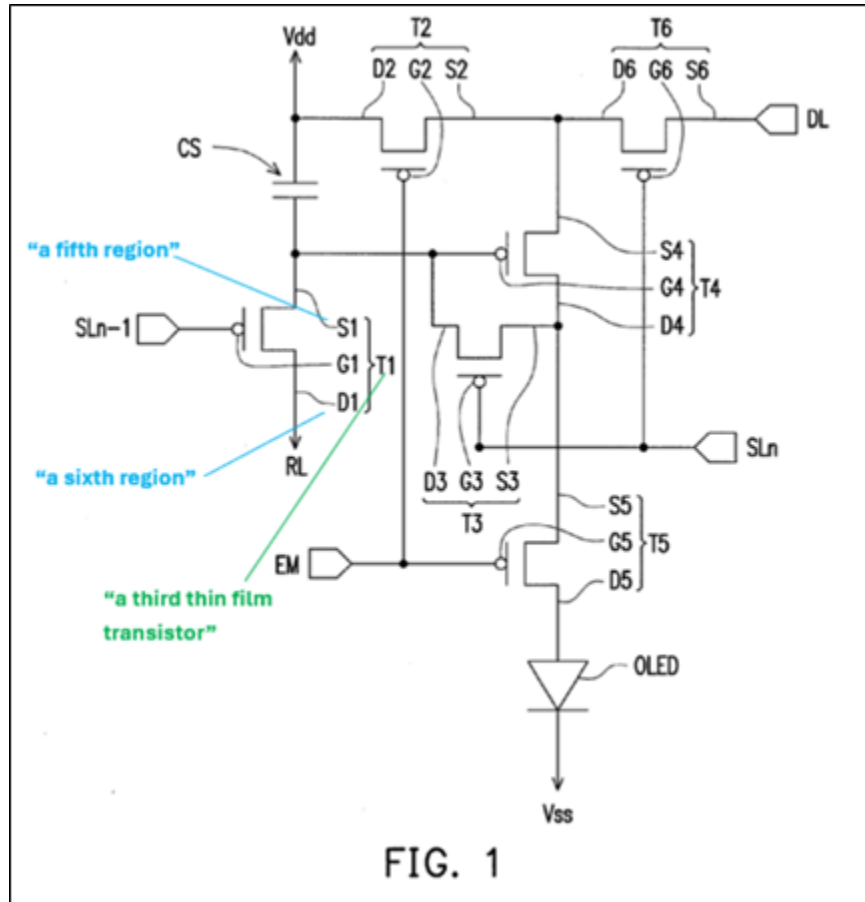
1. 18[a]: “The TFT array substrate of claim 17, further comprising a[n] initialization voltage line,”

Liu100’s “first conductive layer M1 ... comprise[s] a *reference signal line RL*” (Figure 1 (below)). (EX1007, [0038].) Transistor T1 is an initialization TFT configured to provide an initialization voltage to the gate of the driving transistor T4. (EX1002, ¶¶323-324.)

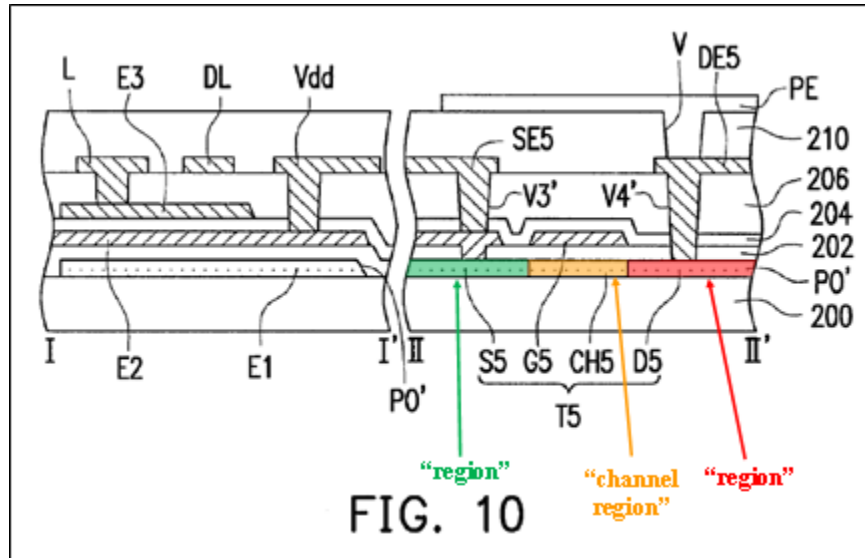


2. 18[b]: “wherein the third thin film transistor further comprises a fifth region adjacent to a side of the third channel region and a sixth region adjacent to another side of the third channel region, and”

Liu100’s “a channel region (not shown) in a region predetermined for forming a first thin film transistor T1” (Figure 1 (below)). (EX1007, [0035].) The *source region S1* is adjacent to a side of the *transistor T1* (including the channel region), and the *drain region D1* is adjacent to another side of the transistor T1 (including the channel region). (EX1002, ¶¶325-326.)

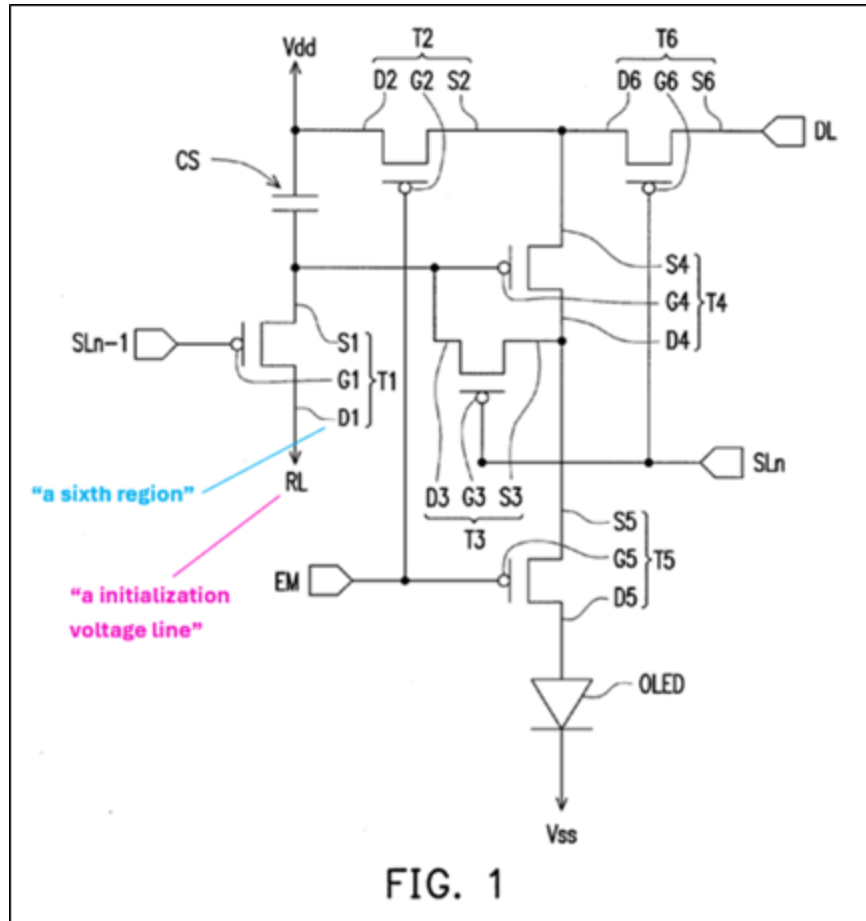


Liu100's transistors comprise a *source region* adjacent to a side of the *channel region* and a *drain region* adjacent to another side of the channel region, the structure of Figure 10 (below) being representative of all transistors, such as transistor T4. (See 1[c]; EX1007, [0058], [0060]; EX1002, ¶327.)



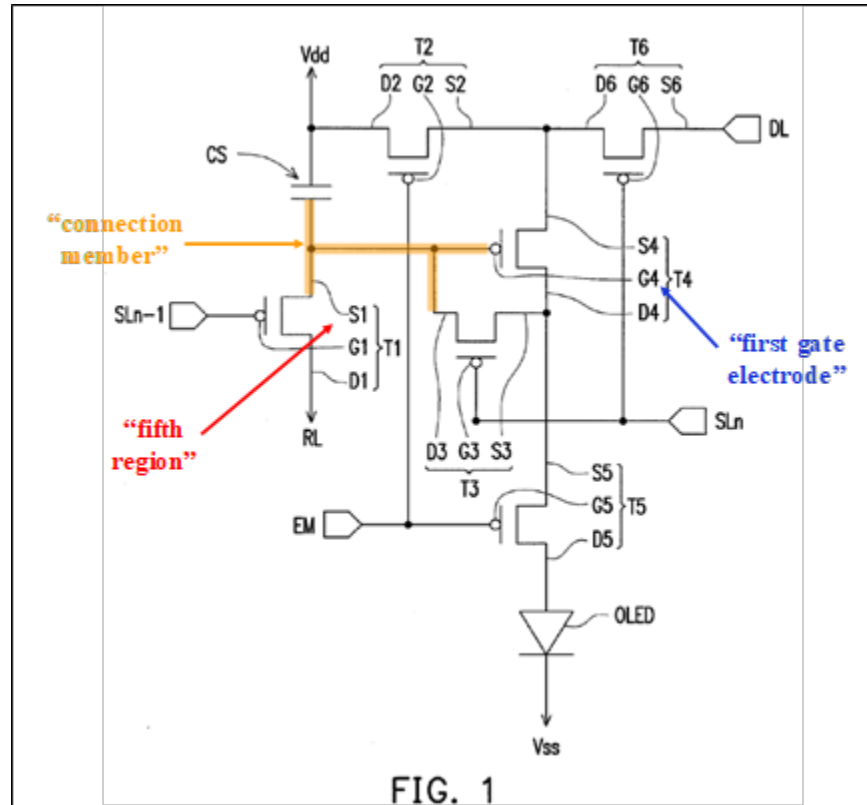
3. 18[c]: “the sixth region is electrically connected to the initialization voltage line.”

Liu100’s *drain region D1* (“sixth region” (18[b])) is electrically connected to *reference signal line RL* (“initialization voltage line” (18[a])) (Figure 1 (below)). (EX1002, ¶¶328-329.)



N. **Claim 19: “The TFT array substrate of claim 18, wherein the fifth region is electrically connected to the first gate electrode via the connection member.”**

Liu100's *source region S1* ("fifth region" (18[b])) is electrically connected to *gate G4* ("first gate electrode" (1[b])) via the *connection member* (Figure 1 (below)). (EX1002, ¶¶330-331.)



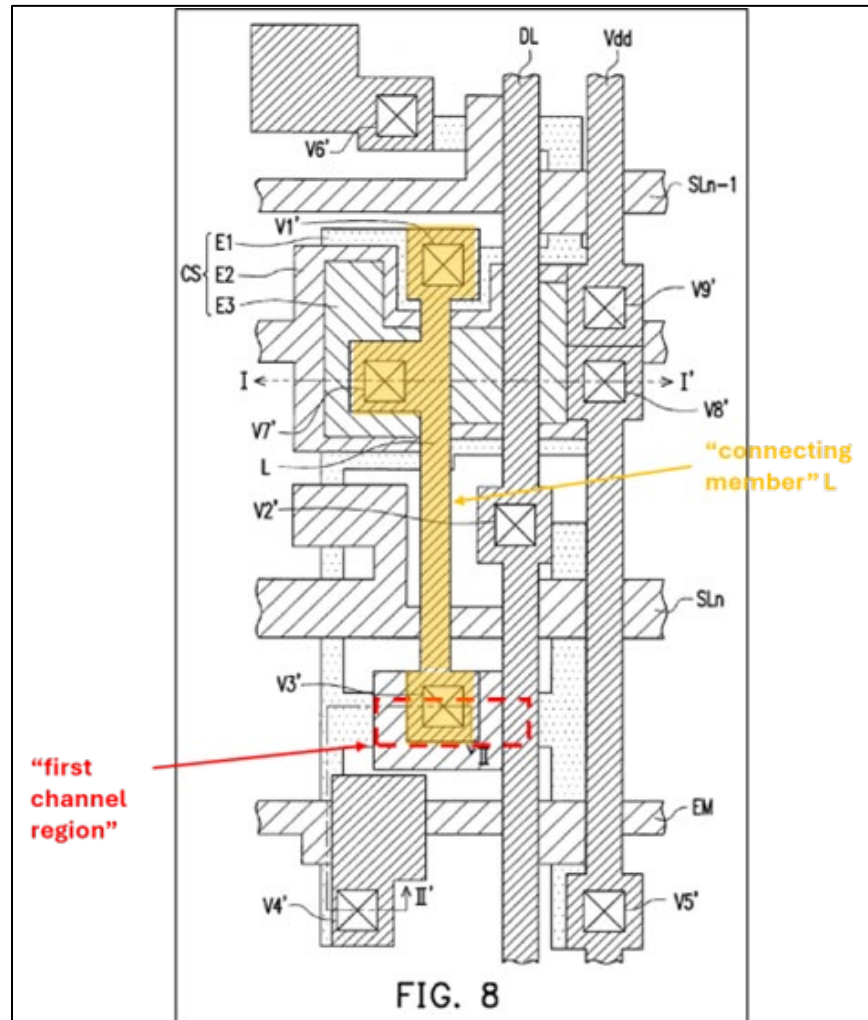
O. Claim 22

1. Element 22[pre]-22[g]

Elements 22[pre]-22[g] are similar to elements 1[pre]-1[g], which Liu100 and/or Ono teach. (EX1002, ¶¶332-339.)

2. 22[h]: “the connection member overlapping a portion of the first channel region in a plan view.”

Liu100’s transistor T4 (“first thin film transistor” (1[b])) comprises “a channel region (not shown).” (EX1007, [0035], [0077].) Figure 8 (below) shows *signal line L* (“connection member” (1[g])) overlapping a portion of the *channel region CH4* (“first channel region” (1[b])) of the transistor T4 in a plan view. (EX1002, ¶¶340-341.)



P. Claims 23, 24, 28, And 29

Claims 23, 24, 28, and 29 are similar to claims 2, 3, 12, and 13, which Liu100 and/or Ono teach. (EX1002, ¶¶342-345.)

XIII. GROUND 9: CLAIMS 7-10, 25, AND 26 ARE OBVIOUS OVER LIU100, ONO, AND OSAME

Liu100 and Ono teach claim 1 (*see* § XII.B). Osame teaches claims 7-10 (*see* § VII.B). Claims 25 and 26 are similar to claims 7 and 10, which Liu100, Ono, and Osame teach. (EX1002, ¶¶346, 351-359.)

It would have been obvious to a POSITA to combine the teachings of Liu100, Ono, and Osame. Liu100, Ono, and Osame are from the same field of endeavor. Liu100, Ono, and Osame all relate to organic light emitting display devices with an array of transistors efficiently using space in the device's pixel structure without compromising image quality. Liu100 discloses a pixel structure of an OLED device that "reduc[es] an area occupied by components of the pixel structure." (EX1007, [0007].) Ono discloses "a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor." (EX1008, [0030].) Osame discloses a "light-emitting device which realizes a high aperture ratio and in which the quality of image is little affected by the variation of the driving TFTs." (EX1014, [0030].) Liu100, Ono, and Osame are all reasonably pertinent to the same technical problem of efficiently using the space in the pixel structure of light-emitting devices. (EX1002, ¶347.)

Ono teaches a luminescent display device where "the gate electrode of the thin-film transistor is used not only simply as the gate electrode but also as one of two electrodes constituting the capacitor." (EX1008, [0029].) "[T]he capacitor can be formed above the thin-film transistor to overlap with the thin-film transistor, enabling efficient use of the pixel space." (*Id.*) This solves the conventional problem "when the number of capacitors or the capacitor area increases, the region

for forming other elements becomes smaller, resulting in less design flexibility.” (EX1008, [0008].) Ono teaches the gate electrode of the driving thin-film transistor in different pixel circuits is used as one of the capacitor electrode formed above the driving thin-film-transistor. (EX1008, [0070], [0091], [0113], [0124], Figs. 3, 4, 6-12). Osame’s technical features may be combined with the teachings of Liu100 and Ono with a reasonable expectation of success to generate a smaller light-emitting device where the storage capacitor has an increased capacitor area but without decreasing the device’s quality. (EX1002, ¶348.)

Osame teaches using semiconductor layers of different shapes in light-emitting devices to increase driving TFT channel length and width without decreasing aperture ratio. These technical features may be combined with the teachings of Liu100 and Ono with a reasonable expectation of success to generate a smaller light-emitting device where the storage capacitor has an increased capacitance but without decreasing the device’s aperture ratio. (EX1002, ¶349.)

A POSITA would be motivated to use the techniques disclosed in Osame and Ono to improve the similar device of Liu100 in the same way. Ono teaches placing a capacitor over a gate electrode of the driving transistor, which was known in the art, and it would be obvious to combine the teachings of Liu100 and Ono. This technique increases the overall capacitance of the pixel structure resulting in improved display performance without using additional area.

(EX1002, ¶350.)

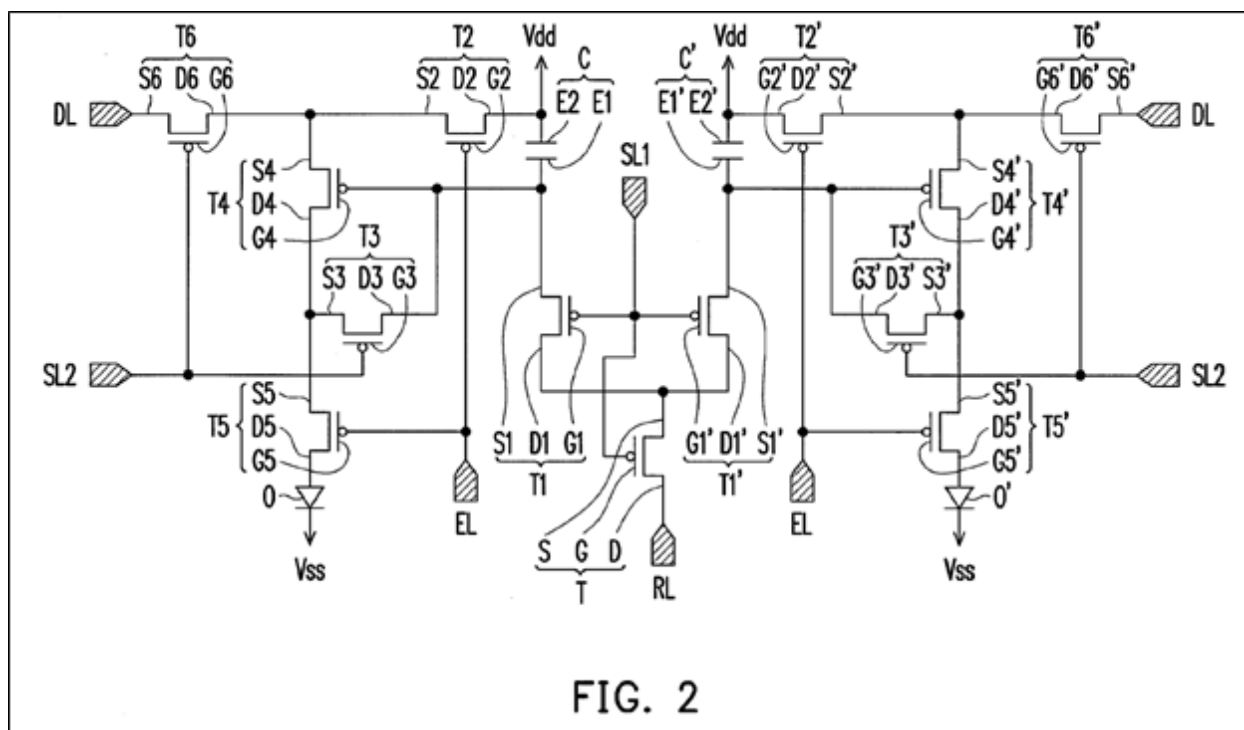
Osame demonstrated an OLED configuration with different shapes of the semiconductor layer's channel region of the driving transistor increased the design flexibility without compromising on device quality. There would have been a reasonable expectation of success for combining Liu100, Ono, and Osame by modifying the configuration of the shape of the semiconductor layer's channel region. (EX1002, ¶350.)

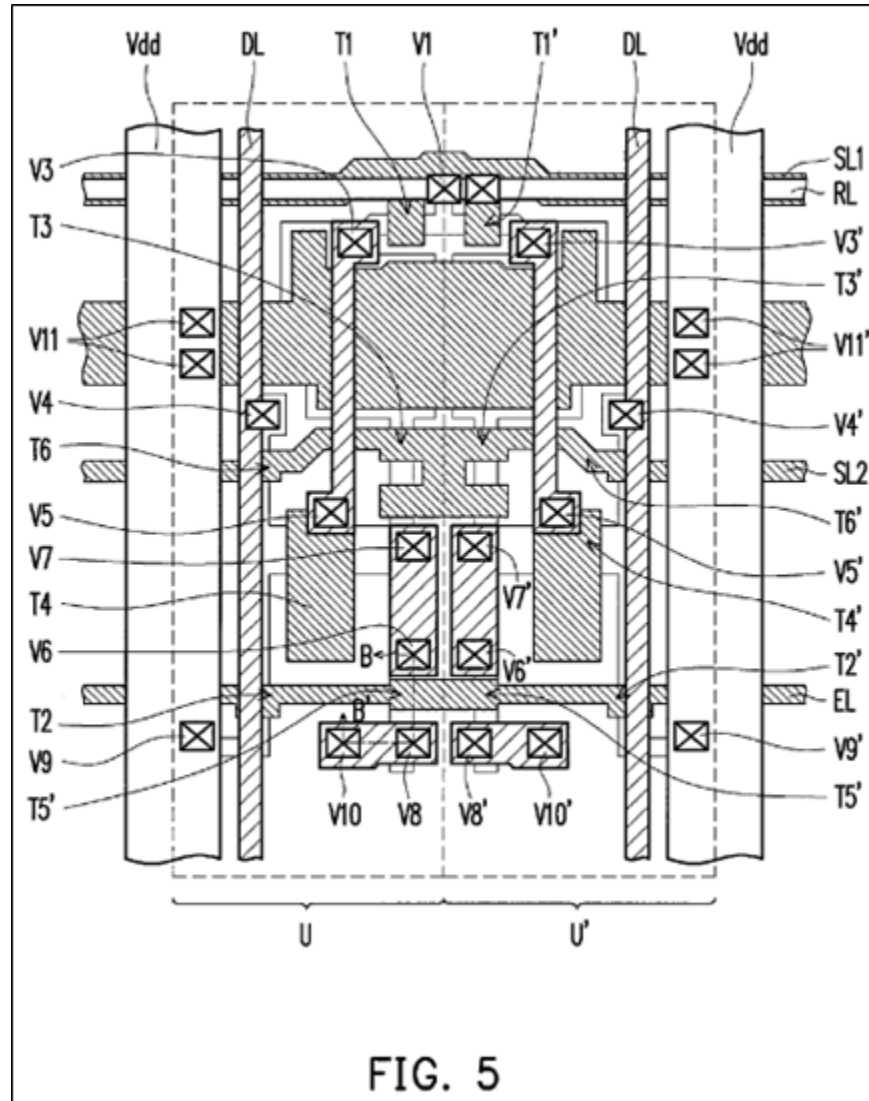
XIV. GROUND 10: CLAIMS 20 AND 21 ARE OBVIOUS OVER LIU100, ONO, AND LIU080

A. Summary Of Liu080

Liu080 discloses a pixel structure of an OLED device with reduced area by sharing a common TFT between two pixel units: “the first pixel unit and the second pixel unit of the pixel structure in the invention share the common TFT.” (EX1012, [0007], [0056]; EX1002, ¶360.)

Figures 2 and 5 (below) show the circuit and plan view, respectively, of Liu080's OLED device. (EX1002, ¶361.)





B. Claim 20: “The TFT array substrate of claim 18, wherein the initialization voltage line extends in the same direction as the first gate line.”

Liu080’s pixel circuit comprises a common transistor T (Figure 2 (below)) comprising a “common drain electrode D is electrically connected to the reference signal line RL.” (EX1012, [0024].) The figure shows the source of the common transistor T connected to the drain D1 of transistor T1. When the common transistor T is on, it sets the gate potential of transistor T1 to a reference voltage

from the *reference signal line RL* (“initialization voltage line” (18[a])) through the transistor T1, initializing the gate of transistor T1. *Scan line SL2* is a “first gate line” electrically connected to the gate electrode of the T6 (“second thin film transistor”). (See 1[c]; EX1002, ¶¶362-363.)

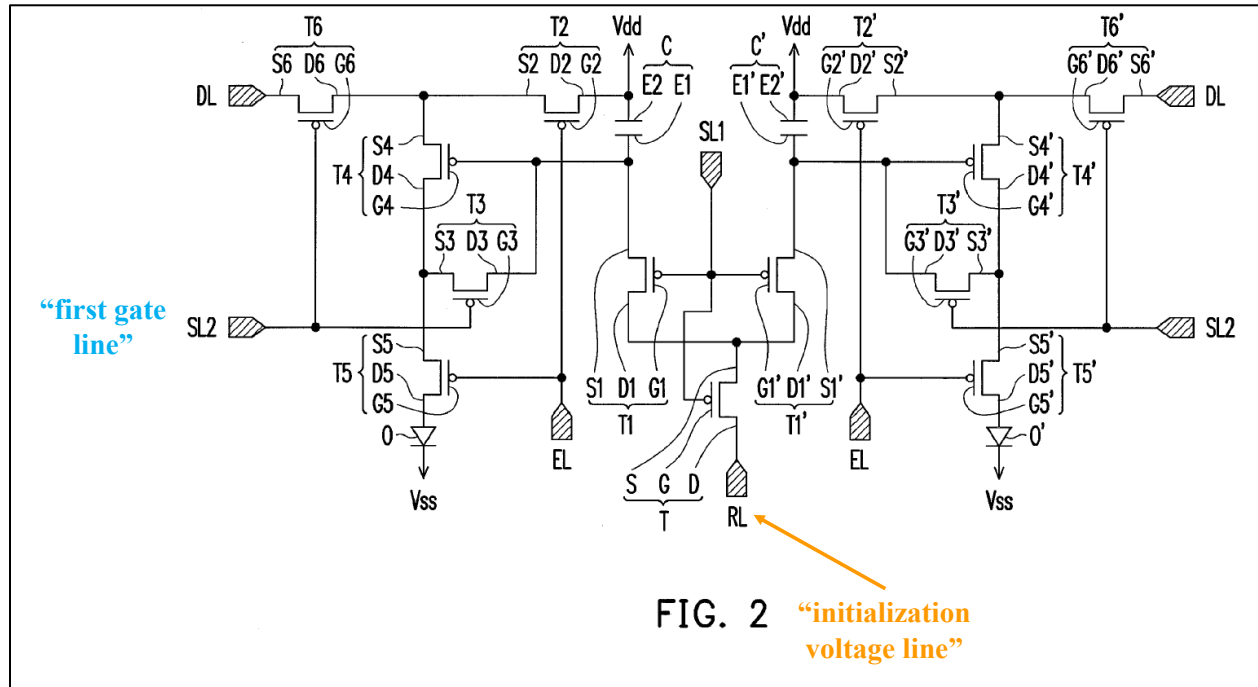
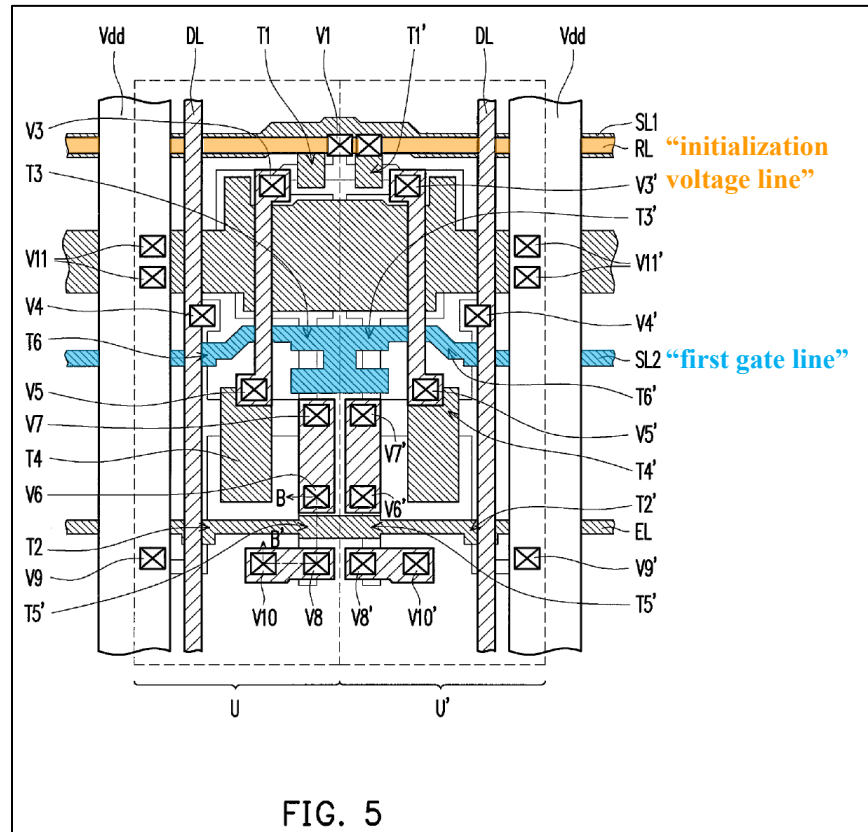


Figure 5 (below) shows “an extending direction of the *reference signal line RL* is parallel to an extending direction of the first scan line SL1 and the second *scan line SL2*.” (EX1012, [0022]; EX1002, ¶364.)



It would have been obvious to a POSITA to combine the teachings of Liu100, Ono, and Liu080. Liu100, Ono, and Liu080 are from the same field of endeavor. They relate to OLED devices with transistors and are directed to ways to efficiently use the spaces in the device's pixel structure for making the OLED devices smaller. Liu100 teaches an OLED device having a pixel structure "capable of reducing an area occupied by components of the pixel structure." (EX1007, [0007].) Ono teaches "a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor." (EX1008, [0030].) And similarly, Liu080 teaches "a pixel structure of an organic light emitting device, where the pixel structures each

can reduce an area occupied by components of the pixel structure.” (EX1012, [0007].) Liu100, Ono, and Liu080 are reasonably pertinent to the same technical problem of efficiently using the space to make the OLED devices smaller by reducing the area of the pixel structure. (EX1002, ¶365.)

Liu080 teaches “the first pixel unit and the second pixel unit of the pixel structure in the invention share the common TFT,” thereby “a pixel area occupied by the TFTs respectively in the first pixel unit and the second pixel unit of the pixel structure can be reduced.” (EX1012, [0056].) Liu080 explains “the area of the pixel structure is reduced for the pixel structure to be applied in high resolution product. The space saved in the pixel structure can also be used for disposing other devices or components when the pixel structure is not to be miniaturized.” (EX1012, [0056].) These technical features of Liu080 may be combined with the teachings of Liu100 and Ono to result in an OLED display with reduced area and space savings generated by sharing common TFTs among pixel units, thereby Liu080 improves upon Liu100 and Ono. Liu100 and Liu080 have similar circuits and are from the same inventor. For example, the circuits of Liu100 and Liu080 both comprise transistors T1-T6 having similar connections, *e.g.*, the transistor T1 connected to the bottom electrode of the capacitor, transistor T6 connected to transistor T4, transistor T3 connected to transistor T4. (EX1007, [0042], Fig. 1; EX1012, [0029], [0031], [0034], Fig. 2.) Given the overlap among Liu100, Ono,

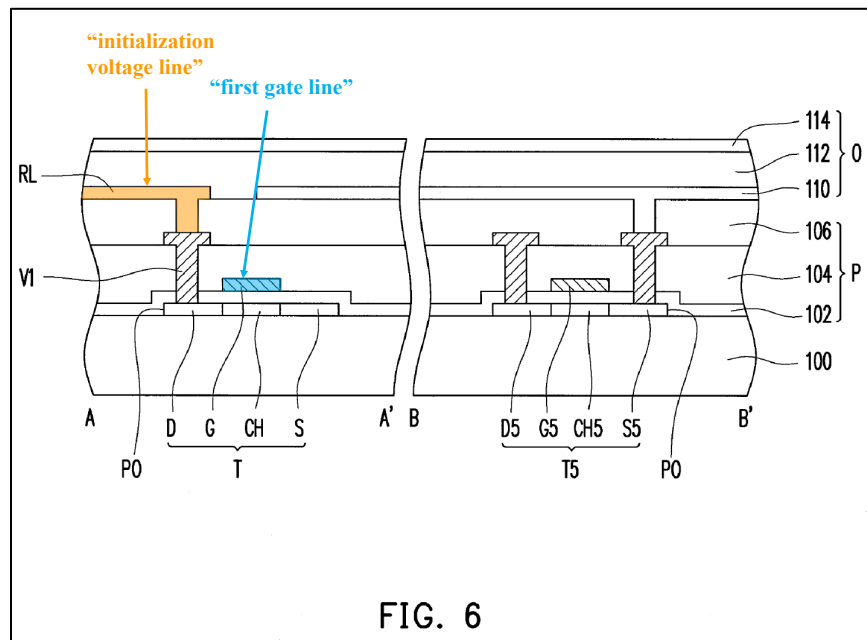
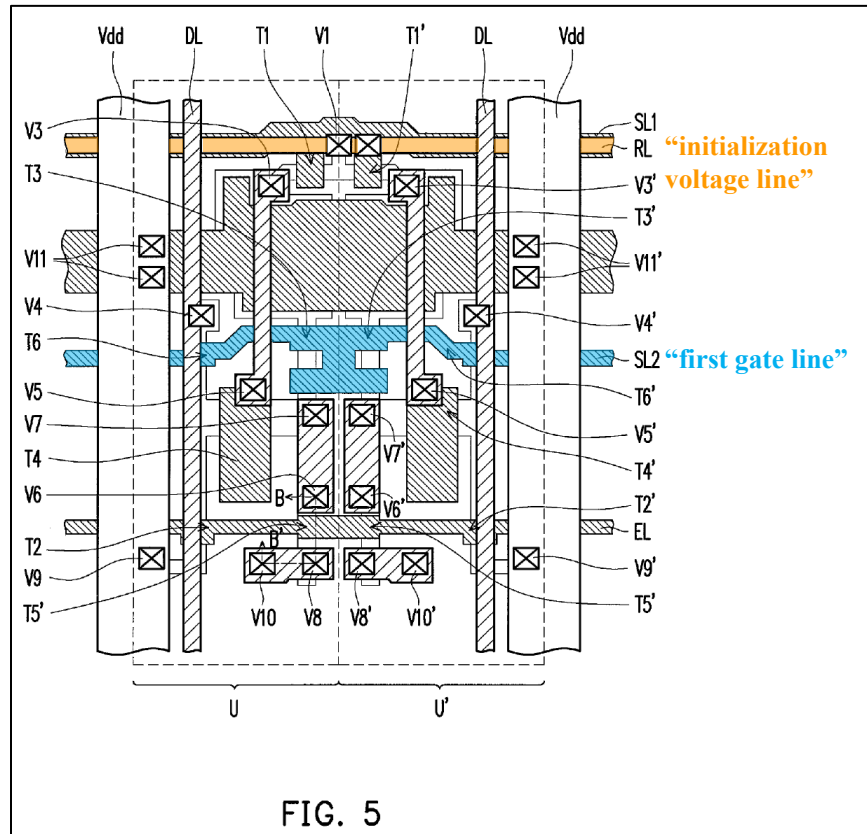
and Liu080, and the prior art has already known and demonstrated such techniques with success, there would have been a reasonable expectation of success.

(EX1002, ¶366.)

Because Liu100, Ono, and Liu080 relate to OLEDs and making OLED devices smaller, a POSITA would have been motivated to use the techniques disclosed in Liu080 to improve the similar devices of Liu100 and Ono in the same way. Liu100 shares transistors, such as taught by Liu080, to reduce the pixel area occupied by the TFTs. It would have been obvious to combine the references and their teachings. (EX1002, ¶367.)

C. Claim 21: “The TFT array substrate of claim 18, wherein the initialization voltage line is formed of a different layer from the first gate line.”

Liu080’s “reference signal line RL can be disposed in overlap with the first scan line SL. ... the reference signal line RL is disposed on top of the first scan line SL1.” (EX1012, [0055].) Figure 5 (below) shows the *reference signal line RL* (“initialization voltage line” (18[a])) disposed on top of SL1, formed on the same layer (“substantially parallel” ([0022])) as *scan line SL2* (“first gate line” (claim 14)). Figure 6 (below) shows the reference signal line RL is formed of a different layer from the scan line SL1. (EX1002, ¶¶368-370.)



It would have been obvious to a POSITA to combine the teachings of Liu100, Ono, and Liu080. (See claim 20.)

XV. THE BOARD SHOULD NOT DENY INSTITUTION UNDER *FINTIV*³

A. A Final Written Decision Will Issue Before Any Trial

A schedule has not yet been issued, and no trial date has been set, in the corresponding district court litigation. A Final Written Decision will issue in October 2026, whereas the trial date for the district court case (which has not been set) will likely be after.

B. Merits Of The Petition Support Institution

As discussed above, the prior art teaches every element of the challenged claims, and are unpatentable. Thus, the merits of the petition weigh strongly in favor of institution. *See* Stewart Memorandum, 2 (“The strength of the unpatentability challenge” is a relevant consideration).

XVI. THE BOARD SHOULD NOT DENY INSTITUTION UNDER 35 U.S.C. § 325(D)

The Petition does not raise the same or substantially the same art previously presented to the Office, nor does the Petition raise the same or substantially the

³ Petitioner is not addressing in full discretionary issues in the Petition per USPTO guidance. *See FAQs for Interim Processes for PTAB Workload Management*, USPTO, <https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management> (last visited Aug. 28, 2025).

same arguments previously presented to the Office in the examination of the '483 patent. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020).

The Board applies a two-part framework for determining whether to deny institution under § 325(d) in view of prosecution of the original patent application and any subsequent reexamination: “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential).

Here, the Board need not reach the second part of the test, because the first part fails: neither the same (or substantially the same) art or arguments were previously presented to the Office. None of the references presented in this petition—Park, Zhan, Ono, Liu100, or Liu080—were considered during prosecution of the '483 patent.

Even if the Board were to conclude otherwise, the Office erred in a material manner. The Examiner allowed the claims without even identifying the prior art of this petition. Where the examination record is not well developed, as here, it may

indicate that the Examiner erred by “overlook[ing] something persuasive.”

Advanced Bionics, IPR2019-01469, Paper 6 at 10.

For all the foregoing reasons, the Board should decline to deny the petition under § 325(d).

XVII. NOTICES AND STATEMENTS

Pursuant to 37 C.F.R. § 42.8(b)(1), BOE Technology Group Co., Ltd., is the real party-in-interest for Petitioner.

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner identifies the following related matters.

- *Samsung Display Co., Ltd., v. BOE Technology Group Co., Ltd., et al.*, No. 2:25-cv-00430 (E.D. Tex.)
- *Samsung Display Co., Ltd., v. BOE Technology Group Co., Ltd., et al.*, No. 2:25-cv-00426 (E.D. Tex.)
- IPR2025-01499

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioner identifies the following counsel (and a power of attorney accompanies this Petition).

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Pursuant to 37 C.F.R. § 42.8(b)(4), service information for lead and back-up counsel is provided above. Petitioner consents to electronic service by email to BOE-Samsung-IPR@mofo.com.

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '483 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

The USPTO is authorized to charge any required fees, including the fee as set forth in 37 C.F.R. § 42.15(a) and any excess claim fees, to Deposit Account No. **03-1952** referencing Docket No. **37294-00000.05.**

Dated: August 31, 2025

Respectfully submitted,

By /s/ Alex S. Yap

Alex S. Yap

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Attorney for Petitioner

Certification of Word Count (37 C.F.R. § 42.24)

I hereby certify that this Petition for *Inter Partes* Review has 13,843 words (as counted by the “Word Count” feature of the Microsoft Word™ word-processing system), exclusive of “a table of contents, a table of authorities, mandatory notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing.”

Dated: August 31, 2025

By /s/ Alex S. Yap

Alex S. Yap

Certificate of Service (37 C.F.R. § 42.6(e)(4) and 42.205(a))

I hereby certify that the attached Petition for *Inter Partes* Review and supporting materials were served as of the below date by Priority Mail Express® on the Patent Owner at the correspondence address indicated for Patent No. 10,720,483.

Lewis Roca Rothgerber Christie LLP
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A courtesy copy of the attached Petition for *Inter Partes* Review and supporting materials were also served on the following litigation counsel:

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Dated: August 31, 2025

By /s/ Alex S. Yap
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