

(19) Japan Patent Office (JP)

(12) Gazette of Unexamined
Patent Applications (A)

(11) Publication Number
2003-167533 (P2003-167533A)

(43) Publication Date June 13, 2003 (2003.6.13)

(51) Int. Cl. ⁷	ID Codes	FI	Theme Codes (Ref.)
G09F 9/30	338 365	G09F 9/30	338 365Z 5C094
H01L 21/336 29/786		H05B 33/14 H01L 29/78	A 614 612Z
H05B 33/14			

Examination Request: Received No. of Claims: 4 OL (Total of 8 pages)

(21) Appl. No.: 2001-370247 (P2001-370247)
(22) Filing Date: Dec. 4, 2001 (2001.12.4)

(71) Applicant 000003078
Toshiba Corporation
1-1-1, Shibaura, Minato-ku, Tokyo
(72) Inventor
Hiroshi NAKAYAMA
Toshiba Corporation, Fukaya Complex
1-9-2, Hatara-cho, Fukaya, Saitama-ken
(74) Agent 100058479
Takehiko SUZUE (and 6 others)

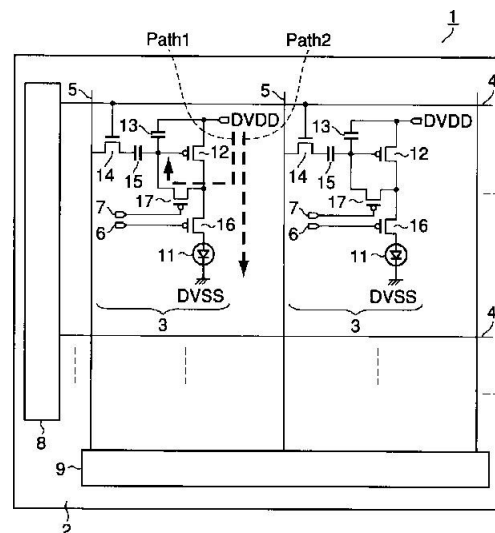
Continued on last page

(54) [Title of the Invention] Display Device

(57) [Abstract]

[Problem] To provide a display device that is less susceptible to variations in the ratio of the electrostatic capacitance of the holding capacitor to the electrostatic capacitance of the kick capacitor.

[Solution] The present invention is a display device 1 comprising: a plurality of scanning lines 4 arranged on a substrate 2 and a plurality of signal lines 5 arranged substantially perpendicular to the scanning lines 4; pixel switches 14 arranged near the intersections of the scanning lines 4 and the signal lines 5; a first capacitor 13 and a second capacitor 15 that hold video signals supplied from the signal lines 5 via the pixel switches 14 for a predetermined period of time; and display elements 11 that perform display operations based on the video signals, the display device characterized in that first capacitor 13 and the second capacitor 15 are configured with the same layer structure on the same plane.



[Claims]

[Claim 1] A display device, comprising: a plurality of scanning lines arranged on a substrate and a plurality of signal lines arranged substantially perpendicular to the scanning lines; pixel switches arranged near the intersections of the scanning lines and the signal lines;

a first capacitor and a second capacitor that hold video signals supplied from the signal lines via the pixel switches for a predetermined period of time; and

display elements that perform display operations based on the video signals, the display device characterized in that the first capacitor and the second capacitor are configured with the same layer structure on the same plane.

[Claim 2] A display device, comprising:

a plurality of scanning lines arranged on a substrate and a plurality of signal lines arranged substantially perpendicular to the scanning lines;

a first transistor having a gate electrode connected to a scanning line and a source electrode connected to a signal line;

a first capacitor having a dielectric film between a pair of electrodes, one of the electrodes being connected to the drain electrode of the first transistor;

a second transistor having a gate electrode connected to the other electrode of the first capacitor and a source electrode connected to a first power supply line;

a second capacitor having a dielectric film between a pair of electrodes, one electrode being connected to the gate electrode of the second transistor and the other electrode being connected to the source electrode of the second transistor;

a third transistor whose gate electrode is connected to a first control line, whose source electrode is connected to the drain electrode of the second transistor, and whose drain electrode is connected to the gate electrode of the second transistor;

a fourth transistor whose gate electrode is connected to a second control line and whose source electrode is connected to the drain electrode of the second transistor; and

a display element having a light modulating layer between a pair of electrodes, one of the electrodes being connected to the drain electrode of the fourth transistor,

the display device characterized in that the dielectric film constituting the first capacitor and the dielectric film constituting the second capacitor are configured with the same layer structure on the same plane.

[Claim 3] The display device according to claim 2, wherein at least one of the first to fourth transistors has a gate insulating film that is the same as the dielectric film constituting the first and second capacitors.

[Claim 4] The display device according to any one of claim 1 to claim 3, wherein the display element is an organic electroluminescent display element.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention] The present invention relates to a display device.

[0002]

[Prior Art] Organic electroluminescence ("organic EL") display devices are lightweight, thin, and highly luminous. For this reason, organic EL display devices have recently attracted attention as monitor displays for portable information devices such as mobile phones.

[0003] An organic EL display device is typically configured to display images using display pixels arranged in a matrix. In such an organic EL display device, scanning lines and signal lines are arranged along the rows and columns of the display pixels, respectively. Each display pixel is composed primarily of an organic EL element, a drive transistor connected in series between a pair of power supply lines to the organic EL element, a holding capacitor that holds the gate voltage of the drive transistor, and a pixel switch that controls the gate voltage of the drive transistor.

[0004] In such an organic EL display device, each display pixel also has a kick capacitor, a reset switch, and an output switch, and can include a threshold cancellation circuit. In an organic EL display device including such a threshold cancellation circuit, variations in the drive current can be prevented based on variations in the threshold voltage of the drive transistor.

[0005] However, in such an organic EL display device, if there is a variation in the ratio of the electrostatic capacitance of the holding capacitors to the electrostatic capacitance of the kick capacitor between display pixels, a variation in the drive current will occur between those display pixels. In addition, if there is a variation in the ratio of the electrostatic capacitance of the holding capacitor to the electrostatic capacitance of the kick capacitor between display devices, a variation in the drive current will occur between those display devices. Thus, variations in the ratio of the electrostatic capacitance of the holding capacitor to the electrostatic capacitance of the kick capacitor should be suppressed as much as possible.

However, it has been difficult to suppress such variations in organic EL display devices of the prior art.

[0006]

[Problem to Be Solved by the Invention] In light of this problem, it is an object of the present invention to provide a display device that is less susceptible to variations in the ratio of the electrostatic capacitance of the holding capacitor to the electrostatic capacitance of the kick capacitor.

[0007] It is another object of the present invention to reduce fluctuations in the video signals supplied to the display elements.

[0008]

[Means for Solving the Problem] In order to solve this problem, the present invention provides a display device, comprising: a plurality of scanning lines arranged on a substrate and a plurality of signal lines arranged substantially perpendicular to the scanning lines; pixel switches arranged near the intersections of the scanning lines and the signal lines; a first capacitor and a second capacitor that hold video signals supplied from the signal lines via the pixel switches for a predetermined period of time; and display elements that perform display operations based on the video signals, the display device characterized in that first capacitor and the second capacitor are configured with the same layer structure on the same plane.

[0009] The present invention also provides a display device, comprising: a plurality of scanning lines arranged on a substrate and a plurality of signal lines arranged substantially perpendicular to the scanning lines; a first transistor having a gate electrode connected to a scanning line and a source electrode connected to a signal line; a first capacitor having a dielectric film between a pair of electrodes, one of the electrodes being connected to the drain electrode of the first transistor; a second transistor having a gate electrode connected to the other electrode of the first capacitor and a source electrode connected to a first power supply line; a second capacitor having a dielectric film between a pair of electrodes, one electrode being connected to the gate electrode of the second transistor and the other electrode being connected to the source electrode of the second transistor; a third transistor whose gate electrode is connected to a first control line, whose source electrode is connected to the drain electrode of the second transistor, and whose drain electrode is connected to the gate electrode of the second transistor; a fourth transistor whose gate electrode is connected to a second control line

and whose source electrode is connected to the drain electrode of the second transistor; and a display element having a light modulating layer between a pair of electrodes, one of the electrodes being connected to the drain electrode of the fourth transistor, the display device characterized in that the dielectric film constituting the first capacitor and the dielectric film constituting the second capacitor are configured with the same layer structure on the same plane.

[0010] In the present invention, switching elements such as transistors and diodes can be used as pixel switches, output switches, and reset switches.

[0011] In the present invention, at least one of the drive control element, the pixel switch transistor, the output switch transistor, and the reset switch transistor may be a thin-film transistor, and the gate insulating film of this transistor may be the same as the dielectric film constituting the capacitance of the holding capacitor and the dielectric film constituting the capacitance of the kick capacitor.

[0012] In the present invention, the display elements are not particularly limited to display elements whose optical characteristics change in response to the drive voltage or drive current. For example, the display elements can be display elements whose luminous intensity changes in response to the drive current, such as organic electroluminescent display elements, and display elements whose transmittance or reflectance changes in response to the drive voltage, such as liquid crystal display elements.

[0013] Note that "the dielectric film constituting the (capacitance of the) holding capacitor being the same as the dielectric film constituting the (capacitance of the) kick capacitor" means these dielectric films were formed at the same time from the same material. This characteristic can be confirmed, for example, by examining the cross-sectional structure of the display device. In other words, if the cross section of these dielectric films is continuous, the dielectric films can be judged to be the same. Also, if the cross section of these dielectric films is discontinuous but there are no structural features indicating that the dielectric films were formed separately and the composition and thickness of the dielectric films are nearly the same, the dielectric films can be judged to be the same.

[0014] Similarly, "the gate insulating film being the same as the dielectric film constituting the (capacitance of the) holding capacitor and the dielectric film constituting the (capacitance of the) kick capacitor" means the dielectric film and gate insulating film are formed at the same

time from the same material. This characteristic can be confirmed, for example, by examining the cross-sectional structure of the display device. In other words, if the cross section of these dielectric films and the gate insulating film is continuous, the dielectric films can be judged to be the same. Also, if the cross section of these dielectric films and the gate insulating film is discontinuous but there are no structural features indicating that the dielectric films and gate insulating film were formed separately and the composition and thickness of the dielectric films and the gate insulating film are nearly the same, the dielectric films can be judged to be the same.

[0015]

[Embodiments of the Invention] Embodiments of the present invention will now be described in detail with reference to the drawings. In each of the drawings, identical or similar elements are denoted by the same reference numbers and redundant description of these elements has been omitted.

[0016] FIG. 1 is a circuit diagram that schematically represents the display device in an embodiment of the present invention. In this embodiment, the display elements are organic EL display elements.

[0017] The display device 1 shown in FIG. 1 is an organic EL display device comprising a substrate 2 such as a glass substrate, a plurality of display pixels 3 arranged in a matrix on the substrate 2, a plurality of scanning lines 4 and a plurality of signal lines 5 extending along the rows and columns of the display pixels 3, and a scanning line driver 8 and signal line driver 9 for driving the scanning lines 4 and signal lines 5. Each display pixel 3 includes a display element 11, a drive control element 12, a holding capacitor 13, a pixel switch 14, a kick capacitor 15, an output switch 16, and a reset switch 17. Note that here transistors are used for each of the drive control element 12, pixel switch 14, output switch 16, and reset switch 17. For example, the pixel switch 14 can be configured with an N-type transistor, and the drive control element 12, output switch 16, and reset switch 17 can be configured with P-type transistors.

[0018] The display element 11, output switch transistor 16, and drive control element 12 are connected in series between a pair of power supply lines DVDD, DVSS in successive order from the DVSS power supply line to the DVDD power supply line. The pixel switch transistor 14 and kick capacitor 15 are connected in series between a signal line 5 and the gate electrode of the drive control element 12 in successive order from the signal line 5 to the drive control element 12. The gate electrode of the pixel

switch transistor 14 is connected to a scanning line 4. The holding capacitor 13 is connected between the power supply line DVDD and the gate electrode of the drive control element 12, and the reset switch transistor 17 is connected between the output switch transistor 16 and the gate electrode of the drive control element 12 on the drive control element 12 side. In addition, the gate electrode of the output switch transistor 16 and the gate electrode of the reset switch transistor 17 are connected, respectively, to control lines 6 and 7.

[0019] In this display device 1, the potential of the power supply line DVDD can be set to, for example, +10V, and the potential of the power supply line DVSS can be set to, for example, 0V. When the pixel switch transistor 14 is driven by a scanning signal supplied from the scanning line 4, it applies the video signal voltage supplied from the signal line 5 to the gate electrode of the drive control element 12. The drive control element 12 supplies a drive current corresponding to the video signal voltage to the organic EL display element 11. An organic EL display element 11 has a structure in which light-emitting layers, which are thin film containing, for example, red, green, or blue fluorescent organic compounds, are sandwiched between a cathode and an anode. In such an organic EL display element 11, electrons and holes are injected into the light-emitting layers to cause their recombination, thereby generating excitons, and light emission occurs when these excitons deactivate.

[0020] The signal line driver 9 supplies video signal voltages to a plurality of signal lines 5 in parallel during each horizontal scanning period. The scanning line driver 8 sequentially supplies scan signals to a plurality of scanning lines 4 during each vertical scan period. Each pixel switch transistor 14 is rendered conductive for one horizontal scanning period by a scanning signal supplied from one of these scanning lines 4, and remains non-conductive until a scanning signal is once again supplied after one vertical scanning period. The drive control elements 12 in one row supply drive current corresponding to the video signal voltages supplied from a plurality of signal lines 5 to the organic EL display elements 11 by rendering these pixel switch transistors 14 conductive.

[0021] In addition, the signal line driver 9 is configured to temporarily output a predetermined reset voltage prior to outputting video signal voltages. In this display device 1, when supplying a reset voltage via the pixel switch transistor 14, control signals from the control lines 6, 7 cause the reset switch transistors 17 to be rendered conductive and

the output switch transistors 16 to remain non-conductive. At this time, the potential of the gate electrode of the drive control element 12 rises to equal the threshold voltage V_{th} of the drive control element 12 due to the current flowing through Path1.

[0022] Next, a video signal voltage is supplied through pixel switch transistor 14, and control signals from control lines 6, 7 cause the reset switch transistor 17 to remain non-conductive and the output switch transistor 16 to be rendered conductive. As a result, the potential of the gate electrode of the drive control element 12 rises to the level of the threshold voltage V_{th} plus the video signal voltage, and the drive current flows through Path2.

[0023] When video is displayed using this method, the drive current is determined by the difference between the reset voltage and the video signal voltage. Therefore, even if there is variation in the threshold voltages between drive control elements 12, it is possible to prevent variation in the drive current caused by the variation in the threshold voltages.

[0024] In the organic EL display device 1 of the present embodiment, the dielectric film that constitutes the capacitance of the holding capacitor 13 is the same as the dielectric film that constitutes the capacitance of the kick capacitor 15. Using this configuration, variations in the ratio of the capacitance of the holding capacitor 13 to the capacitance of the kick capacitor 15 can be suppressed. This will now be explained with reference to FIG. 2.

[0025] FIG. 2 is a cross-sectional view of a portion of the organic EL display in an embodiment of the present invention. In the structure shown in FIG. 2, one of the electrodes 13a of the holding capacitor 13, one of the electrodes 15a of the kick capacitor 15, and a poly-Si film 20a constituting the source-drain region and channel region of the thin-film transistor 20 are arranged on the insulating film 21 formed on the substrate 2, and these are covered by a dielectric film (or insulating film) 22. The other electrode 13b of the holding capacitor 13, the other electrode 15b of the kick capacitor 15, and the gate electrode 20b of the thin-film transistor 20 are arranged side by side on this dielectric film 22, and are covered by an interlayer insulating film 23. The source electrode 20c and drain electrode 20d are provided on the interlayer insulating film 23, and are connected to the source and drain regions of the poly-Si film 20a via contact holes provided in the insulating films 22, 23. Reference number 24 denotes a passivation film. The transistor 20 represents at least one of transistors 12, 14, 16, and 17 shown in FIG. 1.

[0026] The thickness of the dielectric film that constitutes the capacitance of the holding capacitor 13 and the thickness of the dielectric film that constitutes the capacitance of the kick capacitor 15 are ideally uniform throughout the entire display device 1, but in reality, some variation occurs. These variations in film thickness cause variations in both the electrostatic capacitance of the holding capacitor 13 and the electrostatic capacitance of the kick capacitor 15.

[0027] These variations in capacitance do not significantly affect the drive current as long as the ratio of film thicknesses remains nearly constant between the three display pixels. However, in the prior art, dielectric layers with different dielectric constants are used for the holding capacitor 13 and the kick capacitor 15. In other words, the dielectric film constituting the capacitance of the holding capacitor 13 is formed in a separate process from the dielectric film constituting the capacitance of the kick capacitor 15.

[0028] Normally, there is no correlation between film thickness distributions in thin films formed separately. Therefore, in the prior art, variations in the film thickness ratio occur, resulting in variations in the drive current between display devices 1 and between display pixels 3.

[0029] In contrast, as shown in FIG. 2, when the same dielectric film 22 is used for the capacitance of the holding capacitor 13 and the capacitance of the kick capacitor 15, there is no variation in the film thickness ratio due to the formation of different dielectric films. Also, because the holding capacitor 13 and the kick capacitor 15 are arranged in close proximity to each other, the film thickness of the holding capacitor 13 and the film thickness of the kick capacitor 15 do not differ greatly within each display pixel 3. Therefore, as shown in FIG. 2, by using the same dielectric film 22 for the capacitance of the holding capacitor 13 and the capacitance of the kick capacitor 15, variations in the film thickness ratio, that is, variations in the drive current between display devices 1 and between display pixels 3, can be suppressed.

[0030] The present inventor has performed the following simulation to confirm the effect of using the same dielectric film for the capacitance of the holding capacitor 13 and the capacitance of the kick capacitor 15.

[0031] FIG. 3 is a cross-sectional view showing a portion of an organic EL display device in which the dielectric film constituting the capacitance of the holding capacitor is different from the dielectric film constituting the capacitance of the kick capacitor.

[0032] In the structure shown in FIG. 3, one of the electrodes 15a of the kick capacitor 15 and the poly-Si film 20a constituting the source-drain region and channel region of the thin-film transistor 20 are arranged side by side on the insulating film 21 formed on the substrate (not shown), and these are covered with an insulating film (or dielectric film) 22. The other electrode 15b of the kick capacitor 15 and the gate electrode 20b of the thin-film transistor 20 are arranged side by side on top of the insulating film 22, and these are covered by the interlayer insulating film 23. In the structure shown in FIG. 3, electrode 15b also serves as one of the electrodes of the holding capacitor 13. The other electrode 13b of the holding capacitor 13, the source electrode 20c, and the drain electrode 20d are arranged side by side on the interlayer insulating film 22, and these are covered with a passivation film 24. The source electrode 20c and drain electrode 20d are connected to the source and drain regions of the poly-Si film 20a via contact holes provided in the insulating films 22, 23.

[0033] In the organic EL display device 1 shown in FIG. 3, when the thickness of the dielectric film of the holding capacitor 13 and the thickness of the dielectric film of the kick capacitor 15 vary within a range of $\pm 10\%$, the drive current varies within a range of $\pm 30\%$ relative to the center conditions. Meanwhile, in an organic EL display device 1 that has the structure shown in FIG. 2, when the thickness of the dielectric film of the holding capacitor 13 and the thickness of the dielectric film of the kick capacitor 15 vary within a range of $\pm 10\%$, the variation in the drive current with respect to the center conditions is within a range of $\pm 10\%$. In this way, the variation in the drive current can be suppressed very effectively by using the same dielectric film for the capacitance of the holding capacitor 13 and the capacitance of the kick capacitor 15.

[0034] In the present embodiment, the dielectric film 22, as shown in FIG. 2, preferably serves not only as the gate insulating film of the thin-film transistor 20 that constitutes a portion of the display pixel 3, but also as the capacitance of the holding capacitor 13 and the kick capacitor 15. This will now be explained with reference to FIG. 2 to FIG. 5.

[0035] FIG. 4 is a plan view of a portion of an organic EL display device using the structure shown in FIG. 2. FIG. 5 is a plan view of a portion of an organic EL display device using the structure shown in FIG. 3.

[0036] In general, the interlayer insulating film 23 is formed so as to be much thicker than the gate insulating film 22 in order to reduce cross-

shorting between scanning lines 4 and signal lines 5. For example, the thickness of the gate insulating film 22 is set to approximately 80 nm, and the thickness of the interlayer insulating film 23 is set to approximately 660 nm. Therefore, as shown in FIG. 3, when the interlayer insulating film 23 is used as the dielectric film of the holding capacitor 13, the holding capacitor 13 has to be made large in area in order to achieve sufficient capacitance in the holding capacitor 13, as shown in FIG. 3 and FIG. 5.

[0037] In contrast, when the insulating film 22 is used as the dielectric film of the holding capacitor 13 and the kick capacitor 15 in addition to the gate insulating film of the thin-film transistor 20, as shown in FIG. 2, the holding capacitor 13 does not have to be large in area, as shown in FIG. 2 and FIG. 4, and these can achieve sufficient capacitance (usually 0.1 pF or more and typically around 0.2 pF). For example, in the structures shown in FIG. 3 and FIG. 5, the area occupied by the holding capacitor 13 can be reduced by about one-eighth. Therefore, by using such a structure, the area occupied by the holding capacitor 13 and the kick capacitor 15 can be reduced.

[0038] Also, by forming one of the electrodes, in this case the upper electrode 13b, 15b, of the holding capacitor 13 and the kick capacitor 15, so that it has a larger surface area than the other electrode, in this case the lower electrode 13a, 15a, capacitance variation due to lateral misalignment, such as mask misalignment, can be suppressed.

[0039] Also, as in the embodiment described above, when the display pixels 3, scanning line driver 8, and signal line driver 9 are integrally formed at the same time on the substrate 2, one of the electrodes 13a, 15a of the holding capacitor 13 and kick capacitor 15 can be formed at the same time as the semiconductor layer (here, p-Si film) of the thin-film transistors constituting these circuits. Therefore, by simultaneous high-concentration injection of impurities in the source region and drain region of the thin-film transistor into the lower electrodes 13a, 15a of the holding capacitor 13 and kick capacitor 15 as well, the voltage dependence of these capacitors 13, 15 can be suppressed.

[0040] In the present embodiment, for example, the lower electrodes of the capacitors 13, 15 are formed at the same time as the semiconductor layer of the N-type transistor formed on the substrate 2. In other words, a semiconductor layer with a high concentration of N-type impurities (for example, phosphorus) injected at a concentration equivalent to that in the

source region and drain region of the N-type transistor can be used as the lower electrodes.

[0041] The configuration of the display pixel circuit is not limited to one described in the embodiment above, and the present invention can be applied to a generic display pixel circuit with a plurality of capacitors holding video signals.

[0042]

[Effects of the Invention] In the present invention, as explained above, since the same dielectric film is used for the capacitance of the holding capacitor and the capacitance of the kick capacitor, variation in the ratio of the electrostatic capacitance of the holding capacitor to the electrostatic capacitance of the kick capacitor can be suppressed. This makes it possible to suppress variations in drive current between display devices and between display pixels.

[0043] In other words, the present invention provides a display device holding video signals in multiple capacitors in which variations in the ratio of the electrostatic capacitances of these capacitors is less likely to occur. This makes it possible to suppress fluctuations in video signals.

[Brief Description of the Drawings]

[FIG. 1] FIG. 1 is a circuit diagram schematically representing the display device in an embodiment of the present invention.

[FIG. 2] FIG. 2 is a cross-sectional view of a portion of an organic EL display device in an embodiment of the present invention.

[FIG. 3] FIG. 3 is a cross-sectional view of a portion of an organic EL display device in which the dielectric film constituting the capacitance of the

holding capacitor is different from the dielectric film constituting the capacitance of the kick capacitor.

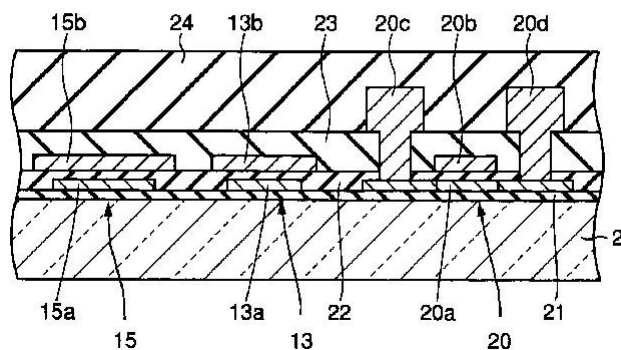
[FIG. 4] FIG. 4 is a plan view schematically representing a portion of an organic EL display device that has adopted the structure shown in FIG. 2.

[FIG. 5] FIG. 5 is a plan view schematically representing a portion of an organic EL display device that has adopted the structure shown in FIG. 3.

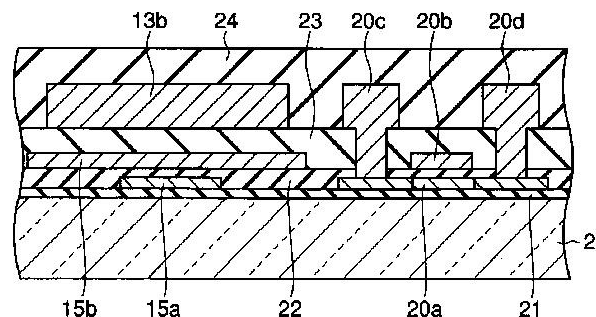
[Reference Numbers]

- 1: Display device
- 2: Substrate
- 3: Display pixel
- 4: Scanning line
- 5: Signal line
- 6, 7: Control line
- 8: Scanning line driver
- 9: Signal line driver
- 11: Display element
- 12: Drive control element
- 13: Holding capacitor
- 13a, 13b, 15a, 15b: Electrode
- 14: Pixel switch
- 15: Kick capacitor
- 16: Output switch
- 17: Reset switch
- 20: Thin film transistor
- 20a: Poly-Si film
- 20b: Gate electrode
- 20c: Source electrode
- 20d: Drain electrode
- 21-23: Insulating film
- 24: Passivation film

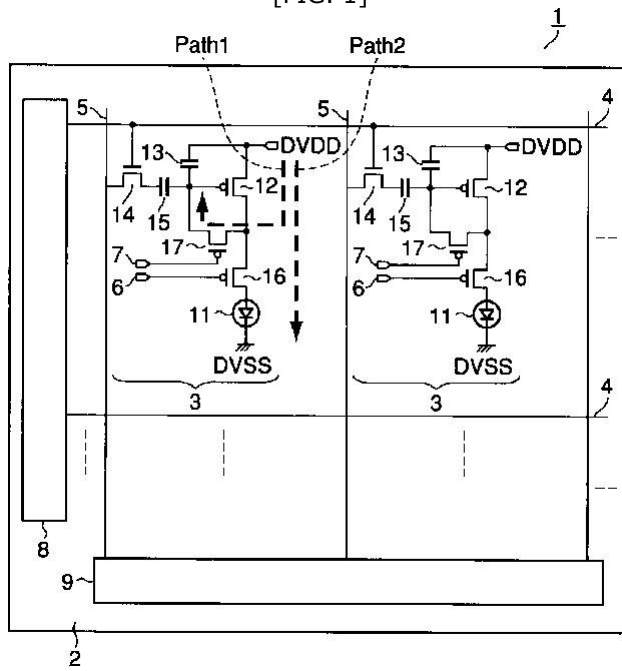
[FIG. 2]



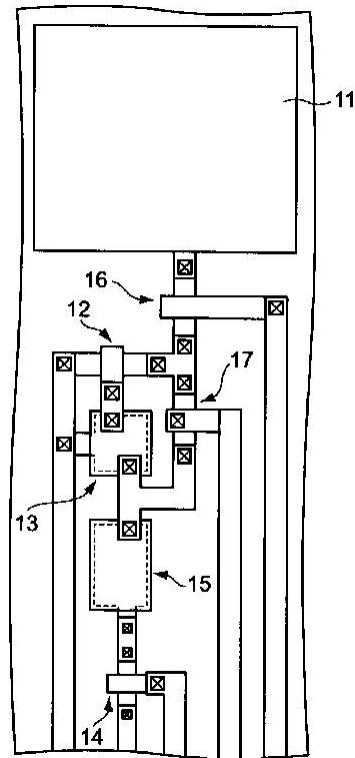
[FIG. 3]



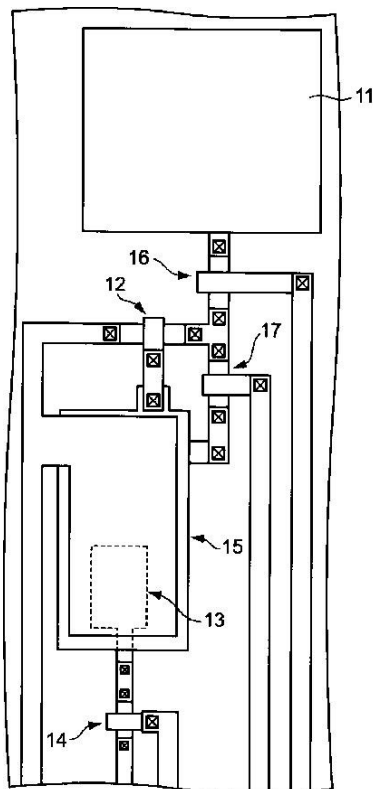
[FIG. 1]



[FIG. 4]



[FIG. 5]



Continued from front page

F Terms (Reference)

3K007 AB02 AB17 BA06 DB03 GA04

5C094 AA03 AA07 AA43 AA55 BA03 BA27 CA19 CA25 DA13 DA15 EA04 FA01 FA02 FB01 FB12 FB14
FB15 FB20

5F110 AA30 BB01 BB02 CC01 DD02 DD11 GG02 GG13 NN03 NN73 QQ08