

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Patent No. 9,299,730

Inter Partes Review No. IPR2025-01499

DECLARATION OF THOMAS CREDELLE

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Exhibit List

Exhibit Description	Exhibit #
U.S. Patent No. 9,299,730	1001
Expert Declaration of Thomas Credelle	1002
Prosecution History of U.S. Patent No. 9,299,730	1003
U.S. Publication No. 2007/0058100 to Ishii	1004
U.S. Publication No. 2003/0141811 to Park	1005
U.S. Publication No. 2002/0118150 to Kwon	1006
U.S. Publication No. 2012/0313100 to Liu	1007
U.S. Publication No. 2011/0128211 to Ono	1008
U.S. Publication No. 2012/0146004 to Lee	1009
U.S. Publication No. 2013/0063330 to Eom	1010
U.S. Publication No. 2012/0007080 to Liu	1011
Japanese Publication No. 2003-167533 to Nakayama	1012
English Translation of Japanese Publication No. 2003-167533	1013
Declaration of Frank McGee	1014
U.S. Publication No. 2008/0186423 to Ishii	1015
U.S. Patent No. 8,097,882 to Park	1016
U.S. Patent No. 6,963,173 to Kawachi	1017
U.S. Publication No. 2012/0211750 to Kakinuma	1018

I, Thomas Credelle, make this declaration in connection with the proceeding identified above.

I. INTRODUCTION

1. I have been retained as an expert witness on behalf of BOE Technology Group Co., Ltd. (“Petitioner” or “BOE”) to provide expert opinions on the patentability of United States Patent No. 9,299,730 (“the ’730 patent”).

2. I am being compensated at my normal rate, plus reimbursement for expenses, for my analysis. My compensation does not depend on the content of my opinions or the outcome of this proceeding.

II. QUALIFICATIONS

3. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae, which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

4. As shown in my curriculum vitae, I have devoted my career to the research and development and product engineering of flat panel displays and materials/optics/electronics for flat panel displays and touch sensors. I have over 20 years of involvement in active-matrix LCD R&D, starting in 1983 at RCA Labs and continuing at GE. I led the product development of active matrix LCDs for notebook computers at Apple in the early 1990s and had close collaboration with

many LCD developers in Asia. Later in my career, I made significant contributions to the design and implementation of new pixel architectures for LCDs and OLEDs while at Clairvoyante; both efforts involved Thin Film Transistor (“TFT”) design modifications to achieve the desired goals of high pixel transmission and reduced circuit complexity.

5. After receiving my Masters in Electrical Engineering from MIT in 1970, I was employed by RCA at Sarnoff Labs in Princeton, NJ as a Member of the Technical Staff and later as a Group Manager in charge of all Active Matrix LCD research. During my time at RCA, I participated in research and development projects relating to optical materials and flat panel displays, including LCD devices. In 1983, I established the TFT LCD Program at Sarnoff Labs. As a Group Manager, I led a project that resulted in the development of the first poly silicon TFT LCD at Sarnoff Labs. I received the Sarnoff Outstanding Achievement Award for Large Area Flat Panel TV Developments.

6. From 1986 to 1991, I was employed by GE as the Manager of TFT LCD Research and Development at the GE Research and Development Center in Schenectady, NY. My duties included contributing to and managing research and development efforts relating to TFT and LCD technology. While employed by GE, I led the team that built the world’s first 1-million-pixel color LCD device. I

also led the development of numerous other optical devices utilizing LCD technology.

7. From 1991 to 1994, I was employed by Apple Computer as the Manager of Display Engineering. In my role at Apple, I supervised all TFT-LCD design (in-house and at vendors), engineering, and qualification for the first PowerBook notebook computers introduced to market in the United States. A key part of my effort was the evaluation and development of active matrix LCDs with improved performance, such as viewing angle, contrast ratio, and uniformity.

8. From 1994 to 1996, I was employed as the Director of Advanced Product Marketing by Allied Signal, where I was involved with the design and engineering of optical films and custom focusing backlight designs for improving the viewing angle performance of LCD devices.

9. From 1996 to 1999, I was employed as the Director of Product Marketing for Motorola's Flat Panel Display Division, where I worked in the development of new flat panel technology. I also worked closely with Motorola groups responsible for integrating TFT-LCD technology into mobile phone products and materials development for OLED displays.

10. From 1999 to 2001, I served as the Vice President of Operations of Alien Technology Corporation. During my time at Alien Technology, I was

involved with the design and architecture of drive electronics packaging technology suitable for flexible display devices.

11. From 2001 to 2007, I served as the Vice President of Engineering for Clairvoyante, Inc. My responsibilities as the VP of Engineering included managing research, development, engineering, and marketing of technologies for improving the resolution and power consumption of color flat panel displays, which required significant changes to the active matrix layout. During my time at Clairvoyante, I was therefore heavily involved with the design of the active matrix array and the LCD or OLED pixel circuit and driving circuitry.

12. From 2007 to 2008, I served as the Senior VP of Engineering for Puredepth, Inc. My responsibilities included the design of hardware and software to create 3D images on TFT-LCDs.

13. From 2012 through 2015, I served as the Vice President of Application Engineering and Device Performance for Innova Dynamics, Inc., a nanotechnology company developing materials to be used in LCDs and touch sensors. In that effort, I led the collaboration with major capacitive touch sensor makers to replace brittle Indium Tin Oxide (“ITO”) transparent conductors with transparent silver nanowire conductors, which are compatible with flexible touch sensors. We successfully fabricated flexible capacitive touch sensors that could be bent without breaking.

14. In 2008, I founded TLC Display Consulting, a company that provides technical consulting in the areas of flat panel displays, liquid crystal displays, OLED, touch sensors, LEDs, and related electronics. I currently serve as the President of TLC Display Consulting.

15. I have been an active member of the Society for Information Display (“SID”) for over 40 years, and am currently a Life Member. I was a member of the Society for Information Display’s Program Committee for 15 years, and the Director of the Society for Information Display’s Symposium Committee for 10 years. In 1984, I was awarded the title of Fellow of the Society for Information Display in recognition of my achievements and contributions to flat panel display technology.

16. My curriculum vitae contains further details regarding my experience, education, publications, and other qualifications that allow me to render expert opinions in connection with this proceeding.

III. MATERIALS CONSIDERED

17. In preparing this declaration, I have reviewed, among other things, the ’730 patent and file history. I have also considered each of the documents cited in this Declaration and the documents specifically identified in the Exhibit List. In formulating my opinions, I have further relied upon my extensive experience in the relevant fields.

IV. SUMMARY OF THE '730 PATENT

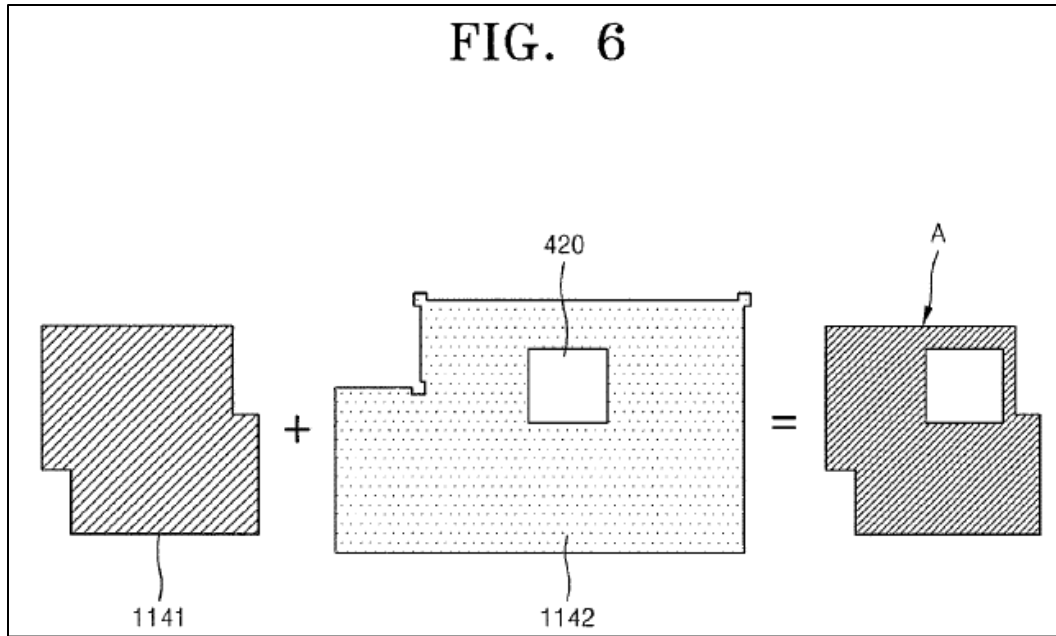
A. Filing And Priority Dates

18. The '730 patent was filed on March 13, 2013, and issued on March 29, 2016. The '730 patent claims priority Korean patent application 10-2012-0104215, which was filed on September 19, 2012.

B. Specification And Claims

19. The '730 patent is titled “Thin Film Transistor Array Substrate and Organic Light-Emitting Diode Display.” The '730 patent discloses “[a] thin film transistor (TFT) array substrate including at least one TFT and one storage capacitor, and an organic light-emitting diode (OLED) display.” (EX1001, 1:17-20; *see also* Abstract.)

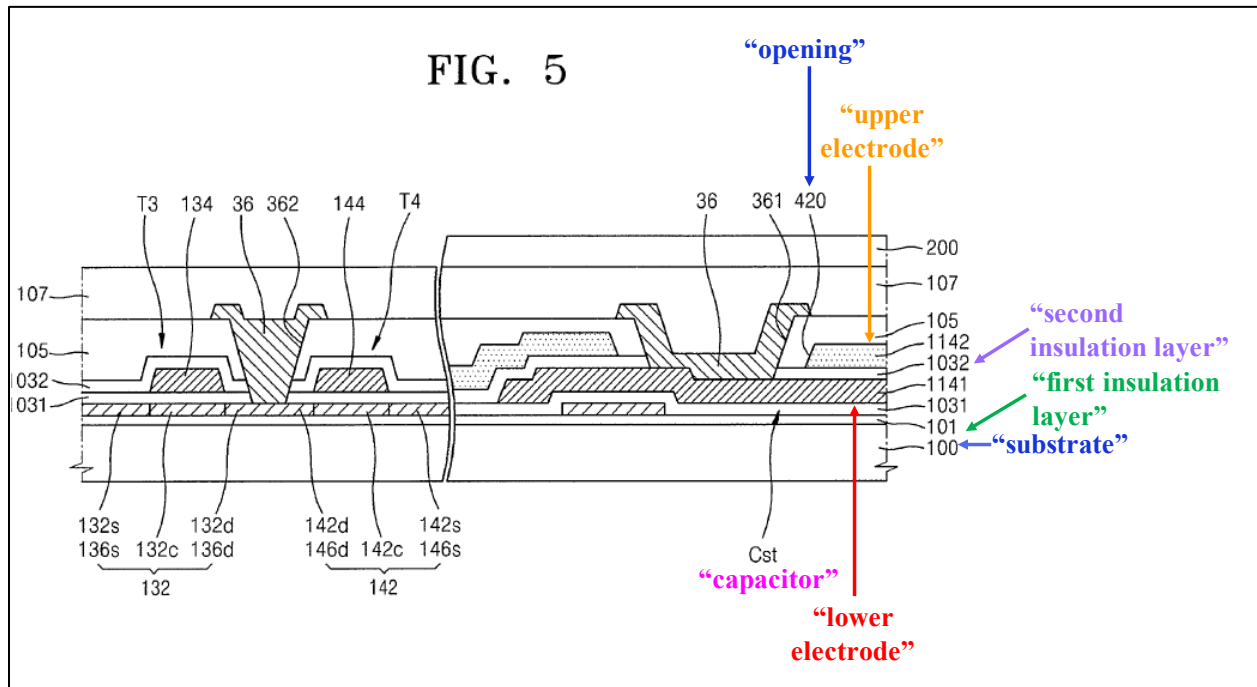
20. The '730 specification explains that “[t]he capacitor may include lower and upper electrodes and a dielectric interposed therebetween.” (EX1001, 1:31-32.) A misalignment between the upper electrode 1141 and the lower electrode 1142 of the storage capacitor may lead to a deviation in the amount of overlap (an overlay deviation) between the electrodes. (EX1001, 1:35-40.) The overlay deviation results in the actual capacitance differing from the target capacitance, thereby causing issues with the OLED display such as “low-gradation spots, abnormal colors, or the like.” (EX1001, 1:40-45.) Figure 6 (below) shows the upper electrode 1142, lower electrode 1141, and opening 420.



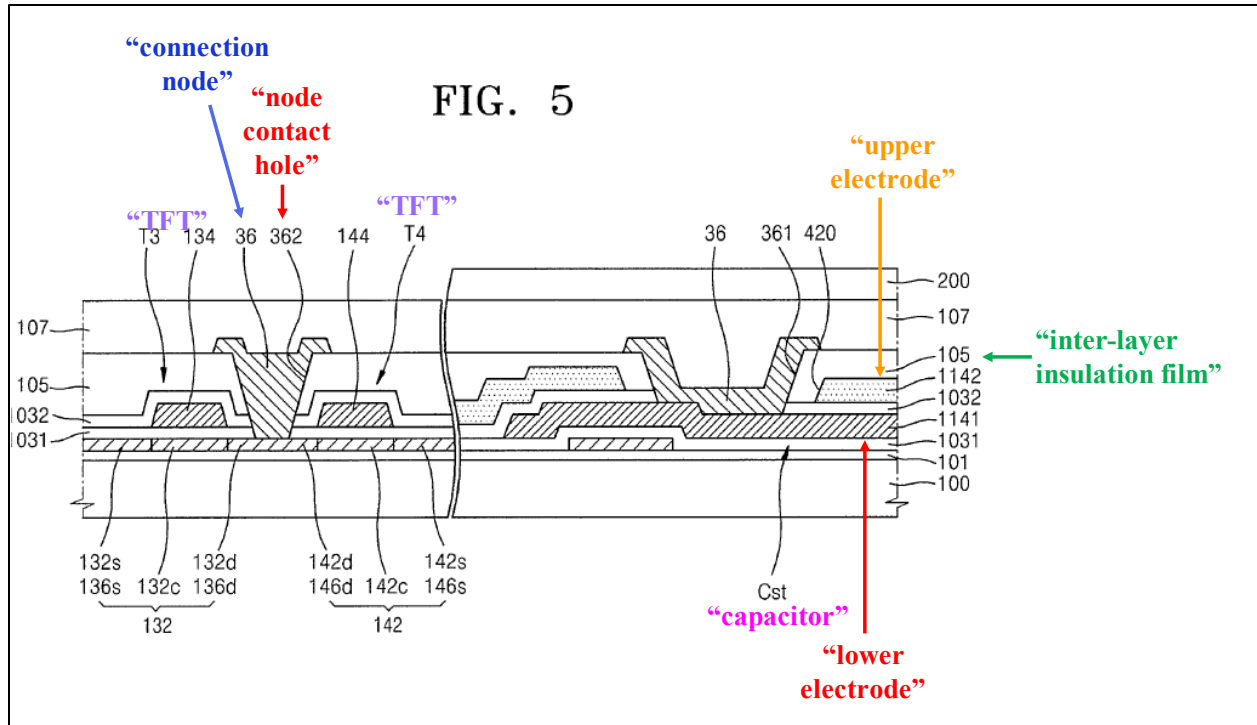
21. Figure 5 (annotated below) shows a cross-sectional view of the TFT array substrate. Independent claim 1 is directed to the TFT array substrate, which comprises:

- **“a substrate”** 100
- **“a first insulation layer”** (first gate insulation film 1031) on the substrate;
- **“a capacitor”** (storage capacitor Cst) comprising a **“lower electrode”** (lower electrode 1141) on the first insulation layer and an **“upper electrode”** (upper electrode 1142) arranged to overlap with the whole lower electrode, the upper electrode extends beyond an edge of the lower electrode and has an **“opening”** (storage opening 420), wherein the upper electrode is insulated from the lower electrode by a **“second**

insulation layer” (second gate insulation film 1032);



- **“an inter-layer insulation film”** (inter-layer insulation film 105)
(Figure 5 (annotated below)) covering the capacitor;
- **“a node contact hole”** (second node contact hole 362) in the inter-layer insulation film and the second insulation layer, and within the opening; and
- **“a connection node”** (connection node 36) on the inter-layer insulation film and electrically coupling the lower electrode and at least one **“TFT”** to each other through the node contact hole.



22. Independent claim 3 recites limitations similar to independent claim 1. Claim 3 further requires “the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”

23. Independent claim 5 recites limitations similar to independent claims 1 and 3. Claim 5 further requires “a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”

24. Independent claims 10, 12, and 14 are each directed to an “organic light-emitting diode (OLED) display.” Claim 10 requires “scan line,” “a data line and a driving voltage line,” a “pixel circuit,” and an “OLED.” Claim 12 recites

limitations from claims 1, 3, and 10. Claim 14 recites limitations from claims 1, 5, and 10.

25. Claims 2, 4, 6-9, 11, 13, and 15-19 are dependent claims. Claims 2 and 11 require that the opening overlaps with the lower electrode. Claims 4 and 13 are directed to the driving voltage line. Claims 6-9 and 15-19 require additional TFTs, including a compensation TFT, an initialization TFT, and/or a switching TFT.

C. Prosecution History

26. I understand that during prosecution of the '730 patent, the Examiner issued a Non-Final Office Action on February 4, 2015 that rejected claims 1, 2, 10, and 11 for being anticipated by Lee (U.S. Pub. No. 2012/0146004) (EX1009). (EX1003, 81-82.) Claims 3-9 and 13-19 were indicated as allowable, but objected to for being dependent upon a rejected base claim. (EX1003, 82.)

27. On May 1, 2015, Applicant responded by amending independent claims 1 and 10 to require “the upper electrode extending beyond an edge of the lower electrode.” (EX1003, 58, 61.) Applicant distinguished over Lee by arguing that Lee’s second electrode 53 (“upper electrode”) of the capacitor does not overlap with the whole first electrode 51a (“lower electrode”). (EX1003, 65.) Applicant also amended claims 3, 5, 12, and 14 to be rewritten in independent form by including limitations from claims 1 and 10. (EX1003, 59-63, 69.)

28. On August 25, 2015, the Examiner issued a Final Office Action that rejected claims 1, 2, 10, and 11 over Eom (U.S. Pub. No. 2013/0063330) (EX1010) in view of Lee. (EX1003, 39-43.) The Examiner also indicated that claims 3-9 and 12-19 were allowable. (EX1003, 43.)

29. On October 26, 2015, Applicant responded by arguing that Eom was not prior art because it was subject to common ownership. (EX1003, 32.)

30. On November 20, 2015, the Examiner issued a Notice of Allowance stating that the prior art of record does not anticipate, teach, or suggest the limitations of the claims. (EX1003, 14-15.)

V. RELEVANT LEGAL STANDARDS AND DEFINITIONS

A. Anticipation

31. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in a single prior art reference or system. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference and that it would have been so recognized by a POSITA. In addition, I understand that an enabling disclosure is a disclosure that allows a POSITA to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to

show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

B. Obviousness

32. I understand that a claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the claimed subject matter was made to a POSITA to which the subject matter pertains. I understand that a patent claim may be obvious to a POSITA in view of the prior art teachings of a single reference or a combination of references.

33. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any secondary considerations to the extent they exist.

34. It is also my understanding that there are principles that may be used as further guidance in an obviousness analysis (especially when considering combinations of references), which include considering whether:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;

- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;
- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;
- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a POSITA;
- there existed at the time of conception and reduction to practice a known problem for which there was an obvious solution encompassed by the patent’s claims; and
- there is some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to

combine prior art reference teachings to arrive at the claimed subject matter.

35. I understand that there are secondary considerations that may tend to show that a claimed invention would not have been obvious to a POSITA. These include, for example, commercial success, long-felt but unsolved needs, failure of others, and unexpected results. I further understand that there must be a relationship, or nexus, between any secondary considerations and the novelty of the claimed invention.

VI. LEVEL OF ORDINARY SKILL IN THE ART FOR THE '730 PATENT

36. I am informed and understand that various factors can be considered in determining a person of ordinary skill in the art (POSITA). I am informed and understand that those factors include: (1) the educational level of the inventors; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) the rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the field.

37. A person of ordinary skill in the art (POSITA) in the field of the '730 patent would have a bachelor's degree in electrical engineering or materials science, including OLED displays, or an equivalent level of skill, knowledge, and experience. This POSITA would have been aware of and generally knowledgeable about OLED materials, and display pixel design, layout, and operation.

38. I agree with this level of ordinary skill for the '730 patent. Based on my experience, I understand and know of the capabilities of a person of this skill level as of the time the '730 priority application was filed in 2012. I am familiar with how a POSITA would have understood and used the terminology found in the '730 patent at the time of the filing of the priority application, and with the state of the art at that time.

VII. CLAIM CONSTRUCTION

39. I have been informed that claim construction requires consideration of the words of the claims themselves, the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. I have also been informed that the specification is usually definitive, as it is the single best guide to the meaning of a disputed term.

40. I have been informed that, in the context of this proceeding, Petitioner did not propose any terms for construction. Instead, Petitioner believes each of the terms of the '730 patent carries its ordinary and customary meaning, which is the meaning that the term would have to a POSITA. I agree with Petitioner and apply the ordinary and customary meaning of the terms in my analysis below.

VIII. PRIOR ART

41. I understand that each of the references discussed herein qualifies as prior art against the '730 patent:

42. U.S. Publication No. 2007/0058100 A1 ("Ishii100," EX1004) was filed on July 7, 2006, claims priority to a Japanese patent application filed on September 15, 2005, and published on March 15, 2007.

43. U.S. Publication No. 2008/0186423 A1 ("Ishii423," EX1015) was filed on January 24, 2008, claims priority to a Japanese patent application filed on February 1, 2007, and published on August 7, 2008.

44. U.S. Publication No. 2003/0141811 A1 ("Park," EX1005) was filed on December 27, 2002, claims priority to a Korean patent application filed on December 29, 2001, and published on July 31, 2003.

45. U.S. Publication No. 2002/0118150 A1 ("Kwon," EX1006) was filed on December 7, 2001, claims priority to a Korean patent application filed on December 29, 2000, and published on August 29, 2002.

46. U.S. Publication No. 2012/0313100 A1 ("Liu," EX1007) was filed on February 2, 2012, claims priority to a foreign application filed on June 10, 2011, and published on December 13, 2012.

47. U.S. Publication No. 2011/0128211 A1 (“Ono,” EX1008) was filed on January 24, 2011, claims priority to a PCT application filed on November 27, 2009, and published on June 2, 2011.

IX. ANALYSIS AND OPINION

A. Claims 1 And 2 Are Obvious Over Ishii100

1. Summary of Ishii100

48. Ishii100 is directed to an “electro-optical device having a storage capacitor of increased area, and enabling high-definition image display, a manufacturing method thereof, an electronic apparatus, and a capacitor.” (EX1004, [0007].) Ishii100 names a “liquid crystal device” as one example of an electro-optical device, but also teaches that “the invention can be applied to . . . an organic EL display” (EX1004, [0002], [0097].)

49. Ishii100 acknowledges that “the capacity of the storage capacitor in the pixel portion may be lowered and display unevenness may occur.” (EX1004, [0006].) This is because “it is necessary to ensure and design a margin in consideration of the alignment between the two kinds of mask.” (*Id.*) Accordingly, the storage capacitor area is decreased so that a sufficient margin is provided and to ensure proper alignment. (*Id.*)

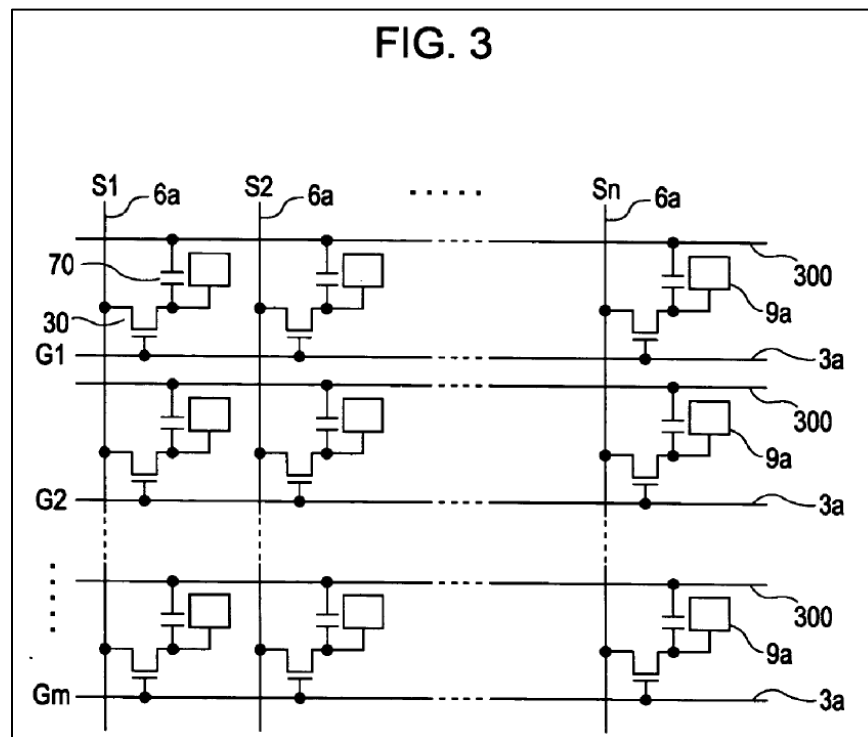
50. Ishii100’s electro-optical device comprises “a storage capacitor 70 [] formed by arranging a relay layer 71 as a pixel-potential side capacitor electrode, which is connected to the highly doped drain region 1e and the pixel electrode 9a

of the TFT 30, and a part of a capacitor line 300 as a fixed-potential-side capacitor electrode so that they face each other with a dielectric film 75 therebetween.”

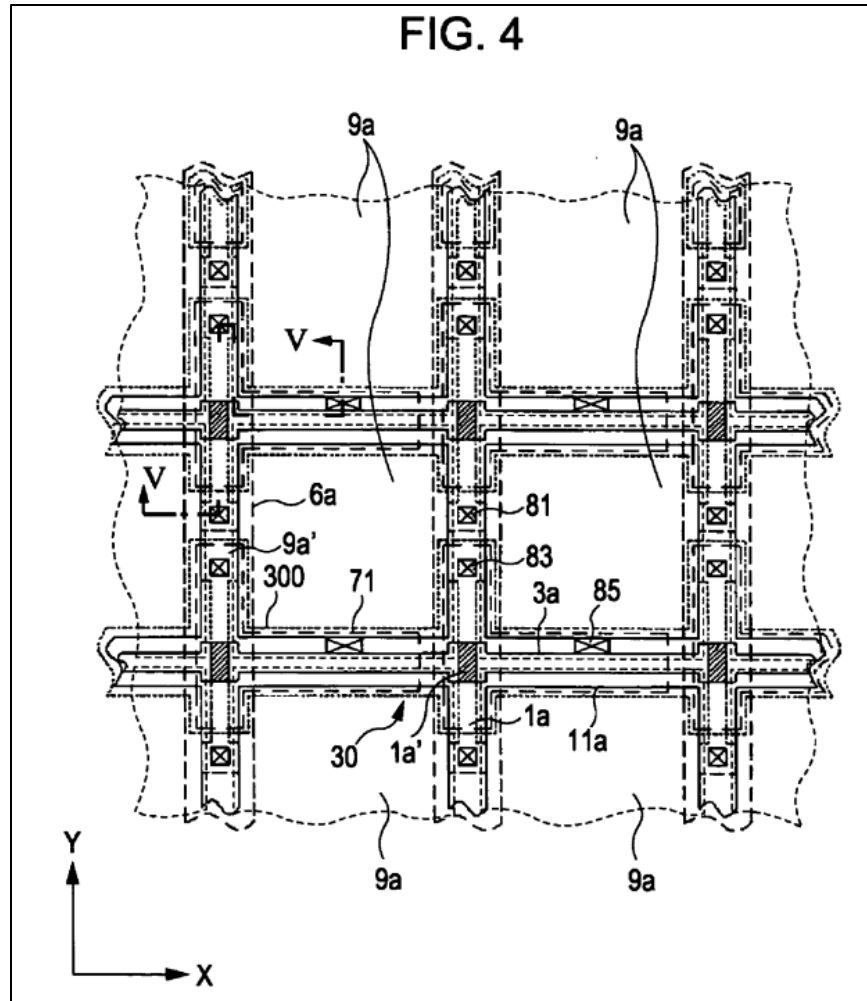
(EX1004, [0056].)

51. Ishii100’s electro-optical device also comprises “a pixel-switching thin-film transistor (hereinafter suitably referred to as ‘TFT’) [that] applies a data signal from a data line to a pixel electrode where a pixel is located and selected by a scanning line.” (EX1004, [0009].)

52. Figure 3 (below) shows a circuit of Ishii100’s storage capacitor 70, pixel electrode 9a, and TFT 30. The circuit also includes scanning lines 3a and data lines 6a.

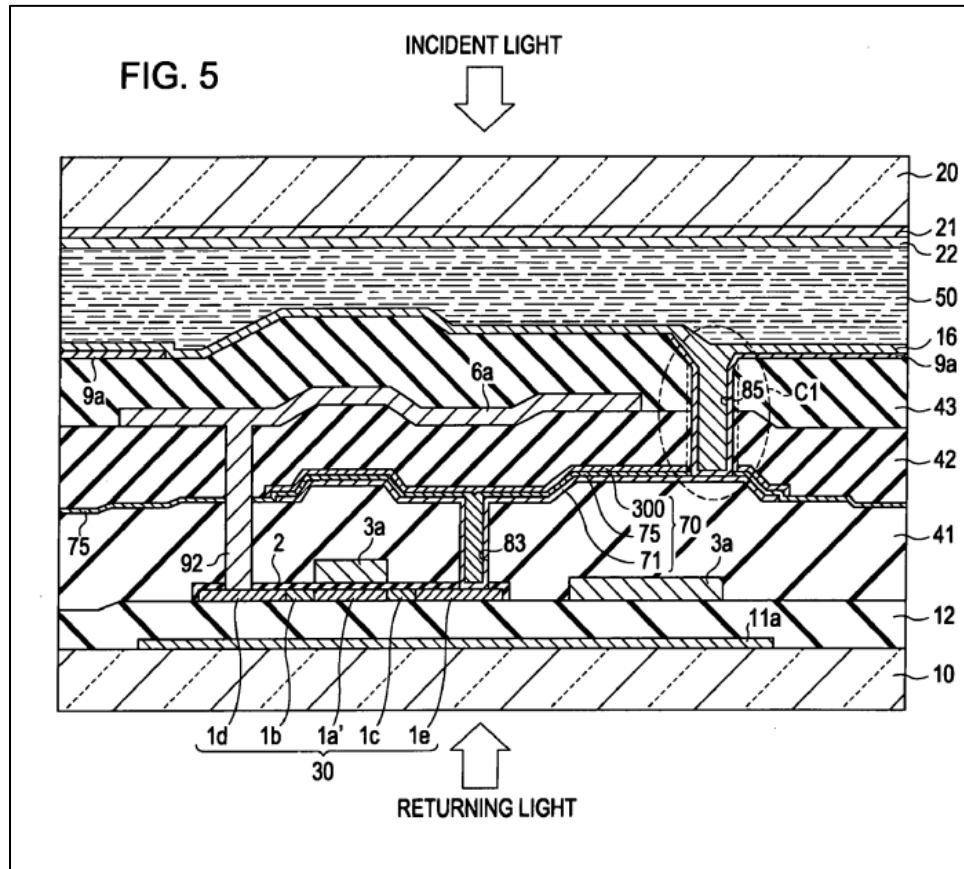


53. Figure 4 below shows a plan view of Ishii100’s disclosed invention.



54. Figure 5 below is a cross-sectional view of Figure 4 at V-V.

(EX1004, [0028].)

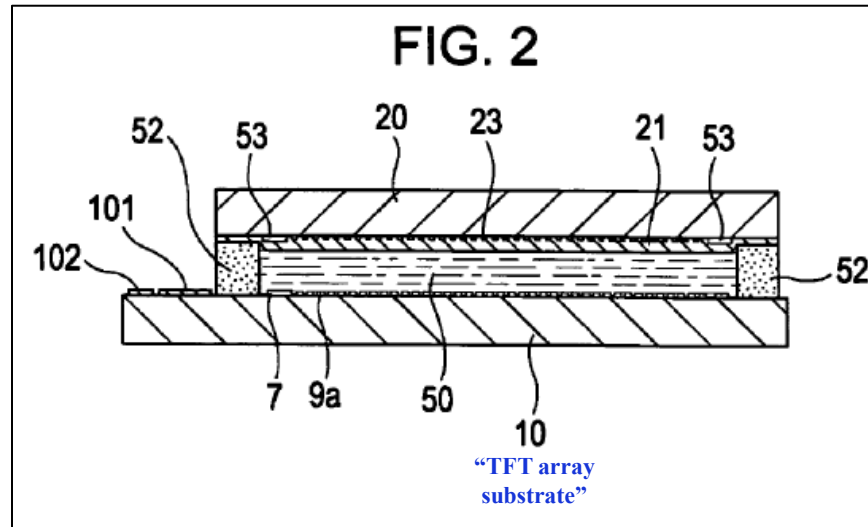


2. Claim 1

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

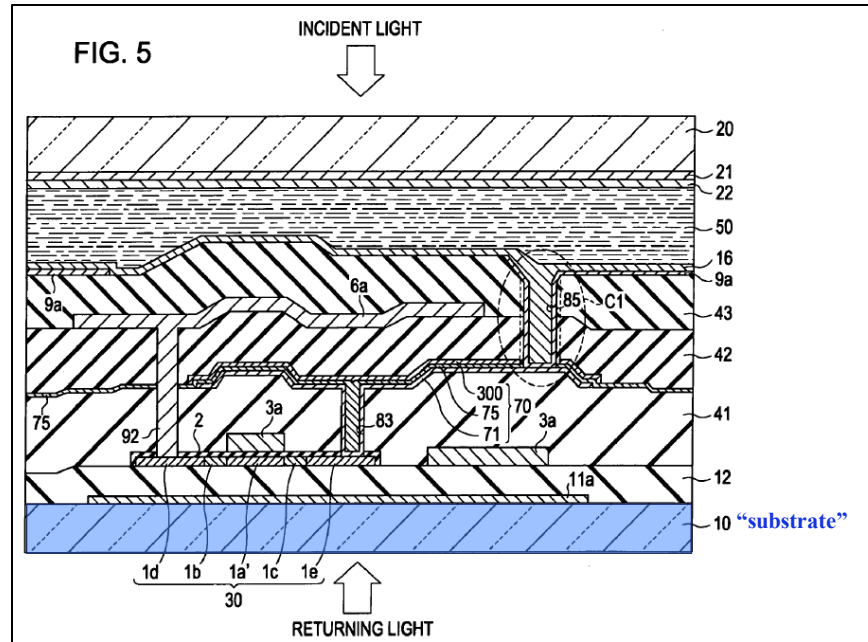
55. Ishii100 teaches “[a] thin film transistor (TFT) array substrate.” For example, Ishii100 discloses “[r]eferring to FIGS. 1 and 2, a *TFT array substrate 10* and a counter substrate 20 are arranged to face each other in the liquid crystal device according to this embodiment.” (EX1004, [0041].) Ishii100 also discloses “a laminated structure in which pixel-switching TFTs (Thin-Film Transistors) which are driver elements, and wiring lines, such as scanning lines and data lines,

are provided is formed on the TFT array substrate 10.” (EX1004, [0044].) Figure 2 (annotated below) shows the *TFT array substrate 10*.



b. 1[a]: “a substrate;”

56. Ishii100 teaches “a substrate.” For example, Ishii100 discloses “[a]s shown in FIG. 5, the liquid crystal device according to this embodiment includes a transparent TFT array *substrate 10* and a transparent counter substrate 20 arranged to face the array substrate.” (EX1004, [0053] (emphasis added).) Figure 5 (annotated below) shows Ishii100’s *substrate 10*.

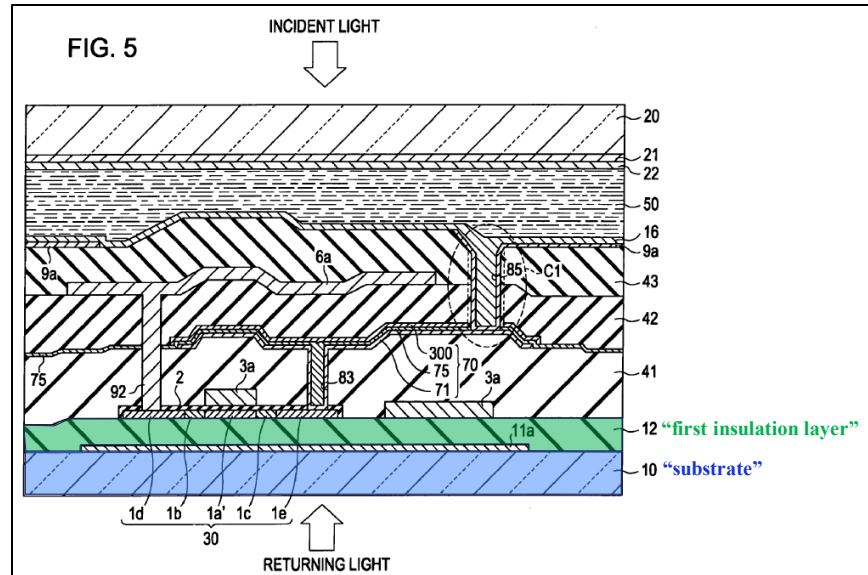


57. As another example, Ishii100 discloses “[r]eferring to FIG. 2, a laminated structure in which pixel-switching TFTs (Thin-Film Transistors) which are driver elements, and wiring lines, such as scanning lines and data lines, are provided is formed on the *TFT array substrate 10*.” (EX1004, [0044] (emphasis added); *see also* EX1004, claim 1.)

c. 1[b]: “a first insulation layer on the substrate;”

58. As shown for element 1[a], Ishii100 teaches a substrate 10 (“substrate”).

59. Ishii100 teaches “a first insulation layer on the substrate.” For example, Ishii100 discloses “an underlying *insulating film 12* is provided under the TFT 30.” (EX1004, [0063] (emphasis added).) Figure 5 (annotated below) shows Ishii100’s *insulating film 12* on the *substrate 10*.



60. Ishii100 also discloses “*a first interlayer insulating film 41* through which a contact hole 81 which leads to the highly doped drain region 1e and a contact hole 83 which leads to the highly doped source region 1d are bored is formed on the scanning line 3a.” (EX1004, [0064].)

- d. 1[c]: “**a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;**”

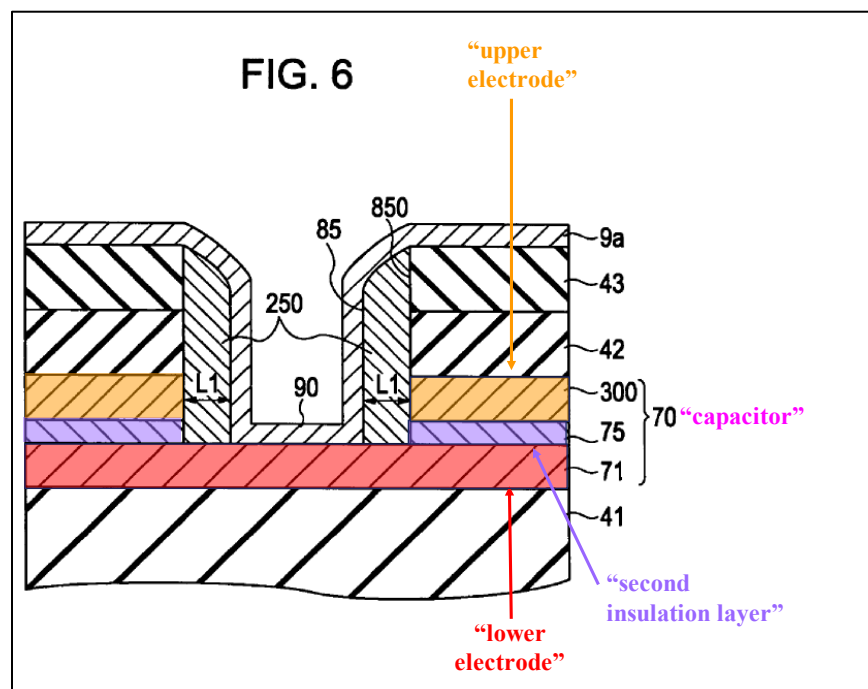
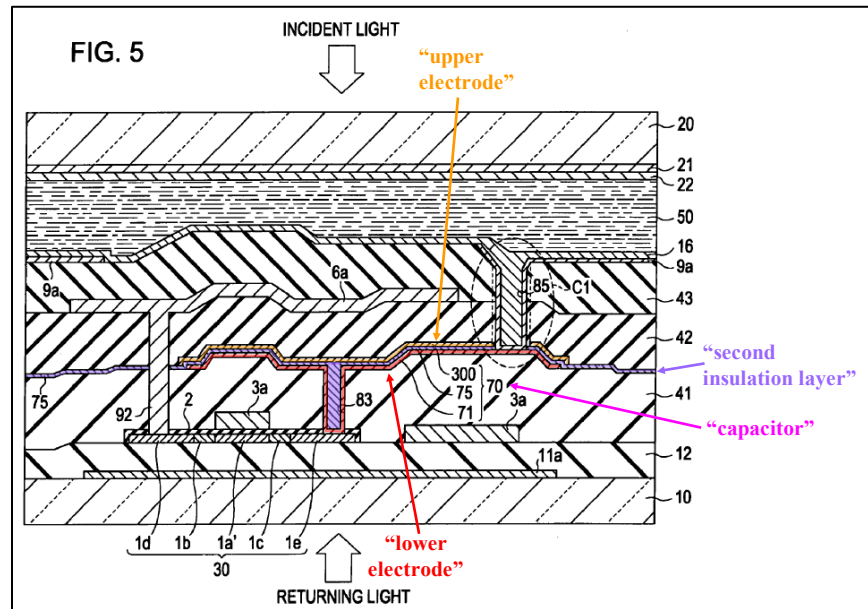
61. Ishii100 teaches “a capacitor comprising a lower electrode . . . and an upper electrode, wherein the upper electrode is insulated from the lower electrode by a second insulation layer.” For example, Ishii100 discloses “in FIG. 5, a *storage capacitor 70* is formed by arranging a *relay layer 71 as a pixel-potential*

side capacitor electrode, which is connected to the highly doped drain region 1e and the pixel electrode 9a of the TFT 30, and a part of *a capacitor line 300 as a fixed-potential-side capacitor electrode* so that they face each other *with a dielectric film 75 therebetween.*” (EX1004, [0056] (emphasis added).) Ishii100 also discloses:

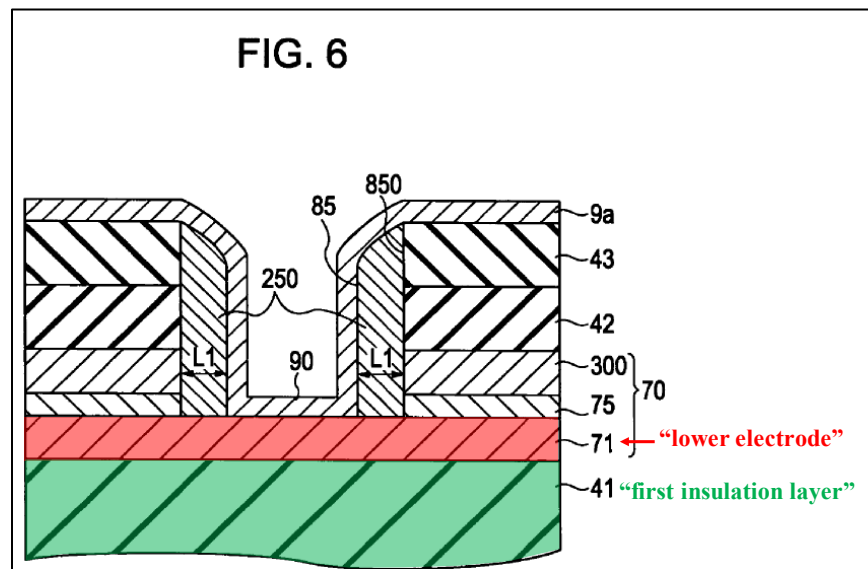
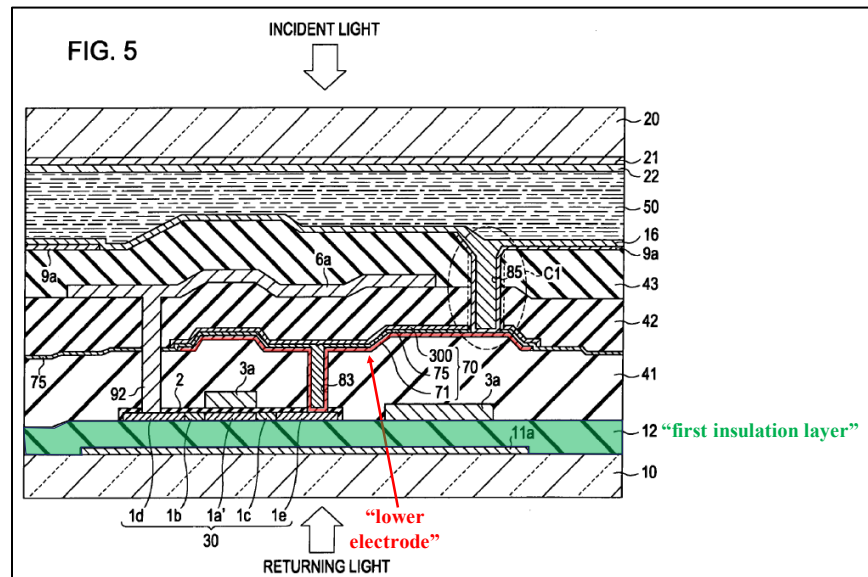
- “the relay layer 71 constitutes an example of ‘the other of a pair of electrodes according to the invention, and the capacitor line 300 constitutes an example of ‘one of a pair of electrodes according to the invention.’” (EX1004, [0061].)
- “Referring to FIG. 6, the storage capacitor 70 is configured such that the relay layer 71 which functions as a pixel-potential-side capacitor electrode, the dielectric film 75, and the capacitor line 300 which functions as a fixed-potential-side capacitor electrode are laminated in this order on the first interlayer insulating film 41.” (EX1004, [0068].)
- “First, in a step shown in FIG. 7A, a relay layer 71 as a pixel-potential-side capacitor electrode, a dielectric film 75, a capacitor line 300 as a fixed-potential-side capacitor electrode, a second interlayer insulating film 42, and a third interlayer insulating film 43 are laminated in order on the first interlayer insulating film 41.”

(EX1004, [0074]; *see also* Claim 1, Claim 3.)

62. Figures 5 and 6 (annotated below) show **capacitor 70** comprising a **relay layer 71** and a **capacitor line 300**, wherein the capacitor line 300 is insulated from the relay layer 71 by the **dielectric film 75**.

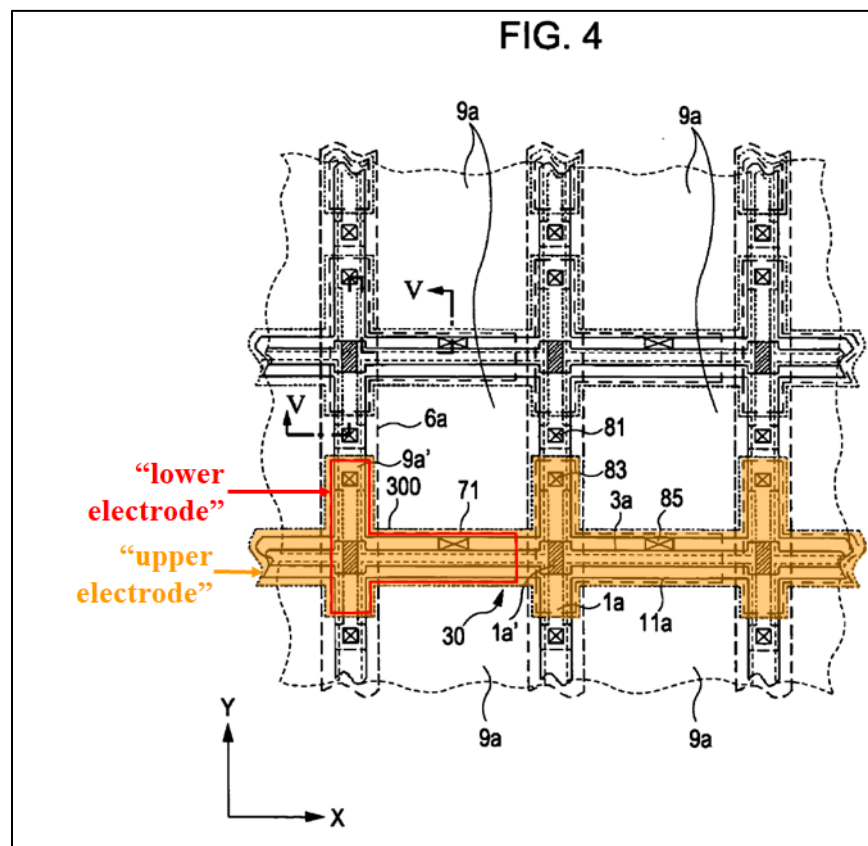


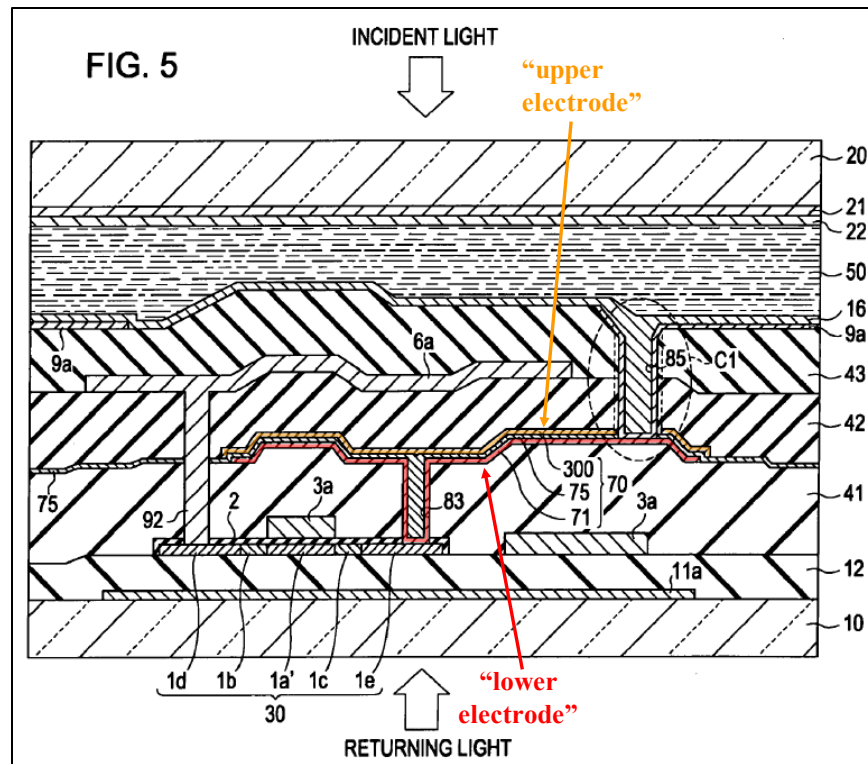
63. Ishii100 also teaches the “lower electrode on the first insulation layer.” Figures 5 and 6 (annotated below) show Ishii100’s *relay layer 71* on the *insulating film 12* and *insulating layer 41*.



64. Ishii100 further teaches the “upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode.” Figures 4 and 5 (annotated below) show *capacitor line 300*

arranged to overlap with the whole **relay layer 71**, the capacitor line 300 extending beyond an edge of the relay layer 71. Ishii100 further discloses “[w]hen this capacitor line 300 is seen in plan view, as shown in FIG. 4, it is formed so as to **overlap** a formation area of a scanning line 3a. . . . Among these, a **protruding portion** contributes to an increase in the formation area of the storage capacitor 70 using a region on the scanning line 3a and a region under the data line 6a. Further, the capacitor line 300 preferably extends from an image display region 10a where a pixel electrode 9a is arranged in its periphery.” (EX1004, [0059].)

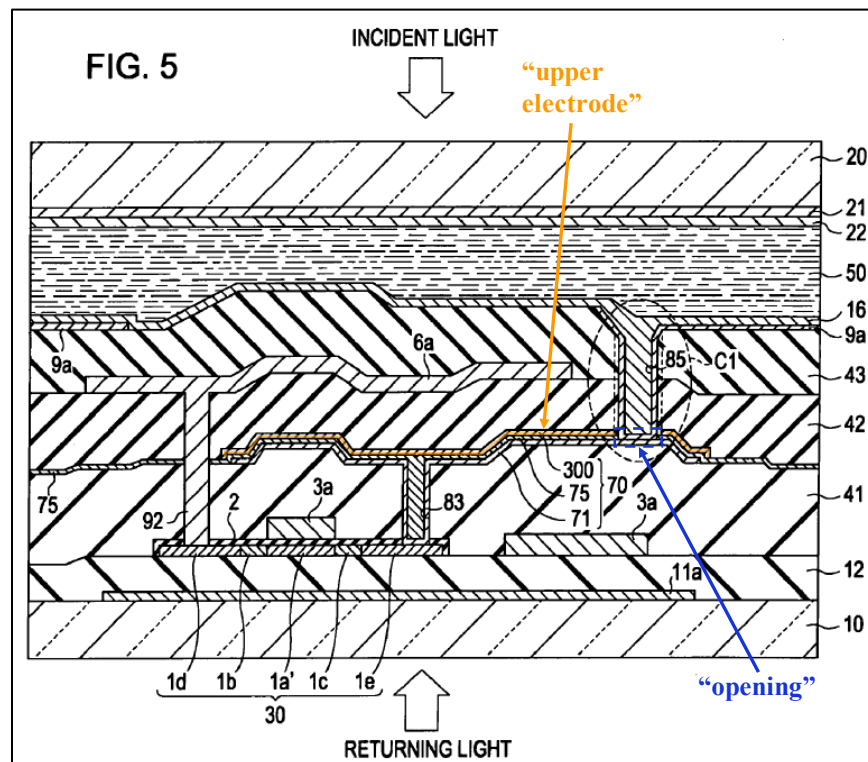


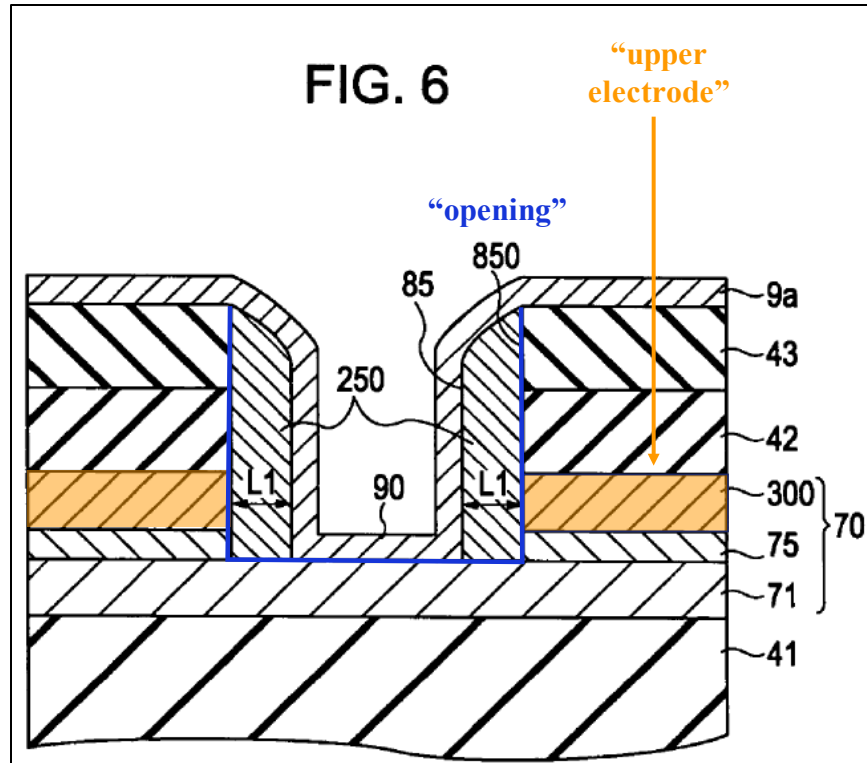


65. Further, it was obvious and known to a POSITA at the time of the '730 patent to have the surface area of the upper electrode of the capacitor be greater than the surface area of the lower electrode of the capacitor. The upper electrode of the capacitor overlaps the whole lower electrode and its surface area is made larger so any overlay deviation (deviation between the upper and lower electrodes) does not change the capacitance. For example, Nakayama teaches forming the upper electrode of a holding capacitor (and kick capacitor) to such that it has a larger surface area than the lower electrode. (EX1012, EX1013, [0038] ("by forming one of the electrodes, in this case the upper electrode 13b, 15b, of the holding capacitor 13 and the kick capacitor 15, so that it has a larger surface area than the other electrode, in this case the lower electrode 13a, 15a, capacitance

variation due to lateral misalignment, such as mask misalignment, can be suppressed”), Figs. 2, 4.) Figure 4 shows that the upper electrode overlaps the whole lower electrode. Accordingly, movement of the upper electrode with respect to the lower electrode may not affect the capacitance because the overlap between the upper and lower electrodes may not change.

66. Ishii100 also teaches “an opening.” Ishii100 discloses “[t]he sidewall 250 is provided on the inner wall of an opening 850 which is opened through the third interlayer insulating film 43, the second interlayer insulating film 42, the capacitor line 300, and the dielectric film 75.” (EX1004, [0070].) Figures 5 and 6 (annotated below) show the *capacitor line 300* having an *opening 850*.





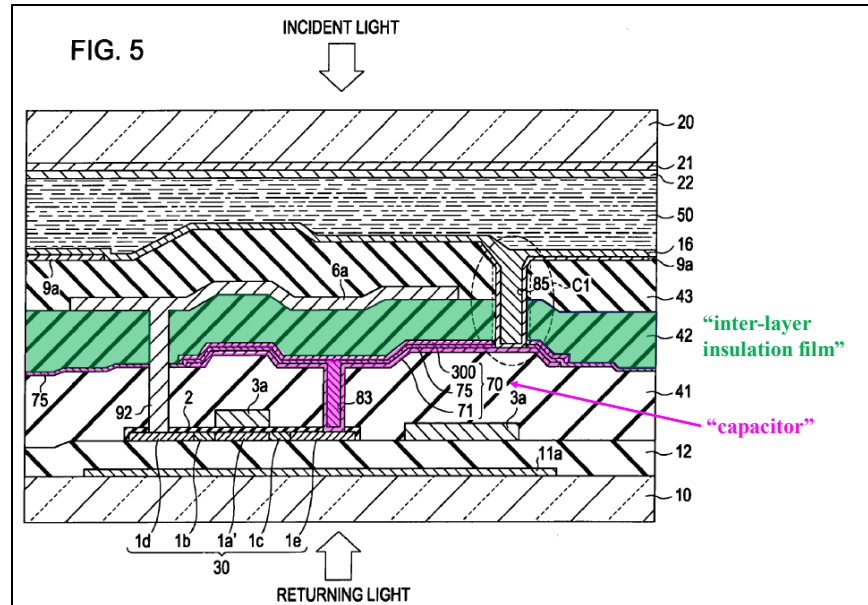
e. **1[d]: “an inter-layer insulation film covering the capacitor;”**

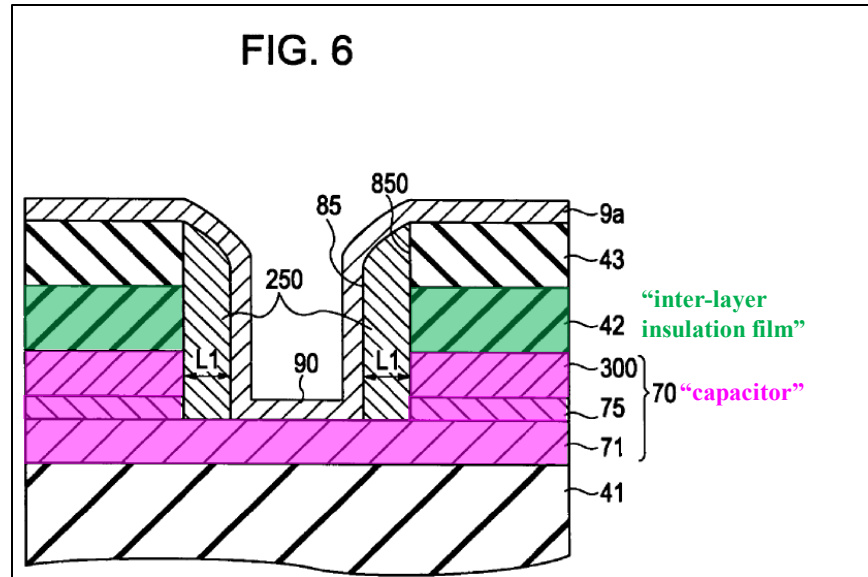
67. As shown for element 1[c], Ishii100 teaches a storage capacitor 70 (“capacitor”) comprising a relay layer 71, a dielectric film 75, and a capacitor line 300.

68. Ishii100 teaches “an inter-layer insulation film covering the capacitor.” For example, Ishii100 discloses “*a relay layer 71* as a pixel-potential-side capacitor electrode, *a dielectric film 75*, *a capacitor line 300* as a fixed-potential-side capacitor electrode, a *second interlayer insulating film 42*, and a third interlayer insulating film 43 *are laminated in order* on the first interlayer insulating film 41.” (EX1004, [0074] (emphases added).) Ishii100 also discloses

“[a] relay layer 71 and a capacitor line 300 are formed on the first interlayer insulating film 41, and *a second interlayer insulating film 42* through which a contact hole 81 which leads to the highly doped source region 1d and a contact hole 85 which leads to the relay layer 71 are bored, *is formed on the relay layer and the capacitor line.*” (EX1004, [0065].)

69. Figures 5 and 6 (annotated below) show *interlayer insulating film 42* covering the *capacitor 70*.





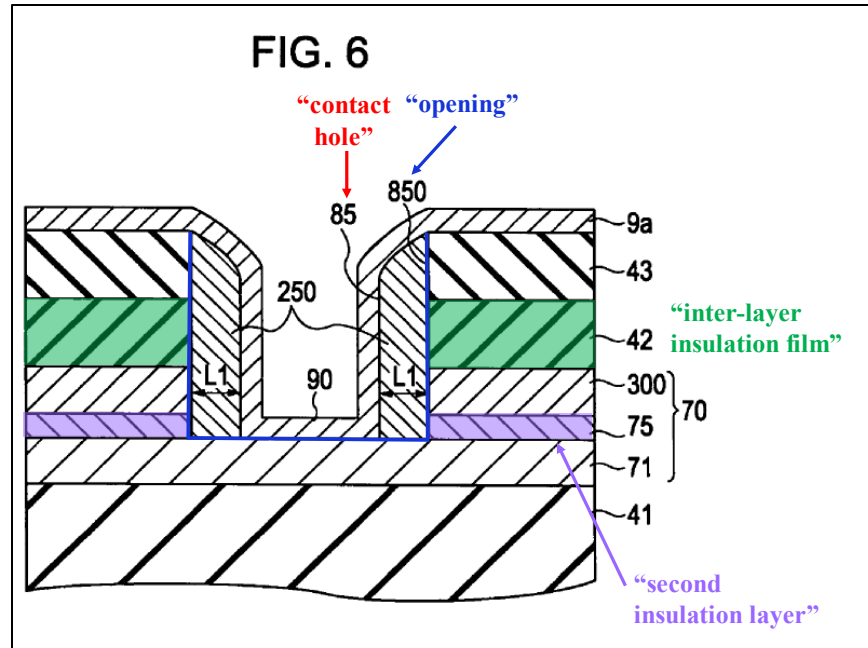
f. 1[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

70. As shown for element 1[d], Ishii100 teaches an interlayer insulating film 42 (“inter-layer insulation film”). As shown for element 1[c], Ishii100 teaches a dielectric film 75 (“second insulation layer”) and an opening 850 (“opening”).

71. Ishii100 teaches “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening.” For example, Ishii100 describes “a sidewall 250 is provided on the inner wall of an opening 850 which is opened through the third interlayer insulating film 43, *the second interlayer insulating film 42*, the capacitor line 300, and *the dielectric film 75*.” (EX1004, [0070] (emphases added); *see also* EX1004, [0075] (“Next, in a step shown in FIG. 7B, an opening 850 which is opened through the third interlayer insulating film 43, the second interlayer insulating film 42, the capacitor line 300, and the dielectric

film 75 is formed by etching, etc. At this time, the relay layer 71 is exposed.”), Claim 1.) “[T]he contact hole 85 [is] surrounded by this sidewall 250.” (EX1004, [0070].) “The contact hole 85 is a self-alignment-type contact hole formed simultaneously with formation of the sidewall 250, and is surrounded by the sidewall 250.” (EX1004, [0071].) And “[t]he storage capacitor 70 is electrically connected to the pixel electrode 9a arranged on the side of the upper layer via the *contact hole 85 which is bored through the second interlayer insulating film 42* and the third interlayer insulating film 43.” (EX1004, [0068] (emphasis added); *see also* EX1004, [0065] (“A relay layer 71 and a capacitor line 300 are formed on the first interlayer insulating film 41, and a second interlayer insulating film 42 through which . . . a contact hole 85 which leads to the relay layer 71 are bored, is formed on the relay layer and the capacitor line.”), Claim 3.)

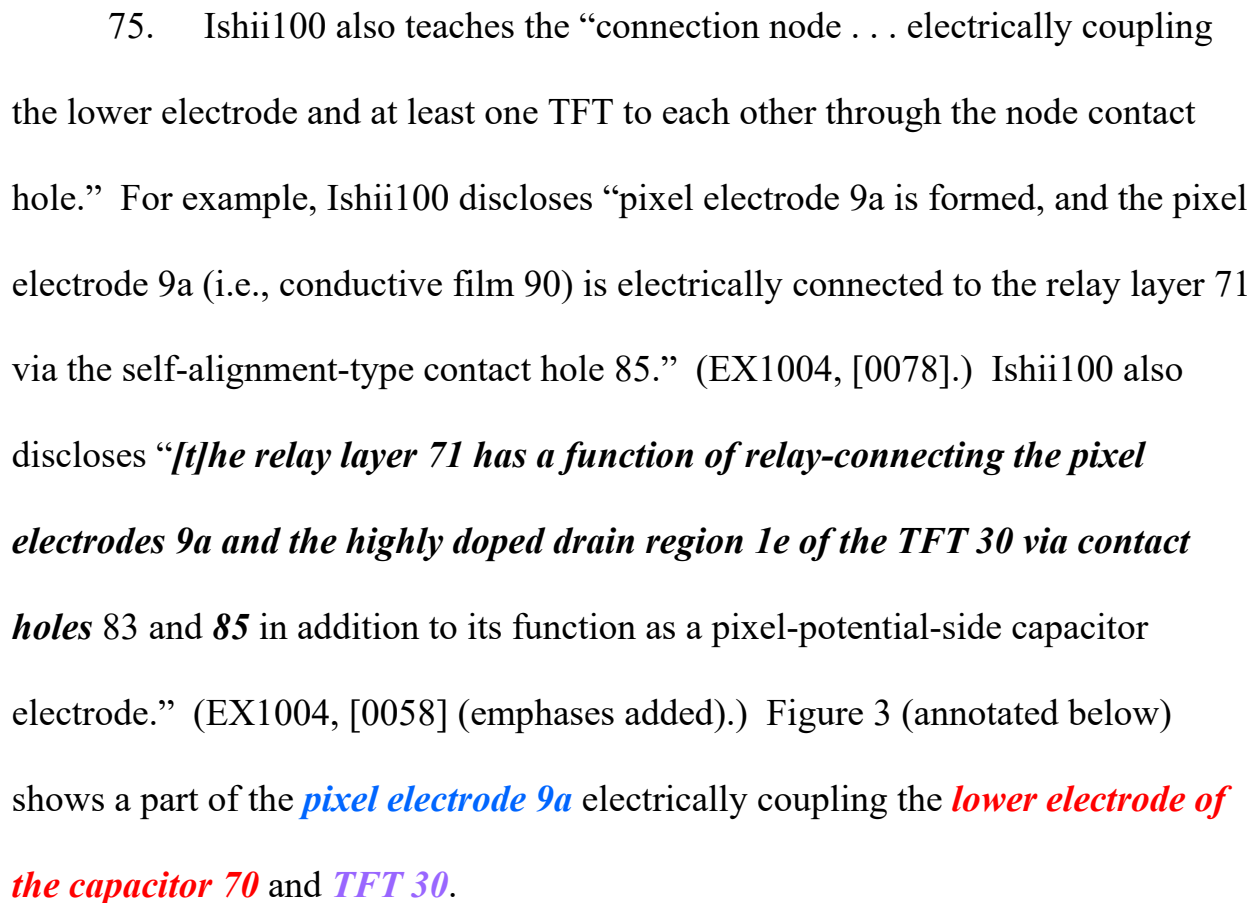
72. Figure 6 (annotated below) shows a *contact hole 85* in the *interlayer insulating film 42* and *dielectric film 75*, and within the *opening 850*.

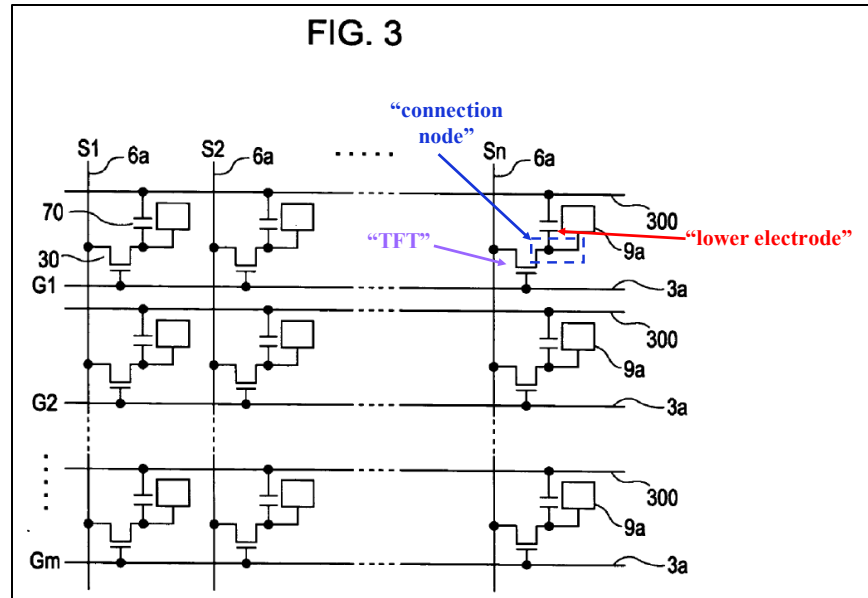


- g. 1[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”**

73. As shown for element 1[d], Ishii100 teaches an interlayer insulating film 42 (“inter-layer insulation film”). As shown for element 1[c], Ishii100 teaches a relay layer 71 (“lower electrode”). As shown for element 1[e], Ishii100 teaches a contact hole 85 (“node contact hole”).

74. Ishii100 teaches “a connection node on the inter-layer insulation film and electrically coupling the lower electrode.” Figure 6 (annotated below) shows a part of the *pixel electrode 9a* on the *interlayer insulating film 42* and electrically coupling the *relay layer 71* through the *contact hole 85*.



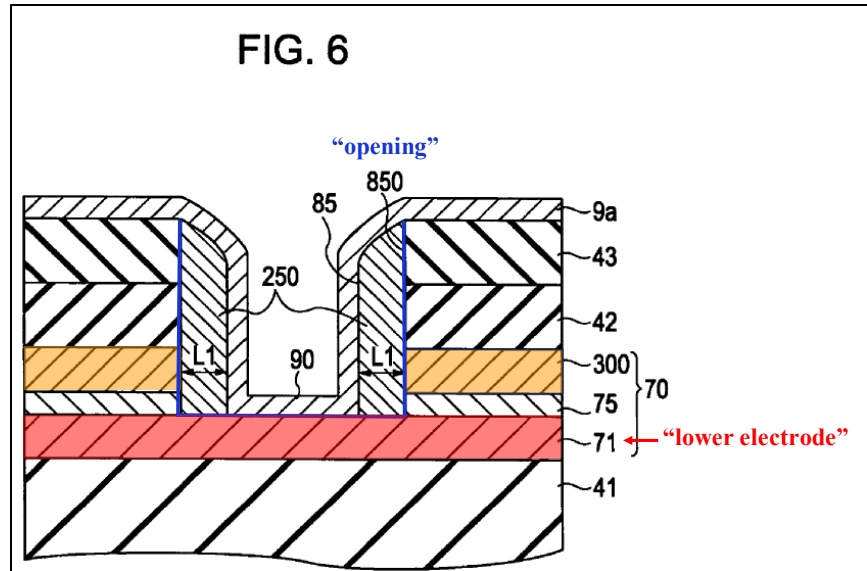


3. Claim 2: “The TFT array substrate of claim 1, wherein the opening overlaps with the lower electrode.”

76. Ishii100 teaches claim 1 as shown above in Section IX.A.2.

77. As shown for element 1[c], Ishii100 teaches an opening 850 (“opening”) and a relay layer 71 (“lower electrode”).

78. Ishii100 teaches “the opening overlaps with the lower electrode.” For example, Ishii100 discloses “*an opening 850* which is opened through the third interlayer insulating film 43, the second interlayer insulating film 42, the capacitor line 300, and the dielectric film 75 is formed by etching, etc. *At this time, the relay layer 71 is exposed.*” (EX1004, [0075] (emphases added).) A POSITA would have understood that the opening 850 being opened such that the relay layer 71 is exposed means that opening 850 overlaps with the relay layer 71. Figure 6 (annotated below) shows the *opening 850* overlapping with the *relay layer 71*.



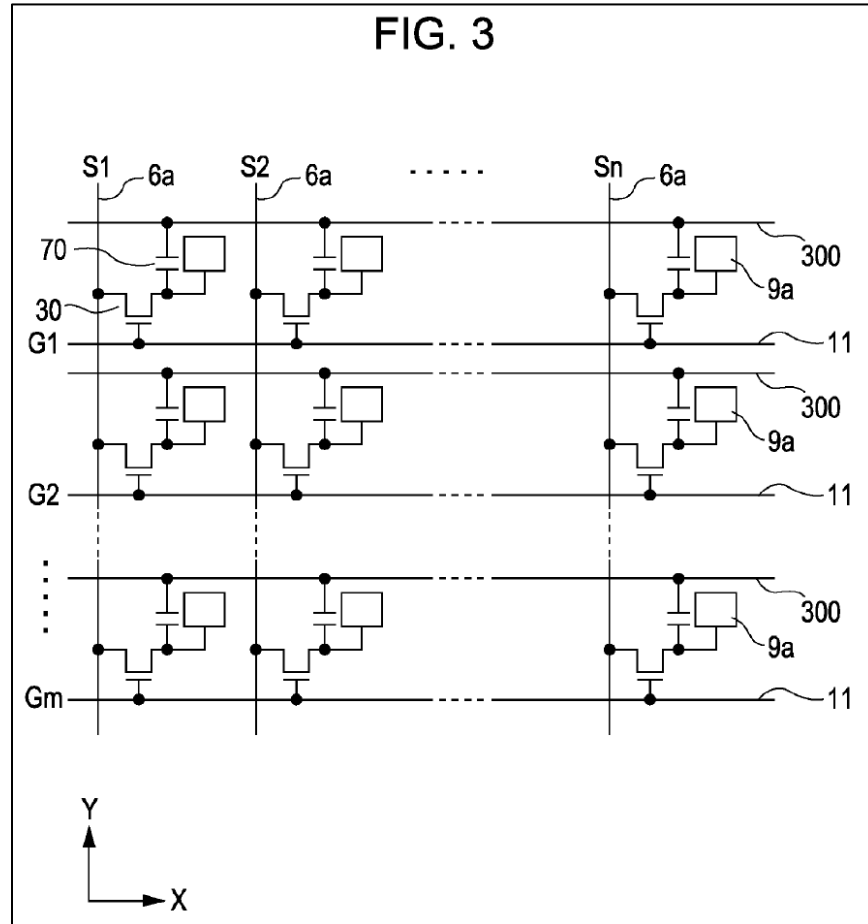
B. Claims 1 And 2 Are Obvious Over Ishii100 And Ishii423

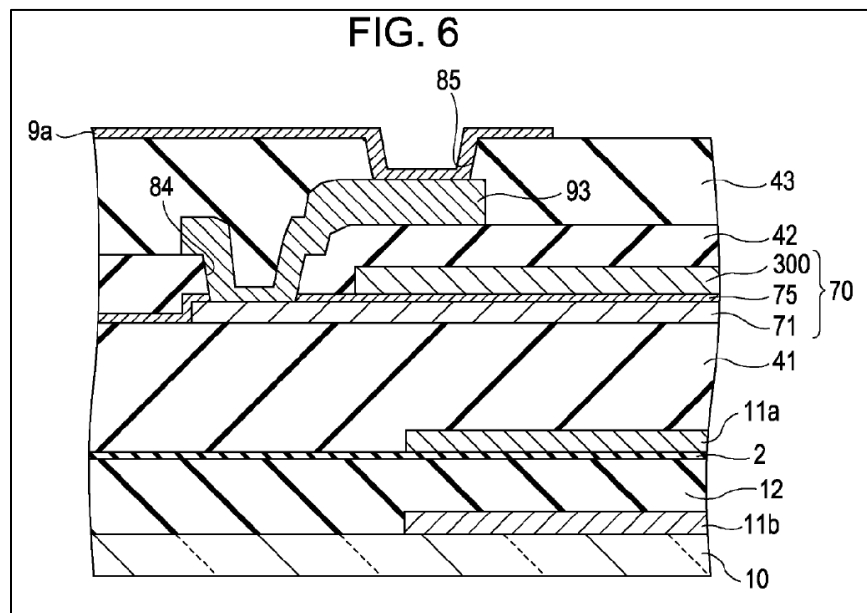
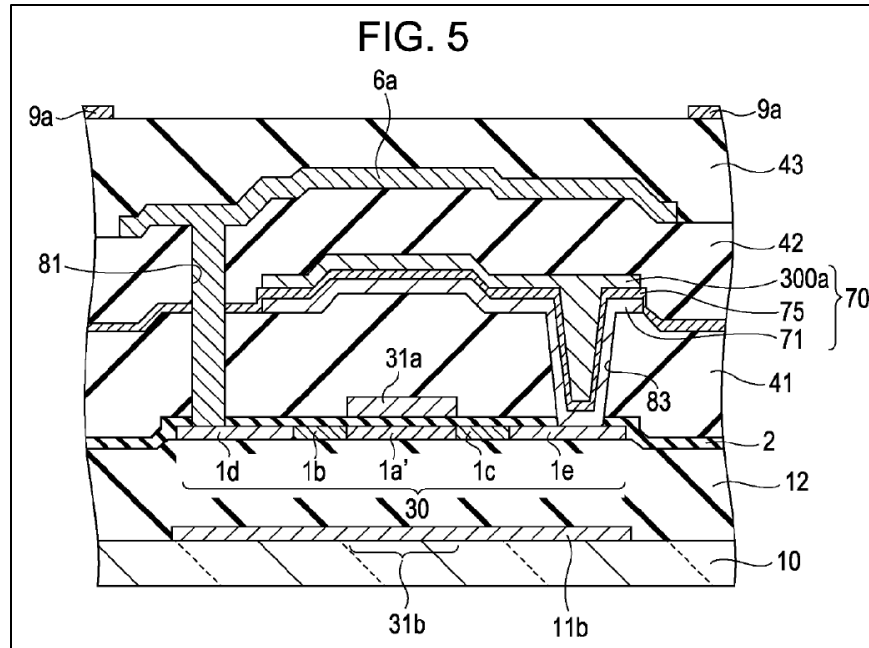
1. Summary of Ishii423

79. Ishii423 is directed to an “electro-optical device” comprising “a substrate, a plurality of data lines, a plurality of scanning lines, pixel electrodes, and transistors.” (EX1015, Abstract.)

80. Ishii423’s pixel circuit is shown in Figure 3 (below), and its display stack is shown in Figures 5 and 6 (below). Ishii423 discloses “the data line 6a and the relay layer 93 are provided in an upper layer than the storage capacitor 70 through the interlayer insulating film 42 on the TFT array substrate 10.” (EX1015, [0111].) “[T]he relay layer 93 is formed in the same layer as the data line 6a (see FIG.5) on the interlayer insulating film 42.” (EX1015, [0113].) “[T]he relay layer 93 [is] provided in an upper layer than the storage capacitor 70 through the interlayer insulating film 42 on the TFT array substrate 10.” (EX1015, [0111].)

Ishii423 also discloses “[t]he pixel electrode 9a is electrically connected through the lower capacitor electrode 71, the contact holes 83, 84 and 85, and the relay layer 93 to the pixel electrode side source/drain region 1e of the semiconductor layer 1a.” (EX1015, [0114].)





2. Claim 1

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

81. As shown above, Ishii100 teaches the preamble of claim 1.

b. 1[a]: “a substrate;”

82. As shown above, Ishii100 teaches element 1[a].

c. 1[b]: “a first insulation layer on the substrate;”

83. As shown above, Ishii100 teaches element 1[b].

d. 1[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

84. As shown above, Ishii100 teaches element 1[c].

e. 1[d]: “an inter-layer insulation film covering the capacitor;”

85. As shown above, Ishii100 teaches element 1[d].

f. 1[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

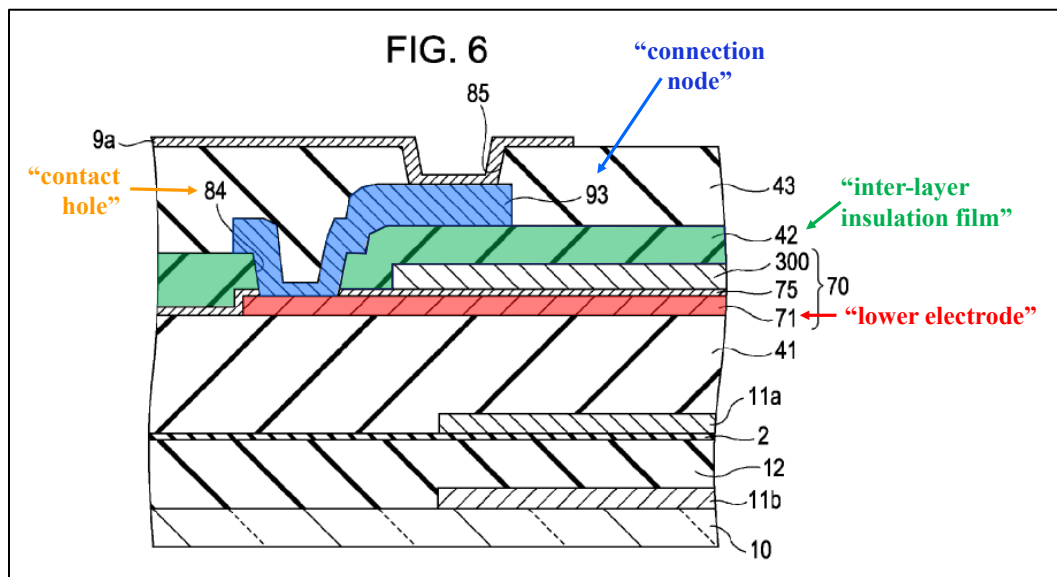
86. As shown above, Ishii100 teaches element 1[e].

g. 1[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”

87. If, for some reason, Ishii100 does not teach a “connection node,”

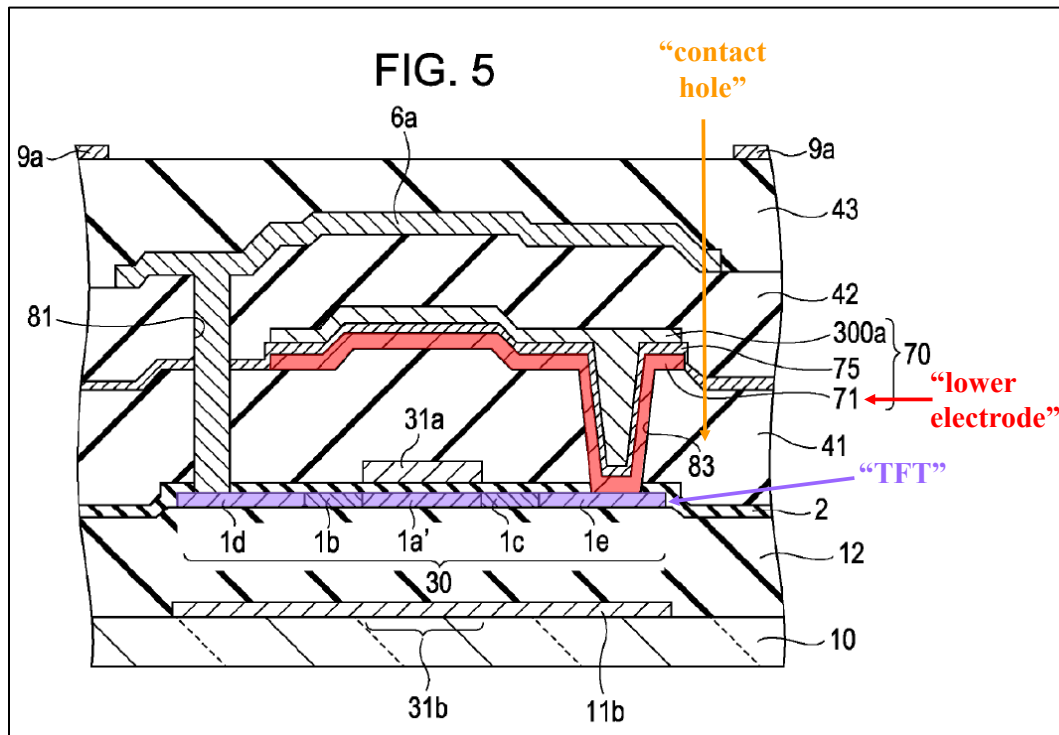
Ishii423 teaches “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through

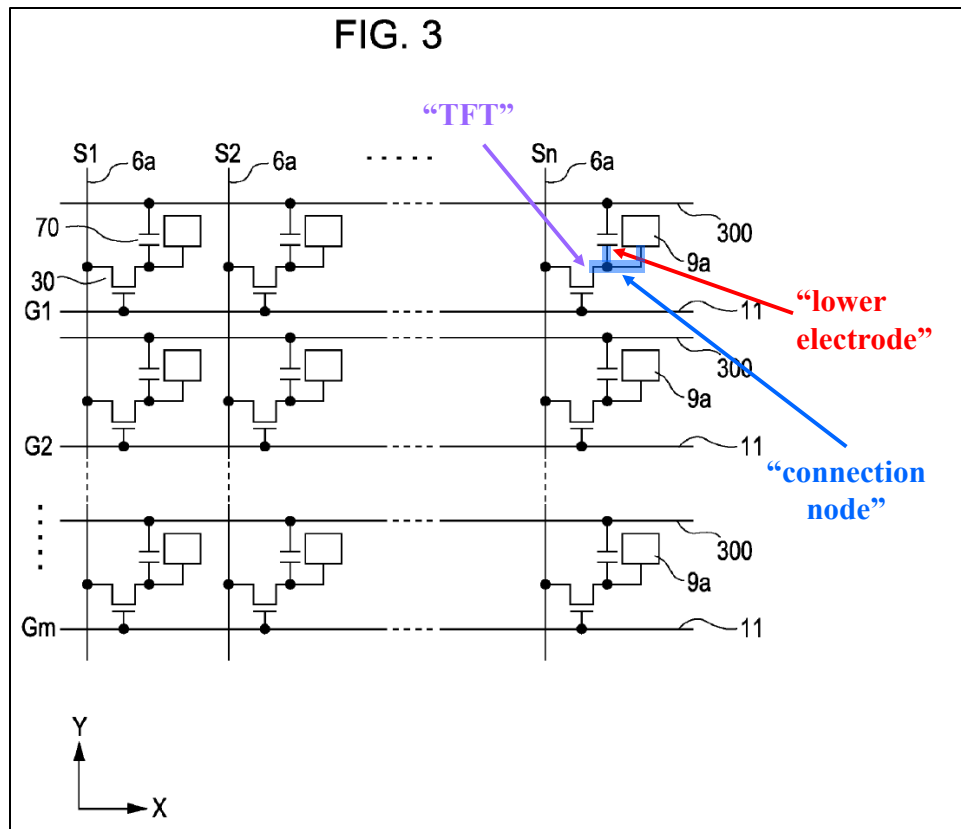
the node contact hole.” For example, Ishii423 discloses “the relay layer 93 [is] provided in an upper layer than the storage capacitor 70 through the interlayer insulating film 42 on the TFT array substrate 10.” (EX1015, [0111].) Ishii423 also discloses “[t]he pixel electrode 9a is electrically connected through the lower capacitor electrode 71, the contact holes 83, 84 and 85, and the relay layer 93 to the pixel electrode side source/drain region 1e of the semiconductor layer 1a.” (EX1015, [0114].) Figure 6 (annotated below) shows the *relay layer 93* on the *interlayer insulating film 42* and electrically coupling the *lower capacitor electrode 71* and pixel electrode 9a to each other through the *contact hole 84*.



88. Figure 5 (annotated below) shows the *lower capacitor electrode 71* electrically coupled to the source/drain region 1e of *TFT 30* through the *contact hole 83*. Figure 3 (annotated below) shows the pixel electrode 9a is coupled to TFT 30, and thus, the relay layer 93 electrically couples the lower electrode 71 and

TFT 30 to each other. Thus, Ishii423 teaches “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”





89. It would have been obvious to a POSITA at the time of the '730 patent to combine the teachings of Ishii100 and Ishii423. Ishii100 and Ishii423 relate to electro-optical devices and improving the quality of electro-optical devices. Ishii100 discloses an electro-optical device with improve storage characteristics in the pixel electrode, thereby achieving a high contrast display. (EX1004, [0013].) The display device is “capable of reducing an area occupied by components of the pixel structure.” (EX1004, [0007].) Ishii100 addresses the “technical problem in that the capacity of the storage capacitor in the pixel portion may be lowered and display unevenness may occur.” (EX1004, [0006].) Ishii423 discloses an electro-optical device with reduced light leakage, thereby being able

to display a high-quality image. (EX1004, [0006].) Ishii423 addresses the “technical problem in which display defects, such as flicker or pixel chrominance non-uniformity, may occur and, as a result, the display image quality decreases.” (EX1004, [0005].) Further, Ishii423 teaches capacitor line 300a and lower electrode 71 are made of metal. (EX1004, [0107], [0108], [0110].) Ishii100 similarly teaches capacitor line 300a and relay layer (lower electrode) 71 are made of metal. (EX1015, [0057].) Thus, Ishii100 and Ishii423 are in the same field of endeavor and reasonably pertinent to the same technical problem of improving the quality of the images from an electro-optical device.

90. Ishii423 teaches the structure of an electro-optical device comprising a relay layer for creating electrical connections. (EX1015, [0108].) For example, “the relay layer 93 is electrically connected through a contact hole 85 (see FIG. 4 and FIG. 6) to the pixel electrode 9a. That is, the lower capacitor electrode 71, in cooperation with the relay layer 93, relays electrical connection between the pixel electrode side source/drain region 1e and the pixel electrode 9a.” (EX1015, [0108].) A POSITA would have been motivated to use a relay layer 93 for electrical connections because a relay layer creates a more reliable connection. These technical features of Ishii423 can be combined with the teachings of Ishii100 with a reasonable expectation of success to generate an electro-optical device that provides improved image quality.

91. Because Ishii100 and Ishii423 relate to electro-optical devices and both have the same objectives of improving the image quality, a POSITA would have been motivated to use the techniques disclosed in Ishii423 of using a relay layer for an electrical connection to improve the similar device of Ishii100 in the same way. Further, Ishii100 and Ishii423 share the same inventor, and also share many of the same circuit components and structure. For example, Ishii100's "entire configuration of a liquid crystal device" shown in Figures 1 and 2 of Ishii100 appears similar to Ishii423's "schematic plan view of a liquid crystal device" shown in Figures 1 and 2 of Ishii423. (EX1004, [0024]; EX1015, [0050].) The Figure 3 pixel circuits of Ishii100 and Ishii423 are also similar to each other having pixel electrode 9a, capacitor line 300, storage capacitor 70, TFT 30, image signals S1, S2, ... Sn, data lines 6a, scanning signals G1, G2, ... Gm, and scanning lines 11. (EX1004, [0047]-[0048]; EX1015, [0088].) Further, the structures of Ishii100 and Ishii423 have a lot of similarities. Ishii100 has a display stack comprising a substrate 10, underlying insulating film 12, interlayer insulating film 41, interlayer insulating film 42, interlayer insulating film 43, pixel electrode 9a, TFT 30 disposed on underlying insulating film 12, capacitor 70 disposed on interlayer insulating film 41, data line 6a disposed on interlayer insulating film 42, and pixel electrode 9a disposed on interlayer insulating film 43. (EX1004, [0062]-[0063], [0065]-[0066], Fig. 5.) Ishii423 has a display stack comprising a substrate

10, base insulating film 12, interlayer insulating film 41, interlayer insulating film 42, interlayer insulating film 43, pixel electrode 9a, TFT 30 disposed on underlying insulating film 12, capacitor 70 disposed on interlayer insulating film 41, data line 6a disposed on interlayer insulating film 42, and pixel electrode 9a disposed on interlayer insulating film 43. (EX1015, [0112]-[0114], Figs. 5, 6.) Thus, it would have been obvious to combine the references and their teachings.

3. Claim 2: “The TFT array substrate of claim 1, wherein the opening overlaps with the lower electrode.”

92. As shown above, Ishii100 teaches claim 2.

C. Claims 3-5 And 10-14 Are Obvious Over Park And Ishii100

1. Summary of Park

93. Park relates “to an active matrix electro luminescence display (ELD) device having thin film transistors and manufacturing method for the same.” (EX1005, [0003].)

94. Park states that there are inorganic ELD devices and organic ELD devices. (EX1005, [0003].) Park explains that the organic ELD device “emits light by recombination of an electron and a hole and thus it is referred to as an organic light emitting diode (OLED).” (*Id.*) Park discloses that these OLED devices have advantages including being “self-luminescent,” able to “display every color[] in the visible range,” and having “a high brightness and a low action voltage” that makes them “suitable for an ultra-thin type display device.” (*Id.*) For

example, Park states: “[r]ecently, an active matrix type display in which a plurality of pixels is arranged in a matrix form and a thin film transistor is connected thereto has been widely applied to the flat panel display devices.” (*Id.*)

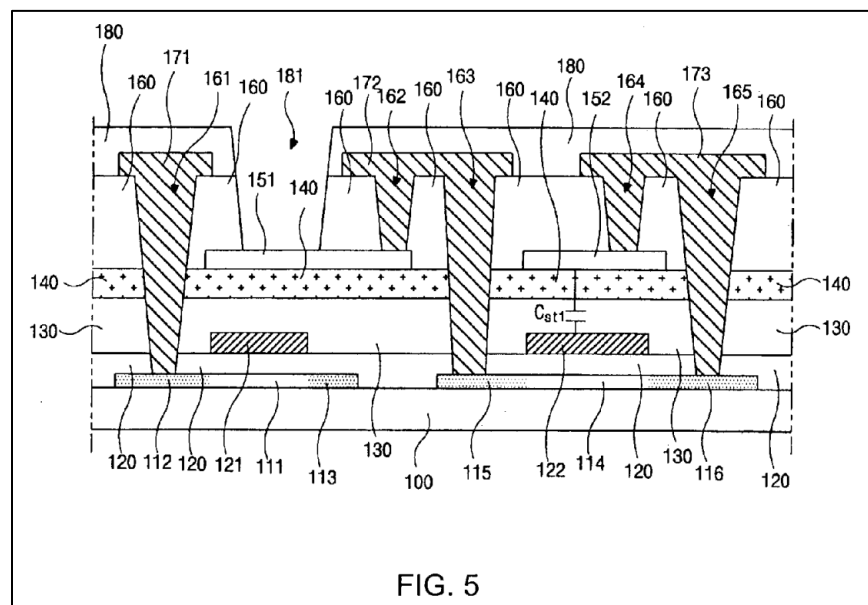
95. Referring to Figure 1, Park discloses that “a pixel of the active matrix organic electro luminescent display device” (prior art) “has a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7.” (EX1005, [0006].) Park explains that the storage capacitor “is for keeping a gate driving voltage of the driving thin film transistor stable and is an important element for displaying high quality images by restraining a pixel voltage fluctuation that is induced by a kick-back voltage of the switching film transistor and a leakage current.” (EX1005, [0015].) The capacitance of the storage capacitor is directly proportional to the area of the electrodes and inversely proportional to the thickness of the dielectric substance. (*Id.*) Therefore, there is a limit to reducing the thickness of the dielectric substance. (*Id.*) But “[i]f the area of the electrode of the storage capacitor is increased, it results in a decrease of an area of the pixel electrode, i.e., the anode electrode 60, and thus an aperture ratio is decreased.” (*Id.*)

96. Referring to Figure 4, Park explains that prior art has been able to overcome this problem. Park states, however, that while this structure of an active matrix organic ELD device can reduce the thickness of the dielectric substance and

increase the storage capacitance of the storage capacitor, the manufacturing process is time-consuming and costly. (EX1005, [0015].)

97. Park therefore discloses “an active matrix organic electro luminescent display (ELD) device in which a storage capacitance of a storage capacitor is increased without reducing an aperture ratio,” and where manufacturing time and cost are reduced. (EX1005, [0017].)

98. Figure 5 below illustrates an embodiment of Park's active matrix organic electro luminescent display device. (EX1005, [0034].)



2. Claim 3

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

(i) Park

99. Park teaches “[a] thin film transistor (TFT) array substrate.” For example, Park discloses an active matrix organic electro luminescent display device that has thin film transistors. (EX1005, [0034] (“The first gate electrode 121, the first source electrode 171 and the first drain electrode (not shown), form *a switching thin film transistor*, and the second gate electrode 122, the second source electrode 173 and the second drain electrode 172 form *a driving thin film transistor*.”) (emphasis added).)

100. Park also discloses that “a pixel of the active matrix organic electro luminescent display device has *a switching thin film transistor 4, a driving thin film transistor 5*, a storage capacitor 6 and a light emitting diode (LED) 7.” (EX1005, [0006] (emphasis added), Fig. 1.)

101. Park describes the plurality of TFTs as part of “an *array substrate* of the active matrix organic electroluminescent display device.” (EX1005, [0014] (emphasis added).) Thus, Park teaches the preamble of claim 3.

(ii) Ishii100

102. The preamble of claim 3 is similar to the preamble of claim 1, which Ishii100 teaches. (See IX.A.2.a.) The table below shows the similarities.

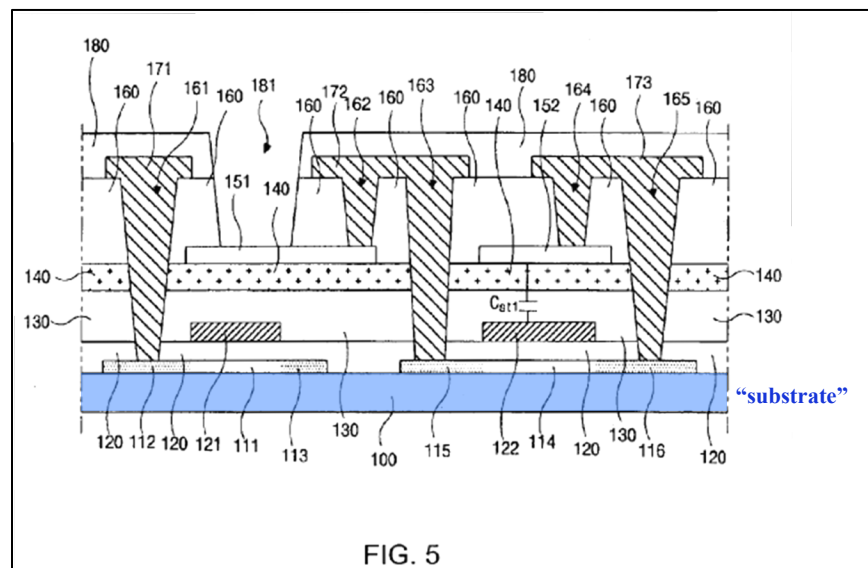
Preamble of Claim 1	Preamble of Claim 3
“A thin film transistor (TFT) array substrate comprising:”	“A thin film transistor (TFT) array substrate comprising:”

b. 3[a]: “a substrate;”

(i) Park

103. Park teaches “a substrate.” For example, Park’s active matrix organic electro luminescent display device “is formed on a transparent insulating substrate.” (EX1005, [0034].)

104. As shown in annotated Figure 5 below, Park discloses “a transparent substrate 100.” (EX1005, [0034].)



105. As another example, claim 1 of Park recites: “[a]n active matrix organic electro luminescent display (ELD) device, comprising: ***a substrate.***” (EX1005, cl. 1 (emphasis added).) Thus, Park teaches element 3[a].

(ii) Ishii100

106. Element 3[a] is similar to element 1[a], which Ishii100 teaches.

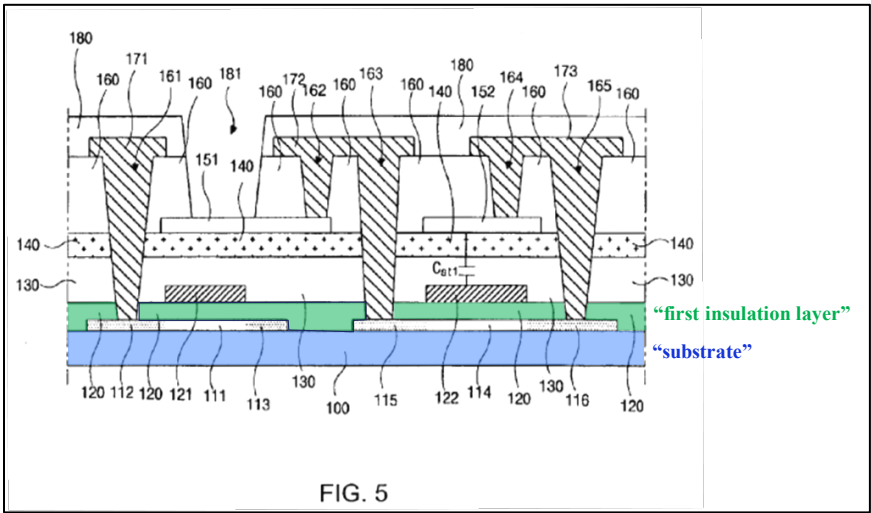
(See IX.A.2.b.) The table below shows the similarities.

Element 1[a]	Element 3[a]
“a substrate;”	“a substrate;”

c. 3[b]: “a first insulation layer on the substrate;”

(i) Park

107. Park teaches “a first insulation layer on the substrate.” As shown for element 3[a], Park teaches a substrate 100 (“substrate”). Park discloses a “gate insulating layer 120.” (EX1005, [0034].) Figure 5 (annotated below) shows the *gate insulating layer 120* on the *substrate 100*. Thus, Park teaches element 3[b].



(i) Ishii100

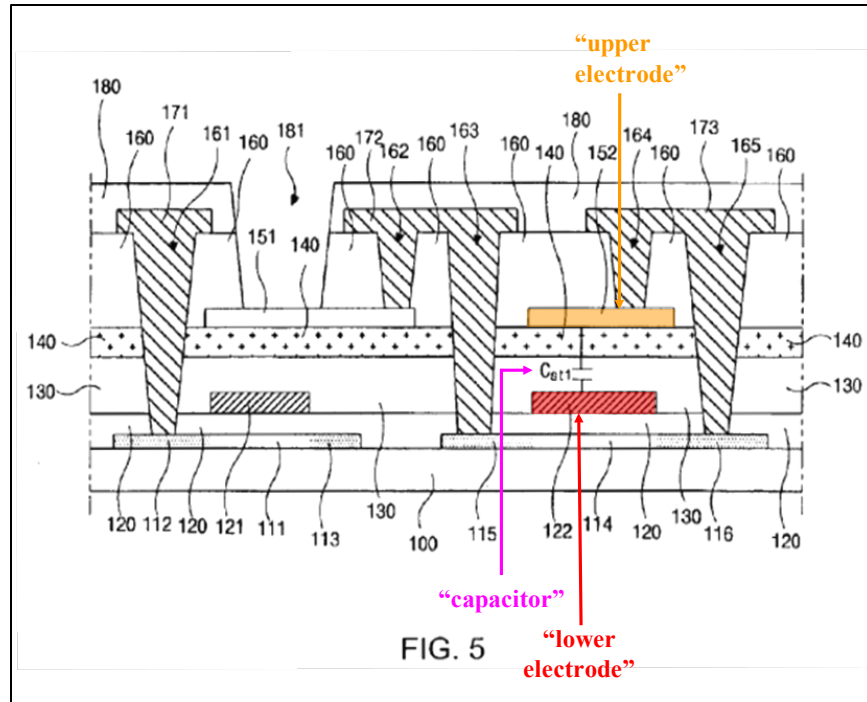
108. Element 3[b] is similar to element 1[b], which Ishii100 teaches. (See IX.A.2.c.) The table below shows the similarities.

Element 1[b]	Element 3[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

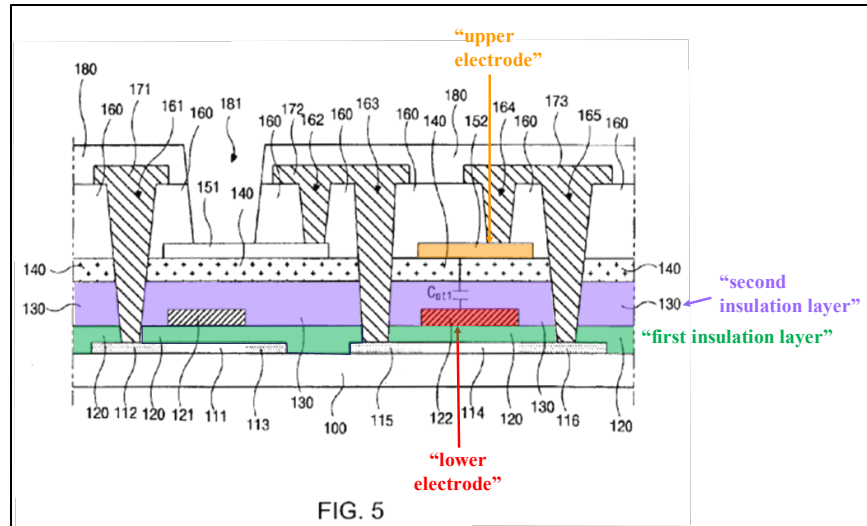
- d. 3[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

(i) Park

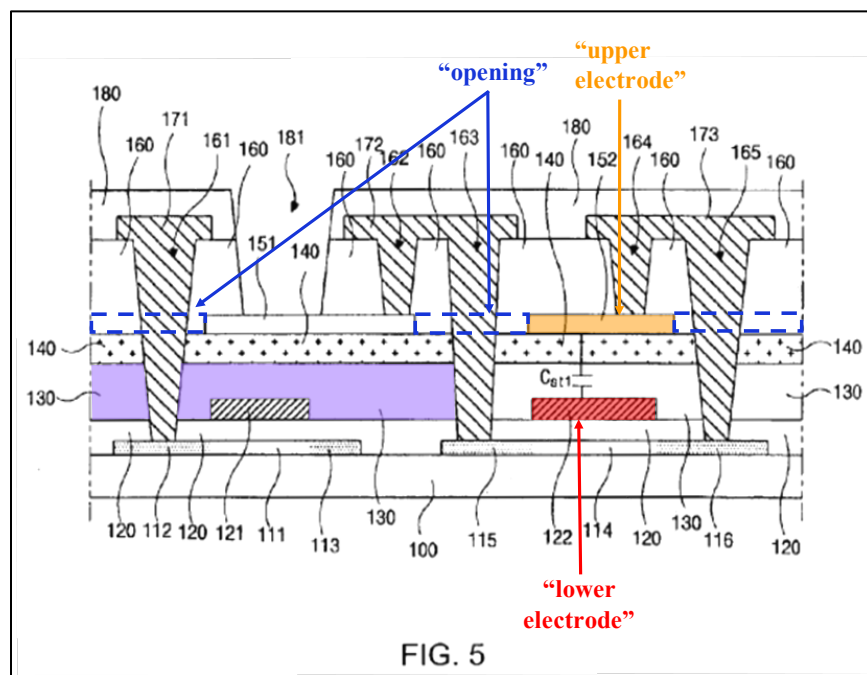
109. Park teaches “a capacitor comprising a lower electrode . . . and an upper electrode.” As shown for element 3[b], Park teaches a gate insulating layer 120 (“first insulation layer”). For example, Park discloses “[t]he capacitor electrode 152 forms a storage capacitor C_{st1} together with the second gate electrode 122.” (EX1005, [0034].) Figure 5 (annotated below) shows the *storage capacitor C_{st1}* comprising a *gate electrode 122* and a *capacitor electrode 152*.



110. Park further teaches the “lower electrode on the first insulation layer, . . . wherein the upper electrode is insulated from the lower electrode by a second insulation layer.” For example, Park discloses “[f]irst and second *inter layers 130* and *140 are sequentially formed on the first and second gate electrodes 121 and 122.*” (EX1005, [0034] (emphases added).) Figure 5 (annotated below) shows the *gate electrode 122* on the *gate insulating layer 120*, wherein the *capacitor electrode 152* is insulated from the gate electrode 122 by an *inter layer 130*.



111. Park additionally teaches the “upper electrode arranged to overlap with the whole lower electrode and having an opening.” Figure 5 (annotated below) shows the *capacitor electrode 152* arranged to overlap with the whole *gate electrode 122* and having an *opening*. Thus, Park teaches element 3[c].



(ii) Ishii100

112. Element 3[c] is similar to element 1[c], except that it does not require that the “upper electrode extend[] beyond an edge of the lower electrode,” as shown in the table below. Ishii100 teaches 1[c], and thus, teaches element 3[c].

(See IX.A.2.d.)

Element 1[c]	Element 3[c]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, <i>the upper electrode extending beyond an edge of the lower electrode</i> and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

(iii) Motivation to combine Park and Ishii100

113. It would have been obvious to a POSITA at the time of the '730 patent to combine the teachings of Park and Ishii100. Park and Ishii100 both relate to light-emitting devices and structures, including teachings for overcoming manufacturing limitations. For example, both address increasing the capacitance of the storage capacitor in the light-emitting devices. Park discloses “an active matrix organic electro luminescent display (ELD) device in which a storage capacitance of a storage capacitor is increased without reducing an aperture ratio and number of masks needed is reduced.” (EX1005, [0017].) Similarly, Ishii100 discloses an “electro-optical device having a storage capacitor of increased area,

and enabling high-definition image display, a manufacturing method thereof, an electronic apparatus, and a capacitor” that can be applied to an organic EL display. (EX1004, [0007], [0097].) Thus, Park and Ishii100 are from the same field of endeavor and reasonably pertinent to the same technical problems of improving the manufacturing and quality of light-emitting display devices, including teachings of structural configurations that increase the storage capacitance.

114. Ishii100 teaches eliminating the need for an additional mask for forming a storage capacitor by including “a self-alignment-type contact hole” in the electro-optical device, and improving the area for the pixel electrode. (EX1004, [0011].) “[A] larger storage capacitor can be formed on the substrate of the same size.” (*Id.*) Ishii100’s technical features may be combined with Park to result in an OLED with greater storage capacitance and reduced manufacturing deviations. There would have been a reasonable expectation of success because such techniques were known in the prior art and have been successfully demonstrated. Ishii100 further teaches a part of a pixel electrode 9a that provides a connection to a lower electrode of a capacitor (relay layer 71) and a TFT 30 through an opening in the upper capacitor electrode (capacitor line 300) in a manner similar to Park. Park teaches contact holes that provide a connection to a gate electrode 122 (lower electrode of the capacitor) and a switching thin film

transistor 4 through an opening of an upper electrode of the capacitor (capacitor electrode 152). (EX1004, [0058], Fig. 3; EX1005, [0006], Fig. 1.)

115. It would have been obvious to combine the teachings of Park and Ishii100. Park and Ishii100 both teach increasing the capacitance of the storage capacitor in a light-emitting display device and both teach using connection members to provide interconnections between layers. A POSITA would be motivated to use Ishii100's techniques to improve the similar device of Park in the same way. Prior art such as Park successfully demonstrated an OLED configuration that improved the capacitance of the storage capacitor.

e. 3[d]: “an inter-layer insulation film covering the capacitor;”

(i) Park

116. Park teaches “an inter-layer insulation film covering the capacitor.” As shown for element 3[c], Park teaches a storage capacitor C_{st1} (“capacitor”) comprising a capacitor electrode 152 and a gate electrode 122. Park discloses “[a] *first passivation layer 160 is formed* of material such as silicon oxide (SiO_2) *on* the anode electrode 151 and *the capacitor electrode 152.*” (EX1005, [0034] (emphases added).) Figure 5 (annotated below) shows the *passivation layer 160* covering the *capacitor C_{st1}* .



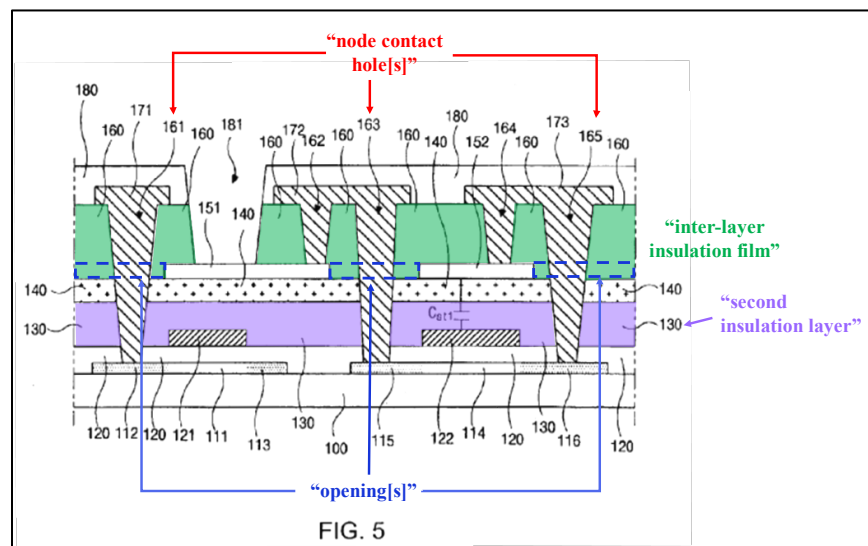
(See IX.A.2.e.) The table below shows the similarities.

f. 3[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

118. Park teaches “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening.” As shown for element 3[d], Park teaches a passivation layer 160 (“inter-layer insulation film”). As shown for element 3[c], Park teaches an “inter layer 130” (“second insulation layer”) and an “opening.”

119. Park teaches contact holes in the interlayer 130 and passivation layer 160 and within the openings of the layer of the anode electrode 151 and capacitor electrode 152. For example, Park discloses “[t]he first, third, and fifth contact holes 161, 163 and 165 are formed all the way to the gate insulating layer 120. The first contact hole 161 exposes a portion of the fast [first] source region 112, the second contact hole 162 the anode electrode 151, the third contact hole 163 the second drain region 115, the fourth contact hole 164 the capacitor electrode 152 and the fifth contact hole 165 the second source region 116.” (EX1005, [0034].)

120. Figure 5 (annotated below) shows the contact holes 161, 163, and 165 in the inter layer 130 and passivation layer 160. The figure also shows contact holes 161, 163, and 165 within the openings.



121. Park then discloses that “[t]hough it is not shown in the figure, the second gate electrode 122 is electrically connected to the first drain region 113. . . .

a first drain electrode (not shown), which is connected to the first drain region 113, . . . are also formed on the first passivation layer 160.” (EX1005, [0034].)

122. A POSITA would have understood that the drain electrode of the switching thin film transistor 4 (first drain electrode connected to the drain region 113) indicated as not shown would have a similar configuration as the source and drain electrodes shown in Figure 5. This would include a node contact hole in the interlayer 130 and passivation layer 160 for electrically connecting the drain electrode of the switching thin film transistor 4, within an opening.

(ii) Ishii100

123. Element 3[e] is similar to element 1[e], which Ishii100 teaches.

(See IX.A.2.f.) The table below shows the similarities.

Element 1[e]	Element 3[e]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

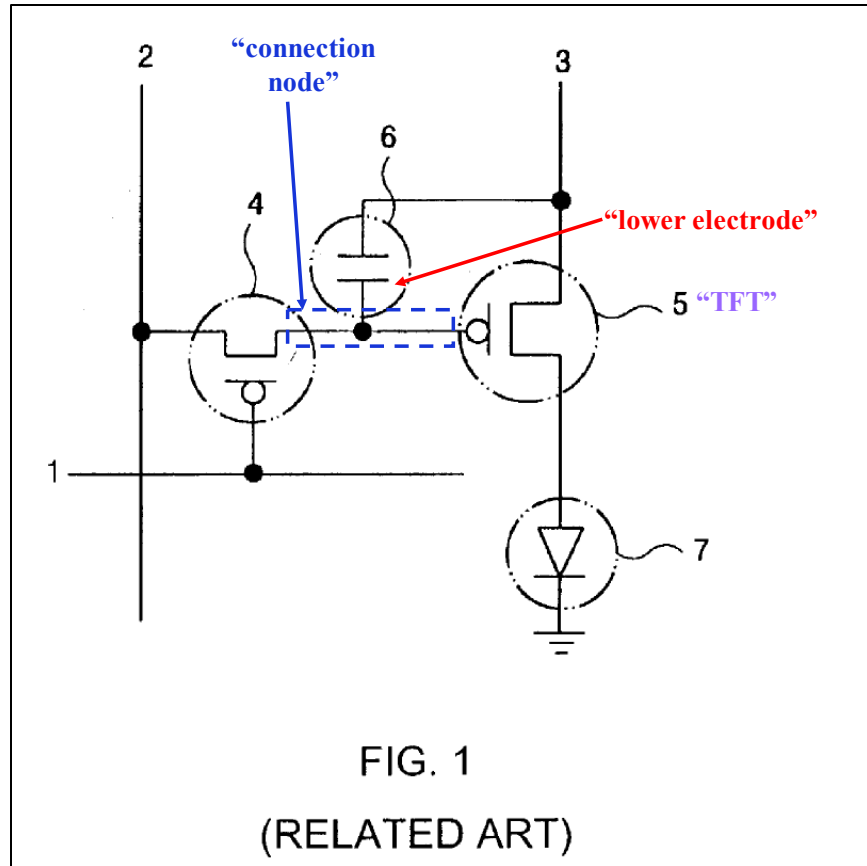
g. 3[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole,”

(i) Park

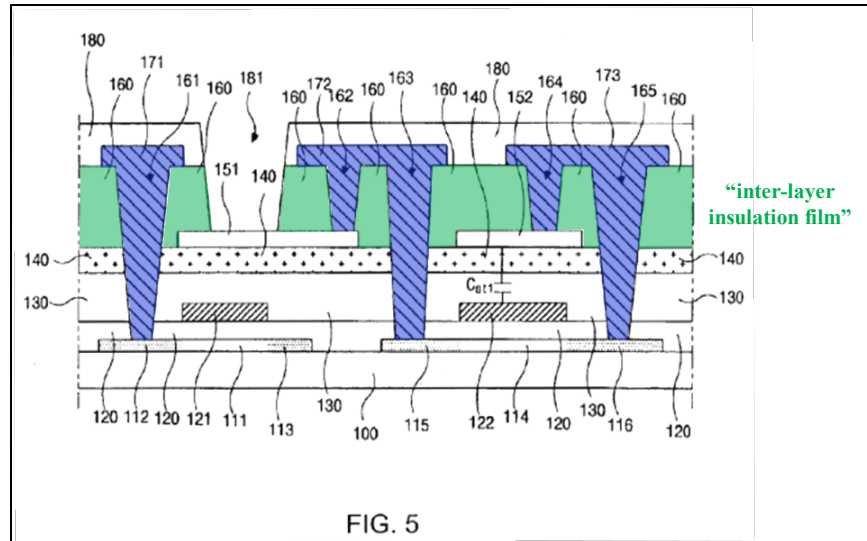
124. Park teaches “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.” As shown for element 3[e], Park teaches a passivation

layer 160 (“inter-layer insulation film”) and a “node contact hole” for electrically connecting the drain electrode of the switching thin film transistor 4 (“TFT”). As shown for element 3[c], Park teaches a gate electrode 122 (“lower electrode”).

125. Figure 1 of Park (annotated below) shows a circuit. Park explains that the “drain electrode of the switching thin film transistor 4 *is connected to* a gate electrode of the thin, film transistor 5” and a “storage capacitor 6 *is connected to* the gate electrode and the source electrode of the driving thin film transistor 5.” (EX1005, [0006] (emphasis added).) The figure shows the *drain of the switching thin film transistor 4* electrically couples the *lower electrode of the capacitor 6* and *driving thin film transistor 5*. A POSITA would have understood that the electrical coupling is through a contact hole because, as explained for element 3[e], Park teaches using contact holes for electrically coupling the drain electrode of the switching thin film transistor 4.



126. Figure 5 (annotated below) shows that contact holes connect to the sources and drains of the transistors using *source and drain electrodes*. As shown for element 3[e], a POSITA would have understood that the drain electrode of the switching thin film transistor 4 (first drain electrode connected to drain region 113) indicated as not shown would have a similar configuration as the source and drain electrodes shown in Figure 5. Thus, Park teaches a connection node on the *passivation layer 160* and further teaches element 3[f].



(ii) Ishii100

127. Element 3[f] is similar to element 1[f], which Ishii100 teaches.

(See IX.A.2.g.) The table below shows the similarities.

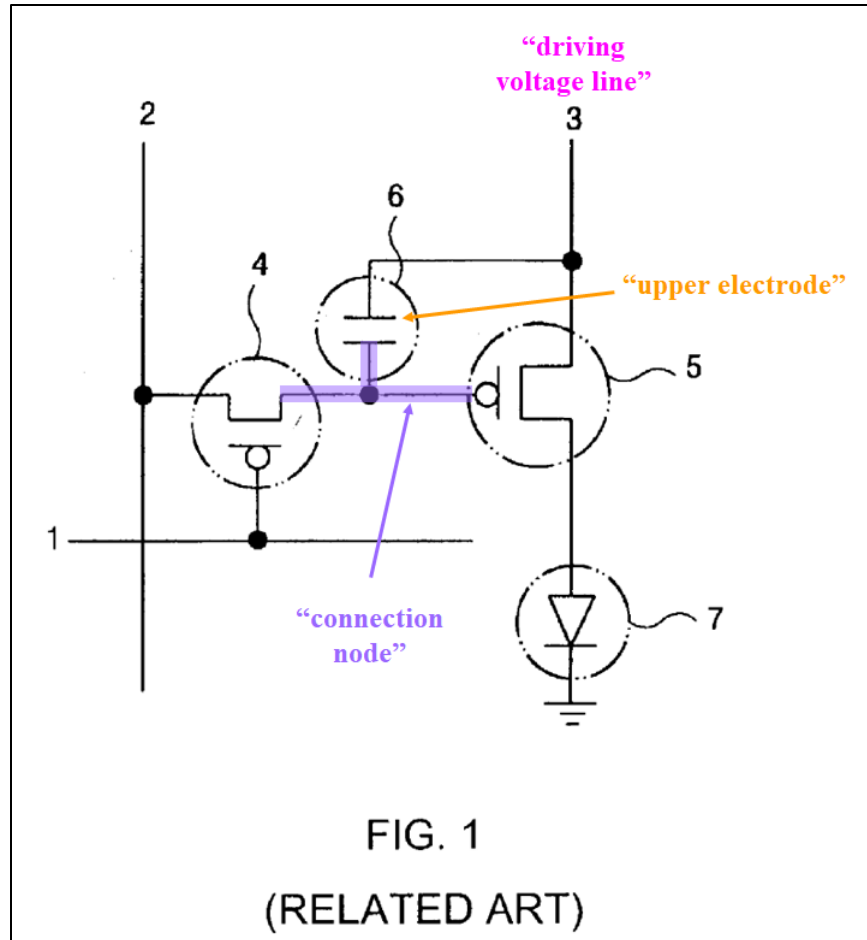
Element 1 [f]	Element 3 [f]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole,”

h. 3[g]: “wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”

128. Park teaches “the upper electrode is configured to receive a driving voltage line formed from the same layer as the connection node.” For example, Park discloses “the first drain electrode (not shown) and the power line (not shown) are formed at this time.” (EX1005, [0011].) As shown for element 3[f], Park teaches a connection node electrically connecting the gate of driving TFT 5,

the lower electrode of capacitor 6, and switching TFT 4. A POSITA would have understood that the first drain electrode (part of the connection node) and the power line being formed at the same time means the two are formed from the same layer. A display device is formed by depositing layers on top of each other sequentially, and thus, two electrodes/lines being formed at the same time means they are formed on the same layer.

129. Park also teaches “the upper electrode is configured to received a driving voltage through a driving voltage line.” As shown for element 3[c], Park teaches a capacitor electrode 152 (“upper electrode”). Park discloses the “storage capacitor 6 is connected to the gate electrode and the source electrode of the driving thin film resistor 5. If a signal is applied to the gate line 1, the switching thin film transistor 4 is turned on. If a signal of the data line 2 is applied to the gate electrode of the driving thin film transistor 5, the driving thin film transistor 5 is turned on and thus the light emitting diode (LED) 7 emits light.” (EX1005, [0006].) Figure 1 (annotated below) shows that Park’s *upper electrode* is configured to receive a driving voltage through *power line 3*. Thus, Park teaches element 3[g].



3. **Claim 4: “The TFT array substrate of claim 3, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”**

130. Ishii100-Park teaches claim 3 as shown above in Section IX.C.2.

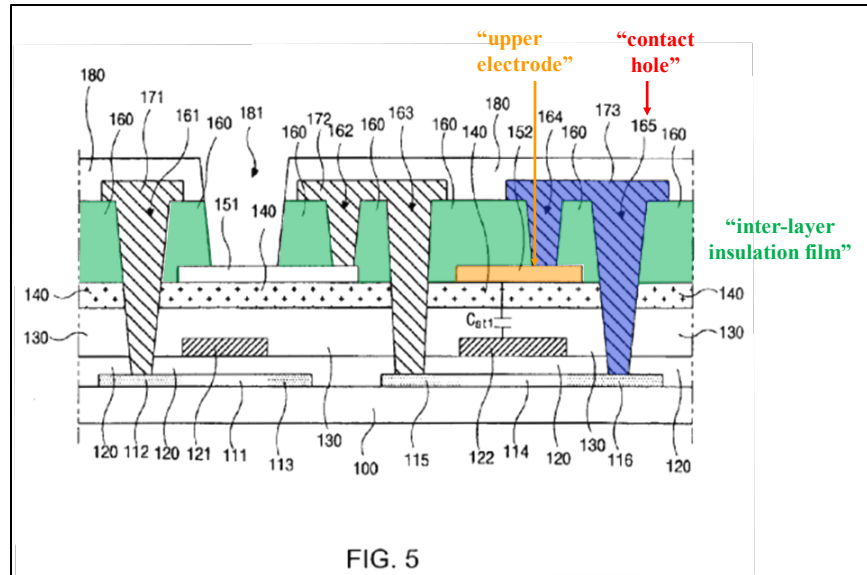
a. Park

131. As shown for element 3[c], Park teaches a capacitor electrode 152 (“upper electrode”). As shown for element 3[g], Park teaches a power line 3 (“driving voltage line”) coupled to the capacitor electrode 152 (“upper electrode”).

As shown for element 3[d], Park teaches a passivation layer 160 (“inter-layer insulation film”).

132. Park teaches “wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.” For example, Park discloses “a power line (not shown), which is connected to the second source electrode 173, are also formed on the first passivation layer 160.” (EX1005, [0034].) Park also discloses “[t]he second source electrode 173 is connected to the capacitor electrode 152 and the second source region 116 through the fourth and fifth contact holes 164 and 165.” (EX1005, [0034].) Park further discloses “[t]he second source electrode 173 may be extended from the power line (not shown) or may be formed of a portion of the power line.” (EX1005, [0034].) Figure 5 (annotated below) shows the *source electrode 173* coupled to the *capacitor electrode 152* through *contact hole 165* in the *passivation layer 160*.

Because the power line is connected to the source electrode 173, which is coupled to capacitor electrode 152 through contact holes 164 and 165, Park teaches claim 4.



b. Ishii100

133. As shown for element 1[c], Ishii100 teaches a capacitor line 300 (“upper electrode”). As shown for element 3[g], Ishii100 teaches a line (“driving voltage line”) coupled to the capacitor line 300 (“upper electrode”). As shown for element 1[d], Ishii100 teaches an interlayer insulating film 24 (“inter-layer insulation film”).

134. It would have been obvious to a POSITA to combine the teachings of Park and Ishii100. (See IX.C.2.g(ii).)

4. Claim 5

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

135. The preamble of claim 5 is similar to the preamble of 1, which Park and/or Ishii100 teach. (See IX.A.2.a.) The table below shows the similarities.

Preamble of Claim 1	Preamble of Claim 5
“A thin film transistor (TFT) array substrate comprising:”	“A thin film transistor (TFT) array substrate comprising:”

b. 5[a]: “a substrate;”

136. Element 5[a] is similar to elements 1[a] and 3[a], which Park and/or Ishii100 teach. (See IX.A.2.b, IX.C.2.b.) The table below shows the similarities.

Element 1[a]	Element 5[a]
“a substrate;”	“a substrate;”

c. 5[b]: “a first insulation layer on the substrate;”

137. Element 5[b] is similar to elements 1[b] and 3[b], which Park and/or Ishii100 teach. (See IX.A.2.c, IX.C.2.b(ii).) The table below shows the similarities.

Element 1[b]	Element 5[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

d. 5[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

138. Element 5[c] is similar to element 3[c], which Park and/or Ishii100 teach. (See IX.C.2.c(i).) The table below shows the similarities.

Element 3[c]	Element 5[c]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

e. 5[d]: “an inter-layer insulation film covering the capacitor;”

139. Element 5[d] is similar to elements 1[d] and 3[d], which Park and/or Ishii100 teach. (See IX.A.2.e, IX.C.2.d(ii).) The table below shows the similarities.

Element 1[d]	Element 5[d]
“an inter-layer insulation film covering the capacitor;”	“an inter-layer insulation film covering the capacitor;”

f. 5[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening;”

140. Element 5[e] is similar to elements 1[e] and 3[e], which Park and/or Ishii100 teach. (See IX.A.2.f, IX.C.2.e(ii).) The table below shows the similarities.

Element 1[e]	Element 5[e]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening;”

- g. **5[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole; and”**

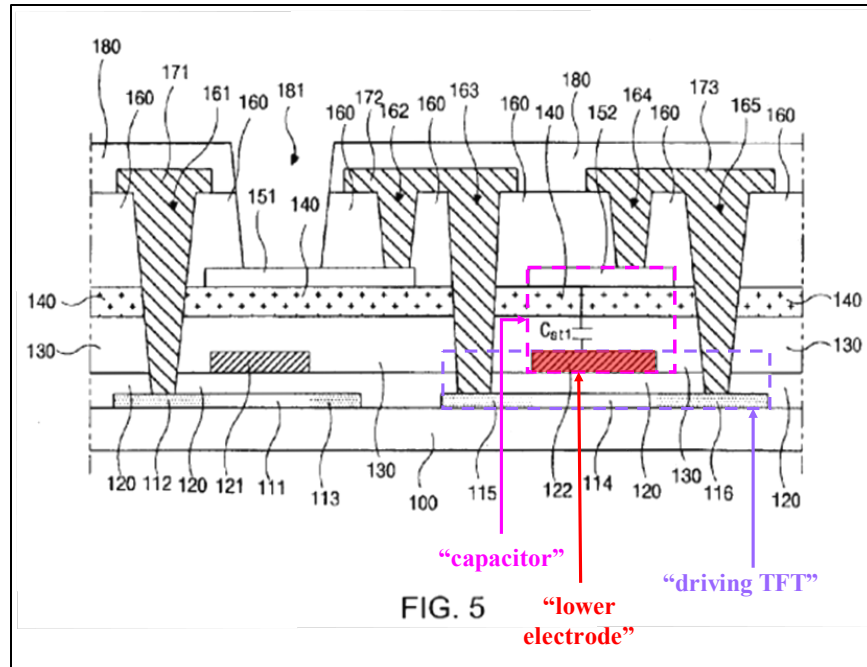
141. Element 5[f] is similar to elements 1[f] and 3[f], which Park and/or Ishii100 teach. (See IX.A.2.g, IX.C.2.f(ii).) The table below shows the similarities.

Element 1[f]	Element 5[f]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole; and”

- h. **5[g]: “a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”**

142. As shown for element 3[c], Park teaches a storage capacitor C_{st1} (“capacitor”) and a gate electrode 122 (“lower electrode”).

143. Park teaches “a driving TFT arranged to overlap with the capacitor.” For example, Park discloses “[t]he capacitor electrode 152 forms a storage capacitor C_{st1} together with the second gate electrode 122.” Figure 5 (annotated below) shows the *driving TFT 4* arranged to overlap with the *capacitor Cst1*.



144. Park also teaches "a driving gate electrode of the driving TFT comprises the lower electrode." For example, Park discloses "*the second gate electrode 122*, the second source electrode 173 and the second drain electrode 172 *form a driving thin film transistor.*" (EX1005, [0034] (emphases added).) Figure 5 (annotated above) shows the *gate electrode 122* of the driving TFT 5 comprising the lower electrode.

5. Claim 10

a. **Preamble: "An organic light-emitting diode (OLED) display comprising:"**

(i) **Park**

145. Park teaches "[a]n organic light-emitting diode (OLED) display." For example, Park discloses an "organic electro luminescence display (ELD) device

emits light by recombination of an electron and a hole and thus it is referred to as an organic light emitting diode (OLED).” (EX1005, [0005].)

(ii) Ishii100

146. Ishii100 teaches “[a]n organic light-emitting diode (OLED) display.” For example, Ishii100 discloses “an electro optical device.” (EX1004, [0002].) A POSITA would have understood an OLED display as one example of an electro optical device. Further, Ishii100 discloses that “the invention can be applied to . . . an organic EL display” (EX1004, [0097].)

b. 10[a]: “a substrate;”

147. Element 10[a] is similar to elements 1[a] and 3[a], which Park and/or Ishii100 teach. (See IX.A.2.b, IX.C.2.b.) The table below shows the similarities.

Element 1[a]	Element 10[a]
“a substrate;”	“a substrate;”

c. 10[b]: “a first insulation layer on the substrate;”

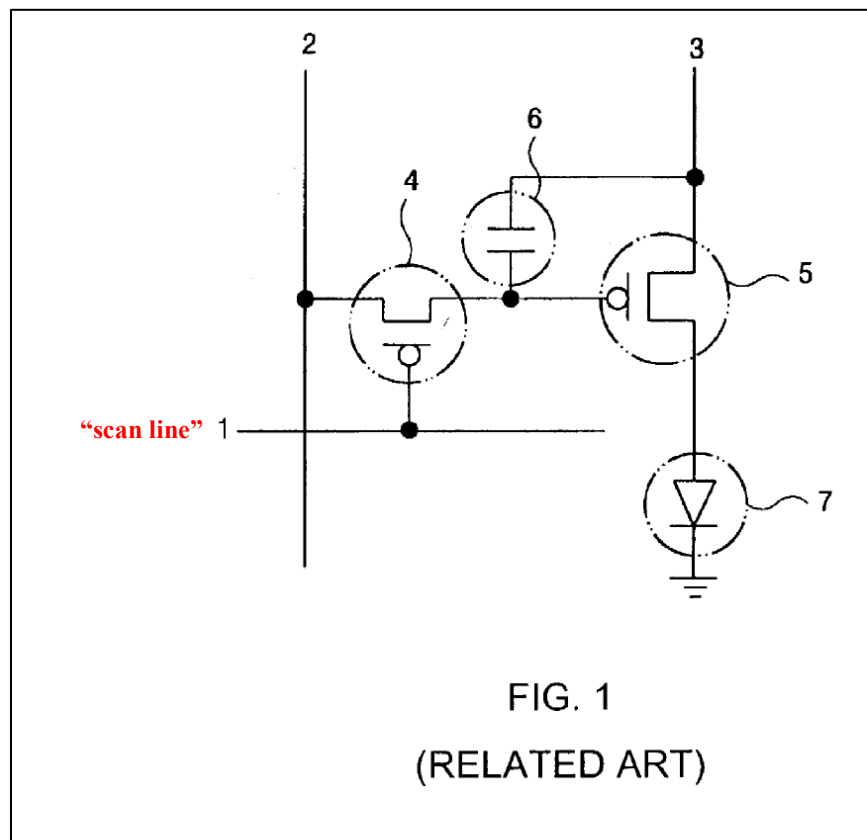
148. Element 10[b] is similar to elements 1[b] and 3[b], which Park and/or Ishii100 teach. (See IX.A.2.c, IX.C.2.b(ii).) The table below shows the similarities.

Element 1[b]	Element 10[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

d. 10[c]: “a scan line on the first insulation layer and configured to deliver a scan signal;”

(i) Park

149. Park teaches a “scan line . . . configured to deliver a scan signal.” For example, Park discloses “[i]f a signal is applied to the gate line 1, the switching thin film transistor 4 is turned on.” (EX1005, [0006].) A POSITA would have understood that the signal being applied to the gate line 1 is delivering a scan signal. Figure 1 (annotated below) shows the *gate line 1*. It would have been obvious to a POSITA to use a gate line to deliver a scan signal (*e.g.*, EX1017, 5:16-21).

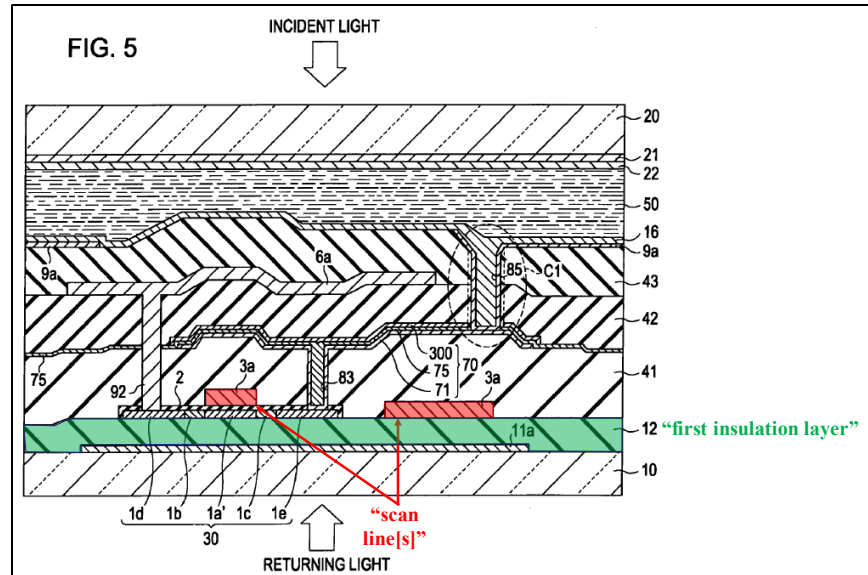


(ii) Ishii100

150. As shown in element 1[b], Ishii100 teaches an insulating film 12 (“first insulation layer”).

151. Ishii100 teaches “a scan line . . . configured to deliver a scan signal.” For example, Ishii100 discloses “*scanning lines 3a* are electrically connected to the gates of the TFTs 30, and *they are configured to sequentially apply scanning signals G1, G2, , and Gm in this order to the scanning lines 3a* in pulses with predetermined timing.” (EX1004, [0048] (emphases added).) Ishii100 also discloses “[r]eferring to FIG. 2, a laminated structure in which pixel-switching TFTs (Thin-Film Transistors) which are driver elements, and wiring lines, such as scanning lines and data lines, are provided is formed on the TFT array substrate 10.” (EX1004, [0044]; *see also* Claim 1.) A POSITA would have understood that applying scan signals to the scanning lines 3a means the scan lines are configured to deliver a scan signal.

152. Ishii100 also teaches “a scan line on the first insulation layer.” Figure 5 (annotated below) shows *scanning line 3a* on *insulating film 12*.



153. It would have been obvious to a POSITA to combine the teachings of Park and Ishii100. (See IX.C.2.g(ii).)

- e. **10[d]: “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”**

(i) Park

154. As shown for element 3[g], Park teaches a power line 3 (“driving voltage line”) configured to deliver a driving voltage. As shown for element 3[d], Park teaches a passivation layer 160 (“inter-layer insulation film”). As shown for element 3[c], Park teaches a second inter layer 130 (“second insulation layer”).

155. Park discloses a source electrode of the switching thin film transistor 4 is connected to the data line 2. When the **data line 2** is applied to the gate

electrode of the driving thin film transistor 5, the driving thin film transistor 5 is turned on and the LED 7 emits light. (EX1005, [0006].)

156. It would have been obvious to a POSITA to use the same material to for the data line and the first source electrode 171 and to form it in the same layer (e.g., EX1016, 8:65-67). Figure 5 (annotated below) shows the *data line 2* and the *power line 3* being insulated by *passivation layer 160* and *second inter layer 130*.

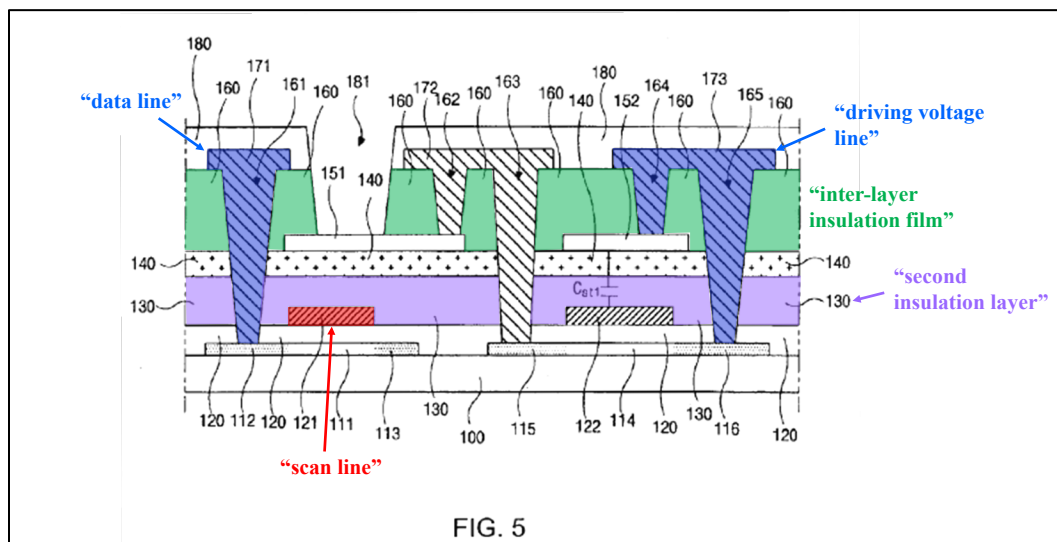


FIG. 5

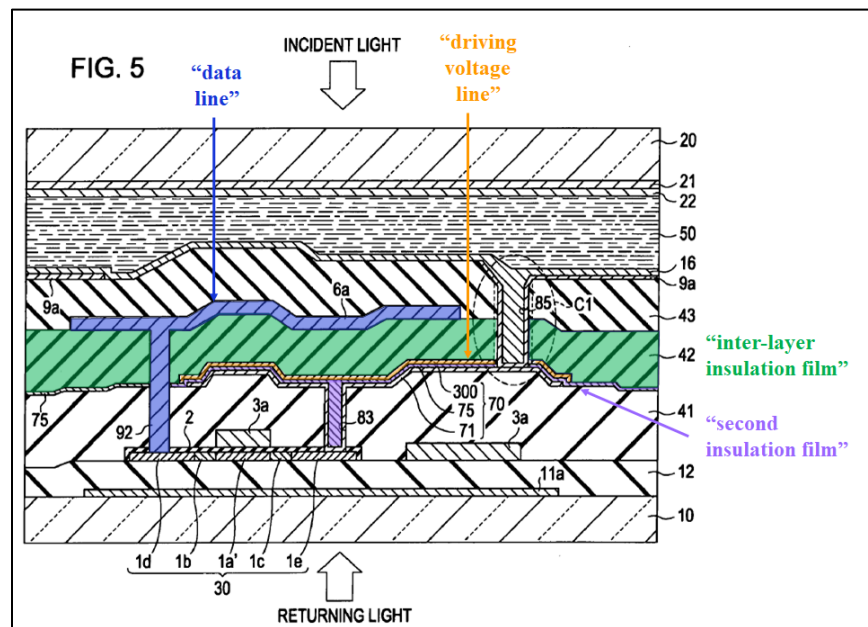
(ii) Ishii100

157. As shown for element 3[g], Ishii100 teaches a capacitor line 300 (“driving voltage line”) configured to deliver a predetermined / fixed potential (“driving voltage”). As shown for element 1[c], Ishii100 teaches a dielectric film 75 (“second insulation layer”). As shown for element 1[d], Ishii100 teaches an interlayer insulating film 42 (“inter-layer insulation film”).

158. Ishii100 teaches a “data line . . . configured to [] deliver a data signal.” For example, Ishii100 discloses “[r]eferring to FIG.3, in each of the plurality of

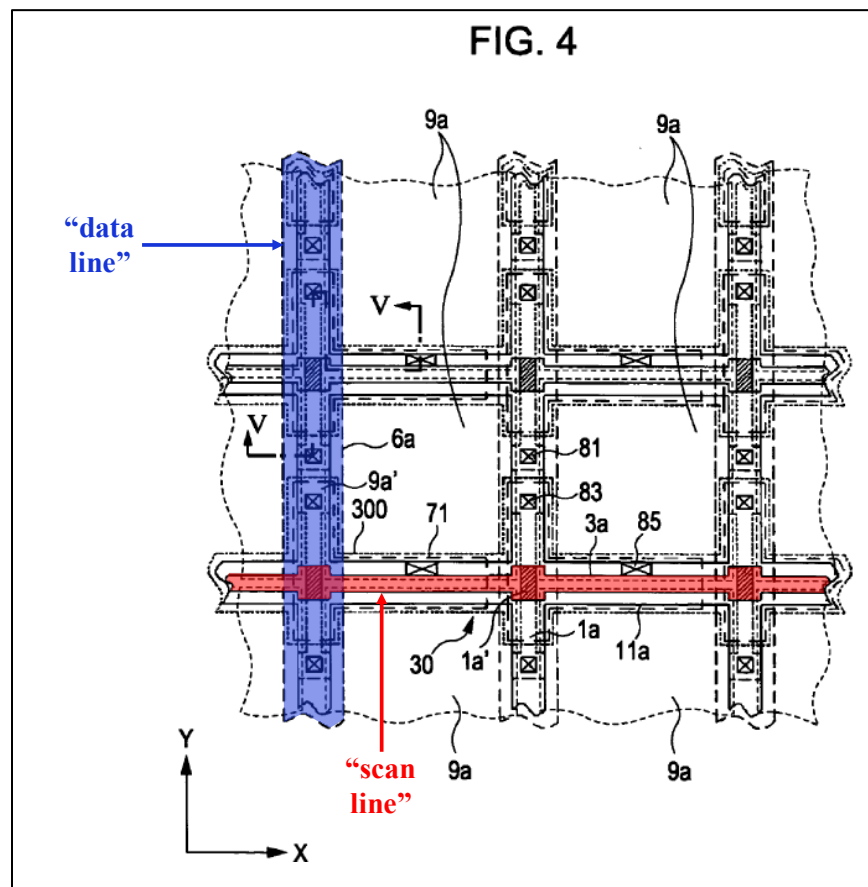
pixel portions formed in a matrix in the image display region 10a (refer to FIG. 1) of the liquid crystal device according to this embodiment, a pixel electrode 9a and a TFT 30 for controlling switching of the pixel electrode 9a are formed, and *a data line 6a to which an image signal S1, S2, ..., or Sn as will be described below is supplied* is electrically connected to the source of the TFT 30.” (EX1004, [0047] (emphasis added).)

159. Ishii100 further teaches “the data line and the driving voltage line being insulated by a second insulation layer and . . . an inter-layer insulation film.” Figure 5 (annotated below) shows the *data line 6* and the *capacitor line 300* being insulated by *interlayer insulating film 42* and *dielectric film 75*.

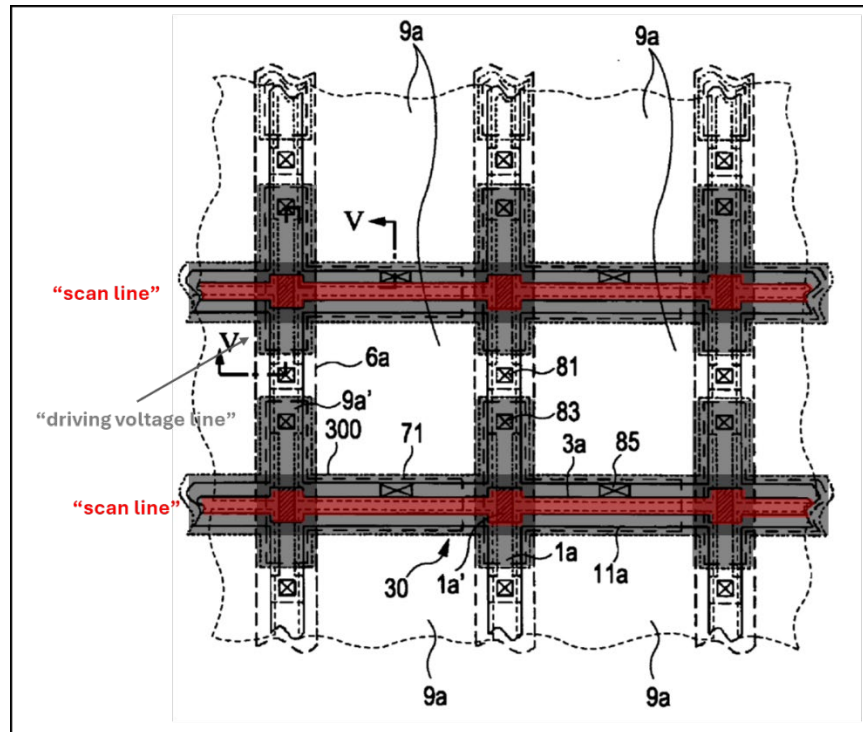


160. Ishii100 also teaches “a data line . . . crossing the scan line.” For example, Ishii100 discloses “[r]eferring to FIG. 4, a plurality of pixel electrodes 9a

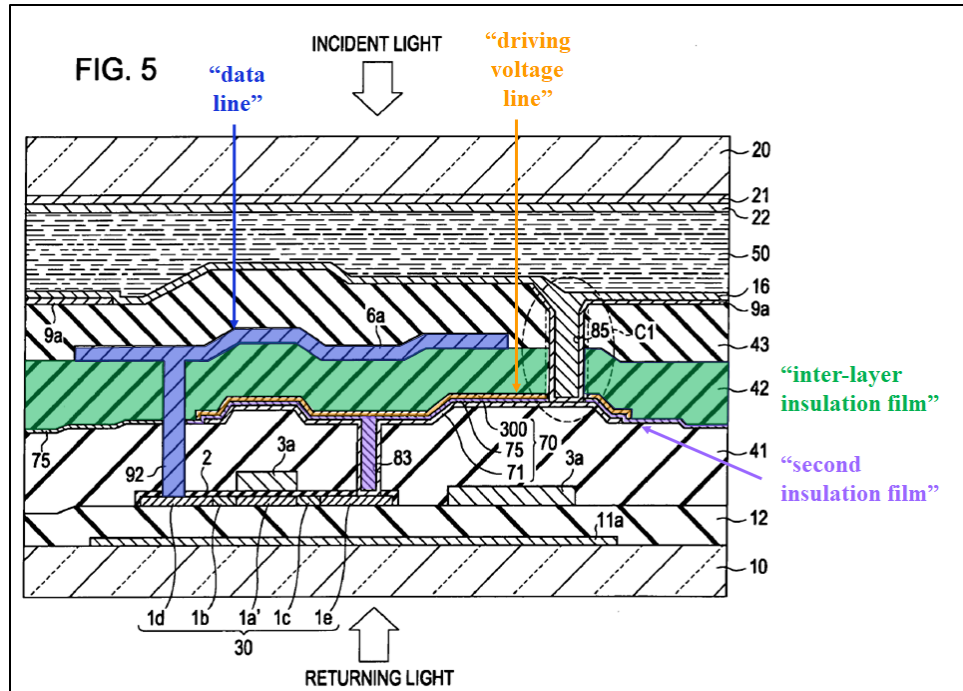
are provided in a matrix on the TFT array substrate 10 (their contours are shown by dotted-line portions 9a), and *the data lines 6a and the scanning lines 3a are provided along vertical and horizontal boundaries of the pixel electrodes 9a, respectively.*” (EX1004, [0052].) Ishii100 also discloses “a plurality of scanning lines and a plurality of data lines which intersect one another.” (EX1004, Claim 1.) Figure 4 (annotated below) shows the *data line 6* crossing the *scan line 3a*.



161. Ishii100 also teaches that the driving line 300 crosses the scan line at each intersection. Figure 4 (annotated below) shows that driving line 300 (gray) crosses the *scan line*.



162. Ishii100 teaches “the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film.” As shown in Figure 5 (annotated below), the *data line 6a* and the *capacitor line 300* are insulated by *interlayer insulating film 42* and *dielectric film 75*.



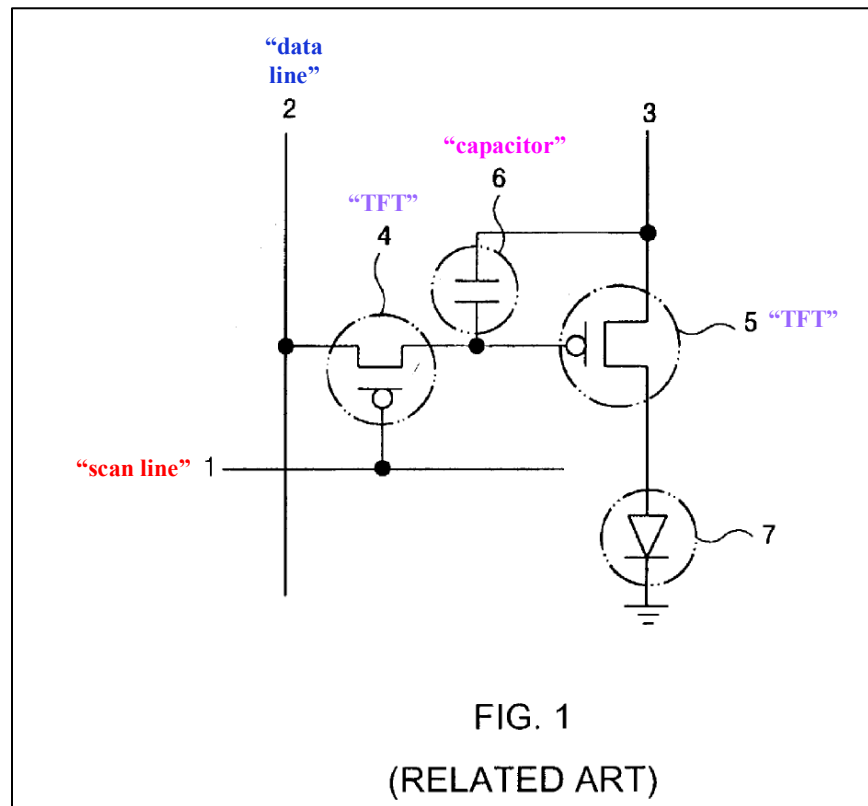
f. 10[e]: “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

(i) Park

163. As shown for element 3[g], Park teaches a power line 3 (“driving voltage line”). As shown for element 10[c], Park teaches a gate line 1 (“scan line”). As shown for element 3[f], Park teaches a TFT 30 (“TFT”). As shown for element 3[c], Park teaches a storage capacitor C_{stl} (“capacitor”).

164. Park teaches “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor.” Park discloses “[i]n FIG. 1, a pixel of the active matrix organic electroluminescent display device has a *switching thin film transistor 4*, a *driving thin film transistor 5*, a *storage capacitor 6* and a light emitting diode (LED) 7. . . . A gate electrode

of the *switching thin film transistor 4* is connected to the *gate lane 1* and a *source electrode is connected to the data line 2.*” (EX1005, [0006] (emphases added).) Figure 1 (annotated below) shows Park’s circuit coupled to the *gate line 1* and the *data line 2* and comprising a *switching TFT 4*, a *driving TFT 5*, and a *storage capacitor 6.*”

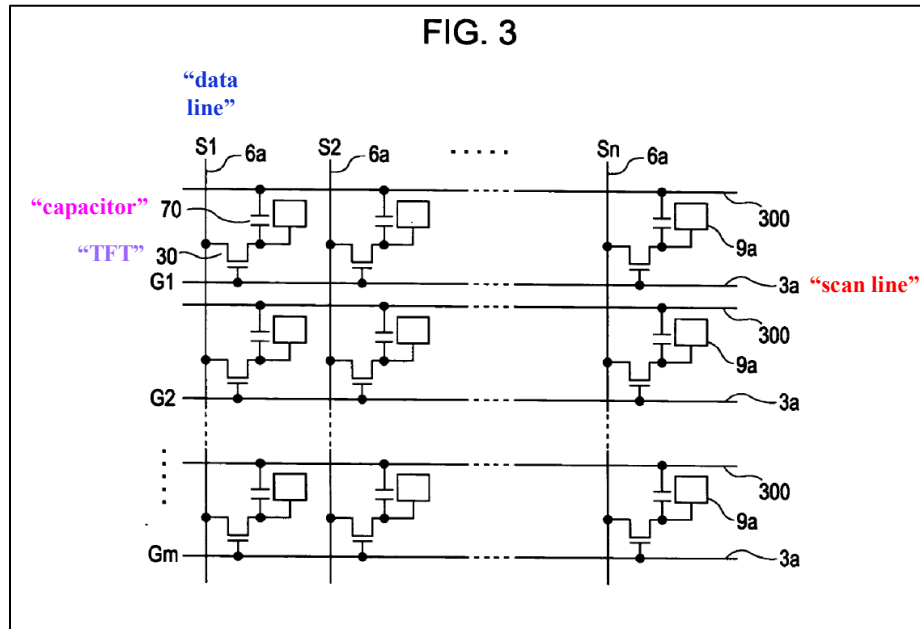


(ii) Ishii100

165. As shown for element 10[c], Ishii100 teaches a scanning line 3a (“scan line”). As shown for element 10[d], Ishii100 teaches a data line 6a (“data line”).

166. Ishii100 teaches “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor.” For example, Ishii100 discloses “FIG. 3 shows an equivalent *circuit* of various elements, wiring lines, etc. in a plurality of pixel portions which are formed in a matrix and which constitute the image display region of the liquid crystal device.” (EX1004, [0046] (emphasis added).) “Referring to FIG.3, in each of the plurality of pixel portions formed in a matrix in the image display region 10a (refer to FIG. 1) of the liquid crystal device according to this embodiment, a pixel electrode 9a and *a TFT 30* for controlling switching of the pixel electrode 9a are formed, and a *data line 6a* to which an image signal S1, S2, ..., or Sn as will be described below is supplied is electrically connected to the source of the TFT 30.” (EX1004, [0047].) Ishii100 also discloses *scanning lines 3a are electrically connected to the gates of the TFTs 30*, and they are configured to sequentially apply scanning signals G1, G2, , and Gm in this order to the scanning lines 3a in pulses with predetermined timing. *The pixel electrodes 9 are electrically connected to the drains of the TFTs 30 to write the pixel signals S1, S2, ... and Sn supplied from the data lines 6a* in the respective pixels with predetermined timing by switching on the TFTs 30 which are switching elements for a certain period.” (EX1004, [0048].) Figure 3 (annotated below) shows the pixel circuit coupled to

the *scan line 3a* and the *data line 6a* and comprising at least one *TFT 30* and a *capacitor 70*.



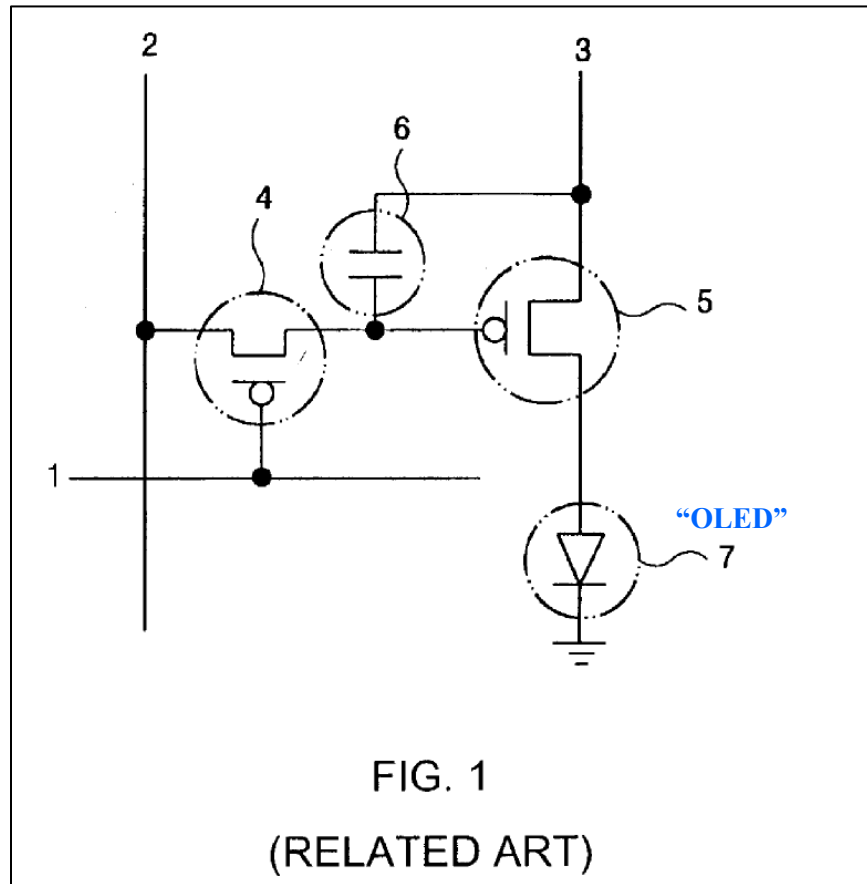
167. It would have been obvious to a POSITA to combine the teachings of Park and Ishii100. (See IX.C.2.g(ii).)

g. 10[f]: “an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

(i) Park

168. Park teaches “an OLED for emitting light by receiving the driving voltage from the pixel circuit.” For example, Park’s Figure 1 pixel circuit shows and discloses “[i]f a signal of the data line 2 is applied to the gate electrode of the driving thin film transistor 5, the driving thin film transistor 5 is turned on and thus the light emitting diode (LED) 7 emits light.” (EX1005, [0006].) Park also discloses “the organic electro luminescence display (ELD) device emits light by

recombination of an electron and a hole and thus it is referred to as an organic light emitting diode (OLED).” (EX1005, [0005].) A POSITA would have understood Park’s OLED 7 emits light by receiving a driving voltage from the Figure 1 circuit (below).

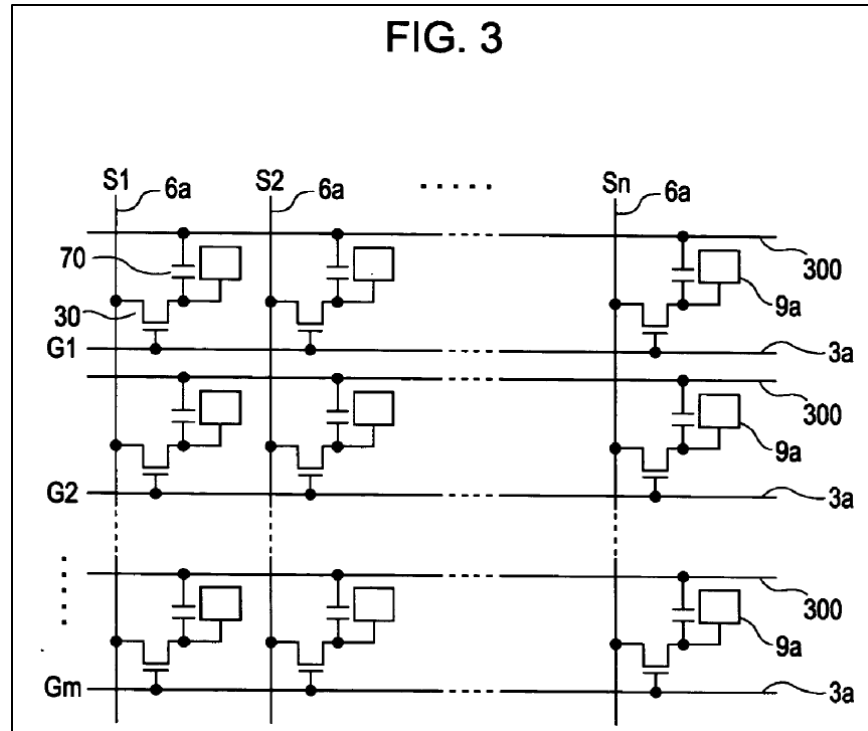


(ii) Ishii100

169. Ishii100 teaches “an OLED for emitting light by receiving the driving voltage from the pixel circuit.” For example, Ishii100 discloses “[p]redetermined levels of the pixel signals $S1$ $S2$, . . . and S_n written in the liquid crystal as an electro-optical material through the pixel electrodes 9a are maintained for a

certain period between the TFT array substrate and the counter electrode 21 formed in the counter substrate.” (EX1004, [0049].) Ishii100 also discloses “[i]f an electro optical device is in a normally white mode, *the transmittance to incident light decreases according to voltage applied in units of pixels*, and if the electro-optical device is in a normally black mode, *the transmittance to incident light increases according to voltage applied in units of pixels*. As a result, light with a contrast according to image signals is emitted from the whole electro-optical device.” (EX1004, [0049].) Thus, Ishii100 teaches transmitting light by receiving a voltage.

170. Figure 3 (below) shows a part of the pixel electrode 9a receiving the voltage from the pixel circuit. Further, Ishii100 teaches that “the invention can be applied to . . . an organic EL display . . .” (EX1004, [0097].)



171. It would have been obvious to a POSITA to combine the teachings of Park and Ishii100. (See IX.C.2.g(ii).)

- h. 10[g]: “wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”**

172. Element 10[g] is similar to element 1[c], which Ishii100 teaches. (See IX.A.2.d.) The table below shows the similarities.

Element 1[c]	Element 10[g]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”

- i. **10[h]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”**

173. Element 10[h] is similar to element 1[e], which Ishii100 teaches.

(See IX.A.2.f.) The table below shows the similarities.

Element 1[e]	Element 10[h]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

- j. **10[i]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole.”**

174. Element 10[i] is similar to element 1[f], which Ishii100 teaches.

(See IX.A.2.g.) The table below shows the similarities.

Element 1[f]	Element 10[i]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole.”

6. Claim 11: “The OLED display of claim 10, wherein the opening overlaps with the lower electrode.”

175. Ishii100-Park teaches claim 10 as shown above in Section IX.C.5.

176. Claim 11 is similar to claim 2, which Ishii100 teaches. (*See* IX.A.3.)

The table below shows the similarities.

Claim 2	Claim 11
“The TFT array substrate of claim 1, wherein the opening overlaps with the lower electrode.”	“The OLED display of claim 10, wherein the opening overlaps with the lower electrode.”

7. Claim 12

a. Preamble: “An organic light-emitting diode (OLED) display comprising:”

177. The preamble of claim 12 is similar to the preamble of claim 10, which Park and/or Ishii100 teach. (*See* IX.C.5.a.) The table below shows the similarities.

Preamble of Claim 10	Preamble of Claim 12
“An organic light-emitting diode (OLED) display comprising:”	“An organic light-emitting diode (OLED) display comprising:”

b. 12[a]: “a substrate;”

178. Element 12[a] is similar to elements 1[a] and 3[a], which Park and/or Ishii100 teach. (*See* IX.A.2.b, IX.C.2.a.) The table below shows the similarities.

Element 1[a]	Element 12[a]
“a substrate;”	“substrate;”

c. 12[b]: “a first insulation layer on the substrate;”

179. Element 12[b] is similar to elements 1[b] and 3[b], which Park and/or Ishii100 teach. (See IX.A.2.c, IX.C.2.b.) The table below shows the similarities.

Element 1[b]	Element 12[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

d. 12[c]: “a scan line on the first insulation layer and configured to deliver a scan signal;”

180. Element 12[c] is similar to element 10[c], which Park and/or Ishii100 teach. (See IX.C.5.d.) The table below shows the similarities.

Element 10[c]	Element 12[c]
“a scan line on the first insulation layer and configured to deliver a scan signal;”	“a scan line on the first insulation layer and configured to deliver a scan signal;”

e. 12[d]: “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

181. Element 12[d] is similar to element 10[d], which Ishii100 teaches. (See IX.C.5.e.) The table below shows the similarities.

Element 10[d]	Element 12[d]
“a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”	“a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

f. 12[e]: “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

182. Element 12[e] is similar to element 10[e], which Park and/or Ishii100 teach. (See IX.C.5.f.) The table below shows the similarities.

Element 10[e]	Element 12[e]
“a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”	“a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

g. 12[f]: “an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

183. Element 12[f] is similar to element 10[f], which Park and/or Ishii100 teach. (See IX.C.5.g.) The table below shows the similarities.

Element 10[f]	Element 12[f]
“an OLED for emitting light by receiving the driving voltage from the pixel circuit,”	“an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

- h. 12[g]: “wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”**

184. Element 12[g] is similar to element 3[c], which Park and/or Ishii100 teach. (See IX.C.2.c(i).) The table below shows the similarities.

Element 3[c]	Element 12[g]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”

- i. 12[h]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”**

185. Element 12[h] is similar to elements 1[e] and 3[e], which Park and/or Ishii100 teach. (See IX.A.2.f, IX.C.2.e(ii).) The table below shows the similarities.

Element 1[e]	Element 12[h]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

- j. **12[i]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole,”**

186. Element 12[i] is similar to elements 1[f] and 3[f], which Park and/or Ishii100 teach. (See IX.A.2.g, IX.C.2.f(ii).) The table below shows the similarities.

Element 1[f]	Element 12[i]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole,”

- k. **12[j]: “wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”**

187. Element 12[j] is similar to element 3[g], which Park and/or Ishii100 teach. (See IX.C.2.g(ii).) The table below shows the similarities.

Element 3[g]	Element 12[j]
“wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”	“wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”

8. **Claim 13: “The OLED display of claim 12, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”**

188. Ishii100-Park teaches claim 12 as shown above in Section IX.C.7.

189. Claim 13 is similar to claim 4, which Park and/or Ishii100 teach.

(See IX.C.3.) The table below shows the similarities.

Claim 4	Claim 13
“The TFT array substrate of claim 3, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”	“The OLED display of claim 12, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”

9. Claim 14

a. Preamble: “An organic light-emitting diode (OLED) display comprising:

190. The preamble of claim 14 is similar to the preamble of claim 10, which Park and/or Ishii100 teach. (See IX.C.5.a.) The table below shows the similarities.

Preamble of Claim 10	Preamble of Claim 14
“An organic light-emitting diode (OLED) display comprising:”	“An organic light-emitting diode (OLED) display comprising:

b. 14[a]: “a substrate;”

191. Element 14[a] is similar to elements 1[a] and 3[a], which Park and/or Ishii100 teach. (See IX.A.2.b, IX.C.2.b.) The table below shows the similarities.

Element 1[a]	Element 14[a]
“a substrate;”	“a substrate;”

c. 14[b]: “a first insulation layer on the substrate;”

192. Element 14[b] is similar to elements 1[b] and 3[b], which Park and/or Ishii100 teach. (See IX.A.2.c, IX.C.2.b(ii).) The table below shows the similarities.

Element 1[b]	Element 14[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

d. 14[c]: “a scan line on the first insulation layer and configured to deliver a scan signal;”

193. Element 14[c] is similar to element 10[c], which Park and/or Ishii100 teach. (See IX.C.5.d.) The table below shows the similarities.

Element 10[c]	Element 14[c]
“a scan line on the first insulation layer and configured to deliver a scan signal;”	“a scan line on the first insulation layer and configured to deliver a scan signal;”

e. 14[d]: “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

194. Element 14[d] is similar to element 10[d], which Ishii100 teaches. (See IX.C.5.e.) The table below shows the similarities.

Element 10[d]	Element 14[d]
“a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”	“a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

f. 14[e]: “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

195. Element 14[e] is similar to element 10[e], which Park and/or Ishii100 teach. (See IX.C.5.f.) The table below shows the similarities.

Element 10[e]	Element 14[e]
“a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”	“a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

g. 14[f]: “an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

196. Element 14[f] is similar to element 10[f], which Park and/or Ishii100 teach. (See IX.C.5.g.) The table below shows the similarities.

Element 10[f]	Element 14[f]
“an OLED for emitting light by receiving the driving voltage from the pixel circuit,”	“an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

- h. 14[g]: “wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”**

197. Element 14[g] is similar to element 3[c], which Park and/or Ishii100 teach. (See IX.C.2.c(i).) The table below shows the similarities.

Element 3[c]	Element 14[g]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”

- i. 14[h]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening;”**

198. Element 14[h] is similar to elements 1[e] and 3[e], which Park and/or Ishii100 teach. (See IX.A.2.f, IX.C.2.e(ii).) The table below shows the similarities.

Element 1[e]	Element 14[h]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening;”

- j. **14[i]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole; and”**

199. Element 14[i] is similar to elements 1[f] and 3[f], which Park and/or Ishii100 teach. (See IX.A.2.g, IX.C.2.f(ii).) The table below shows the similarities.

Element 1[f]	Element 14[i]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole; and”

- k. **14[j]: “a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”**

200. Element 14[j] is similar to element 5[g], which Park teaches. (See IX.C.4.h.) The table below shows the similarities.

Element 5[g]	Element 14[j]
“a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”	“a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”

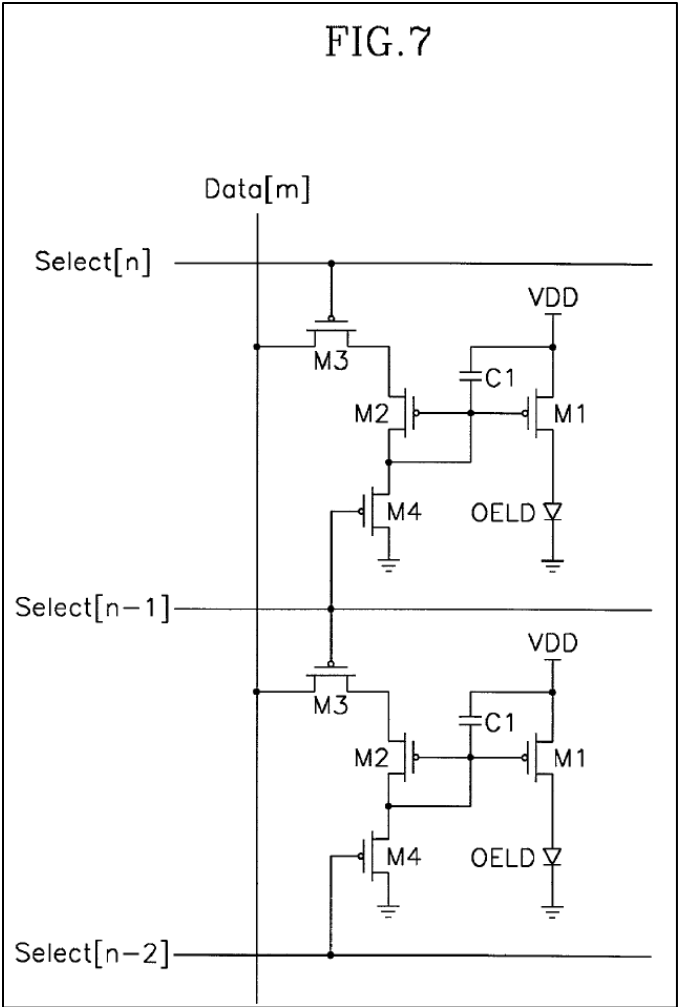
D. Claims 6-9 And 15-19 Are Obvious Over Park, Ishii100, And Kwon

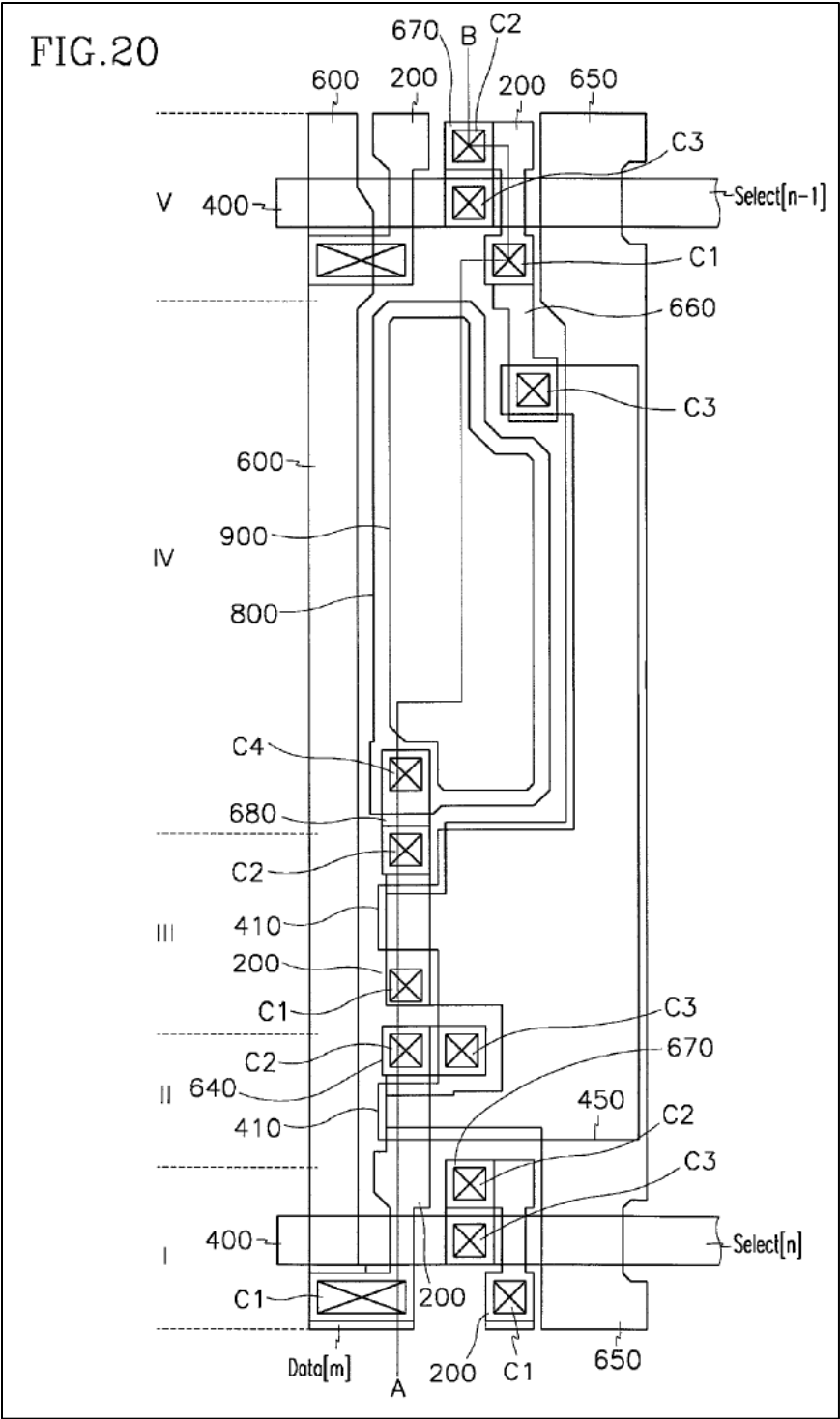
1. Summary of Kwon

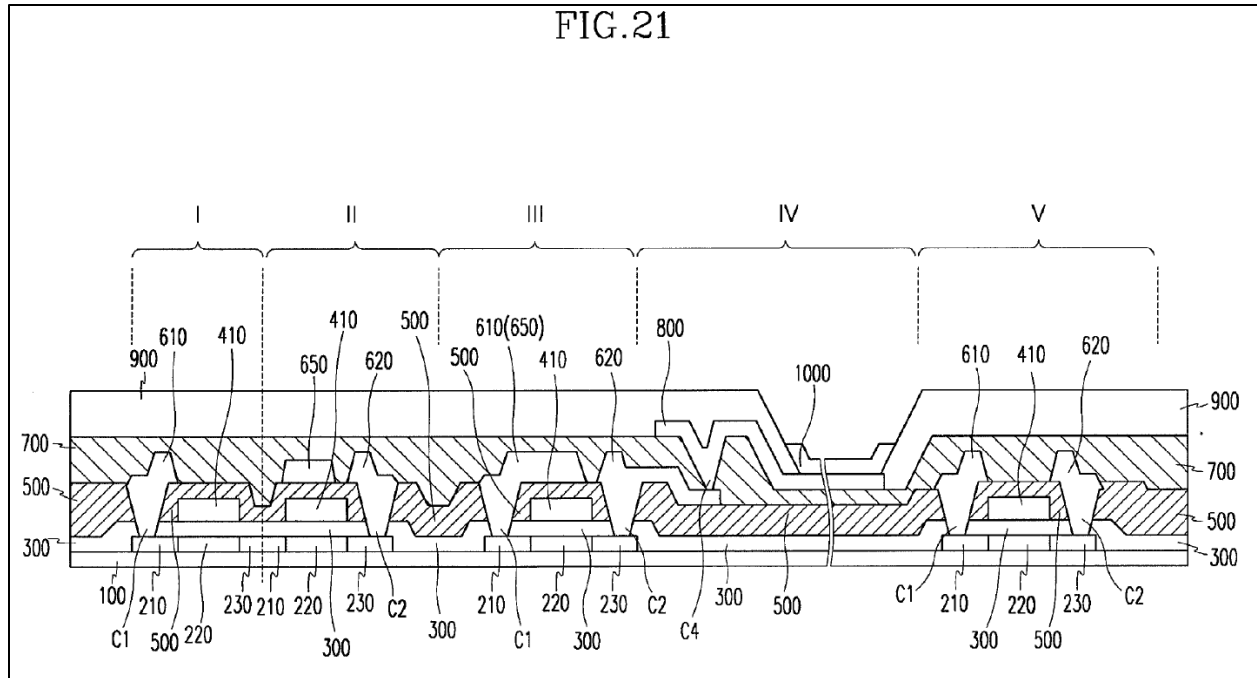
201. Kwon is directed to “an organic EL display (OELD), its driving methods and a pixel circuit that can compensate for deviation of the threshold

voltage of a thin film transistor (TFT) and achieve high gray scale display when driving the pixels of the OLED using the TFT.” (EX1006, [0002].) Kwon describes that “it is difficult for the conventional pixel circuit to achieve high gray scale because the threshold voltage V_{TH} of the TFT varies depending on the manufacturing process thereof.” (EX1006, [0011].) Kwon thereby “provide[s] an OLED for compensating for deviations of the threshold voltage of the TFT and displaying high gray scale.” (EX1006, [0012].)

202. Figure 7 (below) shows Kwon’s pixel circuit. Figures 20 and 21 (below) show plan and cross-sectional views of Kwon’s OLED.





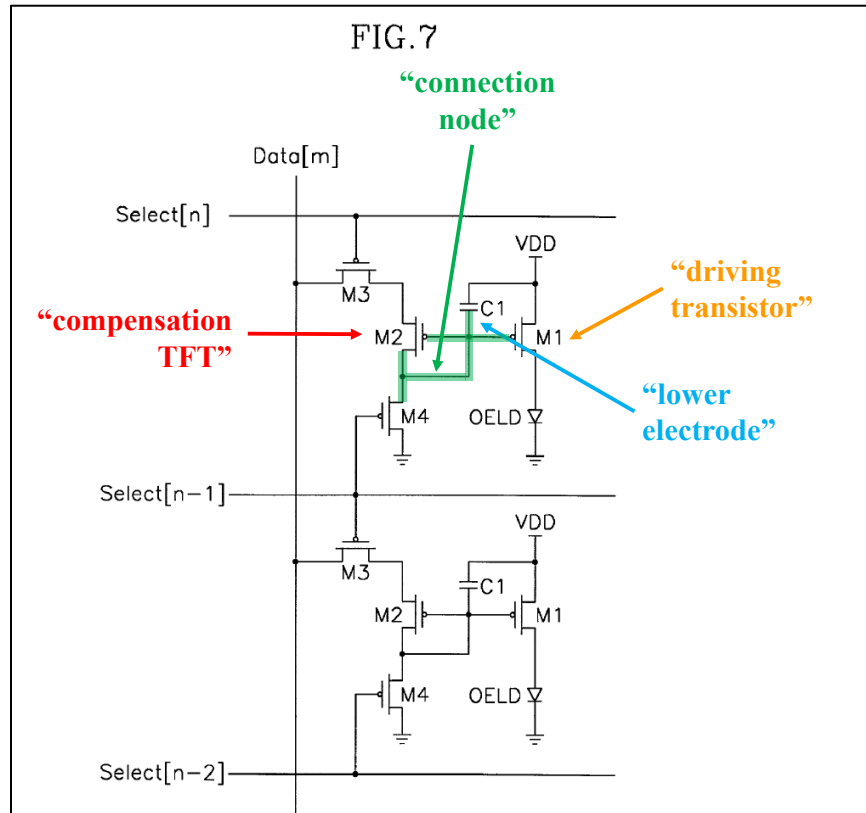


2. **Claim 6: “The TFT array substrate of claim 5, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”**

203. As shown for element 1[g], Park teaches a “connection node” that electrically couples a driving thin film transistor 5 to the lower electrode of a capacitor 6. As shown for element 1[c], Ishii100 teaches a “connection node” that electrically couples a TFT 30 to a lower electrode of a capacitor 70.

204. If, for some reason, neither Park nor Ishii100 teaches the claimed “compensation TFT,” Kwon teaches it. For example, Figure 7 (annotated below) of Kwon shows *transistor M2* coupled to *driving transistor M1* and electrically coupled to the *lower electrode* of capacitor C1 through the *connection node*.

Kwon discloses that “the transistor M2 compensates for deviations of the threshold voltage of the transistor M1 for supplying the current.” (EX1006, [0046].)



205. It would have been obvious to a POSITA to combine the teachings of Park and Ishii100 with Kwon. Park, Ishii100, and Kwon all disclose light emitting devices and pixel circuits for operating these light emitting devices. Park discloses “an active matrix organic electro luminescent display (ELD) device having thin film transistors.” (EX1005, [0017].) Ishii100 discloses an “electro-optical device” that can be applied to an organic EL display and a “liquid crystal device of a TFT active matrix drive system with a built-in drive circuit.” (EX1004, [0007], [0038], [0097].) Kwon discloses “an organic electroluminescent (EL) display, a driving

method of the EL display and a pixel circuit of the EL display.” (EX1006, [0002].)

Thus, Park, Ishii100, and Kwon are in the same field of endeavor.

206. Park, Ishii100, and Kwon teach similar pixel circuits. Park’s pixel circuit comprises “a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7.” (EX1005, [0006].)

Ishii100’s pixel circuit comprises “a pixel electrode 9a and a TFT 30 for controlling switching of the pixel electrode 9a are formed.” (EX1004, [0047].)

Kwon’s “pixel circuit compris[es] a current supplying transistor M1 and a threshold voltage compensation transistor M2 of PMOS transistors, and switches S1 and S2 of PMOS transistors M3 and M4.” (EX1006, [0056].)

207. Kwon explains that “it is difficult for the conventional pixel circuit to achieve high gray scale because the threshold voltage V of the TFT varies depending on the manufacturing process thereof.” (EX1006, [0011].) Like Kwon, Park’s teachings also apply to a conventional pixel circuit. (EX1005, Fig. 1 (“Related Art”).) Kwon then teaches a “pixel circuit that can compensate for deviation of the threshold voltage of a thin film transistor (TFT) and achieve high gray scale display when driving the pixels of the OLED by using the TFT.” (EX1006, [0002].) Kwon’s solution is to include an additional transistor M4 that resets the gate voltage of the driving transistor M1 and a threshold voltage compensation transistor M1 that achieves a high gray scale display. (EX1006,

[0056]-[0057].) These technical features of Kwon's pixel circuits may be combined with the teachings of Park and Ishii100 to generate a display device with high gray scale display by including circuitry in the pixel circuit to compensate for any deviations in the threshold voltage of the driving TFT. The combination of Park, Ishii100, and Kwon results in a display device with high gray scale display. There would have been a reasonable expectation of success because such techniques were known in the prior art and have been successfully demonstrated. Additionally, Park, Ishii100, and Kwon have several overlapping similarities including similar circuits used for active matrix display devices.

208. Because Park, Ishii100, and Kwon have similar circuits, a POSITA would have been motivated to use the technique disclosed in Kwon to improve the similar devices of Park and Ishii100 in the same way. Thus, it would have been obvious to a POSITA to combine Park, Ishii100, and Kwon.

3. Claim 7: “The TFT array substrate of claim 6, wherein a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.”

209. Kwon teaches “a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.” For example, Kwon discloses “a first capacitor electrode 450 is patterned on the same layer with the same material as the scan line 400. The gate electrodes 410 are respectively formed on the portions where the first capacitor electrode 450 is superimposed

with the polycrystal silicon layer 200 of the II and III regions.” (EX1006, [0093].)

It would have been obvious to combine Park, Ishii100, and Kwon. (*See* claim 6.)

4. Claim 8

- a. **8[a]: “The TFT array substrate of claim 5, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”**

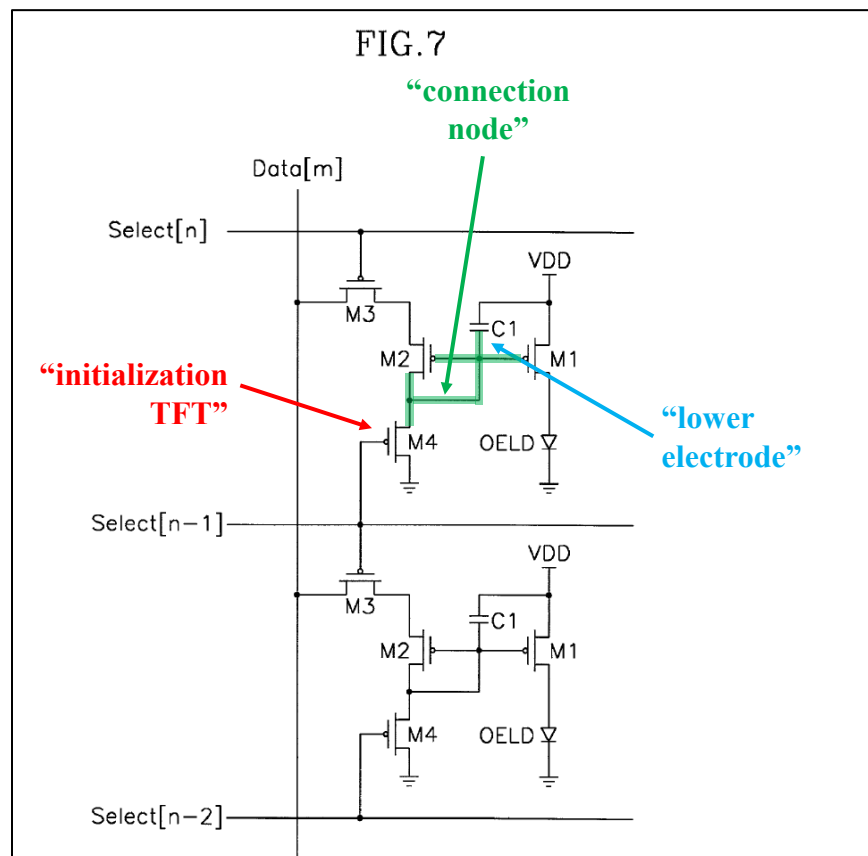
210. As shown for element 1[c], Park teaches a lower electrode of a capacitor 6 and a connection node, and similarly, Ishii100 teaches electrodes E1 and E3 (“lower electrode”) and a connection node. As shown for element 1[f], Park teaches driving thin film transistor 5 and a switching thin film transistor 4, and Ishii100 teaches TFT 30 (“at least one TFT”), and. Both Park and Ishii100 teach the connection node electrically coupling the lower electrode of the capacitor to at least one TFT.

211. If, for some reason, neither Park not Ishii100 teaches an “initialization TFT electrically coupled to the lower electrode through the connection node,” Kwon teaches it. For example, Figure 7 (annotated below) shows a **connection node** that electrically couples the **lower electrode** of capacitor C1 to **transistor M4**. Kwon discloses “an external reset signal reset is supplied to the gate of the transistor M4 to initialize the node A into a ground level.” (EX1006, [0060].) Thus, the transistor M4 is an initialization TFT because it resets (initializes) the

gate of transistor M1. Transistor M1 is a driving transistor: “the current that flows to the OLED via the current driving transistor M1 is expressed in Equation 3.”

(EX1006, [0060], [0050] (“the current flows to the OLED via the transistor M1 to emit light”).) Kwon also discloses “an additional reset signal Reset is supplied to a gate of the transistor M4 for resetting the gate voltage of the transistor M1.”

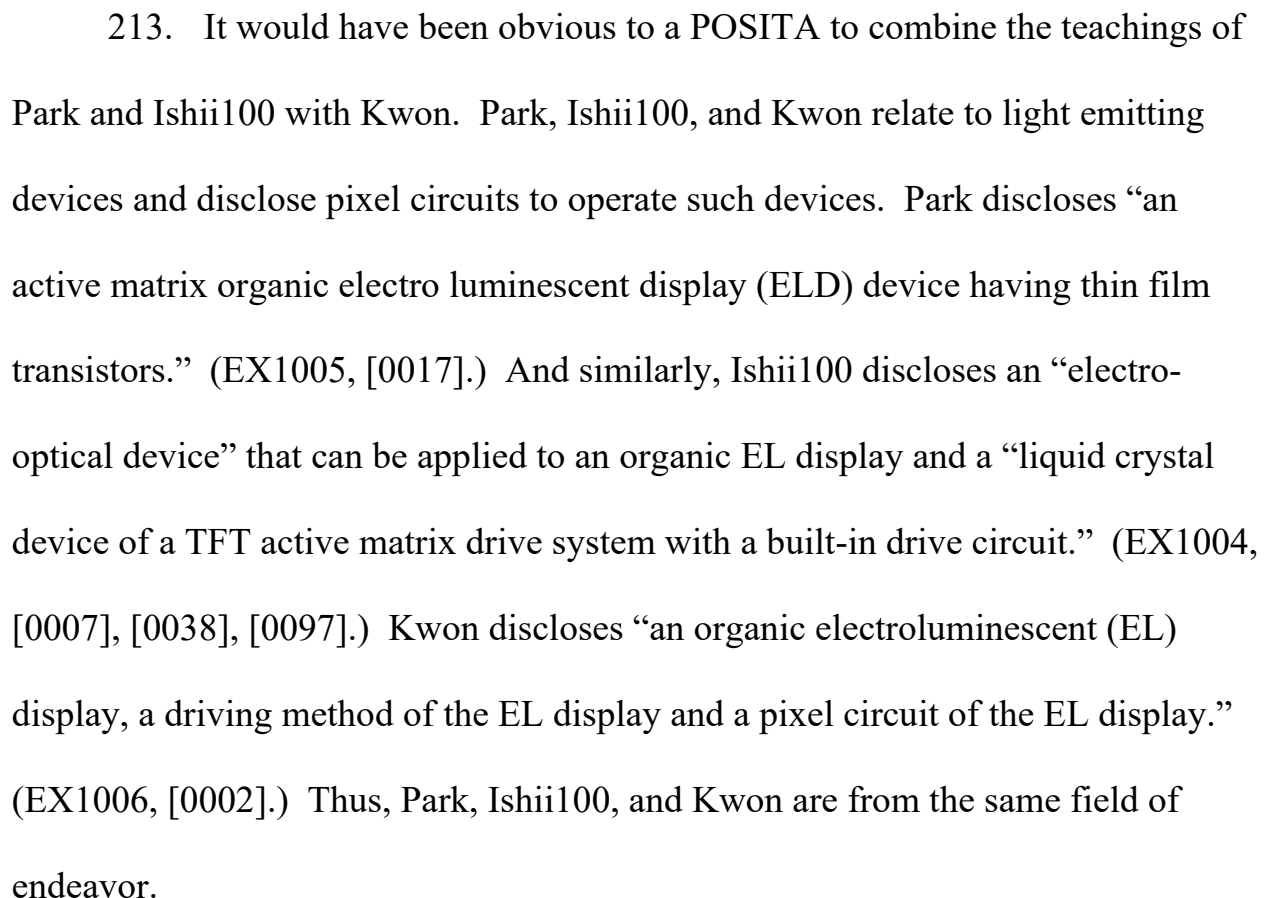
(EX1006, [0057].)



- b. **8[b]: “wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”**

212. As shown for element 8[a], Kwon teaches a transistor M4 (“initialization TFT”) and a current driving transistor M1 (“driving TFT”).

Kwon teaches “the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.” For example, Kwon discloses “an external reset signal Reset is supplied to the gate of the transistor M4 to initialize the node A into a ground level.” (EX1006, [0060].) Figure 7 (annotated below) shows the *transistor M4* is configured to provide a “ground level” voltage to the gate of *transistor M1*. The pixel circuit of Figure 7 “uses the Select Signal Select[n-1] of the previous Scan line instead of an additional external reset Signal Reset, and Supplies the select signal Select[n-1] to the gate of the transistor M4.” (EX1006, [0063].) This means, as shown in the figure, that the gate of transistor M4 is coupled to the previous Select[n-1] line, thereby transistor M4 is turned on in response to previous *Select[n-1] line*. Thus, Kwon teaches element 8[b].



214. Park's pixel circuit comprises "a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7." (EX1005, [0006].) Ishii100's pixel circuit comprises "a pixel electrode 9a and a TFT 30 for controlling switching of the pixel electrode 9a are formed." (EX1004, [0047].) Kwon similarly discloses a "pixel circuit compris[ing] a current supplying transistor M1 and a threshold voltage compensation transistor M2 of PMOS transistors, and switches S1 and S2 of PMOS transistors M3 and M4." (EX1006, [0056].)

215. Kwon explains that "it is difficult for the conventional pixel circuit to achieve high gray scale because the threshold voltage V of the TFT varies depending on the manufacturing process thereof." (EX1006, [0011].) Kwon teaches "pixel circuit that can compensate for deviation of the threshold voltage of a thin film transistor (TFT) and achieve high gray scale display when driving the pixels of the OLED by using the TFT." (EX1006, [0002].) These technical features may be combined with the teachings of Park and Ishii100 to generate a display device with high gray scale display by including circuitry in the pixel circuit to compensate for any deviations in the threshold voltage of the driving TFT. There would have been a reasonable expectation of success because such techniques were known in the prior art and have been successfully demonstrated,

and further given that the circuits of Park, Ishii100, and Kwon are similar and used for active matrix display devices.

216. A POSITA would have been motivated to use the technique disclosed in Kwon to improve the similar devices of Park and Ishii100 in the same way. A POSITA would have been motivated to apply Kwon's teachings of including a transistor M4 to initialize the gate of the current driving transistor (e.g., driving thin film transistor 5 of Park or TFT 30 of Ishii100) because doing so would improve the gray scale display and there would have been a reasonable expectation of success.

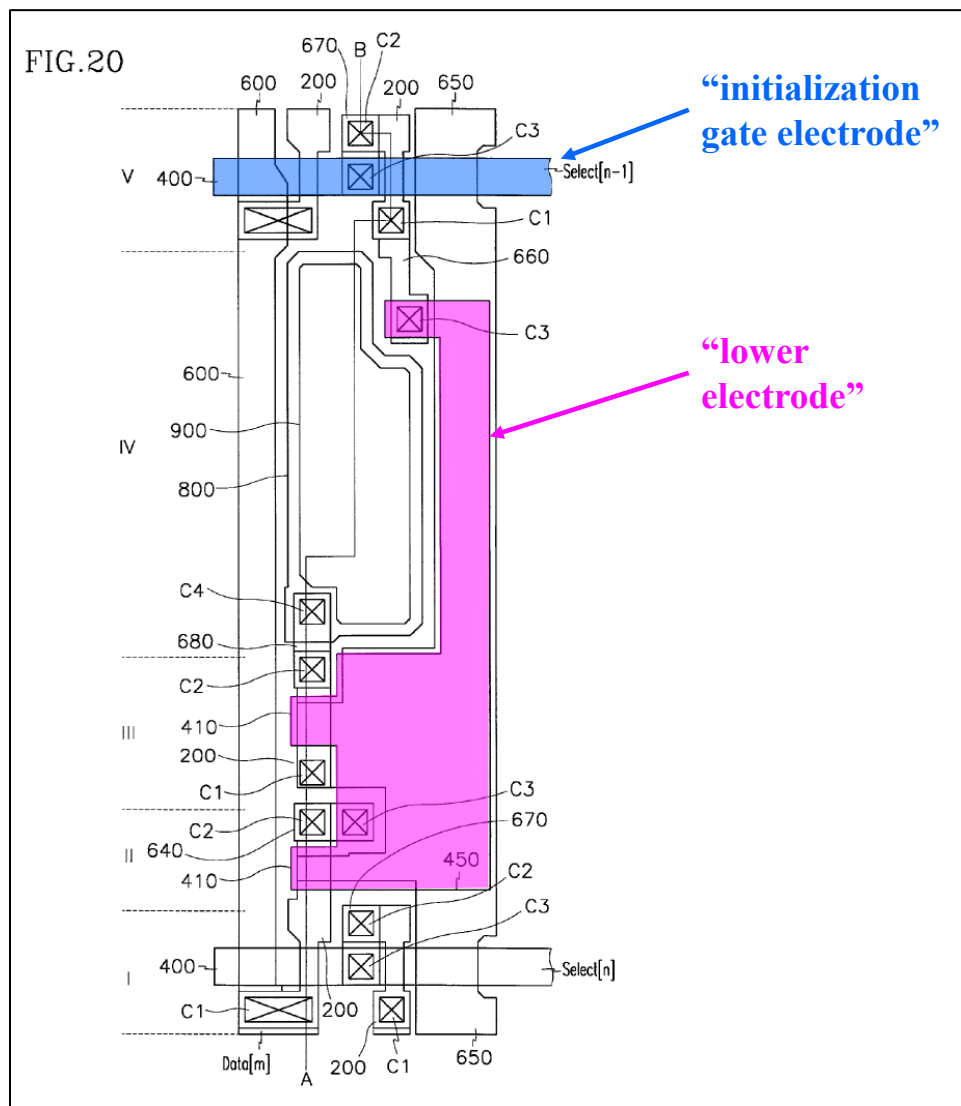
5. Claim 9: "The TFT array substrate of claim 8, wherein an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode."

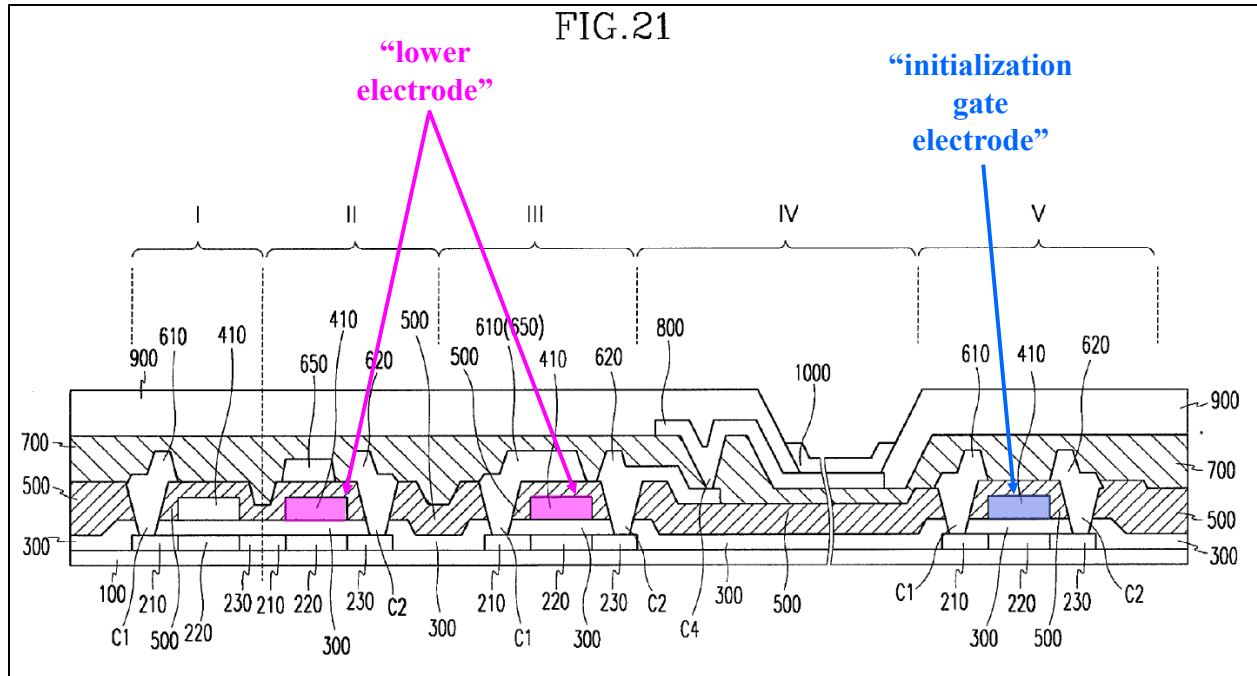
217. As shown for element 8[a], Kwon teaches a transistor M4 ("initialization TFT") and a capacitor C1 having a lower electrode.

218. Kwon teaches "an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode." For example, Kwon discloses "[a] scan line 400 of Al and Cr is patterned in the horizontal direction on the gate insulation layer 300 to be crossed with the polycrystalline silicon layer 200. *Gate electrodes 410 are respectively formed on portions where the scan lines 400* are superimposed with the polycrystalline silicon layer 200 in the I and V regions. Also, a *first capacitor electrode 450 is patterned on the same layer with*

the same material as the scan line 400. The gate electrodes 410 are respectively formed on the portions where the first capacitor electrode 450 is superimposed with the polycrystal silicon layer 200 of the II and III regions.” (EX1006, [0093] (emphases added).) Figures 20 and 21 (annotated below) show the *gate of the transistor M4 (400)* is formed on the same layer as the *capacitor electrode 450*.

Thus, Kwon teaches claim 9.





6. **Claim 15:** “The OLED display of claim 14, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”

219. Park and/or Ishii100 teach claim 14 as shown above Section IX.C.9.

Claim 15 is similar to claim 6, which Kwon teaches. (See claim 6.) The table below shows the similarities.

Claim 6	Claim 15
“The TFT array substrate of claim 5, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”	“The OLED display of claim 14, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”

7. Claim 16: “The OLED display of claim 15, wherein a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.”

220. Park and/or Ishii teach claim 15 as shown above in Section IX.D.6.

221. Claim 16 is similar to claim 7, which Kwon teaches. (*See* claim 7.)

The table below shows the similarities.

Claim 7	Claim 16
“The TFT array substrate of claim 6, wherein a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.”	“The OLED display of claim 15, wherein a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.”

8. Claim 17

a. 17[a]: “The OLED display of claim 14, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”

222. Park and/or Ishii¹⁰⁰ teach claim 14 as shown above in

Section IX.C.9.

223. Element 17[a] is similar to element 8[a], which Ishii100, Park, and/or Kwon teaches. (See IX.D.4.a.) The table below shows the similarities.

Element 8[a]	Element 17[a]
“The TFT array substrate of claim 5, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”	“The OLED display of claim 14, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”

- b. **17[b]: “wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”**

224. Element 17[b] is similar to element 8[b], which Ishii100, Park, and/or Kwon teaches. (See IX.D.4.b.) The table below shows the similarities.

Element 8[b]	Element 17[b]
“wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”	“wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”

9. **Claim 18: “The OLED display of claim 17, wherein an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode.”**

225. Kwon teaches claim 17 as shown above in Section IX.D.6.

226. Claim 18 is similar to claim 9, which Kwon teaches. (See IX.D.5.)

The table below shows the similarities.

Claim 9	Claim 18
“The TFT array substrate of claim 8, wherein an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode.”	: “The OLED display of claim 17, wherein an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode.”

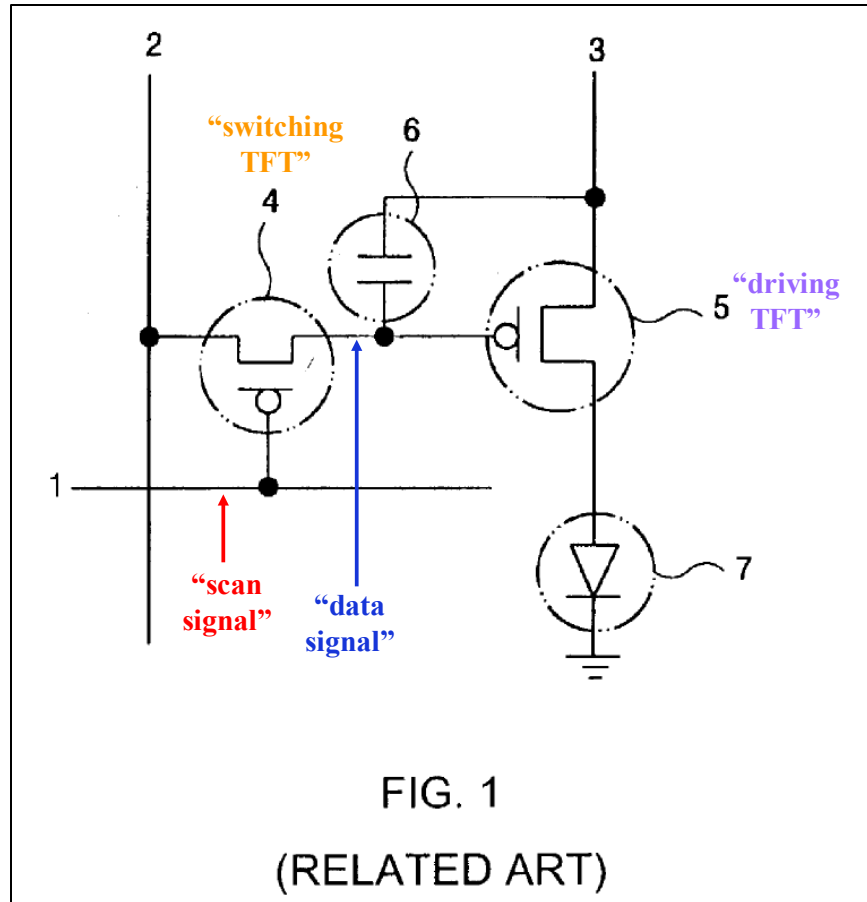
10. Claim 19: “The OLED display of claim 14, further comprising a switching TFT for delivering the data signal to the driving TFT by being turned on by the scan signal.”

227. Park and/or Ishii100 teach claim 14 as shown above in

Section IX.C.9.

228. As shown for element 5[g], Park teaches a driving TFT 5 (“driving TFT”). As shown for element 10[c], Park teaches a gate line 1 (“scan signal”).

229. Park teaches “a switching TFT for delivering the data signal to the driving TFT by being turned on by the scan signal.” For example, Park discloses “[i]f a signal is applied to the gate line 1, the switching thin film transistor 4 is turned on. If a signal of the data line 2 is applied to the gate electrode of the driving thin film transistor 5, the driving thin film transistor 5 is turned on and thus the light emitting diode (LED) 7 emits light.” (EX1005, [0006].) Figure 1 (annotated below) showing a *switching thin film transistor 4* for delivering the *signal of the data line 2* to the *driving thin film transistor 5* by being turned on by the *signal of the gate line 1*.



E. Claims 1-6, 8, And 10-19 Are Obvious Over Liu and Ono

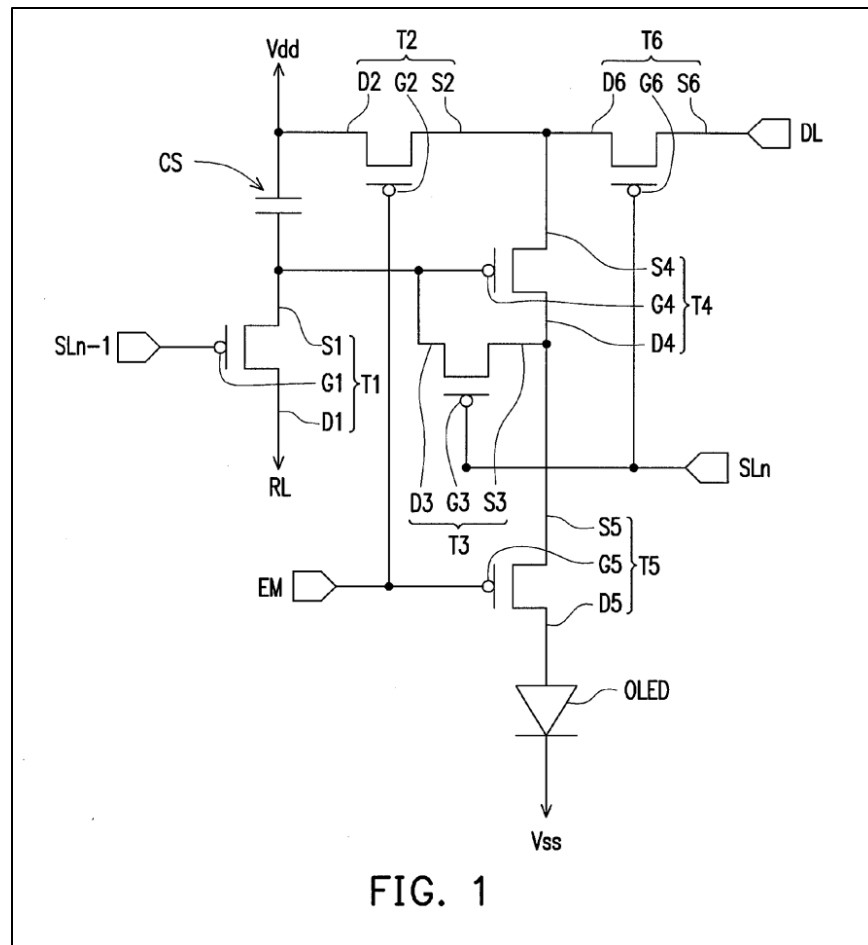
1. Summary of Liu

230. Liu “relates to a semiconductor device,” and specifically the pixel structure of the semiconductor device. (EX1007, [0003].) Liu teaches that “the pixel structure is applied to an organic electro luminescence display device and has a structure comprising six thin film transistors and one capacitor.” (EX1007, [0032].)

231. Liu acknowledges that the “pixel structure of the organic light emitting device in the display is usually driven by the cooperation of a plurality of

thin film transistors (TFTs) and a capacitor.” (EX1007, [0006].) The plurality of TFTs occupies much of the area in a pixel structure, leaving “no extra space for disposing other components.” (*Id.*) Additionally, “the pixel circuit structure can not be miniaturized easily and thus can not be applied in displays with high resolution.” (*Id.*)

232. Liu discloses a pixel structure therefore that is “capable of reducing an area occupied by components of the pixel structure.” (EX1007, [0007].) Figure 1 (shown below) is “a schematic circuit diagram of a pixel structure according to an embodiment of the invention.” (EX1007, [0013].) “[T]he pixel structure is applied to an organic electroluminescence display and has a structure comprising six thin film transistors and one capacitor.” (EX1007, [0032].)



233. Figure 8 (shown below) is a top view of Figure 1, while Figure 10 (shown below) is a cross section of a portion of Figure 1. Liu notes that “the cross-sectional diagram of FIG.10 is a cross-sectional view for the fifth thin film transistor in the 6T1C pixel structure. Since the six thin film transistors in the 6T1C pixel structure are substantially similar, the people skilled in the art may understand the cross-sectional structures of other five thin film transistors in accordance with the description for the fifth thin film transistor shown in FIG. 10.” (EX1007, [0058].)

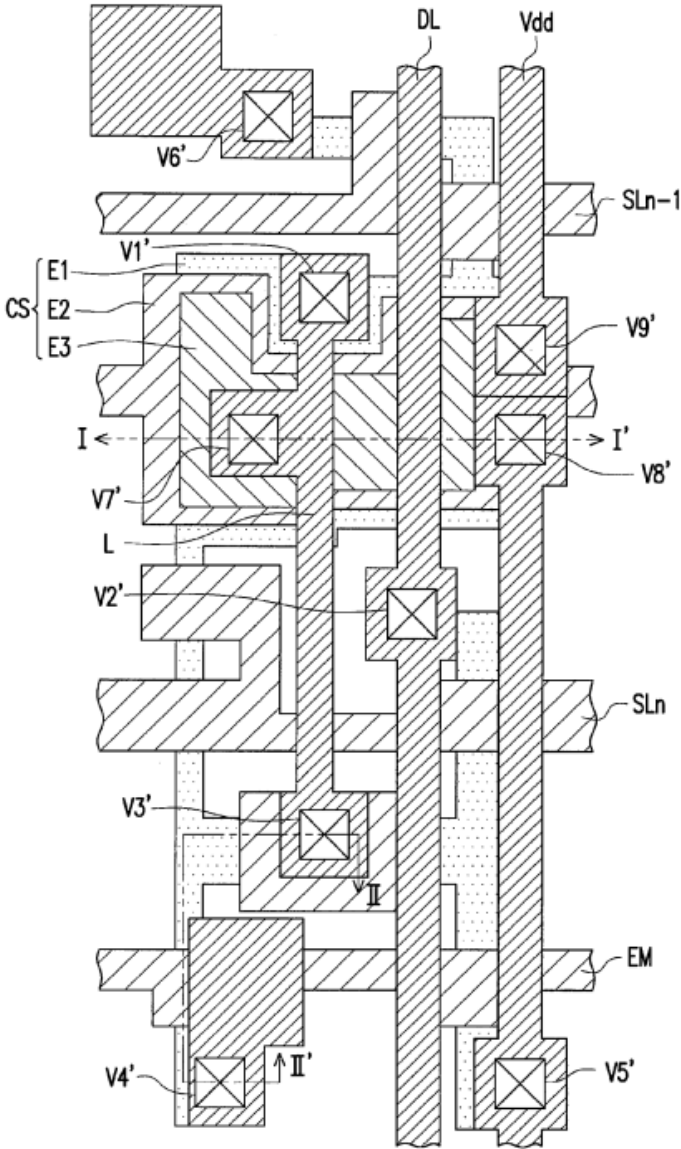


FIG. 8

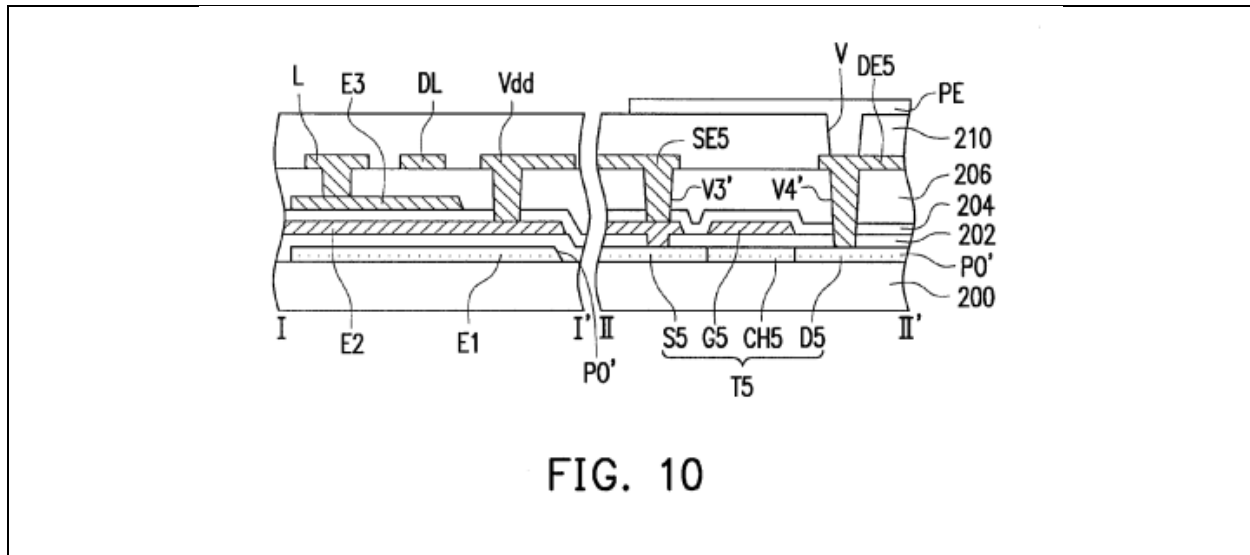


FIG. 10

2. Summary of Ono

234. Ono “relates to luminescent display devices, and particularly to an active-matrix luminescent display device which includes a luminescent element and a driving circuit having a capacitor and a thin-film transistor.” (EX1008, [0003].) Ono teaches that “the luminescent element may be an organic electroluminescent element.” (EX1008, [0046].)

235. Ono states that conventional active-matrix luminescent display devices arrange pixel circuits to include, “for each luminescent element, a driving circuit for driving the luminescent element.” (EX1008, [0005].) Ono explains: “[t]he driving circuit generally includes: a switching transistor which selects a pixel for producing luminescence; a driving transistor which drives a luminescent element; and a capacitor. The driving circuit includes, for example, a capacitor

which holds a voltage for determining an amount of current passed by the driving transistor.” (EX1008, [0006].)

236. Ono recognizes, however, that this arrangement results in less design flexibility because it dedicates a region to the capacitor. (EX1008, [0008].)

Therefore, “when the number of capacitors or the capacitor area increases, the region for forming other elements becomes smaller.” (*Id.*) Accordingly, Ono discloses “a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor.” (EX1008, [0010].) Ono teaches forming an electrode of the capacitor in a region above the driving transistor, such as the gate electrode of the driving transistor for different pixel circuits. (EX1008, [0050], [0070], Fig. 3, Fig. 4, [0091], Fig. 6, Fig. 7, [0113], Fig. 8, Fig. 9, [0124], Figs. 10-12.)

3. Claim 1

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

237. Liu discloses “[a] thin film transistor (TFT) array substrate.” For example, Liu teaches the pixel structure of a semiconductor device includes “at least one thin film transistor.” (EX1007, [0008]-[0009].)

238. Referring to Figure 1, Liu teaches that “the pixel structure is applied to an organic electroluminescence display and has a structure comprising six thin

film transistors” (EX1007, [0032].) Liu discloses “the pixel structure is disposed on a substrate 200.” (EX1007, [0058].)

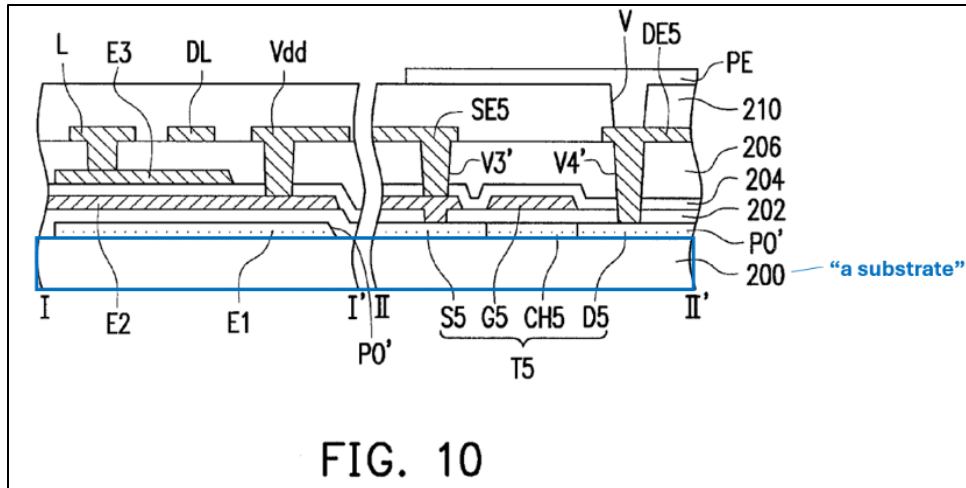
239. Liu further provides additional disclosures that show that it teaches “a thin film transistor (TFT) array substrate:”

- “A pixel structure, comprising: . . . at least one thin film transistor.” (EX1007, cls. 1, 5.)
- “The pixel structure as claimed in claim 1, wherein the at least one thin film transistor comprises six thin film transistors.” (EX1007, cl. 4; *see also* EX1007, cl. 8 (“The pixel structure as claimed in claim 5, wherein the at least one thin film transistor comprises six thin film transistors.”).)

240.

b. 1[a]: “a substrate;”

241. Liu teaches “a substrate.” For example, Liu discloses “the pixel structure is disposed on a substrate 100.” (EX1007, [0032].) As another example, referring to Figure 10 (annotated below), Liu discloses “the pixel structure is disposed on a substrate 200.” (EX[Liu]), [0058].)

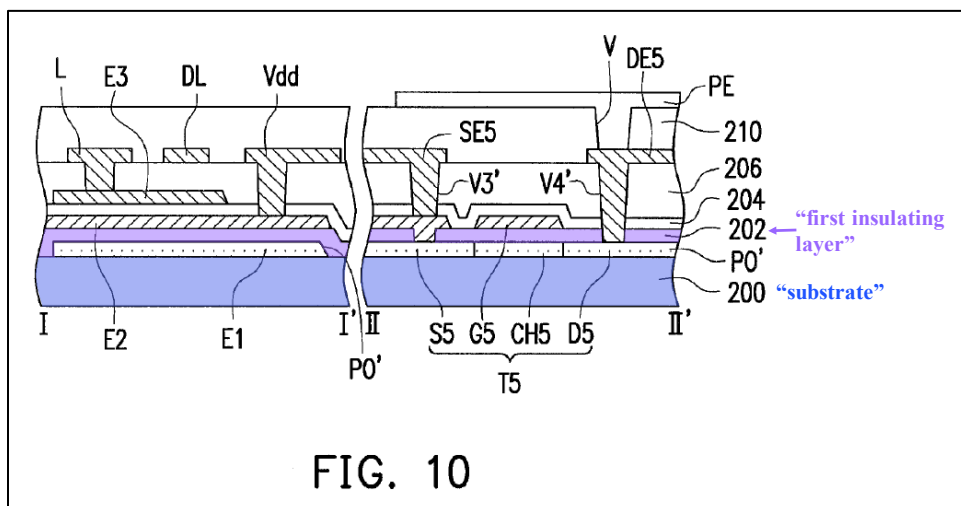


c. 1[b]: “a first insulation layer on the substrate;”

242. As shown for element 1[a], Liu teaches substrate 200 (“substrate”).

243. Liu teaches “a first insulation layer on the substrate.” For example, Liu discloses “[t]he first insulating layer 202 covers the semiconductor layer PO' and has a material similar to or the same with the material of the first insulating layer 102 as described in the first embodiment.” (EX1007, [0062].)

244. Figure 10 (annotated below) shows *insulating layer 202* on the *substrate 200*.

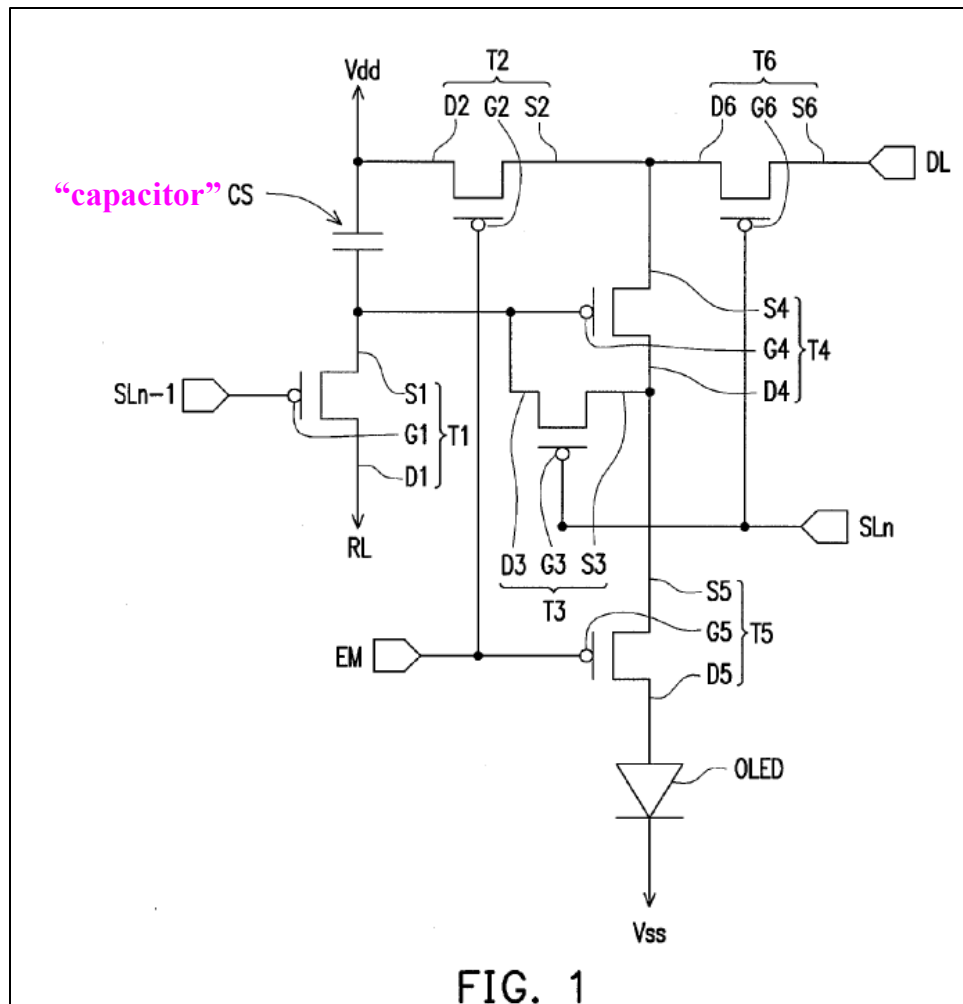


- d. **1[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”**

(i) **Liu**

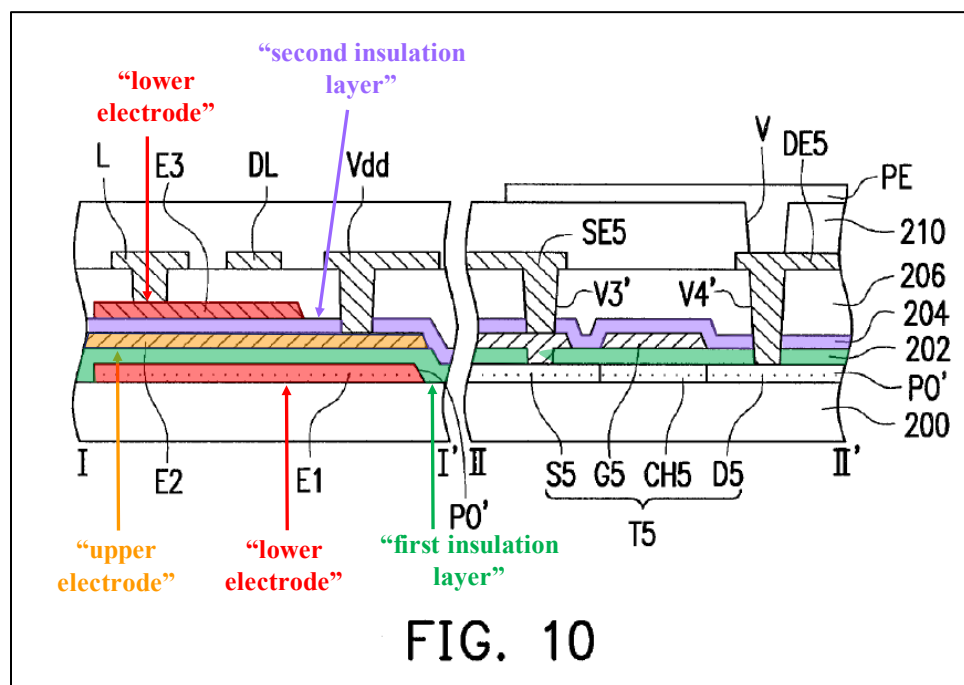
245. As shown for element 1[b], Liu teaches insulating layer 202 (“first insulation layer”).

246. Liu teaches “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode . . . , wherein the upper electrode is insulated from the lower electrode by a second insulation layer.” For example, Liu discloses “the layout of the semiconductor layer PO' is shown in FIG.9A, and the semiconductor layer PO' mainly comprises channel regions, source regions and drain regions of the six thin film transistors and a first electrode E1 of a *capacitor*.” (EX1007, [0060] (emphasis added).) Liu also discloses that “the layout of the first conductive layer M1' is shown in FIG.9B, which mainly comprises gates of the six thin film transistors and a *second electrode E2 of the capacitor CS*.” (EX1007, [0063] (emphasis added).) Figure 1 (annotated below) shows *capacitor CS*.



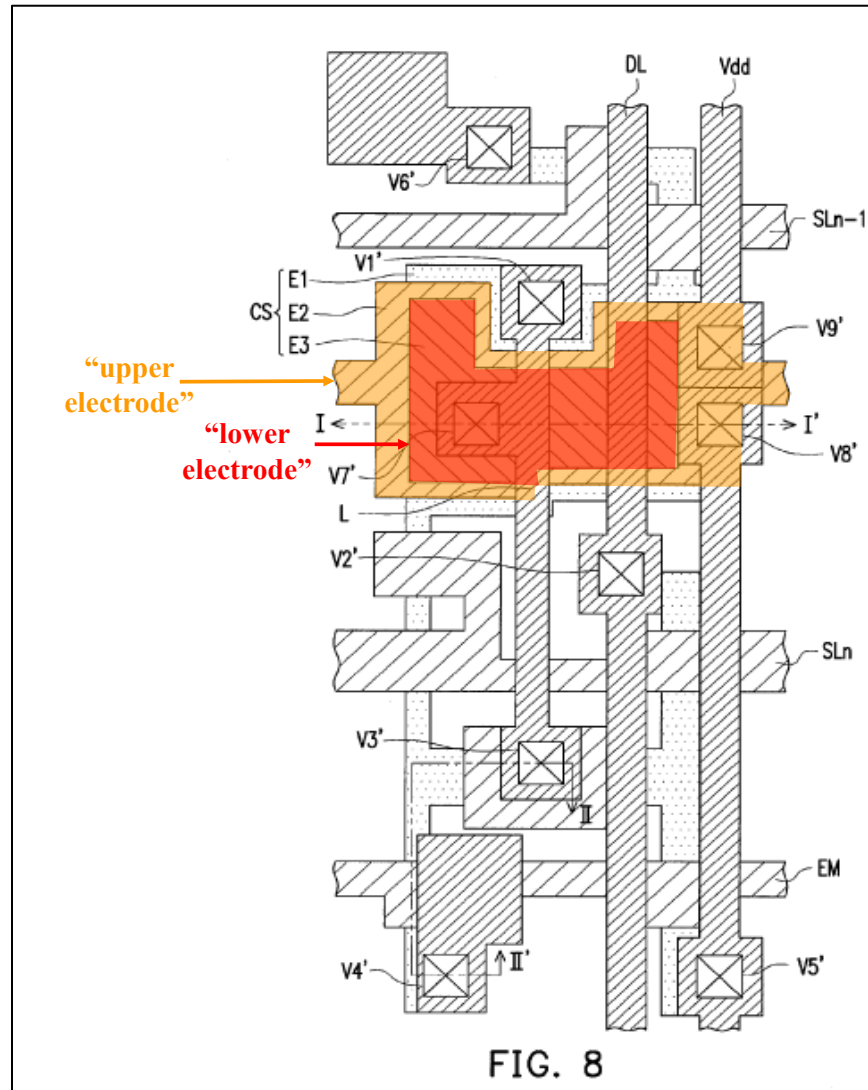
247. Liu discloses that “the layout of the second conductive layer M2 is shown in FIG. 9C, which mainly comprises a *third electrode E3 of the capacitor CS, and the third electrode E3 is disposed above the second electrode E2* of the first conductive layer M1’, as shown in FIG. 10. Hence, “the capacitor CS is formed with the first electrode E1 of the semiconductor layer PO’, the second electrode E2 of the first conductive layer M1’ and the third electrode E3 of the second conductive layer M2’, and the first insulating layer 202 between the first electrode E1 of the semiconductor layer PO’ and the second electrode E2 of the

first conductive layer M1' and the second insulating layer 204 between the second electrode E2 of the first conductive layer M1' and the third electrode E3 of the second conductive layer M2' serve as capacitor dielectric layers of the capacitor CS." (EX1007, [0066] (emphases added).) Figure 10 (annotated below) shows *electrode E3* on *insulating layer 202*. The figure also shows *electrode E3* insulated from *electrode E2* by *insulating layer 204*.



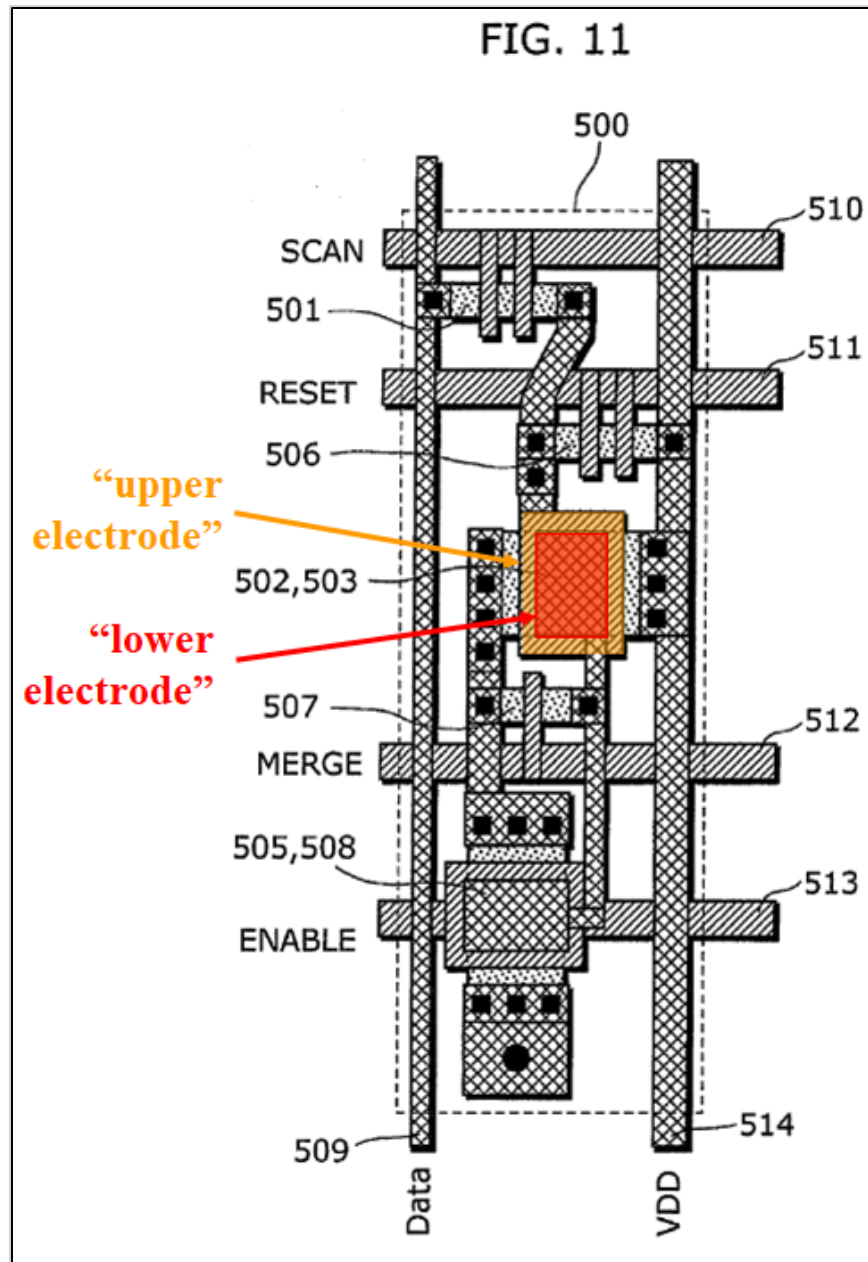
248. Liu teaches "an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening." For example, Figures 8 and 10 (annotated below) show *electrode E2* arranged to overlap with the whole *electrodes E1 and E3*. Figure 10 (annotated above) shows electrode E2 extending beyond an edge of

electrodes E1 and E3. Liu's M2' layer (Figure 9C) has a large region that is not occupied.





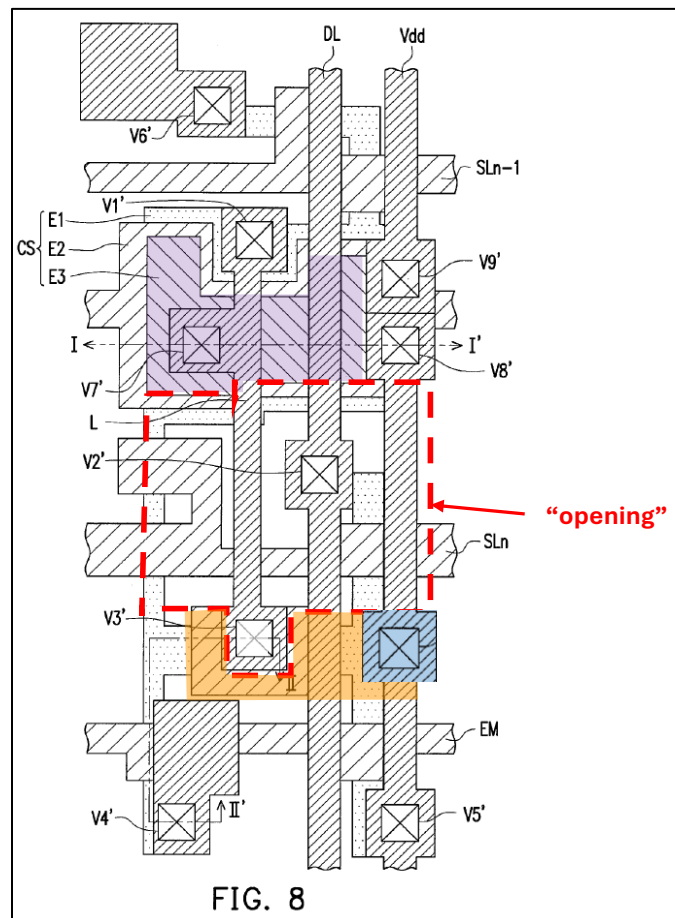
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250. Liu discloses Figure 9C “is a top view showing a second conductive layer of the pixel structure in FIG. 8” and “mainly comprises a third electrode E3 of the capacitor CS.” (EX1007, [0057], [0066].)

251. It would have been obvious to combine Liu and Ono to extend Liu’s upper electrode E2 to a space above the gate of the driving transistor T4. Modified

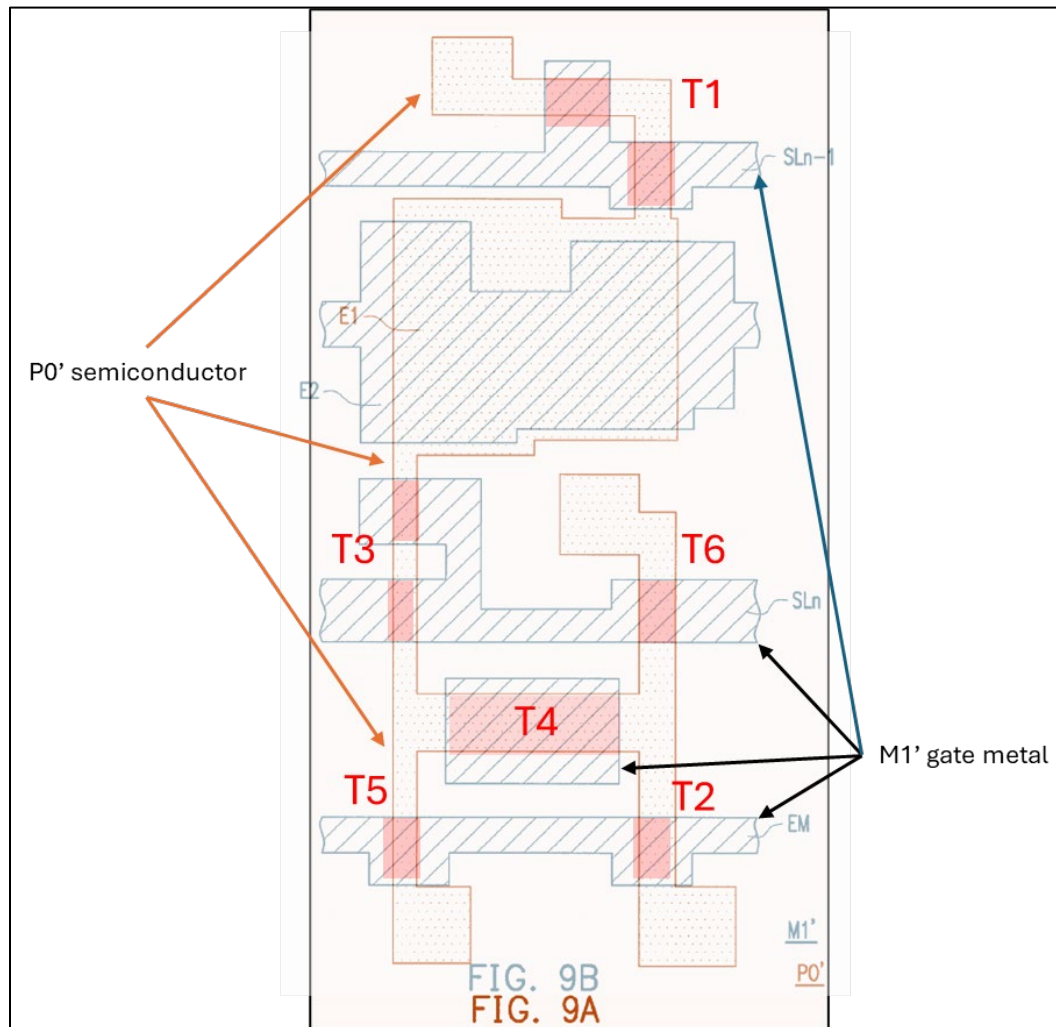
Figure 8 (annotated below) shows the extended *upper electrode (yellow portion)* according to the combination of Liu and Ono and an *opening*. It would have been obvious to a POSITA to include an opening in the electrode of a capacitor. Liu discloses “the layout of the first conductive layer M1' is shown in FIG.9B, which mainly comprises gates of the six thin film transistors.” (EX1007, [0063].) Liu explains that “the first conductive layer M1' has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007, [0064].) The gate of transistor T4 is formed with the first conductive layer M1'.



252. Liu teaches “the first metal pattern includes an opening, and a portion of the connection member overlaps the opening in a plan view.” For example, Figures 9A, 9B, 9C, and 9D (annotated below) show top views of layers PO, M1', and M2', and M3' of Figure 8.



253. A composite of Figures 9A and 9B show the locations of transistors T1 through T6 (see also Fig. 1). Both transistors T1 and T3 have two channels in series.



254. Layer M2' (Figure 9C) “mainly comprises a third electrode E3 of the capacitor CS.” (EX1007, [0057], [0066].) Liu explains that “the first conductive layer M1' has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007, [0064].) The location of T4 is indicated (below) by

red arrows and is located where indicated M1' metal gate crosses the PO' semiconductor layer.

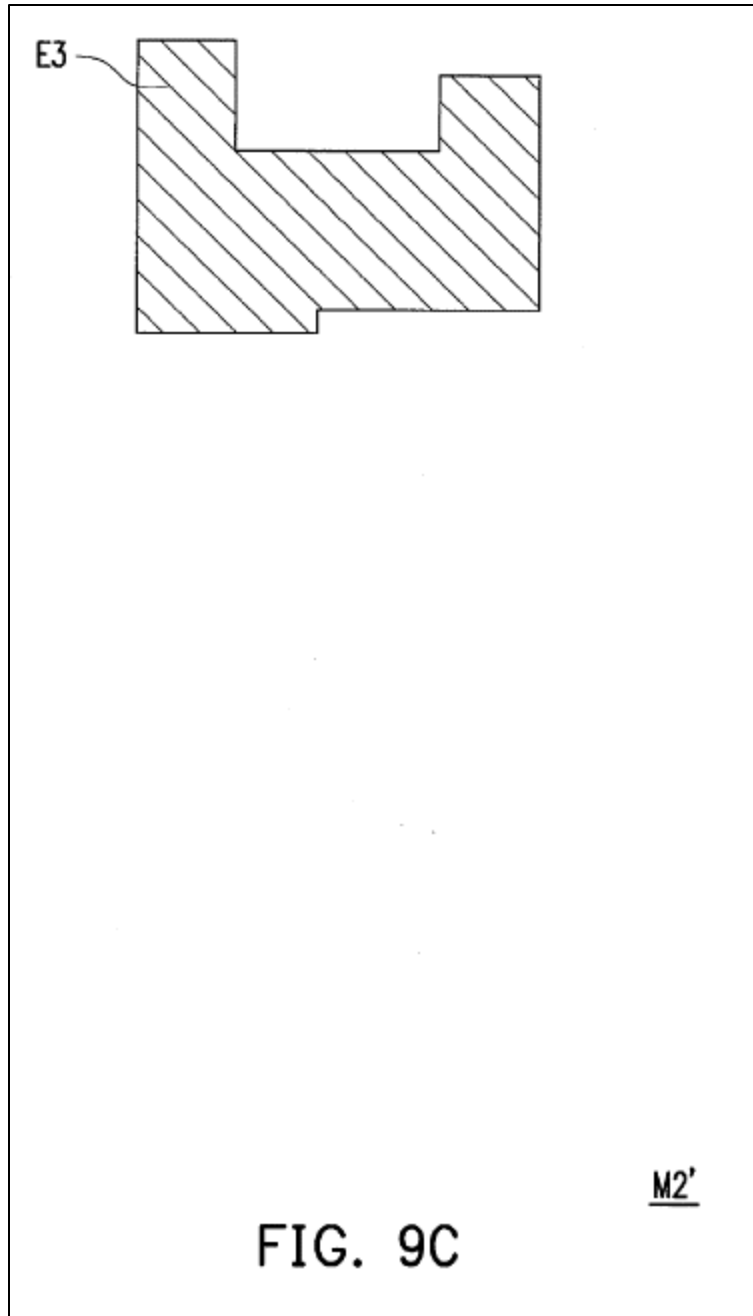
(iii) Motivation to combine Liu And Ono

255. It would have been obvious to a POSITA at the time of the '730 patent to combine the teachings of Liu and Ono. Liu and Ono both teach OLED devices with an array of thin film transistors that efficiently use the spaces in the device's pixel structure without compromising performance to promote the miniaturization of the organic light emitting devices. Liu discloses a pixel structure of an OLED device that is "capable of reducing an area occupied by components of the pixel structure." (EX1007, [0007].) Ono discloses "a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor." (EX1008, [0030].) Thus, Liu and Ono are from the same field of endeavor and reasonably pertinent to the same technical problem of decreasing the area of the pixel structure and increasing the capacitance of the storage capacitor in OLED devices.

256. Ono teaches "the gate electrode of the thin-film transistor is used not only simply as the gate electrode but also as one of two electrodes constituting the capacitor." (EX1008, [0029].) "Thus, the capacitor can be formed above the thin-film transistor to overlap with the thin-film transistor, enabling efficient use of the

pixel space.” (*Id.*) Ono aims to solve the problem “that when the number of capacitors or the capacitor area increases, the region for forming other elements becomes smaller, resulting in less design flexibility.” (EX1008, [0008].) Ono’s technical features can be combined with the teachings of Liu with a reasonable expectation of success to generate a smaller light-emitting device where the storage capacitor has an increased capacitor area but without decreasing the device’s quality.

257. Figure 9C (below) of Liu shows that its M2’ layer has a large amount of unused space above the gate of the driving transistor T4. The unoccupied space makes it easy to extend the upper electrode of the capacitor. A POSITA would have been motivated to extend Liu’s M2’ layer in the space above the gate of the transistor T4, as taught by Ono and other prior art (*e.g.*, EX1018, [0011], [0019]) to increase the capacitance without occupying any additional area. Because no extra layers are added and the space is unoccupied, a POSITA would have had a reasonable expectation of success combining the two references.



258. It would have been obvious to combine Liu and Ono. Liu and Ono both relate to semiconductor configurations that efficiently use pixel space within OLED devices. A POSITA would be motivated to use the techniques disclosed in Ono to improve the similar device of Liu in the same way. Ono teaches placing a

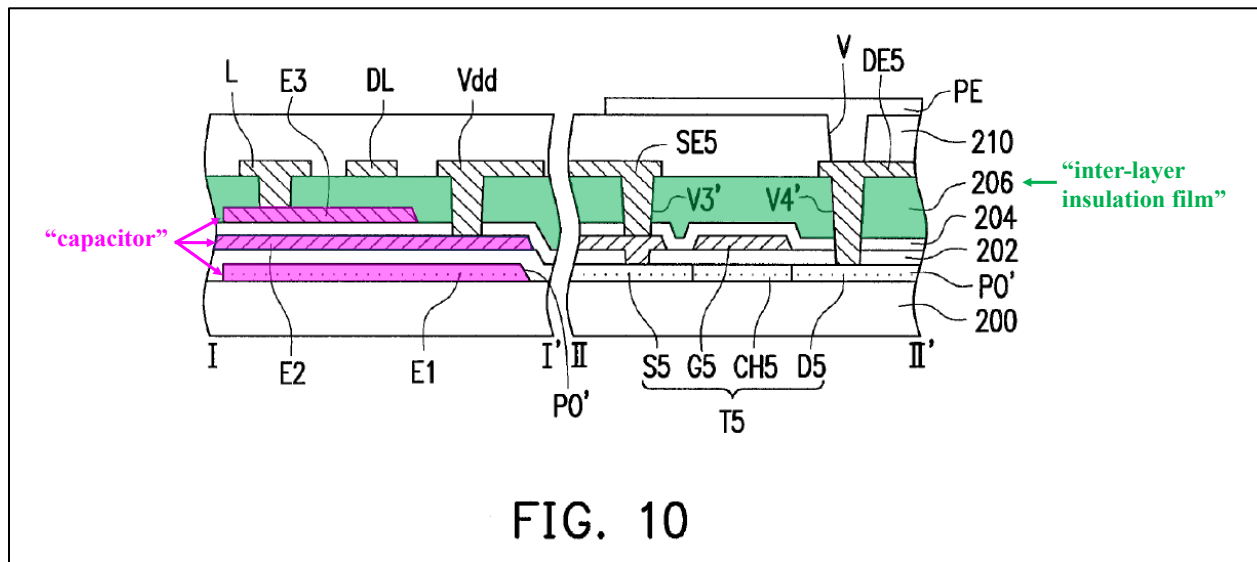
capacitor over a gate electrode, which was known in the art. Ono's technique increases the capacitance of the pixel structure, improving the display performance without using additional area. Prior art such as Ono successfully demonstrated an OLED device configuration that shrinks the size of the components within a pixel structure without compromising performance. There would have been a reasonable expectation of success for combining Liu and Ono by modifying the configuration of the capacitor and gate electrode in Liu.

e. 1[d]: “an inter-layer insulation film covering the capacitor;”

259. As shown for element 1[c], Liu teaches capacitor CS (“capacitor”).

260. Liu-Ono teaches “an inter-layer insulation film covering the capacitor.” For example, Liu discloses “[t]he *third insulating layer 206 covers the second conductive layer M2'* and has a material similar to or the same with the material of the third insulating layer 106 as described in the first embodiment.” (EX1007, [0067] (emphasis added).) Liu also discloses “the second insulating layer 204 between the second electrode E2 of the first conductive layer M1" and the third *electrode E3 of the second conductive layer M2'* serve as capacitor dielectric layers of the *capacitor CS.*” (EX1007, [0066] (emphases added).) As discussed for element 1[c], it would have been obvious to extend the upper electrode of Liu to include an electrode above the transistor T4 according to the teachings of Ono. Figure 10 (annotated below) shows *insulating layer 206*

covering **capacitor CS**. Although the figure shows a cross-section of Liu's device, a POSITA would have understood that the Liu-Ono combination would also have an insulating layer 206 covering the capacitor of the Liu-Ono combination because the modification extends the upper electrode E2, which is under the insulating layer 206.



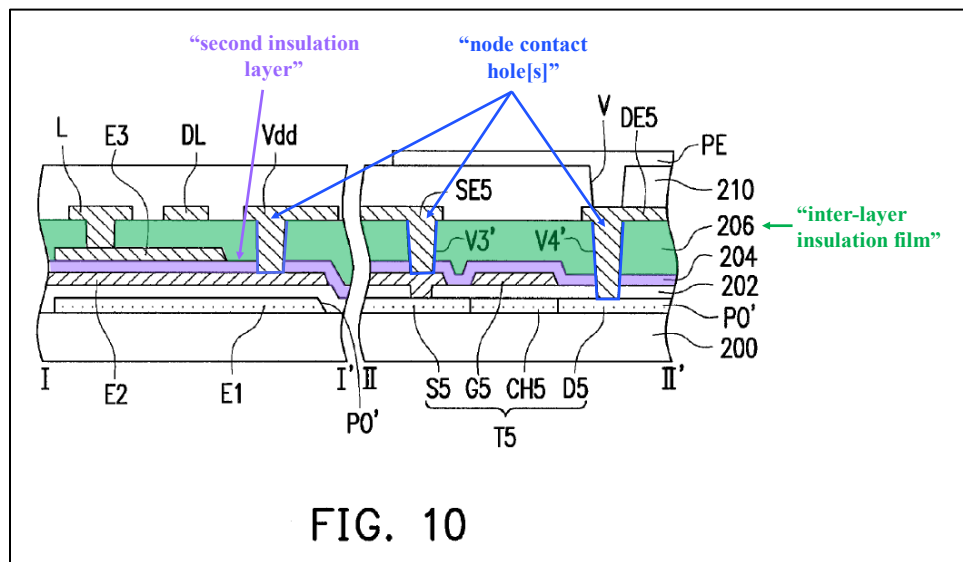
f. 1[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

261. As shown for element 1[d], Liu teaches an insulating layer 206 (“inter-layer insulation film”). As shown for element 1[c], Liu teaches an insulating layer 204 (“second insulation layer”)

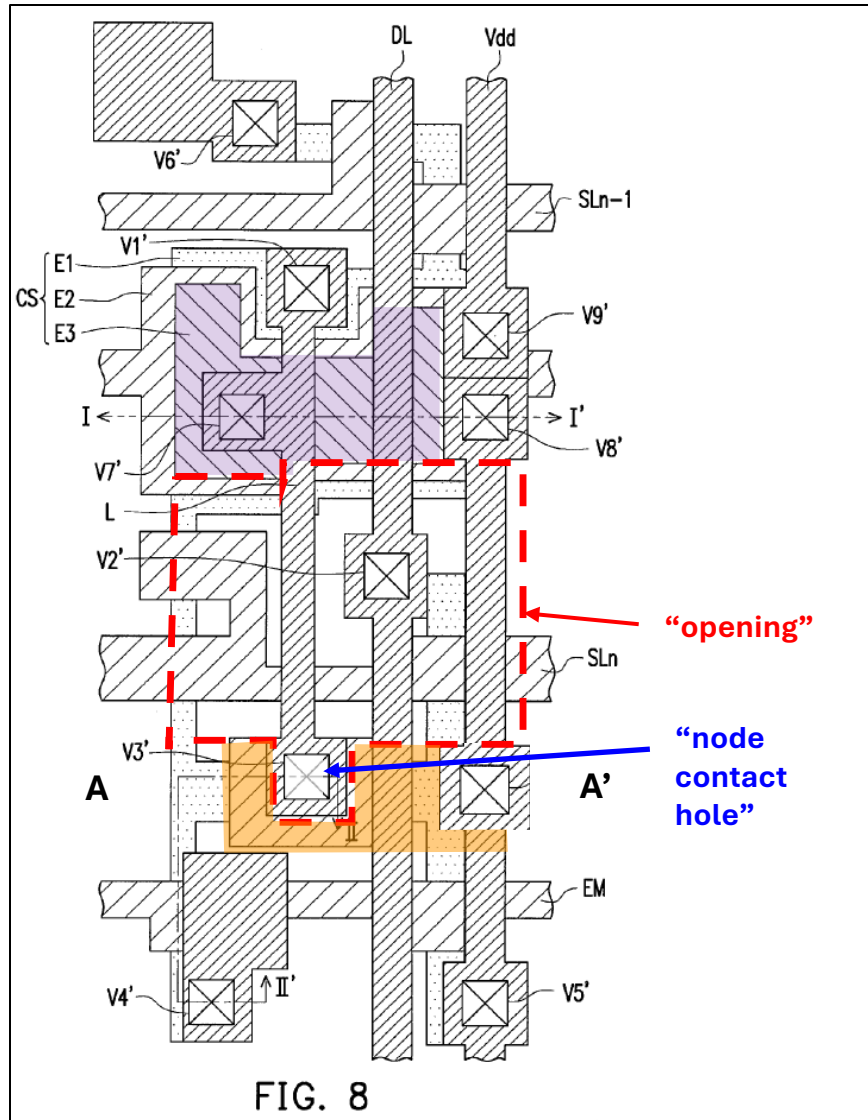
262. Liu teaches “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening.” For example, Liu discloses “[t]he second conductive layer M2’ is disposed on the second insulating layer 204

and has a material similar to or the same with the material of the second conductive layer M2' as described in the first embodiment.” (EX1007, [0066].) Liu also discloses that “third insulating layer 206 covers the second conductive layer M2'” and “the third conductive layer M3' is disposed on the third insulating layer 206.” (EX1007, ¶[0067], [0068].) Liu teaches that the third conductive layer M3' has source electrodes and drain electrodes that “are electrically connected to the source region and the drain regions through contact via structures V1'-V6'.” (EX1007, [0069].)

263. Figure 10 (annotated below) shows the *via structures* including via structure V3' in the *insulation layer 206* and the *insulation layer 204*.



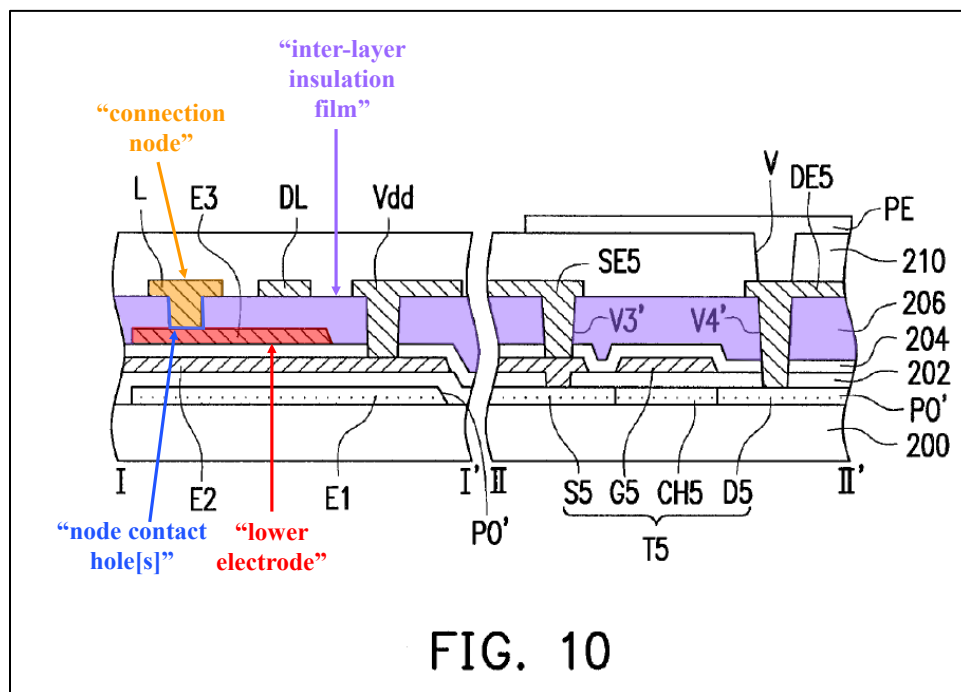
264. Modified Figure 8 (annotated below) shows *via structure V3'* within the *opening*.



- g. 1[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”

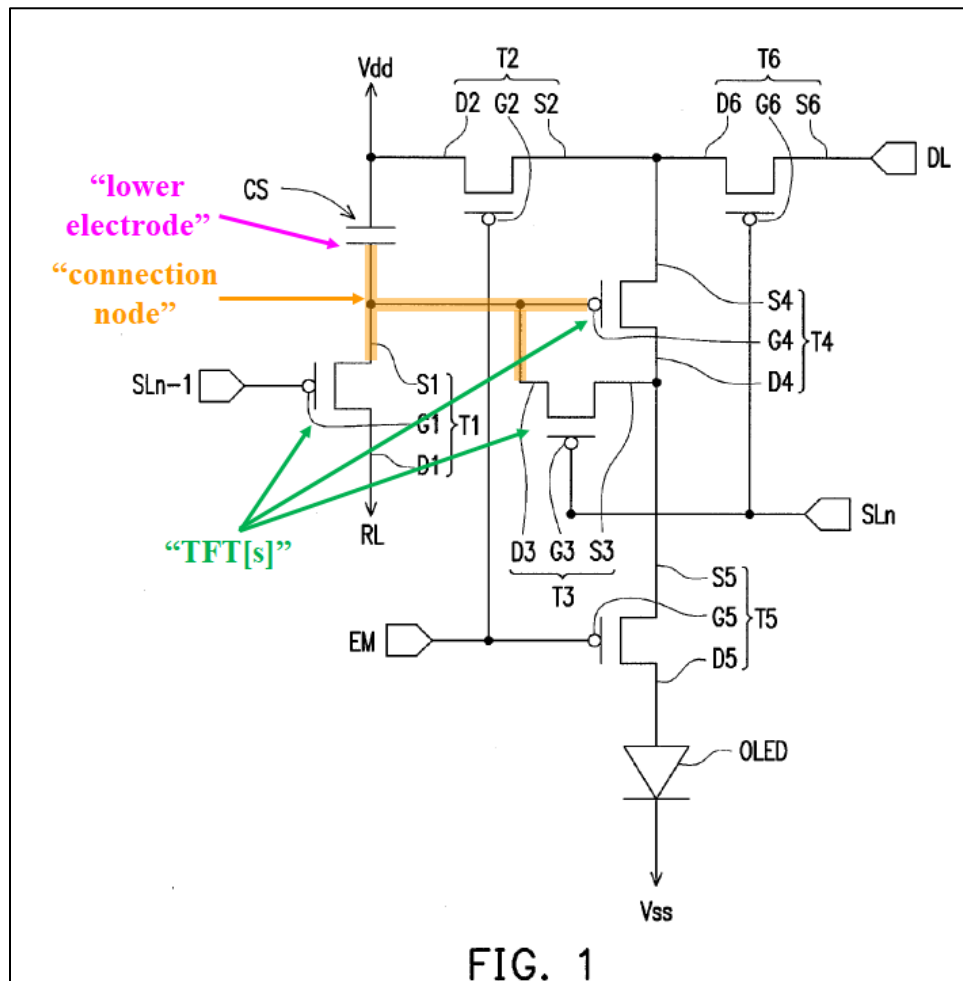
265. As shown for element 1[d], Liu teaches insulation film 206 (“inter-layer insulation film”). As shown for element 1[c], Liu teaches electrodes E1 and E3 (“lower electrode”). As shown for element 1[a], Liu teaches via structures (“node contact hole”).

266. Liu teaches “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.” For example, as shown below in annotated Figure 10, Liu discloses “[t]he third conductive layer M3’ may further comprise a signal line L, and the third electrode E3 of the capacitor CS is electrically connected to the signal line L through a contact via structure V7’.” (EX1007, [0070].) The figure below shows the **signal line L** disposed on **insulating layer 206**. The figure also shows the signal line L electrically coupled to the **electrode E2** through a **via structure**



267. Figure 1 (annotated below) shows the **signal line L** electrically coupling **electrodes E1 and E3** (“lower electrode”) to **transistors T1, T3, and T4** to each other. Liu discloses the electrical coupling as: “[t]he [] source electrodes and the drain electrodes are electrically connected to the source region and the

drain regions through contact via structures V1'-V6'." (EX1007, [0069].) A POSITA would have understood the via structures V1'-V6' are node contact holes. Figure 10 (above), for example, shows some of the via structures V1'-V6', including a via structure where the electrode E3 is electrically coupled to the signal line L, which electrically couples to transistor T4, as shown in Figure 8.

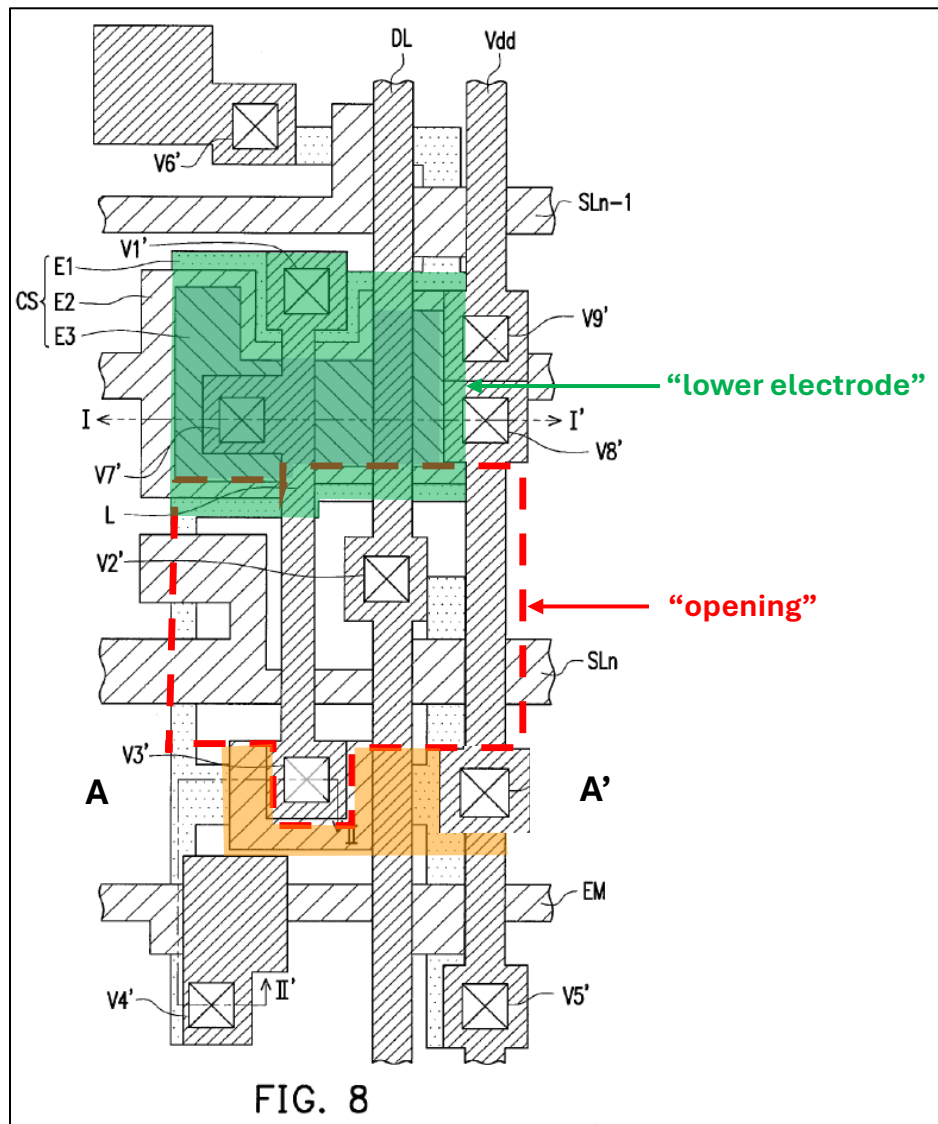


- 4. Claim 2: “The TFT array substrate of claim 1, wherein the opening overlaps with the lower electrode.”**

268. Liu-Ono teaches claim 1 as shown above in Section IX.E.3.

269. As shown for element 1[c], Liu teaches electrodes E1 and E3 (“lower electrode”).

270. Liu teaches “the opening overlaps with the lower electrode.” For example, modified Figure 8 (annotated below) shows the *opening* overlaps with *electrode E1*.



5. Claim 3

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

271. Preamble of claim 1 is similar to the preamble of claim 3, which Liu teaches. (See IX.E.3.a.) The table below shows the similarities.

Preamble of Claim 1	Preamble of Claim 3
“A thin film transistor (TFT) array substrate”	“A thin film transistor (TFT) array substrate”

b. 3[a]: “a substrate;”

272. Element 3[a] is similar to element 1[a], which Liu teaches. (See IX.E.3.b.) The table below shows the similarities.

Element 1[a]	Element 3[a]
“a substrate;”	“a substrate;”

c. 3[b]: “a first insulation layer on the substrate;”

273. Element 3[b] is similar to element 1[b], which Liu teaches. (See IX.E.3.c.) The table below shows the similarities.

Element 1[b]	Element 3[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

d. 3[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

274. Element 3[c] is similar to element 1[c], except that it does not require that the “upper electrode extend[] beyond an edge of the lower electrode,” as

shown in the table below. Liu and/or Ono teaches 1[c], and thus, teaches element 3[c]. (See IX.E.3.d.)

Element 1[c]	Element 3[c]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, <i>the upper electrode extending beyond an edge of the lower electrode</i> and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

e. 3[d]: “an inter-layer insulation film covering the capacitor;”

275. Element 3[d] is similar to element 1[d], which Liu and/or Ono teaches. (See IX.E.3.e.) The table below shows the similarities.

Element 1[d]	Element 3[d]
“an inter-layer insulation film covering the capacitor;”	“an inter-layer insulation film covering the capacitor;”

f. 3[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

276. Element 3[e] is similar to element 1[e], which Liu teaches. (See IX.E.3.f.) The table below shows the similarities.

Element 1[e]	Element 3[e]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

- g. **3[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole,”**

277. Element 3[f] is similar to element 1[f], which Liu teaches.

(See IX.A.2.g.) The table below shows the similarities.

Element 1[f]	Element 3[f]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole,”

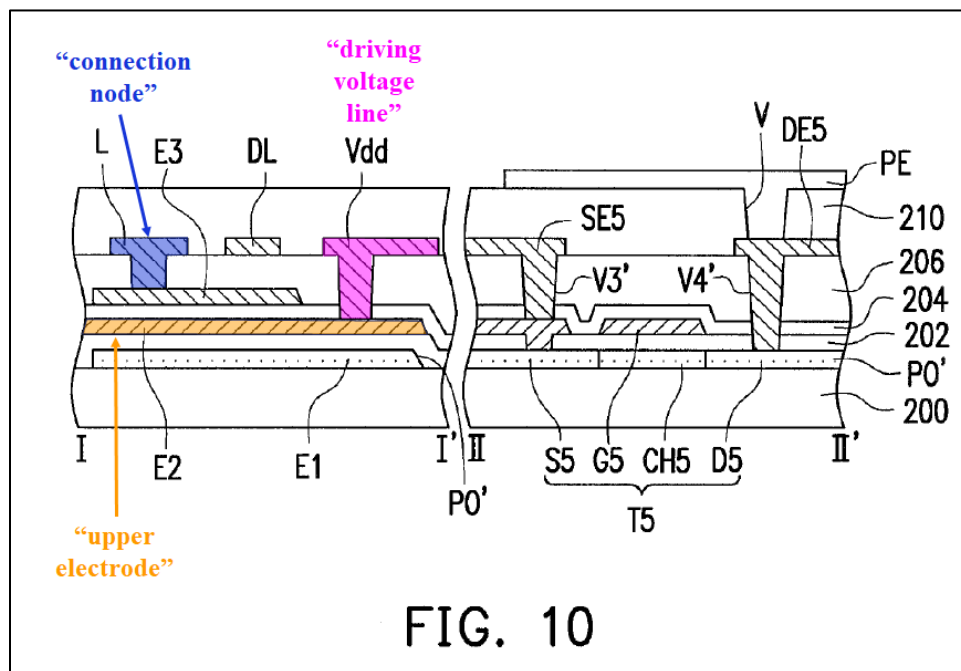
- h. **3[g]: “wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”**

278. As shown for element 1[c], Liu teaches electrode E2 (“upper electrode”). As shown for element 1[f], Liu teaches a signal line L (“connection node”) and a via structure V3’ (“node contact hole”).

279. Liu teaches “the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.” For example, “the third conductive layer M3” further comprises a data line DL and a power line Vdd. . . . the power line Vdd is electrically connected to the second electrode E2 of the capacitor CS through contact via structures V8’-V9’.” (EX1007, [0070].) Figure 10 section I-I’ (annotated below) shows *electrode E2* electrically coupled to the *power line Vdd*. A POSITA would

have understood that by being electrically coupled to the power line Vdd, electrode E2 receives a driving voltage through the power line. As shown for element 1[f], Liu explains that although Figure 10 shows the cross-sectional view of layers specifically for the via structures V3' and V4', the figure represents the layers and configurations of the other via structures. Figure 10 also shows the power line Vdd formed from the same layer as the *via structures*.

280. Liu discloses “the third conductive layer M3” further comprises a data line DL and a power line Vdd.” (EX1007, [0070].) Liu also discloses the “third conductive layer M3” may further comprise a signal line L.” (EX1007, [0070].) Figure 10 (annotated below) also shows the power line Vdd formed from the same layer as the *signal line L*. Thus, Liu teaches element 3[g].

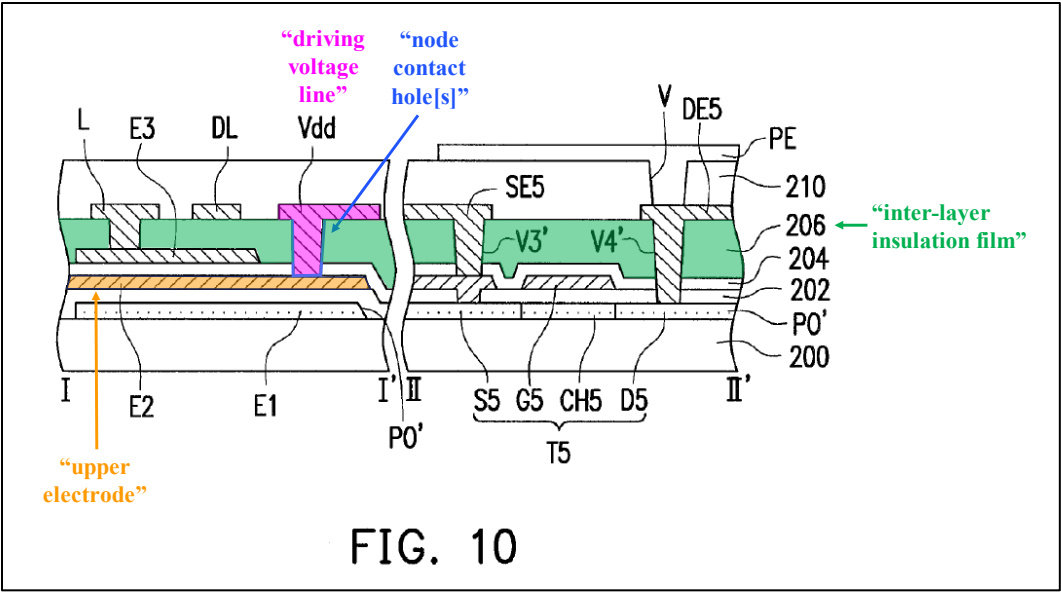


6. Claim 4: “The TFT array substrate of claim 3, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”

281. Liu-Ono teaches claim 3 as shown above in Section IX.E.5.

282. As shown for claim 3, Liu teaches a power line Vdd (“driving voltage line”). As shown for element 1[c], Liu teaches electrode E2 (“upper electrode”). As shown for element 1[d], Liu teaches insulation film 206 (“inter-layer insulation film”).

283. Liu teaches “the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.” For example, Liu discloses “the power line Vdd is electrically connected to the second electrode E2 of the capacitor CS through contact via structures V8'-V9'.” (EX1007, [0070].) Figure 10 shows the *power line Vdd* coupled to *electrode E2* through a *via structure*. The figure also shows the via structure for connecting power line Vdd to electrode E2 is in *insulation film 206*.



7. Claim 5

a. Preamble: “A thin film transistor (TFT) array substrate comprising:”

284. The preamble of claim 5 is similar to the preamble of claim 1, which Liu teaches. (See IX.E.3.a.) The table below shows the similarities.

Preamble of Claim 1	Preamble of Claim 5
“A thin film transistor (TFT) array substrate comprising:”	“A thin film transistor (TFT) array substrate comprising:”

b. 5[a]: “a substrate;”

285. Element 5[a] is similar to elements 1[a] and 3[a], which Liu teaches. (See IX.E.3.b, IX.E.5.b.) The table below shows the similarities.

Element 1[a]	Element 5[a]
“a substrate;”	“a substrate;”

c. 5[b]: “a first insulation layer on the substrate;”

286. Element 5[b] is similar to elements 1[b] and 3[b], which Liu teaches.

(See IX.E.3.c, IX.E.5.c.) The table below shows the similarities.

Element 1[b]	Element 5[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

d. 5[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

287. Element 5[c] is similar to element 3[c], which Liu and/or Ono teaches.

(See IX.E.5.d.) The table below shows the similarities.

Element 3[c]	Element 5[c]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

e. 5[d]: “an inter-layer insulation film covering the capacitor;”

288. Element 5[d] is similar to elements 1[d] and 3[d], which Liu and/or

Ono teaches. (See IX.E.3.e, IX.E.5.e.) The table below shows the similarities.

Element 1[d]	Element 5[d]
“an inter-layer insulation film covering the capacitor;”	“an inter-layer insulation film covering the capacitor;”

- f. 5[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening;”**

289. Element 5[e] is similar to elements 1[e] and 3[e], which Liu teaches.

(See IX.E.3.f, IX.E.5.f.) The table below shows the similarities.

Element 1[e]	Element 5[e]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening;”

- g. 5[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole; and”**

290. Element 5[f] is similar to elements 1[f] and 3[f], which Liu teaches.

(See IX.A.2.g, IX.C.2.f(ii).) The table below shows the similarities.

Element 1[f]	Element 5[f]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole; and”

- h. 5[g]: “a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”**

291. As shown for element 1[c], Liu teaches a capacitor CS comprising electrodes E1 and E3 (“lower electrode”).

292. Liu teaches “a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.” For example, Liu discloses “[t]he third conductive layer M3 has a source electrode and a drain electrode (not shown) in the region predetermined for forming the fourth thin film transistor T4, the source electrode and the drain electrode are electrically connected to the source region S4 and the drain region D4 respectively, and the source region S4, the drain region D4, the source electrode, the drain electrode and the gate G4 form the third thin film transistor T4.” (EX1007, [0069].) Figure 1 (annotated below) shows *transistor T4*, which has a drain D4 coupled to the anode of the OLED when transistor T5 is turned on. The figure also shows the transistor T4 comprises a gate G4, which comprises a driving gate electrode. The *gate G4* is coupled to the *lower electrode* of the *capacitor CS*. A POSITA would have understood transistor T4 is a driving TFT because it controls the driving of the OLED.

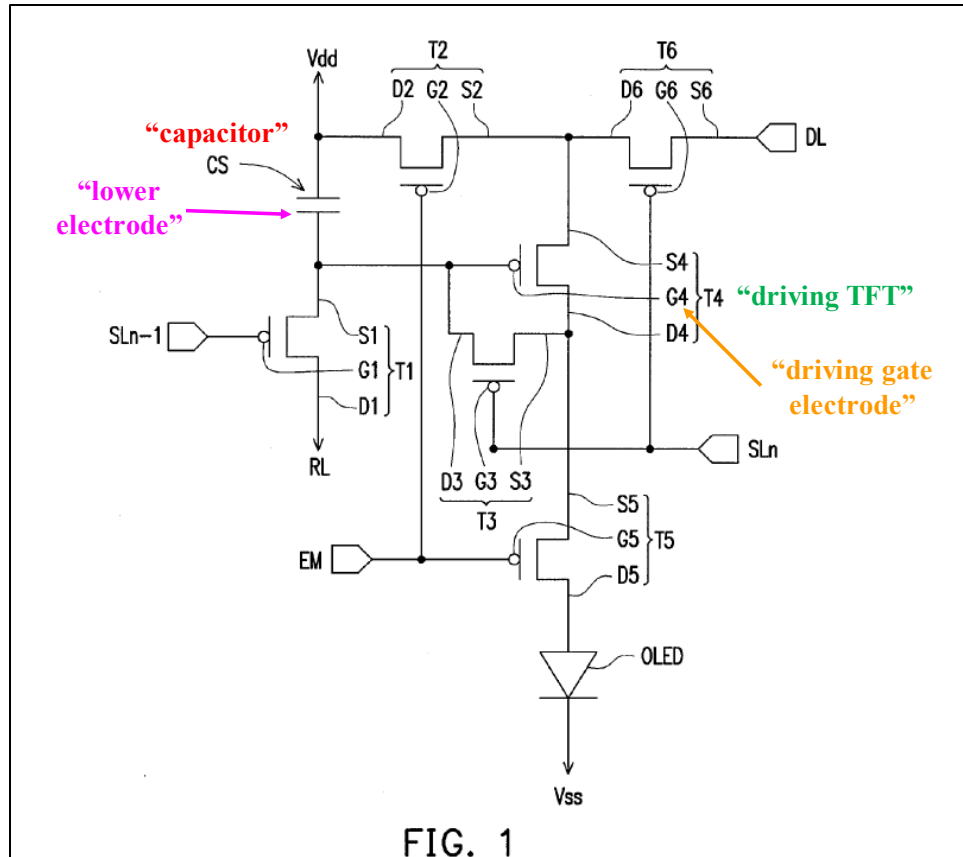


FIG. 1

293. As shown for element 1[c], the capacitor of the Liu-Ono combination comprises electrode E3 that is extended to overlap with transistor T4. It would have been obvious for the gate G4 of transistor T4 to comprise the electrode E1 or E2 because it would increase the size of the capacitor, which, as previously stated, would improve the uniformity of the luminescent display. Ono teaches “one of the capacitor electrodes of the capacitor can be used, . . . as the gate electrode of the driving transistor. . . . [t]herefore, it is possible to arrange a greater number of thin-film transistors and capacitors by efficiently using the limited pixel space.” (EX1008, [0037].) “With this, the gate electrode of the thin-film transistor is used not only simply as the gate electrode but also as one of two electrodes constituting

the capacitor. Thus, the capacitor can be formed above the thin-film transistor to overlap with the thin-film transistor, enabling efficient use of the pixel space. As a result, a complex driving circuit which includes multiple thin-film transistors and multiple capacitors can be formed in a region having a limited area. It is to be noted that the structure of the present invention can be applied to a capacitor for holding the gate Voltage, as well as a capacitor for holding a threshold voltage V_{th} in the driving circuit.” (EX1008, [0030].)

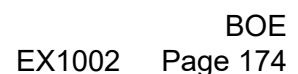
8. Claim 6: “The TFT array substrate of claim 5, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”

294. Liu teach claim 5 as shown above in Section IX.E.7.

295. As shown for element 1[f], Liu teaches transistors T1, T3, and T4 (“at least one TFT”). As shown for claim 5, Liu teaches a transistor T4 (“driving TFT”). As shown for element 1[c], Liu teaches electrodes E1 and E3 (“lower electrode”).

296. Liu teaches “the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.” For example, Liu

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297. It would have been obvious that the transistor T3 is a compensation TFT that couples the gate G4 and drain D4 of the transistor T4 (driving TFT) when turned on in response to the scan signal SLn. By coupling the gate G4 and the drain D4 together, the transistor T3 compensates for the threshold voltage of the transistor T4.

9. Claim 8

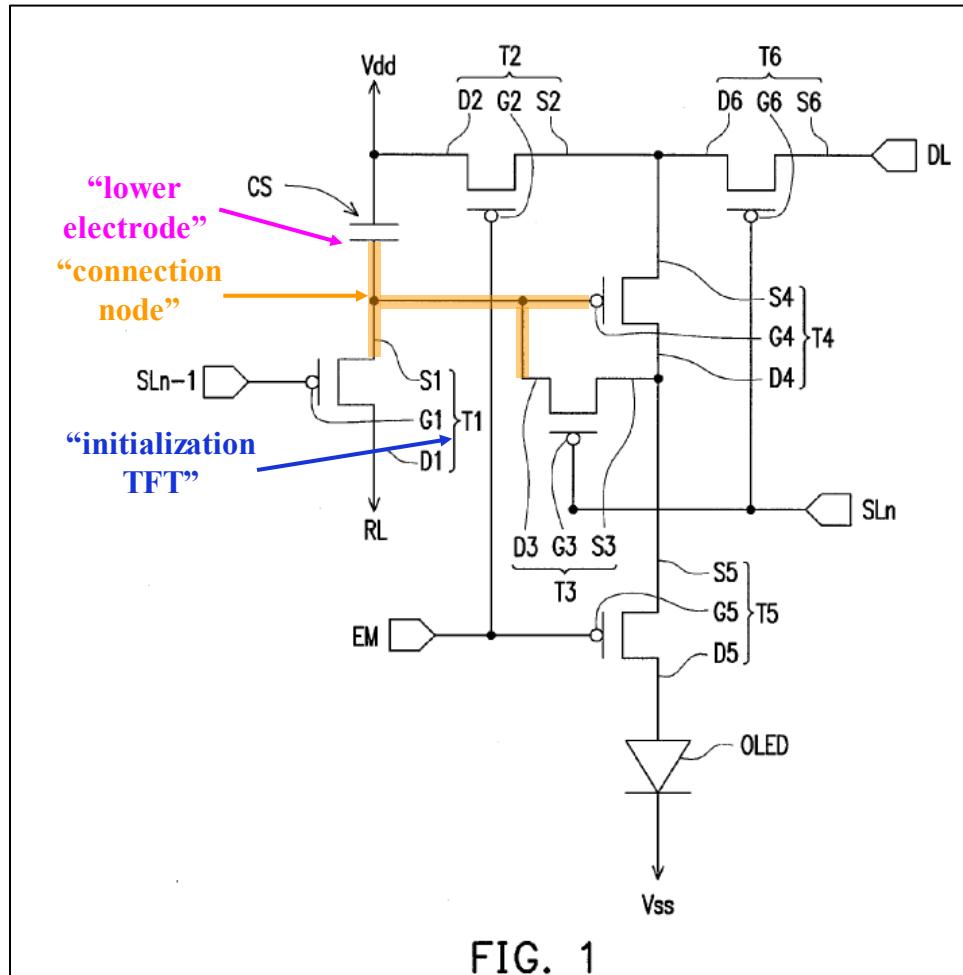
- a. **8[a]: “The TFT array substrate of claim 5, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”**

298. Liu and Ono teach claim 5 as shown above in Section IX.E.7.

299. As shown for element 1[f], Liu teaches transistors T1, T3, and T4 (“at least one TFT”). As shown for element 1[c], Liu teaches electrodes E1 and E3 (“lower electrode”).

300. Liu teaches “the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node.” For example, Liu discloses “the third conductive layer M3 has a source electrode and a drain electrode (not shown) in the region predetermined for forming the first thin film transistor T1, the source electrode and the drain electrode are electrically connected to the source region S1 and the drain region D1 respectively, and the source region S1, the drain region D1, the source electrode, the drain electrode and

the gate G1 form the first thin film transistor T1.” (EX1007, [0069].) Figure 1 (annotated below) shows *transistor T1* electrically coupled to the *lower electrode* of the capacitor through the *connection node*.



- b. **8[b]: “wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”**

301. As shown for element 5[g], Liu teaches a gate G4 (“driving gate electrode”) of transistor T4 (“driving TFT”). As shown for element 8[a], Liu teaches transistor T1 (“initialization TFT”).

302. Liu teaches “the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.” For example, Figure 1 (annotated below) shows the *transistor T1* configured to provide a voltage from *reference signal line RL* to the *gate G4* of *transistor T4*. The gate of transistor T1 is coupled to SLn-1, which means transistor T1 is turned on in response to scan line *SLn-1*. Liu explains “the first conductive layer M1 further comprises a scan line SLn, a scan line SLn-1 and a light emitting signal line EM, wherein the scan line SLn is electrically connected to the gate G3, the scan line SLn-1 is electrically connected to the gate G1.” (EX1007, [0064].) A POSITA would have understood SLn-1 is a previous scan signal because the “n-1” notation refers to a number that is one less than n, *i.e.*, previous.

303. A POSITA would have understood transistor T1 to be an initialization TFT because its drain D1 is coupled to the reference line RL and its source S1 is

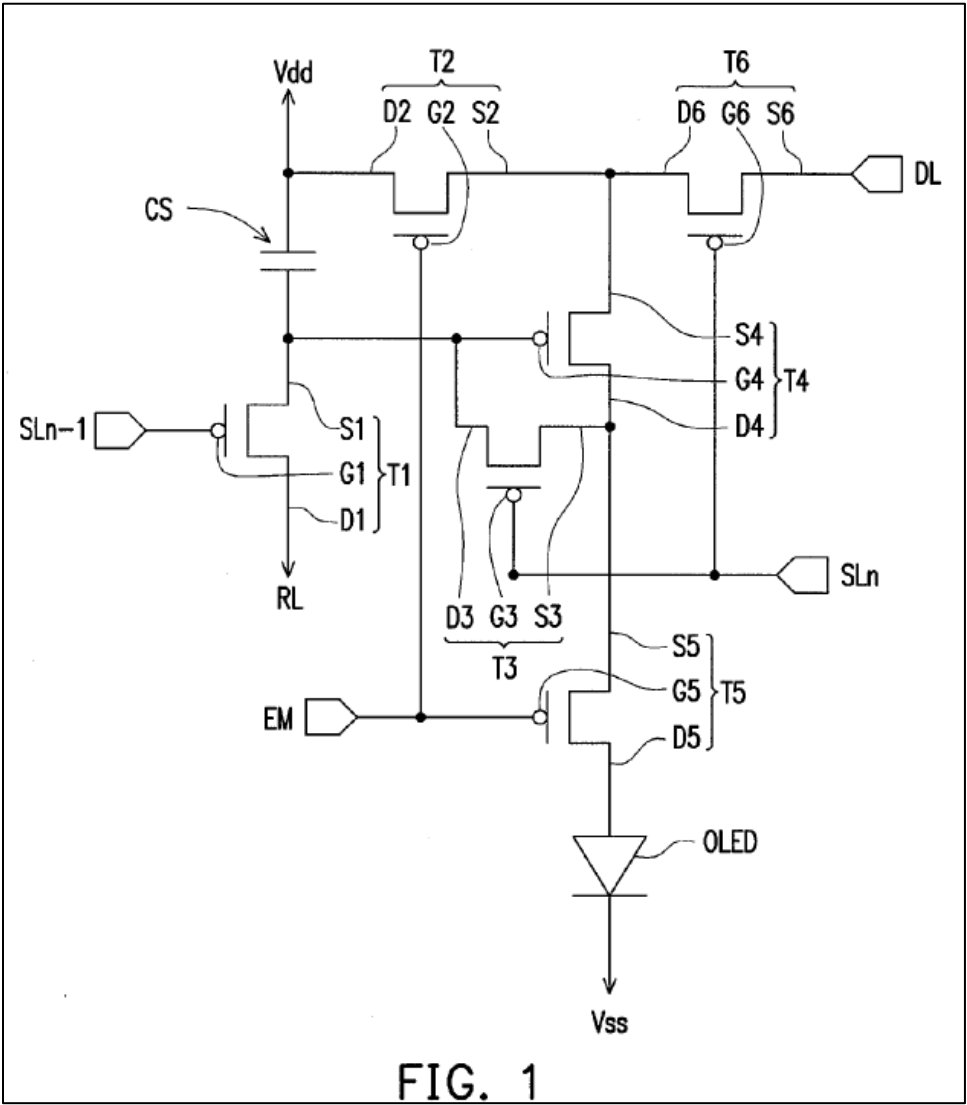
304. Liu teaches “[a]n organic light-emitting diode (OLED) display.” For example, Liu discloses “[t]he pixel electrode PE, the light emitting layer OE and the electrode layer CA form an organic light emitting device OLED.” (EX1007,



a. Preamble: “An organic light-emitting diode (OLED) display comprising:”

304. Liu teaches “[a]n organic light-emitting diode (OLED) display.” For example, Liu discloses “[t]he pixel electrode PE, the light emitting layer OE and the electrode layer CA form an organic light emitting device OLED.” (EX1007,

[0073].) Figure 1 shows a circuit diagram of Liu’s pixel structure including an OLED.



b. 10[a]: “a substrate;”

305. Element 10[a] is similar to elements 1[a] and 3[a], which Liu teaches. (See IX.E.3.b, IX.E.5.b.) The table below shows the similarities.

Element 1[a]	Element 10[a]
“a substrate;”	“a substrate;”

c. 10[b]: “a first insulation layer on the substrate;”

306. Element 10[b] is similar to elements 1[b] and 3[b], which Liu teaches.

(See IX.E.3.c, IX.E.5.c.) The table below shows the similarities.

Element 1[b]	Element 10[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

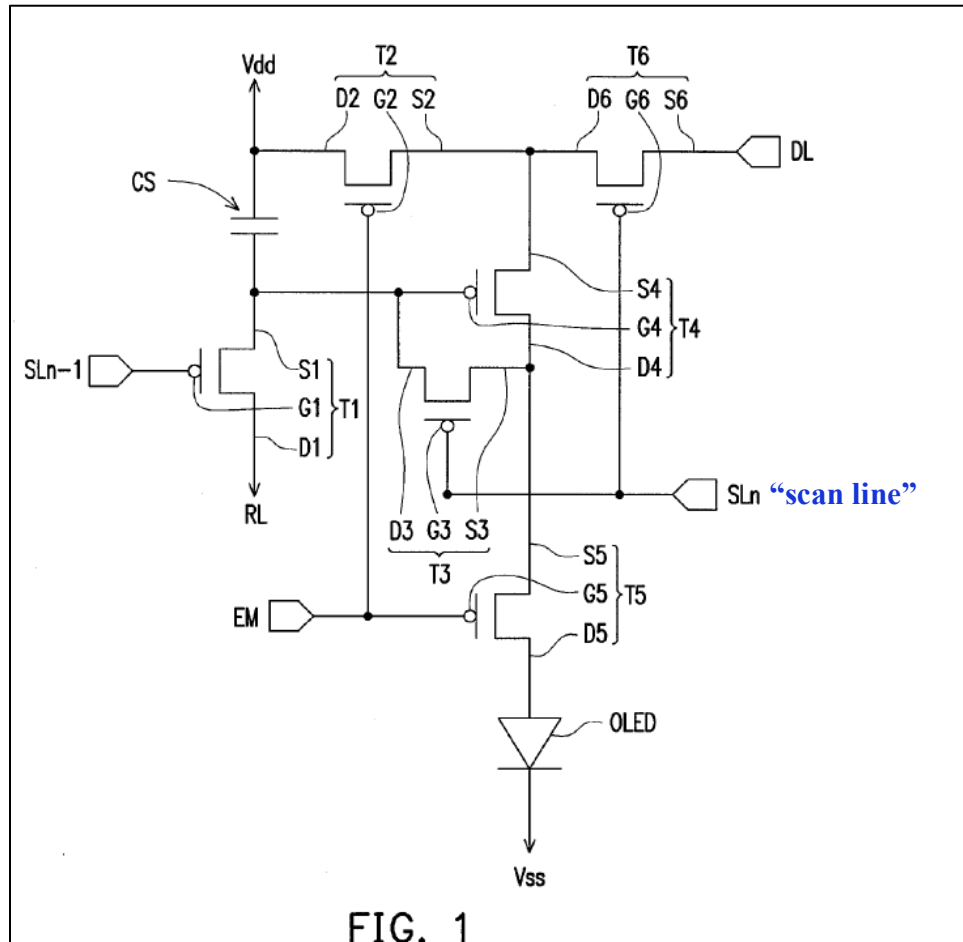
d. 10[c]: “a scan line on the first insulation layer and configured to deliver a scan signal;”

307. As shown for element 1[b], Liu teaches insulating layer 202 (“first insulation layer”).

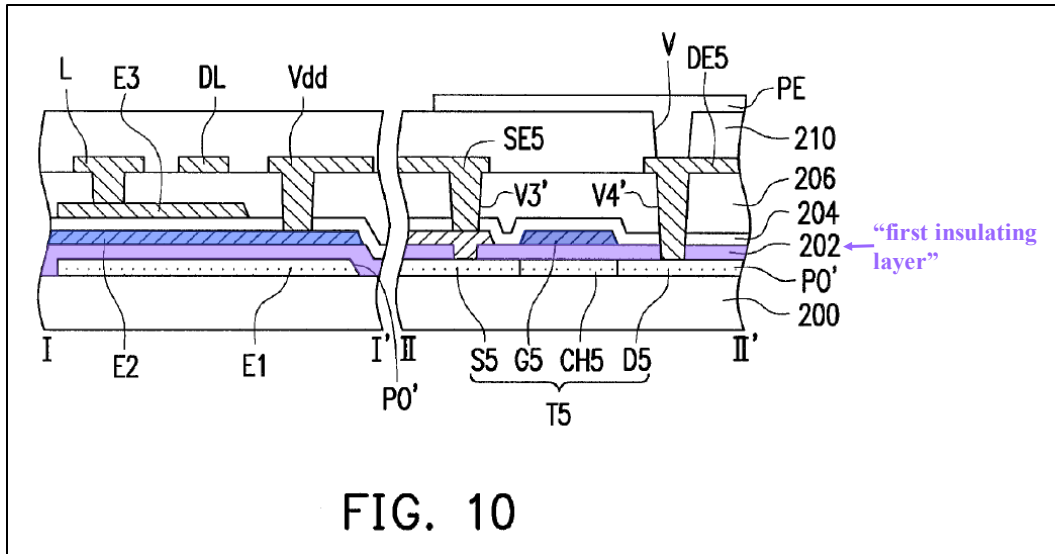
308. Liu teaches “a scan line on the first insulation layer and configured to deliver a scan signal.” For example, Liu discloses “*the first conductive layer M1’ further comprises a scan line SL_n, a scan line SL_{n-1} and a light emitting signal line EM, wherein the scan line SL_n is electrically connected to the gate G3, the scan line SL_{n-1} is electrically connected to the gate G1, and the light emitting signal line EM is electrically connected to the gates G5, G2.*” (EX1007, [0064] (emphasis added).) Since the scan line SL_n is electrically connected to the gate G3, it would have been obvious that it delivers a scan signal. It was known for displays at the time to have scan lines that deliver scan signals. (See, e.g., EX1011, Abstract (“[a] pixel structure including a first scan line, a second scan line, a data

line and a power line substantially perpendicular to the first scan line, . . .).)

Figure 1 (annotated below) shows the scan line SL_n .



309. Figure 10 (annotated below) shows the *first conductive layer M1'* where *scan line SL_n* is located, on the *insulating layer 202*. As Liu explains, “the layout of the first conductive layer M1' is shown in FIG.9B, which mainly comprises gates of the six thin film transistors and a second electrode E2 of the capacitor CS. For example, the first conductive layer M1' has a gate G5 in the region predetermined for forming the fifth thin film transistor T5, as shown in FIG. 10.” (EX1007, [0063].)



310. Thus, Liu teaches a scan line SL_n on the insulating layer 202 and is configured to deliver a scan signal.

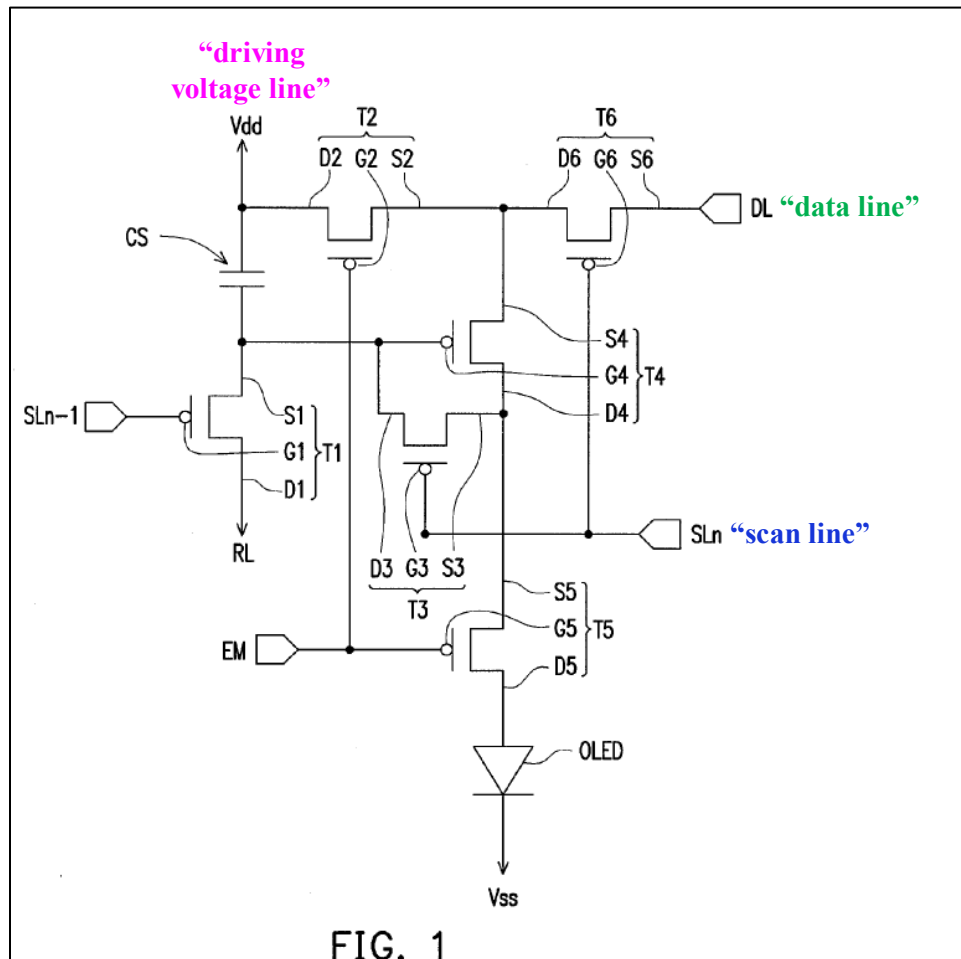
- e. **10[d]: “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”**

311. As shown for element 3[g], Liu teaches a power line V_{dd} (“driving voltage line”) configured to deliver a driving voltage. As shown for element 1[d], Liu teaches an insulating layer 206 (“inter-layer insulation film”). As shown for element 1[c], Liu teaches an insulating layer 204 (“second insulation layer”)

312. Liu teaches “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage.” For example, Liu discloses “the third

conductive layer M3" further comprises a data line DL and a power line Vdd."

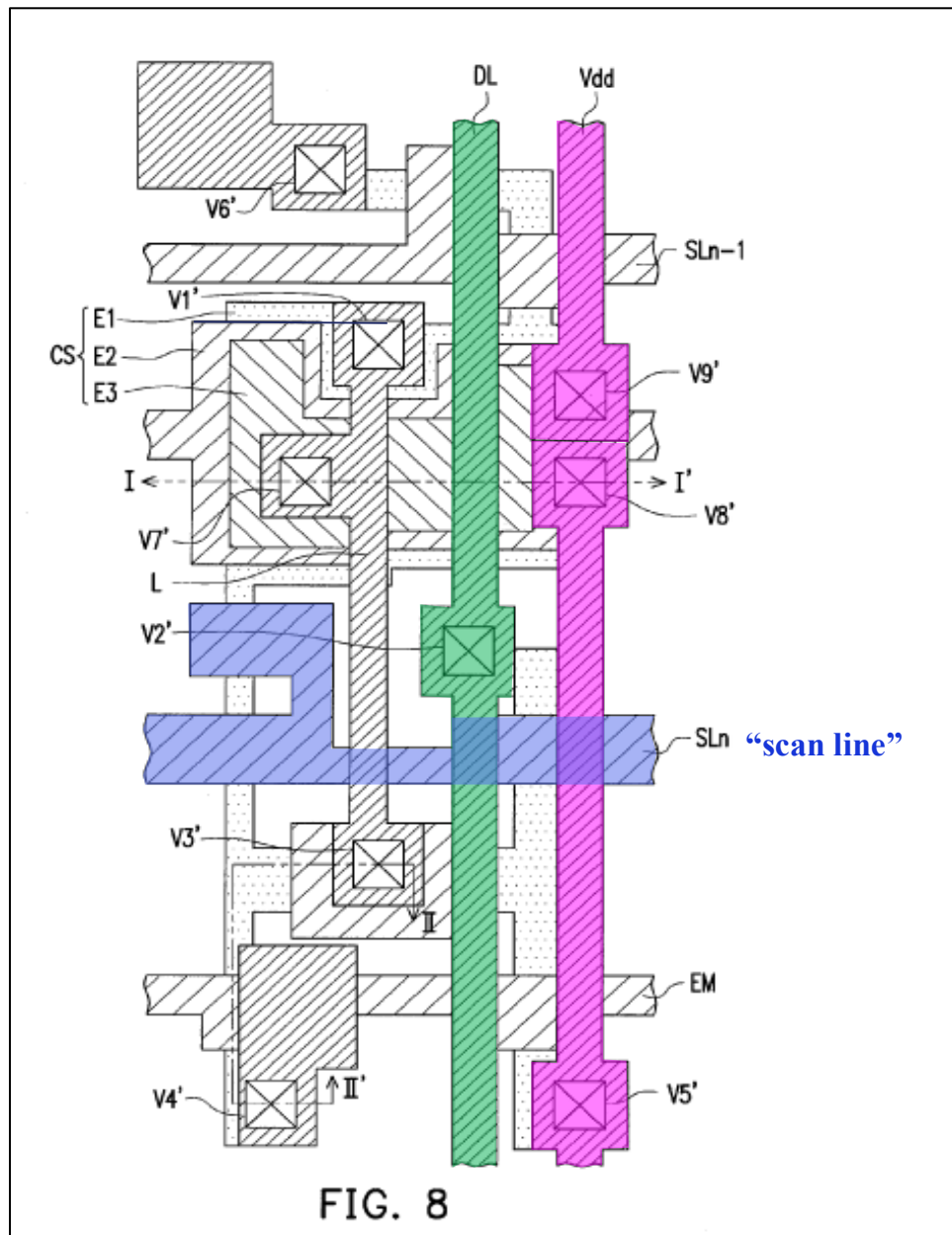
(EX1007, [0070].) Figure 1 (annotated below) shows the *data line DL*, the *power line Vdd*, the *scan SLn*.



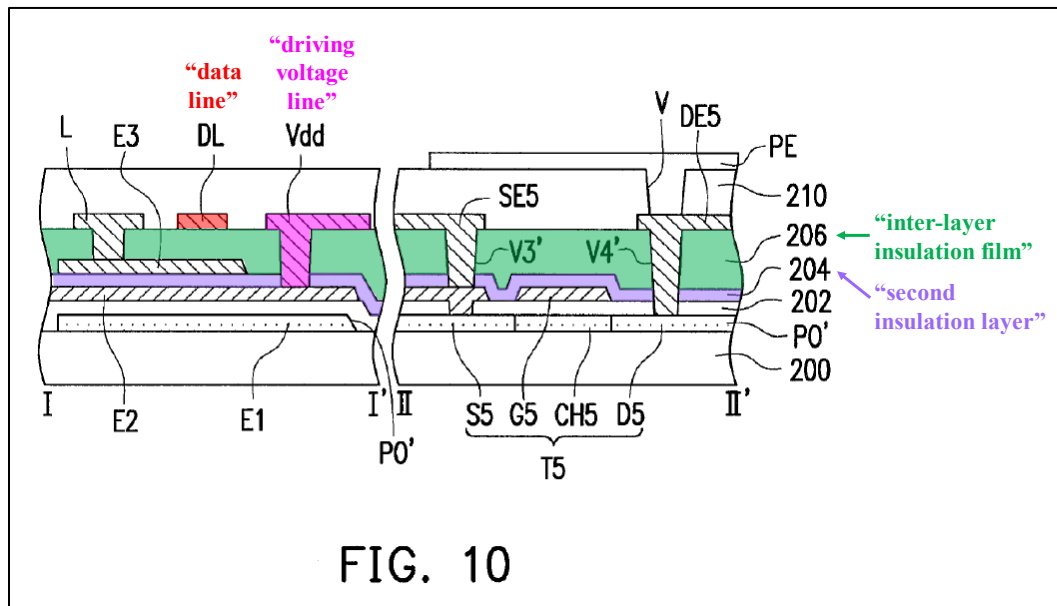
313. Liu also discloses that “[t]he data line DL is electrically connected to the source region S6, and the power line Vdd is electrically connected to the drain region D2, as shown in FIG. 1, FIG. 2 and FIG. 3C.” (EX1007, [0042].) Since the data line DL is electrically connected to the source S6, it would have been obvious that it delivers a scan signal. It was known for displays at the time to have scan

lines that deliver scan signals. (See, e.g., EX1011, Abstract (“[a] pixel structure including a first scan line, a second scan line, a data line and a power line substantially perpendicular to the first scan line, . . .).)

314. Figure 8 (annotated below) shows the *data line DL* and *power line Vdd* crossing the *scan line SLn*.



315. Liu discloses “the third conductive layer M3’ further comprises a data line DL and a power line Vdd.” (EX1007, [0070].) Liu also discloses “[t]he third conductive layer M3’ is disposed on the third insulating layer 206 and has a material similar to or the same with the material of the third conductive layer M3 as described in the first embodiment.” (EX1007, [0068].) Figure 10 (annotated below) shows the *data line DL* and the *power line Vdd* being insulated by *insulating layer 204* and *insulating layer 206*.

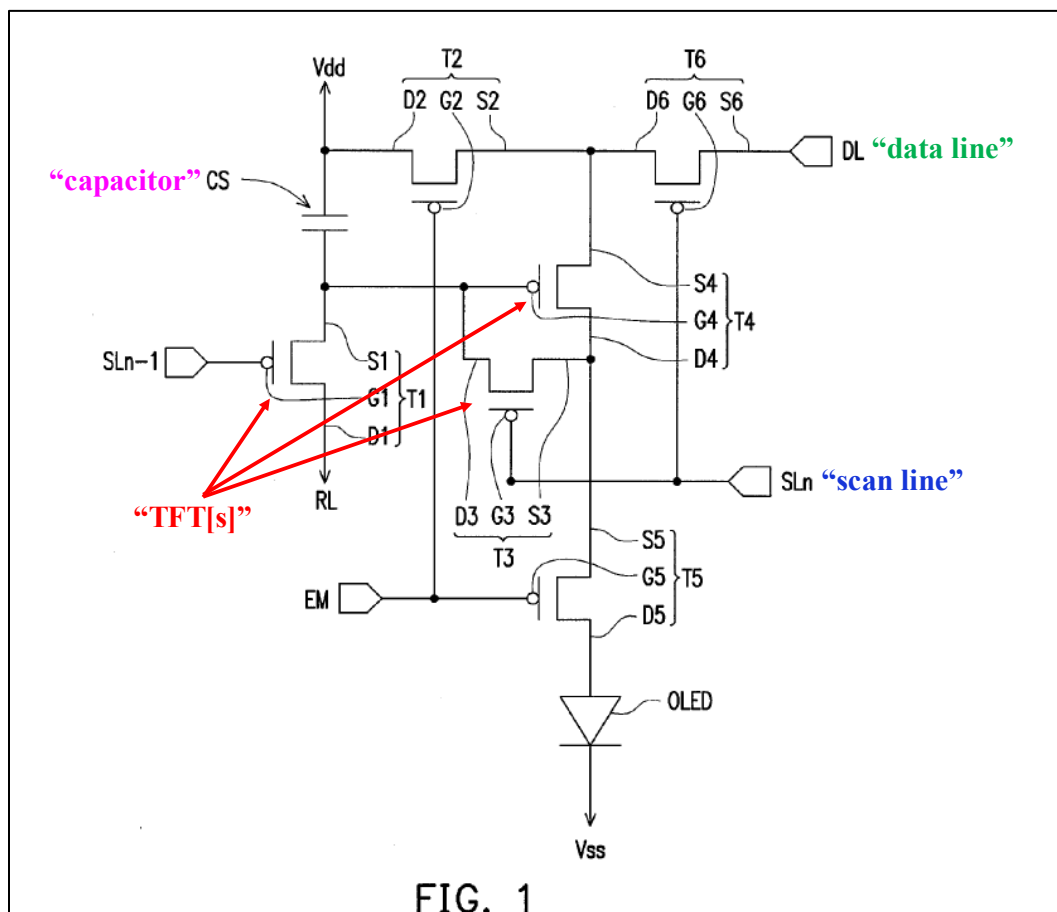


f. 10[e]: “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

316. As shown for element 10[c], Liu teaches a scan line SLn (“scan line”). As shown for element 10[b], Liu teaches a data line DL (“data line”). As shown for element 1[f], Liu teaches transistors T1, T3, and T4 (“at least one TFT”). As

shown for element 1[c], Liu and Ono teach a capacitor CS (“capacitor”) including an extended upper electrode.

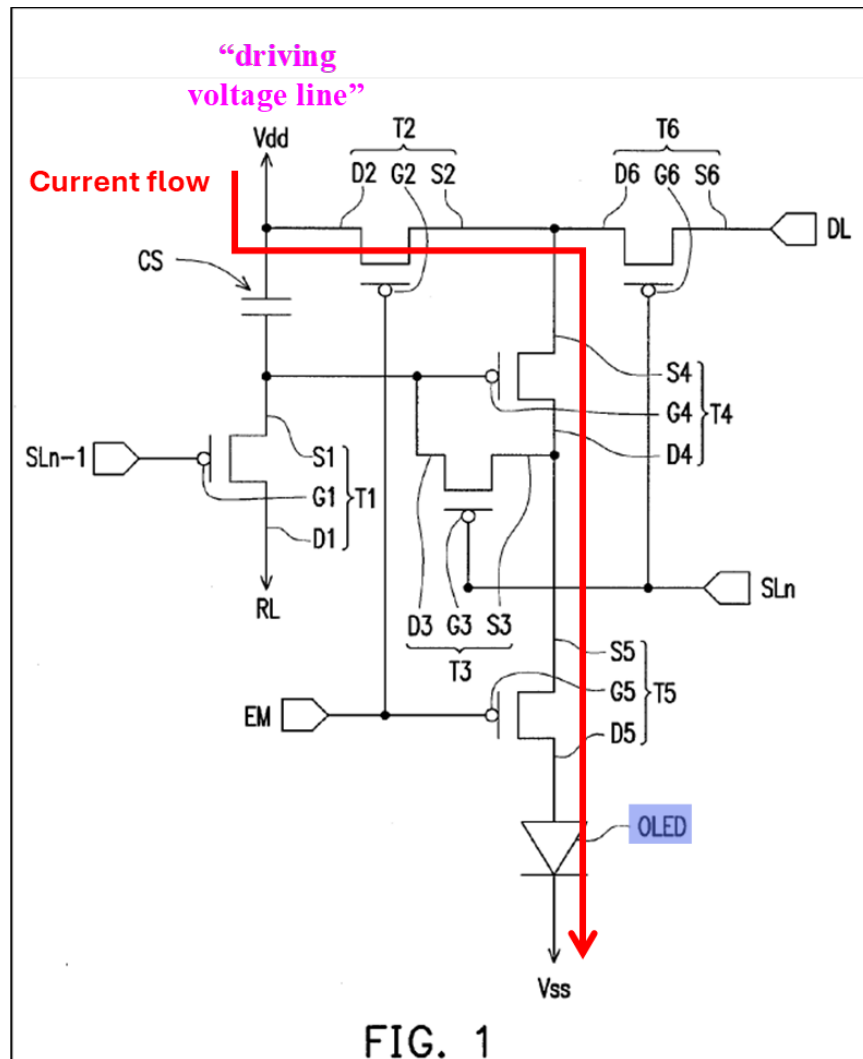
317. Liu teaches “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor.” For example, Liu discloses “FIG. 1 is a schematic circuit diagram of a pixel structure according to an embodiment of the invention.” (EX1007, [0031].) Figure 1 (annotated below) shows the pixel circuit coupled to the *scan line SLn* and the *data line DL* and comprising *transistors T1, T3, and T4* and *capacitor CS*.



g. 10[f]: “an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

318. As shown for element 10[d], Liu teaches Vdd (“driving voltage”). As shown for element 10[e], Liu teaches the circuit of Figure 1 (“pixel circuit”).

319. Liu teaches “an OLED for emitting light by receiving the driving voltage from the pixel circuit.” For example, Liu discloses “[i]f the pixel structure is applied to an organic electroluminescence display, the pixel structure further comprises a light emitting region defining layer 212, a light emitting layer OE and an electrode layer CA, as shown in FIG. 11. The pixel electrode PE, the light emitting layer OE and the electrode layer CA form an organic light emitting device OLED.” (EX1007, [0073].) Figure 1 (annotated below) shows the **OLED**. The OLED is coupled to Vdd via transistors T2, T4, and T5. A POSITA would have understood that the OLED would emit light by receiving **Vdd** from the Figure 1 circuit because current will flow from Vdd through transistors T2, T4, and T5 when light emitting signal line EM is ON and then through OLED to Vss.



- h. 10[g]: “wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”

320. Element 10[g] is similar to element 1[c], which Liu and/or Ono teaches. (See IX.E.3.d.) The table below shows the similarities.

Element 1[c]	Element 10[g]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”

- i. **10[h]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”**

321. Element 10[h] is similar to element 1[e], which Liu teaches.

(See IX.E.3.f.) The table below shows the similarities.

Element 1[e]	Element 10[h]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

- j. **10[i]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole.”**

322. Element 10[i] is similar to element 1[f], which Liu teaches.

(See IX.A.2.g.) The table below shows the similarities.

Element 1[f]	Element 10[i]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole.”

11. Claim 11: “The OLED display of claim 10, wherein the opening overlaps with the lower electrode.”

323. Liu-Ono teaches claim 10 as shown above in Section IX.E.10.

324. Claim 11 is similar to claim 2, which Liu and/or Ono teaches.

(See IX.E.4.) The table below shows the similarities.

Claim 2	Claim 11
“The TFT array substrate of claim 1, wherein the opening overlaps with the lower electrode.”	“The OLED display of claim 10, wherein the opening overlaps with the lower electrode.”

12. Claim 12

a. Preamble: “An organic light-emitting diode (OLED) display comprising:”

325. The preamble of claim 12 is similar to the preamble of claim 10, which Liu teaches. (See IX.E.10.a.) The table below shows the similarities.

Preamble of Claim 10	Preamble of Claim 12
“An organic light-emitting diode (OLED) display comprising:”	“An organic light-emitting diode (OLED) display comprising:”

b. 12[a]: “a substrate;”

326. Element 12[a] is similar to elements 1[a] and 3[a], which Liu teaches. (See IX.E.3.b, IX.E.5.b.) The table below shows the similarities.

Element 1[a]	Element 12[a]
“a substrate;”	“substrate;”

c. 12[b]: “a first insulation layer on the substrate;”

327. Element 12[b] is similar to elements 1[b] and 3[b], which Liu teaches.

(See IX.E.3.c, IX.E.5.c.) The table below shows the similarities.

Element 1[b]	Element 12[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

d. 12[c]: “a scan line on the first insulation layer and configured to deliver a scan signal;”

328. Element 12[c] is similar to element 10[c], which Liu teaches.

(See IX.E.10.d.) The table below shows the similarities.

Element 10[c]	Element 12[c]
“a scan line on the first insulation layer and configured to deliver a scan signal;”	“a scan line on the first insulation layer and configured to deliver a scan signal;”

e. 12[d]: “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

329. Element 12[d] is similar to element 10[d], which Liu teaches.

(See IX.E.10.e.) The table below shows the similarities.

Element 10[d]	Element 12[d]
“a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”	“a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

f. 12[e]: “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

330. Element 12[e] is similar to element 10[e], which Liu and/or Ono teaches. (See IX.E.10.f.) The table below shows the similarities.

Element 10[e]	Element 12[e]
“a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”	“a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

g. 12[f]: “an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

331. Element 12[f] is similar to element 10[f], which Liu teaches. (See IX.E.10.g.) The table below shows the similarities.

Element 10[f]	Element 12[f]
“an OLED for emitting light by receiving the driving voltage from the pixel circuit,”	“an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

- h. 12[g]: “wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”**

332. Element 12[g] is similar to element 3[c], which Liu and/or Ono teaches. (See IX.E.5.d.) The table below shows the similarities.

Element 3[c]	Element 12[g]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”

- i. 12[h]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”**

333. Element 12[h] is similar to elements 1[e] and 3[e], which Liu teaches. (See IX.E.3.f, IX.E.5.f.) The table below shows the similarities.

Element 1[e]	Element 12[h]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

- j. **12[i]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole,”**

334. Element 12[i] is similar to elements 1[f] and 3[f], which Liu teaches.

(See IX.A.2.g, IX.C.2.f(ii).) The table below shows the similarities.

Element 1[f]	Element 12[i]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole,”

- k. **12[j]: “wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”**

335. Element 12[j] is similar to element 3[g], which Liu teaches.

(See IX.E.5.h.) The table below shows the similarities.

Element 3[g]	Element 12[j]
“wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”	“wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”

- 13. Claim 13: “The OLED display of claim 12, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”**

336. Liu-Ono teaches claim 12 as shown above in Section IX.E.12.

337. Claim 13 is similar to claim 4, which Liu teaches. (See IX.E.6.) The table below shows the similarities.

Claim 4	Claim 13
“The TFT array substrate of claim 3, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”	“The OLED display of claim 12, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”

14. Claim 14

a. Preamble: “An organic light-emitting diode (OLED) display comprising:

338. The preamble of claim 14 is similar to the preamble of claim 10, which Liu teaches. (See IX.E.10.a.) The table below shows the similarities.

Preamble of Claim 10	Preamble of Claim 14
“An organic light-emitting diode (OLED) display comprising:”	“An organic light-emitting diode (OLED) display comprising:

b. 14[a]: “a substrate;”

339. Element 14[a] is similar to elements 1[a] and 3[a], which Liu teaches. (See IX.E.3.b, IX.E.5.b.) The table below shows the similarities.

Element 1[a]	Element 14[a]
“a substrate;”	“a substrate;”

c. 14[b]: “a first insulation layer on the substrate;”

340. Element 14[b] is similar to elements 1[b] and 3[b], which Liu teaches. (See IX.E.3.c, IX.E.5.c.) The table below shows the similarities.

Element 1[b]	Element 14[b]
“a first insulation layer on the substrate;”	“a first insulation layer on the substrate;”

d. 14[c]: “a scan line on the first insulation layer and configured to deliver a scan signal;”

341. Element 14[c] is similar to element 10[c], which Liu teaches.

(See IX.E.10.d.) The table below shows the similarities.

Element 10[c]	Element 14[c]
“a scan line on the first insulation layer and configured to deliver a scan signal;”	“a scan line on the first insulation layer and configured to deliver a scan signal;”

e. 14[d]: “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

342. Element 14[d] is similar to element 10[d], which Liu teaches.

(See IX.E.10.e.) The table below shows the similarities.

Element 10[d]	Element 14[d]
“a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”	“a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

- f. 14[e]: “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”**

343. Element 14[e] is similar to element 10[e], which Liu teaches.

(See IX.E.10.f.) The table below shows the similarities.

Element 10[e]	Element 14[e]
“a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”	“a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

- g. 14[f]: “an OLED for emitting light by receiving the driving voltage from the pixel circuit,”**

344. Element 14[f] is similar to element 10[f], which Liu teaches.

(See IX.E.10.g.) The table below shows the similarities.

Element 10[f]	Element 14[f]
“an OLED for emitting light by receiving the driving voltage from the pixel circuit,”	“an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

- h. 14[g]: “wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”**

345. Element 14[g] is similar to element 3[c], which Liu and/or Ono teaches. (See IX.E.5.d.) The table below shows the similarities.

Element 3[c]	Element 14[g]
“a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”	“wherein the capacitor comprises a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by the second insulation layer;”

- i. 14[h]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening;”**

346. Element 14[h] is similar to elements 1[e] and 3[e], which Liu teaches.

(See IX.E.3.f, IX.E.5.f.) The table below shows the similarities.

Element 1[e]	Element 14[h]
“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”	“a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening;”

- j. 14[i]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole; and”**

347. Element 14[i] is similar to elements 1[f] and 3[f], which Liu teaches.

(See IX.A.2.g, IX.C.2.f(ii).) The table below shows the similarities.

Element 1[f]	Element 14[i]
“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”	“a connection node on the inter-layer insulation film and electrically coupling the lower electrode and the at least one TFT to each other through the node contact hole; and”

- k. **14[j]: “a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”**

348. Element 14[j] is similar to element 5[g], which Liu teaches.

(See IX.E.7.h.) The table below shows the similarities.

Element 5[g]	Element 14[j]
“a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”	“a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”

15. **Claim 15: “The OLED display of claim 14, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”**

349. Liu-Ono teaches claim 14 as shown above in Section IX.E.14.

350. Claim 15 is similar to claim 6, which Liu teaches. (See IX.E.8.) The table below shows the similarities.

Claim 6	Claim 15
“The TFT array substrate of claim 5, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”	“The OLED display of claim 14, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”

16. Claim 16: “The OLED display of claim 15, wherein a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.”

351. Liu-Ono teaches claim 15 as shown above in Section IX.E.15.

352. Claim 16 is similar to claim 7, which Liu teaches. (*See Error!*

Reference source not found..) The table below shows the similarities.

Claim 7	Claim 16
“The TFT array substrate of claim 6, wherein a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.”	“The OLED display of claim 15, wherein a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.”

17. Claim 17

a. 17[a]: “The OLED display of claim 14, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”

353. Liu-Ono teaches claim 14 as shown above in Section IX.E.14.

354. Element 17[a] is similar to element 8[a], which Liu teaches.

(*See IX.E.9.a.*) The table below shows the similarities.

Element 8[a]	Element 17[a]
“The TFT array substrate of claim 5, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”	“The OLED display of claim 14, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”

- b. 17[b]: “wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”**

355. Element 17[b] is similar to element 8[b], which Liu teaches.

(See IX.E.9.b.) The table below shows the similarities.

Element 8[b]	Element 17[b]
“wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”	“wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”

- 18. Claim 18: “The OLED display of claim 17, wherein an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode.”**

356. Liu-Ono teaches claim 17 as shown above in Section IX.E.17.

357. Claim 18 is similar to claim 9, which Liu teaches. (See **Error!**

Reference source not found..) The table below shows the similarities.

Claim 9	Claim 18
“The TFT array substrate of claim 8, wherein an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode.”	: “The OLED display of claim 17, wherein an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode.”

19. Claim 19: “The OLED display of claim 14, further comprising a switching TFT for delivering the data signal to the driving TFT by being turned on by the scan signal.”

358. Liu-Ono teaches claim 14 as shown above in Section IX.E.14.

359. As shown for claim 5, Liu teaches a transistor T4 (“driving TFT”).

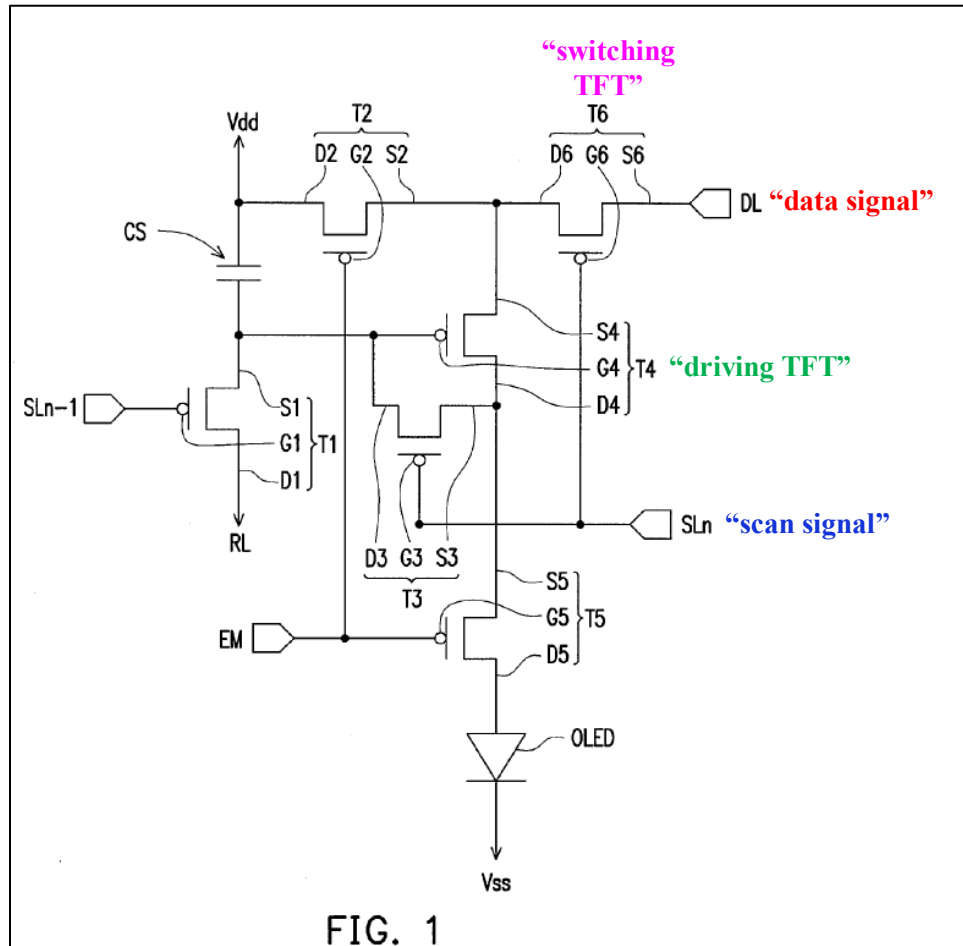
As shown for element 10[d], Liu teaches delivering a data signal via data line DL.

As shown for element 10[c], Liu teaches a scan signal SLn (“scan signal”).

360. Liu teaches “a switching TFT for delivering the data signal to the driving TFT by being turned on by the scan signal.” For example, Liu discloses “[t]he third conductive layer M3 has a source electrode and a drain electrode (not shown) in the region predetermined for forming the sixth thin film transistor T6, the source electrode and the drain electrode are electrically connected to the source region S6 and the drain region D6 respectively, and the source region S6, the drain region D6, the source electrode, the drain electrode and the gate G6 form the sixth thin film transistor T6.” (EX1007, [0069].)

361. Figure 1 (annotated below) shows the source S6 of *transistor T6* coupled to the *data line DL* and the drain D6 coupled to *transistor T4*, thereby delivering the data signal to the transistor T4 when transistor T6 is on. The figure also shows the gate G6 of transistor T6 coupled to the *scan signal SLn*. A POSITA would have understood the scan signal SLn being coupled to the gate G6

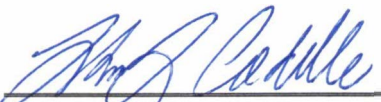
of transistor T4 is “delivering the data signal to the driving TFT by being turned on by the scan signal.”



* * *

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: August 31, 2025


Thomas Credelle

Professional Summary

Mr. Credelle is a recognized expert in the flat panel/touch industry with over 40 years of expertise in all aspects of flat panel displays, LEDs, LED displays, and optics. He has made significant contributions in the areas of R&D, engineering, marketing, and senior management. He has served at an executive level at start-up businesses within major corporations and start-up companies in Silicon Valley and has had extensive interaction with flat panel producers and customers in Japan, Taiwan, Korea and China. Mr. Credelle holds 84 issued US patents in various flat-panel related technologies including display design, display electronics, materials, algorithms, systems, RFID, and optics, with additional pending.

Mr. Credelle is a Fellow of the Society for Information Display and currently consults regarding technology, business, and patent issues involving Flat Panel Display and LED Technology for various clients. He has written expert-analysis reports for private clients on patent portfolios of over 500 patents and has written numerous IPR ITC, and District Court Case reports and has given depositions on many. He has testified at four District Court cases and three ITC Hearings.

Expertise

- Flat Panel Display Technology
- LEDs and LED lighting
- Display electronics
- Electro-optics
- Patent analysis
- Expert witness (reports, testimony)
- TFT and Liquid Crystal Display R&D

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1970	Massachusetts Institute of Technology	M.S., Electrical Engineering Emphasis: Electro-optics and Solid State Physics Thesis: "Optical Properties of High Purity Stannic Oxide"
1969	Drexel University	B.S., Electrical Engineering (Honors Program)

Professional Experience

From: 2008
To: Present
Organization: **TLC Display Consulting**
Title: President
Summary:

- Technical consulting in the field of flat panel displays, LEDs, and display electronics
- Business/patent consulting in the fields of displays, LEDs, optics, new technology

From: 2016
To: 2018
Organization: **RealD**
Title: Acting CEO, RealD Me (2016-2017), Strategic Advisor, RealD 2017-2019)
Summary:

- Business and technical advisor to RealD Intelligent Backlight Business Unit

From: 2012
To: 2016
Organization: **Innova Dynamics, Inc.**, San Francisco, CA
Title: VP, Application Engineering and Device Performance
Summary:

- Primary interface between customer and product engineering
- Testing and qualification of all products
- Business development/technical contact for new opportunities

From: 2008
To: 2018
Organization: **Display Engineering, Inc.** San Jose, CA
Title: Contractor
Summary:

- Design and testing of high-brightness LED backlights for outdoor signage
- Circuit design and thermal analysis of LED light bars
- Developed new methods for passive cooling of LED light sources

From: 2007
To: 2008
Organization: **Puredepth, Inc.**, Redwood City, CA and Auckland, NZ
Title: Senior VP Engineering
Summary:

- Recruited to establish first senior management leadership position for hardware and software engineering related to Puredepth's Multi Layer Display (MLD) technology.
- Rapidly learned details of technology, established new development plans, and supported customer engagements in US, Korea, and Japan.
- Divided time between US and NZ offices, supporting sales/marketing and leading engineering effort.

From: 2001
To: 2007
Organization: **Clairvoyante, Inc**, Cupertino, CA
Title: VP Engineering
Summary:

- Responsible for engineering, product development, product roadmap, marketing of technology that improves resolution and reduces power of color flat panel displays.
- Responsible for applied R&D, IC development, customer training and support for all technology integration programs.
- Creation of new intellectual property to advance adoption of Clairvoyante technology.
- Monthly interaction with leading LCD producers in Taiwan, Korea, Japan; management of all vendors relating to product development (8-10 on-site visits per year).

From: 1999
To: 2001
Organization: **Alien Technology Corporation**, Morgan Hill, CA
Title: VP of Operations
Summary:

- Key member of management team to develop novel technology for nanoblock-IC assembly using fluidic process. Responsible for facilities, manufacturing operations, IT, and HR; managed \$20M construction project for mfg.
- Key contributor to display-related use of Alien manufacturing processes.
- Contributed to patent portfolio for Alien with key inventions in Nanoblock™ IC manufacturing techniques for displays and RFID tags.

From: 1996
To: 1999
Organization: **Motorola**, Flat Panel Display Division, Tempe, AZ
Title: Director, Product Marketing
Summary:

- Responsible for establishing market direction and initial sales approach for new Field Emission Displays (FED) under development within the Division.
- Won potential business for initial small FEDs in industrial and automotive applications.
- Established and managed marketing communications department, creating new brand image for product as well as managing all trade show activities.
- Contributed to product development and spec generation. Generated patent disclosures aimed at solving customer-related issues.

From: 1994
To: 1996
Organization: **Allied Signal**, Los Gatos, CA
Title: Director, Advanced Product Marketing
Summary:

- Responsible for establishing product marketing direction and establishing customer contacts for newly-developed optical films for viewing angle enhancement for LCDs.
- Participated in product development, product improvement based on customer input.

From: 1991
To: 1994
Organization: **Apple Computer**, Cupertino, CA.
Title: Manager, Display Engineering
Summary:

- Responsible for all LCD engineering and qualification for first PowerBook notebook computers introduced to market.
- Extensive interaction with Asian suppliers.
- Generated patent disclosures related to LCD integration in notebook PCs

From: 1986
To: 1991
Organization: **GE** R&D Center, Schenectady, NY
Title: Manager, TFT LCD Research and Development
Summary:

- Managed R&D in TFT and LCD technology for avionics applications. Led the team that built the first 1 million pixel color LCD. Led development of various optical devices based on liquid crystal materials.
- Established photonics effort based on liquid crystal technology.

From: 1970
To: 1986
Organization: **RCA** Sarnoff Labs, Princeton, NJ
Title: Individual Contributor, then Group Manager
Summary:

- Increasing levels of responsibility in the R&D of optical materials and flat panel displays.
- Key contributor to novel methods for large screen flat panel TFT.
- Established TFT LCD Program at Sarnoff Labs in 1983.
- Led development of first polySi TFT LCDs at Sarnoff Labs.

Legal Consulting

Expert Engagement:

Type of Matter: Deposition on patent dispute
Client: Alien Technology
Case Name: Alien v. Avery, Case No. 08-cv-00795
Services Provided: Deposed as expert and inventor on behalf of Alien
Date: October 29, 2008

Expert Engagement:

Type of Matter: Patent Infringement, LCD Projection
Client: McKenna Long & Aldridge LLP
Case Name: Undisclosed
Services Provided: Non-testifying expert on ITC case
Date: November 2011

Expert Engagement:

Type of Matter: LCD backlight
Client: Steptoe and Johnson LLP on behalf of LG
Case Name: In the Matter of Certain Devices for Improving Uniformity Used in a Backlight Module and Products Containing the Same Inv. No. 337-TA-805
Services Provided: Non-testifying expert on ITC case (settled)
Date: November 2011

Expert Engagement:

Type of Matter: Display driving method for eBooks
Client: Klarquist Sparkman LLP on behalf of Amazon (v. Positive Technologies)
Case Name: 2:11-cv-2226, N.D. Calif.
Services Provided: Expert Reports, Testifying Expert (settled)
Date: October 2012 – April 2013

Expert Engagement:

Type of Matter: Display driving method for eBooks
Client: Alston and Bird LLP on behalf of Barnes and Noble (v. Positive Technologies)
Case Name: 3:11-cv-02226-SI
Services Provided: Testifying expert on District Court Case (settled) Non infringement and non-enablement reports written.
Date: March 2013 – July 2013

Expert Engagement:

Type of Matter: LCD driving method
Client: Kenyon and Kenyon LLP on behalf of Sony (v. Surpass)
Case Name: IPR2015-0863
Services Provided: IPR Reports and Deposition
Date: Jan 2015-Mar 2016

Expert Engagement:

Type of Matter: LCD Optics and TFT design
Client: Marc Labgold on behalf of Funai (v. Gold Charm Ltd.)
Case Name: IPR2015-01448
Services Provided: IPR Report
Date: Apr, 2015 – Jul, 2015

Expert Engagement:

Type of Matter: LCD Backlights using LEDs
Client: Shearman & Sterling LLP/Fried Frank LLP on behalf of Mercedes Benz (v. Innovative Display Technologies)
Case Name: IPR2015-01995, IPR2015-01115, IPR2015-01113 and 2: 14-cv-00535 TXEDC
Services Provided: IPR Expert Reports
Date: Mar 2015 – May 2015

Expert Engagement:

Type of Matter: TFT array and LCD panel interconnect
Client: Covington & Burling on behalf of Samsung Display Co. (v. MiiC & Partners)
Case Name: IPR205-01469, IPR2015-01499
Services provided: IPR Expert Reports
Date: May 2015- Mar 2016

Expert Engagement:

Type of Matter: LCD Backlights using LEDs
Client: Mayer Brown on behalf of KJ Pretech (v. Innovative Display Technologies)
Case Name: IPR2015-01866, IPR2015-01867, IPR2015-01868
Services Provided: IPR reports and depositions (3)
Date: Aug 2015-Jun 2016

Expert Engagement:

Type of Matter: LCD backlights using LEDs
Client: Gibson, Dunn, and Crutcher LLP on behalf of Vizio (v. Delaware Display Group LLC)
Case Name: Case No. 13-cv-2112
Services Provided: Non-infringement Report, Deposition, Testifying Expert (settled)
Date: Sep 2015-Mar 2017

Expert Engagement:

Type of Matter: LCD manufacturing, TFT array design
Client: Sughrue Mion PLLC on behalf of TCL
Case Name: Arbitration (Hong Kong) between AUO and TCL
Services Provided: Non-infringement analysis of TFT array design (settled)
Date: Jun 2017 – Sep 2017

Expert Engagement:

Type of Matter: LED display panels
Client: Adduci Mastriani & Schaumberg on behalf of Ultravision Technologies LLC (v. >20 Chinese companies)
Case Name: ITC Case 337-TA-1114
Services Provided: Expert Reports (Invalidity and Non-infringement) and Deposition (3 days)
Date: Jan 2018 – Feb, 2019

Expert Engagement:

Type of Matter: LCD gamma circuit
Client: K&L Gates on behalf of Wistron (v. plaintiff Phenix Longhorn)
Case Name: IPR2018-01255, 2:17 cv-00711 TXEDC
Services Provided: Expert report and Expert Testimony as needed (settled)
Date: May 2018 – Jun 2019

Expert Engagement:

Type of Matter: LED packaging
Client: Davidson, Berquist, Jackson & Gowdey, LLP on behalf of Document Security Systems (v. defendants Seoul Semiconductor, Nichia Corp, Cree, Inc., Everlight Electronics)
Case Name: IPR2018-00966, 2018-01165
Services Provided: Expert Reports, Depositions (2) and Expert Testimony at trial as needed
Date: June 2018 – May 2019

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: Vinson and Elkins on behalf of AUO (v. plaintiff Vista Park Ventures)
Case Name: 2:18 cv-00276, 00278, 00279 TXEDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Dec 2018 – Sep 2019

Expert Engagement:

Type of Matter: LED Display Panels
Client: Fabricant LLP on behalf of Plaintiff Ultravision (v. >10 companies)
Case Name: 2:18 cv-00112, 00118, 00150 TXEDC
Services Provided: Expert report and Expert Testimony as needed; two days deposition in 2020, two depositions in 2021. **Testified at trial May 2021**
Date: Jan 2019 – Present

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: McDermott, Will and Emery on behalf of TCL (v. plaintiff Vista Park Ventures)
Case Name: 2:19 cv-00188, 00189, 00190, 00191 TXEDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Aug 2019 – Oct 2019

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: McDermott, Will and Emery on behalf of GiantPlus (v. plaintiff Vista Park Ventures)
Case Name: 2:19 cv-00183, 00184, 00185, 00187 TXEDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Oct 2019 – Jan, 2020

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: Vincent and Elkins on behalf of JDI (v. plaintiff Vista Park Ventures)
Case Name: 2:19 cv-00323, 00324, 00325 TXEDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Nov 2019 – Jun 2020

Expert Engagement:

Type of Matter: TFT-LCD technology
Client: Sidley on behalf of LG Electronics (v. defendant Hisense)
Case Name: 2:19 cv-09474 CACDC
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Feb. 2020 – Jan. 2021

Expert Engagement:

Type of Matter: Quantum dot technology
Client: Murtha Law on behalf of RPI (v. defendant Samsung)
Case Name: 2:19 cv-20097 KM-ESK
Services Provided: Expert reports and Expert Testimony as needed
Date: Jan. 2020 – Jun 2021

Expert Engagement:

Type of Matter: OLED, touch panels
Client: RAK Law on behalf of Solas (v. defendant Samsung)
Case Name: 2:19-cv-00152-JRG (E.D. Tex)
Services Provided: Expert reports and Expert Testimony; two depositions in 2020.
Testified at trial Mar. 2021.
Date: Apr. 2020 – Mar. 2021

Expert Engagement:

Type of Matter: LCD technology
Client: Morgan Lewis on behalf of Fuji Film (v. plaintiff Vista Park Ventures)
Case Name: 2:20 cv-00064, 65, 66 E.D. Tex.
Services Provided: Expert reports and Expert Testimony as needed (settled)
Date: Jul. 2020 – Oct 2020

Expert Engagement:

Type of Matter: Touch panels
Client: DLA Piper, Alston and Bird, on behalf of Microsoft, Dell (v. plaintiff Neodron)
Case Name: 2:19-cv-00318-ADA (W.D. Tex)
Services Provided: Expert Reports and Expert Testimony as needed (settled)
Date: Aug. 2020 – Nov. 2020

Expert Engagement:

Type of Matter: LCD
Client: Vincent and Elkins on behalf of Japan Display Inc (v. defendant Tianma)
Case Name: 2:20-CV-00283, 284, 285-JRG (E.D. Tex)
Services Provided: Expert Reports, depositions, and Expert Testimony as needed (settled)
Date: Jan 2021 – Jan 2022

Expert Engagement:

Type of Matter: LCD
Client: Perkins Coie on behalf of Truly Semiconductor, Hannstar (v. plaintiff Vista Park Ventures)
Case Name: 2:20-CV-250, 251, 252 (E.D. Tex)
Services Provided: Expert Reports and Expert Testimony as needed (settled)
Date: Jan 2021 – June 2021

Expert Engagement:

Type of Matter: Quantum dots
Client: Mintz on behalf of Nanoco (v. defendant Samsung)
Case Name: 2:20-CV-00038-JRG (E.D. Tex)
Services Provided: Expert Reports, depositions, case settled day before trial opening arguments
Date: Jan 2021 – Jan 2023

Expert Engagement:

Type of Matter: OLED circuits
Client: Morrison Forster on behalf of JOLED (v. defendant Samsung)
Case Name: Case No. 6:20cv559 (W.D. Tex.)
Services Provided: Expert Reports and Expert Testimony (settled)
Date: July 2020 – April 2021

Expert Engagement:

Type of Matter: OLED circuits
Client: Perkins Coie on behalf of AUO (v. defendant Samsung)
Case Name: TBD
Services Provided: Expert Reports and Testimony (settled)
Date: Feb. 2021 – May 2021

Expert Engagement:

Type of Matter: LED circuits
Client: Kim IP on behalf of CAST Lighting (v. Plaintiff WAC Lighting)
Case Name: ITC Inv. No. 337-TA-1261
Services Provided: Expert Reports and Testimony (settled)
Date: May 2021 – Oct 2021

Expert Engagement:

Type of Matter: OLED circuits
Client: RAKLaw on behalf of Solas, Ltd. (v. Defendant Samsung)
Case Name: ITC Inv. No. 337-TA-1243
Services Provided: Expert Reports and **Testified at Hearing Nov. 15-19, 2021**
Date: May 2021 – Dec 2021

Expert Engagement:

Type of Matter: OLED circuits
Client: PV Law on behalf of TCL (vs. Plaintiff SEL Co.)
Case Name: 8:21-cv-00554-JAK-ADS (CDCA)
Services Provided: Expert Reports and Depositions; case settled
Date: July 2021 – July 2023

Expert Engagement:

Type of Matter: LED circuits
Client: Carmichael IP on behalf of Lynk Labs (vs. defendant Samsung)
Case Name: IPR Proceedings
Services Provided: Expert Reports and Depositions, case settled.
Date: Jan 2022 – Jan 2023

Expert Engagement:

Type of Matter: OLED circuits
Client: Baker Botts on behalf of FujiFilm (vs. defendant ButterflyQ)
Case Name: C.A. No. 22-309-JPM
Services Provided: Expert Reports and Depositions, testify at trial if needed (settled Nov, 2023)
Date: Jul 2022 – Nov. 2023

Expert Engagement:

Type of Matter: Outdoor LCD signage
Client: Kilpatrick Townsend on behalf of MRI, Inc. (vs. defendants Samsung et al)
Case Name: ITC 337-TA-1331
Services Provided: Expert Reports, Depositions, **Testified at Hearing June 26-30, 2023**
Date: Oct 2022 – Aug 2023

Expert Engagement:

Type of Matter: OLED circuits and pixel arrangements
Client: Orrick Herrington & Sutcliffe LLP on behalf of BOE (vs. plaintiff Samsung et al)
Case Name: ITC 337-TA-1351
Services Provided: Expert Reports, Depositions. **Testified at Hearing July 16, 2024**
Date: Sep 2023 – Sept 2024

Expert Engagement:

Type of Matter: Light concentrators, LCD backlights
Client: Katz PLLC on behalf of SVV (vs. defendants Asus and Acer)
Case Name: WD Tex 6:22-cv-0311, 312, 313, 511, 512, 513, 639, 640, 641-ADA
Services Provided: Expert Reports, Depositions, **testified at trial (v. Acer), June, 2024; testified at trial (v. ASUS), Sept, 2024**
Date: Jan 2023- Oct 2024 (Plaintiff won in both trials)

Expert Engagement:

Type of Matter: LCD AMOLED circuits,
Client: Kramer Alberti on behalf of Polaris PowerLED Technologies, LLC (vs. defendant Samsung et al)
Case Name: EDTEX 2:22-cv-oo469-JRG
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert (trial scheduled for Jan 2025)
Date: Mar 2023- Dec 2024 (settled)

Expert Engagement:

Type of Matter: LCD AMOLED circuits,
Client: Morrison & Forester LLP on behalf of Crystal Leap (vs. defendant HKC)
Case Name: No. 2:22-cv-00382 (EDTEX)
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert, settled Mar, 2024
Date: Jul 2023- Mar 2024 (settled)

Expert Engagement:

Type of Matter: LCD AMOLED circuits,
Client: Kramer Alberti on behalf of Polaris PowerLED Technologies, LLC (vs. various defendants)
Case Name: 2:23-cv-03478-GW-PD (CD CAL)
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert
Date: Dec 2023- present

Expert Engagement:

Type of Matter: Image sensor circuits,
Client: PVLaw on behalf of Keyence (vs. plaintiff AI Core Technologies, LLC)
Case Name: 2:24-cv-00438-RWS-RSP,
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert
Date: Dec 2023- Nov 2024 (settled)

Expert Engagement:

Type of Matter: AMOLED design, circuits
Client: Morrison & Forester LLP on behalf of BOE (vs. Plaintiff SDC)
Case Name: No. 2:25-cv-00430 (E.D. Tex.), *Samsung Display Co., Ltd. v. BOE Technology Group Co., Ltd. et al.*, No. 2:23-cv-00426 (E.D. Tex.)
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert
Date: Jun 2025 - present

Expert Engagement:

Type of Matter: AMOLED design, circuits
Client: Orrick on behalf of BOE
Case Name: Not yet assigned
Services Provided: Expert Reports (IPR and DC), Depositions, testifying expert
Date: May 2025 - present

Consulting Projects

Consulting Engagement:

Client: Tessera
Services Provided: Business case analysis for M&A department
Date: Mar 2008 to 2011

Consulting Engagement:

Client: Sipix Imaging
Services Provided: Technical consulting on display algorithms
Date: Mar 2008 to 2009

Consulting Engagement:

Client: Holox Technologies, Inc. (self-funded start up in holographic optics)
Services Provided: CEO; business leadership, fund raising, market analysis, optical design of advanced diffusers for LCD backlights, solar collectors, window films.
Date: Sept 2008 to June 2012

Consulting Engagement:

Client: Innova Dynamics, Inc.
Services Provided: Technical and business development consulting in touch screen technology
Date: October 2011 to November 2012

Technical and Patent Consulting:

Client: LG Display
Services Provided: Technical consulting on pixel processing algorithms, OLED displays; patent generation for advanced pixel concepts for OLED.

Date: Aug 2009 to Dec 2011

Consulting Engagement:

Client: Scivax

Services Provided: Technical and business development consulting in nanoimprinting technology

Date: Feb 2018 to Jul 2018

Professional Affiliations, Achievements & Awards

- Fellow of the Society for Information Display (SID)
- Past Director, SID Symposium Committee (10 years)
- Conference and Program Chair, SID Symposium and IDRC
- Past Member, SID Program Committee (15 years)

US Patents & Publications

<u>Patent</u>	<u>Date</u>	<u>Description</u>
10,163,985	12/25/2018	Subpixel arrangement structure for a display device
9,583,034	02/28/2017	Subpixel arrangement structure for a display device
9,041,625	05/26/2015	Subpixel arrangement structure for a display device and display device
9,001,167	04/07/2015	Display panel having crossover connections effecting dot inversion
8,933,959	01/13/2015	Subpixel layouts and subpixel rendering methods for directional displays and systems
8,876,937	11/04/2014	Production of nanostructures
8,797,344	08/05/2015	Memory structures for image processing
8,754,913	06/17/2014	Subpixel arrangement structure of display device
8,704,744	04/22/2014	Systems and methods for temporal subpixel rendering of image data
8,633,886	01/21/2014	Display panel having crossover connections effecting dot inversion
8,519,910	08/27/2013	Image processing method and display device using the same
8,516,683	08/27/2013	Methods of making a radio frequency identification (RFID) tags
8,456,496	06/04/2013	Color flat panel display sub-pixel arrangements and layouts for sub-pixel rendering with split blue sub-pixels
8,456,414	06/04/2013	Gamma adjustment with error diffusion for electrophoretic displays
8,436,799	05/07/2013	Image degradation correction in novel liquid crystal displays with split blue subpixels
8,421,820	04/16/2013	Methods and systems for sub-pixel rendering with adaptive filtering
8,411,022	04/02/2013	Multiprimary color display with dynamic gamut mapping
8,405,692	03/26/2013	Color flat panel display arrangements and layouts with reduced blue luminance well visibility
8,378,947	02/19/2013	Systems and methods for temporal subpixel rendering of image data
8,294,741	10/23/2012	Four color arrangements of emitters for subpixel rendering
8,259,127	09/04/2012	Systems and methods for reducing desaturation of images rendered on high brightness displays
8,144,094	03/27/2012	Liquid crystal display backplane layouts and addressing for non-standard subpixel arrangements

8,134,583	03/13/2012	Two color flat panel display sub-pixel arrangements and layouts for sub-pixel rendering with split blue sub-pixels
8,035,599	10/11/2011	Display panel having crossover connections effecting dot inversion
8,018,476	09/13/2011	Subpixel layouts for high brightness displays and systems
8,013,867	09/06/2011	Systems and methods for implementing improved gamut mapping algorithms
7,969,456	06/28/2011	Methods and systems for sub-pixel rendering with adaptive filtering
7,876,341	06/25/2011	Subpixel layouts for high brightness displays and systems
7,864,194	01/04/2011	Systems and methods for motion adaptive filtering
7,791,679	09/07/2010	Alternative thin film transistors for liquid crystal displays
7,755,652	07/13/2010	Color flat panel display sub-pixel rendering and driver configuration for sub-pixel arrangements with split sub-pixels
7,701,476	04/20/2010	Four color arrangements of emitters for subpixel rendering
7,646,430	01/12/2010	Display system having improved multiple modes for displaying image data from multiple input source formats
7,592,996	09/22/2009	Multiprimary color display with dynamic gamut mapping
7,583,279	09/01/2009	Subpixel layouts and arrangements for high brightness displays
7,573,493	08/11/2009	Four color arrangements of emitters for subpixel rendering
7,573,448	08/11/2009	Dot inversion on novel display panel layouts with extra drivers
7,559,131	07/14/2009	Method of making a radio frequency identification (RFID) tag
7,505,053	03/17/2009	Subpixel layouts and arrangements for high brightness displays
7,492,379	02/17/2009	Color flat panel display sub-pixel arrangements and layouts for sub-pixel rendering with increased modulation transfer function response
7,417,648	08/26/2008	Color flat panel display sub-pixel arrangements and layouts for sub-pixel rendering with split blue sub-pixels
7,397,455	07/08/2008	Liquid crystal display backplane layouts and addressing for non-standard subpixel arrangements
7,283,142	10/16/2007	Color display having horizontal sub-pixel arrangements and layouts
7,260,882	08/28/2007	Methods for making electronic devices with small functional elements supported on a carriers
7,248,271	07/24/2007	Sub-pixel rendering system and method for improved display viewing angles
7,218,301	05/15/2007	System and method of performing dot inversion with standard drivers and backplane on novel display panel layouts
7,187,353	03/06/2007	Dot inversion on novel display panel layouts with extra drivers
7,184,066	02/27/2007	Methods and systems for sub-pixel rendering with adaptive filtering
7,167,186	01/23/2007	Systems and methods for motion adaptive filtering
7,084,923	08/01/2006	Display system having improved multiple modes for displaying image data from multiple input source formats
7,068,287	06/27/2006	Systems and methods of subpixel rendering implemented on display panels
7,046,256	05/16/2006	System and methods of subpixel rendering implemented on display panels
6,985,361	01/10/2006	Electronic devices with small functional elements supported on a carrier
6,917,368	07/12/2005	Sub-pixel rendering system and method for improved display viewing angles

6,816,380	11/09/2004	Electronic devices with small functional elements supported on a carrier
6,731,353	05/04/2004	Method and apparatus for transferring blocks
6,693,384	02/17/2004	Interconnect structure for electronic devices
6,606,247	08/12/2003	Multi-feature-size electronic structures
5,961,362	10/05/1999	Method for in situ cleaning of electron emitters in a field emission device
5,883,467	03/16/1999	Field emission device having means for in situ feeding of hydrogen
5,477,350	12/19/1995	Interferometric spatial switch for polarized or unpolarized light using liquid crystal
5,373,393	12/13/1994	Optical interferometric device with spatial light modulators for switching substantially coherent light
5,363,228	11/08/1994	Optical device with spatial light modulators for switching arbitrarily polarized light
5,345,321	09/06/1994	Compact polarization dependent optical switching units
5,319,477	06/07/1994	Compact polarization independent optical switching units
5,317,445	05/31/1994	Optical device with spatial light modulators for switching polarized light
4,630,893	12/23/1986	LCD pixel incorporating segmented back-to-back diode
4,598,227	07/01/1986	Electron beam convergence and scanning structures for flat panel display device
4,517,489	05/14/1985	Modulator structure and method for flat panel display devices
4,484,103	11/20/1984	Color selection electron beam guide assembly for flat panel display devices
4,362,966	12/07/1982	Electron leakage reduction in flat panel display devices
4,335,332	06/15/1982	Focus mesh structure and biasing technique for flat panel display devices
4,316,118	02/16/1982	Guided beam display device
4,298,819	11/03/1981	Beam Clean up structure for flat panel display devices
4,234,815	11/18/1980	Flat display tube having shielding member between beam guide and screen
4,174,881	11/20/1979	Recording a synthetic focused-image hologram on a thermally deformable plastic
4,153,856	05/08/1979	Proximity focused element scale image display device
4,148,636	04/10/1979	Broadening the spatial frequency pass band of a thermoplastic layer
4,137,478	01/30/1979	Color flat panel television
4,137,077	01/30/1979	Broadening the spatial frequency pass band of a thermoplastic layer
4,131,823	12/26/1978	Modular flat display device with beam convergence
4,121,137	10/17/1978	System for achieving image uniformity in display devices
4,103,205	07/25/1978	Flat display device with beam guide
4,103,204	07/25/1978	Flat display device with beam guide
4,088,920	05/09/1978	Flat display device with beam guide

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1. “Thermoplastic Media for Holographic Recording,” RCA Review: A Technical Journal (1972)
2. “Guided Beam Displays for Large Screen Flat-Panel Color TV,” Information Display (1983)
3. “Recent trends in color avionic LCDs,” Information Display (1987)
4. “Thin-film transistors for video applications,” Inter. Display Research Conference Record (1988)
5. “TFT-LCD for video applications,” Information Display (1989)
6. “LCDs,” JTEC Panel Report on Display Technologies in Japan (1992)
7. “Viewing-Angle-Enhancement System for LCDs” SID Digest of Technical Papers (1995)
8. “SpectraVue™: A new system to enhance the viewing angle of LCDs,” SID Journal (1997)
9. “The Business Case for Motorola's Flat-Panel-Display Division,” Information Display (1997)
10. “MTF of high-resolution PenTile Matrix™ displays,” Proc Eurodisplay (2002)
11. “Adding a White Subpixel,” Information Display (2005)
12. “Low Power, High-Pixel-Density Mobile Displays Using PenTile RGBW™ Architectures,” SID Mobile Displays Digest of Technical Papers (2006)
13. “*Invited Paper*: High-Pixel-Density Mobile Displays: Challenges and Solutions,” SID Digest of Technical Papers (2006)