

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Patent No. 9,299,730

Inter Partes Review No. IPR2025-01499

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

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Exhibit List

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U.S. Patent No. 9,299,730	1001
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Prosecution History of U.S. Patent No. 9,299,730	1003
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U.S. Publication No. 2002/0118150 to Kwon	1006
U.S. Publication No. 2012/0313100 to Liu	1007
U.S. Publication No. 2011/0128211 to Ono	1008
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U.S. Publication No. 2008/0186423 to Ishii	1015
U.S. Patent No. 8,097,882 to Park	1016
U.S. Patent No. 6,963,173 to Kawachi	1017
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Petitioner BOE Technology Group Co., Ltd. (“Petitioner” or “BOE”) respectfully petitions for *inter partes* review of claims 1-19 of U.S. Patent No. 9,299,730 (“the ’730 patent” (EX1001)) in accordance with 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq.*

I. INTRODUCTION

The ’730 patent is directed to a TFT array substrate comprising a capacitor having an upper electrode that overlaps with the whole lower electrode. This overlap accounts for an overlay deviation between the electrodes due to misalignment of the masks during fabrication of the display device. (EX1001, 1:35-40.) If not accounted for, the actual capacitance differs from the target capacitance, causing issues such as “low-gradation spots, abnormal colors, or the like.” (EX1001, 1:40-45.)

The prior art shows that issues with overlay deviation and the solution of creating an overlap in the capacitor electrodes were known before the ’730. For example, Ishii describes a margin between masks during fabrication that needs to be accounted for with decreased capacitor area. Ishii’s upper electrode overlaps with the whole lower electrode and includes an opening in the upper electrode for a self-alignment contact hole. Liu similarly discloses an OLED display comprising a capacitor having an upper electrode overlapping the whole lower electrode.

Petitioner submits the challenged claims are unpatentable for the reasons set

forth in this petition, as supported by Thomas Credelle (EX1002).

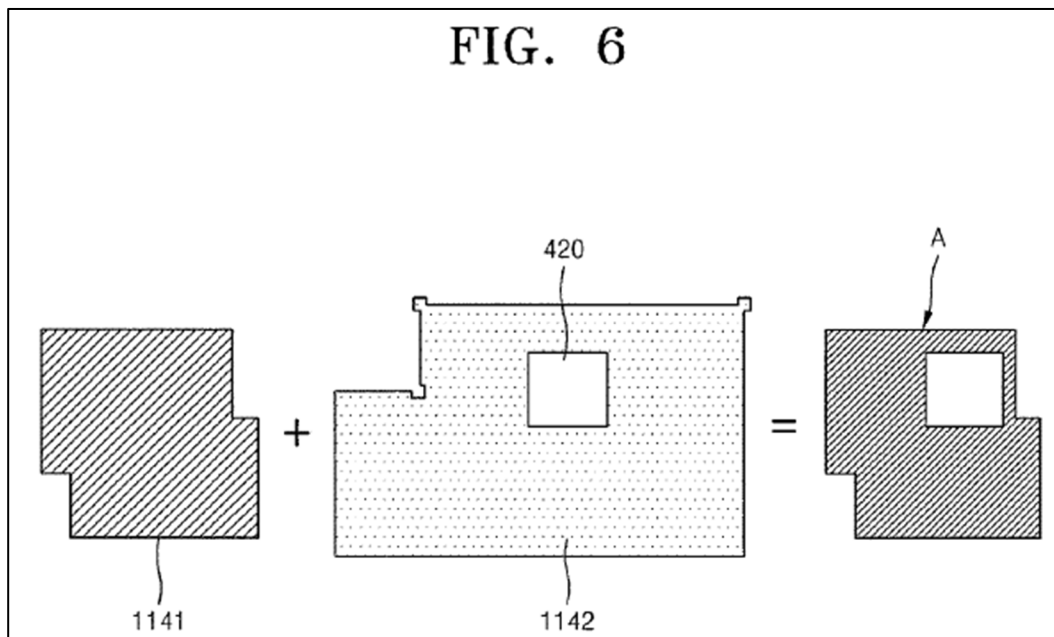
II. SUMMARY OF THE '730 PATENT

The '730 patent discloses a TFT array substrate for an OLED display comprising a capacitor having lower and upper electrodes. (EX1001, 1:49-54.)

The '730 specification explains “the present invention provide[s] a thin film transistor (TFT) array substrate including a storage capacitor structure for maintaining a capacitance to be substantially constant even though an overlay deviation occurs, and an organic light-emitting diode (OLED) display employing the same.” (EX1001, 1:49-54; EX1002, ¶¶19-25.)

“[T]he upper electrode 1142 is arranged to overlap with the whole lower electrode 1141 and has a storage opening 420.” (EX1001, 7:13-15.) Figure 6 (below) shows the upper electrode 1142, lower electrode 1141, and opening 420.

“[T]he whole lower electrode and an upper electrode of a storage capacitor overlap each other.” (EX1001, 12:30-32.) “[T]hus even though an overlay deviation occurs between the two electrodes, a capacitance may be maintained (e.g., always maintained) to be substantially constant. Accordingly, low-gradation spots and abnormal colors due to a capacitance change may be prevented.” (EX1001, 12:32-38; EX1002, ¶20.)



A. Effective Filing Date

The '730 patent was filed on March 13, 2013, published on March 20, 2014, issued on March 29, 2016, and claims priority to a Korean application filed on September 19, 2012. For purposes of this petition only, Petitioner relies on September 19, 2012 as the earliest effective filing date. (EX1002, ¶18.)

B. Prosecution History

During prosecution, the Examiner only issued two Office Actions. The February 4, 2015 Non-Final Office Action, rejected claims 1, 2, 10, and 11 as anticipated by Lee (U.S. Pub. No. 2012/0146004) (EX1009). The Examiner indicated claims 3-9 and 13-19 were allowable, but objected to for being dependent upon a rejected base claim. (EX1003, 82; EX1002, ¶26.)

In response, Applicant added “the upper electrode extending beyond an edge

of the lower electrode” to the claims and argued Lee’s second electrode 53 (“upper electrode”) of the capacitor does not overlap with the whole first electrode 51a (“lower electrode”). (EX1003, 58, 65.) Applicant rewrote claims 3, 5, 12, and 14 in independent form by including limitations from claims 1 and 10. (EX1003, 59-63, 69; EX1002, ¶27.)

The August 25, 2015 Final Office Action rejected claims 1, 2, 10, and 11 over Eom (U.S. Pub. No. 2013/0063330) (EX1010) in view of Lee. (EX1003, 39-43.) The Examiner again indicated claims 3-9 and 12-19 were allowable. (EX1003, 43; EX1002, ¶28.)

Applicant responded on October 26, 2015 by arguing Eom was not prior art because it was subject to common ownership. (EX1003, 32; EX1002, ¶29.)

The Examiner then issued a Notice of Allowance, stating the prior art of record does not anticipate, teach, or suggest nearly all of the limitations of the claims (except “a substrate” and “a first insulation layer on the substrate”). (EX1003, 14-15; EX1002, ¶30.)

C. Level Of Ordinary Skill In The Art

A person of ordinary skill in the art (POSITA) in the field of the ’730 patent would have a bachelor’s degree in electrical engineering or materials science, including OLED displays, or an equivalent level of skill, knowledge, and experience. This POSITA would have been aware of and generally knowledgeable

about OLED materials, and display pixel design, layout, and operation. (EX1002, ¶¶36-38.)

III. CLAIM CONSTRUCTION

For purposes of this petition only, Petitioner does not believe any terms require a form construction. Each term carries its “ordinary and customary meaning” (“the meaning that the term would have to a person of ordinary skill in the art in question” at the time of the invention). *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (citation omitted); (EX1002, ¶¶39-40.)

IV. PRECISE REASONS FOR RELIEF REQUESTED

Pursuant to 37 C.F.R. § 42.104(b), Petitioner requests cancellation of the challenged claims based on the following references (EX1002, ¶¶41-47):

Prior Art	Abbreviation	Date	Prior Art Under §
U.S. 2007/0058100	Ishii100 (EX1004)	March 15, 2007 (published)	102(b)
U.S. 2008/0186423	Ishii423 (EX1015)	August 7, 2008 (published)	102(b)
U.S. 2003/0141811	Park (EX1005)	July 31, 2003 (published)	102(b)
U.S. 2002/0118150	Kwon (EX1006)	August 29, 2002 (published)	102(b)
U.S. 2012/0313100	Liu (EX1007)	February 2, 2012 (filed)	102(e)
U.S. 2011/0128211	Ono (EX1008)	June 2, 2011 (published)	102(b)

The statutory grounds (pre-AIA) for the challenge of each claim are:

Ground	35 U.S.C. §	Claim(s)	Prior Art Reference(s)
1	103	1, 2	Ishii100
2	103	1, 2	Ishii100, Ishii423
3	103	3-5, 10-14	Park, Ishii100
4	103	6-9, 15-19	Park, Ishii100, Kwon
5	103	1-6, 8, 10-19	Liu, Ono

Below, Petitioner discusses why the challenged claims are unpatentable under the statutory grounds raise, including how and where the prior art satisfies each limitation of each challenged claim, as required by 37 C.F.R. § 42.104(b)(4). Petitioner’s showing establishes a reasonable likelihood it will prevail on each ground of unpatentability to each challenged claim.

V. GROUND 1: ISHII100 RENDERS OBVIOUS CLAIMS 1 AND 2

A. Summary Of Ishii100

Ishii100 is directed to an “electro-optical device” (*e.g.*, “organic EL display”) “having a storage capacitor of increased area, and enabling high-definition image display, a manufacturing method thereof, an electronic apparatus, and a capacitor.” (EX1004, [0007], [0097]; EX1002, ¶48.)

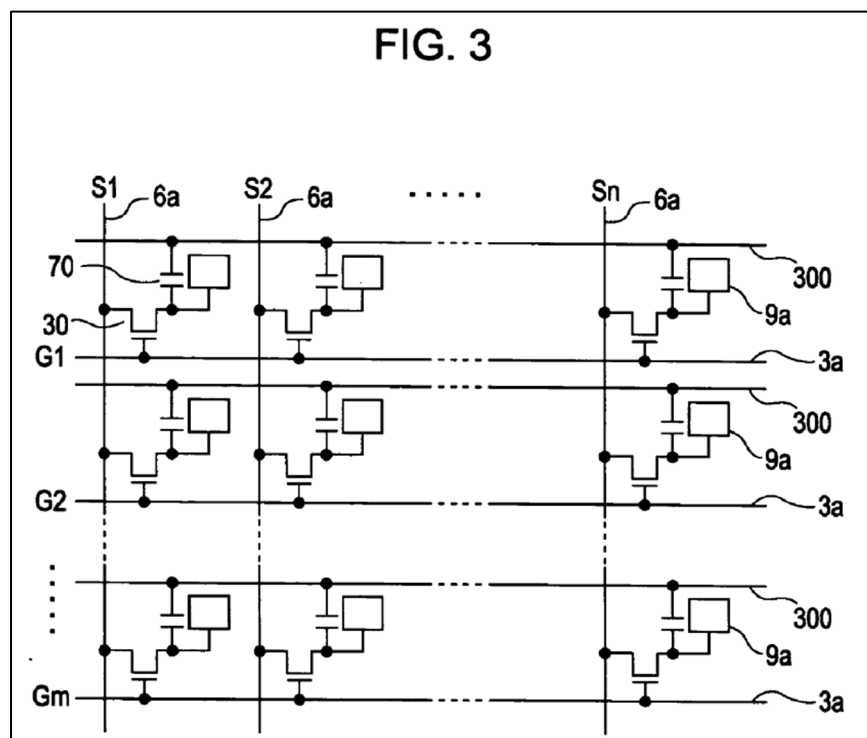
Ishii100 explains “the capacity of the storage capacitor in the pixel portion may be lowered and display unevenness may occur” because “it is necessary to ensure and design a margin in consideration of the between the two kinds of

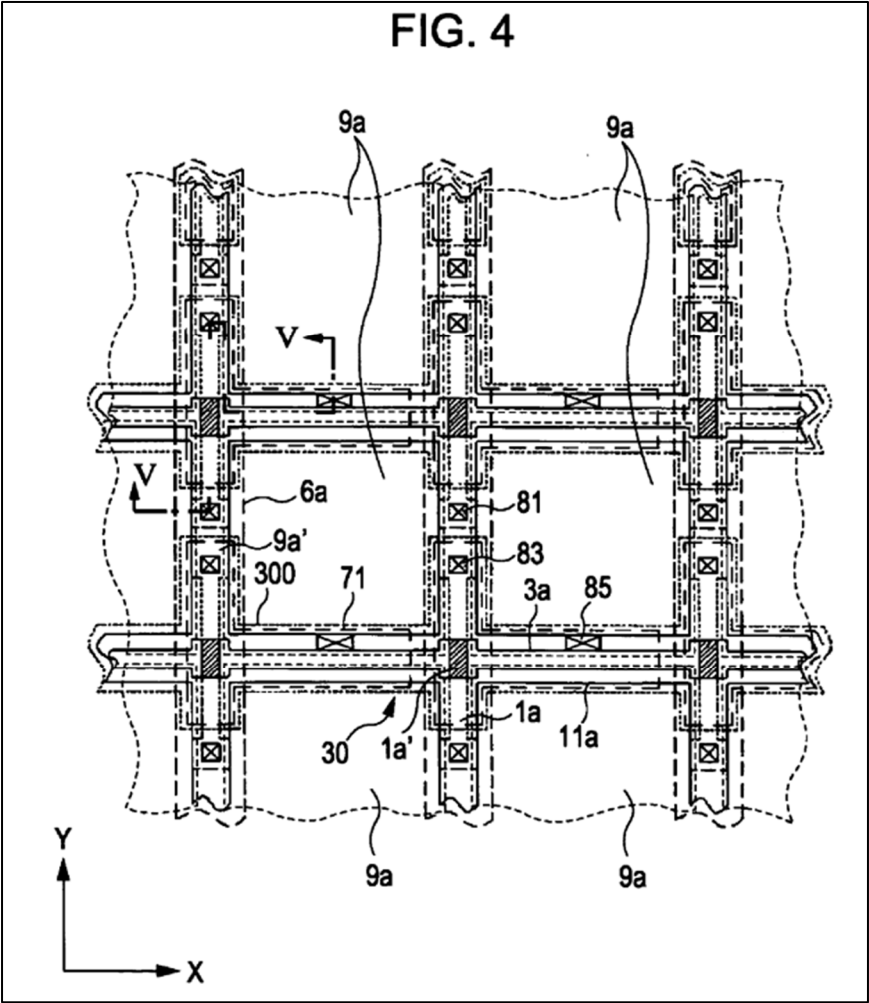
mask.” (EX1004, [0006].) Accordingly, the storage capacitor area is decreased to provide sufficient margin to account for the masks and to ensure proper alignment.

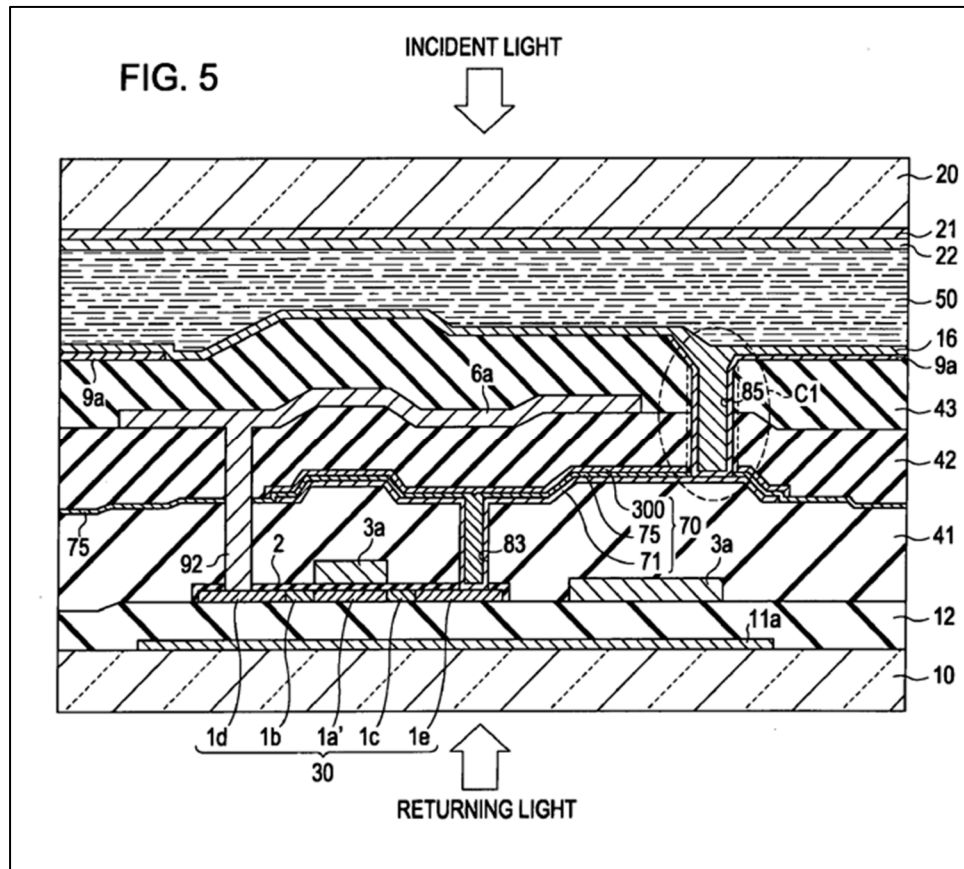
(*Id.*; EX1002, ¶49.)

Ishii100’s electro-optical device comprises a storage capacitor 70, which includes a relay layer 71 (pixel-potential side capacitor electrode) and a part of a capacitor line 300 (fixed-potential-side capacitor electrode) with a dielectric film 75 therebetween. (EX1004, [0056].) It comprises “a pixel-switching thin-film transistor” (TFT) that applies a data signal from a data line to a pixel electrode selected by a scanning line. (EX1004, [0009]; EX1002, ¶¶50-51.)

Figures 3-5 (below) show the circuit, plan view, and cross-sectional view, respectively, of Ishii100’s electro-optical device. (EX1002, ¶¶52-54.)







1. Claim 1

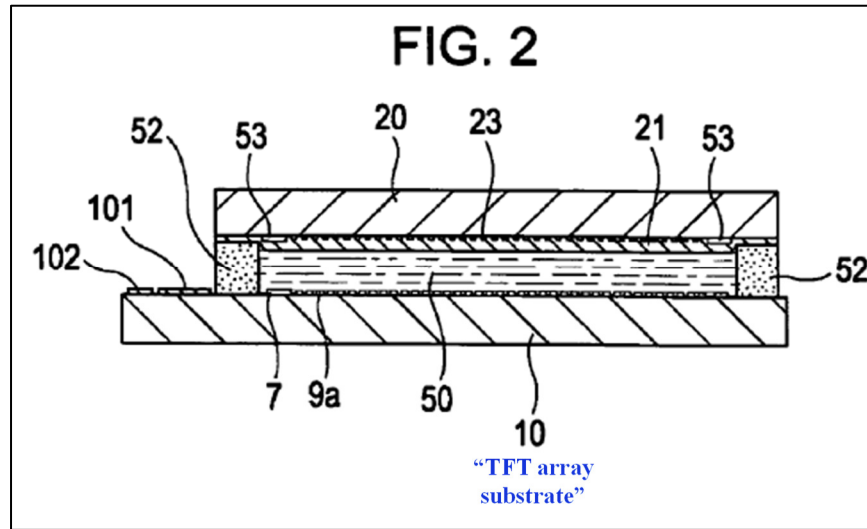
- a. **Preamble: “A thin film transistor (TFT) array substrate comprising:”**

To the extent the preamble is limiting (which Petitioner does not concede), Ishii100 teaches the preamble.

Ishii100 discloses “a **TFT array substrate 10**” (Figure 2¹ (below)). (EX1004, [0041].) Ishii100’s “pixel-switching TFTs (Thin-Film Transistors) [] are driver elements, ... formed on the TFT array substrate 10.” (EX1004, [0044];

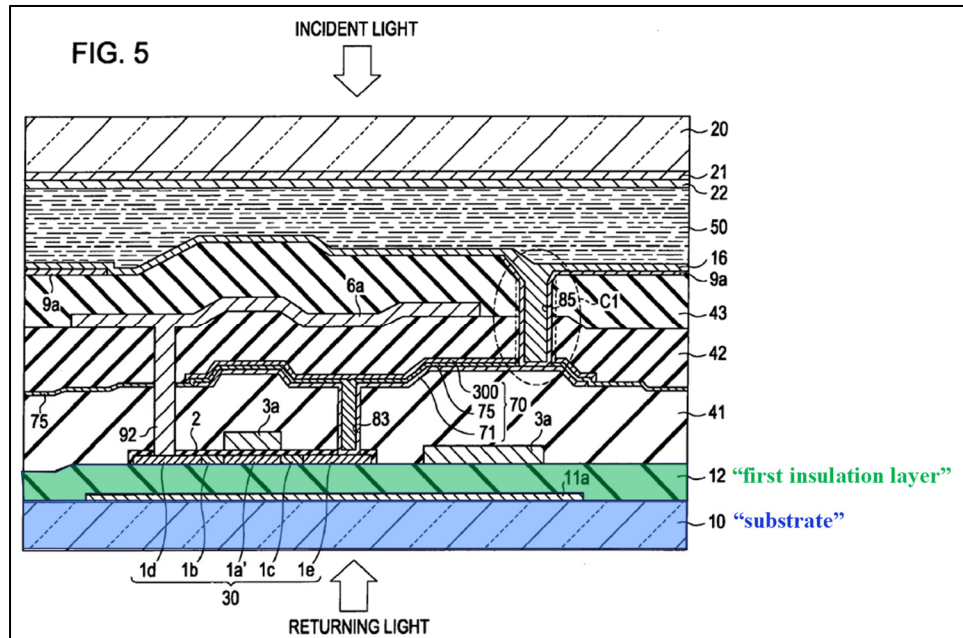
¹ All emphasis and annotations (in color) added, unless otherwise noted.

EX1002, ¶55.)



b. 1[a]: “a substrate;”

Ishii100 discloses “[a]s shown in FIG. 5 [(below)], the liquid crystal device ... includes a transparent TFT array *substrate 10* and a transparent counter substrate 20 arranged to face the array substrate.” (EX1004, [0053]; EX1002, ¶¶56-57.)

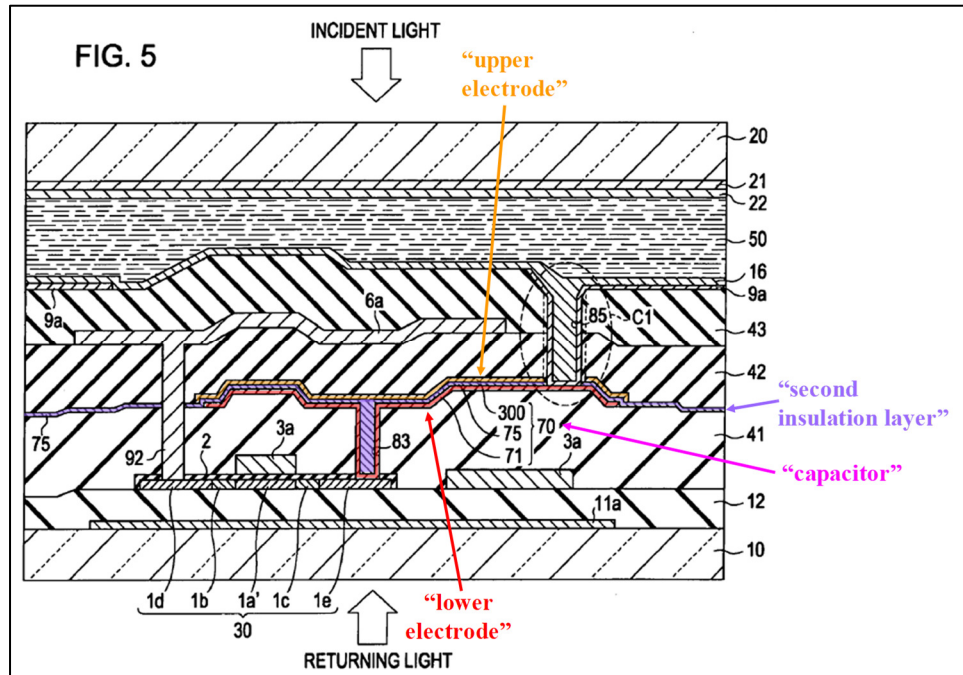
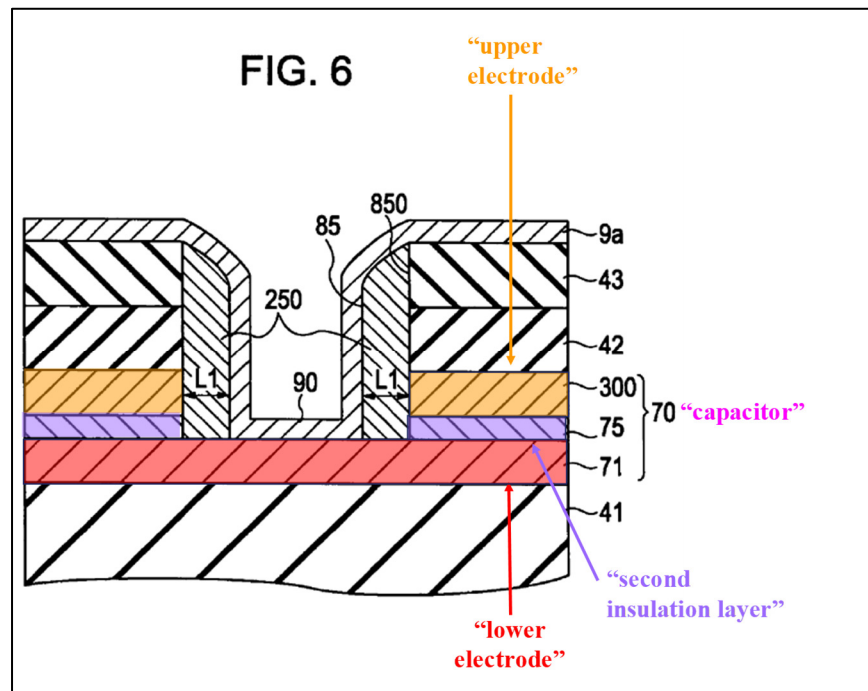


- d. 1[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

Ishii100’s “*storage capacitor 70* is formed by arranging a *relay layer 71* as a *pixel-potential side capacitor electrode*, which is connected to the highly doped drain region 1e and the pixel electrode 9a” and “a part of a *capacitor line 300* as a *fixed-potential-side capacitor electrode* so that they face each other *with a dielectric film 75 therebetween*.” (EX1004, [0056]; also [0068]; EX1002, ¶61.)

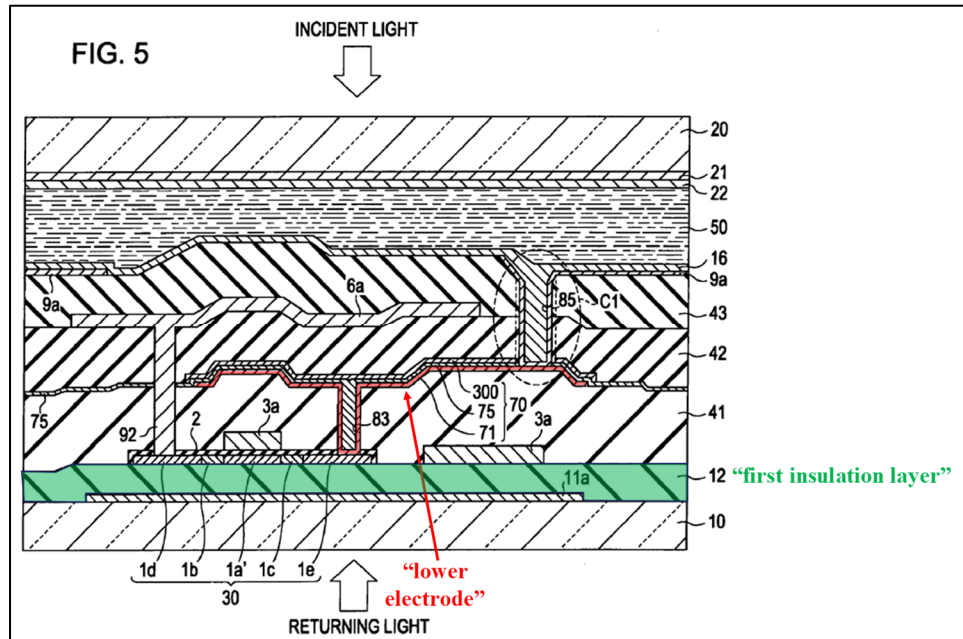
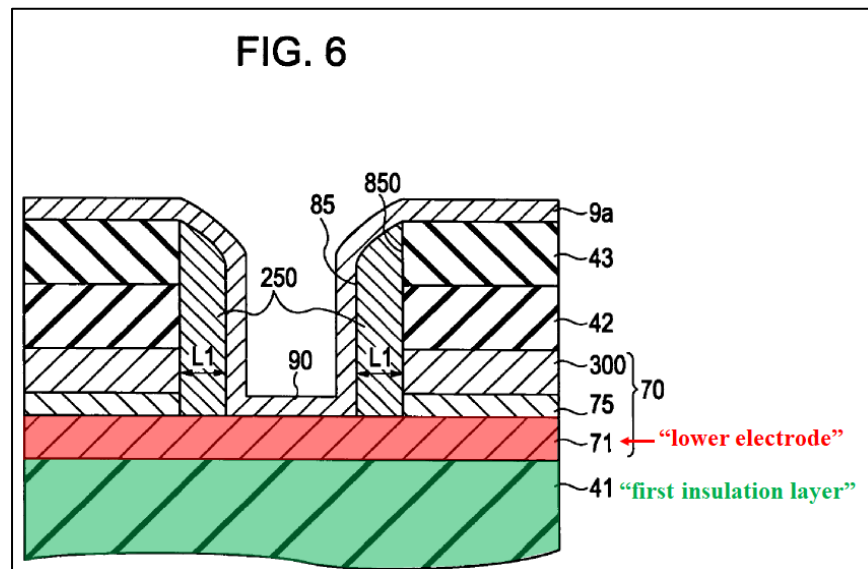
Figures 5 and 6 (below) show *capacitor 70* comprising a *relay layer 71* and a *capacitor line 300*, where the capacitor line 300 is insulated from the relay layer

71 by a *dielectric film 75*. (EX1002, ¶62.)



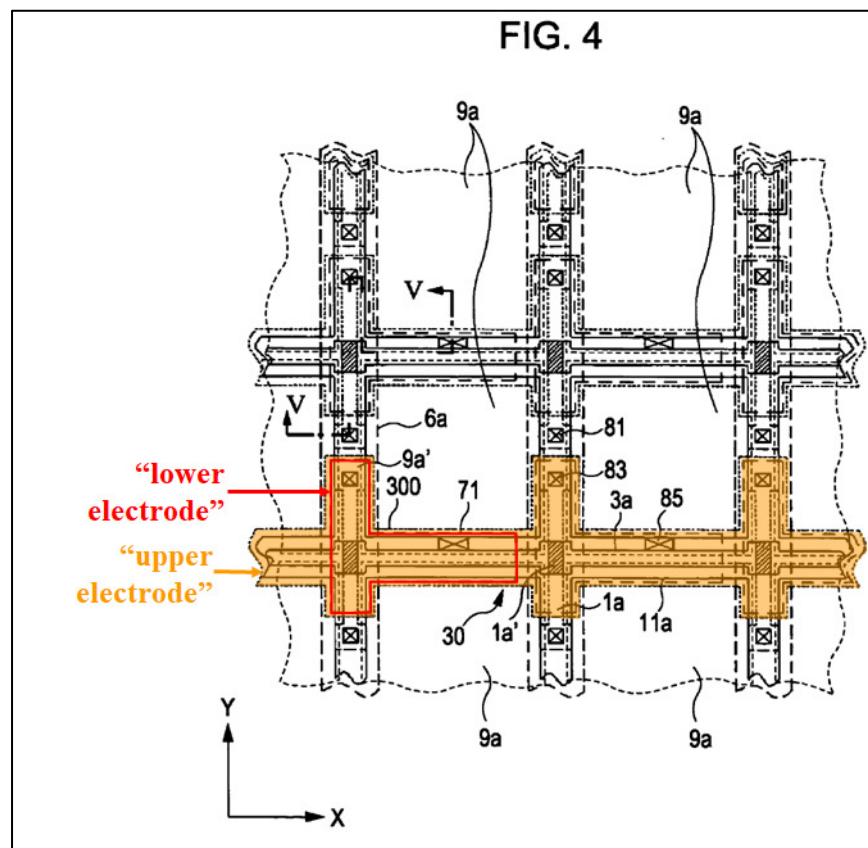
Figures 5 and 6 (below) show Ishii100's *relay layer 71* ("lower electrode") on the *insulating film 12* and *interlayer insulating film 41* ("first insulation

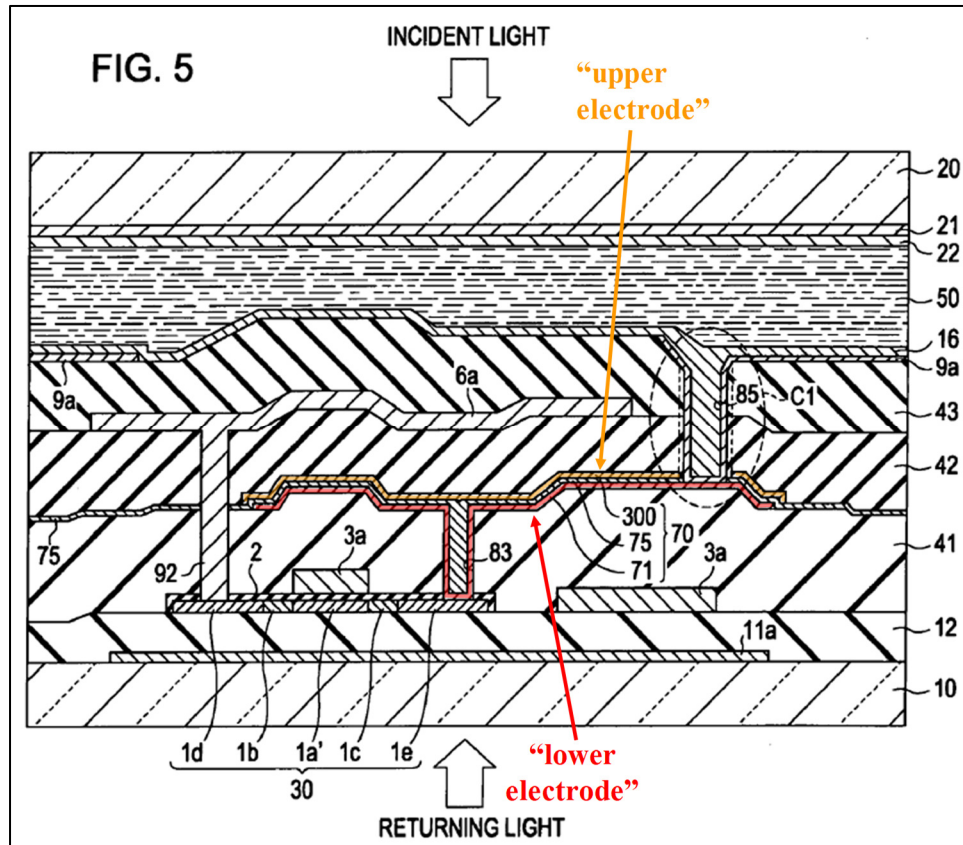
layer”), respectively. (EX1002, ¶¶63.)



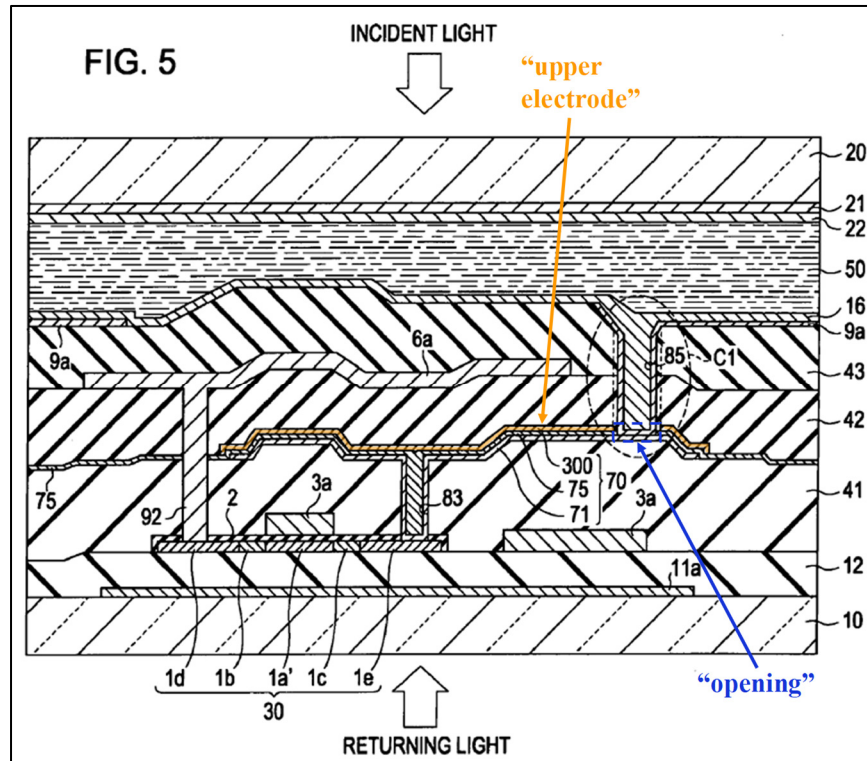
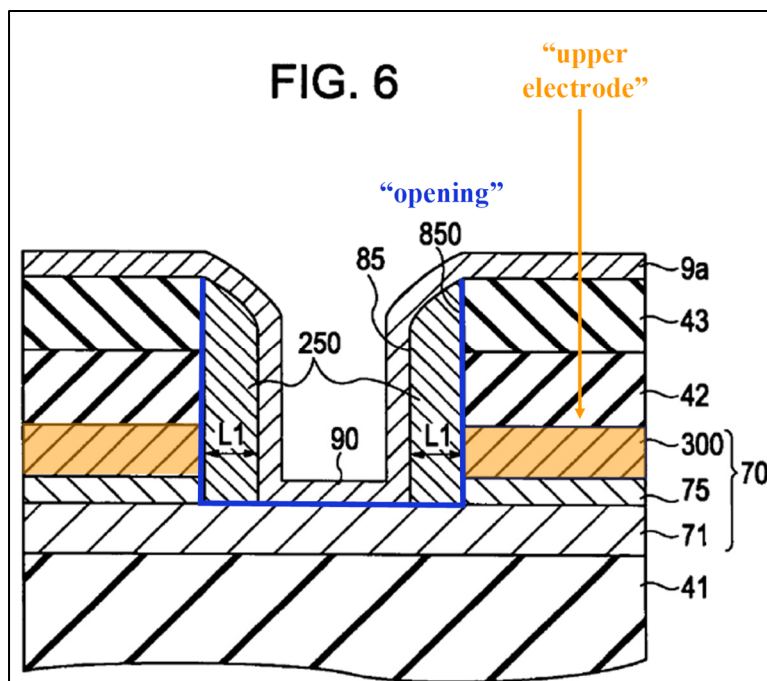
Figures 4 and 5 (below) show **capacitor line 300** (“upper electrode”) arranged to overlap with the whole **relay layer 71** (“lower electrode”), the capacitor line 300 extending beyond an edge of the relay layer 71. Ishii100 discloses “[w]hen this capacitor line 300 is seen in plan view, as shown in FIG. 4,

it is formed so as to **overlap** a formation area of a scanning line 3a. . . . Among these, a **protruding portion** contributes to an increase in the formation area of the storage capacitor 70 using a region on the scanning line 3a and a region under the data line 6a. Further, the capacitor line 300 preferably extends from an image display region 10a where a pixel electrode 9a is arranged in its periphery.” (EX1004, [0059].) It was known at the time of the ’730 to have the upper electrode of capacitor be larger than the lower electrode to prevent any change in capacitance due to the overlay deviation. (See, e.g., EX1012, EX1013, [0038], Figs. 2, 4; EX1002, ¶¶64-65.)





Ishii100 discloses “[t]he sidewall 250 is provided on the inner wall of an *opening 850* which is opened through the third interlayer insulating film 43, the second interlayer insulating film 42, the *capacitor line 300*, and the dielectric film 75.” (EX1004, [0070].) Figures 5 and 6 (below) show the *capacitor line 300* (“upper electrode”) having an *opening 850*. (EX1002, ¶66.)

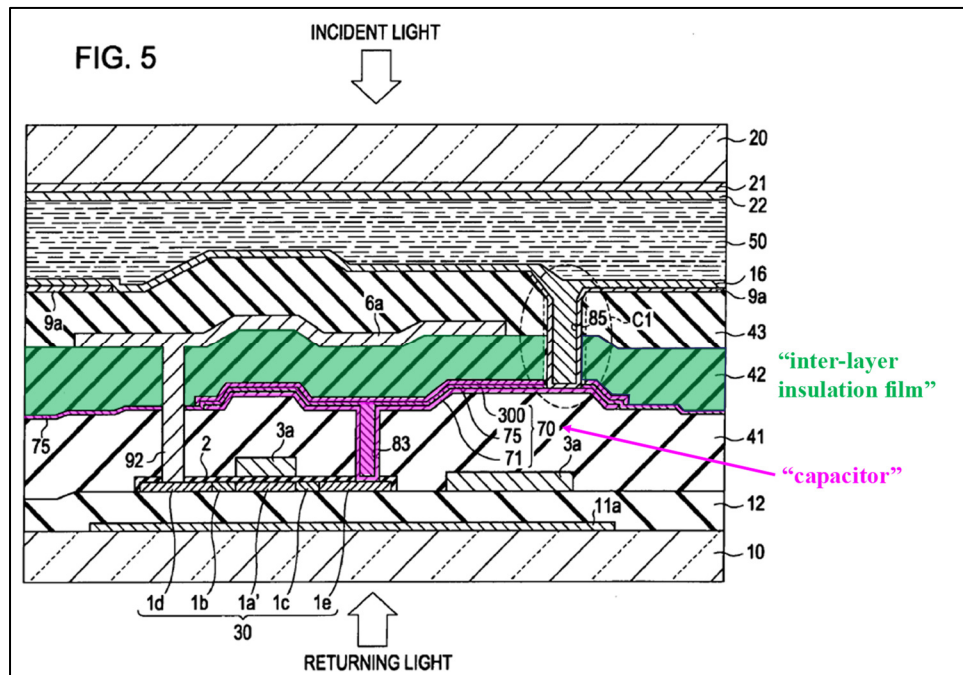


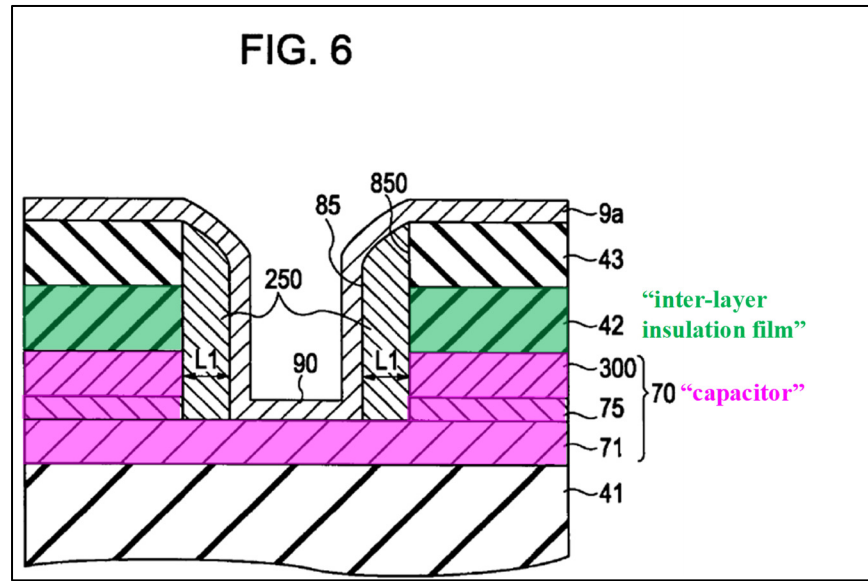
- e. **1[d]: “an inter-layer insulation film covering the capacitor;”**

Ishii100 teaches a storage capacitor 70 (“capacitor” (*see* 1[c])) comprises a

relay layer 71, a dielectric film 75, and a capacitor line 300. Ishii100 discloses “*a second interlayer insulating film 42 through which a contact hole 81 which leads to the highly doped source region id and a contact hole 85 which leads to the relay layer 71 are bored, is formed on the relay layer and the capacitor line.*” (EX1004, [0065]; *also* [0074]; EX1002, ¶¶67-68.)

Figures 5 and 6 (below) show *interlayer insulating film 42* covering the *capacitor 70*. (EX1002, ¶69.)



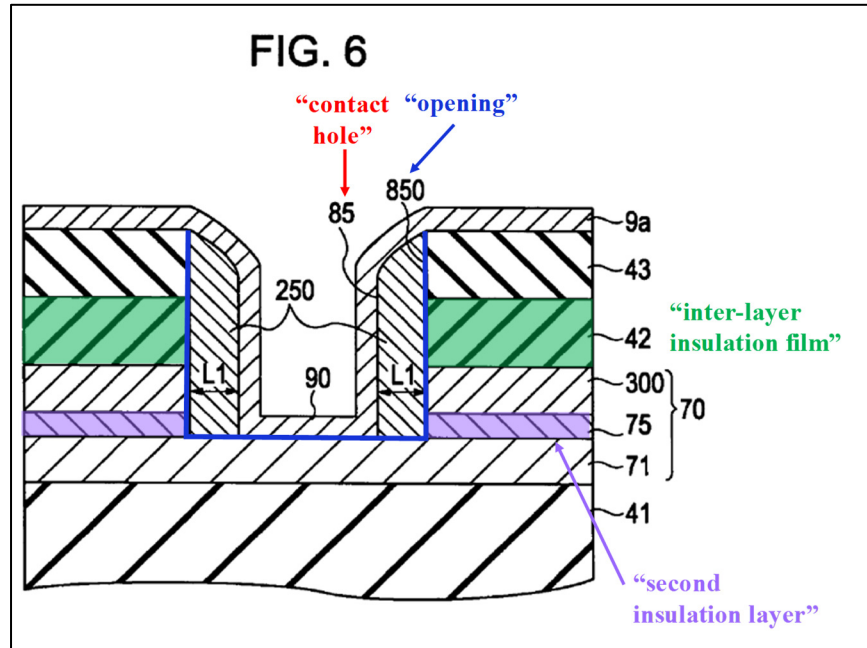


- f. 1[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

Ishii100’s “sidewall 250 is provided on the inner wall of an opening 850 which is opened through the third interlayer insulating film 43, *the second interlayer insulating film 42*, the capacitor line 300, and *the dielectric film 75.*” (EX1004, [0070].) “[T]he contact hole 85 [is] surrounded by this sidewall 250.” (EX1004, [0070].) “The contact hole 85 is a self-alignment-type contact hole formed simultaneously with formation of the sidewall 250, and is surrounded by the sidewall 250.” (EX1004, [0071].) Ishii100 discloses “the *contact hole 85 which is bored through the second interlayer insulating film 42* and the third interlayer insulating film 43.” (EX1004, [0068]; EX1002, ¶¶70-71.)

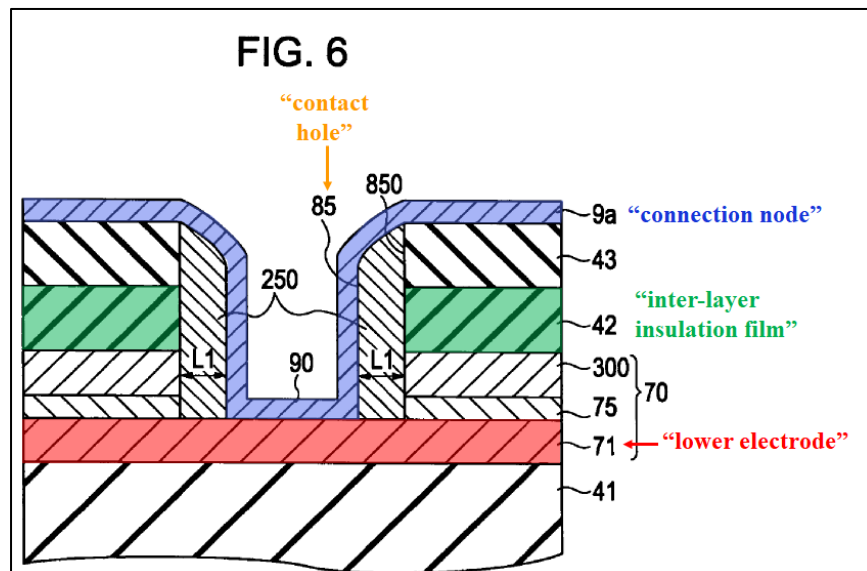
Figure 6 (below) shows a *contact hole 85* in the *interlayer insulating film*

42 (“inter-layer insulation film” (see 1[d]) and dielectric film 75 (“second insulation layer” (see 1[c]), and within the opening 850. (EX1002, ¶72.)

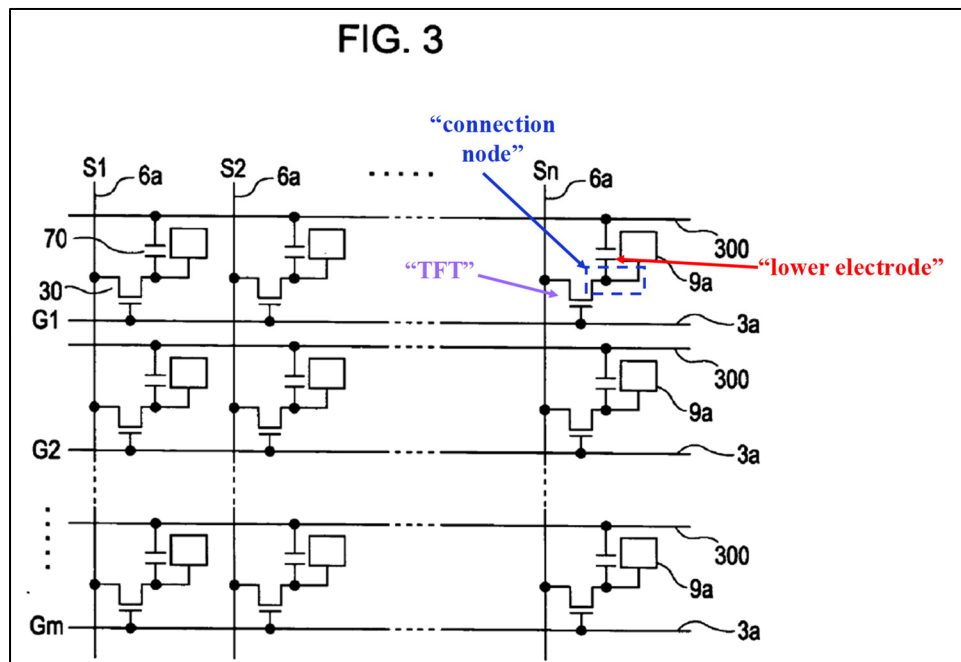


- g. 1[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”

Figure 6 (below) shows a part of the pixel electrode 9a (“connection node”) on the interlayer insulating film 42 and electrically coupling the relay layer 71 (“lower electrode” (see 1[c]) through the contact hole 85 (“node contact hole” (see 1[e])). (EX1002, ¶¶73-74.)



Ishii100's "pixel electrode 9a (i.e., conductive film 90) is electrically connected to the relay layer 71 via the self-alignment-type contact hole 85." (EX1004, [0078].) Ishii100 discloses "[t]he relay layer 71 has a function of relay-connecting the pixel electrodes 9a and ... the TFT 30 via contact hole[] ... 85." (EX1004, [0058].) Figure 3 (below) shows a part of the *pixel electrode 9a* electrically coupling the *lower electrode* of the capacitor 70 and *TFT 30*. (EX1002, ¶75.)



2. Claim 2: “The TFT array substrate of claim 1, wherein the opening overlaps with the lower electrode.”

Ishii100 discloses “*an opening 850* which is opened through the third interlayer insulating film 43, the second interlayer insulating film 42, the capacitor line 300, and the dielectric film 75 is formed by etching, etc. *At this time, the relay layer 71 is exposed.*” (EX1004, [0075].) Figure 6 (below) shows the *opening 850* overlaps with the *relay layer 71* (“lower electrode” (*see 1[c]*)). (EX1002, ¶¶76-78.)

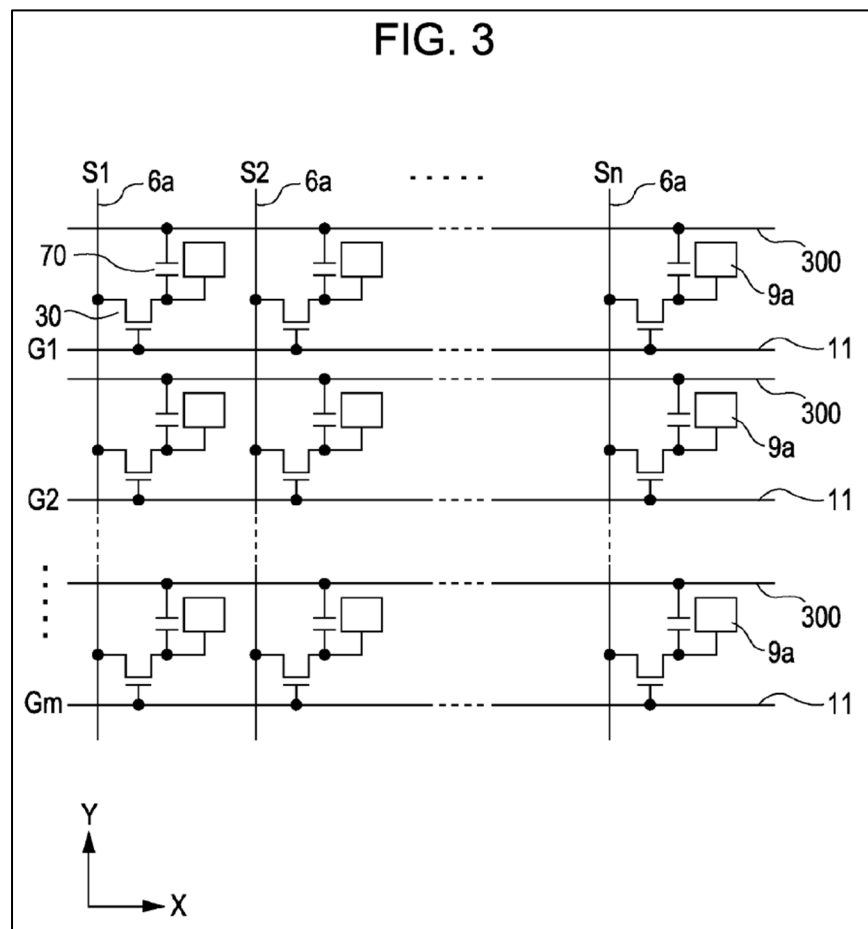
1. Summary Of Ishii423

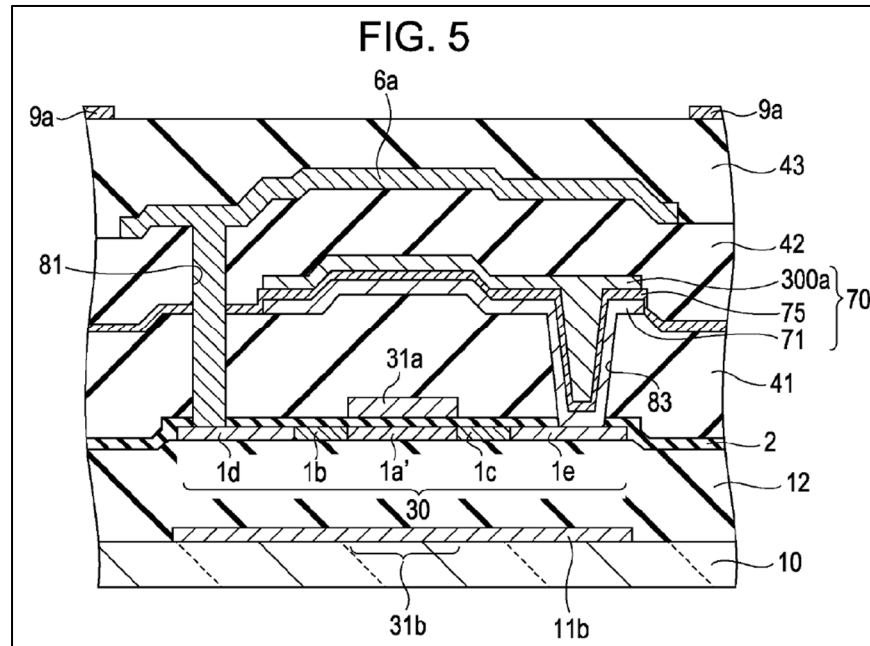
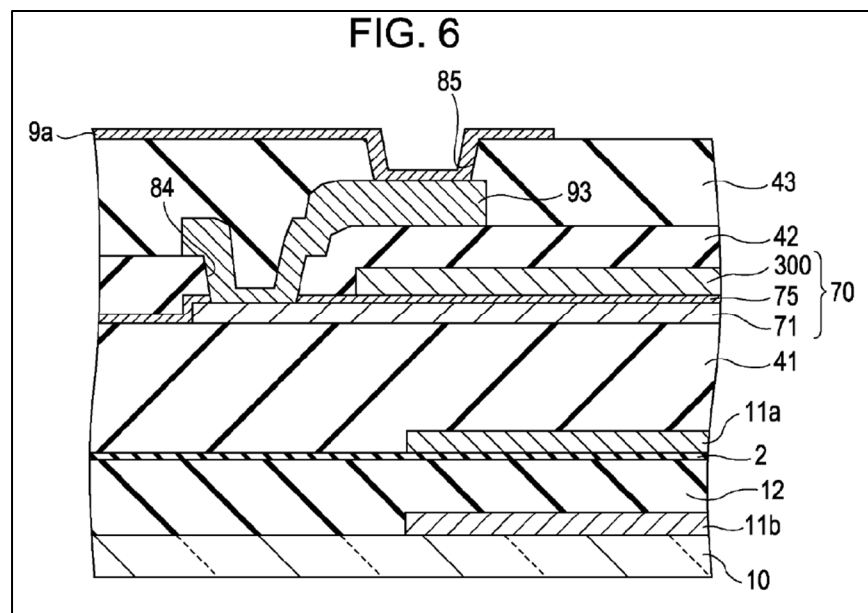
23

capacitor electrode 71, the contact holes 83, 84 and 85, and the relay layer 93 to the pixel electrode side source/drain region 1e of the semiconductor layer 1a.”

(EX1015, [0114]; EX1002, ¶79.)

Figure 3 (below) of Ishii423 shows its pixel circuit, and Figures 5 and 6 (below) of Ishii423 show its display stack. (EX1002, ¶80.)





2. Claim 1

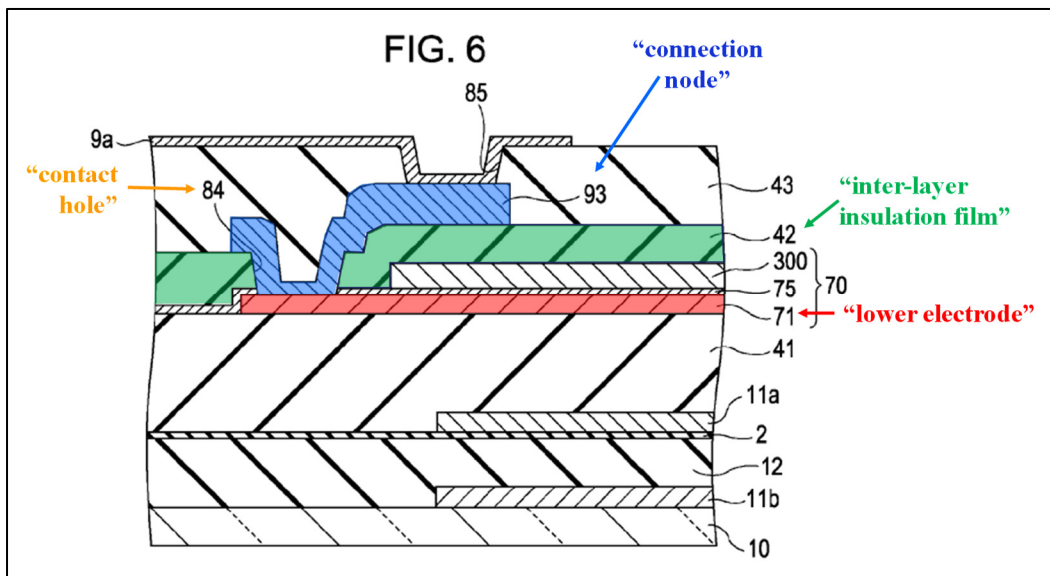
a. 1[pre]-1[e]

Ishii100 teaches elements 1[pre]-1[e]. (See Ground 1; EX1002, ¶¶81-86.)

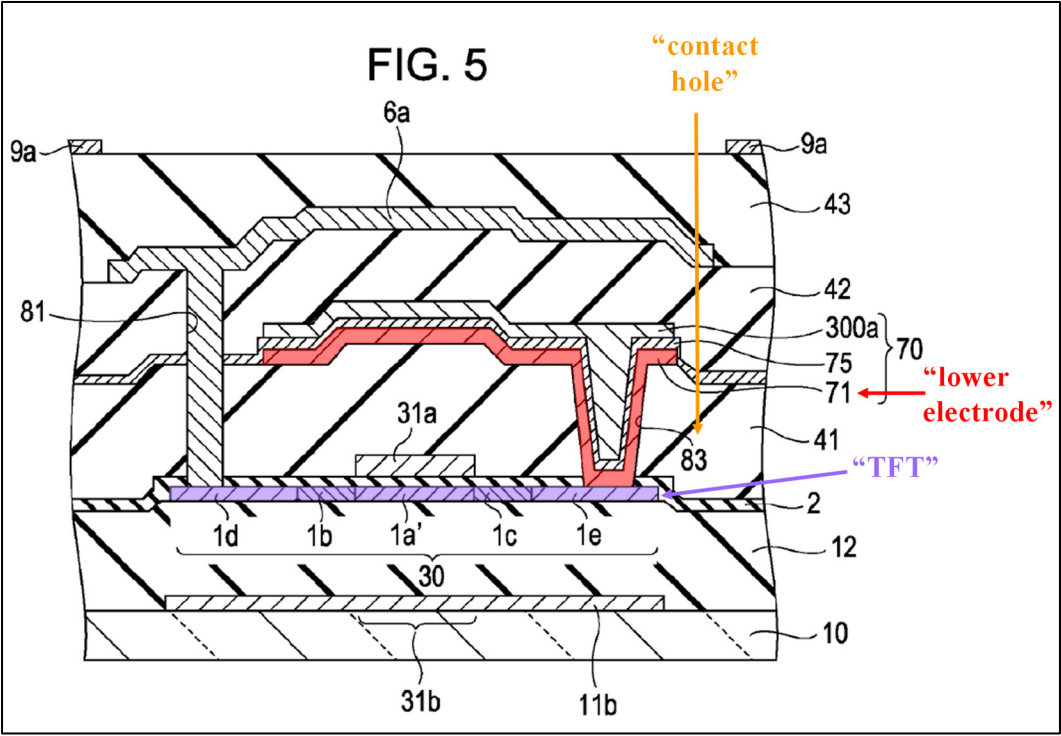
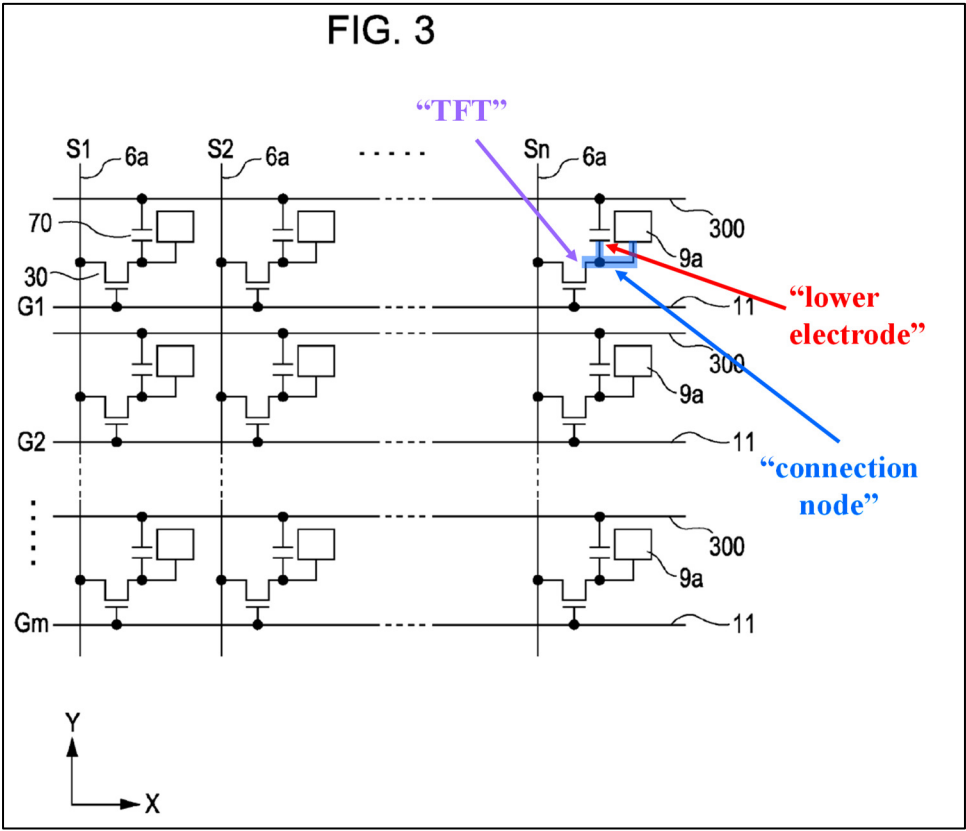
- b. **1[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”**

Ishii100 teaches the “connection node” of element 1[f].

To the extent that Ishii100 does not teach the claimed “connection node,” Ishii423 does. Ishii423 discloses “relay layer 93 [is] provided in an upper layer than the storage capacitor 70 through the interlayer insulating film 42 on the TFT array substrate 10.” (EX1015, [0111].) “The pixel electrode 9a is electrically connected through the lower capacitor electrode 71, the contact holes 83, 84 and 85, and the relay layer 93 to the pixel electrode side source/drain region 1e of the semiconductor layer 1a.” (EX1015, [0114].) Figure 6 (below) shows the *relay layer 93* on the *interlayer insulating film 42* and electrically coupling the *lower capacitor electrode 71* and pixel electrode 9a to each other through the *contact hole 84*. Ishii100 similarly teaches an interlayer insulating film 42 (“inter-layer insulation film” (*see* 1[d])). (EX1002, ¶87.)



The *lower capacitor electrode 71* is electrically coupled to the source/drain region 1e of *TFT 30* through the *contact hole 83* (Figure 5 (below)). Additionally, Figure 3 (below) shows the pixel electrode 9a is coupled to TFT 30, thereby the relay layer 93 electrically couples the lower electrode 71 and *TFT 30* to each other. (EX1002, ¶88.)



It would have been obvious to a POSITA to combine the teachings of Ishii100 and Ishii423. Both disclose electro-optical devices and techniques for improving the display quality of electro-optical devices. Ishii100 describes a “technical problem in that the capacity of the storage capacitor in the pixel portion may be lowered and display unevenness may occur.” (EX1004, [0006].) Ishii100 teaches an electro-optical device with greater storage capacitor and “reduc[ed] [] area occupied by components of the pixel structure,” attaining a high contrast display. (EX1004, [0007], [0013].) Ishii423 describes a “technical problem in which display defects, such as flicker or pixel chrominance non-uniformity, may occur and, as a result, the display image quality decreases.” (EX1015, [0005].) Ishii423 teaches an electro-optical device comprising a light shielding film that reduces light leakage, improving the image quality of the display. (EX1015, [0006].) Additionally, both teach the capacitor line and lower electrode are made of metal. (EX1004, [0107], [0108], [0110]; EX1015, [0057].) Thus, Ishii100 and Ishii423 are in the same field of endeavor and reasonably pertinent to the same technical problem of improving the quality of the images from an electro-optical device. (EX1002, ¶89.)

Ishii423 teaches using a relay layer for creating electrical connections in an electro-optical device: “the relay layer 93 is electrically connected through a contact hole 85 (see FIG. 4 and FIG. 6) to the pixel electrode 9a. That is, the lower

capacitor electrode 71, in cooperation with the relay layer 93, relays electrical connection between the pixel electrode side source/drain region 1e and the pixel electrode 9a.” (EX1015, [0108].) A POSITA would have been motivated to use a relay layer 93 for electrical connections because it creates a more reliable connection to the thin ITO pixel electrode 9a. These technical features of Ishii423 may be combined with the teachings of Ishii100 with a reasonable expectation of success because of the similarities between the structures of Ishii100 and Ishii423. Prior art such as Ishii 423 has demonstrated such success of using a relay layer for electrical connections. The Ishii100-Ishii423 combination results in an electro-optical device that provides improved image quality. (EX1002, ¶89.)

Because Ishii100 and Ishii423 relate to electro-optical devices and both have the same objectives of improving the image quality, a POSITA would have been motivated to use the techniques, such as using a relay layer for an electrical connection, as taught by Ishii423 to improve the similar device of Ishii100 in the same way. Ishii100 and Ishii423 share the same inventor, and share many of the same circuit components and structure. For example, the liquid crystal devices of Ishii100 and Ishii423 shown in Figures 1 and 2 look similar. (EX1004, Figs. 1, 2; EX1015, [0050], Figs. 1, 2.) And Ishii100’s pixel circuit is similar to Ishii423’s pixel circuit. Both comprise pixel electrode 9a, capacitor line 300, storage capacitor 70, TFT 30, image signals S1, S2, ... Sn, data lines 6a, scanning signals

G1, G2, ... Gm, and scanning lines 11. (EX1004, [0047]-[0048]; EX1015, [0088].) There are a lot of similarities (overlap) in the display stack of Ishii100 and Ishii423, both comprising a substrate 10, base/underlying insulating film 12, interlayer insulating film 41, interlayer insulating film 42, interlayer insulating film 43, pixel electrode 9a, TFT 30 disposed on underlying insulating film 12, capacitor 70 disposed on interlayer insulating film 41, data line 6a disposed on interlayer insulating film 42, and pixel electrode 9a disposed on interlayer insulating film 43. (EX1004, [0062]-[0063], [0065]-[0066], Fig. 5; EX1015, [0112]-[0114], Figs. 5, 6.) Given the overlap among Ishii100 and Ishii423, and that the prior art has already known and demonstrated such techniques with success, there would have been a reasonable expectation of success. (EX1002, ¶91.)

Because Ishii100 and Ishii423 are so similar, has the same inventor, and relate to electro-optical devices, a POSITA would have been motivated to use the techniques disclosed in Ishii423 to improve the similar device of Ishii100 in the same way. Ishii100 uses a self-alignment type contact hole to electrically connect the pixel electrode 9a to the relay layer 71 (lower capacitor electrode), Ishii423 has the same connection, but uses a relay layer 93. It would have been obvious to combine Ishii100 and Ishii423. (EX1002, ¶91.)

3. Claim 2: “The TFT array substrate of claim 1, wherein the opening overlaps with the lower electrode.”

Ishii100 teaches claim 2. (*See* Ground 1; EX1002, ¶¶92.)

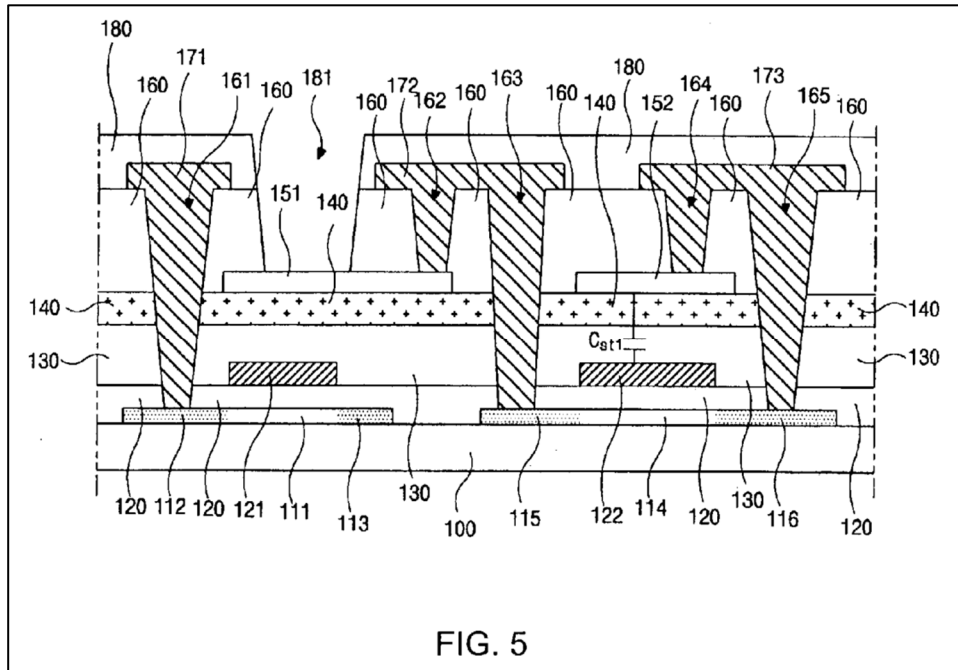
VII. GROUND 3: PARK AND ISHII100 RENDER OBVIOUS CLAIMS 3, 4, AND 10-14

A. Summary Of Park

Park discloses an “active matrix electro luminescence display (ELD) device having thin film transistors and manufacturing method for the same.” (EX1005, [0003].) “[A] pixel of the ... display device has a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7.” (EX1005, [0006]; EX1002, ¶¶93-94.)

Park’s storage capacitor 6 “is for keeping a gate driving voltage of the driving thin film transistor stable and is an important element for displaying high quality images by restraining a pixel voltage fluctuation that is induced by a kick-back voltage of the switching film transistor and a leakage current.” (EX1005, [0015].) Park explains that it is desirable to increase the capacitance of the storage capacitor 6 by increasing the area of the electrodes and/or decreasing the thickness of the dielectric between the electrodes. (*Id.*) “If the area of the electrode of the storage capacitor is increased, it results in a decrease of an area of the pixel electrode, i.e., the anode electrode 60, and thus an aperture ratio is decreased.” (*Id.*; EX1002, ¶¶95-97.)

Park discloses and shows in, *e.g.*, Figure 5 (below) an active matrix organic electro luminescent display (ELD) device comprising a storage capacitor with increased storage capacitance without reducing an aperture ratio, and reduced manufacturing time and costs. (EX1005, [0017], [0034]; EX1002, ¶98.)



B. Claim 3

1. Preamble: “A thin film transistor (TFT) array substrate comprising:”

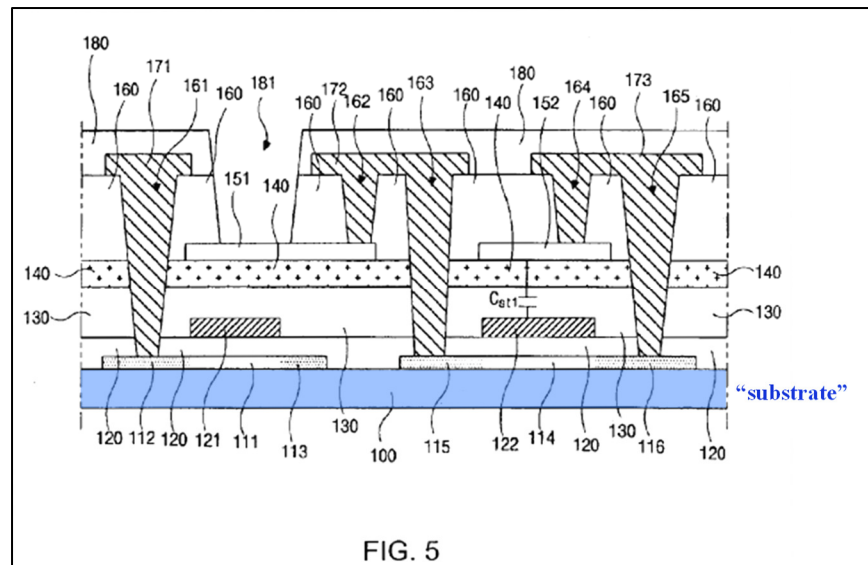
To the extent that the preamble is limiting (which Petitioner does not concede), Park teaches “[a] thin film transistor (TFT) array substrate.”

Park discloses a plurality of TFTs that are part of “an *array substrate* of the active matrix organic electroluminescent display device.” (EX1005, [0014].) “The first gate electrode 121, the first source electrode 171 and the first drain electrode

(not shown), form *a switching thin film transistor*, and the second gate electrode 122, the second source electrode 173 and the second drain electrode 172 form *a driving thin film transistor*.” (EX1005, [0034], [0006], Fig. 1; EX1002, ¶¶99-101.)

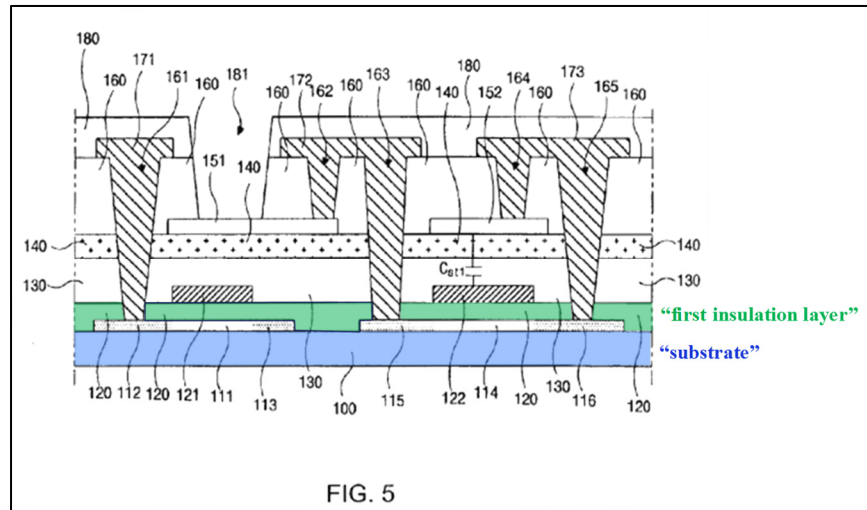
2. 3[a]: “a substrate;”

Park’s device “is formed on a transparent insulating *substrate*” (Figure 5 (below)). (EX1005, [0034], cl. 1; EX1002, ¶¶103-106.)



3. 3[b]: “a first insulation layer on the substrate;”

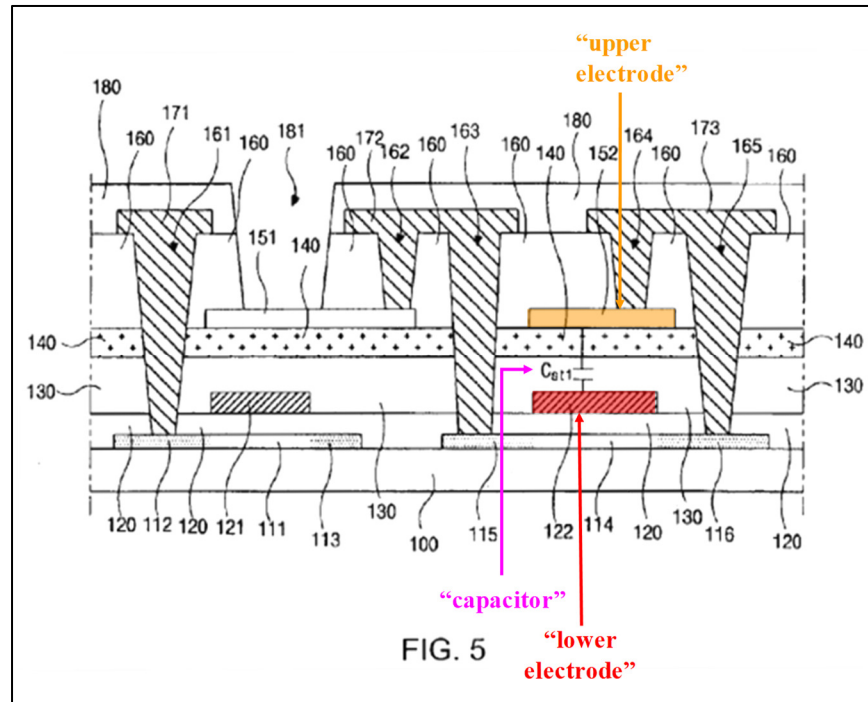
Park discloses a *gate insulating layer 120* (Figure 5 (below)) on the *substrate 100*. (EX1005, [0034]; EX1002, ¶¶107-108.)



4. 3[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

a. Park

Park’s “capacitor electrode 152 forms a storage capacitor C_{st1} together with the second gate electrode 122.” (EX1005, [0034].) Figure 5 (below) shows the storage capacitor C_{st1} comprising a gate electrode 122 and a capacitor electrode 152. (EX1002, ¶109.)



Park discloses “[f]irst and second *inter layers 130* and *140* are sequentially formed on the first and second *gate electrodes 121* and *122*.” (EX1005, [0034].)

Figure 5 (below) shows the *gate electrode 122* on the *gate insulating layer 120* (“first insulation layer” (see 3[b])), wherein the *capacitor electrode 152* is insulated from the gate electrode 122 by an *inter layer 130*. (EX1002, ¶110.)

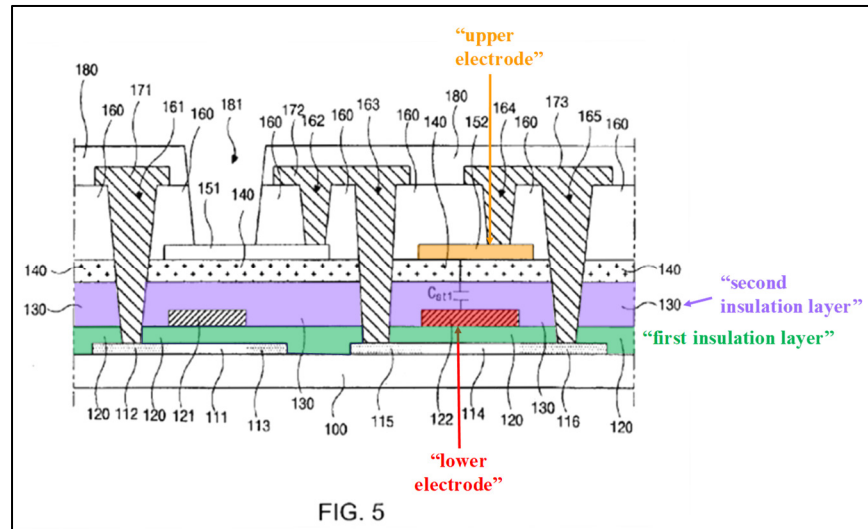


Figure 5 (above) shows the **capacitor electrode 152** arranged to overlap with the whole **gate electrode 122**. Thus, Park teaches the second drain electrode 172 is connected to the second drain region 115 through the third contact holes 163 between the anode electrode 151 and the capacitor electrode 152. (EX1005, [0034]; EX1002, ¶111.)

b. Ishii100

Element 3[c] is similar to element 1[c], which Ishii100 teaches (*see* Ground 1), except it does not require the “upper electrode extend[] beyond an edge of the lower electrode.” (EX1002, ¶112.)

c. Motivation to combine Park and Ishii100

It would have been obvious to a POSITA to combine the teachings of Park and Ishii100. Both disclose light-emitting devices and address manufacturing issues, including increasing the capacitance of the storage capacitor. Park

discloses an ELD device “in which a storage capacitance of a storage capacitor is increased without reducing an aperture ratio and number of masks needed is reduced.” (EX1005, [0017].) Ishii100 discloses an “electro-optical device” (organic EL display) “having a storage capacitor of increased area, and enabling high-definition image display, a manufacturing method thereof, an electronic apparatus, and a capacitor.” (EX1004, [0007], [0097].) Thus, Park and Ishii100 are in the same field of endeavor and directed to increasing the capacitance of the storage capacitor. (EX1002, ¶113.)

Ishii100 teaches including “a self-alignment-type contact hole” in the electro-optical device as a way to connect part of the pixel electrode 9a (part of the connection node) to the lower capacitor electrode, eliminating the need for an additional mask for forming the storage capacitor. (EX1004, [0011].) Ishii100 improves the area of the storage capacitor, thereby “a larger storage capacitor can be formed on the substrate of the same size.” (*Id.*) The Park-Ishii100 combination results in an OLED with greater storage capacitance and reduced manufacturing deviations. Park and Ishii100 have similar circuits. Ishii100’s circuit comprises a part of a pixel electrode 9a connected to a relay layer 71 (lower capacitor electrode) and a TFT 30 via a connection node. (EX1004, [0058], Fig. 3.) This is similar to Park’s circuit, which comprises a gate electrode 122 (lower electrode of the capacitor) connected to a switching thin film transistor 4 via a connection node.

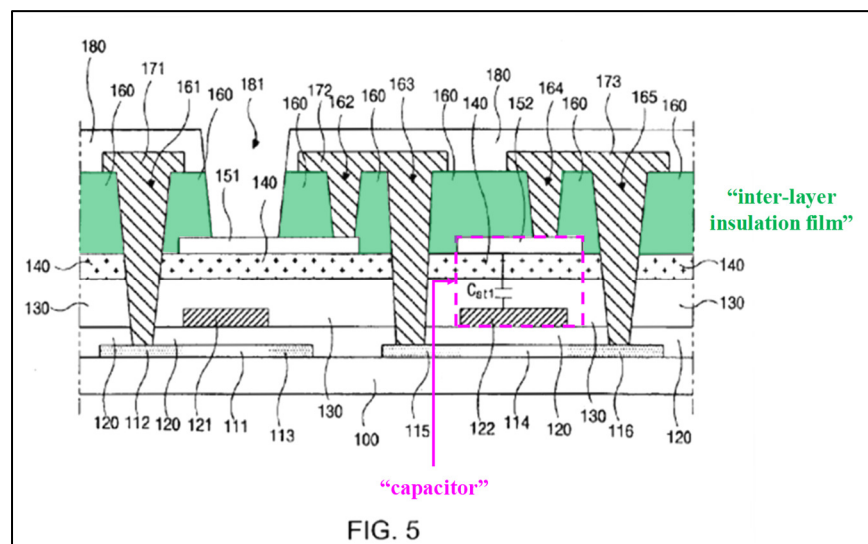
(EX1005, [0006], Fig. 1.) Ishii100 teaches a self-alignment-type contact hole connecting the connection node and the lower capacitor electrode. A POSITA would have been motivated to use Ishii100's self-alignment-type contact hole because, as Ishii100 explains, "positioning between a mask for forming a contact hole and a mask for forming a storage capacitor is not required." (EX1004, [0071].) The combination results in the second gate electrode 122 being electrically connected to the first drain region 113 by the first drain electrode disposed on the first passivation layer 160 through Ishii100's self-alignment-type contact holes. Given the overlap between Park and Ishii100, and the prior art already knew and demonstrated such techniques with success, there would have been a reasonable expectation of success for the Park-Ishii100 combination. (EX1002, ¶114.)

Because Park and Ishii100 both relate to increasing the capacitance of the storage capacitor in a light-emitting display device and both use connection nodes to provide interconnections between layers, a POSITA would be motivated to use the technique disclosed in Ishii100 to improve the similar device of Park in the same way. Thus, it would have been obvious to a POSITA to combine Park and Ishii100. (EX1002, ¶115.)

5. 3[d]: “an inter-layer insulation film covering the capacitor;”

Park’s “*first passivation layer 160 is formed of material such as silicon oxide (SiO₂) on the anode electrode 151 and the capacitor electrode 152.*”

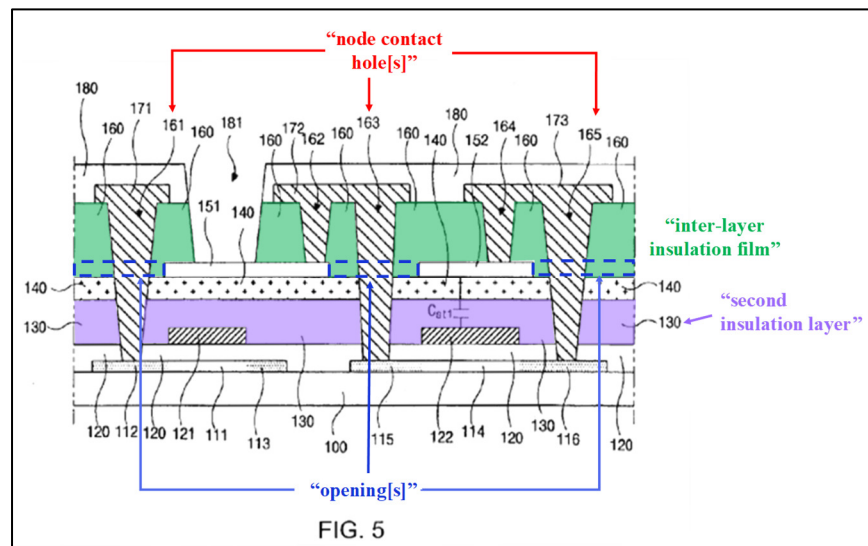
(EX1005, [0034].) Figure 5 (below) shows the *passivation layer 160* covering the *capacitor Cst1*, which comprises a capacitor electrode 152 and a gate electrode 122. (EX1002, ¶¶116-117.)



6. 3[e]: “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening; and”

Park’s “first, third, and fifth contact holes 161, 163 and 165 are formed all the way to the gate insulating layer 120. The first contact hole 161 exposes a portion of the fast [first] source region 112, the second contact hole 162 the anode electrode 151, the third contact hole 163 the second drain region 115, the fourth contact hole 164 the capacitor electrode 152 and the fifth contact hole 165 the

second source region 116.” (EX1005, [0034].) Figure 5 (below) shows the **contact holes 161, 163, and 165** in the **inter layer 130** (“second insulation layer” (see 3[c])) and **passivation layer 160** (“inter-layer insulation film” (see 3[d])). The figure shows contact holes 161, 163, and 165 within the openings. (EX1002, ¶¶118-120.)



Park explains “[t]hough it is not shown in the figure, the second gate electrode 122 is electrically connected to the first drain region 113. . . . a first drain electrode (not shown), which is connected to the first drain region 113, . . . are also formed on the first passivation layer 160.” (EX1005, [0034].) Although Figure 5 specifically shows the contact holes 161, 163, and 164, Park explains contact holes are used to expose a portion of the drain regions. A POSITA would have understood the first drain electrode of the switching thin film transistor 4 is one of those drain regions. (EX1005, [0007], [0034].) A POSITA would thus have

expected the figure to represent the structure of the other transistor electrodes, including the drain electrode of the switching thin film transistor 4, particularly since Park describes the structure of the other drain regions and then states the drain region 113 “not shown.” Thus, the structure of Figure 5 represents the structure of the drain region 113 and associated contact hole, including the contact hole is in the interlayer 130 and passivation layer 160 for electrically connecting the drain electrode of the switching thin film transistor 4, within an opening.

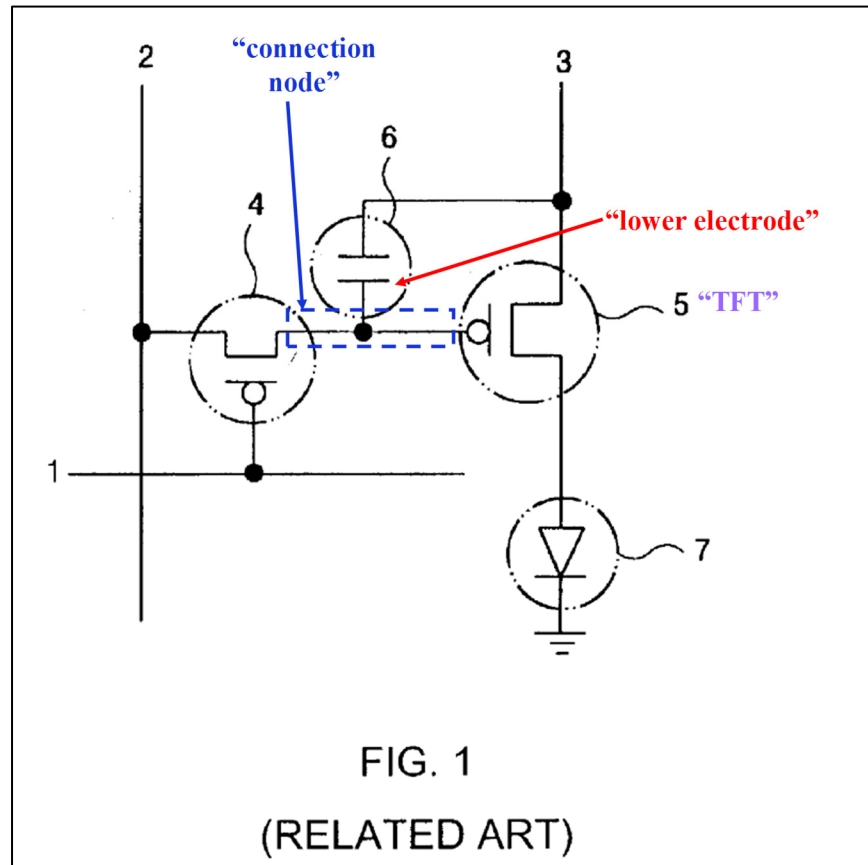
(EX1002, ¶¶121-122.)

Ishii100 similarly teaches “a node contact hole in the inter-layer insulation film and the second insulation layer, and within the opening.” (*See* 1[e]; EX1002, ¶123.)

7. 3[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole,”

Park’s circuit (Figure 1 (below)) shows a “drain electrode of the switching thin film transistor 4 *is connected to* a gate electrode of the thin, film transistor 5” and a “storage capacitor 6 *is connected to* the gate electrode and the source electrode of the driving thin film transistor 5.” (EX1005, [0006].) The figure shows the *drain of the switching thin film transistor 4* electrically couples the *lower electrode of the capacitor 6* (“lower electrode” (*see* 3[c])) and *driving thin*

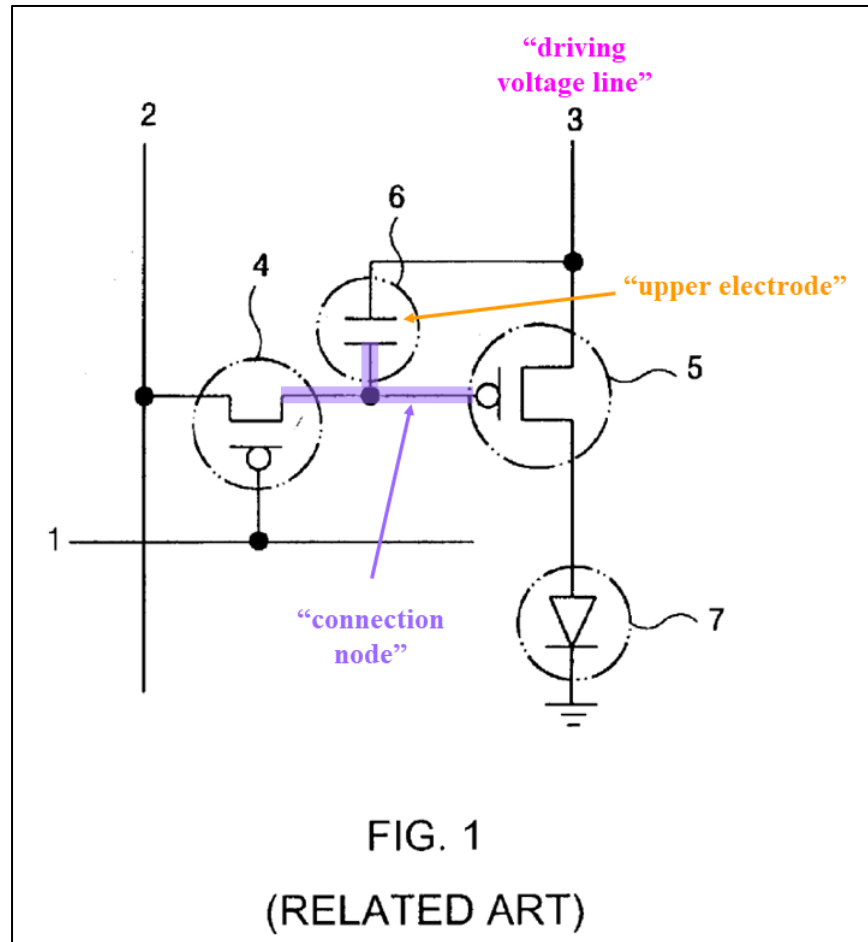
film transistor 5. Park teaches using contact holes for electrically coupling the drain electrode of the switching thin film transistor 4. (See 3[e]; EX1002, ¶¶124-125.)



Park teaches using contact holes (Figure 5 (below)) to connect to the sources and drains of the transistors using *source and drain electrodes* on the *passivation layer 160* (“inter-layer insulation film” (see 3[e])). A POSITA would have understood Park’s Figure 5 represents the structure of the drain electrode of the switching thin film transistor 4 (first drain electrode connected to drain region 113). (See 3[e]; EX1002, ¶¶126-127.)

8. 3[g]: “wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”

Park’s circuit (Figure 1 (below)) includes a capacitor 6 having an *upper electrode* coupled to *power line 3* and a lower electrode coupled to a *connection node*. A POSITA would have understood the power line 3 to be a driving voltage line that provides a driving voltage because it drives the OLED 7 when driving thin film transistor 5 is turned on. (EX1005, [0006].) Thus, Park teaches an “upper electrode [] configured to receive a driving voltage through a driving voltage line.” (EX1002, ¶¶128-129.)



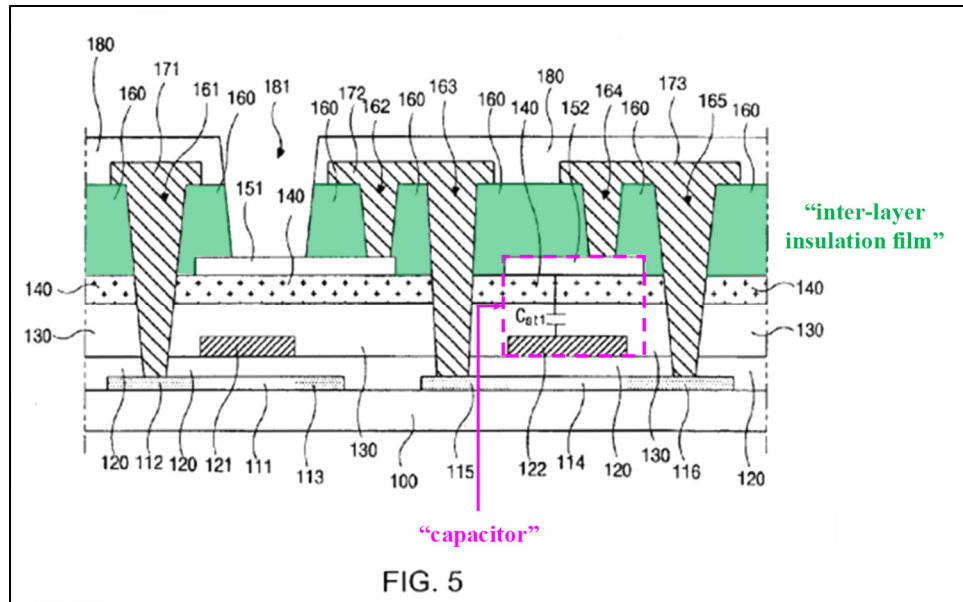
Park's drain of switching TFT 4 as the "first drain electrode" (EX1006, [0007]), which is part of the connection node (*see* Figure 1 (above)). The second source electrode 173 is connected to the power line 3 and may be extended from the power line 3 or be a portion of the power line 3. (EX1005, [0007], [0034]). The power line 3 is formed on the first passivation layer 160 ("inter-layer insulation film" (*see* 3[e])) and is formed of same material as the source and drain electrodes. (EX1005, [0020], [0021], [0034], [0039].) "[T]he first drain electrode (not shown) and the power line (not shown) are formed at this time." (EX1005,

[0011].) A POSITA would have understood the first drain electrode and the power line being formed at the same time means the connection node and power line are formed from the same layer because layers in a display device are deposited sequentially on top of each other. (EX1002, ¶¶128-129.)

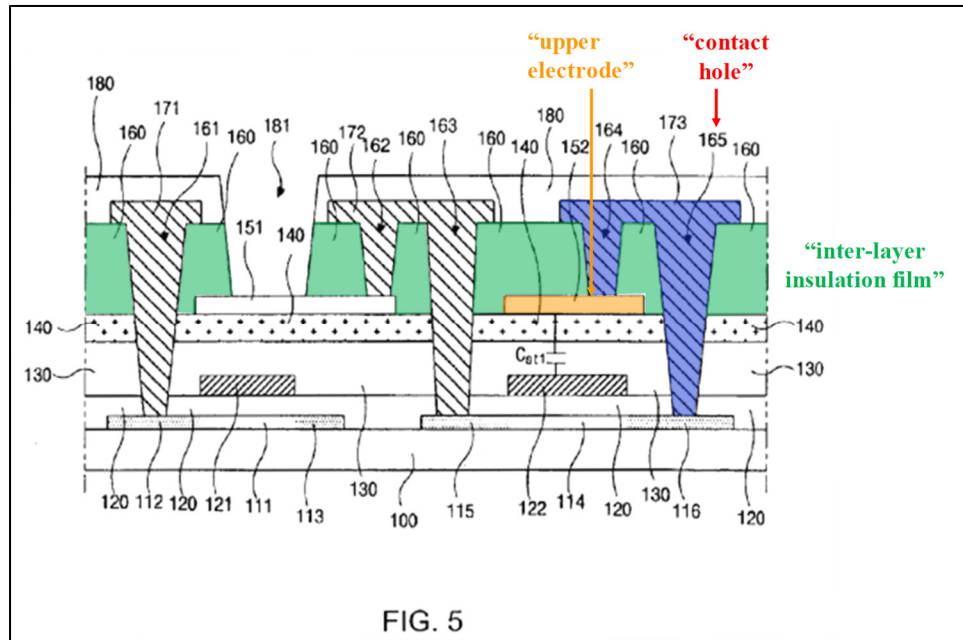
C. Claim 4: “The TFT array substrate of claim 3, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film.”

Park’s power line 3 is coupled to the upper electrode of the capacitor. (*See* 3[g].) Park’s “capacitor electrode 152 forms a storage capacitor C_{st1} together with the second gate electrode 122.” (EX1005, [0034].) Thus, Park’s power line 3 (“driving voltage line” (*see* 3[g])) is coupled to the capacitor electrode 152 (“upper electrode”). (EX1002, ¶131.)

Park discloses “a power line (not shown), which is connected to the second source electrode 173, are also formed on the first passivation layer 160.” (EX1005, [0034].) Park’s “*first passivation layer 160 is formed ... on the anode electrode 151 and the capacitor electrode 152.*” (EX1005, [0034].) Figure 5 (below) shows the *passivation layer 160* (“inter-layer insulation film”) covering the *capacitor Cst1*. (EX1002, ¶132.)



Park's "second source electrode 173 is connected to the capacitor electrode 152 and the second source region 116 through the fourth and fifth contact holes 164 and 165." (EX1005, [0034], [0039].) "The second source electrode 173 may be extended from the power line (not shown) or may be formed of a portion of the power line." (EX1005, [0007], [0034].) The power line 3 is formed on the first passivation layer 160 and is formed of same material as the source and drain electrodes. (EX1005, [0020], [0021], [0034], [0039].) Figure 5 (below) shows the *source electrode 173* (extended from the power line 3 or a portion of the power line 3) coupled to the *capacitor electrode 152* ("upper electrode") through *contact hole 164* in the *passivation layer 160* ("inter-layer insulation film"). (EX1002, ¶132.)



It would have been obvious to a POSITA to combine Park and Ishii100.

(See 3[c]; EX1002, ¶¶133-134.)

D. Claim 5

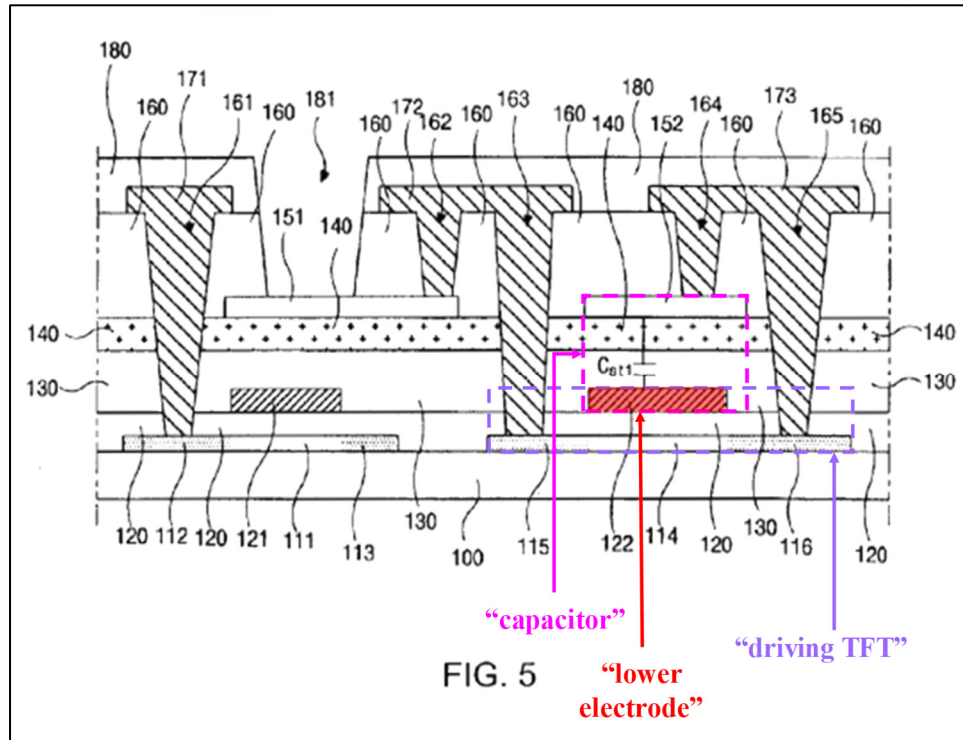
1. Elements 5[pre]-5[f]

Elements 5[pre]-5[f] are similar to elements 1[pre], 1[a]/3[a], 1[b]/3[b], 3[c], 1[d]/3[d], 1[e]/3[e], and 1[f]/3[f], which Park and/or Ishii¹⁰⁰ teach. (EX1002, ¶¶135-141.)

2. **5[g]: “a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”**

Park teaches a *driving TFT 4* (Figure 5 (below)) arranged to overlap with the *capacitor Cst1*. “The capacitor electrode 152 forms a storage capacitor C_{st1} together with the second gate electrode 122.” The *gate electrode 122* is the “lower

electrode.” (See 3[c].) Park’s “second gate electrode 122, the second source electrode 173 and the second drain electrode 172 form a driving thin film transistor.” (EX1005, [0034] (emphases added).) The *gate electrode 122* of the *driving TFT 4* comprises the lower electrode. (EX1002, ¶¶142-144.)



E. Claim 10

1. Preamble: “An organic light-emitting diode (OLED) display comprising:”

To the extent the preamble is limiting (which Petitioner does not concede), Park and/or Ishii100 teach the preamble.

Ishii100 discloses “an electro optical device,” and “the invention can be applied to ... an organic EL display ...” (EX1004, [0002], [0097]; EX1002, ¶146.)

To the extent that Ishii100 does not teach the preamble, Park discloses an “organic electro luminescence display (ELD) device emits light by recombination of an electron and a hole and thus it is referred to as an organic light emitting diode (OLED).” (EX1005, [0005]; EX1002, ¶145.)

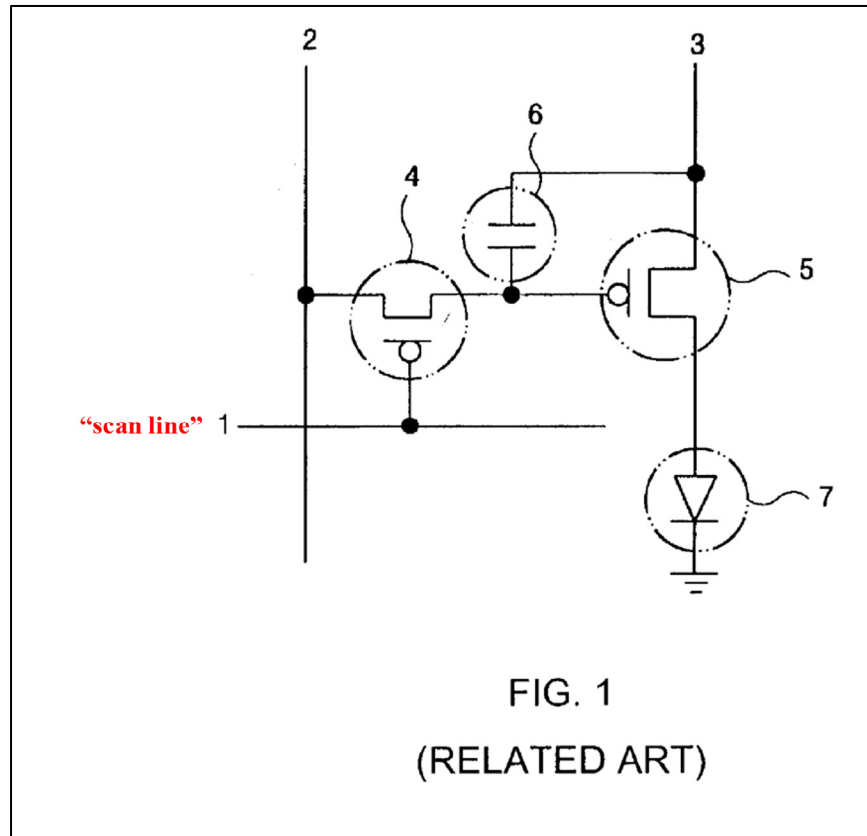
2. Elements 10[a], 10[b], And 10[g]-10[i]

Elements 10[a], 10[b], and 10[g]-10[i] are similar to elements 1[a]/3[a], 1[b]/3[b], 1[c], 1[e], and 1[f] respectively, which Park and/or Ishii100 teach. (EX1002, ¶¶147-148, 172-174.)

3. 10[c]: “a scan line on the first insulation layer and configured to deliver a scan signal;”

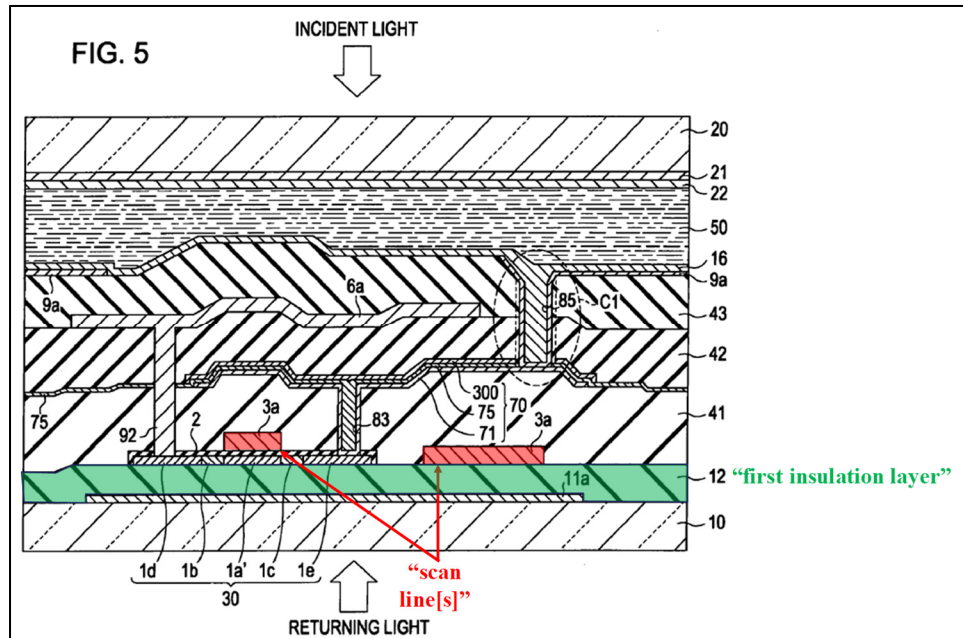
a. Park

Park discloses “[i]f a signal is applied to the gate line 1, the switching thin film transistor 4 is turned on.” (EX1005, [0006].) A POSITA would have understood the signal being applied to the *gate line 1* (Figure 1 (below)) is delivering a scan signal. Park’s gate electrodes 21 and 22 are formed on the gate insulating layer 20 (“first insulation layer” (*see* 1[b])) (EX1005, Fig.3B, [0009].) It would have been obvious to a POSITA to use a gate line to deliver a scan signal. (EX1002, ¶149; *see, e.g.*, EX1017, 5:16-21.)



b. Ishii100

Ishii100's "scanning lines 3a ... are configured to sequentially apply scanning signals G1, G2, , and Gm in this order to the scanning lines 3a in pulses with predetermined timing." (EX1004, [0048].) Figure 5 (below) shows *scanning line 3a* on *insulating film 12* ("first insulation layer" (see 1[b])). (EX1002, ¶¶150-153.)



It would have been obvious to a POSITA to combine Park and Ishii100.

(See 3[c].)

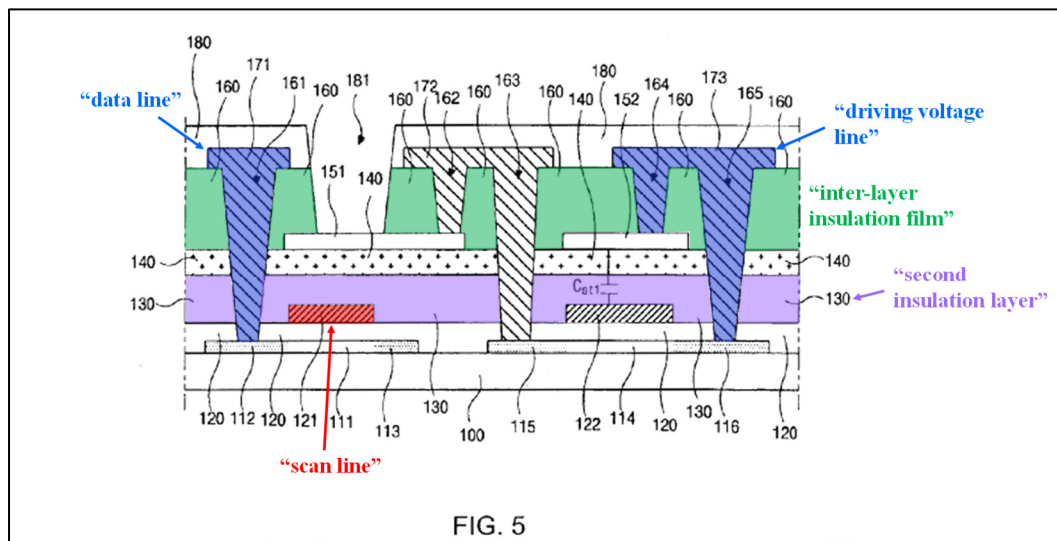
4. 10[d]: “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

a. Park

Park’s source electrode of the switching thin film transistor 4 is connected to the data line 2. If the **data line 2** is applied to the gate electrode of the driving thin film transistor 5, the driving thin film transistor 5 is turned on and the LED 7 emits light. (EX1005, [0006].) Park’s **power line 3** configured to deliver a driving voltage (see 3[g]). (EX1002, ¶¶154-155.)

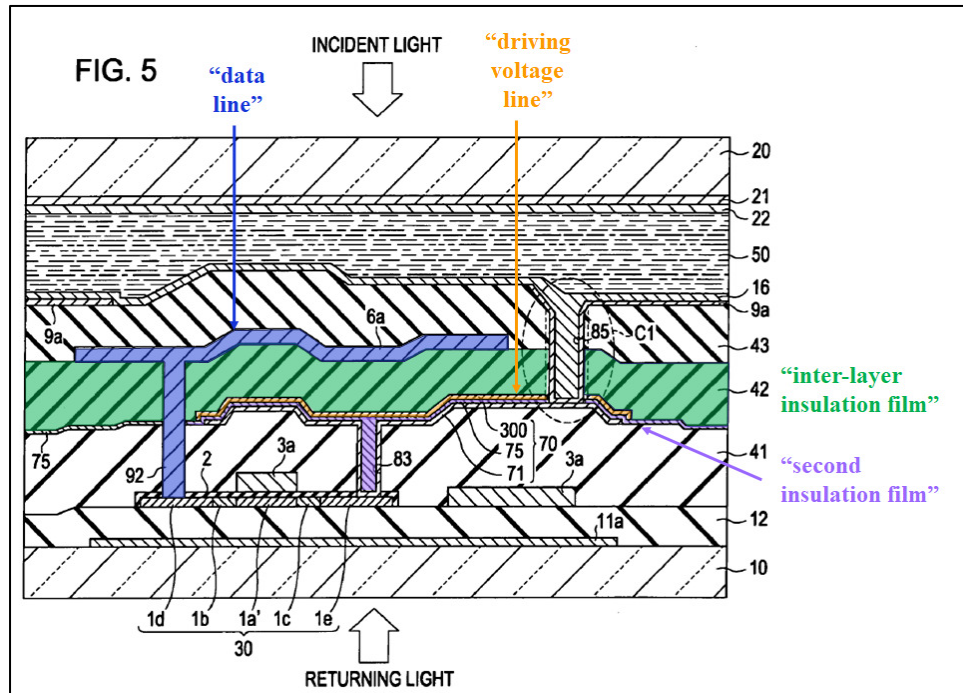
It would have been obvious to a POSITA to extend the data line from the

first source electrode 171 and to form it on the same layer as the first source electrode 171 by using the same material. (See, e.g., EX1016, 8:65-67.) Figure 5 (below) shows the *data line 2* and the *power line 3* (“driving voltage line” (see 3[g])) being insulated by *passivation layer 160* (“inter-layer insulation film” (see 3[e])) and *second inter layer 130* (“second insulation layer”). (EX1002, ¶156.)



b. Ishii100

Ishii100’s “data line 6a to which an image signal S1, S2, ..., or Sn ... is supplied is electrically connected to the source of the TFT 30.” (EX1004, [0047].) Figure 5 (below) shows the *data line 6a* and the *capacitor line 300* (“driving voltage line” (see 3[g])) being insulated by *interlayer insulating film 42* (“inter-layer insulation film” (see 1[d])) and/or *dielectric film 75* (“second insulation layer” (see 1[c])). (EX1002, ¶¶157-159.)



Ishii100's discloses and Figure 4 (below) shows the *data lines 6* crossing the *scanning lines 3a*. “[T]he data lines 6a and the scanning lines 3a are provided along vertical and horizontal boundaries of the pixel electrodes 9a, respectively.” (EX1004, [0052].) Ishii100 discloses “a plurality of scanning lines and a plurality of data lines which intersect one another.” (EX1004, Claim 1.) (EX1002, ¶160.)

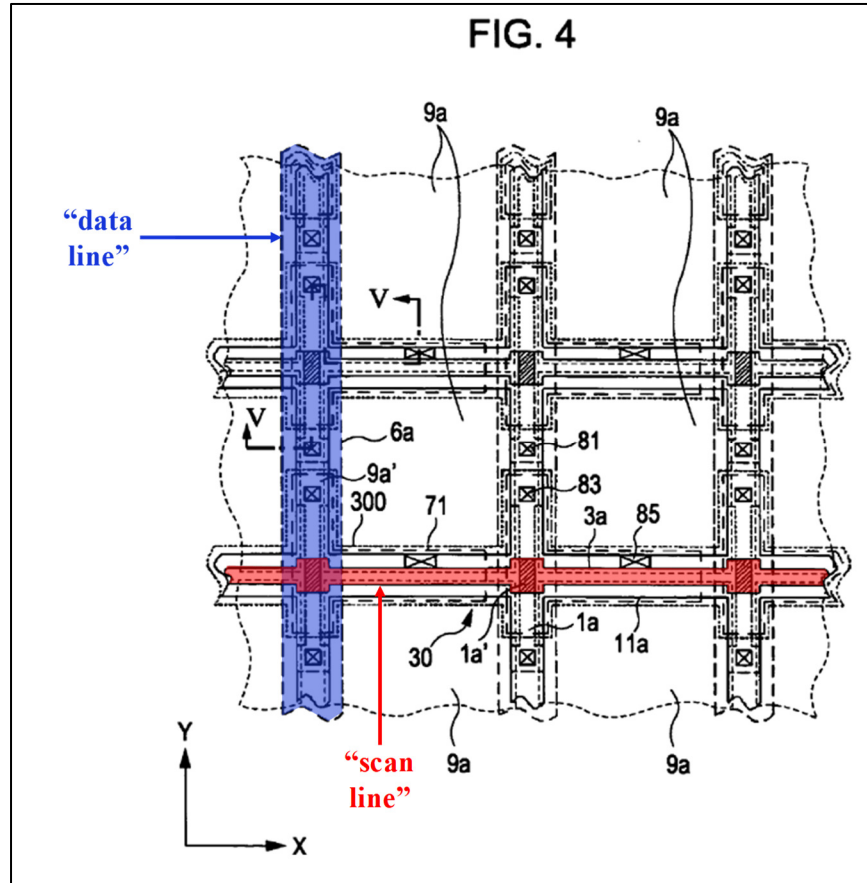
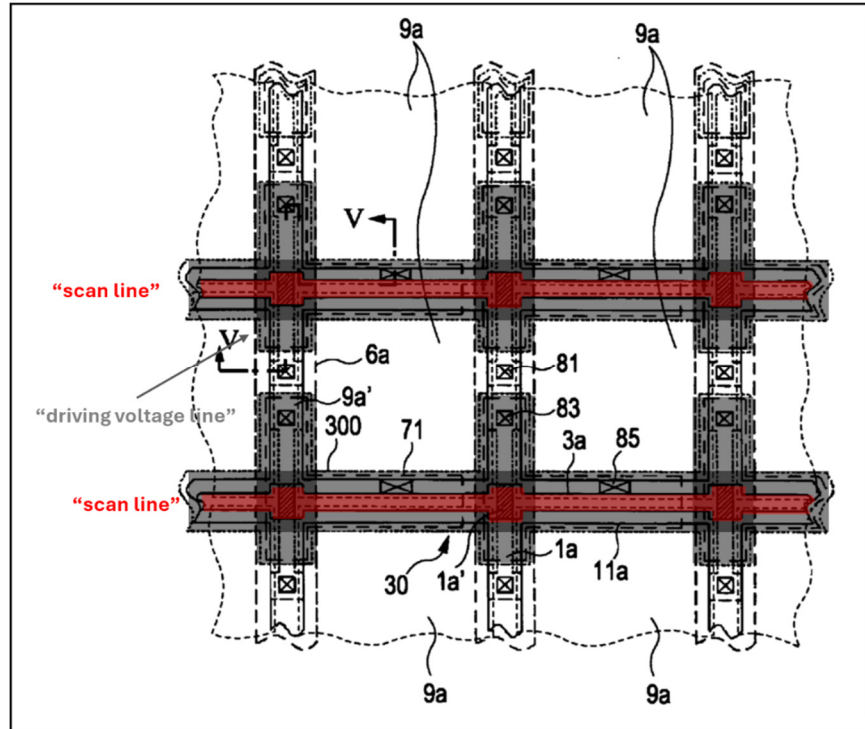


Figure 4 (below) shows the capacitor line 300 (“driving voltage line” (see 3[g])) crosses the *scanning lines 3a*. (EX1002, ¶¶161-162.)



It would have been obvious to a POSITA to combine Park and Ishii100.

(See 3[c].)

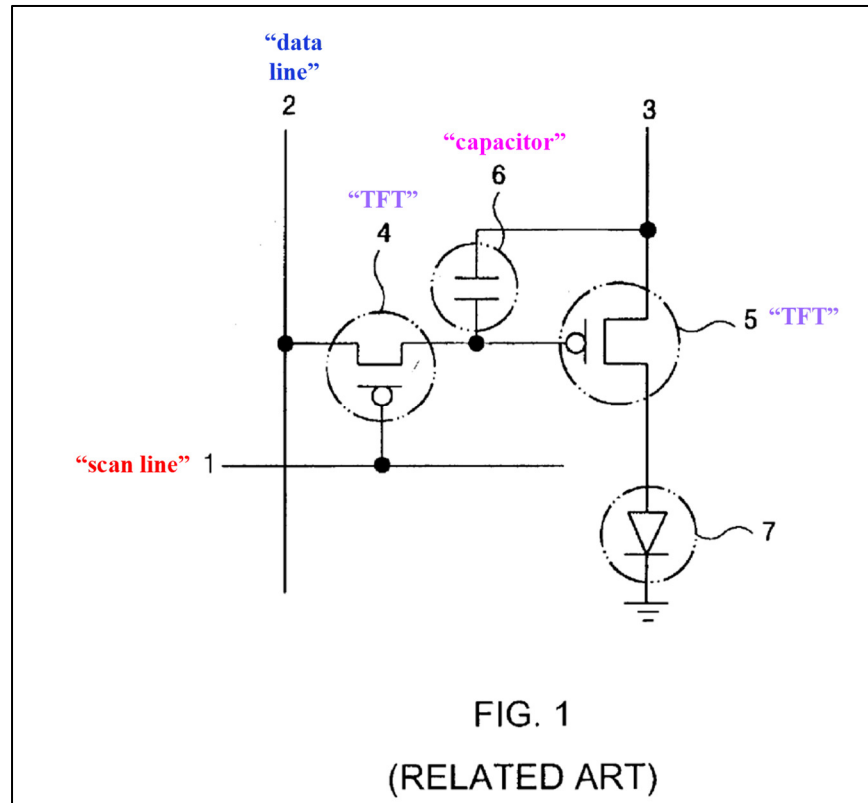
5. 10[e]: “a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;”

a. Park

Park discloses “[i]n FIG. 1 [(below)], a pixel of the active matrix organic electroluminescent display device has a *switching thin film transistor 4*, a *driving thin film transistor 5*, a *storage capacitor 6* and a light emitting diode (LED) 7.

... A gate electrode of the *switching thin film transistor 4* is connected to the *gate lane 1* and a source electrode is connected to the *data line 2*.” (EX1005, [0006];

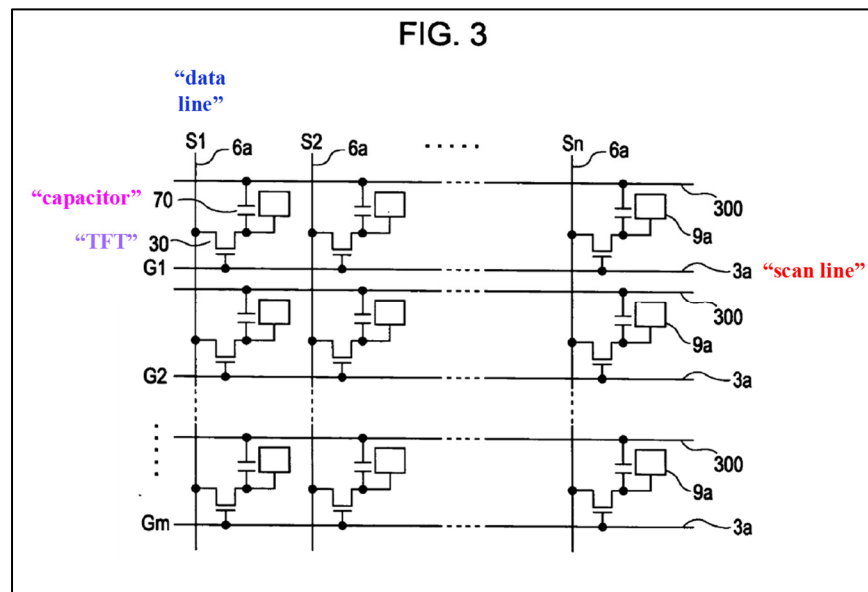
EX1002, ¶¶163-164.)



a. Ishii100

Ishii100 discloses "FIG. 3 shows an equivalent *circuit* of various elements, wiring lines, etc. in a plurality of pixel portions which are formed in a matrix and which constitute the image display region of the liquid crystal device." (EX1004, [0046].) The circuit comprises "a pixel electrode 9a and *a TFT 30* for controlling switching of the pixel electrode 9a are formed, and a *data line 6a* to which an image signal S1, S2, ..., or Sn ... is supplied is electrically connected to the source of the TFT 30." (EX1004, [0047].) "[S]canning lines 3a are electrically connected to the gates of the TFTs 30, and they are configured to sequentially apply scanning signals G1, G2, , and Gm in this order to the scanning lines 3a in

pulses with predetermined timing. *The pixel electrodes 9 are electrically connected to the drains of the TFTs 30 to write the pixel signals S1, S2, . . . and Sn supplied from the data lines 6a.* (EX1004, [0048].) Figure 3 (below) shows the pixel circuit coupled to the *scanning lines 3a* and the *data lines 6a* and comprising at least one *TFT 30* and a *capacitor 70*. (EX1002, ¶¶165-167.)



It would have been obvious to a POSITA to combine Park and Ishii100.

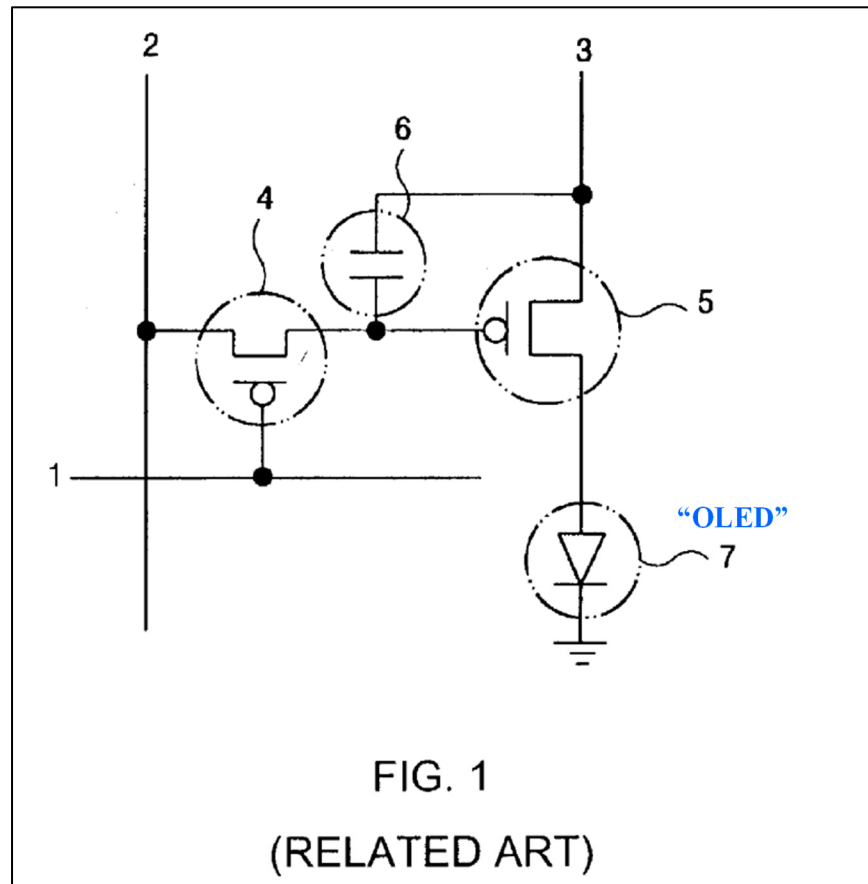
(See 3[c].)

6. 10[f]: “an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

a. Park

Park’s “organic electro luminescence display (ELD) device emits light by recombination of an electron and a hole and thus it is referred to as an organic light emitting diode (OLED).” (EX1005, [0005].) Park discloses “[i]f a signal of the

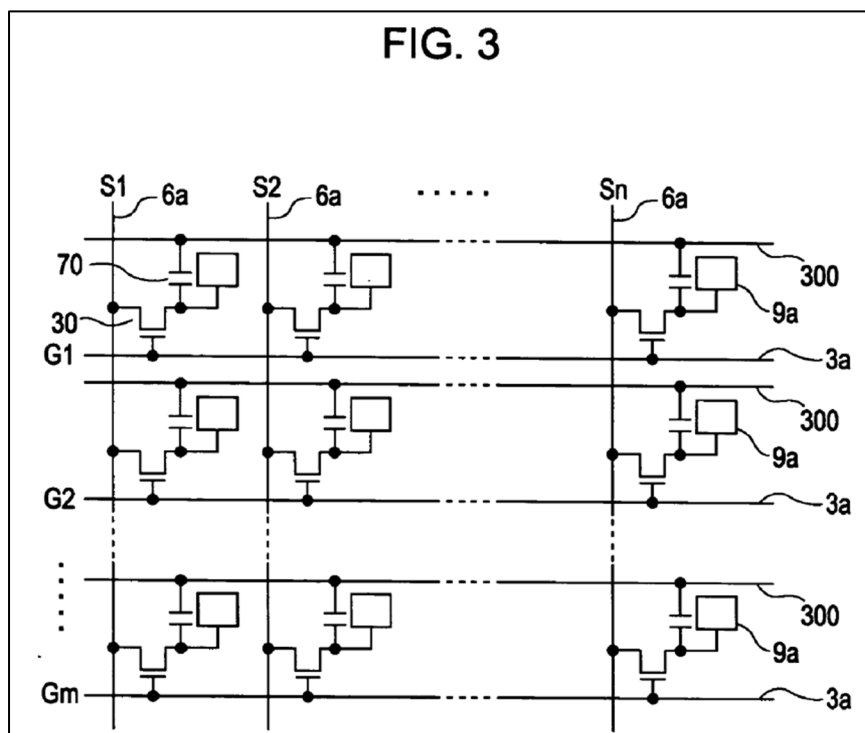
data line 2 is applied to the gate electrode of the driving thin film transistor 5, the driving thin film transistor 5 is turned on and thus the light emitting diode (LED) 7 emits light.” (EX1005, [0006].) Figure 1 (below) shows Park’s OLED receiving the driving voltage from the pixel circuit. (EX1002, ¶168.)



b. Ishii100

Ishii100 discloses “an organic EL display ...” (EX1004, [0097].) Ishii100 discloses “[i]f an electro optical device is in a normally white mode, the transmittance to incident light decreases according to voltage applied in units of pixels, and if the electro-optical device is in a normally black mode, the

transmittance to incident light increases according to voltage applied in units of pixels. As a result, light with a contrast according to image signals is emitted from the whole electro-optical device.” (EX1004, [0049].) Figure 3 (below) shows a part of the pixel electrode 9a receiving the driving voltage from the pixel circuit. (EX1002, ¶¶169-171.)



It would have been obvious to a POSITA to combine Park and Ishii100.

(See 3[c].)

F. Claims 11-14: “The OLED display of claim 10, wherein the opening overlaps with the lower electrode.”

Claim 11, elements 12[pre]-12[j], claim 13, and claim 14 are similar to claim 2, elements 10[pre], 1[a]/3[a], 1[b]/3[b], 10[c]-10[f], 3[c], 1[e]/3[e], 1[f]/3[f], 3[g],

claim 4, and claims 1/3/5/10, respectively, which Park and/or Ishii100 teach.

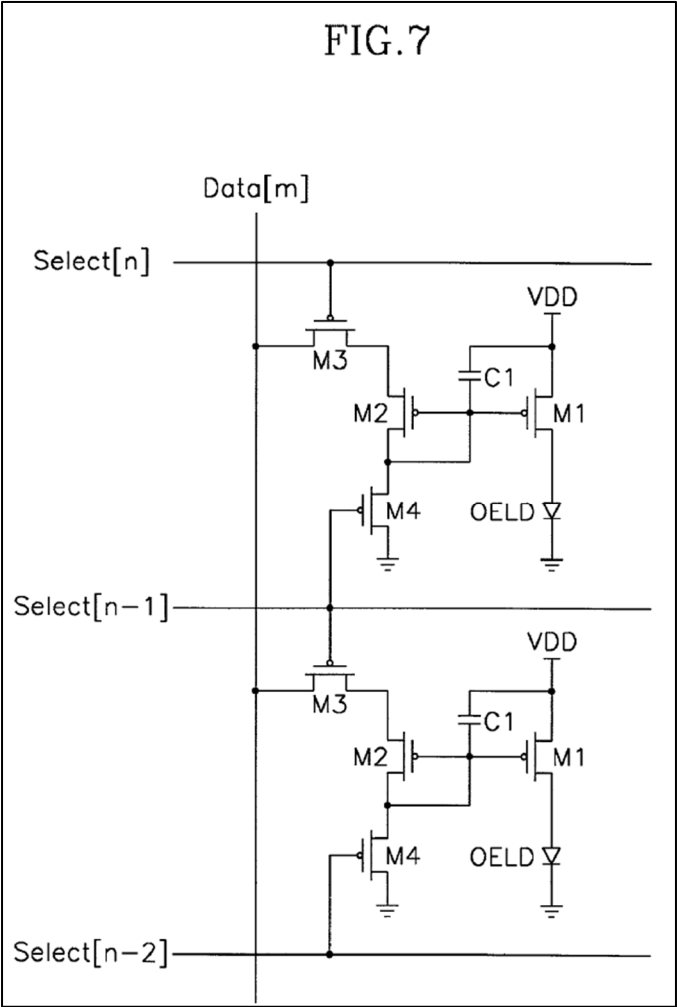
(EX1002, ¶¶175-200.)

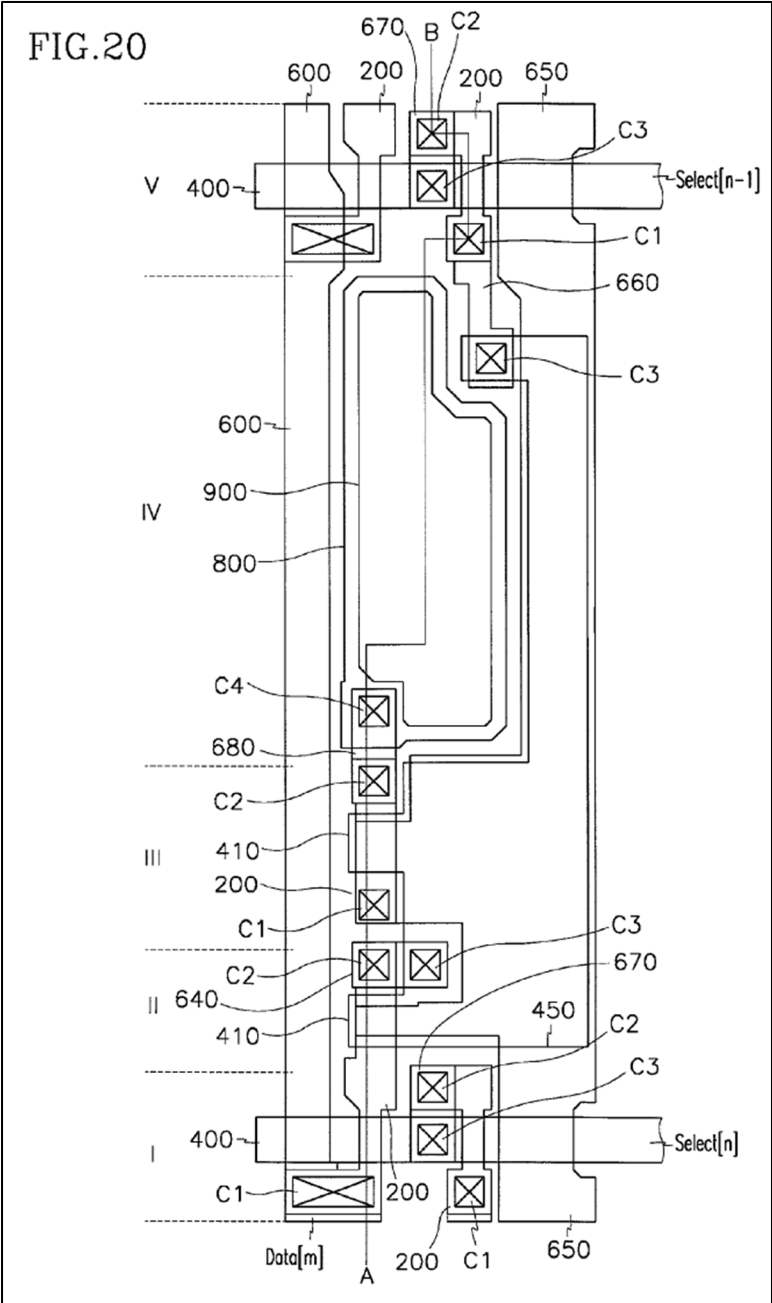
VIII. GROUND 4: PARK, ISHII100, AND KWON RENDER OBVIOUS CLAIMS 6-9 AND 15-19

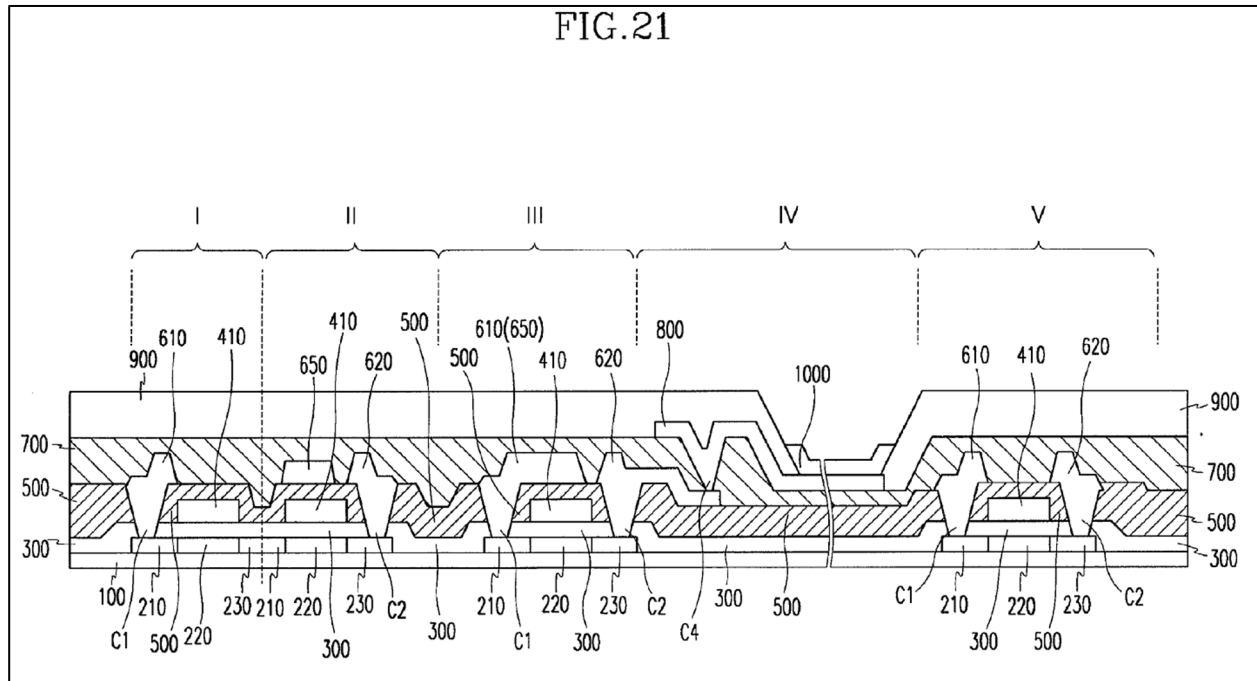
A. Summary Of Kwon

Kwon discloses “an organic EL display (OELD), its driving methods and a pixel circuit that can compensate for deviation of the threshold voltage of a thin film transistor (TFT) and achieve high gray scale display when driving the pixels of the OELD using the TFT.” (EX1006, [0002].) Kwon explains “it is difficult for the conventional pixel circuit to achieve high gray scale because the threshold voltage V_{TH} of the TFT varies depending on the manufacturing process thereof.” (EX1006, [0011].) Kwon “provide[s] an OELD for compensating for deviations of the threshold voltage of the TFT and displaying high gray scale.” (EX1006, [0012]; EX1002, ¶201.)

Figures 7, 20, and 21 (below) show the pixel circuit, and plan and cross-sectional views of the OLED. (EX1002, ¶202.)





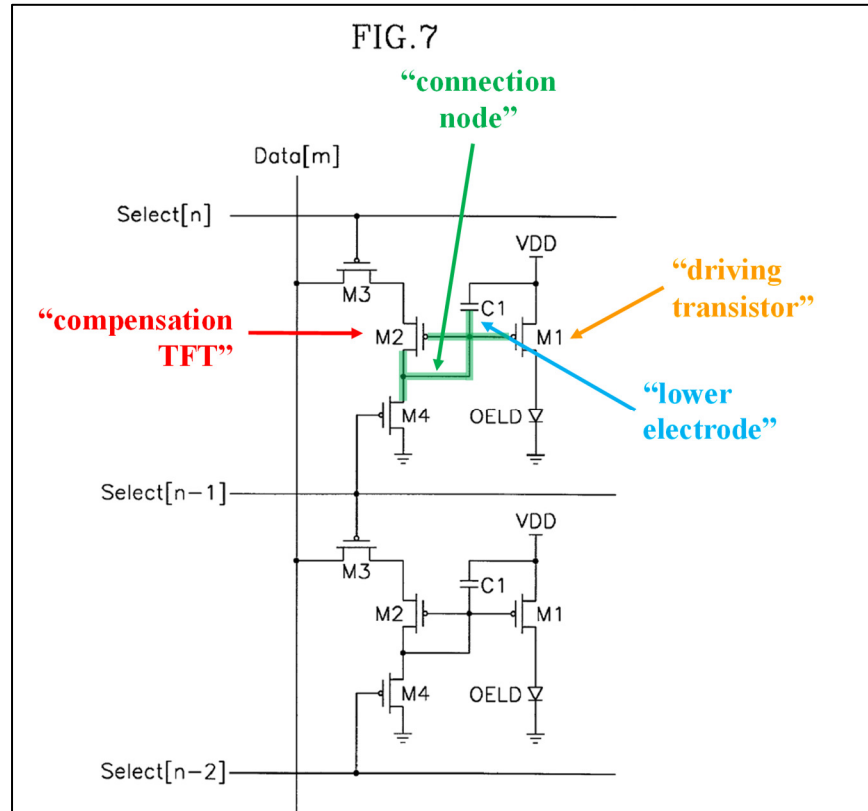


B. Claim 6: “The TFT array substrate of claim 5, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”

Park teaches a connection node electrically couples a driving thin film transistor 5 to the lower electrode of a capacitor 6. (*See* 1[g].) Ishii100 similarly teaches a connection node that electrically couples a TFT 30 to a lower electrode of a capacitor 70. (*See* 1[c]; EX1002, ¶203.)

To the extent that neither Park nor Ishii100 teaches the claimed “compensation TFT,” Kwon teaches it. Figure 7 (below) shows *transistor M2* coupled to *driving transistor M1* and electrically coupled to the *lower electrode* of capacitor C1 through the *connection node*. Kwon’s “transistor M2 compensates

for deviations of the threshold voltage of the transistor M1 for supplying the current.” (EX1006, [0046].) (EX1002, ¶204.)



It would have been obvious to a POSITA to combine the teachings of Park and Ishii100 with Kwon. These references disclose light emitting devices and pixel circuits to operate such devices. Park discloses “an active matrix organic electro luminescent display (ELD) device having thin film transistors.” (EX1005, [0017].) Ishii100 discloses an “electro-optical device” and a “liquid crystal device of a TFT active matrix drive system with a built-in drive circuit.” (EX1004, [0007], [0038], [0097].) Kwon discloses “an organic electroluminescent (EL) display, a driving method of the EL display and a pixel circuit of the EL display.”

(EX1006, [0002].) Thus, Park, Ishii100, and Kwon are in the same field of endeavor. (EX1002, ¶205.)

Park teaches a pixel circuit comprising “a switching thin film transistor 4, a driving thin film transistor 5, a storage capacitor 6 and a light emitting diode (LED) 7.” (EX1005, [0006].) Ishii100 teaches a pixel circuit comprising “a pixel electrode 9a and a TFT 30 for controlling switching of the pixel electrode 9a are formed.” (EX1004, [0047].) Kwon teaches a “pixel circuit compris[ing] a current supplying transistor M1 and a threshold voltage compensation transistor M2 of PMOS transistors, and switches S1 and S2 of PMOS transistors M3 and M4.” (EX1006, [0056]; EX1002, ¶206.)

Kwon explains that “it is difficult for the conventional pixel circuit to achieve high gray scale because the threshold voltage V of the TFT varies depending on the manufacturing process thereof.” (EX1006, [0011].) A POSITA would have understood Park’s teachings similarly apply to a conventional pixel circuit. (EX1005, Fig. 1 (“Related Art”).) Kwon teaches “pixel circuit that can compensate for deviation of the threshold voltage of a thin film transistor (TFT) and achieve high gray scale display when driving the pixels of the OLED by using the TFT.” (EX1006, [0002].) Kwon’s pixel circuit includes an additional transistor M4 that resets the gate voltage of the driving transistor M1 and a threshold voltage compensation transistor M1 to achieve high gray scale display.

(EX1006, [0056]-[0057].) Kwon's technical features may be combined with the teachings of Park and Ishii100 to generate a display device with high gray scale display by including circuitry in the pixel circuit to compensate for any deviations in the threshold voltage of the driving TFT. The combination of Park, Ishii100, and Kwon results in a display device with high gray scale display. There would have been a reasonable expectation of success because such techniques were known in the prior art and have been successfully demonstrated, and given there is an overlap among Park, Ishii100, and Kwon including with their circuits and use for active matrix display devices. (EX1002, ¶207.)

Because Park, Ishii100, and Kwon have similar circuits, a POSITA would have been motivated to use the technique disclosed in Kwon to improve the similar devices of Park and Ishii100 in the same way. Thus, it would have been obvious to a POSITA to combine Park, Ishii100, and Kwon. (EX1002, ¶208.)

C. Claim 7: “The TFT array substrate of claim 6, wherein a compensation gate electrode of the compensation TFT is formed from the same layer as the lower electrode.”

Kwon's “first capacitor electrode 450 is patterned on the same layer with the same material as the scan line 400. The gate electrodes 410 are respectively formed on the portions where the first capacitor electrode 450 is superimposed with the polycrystal silicon layer 200 of the II and III regions.” (EX1006, [0093]; EX1002, ¶209.)

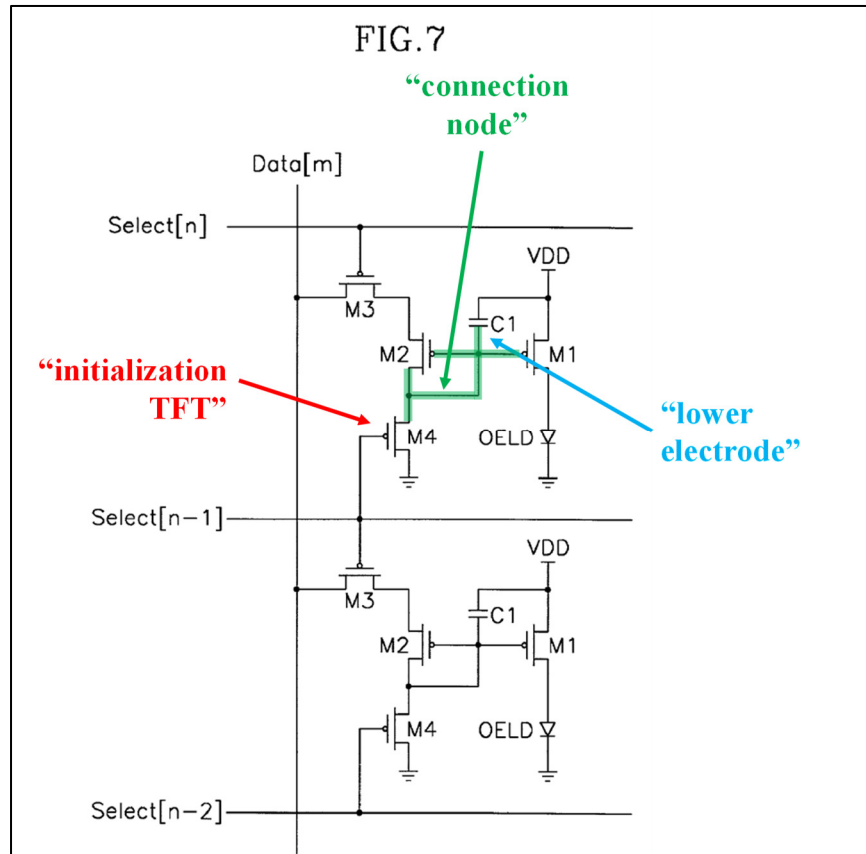
It would have been obvious to combine Park, Ishii100, and Kwon. (*See* claim 6.)

D. Claim 8

1. **8[a]: “The TFT array substrate of claim 5, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”**

Park teaches a connection node electrically coupling the lower electrode of a capacitor 6 to a driving thin film transistor 5 and a switching thin film transistor 4. (*See* 1[g].) Ishii100 similarly teaches a connection node electrically coupling the lower electrode of a capacitor 70 to a TFT 30. (*See* 1[c]; EX1002, ¶210.)

To the extent that neither Park nor Ishii100 teaches an “initialization TFT electrically coupled to the lower electrode through the connection node,” Kwon teaches it. Figure 7 (below) shows a *connection node* electrically coupling the *lower electrode* of capacitor C1 to *transistor M4*. Transistor M4 is an initialization TFT because transistor M4 resets (initializes) the gate of current driving transistor M1. (EX1006, [0060], [0057].) “[T]he current flows to the OLED via the transistor M1 to emit light.” (EX1006, [0050]; EX1002, ¶211.)

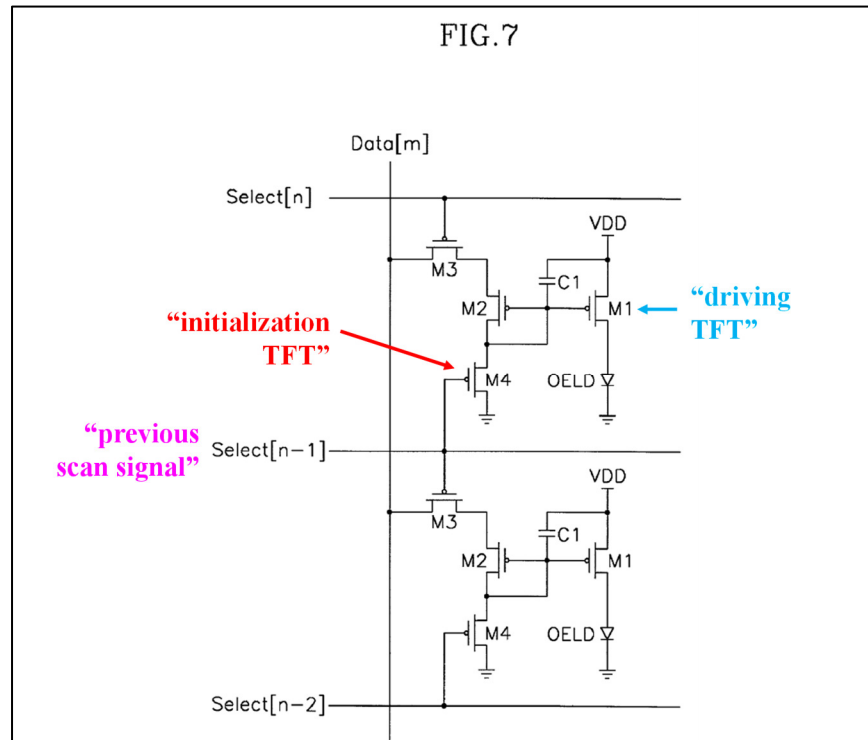


2. 8[b]: “wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”

Kwon’s “external reset signal Reset is supplied to the gate of the transistor M4 to initialize the node A into a ground level.” (EX1006, [0060].) Figure 7 (below) shows the **transistor M4** (“initialization TFT” (see 8[a])) is configured to provide a ground level (“initialization voltage”) to the gate of **transistor M1** (“driving TFT” (see 8[a])). The pixel circuit of Figure 7 “uses the Select Signal $Select[n-1]$ of the previous Scan line instead of an additional external reset Signal Reset, and Supplies the select signal $Select[n-1]$ to the gate of the transistor M4.”

(EX1006, [0063].) The gate of transistor M4 is coupled to, and thus, turned on in response to, the previous signal on the *Select[n-1] line* (“previous scan signal”).

(EX1002, ¶¶212-216.)

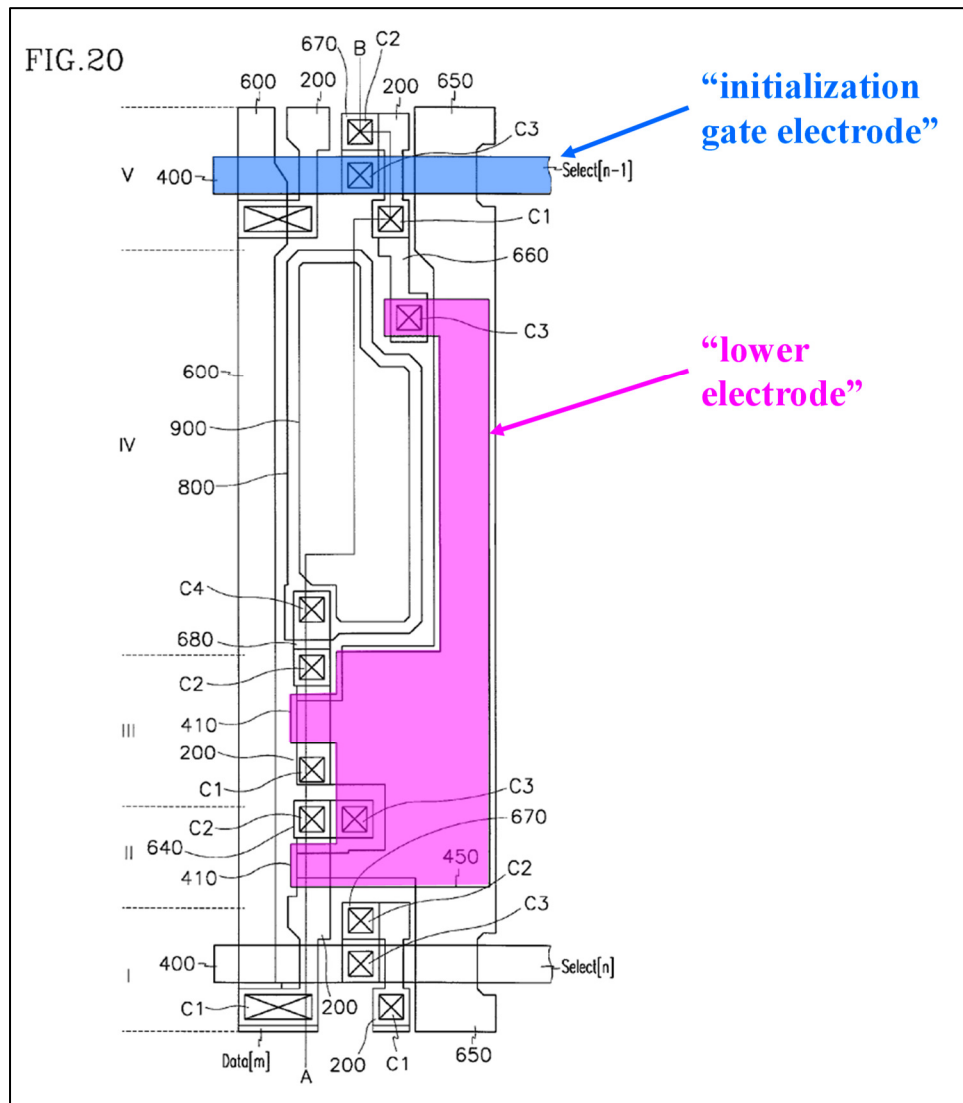


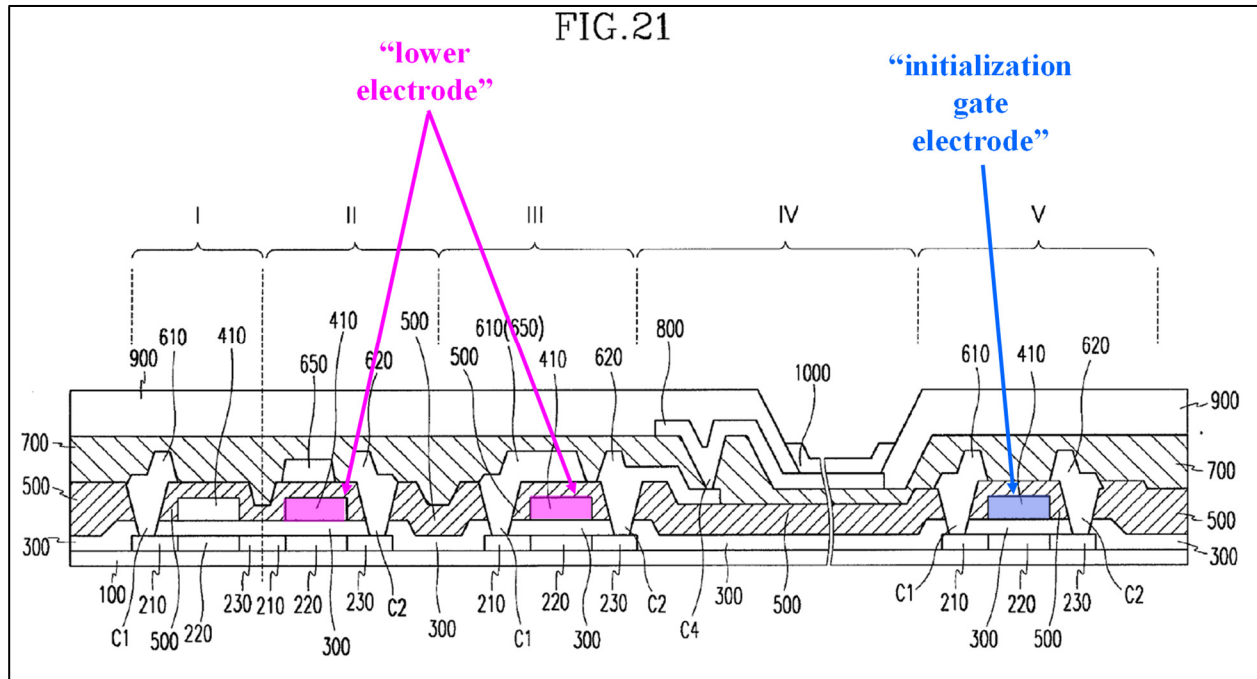
It would have been obvious to combine Park, Ishii¹⁰⁰, and Kwon. (*See* claim 6.)

E. Claim 9: “The TFT array substrate of claim 8, wherein an initialization gate electrode of the initialization TFT is formed from the same layer as the lower electrode.”

Kwon’s “[g]ate electrodes 410 are respectively formed on portions where the scan lines 400 are superimposed with the polycrystalline silicon layer 200 in the I and V regions.” (EX1006, [0093].) One gate electrode is the gate electrode for transistor M4 (“initialization TFT” (see 8[a])). Kwon discloses “a *first*

capacitor electrode 450 is patterned on the same layer with the same material as the scan line 400. The gate electrodes 410 are respectively formed on the portions where the first capacitor electrode 450 is superimposed with the polycrystal silicon layer 200 of the II and III regions.” (EX1006, [0093].) Figures 20 and 21 (below) show the *gate of the transistor M4 (400)* is formed from the same layer as the *capacitor electrode 450*. (EX1002, ¶¶217-218.)





It would have been obvious to combine Park, Ishii100, and Kwon. (See claim 6.)

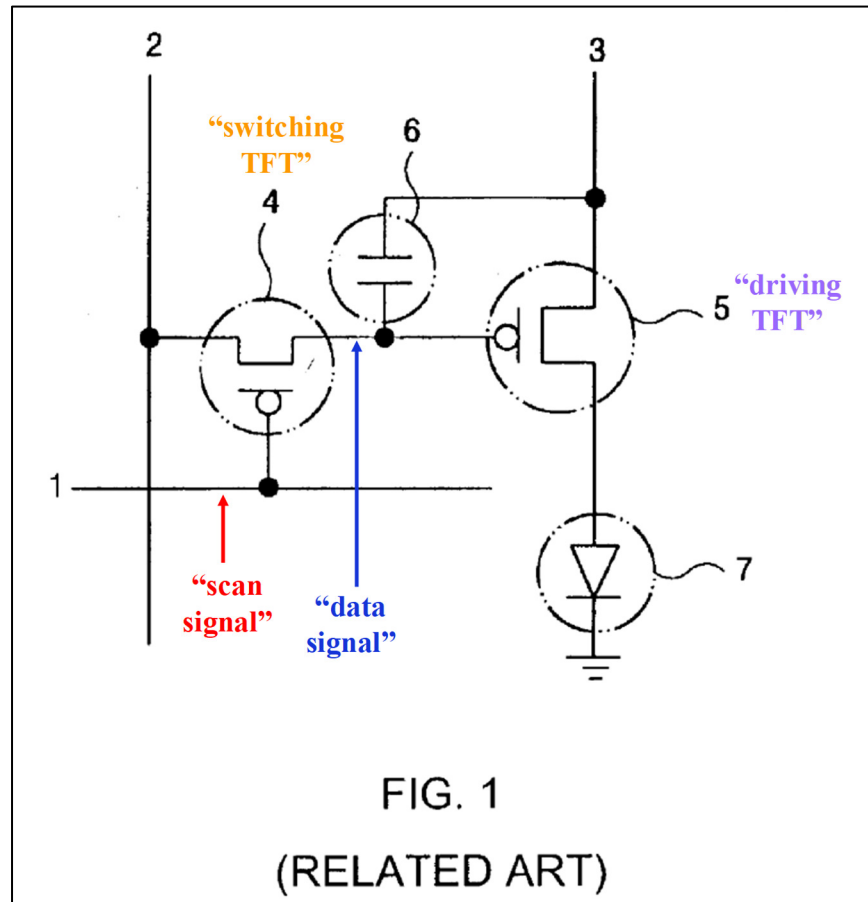
F. Claims 15-18

Claims 15-18 are similar to claims 6-9, which Kwon teaches. (EX1002, ¶¶219-226.)

G. Claim 19: “The OLED display of claim 14, further comprising a switching TFT for delivering the data signal to the driving TFT by being turned on by the scan signal.”

Park discloses a switching thin film transistor 4. “If a signal is applied to the gate line 1, the switching thin film transistor 4 is turned on. If a signal of the data line 2 is applied to the gate electrode of the driving thin film transistor 5, the driving thin film transistor 5 is turned on and thus the light emitting diode (LED) 7 emits light.” (EX1005, [0006].) Figure 1 (below) shows a *switching thin film*

transistor 4 for delivering the *signal of the data line 2* to the *driving thin film transistor 5* by being turned on by the *signal of the gate line 1* (“scan signal” (see 10[c])). (EX1002, ¶¶227-229.)



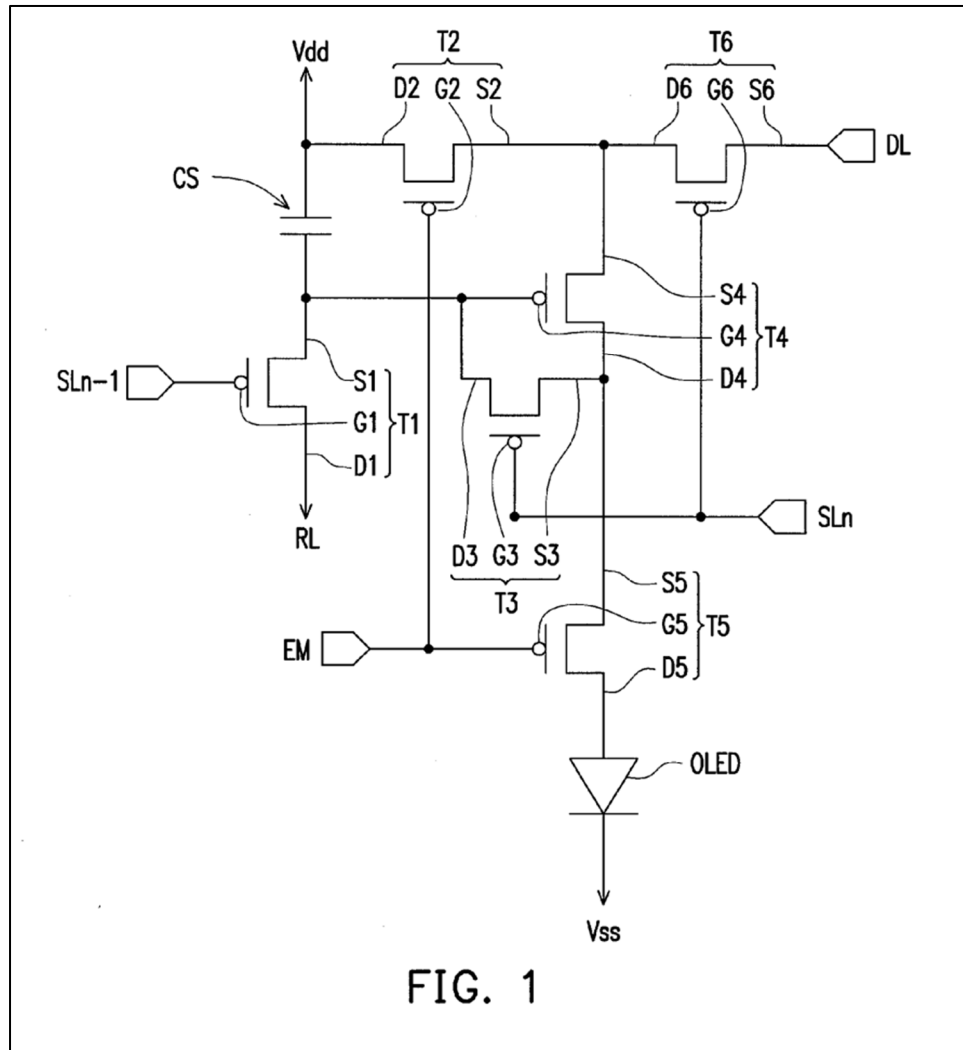
IX. GROUND 5: LIU AND ONO RENDER OBVIOUS CLAIMS 1-6, 8, AND 10-19

A. Summary Of Liu

Liu discloses a “pixel structure [that] is applied to an organic electro luminescence display device and has a structure comprising six thin film transistors and one capacitor.” (EX1007, [0032].) The “pixel structure ... is usually driven by the cooperation of a plurality of thin film transistors (TFTs) and a capacitor.”

(EX1007, [0006].) However, the plurality of TFTs occupies much of the area in a pixel structure, leaving “no extra space for disposing other components.” (*Id.*) Additionally, “the pixel circuit structure can not be miniaturized easily and thus can not be applied in displays with high resolution.” (*Id.*; EX1002, ¶¶230-231.)

Liu’s pixel structure is “capable of reducing an area occupied by components of the pixel structure.” (EX1007, [0007].) Figure 1 (below) is “a schematic circuit diagram of a pixel structure” “comprising six thin film transistors and one capacitor.” (EX1007, [0013], [0032]; EX1002, ¶232.)



Figures 8 and 10 (below) show top and cross-sectional views, respectively, of Liu's pixel structure. (EX1002, ¶233.)

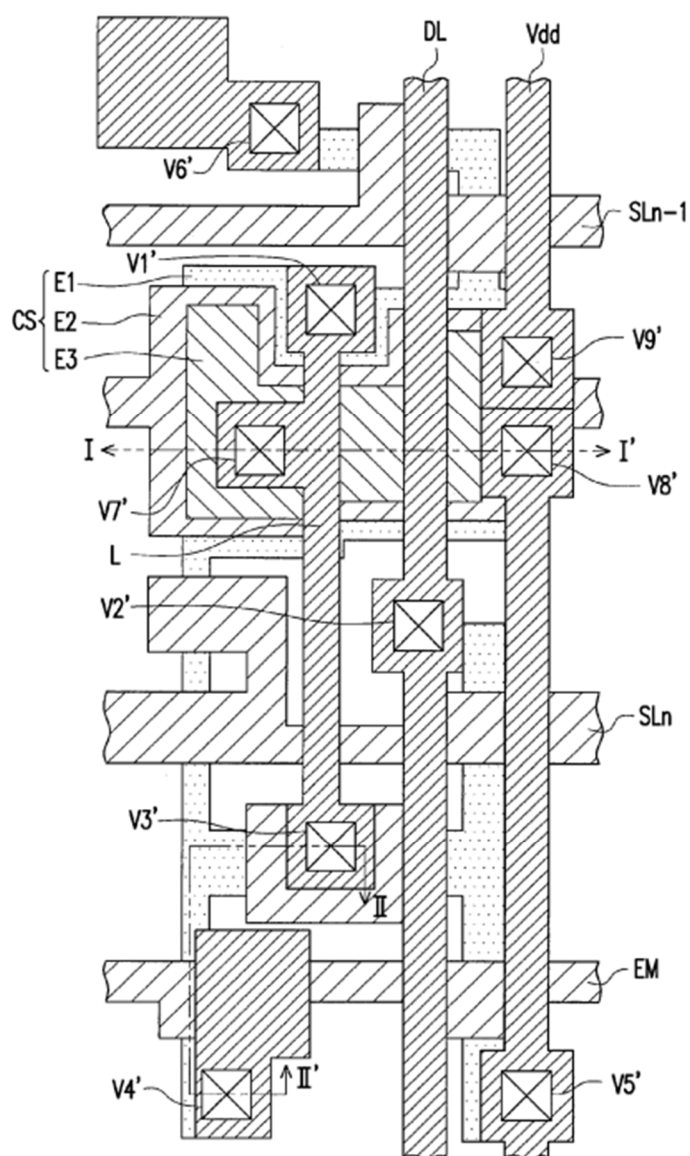
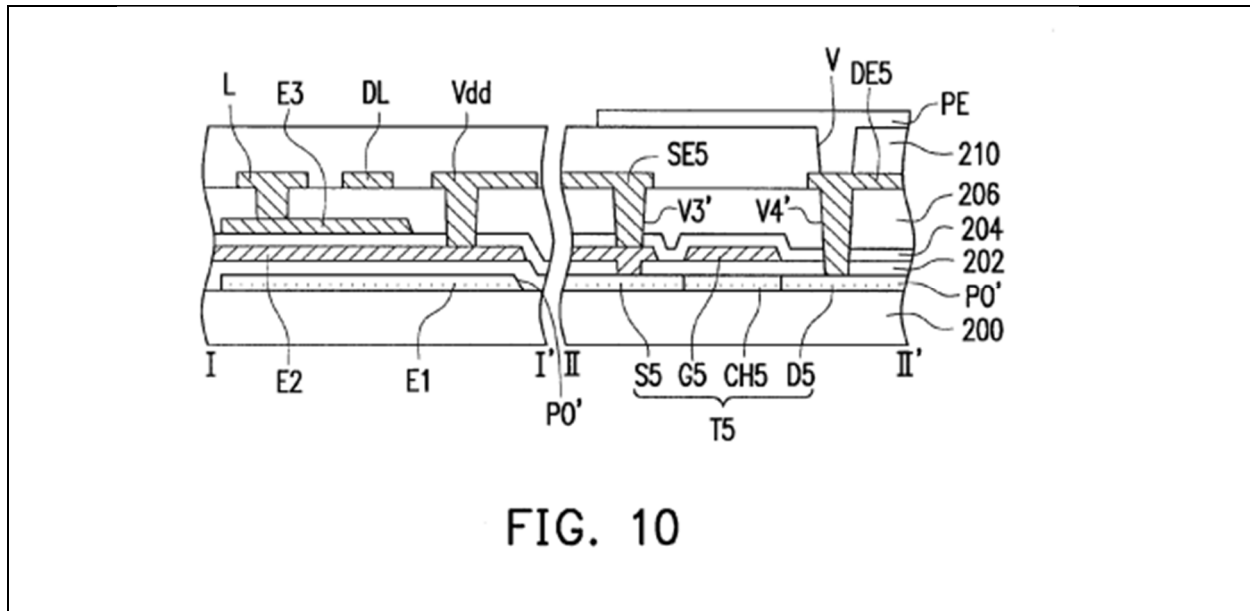


FIG. 8



B. Summary Of Ono

Ono is directed to “an active-matrix luminescent display device which includes a luminescent element and a driving circuit having a capacitor and a thin-film transistor.” (EX1008, [0003], [0046]; EX1002, ¶234.)

Ono explains conventional active-matrix luminescent display devices include, “for each luminescent element, a driving circuit for driving the luminescent element.” (EX1008, [0005].) “The driving circuit generally includes: a switching transistor which selects a pixel for producing luminescence; a driving transistor which drives a luminescent element; and a capacitor. The driving circuit includes, for example, a capacitor which holds a voltage for determining an amount of current passed by the driving transistor.” (EX1008, [0006]; EX1002, ¶235.)

Ono recognizes, however, this arrangement results in less design flexibility

because it dedicates a region to the capacitor. (EX1008, [0008].) Therefore, “when the number of capacitors or the capacitor area increases, the region for forming other elements becomes smaller.” (*Id.*) Accordingly, Ono discloses “a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor.” (EX1008, [0010].) Ono teaches forming the capacitor in a region above the driving transistor and includes the gate electrode of the driving transistor for different pixel circuits. (EX1008, [0050], [0070], Fig. 3, Fig. 4, [0091], Fig. 6, Fig. 7, [0113], Fig. 8, Fig. 9, [0124], Figs. 10-12; EX1002, ¶236.)

C. Claim 1

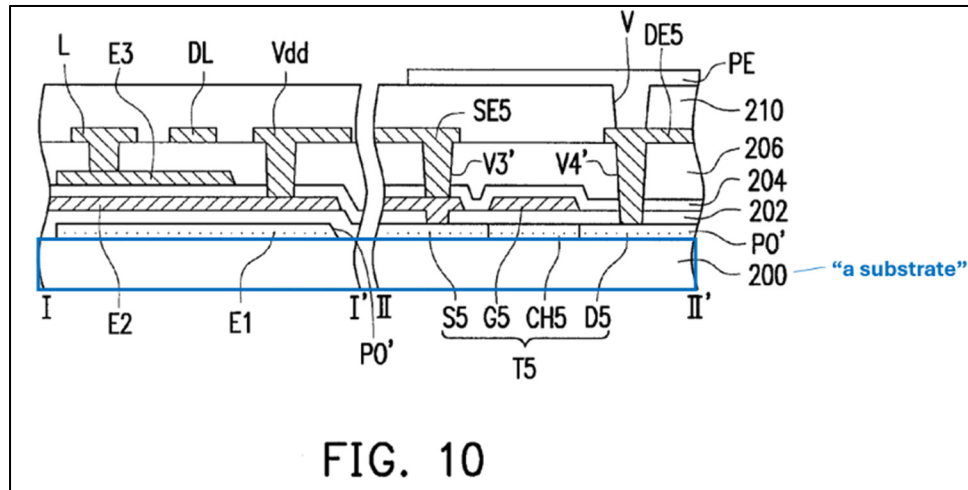
1. Preamble: “A thin film transistor (TFT) array substrate comprising:”

To the extent the preamble is limiting (which Petitioner does not concede), Liu teaches the preamble.

Liu discloses a “pixel structure [] applied to an organic electroluminescence display and has a structure comprising six thin film transistors” (EX1007, [0032].) “[T]he pixel structure is disposed on a substrate 200.” (EX1007, [0058]; EX1002, ¶¶237-239.)

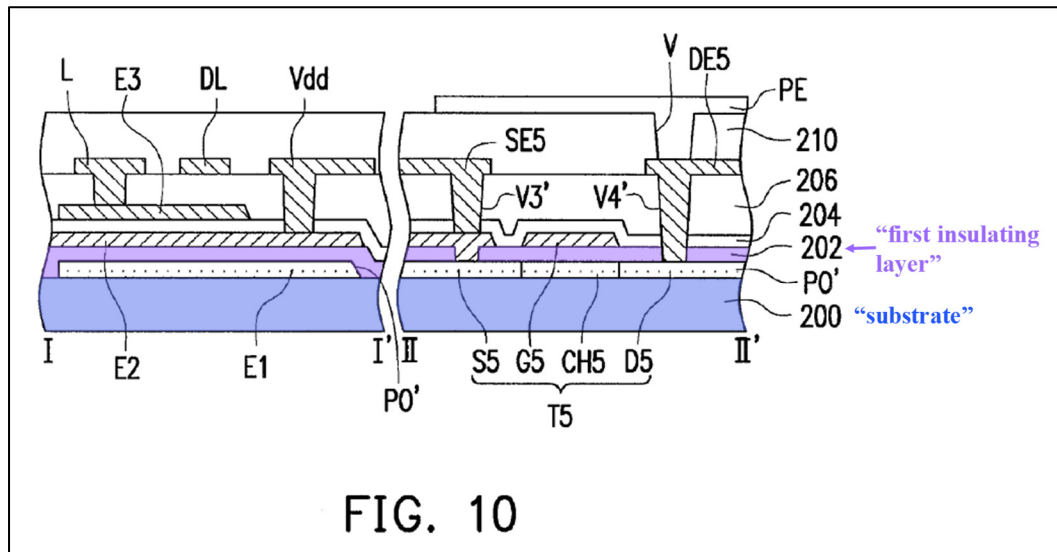
2. 1[a]: “a substrate;”

Liu’s “pixel structure is disposed on a *substrate 200*” (Figure 10 (below)). (EX1011), [0058]; EX1002, ¶241.)



3. 1[b]: “a first insulation layer on the substrate;”

Liu’s “first insulating layer 202 covers the semiconductor layer PO’ and has a material similar to or the same with the material of the first insulating layer 102 as described in the first embodiment.” (EX1007, [0062].) Figure 10 (below) shows *insulating layer 202* on the *substrate 200*. (EX1002, ¶¶242-244.)



4. 1[c]: “a capacitor comprising a lower electrode on the first insulation layer, and an upper electrode arranged to overlap with the whole lower electrode, the upper electrode extending beyond an edge of the lower electrode and having an opening, wherein the upper electrode is insulated from the lower electrode by a second insulation layer;”

- a. Liu

Liu’s “*capacitor CS* is formed with the first *electrode E1* of the semiconductor layer PO”, the second *electrode E2* of the first conductive layer M1” and the third *electrode E3* of the second conductive layer M2, and the first *insulating layer 202* between the first electrode E1 of the semiconductor layer PO’ and the second electrode E2 of the first conductive layer M1” and the second *insulating layer 204* between the second electrode E2 of the first conductive layer M1” and the third electrode E3 of the second conductive layer M2’ serve as capacitor dielectric layers of the capacitor CS.” (EX1007, [0066].) Figure 1 (below) shows *capacitor CS*. (EX1002, ¶¶245-246.)

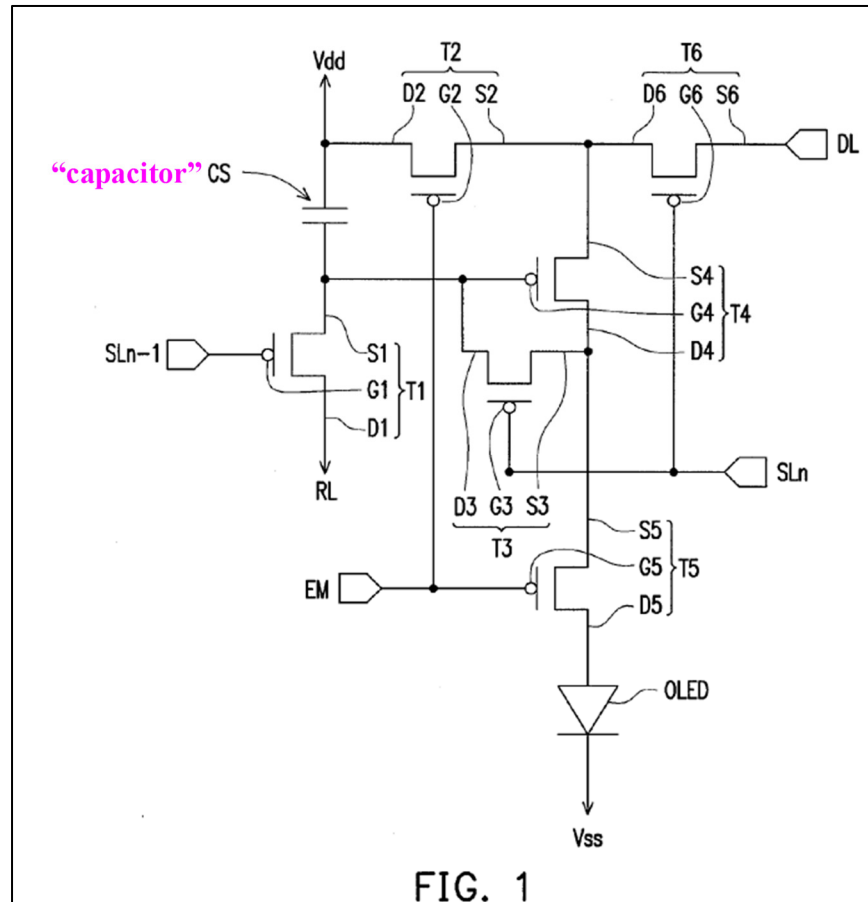
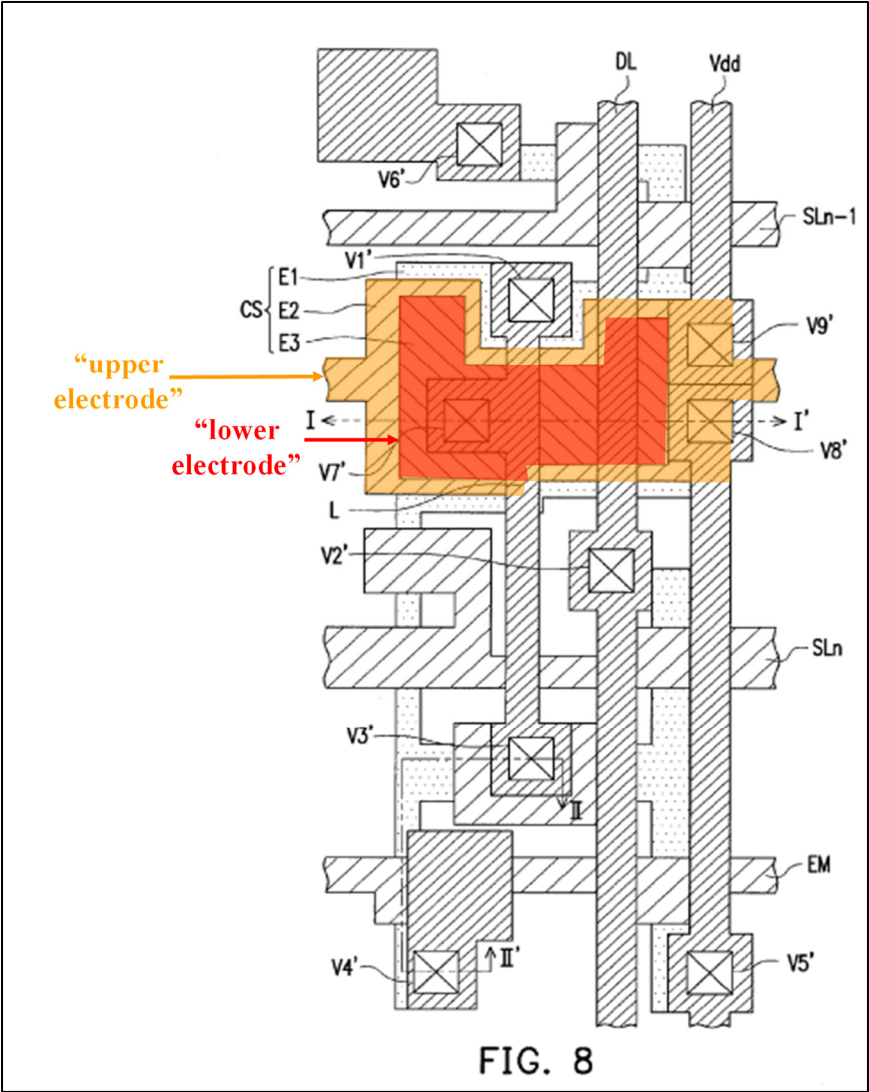
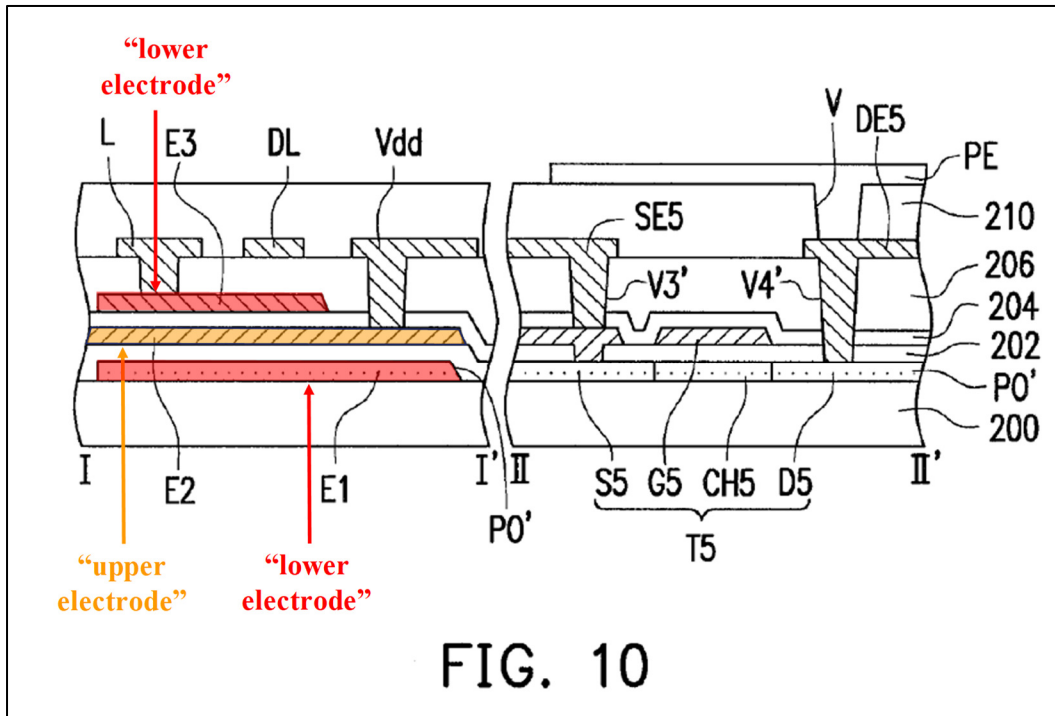


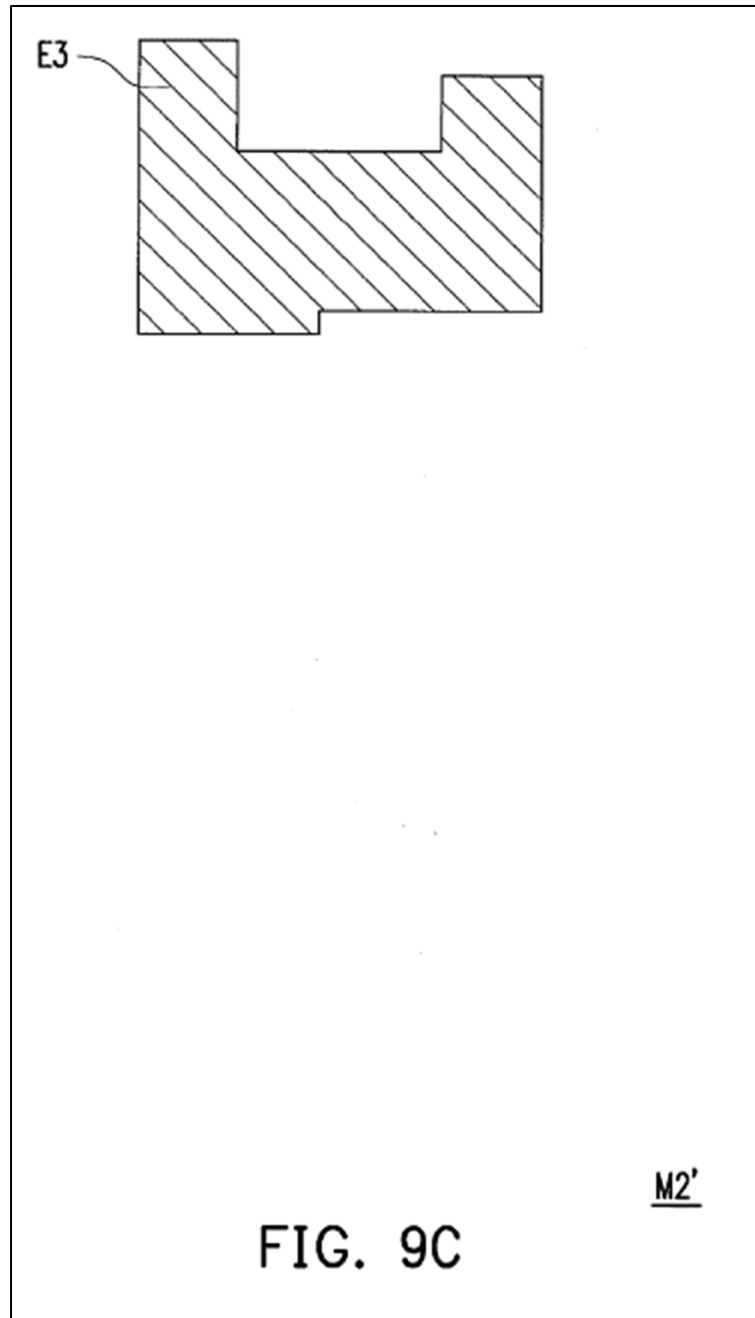
Figure 10 (below) shows *electrode E3* (“lower electrode”) on *insulating layer 202* (“first insulation layer” (see 1[b])) and insulated from *electrode E2* (“upper electrode”) by *insulating layer 204* (“second insulation layer”). (EX1002, ¶247.)

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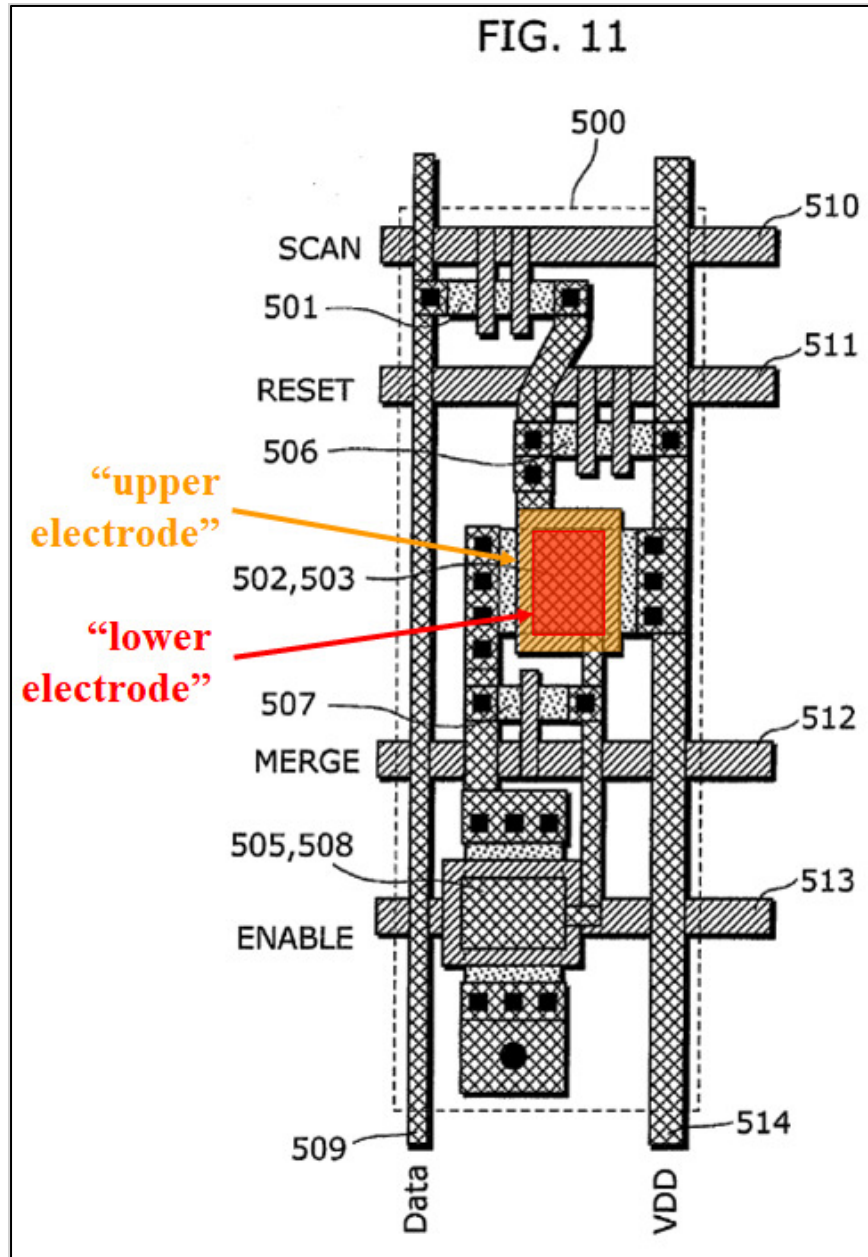
Liu's M2' layer "mainly comprises a third electrode E3 of the capacitor CS" and "is a top view showing a second conductive layer of the pixel structure in FIG. 8" and (EX1007, [0057], [0066].) The M2' layer (Figure 9C (below)) has a large region below electrode E3 that is unoccupied. (EX1002, ¶248.)



b. Ono

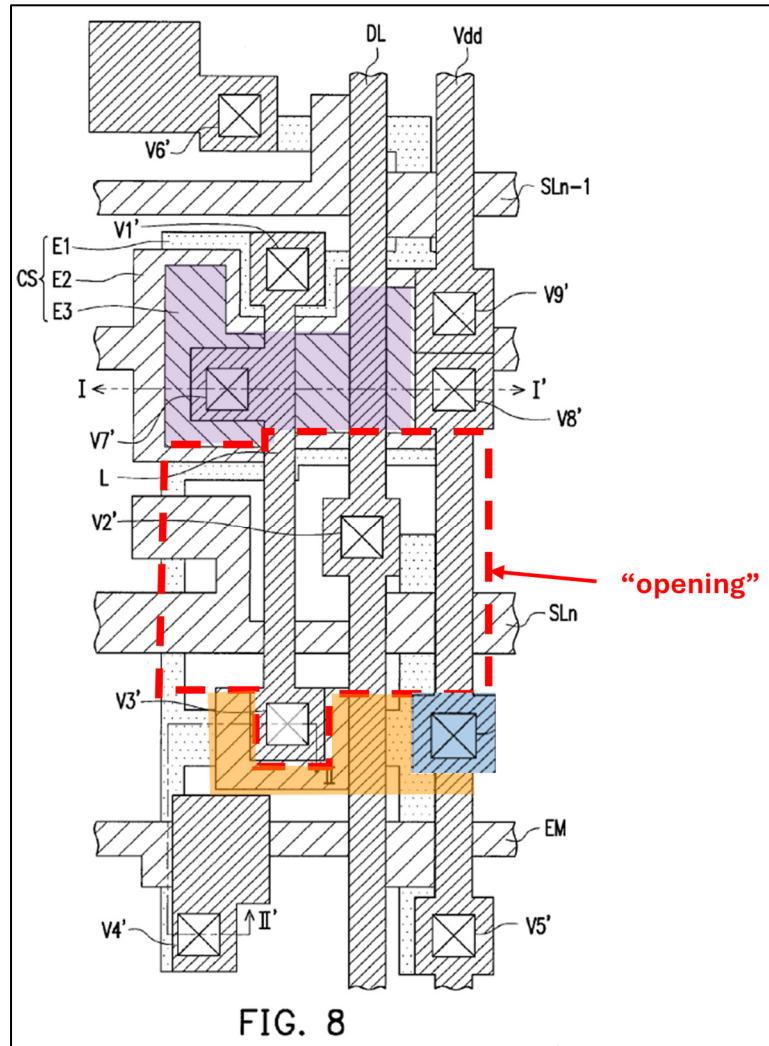
To the extent that Liu does not teach “a capacitor . . . having an opening,” Ono teaches it. Ono discloses “a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a

new region dedicated to the capacitor.” (EX1008, [0030].) Figure 11 (below) of Ono shows a *capacitor electrode 502* (“upper electrode”) over the gate of a *driving thin film transistor 503* (“lower electrode”). Ono’s “driving transistor 503 and the capacitor 502 are formed in the same region in the plane to overlap each other.” (EX1008, [0140]; *also* EX1008, [0107], Figs. 3-10, 12.) Thus, Ono teaches including the upper electrode of the capacitor over the gate of a driving TFT. (EX1002, ¶249.)



The Liu-Ono combination results in extending Liu's electrode E2 to be on top of the driving transistor T4, as taught by Ono. Modified Figure 8 (below) shows the extended *upper electrode* according to the Liu-Ono combination and an *opening*. It would have been obvious to a POSITA to include an opening in the electrode of a capacitor. Liu's "layout of the first conductive layer M1' is shown in

FIG. 9B, which mainly comprises gates of the six thin film transistors.” (EX1007, [0063].) “[T]he first conductive layer M1’ has a gate G4 in the region predetermined for forming the fourth thin film transistor T4.” (EX1007, [0064]; EX1002, ¶¶250-254.)



c. Motivation to combine Liu and Ono

It would have been obvious to combine Liu and Ono to extend electrode E2 in the space above the gate of the transistor T4 to increase the total capacitance.

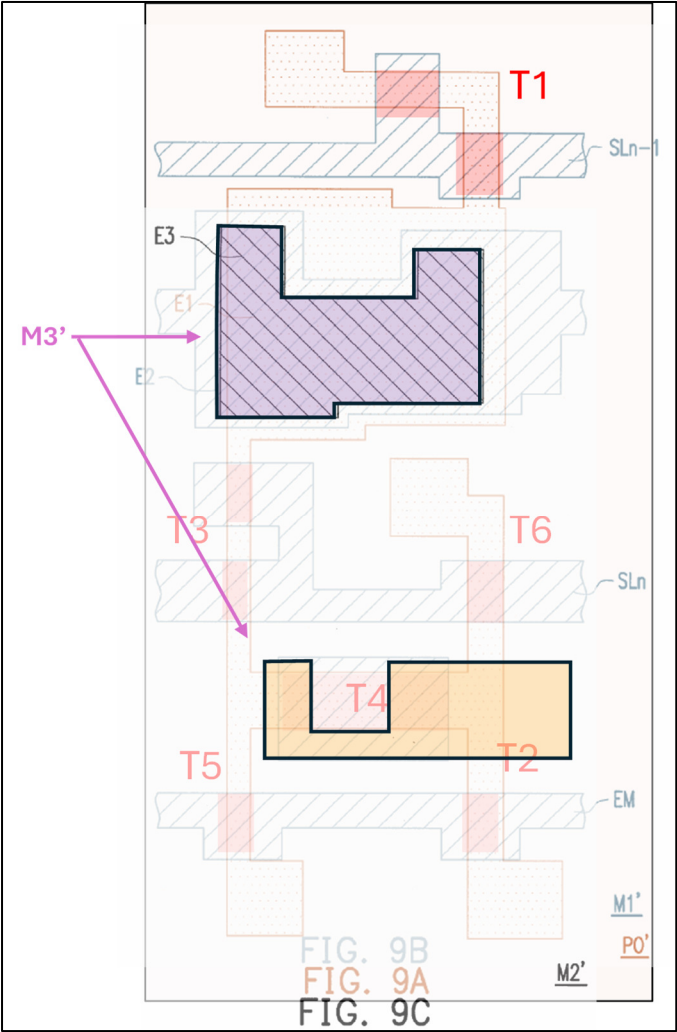
Both disclose OLED devices with an array of thin film transistors and address efficiently using the spaces in the device's pixel structure to promote the miniaturization of OLED devices. Liu discloses a pixel structure of an OLED display device "capable of reducing an area occupied by components of the pixel structure." (EX1007, [0007].) Ono discloses "a luminescent display device with higher design flexibility by forming a capacitor without a region dedicated to the capacitor or a new region dedicated to the capacitor." (EX1008, [0030].) Thus, Liu and Ono are in the same field of endeavor and directed to decreasing the area of the pixel structure and/or increasing the capacitance of the storage capacitor in OLED devices. (EX1002, ¶255.)

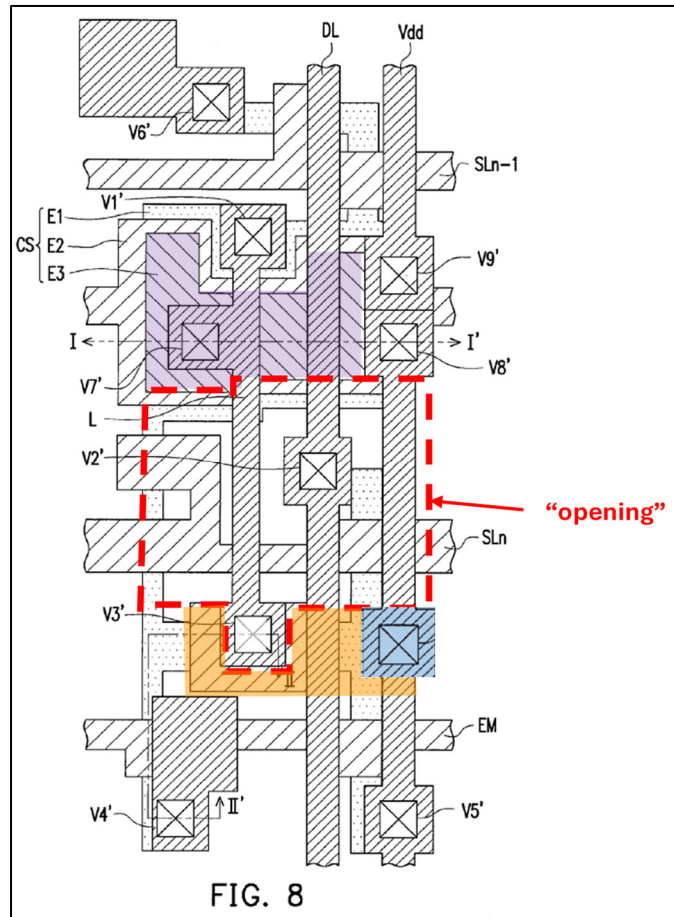
Ono teaches "the gate electrode of the thin-film transistor is used not only simply as the gate electrode but also as one of two electrodes constituting the capacitor." (EX1008, [0029].) "Thus, the capacitor can be formed above the thin-film transistor to overlap with the thin-film transistor, enabling efficient use of the pixel space." (*Id.*) Ono explains "when the number of capacitors or the capacitor area increases, the region for forming other elements becomes smaller, resulting in less design flexibility." (EX1008, [0008].) Ono teaches the gate electrode of the driving thin-film transistor 103/503 in different pixel circuits is used as one of the capacitor electrode formed above the driving thin-film-transistor. (EX1008, [0070], Fig. 3, Fig. 4, [0091], Fig. 6, Fig. 7, [0113], Fig. 8, Fig. 9, [0124], Figs.

10-12.) The Liu-Ono combination results in an OLED with greater capacitance without the need for more area for the pixel structure and higher design flexibility, and better device performance device due to the increased capacitor area for the storage capacitor from efficiently using unoccupied space without decreasing the device's quality. (EX1002, ¶256.)

Liu's M2' layer has a large amount of space above the gate of the driving transistor T4 (*see* Figure 9C). A POSITA would have been motivated to extend Liu's electrode E2 in the space above the gate of the driving transistor T4, as taught by Ono and other prior art (*e.g.*, EX1018, [0011], [0019]), to increase the capacitor area in an unoccupied space. This technique increases the overall capacitance of the pixel structure resulting in improved display performance without using additional area. Because no extra layers are added and the space is unoccupied, a POSITA would have had a reasonable expectation of success combining the two references. (EX1002, ¶257.)

Figures 8 and 9A-9D (below) are modified according to the Liu-Ono combination, showing the extended *upper electrode*. Figures 8 and 9A-9D (below) are modified according to the Liu-Ono combination, showing the extended *upper electrode*. Below is a composite figure overlaying Figures 9A-9D of Liu showing the extended *upper electrode* according to the Liu-Ono combination comprising the extended upper electrode overlapping the power line Vdd and connect to it





Because Liu and Ono both relate to efficiently using pixel space within OLED devices, a POSITA would be motivated to use the techniques disclosed in Ono to improve the similar device of Liu in the same way. Ono teaches placing a capacitor electrode over a gate electrode of the driving transistor, which was known in the art. This technique increases the overall capacitance of the pixel structure resulting in improved display performance without using additional space. Liu's device includes unoccupied space on its layer M2' above the gate electrode of driving transistor T4, thereby making it easy to extend the electrode E2 to include more capacitor area. Ono has successfully demonstrated OLED

device configurations that shrink the size of the components within a pixel structure by placing a capacitor electrode over the gate electrode of the driving transistor 103/503. Thus, it would have been obvious to a POSITA to combine Liu and Ono. (EX1002, ¶258.)

5. 1[d]: “an inter-layer insulation film covering the capacitor;”

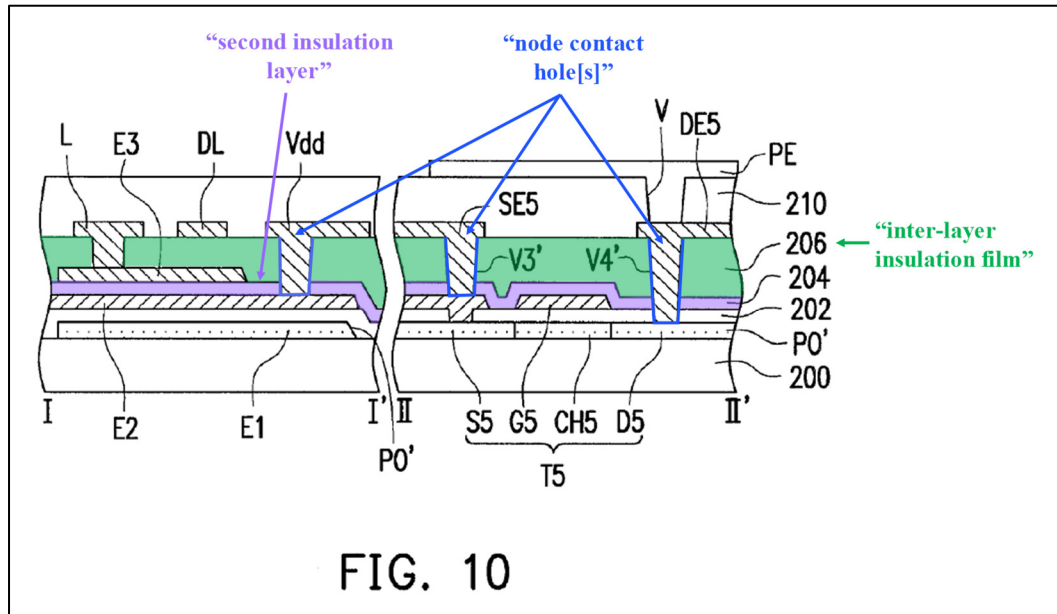
Liu’s “*third insulating layer 206 covers the second conductive layer M2*’ and has a material similar to or the same with the material of the third insulating layer 106 as described in the first embodiment.” (EX1007, [0067].) Liu discloses “the third *electrode E3 of the second conductive layer M2*’ serve as capacitor dielectric layers *of the capacitor CS*.” (EX1007, [0066].) Thus, Liu teaches an insulating layer 206 (“inter-layer insulation film”) that covers the capacitor Cs. It would have been obvious to extend the electrode E2 of Liu to include an electrode above the driving transistor T4 according to the teachings of Ono. (See 1[c]; EX1002, ¶260.)

Figure 10 (below) shows *insulating layer 206* covering the *capacitor* of the Liu-Ono combination, which includes an extended upper electrode in the space above the gate of transistor T4 on the conductive layer M2’. Because the “third insulating layer 206 covers the second conductive layer M2’”, it would cover the capacitor according to the Liu-Ono combination. (EX1002, ¶260.)

Liu’s “second conductive layer M2 is disposed on the *second insulating layer 204* and has a material similar to or the same with the material of the second conductive layer M2 as described in the first embodiment.” (EX1007, [0066].)

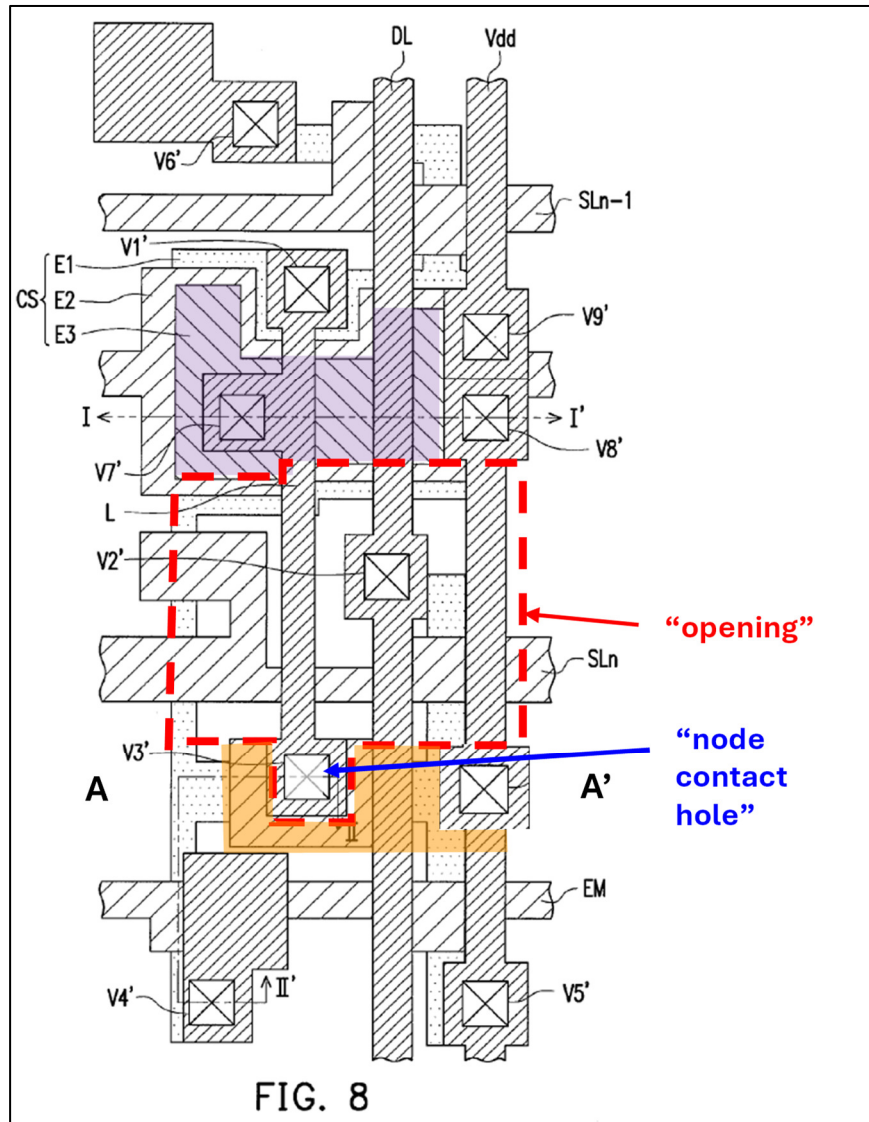
Liu teaches the third conductive layer M3' has source electrodes and drain electrodes "electrically connected to the source region and the drain regions through contact via structures V1'-V6'." (EX1007, [0069].) Figure 10 (below) shows the *via structures* ("node contact hole[s]") including via structure V3' in the

insulation layer 206 and the *insulation layer 204*. (EX1002, ¶¶262-263.)



Modified Figure 8 (below) shows *via structure V3'* within the *opening*.

(EX1002, ¶264.)



7. 1[f]: “a connection node on the inter-layer insulation film and electrically coupling the lower electrode and at least one TFT to each other through the node contact hole.”

Liu’s “third conductive layer M3’ may further comprise a signal line L, and the third electrode E3 of the capacitor CS is electrically connected to the signal line L through a contact via structure V7’.” (EX1007, [0070].) Figure 10 (below) shows the *signal line L* (“connection node”) disposed on *insulating layer 206*

(“inter-layer insulation film” (*see* 1[c])) and electrically coupling the *electrode E3* (“lower electrode” (*see* 1[c])) through *a via structure* (*see* 1[e]). (EX1002, ¶¶265-266.)

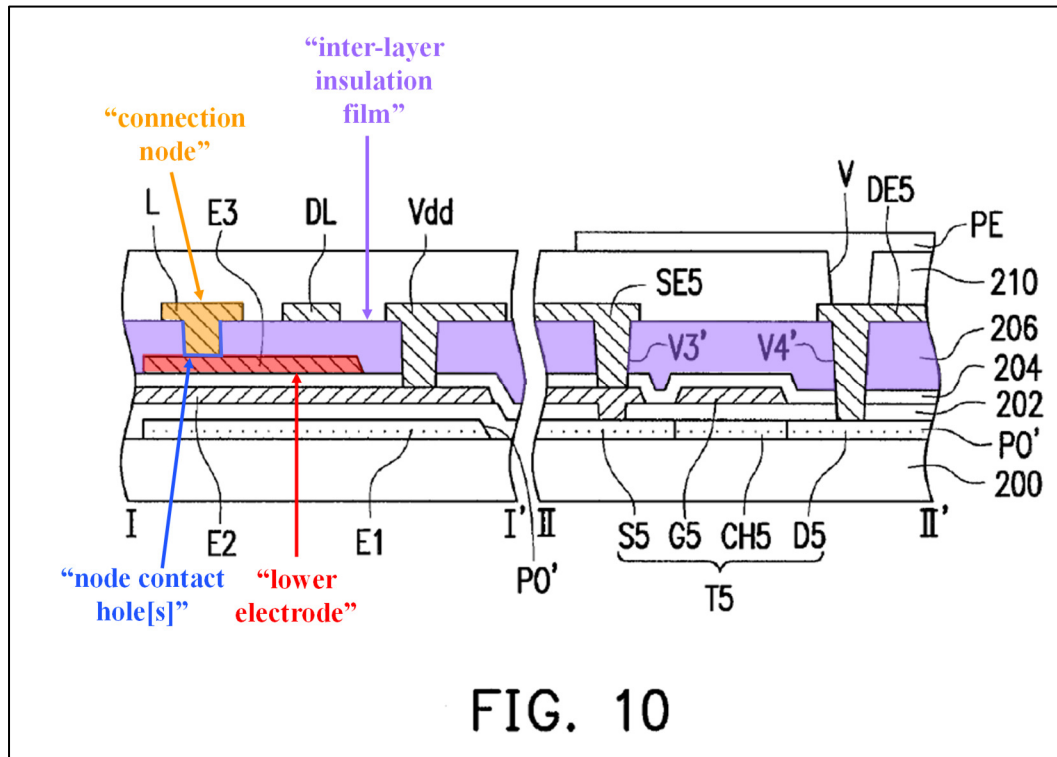
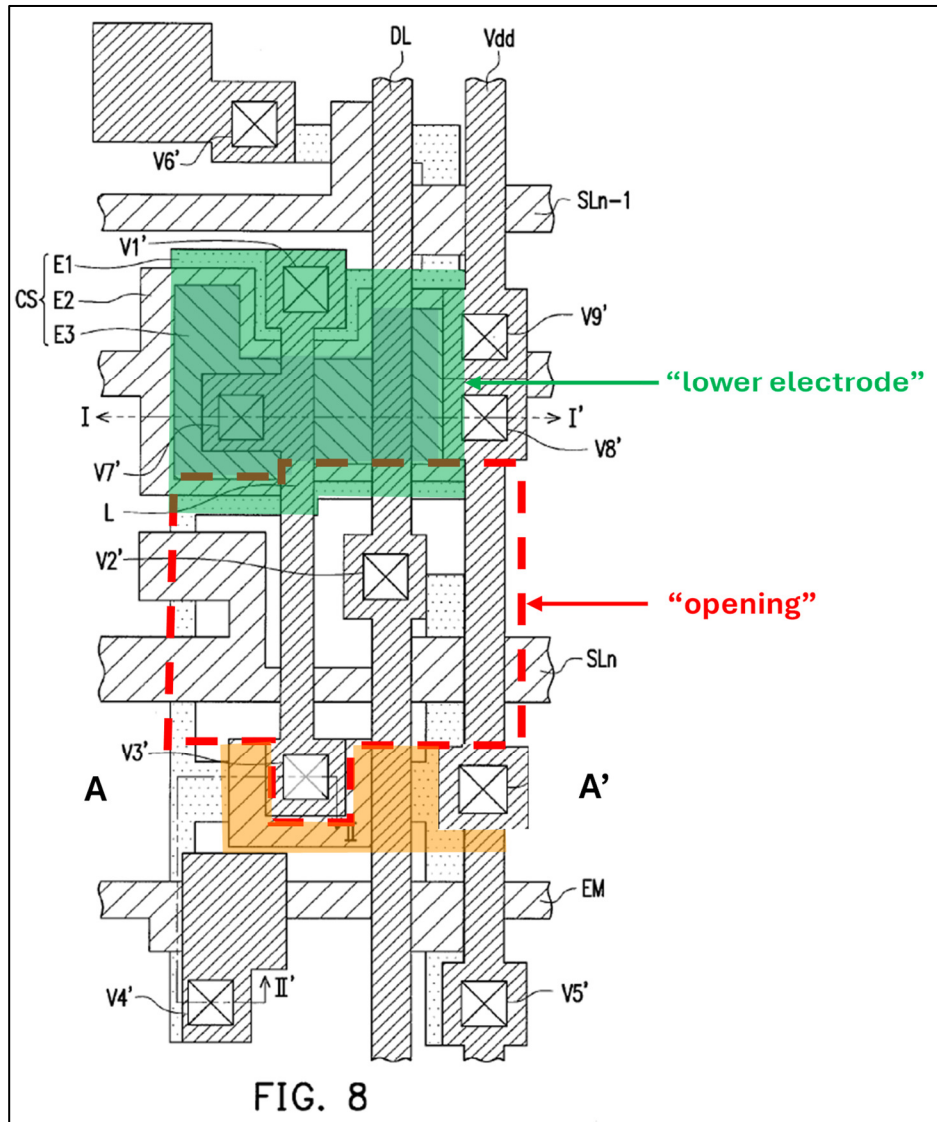


Figure 1 (below) shows the *connection node* electrically coupling *electrodes E1 and E3* (“lower electrode” (*see* 1[c])) to *transistors T1, T3, and T4* (“TFT”) to each other. Liu’s “source electrodes and the drain electrodes are electrically connected to the source region and the drain regions through contact via structures V1'-V6'.” (EX1007, [0069]; EX1002, ¶267.)



E. Claim 3

1. Elements 3[pre]-3[f]

Elements 3[pre]-3[f] are similar to elements 1[pre]-1[f], respectively, which Liu and/or Ono teaches. (EX1002, ¶¶271-277.)

2. 3[g]: “wherein the upper electrode is configured to receive a driving voltage through a driving voltage line formed from the same layer as the connection node.”

Liu’s “third conductive layer M3” further comprises a data line DL and a power line Vdd. . . . the power line Vdd is electrically connected to the second electrode E2 of the capacitor CS through contact via structures V8-V9’.” (EX1007, [0070].) Figure 10 (below) shows *electrode E2* (“upper electrode” (*see* 1[c])) electrically coupled to the *power line Vdd*, thereby electrode E2 receives a driving voltage through a driving voltage line. The power line Vdd is a driving voltage line that provides a driving voltage because it drives the OLED when driving thin film transistor T4 and thin film transistor T5 are turned on. (EX1007, Fig. 1; EX1002, ¶¶278-279.)

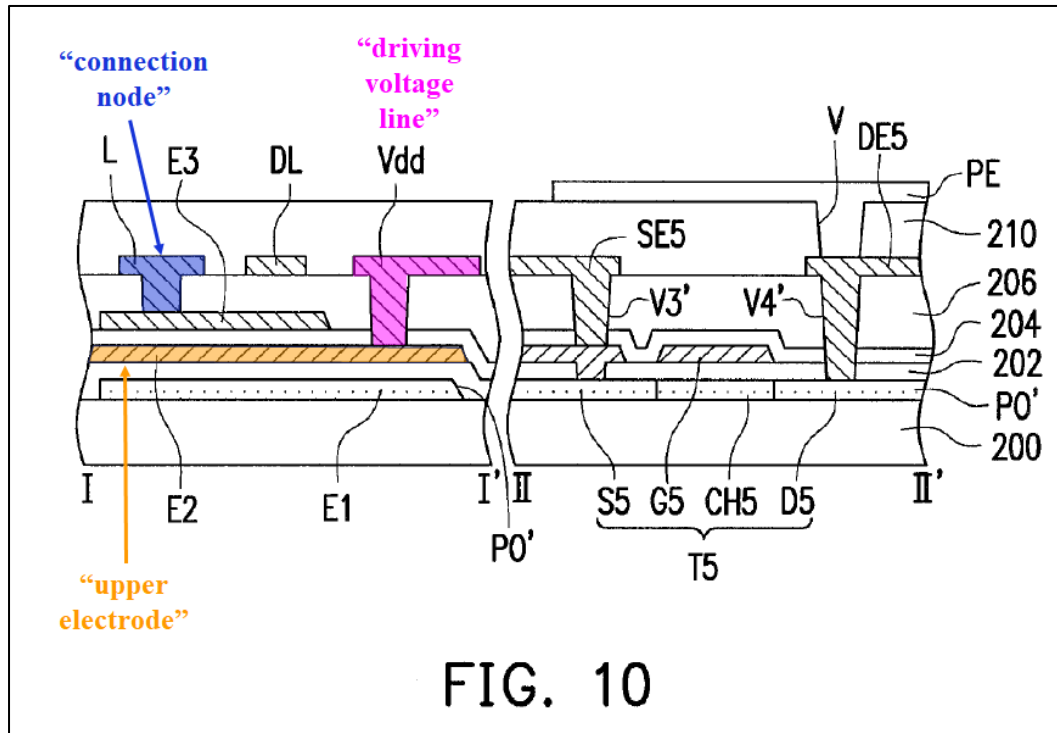


FIG. 10

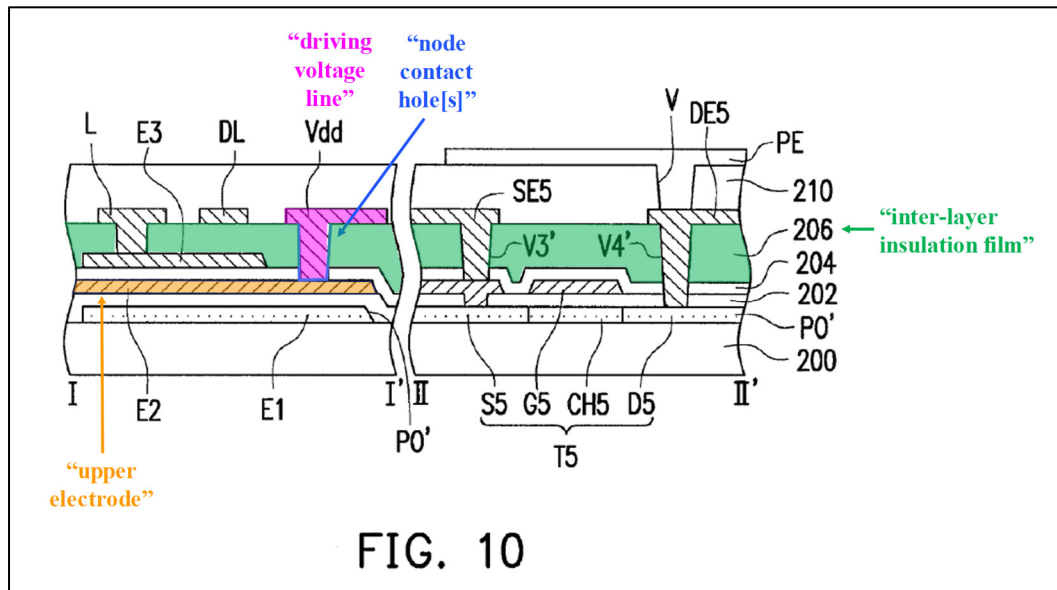
Liu's "third conductive layer M3" further comprises a data line DL and a *power line Vdd*. ... third conductive layer M3" may further comprise a *signal line L*." (EX1007, [0070].) Figure 10 (above) shows the *power line Vdd* ("driving voltage line") formed from the same layer as the *signal line L* ("connection node" (see 1[f])). (EX1002, ¶280.)

F. Claim 4: "The TFT array substrate of claim 3, wherein the driving voltage line is coupled to the upper electrode through another contact hole in the inter-layer insulation film."

Liu's "power line Vdd is electrically connected to the second electrode E2 of the capacitor CS through contact via structures V8-V9'." (EX1007, [0070].)

Figure 10 shows the *power line Vdd* ("driving voltage line" (see claim 3)) is

coupled to the **electrode E2** (“upper electrode” (see 1[c])) through a **via structure** (“contact hole” (see 1[e])). The figure shows the via structure for connecting power line Vdd to electrode E2 is in the **insulation film 206** (“inter-layer insulation film” (see 1[d])). (EX1002, ¶¶281-283.)



G. Claim 5

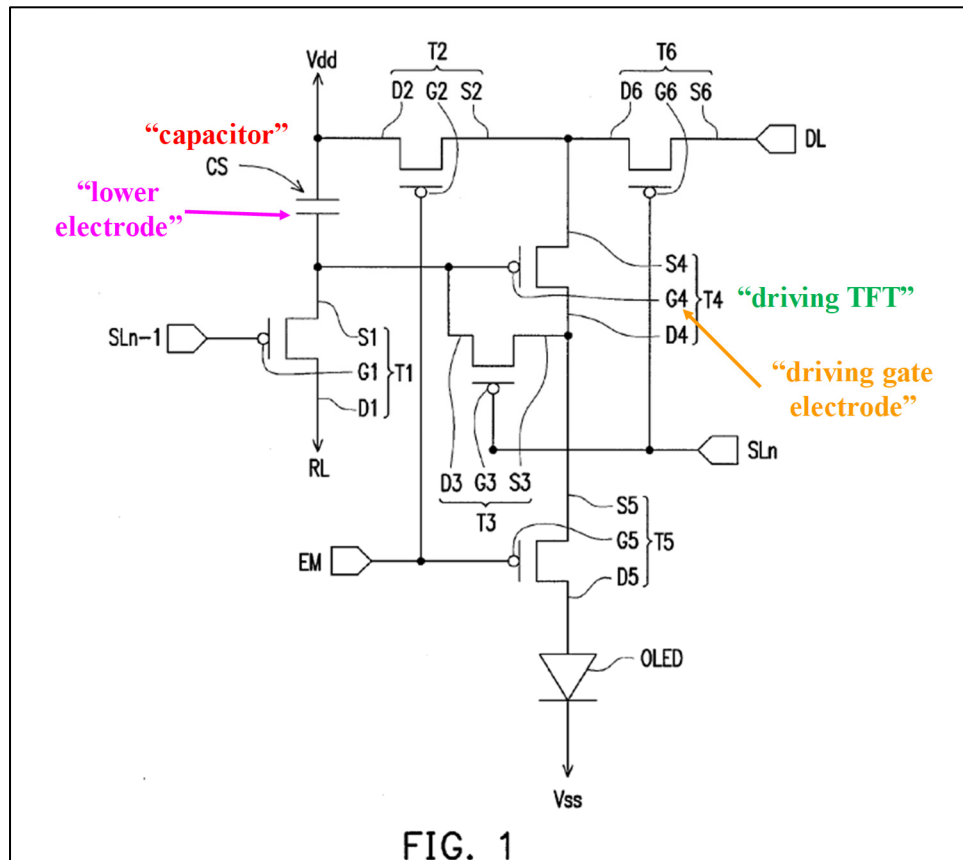
1. Elements 5[pre]-5[f]

Elements 5[pre]-5[f] are similar to elements 1[pre], 1[a]/3[a], 1[b]/3[b], 3[c], 1[d]/3[d], 1[e]/3[e], 1[f]/3[f], which Liu and/or Ono teaches. (EX1002, ¶¶284-290.)

2. 5[g]: “a driving TFT arranged to overlap with the capacitor, wherein a driving gate electrode of the driving TFT comprises the lower electrode.”

Liu discloses a **transistor T4** (Figure 1 (below)) comprising a drain D4 coupled to the anode of the OLED when transistor T5 is turned on, showing it

controls the driving of the OLED, thereby making it a driving TFT. (EX1007, [0069].) Transistor T4 comprises a *gate G4* (“driving gate electrode”) comprising a gate electrode coupled to, thereby comprising, the *lower electrode* of the *capacitor CS* and arranged to overlap with the capacitor. (EX1002, ¶¶291-292.)



The capacitor of the Liu-Ono combination comprises an extended upper electrode, thereby overlapping with transistor T4. (See 1[c].) It would have been obvious for the gate G4 of transistor T4 to comprise the electrode E1 or E2 because Ono teaches sharing the gate electrode of the driving transistor as one of the capacitor electrodes allows efficiently using the limited pixel space. (EX1008,

[0037]; EX1002, ¶293.)

H. Claim 6: “The TFT array substrate of claim 5, wherein the at least one TFT comprises a compensation TFT coupled to the driving TFT and electrically coupled to the lower electrode through the connection node, and wherein the compensation TFT is configured to compensate for a threshold voltage of the driving TFT.”

Liu discloses a *transistor T3* (Figure 1 (below)) electrically coupled to *transistor T4* (“driving TFT” (see claim 5)) and electrically coupled to the *lower electrode* of the *capacitor* through the *connection node*. (EX1007, [0069].)

Transistor T3 is a compensation TFT configured to compensate for a threshold voltage of the transistor T4 because, as Figure 1 (above) shows, it couples the gate electrode G4 and the drain D4 of the driving TFT (transistor T4) to each other in response to the scan signal SLn. (EX1002, ¶¶294-297.)

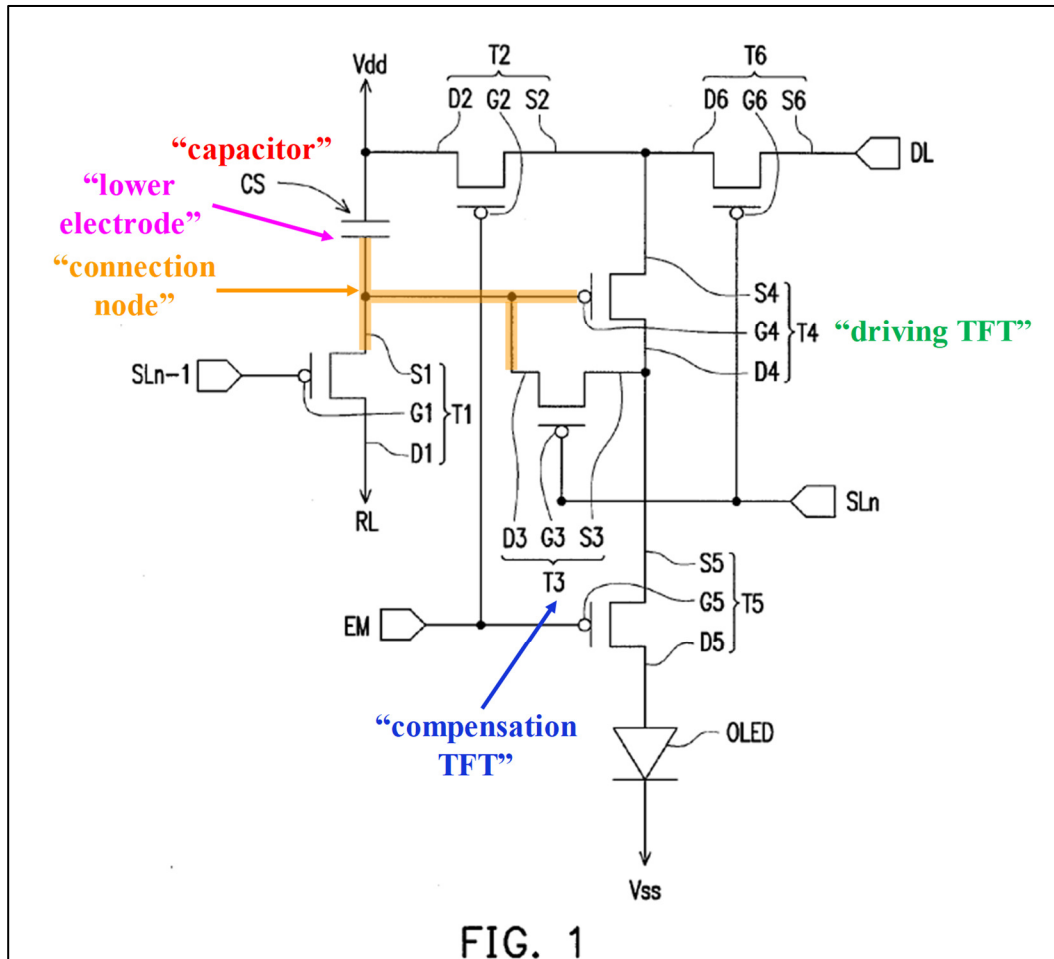
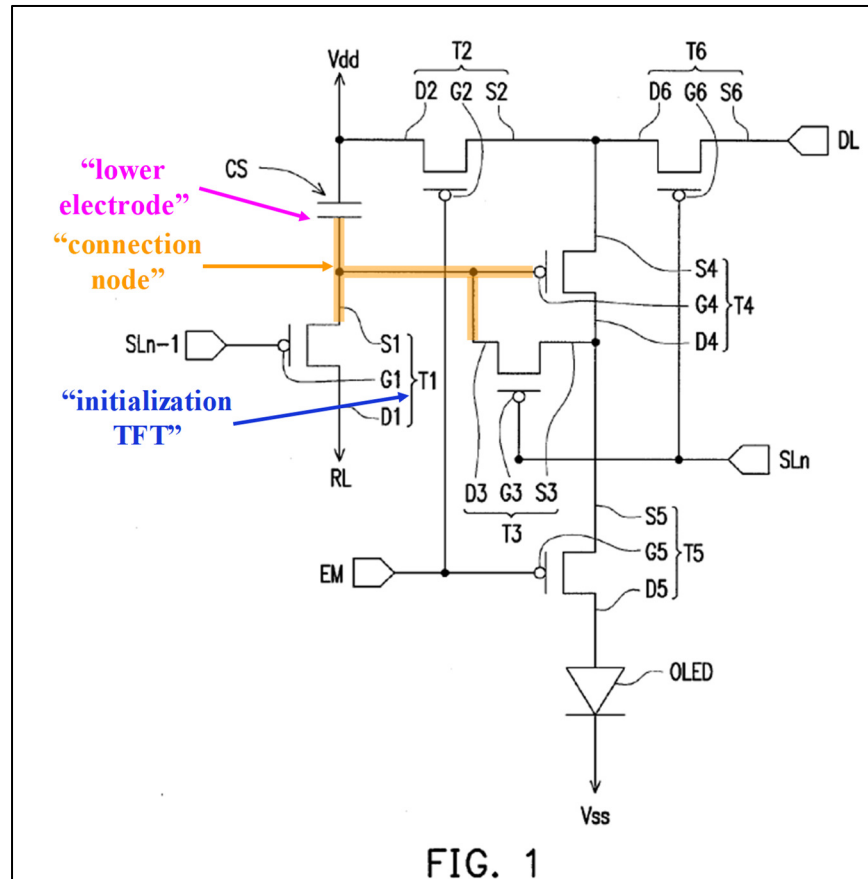


FIG. 1

I. Claim 8

1. 8[a]: “The TFT array substrate of claim 5, wherein the at least one TFT comprises an initialization TFT electrically coupled to the lower electrode through the connection node, and”

Liu discloses a *transistor T1* (Figure 1 (below)) electrically coupled to the *lower electrode* of the capacitor through the *connection node*. (EX1007, [0069]; EX1002, ¶¶298-300.)

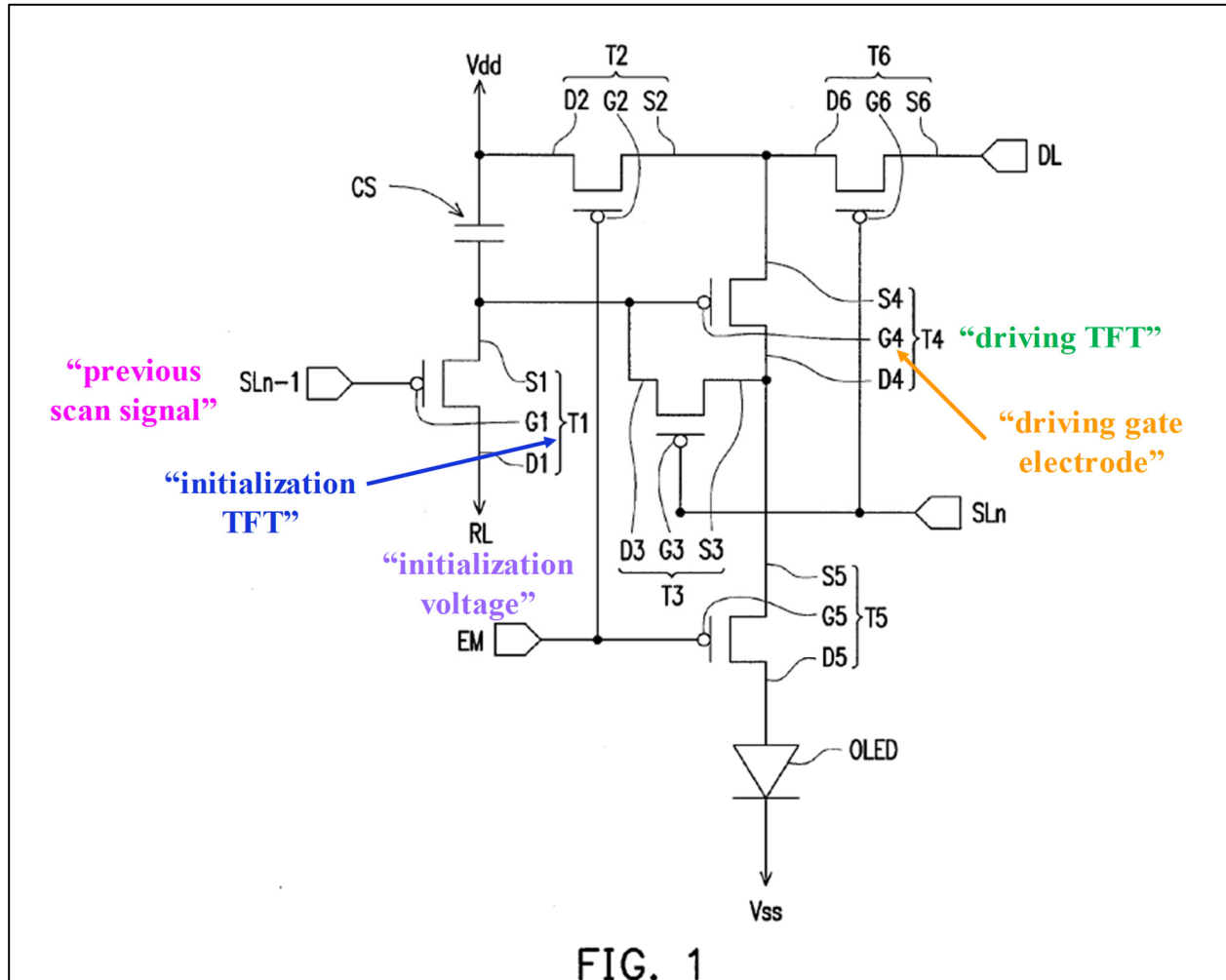


2. 8[b]: “wherein the initialization TFT is configured to provide an initialization voltage to the driving gate electrode of the driving TFT by being turned on in response to a previous scan signal.”

Liu’s Figure 1 (below) shows the *transistor T1* is configured to provide a voltage from *reference signal line RL* to the *gate G4* of *transistor T4*, and thus, transistor T1 is an initialization TFT that provides an initialization voltage. The gate of transistor T1 is coupled to SLn-1, thereby transistor T1 is turned on in response to the previous scan line *SLn-1*. Liu explains “the first conductive layer M1 further comprises a scan line SLn, a scan line SLn-1 and a light emitting signal line EM, wherein the scan line SLn is electrically connected to the gate G3, the

scan line SLn-1 is electrically connected to the gate G1.” (EX1007, [0064];

EX1002, ¶¶301-303.)



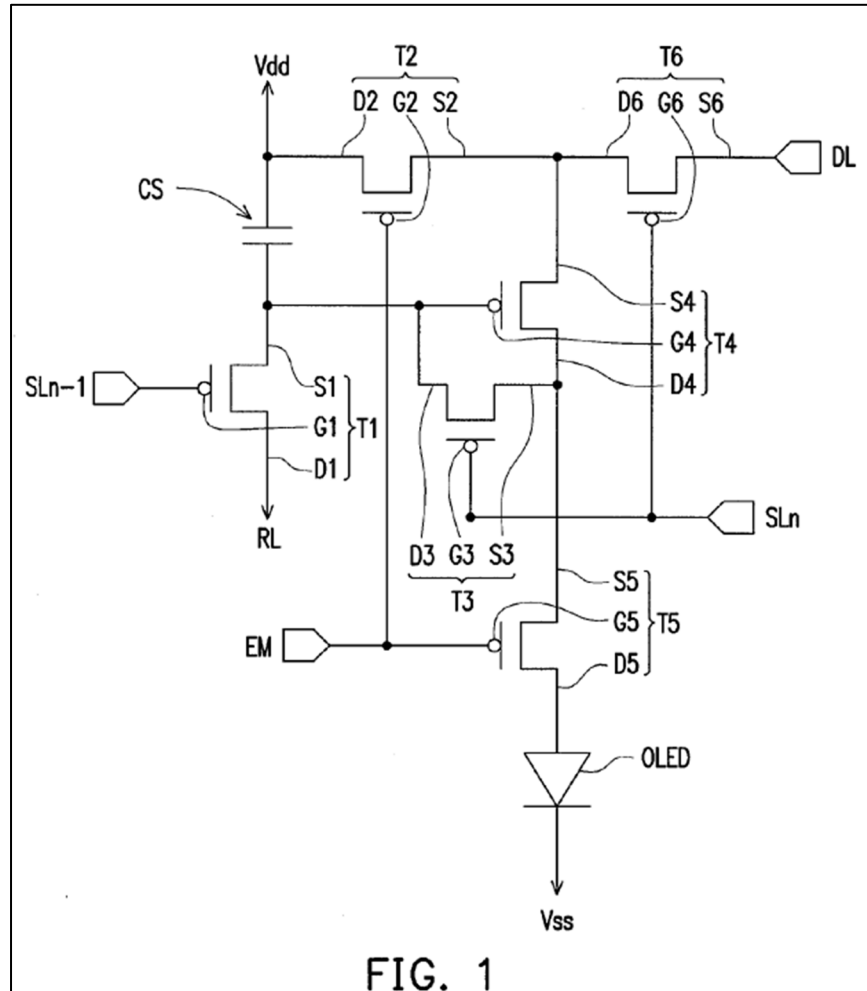
J. Claim 10

1. Preamble: “An organic light-emitting diode (OLED) display comprising:”

To the extent the preamble is limiting (which Petitioner does not concede),
Liu and/or Ono teaches the preamble.

Liu discloses “[t]he pixel electrode PE, the light emitting layer OE and the

electrode layer CA form an organic light emitting device OLED” (Figure 1 (below)). (EX1007, [0073]; EX1002, ¶304.)



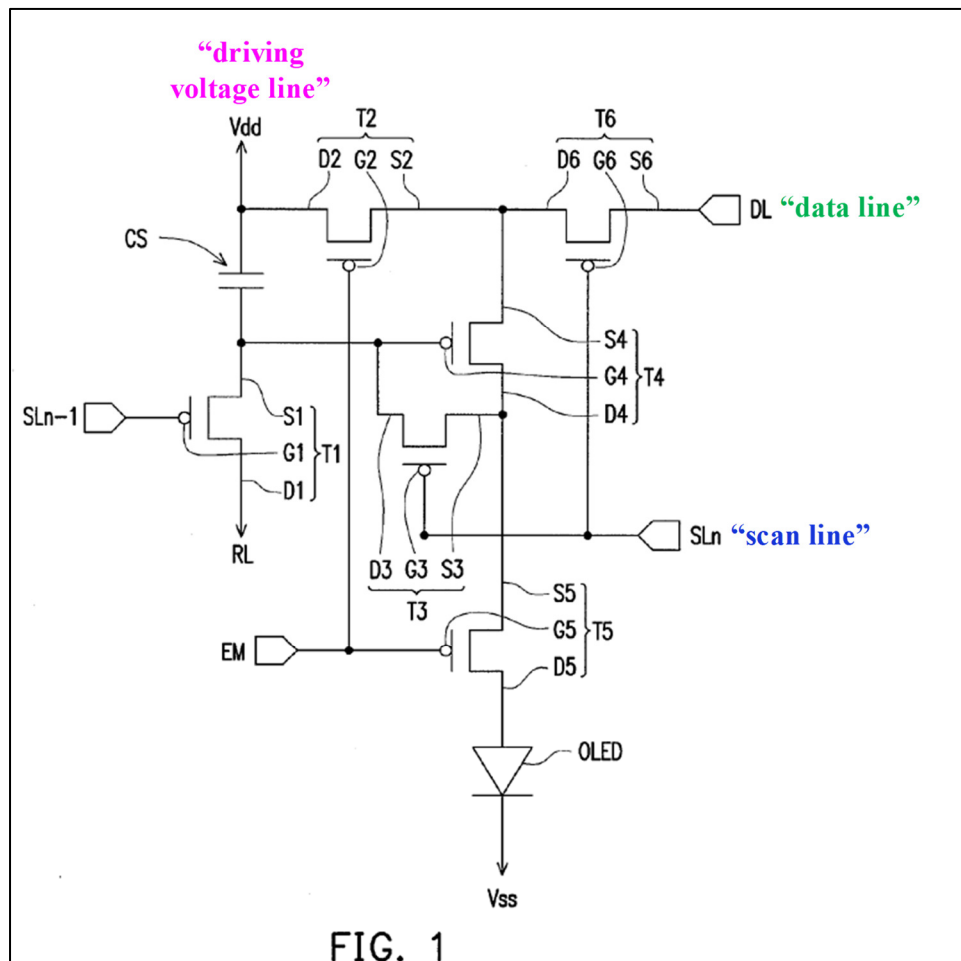
2. Elements 10[a], 10[b], and 10[g]-10[i]

Elements 10[a], 10[b], and 10[g]-10[i] are similar to elements 1[a]/3[a], 1[b]/3[b], 1[c], 1[e], and 1[f] respectively, which Liu and/or Ono teaches. (EX1002, ¶¶305-306, 320-322.)

As Liu explains, “the layout of the first conductive layer M1' is shown in FIG. 9B, which mainly comprises gates of the six thin film transistors and a second electrode E2 of the capacitor CS. For example, the first conductive layer M1' has a gate G5 in the region predetermined for forming the fifth thin film transistor T5, as shown in FIG. 10.” (EX1007, [0063].) A POSITA would have understood this passage to mean the gate of transistor T3 is on the first conductive layer M1'. Liu explains although Figure 10 shows a cross-sectional view specifically for the transistor T5, the figure represents the structure of the other five transistors, including transistor T3. (EX1007, [0058]; *see* 1[e].) Figure 10 (below) shows the *first conductive layer M1'*, the layer includes *scan line SLn*, on the *insulating layer 202* (“first insulation layer” (*see* 1[b])). (EX1002, ¶309.)

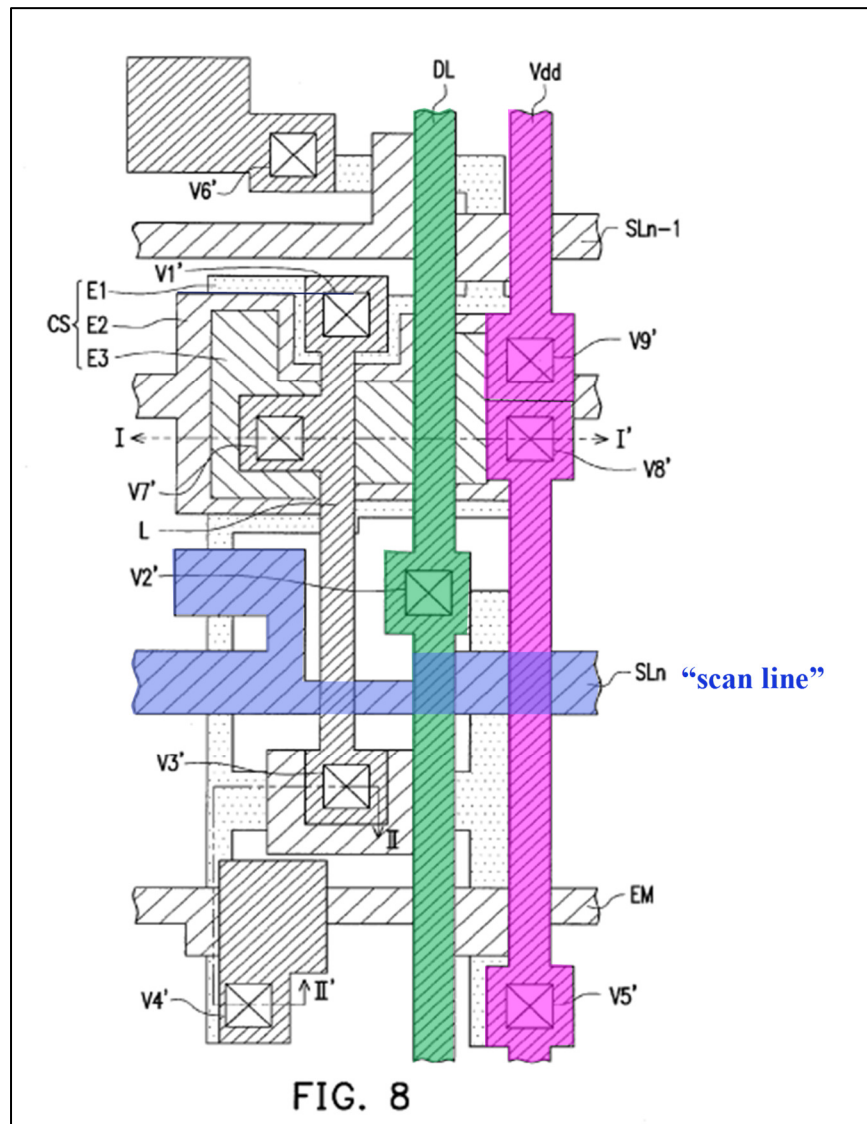
4. 10[d]: “a data line and a driving voltage line crossing the scan line, the data line and the driving voltage line being insulated by a second insulation layer and an inter-layer insulation film and configured to respectively deliver a data signal and a driving voltage;”

Liu’s “third conductive layer M3” further comprises a data line DL and a power line Vdd.” (EX1007, [0070].) Figure 1 (below) shows the *data line DL*, the *power line Vdd* (“driving voltage line” configured to deliver a driving voltage (see 3[g])), and the *scan line SLn*. (EX1002, ¶¶311-312.)

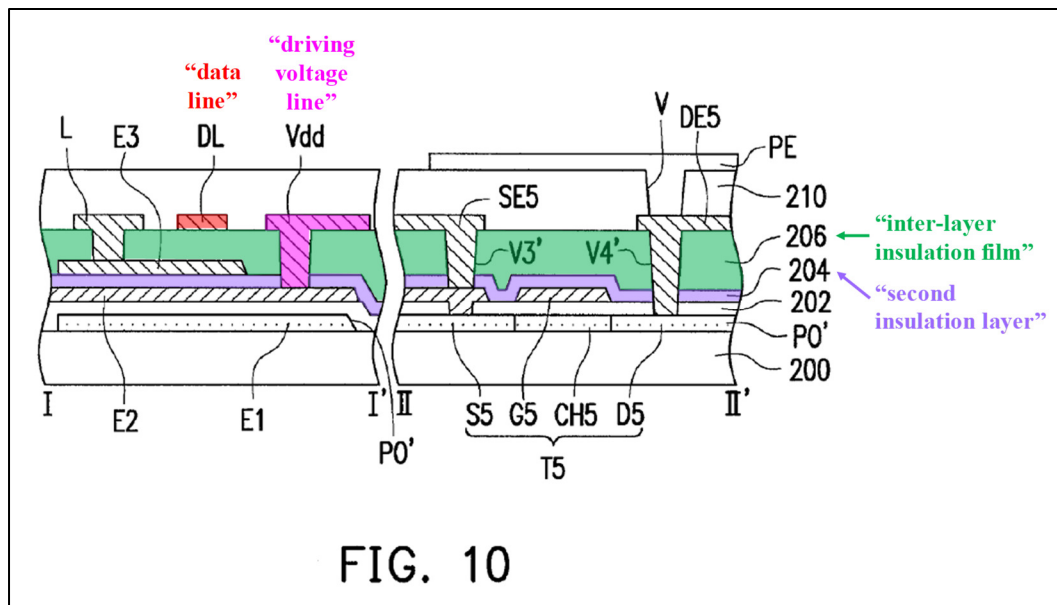


Liu’s “data line DL is electrically connected to the source region S6, and the

power line Vdd is electrically connected to the drain region D2, as shown in FIG. 1, FIG. 2 and FIG. 3C.” (EX1007, [0042].) Because the data line DL is electrically connected to the source S6, it would have been obvious that it delivers a data signal, which was known for displays at the time. Figure 8 (below) shows the *data line DL* and *power line Vdd* crossing the *scan line SLn*. (EX1002, ¶¶313-314.)



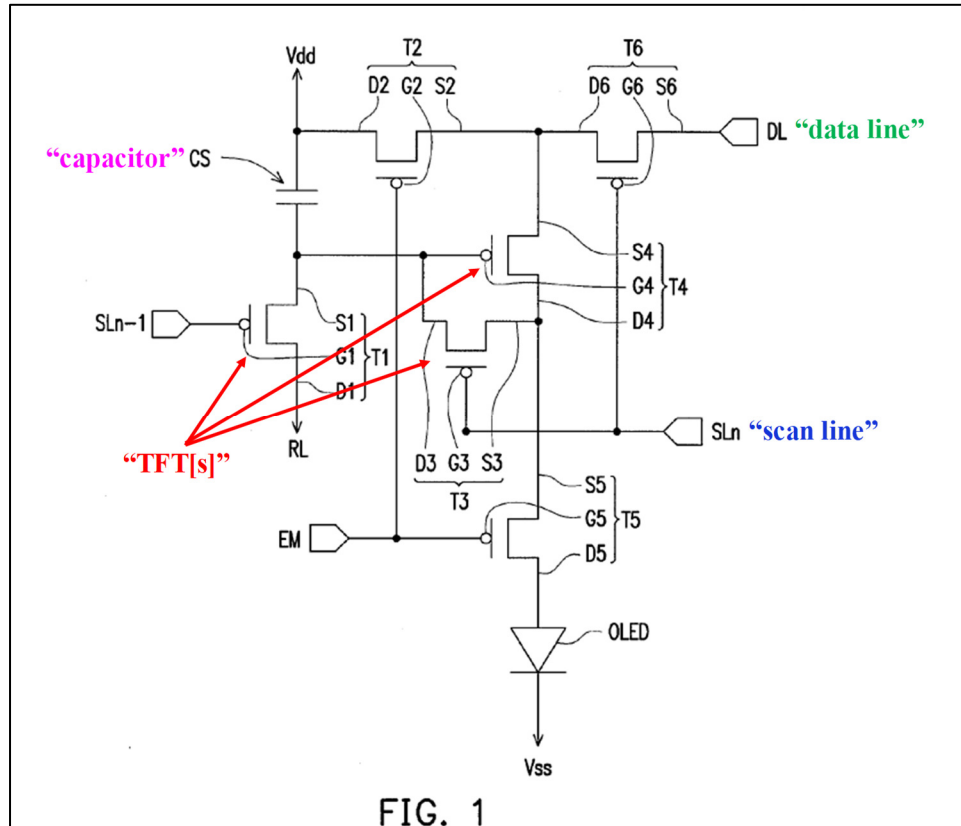
Liu's "third conductive layer M3' further comprises a data line DL and a power line Vdd." (EX1007, [0070].) Liu discloses "[t]he third conductive layer M3' is disposed on the third insulating layer 206 and has a material similar to or the same with the material of the third conductive layer M3 as described in the first embodiment." (EX1007, [0068].) Figure 10 (below) shows the *data line DL* and the *power line Vdd* being insulated by *insulating layer 204* ("second insulation layer" (see 1[c])) and *insulating layer 206* ("inter-layer insulation film" (see 1[d])). (EX1002, ¶315.)



5. 10[e]: "a pixel circuit coupled to the scan line and the data line and comprising at least one thin film transistor (TFT) and a capacitor;"

Liu's "FIG. 1 is a schematic circuit diagram of a pixel structure according to an embodiment of the invention." (EX1007, [0031].) Figure 1 (below) shows the

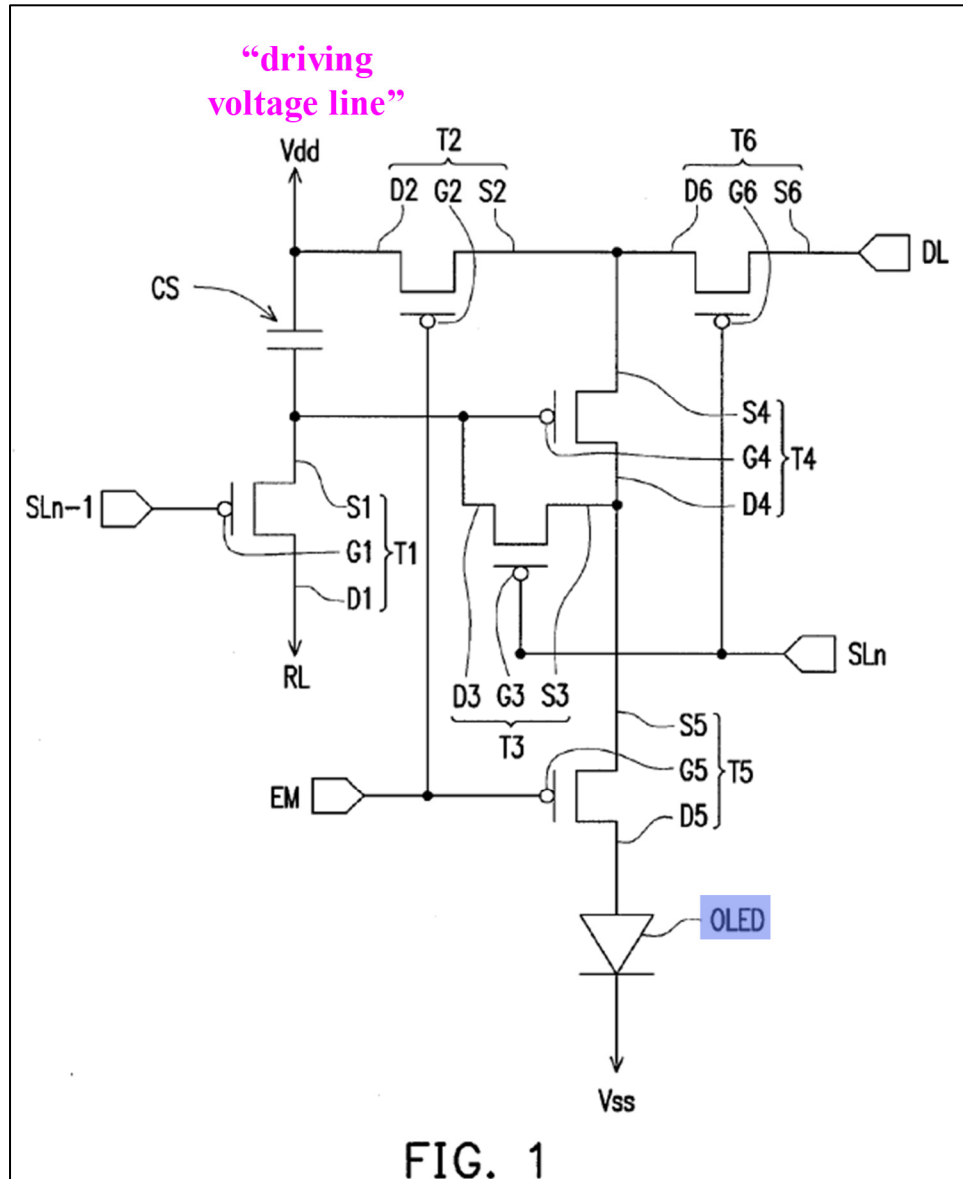
pixel circuit coupled to the *scan line SL_n* and the *data line DL* and comprising *transistors T1, T3, and T4* and *capacitor CS*. (EX1002, ¶¶316-317.)



6. 10[f]: “an OLED for emitting light by receiving the driving voltage from the pixel circuit,”

Liu discloses “[i]f the pixel structure is applied to an organic electroluminescence display, the pixel structure further comprises a light emitting region defining layer 212, a light emitting layer OE and an electrode layer CA, as shown in FIG. 11. The pixel electrode PE, the light emitting layer OE and the electrode layer CA form an organic light emitting device OLED.” (EX1007, [0073].) Figure 1 (below) shows the *OLED* coupled to the power line V_{dd} via

transistors T2, T4, and T5. When these transistors are turned on, the voltage *Vdd* (“driving voltage” (*see* 10[d])) would be delivered to the OLED, causing the OLED to emit light. Thus, Liu teaches an OLED for emitting light by receiving the driving voltage from the pixel circuit. (EX1002, ¶¶318-319.)



K. Claims 11-18

Claim 11, elements 12[pre]-12[j], claim 13, elements 14[pre]-14[j], and

claims 15-18 are similar to claim 2, elements 10[pre], 1[a]/3[a], 1[b]/3[b], 10[c]-10[f], 3[c], 1[e]/3[e], 1[f]/3[f], 3[g], claim 4, elements 10[pre], 1[a]/3[a], 1[b]/3[b], 10[c]-10[f], 3[c], 1[e]/3[e], 1[f]/3[f], 5[g], and claims 6-9, respectively, which Liu and/or Ono teach. (EX1002, ¶¶323-357.)

L. Claim 19: “The OLED display of claim 14, further comprising a switching TFT for delivering the data signal to the driving TFT by being turned on by the scan signal.”

Liu discloses a *transistor T6* (Figure 1 (below)), whose source is coupled to the *data line DL* and the drain D6 coupled to *transistor T4*. (EX1007, [0069].) Transistor T6 is a switching transistor because it delivers the data signal to the transistor T4 to provide the driving current to the OLED in response to the switching operation of transistor T6. The figure shows the gate G6 of transistor T6 coupled to the *scan signal SLn*. A POSITA would have understood the scan signal SLn being coupled to the gate G6 of transistor T4 is “delivering the data signal to the driving TFT by being turned on by the scan signal.” (EX1002, ¶¶358-361.)

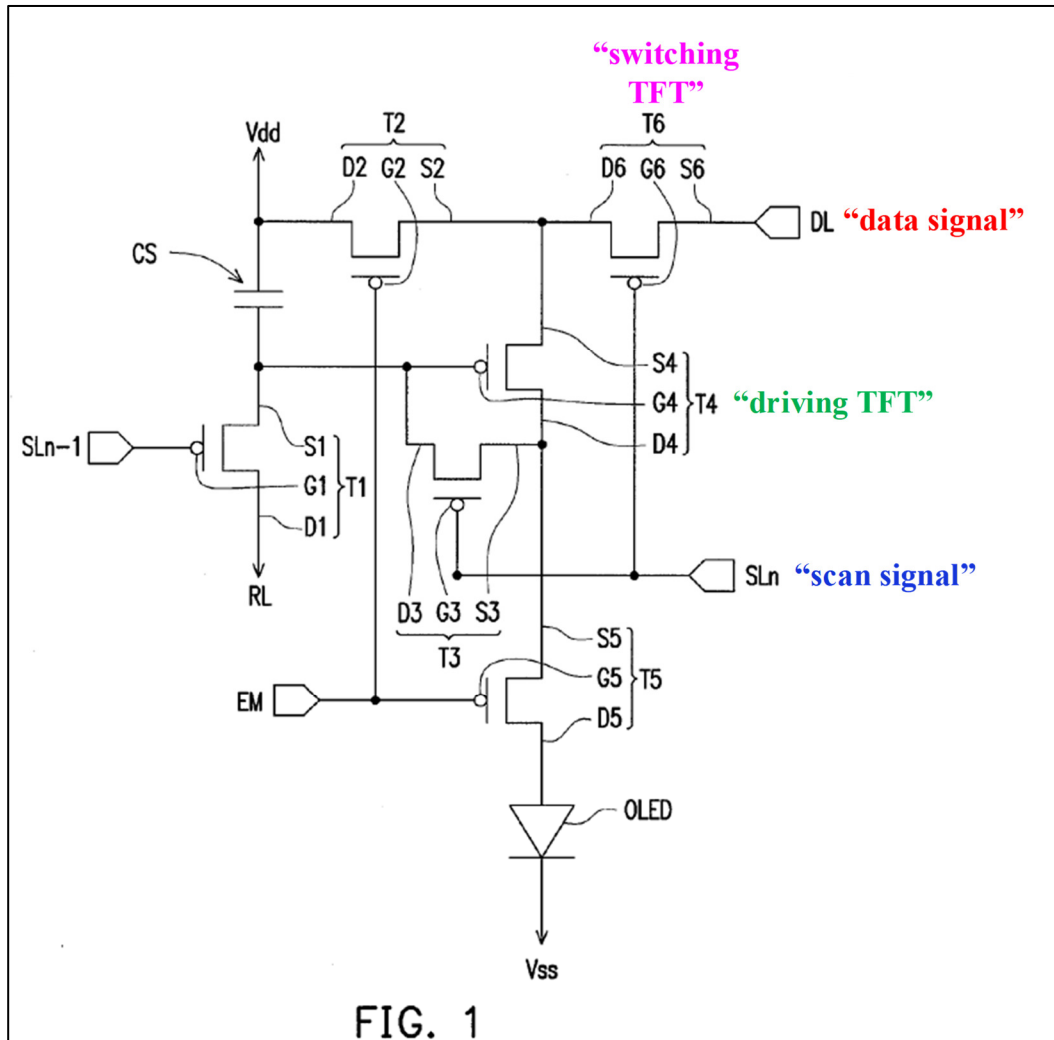


FIG. 1

X. THE BOARD SHOULD NOT DENY INSTITUTION UNDER *FINTIV*²

A. A Final Written Decision Will Issue Before Any Trial

A schedule has not yet been issued and no trial date has been set in the

² Petitioner is not addressing in full discretionary issues in the Petition per USPTO guidance. See *FAQs for Interim Processes for PTAB Workload Management*, USPTO, <https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload->

corresponding district court litigation. A Final Written Decision will issue in October 2026, whereas the trial date for the district court case (which has not been set) will likely be after.

B. Merits Of The Petition Support Institution

As discussed above, the prior art teaches every element of the challenged claims, and are unpatentable. Thus, the merits of the petition weigh strongly in favor of institution. *See* Stewart Memorandum, 2 (“The strength of the unpatentability challenge” is a relevant consideration).

XI. THE BOARD SHOULD NOT DENY INSTITUTION UNDER § 325(D)

The Petition does not raise the same or substantially the same art previously presented to the Office, nor does the Petition raise the same or substantially the same arguments previously presented to the Office in the examination of the ’730. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Gerate GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020).

The Board applies a two-part framework for determining whether to deny institution under § 325(d) in view of prosecution of the original patent application and any subsequent reexamination: “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the

[management](#) (last visited Aug. 28, 2025).

same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated the Office erred in a manner material to the patentability of challenged claims.”

Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential).

Here, the Board need not reach the second part of the test, because the first part fails: neither the same (or substantially the same) art or arguments were previously presented to the Office. None of the references presented in this petition—Ishii100, Ishii423, Park, Kwon, Liu, or Ono—were considered during prosecution of the ’730. And the prior art of this petition teaches a capacitor having an upper electrode overlapping with the whole lower electrode, limitations the prior art of record did not have, and thus is materially different and not cumulative of the art applied during examination.

Even if the Board were to conclude otherwise, the Office erred in a material manner. The Examiner allowed the claims without even identifying the prior art of this petition. Where the examination record is not well developed, as here, it may indicate the Examiner erred by “overlook[ing] something persuasive.” *Advanced Bionics*, IPR2019-01469, Paper 6 at 10.

For all the foregoing reasons, the Board should decline to deny the petition under § 325(d).

XII. NOTICES AND STATEMENTS

Pursuant to 37 C.F.R. § 42.8(b)(1), BOE Technology Group Co., Ltd. is the real party-in-interest for Petitioner.

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner identifies the following related matters.

- *Samsung Display Co., Ltd., v. BOE Technology Group Co., Ltd., et al.*, No. 2:25-cv-00430 (E.D. Tex.)
- *Samsung Display Co., Ltd., v. BOE Technology Group Co., Ltd., et al.*, No. 2:25-cv-00426 (E.D. Tex.)
- IPR2025-01498

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioner identifies the following counsel (and a power of attorney accompanies this Petition).

Lead Counsel	First Backup Counsel	
Alex S. Yap Registration No. 60,609 MORRISON & FOERSTER LLP 707 Wilshire Boulevard, Suite 6000 Los Angeles, CA 90017-3543 Email: AYap@mofo.com Tel: (213) 892-5200 Fax: (213) 892-5454	Mehran Arjomand Registration No. 48,231 MORRISON & FOERSTER LLP 707 Wilshire Boulevard, Suite 6000 Los Angeles, CA 90017-3543 Email: MArjomand@mofo.com Tel: (213) 892-5200 Fax: (213) 892-5454	
	<th data-bbox="812 781 1425 825">Second Backup Counsel</th> Jean Nguyen Registration No. 71,051 MORRISON & FOERSTER LLP 707 Wilshire Boulevard, Suite 6000 Los Angeles, CA 90017-3543 Email: JNguyen@mofo.com Tel: (213) 892-5200 Fax: (213) 892-5454	Second Backup Counsel

Pursuant to 37 C.F.R. § 42.8(b)(4), service information for lead and back-up counsel is provided above. Petitioner consents to electronic service by email to BOE-Samsung-IPR@mofo.com.

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '730 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

The USPTO is authorized to charge any required fees, including the fee as

set forth in 37 C.F.R. § 42.15(a) and any excess claim fees, to Deposit Account

No. **03-1952** referencing Docket No. **37294-00000.06**.

Dated: August 31, 2025

Respectfully submitted,

By /s/ Alex S. Yap

Alex S. Yap

Reg. No. 60,609

MORRISON & FOERSTER LLP

707 Wilshire Boulevard, Suite 6000

Los Angeles, CA 90017-3543

Email: AYap@mofo.com

Tel: (213) 892-5200

Attorney for Petitioner

Certification of Word Count (37 C.F.R. § 42.24)

I hereby certify that this Petition for *Inter Partes* Review has 13,344 words (as counted by the “Word Count” feature of the Microsoft Word™ word-processing system), exclusive of “a table of contents, a table of authorities, mandatory notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing.”

Dated: August 31, 2025

By /s/ Alex S. Yap

Alex S. Yap

Certificate of Service (37 C.F.R. § 42.6(e)(4) and 42.205(a))

I hereby certify that the attached Petition for *Inter Partes* Review and supporting materials were served as of the below date by Priority Mail Express® on the Patent Owner at the correspondence address indicated for U.S. Patent No. 9,299,730.

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

A copy of the attached Petition for *Inter Partes* Review and supporting materials were also served on the following litigation counsel:

aa@rothfirm.com
charles.sanders@lw.com
kevin.wheeler@lw.com
alex.grabowski@lw.com
cassandra.baloga@lw.com
brian.kim@lw.com
jake.vannette@lw.com
au@rothfirm.com
ca@rothfirm.com

Dated: August 31, 2025

/s/ Alex S. Yap
Alex S. Yap