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(54) ADAPTIVE VOLTAGE SCALING FOR AN ELECTRONICS DEVICE

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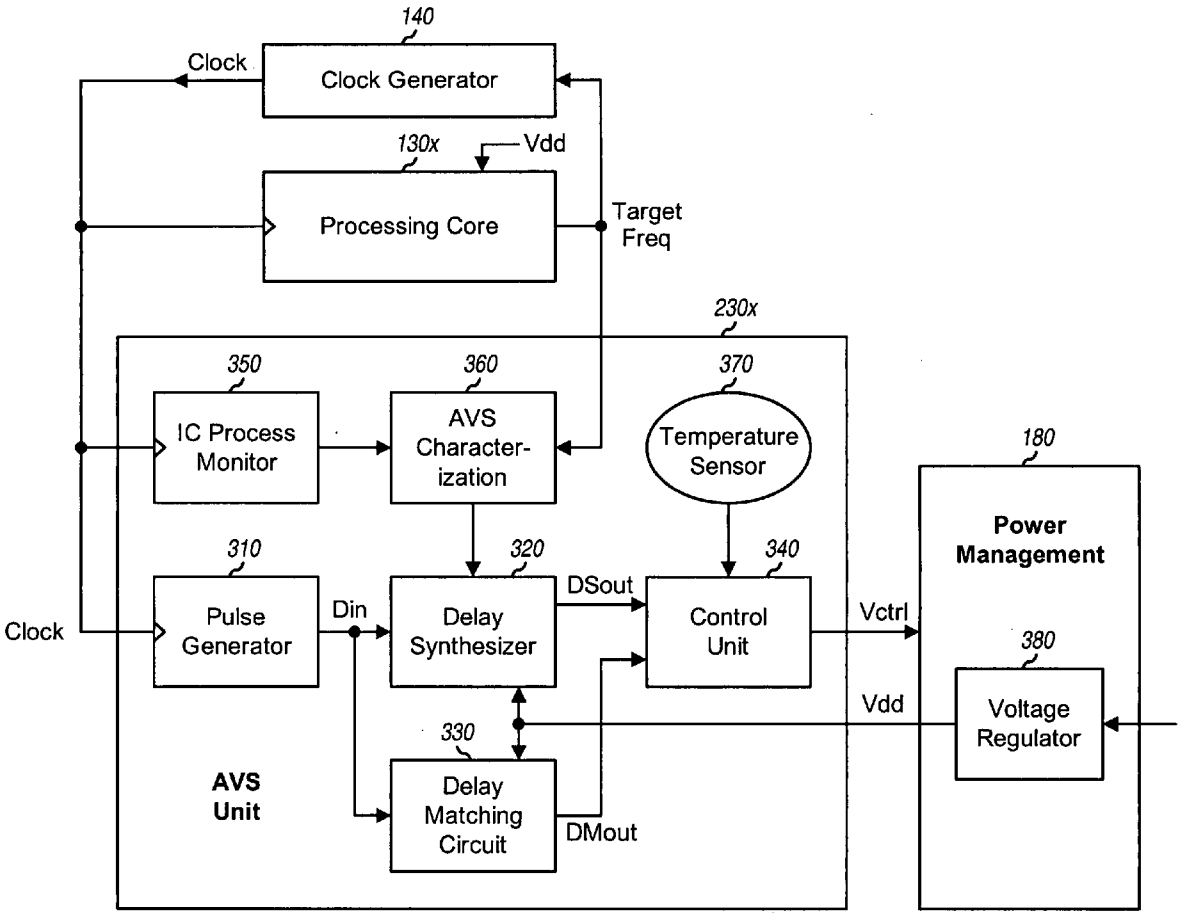
(57) **ABSTRACT**

Techniques for adaptively scaling voltage for a processing core are described. In one scheme, the logic speed and the wire speed for the processing core are characterized, e.g., using a ring oscillator having multiple signal paths composed of different circuit components. A target clock frequency for the processing core is determined, e.g., based on computational requirements for the core. A replicated critical path is formed based on the characterized logic speed and wire speed and the target clock frequency. This replicated critical path emulates the actual critical path in the processing core and may include different types of circuit components such as logic cells with different threshold voltages, dynamic cells, bit line cells, wires, drivers with different threshold voltages and/or fan-outs, and so on. The supply voltage for the processing core and the replicated critical path is adjusted such that both achieve the desired performance.



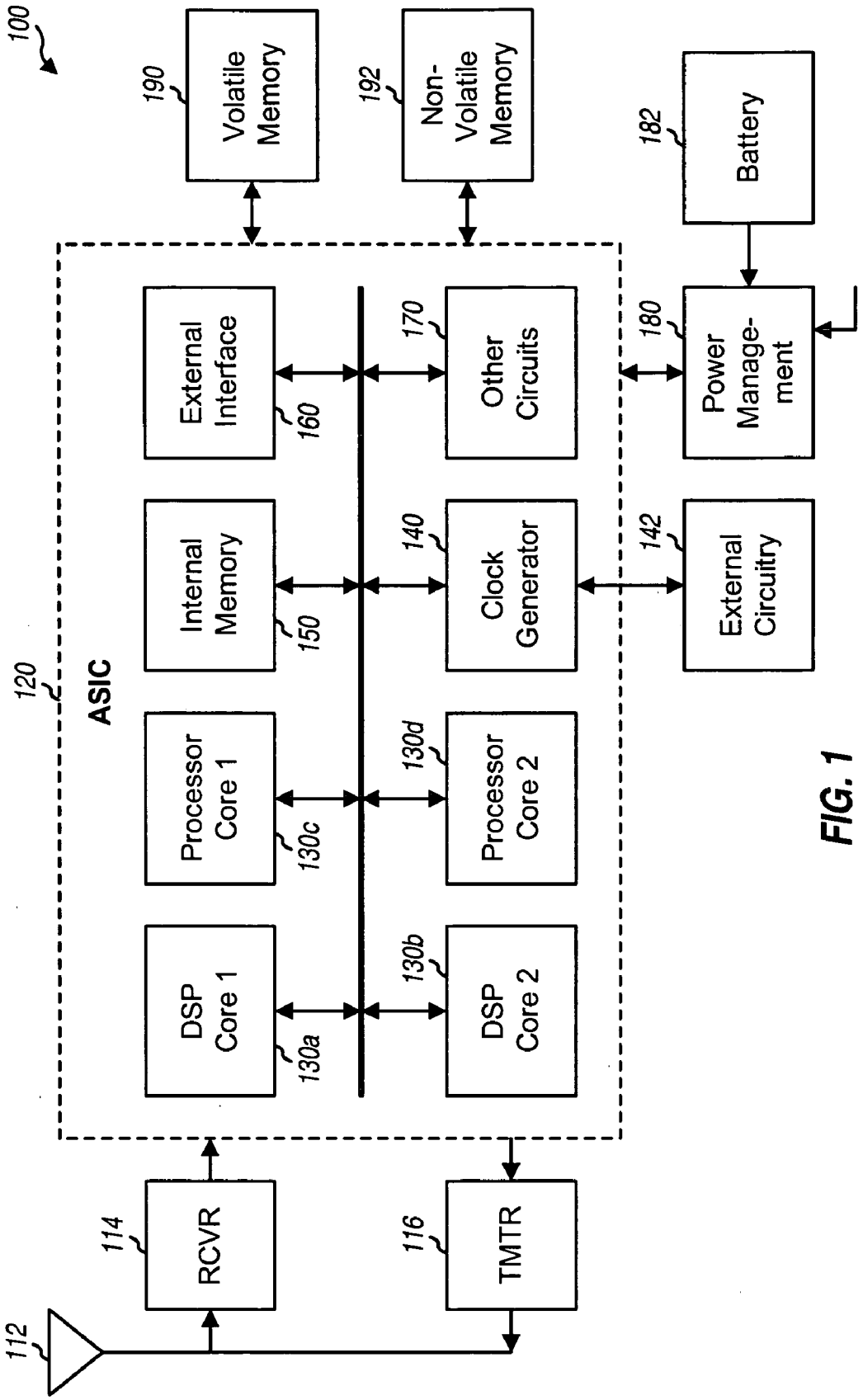

100
190
Volatile Memory
192
Non-Volatile Memory
182
Battery
120
ASIC
External Interface
160
170
Other Circuits
180
Power Manage-ment
Internal Memory
150
140
Clock Generator
142
External Circuitry
Processor Core 1
130c
130d
Processor Core 2
DSP Core 1
130a
130b
DSP Core 2
114
RCVR
116
TMTR
112

FIG. 1

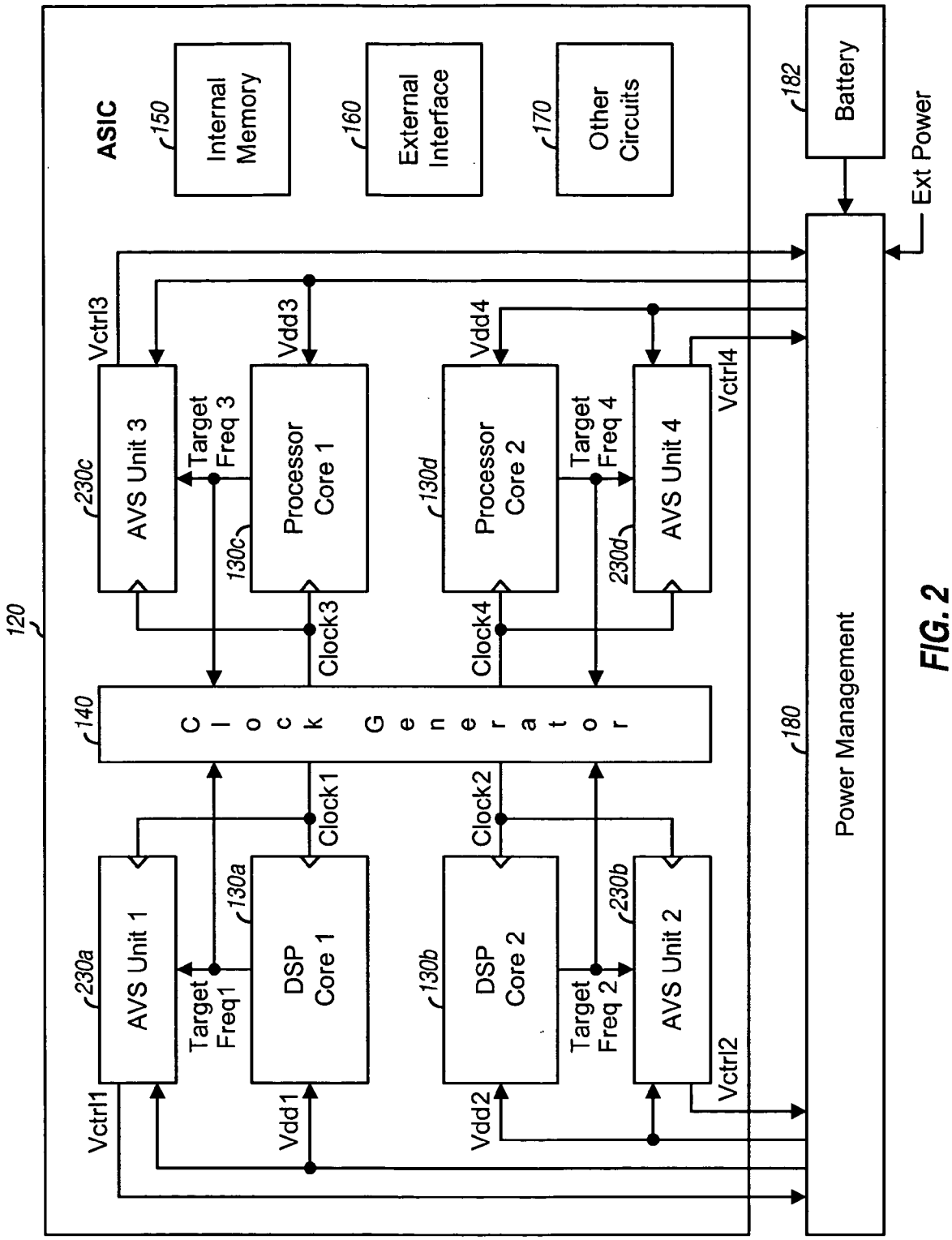

120
ASIC
150
Internal Memory
160
External Interface
170
Other Circuits
182
Battery
Ext Power
Vctrl3
Vdd3
Vdd4
Vctrl4
230c
AVS Unit 3
Target Freq 3
130c
Processor Core 1
130d
Processor Core 2
Target Freq 4
230d
AVS Unit 4
Clock3
Clock4
140
Clock Generator
180
Power Management
Clock1
Clock2
230a
AVS Unit 1
Target Freq1
130a
DSP Core 1
130b
DSP Core 2
Target Freq 2
230b
AVS Unit 2
Vctrl1
Vdd1
Vdd2
Vctrl2

FIG. 2

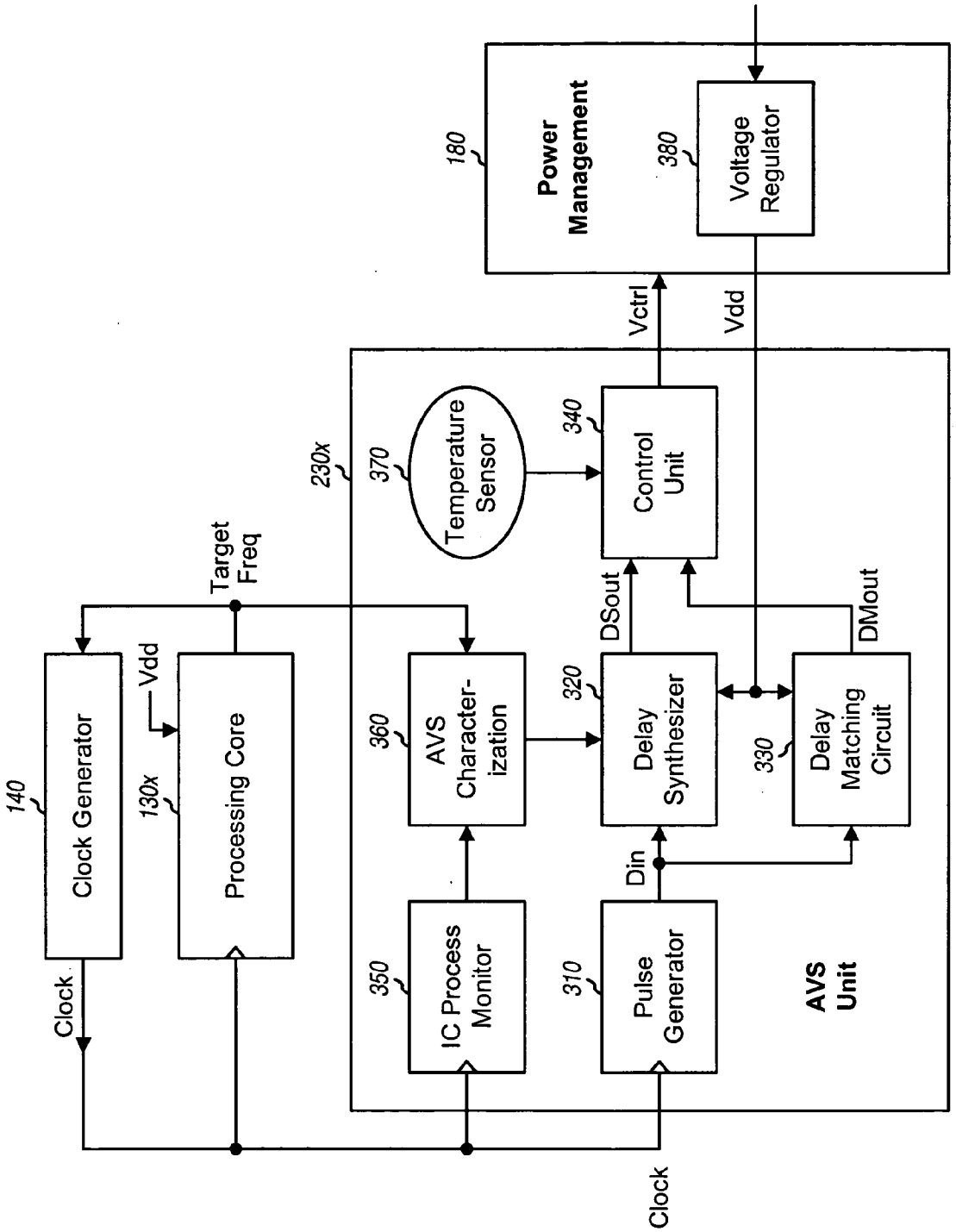

Power Management
180
Voltage Regulator
380
Vctrl
Vdd
230x
370
Temperature Sensor
340
Control Unit
Target Freq
DSout
DMout
Clock Generator
140
Vdd
Processing Core
130x
AVS Character-ization
360
Delay Synthesizer
320
Delay Matching Circuit
330
Din
IC Process Monitor
350
Pulse Generator
310
AVS Unit
Clock
Clock

FIG. 3

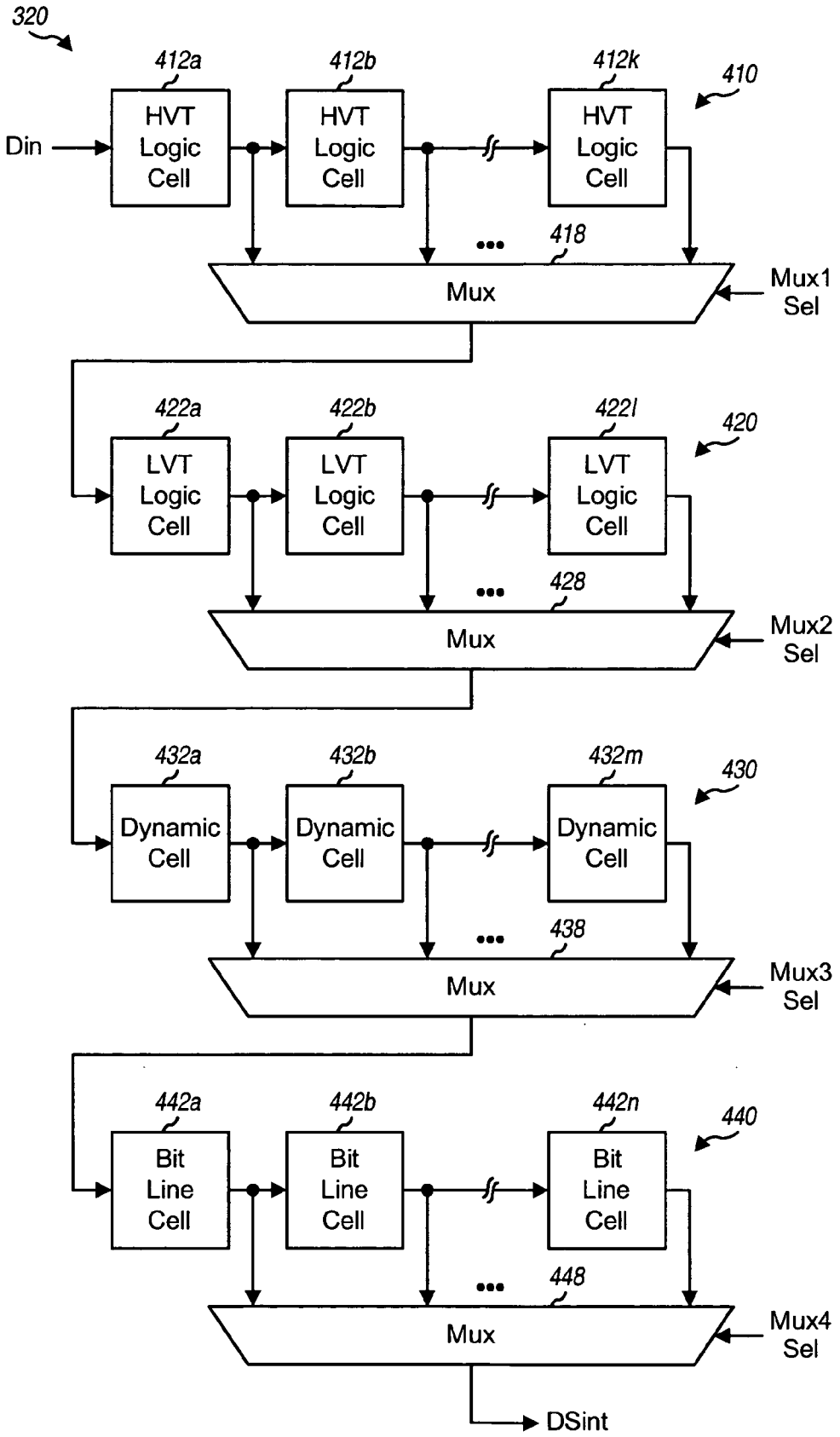

320
412a
412b
412k
410
Din
HVT Logic Cell
HVT Logic Cell
HVT Logic Cell
418
Mux
Mux1 Sel
422a
422b
422l
420
LVT Logic Cell
LVT Logic Cell
LVT Logic Cell
428
Mux
Mux2 Sel
432a
432b
432m
430
Dynamic Cell
Dynamic Cell
Dynamic Cell
438
Mux
Mux3 Sel
442a
442b
442n
440
Bit Line Cell
Bit Line Cell
Bit Line Cell
448
Mux
Mux4 Sel
DSint

FIG. 4A

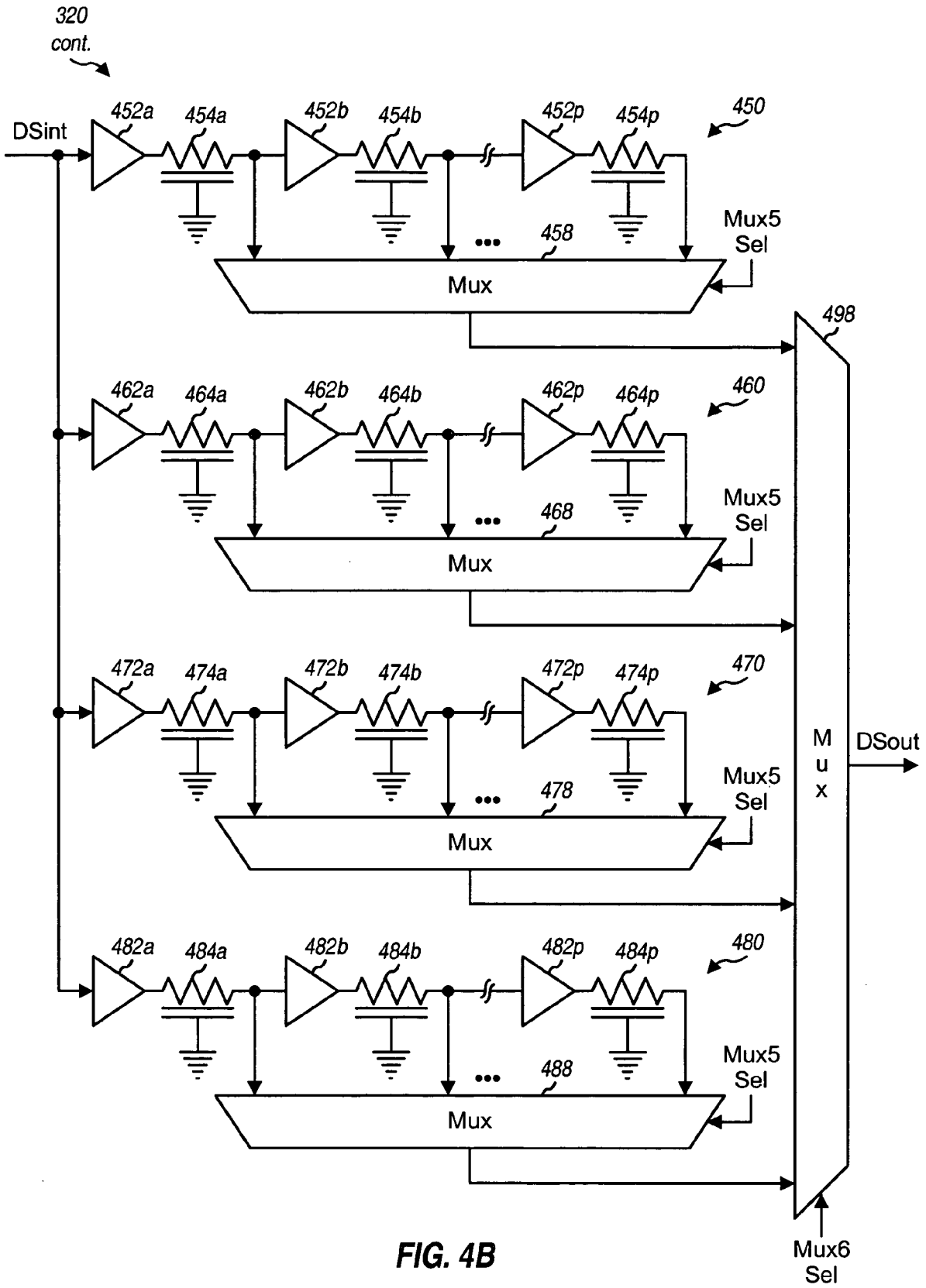

320
cont.
DSint
452a
454a
452b
454b
452p
454p
450
458
Mux5
Sel
Mux
498
462a
464a
462b
464b
462p
464p
460
468
Mux5
Sel
Mux
472a
474a
472b
474b
472p
474p
470
478
Mux5
Sel
Mux
M
u
x
DSout
482a
484a
482b
484b
482p
484p
480
488
Mux5
Sel
Mux
Mux6
Sel

FIG. 4B

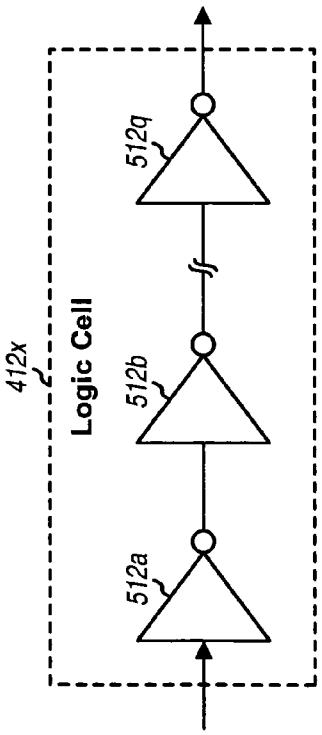


FIG. 5A

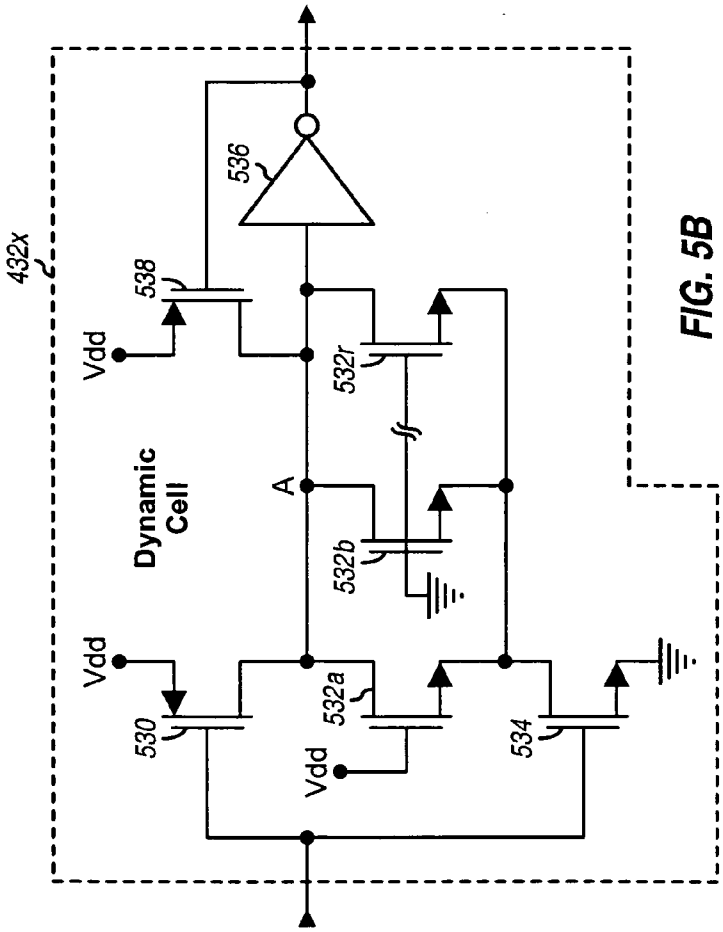


FIG. 5B

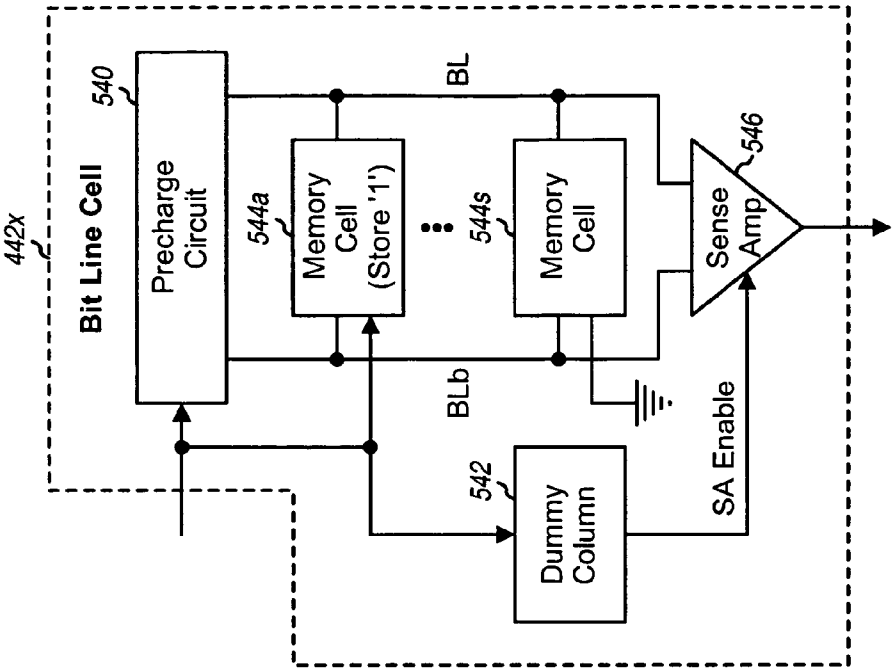


FIG. 5C

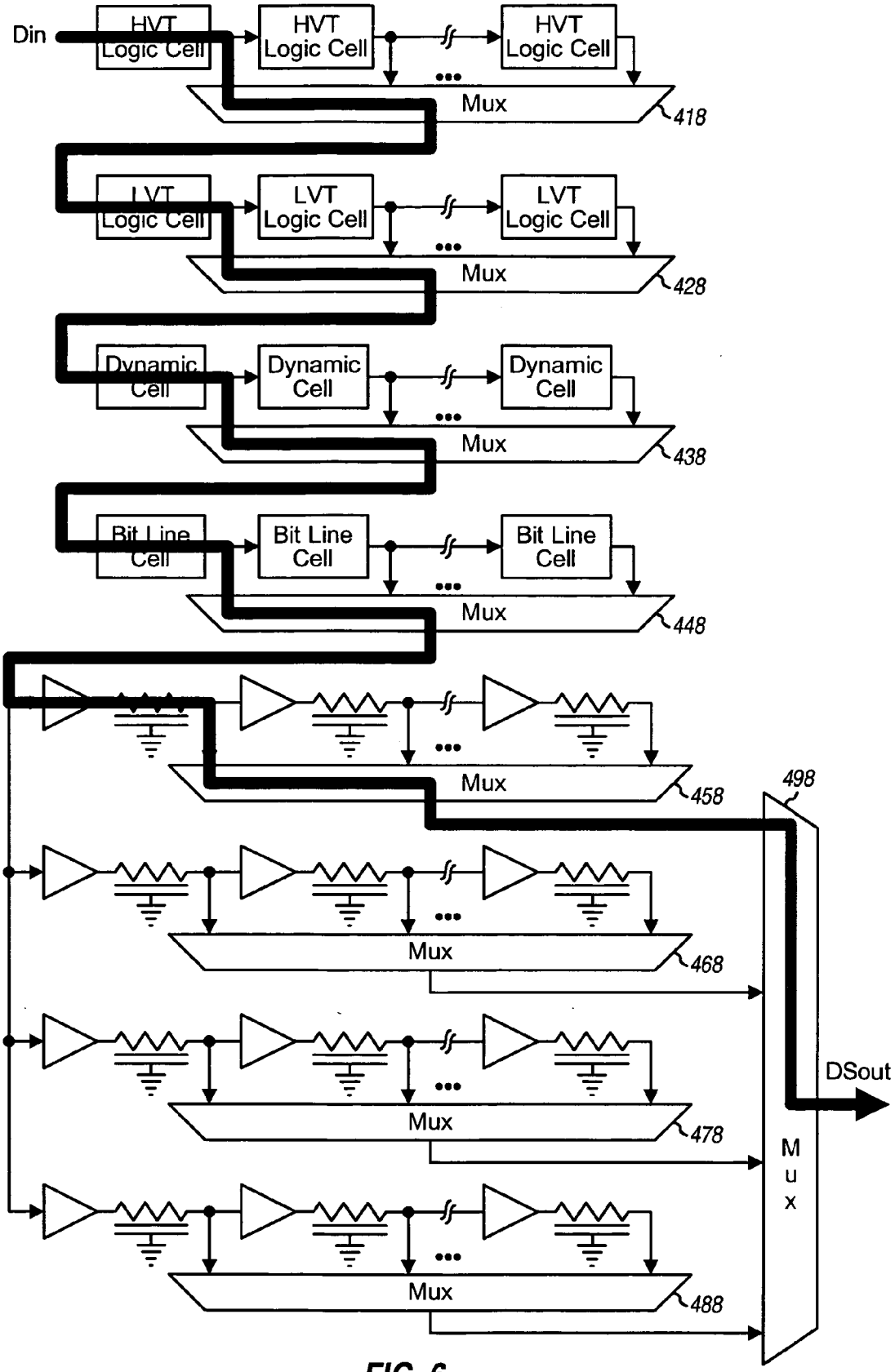

Din
HVT Logic Cell
HVT Logic Cell
HVT Logic Cell
Mux
418
LVT Logic Cell
LVT Logic Cell
LVT Logic Cell
Mux
428
Dynamic Cell
Dynamic Cell
Dynamic Cell
Mux
438
Bit Line Cell
Bit Line Cell
Bit Line Cell
Mux
448
Mux
458
498
Mux
468
DSout
Mux
478
M
u
x
Mux
488

FIG. 6

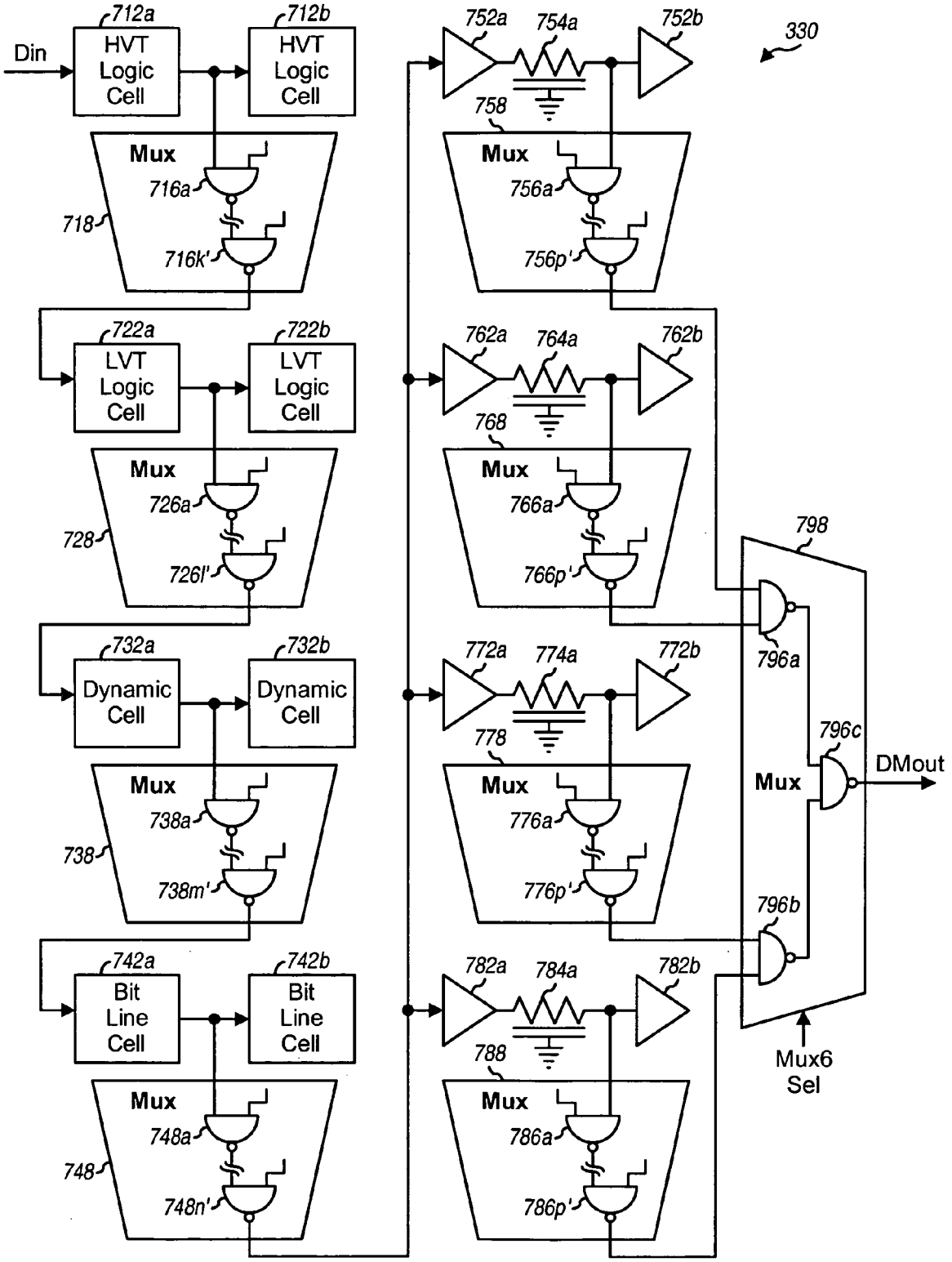

Din
712a
HVT Logic Cell
712b
HVT Logic Cell
Mux
716a
718
716k'
722a
LVT Logic Cell
722b
LVT Logic Cell
Mux
726a
728
726l'
732a
Dynamic Cell
732b
Dynamic Cell
Mux
738a
738
738m'
742a
Bit Line Cell
742b
Bit Line Cell
Mux
748a
748
748n'
752a
754a
752b
330
758
Mux
756a
756p'
762a
764a
762b
768
Mux
766a
766p'
772a
774a
772b
778
Mux
776a
776p'
782a
784a
782b
788
Mux
786a
786p'
798
796a
796c
Mux
DMout
796b
Mux6 Sel

FIG. 7

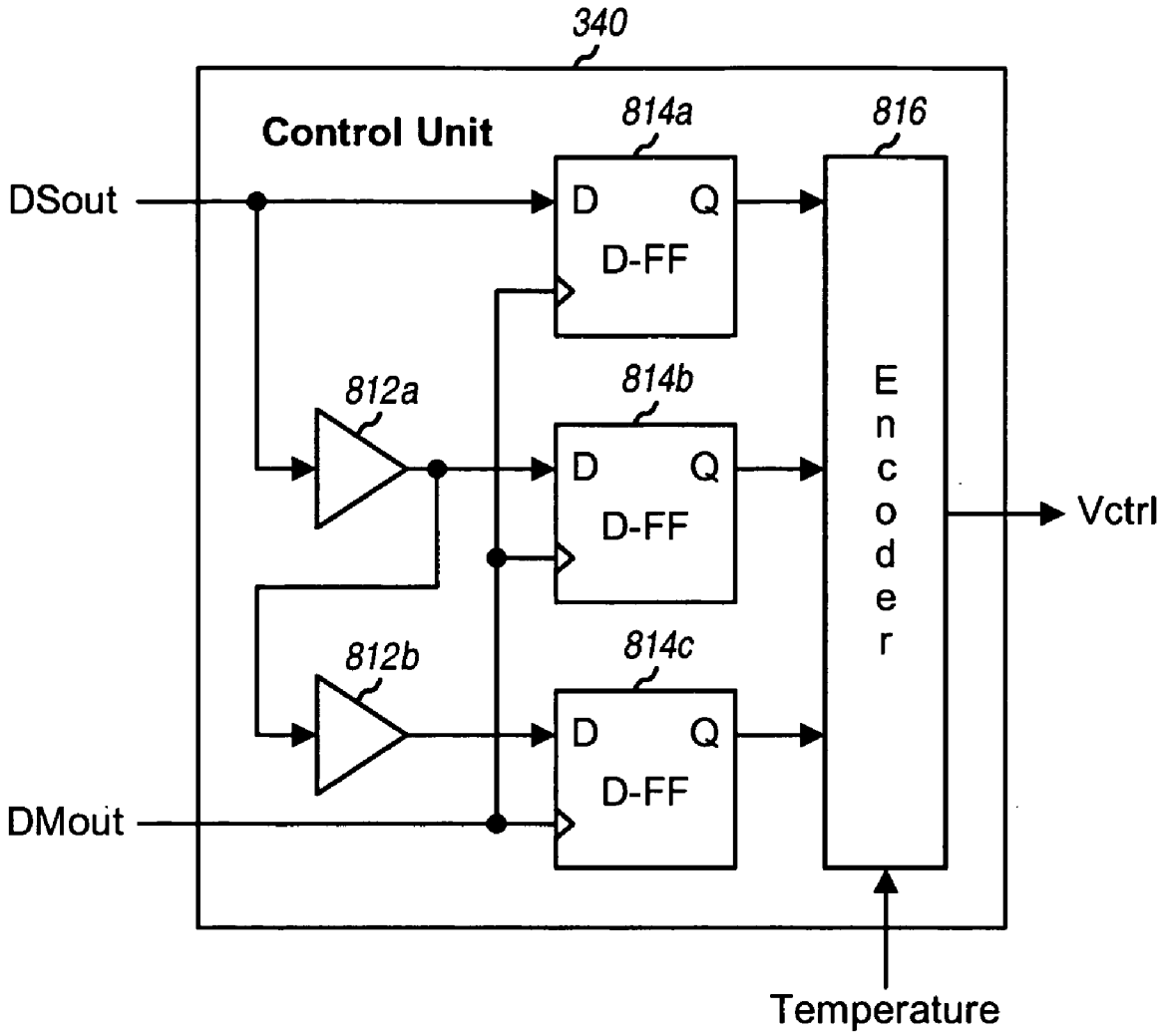

340
Control Unit
814a
816
DSout
D
Q
D-FF
812a
814b
E
n
c
o
d
e
r
D
Q
D-FF
Vctrl
812b
814c
D
Q
D-FF
DMout
Temperature

FIG. 8

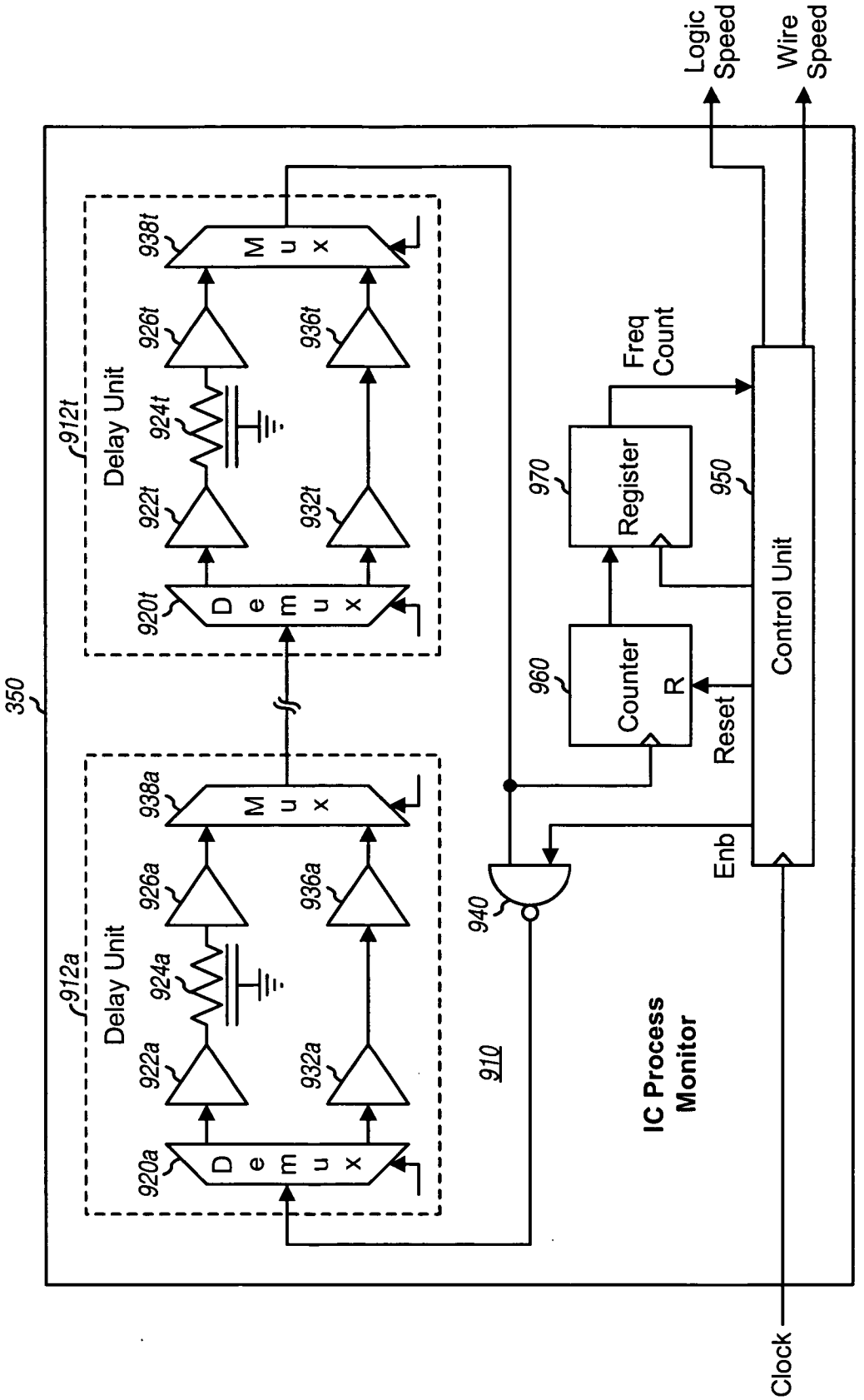

350
Delay Unit
912a
920a
922a
924a
926a
932a
936a
938a
Delay Unit
912t
920t
922t
924t
926t
932t
936t
938t
Demux
Mux
940
910
IC Process Monitor
Counter
960
R
Reset
Register
970
Freq Count
Control Unit
950
Enb
Logic Speed
Wire Speed
Clock

FIG. 9

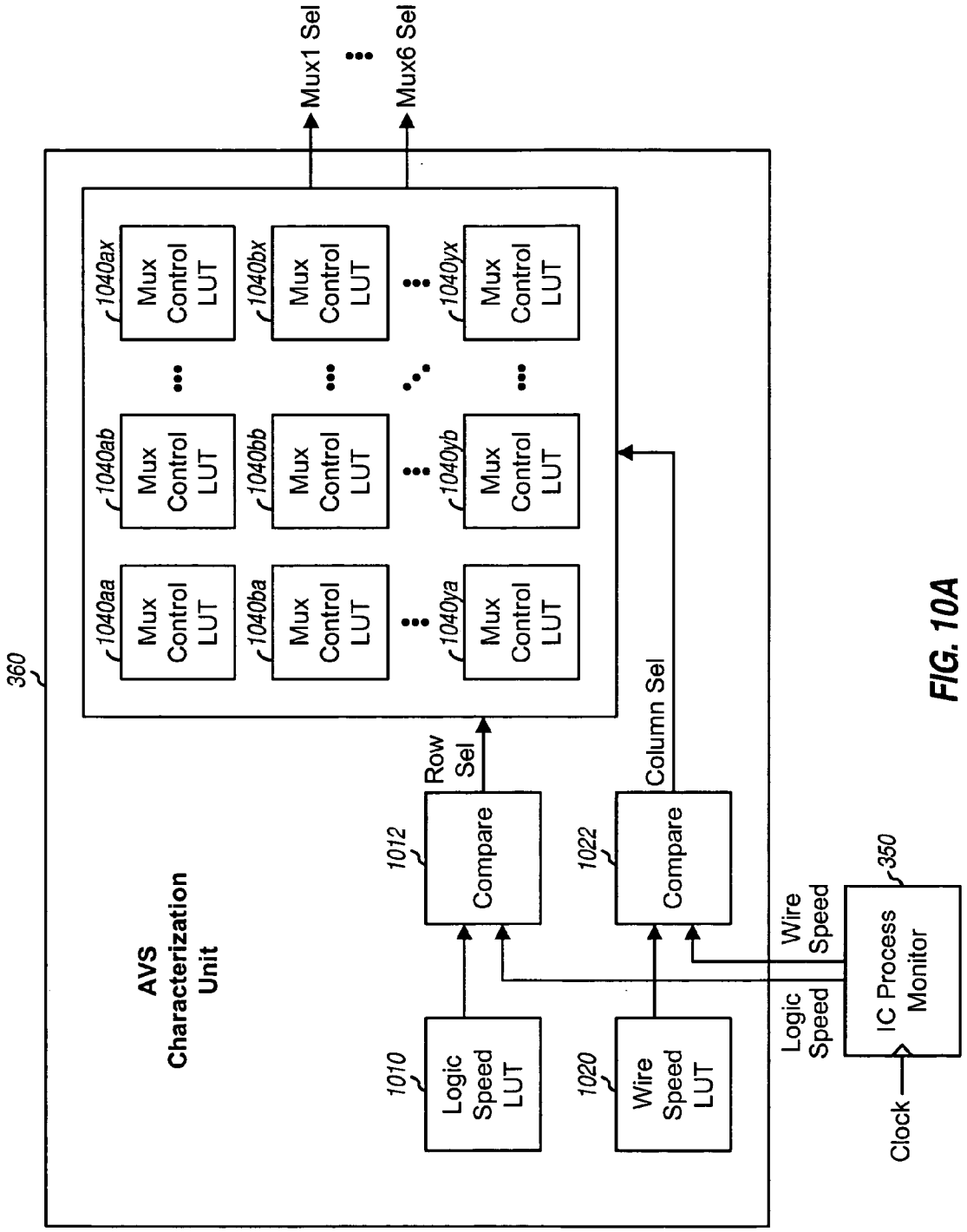

360
AVS Characterization Unit
Mux1 Sel
Mux6 Sel
1040aa
1040ab
1040ax
1040ba
1040bb
1040bx
1040ya
1040yb
1040yx
Mux Control LUT
Row Sel
Column Sel
1012
Compare
1022
Compare
1010
Logic Speed LUT
1020
Wire Speed LUT
Wire Speed
Logic Speed
350
IC Process Monitor
Clock

FIG. 10A

1040ij

	Mux1 Sel	Mux2 Sel	Mux3 Sel	Mux4 Sel	Mux5 Sel	Mux6 Sel
Freq 1	a_1	b_1	c_1	d_1	e_1	f_1
Freq 2	a_2	b_2	c_2	d_2	e_2	f_2
Freq 3	a_3	b_3	c_3	d_3	e_3	f_3
⋮	⋮	⋮	⋮	⋮	⋮	⋮
Freq V	a_V	b_V	c_V	d_V	e_V	f_V

FIG. 10B

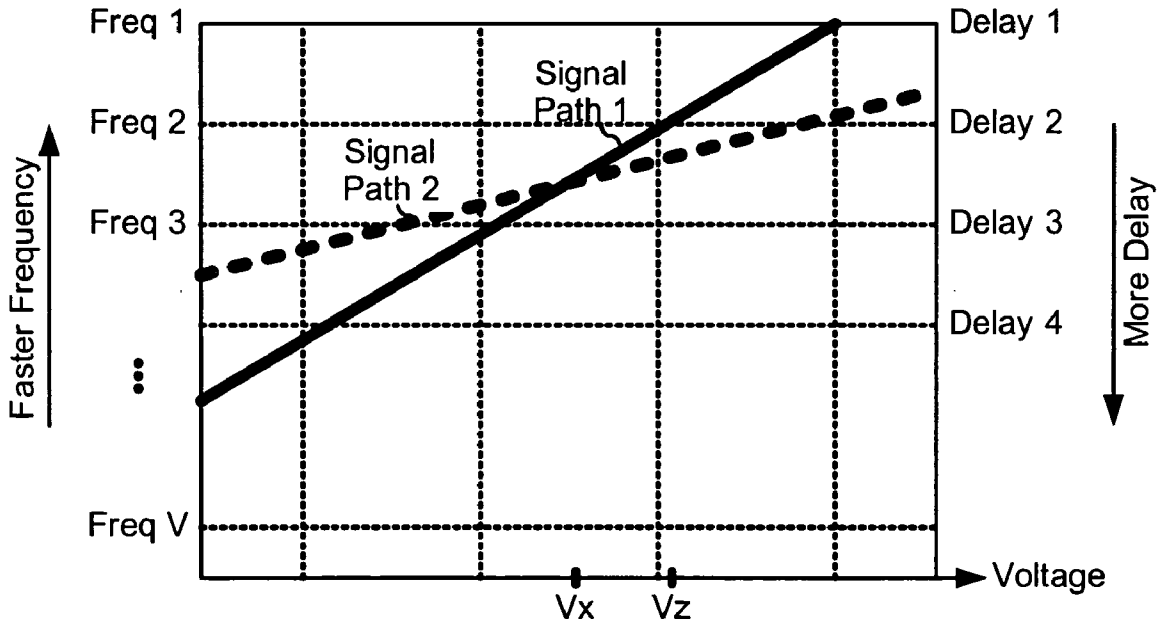


FIG. 11

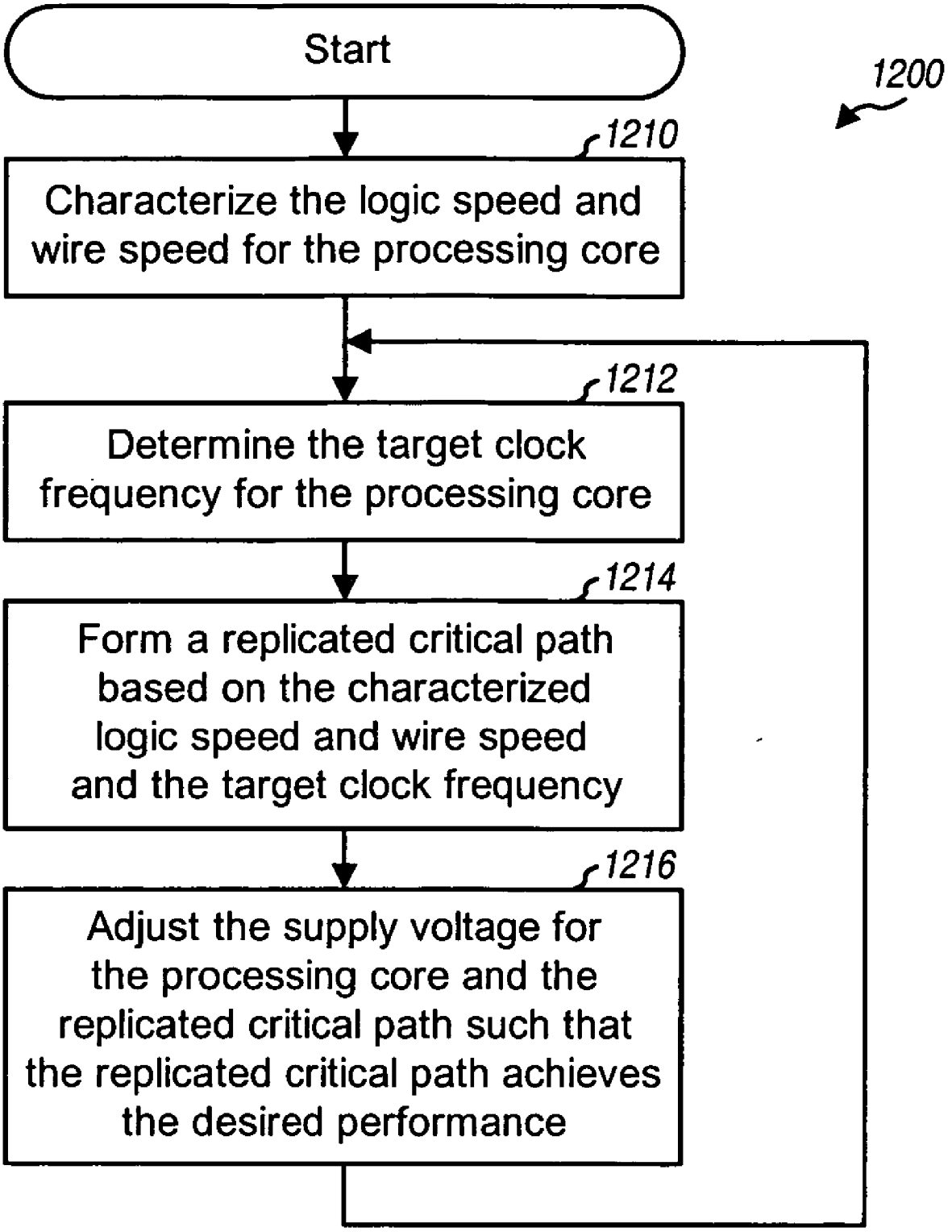

Start
1200
1210
Characterize the logic speed and wire speed for the processing core
1212
Determine the target clock frequency for the processing core
1214
Form a replicated critical path based on the characterized logic speed and wire speed and the target clock frequency
1216
Adjust the supply voltage for the processing core and the replicated critical path such that the replicated critical path achieves the desired performance

FIG. 12

ADAPTIVE VOLTAGE SCALING FOR AN ELECTRONICS DEVICE

RELATED APPLICATIONS

[0001] This application claims the benefit of provisional U.S. Application Ser. No. 60/732,228, entitled "ADAPTIVE VOLTAGE SCALING FOR AN ELECTRONICS DEVICE," filed Oct. **31**, **2005**, assigned to the assignee of the present application, and incorporated herein by reference in its entirety for all purposes

BACKGROUND

[0002] 1. Field

[0003] The present disclosure relates generally to circuits, and more specifically to techniques for conserving battery power for an electronics device.

[0004] 2. Background

[0005] Wireless devices (e.g., cellular phones) are widely used for various applications such as wireless communication, messaging, video, gaming, and so on. The applications and functions for wireless devices are continually expanding to meet growing consumer demands. Consequently, more sophisticated wireless devices are continually being designed with higher level of integration and faster operating speed in order to support more applications and functions with small device sizes.

[0006] Highly integrated wireless devices may consume more power. This may be especially true when operating at a high clock. Higher power consumption can shorten battery life, which is highly undesirable since long battery life is an important design and marketing parameter for portable wireless devices. Hence, a great deal of design effort is often devoted to extending battery life while achieving good performance. For example, wireless devices are often designed to power down as much circuitry as possible when operating in an idle mode to conserve power. An effective method for reducing power consumption when operating in an active mode is to scale or adjust the supply voltage since power consumption is approximately a quadratic function of supply voltage. For example, reducing the supply voltage by 10 percent may save power consumption by almost 20 percent.

[0007] The goal of supply voltage scaling is to reduce the supply voltage as much as possible while maintaining the required performance. This may be achieved by identifying a critical signal path in an integrated circuit (IC), e.g., the signal path with the longest delay, and adjusting the supply voltage such that the critical signal path meets timing requirements. This criterion is difficult to establish in modem VLSI circuits for several reasons. First, the critical signal path can change as the supply voltage is varied. One signal path may be critical at one supply voltage while another signal path may be critical at another supply voltage. Second, at a given supply voltage, the critical signal path may vary from die to die based on IC process and temperature variations. Conventionally, these variations are accounted for by adding a large safety margin to ensure proper operation in all conditions. This large safety margin typically results in higher power consumption much of the time.

[0008] There is therefore a need in the art for techniques to more effectively conserve battery power for a wireless device.

SUMMARY

[0009] Techniques for adaptively scaling supply voltage for electronics devices (e.g., cellular phones) are described herein. In a specific embodiment, the logic speed and the wire speed for a processing core are characterized, e.g., using a ring oscillator. A target clock frequency for the processing core is determined, e.g., based on computational requirements for the core. A replicated critical path is formed based on the characterized logic speed and wire speed and the target clock frequency and using a set of programmable delay lines. This replicated critical path emulates the actual critical path in the processing core and may include different types of circuit components such as, e.g., logic cells with different threshold voltages, dynamic cells, bit line cells, wires, drivers with different threshold voltages and/or fan-outs, and so on, as described below. The supply voltage for the processing core and the replicated critical path is adjusted such that both achieve the desired performance.

[0010] Various aspects and embodiments of the invention are described in further detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The features and nature of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters identify correspondingly throughout.

[0012] FIG. **1** shows a block diagram of a wireless device.

[0013] FIG. **2** shows an ASIC with adaptive voltage scaling (AVS).

[0014] FIG. **3** shows an AVS unit for a processing core.

[0015] FIGS. **4**A and **4**B show a delay synthesizer within the AVS unit.

[0016] FIGS. **5**A, **5**B and **5**C show a logic cell, a dynamic cell, and a bit line cell, respectively, within the delay synthesizer.

[0017] FIG. **6** shows a replicated critical path with a minimum number of cells.

[0018] FIG. **7** shows a delay matching circuit within the AVS unit.

[0019] FIG. **8** shows a control unit within the AVS unit.

[0020] FIG. **9** shows an IC process monitor unit within the AVS unit.

[0021] FIGS. **10**A and **10**B show an AVS characterization unit within the AVS unit.

[0022] FIG. **11** shows plots of the performance of two signal paths.

[0023] FIG. **12** shows a process for performing adaptive voltage scaling.

DETAILED DESCRIPTION

[0024] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any

embodiment or design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments or designs.

[0025] The adaptive voltage scaling techniques described herein may be used for various types of integrated circuits. For example, these techniques may be used for an application specific integrated circuit (ASIC), a digital signal processor (DSP), a digital signal processing device (DSPD), a programmable logic device (PLD), a field programmable gate array (FPGA), a processor, a controller, a microprocessor, and so on. These techniques may also be used for various electronics devices such as wireless communication devices, cellular phones, personal digital assistants (PDAs), portable computers, and so on. For clarity, the techniques are described below for an ASIC within a wireless device, e.g., a cellular phone.

[0026] FIG. **1** shows a block diagram of a wireless device **100**, which may be able to monitor and/or communicate with one or more wireless communication systems. On the receive path, an antenna **112** receives signals transmitted by base stations and/or satellites and provides a received signal to a receiver (RCVR) **114**. Receiver **114** processes (e.g., filters, amplifies, frequency downconverts, and digitizes) the received signal and provides samples to an ASIC **120** for further processing. On the transmit path, ASIC **120** processes data to be transmitted and provides data chips to a transmitter (TMTR) **116**. Transmitter **116** processes (e.g., converts to analog, filters, amplifies, and frequency upconverts) the data chips and generates a modulated signal, which is transmitted via antenna **112**.

[0027] ASIC **120** includes various processing units that support monitoring and/or communication with one or more communication systems. For the embodiment shown in FIG. **1**, ASIC **120** includes DSP cores **130***a* and **130***b*, processor cores **130***c* and **130***d*, a clock generator **140**, an internal memory **150**, an external interface unit **160**, and other circuits **170**. DSP cores **130***a* and **130***b*, perform processing (e.g., demodulation and decoding) for the receive path, processing (e.g., encoding and modulation) for the transmit path, and/or processing for other applications and functions. Each DSP core may include one or more multiply-and-accumulate (MAC) units, one or more arithmetic logic units (ALUs), and so on. Processor cores **130***c* and **130***d* support various functions such as video, audio, graphics, gaming, and so on.

[0028] Clock generator **140** generates clocks used by the processing units within ASIC **120** and may couple to external circuitry **142**, which may include crystals, inductors, capacitors, and so on. Clock generator **140** may include one or more phase locked loops (PLLs) that control the oscillators used to generate the clocks. Internal memory **150** stores data and program codes used by the processing units within ASIC **120**. External interface unit **160** interfaces with other units external to ASIC **120**. Other circuits **170** may include a power control unit that controls power to various processing units within ASIC **120**, PLLs for receiver **114** and transmitter **116**, and/or other circuitry.

[0029] For the embodiment shown in FIG. **1**, ASIC **120** further couples to a power management unit **180**, a volatile memory **190**, and a non-volatile memory **192**. Power management unit **180** couples to a battery **182** and also receives external power via a power connector. Power management unit **180** conditions the received power supply and provides regulated supply voltages for the processing units within ASIC **120**. Volatile memory **190** provides bulk storage for data and program codes used by ASIC **120**. Non-volatile memory **192** provides bulk non-volatile storage.

[0030] In general, wireless device **100** may include fewer, more and/or different integrated circuits than those shown in FIG. **1**. Furthermore, ASIC **120** may include fewer, more and/or different processing units than those shown in FIG. **1**. In general, ASIC **120** may include any number of DSP cores and any number of processor cores. The number of processing units and the types of processing units included in ASIC **120** are typically dependent on various factors such as the communication systems, applications, and functions supported by wireless device **100**.

[0031] FIG. **2** shows an embodiment of ASIC **120** with adaptive voltage scaling (AVS). For this embodiment, one AVS unit **230** is provided for each processing core **130** and is used to adaptively scale the supply voltage for that core. In particular, AVS units **230***a* and **230***b* perform adaptive voltage scaling for DSP cores **130***a* and **130***b*, respectively, and AVS units **230***c* and **230***d* perform adaptive voltage scaling for processor cores **130***c* and **130***d*, respectively.

[0032] Each processing core **130** receives from clock generator **140** a clock used to trigger synchronous circuits within the core. Each core **130** provides to clock generator **140** and to its AVS unit **230** a target frequency for its clock. This target frequency may be selected based on the processing load and computational requirements for the core. For each processing core **130**, clock generator **140** generates the clock at the target frequency and provides this clock to the core as well as to the associated AVS unit **230**. Each processing core **130** and its associated AVS unit **230** also receive a regulated supply voltage (Vdd) from power management unit **180**. The supply voltage for each processing core **130** is set by the associated AVS unit **230** such that the core can operate at the target clock frequency.

[0033] For the embodiment shown in FIG. **2**, the clock for each processing core **130** may be set independently by clock generator **140**, and the supply voltage for each processing core **130** may be set independently by power management unit **180**. In other embodiments, multiple processing cores may share a common clock and/or a common supply voltage that may be jointly set for these cores.

[0034] Adaptive voltage scaling is a closed loop system that adjusts the supply voltage to a level that satisfies performance requirements, which may be quantified by proper operation at a target frequency. In general, a higher supply voltage corresponds to less delay, which allow for operation at a higher frequency with a faster clock. The peak supply voltage can provide the shortest delay and the highest performance level. However, this highest performance level is not required some or much of the time. In such instances, the supply voltage may be reduced. Adaptive voltage scaling thus exploits the variations in computational requirements to scale the supply voltage and reduce the average power consumption while maintaining the required performance. As a result, battery life may be extended, which is highly desirable.

[0035] AVS unit **230** for each processing core **130** adjusts the supply voltage such that the core can meet its perfor-

mance requirements. In an embodiment, each AVS unit simulates the actual performance of the associated core across IC process, temperature, and voltage variations. Each AVS unit emulates the critical path for the associated core, tracks the performance of this critical path, and adjusts the supply voltage to the lowest possible level that allows the critical path to achieve the target performance. The ability to closely track the actual critical path for different conditions results in a highly efficient adaptive voltage scaling.

[0036] Each AVS unit **230** tracks the performance of the critical path in the associated processing core **130**. In an embodiment, this is achieved using a delay synthesizer having a blend of circuit components that closely matches the circuit blend for the critical path in the associated core. These circuit components may include logic cells, transistor devices with different threshold voltages, dynamic cells, bit line cells, wires, drivers with different threshold voltages and/or fan-outs, and so on, which are described below. These different circuit components have electrical characteristics (e.g., delays) that may vary in different manners across IC process, temperature, and voltage variations.

[0037] Logic cells may be formed with inverters and/or other logic gates. The inverters and logic gates are implemented with transistors, which may be P-channel field effect transistors (P-FETs), N-channel FETs (N-FETs), and so on. Each FET device is designed with a particular threshold voltage, which is the voltage at which the device turns on. A low threshold voltage (LVT) results in less delay through the FET device but higher leakage current, which is the current passing through the FET device when it is turned off. Conversely, a high threshold voltage (HVT) results in lower leakage current but more delay. A combination of LVT and HVT devices may be used to achieve good performance where needed and low leakage where required. The electrical characteristics of LVT and HVT devices may vary in different manners with IC process, temperature, and voltage. Computer simulation indicates that an HVT inverter with a drive capability or fan-out of four has a delay that tracks well with the delays of other HVT logic gates. However, the delay of this HVT inverter has a large deviation from the delay of an LVT inverter.

[0038] Wires are relatively long traces etched on an IC die to interconnect circuit components on the IC die. The delay of a wire is affected by the length, width and height of the wire as well as the fan-out of a driver for that wire. The length and width of a wire are typically selected by design, and the thickness of the wire is typically fixed by the IC manufacturing process. The delay of a 2 millimeter (mm) wire may vary by up to 2 orders of magnitude relative to the delay of an HVT inverter with a fan-out of four for a certain voltage range. The delay of a driver varies more relative to the delay of an HVT inverter as the fan-out of the driver increases. Wires have a larger impact on critical path performance as technology feature/transistor size shrinks, the IC die area to feature size ratio increases, and more logic cells are packed into an IC die. This is because more wires are used to connect logic cells as the level of integration increases. Furthermore, wire resistance and capacitance also increase with shrinking geometries. Therefore, a conventional delay synthesizer or a conventional ring oscillator that is composed of mostly logic cells does not accurately track the performance of a critical path that includes wires.

[0039] FIG. **3** shows an embodiment of an AVS unit **230***x* for an associated processing core **130***x*. AVS unit **230***x* may be used for each of AVS units **230***a* through **230***d* in FIG. **2**, and processing core **130***x* may be any one of cores **130***a* through **130***d*.

[0040] Within AVS unit **230***x*, a pulse generator **310** receives a clock from clock generator **140**. In an embodiment, which not shown in FIG. **3**, pulse generator **310** generates a first input signal (DSin) for a delay synthesizer **320** and a second input signal (DMin) for a delay matching circuit **330**. The DSin and DMin signals may each include a pulse for each leading edge in the clock. The pulse on the DMin signal may be delayed by a fixed amount relative to the pulse on the DSin signal. In another embodiment, which is described below, pulse generator **310** generates a single input signal (Din) that is provided to both delay synthesizer **320** and delay matching circuit **330**. The pulse on the Din signal propagates through delay synthesizer **320** and is received via a first input of a control unit **340**. The pulse on the Din signal also propagates through delay matching circuit **330** and is received via a second input of control unit **340**. Delay synthesizer **320** models the critical path for processing core **130***x*. Delay synthesizer **320** includes multiplexers that allow for flexible programming of the delay synthesizer. However, these multiplexers introduce additional delays that may be substantial relative to the total delay of the critical path being replicated. Delay matching circuit **330** accounts for the multiplexer delays within delay synthesizer **320**.

[0041] Control unit **340** receives the pulses from delay synthesizer **320** and delay matching circuit **330** and measures the "pure" delay of the replicated critical path within delay synthesizer **320** based on the received pulses. Control unit **340** generates a voltage control (Vctrl) based on the measured critical path delay and possibly a temperature measurement from a temperature sensor **370**. A voltage regulator **380** within power management unit **180** receives the voltage control from control unit **340**, adjusts the regulated supply voltage (Vdd) based on the voltage control, and provides the regulated supply voltage to processing core **130***x*, delay synthesizer **320**, and delay matching circuit **330**.

[0042] An IC process monitor unit **350** determines the logic and wire delays for ASIC **120** and provides this information to an AVS characterization unit **360**. Unit **360** also receives the target clock frequency for processing core **130***x* and provides Mux Sel signals (as shown in FIG. **3**) that select an appropriate blend of circuit components for the replicated critical path within delay synthesizer **320**. The various blocks within AVS unit **230***x* are described in detail below.

[0043] As shown in FIG. **3**, AVS unit **230***x* is part of a closed-loop system that scales the supply voltage to achieve the desired performance for a critical path within processing core **130***x*. Delay synthesizer **320** may be programmed to obtain a replicated critical path having a blend of circuit components that matches the actual critical path in processing core **130***x*. Furthermore, delay synthesizer **320** may be programmed with different blends of circuit components to track changes in the actual critical path due to IC process and/or other variations. This enables close tracking of the actual critical path and results in high efficiency.

[0044] FIGS. **4**A and **4**B show an embodiment of delay synthesizer **320** within AVS unit **230***x* in FIG. **3**. For this

embodiment, delay synthesizer **320** includes multiple delay lines, with each delay line being composed of a different type of circuit component.

[**0045**] Within delay synthesizer **320**, the Din signal from pulse generator **310** is provided to the input of a delay line **410** composed of K series-connected logic cells **412***a* through **412***k* (e.g., K=32). Each logic cell **412** may be implemented with inverters and/or logic gates formed with HVT devices. The outputs of the K logic cells **412***a* through **412***k* are provided to K inputs of a multiplexer (Mux) **418**. Multiplexer **418** provides one of the K inputs as the multiplexer output based on a Mux**1** Sel control.

[**0046**] The output of multiplexer **418** is provided to the input of a delay line **420** composed of L series-connected logic cells **422***a* through **4221** (e.g., L=32). Each logic cell **422** may be implemented with inverters and/or logic gates formed with LVT devices. The outputs of the L logic cells **422***a* through **4221** are provided to L inputs of a multiplexer **428**. Multiplexer **428** provides one of the L inputs as the multiplexer output based on a Mux**2** Sel control.

[**0047**] The output of multiplexer **428** is provided to the input of a delay line **430** composed of M series-connected dynamic cells **432***a* through **432***m* (e.g., M=32). Dynamic cells **432** are used to model diffusion capacitance. Diffusion capacitance is a result of the capacitive effect of the drain-to-well reverse-biased junction, which is different from the gate capacitance modeled by the delay lines **410** and **420**. Each dynamic cell may be implemented as described below. The outputs of the M dynamic cells **432***a* through **432***m* are provided to M inputs of a multiplexer **438**. Multiplexer **438** provides one of the M inputs as the multiplexer output based on a Mux**3** Sel control.

[**0048**] The output of multiplexer **438** is provided to the input of a delay line **440** composed of N series-connected bit line cells **442***a* through **442***n* (e.g., N=4). Bit line cells **442** are used to track memory access delays and may be implemented as described below. The outputs of the N bit line cells **442***a* through **442***n* are provided to N inputs of a multiplexer **448**. Multiplexer **448** provides one of the N inputs as the multiplexer output (DSint) based on a Mux**4** Sel control.

[**0049**] Referring to FIG. **4**B, the output of multiplexer **448** (DSint) is provided to the inputs of four delay lines **450**, **460**, **470** and **480**. Each of delay lines **450**, **460**, **470** and **480** is composed of P series-connected wire cells (e.g., P=8). Each wire cell includes a driver and a wire. For delay line **450**, drivers **452***a* through **452***p* are implemented with HVT devices and have fan-outs of FOa (e.g., FOa=8). For delay line **460**, drivers **462***a* through **462***p* are implemented with HVT devices and have fan-outs of FOb (e.g., FOb=16). For delay line **470**, drivers **472***a* through **472***p* are implemented with LVT devices and have fan-outs of FOa. For delay line **480**, drivers **482***a* through **482***p* are implemented with LVT devices and have fan-outs of FOb. Each wire has series resistance and parasitic capacitance determined by the length, width and thickness of the wire. The wires for delay lines **450**, **460**, **470** and **480** may be designed to have the same or different lengths (e.g., the same length of 1 mm).

[**0050**] For delay line **450**, drivers **452***a* through **452***p* drive wires **454***a* through **454***p*, respectively, which further couple to P inputs of a multiplexer **458**. Multiplexer **458** provides one of the P inputs as the multiplexer output based on a Mux**5** Sel control. For delay line **460**, drivers **462***a* through **462***p* drive wires **464***a* through **464***p*, respectively, which further couple to P inputs of a multiplexer **468**. Multiplexer **468** provides one of the P inputs as the multiplexer output based on the Mux**5** control. For delay line **470**, drivers **472***a* through **472***p* drive wires **474***a* through **474***p*, respectively, which further couple to P inputs of a multiplexer **478**. Multiplexer **478** provides one of the P inputs as the multiplexer output based on the Mux**5** Sel control. For delay line **480**, drivers **482***a* through **482***p* drive wires **484***a* through **484***p*, respectively, which further couple to P inputs of a multiplexer **488**. Multiplexer **488** provides one of the P inputs as the multiplexer output based on the Mux**5** Sel control. A multiplexer **498** receives the outputs of multiplexers **458**, **468**, **478** and **488** and, based on a Mux**6** Sel control, provides the output of one of these four multiplexers as the delay synthesizer output (DSout).

[**0051**] For the embodiment shown in FIGS. **4**A and **4**B, the Din signal passes through at least one cell in each delay line. In another embodiment, the input signal for each delay line may be provided to one input of the multiplexer for that delay line. For this embodiment, the Din signal can pass directly through the multiplexer and bypass all of the cells in the delay line.

[**0052**] For the delay synthesizer structure shown in FIGS. **4**A and **4**B, delay line **410** emulates logic delays for HVT devices, delay line **420** emulates logic delays for LVT devices, delay line **430** emulates diffusion delays, delay line **440** emulates memory access delays, delay line **450** emulates wire delays with HVT drivers having fan-outs of FOa, delay line **460** emulates wire delays with HVT drivers having fan-outs of FOb, delay line **470** emulates wire delays with LVT drivers having fan-outs of FOa, and delay line **480** emulates wire delays with LVT drivers having fan-outs of FOb.

[**0053**] The delay synthesizer structure shown in FIGS. **4**A and **4**B can flexibly replicate a critical path with a desired blend of circuit components. Each delay line is composed of multiple series-connected cells for a different type of circuit component. The multiplexer for each delay line can include a selectable number of cells for that delay line in the replicated critical path. The same delay synthesizer structure may be used in AVS units **230***a* through **230***d* for cores **130***a* through **130***d*, respectively. The replicated critical path for each core may be individually and flexibly formed by properly controlling the multiplexers in the delay synthesizer for that core. Furthermore, the replicated critical path may be easily varied to match the performance of the actual critical path in the associated core.

[**0054**] In general, a delay synthesizer structure may include any number of delay lines, and each delay line may emulate any type of circuit and may include any number of cells. Such a structure provides great flexibility in replicating a critical path. In another embodiment, a delay synthesizer structure may include multiple hypothesized critical paths, with each hypothesized critical path including a different blend of circuit components. One of the hypothesized critical paths may be selected as the replicated critical path.

[**0055**] FIG. **5**A shows an embodiment of a logic cell **412***x*, which may be used for each of logic cells **412***a* through **412***k*

and **422***a* through **4221** in FIG. **4**A. For this embodiment, logic cell **412***x* is composed of Q series-connected inverters **512***a* through **512***q*, where Q≧1. Q may be selected such that logic cell **412***x* can provide the desired amount of delay across IC process, temperature, and voltage variations. Each inverter **512** may be implemented with HVT or LVT devices. Logic cells **412***a* through **412***k* for delay line **410** in FIG. **4**A may include the same or different numbers of inverters. Logic cells **422***a* through **4221** for delay line **420** may also include the same or different numbers of inverters. Each logic cell may also be implemented with other logic gates (e.g., AND, NAND, OR, NOR, exclusive-OR, or some other logic gate) or any combination of logic gates.

[**0056**] FIG. **5**B shows an embodiment of a dynamic cell **432***x*, which may be used for each of dynamic cells **432***a* through **432***m* in FIG. **4**A. For this embodiment, dynamic cell **432***x* is composed of P-FETs **530** and **538**, R parallel-coupled N-FETs **532***a* through **532***r*, an N-FET **534**, and an inverter **536**, where R≧1. P-FET **530** has its source coupled to the supply voltage, its gate forming the dynamic cell input, and its drain coupled to the drains of N-FETs **532***a* through **532***r*. The gate of N-FET **532***a* is coupled to the supply voltage, and the gates of N-FETs **532***b* through **532***r* are coupled to circuit ground. N-FET **534** has its source coupled to circuit ground, its gates coupled to the dynamic cell input, and its drain coupled to the sources of N-FETs **532***a* through **532***r*. P-FET **538** has its source coupled to the supply voltage, its gate coupled to the output of inverter **536**, and its drains of N-FETs **532***a* through **532***r*. P-FET **538** provides feedback to restore the charge leakage in N-FETs **532***a* through **532***r* when they are all turned off.

[**0057**] The Din signal propagates through dynamic cells **432***a* through **432***m* in delay line **430**. When the Din signal at the input of dynamic cell **432***x* is at logic low, P-FET **530** is turned on and precharges node A to logic high, N-FET **534** is turned off, and the output of inverter **536** is at logic low. When the pulse appears on the Din signal, P-FET **530** is turned off, N-FET **534** is turned on and pulls node A to logic low via N-FET **532***a*, and the output of inverter **536** transitions to logic high. N-FET **532***a* is evaluated and N-FETs **532***b* through **532***r* are not evaluated. The delay through dynamic cells **432***x* is determined by the diffusion capacitance of N-FETs **532***a* through **532***r*.

[**0058**] FIG. **5**C shows an embodiment of a bit line cell **442***x*, which may be used for each of bit line cells **442***a* through **442***n* in FIG. **4**A. For this embodiment, bit line cell **442***x* includes a precharge circuit **540**, a dummy column **542**, S memory cells **544***a* through **544***s*, where S≧1, and a sense amplifier **546**. Upon receiving a pulse on the Din signal at the bit line cell input, precharge circuit **540** precharges both the bit line (BL) and the complementary bit line (BLb) to logic high, and dummy column **542** generates an enable signal for sense amplifier **546**. The Din pulse also selects memory cell **544***a* after a small delay, which is not shown in FIG. **5**C for simplicity. Memory cell **544***a* stores a logic high ('1') and, when enabled, pulls the BLb line to logic low. Sense amplifier **546** senses the voltage difference between the BL and BLb lines and, after a short delay determined by the discharge rate of the BLb line, provides a logic high to one input of multiplexer **448** and to the input of the next bit line cell (if any). Bit line cell **442***x* is able to track memory access delays, e.g., for SRAM, cache, and other memories.

[**0059**] FIG. **6** shows a replicated critical path composed of the minimum number of cells in each delay line for delay synthesizer **320** shown in FIGS. **4**A and **4**B. For this replicated critical path, the Din signal passes through six multiplexers **418**, **428**, **438**, **448**, **458** and **498**. Each multiplexer typically includes multiple levels of logic gates that introduce additional delays. Hence, the total delay observed by the Din signal for the replicated critical path is composed of (1) the delays introduced by the cells used to emulate the actual critical path and (2) the delays introduced by the multiplexers used to form the replicated critical path. The multiplexer delays increase with both the number of multiplexers and the number of inputs for each multiplexer. The multiplexer delays may represent a fairly significant portion of the total delay for the replicated critical path, especially at high speed such as, e.g., 1 GHz and above.

[**0060**] The multiplexer delays may be handled in various manners. In an embodiment, the multiplexer delays are treated as a portion of the logic delays. The delays from other circuit types (e.g., wires, diffusion, and so on) should be sufficiently long to obtain the desired blend of delays (e.g., 20% logic delays and 80% wire delays). For this embodiment, the multiplexers may be implemented with the same device type as most of the logic within the associated core. For example, if the associated core is implemented with mostly LVT devices, then the multiplexers may also be implemented with LVT devices. The delays for other circuit types may be extended, if needed, to obtain the desired blend of delays.

[**0061**] In another embodiment, delay matching circuit **330** is used to estimate the multiplexer delays. The estimated multiplexer delays may then be subtracted from the total delay of delay synthesizer **320** to obtain the "pure" delay of the replicated critical path within the delay synthesizer.

[**0062**] FIG. **7** shows an embodiment of delay matching circuit **330** within AVS unit **230***x* in FIG. **3**. For this embodiment, delay matching circuit **330** includes the same number of delay lines and the same number of multiplexers as delay synthesizer **320**.

[**0063**] Within delay matching circuit **330**, the Din signal from pulse generator **310** is provided to the input of a delay line composed of two series-connected logic cells **712***a* and **712***b*. Logic cell **712***b* simulates the loading for logic cell **712***a* and may be included in delay matching circuit **330** as shown in FIG. **7** or may be omitted. The output of logic cell **712***a* is provided to an input of a partial multiplexer **718** that models the signal path between one input and the output of multiplexer **418**. Multiplexer **718** includes K' series-connected NAND gates **716***a* through **716***k'*, where $K' \approx 2 \cdot \log_2(K)$ and K is the number of inputs for multiplexer **418**.

[**0064**] The output of multiplexer **718** is provided to the input of a delay line composed of two series-connected logic cells **722***a* and **722***b*. A partial multiplexer **728** receives the output of logic cell **722***a* and provides its output to the input of a delay line composed of two series-connected dynamic cells **732***a* and **732***b*. A partial multiplexer **738** receives the output of dynamic cell **732***a* and provides its output to the input of a delay line composed of two series-connected bit line cells **742***a* and **742***b*. A partial multiplexer **748** receives the output of bit line cell **742***a* and provides its output to the inputs of four wire delay lines. The first wire delay line includes a full wire cell composed of a driver **752***a* and a

wire **754***a* and a partial wire cell composed of a driver **752***b*. The second wire delay line includes a full wire cell composed of a driver **762***a* and a wire **764***a* and a partial wire cell composed of a driver **762***b*. The third wire delay line includes a full wire cell composed of a driver **772***a* and a wire **774***a* and a partial wire cell composed of a driver **772***b*. The fourth wire delay line includes a full wire cell composed of a driver **782***a* and a wire **784***a* and a partial wire cell composed of a driver **782***b*. The other ends of wires **754***a*, **764***a*, **774***a* and **784***a* couple to the inputs of partial multiplexers **758**, **768**, **778** and **788**, respectively, which provide their outputs to the four inputs of a multiplexer **798**. Multiplexer **798** also receives the Mux**6** Sel control and provides the output of one of multiplexers **758**, **768**, **778** and **788** as the delay matching circuit output (DMout).

[**0065**] Logic cells **712***a*, **712***b*, **722***a* and **722***b* may be implemented in the same manner as logic cells **412***a*, **412***b*, **422***a* and **422***b*, respectively, within delay synthesizer **320** in FIG. **4**A. Dynamic cells **732***a* and **732***b* may be implemented in the same manner as dynamic cells **432***a* and **432***b*, respectively. Bit line cells **742***a* and **742***b* may be implemented in the same manner as bit line cells **442***a* and **442***b*, respectively. Drivers **752***a*, **762***a*, **772***a* and **782***a* may be implemented in the same manner as drivers **452***a*, **462***a*, **472***a* and **482***a*, respectively, and wires **754***a*, **764***a*, **774***a* and **784***a* may be implemented in the same manner as wires **454***a*, **464***a*, **474***a* and **484***a*, respectively. Partial multiplexers **718**, **728**, **738**, **748**, **758**, **768**, **778** and **788** model the signal path between one input and the output of multiplexers **418**, **428**, **438**, **448**, **458**, **468**, **478** and **488**, respectively. Multiplexer **798** may be implemented in the same manner as multiplexer **498**.

[**0066**] Delay matching network **330** may be used to absorb the delays of the multiplexers within delay synthesizer **320**. This allows AVS unit **230***x* to accurately model the critical path at high frequency.

[**0067**] FIG. **8** shows an embodiment of control unit **340** within AVS unit **230***x* in FIG. **3**. For this embodiment, the DSout signal from delay synthesizer **320** is provided to a data (D) input of a D flip-flop **814***a* and to the input of a delay cell **812***a*. The output of delay cell **812***a* couples to the data input of a D flip-flop **814***b* and to the input of a delay cell **812***b*. The output of delay cell **812***b* couples to the data input of a D flip-flop **814***c*. The DMout signal from delay matching circuit **330** is provided to the clock inputs of D flip-flops **814***a*, **814***b* and **814***c*. Each D flip-flop **814** latches its data input based on the DMout signal and provides it output (Q) to an encoder **816**. Encoder **816** generates the voltage control Vctrl for power management unit **180** based on the outputs of flip-flop **814***a*, **814***b* and **814***c* and possibly a temperature measurement from temperature sensor **370**.

[**0068**] Each of delay cells **812***a* and **812***b* may be designed to provide a predetermined amount of delay, e.g., 5% of a clock period at the highest clock frequency. Each flip-flop **814** provides a logic high if the pulse on its data input arrives earlier than the pulse on its clock input and provides a logic low otherwise. Flip-flop **814***a* provides a logic high if the pulse on the DSout signal arrives before the pulse on the DMout signal. Flip-flop **814***b* provides a logic high if the delayed pulse from delay cell **812***a* arrives before the pulse on the DMout signal. Flip-flop **814***c* provides a logic high if the delayed pulse from delay cell **812***b* arrives before the pulse on the DMout signal. If the supply voltage is too low, then the total delay of the replicated critical path is long and all three flip-flops may provide logic lows. Encoder **816** then generates the voltage control such that the supply voltage is increased. Conversely, if the supply voltage is too high, then the total delay of the replicated critical path is smaller than the target frequency and all three flip-flops may provide logic highs. Encoder **816** then generates the voltage control such that the supply voltage is decreased.

[**0069**] Control unit **340** generates the voltage control to adjust the supply voltage based on the measured critical path delay. The critical path delay may be measured with three flip-flops as shown in FIG. **8** or more than three flip-flops to achieve greater delay resolution. The voltage control may be a 2-bit control that indicates whether to maintain the current supply voltage or to increase or decrease the supply voltage by a predetermined amount. The voltage control may also be a multi-bit control that indicates the amount of voltage to increase or decrease. Control unit **340** may also disregard the outputs of flip-flops **814***a*, **814***b* and **814***c* and provide predetermined voltage controls if the temperature measurement is outside of a nominal temperature range. Control unit **340** may also use the temperature measurement in other manners to generate the voltage control.

[**0070**] Temperature may vary across an IC die due to different compositions of active and passive devices across the IC die. Temperature gradient across IC die may be accounted for by placing multiple delay synthesizers throughout the IC die. For example, multiple (e.g., four) delay synthesizers may be placed at different comers of a processing core. The AVS unit for that processing core may receive the outputs from all delay synthesizers and may adjust the supply voltage based on the slowest delay synthesizer.

[**0071**] The delays for different circuit components (e.g., logic and wire) are typically dependent on IC process variations. For example, a fast IC process corner results in faster logic and hence less logic delays, whereas a slow IC process comer results in slower logic and hence more logic delays. The parasitic resistance and capacitance of wires may also vary due to IC process variations, which would then result in different wire delays. The delays of logic cells and wires for ASIC **120** may be characterized and used for voltage scaling.

[**0072**] FIG. **9** shows an embodiment of IC process monitor unit **350** within AVS unit **230***x* in FIG. **3**. For this embodiment, a ring oscillator **910** is formed with T delay units **912***a* through **912***t* and a NAND gate **940**, where $T \geqq 1$. Within each delay unit **912**, a demultiplexer (Demux) **920** has its input coupled to the output of either NAND gate **940** or a preceding delay unit and its two outputs coupled to the inputs of buffers **922** and **932**. Buffer **922** drives a wire **924** that further couples to the input of a buffer **926**. Buffer **932** drives a buffer **936**. A multiplexer **938** receives the outputs of buffers **926** and **936** at its two inputs and provides one of the two inputs as the delay unit output. For each delay unit **912**, buffers **922** and **926** and wire **924** form a first signal path composed of logic and wire, and buffers **932** and **936** form a second signal path composed of only logic. Buffers **932** and **936** in the second signal path may be implemented in the same manner as buffers **922** and **926** in the first signal path, so that wire **924** is the only difference between the two

signal paths. Either the first or second signal path may be selected by providing the proper Mux/Demux control to demultiplexer **920** and multiplexer **938**.

[**0073**] NAND gate **940** receives the output of the last delay unit **912***t* on one input and an enable (Enb) signal from a control unit **950** on the other input. The output of NAND gate **940** is provided to the input of the first delay unit **912***a*. Ring oscillator **910** is operational when the enable signal is at logic high and provides an oscillator signal having a frequency that is determined by (1) the selected signal path within delay units **912***a* through **912***t* and (2) the characteristics of the circuit components in the selected signal path, which are dependent on IC process. A counter **960** receives the oscillator signal and counts the number of oscillator cycles based on a first control from control unit **950**. A register **970** latches the output of counter **960** based on a second control from control unit **950** and provides a frequency count. Control unit **950** receives the clock and generates the controls for delay units **912***a* through **912***t*, NAND gate **940**, counter **960** and register **970**. Control unit **950** also receives the frequency count from register **970** and provides a logic speed output and a wire speed output for AVS characterization unit **360**.

[**0074**] The logic speed and the wire speed may be determined as follows. Ring oscillator **910** is first configured to operate with the second signal path in all delay units **912***a* through **912***t* by setting the Mux/Demux control to logic high. Counter **960** then samples the frequency of ring oscillator **910** by counting the number of oscillator cycles in a first time window. Register **970** latches the counter output at the end of the first time window and provides a first frequency count that is indicative of the logic speed. Ring oscillator **910** is next configured to operate with the first signal path in all delay units **912***a* through **912***t* by setting the Mux/Demux control to logic low. Counter **960** then samples the frequency of ring oscillator **910** in a second time window of the same duration as the first time window. Register **970** latches the counter output at the end of the second time window and provides a second frequency count that is indicative of the logic and wire speed. The difference between the first and second frequency counts is indicative of the wire speed.

[**0075**] The logic speed and the wire speed provided by control unit **940** are dependent on IC process. In an embodiment, IC process monitor unit **350** is operated once (e.g., during calibration of wireless device **100**) to obtain the logic speed and the wire speed at a predetermined supply voltage. In other embodiments, IC process monitor unit **350** may be operated as needed and possibly for different supply voltages and/or temperatures to obtain the logic speed and the wire speed for different operating conditions. The logic speed and the wire speed are used to form the replicated critical path, as described below.

[**0076**] FIG. **10**A shows an embodiment of AVS characterization unit **360** within AVS unit **230***x* in FIG. **3**. For this embodiment, a look-up table (LUT) **1010** stores a set of nominal logic speed values for different logic characterizations, and a look-up table **1020** stores a set of nominal wire speed values for different wire characterizations. In general, the nominal logic speed and the nominal wire speed may be stored for any number of logic and wire characterizations, respectively, which are typically dependent on IC process variations (e.g., fast, nominal, slow, and so on). The values stored in look-up tables **1010** and **1020** may be determined by computer simulation, empirical measurements, and so on. By characterizing logic speed and wire speed separately, only two look-up tables **1010** and **1020** may be used to store nominal logic speed and nominal wire speed for different characterizations.

[**0077**] A compare unit **1012** receives the measured logic speed from IC process monitor unit **350** and compares the measured logic speed against the values stored in look-up table **1010** to determine the logic characterization for processing core **130***x*. Similarly, a compare unit **1022** receives the measured wire speed from IC process monitor unit **350** and compares the measured wire speed against the values stored in look-up table **1020** to determine the wire characterization for processing core **130***x*. For example, look-up table **1010** may store x and y values for three logic characterizations of fast, nominal, and slow, where x>y. Compare unit **1012** may compare the measured logic speed s against the stored values and may indicate a fast process if s≧x, a nominal process if x>s ≧y, and a slow process if s<y .

[**0078**] A memory **1030** stores a matrix of Mux control look-up tables **1040***aa* through **1040***yx*. Each row of the matrix is for a different logic characterization stored in look-up table **1010**. Each column of the matrix is for a different wire characterization stored in look-up table **1020**. Each Mux control look-up table **1040** stores the values for the Mux Sel controls for multiplexers **418**, **428**, **438**, **448**, **458**, **468**, **478**, **488** and **498** within delay synthesizer **320** in FIGS. **4**A and **4**B. These Mux Sel controls define a replicated critical path that should closely resemble the actual critical path for the characterizations applicable to processing core **130***x*. The values stored in each Mux control look-up table **1040** may be determined by computer simulation, empirical measurements, and so on. The Mux control look-up table at the row indicated by compare unit **1012** and the column indicated by compare unit **1022** is selected for use.

[**0079**] FIG. **10**B shows an embodiment of one Mux control look-up table **1040***ij* within memory **1030**. Look-up table **1040***ij* stores V sets of Mux Sel control values for multiplexer **418**, **428**, **438**, **448**, **458**, **468**, **478**, **488** and **498** within delay synthesizer **320** for V different clock frequencies. The set of Mux Sel control values corresponding to the target frequency for processing core **130***x* is retrieved from look-up table **1040***ij* and provided to the multiplexers within delay synthesizer **320**.

[**0080**] FIG. **11** shows plots of the performance of two exemplary signal paths within a processing core. The delay of each signal path is plotted versus supply voltage. For the example shown in FIG. **11**, signal path **1** has longer delay and is the critical path below Vx volts, and signal path **2** has longer delay and is the critical path above Vx volts. As shown in FIG. **11**, different signal paths can become the critical path in different conditions. This is because each signal path may be composed of a different blend of circuit components that may vary in different manners across voltage, temperature, and IC process variations. The delay of the critical path determines the highest clock frequency for that path and is thus inversely related to frequency. For a given target frequency, the critical path for that frequency may be replicated, and AVS unit **230** adjusts the supply

voltage such that the desired performance can be achieved for the target frequency. For example, if the target frequency is Freq **2**, then signal path **2** may be selected, and the AVS unit adjusts the supply voltage to Vz volts.

[**0081**] FIG. **12** shows an embodiment of a process **1200** for performing adaptive voltage scaling for a processing core. The logic speed and the wire speed for the processing core are characterized (block **1210**). This characterization may be performed once, e.g., during calibration of a wireless device and as described above for FIG. **9**. The target clock frequency for the processing core is determined (block **1212**). The target clock frequency may be dynamically varied based on, e.g., the computational requirements for the processing core. A replicated critical path is formed based on the characterized logic speed and wire speed and the target clock frequency, e.g., as described above for FIGS. **10**A and **10**B (block **1214**). The replicated critical path may include different types of circuit components such as HVT logic, LVT logic, dynamic cells, bit line cells, wires, drivers with different threshold voltages and/or fan-outs, and so on. The supply voltage for the processing core and the replicated critical path is then adjusted such that both achieve the desired performance (block **1216**). Process **1200** may then return to block **1212** to periodically determine the target clock frequency.

[**0082**] The replicated critical path described herein uses a blend of circuit components to emulate the actual critical path. This replicated critical path is generally more accurate than a conventional replicated critical path that is implemented with a ring oscillator or a delay line composed of all logic or mostly logic gates. Furthermore, the replicated critical path described herein may be easily varied by programming the multiplexers to flexibly model different critical paths for different conditions.

[**0083**] The adaptive voltage scaling techniques described herein have the following desirable characteristics:

[**0084**] Seamless programming of the delay lines to track changing critical path (FIGS. **4**A and **4**B).

[**0085**] On-chip logic and wire binning using IC process monitor unit **350** to enable high efficiency tracking (FIG. **9**).

[**0086**] Temperature gradient tracking by placing multiple AVS units in different spots.

[**0087**] Multi-threshold logic delay lines (FIG. **4**A).

[**0088**] Multi-threshold, multiple fan-out drivers for the wire delay lines (FIG. **4**B).

[**0089**] Diffusion dominated path tracking using dynamic cells (FIGS. **4**A and **5**B).

[**0090**] Memory access delay tracking using bit line cells (FIGS. **4**A and **5**C).

[**0091**] Considering multiplexer delays as a portion of the total logic delay and extending other types of delay (e.g., for wire and diffusion) to accommodate for the multiplexer delays.

[**0092**] Delay matching circuit for absorbing the multiplexer delays to enable high-speed operation.

[**0093**] The adaptive voltage scaling techniques described herein may be implemented by various means. For example, these techniques may be implemented in hardware, firmware, software, or a combination thereof. For a hardware implementation, the adaptive voltage scaling may be implemented within an ASIC, a DSP, a processor, a controller, a micro-controller, a microprocessor, an electronic device, other electronic unit designed to perform the functions described herein, or a combination thereof.

[**0094**] Certain portions of the adaptive voltage scaling may be implemented with software modules (e.g., procedures, functions, and so on) that perform the functions described herein. The software codes may be stored in a memory (e.g., memory **150**, **190** or **192** in FIG. **1**) and executed by a processor (e.g., processor core **130***c* or **130***d*). The memory may be implemented within the processor or external to the processor.

[**0095**] The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

1. An integrated circuit comprising:

a delay synthesizer configured to emulate a signal path in a processing core and comprising transistor devices with at least two threshold voltages; and

a control unit coupled to the delay synthesizer and configured to provide a control based on an output of the delay synthesizer.

2. The integrated circuit of claim 1, wherein the control unit is configured to provide the control to adjust a supply voltage for the processing core.

3. The integrated circuit of claim 1, wherein the delay synthesizer comprises a selectable number of transistor devices for each of the at least two threshold voltages.

4. The integrated circuit of claim 1, wherein the least two threshold voltages include high threshold voltage (HVT) and low threshold voltage (LVT).

5. The integrated circuit of claim 4, wherein the delay synthesizer comprises a selectable number of HVT transistor devices and a selectable number of LVT transistor devices.

6. The integrated circuit of claim 1, wherein the delay synthesizer comprises logic cells formed by the transistor devices with the at least two threshold voltages.

7. The integrated circuit of claim 1, wherein the delay synthesizer comprises drivers formed by the transistor devices with the at least two threshold voltages.

8. An integrated circuit comprising:

a delay synthesizer configured to emulate a signal path in a processing core and comprising at least one logic cell, at least one wire, and at least one driver selected from among at least two drivers with different electrical characteristics; and

a control unit coupled to the delay synthesizer and configured to provide a control based on an output of the delay synthesizer.

9. The integrated circuit of claim 8, wherein the at least two drivers have different threshold voltages.

10. The integrated circuit of claim 8, wherein the at least two drivers have different fan-outs.

11. The integrated circuit of claim 8, wherein the delay synthesizer comprises a selectable number of logic cells and a selectable number of wires.

12. The integrated circuit of claim 8, wherein the at least one logic cell is selected from among at least two logic cells with different threshold voltages.

13. The integrated circuit of claim 8, wherein the control unit is configured to provide the control to adjust a supply voltage for the processing core.

14. An integrated circuit comprising:

a delay synthesizer configured to emulate a signal path in a processing core and comprising at least one dynamic cell used to model diffusion capacitance in the processing core; and

a control unit coupled to the delay synthesizer and configured to provide a control based on an output of the delay synthesizer.

15. The integrated circuit of claim 14, wherein the delay synthesizer comprises a selectable number of dynamic cells.

16. The integrated circuit of claim 14, wherein each dynamic cell comprises at least one transistor modeling the diffusion capacitance and first and second transistors configured to charge and discharge the at least one transistor.

17. An integrated circuit comprising:

a delay synthesizer configured to emulate a signal path in a processing core and comprising at least one bit line cell used to model memory access delays; and

a control unit coupled to the delay synthesizer and configured to provide a control based on an output of the delay synthesizer.

18. The integrated circuit of claim 17, wherein the delay synthesizer comprises a selectable number of bit line cells.

19. The integrated circuit of claim 17, wherein each bit line cell comprises at least one memory cell and a sense amplifier coupled to the at least one memory cell.

20. An integrated circuit comprising:

a delay synthesizer configured to emulate a signal path in a processing core and comprising at least one multiplexer for programming the delay synthesizer;

a delay matching circuit configured to estimate delays of the at least one multiplexer in the delay synthesizer; and

a control unit coupled to the delay synthesizer and the delay matching circuit and configured to provide a control based on outputs of the delay synthesizer and the delay matching circuit.

21. The integrated circuit of claim 20, wherein the control unit is configured to provide the control to adjust a supply voltage for the processing core.

22. The integrated circuit of claim 20, wherein the delay synthesizer comprises at least one delay line, wherein each delay line comprises at least one cell and is coupled to a multiplexer operative to select a configurable number of cells in the delay line.

23. The integrated circuit of claim 22, wherein the multiplexer for each delay line is operative to select at least one cell in the delay line.

24. The integrated circuit of claim 20, wherein the delay matching circuit comprises at least one partial multiplexer for the at least one multiplexer in the delay synthesizer, and wherein each partial multiplexer comprises a signal path between one input and an output for an associated multiplexer.

25. An integrated circuit comprising:

at least two delay synthesizers placed in different locations relative to a processing core, wherein each delay synthesizer is configured to emulate a critical signal path in the processing core; and

a control unit coupled to the at least two delay synthesizers and configured to receive outputs of the at least two delay synthesizers and to provide a control to adjust a supply voltage for the processing core.

26. The integrated circuit of claim 25, wherein the at least two delay synthesizers are placed at different corners of the processing core.

27. An integrated circuit comprising:

an oscillator configured to generate an oscillator signal based on logic or both logic and wire; and

a control unit configured to provide first and second outputs based on the oscillator signal, wherein the first output is indicative of logic speed and the second output is indicative of wire speed or both logic and wire speed.

28. The integrated circuit of claim 27, wherein the oscillator comprises at least one delay unit, each delay unit comprising a first signal path comprised of logic and a second signal comprised of both logic and wire.

29. The integrated circuit of claim 27, wherein the control unit is configured to obtain a first frequency count for logic, to obtain a second frequency count for both logic and wire, and to generate the first and second outputs based on the first and second frequency counts.

30. An apparatus comprising:

a characterization unit configured to ascertain a critical signal path in a processing core; and

a delay synthesizer coupled to the characterization unit and configured to emulate the critical signal path ascertained by the characterization unit, the delay synthesizer comprising logic with different threshold voltages, wires, drivers with different fan-outs, or a combination thereof.

31. The apparatus of claim 30, further comprising:

a monitor unit configured to determine logic speed and wire speed for the processing core.

32. The apparatus of claim 30, wherein the characterization unit is configured to receive a target clock frequency for the processing core and to ascertain the critical signal path based on the target clock frequency.

33. The apparatus of claim 32, wherein the target clock frequency is dynamically selected based on performance requirements for the processing core.

34. The apparatus of claim 30, wherein the characterization unit is configured to receive logic speed and wire speed for the processing core and to ascertain the critical signal path based on the logic speed and wire speed.

35. The apparatus of claim 34, wherein the characterization unit comprises a plurality of look-up tables for a

plurality of combinations of logic speed and wire speed, wherein each look-up table indicates the critical signal path for a different combination of logic speed and wire speed.

36. The apparatus of claim 35, wherein each look-up table includes a plurality of signal paths for a plurality of clock frequencies, and wherein the characterization unit is configured to provide a signal path for a target clock frequency in a look-up table call associated with the logic speed and the wire speed received by the characterization unit as the critical signal path.

37. The apparatus of claim 30, further comprising:

a control unit coupled to the delay synthesizer and configured to receive an output from the delay synthesizer and to provide a control to adjust a supply voltage for the processing core.

38. A method comprising:

replicating a critical signal path for a processing core using logic with different threshold voltages, wires, drivers with different fan-outs, or a combination thereof; and

adjusting a supply voltage for the processing core based on delays of the replicated critical signal path.

39. The method of claim 38, further comprising:

determining a target clock frequency for the processing core, and wherein the replicated critical signal path is formed based on the target clock frequency.

40. The method of claim 38, further comprising:

characterizing logic speed and wire speed of the processing core, and wherein the replicated critical signal path is formed based on the logic speed and the wire speed.

41. The method of claim 38, further comprising:

estimating delays of multiplexers within the replicated critical path, and wherein the supply voltage is adjusted further based on the estimated delays of the multiplexers.

42. An apparatus comprising:

means for replicating a critical signal path for a processing core using logic with different threshold voltages, wires, drivers with different fan-outs, or a combination thereof; and

means for adjusting a supply voltage for the processing core based on delay of the replicated critical signal path.

43. The apparatus of claim 42, further comprising:

means for determining a target clock frequency for the processing core, and wherein the replicated critical signal path is formed based on the target clock frequency.

44. The apparatus of claim 42, further comprising:

means for characterizing logic speed and wire speed of the processing core, and wherein the replicated critical signal path is formed based on the logic speed and the wire speed.

45. The apparatus of claim 42, further comprising:

means for estimating delays of multiplexers within the replicated critical path, and wherein the supply voltage is adjusted further based on the estimated delays of the multiplexers.

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