Low Latency Clock Domain Transfer for Simultaneously Mesochronous, Plesiochronous and Heterochronous Interfaces

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Wade L. Williams ; Philip E. Madrid ; Scott C. Johnson **All Authors**

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Abstract:
Microprocessors are employing higher levels of system integration for both higher performance and lower system cost. In doing so, problems that used to be apparent inter-device are now found intra- processor. The integration of the processor core with other units such as the north bridge often increase the number of clock domains within the device. In addition, the frequency of the external interfaces has increased at a much higher rate than the processor frequency. This trend will continue with the advent of multi-core processors which have increasing bandwidth demands. However, as the characteristics of the clock domains become more complex, the problem compounds the burden on the clock domain transfer mechanism to achieve low latency. Presented here is an easily implementable, low latency solution for clock domain transfer in the presence of high frequency mesochronous, plesiochronous, and heterochronous clock signaling.

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