A Power Management Unit with Continuous Co-Locking of Clock Frequency and Supply Voltage for Dynamic Voltage and Frequency Scaling

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Abstract— A power management unit (PMU) architecture is proposed for the domain-specific low power management with dynamic voltage and frequency scaling. The PMU continuously co-locks and dynamically varies the supply voltage and the clock frequency from 89 MHz to 200 MHz and from 1.0 V to 1.8 V , respectively, in less than 40µs. A 32bit RISC processor is used as power management target device. The PMU, 0.36mm^2 with 0.18-µm CMOS process, consumes 5mW, and shows -100dBm/Hz phase noise of clock and 160mV load regulation of supply voltage with 100mA load current from the load, RISC processor.

I. INTRODUCTION

Steady increase of the integration level and functional complexity of the modern handheld devices require low power operation of their ICs. The previous researches achieved the power management by lowering supply voltage to save power consumption of system [1-5], Recently, the Dynamic Voltage and Frequency Scaling (DVFS) system is widely used for power saving.

The previous PMU for DVFS generated the clock frequency and the supply voltage at the same time, and it controlled clock and supply voltage with digital feedback control [2] for the stability of tracking loop. It used the DC-DC converter in the feedback control loop to generate stable supply voltage with dynamically varying values. However, its discrete control decreased power management efficiency, and total feedback control loop could not be integrated on a single chip because the switching regulator in [2] required large value of the inductor and the capacitor. Moreover, its loop could be attacked by the digital noise, due to the direct connection of feedback loop with the load.

In this paper, a PMU architecture with a phase locked loop (PLL) is proposed to solve these problems. Its PLL achieves continuous control of the clock frequency and the supply voltage. The proposed PMU separates the load block from the feedback loop, and prevents the attack of the digital noise from the load to the feedback loop. It is implemented in a single chip by 0.18-µm CMOS technology and tested for power management of a 32bit RISC processor.

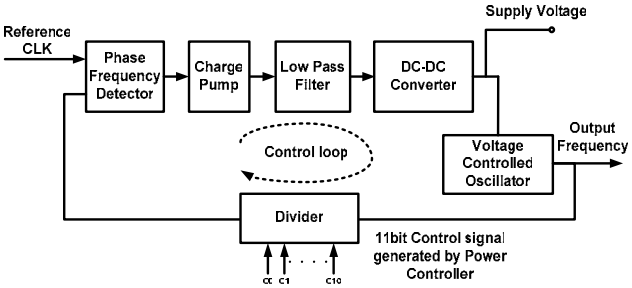

Figure 1. Block diagram of conceptual control loop

The details of the proposed PMU will be explained in the following sections. In section II, the proposed PMU architecture will be introduced. Section III presents detail description of each component of the PMU and section IV shows the measurement results. Finally, Section V concludes the paper.

II. OVERALL ARCHITECTURE

In DVFS system, there are two standard approaches for finding minimum energy point (MEP). The one uses the tracking table, the other uses the load modeling VCO. The former approach is better than the latter in the respect of stability [6]. However, the latter can more efficiently manage the power of the load due to continuous tracking of a minimum energy point [2]. In this paper, the PMU adopts the load modeling VCO for efficient power management.

Fig. 1 shows the conceptual architecture of the PMU. It is composed of phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), linear regulator (LR) and voltage controlled oscillator (VCO) modeling the critical path of the load. The PFD detects phase error between 1MHz reference and feedback clock, and generates UP, DOWN control signals. The CP controls reference voltage using these signals.

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Apple Exhibit 1031
Apple Inc. v. Redstone Logics LLC
IPR2025-01532, Page 1 of 4

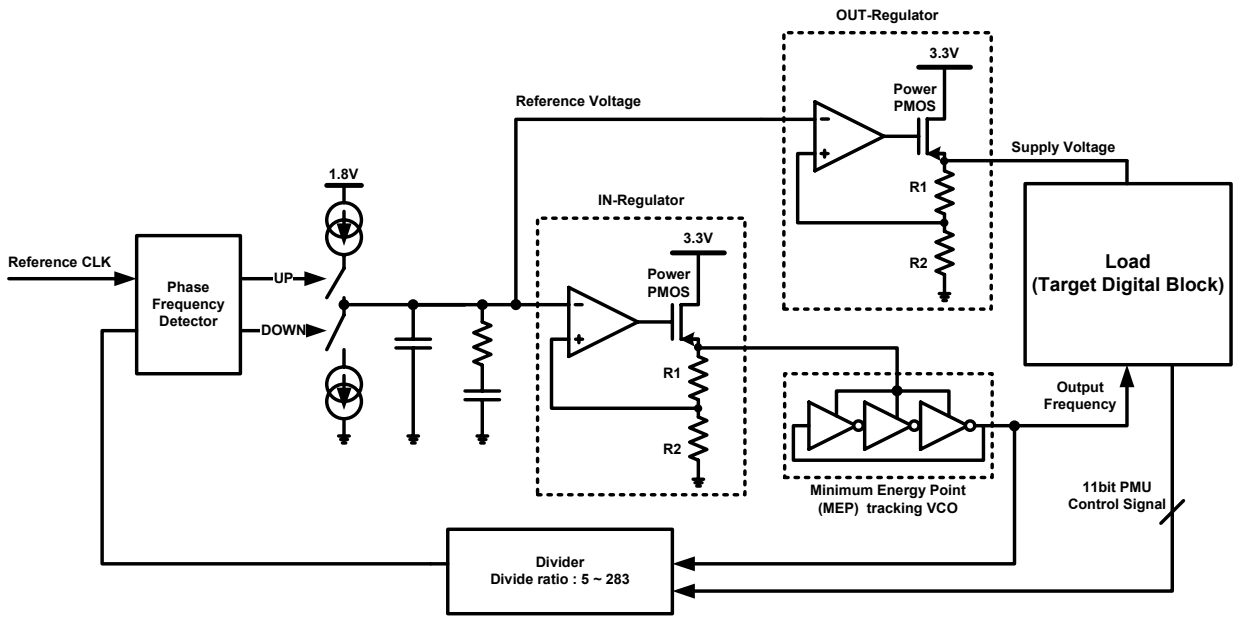

Figure 2. Total block diagram of power management unit for dynamic voltage and frequency scaling

The LPF generates the reference voltage for the LR, and it is converted to the supply voltage by the dc-dc converter. The dc-dc converter using switch regulator is composed of L and C. However, the proposed PMU of Fig. 2 uses the LR not only to remove L but also to reduce C. Moreover, for achieving an area-efficient LR [7-9], the size of the decoupling capacitor is reduced by the sensitively low impedance node (SLIN) scheme proposed in this paper.

The VCO is tracking the load condition, and finds the MEP for the load. The pulse swallow frequency divider can divide the output clock from 5 to 283 with a step of 1. The divided output clock is fed back to PFD to form a control loop. The 11bit control signals indicating the performance requirement of the load are given to the swallow divider.

The supply voltage and the VCO control voltage are supported by the same reference voltage which is continuously determined by frequency feedback loop in Fig. 2. Thus, the supply voltage and VCO output clock frequency are dynamically locked at the same time.

The PMU covers the clock frequency and supply voltage range of 89MHz to 200MHz, and 1.0V to 1.8V, respectively.

III. SPECIFIC DESIGN OF PMU COMPONENTS

A. Linear Regulator (LR)

In Fig. 1, because of the direct connection of the load with the control loop, the digital noise from load may affect the control loop. However, in the proposed PMU of Fig. 2 the regulator is placed outside of the loop control and the load is separated from the control loop for the digital noise not to affect the control loop, so that it can produce more stable target supply voltage and clock frequency than that the previous PMU does. Two LRs have different PMOSs as source follower output drivers. Because of low output impedance of the source follower, this topology can regulate load voltage quickly.

The IN, OUT-regulators convert 0.71 V reference voltage to 1.0 V output voltage and 1.28 V reference voltage to 1.8 V output voltage by using R2 / (R1+R2) ratio.

B. Operational Amplifier

Fig. 3 shows operational amplifier topology with cascade feedback compensation [10]. This topology needs only 100fF small compensation capacitor Cc to reduce the total size of op-amp. Thus, the total size of the op-amp is reduced and it has 50dB open-loop gain, 75° phase margin, and 270MHz unity gain frequency. This Op-Amp forms the LR with source follower power PMOS together.

C. Sensitively Low Impedance Node (SLIN)

In the SLIN of Fig. 4, variation of load current is monitored to enable its operation. Due to load current increase, abrupt voltage drop at the node X in Fig. 4(b) is resulted and the power PMOS turns on. It supplies the current quickly from 3.3 V voltage source to stabilize the load supply voltage.

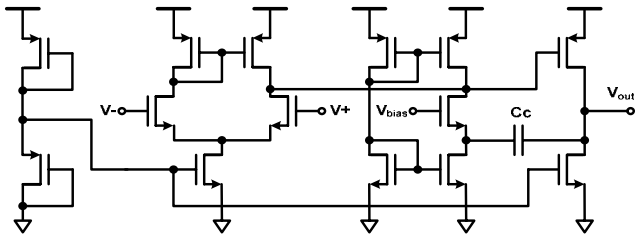

Figure 3. Operational amplifier with cascade feedback compensation

Apple Exhibit 1031
Apple Inc. v. Redstone Logics LLC
IPR2025-01532, Page 2 of 4

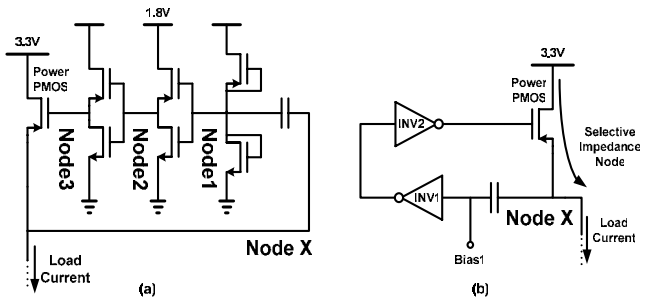

Figure 4. Sensitively Low Impedance Node (SLIN)

The voltage at the node X can be varied from 1.0 V to 1.8 V. It can not be used as a reference voltage to sense the current variation. A new scheme, SLIN, is necessary to sense current variation. In Fig. 4(a), the node 1 is biased at slightly bigger than 0.9V. Voltage drop at the node X pulls down the node 1 voltage under 0.9V. And then, the node 2 goes to 'HIGH', and the node 3 drops to 'LOW' to turn on the power PMOS quickly. The SLIN has 0.5nsec response time for the regulation of variable dc voltage level. With this scheme, the LR can be area-efficient with 1.2nF capacitance.

D. *Minimum Energy Point (MEP) tracking VCO*

To achieve the dynamic voltage and frequency scaling, the VCO should simulate appropriate clock frequency and supply voltage for the load. The critical path delay is determined by RC interconnection, gate and diffusion capacitance. The interconnection and diffusion capacitance maximize the delay at lowest supply voltage, and in contrary, the gate dominant circuit maximizes the delay at highest supply voltage [2]. The maximum variation of the delay exists at two extreme points. Therefore, modeling of two extreme voltage points is enough for the load delay simulation.

IV. Measurement Results

The PMU is fabricated by using 0.18-µm CMOS process, and takes 0.36mm^2 area, excluding pad. It is packaged as the chip on board (COB), and assembled with a RISC processor as its load on a PCB. The 32bit ARM compatible

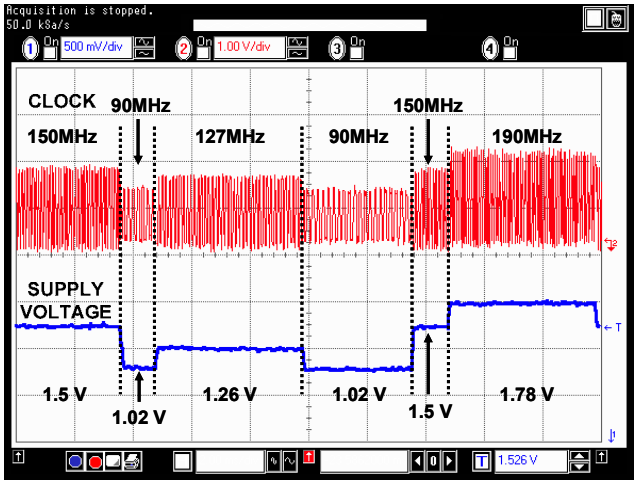

Figure 5. Dynamic voltage and frequency scaling

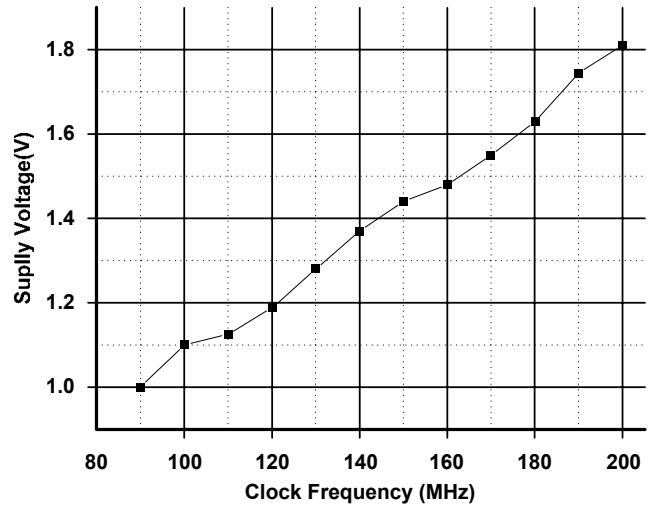

Figure 6. Clock frequency versus supply voltage

RISC processor has 200 MHz clock speed with 1.8 V supply voltage. It runs 3D graphics application which has variable performance requirement, and its clock frequency and supply voltage are dynamically controlled according to its runtime work load information.

A. *Continuous Co-locking of Frequency and Voltage*

The measured waveforms of the PMU are shown in Fig. 5. The output supply voltage of the OUT-regulator is changed to the same voltage level of the IN-regulator at the same time, and the clock peak to peak voltage and target supply voltage are varied equally as shown in Fig. 5. The transition time of supply voltage from 1.0V to 1.8V and clock frequency from 89 MHz to 200 MHz is 37.2µsec with 21.5mV/µsec slew rate. Fig. 6 shows frequency versus supply voltage characteristics of the PMU with the RISC processor. The RISC processor, which is used as the PMU testing load, has critical path of 5nsec with 1.8 V and 12.5nsec at 1.0 V. The supply voltage increases linearly from 1.0 V to 1.8 V with clock frequency form 89 MHz to 200 MHz.

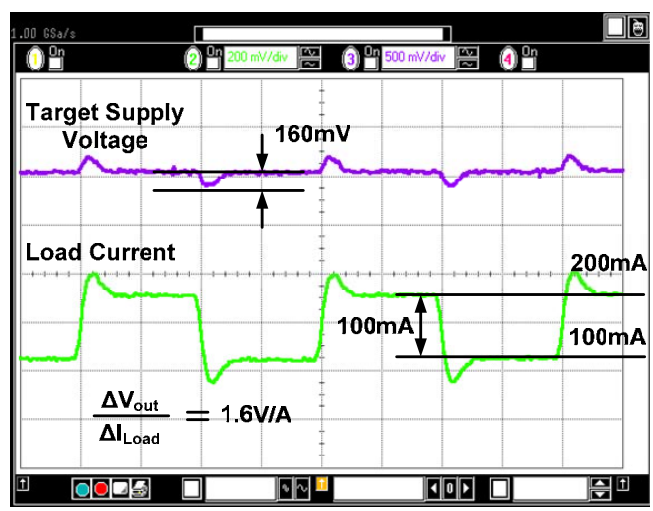

Figure 7. Load regulation of out-regulator

Apple Exhibit 1031
Apple Inc. v. Redstone Logics LLC
IPR2025-01532, Page 3 of 4

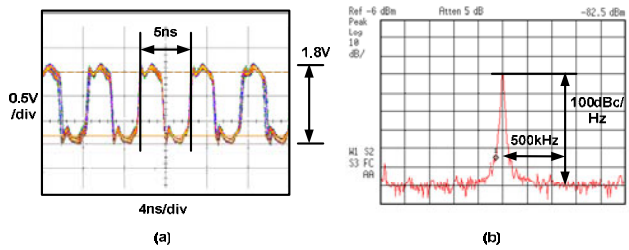

Figure 8. (a) 200MHz clock in time domain (b) in frequency domain

TABLE 1. Comparison results

Measurement factors	Previous work [2]	This work
Capacitance [μF]	4.7	1.2
Inductance [uH]	5.5	no
Integrated on-die	no	yes
Load regulation [mV]	60 (Δ_L = 20mA)	160 (ΔI_L = 100mA)
Full range transition time [μsec]	70	37.2
Area [mm^2]	0.6	0.36

B. *Stable Clock and Supply Voltage Generation*

Fig. 7 shows measurement results of the OUT-regulator with 3.5Ω load resistors. In this case, 350mV peak to peak voltage difference is equivalent to 100mA load current. Its measured load regulation is 160mV. The 200 MHz clock is shown in Fig. 8 (a), and 1.8 V swing is observed. Fig. 8 (b) shows clock characteristics in frequency domain. The peak frequency is 200 MHz, and has magnitude of 60dBm with -100dBc/Hz phase noise at 500 kHz offset.

C. *Results Comparison*

The chip microphotograph is shown in Fig. 9. Its core size is 0.36mm^2. The PMU characteristics are summarized in Table 1. For the comparison, the area of the previous work is normalized to 0.18-μm CMOS technology. The area of this study is only 43% of the switching regulator type PMU. Table 1 shows performance improvement of load regulation and full range transition time of which values are reduced to 50% of the results achieved by previous work.

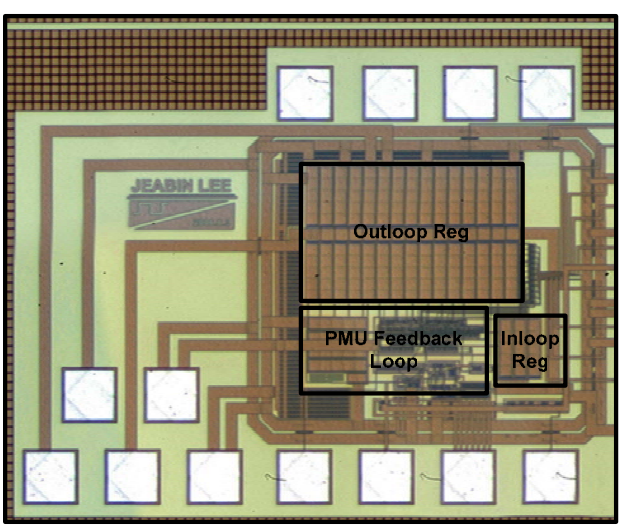

Figure 9. Chip photo of PMU

TABLE 2. PMU Overall characteristics

Measurement factors	Value
Voltage Range[V]	1.0 – 1.8
Frequency Range[MHz]	89 - 200
Varying Time[us]	37.2
Load Regulation[mV]	160 (I_L = 100mA)
Phase Noise[dBc/Hz]	- 100 (@ 500kHz offset f)
Power Consumption[mW]	5
AREA[mm^2]	0.36

V. CONCLUSION

We propose a single chip power management unit for dynamic voltage and frequency scaling, and fabricate a test chip using a 0.18-μm CMOS technology. Its LR removes the inductor, and its SLIN scheme reduces the size of decoupling capacitor by 3/4. It generates continuous co-locking the clock frequency and the supply voltage, and improves load regulation of the supply voltage by 50%. The supply voltage and clock frequency can be dynamically changed from 1.0V to 1.8V and from 89MHz to 200MHz within 40μsec. The supply voltage has 160mV load regulation with the load current variation of 100mA, and clock has -100dBc/Hz phase noise at 500 kHz offset frequency. This PMU has power consumption of 5mW and takes 0.36mm^2. With this clock and supply voltage, the PMU successfully manages power consumption of a test RISC processor.

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Apple Exhibit 1031
Apple Inc. v. Redstone Logics LLC
IPR2025-01532, Page 4 of 4