

U.S. Patent No. 8,549,339 (“’339 Patent”)

Accused Products

Apple’s products comprising two or more sets of processors supporting or based on the Firestorm and Icestorm architectures, and similar efficiency core, performance core architectures, including without limitation the Apple M Series System of Chip (Apple M1 series, Apple M2 series, Apple M3 series, Apple M4 series), and the Apple A Series System on Chip beginning with Apple A10(Apple A10 series, Apple A11 series, Apple A12 series, Apple A13 series, Apple A14 series, Apple A15 series, Apple A16 series, Apple A17 series, and Apple A18 series), and all variants and iterations thereof (collectively, “Accused Products”), infringe at least Claims 1, 5, 8, 9, 10, 14, and 21 of the ’339 Patent.

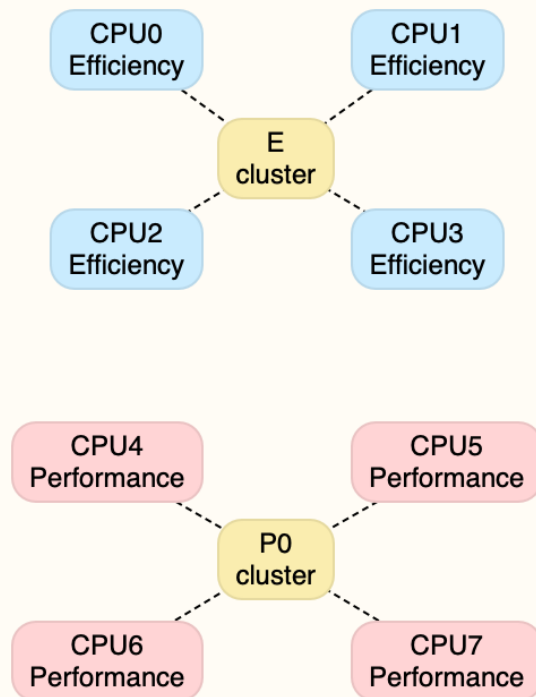
Each Accused Product infringes the claims in substantially the same way, and the evidence shown in this chart is similarly applicable to each Accused Product. For example, each Accused Product includes a Firestorm and Icestorm architectures or similar efficiency core, performance core architectures and, on information and belief, implements substantially the same architectural features described in the reference documentation cited in this chart. Thus, the descriptions and evidence below relating to the Apple M1 Series System on Chip representative products are similarly applicable to the remaining Accused Products listed above. Each claim limitation is literally infringed by each Accused Product. However, to the extent any claim limitation is not met literally, it is nonetheless met under the doctrine of equivalents because the differences between the claim limitation and each Accused Product would be insubstantial, and each Accused Product performs substantially the same function, in substantially the same way, to achieve the same result as the claimed invention. Notably, Defendant has not yet articulated which, if any, particular claim limitations it believes are not met by the Accused Products.

Claim 1

Claim 1	Accused Products
1. A multi-core processor, comprising:	To the extent the preamble is limiting, each Accused Product comprises a multi-core processor. For example, the base model Apple M1 Series System on Chip contains eight cores implementing the Firestorm and Icestorm architecture. On information and belief other Accused Products provide a similar architecture with differing numbers of cores, for example the Max and Pro model Apple M Series System on Chip contain a greater number of cores implementing the Firestorm and Icestorm architecture. <i>See, e.g.:</i>

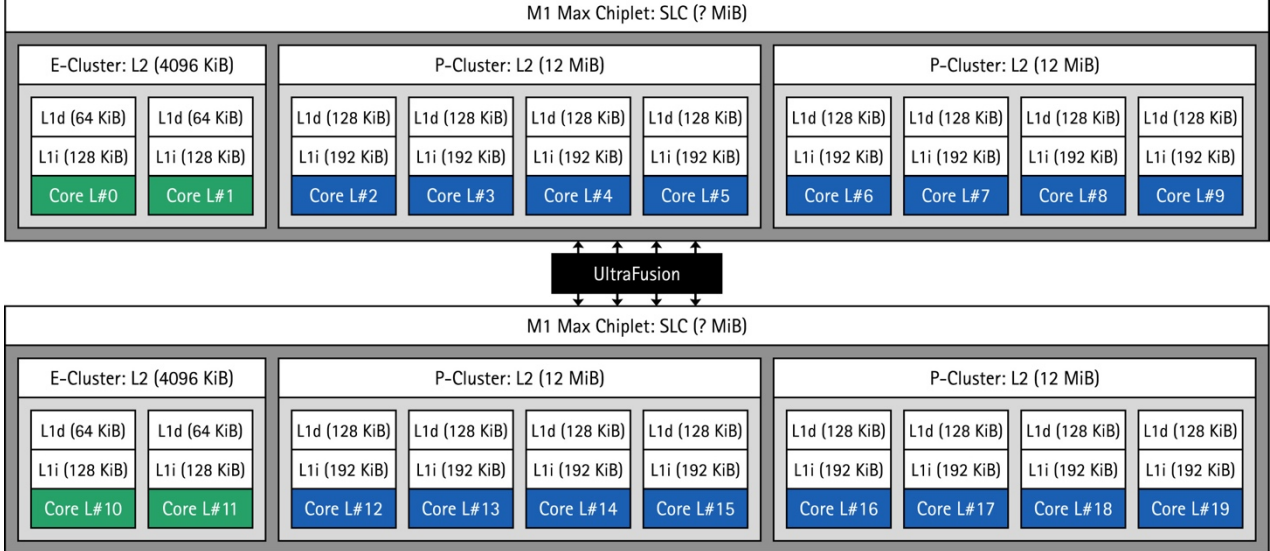
Claim 1	Accused Products
	CPU At its heart, each M1 chip has a total of eight processor cores, all based on Apple's development of technology licensed from Arm. Four are described as Performance cores, dubbed <i>Firestorm</i>, and four are Efficiency cores, or <i>Icestorm</i>. These primarily differ in their compromise between performance and power consumption, with Firestorm cores performing in the same class as better Intel cores, and Icestorm delivering lower performance with much less power requirement and heat production. There are differences in the provision of cache memory, though: • Firestorm has 192+128 KB L1 cache per core, and shares a total of 12 MB L2 cache. • Icestorm has 128+64 KB L1 cache per core, and shares a total of 4 MB L2 cache. https://eclecticlight.co/2021/08/24/whats-in-an-m1-chip-and-what-does-it-do-differently/

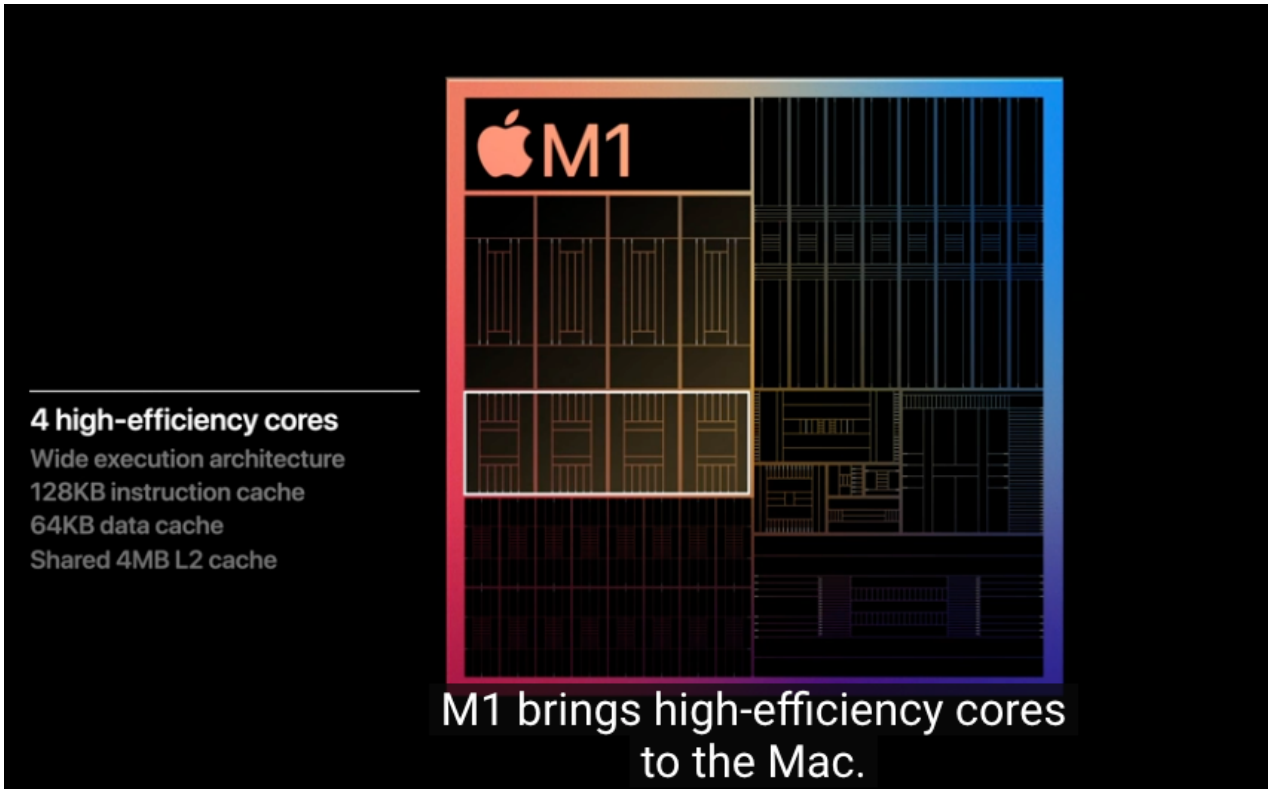
Apple M-series Chips: Base Model (M1-M3)



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<https://eclecticlight.co>

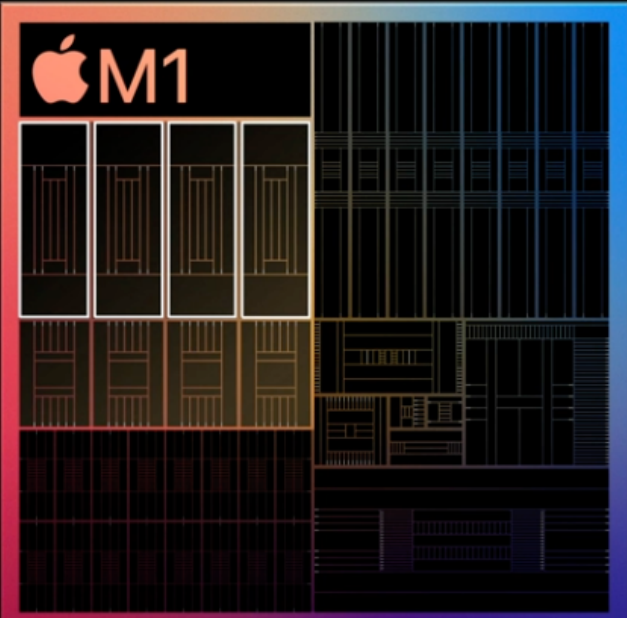
<https://eclecticlight.co/2024/02/19/apple-silicon-1-cores-clusters-and-performance/>

Claim 1	Accused Products
	 https://www.sciencedirect.com/science/article/pii/S1383762124000390?ref=pdf_download&fr=R&R-2&rr=923601bc8d6a6c81#fig2
[1a] a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;	Each Accused Product comprises a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input. For example, the Apple M Series System on Chip contain a set of efficiency cores (e-cores) in an Icestorm architecture wherein each e-core from this set of e-cores is configured to receive a variable frequency depending on the computational load. To handle greater computational load with greater frequency, greater voltage is needed, so on information and belief, the set of e-cores is configures to receive a variable voltage, a first supply voltage. On information and belief the variable frequency is provided by a first PLL having a first clock signal as input. Identification of the precise mechanism used to provide a clock signal is proprietary information of Apple that is the proper subject of fact discovery.

Claim 1	Accused Products
	<i>See, e.g.:</i>  https://www.youtube.com/watch?v=5AwdkGKmZ0I at 9:02

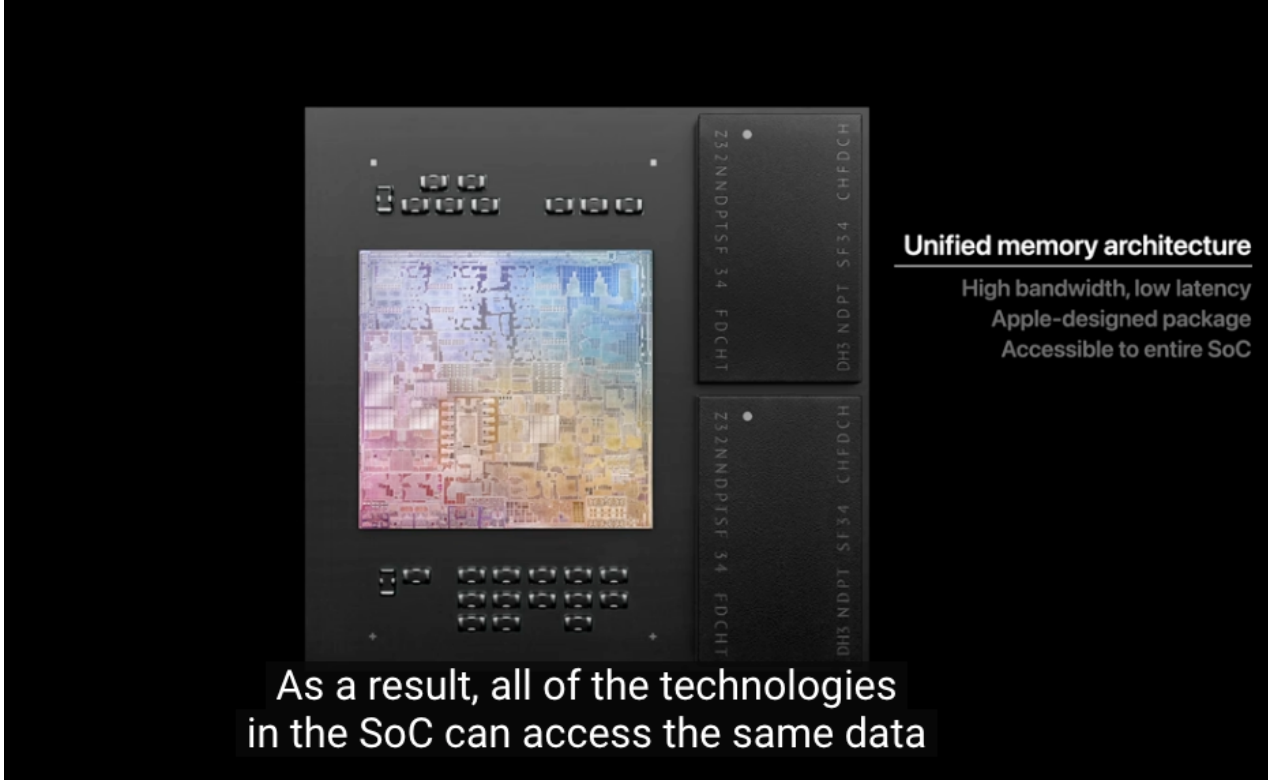
Claim 1	Accused Products
	Variable frequency This is another key feature of Apple silicon cores: unlike most older CPUs, the cores can be run at different frequencies or clock speeds, ranging from 696 MHz up to 4,056 MHz for M3 P cores. Although I don't know whether M3 cores take advantage of this, it's also possible that their voltage is variable. Much of the time, E cores running background threads in an M3 chip do so with the cores at their minimum frequency of only 744 MHz, but when they're used to run threads that have overflowed from P cores their frequency can rise to their maximum of 2,748 MHz. Overflowed threads on E cores thus can't benefit from the same high performance as they would on P cores, but they do run much faster than background threads. Clusters Cores of the same type are grouped into clusters. Within each cluster, all the cores run at the same frequency, and they share local memory in their level 2 (L2) cache. That also makes it easier for threads to be moved around between cores in the same cluster. In M1 and M2 family chips, their E and P cores are arranged in clusters of up to four cores; Apple changed that in the M3, whose clusters can be of as many as 6 cores, all of the same type. In all base version CPUs of M-series chips, there's one cluster of 4 E cores, and one cluster of 4 P cores, so the CPU can be designated as being 4P+4E. Pro, Max and Ultra versions have different numbers of cores, and may have two (or more) clusters of P cores in all. https://eclecticlight.co/2024/02/19/apple-silicon-1-cores-clusters-and-performance/

Claim 1	Accused Products
[1b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and	Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal. For example, the Apple M Series System on Chip contain a set of performance cores (p-cores) in a Firestorm architecture wherein each p-core from this set of p-cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second phase lock loop (PLL) having a second clock signal as input. For example, the Apple M Series System on Chip contain a set of performance cores (p-cores) in a Firestorm architecture wherein each p-core from this set of p-cores is configured to receive a variable frequency depending on the computational load. To handle greater computational load with greater frequency, greater voltage is needed, so on information and belief, the set of p-cores is configures to receive a variable voltage, a second supply voltage. On information and belief the variable frequency is provided by a second PLL having a second clock signal as input. Identification of the precise mechanism used to provide a clock signal is proprietary information of Apple that is the proper subject of fact discovery. Additionally, the first supply voltage provided to the cluster of e-cores is independent from the second supply voltage provided to the cluster of p-cores and the first clock signal is independent form the second clock signal. For example, the e-cores and p-cores operate within different frequency ranges, requiring independent clock signals and supply voltages. <i>See, e.g.:</i>

Claim 1	Accused Products
	4 high-performance cores Ultra-wide execution architecture 192KB instruction cache 128KB data cache Shared 12MB L2 cache  And M1 has four of these incredibly fast, high-performance cores. https://www.youtube.com/watch?v=5AwdkGKmZ0I at 8:53.

Claim 1	Accused Products
	Variable frequency This is another key feature of Apple silicon cores: unlike most older CPUs, the cores can be run at different frequencies or clock speeds, ranging from 696 MHz up to 4,056 MHz for M3 P cores. Although I don't know whether M3 cores take advantage of this, it's also possible that their voltage is variable. Much of the time, E cores running background threads in an M3 chip do so with the cores at their minimum frequency of only 744 MHz, but when they're used to run threads that have overflowed from P cores their frequency can rise to their maximum of 2,748 MHz. Overflowed threads on E cores thus can't benefit from the same high performance as they would on P cores, but they do run much faster than background threads. Clusters Cores of the same type are grouped into clusters. Within each cluster, all the cores run at the same frequency, and they share local memory in their level 2 (L2) cache. That also makes it easier for threads to be moved around between cores in the same cluster. In M1 and M2 family chips, their E and P cores are arranged in clusters of up to four cores; Apple changed that in the M3, whose clusters can be of as many as 6 cores, all of the same type. In all base version CPUs of M-series chips, there's one cluster of 4 E cores, and one cluster of 4 P cores, so the CPU can be designated as being 4P+4E. Pro, Max and Ultra versions have different numbers of cores, and may have two (or more) clusters of P cores in all. https://eclecticlight.co/2024/02/19/apple-silicon-1-cores-clusters-and-performance/

Claim 1	Accused Products
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[1c] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate	Each Accused Product comprises an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

Claim 1	Accused Products
communication between the first set of processor cores and the second set of processor cores.	For example, the Apple M Series System on Chip include Apple's Unified Memory Architecture that is configured to facilitate communications between the e-cores and p-cores. <i>See, e.g.:</i>  https://www.youtube.com/watch?v=5AwdkGKmZ0I at 7:47

Claim 1	Accused Products
	Framework Dispatch Execute code concurrently on multicore hardware by submitting work to dispatch queues managed by the system. iOS 8.0+ iPadOS 8.0+ Mac Catalyst 13.0+ macOS 10.10+ tvOS 9.0+ visionOS 1.0+ watchOS 2.0+ Overview Dispatch, also known as Grand Central Dispatch (GCD), contains language features, runtime libraries, and system enhancements that provide systemic, comprehensive improvements to the support for concurrent code execution on multicore hardware in macOS, iOS, watchOS, and tvOS. The BSD subsystem, Core Foundation, and Cocoa APIs have all been extended to use these enhancements to help both the system and your application to run faster, more efficiently, and with improved responsiveness. Consider how difficult it is for a single application to use multiple cores effectively, let alone to do it on different computers with different numbers of computing cores or in an environment with multiple applications competing for those cores. GCD, operating at the system level, can better accommodate the needs of all running applications, matching them to the available system resources in a balanced fashion. https://developer.apple.com/documentation/Dispatch

Claim 1	Accused Products
	The diagram illustrates a multi-core processor architecture. It features two identical M1 Max Chiplet units, each labeled 'M1 Max Chiplet: SLC (? MiB)'. Each chiplet is divided into three main sections: an E-Cluster (L2 4096 KiB) and two P-Clusters (each L2 12 MiB). The E-Cluster contains two cores, Core L#0 and Core L#1, each with L1d (64 KiB) and L1i (128 KiB) cache. The first P-Cluster contains four cores (Core L#2 to Core L#5), each with L1d (128 KiB) and L1i (192 KiB) cache. The second P-Cluster contains four cores (Core L#6 to Core L#9), each with L1d (128 KiB) and L1i (192 KiB) cache. The two chiplets are connected via an 'UltraFusion' interface, represented by a central black box with four arrows pointing to each of the four P-Clusters. Below the diagram is a URL: https://www.sciencedirect.com/science/article/pii/S1383762124000390?ref=pdf_download&fr=R-R-2&rr=923601bc8d6a6c81#fig2

Claim 5

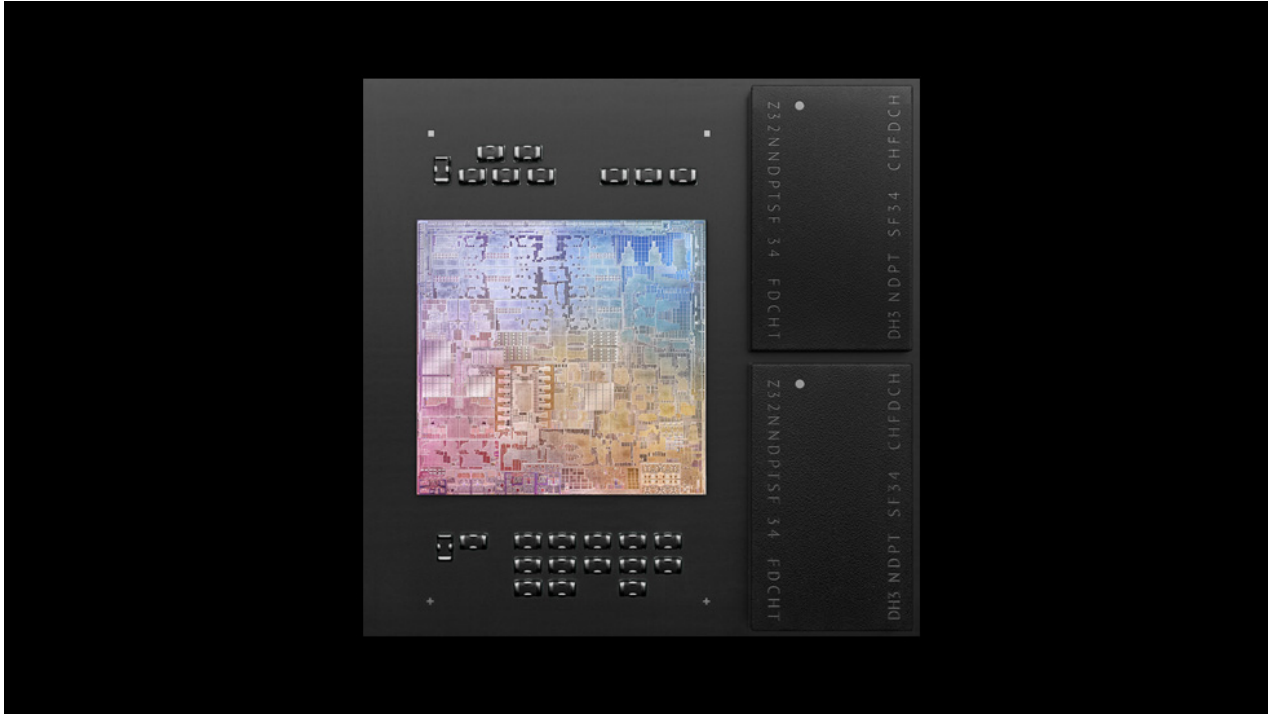
Claim 5	Accused Products
5. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor. For example, the Apple M Series System on Chip control the voltage and frequency provided to the e-cores and p-cores. On information and belief, this is done by a control block, for example a Power Management Processor. Identification of the physical location of the control blocks is proprietary information of Apple is the proper subject of fact discovery. <i>See, e.g.:</i>

Claim 5	Accused Products
	Further coprocessors are thought to include: • Always On Processor (AOP), which handles environmental sensors and activation of the system; • Apple Video Decoder (AVD), which decodes video; • Apple Video Encoder (AVE), which encodes video; • Power Management Processor (PMP), the successor to power management features in the SMC. • Apple Graphics (AGX), which may be a synonym for the GPU; • Secure Enclave Processor (SEP), whose functions are described in the Apple Platform Security Guide. Each runs its own real-time operating system, RTKit, and loads substantial firmware during the boot process. https://eclecticlight.co/2021/08/24/whats-in-an-m1-chip-and-what-does-it-do-differently/

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Claim 5	Accused Products
	The World's Best CPU Performance per Watt M1 features an 8-core CPU consisting of four high-performance cores and four high-efficiency cores. Each of the high-performance cores provides industry-leading performance for single-threaded tasks, while running as efficiently as possible. They are the world's fastest CPU cores in low-power silicon, allowing photographers to edit high-resolution photos with lightning speed and developers to build apps nearly 3x faster than before. And all four can be used together for a huge boost in multithreaded performance. The four high-efficiency cores deliver outstanding performance at a tenth of the power. By themselves, these four cores deliver similar performance as the current-generation, dual-core MacBook Air at much lower power. They are the most efficient way to run lightweight, everyday tasks like checking email or browsing the web, and preserve battery life like never before. And all eight cores can work together to provide incredible compute power for the most demanding tasks and deliver the world's best CPU performance per watt. https://www.apple.com/newsroom/2020/11/apple-unleashes-m1/

Claim 8

Claim 8	Accused Products
8. The multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 1, wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor. For example, on information and belief each core is located a region of the multi-core processor. Identification of the physical arrangement of the cores is proprietary information of Apple that is the proper subject of fact discovery. <i>See, e.g.:</i>  https://www.apple.com/newsroom/2020/11/apple-unleashes-m1/

Claim 8	Accused Products
	The diagram illustrates the M1 Max chiplet architecture, consisting of two identical regions connected by UltraFusion. Each region is labeled 'M1 Max Chiplet: SLC (? MiB)'. Inside each region, there is an 'E-Cluster: L2 (4096 KiB)' and two 'P-Cluster: L2 (12 MiB)'. The E-Cluster contains two cores (L#0 and L#1) with L1d (64 KiB) and L1i (128 KiB) caches. The P-Clusters each contain four cores (L#2-L#5 and L#12-L#15) with L1d (128 KiB) and L1i (192 KiB) caches. Cores L#0 and L#1 are green, while others are blue. A central 'UltraFusion' block connects the two chiplets. Below the diagram is a URL: https://www.sciencedirect.com/science/article/pii/S1383762124000390?ref=pdf_download&fr=R-R-2&rr=923601bc8d6a6c81#fig2

Claim 9

Claim 9	Accused Products
9. The multi-core processor of claim 8, wherein the first region and the second region are overlapping regions of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 8, wherein the first region and the second region are overlapping regions of the multi-core processor. For example, on information and belief there is either some overlap or no overlap of the first and second regions. Identification of the physical arrangement of the cores is proprietary information of Apple that is the proper subject of fact discovery.

Claim 10

Claim 10	Accused Products
10. The multi-core processor of claim 8, wherein the first region and the second region are non-overlapping regions of the multi-core processor.	Each Accused Product comprises a multi-core processor of claim 8, wherein the first region and the second region are non-overlapping regions of the multi-core processor. For example, on information and belief there is either some overlap or no overlap of the first and second regions. Identification of the physical arrangement of the cores is proprietary information of Apple that is the proper subject of fact discovery.

Claim 14

Claim 14	Accused Products
14. The multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores.	Each Accused Product comprises a multi-core processor of claim 1, wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores. <i>See evidence and explanation of claim 5.</i> For example, on information and belief the e-cores and p-cores are located in a common region that is substantially central to the processor cores. Identification of the physical arrangement of the cores is proprietary information of Apple that is the proper subject of fact discovery.

Claim 21

Claim 21	Accused Products
[21pre]. A multi-core processor, comprising:	To the extent the preamble is limiting, each Accused Product comprises a multi-core processor. <i>See analysis and evidence of claim 1 preamble above.</i>

Claim 21	Accused Products
[21a] a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block;	Each Accused Product comprises a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage from a power control block and a first output clock signal from a first phase lock loop (PLL) having a first clock signal as input in a clock control block. <i>See</i> analysis and evidence of claim element [1a] above. Furthermore, each Accused Product includes a power control block and a clock control block. For example, Apple M series multi-core processor should contain a power controller and other controllers for supplying the voltage and clock signals as claimed. <i>See, e.g.:</i> Further coprocessors are thought to include: • Always On Processor (AOP), which handles environmental sensors and activation of the system; • Apple Video Decoder (AVD), which decodes video; • Apple Video Encoder (AVE), which encodes video; • Power Management Processor (PMP), the successor to power management features in the SMC. • Apple Graphics (AGX), which may be a synonym for the GPU; • Secure Enclave Processor (SEP), whose functions are described in the Apple Platform Security Guide. Each runs its own real-time operating system, RTKit, and loads substantial firmware during the boot process. https://eclecticlight.co/2021/08/24/whats-in-an-m1-chip-and-what-does-it-do-differently/

Claim 21	Accused Products
	Variable frequency This is another key feature of Apple silicon cores: unlike most older CPUs, the cores can be run at different frequencies or clock speeds, ranging from 696 MHz up to 4,056 MHz for M3 P cores. Although I don't know whether M3 cores take advantage of this, it's also possible that their voltage is variable. Much of the time, E cores running background threads in an M3 chip do so with the cores at their minimum frequency of only 744 MHz, but when they're used to run threads that have overflowed from P cores their frequency can rise to their maximum of 2,748 MHz. Overflowed threads on E cores thus can't benefit from the same high performance as they would on P cores, but they do run much faster than background threads. Clusters Cores of the same type are grouped into clusters. Within each cluster, all the cores run at the same frequency, and they share local memory in their level 2 (L2) cache. That also makes it easier for threads to be moved around between cores in the same cluster. In M1 and M2 family chips, their E and P cores are arranged in clusters of up to four cores; Apple changed that in the M3, whose clusters can be of as many as 6 cores, all of the same type. In all base version CPUs of M-series chips, there's one cluster of 4 E cores, and one cluster of 4 P cores, so the CPU can be designated as being 4P+4E. Pro, Max and Ultra versions have different numbers of cores, and may have two (or more) clusters of P cores in all. https://eclecticlight.co/2024/02/19/apple-silicon-1-cores-clusters-and-performance/

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[21b] a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically	Each Accused Product comprises a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal

Claim 21	Accused Products
receive a second supply voltage from the power control block and a second output clock signal from a second PLL having a second clock signal as input in the clock control block, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and	<i>See</i> analysis and evidence of claim element [1b] above. Furthermore, each Accused Product includes a power control block and a clock control block. For example, Apple M series multi-core processor should contain a power controller and other controllers for supplying the voltage and clock signals as claimed. <i>See, e.g.:</i> Further coprocessors are thought to include: • Always On Processor (AOP), which handles environmental sensors and activation of the system; • Apple Video Decoder (AVD), which decodes video; • Apple Video Encoder (AVE), which encodes video; • Power Management Processor (PMP), the successor to power management features in the SMC. • Apple Graphics (AGX), which may be a synonym for the GPU; • Secure Enclave Processor (SEP), whose functions are described in the Apple Platform Security Guide. Each runs its own real-time operating system, RTKit, and loads substantial firmware during the boot process. https://eclecticlight.co/2021/08/24/whats-in-an-m1-chip-and-what-does-it-do-differently/

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Claim 21	Accused Products
	The World's Best CPU Performance per Watt M1 features an 8-core CPU consisting of four high-performance cores and four high-efficiency cores. Each of the high-performance cores provides industry-leading performance for single-threaded tasks, while running as efficiently as possible. They are the world's fastest CPU cores in low-power silicon, allowing photographers to edit high-resolution photos with lightning speed and developers to build apps nearly 3x faster than before. And all four can be used together for a huge boost in multithreaded performance. The four high-efficiency cores deliver outstanding performance at a tenth of the power. By themselves, these four cores deliver similar performance as the current-generation, dual-core MacBook Air at much lower power. They are the most efficient way to run lightweight, everyday tasks like checking email or browsing the web, and preserve battery life like never before. And all eight cores can work together to provide incredible compute power for the most demanding tasks and deliver the world's best CPU performance per watt. https://www.apple.com/newsroom/2020/11/apple-unleashes-m1/
[21c] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to	Each Accused Product comprises an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores. <i>See analysis and evidence of claim element [1c] above.</i>

Claim 21	Accused Products
facilitate communication between the first set of processor cores and the second set of processor cores.	