

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
MIDLAND/ODESSA DIVISION**

REDSTONE LOGICS LLC,

Plaintiff,

v.

APPLE INC.,

Defendant.

No. 7:25-cv-00183-ADA

DEFENDANT APPLE INC.'S PRELIMINARY INVALIDITY CONTENTIONS

I. INTRODUCTION

Pursuant to the Agreed Scheduling Order (ECF No. 25), Defendant Apple Inc. provides these Preliminary Invalidity Contentions to Plaintiff Redstone Logics LLC (“Redstone”) for the Asserted Claims of U.S. Patent No. 8,549,339 (the “’339 patent” or “Asserted Patent”). In its July 14, 2025, Preliminary Infringement Contentions, Redstone asserts the following claims against Apple:

- ’339 patent, claims 1, 5, 8, 9, 10, 14, and 21 (the “Asserted Claims”).

A. Claim Construction

As the Court has not yet construed any Asserted Claims, Apple bases these contentions on its current understanding of them. Apple’s positions do not reflect or imply a particular construction of any claim term nor admit that any accused products or services fall within the scope of an Asserted Claim.

Although Apple has considered Redstone’s apparent constructions in Redstone’s Infringement Contentions, Apple does not admit that they are correct or find support in the Asserted Patent. Nothing in these Preliminary Invalidity Contentions operates as an admission or waiver by Apple as to any construction of the Asserted Claims. Nor does Apple admit that the Asserted Claims are valid under 35 U.S.C. § 112 as definite, possessing adequate written description, or sufficiently enabling.

B. Ongoing Discovery and Disclosures

Apple also provides these contentions without the benefit of discovery, including claim construction discovery, fact discovery, third-party discovery, and expert discovery. As one example, fact discovery has not yet begun, and deposing the alleged inventors may reveal information that affects Apple’s contentions, and discovery from third parties with information concerning possible prior art, including additional evidence regarding prior art systems disclosed or cited herein. Apple reserves the right to amend or supplement these Preliminary Invalidity Contentions based on its investigation and discovery from Redstone or third parties with knowledge regarding prior art systems and products, as those investigations may reveal

additional relevant prior art systems and products or further information regarding those systems and products.

As Apple has explained in separate correspondence, Redstone's Infringement Contentions fail to comply with the Court's Order Governing Proceedings and to put Apple on notice of Redstone's infringement theories. These failures prejudice Apple's ability to adequately prepare its defenses. Apple therefore reserves the right to amend or supplement these Preliminary Invalidity Contentions with information it later learns.

Apple incorporates by reference all bases for invalidity identified in subsequent pleadings and discovery responses in this case, in other litigation brought by Redstone involving the Asserted Patent or related patents, and in any post grant proceedings (e.g., *inter partes* review) involving the Asserted Patent or related patents and during prosecution of the Asserted Patent and related patents or applications. Apple further incorporates by reference all admissions regarding the Asserted Patent including in the specification of the Asserted Patent and during prosecution of the Asserted Patent or related patents and patent applications.

These Preliminary Invalidity Contentions further incorporate by reference (1) all prior art identified in Redstone's document production to Apple in this case; (2) all materials regarding invalidity that Redstone should have produced to Apple but has not; and (3) all prior art of which a named inventor of the Asserted Patent is aware or on which they or Redstone contends the alleged invention(s) of the Asserted Patent builds upon. In addition, these Preliminary Invalidity Contentions incorporate all prior art identified in any related litigation or proceeding, including any petitions for *inter partes* review of the Asserted Patent.

II. PRIORITY DATE OF THE ASSERTED PATENT AND CLAIMS

When it served its July 14, 2025, Infringement Contentions, Redstone stated "that the asserted claims of the '339 patent are each entitled to a priority date (invention date) at least as early as February 26, 2010," *i.e.*, the filing date of the U.S. non-provisional application that matured into the '339 patent. Redstone does not claim the '339 patent is entitled to an earlier priority or benefit date and has not attempted to meet its burden in showing entitlement to such a

date. Apple reserves the right to amend or supplement these contentions with additional art if Redstone identifies an earlier priority or benefit date.

III. PRIOR ART IDENTIFICATION AND INVALIDITY CLAIM CHARTS

Apple's invalidity claim charts cite specific parts of prior art references that relate to elements of the Asserted Claims. When the charts cite a figure, the citation includes its caption and related descriptions. Likewise, text that refers to a figure includes the figure and its related visuals.

Skilled artisans in the field may view these references more broadly in the context of other materials and knowledge. The cited portions of prior art references are merely exemplary, and the references may have additional relevant support. Apple may use uncited parts of these references, other documents, systems, and expert or fact testimony to explain or support its arguments. This includes parts of the references that demonstrate how combinations of the references make the Asserted Claims obvious. Apple also may rely on any systems that mention or are mentioned by Apple's identified prior art.

Apple may use Redstone's or the inventors' statements (*e.g.*, during prosecution or related legal proceedings or in this or other cases) to support its positions (*e.g.*, on the scope of the Asserted Patent). Apple also may support its positions using industry publications, standards, products, or testimony to show what a skilled person would have known.

The prior art may show the claimed elements either directly or indirectly. These references also are relevant to understanding the state of the art and the motivations to combine ideas. Obviousness combinations are presented as alternatives to Apple's positions that some references alone anticipate the Asserted Claims. Any listed combinations are exemplary and reflect what the skilled artisan would know. Apple may identify more combinations later. If Redstone argues that some claim elements are missing from Apple's references, Apple may present additional references.

Lastly, Apple denies infringement, and none of Apple's statements constitute an admission that its products satisfy any claim elements. That a cited reference includes an

element similar to one in an accused product does not mean Apple agrees with Redstone's interpretation of the claims or admits infringement.

IV. PRELIMINARY INVALIDITY CONTENTIONS FOR THE ASSERTED PATENT

A. Prior Art References¹

1. Prior Art Patents and Publications

The following prior art patents and printed publications anticipate the Asserted Claims under 35 U.S.C. § 102(a), (b), (e), and/or (g) or render them obvious under 35 U.S.C. § 103, either alone or in combination.

Prior Art	Date of Issue / Publication	Effective Filing Date
U.S. Patent No. 7,263,457 ("White")	8/28/2007	1/3/2006
U.S. Pub No. 2007/0096775 ("Elgebaly")	5/3/2007	11/22/2005
U.S. Pub No. 2009/0271646 ("Talwar")	10/29/2009	10/31/2008
U.S. Pub No. 2010/0073068 ("Cho")	3/25/2010	9/22/2008
U.S. Patent No. 8,122,270 ("Allarey")	2/21/2012	9/29/2008
U.S. Pub. No. 2012/0060170 ("Vajda")	3/8/2012	5/26/2009
U.S. Pub. No. 2008/0209133 ("Ozer")	8/28/2008	2/22/2007
U.S. Pub. No. 2009/0158078 ("Knoth")	6/18/2009	12/12/2007
U.S. Pub. No. 2010/0122101 ("Naffziger")	5/13/2010	11/11/2008

¹ If prior art patents, publications, or systems are identified in the attached claim charts but are absent from the tables and lists below, those prior art patents, publications, or systems are also prior art to the Asserted Patent.

Prior Art	Date of Issue / Publication	Effective Filing Date
U.S. Pub. No. 2005/0034002 ("Flautner")	2/10/2005	8/4/2003
U.S. Pub No. 2011/0153984 ("Wolfe")	6/23/2011	12/21/2009
U.S. Pub No. 2007/0080696 ("Kumar")	4/12/2007	10/11/2005
U.S. Pub. No. 2005/0289365 ("Bhandarkar")	12/29/2005	6/29/2004
U.S. Pub. No. 2008/0046770 ("Jong")	2/21/2008	7/5/2007
U.S. Pub. No. 2008/0101523 ("Kurd 2008")	5/1/2008	10/26/2006
U.S. Pub. No. 2008/0172565 ("Chu")	7/17/2008	12/31/2007
U.S. Pub. No. 2010/0293401 ("De Cesare")	11/18/2010	5/13/2009
U.S. Pub. No. 2008/0256381 ("Jacobowitz 2008")	10/16/2008	4/12/2007
U.S. Pub. No. 2009/0106576 ("Jacobowitz 2009")	4/23/2009	10/17/2007
U.S. Patent No. 8,359,487 ("Muraki")	1/22/2013	3/19/2008
U.S. Patent No. 8,892,931 ("Kruglick")	11/18/2014	10/20/2009
U.S. Patent No. 7,949,887 ("Gunther")	5/24/2011	11/1/2006
U.S. Patent No. 7,290,156 ("Gaskins")	10/30/2007	4/1/2004
U.S. Pub. No. 2006/0136763 ("Jorgenson")	6/5/2007	12/21/2004

Prior Art	Date of Issue / Publication	Effective Filing Date
U.S. Pub. No. 2010/0188115 (“Von Kaenel”)	7/29/2010	1/28/2009
U.S. Pub. No. 2008/0276261 (“Munshi”)	11/6/2008	5/3/2007
U.S. Patent No. 8,161,314 (“Jacobowitz ’314”)	4/17/2012	4/12/2007
U.S. Patent No. 8,028,185 (“Branover ’185”)	9/27/2011	3/11/2008
U.S. Patent No. 7,412,353 (“Borkar ’353”)	8/12/2008	9/28/2005
U.S. Patent No. 7,581,087 (“Kallacheril”)	8/25/2009	2/22/2006
U.S. Patent No. 8,566,836 (“Ramaraju ’836”)	10/22/2013	11/13/2009
U.S. Patent No. 8,615,647 (“Hum”)	12/24/2013	7/22/2008
U.S. Patent No. 9,563,250 (“Rychlik”)	2/7/2017	12/16/2009
U.S. Patent No. 8,037,340 (“Kim ’340”)	10/11/2011	11/28/2007
U.S. Patent No. 8,276,015 (“Floyd”)	9/25/2012	2/23/2009
U.S. Patent No. 8,250,395 (“Carter”)	8/21/2012	11/12/2009
U.S. Pub. No. 2009/0309243 (“Carmack”)	12/17/2009	6/11/2008
U.S. Patent No. 8,578,193 (“Kim ’193”)	11/5/2013	11/28/2007
U.S. Patent No. 8,892,916 (“Bieswanger”)	11/18/2014	8/6/2008

Prior Art	Date of Issue / Publication	Effective Filing Date
U.S. Patent No. 8,452,991 ("Geissler")	5/28/2013	8/20/2009
U.S. Patent No. 7,451,333 ("Naveh")	11/11/2008	9/3/2004
U.S. Patent No. 7,689,848 ("Abbo")	3/30/2010	12/13/2006
U.S. Patent No. 7,917,799 ("Jacobowitz '799")	3/29/2011	4/12/2007
U.S. Patent No. 8,352,669 ("Wu")	1/8/2013	4/27/2009
U.S. Patent No. 7,568,115 ("Borkar '115")	7/28/2009	9/28/2005
U.S. Patent No. 7,724,078 ("Kurd '078")	5/25/2010	3/22/2007
U.S. Patent No. 7,724,028 ("Ansari")	5/25/2010	4/11/2008
U.S. Patent No. 7,434,080 ("Kuo")	10/7/2008	9/3/2002
U.S. Patent No. 6,825,690 ("Kundu")	11/30/2004	5/28/2003
U.S. Patent No. 7,669,155 ("Ganesan")	2/23/2010	3/26/2007
U.S. Patent No. 7,566,923 ("McGrath")	7/28/2009	12/23/2005
U.S. Patent No. 7,330,994 ("Frederick")	2/12/2008	4/26/2005
U.S. Patent No. 7,003,423 ("Kabani")	2/21/2006	12/18/2003
U.S. Patent No. 6,922,111 ("Kurd '111")	7/26/2005	12/20/2002
U.S. Pub. No. 2011/0119672 ("Ramaraju 2011")	5/19/2011	11/13/2009

Prior Art	Date of Issue / Publication	Effective Filing Date
U.S. Pub. No. 2010/0115304 ("Finkelstein")	5/6/2010	10/31/2008
U.S. Pub. No. 2008/0162770 ("Titiano")	7/3/2008	12/11/2007
U.S. Pub. No. 2008/0276026 ("Branover 2008")	11/6/2008	5/2/2007
U.S. Pub. No. 2011/0022356 ("Nussbaum")	1/27/2011	7/24/2009
U.S. Pub. No. 2006/0282692 ("Oh")	12/14/2006	6/6/2006
U.S. Patent No. 7,447,873 ("Nordquist")	11/4/2008	11/29/2005
U.S. Pub. No. 2006/0190755 ("Kim 2006")	8/24/2006	2/16/2006
U.S. Pub. No. 2009/0138737 ("Kim 2009")	5/28/2009	11/28/2007
Williams et al., <i>Low Latency Clock Domain Transfer for Simultaneously Mesochronous, Plesiochronous and Heterochronous Interfaces</i> , 2007 ("Williams")	2007	N/A
Nawathe, <i>Design of High Performance Low Power Microprocessors</i> , 2010 ("Nawathe")	2010	N/A
Lee et al., <i>Dynamic Voltage and Frequency Scaling (DVFS) Scheme for Multi-Domains Power Management</i> , 2007 ("Lee")	11/12/2007	N/A
Rotem et al., <i>Multiple clock and voltage domains for chip multi processors</i> , 2009 ("Rotem")	12/12/2009	N/A

Prior Art	Date of Issue / Publication	Effective Filing Date
Madduri et al., <i>A monitor interconnect and support subsystem for multicore processors</i> , 2009 (“Madduri”)	4/20/2009	N/A
Xanthopoulos, <i>Clocking in Modern VLSI Systems</i> , 2009 (“Xanthopoulos”)	2009	N/A
Orgas et al., <i>Variation-Adaptive Feedback Control for Networks-on-Chip with Multiple Clock Domains</i> , 2008 (“Orgas”)	2008	N/A
Magklis et al., <i>Independent Front-end and Back-end Dynamic Voltage Scaling for a GALS Microarchitecture</i> , 2006 (“Magklis”)	2006	N/A
Herbert & Marculescu, <i>Analysis of Dynamic Voltage/Frequency Scaling in Chip-Multiprocessors</i> , 2007 (“Herbert”)	2007	N/A
Grammatikakis et al., <i>Power-Aware Multicore SoC and NoC Design</i> , 2010 (“Grammatikakis”)	January 2010	N/A
Guang et al., <i>A review of dynamic power management methods in NoC under emerging design considerations</i> , 2009 (“Guang”)	2009	N/A
Guang et al. <i>System-Level Exploration of Run-time Clusterization for Energy-efficient On-Chip Communication</i> , 2009 (“Guang”)	2009	N/A
Karpuzcu et al., <i>The BubbleWrap Many-Core: Popping Cores for Sequential Acceleration</i> , 2009 (“Karpuzcu”)	December 2009	N/A

Prior Art	Date of Issue / Publication	Effective Filing Date
Rangan et al., <i>Thread Motion: Fine-Grained Power Management for Multi-Core Systems</i> , 2009 (“Rangan”)	June 2009	N/A
Strik et al., <i>Heterogeneous multiprocessor for the management of realtime video and graphics streams</i> , 2000 (“Strik”)	1/1/2000	N/A
Chen et al., <i>Clock Power Issues in System-on-a-Chip Designs</i> (“Chen”)	April 1999	N/A
Fan et al., <i>A Synchronized Variable Frequency Clock Scheme in Chip Multiprocessors</i> , 2008 (“Fan”)	2008	N/A
Bhunja et al., <i>GAARP: A Power-Aware GALS Architecture for Real-Time Algorithm-Specific Tasks</i> , 2005 (“Bhunja”)	June 2005	N/A
Nose et al., <i>Deterministic inter-core synchronization with periodically all-in-phase clocking for low-power multi-core SoCs</i> , 2005 (“Nose”)	2005	N/A
Hattori et al., <i>A Power Management Scheme Controlling 20 Power Domains for a Single-Chip Mobile Processor</i> , 2007 (“Hattori”)	2007	N/A

2. Prior Art Systems and Products

The following prior art products or systems invalidate the Asserted Claims under 35 U.S.C. § 102(a), (b), and/or (g) or render the Asserted Claims obvious under 35 U.S.C. § 103, either alone or in combination.

Prior Art	Short Name	Date of Use, Sale, Offer for Sale, or Invention
AMD Quad-Core Opteron	“Opteron”	At least as early as 2005
Intel Itanium 65 nm Dual-Core Processor	“Itanium Dual-Core”	At least as early as 2004
Intel Itanium 65 nm Quad-Core Processor	“Itanium Quad-Core”	At least as early as 2004
Intel 65 nm Core Duo Processor	“Core Duo”	At least as early as 2006
Intel 65 nm Xeon Dual-Core Processor	“Xeon Dual-Core”	At least as early as 2006
Intel Nehalem 45nm Dual-Core Penryn Processor	“Nehalem Dual-Core”	At least as early as 2007
Intel Nehalem 45nm Quad-Core Processor	“Nehalem Quad-Core”	At least as early as 2009
Intel Nehalem 45nm 6-Core Xeon Processor	“Nehalem 6-Core”	At least as early as 2009
Intel Nehalem 45nm 8-Core Xeon Processor	“Nehalem 8-Core”	At least as early as 2007
Intel Westmere 32 nm	“Westmere”	At least as early as 2004
Intel Single-chip Cloud Computer	“SCC”	At least as early as 2009
MSC8156 Six Core Digital Signal Processor	“NXP”	At least as early as August 2009
ARM ARM1176JZF Processor	“ARM”	At least as early as August 31, 2007
NVIDIA Tegra 2 Microprocessor	“NVIDIA”	At least as early as February 15, 2010
IBM Power6	“Power6”	At least as early as 2007
STI CELL Hetero	“STI CELL”	At least as early as 2007
PA Semi PA6T-1682M	“PA Semi”	At least as early as 2007

Apple may rely on physical samples, executable software, or source code as evidence of the relevant functionality of these prior art products and systems. Apple will make available for inspection any additional documentation, evidence, or physical samples of products, systems, or software listed above and related source code in its possession or that becomes available during discovery.

3. The Accused Functionality

Apple denies that the accused M Series or A Series system-on-chips, or any other Apple product, service, or functionality infringes any valid or enforceable claim of the Asserted Patent. As noted, Redstone has not and cannot meet its burden to show entitlement to a priority date or benefit date earlier than the Asserted Patent's filing date of February 26, 2010.

By alleging that the accused M Series—and the later-accused A Series—system-on-chips infringe, Redstone admits that the same functionality would invalidate the Asserted Claims of the Asserted Patent. *See Upsher-Smith Labs., Inc. v. PamLab, L.L.C.*, 412 F.3d 1319, 1322 (Fed. Cir. 2005) (“A century-old axiom of patent law holds that a product which would literally infringe if later in time anticipates if earlier.”) (citation omitted); *accord Peters v. Active Mfg. Co.*, 129 U.S. 530, 537 (1889) (“That which infringes, if later, would anticipate if earlier.”); *see also Vanmoor v. Wal-Mart Stores, Inc.*, 201 F.3d 1363, 1366 (Fed. Cir. 2000) (affirming patent invalidity based on patentee's infringement allegations because accused product was on sale before invention's critical date).

Apple also has patents and publications related to the accused M Series and A Series system-on-chips that predate the Asserted Patent's earliest priority date. Apple identifies examples of these references herein.

4. State of the Art and Admitted Prior Art

The Asserted Patent acknowledges that many aspects of the alleged invention were already known in the art. It states that components “can be arranged, substituted, combined, and designed in a wide variety of different configurations,” all of which are part of the invention. '339 patent, 1:49-57. The Asserted Patent also acknowledges that one skilled in the art would

understand how to implement the inventions or design its circuits. *Id.* at 5:38-6:9. The Asserted Patent further concedes that the “depicted architectures are merely exemplary, and that in fact many other architectures can be implemented which achieve the same functionality.” *Id.* at 6:33-55. Apple may rely on those admissions. *See Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1998) (“A statement in a patent that something is in the prior art is binding on the applicant and patentee for determinations of anticipation and obviousness.”); *In re Fout*, 675 F.2d 297, 300 (C.C.P.A. 1982) (“Valid prior art may be created by the admissions of the parties.”).

B. Identification of Anticipation and Obviousness Combinations

Under the Court’s January 23, 2024, Standing Order Governing Proceedings (OGP) 4.4-Patent Cases, Section II.4, Apple provides the following exemplary charts identifying examples of prior art and prior art combinations that anticipate or render obvious each Asserted Claim. Apple’s investigation and review of these references remains ongoing, and it reserves the right to supplement or add to these exemplary charts.

Exhibit	Invalidity Chart Reference(s)
1	White
2	Elgebaly
3	Talwar
4	Cho
5	Vajda
6	Ozer
7	Knoth
8	Naffziger
9	Allarey
10	Flautner

Exhibit	Invalidity Chart Reference(s)
11	Wolfe
12	Kumar
13	Bhandarkar
14	Jong
15	Kurd 2008
16	Chu
17	Jacobowitz 2008
18	Jacobowitz 2009
19	Gunther
20	Gaskins
21	Jorgenson
22	Muraki
23	Ramaraju 2011
24	Finkelstein
25	Titiano
26	Branover 2008
27	Nussbaum
28	Oh
29	Nordquist
30	Kim 2006
31	Kim 2009
32	Von Kaenel
33	De Cesare

Exhibit	Invalidity Chart Reference(s)
34	Kruglick
35	Nawathe
36	Williams
37	Lee
38	Opteron
39	Itanium Quad-Core
40	Nehalem 8-Core
41	Westmere
42	SCC
43	NXP
44	ARM
45	NVIDIA

In these exhibits, where Apple cites to a particular figure in a prior art reference, the citation encompasses the caption and description of the figure and any text relating to the figure in addition to the figure itself. Conversely, where a cited portion of text refers to a figure, the citation should be understood to include the figure as well. Witness testimony or discovery may provide additional evidence and context for the features and elements of the prior art references above.

If any specific reference lacks a limitation of the Asserted Claims, each of the other references in the attached exhibits may be used in combination with other references identified in these contentions to render the asserted claims invalid under 35 U.S.C. § 103. Apple provides exemplary obviousness combinations below. Apple's investigation remains in its early stages, and its further investigation and discovery may lead to additional prior art and prior art combinations. Apple's inclusion of exemplary combinations does not preclude it from

identifying other prior art and invalidating combinations. Apple reserves the right to identify additional specific combinations as well as to detail and explain such combinations.

The Asserted Claims of the '339 Patent are rendered obvious by:

- White alone or in combination with at least one of Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Elgebaly alone or in combination with at least one of White, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Talwar alone or in combination with at least one of White, Elgebaly, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;

- Knoth alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Naffziger alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Allarey alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Flautner alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim

- 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Wolfe alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
 - Bhandarkar alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
 - Jong alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;

- Chu alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Jacobowitz 2008 alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Jacobowitz 2009 alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Jorgenson alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim

- 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Nordquist alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
 - Kim 2009 alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
 - Kruglick alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;

- Opteron alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Itanium Quad-Core, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Itanium Quad-Core alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Nehalem 8-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Nehalem 8-Core alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh, Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Westmere, Intel SCC, NXP, ARM, NVIDIA and/or the admitted prior art;
- Intel SCC alone or in combination with at least one of White, Elgebaly, Talwar, Cho, Vajda, Ozer, Knoth, Naffziger, Allarey, Flautner, Wolfe, Kumar, Bhandarkar, Jong, Kurd 2008, Chu, Jacobowitz 2008, Jacobowitz 2009, Gunther, Gaskins, Jorgenson, Muraki, Ramaraju 2011, Finkelstein, Titiano, Branover 2008, Nussbaum, Oh,

Nordquist, Kim 2006, Kim 2009, Von Kaenel, De Cesare, Kruglick, Nawathe, Williams, Lee, Opteron, Itanium Quad-Core, Nehalem 8-Core, Westmere, NXP, ARM, NVIDIA and/or the admitted prior art;

Apple identifies these obviousness combinations as alternatives to its anticipation and single-reference obviousness contentions. By identifying them, Apple does not concede that any reference is not anticipatory or would not render the Asserted Claims obvious in light of the skilled artisan's knowledge.

1. Motivations to Combine, Reasonable Expectation of Success, and Obviousness

Each Asserted Claim is obvious in view of the items of prior art identified above, both alone (coupled with the skilled artisan's knowledge) and in combination with other items of prior art identified above.

The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including “(1) the scope and content of the prior art; (2) the level of ordinary skill in the art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness.” *Miles Labs., Inc. v. Shandon, Inc.*, 997 F.2d 870, 877 (Fed. Cir. 1993); *see also Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17-18 (1966). The Supreme Court's decision in *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398, 415-16 (2007), reaffirmed *Graham* and further held that a claimed invention can be obvious even if there is no teaching, suggestion, or motivation for combining the prior art to produce that invention. *KSR* holds that patents based on new combinations of elements or components already known in a technical field may be found to be obvious. *See generally KSR*, 550 U.S. 398. The Court in *KSR* rejected a rigid application of the “teaching, suggestion, or motivation [to combine]” test. *Id.* at 418-19.

“In determining whether the subject matter of a patent claim is obvious, neither the particular motivation or the avowed purpose of the patentee controls. What matters is the objective reach of the claim.” *Id.* at 419. “Under the correct analysis, any need or problem

known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *Id.* at 420. In *KSR*, the Supreme Court emphasized the principle that “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *Id.* at 416. A key inquiry is whether the “improvement is more than the predictable use of prior art elements according to their established functions.” *Id.* at 417.

Notably, each item of prior art is in the same technical field as the Asserted Patent. *Compare* ’339 patent, *with* Exs. 1-45. Thus, a skilled artisan would have recognized the obviousness of combining a beneficial concept disclosed in one item of prior art with a beneficial concept disclosed in another item of prior art.

Furthermore, a skilled artisan would have readily taken teachings from one item of prior art and applied them to other items of prior art, with predictable results. As noted above, multiple items of prior art teach or suggest the concepts claimed in the Asserted Patent. If Redstone argues that any concepts claimed in the Asserted Patent were not disclosed in any item of prior art, it would have been obvious to adapt each item of prior art to include the concept or combine it with other items of prior art that disclose the concept. In addition, the charted disclosures in Exhibits 1-45 were well known to skilled artisans and understood to be among a menu of available design choices for contactless inductive power transfer systems.

Additionally, common industry knowledge supplied a motivation to combine the charted disclosures in the items of prior art with each other. Each combination would have produced no unexpected results and would have been a known alternative to a person of ordinary skill in the art (“POSITA”).

No showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have yielded expected results and at most would simply represent a known alternative to one of skill in the art. *See Apple Inc. v. Samsung Elecs. Co.*, 839 F.3d 1034, 1058 (Fed. Cir. 2016); *Intercontinental Great Brands LLC v. Kellogg N. Am. Co.*, 869 F.3d 1336, 1344 (Fed. Cir. 2017).

Nevertheless, in addition to the information under the headings for the Asserted Patent and elsewhere in these contentions, Apple identifies exemplary motivations and reasons to combine.

The Asserted Patent itself establishes motivations to combine the identified prior art to create a multi-core processor with communication between cores. The Asserted Patent claims many generic elements of a multi-core processor and means for handling communication between processor cores. The Asserted Claims of the Asserted Patent also, at most, only slightly modify a known solution to a common issue at the time or merely arrange old elements, with each performing the same previously known function and yielding no more than what the skilled artisan would have expected from such an arrangement. As discussed above, the Asserted Patent admits that many implementations, arrangements, and combinations of these multi-core processors would be known to those skilled in the art and are “explicitly contemplated” as part of the disclosure. ’339 patent, 1:44-57.

All Asserted Claims also are obvious based on one or more combinations above. The accompanying charts explain how different portions of each reference discloses each limitation of the Asserted Claims. Should Redstone argue that any reference lacks a feature, the skilled artisan would at a minimum, as of the Asserted Patent’s filing date, have been motivated to modify the reference to include the allegedly missing feature(s), or to combine it with other references that include that feature.

A skilled artisan would have been motivated to combine the disclosures charted in Exhibits 1-45 for at least the following reasons:

- (A) the Asserted Claims combine prior art elements according to known methods to yield predictable results;
- (B) the Asserted Claims involve the simple substitution of one known element for another to obtain predictable results;
- (C) the Asserted Claims involve the use of known technique to improve similar devices (methods, or products) in the same way;
- (D) the Asserted Claims apply a known technique to a known device (method, or

product) ready for improvement to yield predictable results;

(E) the Asserted Claims involve combinations of prior art references that would have been “obvious to try”—a POSITA could have reached the Asserted Claims by choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;

(F) the Asserted Claims are simply variations of work from one field of endeavor or a different one that would have been prompted based on design incentives or other market forces because the variations were predictable to one of ordinary skill in the art.

See KSR, 550 U.S. at 415-18; *see also* Manual of Patent Examining Procedure § 2143.

Additional evidence that there would have been a motivation to combine the identified references includes the interrelated teachings of multiple references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged inventions; and the background knowledge that would have been possessed by a POSITA. *See Arctic Cat Inc. v. Bombardier Rec. Prod. Inc.*, 876 F.3d 1350, 1359 (Fed. Cir. 2017); *Intercontinental Great Brands*, 869 F.3d at 1344 (Fed. Cir. 2017); *Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1003 (Fed. Cir. 2016); *Norgren Inc. v. ITC*, 699 F.3d 1317, 1322-23 (Fed. Cir. 2012).

For example, both the Asserted Patent and the prior art references in Apple’s charts are directed to the fields of processor technology, communication between processor cores, and processor efficiency. Additionally, both the Asserted Patent and these references identify and address many of the same technical issues (*e.g.*, excessive power consumption and ineffective communication between cores in different power domains) and suggest similar solutions to those issues (*e.g.*, implementing different power domains with dynamic voltage and frequency scaling and employing interfaces with level shifters between the domains). For example, the Asserted Patent recognizes that “a conventional multi-core processor generally shares the same supply

voltage and clock signal to simplify the interfaces between the processor cores” and “dynamic supply voltage and clock speed control may be utilized, so that a multi-core processor may operate at high power and high clock frequency when needed and at low power when the computing requirements are reduced.” ’339 patent, 1:6-15. The Asserted Patent does not describe novel processor components to improve on conventional multi-core processors. *E.g.*, *id.* at 6:28-32; *see generally id.*

Accordingly, the Asserted Patent proposes mechanisms to improve power management by providing independent supply voltages and clock signals to flexibly and efficiently allocate power among the core domains based on their workloads. For example, the Asserted Patent states that “[a] power profile associated with an individual processor core...[and] may include, without limitation, one or more power-supply voltages of the core processor, clock rates of the core processor, clock multipliers of the core processor, power throttling of the core processor, and/or sleep state cycles of the core processor.” ’339 patent, 1:62-2:3. The Asserted Patent also explains that “[t]he power profile associated with a stripe may be determined based on the computational requirements of the tasks assigned to the processor cores in the stripe” and “[b]ased on the measured operational information (*e.g.*, supply voltage and local temperature) and the performance data, the power control block 108 may then be configured to select a supply voltage for each stripe...[where] the tasks with the highest computational requirements may be scheduled into the topmost stripe, such as the stripe 112...configured to operate at a high supply voltage...[and] tasks with lesser computational requirements may be scheduled into the stripe 114...configured to operate lower supply voltages.” *Id.* at 2:41-46.

The skilled artisan would have known of the issues of excessive power consumption and communication between cores. The skilled artisan also would have known of the solutions of providing different supply voltages and clock signals to the cores of the processor and to interface between the cores to effectively reduce the power consumption of the multi-core processor. The skilled artisan thus would have been motivated to identify these solutions to these problems in the prior art that Apple identifies. The prior art relates to processor

technology, including multi-core processors and processors with independent supply voltages and clock signals. The skilled artisan would have been motivated to combine their teachings with a reasonable expectation of success. Moreover, multiple cores or sets of cores, voltage supplies, reference clocks, PLLs, and interface blocks were well known in the art. Replacing a component of a processor design for one of these components would have been a matter of simple substitution of one known element for another to obtain predictable results. For example, the skilled artisan would have been motivated to combine the concept of multiple independent reference clocks with a commercial multi-core processor to solve the problems of power consumption known to the skilled artisan and identified in the Asserted Patent.

By way of example, if one of Apple's charted references does not expressly disclose a first and second PLLs receiving a first and second clock signal, where the first and second clock signals are independent from each other, it would have been obvious at least by the purported February 26, 2010, priority date for a skilled artisan to use a first and second clock signal that are independent from each other. That separate PLLs could have independent inputs clock signals was well known and well understood in the field. *See, e.g.,* White, 7:40-45 ("Additionally, in some embodiments, frequency regulator 140 may include clock trees or other circuitry configured to split or divide a clock signal into multiple individual signals and may include multiple clock sources in order to supply multiple, independent clock signals of different frequencies."); Bhandarkar, Fig. 3, [0032] ("In still other embodiments, power source 340 and clock source 345 provide entirely independent power supply voltages and clock frequencies to each of processors 310 and 315."); Nehalem 8-Core, Tam at 154 ("The filter PLL (FtrPLL) receives and filters the external system clock and generates three low-jitter internal PLL reference clocks at 1X, 2X, and 4X of the system clock (BCLK) frequency. These reference clocks are distributed to the cascaded PLLs in a balanced fashion to achieve minimal skew and to ensure high synchronism between the independent clock domains at the common BCLK reference edges even when the domains are operating pseudo-asynchronously at different frequencies.").

In addition, the skilled artisan would have recognized that a multi-core processor with independent clock signals to either each core or each set of cores was well known and obvious to try when designing a multi-core processor. *See, e.g.*, Cho, [0036] (“Changing the frequency of individual clock signals may be performed for temperature control purposes. For example, if a given functional unit is reporting a temperature over a predetermined threshold, control logic 305 may direct clock control unit 310 to reduce the frequency of its corresponding clock signal. . . . Since the clock signals are independently controllable, the other clock signals need not be affected by a frequency change of a particular one of the clock signals.”); Elgebaly, [0032] (“Each processing core 130 receives from clock generator 140 a clock used to trigger synchronous circuits within the core. Each core 130 provides to clock generator 140 and to its AVS unit 230 a target frequency for its clock.”); White, 7:23-8:40 (“Frequency regulator 140 may include any of various sorts of clock sources, such as an oscillator or phase locked loop (PLL) to generate a reference clock signal. Additionally, in some embodiments, frequency regulator 140 may include clock trees or other circuitry configured to split or divide a clock signal into multiple individual signals and may include multiple clock sources in order to supply multiple, independent clock signals of different frequencies.”); Vajda, [0065] (“The multi-core chip can contain several processor cores that “may be adapted to operate on either a first operating frequency or at least one second frequency.”)

The skilled artisan further would have recognized that the references disclose independent supply voltages to the cores or sets of cores. *See, e.g.*, White, 9:54-11:23 (“One or more voltage regulators, such as voltage regulator 130, may be configured to supply voltage to each logic core 120 and/or common bridge logic 110 at a different level.”); Bhandarkar, [0018] (“In such embodiments, each of processor cores 111 a-d that are stalled may be put into a lower power state, thereby removing some of the demand for power and freeing up capacity for heat dissipation, thereby allowing the frequency of the processor clock and/or the voltage of the supplied power to be increased so as to allow the other ones of processor cores 111 a-d that are not stalled to execute instructions faster.”); Cho, [0037] (“In the embodiment shown, each of

voltage control signals vctrl1-vctrl4 corresponds to a unique one of the functional units. Accordingly, power control unit 320 may control the power consumption of each of the functional units independently of one another.”); Elgebaly, [0032] (“Each processing core 130 and its associated AVS unit 230 also receive a regulated Supply Voltage (Vdd) from power management unit 180.”). The skilled artisan would have understood that the prior art references were addressing the issue of efficient power consumption and thus looked to these references for disclosures to solve this problem. *See, e.g.*, Elgebaly, [0006]; White, 9:54-11:23; Gaskins, [Abstract] (noting speed of processing as an additional benefit); Vajda, [0063] (avoiding overheating from inefficient power management); Cho, [Abstract] (temperature control).

The skilled artisan further would have recognized motivations to combine certain references from Exhibits 1-45. As one example, to the extent Itanium or Opteron do not anticipate each element of the Asserted Claims, these systems would have rendered the Asserted Claims obvious in combination with at least Cho, Talwar, or Vajda. The skilled artisan would be motivated to combine these references because each relate to advancements in multi-core processor technology. *See* Stackhouse, at 18; Dorsey; Cho, at [0009]; Talwar, at [0011]; Vajda, at [0011]. Further, the skilled artisan would have recognized the overlapping objectives of these references, with each seeking to solve a similar technical problem (temperature control and resource consumption) with a similar solution (processor architecture and dynamic resource management). *Compare*, Stackhouse, at 19; Dorsey (addressing temperature control in the processor), *with* Cho, at [0010]; Talwar, at [0018]; Vajda, at [0063] (providing solutions for power and thermal management of the multi-core processor). The compatibility in processor design would provide the skilled artisan yet another motivation to combine these references. *See, e.g.*, Stackhouse, at 28; Dorsey; Cho, at [0035]; Talwar, at [0012]; Vajda, at [0067] (generating different clock signals to the cores of the multi-core processor via PLLs or otherwise conventional technology). Thus motivated, the skilled artisan would have had a reasonable expectation of success in combining Cho, Talwar, or Vajda’s implementation of sets of processor cores into the Itanium or Opteron systems. *See* Exs. 3-5.

The skilled artisan would have identified similar motivations to combine White or Elgebaly with Cho, Talwar, or Vajda, and would have had a reasonable expectation of success in combining the sets of processor cores disclosed by Cho, Talwar, and Vajda into the multi-core processors disclosed by White and Elgebaly. *See, e.g.*, White, at 2:15-67 (disclosing a multi-core processor with independent voltage and clock signals for purposes of power and temperature management), 7:23-45 (disclosing PLLs, at least, for generating the reference clocks); Elgebaly, at [0006]-[0008] (discussing the goal of efficient power consumption in dynamic voltage management); [0028] (disclosing PLLs for generating multiple clock signals). In addition to Cho, Talwar, or Vajda, the skilled artisan would recognize the motivations to combine White or Elgebaly with at least Williams or Gaskins. The skilled artisan would find that the clock frequency generation techniques disclosed in at least Bhandarkar, Williams, and Gaskins would be a routine substitution into the multi-core processor architecture disclosed by White and Elgebaly. *Compare, e.g.*, Bhandarkar, at [0032] (disclosing independent clock frequencies supplied to clock logics for each sets of cores); Williams, at 1, FIG. 1 (disclosing clock generation involving multiple oscillators and PLLs for supplying reference clocks to different domains); Gaskins, at 5:14-6:8, FIG. 2 (disclosing multiple PLLs with independent input clocks to generate separate core source clocks), *with* White, at 7:23-45; Elgebaly, at [0028] (describing similar clock generation techniques via PLLs, oscillators, or other generation techniques). The shared goals between White, Williams, and Gaskins—effective power management—further would motivate the skilled artisan to combine the references. *See, e.g.*, White, at 2:15-67; Elgebaly, at [0006]-[0008]; Bhandarkar, at [0010] (identifying the invention as concerning management of power consumption and heat dissipation); Williams, at 1 (navigating increasing bandwidth demands on multi-core processors); Gaskins, at 6:52-63 (identifying power savings available with modulation of frequency and voltage). The skilled artisan would therefore have a reasonable expectation of success combining the clock generation techniques of Bhandarkar, Williams, and Gaskins into the multi-core processors of White and Elgebaly. *See* Exs. 13, 20, 36.

As another example, the skilled artisan also would have found motivations to combine Jacobowitz 2009 with at least Kruglick or Jorgenson. Each reference has the same technical scope—processor architecture—and each reference addresses the problem of communication between cores within a processor. *See* Jacobowitz 2009, at [0019] (noting the utility in synchronicity between individual cores in a large processing system); Kruglick, at 2:12-30 (highlighting the disclosure of a power management system monitoring voltage to individual cores of a multi-core processor); Jorgenson, at [0025]-[0026] (discussing the need to carry commands throughout a processor system for power and frequency management). The skilled artisan, to the extent they believed Jacobowitz 2009 did not sufficiently provide an interface block configured to facilitate communication between a first and second set of processor cores, would have recognized that Jacobowitz 2009 alludes to processing systems larger than four cores (*see, e.g.*, Jacobowitz 2009, at [Abstract], [0027]), and thus would have looked to references like Kruglick and Jorgenson with larger processor systems for solutions. *E.g.*, Kruglick, at 2:61-3:16, FIG. 1 (disclosing its power management system for an exemplary 16-core processor); Jorgenson, at [0025]-[0026] (disclosing communication to processor peripherals of variable number). The skilled artisan would have found the interface technologies disclosed by Kruglick and Jorgenson to be known in the art, and thus to produce predictable results as applied to Jacobowitz 2009's processor architecture. *See* Kruglick, at 2:61-3:16 (outlining that the power monitor and manager can be any number of known technologies); Jorgenson, at [0030]-[0031] (describing the configuration of generic technologies). The skilled artisan would therefore have a reasonable expectation of success combining the disclosures regarding communication within a processor system from Kruglick or Jorgenson into the multi-core processor of Jacobowitz 2009. *See* Exs. 21, 34.

The skilled artisan would have identified that the technologies disclosed in these prior art references also had been integrated into commercially successful multi-core processors already, giving the artisan a reasonable expectation of success. *See, e.g.*, Xanthopoulos, at 252–55 (referencing Intel Itanium processor); Nawathe, at 18 (referencing the AMD Opteron processor);

Grammatikakis, at 174 (referencing Intel's dynamic voltage and frequency scaling designs). That the references all come from the same field and address the same issues would have encouraged the skilled artisan to combine the methods and techniques disclosed to yield predictable results. The skilled artisan further would have recognized the design incentives and market forces associated with solving the power management problem in conventional multi-core chips as of the priority date (*see, e.g.*, Talwar, [0011]-[0013]) and thus would have looked to combine the charted prior art references to solve the problem.

The *Graham* factors support such combination: the scope and content of the prior art all relate to these same fields; the differences between the prior art and the claimed invention are minimal for this specific element; and the level of ordinary skill in the art would find the combination obvious. The skilled artisan would have had a reasonable expectation of success for such combination for the same reasons discussed above.

Apple anticipates that its technical testifying expert(s) will provide more detailed explanations of motivations to combine, and why a reasonable expectation of success would exist, for each of the items of prior art, alone and in combination. Apple incorporates by reference all expert declarations and reports on motivations to combine that it has submitted or will submit in this case, IPR proceedings, or *ex parte* reexaminations.

Apple is unaware of any secondary considerations of non-obviousness for the Asserted Claims and contends that no such secondary considerations exist. Apple reserves the right to address any alleged secondary considerations of non-obviousness that Redstone may raise.

V. GROUNDS OF INVALIDITY OTHER THAN ANTICIPATION OR OBVIOUSNESS

The Asserted Claims also are invalid for failure to meet one or more of the requirements of 35 U.S.C. §§ 101 or 112. To date, Redstone has not identified any way in which it disputes that the Asserted Claims are invalid under 35 U.S.C. § 112 or patent-eligible under 35 U.S.C. § 101. Redstone also has not sufficiently identified the full scope of its infringement positions or its claim construction theories. Apple reserves the right to argue that the specification does not

enable or provide a written description for such a position or theory, that Redstone's positions or theories render the claim indefinite, or that the Asserted Patent does not claim patentable subject matter. Moreover, Apple's discovery and investigation in connection with this lawsuit is ongoing, and these grounds for invalidity are based on information obtained to date.

These grounds include, but are not limited to: inadequate written description under 35 U.S.C. § 112(a); lack of enablement under 35 U.S.C. § 112(a); and indefiniteness under 35 U.S.C. § 112(b) for the Asserted Claims. Apple may provide more fulsome explanations of its written description, enablement, or indefiniteness defenses in its claim construction briefs and invalidity expert reports, per the Agreed Scheduling Order (ECF No. 25). Apple may amend or supplement these disclosures to include all additional grounds.

A. Lack of Written Description and Lack of Enablement Under 35 U.S.C. § 112

Under 35 U.S.C. § 112, first paragraph, a patent specification:

shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make, and use the same[.]

The Federal Circuit has held that this language creates two closely related, yet separate requirements for a specification: (i) a written description of the invention ("written description") and (ii) a written description of the manner and process of making and using the invention ("enablement"). *See Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1344 (Fed. Cir. 2010) (*en banc*).

To satisfy the written description requirement, the description must "clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed." *Id.* at 1351 (internal citation omitted). The test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date. *Id.*

The test requires an objective inquiry into the four corners of the specification from the perspective of the skilled artisan. Based on that inquiry, the specification must describe an

invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed. “Whether the written description requirement is satisfied is a fact-based inquiry that will depend on the nature of the claimed invention, and the knowledge of one skilled in the art at the time an invention is made and a patent application is filed.” *Carnegie Mellon Univ. v. Hoffmann La Roche Inc.*, 541 F.3d 1115, 1122 (Fed. Cir. 2008) (internal citation omitted). Actual “possession” or reduction to practice outside of the specification is not enough. Instead, the specification itself must demonstrate possession.

Although the written description requirement does not demand any particular form of disclosure, a description that merely renders the invention obvious does not satisfy the requirement. *See Lockwood v. Am. Airlines*, 107 F.3d 1565, 1571-72 (Fed. Cir. 1997).

To satisfy § 112’s enablement requirement, the disclosure “must teach those skilled in the art how to make and use the full scope of the claimed invention without ‘undue experimentation.’” *Genentech, Inc. v. Novo Nordisk, A/S*, 108 F.3d 1361, 1365 (Fed. Cir. 1997) (citations omitted). Moreover, “[i]t is the specification, not the knowledge of one skilled in the art, that must supply the novel aspects of [the] invention in order to constitute adequate enablement.” *Id.* at 1366. The Federal Circuit has enumerated several factors to consider in determining whether a disclosure would require “undue experimentation”: “(1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims.” *In re Wands*, 858 F.2d 731, 737 (Fed. Cir. 1988).

Apple discusses exemplary terms lacking written description or enablement under § 112 below. Certain claim limitations fail to describe an invention understandable to a skilled artisan at the time of the invention or show that the inventor actually possessed the invention claimed. *See Ariad*, 598 F.3d at 1351. Certain claims also are invalid because the specification fails to teach those skilled in the art at the time of the alleged invention how to make and use the full scope of the claimed invention without undue experimentation. *See ALZA Corp. v. Andrx*

Pharms., LLC, 603 F.3d 935, 940 (Fed. Cir. 2010). Certain claim limitations further fail to provide a scope of enablement commensurate with the scope of the claim as asserted. *See Halliburton Oil Well Cementing Co. v. Walker*, 329 U.S. 1, 12-13 (1946); *Amgen Inc. v. Sanofi*, 598 U.S. 594, 610 (2023) (“If a patent claims an entire class of processes, machines, manufactures, or compositions of matter, the patent’s specification must enable a person skilled in the art to make and use the entire class.”).

The Asserted Claims as a whole (rather than only as the sum of its individual limitations) also are invalid for lack of written description and enablement. *See, e.g., Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 F.3d 1336, 1346-51 (Fed. Cir. 2013). By way of example, the skilled artisan at the time of the alleged invention would not have understood that the named inventors of the Asserted Patent possessed the claimed subject matter as of the effective filing date. Nor would the patent’s disclosure have enabled the skilled artisan to practice the Asserted Claims without undue experimentation.

Any deficiencies under § 112 invalidate the related independent claims and all those that depend on them. Based on Apple’s present understanding of the Asserted Claims and Redstone’s apparent interpretation of these claims as reflected in its Infringement Contentions, Apple identifies examples of claim elements of the Asserted Patent that lack written description or that are not enabled below:

- “wherein each processor core from the first/second set of processor cores is configured to dynamically receive a first/second supply voltage and a first/second output clock signal of a first/second phase lock loop (PLL) having a first/second clock signal as input” (claims 1, 21)
- “wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal” (claims 1, 21)
 - For example, the Asserted Patent does not provide written description support for, or enable, a first clock signal and a second clock signal being independent or even different.

- “wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores” (claims 1, 21)
 - For example, the Asserted Patent does not provide written description support for, or enable, using an interface block consisting of a shared cache to facilitate communication between the first and second set of processor cores.
- “wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a periphery of the multi-core processor” (claim 5)
- “wherein the first set of processor cores are located in a first region of the multi-core processor, and the second set of processor cores are located in a second region of the multi-core processor” (claim 8)
- “wherein the first region and the second region are overlapping/non-overlapping regions of the multi-core processor.” (claims 9/10)
- “wherein the first set of processor cores and the second set of processor cores are configured to receive one or more control signals from one or more control blocks located in a common region that is substantially central to the first set of processor cores and the second set of processor cores” (claim 14)

B. Indefiniteness Under 35 U.S.C. § 112

“[A] patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014); *see also Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (quoting *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1377 (Fed. Cir. 2000) (“[F]irst, [the claim] must set forth what ‘the applicant regards as his invention’ and second, it must do so with sufficient particularity and distinctness, i.e., the claim must be sufficiently, ‘definite.’”)) (second alteration in original)).

Exemplary indefinite terms under 35 U.S.C. § 112, second paragraph, appear below.

Any deficiencies that render a claim indefinite invalidate its dependent claims. Based on Apple's present understanding of Redstone's Infringement Contentions, at least one of these claim terms are indefinite because they are inconsistent with or broader than the alleged invention disclosed in the specification and during prosecution. Given Redstone's apparent construction of the claims, the skilled artisan would not understand what is claimed with reasonable certainty.

- “a first/second set of processor cores of the multi-core processor” (claims 1, 8-10, 21)
- “configured to dynamically receive a first/second supply voltage and a first/second output clock signal of a first/second phase lock loop (PLL) having a first/second clock signal as input” (claims 1, 21)
- “wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal” (claims 1, 21)
- “an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores” (claims 1, 21)
- “wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores” (claims 1, 21)
- “one or more control signals from one or more control blocks” (claim 5, 14)
- “located in a periphery of the multi-core processor” (claims 5)
- “located in a first/second region” (claim 8)
- “overlapping/non-overlapping regions” (claims 9/10)
- “located in a common region that is substantially central to the first set of processor cores and the second set of processor cores” (claim 14)

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Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the above and foregoing document has been served via electronic mail to all counsel of record on September 8, 2025.

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