Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems

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Abstract: **Issues associated with the integration of transceiver components on to a single silicon substrate are discussed. In particular, recently proposed receiver and transmitter architectures for high integration are examined on the promise of providing multi-standard capability. In addition, existing barriers to lower power transceiver operation are examined as well as some proposed directions for future integrated transceiver research and development.**

I. Introduction

Explosive growth in the portable communications market has led to consumer demand for low-cost, small-form factor, low-power transceivers[1]. In addition, developers of new wireless applications are looking to provide consumers with both the convenience of added connectivity and the benefit of additional services provided by a transceiver able to operate off of multiple RF standards. The VLSI capabilities of CMOS make this technology particularly well-suited for very high levels of mixed signal radio integration [2][3][4][5][7] while increasing the functionality of a single-chip radio to cover multiple RF standards.

From the perspective of radio performance, most standards outline a set of test conditions which dictate the noise, intermodulation, and blocking performance required of the receiver as well as the power output and the spectral emission profile of the transmitter. Because most single-chip radio solutions attempt to push the channel filtering function to a lower frequency, more aggressive dynamic range requirements are imposed on the Intermediate Frequency (IF) and baseband components than would otherwise be in the discrete component counterpart. Moreover, these increased dynamic range requirements imply the use of power-hungry circuits which run contrary to the goals of portable electronics. However, a closer examination of the required transceiver performance of most standards reveals that high performance is needed only during brief or rare occurrences of a weak received signal in the presence of strong adjacent channel interferer(s).

This paper will focus on radio systems which attempt to integrate all of the transceiver functions onto a single silicon substrate. Section II will briefly review the operation of a conventional super-heterodyne receiver. With an understanding of a traditional discrete-component super-heterodyne receiver, the barriers to integration and potential integrated solutions will be examined. This is followed by an overview of several receiver systems which attempt to address the problems associated with high levels of integration. As an example of a highly integrated receiver, a description of a 0.6um CMOS prototype single chip receiver which meets the specifications of the Digital European Cordless Telephone (DECT) standard is then presented. Although this experimental device was designed for a single standard, much of the radio architecture was developed with the intention of demonstrating multi-standard operation. After looking at receiver systems, section III provides parallel discussions on integration and multi-standard issues related to the transmitter. This is followed in section IV with a brief overview of the existing barriers which prevent low-power operation of radio transceivers and the issues which must be addressed to allow extended battery life for future low-cost highly integrated radio systems.

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II. Radio Architectures & Integration

A. Conventional Superheterodyne Receiver

Most RF communication transceivers manufactured today utilize some variant of the conventional super-heterodyne approach. In this system, shown in Fig. 1, the receiver is implemented with a collection of discrete-component filters and various technologies such as GaAs, silicon bipolar and CMOS.

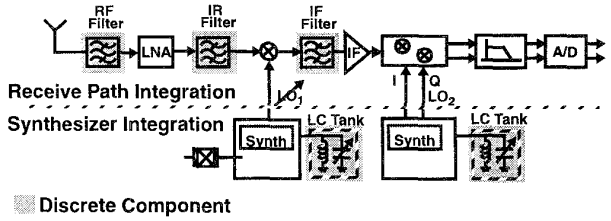

FIGURE 1. Conventional Super-Heterodyne Receiver.

The discrete-component RF front-end filter serves to remove out-of-band energy and perform rejection of image-band signals. The noise or image-rejection filter, which follows the LNA, further attenuates the undesired signals present at the image frequencies. An RF channel-select frequency synthesizer tunes the desired band to a fixed intermediate frequency where a discrete-component filter performs a first order attenuation of out-of-channel energy. High-quality, low phase-noise Voltage Controlled Oscillators (VCO) are typically realized with discrete-component high-Q inductors and varactor diodes.

Both the operation of a super-heterodyne receiver and the superior performance of this radio receiver system may be understood by observing how the signal spectrum is frequency translated and passed through the IF stage. After an initial amplification of the received signals by the LNA, the entire signal spectrum, both wanted and unwanted signal energy, is frequency translated to a fixed IF by a mixer utilizing a Local Oscillator (LO) that tunes to the desired carrier frequency, as illustrated in Fig. 2(a) & (b). At the output of the first mixer, the desired received channel always resides at exactly the same IF frequency. Because the desired carrier at IF is always frequency translated to the same intermediate frequency, an IF filter may now be used to remove signal energy in alternate channels; this is shown in Fig. 2(b). After the IF filter, the desired signal is isolated allowing the use of a variable gain amplifier to adjust the amplitude of

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the desired signal in turn reducing the dynamic range requirements of all subsequent blocks; shown in Fig. 2(c). As described in later sections, the removal of the IF filter within integrated receivers eliminates the possibility of performing a large amplitude adjustment of the desired signal. In addition, the weak desired signal may exist in the

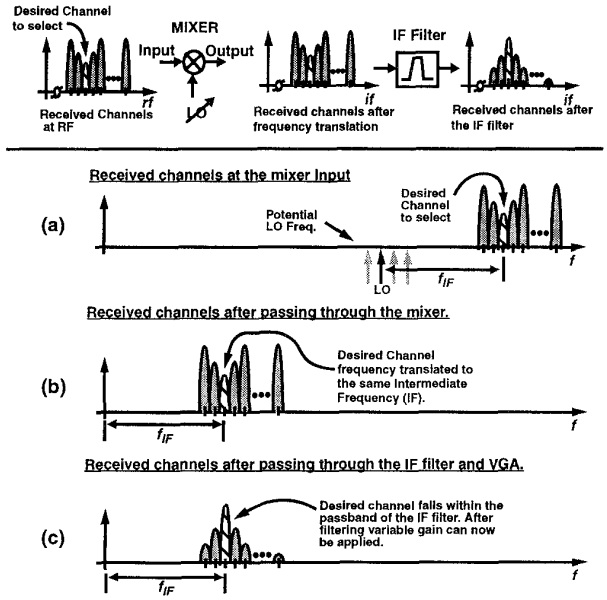

FIGURE 2. Signal Spectrum moving through a super-het.

presence of a large alternate channel signals which again are difficult to attenuate at IF in an integrated solution. For these reasons integrated receivers typically have much larger dynamic range requirements placed on the analog baseband blocks as compared to a discrete super-heterodyne system.

The high-Q associated with the discrete components found on a super-heterodyne receiver is difficult and somewhat impractical to realize at high frequency as an integrated solution. A superior performance with respect to *selectivity*, a measure of a receivers ability to separate the desired band about the carrier from unwanted signals received at other frequencies, and *sensitivity*, the minimal signal at the receiver input such that there is a sufficient signal-to-noise ratio at the receiver output, can only be achieved with the use of high-Q discrete components found on a super-heterodyne receiver. However, using these components run contrary to the goal of high integration required by modern portable communication systems. In addition, the discrete IF filter typically has a frequency response which is specific to the channel bandwidth of an individual application which limits the ability of a super-heterodyne receiver designed for one standard to be reused by other standards.

The challenge of fully integrating a receiver is to replace the functions traditionally implemented by high performance, high-Q discrete components with integrated on-chip solutions. Problems associated with full integration of the receiver can be separated into two categories. First, the integration of the receive signal path requires the elimination of the noise or image-rejection filter and the discrete-component IF filter (Fig. 1). Second, an integrated low-phase noise channel-select synthesizer must be realized using the relatively low-Q on-chip VCOs with associated poor phase-noise performance. Three receiver architectures which attempt to integrate much of the functionality of a discrete component receiver will now be evaluated for the promise of integration and providing multi-mode/multi-standard operation.

B. Direct Conversion Receiver (Homodyne)

One receiver architecture that eliminates many off-chip components in the receive signal path is the direct conversion, or homodyne architecture[2]. In this approach, shown in Fig. 3, all of the potential in-band channels are frequency translated from the carrier directly to baseband using a single mixer stage. Energy from undesired channels is removed with on-chip filtering at baseband. In a direct conversion receiver, the IF stage is eliminated as is the need for image-rejection filtering.

In a homodyne receiver, all of the channels are frequency translated to baseband before any channel filtering is performed. This allows the possibility of on-chip programmable filter structures to accommodate the variable channel bandwidth in turn facilitating multi-mode or multi-standard operation.

Although the direct conversion receiver allows for higher levels of integration than a super-heterodyne system, there are problems associated with this architecture. Because the local oscillator is at the same frequency as the RF carrier, the potential exists for LO leakage to either the mixer input or to the antenna where radiation may occur. The unintentionally transmitted LO signal may reflect off nearby objects and be "re-received" consequently self-mixing with the local oscillator resulting in a time-varying or "wandering" DC offset at the output of the mixer. This time varying DC offset, together with inherent baseband circuit offsets as well as DC components arising from second order intermodulation and 1/f noise, significantly reduces the dynamic range of the receiver. In addition, a direct conversion receiver requires a high-frequency, low phase-noise, channel-select frequency synthesizer, which is difficult to achieve with a relatively low-Q integrated VCO.

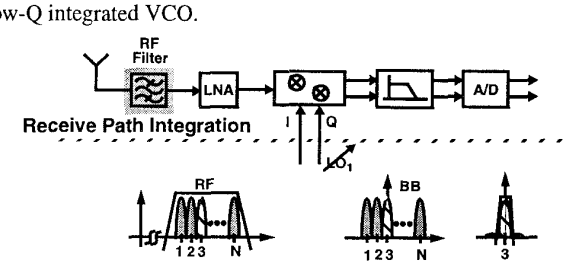

FIGURE 3. Direct Conversion Architecture.

C. Low-IF single conversion

One integrated receiver architecture which alleviates many of the DC offset problems that plague direct conversion receivers is the Low-IF receiver architecture[3], shown in Fig. 4. Similar to direct conversion, a single mixer stage is used to frequency translate all of the desired channels to a low intermediate frequency; this IF is typically on the order of one or two channel bandwidths. Here, the signal is passed through an ADC where a digital multiplication may be performed before the channels are recombined to implement an image-rejection function. The primary advantage of a low-IF system is that the desired channel is offset from DC. Therefore, the typical problems arising from DC offsets found in direct-conversion receivers may be bypassed.

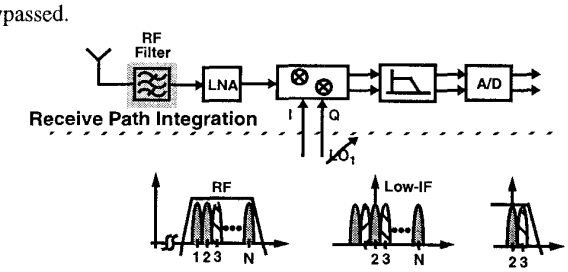

FIGURE 4. Low-IF Receiver System.

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In the Low-IF receiver some method of image-rejection must be performed because the desired carrier is down-converted to a low-IF. This is accomplished by using some variant of an image-rejection mixer. Because the IF is on the order of the channel bandwidth, all of the imageband attenuation must be performed by an on-chip image-rejection mixer where the image rejection is limited by matching considerations to about 40dB. In addition, alternate channel blockers are folded in closer to the desired carrier by twice the IF frequency making filtering of out-of-channel energy even more difficult. Moreover, if an ADC is used, the required performance with respect to bandwidth and resolution becomes difficult for multi-standard operation.

D. Wideband IF with Double Conversion.

An alternative architecture well suited for integration of the entire receiver is wide-band IF with double conversion [5]. Shown in Fig. 5, this receiver system takes all of the potential channels and frequency translates them from RF to IF using a mixer with a fixed frequency local oscillator(LO1). A simple low-pass filter is used at IF to remove any upconverted frequency components, allowing all channels to pass to the second stage of mixers. All of the channels at IF, are then frequency translated directly to baseband using a tunable, channel-select frequency synthesizer(LO2). Alternate channel energy is then removed with a baseband filtering network where variable gain may be provided.

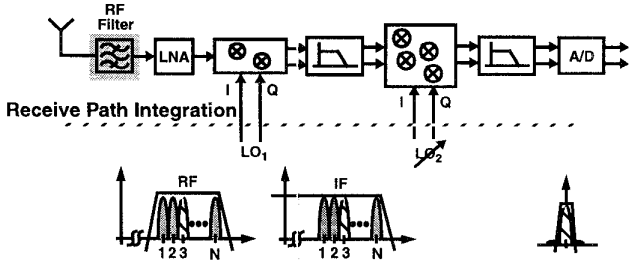

FIGURE 5. Wide-band IF with Double Conversion.

This approach is similar to a superheterodyne receiver architecture in that the frequency translation is accomplished in multiple steps. However, unlike a conventional superheterodyne receiver, the first local oscillator frequency translates all of the received channels, maintaining a large bandwidth signal at IF. The channel selection is then realized with the lower frequency tunable second LO. As in the case of direct conversion, channel filtering can be performed at baseband, where digitally-programmable filter implementations can potentially enable more multi-standard capable receiver features.

The wide-band IF architecture offers two potential advantages with respect to integrating the frequency synthesizer over a direct conversion approach. The foremost advantage is the fact that the channel tuning is performed using the second lower-frequency, or IF, local oscillator and not the first, or RF, synthesizer. Consequently, the RF local oscillator can be implemented as a fixed-frequency crystal-controlled oscillator, and can be realized by several techniques which allow the realization of low phase noise in the local oscillator output with low-Q on-chip components. One such approach is the use of wide phase-locked loop (PLL) bandwidth in the synthesizer to suppress the VCO contribution to phase noise near the carrier. This concept is illustrated in Fig. 6, where the noise transfer functions are given for the VCO, divider, and phase detector (PD) to the synthesizer output. Note that the VCO phase noise transfer function has a high-pass transfer function close in to the carrier and the bandwidth of suppression is related to the PLL loop bandwidth.

In addition, since channel tuning is performed by the IF local oscillator, operating at a lower frequency, a reduction in the required divider ratio of the phase-locked loop necessary to perform channel selection results. The noise generated by the reference oscillator, phase detector and

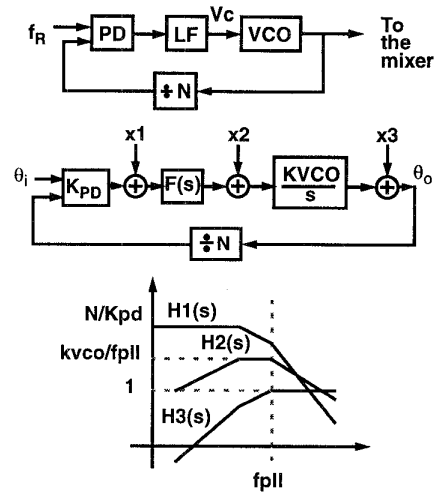

FIGURE 6. PLL and the component noise transfer functions about the carrier.

divider circuits of a PLL all contribute to the phase noise performance of a frequency synthesizer. With a lower divider ratio, the contribution to the frequency synthesizer output phase noise from the reference oscillator, phase detector and divider circuits can be significantly reduced. Moreover, a lower divider ratio implies a reduction in spurious tones generated by the PLL.

An additional advantage associated with the wide-band IF architecture is that there are no local oscillators operating at the same frequency as the incoming RF carrier. This eliminates the potential for the LO re-radiation problem that results in *time-varying* DC offsets. Although the second local oscillator is at the same frequency as the IF desired carrier in the wide-band IF system, the offset which results at baseband from self mixing is relatively constant and is easily cancelled.

The Wideband IF receiver realizes an image-rejection function with the use of six mixers, similar to the Weaver method [6]. The frequency translation is performed by retaining only one of the two sidebands about LO1. The edge of the image-rejection band is set by the frequency of LO1 allowing the flexibility of tuning LO1 to perform band selection among different standards. The polarity of the mixer configuration can be reversed at baseband to reject the alternate sideband about LO1 in turn providing further flexibility for multi-standard operation. This concept is further developed in [5] and recently demonstrated in [7]. Similar to a direct conversion receiver, all of the channel filtering is performed at baseband, facilitating the implementation of programmable filter structures for multi-standard applications.

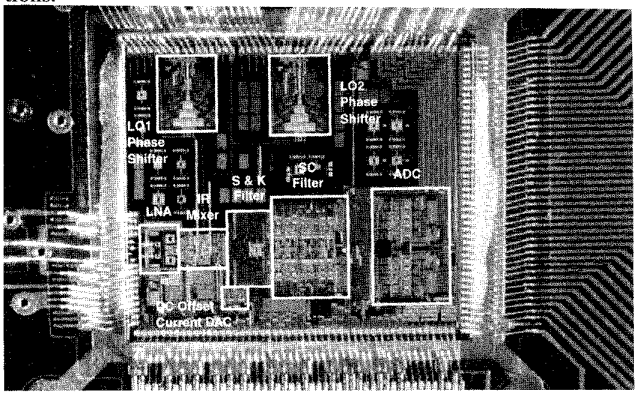

FIGURE 7. DECT prototype chip shown attached directly to the testboard using COB.

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A prototype device was fabricated based on the wideband IF architecture. The chip was realized in a 0.6μm double poly CMOS process and utilized a 3.3v supply. The receiver which was designed to meet the specifications of the DECT standard has a measured reference sensitivity of -90dBm, dissipates 198mW, and has a input referred 3rd order intermodulation intercept point of -7dBm. The chip, shown assembled in Fig. 7 with testboard using chip-on-board wirebonding, is 7.5mm by 6.5mm.

III. Transmitter

Transmitters perform three primary functions; modulation, frequency translation and power amplification. Consequently, the key performance specifications are modulation accuracy, spectral emission and output power level. Transmitter architectures can be divided into two main categories: mixer based frequency translation and PLL based frequency translation. The first approach employs an I/Q modulator and uses mixers to perform the necessary up-conversion, while the second uses an I/Q modulator and PLL to perform frequency translation. A discussion of the two architectures will follow with emphasis on the potential for integration, low power operation and multi-standard capability.

A. Mixer Based Transmitters

A two step or indirect up-conversion transmitter[12] is shown in Fig. 8. The digital data first passes through a Digital to Analog Converter (DAC) and is then filtered to suppress distortion introduced by the DAC. Frequency translation to a fixed IF is then performed by the I/Q mixers after which the signal is summed. The signal then passes through an off chip lowpass filter to suppress LO2 harmonics which may violate the spectral mask requirements and cause distortion in the PA. Unlike the receiver, the requirements of the IF filter are substan-

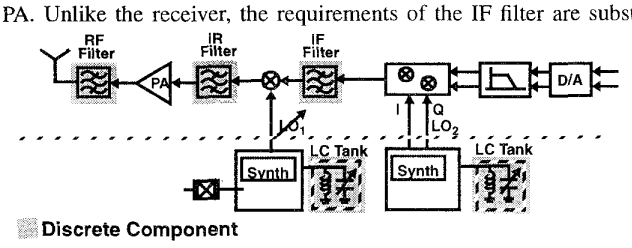

FIGURE 8. Conventional Two-Step Transmit Path.

tially relaxed as no close-in, large blocking signals are present. The signal is then frequency translated to RF by a mixer and an RF channel select frequency synthesizer. A discrete RF bandpass filter attenuates the image created by the second mixer and filters any additional spurs which may violate the spectral mask requirements. The desired output power level is achieved by providing gain with a discrete Power Amplifier (PA). Finally, a discrete bandpass filter removes energy transmitted outside of the desired band. As previously mentioned in the receiver section, the VCOs for both LO1 and LO2 are typically realized with high-Q discrete components which are able to produce a low-phase noise oscillator.

The role of each discrete component will now be examined with respect to the possibility of complete integration. The IF filtering requirements can be relaxed if the intermediate frequency is selected such that none of the LO2 harmonics fall directly in the transmit or receive band where emission specification are usually the most stringent. Furthermore, increasing the IF will push the image band further away from the desired signal allowing more image rejection by the RF filters. Finally, a differential signal path can suppress the even-order harmonics, further relaxing the filtering requirements. Moreover, the IF filter may be eliminated all together with a direct up-conversion transmitter as shown in Fig. 9.

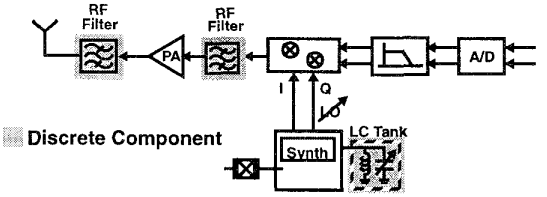

FIGURE 9. Conventional Direct Conversion Transmit Path.

The single step or direct conversion transmitter uses an I/Q modulator and performs frequency translation in one step[14]. Since no IF exists, an IF filter is not required in this architecture. Moreover, this architecture eliminates the need for any image rejection as there are no image signals created by a single step frequency translation. This further lowers the requirements of the bandpass filter before the PA which reduces unwanted harmonics and noise from the up-conversion process. The inclusion of this filter may allow a lower performance RF filter, which attenuates all energy outside of the transmit band to be used. If, however, the bandpass filter before the PA is removed to achieve higher integration, a higher performance RF filter may be required after the PA. This requirement may lead to a larger insertion loss through the RF filter and reduces the effective efficiency of the PA by lowering the output power at the antenna for a given input power. Thus a trade-off exists between integration and power consumption. The bandpass filter before the PA may be integrated, but the performance of on-chip RF bandpass filters is limited by the low Q components. Therefore, because more filtering is required by the RF frontend filter after the PA, power consumption increases. Minimizing the spurious tones and noise created by the up-conversion process is therefore necessary to reduce power consumption. A possible solution is the Phase Locked Loop based transmitter, which will be discussed in the next section.

Another barrier to integration in a single-step transmitter is LO or VCO pulling. The output of the modulator and the PA as well as the local oscillator all run at the same frequency, namely the RF frequency. As a result, the output of the local oscillator may be "pulled," by the large signal emitted from the PA. This has the effect of modulating (or altering) the VCO frequency. Without exceptional isolation between the PA and VCO, integration of the PA with the VCO in a single-step transmitter may be difficult to achieve. However, this problem may be eliminated in single-step transmitters with the use of an offset mixing scheme, in which two local oscillators LO1 and LO2 (similar to the LO1 and LO2 of the two-step case) are first mixed to generate the desired RF channel-select local oscillator[13]. This LO is then mixed with the baseband data signal to generate the RF data signal. This method avoids the VCO pulling problem of single-step architectures, as neither VCO is operating at the RF carrier frequency.

Both direct and indirect up-conversion transmitters hold promise for multi-standard operation. With proper selection of the UHF synthesizer frequency both the GSM and DCS1800 bands could be supported with the lower and upper mixing products of LO1 and LO2, respectively. In addition, both transmitters can operate with constant and non-constant envelope modulation schemes.

B. Phase Locked Loop Transmitters

One method of reducing the filtering requirements in the transmit path is to use the filtering inherent in a Phase Locked Loop (PLL) in order to reduce the harmonics and noise generated in the frequency translation process [15][16]. A typical PLL based transmitter is shown in Fig. 10. Like the two step transmitter, a quadrature modulator translates the baseband signal to a fixed IF, after which the IF signal is translated to RF by the PLL. The transmitter PLL is similar to the pre-

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example of a condition which leads to very high dynamic range requirements in the backend of integrated radio receivers; this is illustrated in Fig. 12. Higher required dynamic range in both the baseband filters

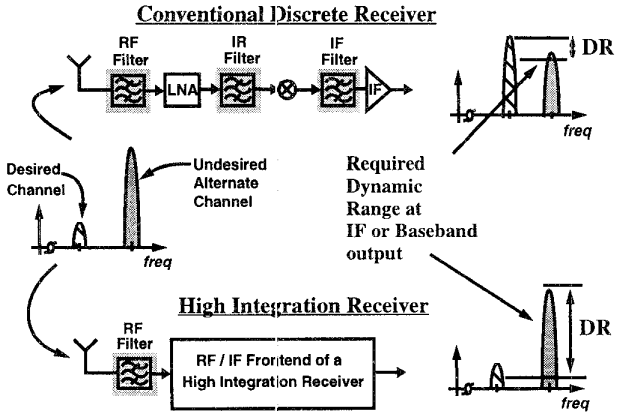

FIGURE 12. Effect of blockers on dynamic range in both discrete and integrated receivers.

and/or ADC typically implies a higher receiver power consumption. The condition of an adjacent channel blocker may only occur during very brief intervals of the receiver's operation time. However, currently integrated radios are designed to handle high dynamic range conditions of an alternate channel blockers at all times, as shown in Fig. 12. A more optimal approach to handling the high dynamic range required of integrated baseband components may rest in developing transceiver systems which sense when a strong alternate channel condition exists. This would allow the receiver to fall back to a low-power, low-performance mode when high performance was not required. Then, when a strong alternate channel signal arises, the receiver would increase the dynamic range in the back-end to meet the particular condition present. Again, by monitoring the presence of the blocker, the receiver could then return to a low performance, optimal power consumption mode of operation when the blocker disappears. A parallel strategy may be applied to optimize the frequency synthesizer power consumption verses the required phase noise performance which again would be determined by the blocking condition which is sensed by an intelligent receiver system. This concept could potentially be extended to optimize the receiver power consumption versus noise figure and required sensitivity for a given received signal strength.

V. Conclusion

This paper has provided a survey of high-integration transceiver systems which hold the promise of multi-standard operation. Although several academic publications have demonstrated the ability of high-integration CMOS systems to meet the performance requirements of various standards/applications, research is still required to make commercial integrated CMOS single-chip transceiver solutions a reality in production. These will mainly come through research and development in the following areas.

- Further improvement of on-chip inductors, filters and oscillators in a standard CMOS process.
- Development of single-chip transceiver systems which provide intelligent power optimized transceiver systems.
- Continued improvement in high frequency CMOS device modeling and simulation.

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viously mentioned frequency synthesizer PLL, except the reference frequency is replaced by the IF signal and the dividers are replaced by a down-conversion mixer. In the phase detector, the IF signal is compared with the downconverted version of the RF signal, which is created by the downconversion mixer in the feedback path. The phase detector is followed by a charge pump and a discrete loop filter before the transmit VCO is reached. The discrete VCO then feeds the PA directly. An RF filter is not necessary because noise and distortion introduced by the quadrature modulator and frequency synthesizers are filtered by the bandpass action of the PLL. Significant power savings can occur because the RF filter loss is removed. Depending on the specification, filters may be needed after the quadrature modulator and after the feedback mixer.

Full integration of a PLL based transmitter will minimize power advantages. The power savings occur because a high performance, discrete VCO can be designed to transmit very little unwanted energy. An integrated VCO could not achieve this performance, thus requiring a front end RF filter. Once again integration and low-power are conflicting requirements.

PLL based transmitters are inherently limited with regards to multi-standard operation because such transmitters only operate with constant envelope modulation schemes. However, multi-band operation has been shown for the GSM and PCS bands [16].

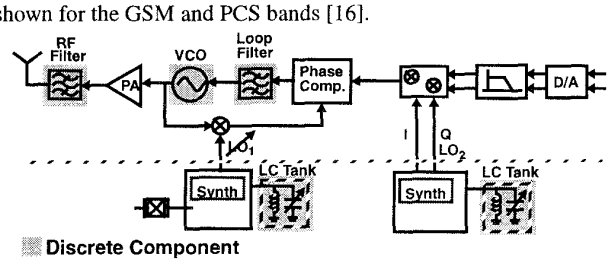

FIGURE 10. Direct Modulation Transmit Path.

IV. Low Power Considerations

The proposed integrated transceiver systems suggested to date all hold the promise of highly integrated solutions with potentially the same performance as a discrete component system[2][3][5]. However, a fundamental drawback still arises with respect to high performance with low-power operation. The barriers to transceiver low-power operation can be separated into issues related to the transmitter and receiver.

For most commercial portable transceivers the dominant source of power consumption is the power amplifier used in the transmitter. Currently, attempts have been made to increase the overall power added efficiency of the power amplifier by using non-linear power amplifier configurations. However, the use of these amplifiers has been limited to standards which utilize constant envelope modulation schemes. To allow non-constant envelope modulation, future transmitter systems will seek to compensate for the non-linearities associated with high efficiency power amplifiers [17][18]. In addition, most power amplifiers are designed to have maximum power added efficiency only when operating at the maximum output power. However, under normal operating conditions, the power amplifier typically emits an output power far below the maximum power level. Thus, under normal operation, the power efficiency is suboptimal. One approach to improving the PA power efficiency over a broader range of output power is to use a power amplifier in conjunction with a DC-DC converter as shown in Fig. 11(a). Since the DC-DC converter provides a power level control mechanism, a high efficiency switch-mode PA can be used such as Class D, E, and F, the concept of which is shown in Fig. 11(b). One recent implementation of a CMOS Class E PA is given in [19]. This power amplifier was designed in a 0.35μm standard CMOS process and achieves a power added efficiency of 48% at 1.9 GHz for a broad range of output power levels.

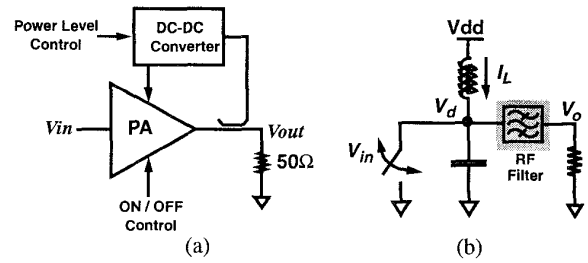

FIGURE 11. (a) Block level concept of high efficiency PA configuration (b) Simplified representation of a switch-mode PA.

A closer examination of the dominant source of power consumption in a receiver reveals that in the receive path of an integrated receiver, all of the high-Q filtering has been removed as compared to the discrete component counterpart. Therefore, all of the receiver systems suggested thus far suffer from a fundamental problem of having to provide the capability to handle large alternate channel blockers or out-of-band blockers while attempting to recover a weak desired carrier. Without the benefit of a super-heterodyne receiver's high-Q filtering at IF, all of the subsequent components in the receiver path must provide the capability of handling both a large undesired signal while attempting to recover a relatively weak desired signal. This implies that backend receiver components must have a high dynamic range. In addition, without filtering before the baseband blocks, intermodulation of alternate channel bands places a higher linearity requirement on all of the IF and baseband blocks.

To address the divergent requirements of a high performance, high integration and low-power, future transceivers will in all likelihood require a combination of approaches to reduce the dynamic range requirements and power consumption of the receiver. First, the development of high-Q on-chip inductors and capacitors are essential to realize integrated, high-frequency, high-Q image-reject and channel filters as well as low-phase noise integrated VCOs. To date, progress in realizing high-Q components has been achieved at the expense of modifying a standard silicon process. Silicon micro-machining is one such approach which utilizes existing CMOS processes with minor modifications to synthesize on-chip high frequency filters and resonant components [20][21]. Alternatively, methods have been suggested which seek to improve the Q of on-chip inductors by either vastly increasing the substrate sheet resistance [23] which inturn reduces the induced eddy currents resulting in higher Qs or in combination with a lower inductor series resistance [22]. However, with the modification or additional processing steps added to conventional silicon processes both the cost and complexity also rise.

A yet unexplored area where a reduction in the receiver power consumption may lie in the exploitation of high integration CMOS transceivers. By rethinking the transceiver as a "system-on-a-chip," radio architectures may be developed to optimize power consumption for needed performance. Most radio standards or applications outline a set of test conditions which specify the required performance of both the transmitter and receiver. A closer examination of the standards reveals that typically, high performance in terms of linearity, noise figure and dynamic range are only required during brief intervals. However, contemporary receivers and transmitters found in products are typically over-designed to meet the most difficult performance requirements even when not required. This results in higher power consumption than is really necessary. Receiving a weak desired signal in the presence of a strong alternate channel signal is an excellent

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