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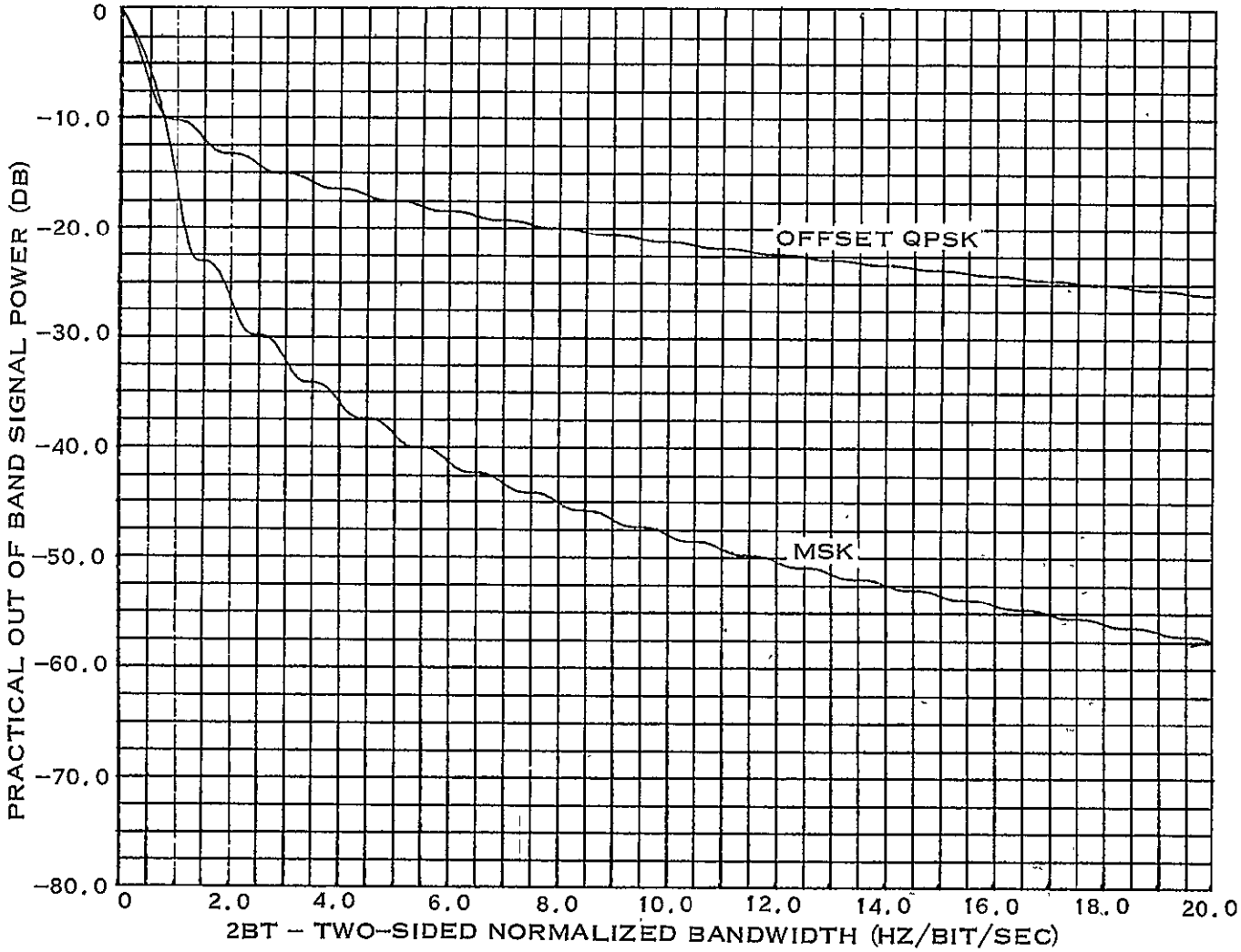

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Figure 2-15. Fractional Out-of-Band Power (Normalized Two-Sided Bandwidth = 2BT)

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where

$E_s(C^2)$ = the mean square crosstalk

A = relative peak amplitude of interfering signal

$k = \Delta f/R = 1,2,3, \ldots$

R = the bit rate

Δf = the frequency displacement from an adjacent channel center frequency.

For $k \gg 1$, the mean-square crosstalk decreases at a rate proportional to $1/k^4$ or 40 dB/decade. This is the same rate of decrease as the out-of-band power. A plot of Equation (2-39), in decibels and normalized, is shown in Figure 2-16. Note that from k = 1 to k = 2, the crosstalk decreases 12 dB; also note that the mean-square crosstalk level at k = 2 is approximately 40 dB below the peak signal amplitude. Equation (2-39) does not, however, relate the crosstalk to signal-to-noise degradation.

White[14] has considered the worst case crosstalk problem for MSK. His formula for the worst case crosstalk ratio for MSK is:

$$C_{MAX} = \frac{A}{4\pi(k^2 - 0.25)} \tag{2-40}$$

White has also computed the signal-to-noise ratio loss as a function of the relative power of the unfiltered interference signal for various center frequency separations. This information is reproduced in Figure 2-17. A comparison with BPSK is given by the dashed lines. It is obvious that MSK provides significant reduction in crosstalk. Note that an interfering signal 25 dB greater than the desired signal causes a 3-dB degradation in S/N for MSK while an interfering signal only 3 dB greater in amplitude can cause a 3-dB degradation in S/N for BPSK. A comparison of crosstalk for various modulation methods is given in Table 2-1. This table shows the minimum permissible frequency separation (in terms of bit rate) for a worst case S/N ratio degradation of 1 dB from an interfering signal. The level of the interference signal is relative to the level of desired signal. Note that MSK has the smallest separation requirements for any condition while BPSK has the largest. Also note that *no* channel filter is assumed for these data. Obviously, a receiver filter will improve all schemes, but MSK should still provide the least relative crosstalk. In particular, it would appear that a channel BW of 2R and a channel separation of 2R would provide a dynamic range of at least 23 dB.

2.5 PREMODULATION DATA ENCODING AND POSTDETECTION DECODING

The only baseband data code discussed so far has been NRZ-L. In addition to NRZ-L data, two differentially encoded forms of NRZ are possible. These are NRZ-M (NRZ-mark) and NRZ-S (NRZ-space). NRZ-M is produced by differentially encoding a data bit with the previous symbol to produce a new symbol:

$$S_n = D_n \oplus S_{n-1} \tag{2-41}$$

for NRZ-M data. A similar equation is valid for NRZ-S, with the data being complemented:

[14] White.

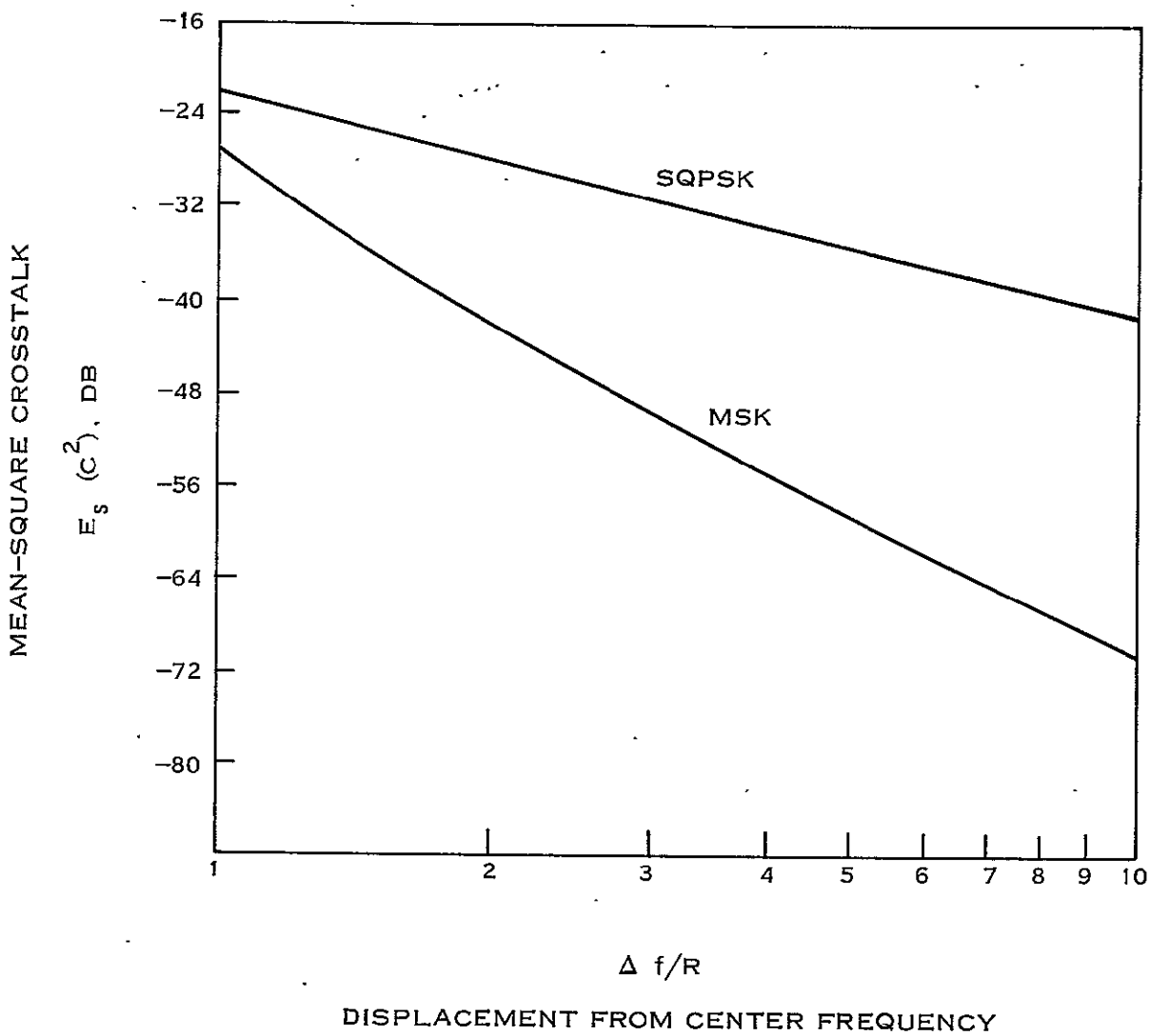

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Figure 2-16. Mean-Square Crosstalk as a Function of Displacement of Channel Carrier (Unfiltered)

$$S_n = \overline{D}_n \oplus S_{n-1} \tag{2-42}$$

where

D_n = NRZ-L data

S_n = the NRZ-M or NRZ-S symbols

and n has a duration of T. These codes have the advantage that the NRZ-M or NRZ-S symbol data stream can be inverted, yet the correct data polarity is produced when decoded:

$$D_n = S_n \oplus S_{n-1}$$

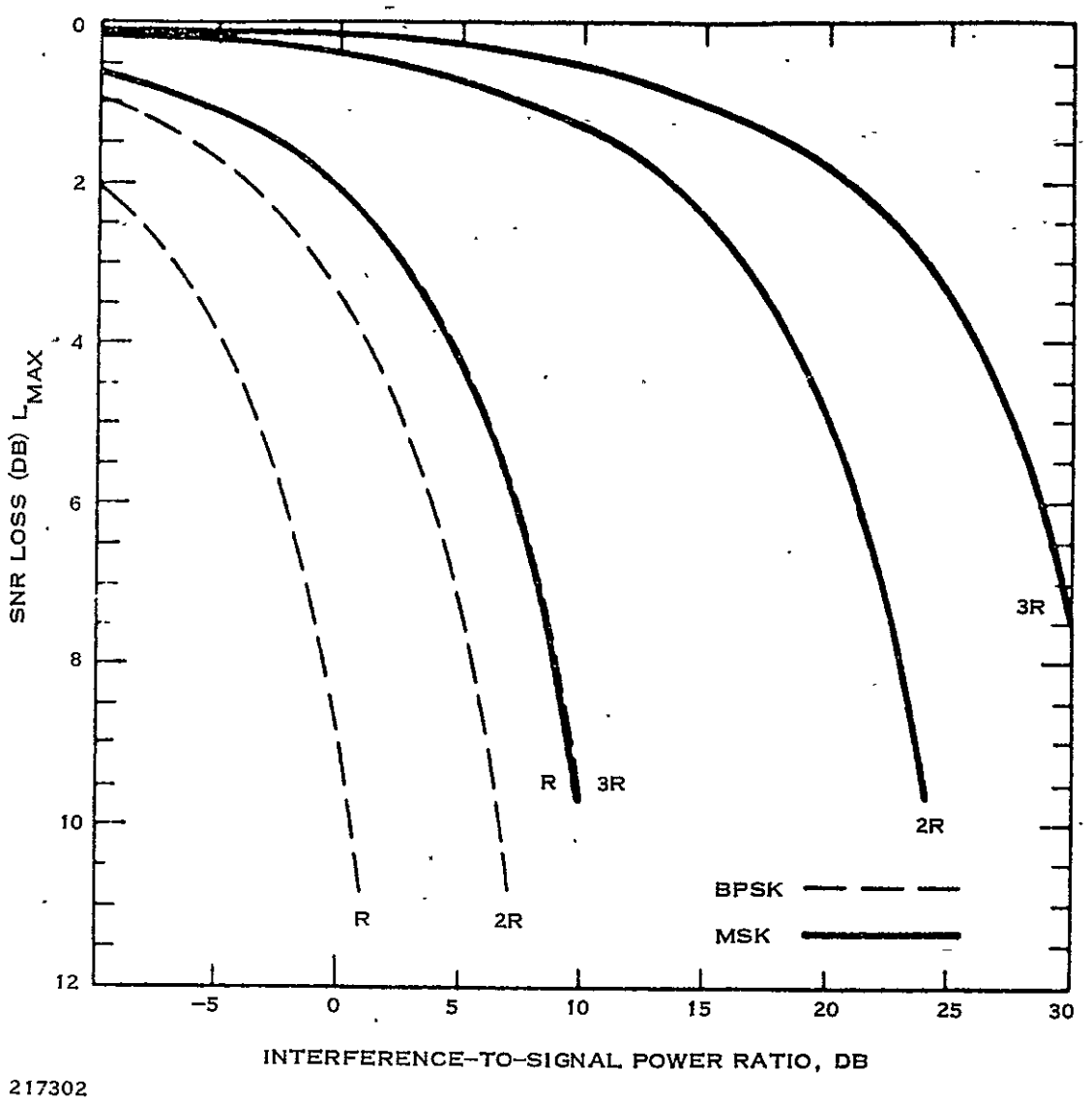

Figure 2-17. S/N Ratio Loss Caused By Interference From an Adjacent Signal as a Function of Separation and Relative Level (dB) for MSK and BPSK

$$D_n = S_n \oplus S_{n-1}$$

or (2-43)

$$D_n = \overline{S}_n \oplus S_{n-1}$$

Figure 2-18 shows the relationship of various baseband codes. The three versions of NRZ are shown at the top. Return-to-zero (RZ), three versions of biphase (BI-ϕ), and three versions of the delay code are also shown. RZ data is characterized by representing a one as a pulse and a zero as the absence of a pulse. The width of the pulse can be any value equal to or less than 1/2 bit time, with 1/2T width being typical. The case for RZ with a 1/2T pulsewidth is easily implemented by simply ANDing the data with the clock:

$$S_n = D_n \cdot C_n \tag{2-44}$$

TABLE 2-1. MINIMAL PERMISSIBLE CENTER FREQUENCY SEPARATION (Hz) FOR APPROXIMATE WORST CASE CROSSTALK AND AN S/N RATIO LOSS OF 1 dB OR LESS FROM INTERFERING WAVEFORM

	Interference Level, A^2 (dB)			
Modulation	0 (R)	10 (R)	20 (R)	30 (R)
BPSK	6	19	59	186
SQPSK, AQPSK	5	14	42	131
QPSK	4.5	13.5	41.5	131
MSK	1.5	2.5	4	7
CPQFSK	1.75	3	5	8.75
Bi-orthogonal FSK	3.25	9.75	29.75	93.25

R is the information rate.

where

S_n = the RZ symbol output

D_n = the input data

C_n = the data clock.

Although Figure 2-18 shows direct implementation of Equation (2-44), a quadrature-phase clock is preferred. A 90-degree phase-shifted clock prevents the generation of any glitches and places the data pulse in the center of a bit cell; this latter case makes data detection easy.

A schematic of the encoder/decoder circuitry for NRZ-M data is shown in Figure 2-19. Note that the same circuitry can be used for NRZ-S; the $\overline{Q}$ (complemented) data is substituted at the input to the exclusive-OR gate. A schematic of an NRZ encoder/decoder is shown in Figure 2-20.

All forms of NRZ data have the disadvantage of potentially long periods without a transition. Since the coherent demodulator for MSK must extract the mark and space reference frequencies, long periods without a sample of one can introduce significant phase errors in the recovered carriers. Therefore, another code which guarantees more numerous transitions is desirable. One such baseband data code group is the biphase group. There are three basic versions of this code; these are shown in Figure 2-18.

The first is biphase L which is also called Manchester. This baseband code is easily generated by modulo-2 adding the NRZ-L data with the clock. This guarantees a transition in the data at least once per bit interval. Biphase L data is characterized by a one being represented as a positive data transition in the center of the bit cell while a zero is represented as a negative transition in the center of the bit cell. The mathematical coding is:

$$S_n = D_n \oplus C_n \tag{2-45}$$

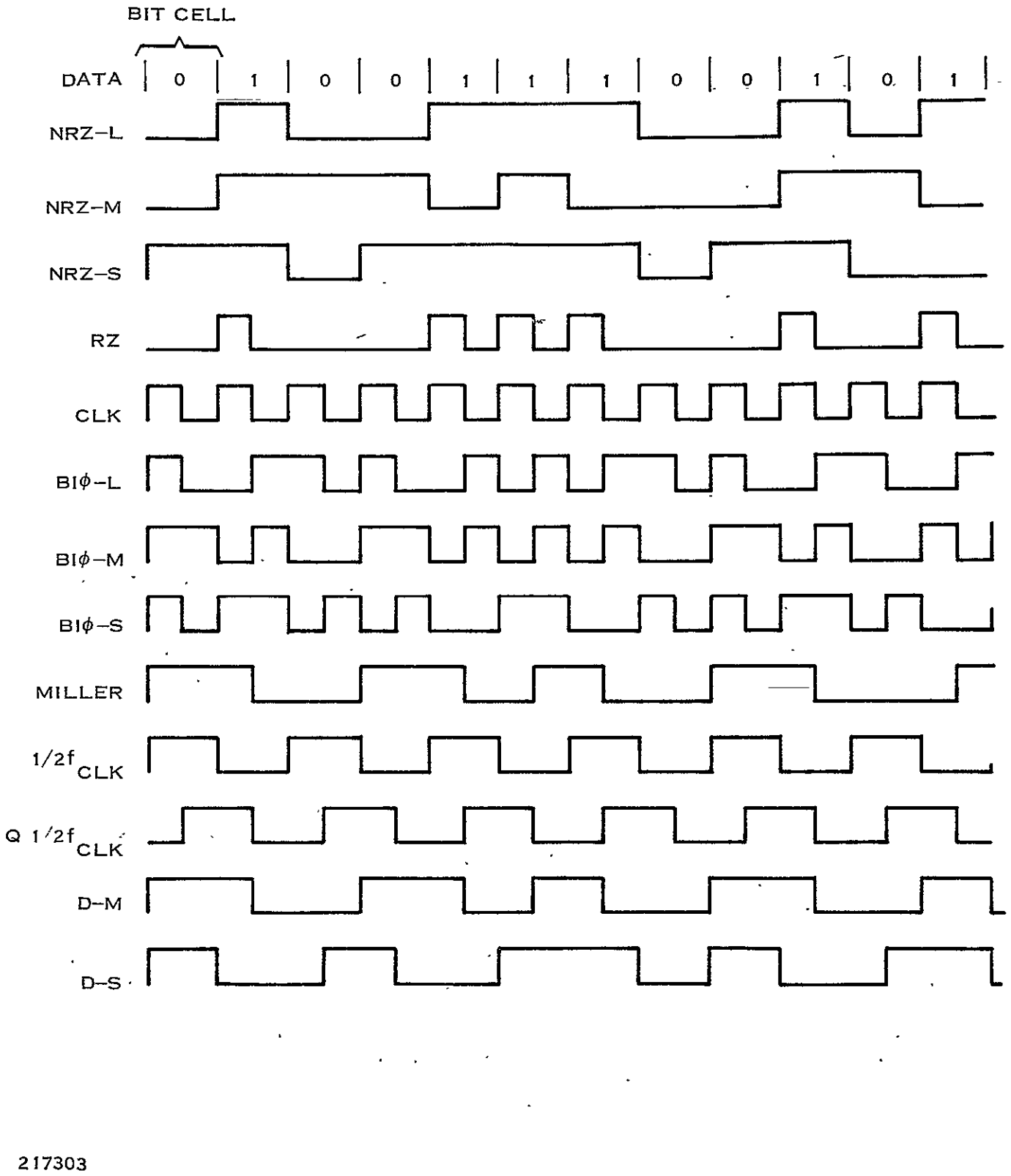

Figure 2-18. Various Data Codes for Baseband Use

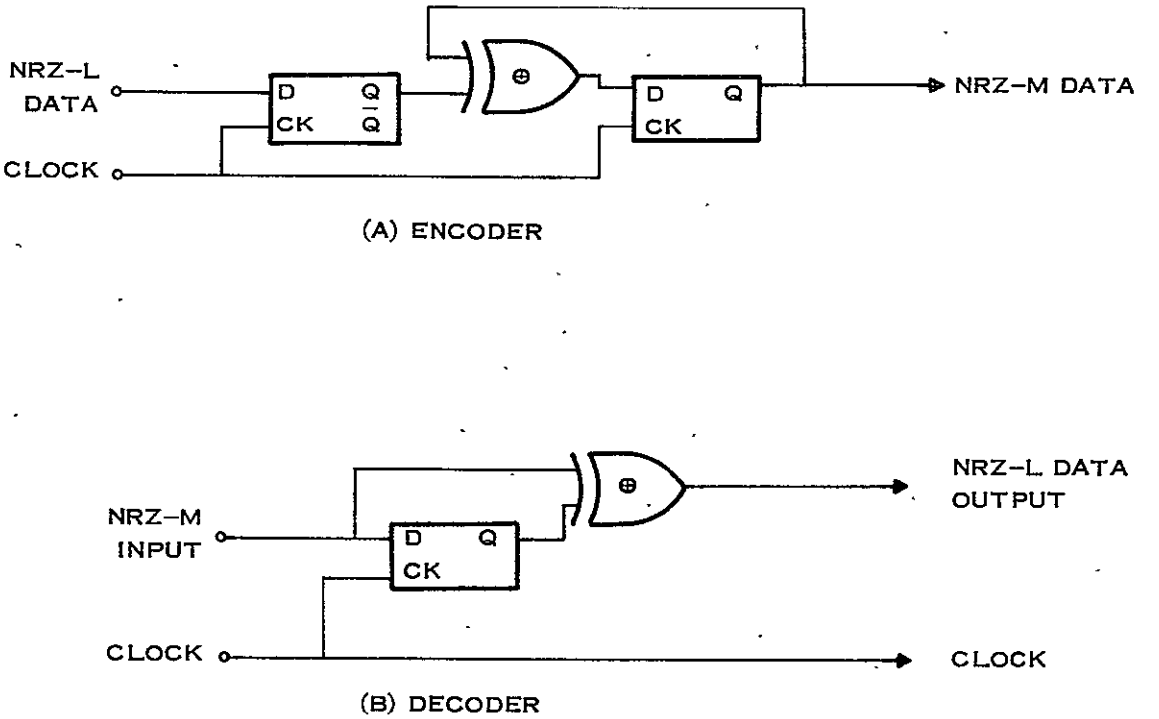

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Figure 2-19. Schematic of Encoder/Decoder for NRZ-M Data

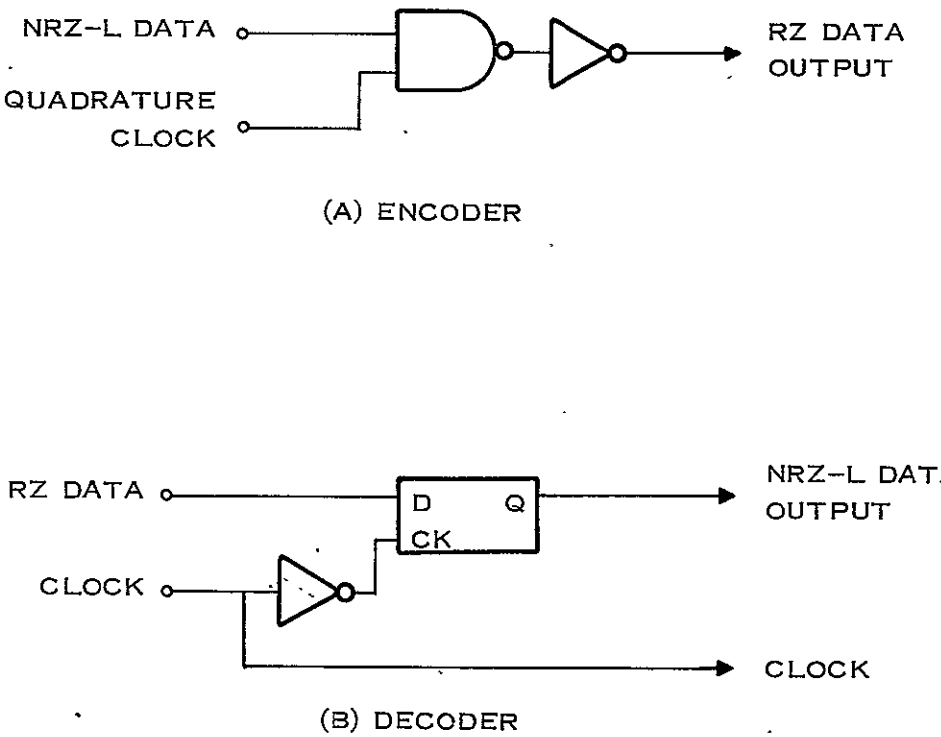

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Figure 2-20. Schematic of RZ Encoder/Decoder

where

S_n = the Manchester data output symbol

D_n = the NRZ-L input data

C_n = the clock

and n has a duration of 1/2T in this case. Decoding is simply:

$$D_n = S_n \oplus C_n$$

The other two forms of biphase coding, biphase M and biphase S, are the mark and space counterparts of NRZ-M and NRZ-S. Biphase M was originally defined as: A 'one' is represented by a frequency equal to the clock frequency while a 'zero' is represented by a frequency equal to one-half the clock frequency." Biphase S was similarly defined except the input data was inverted. However, the biphase M and S data can be generated from differentially encoded NRZ data, i.e., from NRZ-S and NRZ-M, respectively.

Let P_n represent the biphase S data symbol, C_n represent the clock, D_n represent the NRZ-L data, and S_n represent the NRZ-M data over time interval N where N has a period of 1/2T. Then from Equation (2-41):

$$S_n = D_n \oplus S_{n-2}$$

and (2-46)

$$S_{n-1} = D_{n-1} \oplus S_{n-3}$$

Now, it can be shown that:

$$\overline{P}_n = S_{n-1} \oplus C_{n-1} \tag{2-47}$$

The same equation can be used to represent biphase M data, if D_{n-1} in Equation (2-46) is complemented so as to generate NRZ-S data. Therefore, biphase M and biphase S data are generated by the same process used to generate Manchester data except that, in these cases, NRZ-S and NRZ-M rather than NRZ-L are used as an input to the exclusive-OR gate.

Decoding is done by the following manipulations:

$$\begin{aligned}
\overline{P}_n \oplus \overline{P}_{n-2} &= (S_{n-1} \oplus C_{n-1}) \oplus (S_{n-3} \oplus C_{n-3}) \\
&= (S_{n-1} \oplus S_{n-3}) \oplus (C_{n-1} \oplus C_{n-3}) \\
&= (S_{n-1} \oplus S_{n-3}) \oplus (C_{n-1} \oplus C_{n-1}) \\
&= S_{n-1} \oplus S_{n-3} \\
\overline{P}_n \oplus \overline{P}_{n-2} &= S_{n-1} \oplus S_{n-3}
\end{aligned} \tag{2-48}$$

From Equation (2-46):

$$\begin{aligned}
S_{n-1} + S_{n-3} &= D_{n-1} \\
D_{n-1} &= P_n \oplus P_{n-2} = P_n \oplus P_{n-2}
\end{aligned} \tag{2-49}$$

Hence, it is possible to reproduce the data without regard to the polarity of the biphase data and without using the recovered data clock. The latter case is the reason that either biphase M or biphase S must be used with MSK since the data clock recovered from MSK has a 180-degree ambiguity. Note that the separation for the differential decoder is two 1/2-bit intervals. Also note that, for MSK, biphase data is treated as special structured NRZ data having an effective clock rate of twice the actual data rate.

A simplified schematic of the encoder/decoder circuit for Manchester data is shown in Figure 2-21. Note that the encoder and decoder are the same and that both use the data clock. A similar set of schematics for biphase S (or biphase M if the NRZ data is inverted) is shown in Figure 2-22. For the encoding operation, NRZ-L data is first converted to NRZ-M data. Then, NRZ-M data is exclusive-OR'ed with the clock and the complement of this data is the desired biphase S data. Note that NRZ-L data is essentially replaced by NRZ-M data to produce the biphase S data. The decoding operation omits the clock and NRZ-L data is reconstructed directly from the biphase bit stream. Clock polarity is unimportant.

The final data encoding scheme considered as part of this study is the Miller code (also called the Delay code). This code has the advantage of providing at least one transition during each 2-bit interval, 2T, but has a maximum transition rate of once per bit interval. Compare this with biphase or Manchester data that can have two transitions per bit interval. The interest in the delay codes arose as a means to conserve bandwidth. The results of the use of certain versions of Miller data are discussed later. This subsection is concerned with only the methods of encoding and decoding the data and its baseband characteristics.

Figure 2-18 shows three versions of the delay code. The first is generated from biphase L or Manchester data; it is called Miller coding. The second version is designated D-M and is generated from biphase M data; the last is D-S, generated frim biphase S data. In all three cases, the delay code is generated rather simply by applying the biphase data to the clock input of a flip-flop (FF), thus causing the FF to toggle. For the cases shown, the toggling occurs on the positive edge of the data. In some cases, it may be desirable to invert the biphase data before converting it to a delay code; ultimately, this will have no effect on the output data, although it changes the timing relationship.

Miller data can be defined verbally with respect to NRZ-L data: a one is characterized by a transition (either direction) in the *center* of a bit cell; a zero is characterized by a transition at the end of a bit cell unless the zero is followed by a one, in which case the transition is omitted. Note that this definition really describes the characteristics that can be used to decode the data; it is easier to sketch the data pattern by beginning with biphase data. This is particularly true for the other forms of the delay code.

The D-M version bears a similar relationship to NRZ-S data, except a transition at the end of a bit cell represents an NRZ-S zero. For the D-S version, a transition at the end of a bit cell represents a zero for NRZ-M data. In other words, for D-M and D-S, the effective bit cells are displaced 1/2 bit and the code represents inverted differential NRZ data.

The complete encoding operation for D-S consists of three steps: (1) conversion from NRZ-L to NRZ-M; (2) conversion from NRZ-M to biphase S; and (3) conversion from biphase S to D-S. The first two conversions have already been discussed. The last conversion is simply a division by 2, as previously stated. This division can be represented mathematically by:

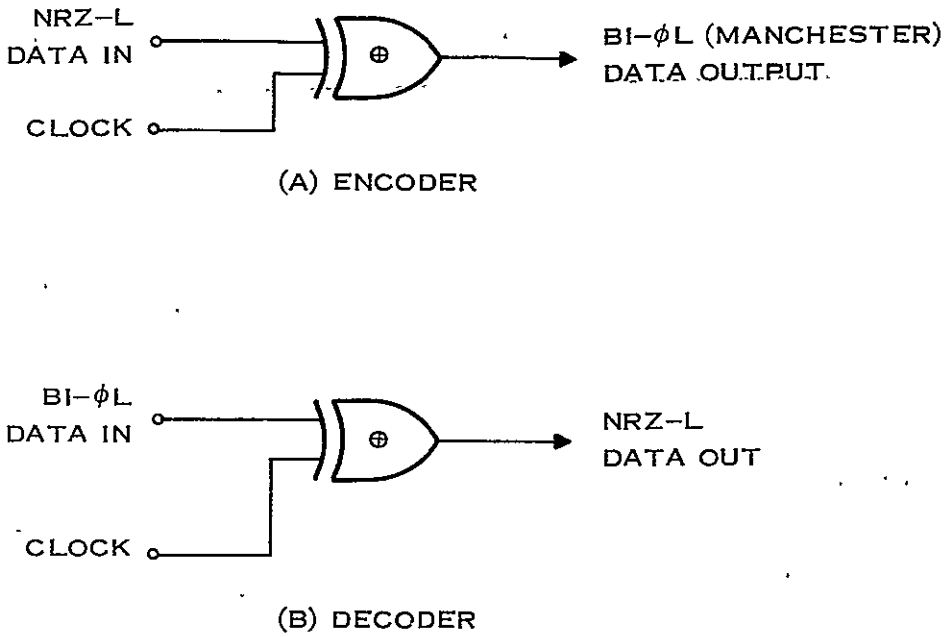

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Figure 2-21. Encoder/Decoder for Manchester Data

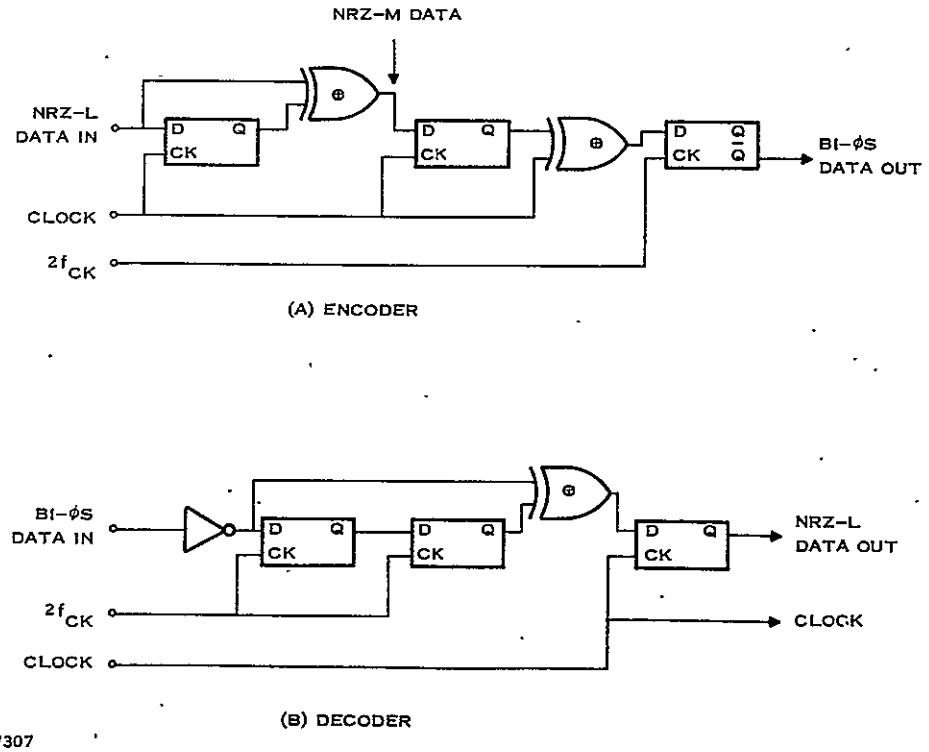

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Figure 2-22. Encoder/Decoder for Bi-Phase Space Data

$$M_n = (P_n \oplus P_{n-1})\, P_n \oplus M_{n-1}$$

where

M_n = the delay code bit symbol

P_n = the biphase code bit symbol

n = a duration of 1/2T.

The delay codes have some shared unique properties. First, the duration of a one or a zero value of the code may be T, 3/2T, or 2T. The pattern locations are random if the data is random. Therefore, for MSK, this code may be treated as structured NRZ data with an effective clock rate of twice the data rate. The code has no sense of polarity; i.e., a one or zero is represented by a transition in either direction. Therefore, a string of ones will look the same as a string of zeros until the bit cell limits are defined; the only difference is the phase of the coded waveform. This ambiguity is resolved by observing that a unique phase exists for a data pattern that results in the lowest possible output frequency. For Miller data, alternating ones and zeros (NRZ-L data) produce square-wave Miller data with a frequency of 1/4 f_{ck}. For D-S, the equivalent is an all ones NRZ-L input. This unique pattern must be used to resolve ambiguities in the decoded data. The ability of this pattern to establish the correct polarity of the output data is based on the fact that this pattern produces transitions only in the center of the bit cell. Hence, it can be used to establish the correct clock phase. Note that this is in addition to any other ambiguity corrections. The use of D-M or D-S instead of basic Miller simply removes any restrictions on the clock phase and/or biphase data polarity at the encoder while maintaining the desired polarity of the decoded data. It is necessary to specify only the basic source of the data, not the polarity.

Figure 2-23 shows a method of generating Miller, D-M, or D-S data from biphase data. The input may also be inverted; this results in the decoded data being inverted. In the case of NRZ-M or NRZ-S (biphase S or biphase M), the polarity is corrected at the output of a differential decoder.

Figure 2-24 shows a decoder for converting D-S data to NRZ-L data; a five-bit all-ones decoder is included for selecting the properly decoded data channel. Figure 2-25 provides the associated timing diagram. The input D-S (Miller-X) data is shifted through a 2-bit shift register using a synchronous clock that is an integer multiple of the data clock (8 times). An exclusive-OR gate detects transitions in the delay-code data. The resulting pulses are applied to two channels of the decoder. One channel uses clock to gate the pulses; the other uses $\overline{\text{clock}}$ to gate the pulses. These pulses essentially form an RZ representation of NRZ-M data in one channel and meaningless data in the other channel. A resettable latch and a single-bit register reconstruct the NRZ-M data. Finally an exclusive-OR differential decoder converts this data to

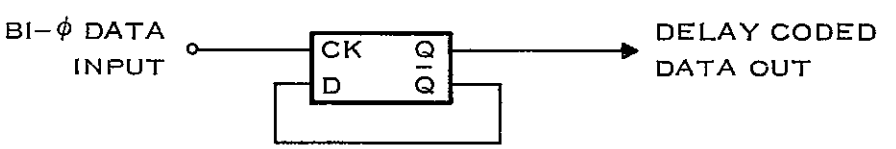

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Figure 2-23. Encoder for Converting Bi-Phase Data to Miller or Delay-Coded Data

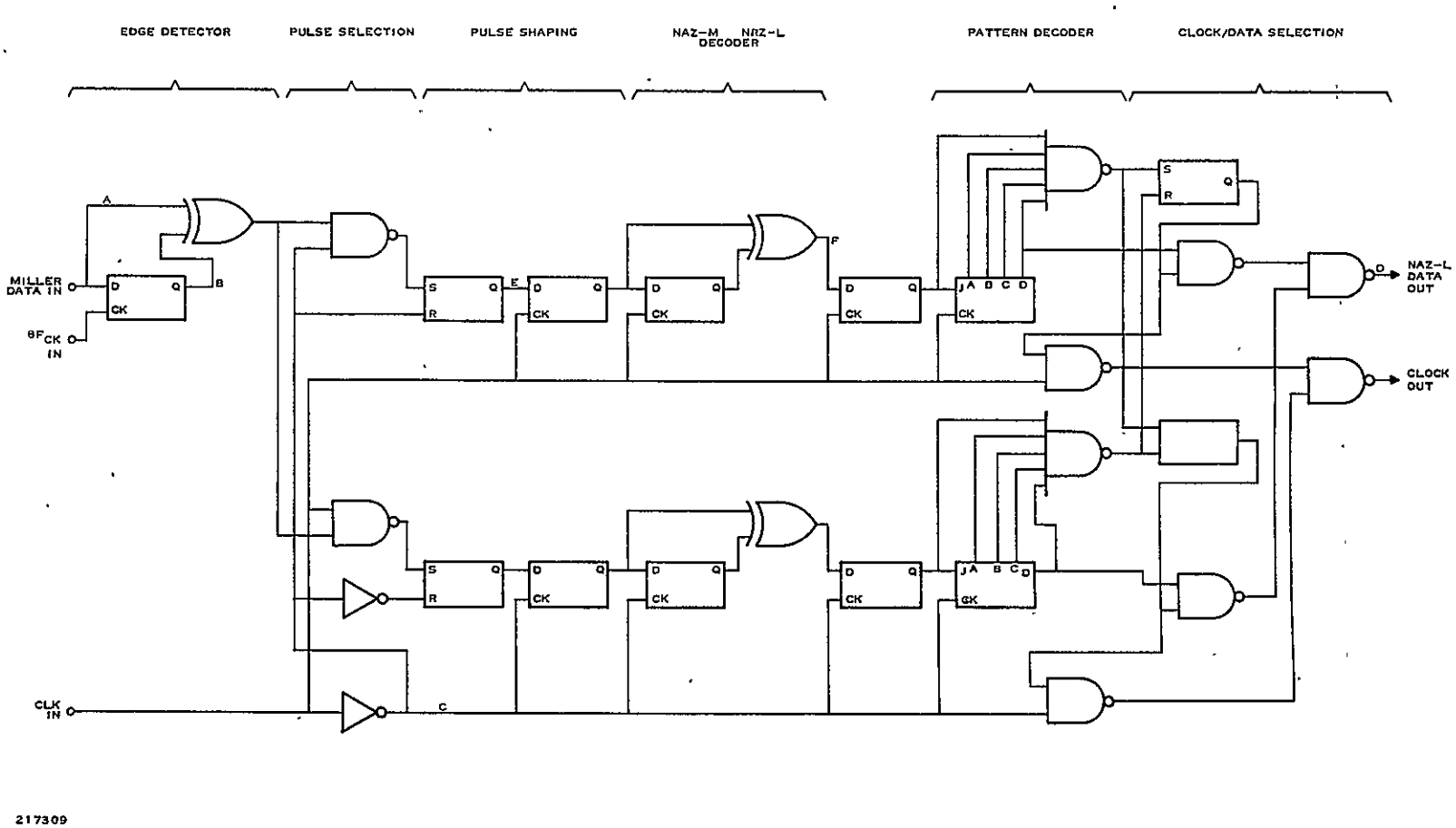

Figure 2-24. Miller Data Decoder Schematic

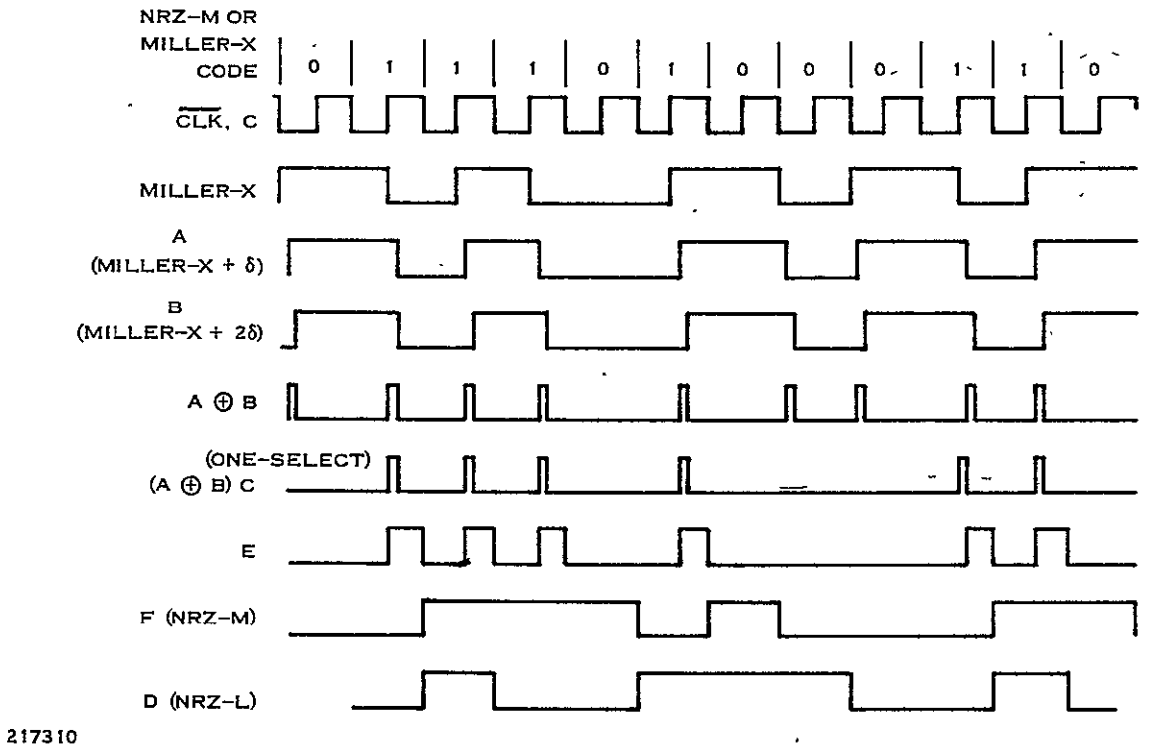

Figure 2-25. Timing Diagram for Miller Decoder

NRZ-L data. (The other channel gated by the wrong clock phase contains meaningless data.) The data from each channel are applied to an all-ones decoder. (This all-ones pattern represents an alternating one/zero pattern input to the D-S encoder.) Only one clock phase can reproduce five consecutive ones. (Actually, only three consecutive ones are needed, but five are used to reduce the probability of a single error producing false selection of the channel.) When five consecutive ones are detected, a latch is set. The latch selects as the proper data and clock source the channel containing the five consecutive ones. Note that only one channel can be selected at any given time, but either can be selected, depending on the phase of the recovered clock. However, once selected, the channel selection will not normally change unless lock is lost. A small probability of false selection does exist, however.

A final comparison of baseband codes is made by comparing the power spectral densities of NRZ, Manchester, and Miller codes. Although the spectra of MSK cannot be directly evaluated from the baseband spectra, it is worthwhile to compare the relative characteristics of the spectra of three codes.

The spectrum of random NRZ data is shown in Figure 2-26. The frequency is normalized to the bit rate frequency, 1/T. The amplitude is given in decibels normalized to bit time, T. The spectrum was computed from:

$$W(f) = 10 \log \left[\frac{\sin^2 (2\pi f T/2)}{(2\pi f T/2)^2} \right] \tag{2-50}$$

Two important characteristics are to be observed in this spectrum. First, the maximum power spectral density occurs at DC; this implies a long dwell time at the mark and space frequencies for MSK. The second characteristic to be noted is that nulls occur at multiples of 1/T. Also, note the similarity between the baseband spectrum for NRZ data and the spectrum for antipodal PSK or discontinuous-phase FSK (Figure 2-2).

The baseband spectrum of Manchester data is shown in Figure 2-27. The spectrum was computed from

$$W(f) = 10 \log \left[\frac{\sin^4 (2\pi f T/4)}{(2\pi f T/4)^2} \right] \tag{2-51}$$

The PSD for this code has a null at DC and nulls at multiples of 2/T. The primary data lobe occupies a spectral width of 2/T instead of the 1/T range for NRZ data. The spectrum contains no DC component, thus indicating symmetry about the time axis and the generation of a carrier at the center frequency, f_0, when applied to an MSK modulator. The wider baseband spectrum implies a wider bandwidth occupancy at RF.

The baseband spectrum for Miller data was computed from:

$$W(f) = 10 \log \left[\frac{2[23 - 2\cos(\omega T/2) - 22\cos(\omega T) - 12\cos(3\omega T/2) + 5\cos(2\omega T) \ldots}{\ldots + 12\cos(5\omega T/2) + 2\cos(3\omega T) - 8\cos(7\omega T/2) + 2\cos(4\omega T)]} \Bigg/ \omega^2 T^2 [17 + 8\cos(4\omega T)] \right]$$

The PSD plot from this equation is shown in Figure 2-28. Note that this spectrum has a DC component but with a power density much less than the peak of the spectrum that occurs at 0.4/T. The spectrum has nulls at multiples of 2/T, but the power content in the center of all lobes is reduced. Note that the majority of the energy is concentrated in the region of 0.2/T to 0.5/T; however, there is a peak in the PSD at F = 1.6/T. This would tend to indicate that the spectrum of MSK using Miller data would be similarly compressed.

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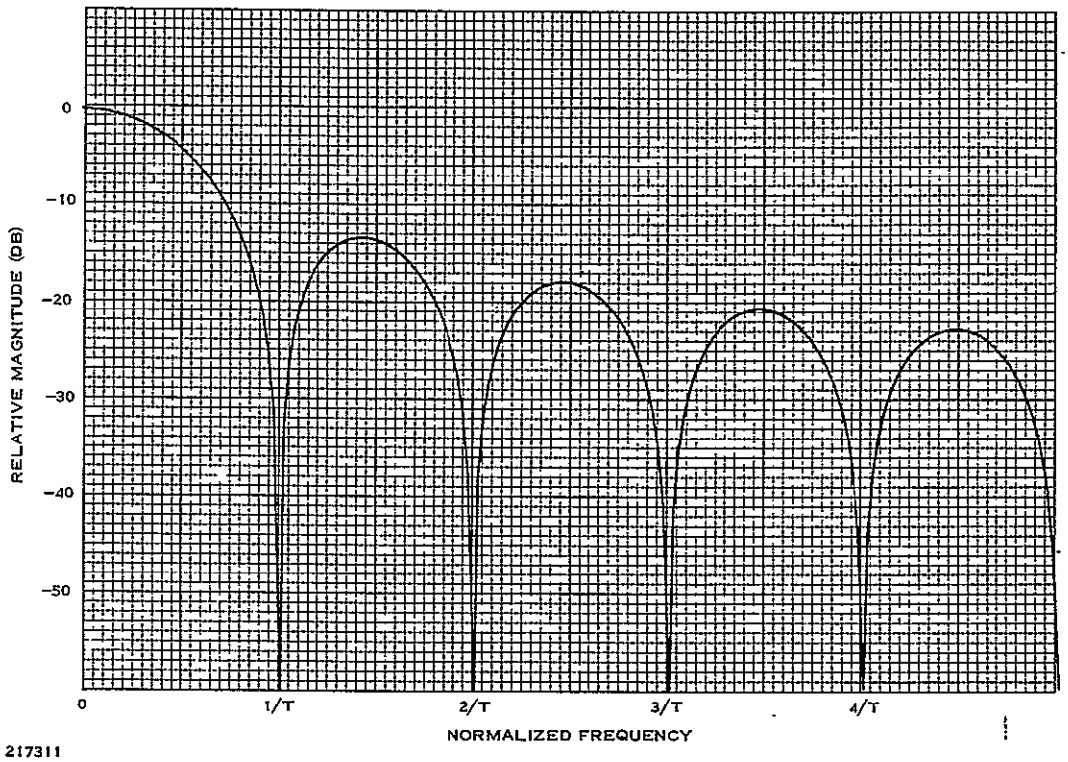

Figure 2-26. Power Spectral Density of Random NRZ Data

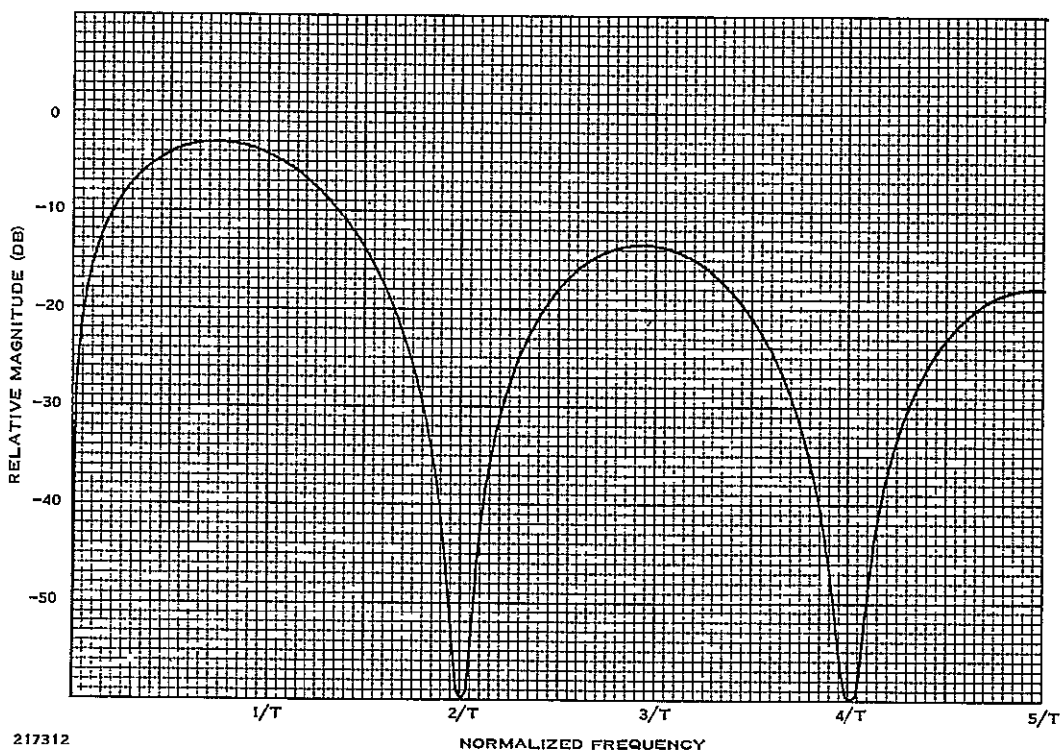

Figure 2-27. Power Spectral Density of Random Manchester Data

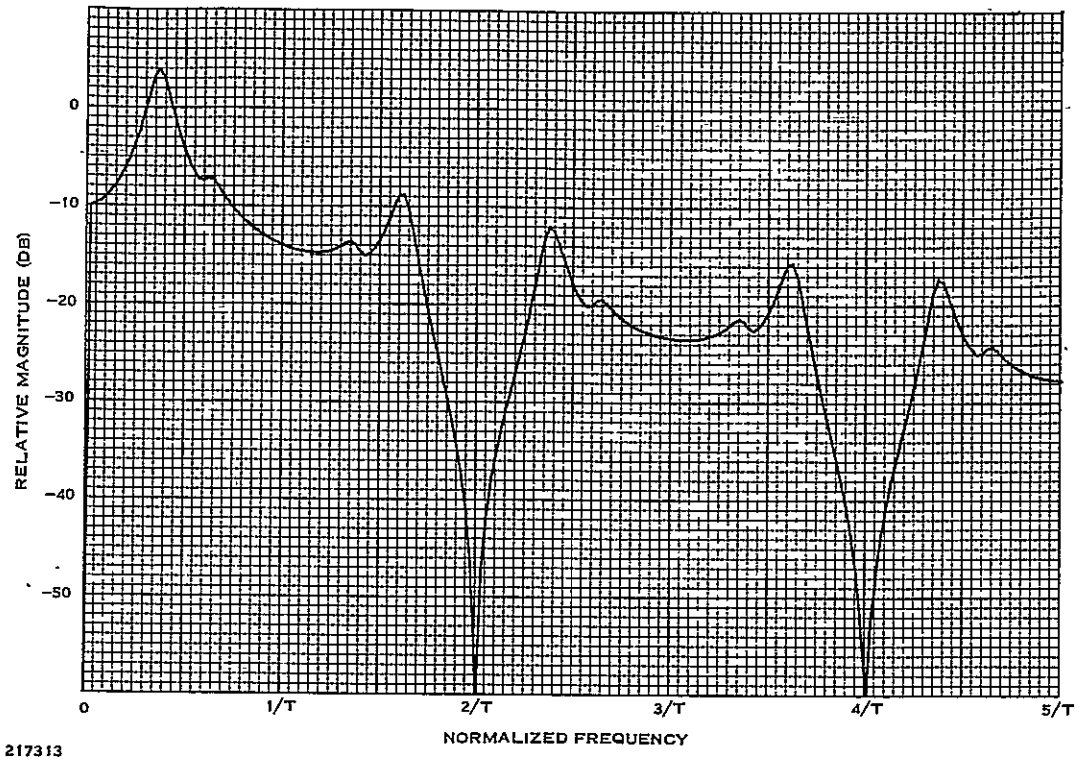

Figure 2-28. Power Spectral Density of Random Miller Data

SECTION III

MSK COHERENT DEMODULATOR DESIGN

This section outlines the design of the coherent demodulator built and tested as part of this study effort. In addition to the basic design concept, detailed design considerations for the mark/space phase-lock loops, the bit sync recovery circuits, the timing generator, the demodulator, and the data detector/decoder are presented. The design of an AGC circuit is also described. The detailed schematics and board layout are contained in Appendix B.

3.1 DESIGN CONCEPT

The underlying principles for the basic coherent demodulator design were presented in Section 2. In particular, Figure 2-11 shows the concept in a simplified block diagram. The detailed block diagram is shown in Figure 3-1. A 180-kHz bandpass filter with a bandwidth of 800 Hz is included to limit the channel bandwidth. The data rate for the previously constructed modulator is 320 Hz; hence, the channel bandwidth is limited to approximately 3R for NRZ (for bi-phase or Miller data, this is 1.5 R equivalent NRZ BW).

The 180-kHz center frequency is chosen because this is the IF of the existing breadboard receiver. The filter was designed to have a 3-dB bandwidth of 800 Hz, with a center frequency of 180 kHz. The 50-dB bandwidth was designed to be 3200 Hz. This filter design enables the breadboard to be used to verify performance of MSK/Miller data, with a channel spacing of 3R where R is the NRZ bit rate. The design was specified as linear phase with 1-dB passband ripple, maximum.

Frequency doubling is accomplished with an analog multiplier operated as a squaring circuit. As previously discussed, this results in discrete spectral lines at $2f_m$ and $2f_s$. Phase-lock loops with VCXOs are used to recover the mark and space frequencies. The input signal to the squaring circuit is designed to be 20 Vpp. The output voltage from the multiplier is (XY)/10. The squaring operation is given by:

$$[10 \cos (\omega t)]^2/10 = 5(1 + \cos 2\omega t) \qquad (3\text{-}1)$$

Simple filtering removes the dc component and provides carriers at twice the mark and space frequencies with a peak of 5 volts.

The mark and space PLLs lock to these carriers. Each carrier is present, on the average, only 50 percent of the time. Therefore, the PLLs must provide a close estimate of the correct frequency and phase of the recovered carriers during periods when an input is not present. This implies a narrow-bandwidth PLL and a stable VCO; hence, a VCXO is chosen. A single flip-flop divide-by-two following each PLL output provides the mark and space reference frequencies.

A simple mixer and phaselock loop is used to recover the data clock and to provide the necessary timing information to control the reset integrators and sampling circuits. A monolithic PLL is chosen for this function. The integral VCO frequency is selected to be a binary multiple of the $f_{ck}/2$ reference to make frequency division easy while providing symmetrical outputs.

The timing generator is a simple shift register with precise edge detection circuitry and gating to produce the necessary sampling pulses and reset control pulses for the I- and Q-channel data detectors. The shift register approach, using the $f_{ck}/2$ clock as an input, precisely controls the timing sequence and pulsewidths. A high-frequency clock (≈2 MHz) is used to control edge detecton and pulsewidth.

The filtered MSK signal, S(t), is applied to the I and Q demodulators; the cos (ω_0 t) cos (πt/2T) recovered carrier is applied to the I demodulator while the sin (ω_0 t) sin (πt/2T) quadrature carrier is applied to the Q demodulator. Analog X-Y multipliers are selected for the I and Q demodulators. The coherently demodulated signals are then applied to reset integrators that serve as matched filters.

The matched-filter data-detection circuitry consists of simple operational-amplifier integrators using analog switches to dump the integrating capacitors at the end of two bit times. The output of each integrator is applied to a zero-voltage threshold comparator. The comparators make hard decisions on the integrated signal; a logic-one or logic-zero is selected, depending on the polarity of the input. A simple "D" flip-flop is used as a digital sample-and-hold device. Each comparator state is sampled just before dumping the associated integrator, i.e., at the peak of the integrator output.

The outputs from the sample-and-hold registers are shown being multiplexed by the $f_{ck}/2$ signal. This is *not* necessary for NRZ data but was retained to emphasize that the data are effectively multiplexed between the I and Q channels, and simplifies the decoder for bi-phase data. In fact, the register outputs can be applied directly to an exclusive-OR differential decoder; the output of the decoder is then applied to a "D" FF buffer register that is clocked by the recovered f_{ck} signal. The NRZ output and recovered clock are thus synchronized.

The circuit, as shown in Figure 3-1, multiplexes the I and Q symbols into a single serial bit stream that is shifted through registers by the recovered clock (or *effective* clock for bi-phase or Miller data). The exclusive-OR gate connected across the first storage register provides an NRZ output (or a Miller data output to a decoder for Miller data). The exclusive-OR gate across the last two stages provides the decoding for bi-phase (bi-phase S for this circuit) data. This decoded NRZ-L data is buffered by a single register; the "clock" is actually twice the desired NRZ clock frequency and must be divided by two. The Miller decoder is shown, but its input is taken from the "NRZ OUT" point.

3.2 MARK/SPACE PLL DESIGN

The key to the proper operation of the coherent demodulator for MSK lies in the design of the phase-lock loop carrier-recovery circuits. This is particularly true for NRZ data because random data results in extended periods when only a mark or space reference is available. The PLLs must provide a good estimate of the proper carrier frequency *and* phase during these periods. In addition, the switching between the mark/space frequencies results in replicating the data at the output of each phase detector. Therefore, the loop bandwidth must be narrow enough to reject this "false phase error" signal. Furthermore, it is necessary to take measures to prevent this data modulation of the phase error signal from causing saturation of any linear processing elements.

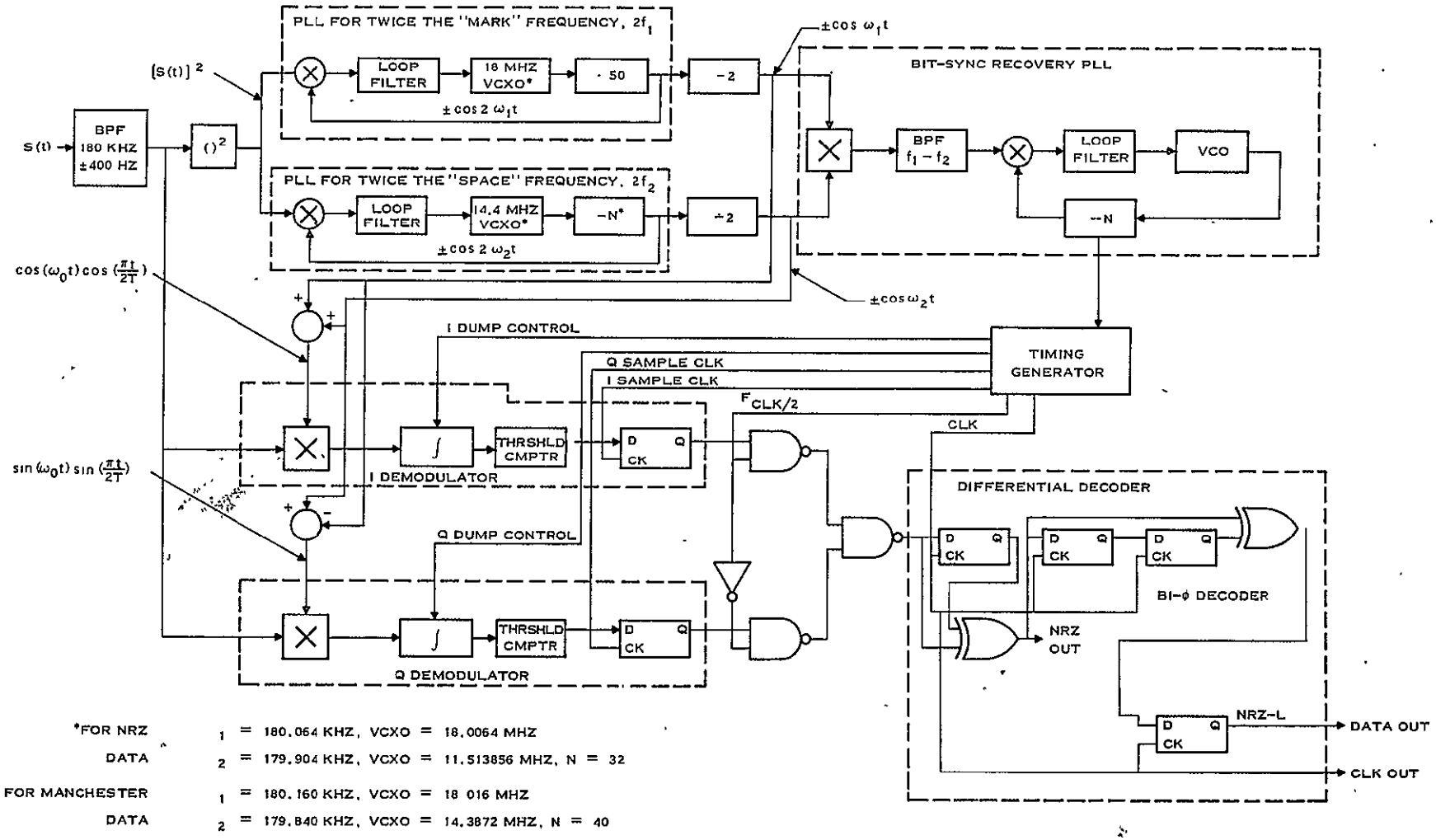

Figure 3-1. Block Diagram for a MSK Coherent Demodulator

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Each loop bandwidth must be narrow enough that the noise bandwidth is small and, therefore, the phase noise in the recovered carrier is small. A diametrical requirement is to minimize the acquisition time by *increasing* the loop bandwidth. This latter requirement is particularly important when the system is to operate in a burst-transmission mode. Therefore, some compromise loop-bandwidth is required. Acquisition in noise is also a consideration.

The narrow loop bandwidths and extended periods when no reference signal is present necessitate the use of a VCXO. Most VCXOs perform best when operated at frequencies above 10 MHz. In addition, it is necessary to operate the VCXO at a high frequency to provide a good fine-frequency measurement of the received signal in a short time interval (0.1 to 0.5 second). Therefore, the VCXO center frequencies are selected as shown in Figure 3-1; the corresponding division ratios are also shown.

3.2.1 Phase Detector Design

Several phase detector options are available. If the input is limited and converted to a square wave, an exclusive-OR phase detector can be used. However, for low S/N ratios, this technique is not as good as linear phase detector.[15] The phase detector chosen for this design uses an analog switch to implement a switching phase detector. Basically, this design provides full-wave retification of an input sinusoid, but shifted 90 degrees for a no-phase-error condition.

A simplified schematic of the phase detector and its associated waveforms are shown in Figure 3-2. The input signal is inverted; both the inverted and non-inverted signals are then applied to the inputs of a double-pole analog switch. The switch is driven from a TTL reference source obtained from the countdown-chain for the VCXO. The waveforms shown in Figure 3-2(b) show the proper "no-phase-error, in-lock" condition. The inverted and non-inverted signals are selected on alternate half cycles. The average dc value is zero. The maximum positive phase-error condition is shown in Figure 3-2(c). (A similar negative-value condition exists for a –90-degree phase error). Therefore, the maximum phase detector output for a $\pm\pi/2$ phase error is simply the dc component of the full-wave-rectified signal given by:

$$V_{max}(\phi) = \frac{2V_{pk}}{\pi}\left(1 + \frac{2\cos 4\omega t}{3} - \frac{2\cos 8\omega t}{15} + \cdots\right) \tag{3-2}$$

where V_{pk} is the peak value of the frequency-doubled input signal and ω is the frequency of the mark or space signal. For this design, the value of V_{pk} is 5 as given by Equation (3-1). Therefore, the maximum dc output from the phase detector corresponding to a maximum phase error of 90 degrees or $\pi/2$ radians is:

$$V_{max}(\phi) = \frac{2V_{pk}}{\pi}$$
$$= 3.2 \text{ volts}$$

[15] Floyd M. Gardner, *Phaselock Techniques*, John Wiley and Sons, Inc., (New York, 1966).

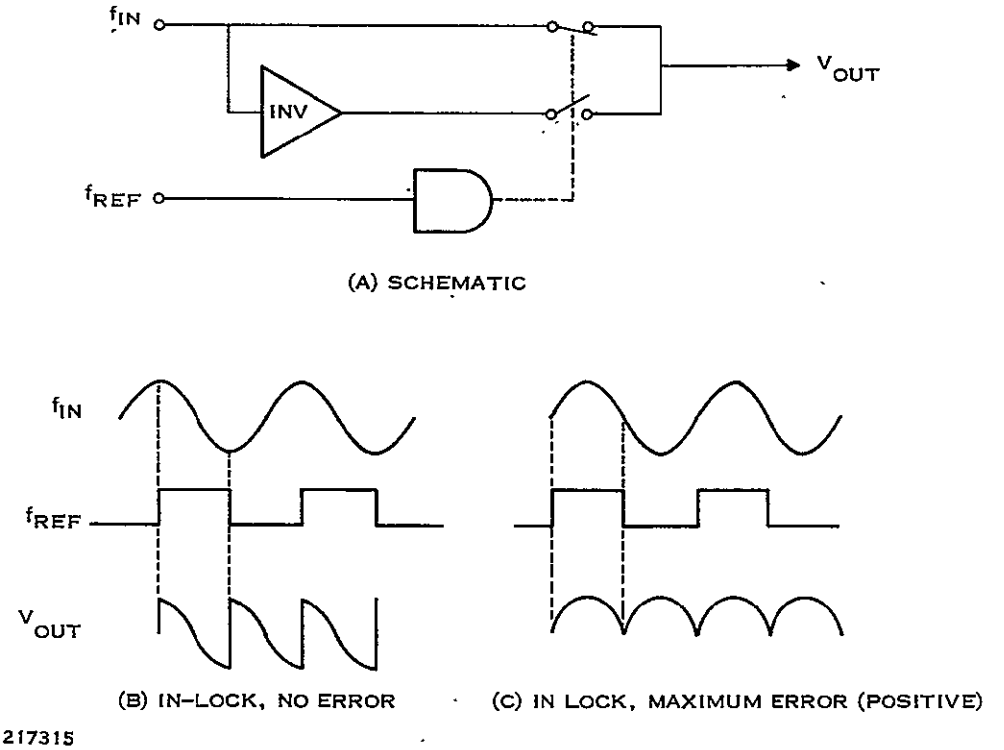

Figure 3-2. Phase Detector Schematic and Waveforms

The phase detector gain constant is therefore:

$$k_d = 3.2/(\pi/2) = 2.0 \text{ volts/radian} \tag{3-3}$$

Note that the phase detector gain is a function of the input signal level Equation (3-2). Since the value of k_d determines several PLL parameters, particularly loop bandwidth, it is necessary to provide a constant-amplitude signal at the input to the phase detectors. This can be done by providing amplitude limiting before the channel filtering or by using AGC. The use of AGC is preferred since it introduces no nonlinearities in the system.

The peak signal input to the analog switch is only ±5 volts and well within its capability. The input frequency is 360 kHz. The total switching time of a DG190 is only 300 ns; therefore, this device can easily accommodate the input signal. The maximum phase error introduced should be less than 20 degrees. The use of high-level input signals minimizes the effects of switching transients.

The same basic phase detector design can be used for a quadrature lock detector. It is necessary to use only a 90-degree phase-shifted reference signal for the lock detector. The output will then be a full-wave-rectified signal with a dc value of 2 Vdc when the loops are in lock; otherwise, the output is a sinusoid and/or noise with zero mean.

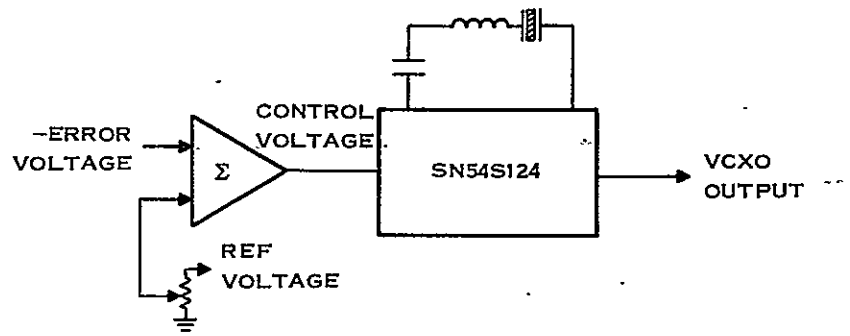

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Figure 3-3. Schematic Diagram of VCXO Design

3.2.2 VCXO Design

The VCXO uses an SN54S124 monolithic VCO, with a crystal as the frequency-determining element. An attempt was made to design a VCXO that would be very stable for a fixed input voltage. This will minimize frequency error at the time of acquisition and reduce phase jitter. In addition, one VCXO frequency is needed for NRZ data demodulation but another frequency is needed for bi-phase and Miller demodulation. Hence, the SN54S124 is wired to select one of two crystal oscillators. The control voltage is supplied from an operational amplifier that combines the error voltage with a bias voltage. The bias voltage is used to adjust the rest (zero-error) frequency of the VCXO. A simplified schematic of the VCXO is shown in Figure 3-3.

The circuit was tested at room temperature, using zener-regulated voltages for the oscillator and reference. The frequency stability was measured and found to be better than 2×10^{-5} over a 48-hour period at 18 MHz. This stability allows the loop bandwidth to be designed for as low as 10 Hz at 360 kHz. The frequency change versus control voltage was measured for three crystal frequencies. The linear control range for each was found to be as follows:

f_o	Δf	For	ΔV_c	K_o
18 MHz	17.956 to 17.996		1.0 to 2.75	143 rad/s/mV
13.6 MHz	13.583 to 13.610		1.0 to 2.50	113 rad/s/mV
11.5 MHz	11.494 to 11.510		1.0 to 3.00	50 rad/s/mV

Fortunately, the VCXO gain constant, K_o, is almost constant as a function of center frequency. Therefore, only a single PPL design is required. The actual VCXO crystal frequencies are shown in Figure 3-1. The LC combination helps linearize and extend the control range of the VCXO as well as minimizing spurious oscillations. The TTL output is well suited for direct application to the divider chain. The frequencies were selected to provide easy integer frequency division, minimum interaction, and an operating frequency high enough that the VCXO tuning range is adequate. In addition, it was desired to multiply the "mark" carrier frequency value by a large number to provide a good frequency measurement of the received signal in a short measurement interval (100 ms). Therefore, the division ratios are those in Figure 3-1. The VCXO frequencies and the division ratios are selected by logic circuitry as a function of NRZ or bi-phase/Miller operation.

3.2.3 Loop Filter

The loop filter design determines the loop characteristics. Therefore, it is necessary to define the loop requirements before the loop filter can be designed. In addition, there are two basic loop filter designs to choose from.[16] Considerations that affect the loop filter design are noise bandwidth, acquisition time, expected initial frequency error, and maximum allowable phase error.

It is desirable to minimize the acquisition time of the loops, particularly for burst-mode operation. Unfortunately, this implies increasing the loop bandwidth, which is a mutually conflicting requirement with respect to loop noise bandwidth. Therefore, a compromise design is necessary. Since it is desirable to minimize the final in-lock phase error, the active (or integrator) loop filter design is preferable; however, this does require a means to dump the integrator until a valid signal is present.

As previously stated, the VCXO stability was found to be on the order of ±5 Hz at 360 kHz; therefore, a loop bandwidth of less than 5 Hz would be impractical in the acquisition mode. A loop bandwidth of 20 Hz was selected; this minimizes acquisition time for initial frequency errors of as much as ±20 Hz. A 20-Hz loop bandwidth provides an acquisition time of less than 50 ms for a damping factor range of 0.7 to 1.0. This is equivalent to a bit-sync code length of 15 to 20 bits at a data rate of 320 BPS—well within the capabilities of the breadboard. Therefore, the loop bandwidth, ω_n, is:

$$\begin{aligned} \omega_n &= 2\pi(20\text{ Hz}) \\ &= 125\text{ rad/s} \end{aligned} \tag{3-4}$$

Selecting a nominal damping factor of $\zeta = 0.7$, the loop noise bandwidth is:

$$\begin{aligned} B_L &= \frac{\omega_n}{2}\left(\zeta + \frac{1}{4\zeta}\right) \\ &= 0.53\ \omega_n \\ &= 66\text{ Hz} \end{aligned} \tag{3-5}$$

The mean-square phase jitter is related to the loop bandwidth by:

$$\theta_{no}{}^2 = \frac{W_i\, B_L}{P_s} \tag{3-6}$$

where P_s/W_i is the signal-to-noise power density.

If the rms phase jitter is to be equal to or less than 10 degrees (≈0.2 radian), the minimum signal-to-noise power density of the input is:

$$\begin{aligned} P_s/W_i &= \frac{B_1}{\theta_{no}{}^2} \\ &= 32\text{ dB} \end{aligned} \tag{3-7}$$

[16] Gardner.

For a data rate of 320 BPS, this corresponds to an E_b/N_o of:

$$E_b/N_o = 32 \text{ dB} - 10 \log 320$$
$$= 7.1 \text{ dB}$$

Therefore, the loop bandwidth of 20 Hz should provide good performance (minimum effect on BER tests) for measurements of BER with E_b/N_o as low as 7 db.

A block diagram for the mark PLL is shown in Figure 3-4. For this loop,

$$K_d = 2 \text{ v/rad}$$
$$K_o = 143{,}000 \text{ rad/s/V}$$
$$\omega_n = 125 \text{ rad/s}$$
$$\zeta = 0.7$$
$$N = 50$$

A simplified schematic of the active loop filter is shown in Figure 3-5. For this loop filter, the appropriate relationships are:

$$\omega_n = \sqrt{\frac{K_o K_d}{N\tau_1}} \tag{3-8}$$

and

$$\zeta = \frac{\tau_2}{2}\,\omega_n \tag{3-9}$$

where

$$\tau_1 = R_1 C$$
$$\tau_2 = R_2 C$$

From this relationship,

$$\tau_1 = \frac{K_o K_d}{N\omega_n{}^2}$$
$$= 0.3$$
$$\tau_2 = \frac{2\zeta}{\omega_n}$$
$$= 0.0112$$

Selecting C = 2.2 μf, then,

$$R_1 = \frac{\tau_1}{C}$$

$$= 166K$$

$$R_2 = \frac{\tau_2}{C}$$

$$= 5.1K$$

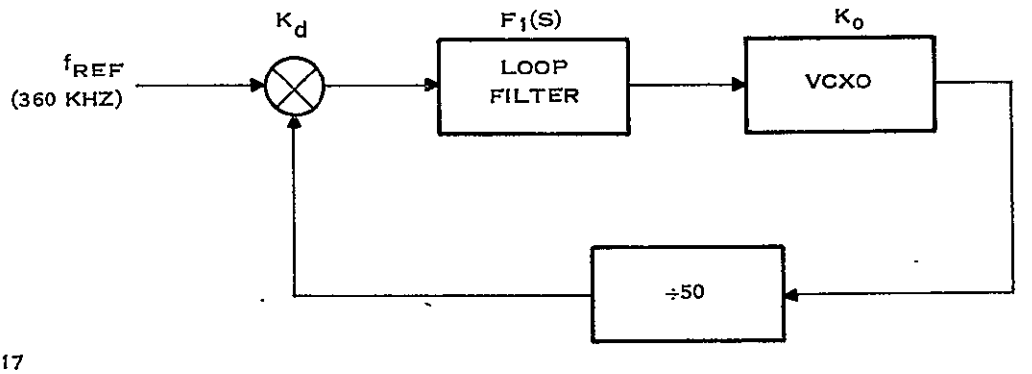

Figure 3-4. Basic Phase-Lock Loop Block Diagram

The PPL design discussed to this point would be complete if the input reference signal were a continuous sinewave. This loop does not have a continuous input signal, however; the data causes the instantaneous frequency to be switched between the mark and space carrier. Therefore, the reference is missing 50 percent of the time. This causes the input data pattern to be replicated on the error voltage output from the phase detector. It is desirable to attenuate this data pattern beyond that of the 6-db/octave provided by the loop to minimize the noise on the output of the VCXO. (This is particularly important in the mark loop since this signal is used to measure the fine frequency of the received signal during message transmission). This can be done after the phase detector.

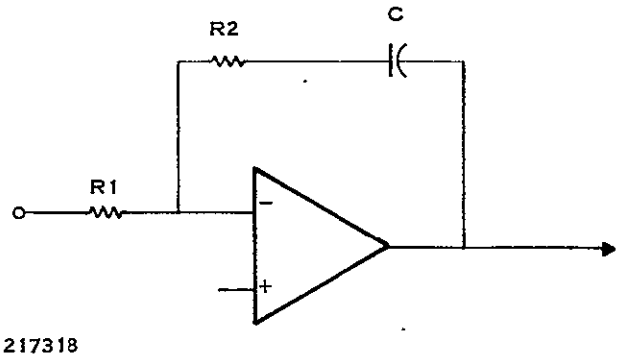

Figure 3-5. Simplified Schematic Diagram of Active Loop Filter

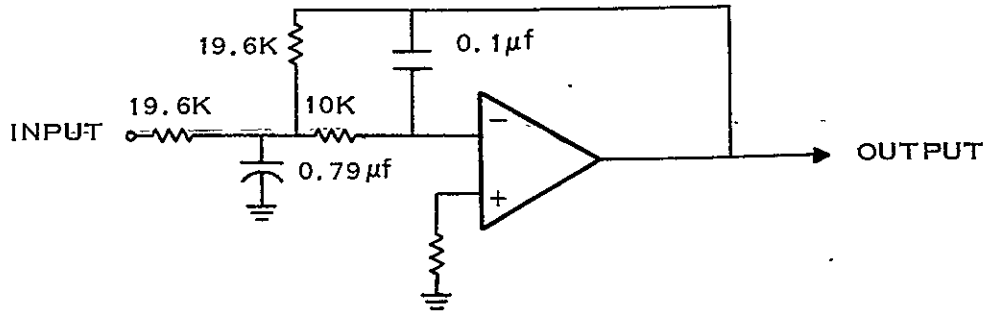

Figure 3-6. Schematic Diagram of Low-Pass Filter for Phase-Lock Loops

3.2.4 Low-Pass Filter Design for Data Rejection

The replication of data on the phase error output from the phase detector causes undesirable affects. A low-pass filter can be added after the phase detector. The filter cutoff frequency should be low enough that adequate attenuation of the data is realized, but not low enough to adversely affect the dominant loop pole-zero (stability) characteristics.

A schematic of an active low-pass filter design is shown in Figure 3-6. A cutoff frequency of 40 Hz was selected for the initial design; a damping factor of 0.5 was chosen. The transfer function is:

$$F_2(S) = \frac{\omega_o^2}{S^2 + 2\zeta\,\omega_o\,S + \omega_o^2} \tag{3-10}$$

Standard filter design equations were used to calculate the component values shown. These values provide a pair of poles at:

$$S = -128 \pm j\,220$$

When compared with a loop zero at s = –91, it is obvious that the LPF will affect the overall loop characteristics. A full loop analysis is required.

3.2.5 Loop Analysis

The design previously outlined was analyzed, using a transfer function analysis computer program. The analysis revealed that the loop would be unstable with the LPF in the circuit. An analysis of the open-loop phase and gain characteristics revealed that it was necessary to reduce the loop gain. The loop gain was subsequently reduced by 12 db and the damping was adjusted accordingly. The revised loop filter design has the following transfer function:

$$F(S) = \frac{1.57 \times 10^{-2}\,(S + 45.45)}{S}$$

Referring to Figure 3-5, the new resistor values are:

$R_1 = 637K$

$R_2 = 10K$

All other elements remain the same.

The open-loop phase/gain response, the closed-loop phase/gain response, the root locus, and the transient response of the revised loop design were computed and plotted. The open-loop gain/phase characteristics are shown in Figure 3-7. The phase margin is 40 degrees. The effective loop bandwidth is approximately 16 Hz.

The closed-loop response characteristics are shown in Figure 3-8. The maximum peaking is 3.6 dB. Note that the loop has an attenuation of 25.5 dB at 80 Hz; it has a loss of 45 dB at 160 Hz. A standard PLL design would have only 10- and 16-dB attenuation at these respective frequencies. Therefore, the loop will have good rejection of data-modulation spectral components greater than ±80 Hz removed from the frequency-doubled reference carriers. The design has two pairs of closed-loop poles. One pair is located at $S = -59 \pm j\,53$, having a natural frequency of 12.6 Hz and a damping factor of 0.74. The second pair is located at $S = -69 \pm j\,193$, having a natural frequency of 32.6 Hz and a damping ratio of 0.34. The pole locations are similar to those for a 4-pole Butterworth filter, but shifted out along the negative real axis to provide better stability.

A root-locus of the PLL design is shown in Figure 3-9. There are two poles located initially at the origin and a pair located at $S = -128 \pm j\,220$. There is one zero located at $S = -45$. The two poles at the origin initially move along the imaginary axis, before moving into the complex plane. Their position is indicated for the design-value loop gain. As the gain is increased, they converge on the negative real axis at $S = -98$. They separate, with one migrating toward zero while the other moves toward negative infinity. The complex pole pair moves toward the right half plane. Their position for the selected loop gain is marked. This pole pair is responsible for loop instability as the loop gain increases. The pair crosses the imaginary axis when the loop gain is increased 8 dB above the design value; i.e., the root locus indicates a gain margin of 8 dB.

The time response to a unit step in phase is shown in Figure 3-10. The peak overshoot, 47 percent, occurs at $t = 25$ ms. This is equivalent to a second-order loop with a damping factor of 0.3; however, the transient behavior is more heavily damped and there is only 2 percent undershoot. The loop settles to within 2 percent after only 65 ms. Although the loop characteristics were not evaluated for a step in frequency as would be the case during loop acquisition, the loop can be expected to settle within a few percent of final value in less than 100 ms. Therefore, the loop appears to be a good compromise between minimum noise bandwidth and reasonable acquisition time. In practice, for burst-mode operation, it may be desirable to sacrifice some noise performance for shorter acquisition time.

3.2.6 Lock Detector Design

An indication that the PLLs are in-lock was needed. A simple quadrature lock detector was chosen. The design uses the same detector as does the phase detector, with the DG190 being switched by a quadrature square-wave signal derived from the VXCO. A simple low-pass filter

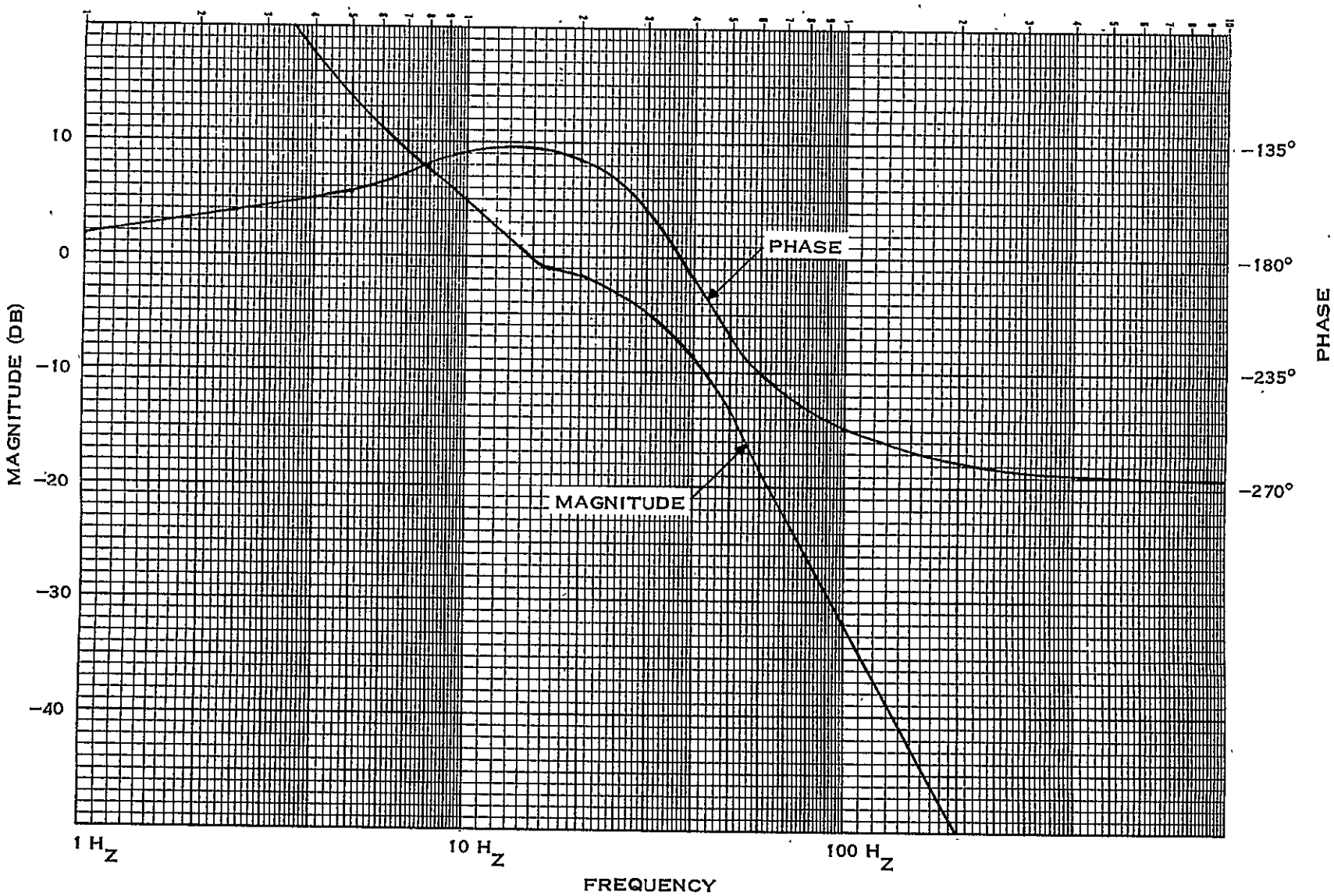

Figure 3-7. Mark/Space Phase-Lock Loop Open-Loop Response

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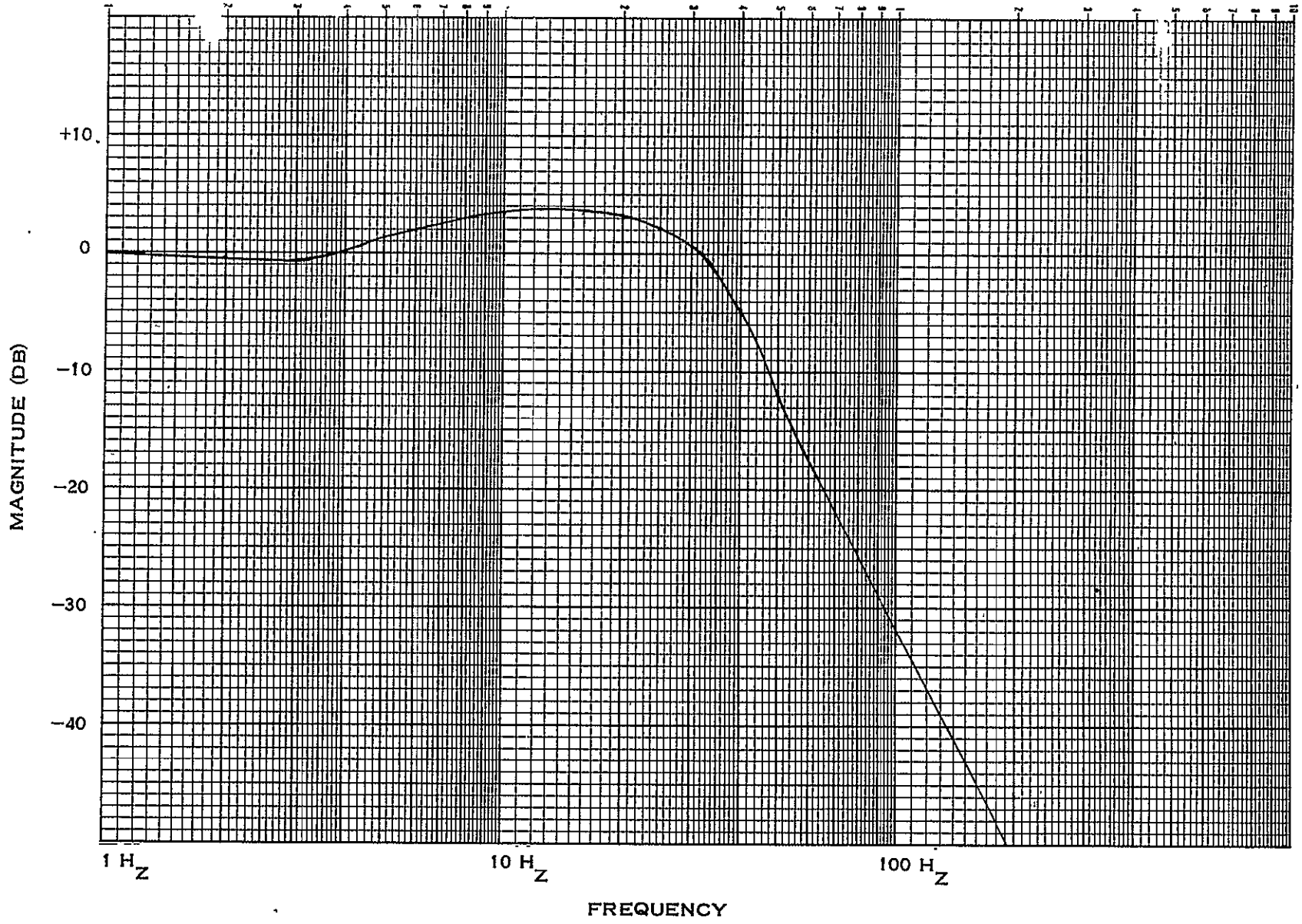

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Figure 3-8. Mark/Space Phase-Lock Closed-Loop Response

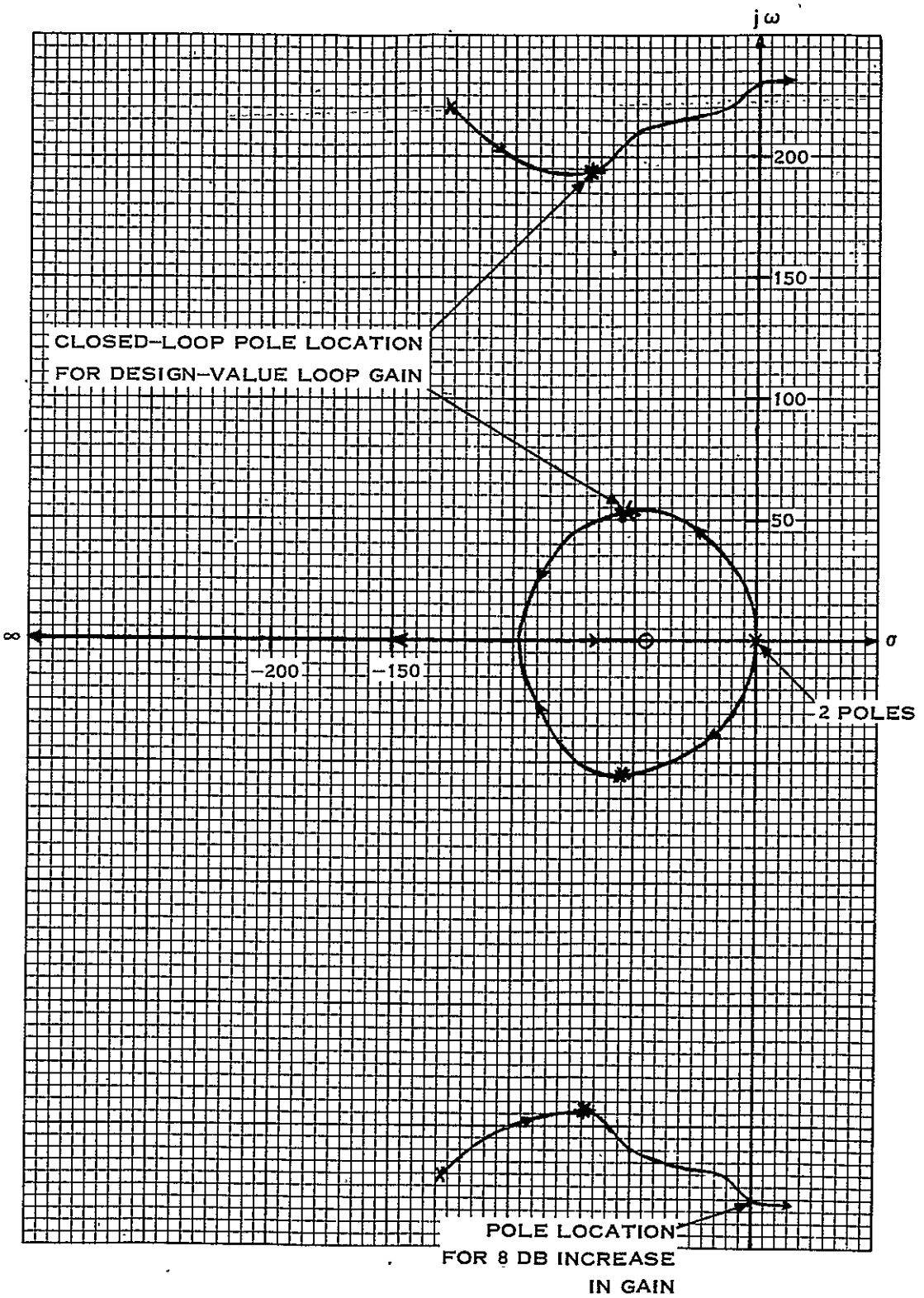

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Figure 3-9. Mark/Space Phase-Lock Loop Root Locus

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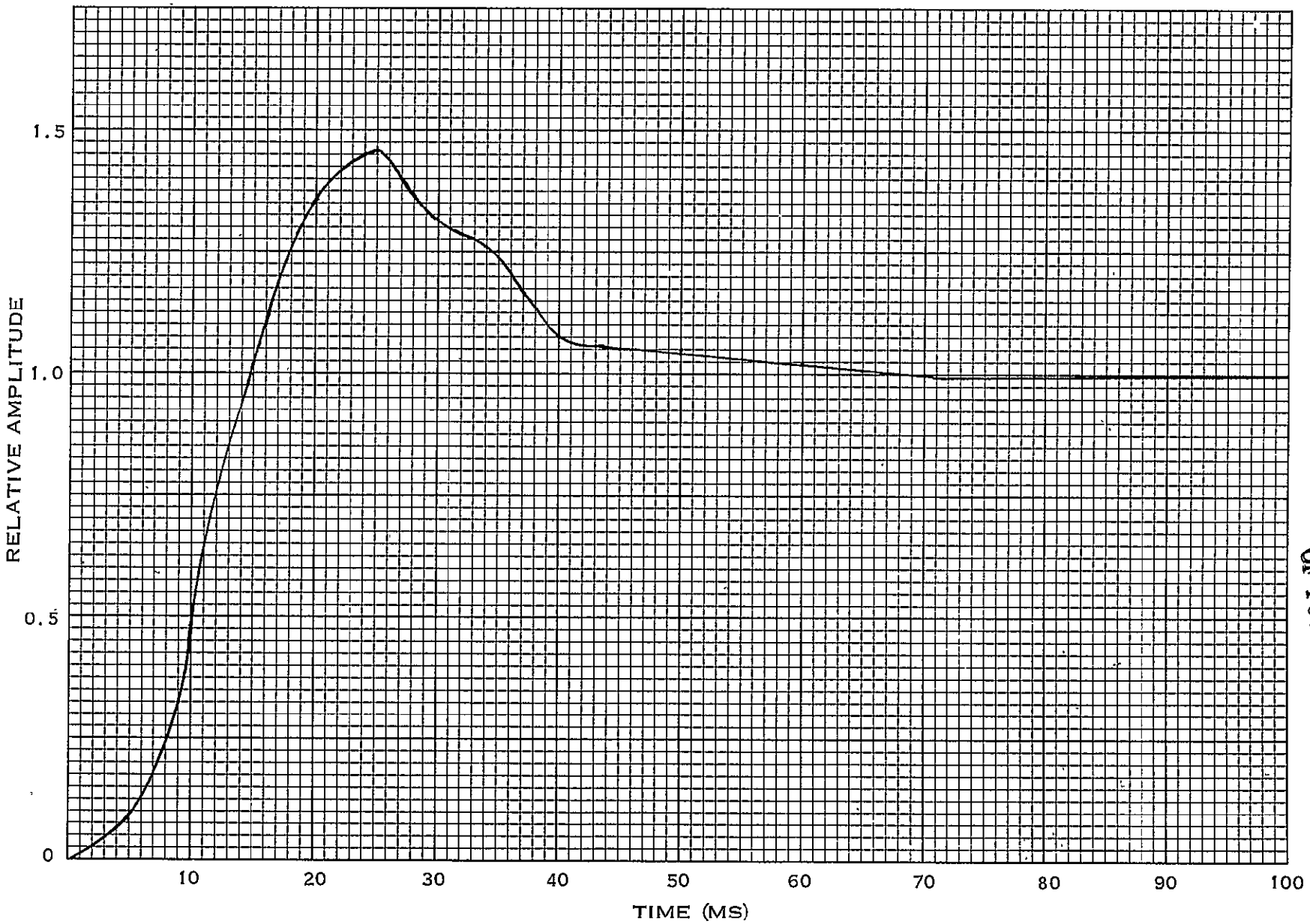

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Figure 3-10. Mark/Space Phase-Lock Loop Time Response to a Step in Phase

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removes the carrier component and the data, thus extracting the dc component. This filter also determines the time constant of the lock detector. A threshold comparator is used to make a hard decision on the average dc voltage output from the filter to determine lock. The comparator also uses a positive feedback scheme to provide hysteresis. The output is used to drive an LED indicator.

3.3 BIT SYNC RECOVERY CIRCUIT DESIGN

Bit sync is recovered simply by mixing the recovered mark and space carriers and extracting the difference frequency. This difference frequency is equal to ½ f_{ck}. This signal is used as a reference for a phase-lock loop that serves as a frequency multiplier and filter. Multiples of the clock are used for decoding and data detection.

3.3.1 Mixer Design

The outputs from the mark/space carrier recovery loops are square waves. Therefore, it is desirable to use a logic device as a mixer. Such a device is an exclusive-OR gate. Since the mark and space carriers are at different frequencies, the output of the exclusive-OR gate is a series of pulses whose width's continuously change from zero to one full period. After filtering, the pulsewidth-modulated signal yields a triangular output at the difference frequency.

The complete mixer circuit consists of an exclusive-OR gate, followed by a capacitively-coupled low-pass filter. Capacitive coupling removes the dc component. The low-pass filter rejects the RF components (≈180 kHz and greater) while passing the components of the difference-frequency triangular wave; i.e., the LPF was designed to have a cutoff frequency of 3,200 Hz. The decoupling circuit has a low-frequency cutoff frequency of 16 Hz. Hence, the circuit constitutes a BPF from 16 Hz to 3,200 Hz. The output signal has a value of ±2 V.

3.3.2 Phase-Lock Loop

The phase-lock loop multiplier must supply a multiple of the clock frequency, a data clock, and a frequency equal to half the data clock. The 1/2 f_{ck} signal must be in phase with the difference frequency derived from the mixer. The loop must function properly for both NRZ and bi-phase/Miller data. The highest reference frequency is, therefore, 320 Hz. Selecting the multiplication ratio to be 16 to simplify division, the chosen VCO frequency is 5,120 Hz.

A National LM565 monolithic phase-lock loop was selected. The reference input is converted to a square wave within the device; hence, the triangular wave is functionally equivalent to a square wave. The feedback signal to the phase detector is a square wave. The phase-lock loop is a high-gain device. When the loop is in-lock, the output signal is in quadrature with the reference. Therefore, a 90-degree phase shifter is required in the feedback circuit to place the recovered $f_{ck}/2$ signal in phase with the reference. However, it was found that the exclusive-OR mixer preceding the PLL also introduced a 90-degree phase shift, thus negating the effects of the quadrature nature of the PLL; hence, no additional phase shift is required.

The basic mixer, filter, and PLL circuit are shown in Figure 3-11. The LM565 PLL has a center frequency of 5,120 Hz. When either Manchester or Miller data are selected, a 4-stage binary counter provides a divide-by-16 function to yield an $f_{ck}/1$ frequency of 320 Hz. When NRZ is selected, and additional division by 2 yields an output of 160 Hz. The circuit also provides outputs at f_{ck} and 8 f_{ck}.

The loop bandwidth for this circuit has a design value of 10 Hz, with a damping factor of 0.7. The LM565 has a center frequency stability of ±0.2 percent, thus ensuring that the error signal will always fall within the loop bandwidth. The selected loop bandwidth is compatible with that of the mark/space PLLs. Therefore, the total acquisition time is not adversely affected. The loop parameters were calculated from published design notes for the LM565 PLL.[17]

3.4 TIMING GENERATOR DESIGN

The basic function of the timing generator is to provide properly timed sampling pulses and integrator reset pulses for the I- and Q-channel data detectors. A simplified schematic of the timing generator and its associated waveforms are shown in Figure 3-12. The input gating structure preceding the 8-bit shift register is an inhibit circuit designed to prevent a clock transition from occurring coincidentally with the J-K input. This allows the 2-MHz clock to be completely asynchronous with respect to the recovered $f_{ck}/2$ signal.

The recovered $f_{ck}/2$ square-wave clock contains all the necessary timing information. The period, 2T, is used to time the integration period. Its symmetrical square-wave characteristic is used to establish the 1-bit staggered integration relationship between the I and Q channels. The 2-MHz clock is used to detect the edges in the $f_{ck}/2$ signal and to establish the width and delay of the sample-and-dump pulses.

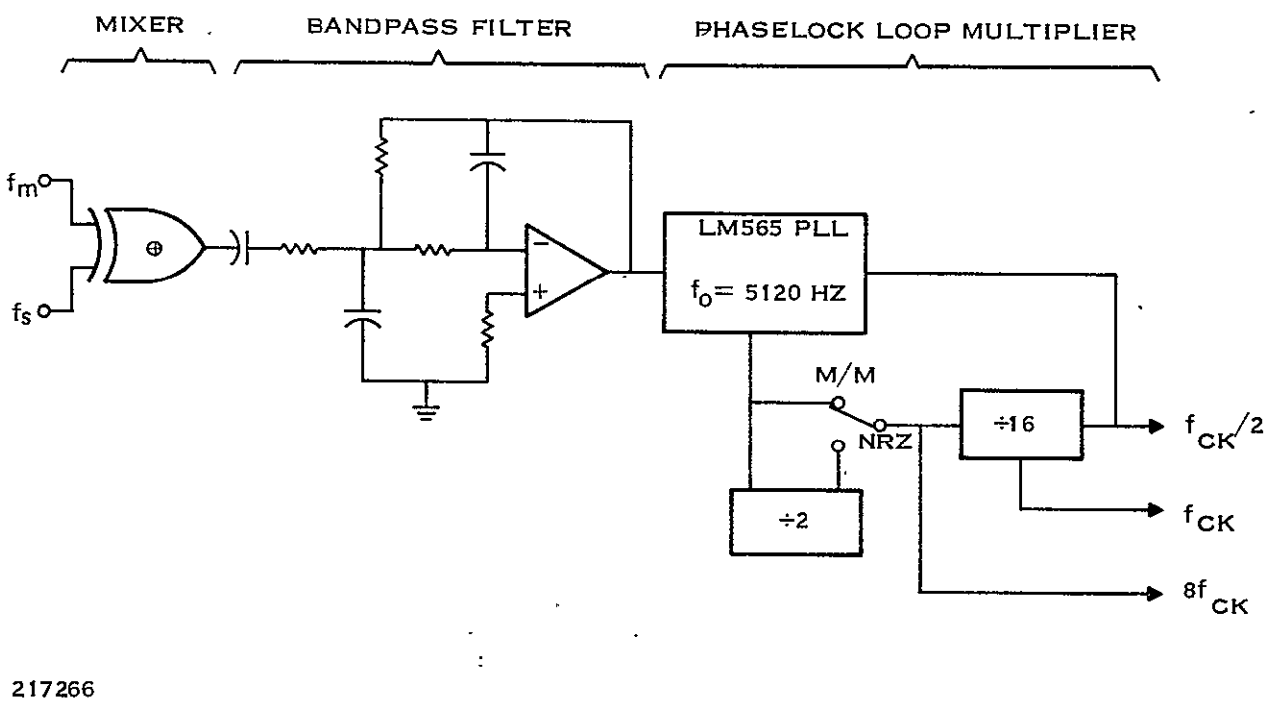

Figure 3-11. Bit-Sync Recovery Circuitry

[17] Thomas B. Mills, "The Phase-Locked Loop IC as a Communication System Building Block," from National's "Linear Applications, Vol. 1" handbook, February 1973.

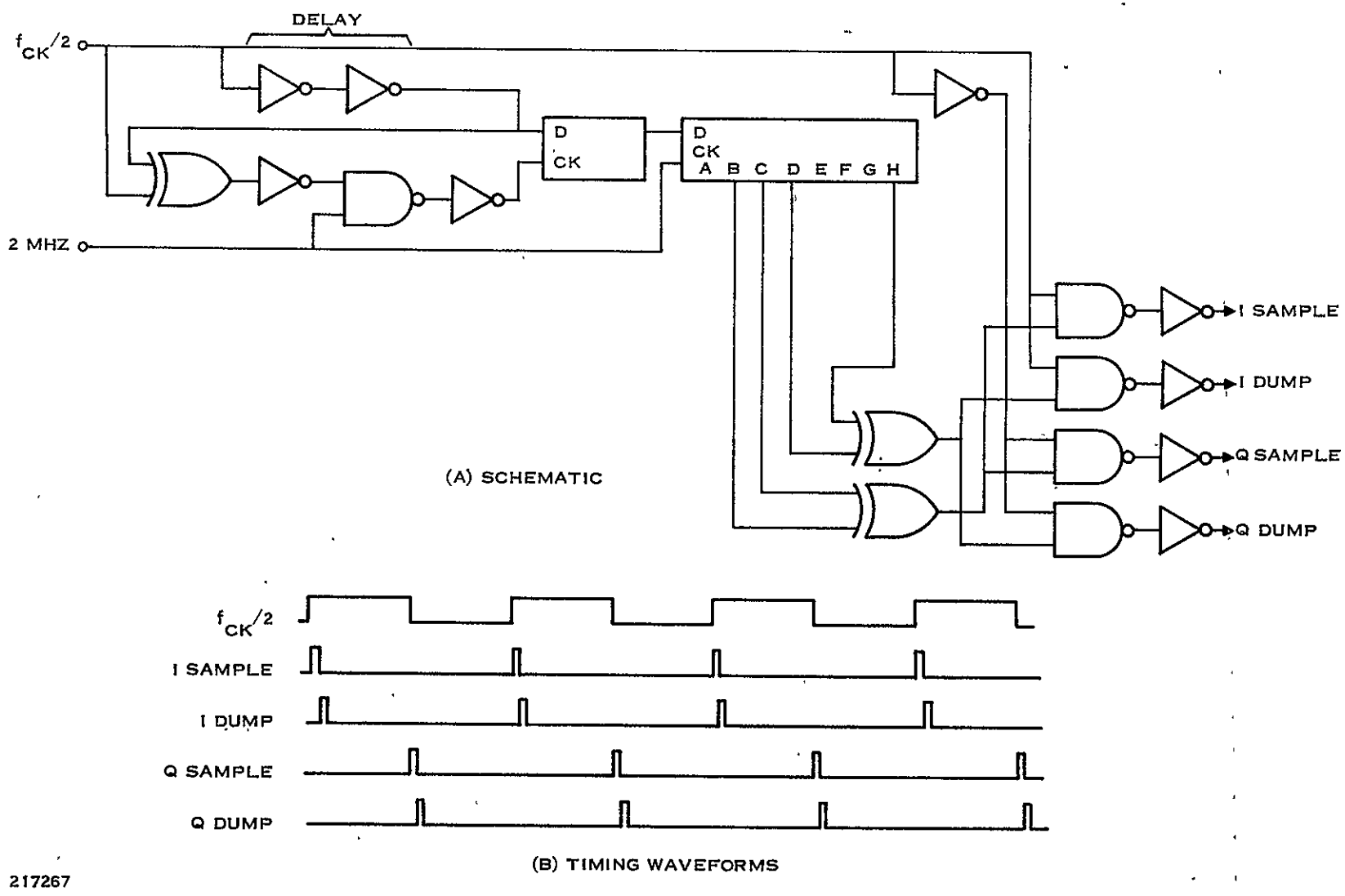

Figure 3-12. Timing Generator and Associated Waveforms

The recovered $f_{ck}/2$ square-wave signal is shifted through the 8-stage shift register by the 2-MHz clock. An exclusive-OR gate across the B-C stages of the register is used to detect each transition in $f_{ck}/2$. The output is a sequence of 0.5-μs pulse at a PRR equal to f_{ck}. This pulse sequence is ANDed with the $f_{ck}/2$; it is also ANDed with the inverse of $f_{ck}/2$ (complement) signal to produce the Q sample pulses delayed in time by 1-bit period with respect to the I-sample pulses.

A 0.5-μs delay is provided between the first exclusive-OR gate and the second exclusive-OR gate. The second exclusive-OR gate produces 2-μs wide pulses at the clock rate. These pulses are similarly gated to produce the I- and Q-dump pulses 0.5-μs after the sampling pulses. Therefore, this rather simple circuit establishes the proper timing signals to perform the data-detection function for the I- and Q-channel signals.

3.5 DATA DEMODULATOR DESIGN

The purpose of the demodulator is to provide synchronous demodulation of the MSK signal, as described in Section 2. The proper carrier required for the I-channel demodulator is cos $(\omega_o t)$ cos $(\pi t/2T)$ that is obtained by adding the recovered mark and space carriers together. The proper Q-demodulator injection signal is obtained by subtracting the recovered mark carrier from the recovered space carrier.

Unfortunately, the recovered mark and space carriers are in the form of square-wave signals. To convert these signals to sinusoids would require careful filtering (very little phase shift) to remove the harmonics. This was found to be unnecessary, however, since the input signal contains no harmonics. Therefore, linear addition of the two square-wave signals produces a fundamental at the desired frequency plus harmonics. This linear sum, when linearly multiplied by the MSK signal, results in the desired output plus several harmonic signals; the harmonics are easily removed by the matched filter. Hence, the demodulator is constructed rather simply by using an analog multiplier as the mixer and applying a square-wave carrier to one input while applying the well-filtered MSK signal to the other input. This method causes no deleterious effects on the demodulator output.

The Analog Devices AD532 monolithic multiplier was selected for the demodulator. This particular device has positive and negative inputs for both the X and Y ports. This feature eliminates the need for separate summing amplifiers to combine the mark and space carriers. A schematic of the I and Q demodulator is shown in Figure 3-13. The correct polarity to effect the proper sum or difference by the multiplier is established by inverters. An open-collector gate is used to provide precise amplitude control of the output signals. Each signal is ac-coupled into the analog multiplier. The composite MSK signal is applied to the +Y input of each multiplier. The peak-to-peak amplitudes of the two input signals are approximately equal, although this is not critical. The output from each multiplier contains RF components, a cos $(\pi t/T)$ component, and a dc component; the dc component represents the desired data for a 2T interval.

3.6 DATA DETECTOR DESIGN

The data detector is a matched filter for square-wave data. The information portion of the demodulated data is indeed a square-wave signal (the dc component) having a period of 2T. Hence, the matched filter is simply a reset integrator that is allowed to integrate for a period of

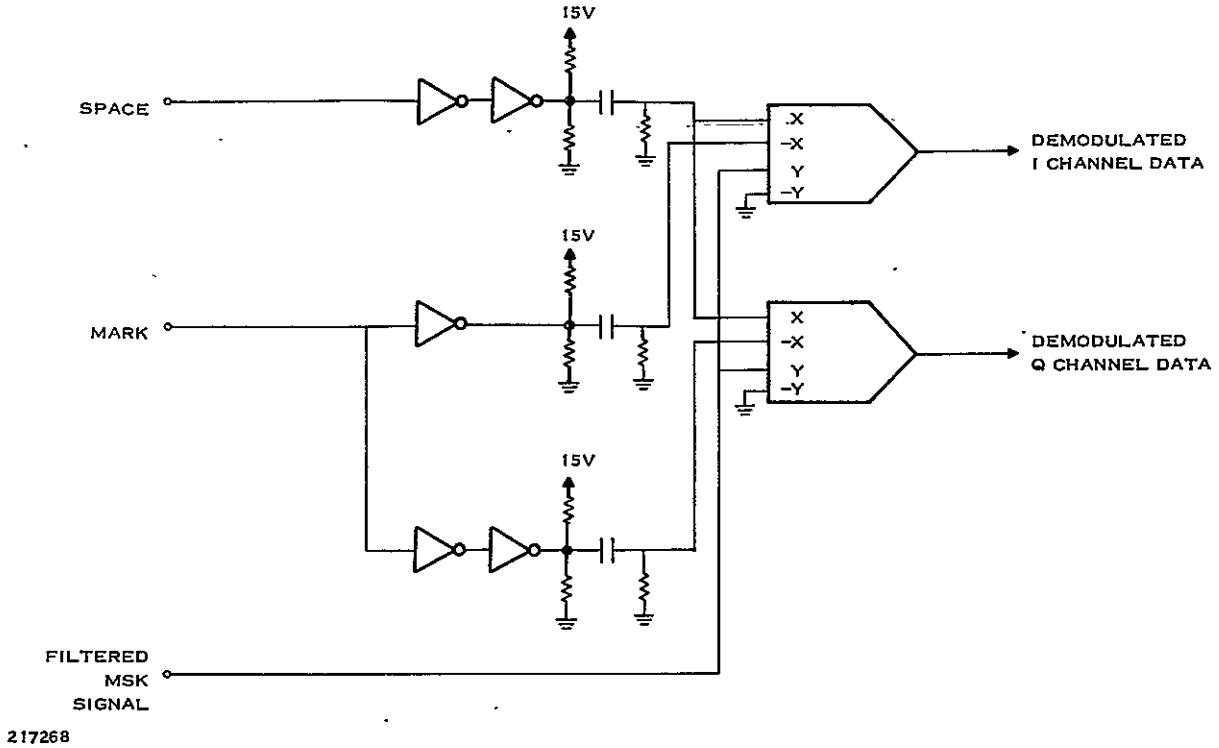

Figure 3-13. I- and Q-Demodulator Schematic Diagram

2T. The filter removes all RF components and the cos ($\pi t/T$) component. (The mean value of the integral of this sinusoid over a 2T internal is zero.) Thus, the integrator is at its peak voltage just before being reset. The integrator output may be either positive or negative.

A threshold comparator with a zero-voltage reference is used to make hard decisions on the output signal; i.e., a logic one or a logic zero is determined by the polarity of the input. The state of each comparator is sampled and stored in a 1-bit register immediately before resetting the integrator as suggested in Subsection 3.6, describing the timing generator. This has the effect of sampling the demodulated signal at the peak of the correlation function.

A schematic of the matched filter data detector is shown in Figure 3-14; the same circuit is used for both the I and Q channels. A simple operational amplifier integrator using an LM108 is shown. An analog switch (DG187) is used to reset the integrator. A 0.01-μf integrator capacitor was selected as a good compromise between minimizing stray capacitive effects and minimizing reset time. The RC time constant was chosen to yield a peak output voltage of ±5 volts. An LM111 comparator converts the bipolar output from the integrator into a logic-level signal. A single "D" flip-flop provides the digital sample-and-hold function, thus completing the data-detection circuit. The output from the flip-flops for the I- and Q-channel data detectors represents the respective I- and Q-symbol bit streams.

The data-detection circuits function the same for any data code; the only requirement is that the *effective* NRZ clock frequency be used to generate the timing signals for Manchester or Miller data. The proper conversion is accomplished by the data decoder following the data detection circuits.

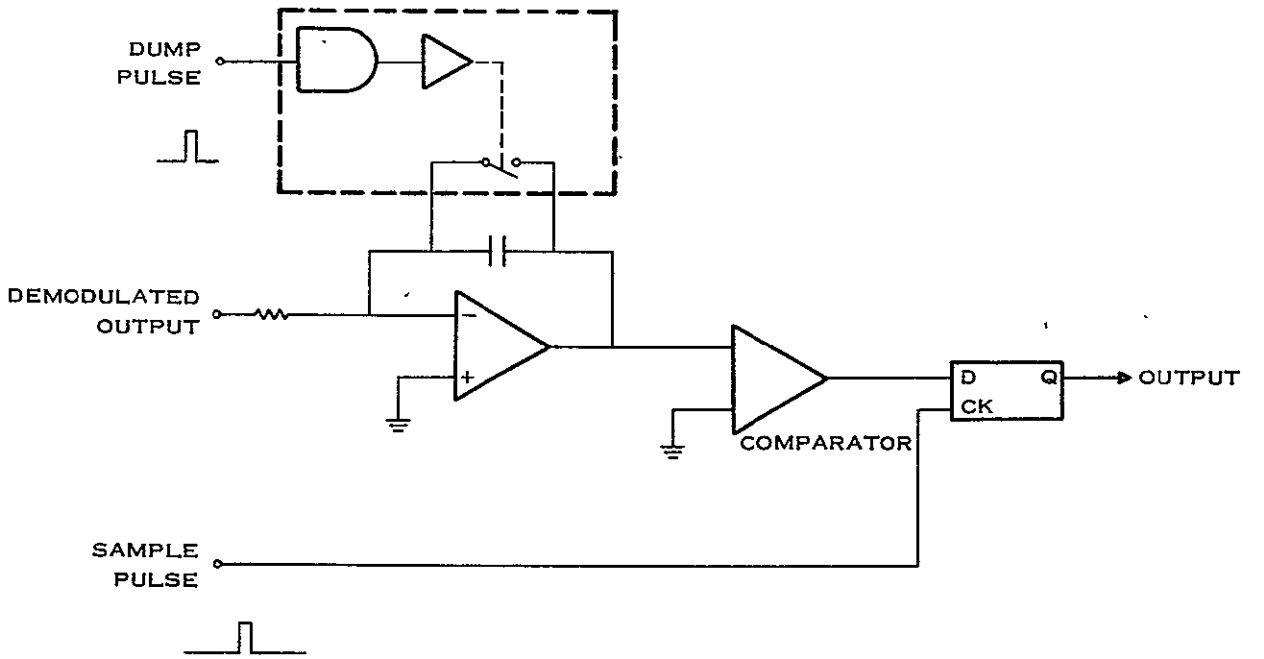

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Figure 3-14. Simplified Schematic Diagram for Data Detector

3.7 DATA DECODER

The final step in the demodulation process is the conversion of the I/Q symbols into NRZ-L data. This is obviously a function of the encoded data. The breadboard was designed to process four types of data: (1) NRZ-L, (2) NRZ-M, (3) bi-phase space, and (4) Miller generated from bi-phase space. For basic NRZ-L data, the only decoding required is a simple differential decoder (exclusive-OR gate) connected between the I- and Q-channel outputs, followed by a simple buffer register clocked by the recovered bit clock, f_{ck}.

For NRZ-M data, the data output from the above differential decoder represents NRZ-M data. Hence, another differential decoder is required to complete the conversion to NRZ-L data. Once again, this is implemented using an exclusive-OR gate across a 1-bit delay.

The use of bi-phase s data requires only the addition of another delay stage. Recall that bi-phase data uses an effective clock equal to 2 f_{ck}. Hence, the detecting and decoding are accomplished using this clock frequency. It is necessary to connect only an exclusive-OR gate across a two-stage delay, each stage being clocked by 2 f_{ck}. The output of this differential decoder is NRZ-L data. It is necessary to buffer the output, using a single register clocked by f_{ck} to synchronize the data.

Miller data requires a special decoder to convert this code back to NRZ-L data. It is accomplished precisely as described in Subsection 2.5. The output from the first exclusive-OR gate is routed to this decoder. A special 8 f_{ck} clock is used to provide edge detection. The NRZ-M bit pattern is reconstructed from these data patterns. Then, the NRZ-M data is converted to NRZ-L data by using two clock phases. A two-channel output is derived, only one of which contains valid data. An all-ones decoder is used to select the valid-data channel.

A schematic of the compound decoder is shown in Figure 3-15. The Miller decoder is not shown, since it is identical to the decoder described in Subsection 2.5.

3.8 AGC CIRCUIT

The proper operation of the mark/spare phase-lock loops depends on maintaining a constant amplitude input to the phase detectors. This can be achieved by using a limiter or an AGC circuit. The AGC method was chosen to ensure linear operation and to realize maximum performance in low S/N ratio conditions. A simplified schematic of the selected AGC design is shown in Figure 3-16.

A junction FET is used as a voltage-variable resistor is an attenuator circuit. Resistor R2 and the FET form the attenuator. When the FET is off, the circuit offers minimum attenuation and, hence, maximum overall gain. Resistor R_{10}, capacitor C, and the diode CR_3 form a rectifier and peak detector. The attack time is determined by the time constant $R_{10}C$. The release time (and, hence, stability) is determined by R_9C. A voltage-follower isolates the detector circuit from the threshold comparator. The peak dc voltage is thus applied to the comparator circuit.

The comparator circuit essentially adds the negative dc voltage from the detector to a voltage set by the threshold reference voltage derived via R_7 and R_8. If the sum is positive, the output from the comparator operational amplifier is negative and diode CR_2 is forward-biased. Resistors R_3, R_5, and R_6 are selected to have the same value; hence, a negative voltage is maintained at the output of the operational amplifier and diode CR1 is reverse-biased. The circuit continues to operate at maximum gain as long as the detected signal is below the AGC threshold.

When the detected signal exceeds the AGC threshold voltage, a net negative voltage exists at the input to the comparator operational amplifier; a net positive voltage is thus produced at the output of the operational amplifier. Diode CR_2 is reverse-biased and the gain is determined by the ratio R_4/R_5. This amplified difference voltage is applied to the gate of the FET. The resistance of the FET is decreased and, hence, the overall gain is decreased. The result is automatic regulation of the output voltage to maintain a peak output equal to the AGC threshold.

The AGC circuit was modeled on the computer, using a nonlinear modeling program. The parameters were scaled to minimize run time. The selection of the proper time constants (R_9C and $R_{10}C$) was obtained using this method. In addition, a good estimate of the transient nature of the circuit was obtained. The actual measured performance of the AGC was close to that obtained with the model. The final detailed circuit design is contained in Appendix B.

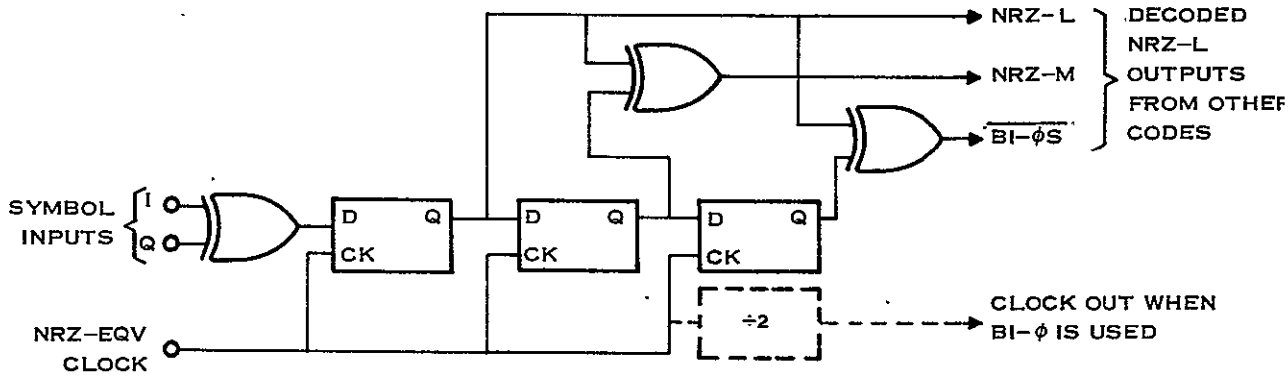

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Figure 3-15. Decoder for Three Codes

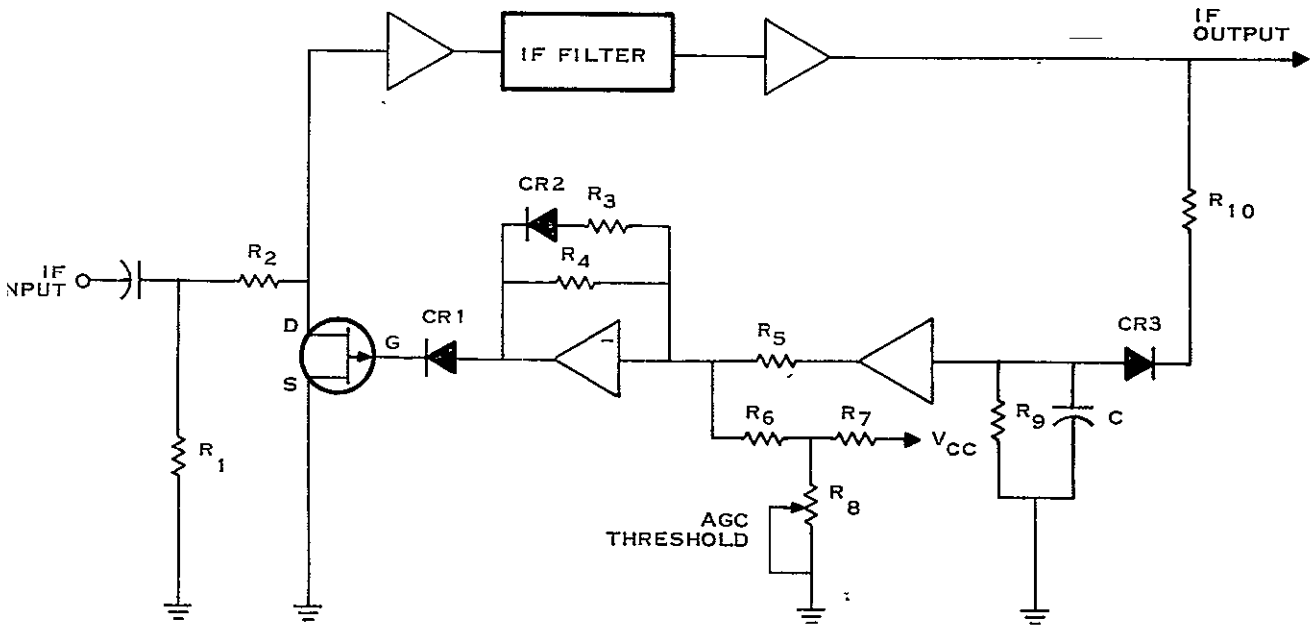

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Figure 3-16. Simplified AGC Circuit Schematic Diagram

SECTION IV
BREADBOARD TEST RESULTS

The main goal for this phase of the study of Advanced Data Collection/Position Location Systems was to build and test a coherent demodulator for MSK signals. The principles for the coherent demodulator were discussed in Section 2 while the circuitry was described in Section 3. A block diagram of the coherent demodulator is shown in Figure 3-1. The entire coherent demodulator, except for the 180-kHz crystal filter, was constructed on a single circuit card measuring 5.1 by 10.0 inches. A photograph of this breadboard demodulator is shown in Figure 4-1.

Several key performance measurements were made using the coherent demodulator. Among these were:

1. BER versus signal-to-noise ratio (E_b/N_o) for NRZ, Manchester, and Miller encoded data.
2. Time required to acquire and lock to messages transmitted in the burst mode as a function of E_b/N_o.
3. Ability of the mark/space phaselock loops to maintain lock for various codes and E_b/N_o ratios.
4. Time to accurately measure the frequency in the presence of data and noise.
5. Mutual interference as a function of channel separation.
6. Effects of bandwidth-limiting on the BER performance of MSK signals.
7. Effects of amplitude-limiting on the BER performance of MSK signals.

In addition, the performance of a simplified noncoherent FSK-type modulator was evaluated in conjunction with the coherent demodulator. The results of all tests are presented in this section.

4.1 BER TEST RESULTS

The BER performance as a function of signal-to-noise density (E_b/N_o) was measured for three types of MSK data. These tests were performed using a pseudorandom noise (PN) code having a length of approximately 32K bits. The continuous MSK data was summed with additive white Gaussian noise. The noise power density was calibrated using a filter having a known noise bandwidth. The noise power density and E_b/N_o ratio was established before the narrowband filter and AGC amplifier to evaluate the effects of these elements on BER performance.

The first set of data was obtained using the digital MSK modulator, continuous PN data, AGC in the receiver, a crystal filter with a 3-dB bandwidth of 900 Hz, and the coherent demodulator. The signal amplitude and noise level were adjusted so that the AGC was fully functional over all ranges of E_b/N_o ratios for which the tests were conducted, but low enough that no nonlinearities were encountered, even on noise peaks. The system was calibrated for a fixed amplitude; then the E_b/N_o was precisely established using a precision attenuator to vary the signal amplitudes. The tests were conducted for NRZ data, Manchester (bi-phase space) data, and Miller data. The results of numerously repeated tests are shown in Figure 4-2.

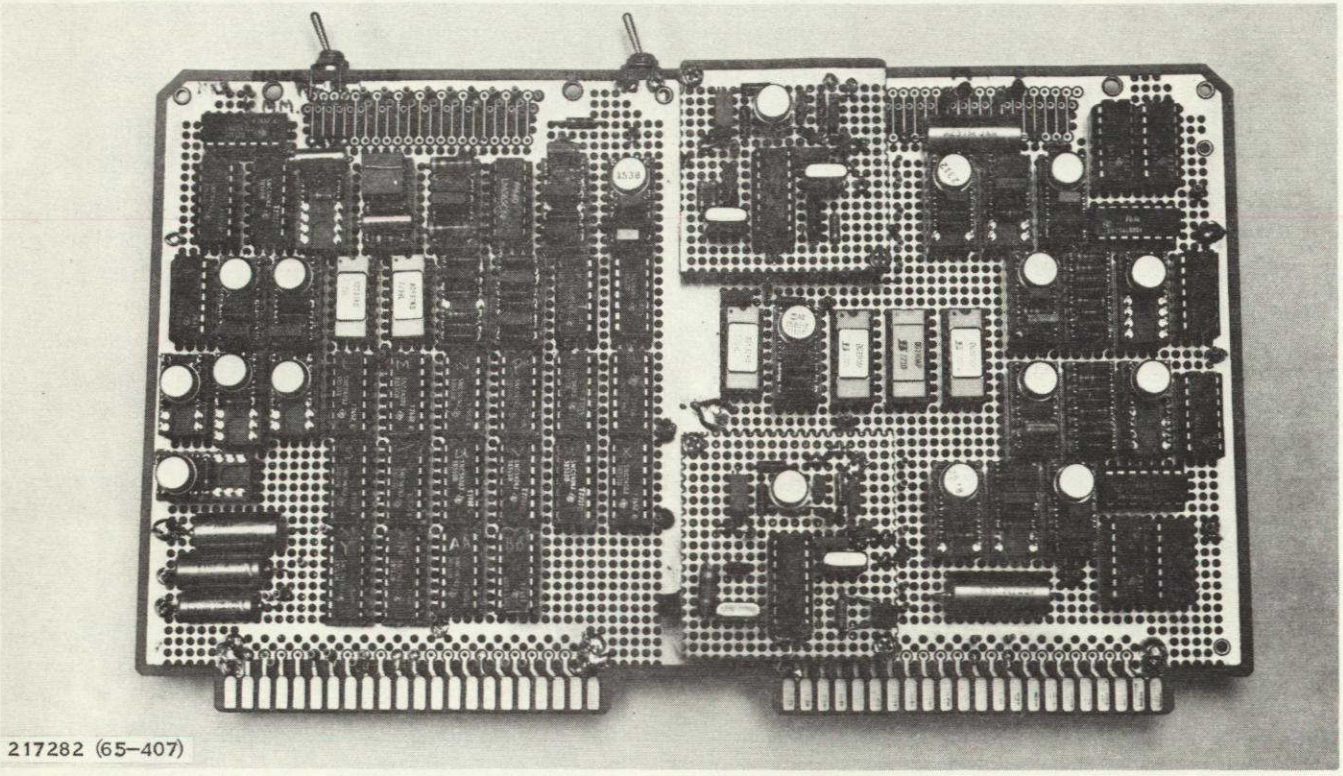

Figure 4-1. Breadboard MSK Coherent Demodulator

For reference, the theoretical performance of PSK modulation using NRZ data is included. (This is also the approximate theoretical reference for NRZ/MSK.) Note that the actual performance of NRZ/MSK data differs significantly from the expected theoretical performance, particularly for high signal-to-noise ratios. This is attributable to the inability of the mark/space PLLs to maintain a good estimate of carrier phase when NRZ data is transmitted. This is to be expected since random NRZ data can have periods of infrequent transitions, i.e., long strings of ones (mark) or zeros (space). This phenomenon is characterized by the nonparallel relationship of the measured performance curve with respect to the theoretical curve.

A second reference curve, the theoretical performance curve for Miller/MSK data, is also shown. This is the actual theoretical performance to be expected of an ideal Miller/MSK system. The curve is based on a maximum integration time (in the matched filter) of one bit period where a bit period is referenced to NRZ data. This curve also contains an allowance for the differential encoding effects inherent in MSK. Even though the curve is designated only for Miller encoded data, it is also valid for Manchester data when a filter matched to one bit period is used in the data detector, as in the case for the breadboard system.

The system was configured for bi-phase (Manchester) data. The same performance measurements were made with E_b/N_o being calculated based on the actual bit time, not the effective bit time. Therefore, the Manchester/MSK data plotted in Figure 4-2 is normalized to the actual bit rate. This data is only 2 dB off the theoretical curve. Part of this loss in performance is caused by minor errors present in the phaselock loops and demodulators, and part of this loss is caused

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by energy lost in discrete tones present in Manchester data. (These tones are observed in spectral photographs for Manchester data.) However, this represents a 3.5- to 4.0-dB improvement over the best performance achieved with the noncoherent demodulators tested previously (Main Report, Figures 3-32 and 3-33A). The curves for the coherent demodulator include the effects of clock recovery, while those for the noncoherent demodulators do not. Also, note that the measured performance curve for Manchester data follows the theoretical curve rather consistently, indicating that the mark/space phaselock loops have negligible deleterious effects on the BER performance. By comparing the BER performance of Manchester data with that for NRZ data, the advantage of the more frequent mark/space transitions offered by Manchester encoding becomes obvious. Even though NRZ data has a theoretical advantage over Manchester data, this advantage is difficult to realize in a practical low-data-rate system; in high-data-rate systems, this effect is diminished. (High data rate here refers to rates greater than 10 KBPS.)

The system was configured for Miller data and a set of performance measurements was taken. The BER for Miller data is plotted in Figure 4-2. Note that the curve is only 1 dB off theoretical and indicates a 0.5- to 1.0-dB improvement over Manchester data. This improvement results mainly from the fact that the spectrum for Miller/MSK data contains no significant energy in discrete spectral lines. The spectrum of Manchester/MSK data does. The curve for Miller data is also well-behaved, indicating proper operation of the mark/space phaselock loops. The BER performance shown for Miller data also includes the effects of the special pattern decoder. The close tracking of the measured curve with respect to theoretical indicates that the 5-bit code comparison produces a negligible number of false channel selections. This is a significant finding for the practical use of Miller data in such a system. Therefore, the use of Miller/MSK appears to be the best choice for low-data-rate data collection systems, from a BER performance viewpoint.

To determine the effects of bandwidth limiting produced by the crystal filter, a BER performance test was conducted after substituting an LC filter having a bandwidth of 12 kHz for the crystal filter. The results are shown, for comparison with other demodulators, in Figure 4-3. There is almost no difference in the BER performance between the Miller/MSK data in Figure 4-2 and the equivalent data in Figure 4-3. This indicates that the bandwidth-limiting action of the narrow crystal filter having a bandwidth of 3R (equivalent to 1.5R for Miller encoded data) has no significant effect on BER. This is not surprising since Mathwich[18] has shown that no significant degradation occurs for bandwidths as low as 0.75R.

Figure 4-3 also compares the coherent demodulation of MSK with the noncoherent demodulation of MSK and RAMS. The coherent demodulator provides a 4-dB improvement over the best noncoherent demodulator tested. Furthermore, it provides from 1- to 3-dB improvement over that achieved on RAMS using ±60-degree PSK. Even though the measured MSK/Miller performance is 5 dB off the theoretical curve for BPSK using Manchester data, it is only 2-dB inferior to the best measured performance achieved, using ±60-degree PSK and Manchester data. Therefore, the use of MSK/Miller data and a coherent demodulator for low-data-rate transmission systems similar to RAMS approaches the best practical combination.

[18] Mathwich.

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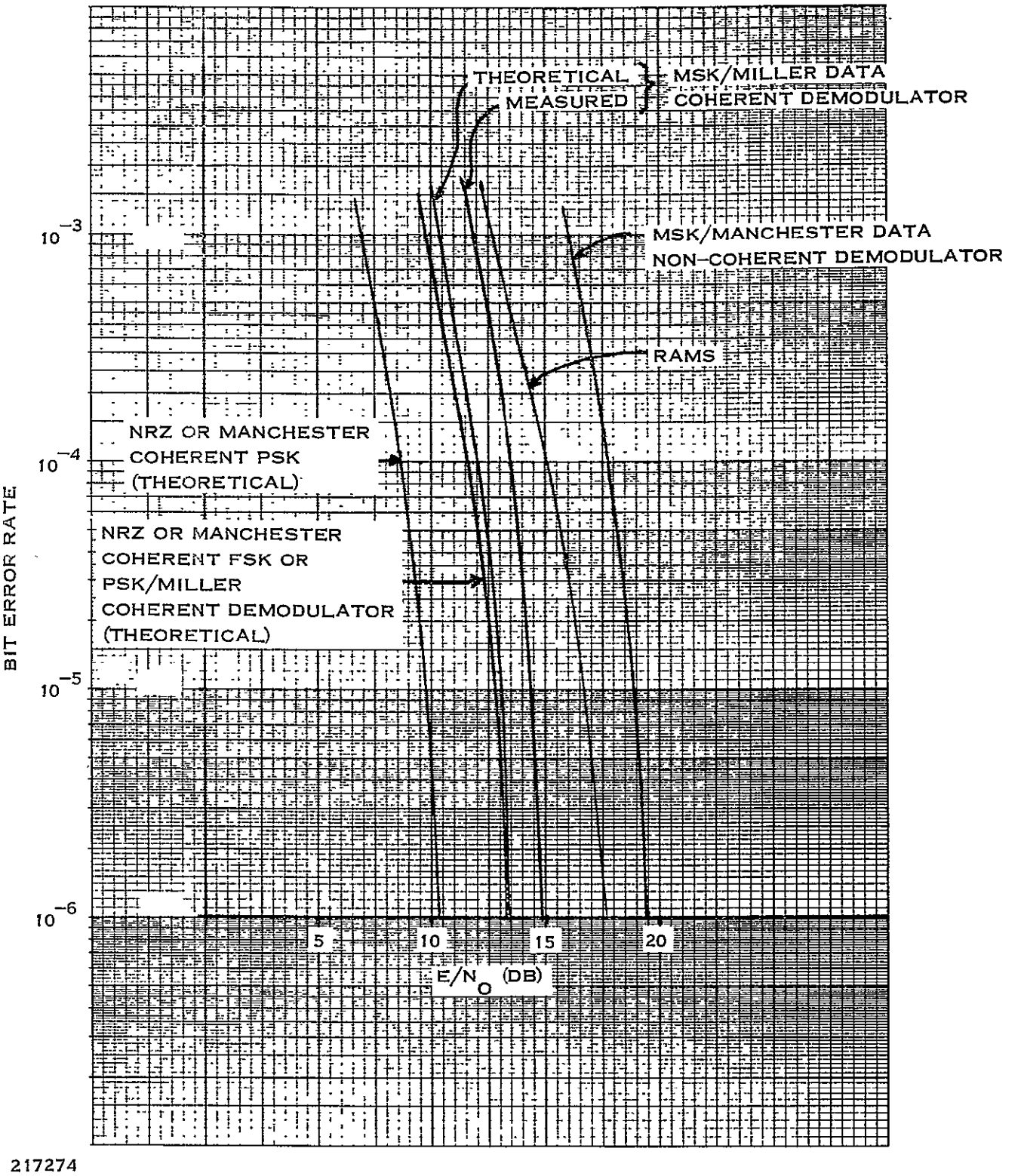

Figure 4-3. Comparison of Coherent MSK Demodulator With Other Demodulators

A key consideration for the application of MSK to data-collection systems is the practicality of simply generating the MSK signal. The problem has been addressed recently by Amorosa and Kivett[19] by using amplitude modulation to produce antipodal BPSK, followed by a suitable filter to synthesize the MSK signal. This method is limited to cases where the ratio of carrier to bit rate is large; this is the case for application in data-collection systems. A second method of generating only MSK signals was considered in this study.

The concept for this design is based on the single-oscillator FSK approach. It too is limited to cases where the data rate is low with respect to the oscillator frequency. The phase-continuity requirement for MSK is achieved rather simply, since the phase of a crystal oscillator cannot change rapidly because of the Q of the crystal. The spectral characteristics of an MSK signal generated in this manner have already been discussed in Section 2 and are no different from those generated using the digital oscillator approach.

The question of BER performance when using a noncoherent demodulator to demodulate such a signal was addressed in the main body of this report; the results obtained showed that the VCXO approach produced almost identical results as those obtained using a true MSK generator. This phase of the study sought to test the VCXO approach to MSK generation by using the coherent demodulator. The test was conducted using Manchester data. The results show that the BER performance is almost identical to that obtained using the true MSK modulator. In fact, no separate curve was plotted because of the almost identical BER results obtained with this method. This represents a significant milestone in the practical application of MSK to low-data-rate data-collection systems. The only critical parameters imposed on the VCXO design are the short-term stability of the VCXO frequency (needed to ensure the accuracy of frequency measurement for Doppler-shift determination) and reasonable accuracy in maintaining the modulation index at 0.25.

The effect of amplitude limiting in the presence of noise on the BER performance is a final consideration in this section. The coherent demodulator was designed to use AGC for level control. However, an amplitude limiter was built and substituted for the AGC circuit. The limiter was installed ahead of the crystal filter to ensure that the harmonics produced by the limiter would be removed. (In a practical system, this would not be desirable because of cross-modulation effects when many received signals are present. The limiter should follow the channel filter and the limiter should be followed by a harmonic filter.) The same test setup was used to perform the BER test, first with the limiter and then with AGC. Manchester data were used in both cases. The results of these tests are plotted in Figure 4-4. The limiter causes a 1-dB degradation in performance.

4.2 BURST-MODE PERFORMANCE DATA

The system was configured to operate in the burst-data mode, using Miller data. The bit sync code length was set at 24 bits. The message length was set at 128 bits. The system E_b/N_o range was adjusted to span the same range as that used to determine the continuous-mode BER performance. The system was set to transmit 100 messages. The system was started and allowed to transmit 100 messages for each E_b/N_o setting from 7 dB to 18 dB, in 1-dB steps. The system successfully received all 100 messages for E_b/N_o greater than 12 dB. The remainder of the data

[19] Frank Amorosa and James A. Kivett, "Simplified MSK Signaling Technique," IEEE Transactions on Communications, Concise Papers, April 1977.

is plotted in Figure 4-5. The theoretical curve was obtained from the theoretical BER curve for a 128-bit message by:

$$P_s = (1 - P_e)^{128}$$

The calculation disregarded the error pairing caused by differential encoding since a single error causes loss of the message.

The measured data points follow the theoretical curve rather closely—well within the error to be expected in such measurements. Note that 10 dB is the minimum E_b/N_0 necessary to ensure a 90-percent probability of success for a 128-bit message; 13 dB is needed to produce an expected success probability greater than 99 percent. (Longer messages would require greater signal-to-noise ratios to ensure the same probability of success; shorter messages, smaller signal-to-noise ratios.) A forward error correcting (FEC) code would improve the probability of success for low signal-to-noise ratios. The rather close tracking between measured and theoretical data indicates the ability of the mark/space phaselock loops for successful acquisition in the presence of noise. However, the minimum bit sync code duration needs to be at least 50 ms (16 bits at 320 BPS) to ensure adequate time for acquisition.

Similar results were obtained for Manchester data. However, NRZ data produced poor results because of the lack of continuous data transitions. Therefore, NRZ is not a good choice for burst-mode operations in low-data-rate systems.

4.3 POWER SPECTRAL DENSITY MEASUREMENTS

The spectra of MSK data generated from three different data codes were obtained using the HP141 spectrum analyzer. The analyzer was connected to the 20-kHz output of the MSK modulator. Photographs for NRZ, Manchester, and Miller data are shown in Figure 4-6. The spectrum for NRZ/MSK shown in Figure 4-6 can be compared with the theoretical PSD shown in Figure 2-7. The actual measured spectrum is observed to be very close to the calculated PSD. Note that there are no discrete spectral lines in the spectrum for NRZ/MSK data. Also, note that most of the power is contained in a bandwidth less than 1R.

The second photograph in Figure 4-6 shows the measured PSD of Manchester/MSK data. Note the presence of discrete spectral lines at f_o and at multiples of the data clock frequency of 320 Hz. These discrete lines are superimposed on the spectrum of random data having characteristics very similar to that produced by random NRZ data having a clock rate of 640 Hz. Unfortunately, no theoretical PSD is available for Manchester/MSK data.

The third photograph in Figure 4-6 shows the spectral characteristics of Miller/MSK data. Note the similarity between this PSD and that of NRZ/MSK. The spectrum is almost identical to that obtained from NRZ data with a data rate of 640 BPS. There are no discrete spectral lines for this data. The primary data lobe is approximately 2R (640 Hz) wide for a data rate of 320 Hz. Note the slight peaking in the PSD near f_m and f_s. The PSD characteristics indicate that this code can be treated as NRZ data with a data rate of 2R or 640 BPS. This is in agreement with the BER performance discussed earlier.

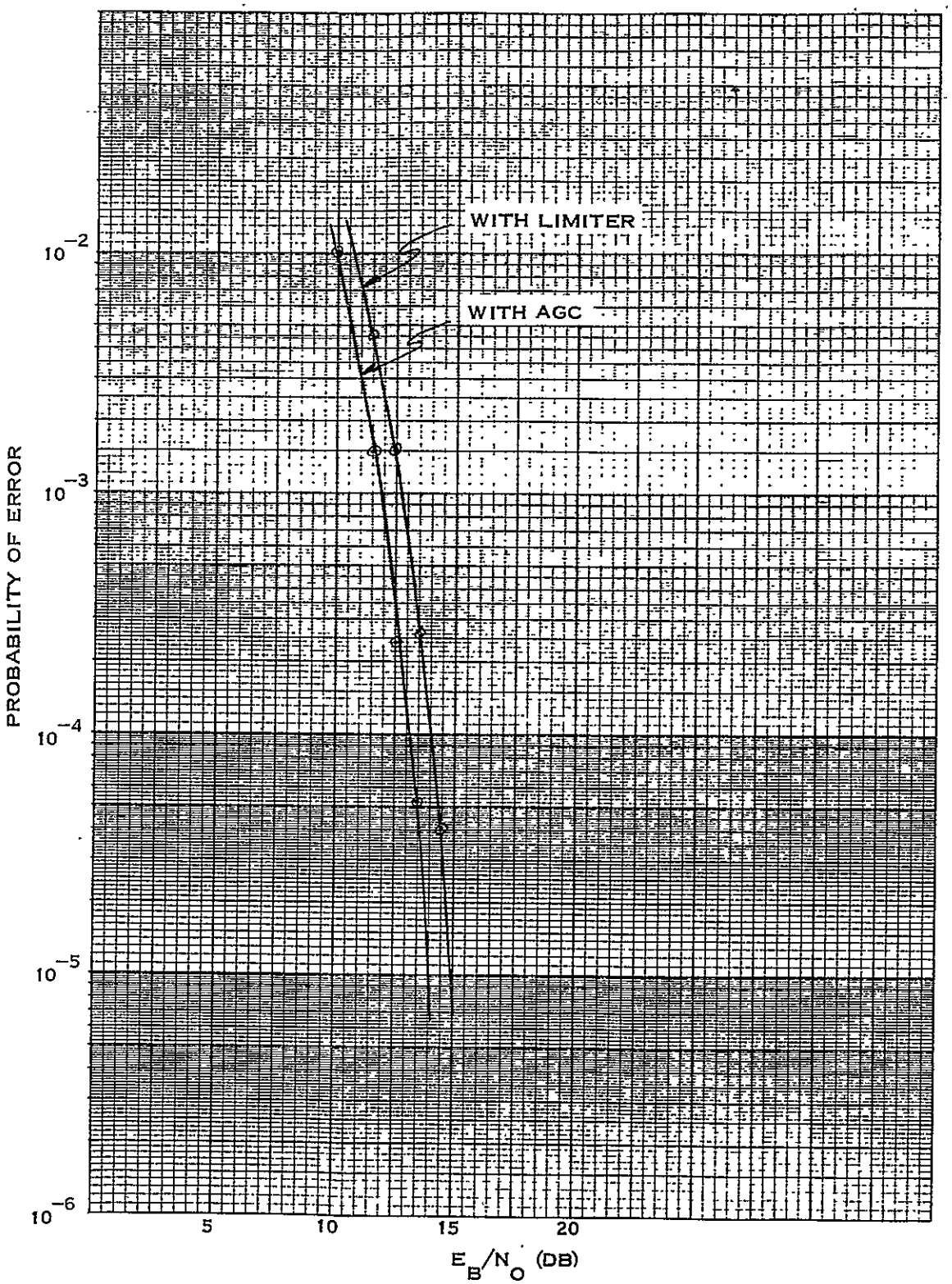

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Figure 4-4. Effects of Amplitude Limiting on BER

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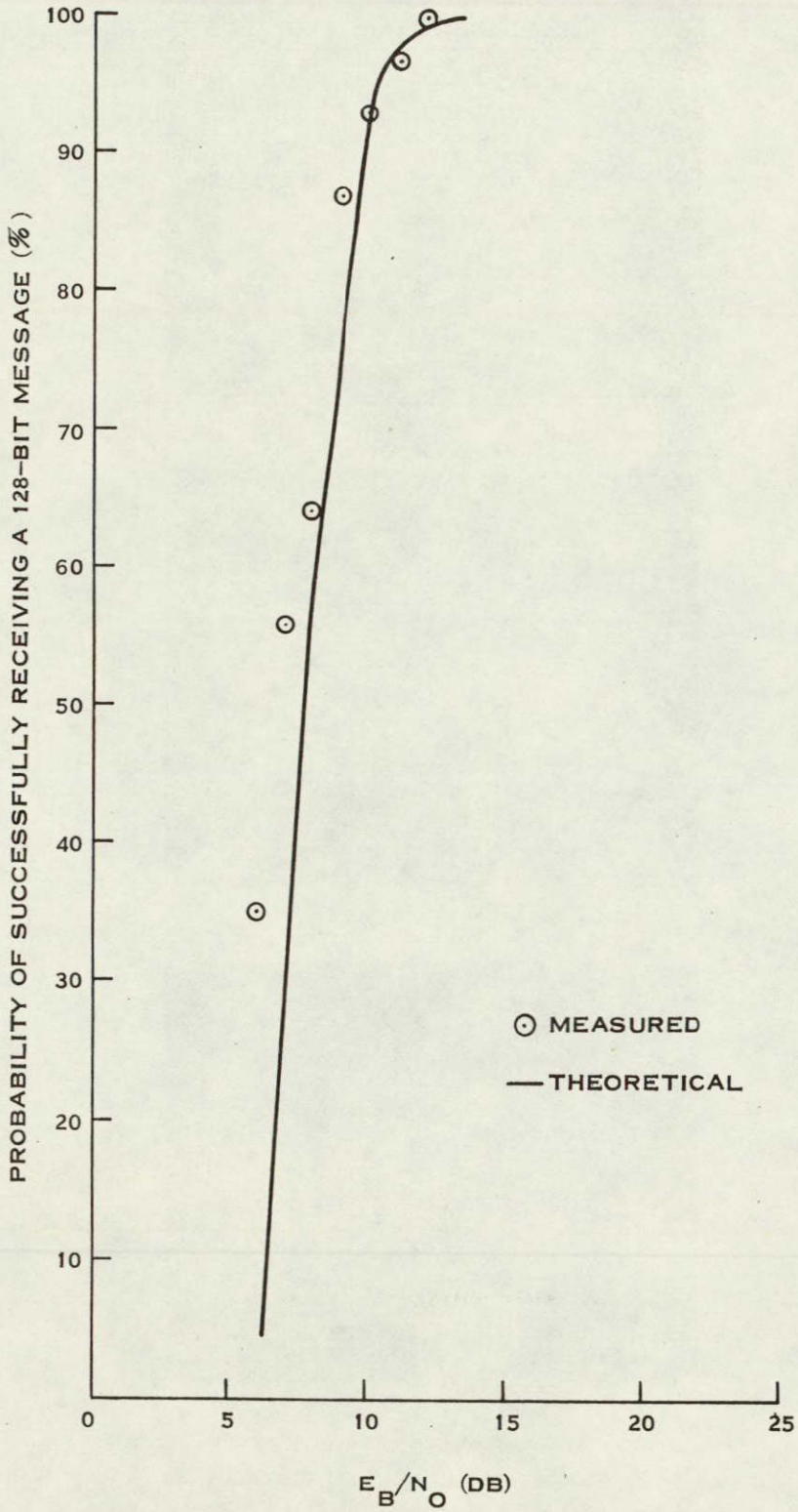

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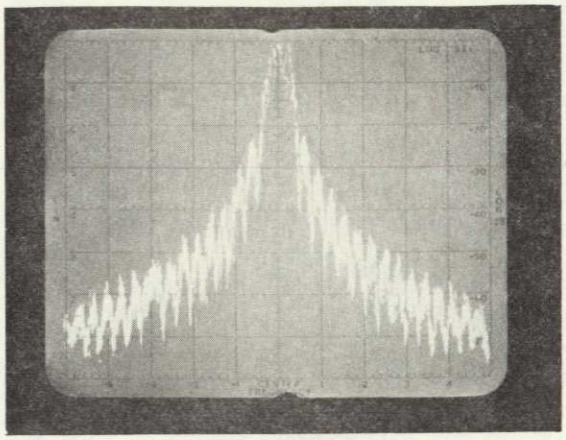
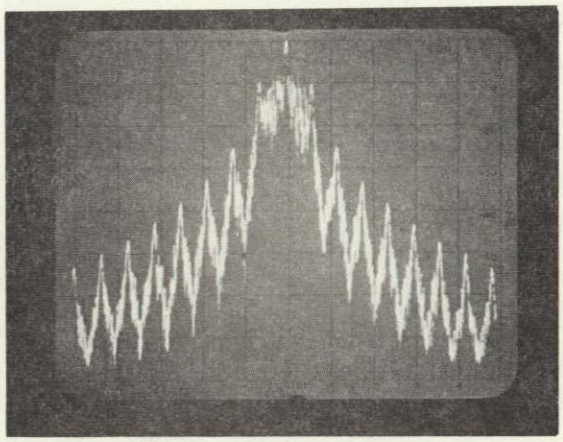
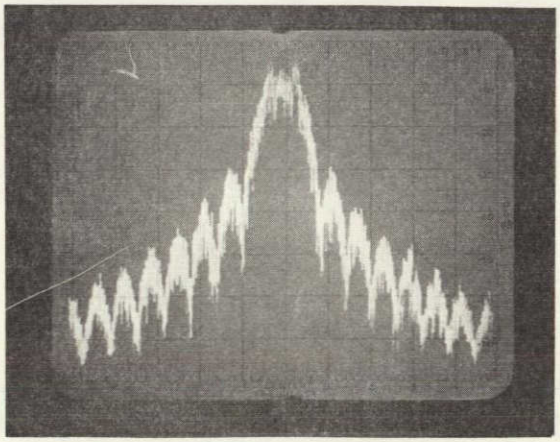
Figure 4-5. Burst Mode Performance Curve



(A) NRZ/MSK DATA



(B) MANCHESTER/MSK DATA



(C) MILLER/MSK DATA

ALL PHOTOGRAPHS TAKEN WITH A VERTICAL SCALE OF 10 DB PER DIVISION AND HORIZONTAL SCALE OF 500 HZ PER DIVISION. DATA RATE IS 320 BPS.

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Figure 4-6. Spectra of Unfiltered MSK Signals

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The PSDs of both Manchester and Miller coded MSK data, after filtering by the 180-kHz crystal IF filter, are shown in Figure 4-7. Note that the sidelobe attenuation is over 50 dB for frequency displacement greater than ±3R. This permits channel spacings of ±3R. The main data lobe is unaffected.

The PSDs of the MSK signals, after being squared, are shown in Figure 4-8. The PSD is almost identical to that of CPFSK, with a modulation index of 0.5 and a data rate of 640 BPS. Note the generation of discrete spectral lines at ±320 Hz; these lines provide the references for the mark/space phaselock loops.

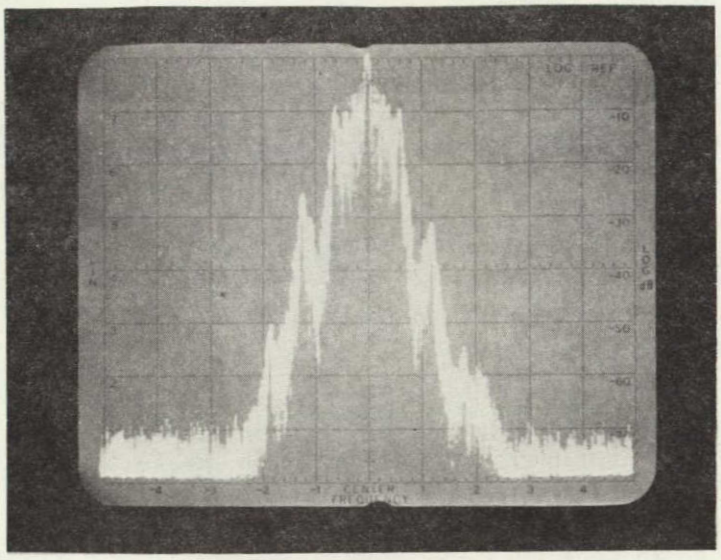
4.4 MARK/SPACE PHASE-LOCK LOOP ACQUISITION TIME

The system was configured for burst-mode operation. The data generator was set to produce 45 bits of bit sync, 16 bits of frame sync, and 128 bits of message data for a message length of approximately 600 ms. Bi-phase space coding was used for this test. The message repetition rate was approximately one message every 2 seconds. An oscilloscope was set to trigger on the message-start pulse; the vertical inputs were connected to the mark and space phase detector filter outputs. The results of this test are shown in Figure 4-9. Note that the loops acquire lock in less than 100 ms and that all transients are damped within 200 ms. The major acquisition transient is completed within 50 ms. However, the acquisition transient is longer in the presence of noise. It appears that it may be necessary to increase the acquisition-loop bandwidth at the expense of noise rejection for burst-mode operations to keep the acquisition time less than 100 ms.

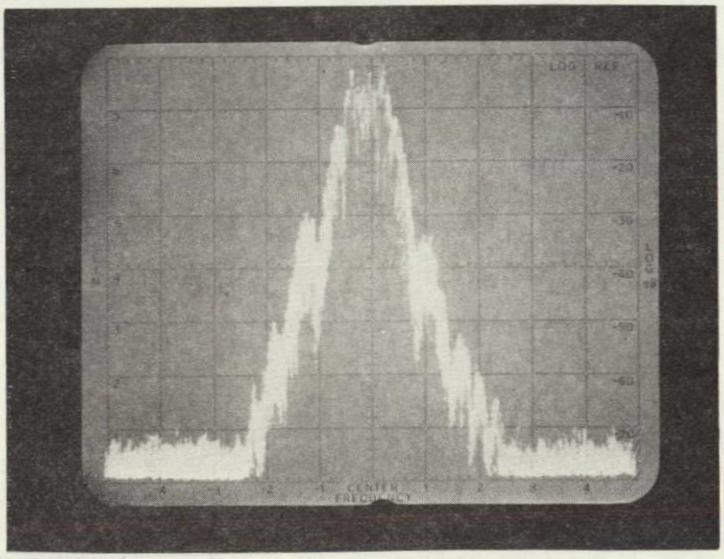
4.5 FREQUENCY MEASUREMENT ACCURACY

A key question to be answered as part of this study was whether or not the frequency of the recovered mark or space carrier could be measured accurately enough, in the presence of data modulation, to provide good Doppler resolution. The required accuracy is at least ±0.5 Hz. The time of the measurement is limited to 100 ms. The method used to achieve these requirements is to measure the frequency of the direct output from the mark phase-lock loop VCXO that operates at 18,016,000 Hz for Manchester or Miller data (or 18,006,400 Hz for NRZ). This frequency is 100 times the frequency for which the accurate measurement is desired. Therefore, a 0.1-second measurement period allows the frequency measurement of the 180.160 (or 180.064) kHz signal to be made within ±0.1 Hz, ignoring the effects of noise and data.

The system was set up for burst-mode operation. A 45-bit bit-sync code, a 16-bit frame-sync code, and a 128-bit message length were selected. This resulted in a message duration of 0.6 second. A counter was connected to the buffered output from the 18-MHz VCXO. The system master oscillator was adjusted to provide a frequency indication of 18,016,000 MHz ±1 Hz when operating in the continuous mode. The system was switched to the burst mode and the counter was set for a 0.1-s measurement interval. A variable delay trigger allowed starting the count at various points in the message transmission interval. For Manchester or Miller data, the measurements indicated a count between 1,801,596 and 1,801,605 for all measurement intervals beginning between 0.3 and 0.5 second after message transmission began. Noise had little effect on the accuracy of the measurement for E_b/N_o as low as 9 dB. The results for NRZ data were not very encouraging, however. They were found to be pattern sensitive, with errors exceeding ±2 Hz in many instances; noise seemed to have a greater effect on accuracy.



(A) MANCHESTER/MSK DATA



(B) MILLER/MSK DATA

VERTICAL SCALE IS 10 DB/DIVISION;
HORIZONTAL SCALE IS 500 HZ/DIVISION.

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Figure 4-7. Spectra of MSK Signals Filtered by a 180-kHz IF Crystal Filter

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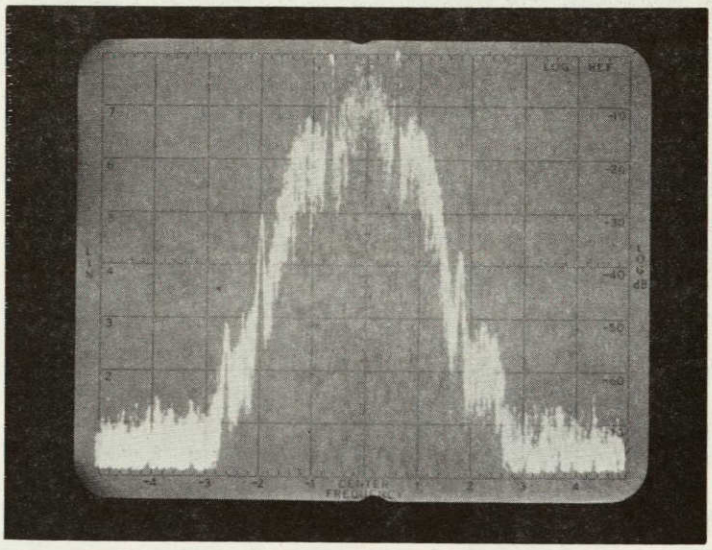
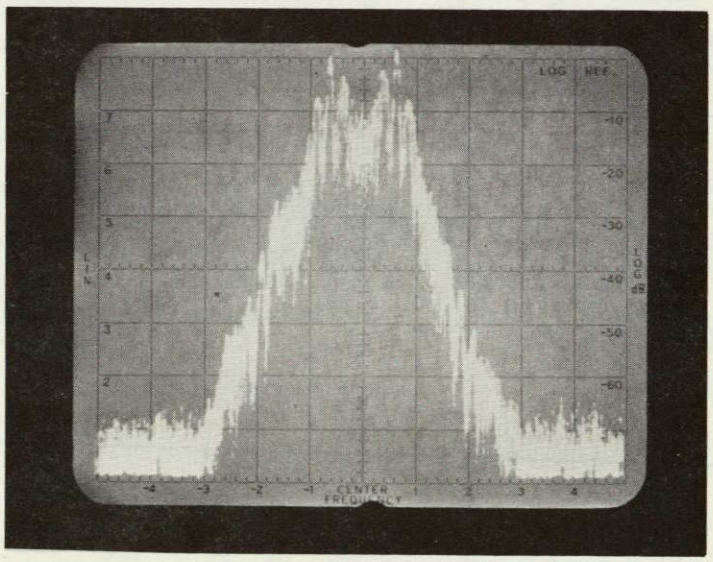


(A) MANCHESTER



(B) MILLER

VERTICAL SCALE IS 10 DB/DIVISION;
HORIZONTAL SCALE IS 500 HZ/DIVISION.

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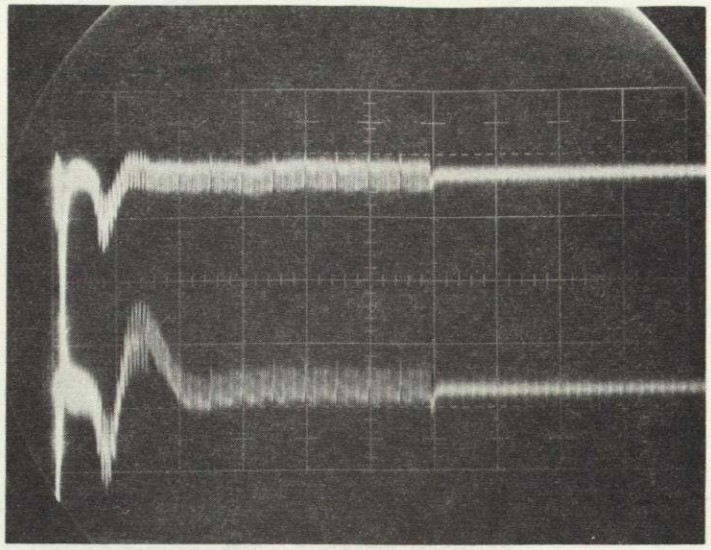
Figure 4-8. Spectra of Frequency-Doubled MSK Signals, i.e., Output From Squaring Circuit



UPPER TRACE IS OUTPUT OF MARK PHASE DETECTOR LPF.
LOWER TRACE IS OUTPUT OF SPACE PHASE DETECTOR LPF.
TIME SCALE IS 0.1 S/DIVISION. VERTICAL SCALE IS 0.5
217280 RADIAN/DIVISION.

Figure 4-9. Acquisition Transient for the Mark and Space Phase-Lock Loops

From these measurements, it can be concluded that a frequency-measurement accuracy of ±0.5 Hz can be obtained when either Manchester or Miller data is used; such accuracy cannot be maintained with NRZ data. The most accurate measurement is obtained during the message portion of the data, i.e., after allowing acquisition transients to be adequately damped. In a practical system having a 100-ms carrier (mark frequency) preamble followed by a 100-ms bit-sync code, frequency measurement can be started upon recognition of frame sync. Miller or Manchester data has little effect on accuracy when a well-designed phaselock loop using a VCXO is used to recover the mark frequency. When the VCXO operates at a frequency 100 times the frequency to be measured, a ±0.5-Hz accuracy is obtainable in a 100-ms measurement time. (Note: These conclusions are based on a 320 BPS data rate; some degradation may result for lower bit rates. This can probably be offset by a correspondingly reduced loop bandwidth in the tracking mode.)

4.6 DETERMINATION OF CROSSTALK/MUTUAL INTERFERENCE CHARACTERISTICS OF BREADBOARD MSK SYSTEM

The system was configured to operate in the burst mode. The data generator was set to produce Manchester data. The noncoherent MSK modulator output was summed with the main MSK modulator output. A frequency synthesizer was used to provide a variable-frequency LO to the noncoherent modulator so that the final output frequency from the noncoherent modulator could be changed. To prevent coherence in the data, the digital oscillator was supplied with Miller encoded data while the noncoherent modulator received Manchester data. The

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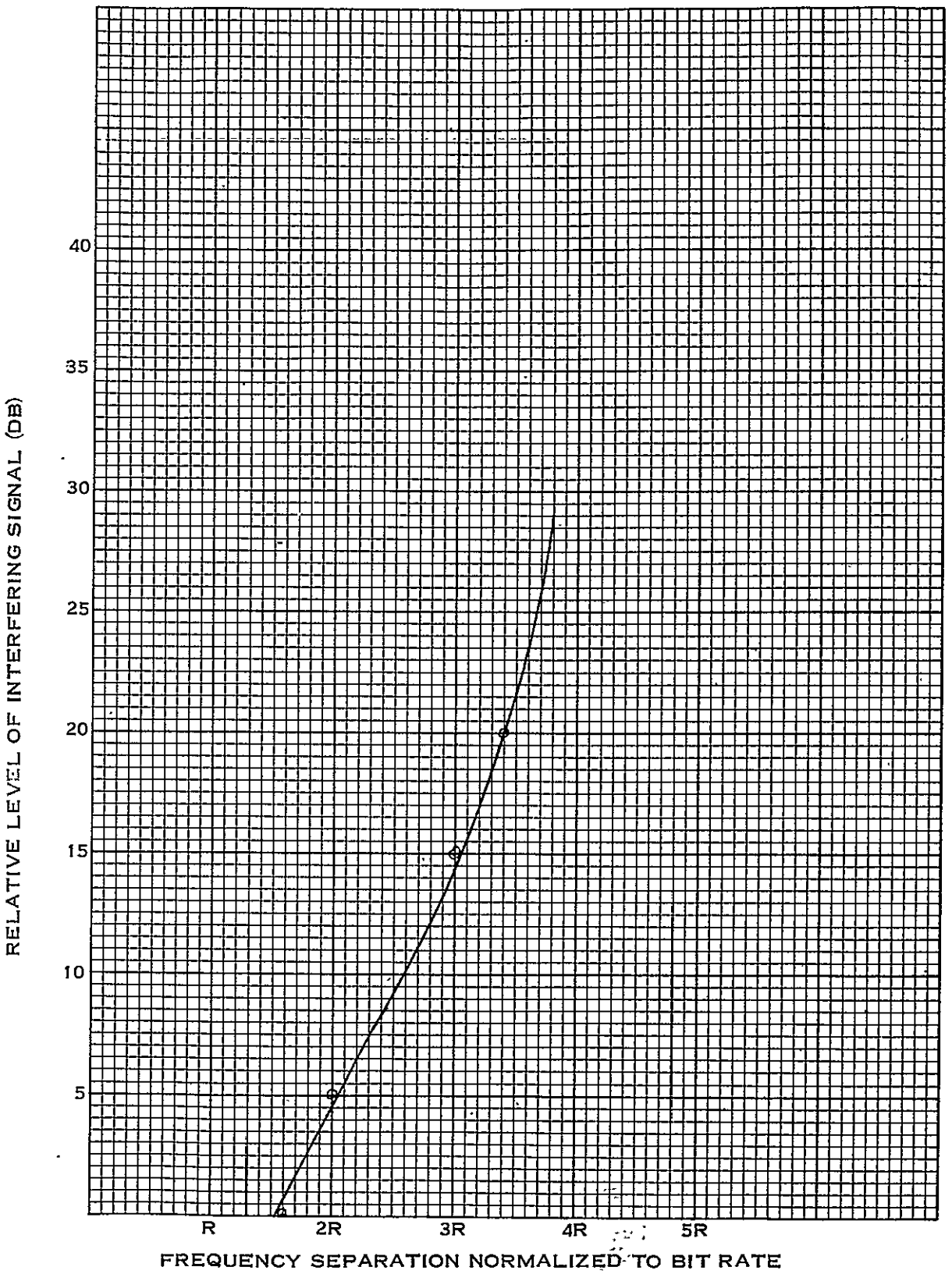

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Figure 4-10. Mutual Interference Characteristics of MSK

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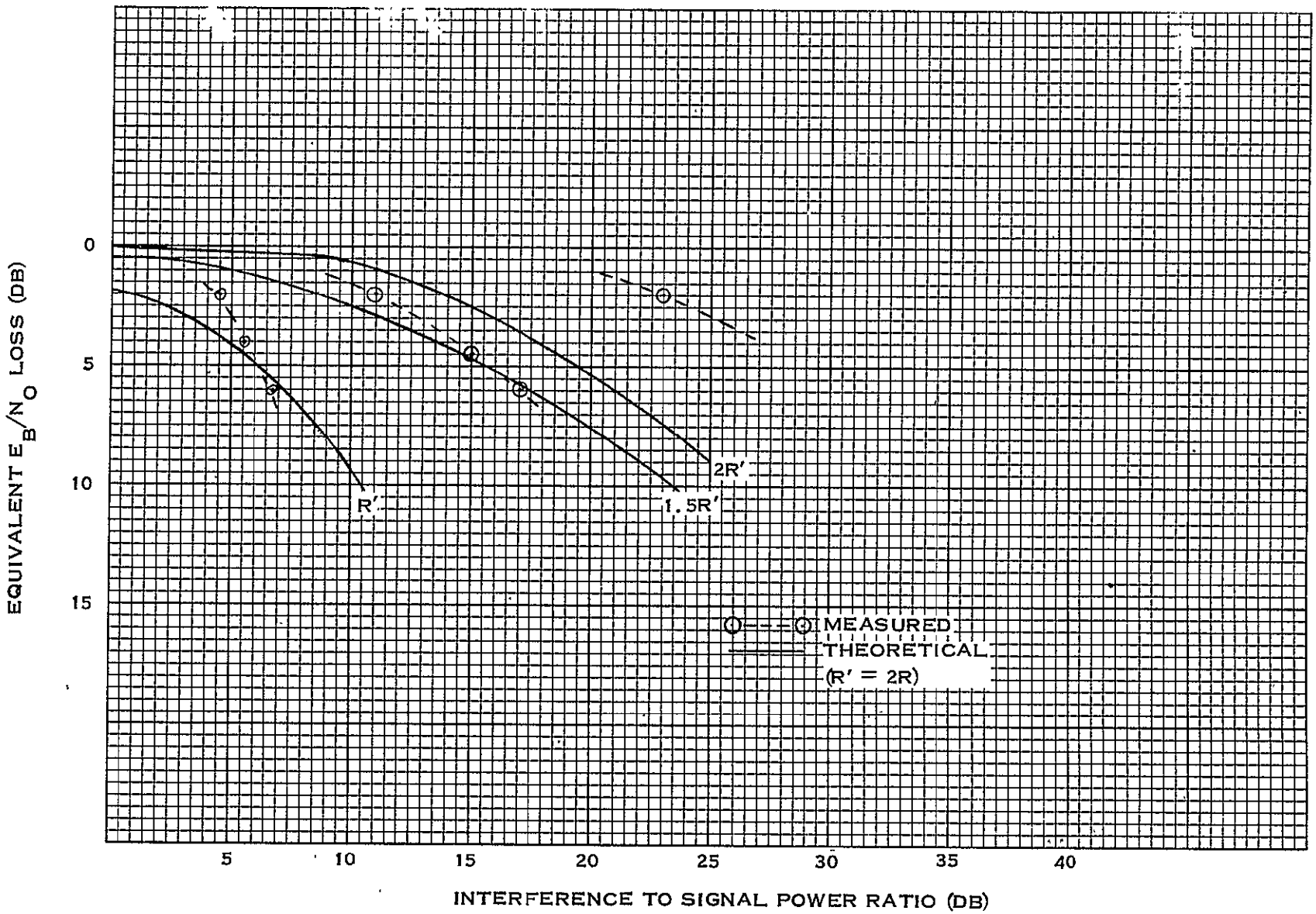

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Figure 4-11. S/N Ratio Loss as a Function of Adjacent Channel Separation and the Relative Power in the Adjacent Channel

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the level of the interference could not be increased enough to cause further degradation. These measured results tend to validate the superior crosstalk performance of MSK suggested by White.[21]

4.7 PHASE/MAGNITUDE CHARACTERISTICS OF CRYSTAL FILTER USED IN BREADBOARD TESTS

The parameters of the crystal filter used as the IF filter in the breadboard receiver were measured using an HP3575 network analyzer. The magnitude versus frequency characteristics are shown in Figure 4-12; the phase versus frequency characteristics are shown in Figure 4-13. The passband is reasonably flat over 500 Hz and the 3-dB bandwidth is approximately 900 Hz. The insertion loss is approximately 8 dB. The filter has 30-dB attenuation at frequencies ±1 kHz from center frequency, with attenuation greater than 50 dB for frequency separations greater than ±1.5 kHz. Thus, the filter is close to the design goal.

The phase characteristics of the filter are shown in Figure 4-13. They show that the filter has very nearly linear phase shift over the passband and these linear phase characteristics extend well into the rejection band, ensuring good performance of the MSK receiver even when Manchester/Miller data are used.

The filter has a bandwidth of 3R. The phase and magnitude characteristics are adequate for all tests conducted, but can be reduced somewhat in a final design of MSK equipment.

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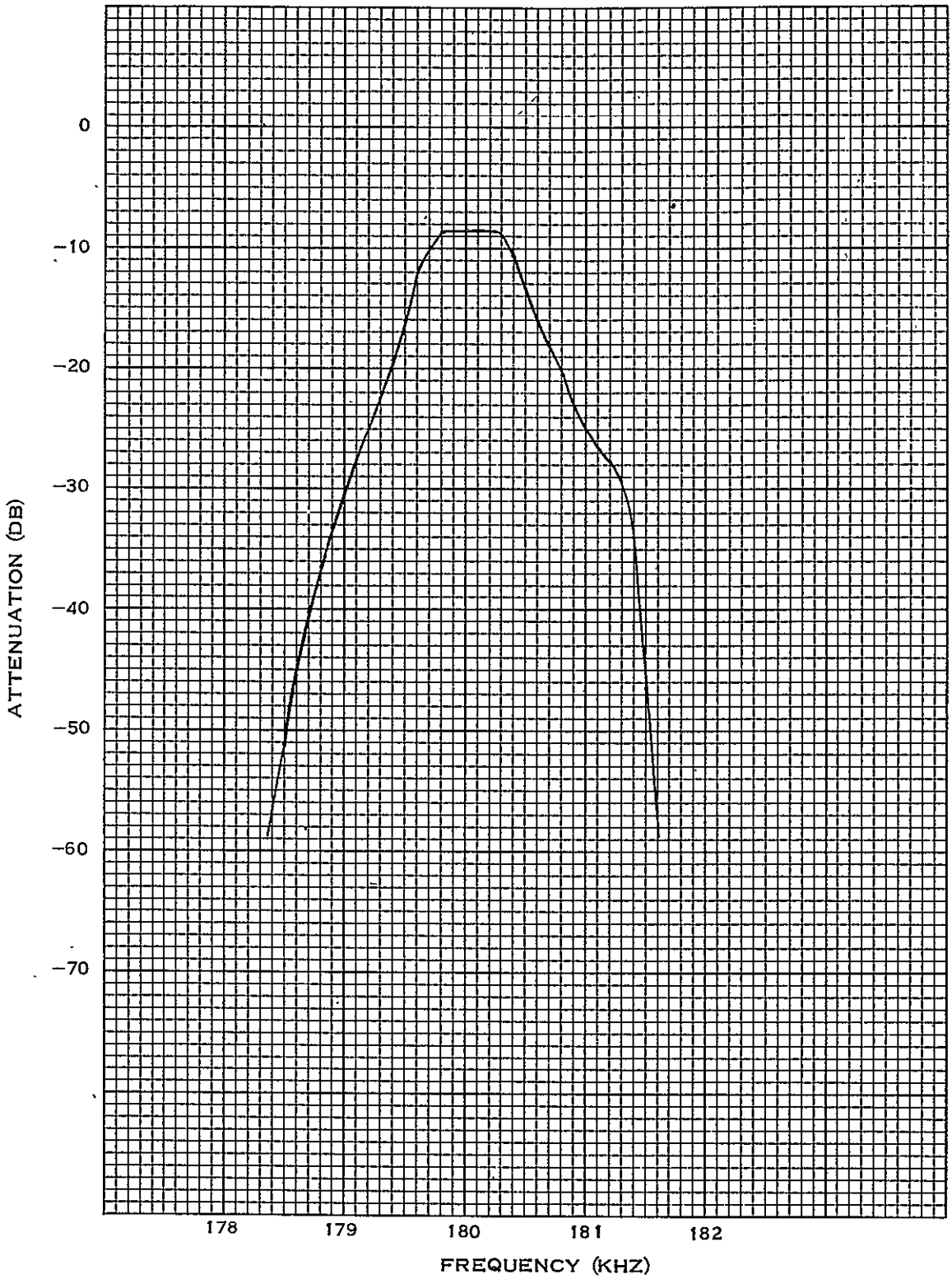

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Figure 4-12. IF Crystal Filter Magnitude Response

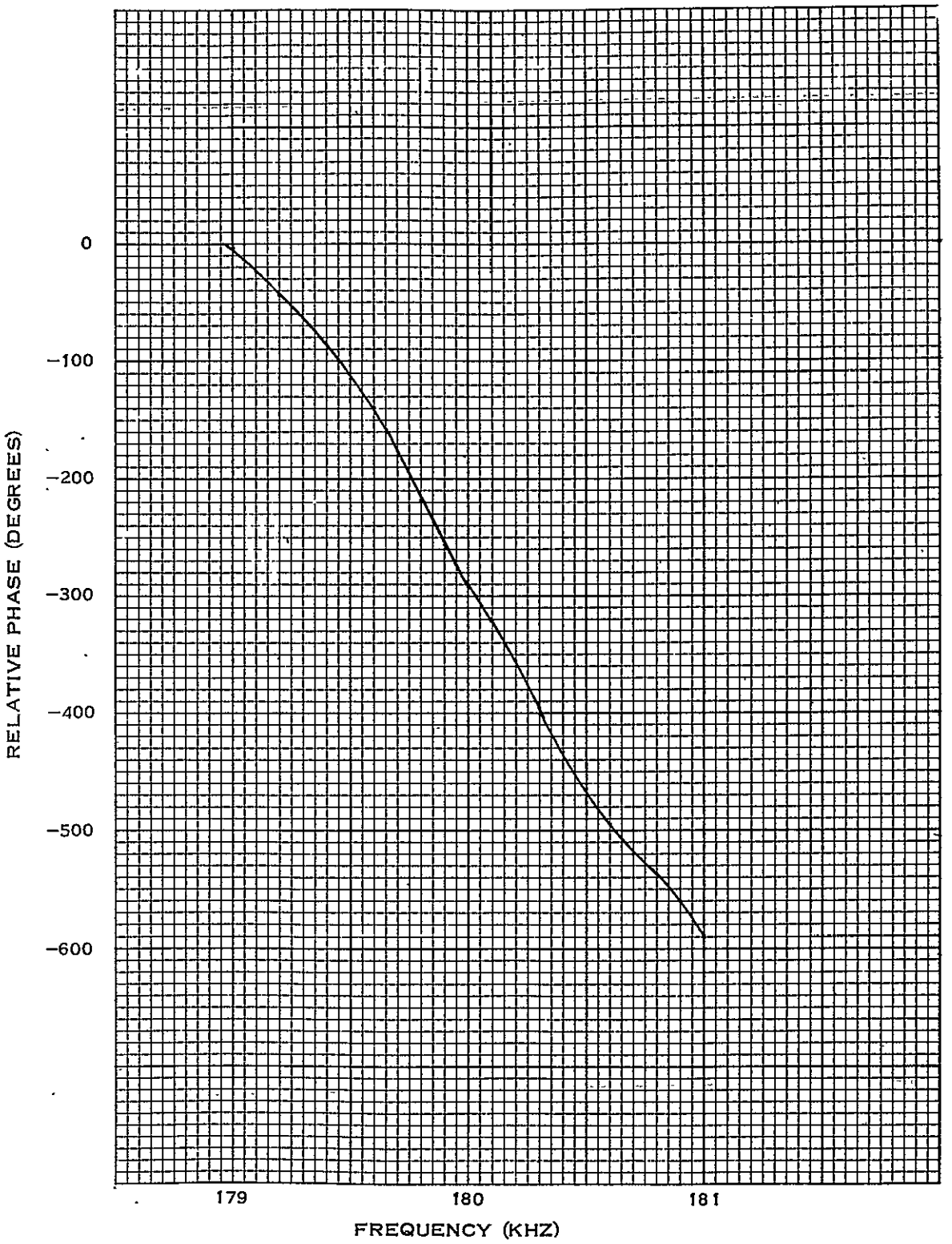

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Figure 4-13. IF Crystal Filter Phase Response

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APPENDIX A

DERIVATION OF THE RELATIONSHIP BETWEEN THE FSK METHOD OF GENERATING MSK AND THE PSK METHOD OF GENERATING MSK

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Minimum Shift Keying (MSK) is generated by selecting one of four signals at the beginning of each bit time. The four signal sources are:

$$
\begin{aligned}
S1(t) &= \cos(\omega_m t) = \cos\left(\omega_o + \frac{\pi}{2T}\right) t \\
S2(t) &= -\cos(\omega_m t) = -\cos\left(\omega_o + \frac{\pi}{2T}\right) t \\
S3(t) &= \cos(\omega_s t) = \cos\left(\omega_o - \frac{\pi}{2T}\right) t \\
S4(t) &= -\cos(\omega_s t) = -\cos\left(\omega_o - \frac{\pi}{2T}\right) t
\end{aligned}
\tag{A-1}
$$

Signals S1(t) and S2(t) are the mark frequency and the inverse of the mark frequency, respectively. Signals S3(t) and S4(t) are the space frequency and the inverse of the space frequency, respectively. Now, form the following definitions:

$$
\begin{aligned}
U_n &\equiv \text{the selection of the noninverted signal} \\
\overline{U}_n &\equiv \text{the selection of the inverted signal} \\
V_n &\equiv \text{the selection of the mark frequency} \\
\overline{V}_n &\equiv \text{the selection of the space frequency}
\end{aligned}
\tag{A-2}
$$

For MSK, it is permissible to use the data to select either the phase (U_n or $\overline{U}_n$) or the frequency (V_n or $\overline{V}_n$). To maintain compatibility with noncoherent (FSK) type demodulators, the data will be used to select frequency, i.e.:

$$V_n \equiv D_n \tag{A-3}$$

From Equation Set (A-1), the following logic equations can be established:

$$
\begin{aligned}
S1_n &= U_n \; V_n \\
S2_n &= \overline{U}_n \; V_n \\
S3_n &= U_n \; \overline{V}_n \\
S4_n &= \overline{U}_n \; \overline{V}_n
\end{aligned}
\tag{A-4}
$$

Either U_n or $\overline{U}_n$ is selected to maintain phase continuity.

Trigonometric expansion of right members of Equation Set (A-1) yields:

$$
\begin{aligned}
S1(t) &= \cos(\omega_o t)\cos\left(\frac{\pi t}{2T}\right) - \sin(\omega_o t)\sin\left(\frac{\pi t}{2T}\right) \\
S2(t) &= -\cos(\omega_o t)\cos\left(\frac{\pi t}{2T}\right) + \sin(\omega_o t)\sin\left(\frac{\pi t}{2T}\right) \\
S3(t) &= \cos(\omega_o t)\cos\left(\frac{\pi t}{2T}\right) + \sin(\omega_o t)\sin\left(\frac{\pi t}{2T}\right) \\
S4(t) &= -\cos(\omega_o t)\cos\left(\frac{\pi t}{2T}\right) - \sin(\omega_o t)\sin\left(\frac{\pi t}{2T}\right)
\end{aligned}
\tag{A-5}
$$

These equations define two orthogonal signals that can be modulated in antipodal PSK fashion, using phasor symbols derived from the data. Let the symbol that modulates the cosine function be designated I_n while the sine function modulating symbol is designated Q_n. Then,

$$
\begin{aligned}
S1_n &= I\,\overline{Q} \\
S2_n &= \overline{I}\,Q \\
S3_n &= I\,Q \\
S4_n &= \overline{I}\,\overline{Q}
\end{aligned}
\tag{A-6}
$$

is a set of logic equations that defines the MSK modulating process in terms of PSK phasor symbols. The first objective is to establish the relationship between the U, V symbols of Equation Set (A-4) and the I, Q symbols of Equation Set (A-6). The final objective is to establish a direct relationship between the data and the I, Q phasor symbols.

First, combining Equation Sets (A-4) and (A-6):

$$
\begin{aligned}
S1_n &= U_n\,V_n = I_n\,\overline{Q}_n \\
S2_n &= \overline{U}_n\,V_n = \overline{I}_n\,Q_n \\
S3_n &= U_n\,\overline{V}_n = I_n\,Q_n \\
S4_n &= \overline{U}_n\,\overline{V}_n = \overline{I}_n\,\overline{Q}_n
\end{aligned}
\tag{A-7}
$$

The U_n term can be eliminated from one pair by:

$$S1_n, \oplus S2_n = U_n\,V_n \oplus \overline{U}_n\,V_n = V_n\,(U_n \oplus \overline{U}_n) = V_n$$

Also,

$$
\begin{aligned}
S1_n \oplus S2_n &= I_n\overline{Q}_n \oplus \overline{I}_n Q_n \\
&= I_n\overline{Q}_n\,\overline{(\overline{I}_n Q_n)} + \overline{I}_n Q_n\,\overline{(I_n\overline{Q}_n)} \\
&= I_n\overline{Q}_n + \overline{I}_n Q_n \\
&= I_n \oplus Q_n
\end{aligned}
$$

Elimination of V_n from the $S1_n$ and $S3_n$ pair yields:

$$S1_n \oplus S3_n = U_n V_n \oplus U_n \overline{V}_n = U_n (V_n \oplus \overline{V}_n) = U_n$$

$$S1_n \oplus S3_n = I_n \overline{Q}_n \oplus I_n Q_n = I_n (\overline{Q}_n \oplus Q_n) = I_n$$

Hence,

$$\begin{aligned} V_n &= I_n \oplus Q_n \\ U_n &= I_n \end{aligned} \tag{A-8}$$

Manipulation of Equation (A-8) yields:

$$\begin{aligned} I_n &= U_n \\ Q_n &= U_n \oplus V_n \end{aligned} \tag{A-9}$$

Equation Sets (A-8) and (A-9) provide the desired link between the FSK (U, V) symbols and the PSK (I, Q) symbols.

The final step in the derivation is to show the relationship between the I, Q symbols and the data. This will be done by first obtaining the relationship between the data and the U, V symbols and then using Equation Set (A-9) to establish the desired relationship.

Equation (A-3) establishes the relationship between the data and the V symbol. Hence, it is necessary to establish a relationship for only the U symbol. From the basic definition of MSK, the following logic equations are readily obtained:

$$\begin{aligned} S1_n &= D_n S1_{n-1} + D_n S3_{n-1} N + D_n S4_{n-1} \overline{N} \\ S2_n &= D_n S2_{n-1} + D_n S3_{n-1} \overline{N} + D_n S4_{n-1} N \\ S3_n &= \overline{D}_n S3_{n-1} + \overline{D}_n S1_{n-1} N + D_n S2_{n-1} \overline{N} \\ S4_n &= \overline{D}_n S4_{n-1} + \overline{D}_n S1_{n-1} \overline{N} + \overline{D}_n S2_{n-1} N \end{aligned} \tag{A-10}$$

where N is a square-wave signal at one-half the bit clock frequency and represents alternating ones and zeros. As was previously shown:

$$U_n = S1_n \oplus S3_n \tag{A-11}$$

From Equation (A-10):

$$\begin{aligned} S1_n \oplus S3_n = {} & (D_n S1_{n-1} + D_n S3_{n-1} N + D_n S4_{n-1} \overline{N}) \\ & \oplus (\overline{D}_n S3_{n-1} + \overline{D}_n S1_{n-1} N + \overline{D}_n S2_{n-1} \overline{N}) \end{aligned} \tag{A-12}$$

Since $D_n = V_n$, then, from Equation (A-4):

$$\begin{aligned} S1_{n-1} &= U_{n-1} V_{n-1} = U_{n-1} D_{n-1} \\ S2_{n-1} &= \overline{U}_{n-1} V_{n-1} = \overline{U}_{n-1} D_{n-1} \\ S3_{n-1} &= U_{n-1} \overline{V}_{n-1} = U_{n-1} \overline{D}_{n-1} \\ S4_{n-1} &= \overline{U}_{n-1} \overline{V}_{n-1} = \overline{U}_{n-1} \overline{D}_{n-1} \end{aligned} \tag{A-13}$$

Substituting Equation Set (A-13) into Equation (A-12) yields:

$$U_n = (D_n D_{n-1} U_{n-1} + D_n \overline{D}_{n-1}\ U_{n-1} N + D_n \overline{D}_{n-1}\ U_{n-1}\ \overline{N})$$
$$\oplus\ (\overline{D}_n \overline{D}_{n-1}\ U_{n-1} + \overline{D}_n D_{n-1}\ U_{n-1}\ N + \overline{D}_n D_{n-1}\ \overline{U}_{n-1}\ \overline{N})$$
$$U_n = D_n\ [D_{n-1} U_{n-1} + \overline{D}_{n-1}\ (U_{n-1} N + \overline{U}_{n-1}\ \overline{N})] \oplus \overline{D}_n\ [\overline{D}_{n-1}\ U_{n-1} + D_{n-1}\ \overline{(U_{n-1} \oplus N)}]$$
$$= D_n\ [D_{n-1}\ U_{n-1} + \overline{D}_{n-1}\ \overline{(U_{n-1} \oplus N)}] \oplus \overline{D}_n\ [\overline{D}_{n-1}\ U_{n-1} + D_{n-1}\ \overline{(U_{n-1} \oplus N)}]$$

Let $X = U_{n-1} \oplus N$; then,

$$U_n = D_n\ [D_{n-1}\ U_{n-1} + D_{n-1}\ \overline{X}] \oplus D_n\ [\overline{D}_{n-1}\ U_{n-1} + D_{n-1}\ \overline{X}]$$
$$= [D_n D_{n-1}\ U_{n-1} + D_n \overline{D}_{n-1}\ \overline{X}] \oplus [\overline{D}_n \overline{D}_{n-1}\ U_{n-1} + \overline{D}_n D_{n-1}\ \overline{X}]$$
$$= [D_n D_{n-1}\ U_{n-1} + D_n \overline{D}_{n-1}\ \overline{X}]\ [\overline{D}_n \overline{D}_{n-1}\ U_{n-1} + \overline{D}_n D_{n-1}\ \overline{X}]$$
$$+ [D_n D_{n-1}\ U_{n-1} + D_n \overline{D}_{n-1}\ \overline{X}]\ [\overline{D}_n \overline{D}_{n-1}\ U_{n-1} + \overline{D}_n D_{n-1} \overline{X}]$$
$$= [D_n D_{n-1}\ U_{n-1} + D_n \overline{D}_{n-1}\ \overline{X} + D_n D_{n-1}\ U_{n-1} + D_n \overline{D}_{n-1}\ \overline{U}_{n-1}\ \overline{X}$$
$$+ D_n \overline{D}_{n-1}\ \overline{U}_{n-1}\ \overline{X} + D_n \overline{D}_{n-1}\ \overline{U}_{n-1}\ \overline{X} + D_n D_{n-1}\ U_{n-1}\ X]$$
$$+ [\overline{D}_n \overline{D}_{n-1}\ U_{n-1} + \overline{D}_n D_{n-1}\ \overline{X} + \overline{D}_n \overline{D}_{n-1}\ U_{n-1}\ X + \overline{D}_n \overline{D}_{n-1} U_{n-1}$$
$$+ \overline{D}_n \overline{D}_{n-1}\ U_{n-1}\ X + \overline{D}_n D_{n-1}\ \overline{U}_{n-1}\ \overline{X} + \overline{D}_n D_{n-1}\ \overline{U}_{n-1}\ \overline{X}]$$

Further reduction yields:

$$U_n = D_n D_{n-1} U_{n-1} + D_n \overline{D}_{n-1} \overline{X} + \overline{D}_n \overline{D}_{n-1} U_{n-1} + \overline{D}_n D_{n-1} \overline{X}$$
$$= U_{n-1} (D_n D_{n-1} + \overline{D}_n \overline{D}_{n-1}) + \overline{X} (D_n \overline{D}_{n-1} + \overline{D}_n D_{n-1})$$
$$= U_{n-1} \overline{(D_n \oplus D_{n-1})} + \overline{X} (D_n \oplus D_{n-1})$$

Let $W = D_n \oplus D_{n-1}$; then, $U_n = U_{n-1}\ W + XW$

But $X = U_{n-1} \oplus N$; hence, $U_{n-1} = X \oplus N$

Therefore,

$$U_n = (X \oplus N)\ \overline{W} + \overline{X}W$$
$$= X\overline{NW} + \overline{X}\ (N + W)$$

By letting $Z = \overline{NW}$ or $\overline{Z} = N + \overline{W}$, then

$$U_n = XZ + \overline{XZ}$$
$$= (X \oplus Z)$$

Substituting for X and Z yields:

$$U_n = \overline{(U_{n-1} \oplus N \oplus \overline{NW}}$$
$$= U_{n-1} \oplus \overline{N}W$$

A final result is obtained after substituting for W:

$$U_n = U_{n-1} \oplus \overline{N}\,(D_n \oplus D_{n-1}) \tag{A-14}$$

Equation (A-14) provides the desired relationship between the data and the U symbol. By using Equation Set (A-9), the proper relationship between the data and the I, Q symbols can be found.

Since $U_n = I_n$ and $V_n = D_n$, $Q_n = I_n \oplus D_n$ and, hence,

$$\begin{aligned} I_n &= I_{n-1} \oplus \overline{N}\,(D_n \oplus D_{n-1}) \\ Q_n &= I_n \oplus D_n \\ Q_{n-1} &= I_{n-1} \oplus D_{n-1} \\ I_{n-1} &= D_{n-1} \oplus Q_{n-1} \end{aligned}$$

Therefore,

$$\begin{aligned} I_n &= D_{n-1} \oplus Q_{n-1} \oplus \overline{N}\,(D_n \oplus D_{n-1}) \\ &= D_{n-1}\,(1 \oplus \overline{N}) \oplus \overline{Q}_{n-1} \oplus \overline{N}\,D_n \\ &= N\,D_{n-1} \oplus \overline{N}\,D_n \oplus \overline{Q}_{n-1} \\ &= N\,D_{n-1} \oplus \overline{N}\,D_n \oplus I_{n-1} \oplus D_{n-1} \\ &= I_{n-1} \oplus D_{n-1}\,(1 \oplus N) \oplus \overline{N}\,D_n \\ &= I_{n-1} \oplus \overline{N}\,D_{n-1} \oplus \overline{N}\,D_n \\ &= I_{n-1} \oplus \overline{N}\,(D_n \oplus D_{n-1}) \end{aligned}$$

Similarly,

$$\begin{aligned} Q_n &= I_n \oplus D_n \\ &= I_{n-1} \oplus \overline{N}\,(D_n \oplus D_{n-1}) \oplus D_n \\ &= I_{n-1} \oplus \overline{N}\,D_{n-1} \oplus D_n\,(1 \oplus \overline{N}) \\ &= D_{n-1} \oplus Q_{n-1} \oplus \overline{N}\,D_{n-1} \oplus N\,D_n \\ &= Q_{n-1} \oplus D_{n-1}\,(1 \oplus \overline{N}) \oplus N\,D_n \\ &= Q_{n-1} \oplus N\,D_{n-1} \oplus N\,D_n \\ &= Q_{n-1} \oplus N\,(D_n \oplus D_{n-1}) \end{aligned}$$

Therefore, the desired equations are:

$$\begin{aligned} I_n &= I_{n-1} \oplus \overline{N}\,(D_n \oplus D_{n-1}) \\ Q_n &= Q_{n-1} \oplus N\,(D_n \oplus D_{n-1}) \end{aligned} \tag{A-15}$$

Equation Set (A-15) provides the basis for generating the I, Q phasor symbols from an NRZ-L bit stream. The I, Q symbols can be used in a PSK modulator approach, but the intent here is to show their relationship to the U, V symbols of an FSK approach. A coherent demodulator extracts the I, Q symbols. Equation Set (A-9) provides the proper decoding relationship. Since $Q_n = I_n \oplus V_n$ and $V_n = D_n$, the data can be unambiguously recovered from:

$$D_n \; I_n \oplus Q_n \tag{A-16}$$

The interpetation of Equation Set (A-15) is as follows. The data is differentially encoded with the previous data bit, $D_n \oplus D_{n-1}$. The clock phase, N or $\overline{N}$ is completely arbitrary. For the phase given in Equation Set (A-15), when N = 0, a new I_n symbol is generated by differentially encoding the previous I symbol, I_{n-1}, with the differentially encoded data: $I_n = I_{n-1} \oplus (D_n \oplus D_{n-1})$. The Q_n symbol is unchanged since $Q_n = Q_{n-1} \oplus 0 = Q_{n-1}$. At the next clock time, the I symbol is unchanged while the Q symbol is changed. Thus, the I and Q symbols are staggered in phase by one bit period and each exists for two bit periods. Note that this relationship exists in the coherent demodulator regardless of the method used to generate the MSK signal.

APPENDIX B

MSK COHERENT DEMODULATOR DETAILED SCHEMATICS

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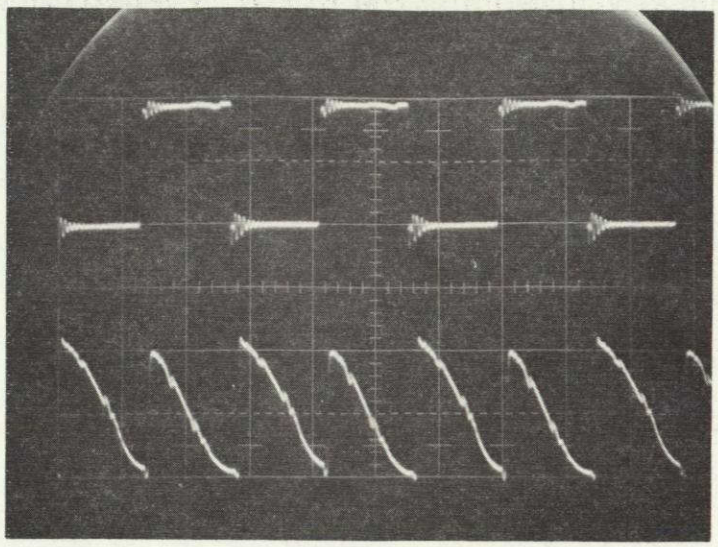
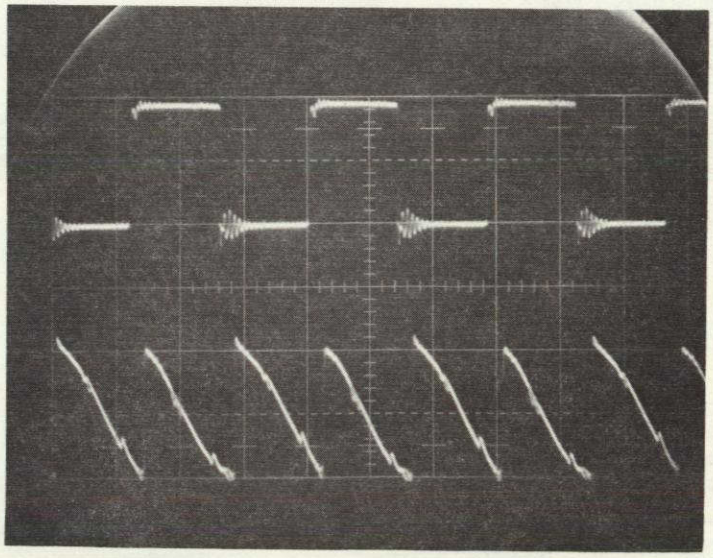
MSK COHERENT DEMODULATOR DETAILED SCHEMATICS

This appendix contains schematics of the MSK Coherent Demodulator, the Miller decoder, and the modified IF receiver, including the AGC and crystal filter. A board layout for each piece of equipment built as part of this study is also included. Photographs of mark/space phaselock loop waveforms are shown in Figure B-1. Photographs of the I- and Q-channel demodulator waveforms are shown in Figure B-2.



(A) MARK PHASELOCK LOOP



(B) SPACE PHASELOCK LOOP

UPPER TRACE: OUTPUT FROM VCXO

LOWER TRACE: PHASE DETECTOR OUTPUT

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Figure B-1. Mark/Space PLL Phase Detector Waveforms

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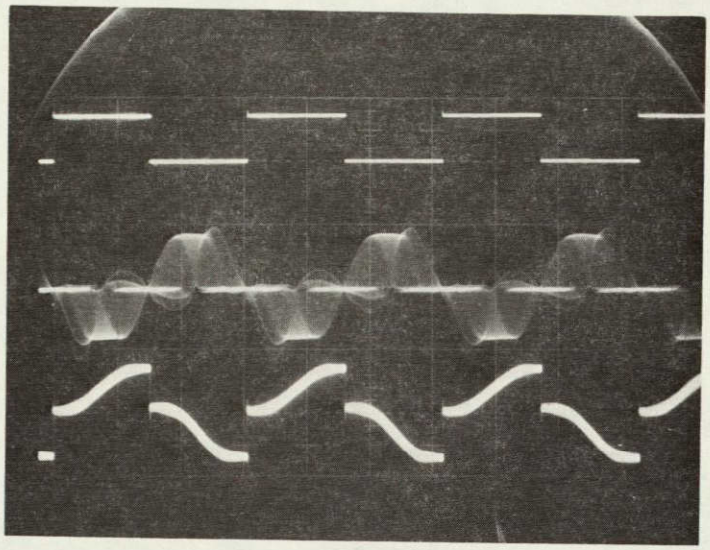
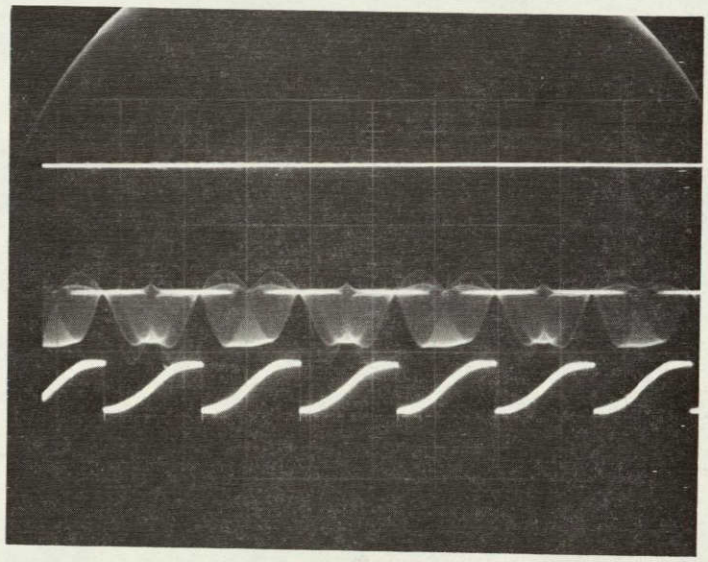


(A) I-CHANNEL WAVEFORMS



(B) Q-CHANNEL WAVEFORMS

UPPER TRACE: DETECTED DATA, 5V/DIV
CENTER TRACE: DEMODULATOR OUTPUT, 5V/DIV
LOWER TRACE: MATCHED FILTER OUTPUT, 2V/DIV
HORIZONTAL SCALE: 2 MS/DIV

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Figure B-2. Demodulator Waveforms for All-Ones Bi-Phase Data I Input

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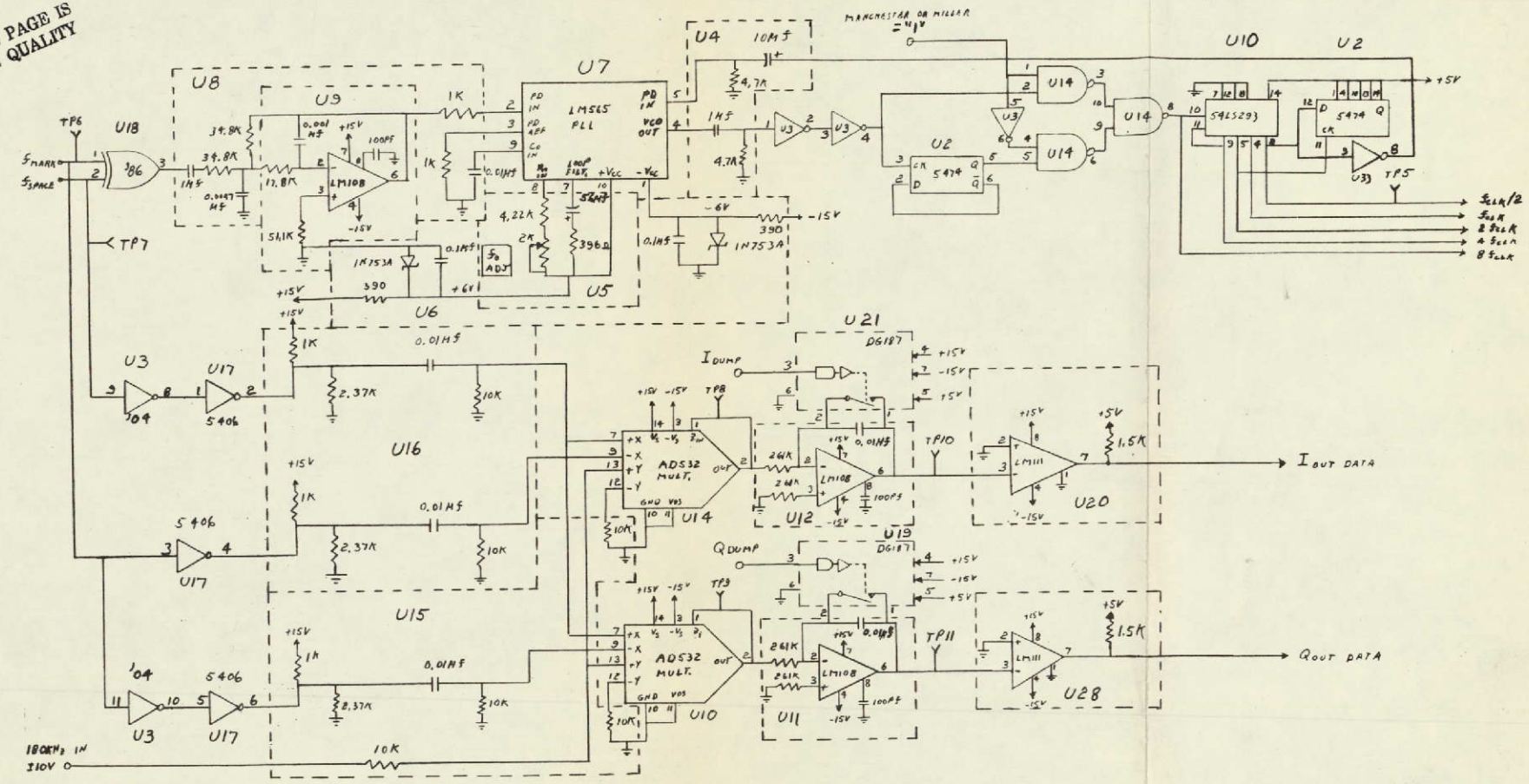

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Figure B-3. MSK Coherent Demodulator: Demodulator, Data Detector, and Bit Sync PLL

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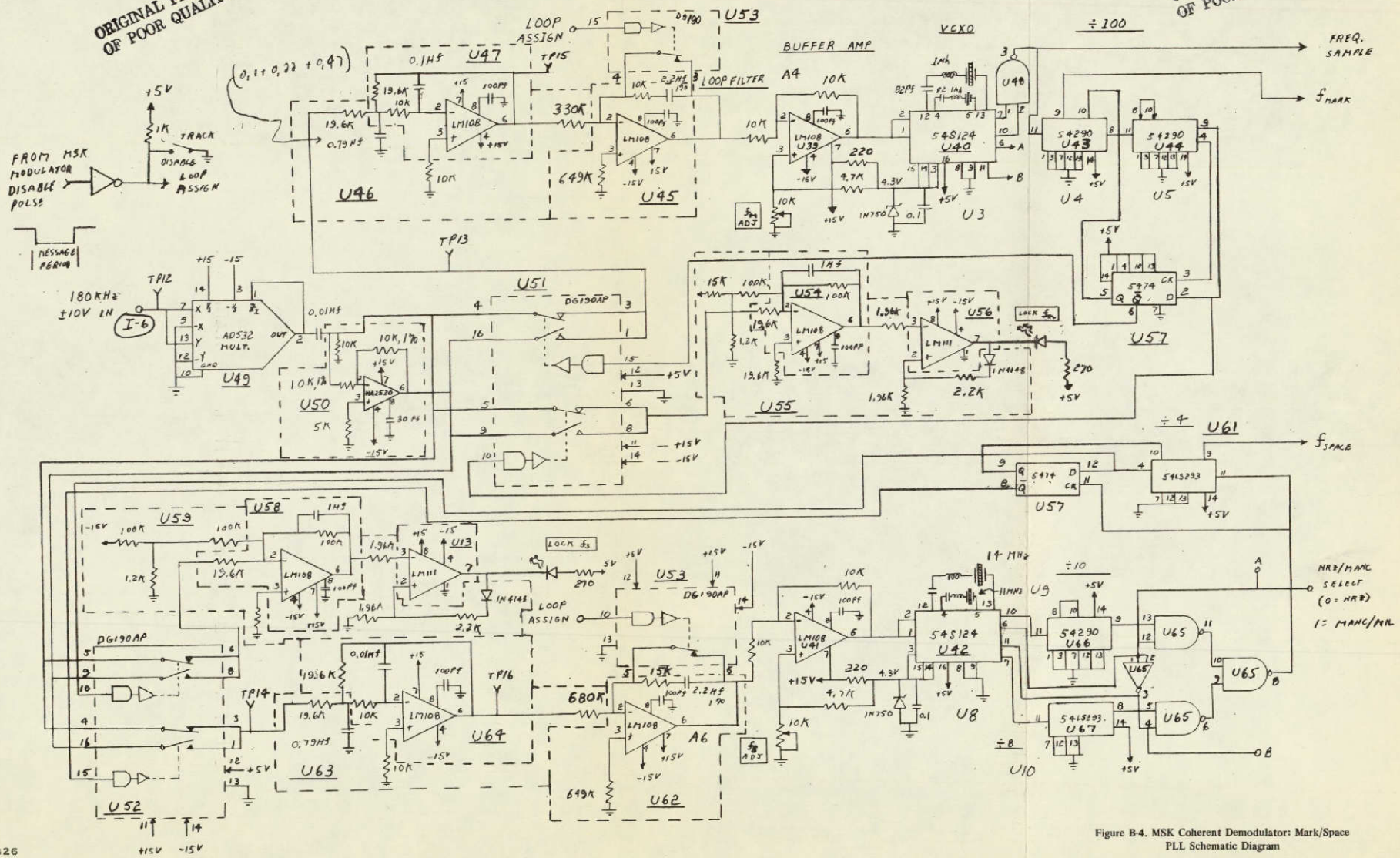

Figure B-4. MSK Coherent Demodulator: Mark/Space PLL Schematic Diagram

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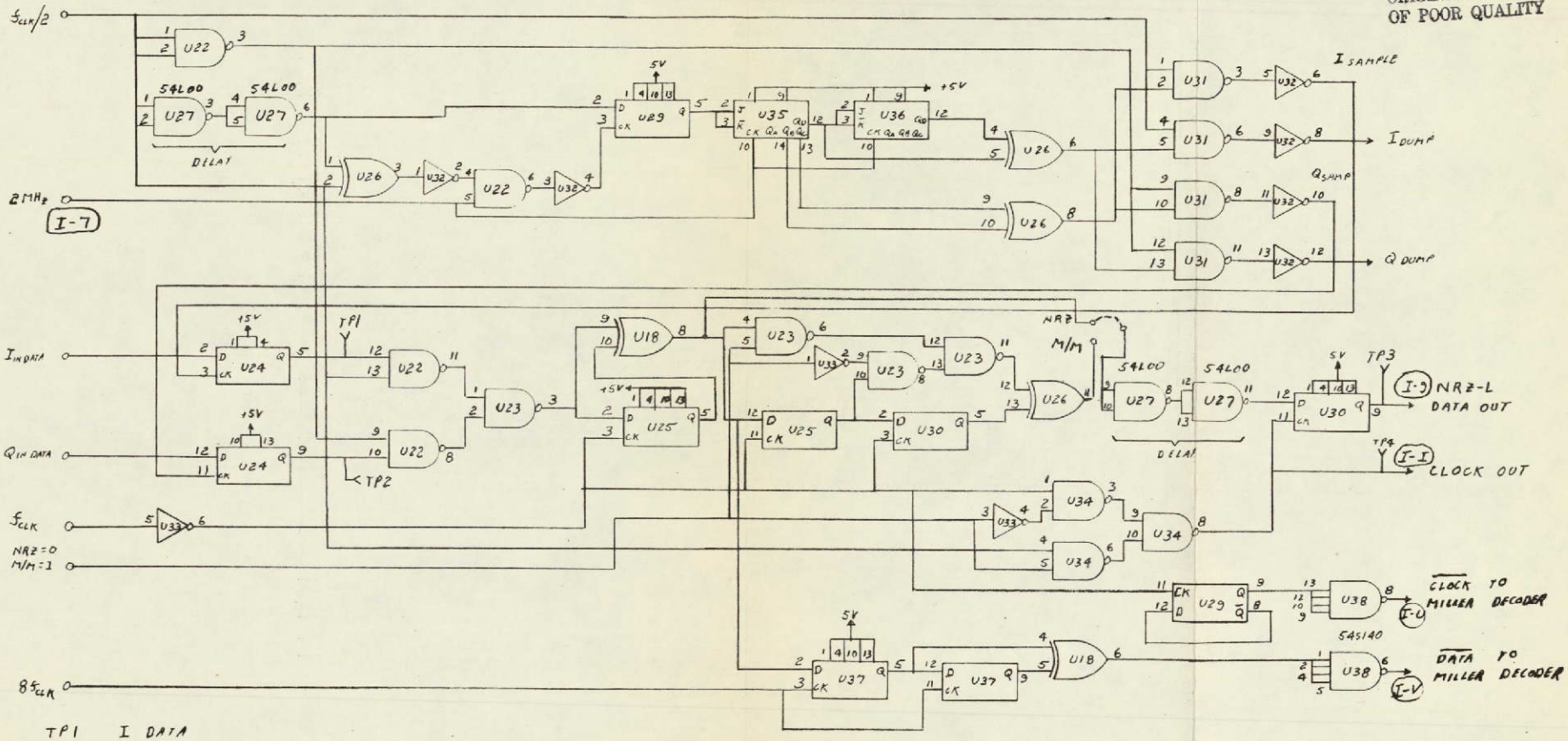

TP1	I DATA
TP2	Q DATA
TP3	NRZ-L DATA OUT
TP4	NRZ-L CLOCK OUT
TP5	$f_{CLK}/2$
TP6	f_{mark}
TP7	f_{space}
TP8	I MULTIPLIER OUT
TP9	Q MULTIPLIER OUT
TP10	I INTEGRATOR OUT
TP11	Q INTEGRATOR OUT
TP12	180 kHz IN
TP13	MARK PHASE DET OUTPUT
TP14	SPACE PHASE DET OUTPUT
TP15	MARK FILTER OUT
TP16	SPACE FILTER OUT

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Figure B-5. MSK Coherent Demodulator: Timing Generator/Data Decoder

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MSK COHERENT DEMODULATOR BREADBOARD LAYOUT

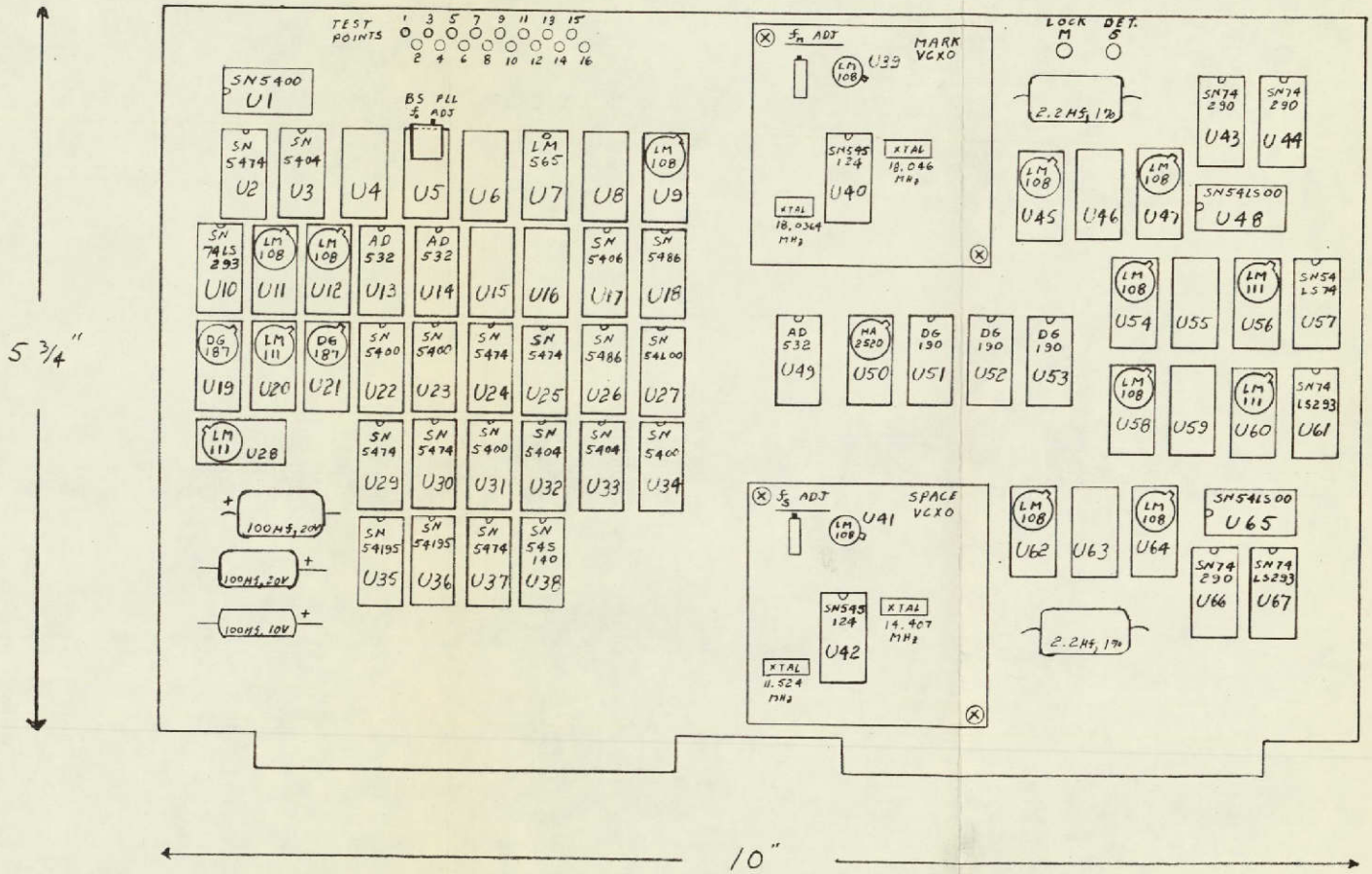

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Figure B-6. MSK Coherent Demodulator: Breadboard Layout

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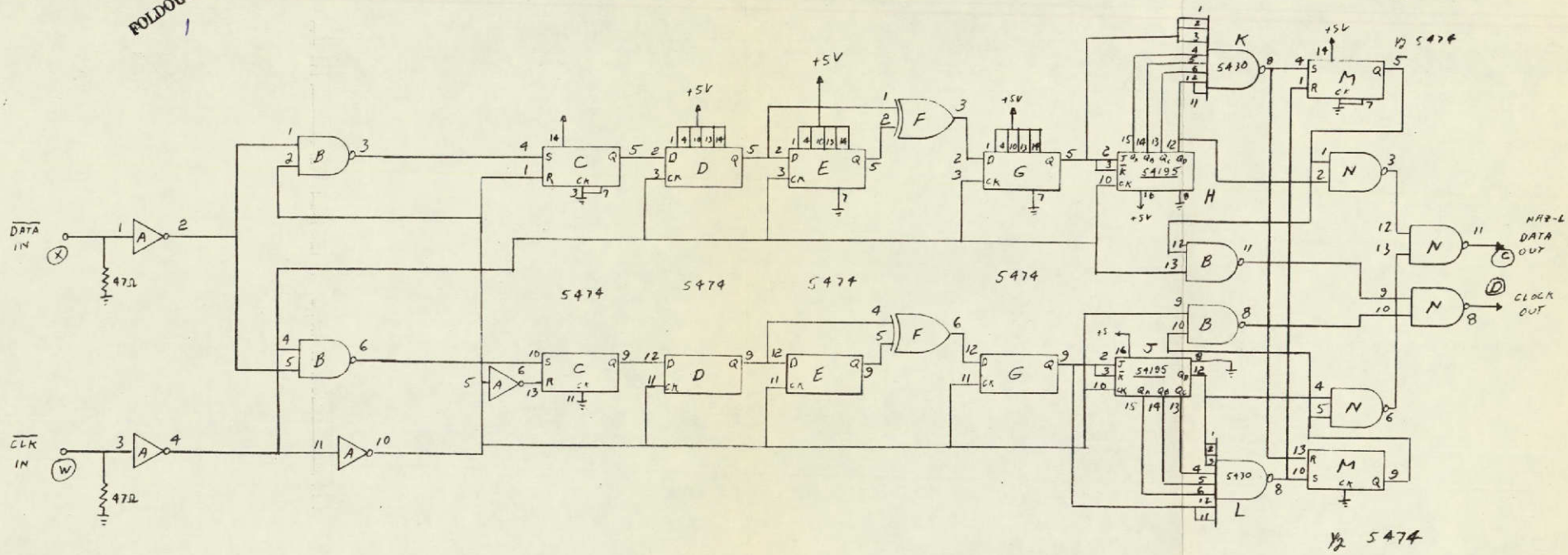
FOLDOUT FRAME 2



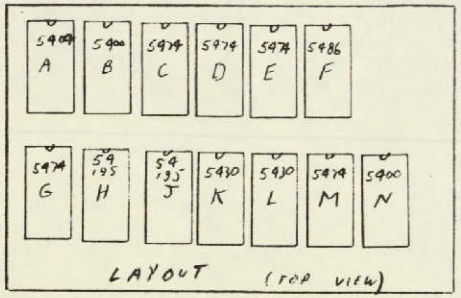


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Figure B-7. Miller Data Decoder Schematic Diagram

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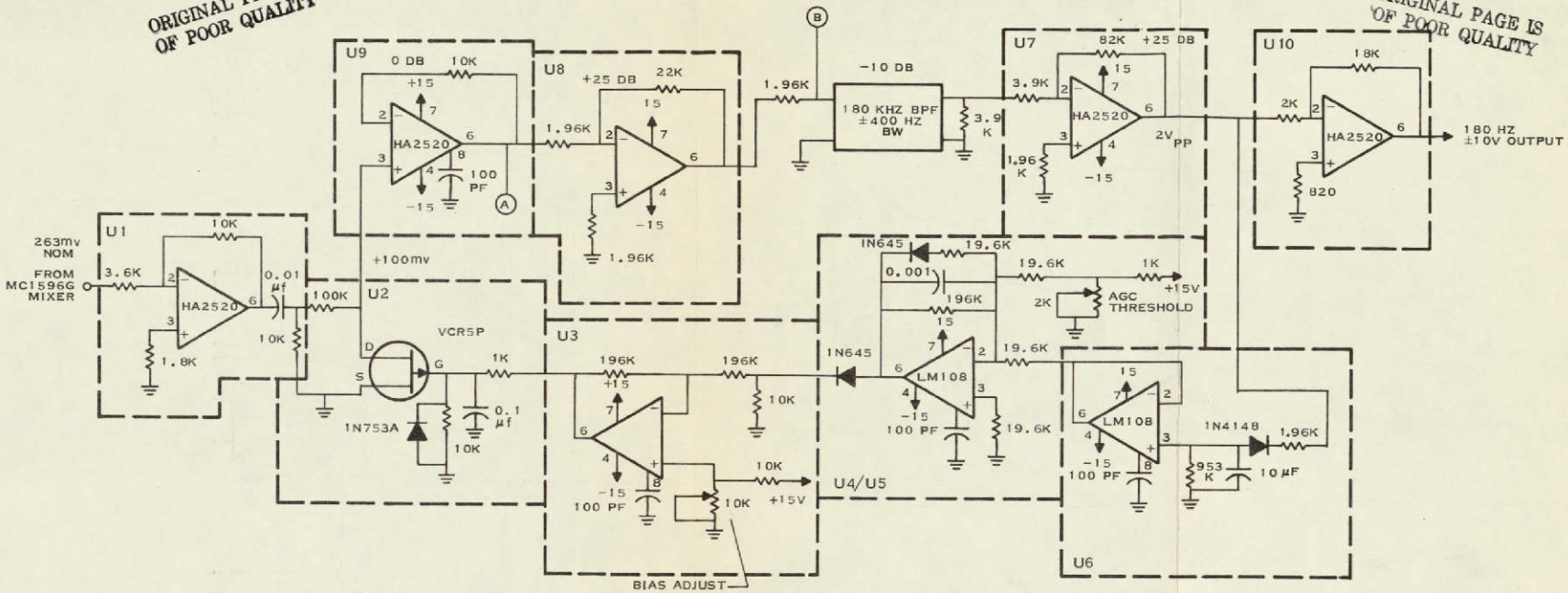
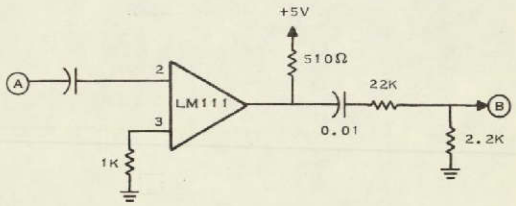
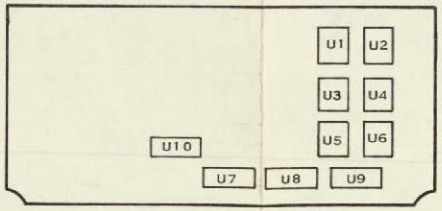




LIMITER TO BE SUBSTITUTED BETWEEN POINTS A AND B. (U8)



AGC CIRCUIT LAYOUT ON RECEIVER BOARD

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Figure B-8. MSK Receiver Filter/Amplifier With AGC Circuit

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