UTILITY PATENT APPLICATION TRANSMITTAL
TRACK 1 PRIORITIZED EXAMINATION
(Only for new nonprovisional applications under 37 CFR 1.53(b))

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/Si Vuong/
Si Vuong

Docket No. : 224123
Inventor(s) : Sang-Shin Lee
Title : PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

ADDRESS TO: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

June 24, 2022

1. __X__ **FEE TRANSMITTAL FORM**

2. **IF A CONTINUING APPLICATION**
__X__ This application is a continuation of patent application No. 17/005,753.

Prior application information: Examiner Kwang-Su Yang; Group Art Unit: 2691.

_____ This application claims the benefit of Provisional Application No. _____ pursuant to 35 U.S.C. §119(e) and 37 CFR §1.78(a)(4).

3. **APPLICATION COMPRISED OF**

Specification
__29__ Specification, claims and Abstract (total pages)

Drawings
__6__ Sheets of formal drawing(s) (FIGS. 1 to 6)

Inventor's Declaration(s)
__X__ Executed Declaration (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional)
_____ Executed Declaration/Assignment (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional)

Power of Attorney by Applicant(s)
__X__ Executed (new or copy from a prior application (37 CFR 1.63(d)) (for continuation and divisional) with transmittal

Application Data Sheet
__X__ Newly executed ADS
_____ Unexecuted ADS

4. _____ **Microfiche Computer Program** *(Appendix)*

UTILITY PATENT APPLICATION TRANSMITTAL
TRACK 1 PRIORITIZED EXAMINATION
(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.: 224123

5. _____ **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, all necessary)*
   _____ Computer Readable Copy
   _____ Paper Copy (identical to computer copy)
   _____ Statement verifying identity of above copies

6. **APPLICANT(S) STATUS UNDER 37 CFR § 1.27 or 1.29**
   _____ Applicant(s) and any others associated with it/them under § 1.27(a) are a SMALL ENTITY
   _____ Applicant(s) and any others associated with it/them under § 1.29(a) are a MICRO ENTITY
   _____ Certification of Micro Entity Status (Gross Income Basis)

7. **ALSO ENCLOSED ARE**
   __X__ Certification and Request for Prioritized Examination under 37 CFR 1.102(e)
   _____ Request and Certificate under 35 U.S.C. §122(b)(2)(B)(i) **(Request for Non-Publication)**
   _____ Preliminary Amendment
   _____ Includes "Cross-Reference to Related Applications"
   _____ A Petition for Extension of Time for the parent application and the required fee are being filed concurrently herewith.
   _____ This application is owned by _____ pursuant to an Assignment recorded at Reel _____, Frame _____
   _____ Information Disclosure Statement (IDS)
   _____ Copies of IDS Citations
   _____ Certified copy of Priority Document(s) (*paper filing only, if foreign priority is claimed)*
   _____ English Translation Document *(if applicable)*
   _____ Return Receipt Postcard (MPEP 503) (should be specifically itemized).
   _____ Other: _____

8. **DIRECT ALL CORRESPONDENCE TO: CUSTOMER NUMBER 23363**

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

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FEE TRANSMITTAL
UTILITY PATENT APPLICATION
TRACK 1 PRIORITIZED EXAMINATION

DATE: June 24, 2022

Docket No. : 224123 Duplicate __
Inventor(s) : Sang-Shin Lee
Title : PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

FEE CALCULATION

CLAIMS AS FILED						
	Number Filed	Number Extra	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Total Claims	25 – 20	= 5	5 x $100.00	$50.00	$25.00	$500.00
Independent Claims	2 – 3	= 0	0 x $480.00	$240.00	$120.00	$0.00
Multiple-Dependent Claims Fee			$860.00	$430.00	$215.00	$0.00

BASIC FILING, SEARCH, AND EXAMINATION FEES				
	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Basic Filing Fee	$320.00	$80.00	$80.00	$320.00
Search Fee	$700.00	$350.00	$175.00	$700.00
Examination Fee	$800.00	$400.00	$200.00	$800.00

APPLICATION SIZE FEE							
EFS Paper Size Equivalent	Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof (round up to whole number)	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
35 *.75	= 27 – 100	= 0/50	= 0	0 x $420.00	$210.00	$105.00	$0.00

TRACK 1 PRIORITIZED EXAMINATION				
	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Prioritized-Examination Fee	$4,200.00	$2,100.00	$1,050.00	$4,200.00
Processing Fee	$140.00	$70.00	$35.00	$140.00

OTHER				
	Large Entity Rate	Small Entity Rate	Micro Entity Rate	Fee
Late Submission of Oath/Declaration Fee	$160.00	$80.00	$40.00	$0.00
Non-Electronic Filing Fee	$400.00	$200.00	$200.00	$0.00
			TOTAL AMOUNT OF FEES	$6,660.00
List Independent Claims: 1 and 10				

METHOD OF PAYMENT

__X__ Submitted herewith is the fee of $6,660.00.

__X__ The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required during the **entire pendency** of the application to Deposit Account No. 03-1728. Please show our docket number with any charge or credit to our Deposit Account.

Respectfully submitted,

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SJF/smv

ABSTRACT

A pixel arrangement structure of an organic light emitting diode (OLED) display is provided. The pixel arrangement structure includes: a first pixel having a center coinciding with a center of a virtual square; a second pixel separated from the first pixel and having a center at a first vertex of the virtual square; and a third pixel separated from the first pixel and the second pixel, and having a center at a second vertex neighboring the first vertex of the virtual square. The first pixel, the second pixel, and the third pixel have polygonal shapes.

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 17/005,753, filed August 28, 2020, which is a continuation of U.S. Patent Application No. 13/872,018, filed April 26, 2013, now U.S. Patent No. 10,832,616, which claims priority to and the benefit of Korean Patent Application No. 10-2013-0044993, filed in the Korean Intellectual Property Office on April 23, 2013, and is a continuation in part of U.S. Patent Application No. 13/614,197, filed September 13, 2012, now U.S. Patent No. 9,818,803, which claims priority to and the benefit of Korean Patent Application No. 10-2012-0022967, filed in the Korean Intellectual Property Office on March 6, 2012. The entire contents of all of the above applications are incorporated herein by reference.

BACKGROUND

1. Field

[0002] Aspects of embodiments of the present invention relate generally to a pixel arrangement structure for an organic light emitting diode (OLED) display.

2. Description of the Related Art

[0003] A display device is a device that displays an image. Recently, an OLED display has been drawing attention.

[0004] The OLED display has a self-luminous characteristic. Because the OLED display does not need a separate light source, unlike a liquid crystal display, it can have a relatively smaller thickness and weight than liquid crystal displays. In addition,

the OLED display exhibits high-quality characteristics such as low power consumption, high luminance, high response speed, etc.

[0005] In general, the OLED display includes a plurality of pixels for emitting light of different colors. The plurality of pixels emit light to display an image.

[0006] Here, the pixel refers to a minimum unit for displaying the images. For instance, there may be a gate line, a data line, and a power line such as a driving power line to drive each pixel. In addition, there may be an insulation layer such as a pixel definition layer to define an area and a shape of each pixel. Further, each pixel may be positioned between its neighboring pixels.

[0007] An organic emission layer included in the pixel of an OLED display may be deposited and formed by using a mask such as a fine metal mask (FMM). When reducing a gap between the neighboring pixels to obtain a high aperture ratio of the pixels, deposition reliability may be deteriorated. On the other hand, when increasing the gap between the pixels to improve the deposition reliability, the aperture ratio of the pixels may be deteriorated.

[0008] The above information disclosed in this Background section is only for enhancement of understanding of the background of the invention and therefore it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY

[0009] Aspects of embodiments of the present invention relate generally to a pixel arrangement structure for an OLED display. More particularly, aspects of embodiments of the present invention relate to a pixel arrangement structure of an OLED display that displays an image by emitting light through a plurality of pixels.

[0010] An exemplary embodiment of the present invention provides a pixel arrangement structure for an OLED display having an improved aperture ratio of each of the pixels while efficiently setting up gaps between the pixels.

[0011] According to an exemplary embodiment of the present invention, a pixel arrangement structure of an organic light emitting diode display is provided. The pixel arrangement structure includes: a first pixel having a center coinciding with a center of a virtual square; a second pixel separated from the first pixel and having a center at a first vertex of the virtual square; and a third pixel separated from the first pixel and the second pixel, and having a center at a second vertex neighboring the first vertex of the virtual square.

[0012] The second pixel may include a pair of second pixels. The second pixels may be separated from each other by the first pixel.

[0013] The third pixel may include a pair of third pixels. The third pixels may be separated from each other by the first pixel.

[0014] The second pixels and the third pixels may enclose the first pixel in the virtual square.

[0015] The first pixel, the second pixels, and the third pixels may have polygonal shapes. The second pixels and the third pixels may have a larger area than the first pixel.

[0016] The first pixel may have a quadrilateral shape. The second pixels and the third pixels may have hexagonal or octagonal shapes.

[0017] The second pixels and the third pixels may have octagonal shapes.

[0018] The second pixels and the third pixels may have a same area. A distance between the first pixel and the second pixels, a distance between the first pixel and the third pixels, and a distance between the second pixels and the third pixels may be a same first length.

[0019] The first pixel may include a plurality of first pixels. The plurality of first pixels may have a same quadrilateral shape. A distance between neighboring ones of the plurality of first pixels may be a second length that is longer than the first length.

[0020] The second pixels may have a larger area than the third pixels. A distance between the second pixels and the third pixels may be a first length. A distance between the first pixel and the second pixels, and a distance between the first pixel and the third pixels may be a same second length.

[0021] The first pixel may include a plurality of first pixels. The plurality of first pixels may have a same quadrilateral shape. A distance between neighboring ones of the plurality of first pixels may be a third length that is longer than the first length and the second length.

[0022] The first pixel may include a plurality of first pixels. Neighboring ones of the plurality of first pixels may have quadrilateral shapes that are symmetrical to each other. A distance between the neighboring ones of the plurality of first pixels may be a third length that is longer than the first length and the second length.

[0023] The first pixel may include a plurality of first pixels. Neighboring ones of the plurality of first pixels may have quadrilateral shapes that are symmetrical to each other.

[0024] The second pixels may have a larger area than the third pixels.

[0025] The third pixels may have a larger area than the second pixels.

[0026] The first pixel, the second pixel, and the third pixel may be configured to emit different color lights.

[0027] The first pixel, the second pixel, and the third pixel may be configured to emit green light, blue light, and red light, respectively.

[0028] According to an exemplary embodiment of the present invention, a pixel arrangement structure of an organic light emitting diode (OLED) display is provided. The pixel arrangement structure includes: a first pixel having a center coinciding with a

center of a virtual square; a second pixel separated from the first pixel and having a center at a first vertex of the virtual square; and a third pixel separated from the first pixel and the second pixel, and having a center at a second vertex neighboring the first vertex of the virtual square. The first pixel, the second pixel, and the third pixel have polygonal shapes.

[0029] In one embodiment, the second pixel includes a pair of second pixels, and the second pixels are separated from each other by the first pixel.

[0030] In one embodiment, the third pixel includes a pair of third pixels, and the third pixels are separated from each other by the first pixel.

[0031] In one embodiment, the second pixel includes a pair of second pixels, the third pixel includes a pair of third pixels, and the second pixels and the third pixels enclose the first pixel in the virtual square.

[0032] In one embodiment, each of the second pixels and the third pixels is larger in area than the first pixel.

[0033] In one embodiment, the first pixel has an octagonal shape, and at least one of the second pixel or the third pixel has an octagonal shape.

[0034] In one embodiment, the first pixel has an octagonal shape, and one of the second pixel or the third pixel has a hexagonal shape and an other of the second pixel or the third pixel has a quadrilateral shape.

[0035] In one embodiment, the virtual square includes a pair of virtual squares sharing a common side, the first pixel includes a pair of first pixels having centers respectively coinciding with centers of the virtual squares, and the first pixels have octagonal shapes that are symmetrical to each other.

[0036] In one embodiment, each of the second pixels is larger in area than each of the third pixels.

[0037] In one embodiment, a distance between the first pixel and the second pixels as well as a distance between the first pixel and the third pixels is a same first length.

[0038] In one embodiment, the virtual square includes a pair of virtual squares sharing a common side, the first pixel includes a pair of first pixels having centers respectively coinciding with centers of the virtual squares, a distance between each of the second pixels and the third pixels is a same second length, and a distance between the first pixels is a third length that is longer than the first length and the second length.

[0039] In one embodiment, the first pixel, the second pixel, and the third pixel are configured to emit different color light.

[0040] In one embodiment, the first pixel is configured to emit green light, one of the second pixel or the third pixel is configured to emit blue light, and an other of the second pixel or the third pixel is configured to emit red light.

[0041] According to an exemplary embodiment of the present invention, the pixel arrangement structure of the OLED display improves the aperture ratio of the pixels while efficiently setting up the gaps between the pixels.

BRIEF DESCRIPTION OF THE DRAWINGS

[0042] FIG. 1 is a view of a pixel arrangement structure of an OLED display according to a first exemplary embodiment.

[0043] FIG. 2 is a view of a pixel arrangement structure of an OLED display according to a second exemplary embodiment.

[0044] FIG. 3 is a view of a pixel arrangement structure of an OLED display according to a third exemplary embodiment.

[0045] FIG. 4 is a view of a pixel arrangement structure of an OLED display according to a fourth exemplary embodiment.

[0046] FIG. 5 is a view of a pixel arrangement structure of an OLED display according to a fifth exemplary embodiment.

[0047] FIG. 6 is a view of a pixel arrangement structure of an OLED display according to a sixth exemplary embodiment.

DETAILED DESCRIPTION

[0048] Several exemplary embodiments according to the present invention are described hereinafter in detail with reference to the accompanying drawing to allow one of ordinary skill in the art to practice the invention without undue experimentation. The present invention can be embodied in several different forms, and is not limited to the exemplary embodiments that are described herein.

[0049] In order to clarify the description of embodiments of the present invention, parts that are not related to the invention may be omitted. In addition, the same elements or equivalents are referred to with the same reference numerals throughout the specification.

[0050] Further, since sizes and thicknesses of constituent members shown in the accompanying drawing may be arbitrarily given for better understanding and ease of description, the present invention is not limited to the illustrated sizes and thicknesses.

[0051] In addition, unless explicitly described to the contrary, the word "comprise" and variations such as "comprises" or "comprising" will be understood to imply the inclusion of stated elements but not the exclusion of any other elements.

[0052] Nevertheless, even though each of the pixels are drawn as stereotypical polygonal shapes in the drawings, the present invention is not limited to this shape. That is, the shapes of the pixels may be modified to avoid interference with the other components of the OLED (e.g., wirings) within the spirit and scope of the appended claims.

[0053] A pixel arrangement structure (or pixel arrangement) of an OLED display according to a first exemplary embodiment will be described with reference to FIG. 1. FIG. 1 is a view schematically showing a portion of pixels forming an OLED display.

[0054] As shown in FIG. 1, the pixel arrangement structure of the OLED display includes a plurality of first pixels 100, a plurality of second pixels 200, and a plurality of third pixels 300. Here, the pixel refers to a minimum unit for displaying an image (for example, the minimum addressable unit of the display).

[0055] Further, among the first pixels 100, the second pixels 200, and the third pixels 300, power lines for driving each of the pixels, such as a gate line, a data line, a driving power line, and the like, may be located. In addition, an insulation layer, such as a pixel defining layer, for defining each of the pixels may be disposed. Finally, an OLED including an anode, an organic emission layer, and a cathode to correspond to each of the first pixels 100, the second pixels 200, and the third pixels 300 may be disposed. These configurations are technologies known in the art and further description thereof is omitted for ease of description. A shape of each of the pixels may be defined by the power lines, the pixel defining layer, the anode, or the like, but is not limited thereto.

[0056] In the pixel arrangement of FIG. 1, each of the first pixels 100 has a smaller area than neighboring second pixels 200 and third pixels 300, and has a quadrilateral (i.e., four-sided) shape among polygon shapes. For example, in the pixel arrangement of FIG. 1, each of the first pixels 100 has the same quadrilateral shape (e.g., a square or rhombus). The first pixels 100 are spaced apart from each other and arranged in rows, such as along a first virtual straight line VL1. The first pixels 100 emit green light, and may include an organic emission layer for emitting green light.

[0057] The second pixels 200 are arranged diagonally with respect to the first pixels 100, such as at first vertices P1 along one diagonal of a virtual square VS having one of the first pixels 100 as a center point (or center) of the virtual square VS. In a similar fashion, the third pixels 300 are arranged diagonally with respect to the first pixels 100, such as at second vertices P2 along the other diagonal of the virtual square VS.

[0058] In the virtual square VS, each of the second pixels 200 is separated from the first pixel 100, and is centered at one of the first vertices P1 of the virtual square VS. Each of the second pixels 200 has a larger area than the neighboring first pixel 100 and has an octagonal (i.e., eight-sided) shape. In FIG. 1, the second pixels 200 each have the same octagonal shape. In addition, the second pixels 200 are arranged diagonally and separated from each other by the first pixels 100. The second pixels 200 emit blue light, and may include an organic emission layer for emitting blue light.

[0059] In a similar fashion, in the virtual square VS, each of the third pixels 300 is separated from the first pixel 100 and the second pixels 200, and is centered at one of the second vertices P2 neighboring the first vertices P1 of the virtual square VS. Each of the third pixels 300 has a larger area than the neighboring first pixel 100 and the same area as each of the second pixels 200. Further, the third pixels have an octagonal shape (e.g., similar to or the same as the second pixels 200). In FIG. 1, the third pixels 300 each have the same octagonal shape. In addition, the third pixels 300 are arranged diagonally and separated from each other by the first pixels 100. The third pixels 300 emit red light, and may include an organic emission layer for emitting red light.

[0060] The third pixels 300 and the second pixels 200 are spaced apart from each other and alternately arranged in rows, such as along a second virtual straight line VL2. In a similar fashion, the third pixels 300 and the second pixels 200 are spaced apart from each other and alternately arranged in columns. Accordingly, in the virtual square VS, two of the second pixels 200 having their corresponding centers positioned at the first vertices P1 and two of the third pixels 300 having their corresponding centers positioned at the second vertices P2 to enclose a corresponding one of the first pixels 100 (e.g., in the virtual square VS).

[0061] As described above, the center of each of the second pixels 200 is positioned at one of the first vertices P1 of the virtual square VS. In addition, the

center of the corresponding first pixel 100 is the center of the virtual square VS. Further, the center of each of the third pixels 300 is positioned at one of the second vertices P2. Moreover, the second pixels 200 and the third pixels 300 each have the same area.

[0062] As a non-limiting example, the distance (e.g., a shortest distance) between one of the first pixels 100 and an adjacent one of the second pixels 200 is a first length L1, the distance between one of the first pixels 100 and an adjacent one of the third pixels 300 is the same first length L1, and the distance between one of the second pixels 200 and an adjacent one of the third pixels 300 is the same first length L1, as shown in FIG. 1. In addition, the distance (e.g., a shortest distance) between the neighboring first pixels 100 is a second length L2 that is longer than the first length L1. It should be noted that L1, L2, L3, . . . may be used throughout to represent shortest distances between corresponding pixels.

[0063] Therefore, the gap of the first length L1 is formed between adjacent pairs of the first pixels 100 and the second pixels 200, between adjacent pairs of the first pixels 100 and the third pixels 300, and between adjacent pairs of the second pixels 200 and the third pixels 300. In addition, the gap of the second length L2 that is longer than the first length L1 is formed between the neighboring ones of the first pixels 100. This results in improved deposition reliability when using a fine metal mask to form the green, blue, and red organic emission layers respectively included in the first pixels 100, the second pixels 200, and the third pixels 300.

[0064] In addition, by enclosing each of the first pixels 100 by a pair of the second pixels 200 and a pair of the third pixels 300, the aperture ratio of the first pixels 100, the second pixels 200, and the third pixels 300 may be improved. Accordingly, a manufacturing time and manufacturing cost of the entire OLED display may be reduced and the display quality of the image of the OLED display may be improved.

[0065] As described above, in the pixel arrangement structure of the OLED display of FIG. 1, the first pixels 100, the second pixels 200, and the third pixels 300 have polygonal shapes (e.g., the first pixels have a quadrilateral shape and the second pixels 200 and the third pixels 300 have an octagonal shape). In addition, it is worth considering that the deposition process of the organic emission layer is one of the unique manufacturing characteristics of the OLED display. Accordingly, to improve the deposition reliability of the organic emission layer in the deposition process using the fine metal mask and to improve the aperture ratio of the first pixels 100, the second pixels 200, and the third pixels 300, the center of each of the first pixels 100 is positioned at the center of a virtual square VS formed by a first pair of diagonal vertices P1 and a second pair of diagonal vertices P2. In the virtual square VS, the centers of a pair of the second pixels 200 are positioned at the first vertices P1, and the centers of a pair of the third pixels 300 are positioned at the second vertices P2.

[0066] In addition, in the pixel arrangement structure of the OLED display of FIG. 1, the first pixels 100, the second pixels 200, and the third pixels 300 respectively emit green, blue, and red light. However, in pixel arrangement structures of other OLED displays, the first pixels 100, the second pixels 200, and the third pixels 300 may emit light of different colors. For example, at least one of the second pixels 200 or the third pixels may emit white light.

[0067] Next, a pixel arrangement structure of an OLED display according to a second exemplary embodiment will be described with reference to FIG. 2. Parts that are different from the exemplary embodiment of FIG. 1 will be described, while the description of parts that are equivalent to the first exemplary embodiment may be omitted. For better comprehension and ease of description, constituent elements of the second exemplary embodiment that are the same as or similar to those of the first embodiment of FIG. 1 will have the same reference numerals.

[0068] As shown in FIG. 2, the pixel arrangement structure of the OLED display includes a plurality of first pixels 100, a plurality of second pixels 200, and a plurality of third pixels 300. The plurality of first pixels 100 have the same quadrilateral shape (e.g., a parallelogram). In addition, the second pixels 200 have a larger area than the third pixels 300. The second pixels 200 and the third pixels 300 may have polygonal shapes, such as octagonal or hexagonal (i.e., six-sided).

[0069] In a similar fashion to that of FIG. 1, the centers of a pair of the second pixels 200 are positioned at first vertices P1 along one diagonal of a virtual square VS having a center coinciding with a center of one of the first pixels 100. In addition, the centers of a pair of the third pixels 300 are positioned at second vertices P2 along another diagonal of the virtual square VS. However, in FIG. 2, the second pixels 200 have a larger area than the third pixels 300.

[0070] As a non-limiting example, the distance between adjacent ones of the second pixels 200 and the third pixels 300 is a third length L3, while the distance between each of the first pixels 100 and adjacent ones of the second pixels 200 or the third pixels 300 have a same fourth length L4. In addition, the distance between neighboring ones of the first pixels 100 is a fifth length L5 that is longer than the third length L3 and the fourth length L4.

[0071] Accordingly, the gap of the fourth length L4 is formed between adjacent pairs of the first pixels 100 and the second pixels 200, and between adjacent pairs of the first pixels 100 and the third pixels 300. In addition, the gap of the third length L3 is formed between adjacent pairs of the second pixels 200 and the third pixels 300. Further, the gap of the fifth length L5 that is longer than the third length L3 and the fourth length L4 is formed between the neighboring ones of the first pixels 100. This results in improved deposition reliability in the deposition process using the fine metal mask to form the green, blue, and red organic emission layers respectively included in the first pixels 100, the second pixels 200, and the third pixels 300.

[0072] In addition, by enclosing each of the first pixels 100 by a pair of the second pixels 200 and a pair of the third pixels 300, the aperture ratio of the first pixels 100, the second pixels 200, and the third pixels 300 may be improved. Accordingly, the manufacturing time and the manufacturing cost of the OLED display may be reduced and the display quality of the image of the OLED display may be improved.

[0073] Further, in the pixel arrangement structure of the OLED display of FIG. 2, the second pixels 200 that emit blue have the shortest life span among the first pixels 100, the second pixels 200, and the third pixels 300. Accordingly, the second pixels 200 have a larger area than the third pixels 300, thereby suppressing the deterioration of the life span of the OLED display. That is, the pixel arrangement structure of the OLED display of FIG. 2 provides improved life span.

[0074] Next, a pixel arrangement structure of an OLED display according to a third exemplary embodiment will be described with reference to FIG. 3. Parts that are different from the above exemplary embodiments will be described, while the description of parts that are equivalent to the above exemplary embodiments may be omitted. For better comprehension and ease of description, constituent elements of the third exemplary embodiment that are the same as or similar to the above exemplary embodiments will have the same reference numerals.

[0075] As shown in FIG. 3, the pixel arrangement structure of the OLED display includes a plurality of first pixels 100, a plurality of second pixels 200, and a plurality of third pixels 300. Among the plurality of first pixels 100, the neighboring first pixels 100 have a quadrilateral shape (e.g., parallelogram) and are symmetrical to each other. In addition, the second pixels 200 have a larger area than the third pixels 300. The second pixels 200 and the third pixels may have polygonal shapes (e.g., hexagonal or octagonal).

[0076] In a similar fashion to that of FIGs. 1–2, the centers of a pair of the second pixels 200 are positioned at first vertices P1 along one diagonal of a virtual square VS

having a center coinciding with a center of one of the first pixels 100. In addition, the centers of a pair of the third pixels 300 are positioned at second vertices P2 along another diagonal of the virtual square VS. However, in FIG. 3, the neighboring first pixels 100 have a quadrilateral shape and are symmetrical to each other, while the second pixels 200 have a larger area than the third pixels 300. This results in improved deposition reliability in the deposition process using the fine metal mask to form the green, blue, and red organic emission layers respectively included in the first pixels 100, the second pixels 200, and the third pixels 300.

[0077] In addition, by placing each of the first pixels 100 between a pair of the second pixels 200 and between a pair of the third pixels 300, the aperture ratio of the first pixels 100, the second pixels 200, and the third pixels 300 may be improved. Accordingly, the manufacturing time and the manufacturing cost of the OLED display may be reduced and the display quality of the image of the OLED display may be improved.

[0078] Further, in the pixel arrangement structure of the OLED display of FIG. 3, the second pixels 200 that emit blue have the shortest life span among the first pixels 100, the second pixels 200, and the third pixels 300. Accordingly, the second pixels 200 have a larger area than the third pixels 300, thereby suppressing the deterioration of the life span of the OLED display. That is, the pixel arrangement structure of the OLED display provides improved life span.

[0079] Next, a pixel arrangement structure of an OLED display according to a fourth exemplary embodiment will be described with reference to FIG. 4. Parts that are different from the above exemplary embodiments will be described, while the description of parts that are equivalent to the above exemplary embodiments may be omitted. For better comprehension and ease of description, constituent elements of the fourth exemplary embodiment that are the same as or similar to the above exemplary embodiments will have the same reference numerals.

[0080] As shown in FIG. 4, the pixel arrangement structure of the OLED display includes a plurality of first pixels 100, a plurality of second pixels 200, and a plurality of third pixels 300. Among the plurality of first pixels 100, the neighboring first pixels 100 have a quadrilateral shape (e.g., parallelogram) and are symmetrical to each other. In addition, the third pixels 300 have a larger area than the second pixels 200. The second pixels 200 and the third pixels may have polygonal shapes (e.g., hexagonal or octagonal).

[0081] In a similar fashion to that of FIGs. 1–3, the centers of a pair of the second pixels 200 are positioned at the first vertices P1 along one diagonal of a virtual square VS having a center coinciding with a center of one of the first pixels 100. In addition, the centers of a pair of the third pixels 300 are positioned at second vertices P2 along another diagonal of the virtual square VS. However, in FIG. 4, the neighboring first pixels 100 have a quadrilateral shape and are symmetrical to each other, while the third pixels 300 have a larger area than the second pixels 200. This results in improved deposition reliability in the deposition process using the fine metal mask to form the green, blue, and red organic emission layers respectively included in the first pixels 100, the second pixels 200, and the third pixels 300.

[0082] In addition, by enclosing each of the first pixels 100 by a pair of the second pixels 200 and a pair of the third pixels 300, the aperture ratio of the first pixels 100, the second pixels 200, and the third pixels 300 may be improved. Accordingly, the manufacturing time and the manufacturing cost of the OLED display may be reduced and the display quality of the image of the OLED display may be improved.

[0083] Next, a pixel arrangement structure of an OLED display according to a fifth exemplary embodiment will be described with reference to FIG. 5. Parts that are different from the above exemplary embodiments will be described, while the description of parts that are equivalent to the above exemplary embodiments may be omitted. For better comprehension and ease of description, constituent elements of

the fifth exemplary embodiment that are the same as or similar to the above exemplary embodiments will have the same reference numerals.

[0084] As shown in FIG. 5, the pixel arrangement structure of the OLED display includes a plurality of first pixels 100, a plurality of second pixels 200, and a plurality of third pixels 300. Among the plurality of first pixels 100, the neighboring first pixels 100 have a octagonal shape and are symmetrical to each other. In addition, the second pixels 200 have a larger area than the third pixels 300. The second pixels 200 and the third pixels 300 may have quadrilateral shapes (e.g., rhombus).

[0085] In a similar fashion to that of FIGs. 1–3, the centers of a pair of the second pixels 200 are positioned at the first vertices P1 along one diagonal of a virtual square VS having a center coinciding with a center of one of the first pixels 100. In addition, the centers of a pair of the third pixels 300 are positioned at second vertices P2 along another diagonal of the virtual square VS. However, in FIG. 5, the neighboring first pixels 100 have a octagonal shape and are symmetrical to each other, while the second pixels 200 have a larger area than the third pixels 300. This results in improved deposition reliability in the deposition process using the fine metal mask to form the green, blue, and red organic emission layers respectively included in the first pixels 100, the second pixels 200, and the third pixels 300.

[0086] In addition, by enclosing each of the first pixels 100 by a pair of the second pixels 200 and a pair of the third pixels 300, the aperture ratio of the first pixels 100, the second pixels 200, and the third pixels 300 may be improved. Accordingly, the manufacturing time and the manufacturing cost of the OLED display may be reduced and the display quality of the image of the OLED display may be improved.

[0087] Hereinafter, a pixel arrangement structure (or pixel arrangement) of an OLED display according to an exemplary embodiment will be described with reference to FIG. 6. FIG. 6 is a view schematically showing a portion of pixels forming an OLED display.

[0088] FIG. 6 shows a pixel arrangement structure of an OLED display according to an exemplary embodiment of the present invention.

[0089] As shown in FIG. 6, the pixel arrangement structure of the OLED display includes a plurality of first pixels 100, a plurality of second pixels 200, and a plurality of third pixels 300.

[0090] According to one embodiment, the pixel refers to a minimum unit for displaying an image (for example, the minimum addressable unit of the display).

[0091] In one embodiment, among the first pixels 100, the second pixels 200, and the third pixels 300, power lines for driving each of the pixels, such as a gate line, a data line, a driving power line, and the like, are located. In addition, in one embodiment, an insulation layer, such as a pixel defining layer, for defining each of the pixels is disposed. Further, in one embodiment, an OLED including an anode, an organic emission layer, and a cathode to correspond to each of the first pixels 100, the second pixels 200, and the third pixels 300 is disposed. These configurations are technologies known in the art and further description thereof is omitted for ease of description. In one embodiment, the shape of each of the pixels is defined by the power lines, the pixel defining layer, the anode, or the like.

[0092] In the pixel arrangement of FIG. 6, each of the first pixels 100 has a smaller area (e.g., is smaller in area) than neighboring second pixels 200 and third pixels 300, and has a polygon shape. In FIG. 6, the first pixels 100 have an octagonal shape among the polygon shapes. In other embodiments, the first pixels 100 have one or more of various polygon shapes such as a triangle, a rectangle, a pentagon, a hexagon, a heptagon, and the like. For example, the first pixels 100 that neighbor each other among the plurality of first pixels 100 have hexagon shapes that are symmetrical to each other. In one embodiment, each of the plurality of first pixels 100 has the same hexagonal shape.

[0093] In one embodiment, the first pixels 100 are spaced apart from each other and arranged in rows, such as along a first virtual straight line VL1. In one embodiment, the first pixels 100 emit green light, and include an organic emission layer for emitting green light. In other embodiments, the first pixels 100 include an organic emission layer that emits light of one or more of various colors such as blue, red, or white color for emitting blue light, red light, or white light.

[0094] In FIG. 6, the second pixels 200 are arranged diagonally with respect to the first pixels 100, namely at first vertices P1 along one diagonal of a virtual square VS having one of the first pixels 100 as a center point (or center) of the virtual square VS. In a similar fashion, in FIG. 6, the third pixels 300 are arranged diagonally with respect to the first pixels 100, namely at second vertices P2 along the other diagonal of the virtual square VS.

[0095] In the virtual square VS of FIG. 6, each of the second pixels 200 is separated from the first pixel 100, and is centered at one of the first vertices P1 of the virtual square VS. Each of the second pixels 200 has a larger area than the neighboring first pixel 100 and the neighboring third pixels 300, and has a hexagonal shape. In other embodiments, the second pixels 200 have one or more of various polygonal shapes such as a triangle, a rectangle, a pentagon, a hexagon, a heptagon, and the like.

[0096] In FIG. 6, the second pixels 200 each have the same hexagonal shape. In addition, the second pixels 200 are arranged diagonally and separated from each other by the first pixels 100. In one embodiment, the second pixels 200 emit blue light, and include an organic emission layer for emitting blue light. In other embodiments, the second pixels 200 include an organic emission layer that emits light of one or more of various colors such as red, green, or white for emitting red light, green light, or white light.

[0097] In a similar fashion, in the virtual square VS of FIG. 6, each of the third pixels 300 is separated from the first pixel 100 and the second pixels 200, and is centered at one of the second vertices P2 neighboring the first vertices P1 of the virtual square VS. Each of the third pixels 300 has a larger area than the neighboring first pixel 100 and a smaller area than the neighboring second pixels 200. The third pixels 300 has a quadrilateral shape among polygon shapes. In other embodiments, the third pixels 300 have one or more of various polygonal shapes such as a triangle, a rectangle, a pentagon, a hexagon, a heptagon, and the like.

[0098] In FIG. 6, the third pixels 300 each have the same quadrilateral shape. In addition, the third pixels 300 are arranged diagonally and separated from each other by the first pixels 100. In one embodiment, the third pixels 300 emit red light, and include an organic emission layer for emitting red light. In other embodiments, the third pixels 300 include an organic emission layer that emits light of one or more of various colors such as blue, green, or white for emitting emit blue light, green light, or white light.

[0099] In FIG. 6, each of the second pixels 200 and the third pixels 300 has a hexagonal shape and a quadrilateral shape, respectively. In another embodiment, each of the second pixels 200 and the third pixels 300 respectively has a quadrilateral shape and a hexagonal shape. That is, in this other embodiment, one of the second pixels 200 or the third pixels 300 has a hexagonal shape and the other has a quadrilateral shape.

[00100] In one embodiment, the first pixels 100, the second pixels 200, and the third pixels 300 respectively emit green light, blue light, and red light. In other embodiments, the first pixels 100, the second pixels 200, and the third pixels 300 emit light of the same color. In still other embodiments, the first pixels 100, the second pixels 200, and the third pixels 300 emit light of different colors. In some embodiments, the first pixels 100 emit green light, and one of the second pixels 200 or the third pixels 300 emit blue light while the other emit red light.

[00101] In FIG. 6, third pixels 300 and the second pixels 200 are spaced apart from each other and alternately arranged in rows, such as along a second virtual straight line VL2. In a similar fashion, in FIG. 6, the third pixels 300 and the second pixels 200 are spaced apart from each other and alternately arranged in columns. Accordingly, in FIG. 6, in the virtual square VS, two of the second pixels 200 have their corresponding centers positioned at the first vertices P1 and two of the third pixels 300 have their corresponding centers positioned at the second vertices P2 to enclose a corresponding one of the first pixels 100 in the virtual square VS.

[00102] As described and illustrated in FIG. 6, the center of each of the second pixels 200 is positioned at one of the first vertices P1 of the virtual square VS. In addition, the center of the corresponding first pixel 100 is the center of the virtual square VS. Further, the center of each of the third pixels 300 is positioned at one of the second vertices P2. Therefore, the plurality of second pixels 200 of which the centers are positioned at the first vertices P1 and the plurality of third pixels 300 of which the centers are positioned at the second vertices P2 respectively enclose one of the first pixels 100 in the virtual square VS.

[00103] Further, and as illustrated in FIG. 6, the first pixels 100, the second pixels 200, and the third pixels 300 have polygon shapes. In FIG. 6, the distance between one of the first pixels 100 and an adjacent one of the second pixels 200 as well as a distance between one of the first pixels 100 and an adjacent one of the third pixels 300 is the same first length L1. In addition, a distance between one of the second pixels 200 and an adjacent one of the third pixels 300 is a second length L2 that is different from the first length L1. Further, in FIG. 6, a distance between neighboring first pixels 100 is a third length L3 that is longer than the first length L1 and the second length L2.

[00104] For example, in some embodiments, the first length L1 is between 15 um (micrometers) and 35 um, the second length L2 is between 20 um and 45 um, and the third length L3 is between 25 um and 65 um.

[00105] Therefore, gaps of the first length L1 are formed between adjacent pairs of the first pixels 100 and the second pixels 200, and between adjacent pairs of the first pixels 100 and the third pixels 300. In addition, the gaps of the third length L3 that is longer than the first length L1 are formed between the neighboring ones of the first pixels 100. In one embodiment, this results in improved deposition reliability in the deposition process using the fine metal mask to form the green, blue, and red organic emission layers respectively included in the first pixels 100, the second pixels 200, and the third pixels 300.

[00106] In addition, in one embodiment, the plurality of second pixels 200 and the plurality of third pixels 300 are arranged to enclose the first pixels 100 in the virtual squares VS so that an aperture ratio of each of the first pixels 100, the second pixels 200, and the third pixels 300 can be improved. Accordingly, in one embodiment, the manufacturing time and the manufacturing cost of the OLED display is reduced and the display quality of the image of the OLED display is improved.

[00107] Further, in the pixel arrangement structure of the OLED display of FIG. 6 according to an exemplary embodiment of the present invention, the second pixels 200 that emit blue light have the shortest life span among the first pixels 100, the second pixels 200, and the third pixels 300. Accordingly, the second pixels 200 have a larger area than the first pixels 100 and the third pixels 300, thereby suppressing the deterioration of the life span of the OLED display. That is, in one embodiment, the pixel arrangement structure of the OLED display of FIG. 6 provides improved life span.

[00108] As described above, in the pixel arrangement structure of the OLED display of FIG. 6 according to an exemplary embodiment of the present invention, the first pixels 100, the second pixels 200, and the third pixels 300 have simple polygonal shapes such as an octagon, a hexagon, and a quadrangle. In consideration of the deposition process of the organic emission layer, which in one embodiment is a unique manufacturing feature of the OLED display, a center of one of the first pixels 100 is

positioned at the center of the virtual square VS, a center of one of the second pixels 200 is positioned at the first vertex P1, and a center of one of the third pixels 300 is positioned at the second vertex P2 to both improve deposition reliability of the organic emission layer in the deposition process using the fine metal mask and improve an aperture of each of the first, second, and third pixels 100, 200, and 300.

[00109] That is, according to an exemplary embodiment of the present invention as illustrated in FIG. 6, the pixel arrangement structure of the OLED display includes a plurality of first pixels 100 having an octagonal shape, a plurality of second pixels 200 having a hexagonal shape, and a plurality of third pixels 300 having a quadrilateral shape. In one or more embodiments, the shapes and arrangement of the first pixels 100, the second pixels 200, and the third pixels 300 improve the deposition reliability of the organic emission layer while also improving the aperture ratio of each of the first pixels 100, the second pixels, 200, and the third pixels 300.

[00110] While this invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, and equivalents thereof.

<Description of some symbols>

first pixel 100, second pixels 200, third pixels 300

WHAT IS CLAIMED IS:

1. An organic light emitting diode (OLED) display, comprising:

a plurality of individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display and comprising:

a plurality of red pixels comprising an organic emission layer for emitting red light;

a plurality of blue pixels comprising an organic emission layer for emitting blue light; and

a plurality of green pixels comprising an organic emission layer for emitting green light;

wherein each of the red pixels, the blue pixels, and the green pixels are spaced apart from each other;

wherein a first one of the green pixels has a center coinciding with a center of a virtual square, each vertex of the virtual square coinciding with a center of a different one of the green pixels and each edge of the virtual square passing through three consecutive green pixels;

wherein at least two of the blue pixels and at least two of the red pixels are located within the boundaries of the virtual square;

wherein a shortest distance between the first green pixel and one of the at least two blue pixels within the virtual square as well as a shortest distance between the first green pixel and one of the at least two red pixels within the virtual square is a same first length;

wherein the first length is smaller than a shortest distance between the first green pixel and an adjacent one of the green pixels;

wherein each of the at least two blue pixels has a larger area than each of the at least two red pixels;

wherein each of the at least two blue pixels has a larger area than that of the first green pixel; and

wherein the first green pixel has a convex shape such that a line bisecting the first pixel along its long axis has a greater length than a line bisecting the first pixel along its short axis.

2. The display of claim 1, wherein the first length is smaller than a shortest distance between one of the at least two blue pixels and one of the at least two red pixels.

3. The display of claim 2, wherein the first green pixel has a different shape than the one of the blue pixels and the one of the red pixels.

4. The display of claim 2, wherein the one of the red pixels has a larger area than that of the first pixel.

5. The display of claim 2, wherein the one of the blue pixels and the one of the red pixels are four-sided polygons.

6. The display of claim 1, wherein the first length is equal to a shortest distance between one of the at least two blue pixels and one of the at least two red pixels.

7. The display of claim 6, wherein the first green pixel has a different shape than the one of the blue pixels and the one of the red pixels.

8. The display of claim 6, wherein the one of the red pixels has a larger area than that of the first pixel.

9. The display of claim 6, wherein the one of the blue pixels and the one of the red pixels are four-sided polygons.

10. A method for manufacturing an organic light emitting diode (OLED) display, comprising:

depositing, using a fine metal mask, organic light-emitting material configured to emit a first color of light;

forming a plurality of first pixels to emit the first color of light;

depositing, using a fine metal mask, organic light-emitting material configured to emit a second color of light;

forming a plurality of second pixels to emit the second color of light;

depositing, using a fine metal mask, organic light-emitting material configured to emit a third color of light; and

forming a plurality of third pixels to emit the third color of light;

wherein:

the first pixels, the second pixels, and the third pixels are individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display;

each of the first pixels, the second pixels, and the third pixels are spaced apart from each other;

one of the first pixels has a center coinciding with a center of a virtual square, each vertex of the virtual square coinciding with a center of a different one of the first

pixels and each edge of the virtual square passing through three consecutive first pixels;

wherein at least two of the second pixels and at least two of the third pixels are within the boundaries of the virtual square;

wherein a shortest distance between the one of the first pixels and one of the at least two second pixels within the virtual square as well as a shortest distance between the one of the first pixels and one of the at least two third pixels within the virtual square is a same first length;

wherein the first length is smaller than a shortest distance between the one of the first pixels and an adjacent one of the first pixels;

wherein each of the at least two second pixels has a larger area than each of the at least two third pixels;

wherein each of the at least two second pixels has a larger area than that of the one of the first pixels; and

wherein the one of the first pixels has a convex shape such that a line bisecting the one of the first pixels along its long axis has a greater length than a line bisecting the one of the first pixels along its short axis.

11. The method of claim 10, wherein the first pixels are formed before the second and third pixels are formed.

12. The method of claim 10, wherein the second pixels are formed before the first and third pixels are formed.

13. The method of claim 10, wherein the third pixels are formed before the first and second pixels are formed.

14. The method of claim 10, wherein the one of the first pixels has a different shape than the one of the at least two second pixels and the one of the at least two third pixels.

15. The method of claim 10, wherein the one of the at least two third pixels has a larger area than that of the one of the first pixels.

16. The method of claim 10, wherein the one of the at least two second pixels and the one of the at least two third pixels are four-sided polygons.

17. The method of claim 10, wherein the first pixels include an organic emission layer for emitting green light, the second pixels include an organic emission layer for emitting blue light, and the third pixels include an organic emission layer for emitting red light.

18. The method of claim 17, wherein the first length is smaller than a shortest distance between the one of the at least two second pixels and the one of the at least two third pixels.

19. The method of claim 18, wherein the one of the first pixels has a different shape than the one of the at least two second pixels and the one of the at least two third pixels.

20. The method of claim 18, wherein the one of the at least two third pixels has a larger area than that of the one of the first pixels.

21. The method of claim 18, wherein the one of the at least two second pixels and the one of the at least two third pixels are four-sided polygons.

22. The method of claim 17, wherein the first length is equal to a shortest distance between the one of the at least two second pixels and the one of the at least two third pixels.

23. The method of claim 22, wherein the one of the first pixels has a different shape than the one of the at least two second pixels and the one of the at least two third pixels.

24. The method of claim 22, wherein the one of the at least two third pixels has a larger area than that of the one of the first pixels.

25. The method of claim 22, wherein the one of the at least two second pixels and the one of the at least two third pixels are four-sided polygons.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	224123/411598-06419
	Application Number	
Title of Invention	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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For further information see 37 CFR 1.33(a).

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Customer Number	23363		
Email Address	pto@lewisroca.com	Add Email	Remove Email

Application Information:

Title of the Invention	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY		
Attorney Docket Number	224123/411598-06419	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	**Suggested Figure for Publication (if any)**	

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Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	23363		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17/005753	2020-08-28

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	224123/411598-06419
	Application Number	
Title of Invention	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17/005753	Continuation of	13/872018	2013-04-26	10832616	2020-11-10

Prior Application Status: Patented — Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/872018	Continuation in part of	13/614197	2012-09-13	9818803	2017-11-14

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. — Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
10-2012-0022967	KR	2012-03-06	506F

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
10-2013-0044993	KR	2013-04-23	gnkPLfnhL4

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☒ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	224123/411598-06419
	Application Number	
Title of Invention	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (01-22)
Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	224123/411598-06419
	Application Number	
Title of Invention	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	SAMSUNG DISPLAY CO., LTD.

Mailing Address Information For Applicant:

Address 1	1, Samsung-ro, Giheung-gu		
Address 2			
City	Yongin-si, Gyeonggi-do	**State/Province**	
Country	KR	Postal Code	17113
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (01-22)
Approved for use through 05/31/2024. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	224123/411598-06419
	Application Number	
Title of Invention	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Steven French/			Date (YYYY-MM-DD)	2022-06-24
First Name	Steven	Last Name	French	Registration Number	78743

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (01-22)
Approved for use through 05/31/2024. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	224123/411598-06419
	Application Number	
Title of Invention	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Sang-Shin Lee	Nonprovisional Application Number (if known):	To Be Determined
Title of Invention:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.
2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.
3. The applicable box is checked below:

I. ☑ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Steven French/	Date June 24, 2022
Name (Print/Typed) Steven French	Practitioner Registration Number 78743

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☐ *Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

FIG.1

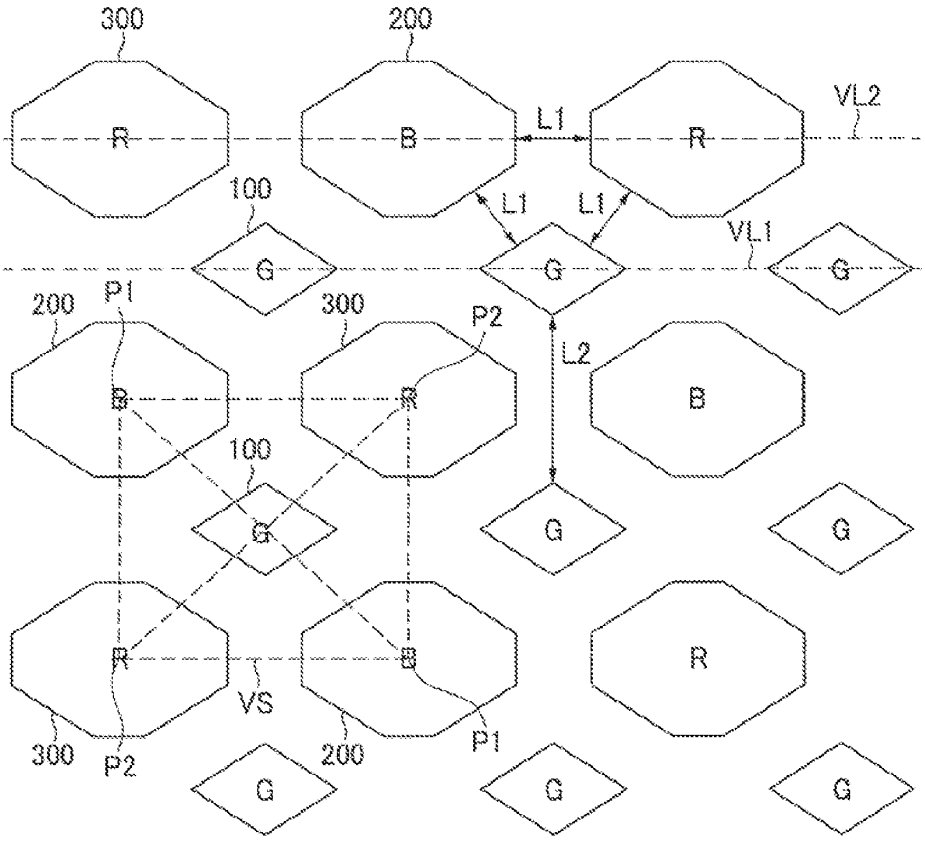

300
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B
R
L1
VL2
100
L1
L1
VL1
G
G
G
200
P1
300
P2
L2
B
R
B
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G
G
G
R
B
R
VS
300
P2
200
P1
G
G
G

FIG.2

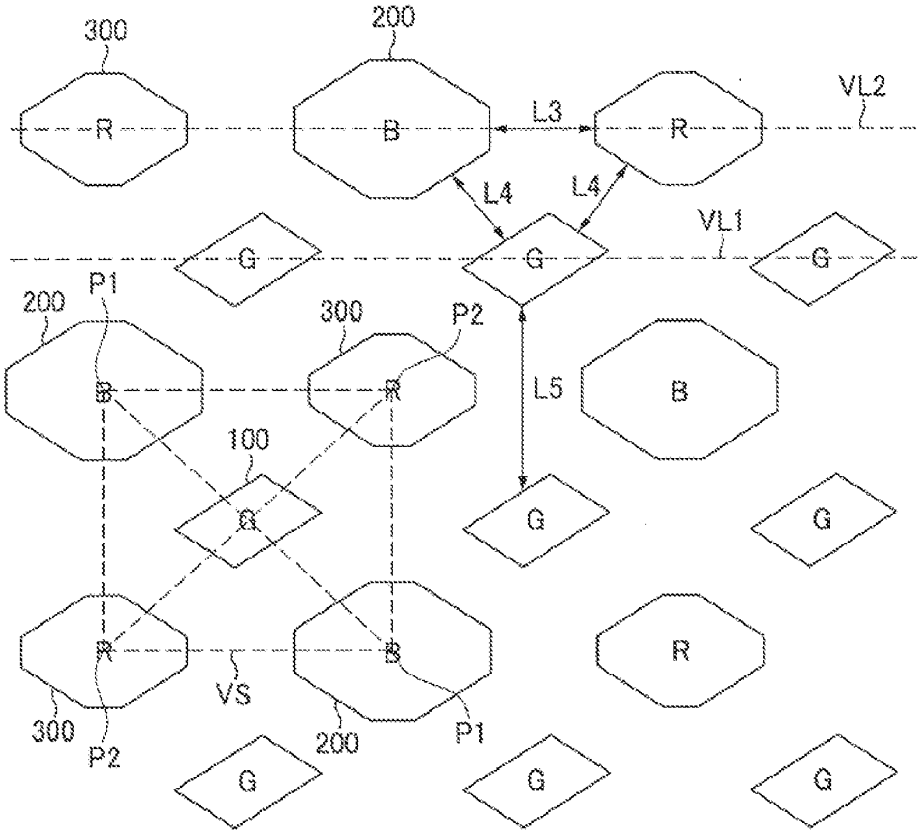

300
200
R
B
L3
R
VL2
L4
L4
VL1
G
G
G
200
P1
300
P2
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P1
G
G
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FIG.3

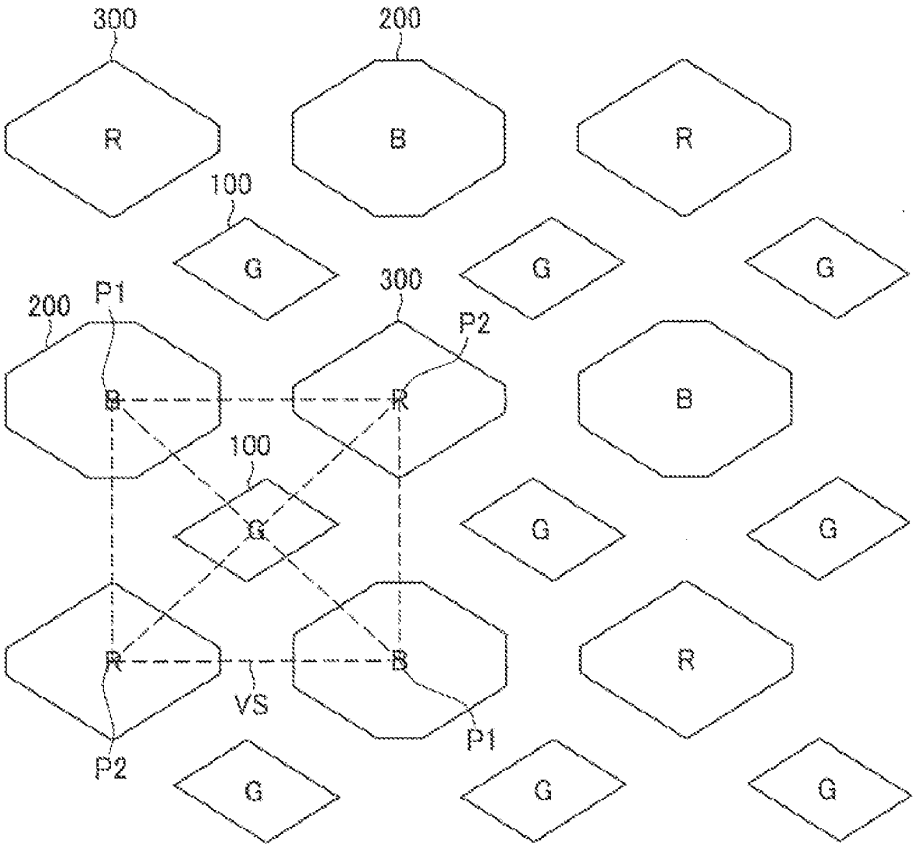


FIG.4

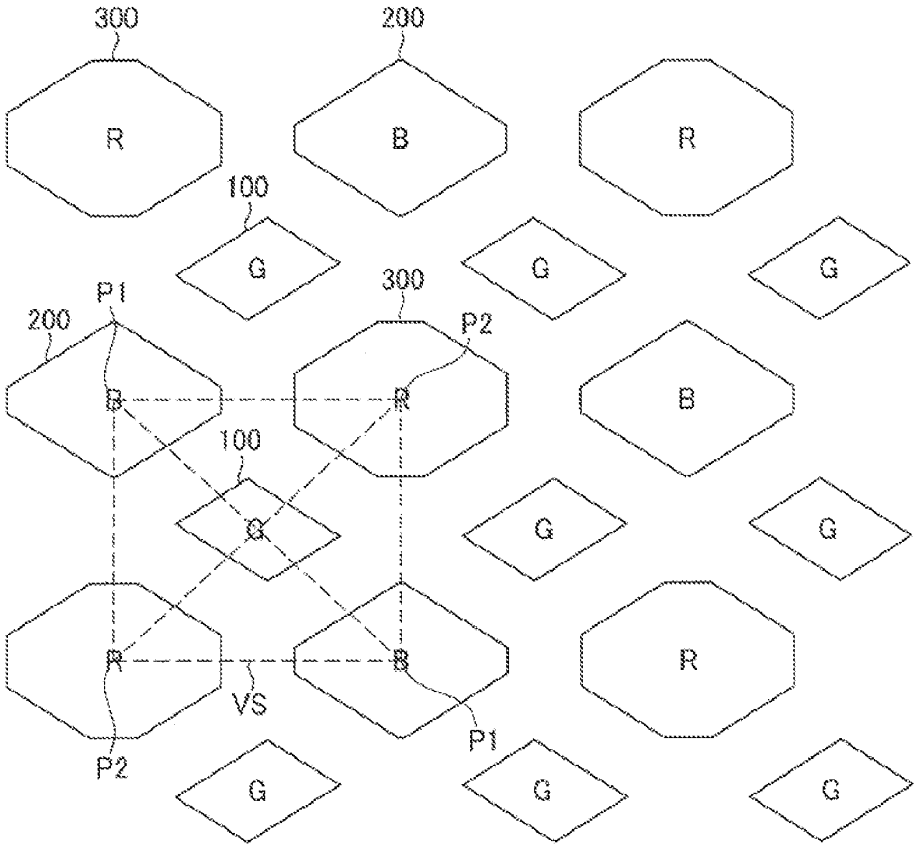
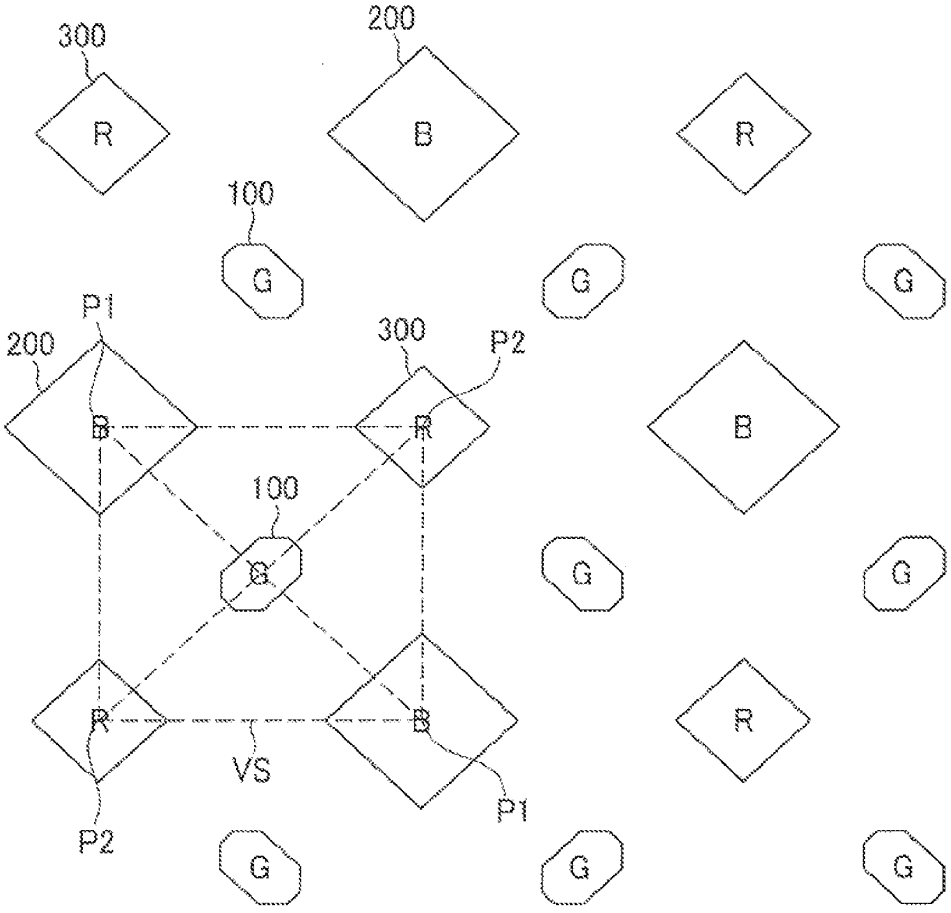


FIG.5



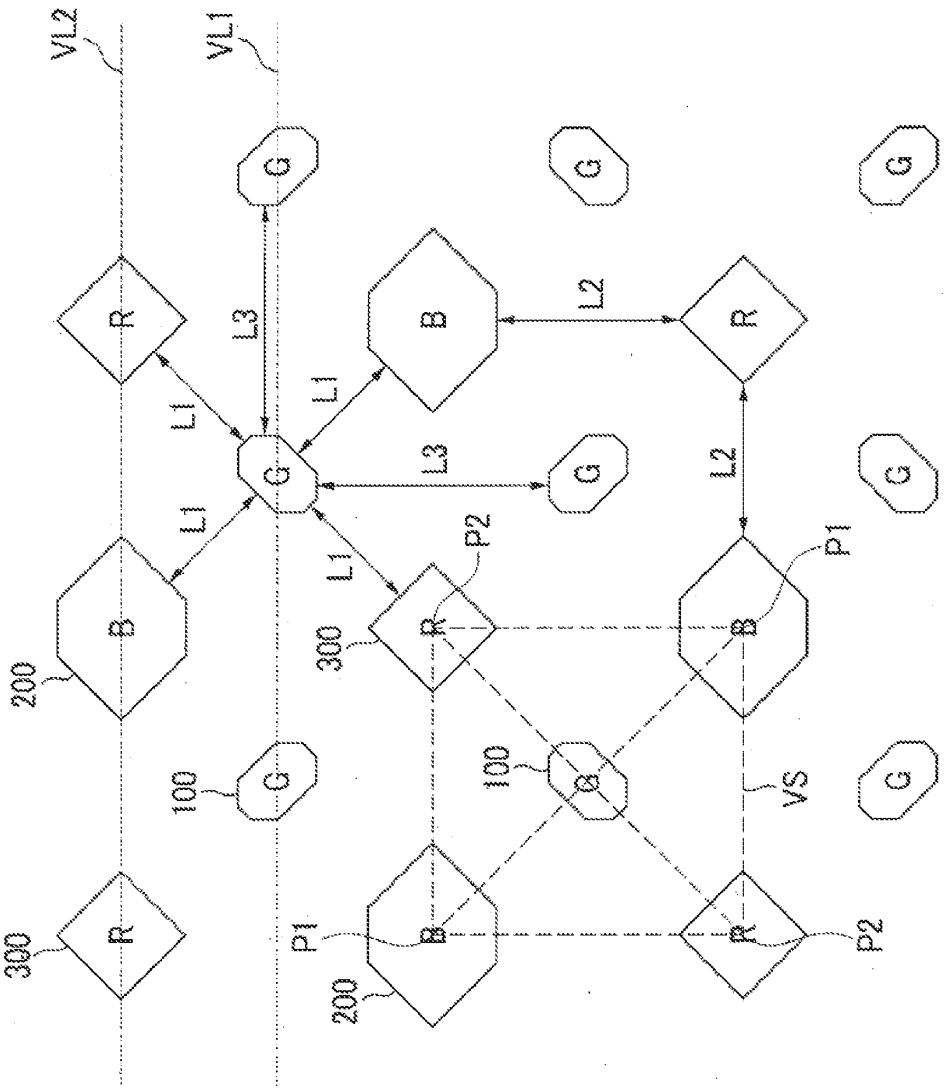

VL2
VL1
G
G
G
R
L3
B
L2
R
L1
L1
G
L3
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L2
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L1
P2
P1
L1
300
R
B
200
B
100
G
100
G
VS
G
300
R
P1
B
R
P2
200

FIG. 6

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PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	**06/24/2022 11:27:01 PM ET**	**224123/411598-06419**

Title of Invention

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4376	FILED BY	Si Vuong
PATENT CENTER #	60740671	FILING DATE	-
CUSTOMER #	23363	FIRST NAMED INVENTOR	Sang-Shin LEE
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Steven French

Documents

TOTAL DOCUMENTS: 9

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
224123_ADS.pdf	8	Application Data Sheet	2174 KB
224123_TrackOneRequest.pdf	2	Track One Request	112 KB
224123_CONApplicationTransmittal.pdf	3	Transmittal of New Application	148 KB
224123_ParentDec_08272020.pdf	2	Oath or Declaration filed	124 KB
224123_Abstract.pdf	1	Abstract	86 KB
224123_Claims.pdf	6	Claims	74 KB

224123_CONDrawingsAsFiled.pdf	6	Drawings-only black and white line drawings	191 KB
224123_Specification.pdf	22	Specification	108 KB
224123_POA.pdf	2	Power of Attorney	1040 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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224123_Specification.pdf	8913D6895F3E201D0565B0F1D3A7696F3127C42F0FE8F5A9789A2E981FEBB8CF4426455C9C7823113A6EDC5115D309136439BC41A396F3324EA32CF8E83A2B31
224123_POA.pdf	4A9300CCF4F967F3DE57B0E35AF40D8EA927D87983F358B98C098A09E125C2A9FB1007529AEC5D40BB0651DABF1B75FDA1C37251A06F270A386BF477ABD301E7

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

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Alexandria, VA 22313 - 1450
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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	06/24/2022 11:27:01 PM ET	224123/411598-06419

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PATENT CENTER #	60740671	AUTHORIZED BY	Steven French
CUSTOMER #	23363	FILING DATE	-
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Sang-Shin LEE

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 4792	E20226NN28382313	Si Vuong

PRE-AUTHORIZED ACCOUNT	PRE-AUTHORIZED CATEGORY
031728	37 CFR 1.16 (National application filing, search, and examination fees); 37 CFR 1.17 (Patent application and reexamination processing fees)

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1830	PROCESSING FEE, EXCEPT IN PROVISIONAL APPLICATIONS	140.00	1	140.00
1817	REQUEST FOR PRIORITIZED EXAMINATION	4200.00	1	4200.00
1111	UTILITY PATENT APPL. SEARCH FEE	700.00	1	700.00
1011	BASIC FILING FEE - UTILITY (PAPER FILING ALSO REQUIRES NON-ELECTRONIC FILING FEE UNDER 1.16(T))	320.00	1	320.00

1311	PATENT APPL. EXAMINATION FEE	800.00	1	800.00
1202	EACH CLAIM IN EXCESS OF 20	100.00	5	500.00
			TOTAL AMOUNT:	**$6,660.00**

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on June 24, 2022 at or before 11:59 p.m. Eastern Standard Time under the Rules of 37 CFR § 1.10.

/Si Vuong/
Si Vuong

Inventor	:	Sang-Shin Lee
Application No.	:	To Be Determined
Filed	:	June 24, 2022
Title	:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY
Grp./Div.	:	To Be Determined
Examiner	:	To Be Determined
Docket No.	:	224123

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS IN ACCORDANCE WITH 37 CFR 1.5

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
June 24, 2022

Commissioner:

Attached herewith is a General Power of Attorney for the above-identified patent application.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Steven J. French/
Steven J. French
Reg. No. 78,743
626/795-9900

JEJ/smv

118031108.1 06/24/22 7:55PM

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 23363

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box)

SAMSUNG DISPLAY CO., LTD.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Dong-Ho Lee	Date (Optional)	
Name	Dong-Ho Lee		
Title	Group Leader, IP Prosecution Group		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/01 (06-12)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/872,018 filed on April 26, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Sang-Shin Lee Date (Optional): 2020.08.27

Signature: Sang-Shin Lee

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/808,982	06/24/2022	2611	2320	224123/411598-06419	25	2

CONFIRMATION NO. 4376

23363
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

FILING RECEIPT

OC000000134885360

Date Mailed: 07/01/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Sang-Shin LEE, Yongin-si, KOREA, REPUBLIC OF;

Applicant(s)

SAMSUNG DISPLAY CO., LTD., Yongin-si, KOREA, REPUBLIC OF;

Power of Attorney: The patent practitioners associated with Customer Number 23363

Domestic Priority data as claimed by applicant

This application is a CON of 17/005,753 08/28/2020
which is a CON of 13/872,018 04/26/2013 PAT 10832616
which is a CIP of 13/614,197 09/13/2012 PAT 9818803

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
REPUBLIC OF KOREA 10-2012-0022967 03/06/2012 Access Code Provided
REPUBLIC OF KOREA 10-2013-0044993 04/23/2013 Access Code Provided

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 06/30/2022
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/808,982**
Projected Publication Date: 10/06/2022
Non-Publication Request: No
Early Publication Request: No
Title

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Preliminary Class

345

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: Yes

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

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technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/808,982

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	25 minus 20 =	* 5			OR	x 100 =	500
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2320

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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Document details: Country/Office: KR
Filing date: 23 Apr 2013 (23.04.2013)
Application number: 10-2013-0044993

Date of availability of document: 02 May 2013 (02.05.2013)

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Date of issue of this certificate: 05 Jul 2022 (05.07.2022)

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KOREAN INTELLECTUAL PROPERTY OFFICE

별첨 사본은 아래 출원의 원본과 동일함을 증명함.

This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office.

출 원 번 호 : 10-2013-0044993
Application Number

출 원 년 월 일 : 2013년 04월 23일
Filing Date Apr. 23, 2013

출 원 인 : 삼성디스플레이 주식회사
Applicant(s) Samsung Display Co., Ltd.

2022년 07월 01일

특 허 청
COMMISSIONER

제출 일자 : 2013-04-23

【서지사항】

【서류명】 특허출원서

【참조번호】 1667

【출원구분】 특허출원

【출원인】

【명칭】 삼성디스플레이 주식회사

【특허고객번호】 1-2012-016455-2

【대리인】

【명칭】 팬코리아특허법인

【대리인번호】 9-2007-100081-9

【지정된변리사】 김동준, 김재만

【포괄위임등록번호】 2012-029467-3

【발명의 국문명칭】 유기 발광 표시 장치의 화소 배열 구조

【발명의 영문명칭】 PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

【발명자】

【성명】 이상신

【성명의 영문표기】 LEE, SANG-SHIN

【주민등록번호】 770602-1XXXXXX

【우편번호】 445-738

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【취지】 위와 같이 특허청장에게 제출합니다.

대리인 팬코리아특허법인 (서명 또는 인)

【수수료】

【출원료】	0	면	38,000 원
【가산출원료】	16	면	0 원
【우선권주장료】	1	건	18,000 원
【심사청구료】	0	항	0 원
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【발명의 설명】

【발명의 명칭】

유기 발광 표시 장치의 화소 배열 구조{PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY}

【기술분야】

【0001】 본 발명은 유기 발광 표시 장치의 화소 배열 구조에 관한 것으로서, 보다 상세하게는 복수의 화소가 발광하여 이미지(image)를 표시하는 유기 발광 표시 장치의 화소 배열 구조에 관한 것이다.

【발명의 배경이 되는 기술】

【0002】 표시 장치는 이미지를 표시하는 장치로서, 최근 유기 발광 표시 장치(organic light emitting diode display)가 주목 받고 있다.

【0003】 유기 발광 표시 장치는 자체 발광 특성을 가지며, 액정 표시 장치(liquid crystal display device)와 달리 별도의 광원을 필요로 하지 않으므로 두께와 무게를 줄일 수 있다. 또한, 유기 발광 표시 장치는 낮은 소비 전력, 높은 휘도 및 높은 반응 속도 등의 고품위 특성을 나타낸다.

【0004】 일반적으로 유기 발광 표시 장치는 각각이 서로 다른 색의 빛을 발광하는 복수의 화소들을 포함하며, 이 복수의 화소들이 발광하여 이미지(image)를 표시한다.

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【0005】 여기서, 화소란 이미지를 표시하는 최소 단위를 의미하며, 이웃하는 화소 사이에는 각 화소를 구동하기 위한 게이트 라인, 데이터 라인, 구동 전원 라인 등의 전원 라인 및 각 화소의 면적 또는 형태 등을 정의하기 위한 화소 정의막 등의 절연층 등이 위치할 수 있다.

【0006】 종래의 유기 발광 표시 장치의 화소를 구성하는 유기 발광층은 파인 메탈마스크(fine metal mask, FMM) 등의 마스크를 이용하여 증착 형성하였는데, 화소의 개구율 확보를 위해 이웃하는 화소 간의 갭(gap)을 짧게 형성할 경우 증착 신뢰도가 저하되는 문제점이 있었으며, 증착 신뢰도 향상을 위해 화소 간의 갭을 멀게 형성할 경우 화소의 개구율이 저하되는 문제점이 있었다.

【발명의 내용】

【해결하고자 하는 과제】

【0007】 본 발명의 일 실시예는 상술한 문제점을 해결하기 위한 것으로서, 화소의 개구율이 향상되는 동시에 화소 간의 갭이 효율적으로 설정된 유기 발광 표시 장치의 화소 배열 구조를 제공하고자 한다.

【과제의 해결 수단】

【0008】 상술한 기술적 과제를 달성하기 위한 본 발명의 일 측면은 유기 발광 표시 장치의 화소 배열 구조에 있어서, 제1 화소, 상기 제1 화소와 이격되어 있으며, 상기 제1 화소의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형의 제1 꼭지점에 중심점이 위치하는 제2 화소, 및 상기 제2 화소와 이격되어 있으며,

상기 가상의 정사각형의 상기 제1 꼭지점과 이웃하는 제2 꼭지점에 중심점이 위치하는 제3 화소를 포함하며, 상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 다각형 형태를 가지는 유기 발광 표시 장치의 화소 배열 구조를 제공한다.

【0009】 상기 제2 화소는 복수개이며, 상기 복수개의 제2 화소는 상기 제1 화소를 사이에 두고 상호 이격되어 있을 수 있다.

【0010】 상기 제3 화소는 복수개이며, 상기 복수개의 제3 화소는 상기 제1 화소를 사이에 두고 상호 이격되어 있을 수 있다.

【0011】 상기 제2 화소는 복수개이며, 상기 제3 화소는 복수개이며, 상기 복수개의 제2 화소 및 상기 복수개의 제3 화소 각각은 상기 가상의 정사각형 상에서 상기 제1 화소를 둘러싸고 있을 수 있다.

【0012】 상기 제2 화소 및 상기 제3 화소는 상기 제1 화소 대비 큰 면적을 가질 수 있다.

【0013】 상기 제1 화소는 팔각형 형태를 가지며, 상기 제2 화소 및 상기 제3 화소 중 어느 하나는 육각형 형태를 가지며, 다른 하나는 사각형 형태를 가질 수 있다.

【0014】 상기 제1 화소는 복수개이며, 상기 복수개의 제1 화소 중 이웃하는 제1 화소 각각은 서로 대칭인 팔각형 형태를 가질 수 있다.

【0015】 상기 제2 화소는 상기 제3 화소 대비 큰 면적을 가질 수 있다.

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【0016】 상기 제1 화소와 상기 제2 화소 사이의 거리 및 상기 제1 화소와 상기 제3 화소 사이의 거리 각각은 동일한 제1 길이를 가질 수 있다.

【0017】 상기 제2 화소와 상기 제3 화소 사이의 거리는 제2 길이를 가지며, 이웃하는 상기 제1 화소 사이의 거리는 상기 제1 길이 및 상기 제2 길이 각각 대비 긴 제3 길이를 가질 수 있다.

【0018】 상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 서로 다른 색의 빛을 발광할 수 있다.

【0019】 상기 제1 화소는 녹색의 빛을 발광하며, 상기 제2 화소 및 상기 제3 화소 중 어느 하나는 청색의 빛을 발광하며 다른 하나는 적색의 빛을 발광할 수 있다.

【발명의 효과】

【0020】 상술한 본 발명의 과제 해결 수단의 일부 실시예 중 하나에 의하면, 화소의 개구율이 향상되는 동시에 화소 간의 갭이 효율적으로 설정된 유기 발광 표시 장치의 화소 배열 구조가 제공된다.

【도면의 간단한 설명】

【0021】 도 1은 본 발명의 일 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

【발명을 실시하기 위한 구체적인 내용】

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【0022】 이하, 첨부한 도면을 참고로 하여 본 발명의 여러 실시예들에 대하여 본 발명이 속하는 기술 분야에서 통상의 지식을 가진 자가 용이하게 실시할 수 있도록 상세히 설명한다. 본 발명은 여러 가지 상이한 형태로 구현될 수 있으며 여기에서 설명하는 실시예들에 한정되지 않는다.

【0023】 본 발명을 명확하게 설명하기 위해서 설명과 관계없는 부분은 생략하였으며, 명세서 전체를 통하여 동일 또는 유사한 구성요소에 대해서는 동일한 참조 부호를 붙이도록 한다.

【0024】 또한, 도면에서 나타난 각 구성의 크기 및 두께는 설명의 편의를 위해 임의로 나타내었으므로, 본 발명이 반드시 도시된 바에 한정되지 않는다.

【0025】 또한, 명세서 전체에서, 어떤 부분이 어떤 구성요소를 "포함" 한다고 할 때, 이는 특별히 반대되는 기재가 없는 한 다른 구성요소를 제외하는 것이 아니라 다른 구성요소를 더 포함할 수 있는 것을 의미한다.

【0026】 이하, 도 1을 참조하여 본 발명의 일 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 설명한다. 도 1은 유기 발광 표시 장치를 구성하는 화소들의 일 부분을 개략적으로 나타낸 도면이다.

【0027】 도 1은 본 발명의 일 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

【0028】 도 1에 도시된 바와 같이, 본 발명이 일 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 복수의 제1 화소(100), 복수의 제2 화소(200) 및 복

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수의 제3 화소(300)를 포함한다.

【0029】 여기서, 화소(pixel)란 이미지를 표시하는 최소 단위를 의미한다.

【0030】 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 사이에는 각 화소를 구동하기 위한 게이트 라인, 데이터 라인, 구동 전원 라인 등의 전원 라인 및 각 화소를 정의하기 위한 화소 정의막 등의 절연층 등이 위치할 수 있으며, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각에 대응하여 애노드 전극, 유기 발광층 및 캐소드 전극을 포함하는 유기 발광 소자(organic light emitting diode)가 위치할 수 있다. 상기한 구성들은 종래에 공지된 기술들이므로 설명의 편의상 설명하지 않으며, 각 화소의 형태는 전원 라인들, 화소 정의막 또는 애노드 전극 등에 의해 정의될 수 있으나, 이에 한정되지는 않는다.

【0031】 제1 화소(100)는 이웃한 제2 화소(200) 및 제3 화소 대비 작은 면적을 가지고 있으며, 다각형 형태를 가지고 있다. 제1 화소(100)는 다각형의 형태 중 팔각형의 형태를 가지고 있으나, 이에 한정되지 않고 삼각형, 사각형, 오각형, 육각형, 칠각형 등의 다각형 형태를 가질 수 있다. 제1 화소(100)는 복수개이며, 복수개의 제1 화소(100) 중 이웃하는 제1 화소(100) 각각은 서로 대칭인 팔각형 형태를 가지고 있다. 한편, 복수개의 제1 화소(100) 각각은 서로 동일한 팔각형 형태를 가지고 있을 수 있다. 복수개의 제1 화소(100) 각각은 상호 이격되어 가상의 제1 직선(VL1) 상에 배열되어 있다. 제1 화소(100)는 녹색의 빛을 발광하며, 녹색의 빛을 발광하는 유기 발광층을 포함할 수 있다. 한편, 제1 화소(100)는 청색, 적색 또는 백색 등의 다양한 색상의 빛을 발광하는 유기 발광층을 포함하여, 청색,

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적색 또는 백색의 빛을 발광할 수 있다.

【0032】 제1 화소(100)의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형(VS)의 제1 꼭지점(P1)에 제2 화소(200)가 위치하고 있으며, 가상의 정사각형(VS)의 제2 꼭지점(P2)에 제3 화소(300)가 위치하고 있다.

【0033】 제2 화소(200)는 제1 화소(100)와 이격되어 있으며, 가상의 정사각형(VS)의 제1 꼭지점(P1)에 중심점이 위치하고 있다. 제2 화소(200)는 이웃하는 제1 화소(100) 및 제3 화소(300) 각각 대비 더 큰 면적을 가지고 있으며, 다각형의 형태 중 육각형의 형태를 가지고 있다. 한편, 제2 화소(200)는 삼각형, 사각형, 오각형, 칠각형, 팔각형 등의 다각형 형태를 가질 수 있다. 제2 화소(200)는 복수개이며, 복수개의 제2 화소(200) 각각은 서로 동일한 육각형 형태를 가지고 있다. 복수개의 제2 화소(200)는 제1 화소(100)를 두고 상호 이격되어 있다. 제2 화소(200)는 청색의 빛을 발광하며, 청색의 빛을 발광하는 유기 발광층을 포함할 수 있다. 한편, 제2 화소(200)는 적색, 녹색 또는 백색 등의 다양한 색상의 빛을 발광하는 유기 발광층을 포함하여, 적색, 녹색 또는 백색의 빛을 발광할 수 있다.

【0034】 제3 화소(300)는 제1 화소(100) 및 제2 화소(200)와 이격되어 있으며, 가상의 정사각형(VS)의 제1 꼭지점(P1)과 이웃하는 제2 꼭지점(P2)에 중심점이 위치하고 있다. 제3 화소(300)는 이웃하는 제1 화소(100) 대비 더 큰 면적을 가지고 있는 동시에 이웃하는 제2 화소(200) 대비 더 작은 면적을 가지고 있다. 제3 화소(300)는 다각형의 형태 중 사각형의 형태를 가지고 있다. 한편, 제3 화소(300)는 삼각형, 오각형, 육각형, 칠각형, 팔각형 등의 다각형 형태를 가질 수 있

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다. 제3 화소(300)는 복수개이며, 복수개의 제3 화소(300) 각각은 서로 동일한 사각형의 형태를 가지고 있다. 복수개의 제3 화소(300)는 제1 화소(100)를 두고 상호 이격되어 있다. 제3 화소(300)는 적색의 빛을 발광하며, 적색의 빛을 발광하는 유기 발광층을 포함할 수 있다. 한편, 제3 화소(300)는 청색, 녹색 또는 백색 등의 다양한 색상의 빛을 발광하는 유기 발광층을 포함하여, 청색, 녹색 또는 백색의 빛을 발광할 수 있다.

【0035】 한편, 제2 화소(200) 및 제3 화소(300) 각각은 육각형 형태 및 사각형 형태를 가지나, 제2 화소(200) 및 제3 화소(300) 각각은 사각형 형태 및 육각형 형태 각각을 가질 수 있다. 즉, 제2 화소(200) 및 제3 화소(300) 중 어느 하나는 육각형 형태를 가지며, 다른 하나는 사각형 형태를 가질 수 있다.

【0036】 또한, 제1 화소(100), 제2 화소(200), 제3 화소(300) 각각은 녹색, 청색, 적색 각각의 빛을 발광하나, 제1 화소(100), 제2 화소(200), 제3 화소(300) 각각은 서로 다른 색의 빛을 발광하거나 서로 동일한 색의 빛을 발광할 수 있다. 구체적으로, 제1 화소(100)는 녹색의 빛을 발광하며, 제2 화소(200) 및 제3 화소(300) 중 어느 하나는 청색의 빛을 발광하며 다른 하나는 적색의 빛을 발광할 수 있다.

【0037】 복수개의 제3 화소(300) 및 복수개의 제2 화소(200) 각각은 가상의 제2 직선(VL2) 상에서 상호 교호적으로 배열되며, 이로 인해 제1 꼭지점(P1)에 중심점이 위치하는 복수개의 제2 화소(200) 및 제2 꼭지점(P2)에 중심점이 위치하는 복수개의 제3 화소(300) 각각은 가상의 정사각형(VS) 상에서 제1 화소(100)를 둘러

싸고 있다.

【0038】 이와 같이, 제1 화소(100)의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형(VS)의 제1 꼭지점(P1)에 제2 화소(200)의 중심점이 위치하고, 제2 꼭지점(P2)에 제3 화소(300)의 중심점이 위치함으로써, 제1 꼭지점(P1)에 중심점이 위치하는 복수개의 제2 화소(200) 및 제2 꼭지점(P2)에 중심점이 위치하는 복수개의 제3 화소(300) 각각이 가상의 정사각형(VS) 상에서 제1 화소(100)를 둘러싸고 있는 동시에, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각이 다각형 형태를 가지기 때문에, 제1 화소(100)와 제2 화소(200) 사이의 거리 및 제1 화소(100)와 제3 화소(300) 화소 사이의 거리 각각은 동일한 제1 길이(L1)를 가지며, 이웃하는 제2 화소(200)와 제3 화소(300) 사이의 거리는 제1 길이(L1)와는 다른 제2 길이(L2)를 가지며, 이웃하는 제1 화소(100) 사이의 거리는 제1 길이(L1) 및 제2 길이(L2) 각각 대비 긴 제3 길이(L3)를 가지게 된다.

【0039】 일례로, 제1 길이(L1)는 15um 내지 35um일 수 있고, 제2 길이(L2)는 20um 내지 45um일 수 있으며, 제3 길이(L3)는 25um 내지 65um일 수 있다.

【0040】 이로 인해, 제1 화소(100)와 제2 화소(200)의 사이 및 제1 화소(100)와 제3 화소(300) 각각의 사이에는 제1 길이(L1)의 갭(gap)이 형성되는 동시에, 이웃하는 제1 화소(100) 사이에는 제1 길이(L1) 대비 긴 제3 길이(L3)의 갭이 형성됨으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각에 포함된 녹색의 유기 발광층, 청색의 유기 발광층 및 적색의 유기 발광층 각각을 형성하는 파인메탈마스크를 이용한 증착 공정 시 증착 신뢰도가 향상된다.

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【0041】 또한, 복수의 제2 화소(200) 및 복수의 제3 화소(300) 각각이 제1 화소(100)를 가상의 정사각형(VS) 상에서 둘러싸도록 배열됨으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 개구율을 향상시킬 수 있다. 이는 전체적인 유기 발광 표시 장치의 제조 시간 및 제조 비용을 절감하는 동시에 유기 발광 표시 장치가 표시하는 이미지의 품질을 향상시키는 요인으로서 작용된다.

【0042】 또한, 본 발명의 일 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 중 다른 화소 대비 수명이 짧은 청색의 빛을 발광하는 제2 화소(200)가 제1 화소(100) 및 제3 화소(300) 각각 대비 큰 면적을 가짐으로써, 전체적인 유기 발광 표시 장치의 수명이 저하되는 것이 억제된다. 즉, 수명이 향상된 유기 발광 표시 장치의 화소 배열 구조가 제공된다.

【0043】 상술한 바와 같이, 본 발명의 일 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각이 단순히 팔각형, 육각형 및 사각형 각각 등의 다각형의 형태를 가지는 것이 아니라, 유기 발광 표시 장치의 고유의 제조 특성인 유기 발광층의 증착 공정을 고려하여, 파인메탈마스크를 이용한 증착 공정 시 유기 발광층의 증착 신뢰도를 향상시키는 동시에 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 개구율을 향상시키기 위해, 가상의 정사각형(VS)의 중심점에 제1 화소(100)의 중심점을 위치시키고, 제1 꼭지점(P1)에 제2 화소(200)의 중심점을 위치시키고, 제2 꼭지점(P2)에 제3 화소(300)의 중심점을 위치시키는 것이다.

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【0044】 즉, 유기 발광층의 증착 신뢰도를 향상시키는 동시에 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 개구율을 향상시키는 팔각형의 제1 화소(100), 육각형의 제2 화소(200) 및 사각형의 제3 화소(300)를 포함하는 유기 발광 표시 장치의 화소 배열 구조가 제공된다.

【0045】 본 발명을 앞서 기재한 바에 따라 바람직한 실시예를 통해 설명하였지만, 본 발명은 이에 한정되지 않으며 다음에 기재하는 특허청구범위의 개념과 범위를 벗어나지 않는 한, 다양한 수정 및 변형이 가능하다는 것을 본 발명이 속하는 기술 분야에 종사하는 자들은 쉽게 이해할 것이다.

【부호의 설명】

【0046】 제1 화소(100), 제2 화소(200), 제3 화소(300)

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【특허청구범위】

【청구항 1】

유기 발광 표시 장치의 화소 배열 구조에 있어서,

제1 화소;

상기 제1 화소와 이격되어 있으며, 상기 제1 화소의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형의 제1 꼭지점에 중심점이 위치하는 제2 화소; 및

상기 제2 화소와 이격되어 있으며, 상기 가상의 정사각형의 상기 제1 꼭지점과 이웃하는 제2 꼭지점에 중심점이 위치하는 제3 화소

를 포함하며,

상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 다각형 형태를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 2】

제1항에서,

상기 제2 화소는 복수개이며,

상기 복수개의 제2 화소는 상기 제1 화소를 사이에 두고 상호 이격되어 있는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 3】

제1항에서,

상기 제3 화소는 복수개이며,

상기 복수개의 제3 화소는 상기 제1 화소를 사이에 두고 상호 이격되어 있는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 4】

제1항에서,

상기 제2 화소는 복수개이며,

상기 제3 화소는 복수개이며,

상기 복수개의 제2 화소 및 상기 복수개의 제3 화소 각각은 상기 가상의 정사각형 상에서 상기 제1 화소를 둘러싸는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 5】

제4항에서,

상기 제2 화소 및 상기 제3 화소는 상기 제1 화소 대비 큰 면적을 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 6】

제5항에서,

상기 제1 화소는 팔각형 형태를 가지며,

상기 제2 화소 및 상기 제3 화소 중 어느 하나는 육각형 형태를 가지며, 다른 하나는 사각형 형태를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 7】

제6항에서,

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상기 제1 화소는 복수개이며,

상기 복수개의 제1 화소 중 이웃하는 제1 화소 각각은 서로 대칭인 팔각형 형태를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 8】

제7항에서,

상기 제2 화소는 상기 제3 화소 대비 큰 면적을 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 9】

제8항에서,

상기 제1 화소와 상기 제2 화소 사이의 거리 및 상기 제1 화소와 상기 제3 화소 사이의 거리 각각은 동일한 제1 길이를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 10】

제9항에서,

상기 제2 화소와 상기 제3 화소 사이의 거리는 제2 길이를 가지며,

이웃하는 상기 제1 화소 사이의 거리는 상기 제1 길이 및 상기 제2 길이 각각 대비 긴 제3 길이를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 11】

제1항 내지 제10항 중 어느 한 항에서,

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상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 서로 다른 색의 빛을 발광하는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 12】

제11항에서,

상기 제1 화소는 녹색의 빛을 발광하며,

상기 제2 화소 및 상기 제3 화소 중 어느 하나는 청색의 빛을 발광하며 다른 하나는 적색의 빛을 발광하는 유기 발광 표시 장치의 화소 배열 구조.

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제출 일자 : 2013-04-23

【요약서】

【요약】

유기 발광 표시 장치의 화소 배열 구조는 제1 화소, 상기 제1 화소와 이격되어 있으며, 상기 제1 화소의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형의 제1 꼭지점에 중심점이 위치하는 제2 화소, 및 상기 제2 화소와 이격되어 있으며, 상기 가상의 정사각형의 상기 제1 꼭지점과 이웃하는 제2 꼭지점에 중심점이 위치하는 제3 화소를 포함하며, 상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 다각형 형태를 가진다.

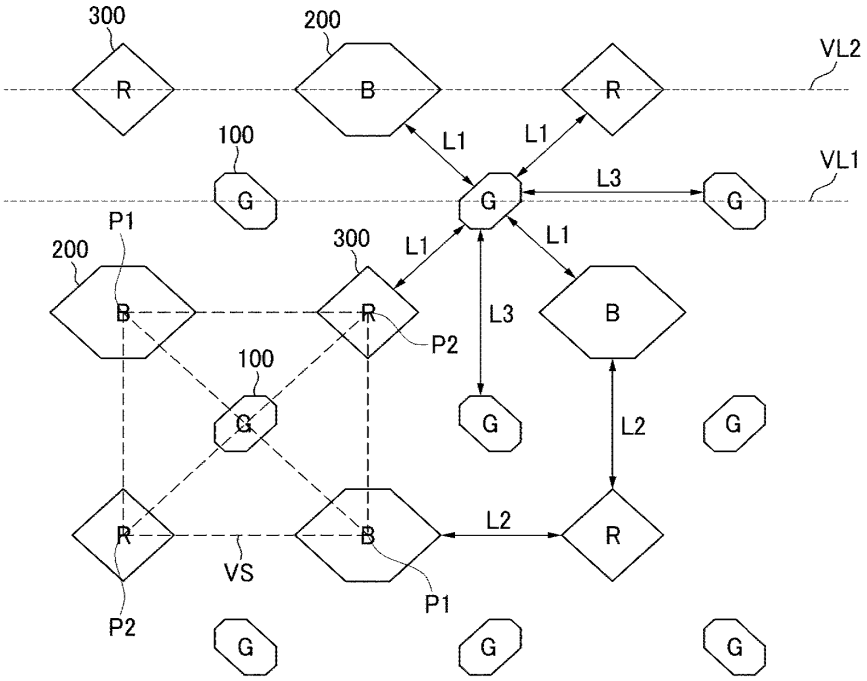
【대표도】

도 1

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【도면】

【도 1】



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【지정된변리사】 김재만

【포괄위임등록번호】 2008-081420-6

【발명의 국문명칭】 유기 발광 표시 장치의 화소 배열 구조

【발명의 영문명칭】 PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DISPLAY DEVICE

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【취지】 위와 같이 특허청장에게 제출합니다.

대리인 팬코리아특허법인 (서명 또는 인)

【수수료】

【출원료】	0	면	38,000 원
【가산출원료】	23	면	0 원
【우선권주장료】	0	건	0 원
【심사청구료】	14	항	690,000 원
【합계】	728,000 원		

【수수료 자동납부번호】 064-094949-04-013

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제출 일자 : 2012-03-06

【발명의 설명】

【발명의 명칭】

유기 발광 표시 장치의 화소 배열 구조{PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DISPLAY DEVICE}

【기술분야】

【0001】 본 발명은 유기 발광 표시 장치의 화소 배열 구조에 관한 것으로서, 보다 상세하게는 복수의 화소가 발광하여 이미지(image)를 표시하는 유기 발광 표시 장치의 화소 배열 구조에 관한 것이다.

【발명의 배경이 되는 기술】

【0002】 표시 장치는 이미지를 표시하는 장치로서, 최근 유기 발광 표시 장치(organic light emitting diode display)가 주목 받고 있다.

【0003】 유기 발광 표시 장치는 자체 발광 특성을 가지며, 액정 표시 장치(liquid crystal display device)와 달리 별도의 광원을 필요로 하지 않으므로 두께와 무게를 줄일 수 있다. 또한, 유기 발광 표시 장치는 낮은 소비 전력, 높은 휘도 및 높은 반응 속도 등의 고품위 특성을 나타낸다.

【0004】 일반적으로 유기 발광 표시 장치는 각각이 서로 다른 색의 빛을 발광하는 복수의 화소들을 포함하며, 이 복수의 화소들이 발광하여 이미지(image)를 표시한다.

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【0005】 여기서, 화소란 이미지를 표시하는 최소 단위를 의미하며, 이웃하는 화소 사이에는 각 화소를 구동하기 위한 게이트 라인, 데이터 라인, 구동 전원 라인 등의 전원 라인 및 각 화소의 면적 또는 형태 등을 정의하기 위한 화소 정의막 등의 절연층 등이 위치할 수 있다.

【0006】 종래의 유기 발광 표시 장치의 화소를 구성하는 유기 발광층은 파인 메탈마스크(fine metal mask, FMM) 등의 마스크를 이용하여 증착 형성하였는데, 화소의 개구율 확보를 위해 이웃하는 화소 간의 갭(gap)을 짧게 형성할 경우 증착 신뢰도가 저하되는 문제점이 있었으며, 증착 신뢰도 향상을 위해 화소 간의 갭을 멀게 형성할 경우 화소의 개구율이 저하되는 문제점이 있었다.

【발명의 내용】

【해결하고자 하는 과제】

【0007】 본 발명의 일 실시예는 상술한 문제점을 해결하기 위한 것으로서, 화소의 개구율이 향상되는 동시에 화소 간의 갭이 효율적으로 설정된 유기 발광 표시 장치의 화소 배열 구조를 제공하고자 한다.

【과제의 해결 수단】

【0008】 상술한 기술적 과제를 달성하기 위한 본 발명의 일 측면은 유기 발광 표시 장치의 화소 배열 구조에 있어서, 제1 화소, 상기 제1 화소와 이격되어 있으며, 상기 제1 화소의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형의 제1 꼭지점에 중심점이 위치하는 제2 화소, 및 상기 제2 화소와 이격되어 있으며,

상기 가상의 정사각형의 상기 제1 꼭지점과 이웃하는 제2 꼭지점에 중심점이 위치하는 제3 화소를 포함하는 유기 발광 표시 장치의 화소 배열 구조를 제공한다.

【0009】 상기 제2 화소는 복수개이며, 상기 복수개의 제2 화소는 상기 제1 화소를 사이에 두고 상호 이격되어 있을 수 있다.

【0010】 상기 제3 화소는 복수개이며, 상기 복수개의 제3 화소는 상기 제1 화소를 사이에 두고 상호 이격되어 있을 수 있다.

【0011】 상기 복수개의 제2 화소 및 상기 복수개의 제3 화소 각각은 상기 제1 화소를 둘러싸도록 가상의 직선 상에서 상호 교호적으로 배열될 수 있다.

【0012】 상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 다각형 형태를 가지며, 상기 제2 화소 및 상기 제3 화소는 상기 제1 화소 대비 큰 면적을 가질 수 있다.

【0013】 상기 제1 화소는 사각형 형태를 가지며, 상기 제2 화소 및 상기 제3 화소 각각은 팔각형 형태를 가질 수 있다.

【0014】 상기 제1 화소는 복수개이며, 상기 복수개의 제1 화소 각각은 동일한 사각형 형태를 가질 수 있다.

【0015】 상기 제2 화소와 상기 제3 화소 각각은 서로 동일한 면적을 가지며, 상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각 사이의 거리는 동일한 제1 길이를 가지며, 이웃하는 상기 제1 화소 간의 거리는 상기 제1 길이 대비 긴 제2 길이를 가질 수 있다.

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【0016】 상기 제2 화소는 상기 제3 화소 대비 큰 면적을 가지며, 상기 제2 화소와 상기 제3 화소 사이의 거리는 제3 길이를 가지며, 상기 제1 화소와 상기 제2 화소 사이의 거리 및 상기 제1 화소와 상기 제3 화소 사이의 거리 각각은 동일한 제4 길이를 가지며, 이웃하는 상기 제1 화소 간의 거리는 상기 제3 길이 및 상기 제4 길이 대비 긴 제5 길이를 가질 수 있다.

【0017】 상기 제1 화소는 복수개이며, 상기 복수개의 제1 화소 중 이웃하는 제1 화소 각각은 서로 대칭인 사각형 형태를 가질 수 있다.

【0018】 상기 제2 화소는 상기 제3 화소 대비 큰 면적을 가질 수 있다.

【0019】 상기 제3 화소는 상기 제2 화소 대비 큰 면적을 가질 수 있다.

【0020】 상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 서로 다른 색의 빛을 발광할 수 있다.

【0021】 상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 녹색, 청색 및 적색 각각의 빛을 발광할 수 있다.

【발명의 효과】

【0022】 상술한 본 발명의 과제 해결 수단의 일부 실시예 중 하나에 의하면, 화소의 개구율이 향상되는 동시에 화소 간의 갭이 효율적으로 설정된 유기 발광 표시 장치의 화소 배열 구조가 제공된다.

【도면의 간단한 설명】

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【0023】도 1은 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

도 2는 본 발명의 제2 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

도 3은 본 발명의 제3 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

도 4는 본 발명의 제4 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

【발명을 실시하기 위한 구체적인 내용】

【0024】이하, 첨부한 도면을 참고로 하여 본 발명의 여러 실시예들에 대하여 본 발명이 속하는 기술 분야에서 통상의 지식을 가진 자가 용이하게 실시할 수 있도록 상세히 설명한다. 본 발명은 여러 가지 상이한 형태로 구현될 수 있으며 여기에서 설명하는 실시예들에 한정되지 않는다.

【0025】본 발명을 명확하게 설명하기 위해서 설명과 관계없는 부분은 생략하였으며, 명세서 전체를 통하여 동일 또는 유사한 구성요소에 대해서는 동일한 참조 부호를 붙이도록 한다.

【0026】또한, 여러 실시예들에 있어서, 동일한 구성을 가지는 구성요소에 대해서는 동일한 부호를 사용하여 대표적으로 제1 실시예에서 설명하고, 그 외의 실시예에서는 제1 실시예와 다른 구성에 대해서만 설명하기로 한다.

【0027】 또한, 도면에서 나타난 각 구성의 크기 및 두께는 설명의 편의를 위해 임의로 나타내었으므로, 본 발명이 반드시 도시된 바에 한정되지 않는다.

【0028】 또한, 명세서 전체에서, 어떤 부분이 어떤 구성요소를 "포함" 한다고 할 때, 이는 특별히 반대되는 기재가 없는 한 다른 구성요소를 제외하는 것이 아니라 다른 구성요소를 더 포함할 수 있는 것을 의미한다.

【0029】 이하, 도 1을 참조하여 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 설명한다. 도 1은 유기 발광 표시 장치를 구성하는 화소들의 일 부분을 개략적으로 나타낸 도면이다.

【0030】 도 1은 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

【0031】 도 1에 도시된 바와 같이, 본 발명이 제1 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 복수의 제1 화소(100), 복수의 제2 화소(200) 및 복수의 제3 화소(300)를 포함한다.

【0032】 여기서, 화소(pixel)란 이미지를 표시하는 최소 단위를 의미한다.

【0033】 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 사이에는 각 화소를 구동하기 위한 게이트 라인, 데이터 라인, 구동 전원 라인 등의 전원 라인 및 각 화소를 정의하기 위한 화소 정의막 등의 절연층 등이 위치할 수 있으며, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각에 대응하여 애노드 전극, 유기 발광층 및 캐소드 전극을 포함하는 유기 발광 소자(organic light emitting diode)가

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위치할 수 있다. 상기한 구성들은 종래에 공지된 기술들이므로 설명의 편의상 설명하지 않으며, 각 화소의 형태는 전원 라인들, 화소 정의막 또는 애노드 전극 등에 의해 정의될 수 있으나, 이에 한정되지는 않는다.

【0034】 제1 화소(100)는 이웃한 제2 화소(200) 및 제3 화소 대비 작은 면적을 가지고 있으며, 다각형의 형태 중 사각형의 형태를 가지고 있다. 제1 화소(100)는 복수개이며, 복수개의 제1 화소(100)는 서로 동일한 사각형 형태를 가지고 있다. 복수개의 제1 화소(100)는 상호 이격되어 가상의 제1 직선(VL1) 상에 배열되어 있다. 제1 화소(100)는 녹색의 빛을 발광하며, 녹색의 빛을 발광하는 유기 발광층을 포함할 수 있다.

【0035】 제1 화소(100)의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형(VS)의 제1 꼭지점(P1)에 제2 화소(200)가 위치하고 있으며, 가상의 정사각형(VS)의 제2 꼭지점(P2)에 제3 화소(300)가 위치하고 있다.

【0036】 제2 화소(200)는 제1 화소(100)와 이격되어 있으며, 가상의 정사각형(VS)의 제1 꼭지점(P1)에 중심점이 위치하고 있다. 제2 화소(200)는 이웃하는 제1 화소(100) 대비 더 큰 면적을 가지고 있으며, 다각형의 형태 중 팔각형의 형태를 가지고 있다. 제2 화소(200)는 복수개이며, 복수개의 제2 화소(200)는 서로 동일한 팔각형의 형태를 가지고 있다. 복수개의 제2 화소(200)는 제1 화소(100)를 두고 상호 이격되어 있다. 제2 화소(200)는 청색의 빛을 발광하며, 청색의 빛을 발광하는 유기 발광층을 포함할 수 있다.

【0037】 제3 화소(300)는 제1 화소(100) 및 제2 화소(200)와 이격되어 있으

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며, 가상의 정사각형(VS)의 제1 꼭지점(P1)과 이웃하는 제2 꼭지점(P2)에 중심점이 위치하고 있다. 제3 화소(300)는 이웃하는 제1 화소(100) 대비 더 큰 면적을 가지고 있는 동시에 제2 화소(200)와 동일한 면적을 가지고 있으며, 다각형의 형태 중 팔각형의 형태를 가지고 있다. 제3 화소(300)는 복수개이며, 복수개의 제3 화소(300)는 서로 동일한 팔각형의 형태를 가지고 있다. 복수개의 제3 화소(300)는 제1 화소(100)를 두고 상호 이격되어 있다. 제3 화소(300)는 적색의 빛을 발광하며, 적색의 빛을 발광하는 유기 발광층을 포함할 수 있다.

【0038】 복수개의 제3 화소(300) 및 복수개의 제2 화소(200) 각각은 가상의 제2 직선(VL2) 상에서 상호 교호적으로 배열되며, 이로 인해 제1 꼭지점(P1)에 중심점이 위치하는 복수개의 제2 화소(200) 및 제2 꼭지점(P2)에 중심점이 위치하는 복수개의 제3 화소(300) 각각은 제1 화소(100)를 둘러싸고 있다.

【0039】 이와 같이, 제1 화소(100)의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형(VS)의 제1 꼭지점(P1)에 제2 화소(200)의 중심점이 위치하고, 제2 꼭지점(P2)에 제3 화소(300)의 중심점이 위치하며, 제2 화소(200) 및 제3 화소(300)가 동일한 면적을 가짐으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각 사이의 거리는 동일한 제1 길이(L1)를 가지며, 이웃하는 제1 화소(100) 간의 거리는 제1 길이(L1) 대비 긴 제2 길이(L2)를 가지게 된다.

【0040】 이로 인해, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 사이에는 제1 길이(L1)의 갭(gap)이 형성되는 동시에, 이웃하는 제1 화소(100) 사이에는 제1 길이(L1) 대비 긴 제2 길이(L2)의 갭이 형성됨으로써, 제1 화소(100),

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제2 화소(200) 및 제3 화소(300) 각각에 포함된 녹색의 유기 발광층, 청색의 유기 발광층 및 적색의 유기 발광층 각각을 형성하는 파인메탈마스크를 이용한 증착 공정 시 증착 신뢰도가 향상된다. 또한, 복수의 제2 화소(200) 및 복수의 제3 화소(300) 각각이 제1 화소(100)를 둘러싸도록 배열됨으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 개구율을 향상시킬 수 있다. 이는 전체적인 유기 발광 표시 장치의 제조 시간 및 제조 비용을 절감하는 동시에 유기 발광 표시 장치가 표시하는 이미지의 품질을 향상시키는 요인으로서 작용된다.

【0041】 상술한 바와 같이, 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각이 단순히 다각형의 형태를 가지는 것이 아니라, 유기 발광 표시 장치의 고유의 제조 특성인 유기 발광층의 증착 공정을 고려하여, 파인메탈마스크를 이용한 증착 공정시 유기 발광층의 증착 신뢰도를 향상시키는 동시에 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 개구율을 향상시키기 위해, 가상의 정사각형(VS)의 중심점에 제1 화소(100)의 중심점을 위치시키고, 제1 꼭지점(P1)에 제2 화소(200)의 중심점을 위치시키고, 제2 꼭지점(P2)에 제3 화소(300)의 중심점을 위치시키는 것이다.

【0042】 한편, 본 발명의 제1 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조에서 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각은 녹색, 청색 및 적색 각각의 색을 발광하나, 본 발명의 다른 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조에서는 이에 한정되지 않고, 제1 화소, 제2 화소 및 제3 화소 각각이 서로 다른 색의 빛을 발광할 수 있다. 일례로, 제2 화소 및 제3 화소 중

하나 이상의 화소가 백색 등의 빛을 발광할 수 있다.

【0043】 이하, 도 2를 참조하여 본 발명의 제2 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조에 대하여 설명한다.

【0044】 이하, 제1 실시예와 구별되는 특징적인 부분만 발췌하여 설명하며, 설명이 생략된 부분은 제1 실시예에 따른다. 그리고, 본 발명의 제2 실시예에서는 설명의 편의를 위하여 동일한 구성요소에 대하여는 본 발명의 제1 실시예와 동일한 참조번호를 사용하여 설명한다.

【0045】 도 2는 본 발명의 제2 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

【0046】 도 2에 도시된 바와 같이, 본 발명이 제2 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 복수의 제1 화소(100), 복수의 제2 화소(200) 및 복수의 제3 화소(300)를 포함한다.

【0047】 복수개의 제1 화소(100)는 서로 동일한 사각형 형태를 가지고 있다.

【0048】 제2 화소(200) 및 제3 화소 각각은 서로 다른 면적을 가지고 있으며, 제2 화소(200)가 제3 화소(300) 대비 큰 면적을 가지고 있다.

【0049】 이와 같이, 제1 화소(100)의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형(VS)의 제1 꼭지점(P1)에 제2 화소(200)의 중심점이 위치하고, 제2 꼭지점(P2)에 제3 화소(300)의 중심점이 위치하며, 제2 화소(200)가 제3 화소(300) 대비 큰 면적을 가짐으로써, 제2 화소(200)와 제3 화소(300) 사이의 거리는 제3 길

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이(L3)를 가지고, 제1 화소(100)와 제2 화소(200) 사이의 거리 및 제1 화소(100)와 제3 화소(300) 사이의 거리 각각은 동일한 제4 길이(L4)를 가지며, 이웃하는 제1 화소(100) 간의 거리는 제2 길이(L2) 및 제4 길이(L4) 대비 긴 제5 길이(L5)를 가진다.

【0050】 이로 인해, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 사이에는 제3 길이(L3) 또는 제4 길이(L4)의 갭(gap)이 형성되는 동시에, 이웃하는 제1 화소(100) 사이에는 제3 길이(L3) 및 제4 길이(L4) 대비 긴 제5 길이(L5)의 갭이 형성됨으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각에 포함된 녹색의 유기 발광층, 청색의 유기 발광층 및 적색의 유기 발광층 각각을 형성하는 파인메탈마스크를 이용한 증착 공정 시 증착 신뢰도가 향상된다. 또한, 복수의 제2 화소(200) 및 복수의 제3 화소(300) 각각이 제1 화소(100)를 둘러싸도록 배열됨으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 개구율을 향상시킬 수 있다. 이는 전체적인 유기 발광 표시 장치의 제조 시간 및 제조 비용을 절감하는 동시에 유기 발광 표시 장치가 표시하는 이미지의 품질을 향상시키는 요인으로서 작용된다.

【0051】 또한, 본 발명의 제2 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 중 다른 화소 대비 수명이 짧은 청색의 빛을 발광하는 제2 화소(200)가 제3 화소(300) 대비 큰 면적을 가짐으로써, 전체적인 유기 발광 표시 장치의 수명이 저하되는 것이 억제된다. 즉, 수명이 향상된 유기 발광 표시 장치의 화소 배열 구조가 제공된다.

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【0052】 이하, 도 3을 참조하여 본 발명의 제3 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조에 대하여 설명한다.

【0053】 이하, 제1 실시예와 구별되는 특징적인 부분만 발췌하여 설명하며, 설명이 생략된 부분은 제1 실시예에 따른다. 그리고, 본 발명의 제3 실시예에서는 설명의 편의를 위하여 동일한 구성요소에 대하여는 본 발명의 제1 실시예와 동일한 참조번호를 사용하여 설명한다.

【0054】 도 3은 본 발명의 제3 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조를 나타낸 도면이다.

【0055】 도 3에 도시된 바와 같이, 본 발명이 제3 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 복수의 제1 화소(100), 복수의 제2 화소(200) 및 복수의 제3 화소(300)를 포함한다.

【0056】 복수개의 제1 화소(100) 중 이웃하는 제1 화소(100) 각각은 서로 대칭인 사각형 형태를 가지고 있다.

【0057】 제2 화소(200) 및 제3 화소 각각은 서로 다른 면적을 가지고 있으며, 제2 화소(200)가 제3 화소(300) 대비 큰 면적을 가지고 있다.

【0058】 이와 같이, 제1 화소(100)의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형(VS)의 제1 꼭지점(P1)에 제2 화소(200)의 중심점이 위치하고, 제2 꼭지점(P2)에 제3 화소(300)의 중심점이 위치하며, 이웃하는 제1 화소(100) 각각이 서로 대칭인 사각형 형태를 가지는 동시에 제2 화소(200)가 제3 화소(300) 대비 큰

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면적을 가짐으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각에 포함된 녹색의 유기 발광층, 청색의 유기 발광층 및 적색의 유기 발광층 각각을 형성하는 파인메탈마스크를 이용한 증착 공정 시 증착 신뢰도가 향상된다. 또한, 복수의 제2 화소(200) 및 복수의 제3 화소(300) 각각이 제1 화소(100)를 둘러싸도록 배열됨으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 개구율을 향상시킬 수 있다. 이는 전체적인 유기 발광 표시 장치의 제조 시간 및 제조 비용을 절감하는 동시에 유기 발광 표시 장치가 표시하는 이미지의 품질을 향상시키는 요인으로서 작용된다.

【0059】 또한, 본 발명의 제3 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 중 다른 화소 대비 수명이 짧은 청색의 빛을 발광하는 제2 화소(200)가 제3 화소(300) 대비 큰 면적을 가짐으로써, 전체적인 유기 발광 표시 장치의 수명이 저하되는 것이 억제된다. 즉, 수명이 향상된 유기 발광 표시 장치의 화소 배열 구조가 제공된다.

【0060】 이하, 도 4를 참조하여 본 발명의 제4 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조에 대하여 설명한다.

【0061】 이하, 제1 실시예와 구별되는 특징적인 부분만 발췌하여 설명하며, 설명이 생략된 부분은 제1 실시예에 따른다. 그리고, 본 발명의 제4 실시예에서는 설명의 편의를 위하여 동일한 구성요소에 대하여는 본 발명의 제1 실시예와 동일한 참조번호를 사용하여 설명한다.

【0062】 도 4는 본 발명의 제4 실시예에 따른 유기 발광 표시 장치의 화소

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배열 구조를 나타낸 도면이다.

【0063】 도 4에 도시된 바와 같이, 본 발명이 제4 실시예에 따른 유기 발광 표시 장치의 화소 배열 구조는 복수의 제1 화소(100), 복수의 제2 화소(200) 및 복수의 제3 화소(300)를 포함한다.

【0064】 복수개의 제1 화소(100) 중 이웃하는 제1 화소(100) 각각은 서로 대칭인 사각형 형태를 가지고 있다.

【0065】 제2 화소(200) 및 제3 화소 각각은 서로 다른 면적을 가지고 있으며, 제3 화소(300)가 제2 화소(200) 대비 큰 면적을 가지고 있다.

【0066】 이와 같이, 제1 화소(100)의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형(VS)의 제1 꼭지점(P1)에 제2 화소(200)의 중심점이 위치하고, 제2 꼭지점(P2)에 제3 화소(300)의 중심점이 위치하며, 이웃하는 제1 화소(100) 각각이 서로 대칭인 사각형 형태를 가지는 동시에 제3 화소(300)가 제2 화소(200) 대비 큰 면적을 가짐으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각에 포함된 녹색의 유기 발광층, 청색의 유기 발광층 및 적색의 유기 발광층 각각을 형성하는 파인메탈마스크를 이용한 증착 공정 시 증착 신뢰도가 향상된다. 또한, 복수의 제2 화소(200) 및 복수의 제3 화소(300) 각각이 제1 화소(100)를 둘러싸도록 배열됨으로써, 제1 화소(100), 제2 화소(200) 및 제3 화소(300) 각각의 개구율을 향상시킬 수 있다. 이는 전체적인 유기 발광 표시 장치의 제조 시간 및 제조 비용을 절감하는 동시에 유기 발광 표시 장치가 표시하는 이미지의 품질을 향상시키는 요인으로서 작용된다.

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【0067】본 발명을 앞서 기재한 바에 따라 바람직한 실시예를 통해 설명하였지만, 본 발명은 이에 한정되지 않으며 다음에 기재하는 특허청구범위의 개념과 범위를 벗어나지 않는 한, 다양한 수정 및 변형이 가능하다는 것을 본 발명이 속하는 기술 분야에 종사하는 자들은 쉽게 이해할 것이다.

【부호의 설명】

【0068】제1 화소(100), 제2 화소(200), 제3 화소(300)

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【특허청구범위】

【청구항 1】

유기 발광 표시 장치의 화소 배열 구조에 있어서,

제1 화소;

상기 제1 화소와 이격되어 있으며, 상기 제1 화소의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형의 제1 꼭지점에 중심점이 위치하는 제2 화소; 및

상기 제2 화소와 이격되어 있으며, 상기 가상의 정사각형의 상기 제1 꼭지점과 이웃하는 제2 꼭지점에 중심점이 위치하는 제3 화소

를 포함하는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 2】

제1항에서,

상기 제2 화소는 복수개이며,

상기 복수개의 제2 화소는 상기 제1 화소를 사이에 두고 상호 이격되어 있는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 3】

제2항에서,

상기 제3 화소는 복수개이며,

상기 복수개의 제3 화소는 상기 제1 화소를 사이에 두고 상호 이격되어 있는 유기 발광 표시 장치의 화소 배열 구조.

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【청구항 4】

제3항에서,

상기 복수개의 제2 화소 및 상기 복수개의 제3 화소 각각은 상기 제1 화소를 둘러싸도록 가상의 직선 상에서 상호 교호적으로 배열되는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 5】

제4항에서,

상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 다각형 형태를 가지며,

상기 제2 화소 및 상기 제3 화소는 상기 제1 화소 대비 큰 면적을 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 6】

제5항에서,

상기 제1 화소는 사각형 형태를 가지며,

상기 제2 화소 및 상기 제3 화소 각각은 팔각형 형태를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 7】

제6항에서,

상기 제1 화소는 복수개이며,

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상기 복수개의 제1 화소 각각은 동일한 사각형 형태를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 8】

제7항에서,

상기 제2 화소와 상기 제3 화소 각각은 서로 동일한 면적을 가지며,

상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각 사이의 거리는 동일한 제1 길이를 가지며,

이웃하는 상기 제1 화소 간의 거리는 상기 제1 길이 대비 긴 제2 길이를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 9】

제7항에서,

상기 제2 화소는 상기 제3 화소 대비 큰 면적을 가지며,

상기 제2 화소와 상기 제3 화소 사이의 거리는 제3 길이를 가지며,

상기 제1 화소와 상기 제2 화소 사이의 거리 및 상기 제1 화소와 상기 제3 화소 사이의 거리 각각은 동일한 제4 길이를 가지며,

이웃하는 상기 제1 화소 간의 거리는 상기 제3 길이 및 상기 제4 길이 대비 긴 제5 길이를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 10】

제6항에서,

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상기 제1 화소는 복수개이며,

상기 복수개의 제1 화소 중 이웃하는 제1 화소 각각은 서로 대칭인 사각형 형태를 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 11】

제10항에서,

상기 제2 화소는 상기 제3 화소 대비 큰 면적을 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 12】

제10항에서,

상기 제3 화소는 상기 제2 화소 대비 큰 면적을 가지는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 13】

제1항 내지 제12항 중 어느 한 항에서,

상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 서로 다른 색의 빛을 발광하는 유기 발광 표시 장치의 화소 배열 구조.

【청구항 14】

제13항에서,

상기 제1 화소, 상기 제2 화소 및 상기 제3 화소 각각은 녹색, 청색 및 적색 각각의 빛을 발광하는 유기 발광 표시 장치의 화소 배열 구조.

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제출 일자 : 2012-03-06

【요약서】

【요약】

유기 발광 표시 장치의 화소 배열 구조는 제1 화소, 상기 제1 화소와 이격되어 있으며 상기 제1 화소의 중심점을 정사각형의 중심점으로 하는 가상의 정사각형의 제1 꼭지점에 중심점이 위치하는 제2 화소, 및 상기 제2 화소와 이격되어 있으며 상기 가상의 정사각형의 상기 제1 꼭지점과 이웃하는 제2 꼭지점에 중심점이 위치하는 제3 화소를 포함한다.

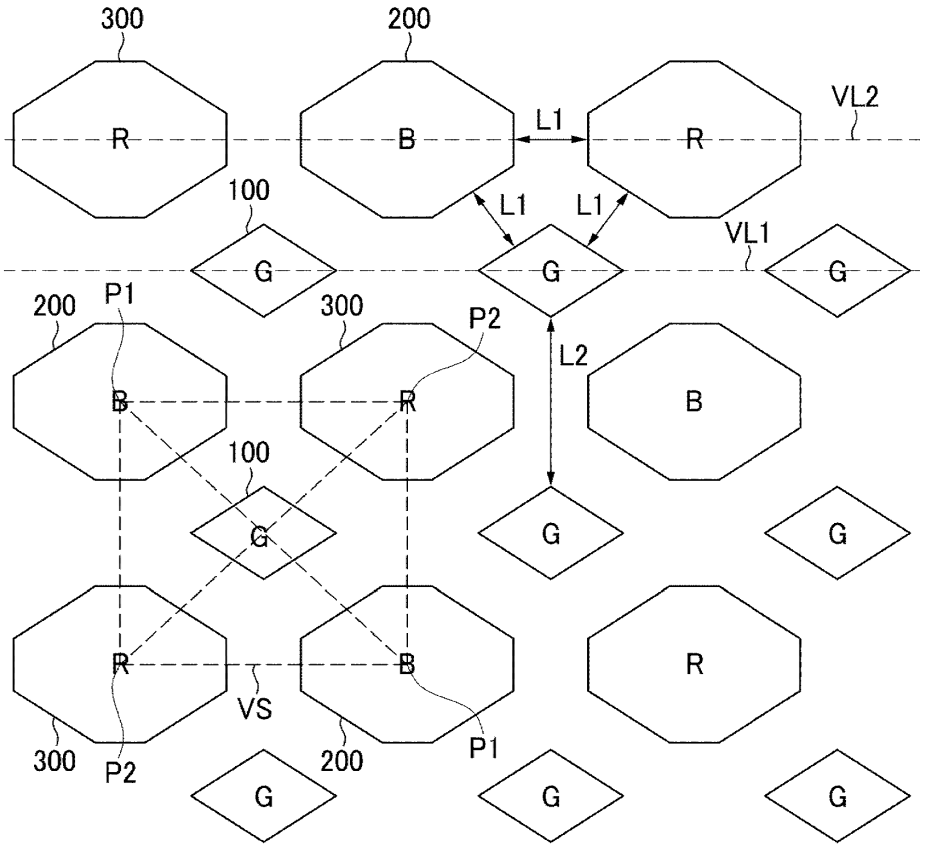
【대표도】

도 1

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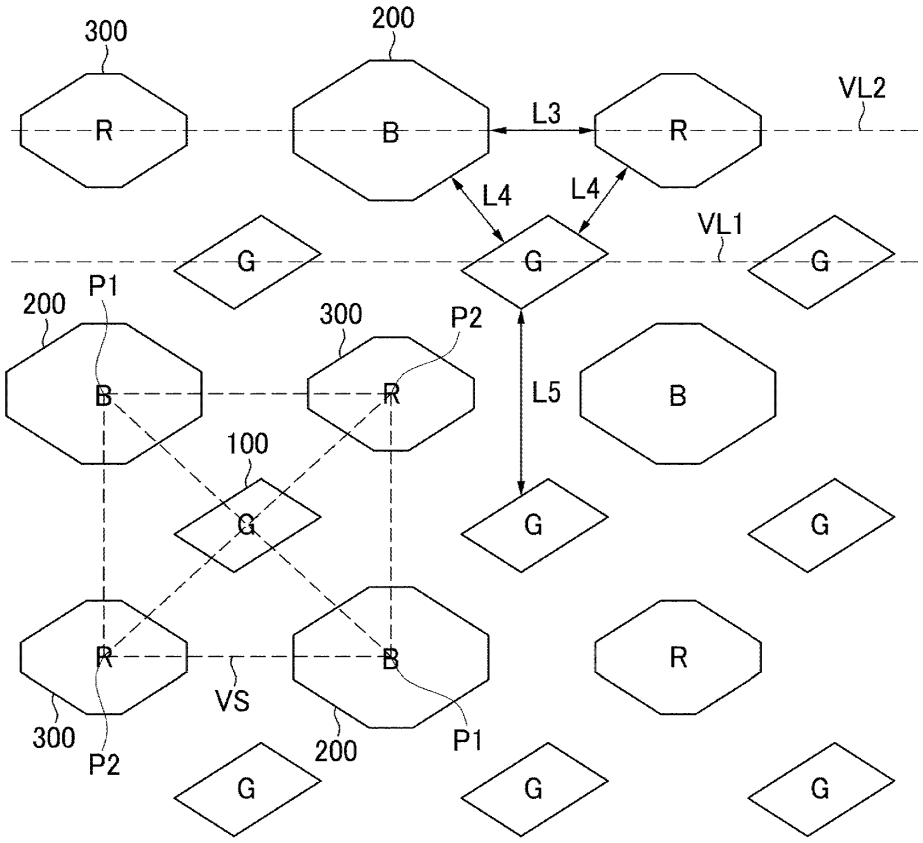
【도면】

【도 1】



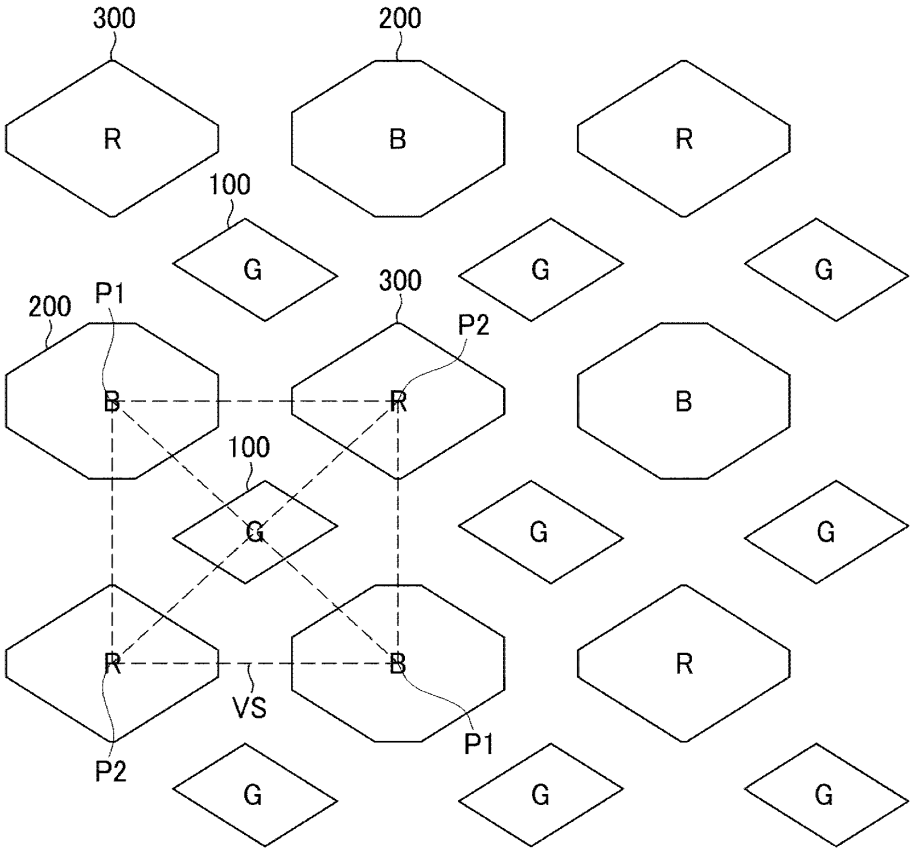
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【도 2】

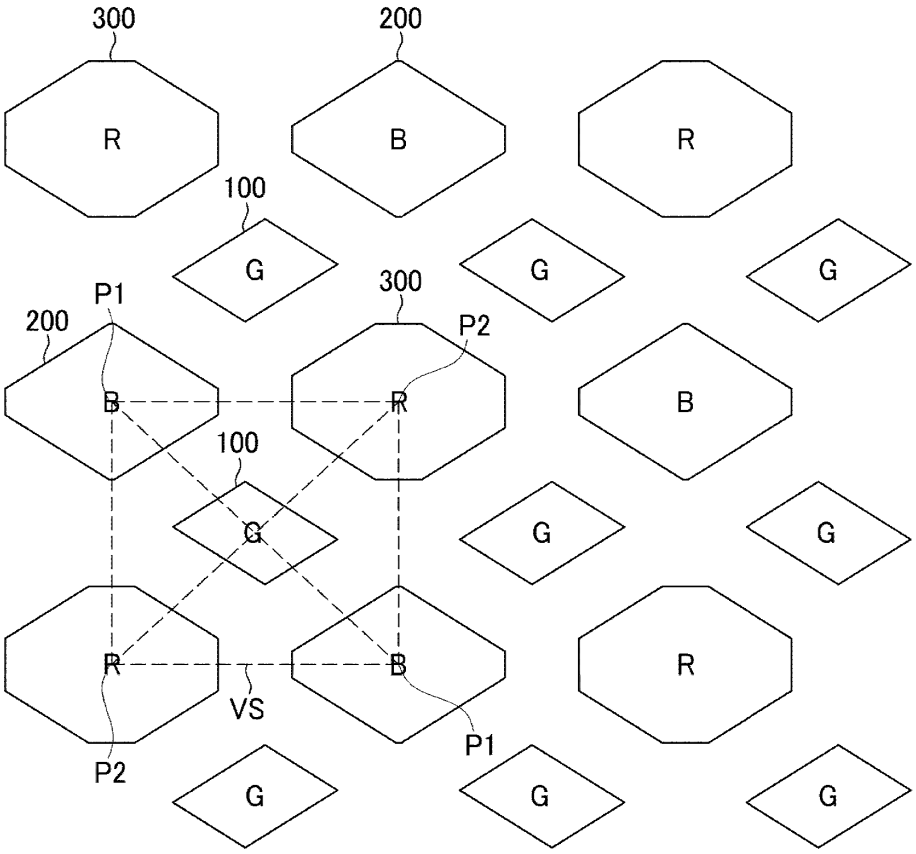


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【도 3】



【도 4】



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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224123
	Application Number	17/808,982
	Filing Date	June 24, 2022
	Inventor(s)	Sang-Shin Lee
	Group Art Unit	2691
	Examiner Name	DOCKET CENTRAL

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224123
	Application Number	17/808,982
	Filing Date	June 24, 2022
	Inventor(s)	Sang-Shin Lee
	Group Art Unit	2691
	Examiner Name	DOCKET CENTRAL

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		SIPO Office action dated March 11, 2015, corresponding to Chinese Patent application 201310035429.X, (7 pages)
		Taiwan Office action dated March 30, 2015, corresponding to Taiwanese Patent application 102101000, (7 pages)
		Korean Patent Abstracts of Korean Publication No. 10-2003-0031207 A, published April 21, 2003, which corresponds to KR 10-0807524 B1, 2 pages
		U.S. Office action dated July 15, 2015, for U.S. Patent Application 13/614,197, (11 pages)
		U.S. Office action dated December 2, 2015, for U.S. Patent application 13/614,197, (12 pages)
		U.S. Final Office Action dated February 1, 2021, issued in U.S. Patent Application No. 16/505,536 (8 pages)
		U.S. Office Action dated May 25, 2021, issued in U.S. Patent Application No. 16/505,536 (15 pages)
		U.S. Office Action dated October 21, 2020, issued in U.S. Patent Application No. 16/882,384 (24 pages)

EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

SJF/eg

118232178.1

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224123
	Application Number	17/808,982
	Filing Date	June 24, 2022
	Inventor(s)	Sang-Shin Lee
	Group Art Unit	2691
	Examiner Name	DOCKET CENTRAL

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		US Final Office Action dated November 24, 2021, issued in US Patent Application No. 16/505,536 (19 pages)
		U.S. Office Action from Application No. 16/505,536, dated May 11, 2022, 53 pages.
		Advisory Action for U.S. Application No. 13/614,197 dated May 18, 2015, 3 pages.
		Advisory Action for U.S. Application No. 13/872,018 dated November 14, 2016, 3 pages.
		Advisory Action for U.S. Application No. 13/872,018 dated December 8, 2015, 3 pages.
		Advisory Action for U.S. Application No. 16/505,536 dated April 7, 2021, 3 pages.
		Ex Parte Quayle Action for U.S. Application No. 13/614,197 dated January 5, 2017, 5 pages.
		Ex Parte Quayle Action for U.S. Application No. 15/090,591 dated August 5, 2016, 6 pages.
		Final Office Action for U.S. Application No. 13/614,197 dated December 2, 2015, 11 pages.
		Final Office Action for U.S. Application No. 13/872,018 dated May 11, 2017, 16 pages.
		Final Office Action for U.S. Application No. 13/872,018 dated June 23, 2016, 12 pages.
		Final Office Action for U.S. Application No. 13/872,018 dated October 16, 2015, 15 pages.
		Final Office Action for U.S. Application No. 14/059,356 dated June 18, 2015, 15 pages.
		Final Office Action for U.S. Application No. 15/811,599 dated January 21, 2020, 18 pages.
		Final Office Action for U.S. Application No. 16/505,536 dated October 27, 2020, 15 pages.
		Notice of Allowance for U.S. Application No. 13/614,197 dated March 22, 2017, 7 pages.
		Notice of Allowance for U.S. Application No. 13/614,197 dated July 11, 2017, 7 pages.
		Notice of Allowance for U.S. Application No. 13/872,018 dated February 19, 2020, 5 pages.
		Notice of Allowance for U.S. Application No. 13/872,018 dated May 28, 2020, 5 pages.
		Notice of Allowance for U.S. Application No. 14/059,356 dated April 27, 2016, 5 pages.

EXAMINER SIGNATURE		DATE CONSIDERED	

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SJF/eg

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224123
	Application Number	17/808,982
	Filing Date	June 24, 2022
	Inventor(s)	Sang-Shin Lee
	Group Art Unit	2691
	Examiner Name	DOCKET CENTRAL

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		Notice of Allowance for U.S. Application No. 14/059,356 dated November 25, 2015, 5 pages.
		Notice of Allowance for U.S. Application No. 15/090,591 dated February 13, 2017, 5 pages.
		Notice of Allowance for U.S. Application No. 15/090,591 dated July 31, 2017, 5 pages.
		Notice of Allowance for U.S. Application No. 15/090,591 dated December 9, 2016, 5 pages.
		Notice of Allowance for U.S. Application No. 15/688,760 dated January 30, 2019, 5 pages.
		Notice of Allowance for U.S. Application No. 15/688,760 dated September 14, 2018, 5 pages.
		Notice of Allowance for U.S. Application No. 15/811,599 dated February 14, 2019, 7 pages.
		Notice of Allowance for U.S. Application No. 15/811,599 dated March 31, 2020, 5 pages.
		Notice of Allowance for U.S. Application No. 15/811,599 dated July 10, 2020, 5 pages.
		Notice of Allowance for U.S. Application No. 16/261,437 dated January 10, 2020, 6 pages.
		Notice of Allowance for U.S. Application No. 16/261,437 dated April 27, 2020, 5 pages.
		Notice of Allowance for U.S. Application No. 16/261,437 dated August 14, 2020, 5 pages.
		Notice of Allowance for U.S. Application No. 16/261,437 dated December 28, 2020, 5 pages.
		Office Action for U.S. Application No. 13/872,018 dated February 29, 2016, 14 pages.
		Office Action for U.S. Application No. 13/872,018 dated June 30, 2015, 13 pages.
		Office Action for U.S. Application No. 13/872,018 dated December 30, 2016, 14 pages.
		Patent Board Decision on Appeal for U.S. Application No. 13/872,018 dated December 2, 2019, 8 pages.
		Restriction Requirement for U.S. Application No. 13/872,018 dated November 5, 2014, 8 pages.

EXAMINER SIGNATURE		DATE CONSIDERED	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. [3]Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [6]Applicant is to place a check mark here if English Language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224123
	Application Number	17/808,982
	Filing Date	June 24, 2022
	Inventor(s)	Sang-Shin Lee
	Group Art Unit	2691
	Examiner Name	DOCKET CENTRAL

OTHER DOCUMENTS		
EXAMINER INITIALS	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		Restriction Requirement for U.S. Application No. 15/811,599 dated March 28, 2018, 7 pages.
		U.S. Advisory Action from Application No. 13/614,197, dated February 5, 2016, 3 pages.
		U.S. Notice of Allowance from Application No. 14/059,356, dated September 10, 2015, 5 pages.
		U.S. Restriction Requirement from Application No. 13/614,197, dated August 18, 2014, 7 pages.
		U.S. Restriction Requirement from Application No. 16/505,536, dated August 5, 2019, 7 pages.
		U.S. Office Action dated July 8, 2022, issued in US Patent Application No. 17/005,753, 48 pages.

EXAMINER SIGNATURE		DATE CONSIDERED	

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SJF/eg

118232178.1

Electronic Acknowledgement Receipt

EFS ID:	46202596
Application Number:	17808982
International Application Number:	
Confirmation Number:	4376
Title of Invention:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Sang-Shin LEE
Customer Number:	23363
Filer:	Steven James French/Elizabeth Gomez
Filer Authorized By:	Steven James French
Attorney Docket Number:	224123/411598-06419
Receipt Date:	15-JUL-2022
Filing Date:	24-JUN-2022
Time Stamp:	15:35:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		224123_IDS.pdf	262825 9b007f5a7760c92864e15fe9311fa2fdd1df5d1c	yes	19

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	2
	Information Disclosure Statement (IDS) Form (SB08)	3	19

Warnings:					
Information:					
2	Other reference-Patent/Application/ Search Documents	7-8-22_OA_195033.pdf	2500974 47c8aab9db3fa9f1e57c0f072579d737fbc9f1ba	no	48
Warnings:					
Information:					
		Total Files Size (in bytes):	2763799		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on July 15, 2022 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Elizabeth Gomez/
Elizabeth Gomez

Inventor(s)	: Sang-Shin Lee	Confirmation No. 4376
Application No.	: 17/808,982	
Filed	: June 24, 2022	
Title	: PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	
Grp./Div.	: 2691	
Examiner	: DOCKET CENTRAL	
Docket No.	: 224123	

INFORMATION DISCLOSURE STATEMENT
FOR A CONTINUING NON-CPA APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
July 15, 2022

Commissioner:

In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, enclosed is an information disclosure statement. The references listed thereon are not enclosed because they were of record in the parent application, Application No. 17/005,753, filed August 28, 2020, except for the July 8, 2022 Office action mailed in Appl. No. 17/005,753, which is enclosed herewith.

It is respectfully requested that these references be considered in the examination of this application, and identified in the list of references cited on the patent issuing on this application. Applicant also requests that an initialed copy of the information disclosure statement be entered in the application file and returned to applicant with the next communication from the Office in accordance with MPEP § 609.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Steven French/
Steven J. French
Reg. No. 78,743
626/795-9900

SJF/eg
Information Disclosure Statement w/ reference

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/808,982	06/24/2022	Sang-Shin LEE	224123/411598-06419	4376

23363 7590 07/27/2022

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER
CENTRAL, DOCKET

ART UNIT	PAPER NUMBER
2691	

NOTIFICATION DATE	DELIVERY MODE
07/27/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PLPrivatePair@lrrc.com
pto@lewisroca.com

Decision Granting Request for Prioritized Examination (Track I)	**Application No.** 17/808,982	**Applicant(s)** LEE, Sang-Shin	
	Examiner CHERYL P GIBSON BAYLOR	**Art Unit** OPET	**AIA (FITF) Status** Yes

1. THE REQUEST FILED 24 June 2022 IS **GRANTED** .

The above-identified application has met the requirements for prioritized examination

A. ☑ for an original nonprovisional application (Track I).
B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination**. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

A. filing a **petition for extension of time** to extend the time period for filing a reply;

B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims** , or a multiple dependent claim;

C. filing a **request for continued examination** ;

D. filing a notice of appeal;

E. filing a request for suspension of action;

F. mailing of a notice of allowance;

G. mailing of a final Office action;

H. completion of examination as defined in 37 CFR 41.102; or

I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to CHERYL GIBSON BAYLOR at (571)272-3213. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.

/CHERYL GIBSON BAYLOR/ Paralegal Specialist, OPET	

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17808982
Filing Date	2022-06-24
First Named Inventor	Sang-Shin Lee
Art Unit	2691
Examiner Name	KWANG-SU YANG
Attorney Docket Number	224123/411598-06419

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060119738	A1	2006-06-08	Kido	

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

	1		

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2022-09-14
Name/Print	Jun-Young E. Jeon	Registration Number	43693

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	46619755
Application Number:	17808982
International Application Number:	
Confirmation Number:	4376
Title of Invention:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Sang-Shin LEE
Customer Number:	23363
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Filer Authorized By:	Jun-Young E. Jeon
Attorney Docket Number:	224123/411598-06419
Receipt Date:	14-SEP-2022
Filing Date:	24-JUN-2022
Time Stamp:	20:04:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	224123_IDS.pdf	1041919 d6bd46b2c5881839dfcb13b086c61e69bd130ac4	no	4

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/808,982	06/24/2022	Sang-Shin LEE	224123/411598-06419

CONFIRMATION NO. 4376

23363
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

PUBLICATION NOTICE

OC000000136516943

Title:PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Publication No.US-2022-0319404-A1
Publication Date:10/06/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/808,982	06/24/2022	Sang-Shin LEE	224123/411598-06419	4376

23363 7590 10/14/2022

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EXAMINER	
YANG, KWANG-SU	

ART UNIT	PAPER NUMBER
2691	

NOTIFICATION DATE	DELIVERY MODE
10/14/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PLPrivatePair@lrrc.com
pto@lewisroca.com

Office Action Summary	Application No. 17/808,982	Applicant(s) LEE, Sang-Shin	
	Examiner KWANG-SU YANG	Art Unit 2691	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 06/24/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-25 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-7,9-19,21-23 and 25 is/are rejected.

8) ☑ Claim(s) 8,20 and 24 is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☑ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 06/24/2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☑ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Priority

2. Receipt is acknowledged of certified copies of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

3. Claims 1-25 are objected to because of the following informalities:

- In line 10 of claim 1: "… green light; …" should be changed to --… green light, …--;
- In line 12 of claim 1: "… from each other; …" should be changed to --… from each other, …--;
- In line 16 of claim 1: "… consecutive green pixel; …" should be changed to --… consecutive green pixel, …--;
- In line 18 of claim 1: "… the virtual square; …" should be changed to --… the virtual square**,** …--;
- In lines 21-22 of claim 1: "… a same first length; …" should be changed to --… a first same length, …--;
- In line 24 of claim 1: "… the green pixels; …" should be changed to --… the green pixels, and …--;

- In line 26 of claim 1: "… two red pixels; …" should be changed to --… two red pixels, …--;
- In line 28 of claim 1: "… first green pixel; and …" should be changed to --… first green pixel, and …--;
- In line 30 of claim 1: "… along its long axis …" should be changed to --… along long axis …--;
- In line 31 of claim 1: "… along its short axis …" should be changed to --… along short axis …--;
- In line 2 of claim 4 and line 2 of claim 8: "… has a larger area than that of the first pixel …" should be changed to --… has an area larger than the first green pixel …--.
- In line 11 of claim 10: "… the third color of light; …" should be changed to --… the third color of light, …--.
- In line 17 of claim 10: "… from each other; …" should be changed to --… from each other; and …--;
- In lines 20-21 of claim 10: "… consecutive green pixel; …" should be changed to --… consecutive green pixel, …--;
- In line 23 of claim 10: "… the virtual square; …" should be changed to --… the virtual square, …--;
- In line 27 of claim 10: "… a same first length; …" should be changed to --… a first same length, …--;
- In line 29 of claim 10: "… the first pixels; …" should be changed to --… the first pixels, …--;

- In line 31 of claim 1: "… two third pixels; …" should be changed to --… two third pixels, …--;
- In line 33 of claim 1: "… the first pixels; and …" should be changed to --… the first pixels, and …--;
- In line 35 of claim 10: "… along its long axis …" should be changed to --… along long axis …--;
- In line 36 of claim 10: "… along its short axis …" should be changed to -- … along short axis …--; and
- In line 2 of claim 15 and line 2 of claim 20: "… has a larger area than that of the one of the first pixels …" should be changed to --… has an area larger than the one of the first pixels …--.

Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998);

In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

5. Claims 1-7, 9-19, 21-23 and 25 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 4-5, 3, 6-10, 13-15, 11, 20, 12, 16, 23-24, 25-27 and 28 of copending Application No. 17/808,983 in view of Phan (U.S. Patent No. US 7,215,347 B2).

The following is an example for comparing claim 1 of this application with claim 1 of Application No. 17/808,983.

Claim 1 of this application	Claim 1 of Application No. 17/808,983
An organic light emitting diode (OLED) display, comprising:	An organic light emitting diode (OLED) display, comprising:
a plurality of individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display and comprising:	a plurality of individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display and comprising:
a plurality of red pixels comprising an organic emission layer for emitting red light; a plurality of blue pixels comprising an organic emission layer for emitting blue light; and a plurality of green pixels comprising an organic emission layer for emitting green light;	a plurality of red pixels comprising an organic emission layer for emitting red light; a plurality of blue pixels comprising an organic emission layer for emitting blue light; and a plurality of green pixels comprising an organic emission layer for emitting green light;
wherein each of the red pixels, the blue pixels, and the green pixels are spaced apart from each other;	wherein the plurality of red pixels, the plurality of blue pixels, and the plurality of green pixels are spaced apart from one another;
wherein a first one of the green pixels has a center coinciding with a center of a virtual square, each vertex of the virtual square coinciding with a center of a different one of the green pixels and each edge of the virtual square passing through three consecutive green pixels;	

	wherein a first one of the red pixels has a center coinciding with a center of a virtual square, each vertex of the virtual square coinciding with a center of a different one of the red pixels; wherein the boundary of the virtual square only passes through eight of the plurality of pixels, of which four are blue pixels; wherein at least four green pixels are located entirely within the boundary of the virtual square;
wherein at least two of the blue pixels and at least two of the red pixels are located within the boundaries of the virtual square;	
wherein a shortest distance between the first green pixel and one of the at least two blue pixels within the virtual square as well as a shortest distance between the first green pixel and one of the at least two red pixels within the virtual square is a same first length; wherein the first length is smaller than a shortest distance between the first green pixel and an adjacent one of the green pixels;	wherein a shortest distance between the first red pixel and one of the four green pixels is a first length that is smaller than a shortest distance between two of the four green pixels;
wherein each of the at least two blue pixels has a larger area than each of the at least two red pixels;	wherein each of the four blue pixels through which the boundary of the virtual square pass has a larger area than each of the four green pixels.
wherein each of the at least two blue pixels has a larger area than that of the first green pixel; and	
wherein the first green pixel has a convex shape such that a line bisecting the first pixel along its long axis has a greater length than a line bisecting the first pixel along its short axis.	

Claim 1 of Application No. 17/808.983 anticipates claim 1 of the instant application except for the limitations "**wherein a first one of the green pixels has a center coinciding with a center of a virtual square, each vertex of the virtual square coinciding with a center of a different one of the green pixels and each edge of the virtual square passing through three consecutive green pixels; wherein at least two of the blue pixels and at least two of the red pixels are located within the boundaries of the virtual square; wherein each of the at least two blue pixels has a larger area than that of the first green pixel; and wherein the first green pixel has a convex shape such that a line bisecting the first pixel along its long axis has a greater length than a line bisecting the first pixel along its short axis.**"

Phan (Figs. 1-12) teaches

wherein a first one (e.g., a green dot at (3,4)) **of the green pixels has a center coinciding with a center of a virtual square** (Figs. 9.8 and 11a)**, each vertex of the virtual square coinciding with a center of a different one of the green pixels and each edge of the virtual square passing through three consecutive green pixels** (e.g., four edges: ({(3,2), (2,3), (1,4)}, {(1,4), (2,5), (3,6)}, {(3,6), (4,5), (5,4)}, {(5,4), (4,3), (3,2)}) (Figs. 9.8 and 11a)**;**

wherein at least two of the blue pixels (e.g., blue dots at (2,4) and (4,4)) **and at least two of the red pixels** (e.g., red dots at (3,3) and (3,5)) **are located within the boundaries of the virtual square** (Fig. 9.8)**;**

wherein each of the at least two second pixels (e.g., the blue dots at (2,4) and (4,4)) **has a larger area than that of the one of the first pixels** (e.g., the green dot at (3,4)) (Figs. 9.8, 11b and 12)**; and**

wherein the one (e.g., the green dot at (3,4) which matches the left lower green dot in Fig. 11b) **of the first pixels has a convex shape such that a line bisecting the one of the first pixels along its long axis** (a horizontal axis) **has a greater length than a line bisecting the one of the first pixels along its short axis** (a vertical axis) (Figs. 9.8, 11b and 12)**.**

Therefore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used dynamic pixels as taught by Phan in an organic light emitting diode display of Application No. 17/808,982 because overlapping of dynamic pixels on the static pixels creates an enhanced resolution at the human's eye.

Claims 2-7, 9-19, 21-23 and 25 are similarly rejected over claims 4-5, 3, 6-10, 13-15, 11, 20, 12, 16, 23-24, 25-27 and 28 of copending Application No. 17/808,983 in view of Phan.

This is a provisional nonstatutory double patenting rejection.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use

> the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 11-13 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification discloses "disposition process using a fine metal mask to form the green, blue, and red organic light emission layers respectively included in the first pixels 100, the second pixels 200, and the third pixels 300" ([0063], [0071], [0076], [0081], [0085 and [00105]), but the specification does not disclose the order of forming the first pixels, the second pixels, and the third pixels claimed in claims 11-13.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.

9. Claims 1-3 and 5 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Phan.

As to claim 1, Phan (Figs. 1-12) teaches **an organic light emitting diode (OLED) display** (Organic Light Emitting Diode (OLED) display; col. 1, lines 21-22)**, comprising:**

a plurality of individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display (the pixels generally consist of so-called dots representing the three basic colors red, green and blue; col. 1, lines 49-51) **and comprising:**

a plurality of red pixels (red dots 13) **comprising an organic emission layer** (by inherency of OLED display) **for emitting red light** (red) (Figs. 1a and 2a)**;**

a plurality of blue pixels (blue dots 15) **comprising an organic emission layer** (by inherency of OLED display) **for emitting blue light** (blue) (Figs. 1a and 2a)**; and**

a plurality of green pixels (green dots 14) **comprising an organic emission layer** (by inherency of OLED display) **for emitting green light** (green) (Figs. 1a and 2a)**;**

wherein each of the red pixels, the blue pixels, and the green pixels are spaced apart from each other (dots 11 are separated by masks 11; col. 4, lines 47-48) (Figs. 3a-3e)**;**

wherein a first one (e.g., a green dot at (3,4)) **of the green pixels has a center coinciding with a center of a virtual square** (Figs. 9.8 and 11a)**, each vertex of the virtual square coinciding with a center of a different one of the green pixels and each edge of the virtual square passing through three consecutive green pixels** (e.g., four edges: {(3,2), (2,3), (1,4)}, {(1,4), (2,5), (3,6)}, {(3,6), (4,5), (5,4)}, {(5,4), (4,3), (3,2)}) (Figs. 9.8 and 11a)**;**

wherein at least two of the blue pixels (e.g., blue dots at (2,4) and (4,4)) **and at least two of the red pixels** (e.g., red dots at (3,3) and (3,5)) **are located within the boundaries of the virtual square** (Fig. 9.8)**;**

wherein a shortest distance between the first green pixel (e.g., the green dot at (3,4)) **and one** (e.g., the blue dot at (2,4)) **of the at least two blue pixels within the virtual square as well as a shortest distance between the first green pixel** (e.g., the green dot at (3,4)) **and one** (e.g., the red dot at (3,3)) **of the at least two red pixels within the virtual square is a same first length** (Figs. 9.8 and 11a)**;**

wherein the first length is smaller than a shortest distance between the first green pixel (e.g., the green dot at (3,4)) **and an adjacent one** (e.g., the green dot at (2,5)) **of the green pixels** (Figs. 9.8 and 11a)**;**

wherein each of the at least two blue pixels (e.g., the blue dots at (2,4) and (4,4)) **has a larger area than each of the at least two red pixels** (e.g., the red dots at (3,3) and (3,5)) (Figs. 9.8, 11b and 12)**;**

wherein each of the at least two blue pixels (e.g., the blue dots at (2,4) and (4,4)) **has a larger area than that of the first green pixel** (e.g., the green dot at (3,4)) (Figs. 9.8, 11b and 12)**; and**

wherein the first green pixel (e.g., the green dot at (3,4) which matches the left lower green dot in Fig. 11b) **has a convex shape such that a line bisecting the first pixel along its long axis** (a horizontal axis) **has a greater length than a line bisecting the first pixel along its short axis** (a vertical axis) (Figs. 9.8, 11b and 12)**.**

As to claim 2, Phan teaches

wherein the first length is smaller than a shortest distance between one (e.g., the blue dot at (2,4)) **of the at least two blue pixels and one** (e.g., the red dot at (3,5)) **of the at least two red pixels** (Figs. 9.8 and 11b)**.**

As to claim 3, Phan teaches

wherein the first green pixel (e.g., the green dot at (3,4) which matches the left lower green dot in Fig. 11b) **has a different shape than the one** (e.g., the blue dot at (2,4) which matches the left upper blue dot in Fig. 11b) **of the blue pixels and the one** (e.g., the red dot at (3,5) which matches the right lower red dot in Fig. 11b) **of the red pixels** (Figs. 9.8 and 11b)**.**

As to claim 5, Phan teaches

wherein the one (e.g., the blue dot at (2,4)) **of the blue pixels and the one** (e.g., the red dot at (3,5)) **of the red pixels are four-sided polygons** (Figs. 9.8 and 11b)**.**

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 10, 14, 16-19 and 21 are rejected under 35 U.S.C. 103 as being unpatentable over Shim (U.S. Pub. No. US 2014/0191202 A1) in view of Phan

.

As to claim 10, Shim (Figs. 1-8) teaches **a method for manufacturing an organic light emitting diode (OLED) display** (making three sub-pixel regions that each have a top emission OLED micro-cavity structure; (Figs. 8A-8O)**, comprising:**

depositing, using a fine metal mask, organic light-emitting material configured to emit a first color of light (a green emissive layer 752 can be

highly defined using an evaporation deposition technique with a fine metal mask; [0080], lines 11-4; Fig. 8N);

forming a plurality of first pixels to emit the first color of light (a green subpixel region G) (Figs. 8N-8O);

depositing, using a fine metal mask, organic light-emitting material configured to emit a second color of light (a blue emissive layer 753 can be highly defined using an evaporation deposition technique with a fine metal mask; [0080], lines 11-4; Fig. 8N);

forming a plurality of second pixels to emit the second color of light (a blue subpixel region B) (Figs. 8N-8O);

depositing, using a fine metal mask, organic light-emitting material configured to emit a third color of light (a red emissive layer 751 can be highly defined using an evaporation deposition technique with a fine metal mask; [0080], lines 11-4; Fig. 8N); **and**

forming a plurality of third pixels to emit the third color of light (a red subpixel region R) (Figs. 8N-8O).

Shim does not expressly teach wherein: the first pixels, the second pixels, and the third pixels are individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display; each of the first pixels, the second pixels, and the third pixels are spaced apart from each other; one of the first pixels has a center coinciding with a center of a virtual square, each vertex of the virtual square coinciding with a center of a different one of the

first pixels and each edge of the virtual square passing through three consecutive first pixels; wherein at least two of the second pixels and at least two of the third pixels are located within the boundaries of the virtual square; wherein a shortest distance between the one the first pixels and one of the at least two second pixels within the virtual square as well as a shortest distance between the one the first pixels and one of the at least two third pixels within the virtual square is a same first length; wherein the first length is smaller than a shortest distance between the one of the first pixels and an adjacent one of the first pixels; wherein each of the at least two second pixels has a larger area than each of the at least two the pixels; wherein each of the at least two second pixels has a larger area than that of the one of the first pixels; and wherein the one of the first pixels has a convex shape such that a line bisecting the one of the first pixels along its long axis has a greater length than a line bisecting the one of the first pixels along its short axis.

Phan (Figs. 1-12) teaches **wherein:**

the first pixels, the second pixels, and the third pixels are individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display (the pixels generally consist of so-called dots representing the three basic colors red, green and blue; col. 1, lines 49-51)**;**

each of the first pixels, the second pixels, and the third pixels are spaced apart from each other (dots 11 are separated by masks 11; col. 4, lines 47-48) (Figs. 3a-3e)**;**

one (e.g., a green dot at (3,4)) **of the first pixels has a center coinciding with a center of a virtual square** (Figs. 9.8 and 11a)**, each vertex of the virtual square coinciding with a center of a different one of the first pixels and each edge of the virtual square passing through three consecutive first pixels** (e.g., four edges: {(3,2), (2,3), (1,4)}, {(1,4), (2,5), (3,6)}, {(3,6), (4,5), (5,4)}, {(5,4), (4,3), (3,2)}) (Figs. 9.8 and 11a)**;**

wherein at least two of the second pixels (e.g., blue dots at (2,4) and (4,4)) **and at least two of the third pixels** (e.g., red dots at (3,3) and (3,5)) **are located within the boundaries of the virtual square** (Fig. 9.8)**;**

wherein a shortest distance between the one (e.g., the green dot at (3,4)) **the first pixels and one** (e.g., the blue dot at (2,4)) **of the at least two second pixels within the virtual square as well as a shortest distance between the one** (e.g., the green dot at (3,4)) **the first pixels and one** (e.g., the red dot at (3,3)) **of the at least two third pixels within the virtual square is a same first length** (Figs. 9.8 and 11a)**;**

wherein the first length is smaller than a shortest distance between the one (e.g., the green dot at (3,4)) **of the first pixels and an adjacent one** (e.g., the green dot at (2,5)) **of the first pixels** (Figs. 9.8 and 11a)**;**

wherein each of the at least two second pixels (e.g., the blue dots at (2,4) and (4,4)) **has a larger area than each of the at least two the pixels** (e.g., the red dots at (3,3) and (3,5)) (Figs. 9.8, 11b and 12)**;**

wherein each of the at least two second pixels (e.g., the blue dots at (2,4) and (4,4)) **has a larger area than that of the one of the first pixels** (e.g., the green dot at (3,4)) (Figs. 9.8, 11b and 12)**; and**

wherein the one (e.g., the green dot at (3,4) which matches the left lower green dot in Fig. 11b) **of the first pixels has a convex shape such that a line bisecting the one of the first pixels along its long axis** (a horizontal axis) **has a greater length than a line bisecting the one of the first pixels along its short axis** (a vertical axis) (Figs. 9.8, 11b and 12)**.**

Therefore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used dynamic pixels as taught by Phan in a method for manufacturing an organic light emitting diode display of Shim because overlapping of dynamic pixels on the static pixels creates an enhanced resolution at the human's eye.

As to claim 14, Phan teaches

wherein the one (e.g., the green dot at (3,4) which matches the left lower green dot in Fig. 11b) **of the first pixels has a different shape than the one** (e.g., the blue dot at (2,4) which matches the left upper blue dot in Fig. 11b) **of the at least two second pixels and the one** (e.g., the red dot at (3,5) which

matches the right lower red dot in Fig. 11b) **of the at least two third pixels** (Figs. 9.8 and 11b)**.**

Therefore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used dynamic pixels as taught by Phan in a method for manufacturing an organic light emitting diode display of Shim because overlapping of dynamic pixels on the static pixels creates an enhanced resolution at the human's eye.

As to claim 16, Phan teaches

wherein the one (e.g., the blue dot at (2,4)) **of the at least two second pixels and the one** (e.g., the red dot at (3,5)) **of the at least two third pixels are four-sided polygons** (Figs. 9.8 and 11b)**.**

Therefore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used dynamic pixels as taught by Phan in a method for manufacturing an organic light emitting diode display of Shim because overlapping of dynamic pixels on the static pixels creates an enhanced resolution at the human's eye.

As to claim 17, Phan teaches

wherein the first pixels include an organic emission layer (by inherency of OLED display) **for emitting green light** (green)**, the second pixels include an organic emission layer** (by inherency of OLED display) **for emitting**

blue light (blue)**, and the third pixels include an organic emission layer** (by inherency of OLED display) **for emitting red light** (red) (Figs. 9.8 and 11b)**.**

Therefore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used dynamic pixels as taught by Phan in a method for manufacturing an organic light emitting diode display of Shim because overlapping of dynamic pixels on the static pixels creates an enhanced resolution at the human's eye.

As to claim 18, Phan teaches

wherein the first length is smaller than a shortest distance between the one (e.g., the blue dot at (2,4)) **of the at least two second pixels and the one** (e.g., the red dot at (3,5)) **of the at least two third pixels** (Figs. 9.8 and 11b)**.**

Therefore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used dynamic pixels as taught by Phan in a method for manufacturing an organic light emitting diode display of Shim because overlapping of dynamic pixels on the static pixels creates an enhanced resolution at the human's eye.

As to claim 19, Phan teaches

wherein the one (e.g., the green dot at (3,4) which matches the left lower green dot in Fig. 11b) **of the first pixels has a different shape than the one** (e.g., the blue dot at (2,4) which matches the left upper blue dot in Fig. 11b) **of**

the at least two second pixels and the one (e.g., the red dot at (3,5) which matches the right lower red dot in Fig. 11b) **of the at least two third pixels** (Figs. 9.8 and 11b)**.**

Therefore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used dynamic pixels as taught by Phan in a method for manufacturing an organic light emitting diode display of Shim because overlapping of dynamic pixels on the static pixels creates an enhanced resolution at the human's eye.

As to claim 21, Phan teaches

wherein the one (e.g., the blue dot at (2,4)) **of the at least two second pixels and the one** (e.g., the red dot at (3,5)) **of the at least two third pixels are four-sided polygons** (Figs. 9.8 and 11b)**.**

Therefore, it would have been obvious to one of ordinary skill in the art before the effective filing date of the claimed invention to have used dynamic pixels as taught by Phan in a method for manufacturing an organic light emitting diode display of Shim because overlapping of dynamic pixels on the static pixels creates an enhanced resolution at the human's eye.

Allowable Subject Matter

12. Claims 8, 20 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art, Phan and Shim, either individually or in combination, does not teach the limitation "**wherein the one of the red pixels has a larger area than that of the first pixel**" of claim 8 and the limitation "**wherein the one of the at least two third pixels has a larger area than that of the one of the first pixels**" of claims 20 and 24 in combination with other limitations of the base claim and any intervening claim(s).

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Han (U.S. Pub. No. US 2011/0177640 A1) is cited to teach a method for manufacturing an organic light emitting diode (OLED) display, in which the organic emission layer may be formed by a deposition process using a fine metal mask (FMM).

Inquiry

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwang-Su Yang whose telephone number is (571)270-7307. The examiner can normally be reached on Mon-Fri during 9:00am-6:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen, can be reached on (571)272-7772. The

fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/KWANG-SU YANG/
Primary Examiner, Art Unit 2691

Notice of References Cited	Application/Control No. 17/808,982	Applicant(s)/Patent Under Reexamination LEE, Sang-Shin	
	Examiner KWANG-SU YANG	Art Unit 2691	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20140191202-A1	07-2014	SHIM; Sungbin	H01L27/3213	257/40
*	B	US-20110177640-A1	07-2011	Han; Ji-Hwan	H01L27/3211	438/34
	C					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
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NON-PATENT DOCUMENTS

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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/808,982	LEE, Sang-Shin
	Examiner	**Art Unit**
	KWANG-SU YANG	2691

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/07/2022								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
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	24	O								
	25	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/808,982	LEE, Sang-Shin
	Examiner	Art Unit
	KWANG-SU YANG	2691

CPC - Searched*		
Symbol	Date	Examiner
G09G3/3208 H01L27/3218 H01L27/3216	10/06/2022	KY

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E Search: IDS Search	10/06/2022	KY
PE2E Search: Inventor and Assignee Search	10/06/2022	KY
PE2E Search: Text Search	10/06/2022	KY

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/KWANG-SU YANG/ Primary Examiner, Art Unit 2691	

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L213	2	"17808982"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/06 05:23 PM
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L217	346	(US-20030031207-$ | US-20040096706-$ | US-20080111130-$ | US-20090017910-$ | US-20090049515-$ | US-20110023996-$ | US-20110039773-$ | US-20110106565-$ | US-20110108050-$ | US-20110117613-$ | US-20110129531-$ | US-20120000887-$ | US-20120014074-$ | US-20120022967-$ | US-20160047800-$ | US-20200000840-$ | US-0000840-$ | US-0000887-$ | US-0001525-$ | US-0001527-$ | US-0001542-$ | US-0002911-$ | US-0012820-$ | US-0014074-$ | US-0015110-$ | US-0017910-$ | US-0018765-$ | US-0018858-$ | US-0022967-$ | US-0023996-$ | US-0027377-$ | US-0031207-$ | US-0033084-$ | US-0036421-$ | US-0037827-$ | US-0039773-$ | US-	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/06 07:26 PM

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L222	1	L221 AND (organic adj3 emitting SAME red SAME green SAME blue SAME (virtual ADJ square rhombus) SAME shortest ADJ distance SAME convex).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/06 09:27 PM
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L225	5	L223 AND (pixel sub$1pixel) NEAR (arrangement structure) SAME organic adj3 emitting SAME (pentile bayer) AND red SAME green SAME blue AND shortest ADJ distance	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/06 09:31 PM
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L227	100	(pixel sub$1pixel) NEAR (arrangement structure) SAME organic adj3 emitting SAME (pentile bayer) AND red SAME green SAME blue	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/06 09:44 PM
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L231	5729	(pixel sub$1pixel) AND organic adj3 emitting AND (pentile bayer)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/06 09:47 PM
L232	326	(pixel sub$1pixel) SAME organic adj3 emitting SAME (pentile bayer) AND red SAME green SAME blue	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2022/10/06 09:47 PM
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PE2E SEARCH - Search History (Similarity Search)

No Similarity Results available

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17808982
Filing Date	2022-06-24
First Named Inventor	Sang-Shin Lee
Art Unit	2691
Examiner Name	KWANG-SU YANG
Attorney Docket Number	224123/411598-06419

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	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

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Examiner Signature	/KWANG-SU YANG/	Date Considered	10/06/2022

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2022-09-14
Name/Print	Jun-Young E. Jeon	Registration Number	43693

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		
	Attorney Docket Number	224123
	Application Number	17/808,982
	Filing Date	June 24, 2022
	Inventor(s)	Sang-Shin Lee
	Group Art Unit	2691
	Examiner Name	DOCKET CENTRAL

U.S. PATENT DOCUMENTS				
EXAMINER INITIALS	Cite No.[1]	DOCUMENT NUMBER Number - Kind Code[2] (If Known)	PUBLICATION DATE OR ISSUE DATE MM-DD-YYYY	NAME OF PATENTEE
		4,491,863	01-01-1985	Kurahashi
		4,642,619	02-10-1987	Togashi
		4,965,565 A	10-23-1990	Noguchi
		5,113,274 A	05-12-1992	Takahashi et al.
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		5,485,293 A	01-16-1996	Robinder
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		6,747,618 B2	06-08-2004	Arnold et al.
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		6,933,976 B1	08-23-2005	Suzuki
		6,950,115 B2	09-27-2005	Brown Elliott
		7,075,242 B2	07-11-2006	Miller et al.
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EXAMINER SIGNATURE	/KWANG-SU YANG/	DATE CONSIDERED	10/06/2022

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		7,397,485 B2	07-08-2008	Miller et al.
		7,612,811 B2	11-03-2009	Takeuchi et al.
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		8,754,913 B2	06-17-2014	Hwang et al.
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	Cite No.[1]	Foreign Patent Document Country Code[3] - Number[4] - Kind Code[5] (If Known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6] (✓)
		CN 1726593 A	01-25-2006	Miller et al.	Corresponds to U.S. Pub. 2004/0113875 A1, listed above
		CN 1874000 A	12-06-2006	Zhao	Abstract
		CN 101009304 A	08-01-2007	Zhao et al.	Abstract
		CN 100439989 C	12-03-2008	Credelle et al.	Corresponds to US 7,755,652 B2, listed above.
		CN 100448020 C	12-31-2008	AUO OPTRONICS CO., LTD	Abstract
		CN 101449382 A	06-03-2009	Smith et al.	Abstract
		CN 102354479 A	02-15-2012	Liu et al.	Corresponds to US 8,334,859 B2 listed above.
		CN 103311266 A	09-18-2013	Lee	Abstract

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		CN 203260586 U	10-30-2013	Lee	Abstract
		CN 105206647 A	12-30-2015	Lee	Abstract
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		JP 10-39791	02-13-1998	Nakamura et al.	Japan Patent Abstract
		JP 2000-235891	08-29-2000	Fujimori et al.	Patent Abstracts of Japan
		JP 2001-33757 A	02-09-2001	Ikeda et al.	Corresponds to U.S. 6,552,706 B1 listed above.

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	Filing Date	June 24, 2022
	Inventor(s)	Sang-Shin Lee
	Group Art Unit	2691
	Examiner Name	DOCKET CENTRAL

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		Restriction Requirement for U.S. Application No. 15/811,599 dated March 28, 2018, 7 pages.
		U.S. Advisory Action from Application No. 13/614,197, dated February 5, 2016, 3 pages.
		U.S. Notice of Allowance from Application No. 14/059,356, dated September 10, 2015, 5 pages.
		U.S. Restriction Requirement from Application No. 13/614,197, dated August 18, 2014, 7 pages.
		U.S. Restriction Requirement from Application No. 16/505,536, dated August 5, 2019, 7 pages.
		U.S. Office Action dated July 8, 2022, issued in US Patent Application No. 17/005,753, 48 pages.

EXAMINER SIGNATURE	/KWANG-SU YANG/	DATE CONSIDERED	10/06/2022

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SJF/eg

118232178.1 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KY/

Bibliographic Data

Application No: 17/808,982

Foreign Priority claimed: (•) Yes ( ) No

35 USC 119 (a-d) conditions met: [✓] Yes [ ] No [ ] Met After Allowance

Verified and Acknowledged: /KWANG-SU YANG/ Examiner's Signature [ ] Initials

Title: PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
06/24/2022	345	2691	224123/411598-06419
RULE			

APPLICANTS

SAMSUNG DISPLAY CO., LTD., Yongin-si, KOREA, REPUBLIC OF

INVENTORS

Sang-Shin LEE, Yongin-si, KOREA, REPUBLIC OF

CONTINUING DATA

This application is a CON of 17005753 08/28/2020

17005753 is a CON of 13872018 04/26/2013 PAT 10832616

13872018 is a CIP of 13614197 09/13/2012 PAT 9818803

FOREIGN APPLICATIONS

KOREA, REPUBLIC OF KR10-2012-0022967 03/06/2012

KOREA, REPUBLIC OF KR10-2013-0044993 04/23/2013

IF REQUIRED, FOREIGN LICENSE GRANTED**

06/30/2022

STATE OR COUNTRY

KOREA, REPUBLIC OF

ADDRESS

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001
UNITED STATES

FILING FEE RECEIVED

$6,660

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

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	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

	1	US Office Action dated September 19, 2022, issued in US Patent Application No. 17/808,985 (25 pages)	
	2	US Office Action dated October 14, 2022, issued in US Patent Application No. 17/808,983 (23 pages)	

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	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

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See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Peter Hsueh/	Date (YYYY-MM-DD)	2022-10-26
Name/Print	Peter Hsueh	Registration Number	45574

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	17808982
Filing Date:	24-Jun-2022
Title of Invention:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Sang-Shin LEE
Filer:	Peter C. Hsueh/Elizabeth Gomez
Attorney Docket Number:	224123/411598-06419

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt	
EFS ID:	46902064
Application Number:	17808982
International Application Number:	
Confirmation Number:	4376
Title of Invention:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Sang-Shin LEE
Customer Number:	23363
Filer:	Peter C. Hsueh/Elizabeth Gomez
Filer Authorized By:	Peter C. Hsueh
Attorney Docket Number:	224123/411598-06419
Receipt Date:	26-OCT-2022
Filing Date:	24-JUN-2022
Time Stamp:	23:28:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$260
RAM confirmation Number	E20220PN29052513
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Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	224123_IDS.pdf	1041987 370a98e060905a90a580f5990deb62225f43e93b	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Other reference-Patent/Application/ Search Documents	9-19-22_OA_224130.pdf	1390668 ff5b8827343c8337c74a69ca91e092271f7c74be	no	25
Warnings:					
Information:					
3	Other reference-Patent/Application/ Search Documents	10-14-22_OA_224128.pdf	1304804 ea294a1cf64669a663ab410aa9d534cc1ded1598	no	23
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4	Fee Worksheet (SB06)	fee-info.pdf	38360 4890e7a8bfac7757a1170c273d0d157c3ba170d3	no	2
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		Total Files Size (in bytes):	3775819		

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New International Application Filed with the USPTO as a Receiving Office

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	17808982
Filing Date	2022-06-24
First Named Inventor	Sang-Shin Lee
Art Unit	2691
Examiner Name	YANG, KWANG-SU
Attorney Docket Number	224123/411598-06419

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5742129		1998-04-21	Nagayama et al.	
	2	6838819	B2	2005-01-04	Kim et al.	
	3	7187425	B2	2007-03-06	Yamazaki	
	4	7301273	B2	2007-11-27	Dedene et al.	
	5	8118633	B2	2012-02-21	Yuasa	
	6	8587003	B2	2013-11-19	Ando	
	7	8883532	B2	2014-11-11	Ando	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20030218618	A1	2003-11-27	Phan	
	2	20090321727	A1	2009-12-31	Yutani et al.	
	3	20100315318	A1	2010-12-16	Lee et al.	
	4	20120176298	A1	2012-07-12	Suh et al.	
	5	20160124557	A1	2016-05-05	Choi	
	6	20220319406	A1	2022-10-06	Lee	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	1168448	EP	A2	2002-01-02	Kim et al.	Corresponds to US 6838819, listed above	
	2	1450408	EP	A2	2004-08-25	Dedene et al.	Corresponds to US 7301273, listed above	

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	3	8-227276	JP	A	1996-09-03	Nagayama et al.	Corresponds to US 5742129, listed above	
	4	2001-76881	JP	A	2001-03-23	SHARP KK	Abstract	
	5	2005-62416	JP	A	2005-03-10	Yamazaki	Corresponds to US 7187425, listed above	
	6	2008-277264	JP	A	2008-11-13	Yuasa	Corresponds to US 8118633, listed above	
	7	2008-298966	JP	A	2008-12-11	KYOCERA CORP	Abstract	
	8	2012-79631	JP	A	2012-04-19	Ando	Corresponds to US 8587003, listed above	
	9	10-2006-0118868	KR	A	2006-11-24	Seong	Abstract	

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	US Office Action dated November 3, 2022, issued in US Patent Application No. 17/808,984 (25 pages).	
	2	US Office Action dated November 10, 2022, issued in US Patent Application No. 17/865,304 (23 pages).	

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	Art Unit	2691
	Examiner Name	YANG, KWANG-SU
	Attorney Docket Number	224123/411598-06419

	3	Chinese Office Action dated September 13, 2022, issued in Chinese Patent Application No. 201910040602.2 (9 pages).	

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Examiner Signature		Date Considered	

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SIGNATURE

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Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2022-11-17
Name/Print	Jun-Young E. Jeon	Registration Number	43693

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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(54) Display element array for emissive fixed format display

(57) The present invention provides a multicolor OLED pixel structure having a plurality of light emitting color elements, each color element emitting light of a particular color. Optical centers of the color elements coincide substantially at an optical center for the pixel structure and any portion of a color element of the pixel structure has an equally luminous portion of the same color element located diametrically opposite thereto with respect to the optical center of the pixel structure. Light from all the color elements adds to be able to form emitted white light.

A plurality of pixel structures may be formed into an array for an active or passive display.

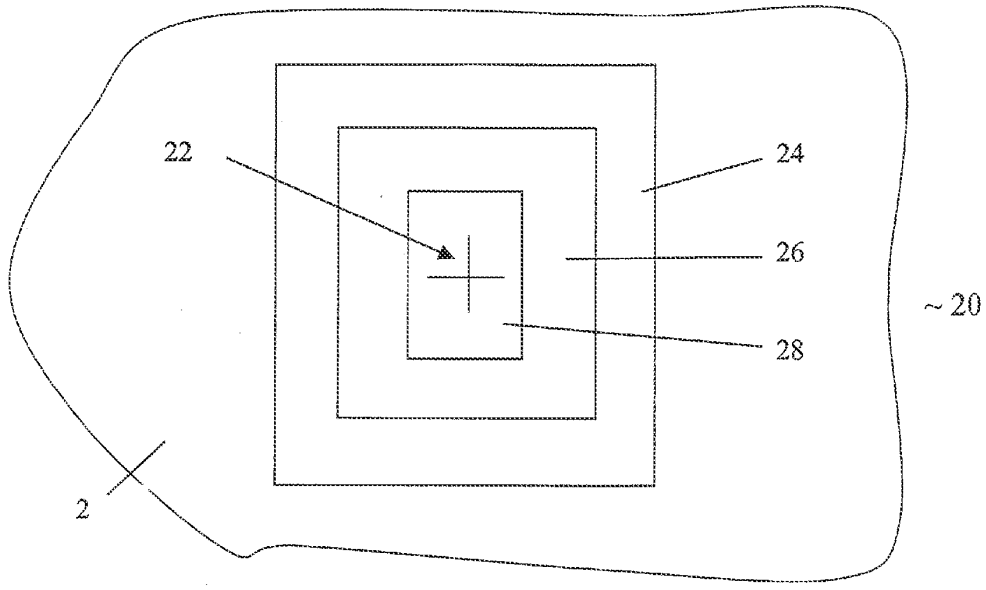


Fig. 7

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Description

Field of the invention

[0001] The present invention relates to emissive, fixed format displays especially direct view displays, for instance having emissive elements comprising Organic Light Emitting Diodes (OLED) and methods of fabricating and operating the same.

Background of the invention

[0002] Emissive, fixed format especially direct view displays such as Light Emitting Diode (LED), Field-Emission (FED), Plasma, EL and OLED displays have been used in situations where conventional CRT displays are too bulky and/or heavy and provide an alternative to non-emissive displays such as Liquid Crystal displays (LCD). Fixed format means that the displays comprise an array of light emitting cells or pixel structures that are individually addressable rather than using a scanning electron beam as in a CRT. Fixed format relates to pixelation of the display as well as to the fact that individual parts of the image signal are assigned to specific pixels in the display. Even in a color CRT, the phosphor triads of the screen do not represent pixels; there is neither a requirement nor a mechanism provided, to ensure that the samples in the image in any way align with these. The term "fixed format" is not related to whether the display is extendable, e.g. via tiling, to larger arrays. Fixed format displays may include assemblies of pixel arrays, e.g. they may be tiled displays and may comprise modules made up of tiled arrays which are themselves tiled into supermodules. Thus "fixed format" does not relate to the fixed size of the array but to the fact that the display has a set of addressable pixels in an array or in groups of arrays. Making very large fixed format displays as single units manufactured on a single substrate is difficult. To solve this problem, several display units or "tiles" may be located adjacent to each other to form a larger display, i.e. multiple display element arrays are physically arranged side-by-side so that they can be viewed as a single image. Transferring image data by packetized data transmission to the various display devices makes segregation of the displayed image into tiles relatively easy. At the junction of the tiles, usually some means to hide the join is applied. Such could be an opaque mask, as is for instance done in the case of tiled LCD displays, where the image of individual LCD panels is projected on a black matrix. To maintain a uniform appearance to the display, this mask is extended over the complete surface of the display and comprises an array of openings that coincide with the light emitting pixel structures of the display, or an array of openings that coincides with a group of light emitting pixel structures of the display (e.g. array of 4x4 pixels in one opening of the mask). OLED displays provide certain advantages for tiled displays such as lightweight, ease of manufacture, wide angle of view, and the ability to use back-connectors which allows close tiling with the smallest joint between tiles.

[0003] The human eye can detect very subtle color shifts or brightness changes and the optical non-uniformity and asymmetry introduced at the borders of tiles can produce disturbing optical effects. The traditional method of manufacture of OLED displays results in a pixel structure as shown schematically in Fig. 1 with a transparent substrate 2, usually a glass substrate, being closest to the viewer and facing in the display direction. Behind this substrate a series of layers 4-8 are deposited, e.g. at least a first transparent electrode 4, the organic light emitting element 6 and a second electrode 8. An organic LED material is deposited for each color in each pixel structure, e.g. three color elements 6, red, green and blue, for each pixel structure. Thus, each pixel structure can emit white light or any color by controlling the light energy emitted from each color element of a pixel structure. Usually additional layers are deposited such as electron and hole transport layers 7, 5 (see Fig. 1 that has been adapted from Fig. 4-13 of "Display Interfaces", R. L. Myers, Wiley, 2002). Thus, the light emitting elements 6 are located at a certain distance below the transparent substrate 2 and light can be reflected towards the viewer from the edges of the glass substrate 2 at the tile edges. Which light is reflected depends on which color element 6 of the edge-closest pixel structure is closest to the edge of the tile. The conventional color elements 6R, 6G, 6B of one pixel structure of an OLED are shown in Fig. 2 deposited onto a substrate 2 - the electrodes and other layers are not shown. The color elements 6R, 6G, 6B are arranged in parallel, rectangular strips. The tile edge effect of such an arrangement differs depending upon which edge 10, 12 of the tile is closest to the pixel structure. If the edge (10) is parallel to the strips, then the light reflected towards the viewer from the edge of the glass substrate 2 at certain viewing angles will be dominated by the color of the closest color emitting element 6, e.g. 6B emitting blue light. This color will generate a color shift near the tile edge 10 generating a colored "halo" effect along edge 10, particularly at certain viewing angles. At the edge 12, all three color elements are equally close to the edge and therefore balanced colored light is reflected from the tile edge. This will not cause a color shift but may make the edge look slightly brighter or darker at certain viewing angles.

[0004] A further problem is the effect of viewing angle and parallax resulting in vignetting, e.g. with masks or other optical elements. As there is a significant distance in the viewing direction between the emitting point of light of the OLED pixel structure and the mask, a viewer will see light emitted from more or less of the pixel structure surface area depending on the angle of view (see Fig. 3a). This distance is determined as a minimum by the thickness of the substrate 2. This problem can be reduced by using non-occluded masks. A non-occluded mask has openings which are larger than the light emit-

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ting surface area of a pixel structure so that when viewed along a normal to the pixel structure, light from the complete emitting surface of the pixel structure can be seen (non-occluded mask 9 of Fig. 3a). However, even with a non-occluded mask 9, parallax effects caused by the mask can occur at larger angles of view, an effect called vignetting. The effect of vignetting is to reduce the light intensity from a part of the pixel structure. If this part has a predominance in one of the colors emitted from the pixel structure, the result will be a color shift which depends on viewing angle. In addition, mask misalignment can reduce the viewing angle in the direction in which an edge of the mask opening is closest to the pixel structure (see Fig. 3b) and/or can produce color shifts.

[0005] A further problem can occur with displays in which an array of optical elements is used, e.g. commercial large size displays such as e.g. as used in shopping malls, train stations, airports etc. Such displays may be arranged on a wall at a certain distance from the average viewer. Due to physical restrictions such as the height of the target observer who will normally be between 1 and 2 meters, it is not necessary for the display to emit light in a wide angle. Power and cost can be saved by directing the display beam only within a useful angle. One way of doing this is to provide an optical element such as a lens in front of the display that concentrates the emitted light within the desired viewing angle. For instance, each pixel structure may be associated with a lens. However, misalignments between the optical axis of the lens and the pixel structure as well as the difference in optical centers of gravity of each color element of a conventional pixel structure means that the color displayed depends on the angle of view. A known partial solution to this problem is described in US 2002/0050958 that requires each color element of a pixel structure to have its own lens. However, for high resolution displays this involves manufacturing and accurately placing very small lenses. The array of optical elements can have other functions besides the tailoring of the light distribution produced by the pixels.

Summary of the Invention

[0006] It is an object of the present invention to provide emissive, fixed format displays, especially tiled arrays made up of smaller display tiles, for instance, OLED displays which do not show as many of the color shift effects of conventional displays as well as methods of manufacturing and operating such improved displays.

[0007] The present invention provides a multicolor OLED pixel structure, comprising: a plurality of light emitting color elements, each color element emitting light of a particular color, the optical centers of the color elements coinciding substantially at an optical center for the pixel structure; any portion of a color element of the pixel structure having an equally luminous portion of the same color element located diametrically opposite thereto with respect to the optical center of the pixel structure. Light from all the color elements may add to be able to form emitted white light. The symmetry of the pixel structure provides improved operation when an optical element is placed between the pixel structure and the viewer, e.g. a lens or for example a mask, either occluded or non-occluded. The outer shape of the pixel structure may be polygonal, e.g. in particular rectangular as this allows good packing of the pixel structures in a rectangular array. Preferably, each one or more color elements which emit one color are arranged symmetrically about a line passing through the optical center. Each one or more color elements which emit one color are preferably arranged symmetrically about a second line passing through the optical center which is perpendicular to the first line. Advantageously the plurality of light emitting color elements comprise elements which emit light of one of three or more primary colors, and one or more color elements emitting one primary color are arranged substantially concentrically with respect to one or more color elements emitting another primary color.

[0008] The plurality of light emitting color elements preferably comprise rectangular elements arranged in a row. The pixel structure has an outer envelope which defines the periphery of a light emitting area and the plurality of light emitting color elements preferably comprise elements which emit light of one of a number of primary colors, a light emitting element of each primary color extending to the outer envelope.

[0009] Preferably, the light emitting elements emitting one color extend to at least two different positions on the periphery, e.g. as defined by an envelope around the light emitting areas. This reduces color shifts as all color elements are exposed or occluded by vignetting elements. The pixel structure may be sandwiched between a first main electrode common to all light emitting color elements and a plurality of second electrodes, each second electrode contacting one of the light emitting color elements. Preferably, the pixel structure has a plurality of conducting areas local to each pixel for connection to an electrical power supply. By using local contacts the supply to each pixel structure can be improved.

[0010] The present invention also provides an array of pixel structures as described above. For example, each pixel structure being located on a transparent or an opaque substrate, each pixel structure comprising: a plurality of light emitting color elements, each color element emitting light of a particular color; the optical centers of the color elements coinciding substantially at an optical center for the pixel structure; any portion of a color element of the pixel structure having an equally luminous portion of the same color element located diametrically opposite thereto with respect to the optical center of the pixel structure. In the array each pixel structure can be sandwiched between a first main electrode common to all light emitting color elements and a plurality of second electrodes, each second electrode contacting one of the light emitting color elements. Each pix-

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el structure preferably has a plurality of conducting areas local to each pixel for connection to an electrical power supply. The conductive areas may be for connection to a PCB. The array may have a display direction and may further comprise an optical element located on the display direction side of the array. The optical element can be a vignetting element, a lens or a mask or similar.

[0011] The pixel structures in array form may form a passive matrix OLED display. The display may be a display tile. Tiles may be abutted to each other in a linear or a 2 or more dimensional array of tiles to form a larger array, a module of a display formed from a plurality of modules, a supermodule and an array formed from a plurality of such supermodules, etc.

[0012] The present invention provides a method of manufacture of a multicolor OLED pixel structure, comprising: forming a plurality of light emitting color elements on a substrate, each color element being for emitting light of a particular color; the optical centers of the color elements coinciding substantially at an optical center for the pixel structure; any portion of a color element of the pixel structure having an equally luminous portion of the same color element located diametrically opposite thereto with respect to the optical center of the pixel structure. The pixel structures may be formed in an array, whereby each of the pixel structures in the array and each color element may be addressed separately. The array by be formed into a display and may be provided with contacts for back connecting the array to electronic circuitry, e.g. driver circuits, addressing circuits, power circuits.

[0013] The dependent claims define independent embodiments of the present invention. The present invention will now be described with reference to the following drawings.

Brief Description of the Drawings

[0014]

Fig. 1 shows a cross-section through the layers of a conventional OLED pixel structure.

Fig. 2 shows a top view of the color elements of a conventional OLED multi-color pixel structure.

Figs. 3a shows a non-occluded mask that can be used with the present invention and Fig. 3b shows parallax/vignetting effects which occur when there is mask misalignment.

Fig. 4 shows a schematic representation of a pixel structure design in accordance with an embodiment of the present invention.

Figs. 5 - 9 show schematic representations of alternative pixel structure designs in accordance with embodiments of the present invention.

Fig. 10 is a schematic representation of a Cartesian pixel structure array that can be used with the present invention.

Fig. 11 shows a preferred pixel structure in accordance with an embodiment of the present invention.

Fig. 12 shows yet a further pixel structure in accordance with an embodiment of the present invention.

Fig. 13 shows the pixel structure of Fig. 5 with a mask and optical element in accordance with an embodiment of the present invention.

Figs. 14A shows a back view of a pixel electrode arrangement for the pixel structure of Fig. 5 in accordance with an embodiment of the present invention. Fig. 14B shows a cross-sectional view through the arrangement of Fig. 14A.

Fig. 15 shows a conventional addressing electrode scheme for an OLED display.

Fig. 16 shows an addressing electrode arrangement for the pixel structure of Fig. 11 in accordance with an embodiment of the present invention.

Fig. 17A shows a cross-section through a display element and a driver board in accordance with an embodiment of the present invention. Fig. 17B shows and alternative electrode arrangement for the pixel structure of Fig. 11 in accordance with an embodiment of the present invention.

Description of the Illustrative embodiments

[0015] The present invention will be described with reference to certain embodiments and to certain drawings but the present invention is not limited thereto but only by the attached claims. The embodiments are presented by way of example only and the skilled person will appreciate that the present invention has a wide application. For example, the present invention will be particularly described with reference to tiles for tiled displays that require back-connections but the present invention is not limited thereto and may be used with non-tiled displays. Further, the present invention provides arrays of emissive pixels provided with a means for directing or obscuring light in certain directions, e.g. a mask or an optical element such as a lens, a Fresnel lens, a diffraction grating, a holographic element such as a hologram, a diffractive or refractive optical element or a combination of any of these. For instance, the display can either have a mask, or an optical element per pixel such as a lens, or a plurality of lenses/optical elements per pixel, e.g. microlenses, or a combination of optical element(s), especially refractive optical elements and a mask. Lenses and masks both cause vignetting and result in color shifts unless the pixel area is oversize and the vignetted area of the pixel is compensated by an emissive part on the other side of the symmetry axis of the pixel becoming apparent, i.e. another part diametrically opposite in the pixel layout which contributes to the emissive light output which is exposed when the other side of the pixel is vignetted. When a mask is used and a color shift occurs, this color shift will always be caused by vignetting. Vignetting is defined as the gradual reduction of luminance as the off-axis angle increases resulting from the partial obscuration of the light bundle by

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limiting apertures of optical elements within the optical system. Due to the fact that there is a distance between the active emissive elements of an OLED and the mask lying on or adjacent to the outer surface of the substrate, the mask can reduce the optical aperture of the pixel and cause vignetting. When an asymmetric color pixel structure is vignetted then the part of the aperture which is obscured will contain more of one color than the others. Thus it will cause a color shift. This is most pronounced at the edges of the display, i.e. where the viewing angle is not perpendicular to the display. However, when an optical element such as a lens is used, the color shift can be caused by vignetting and/or the operation of the optical element or especially defects therein. Optical elements can give rise to a color shift, without the occurrence of vignetting. The fact that the optical centers of the different colors in a pixel do not coincide gives rise to a color shift due to refraction effects in the optical element. If one color center is located far off the optical axis of a lens, then it will refract differently than another color center lying close to the axis. Thus, colors will be directed from the optical element in different directions and the color generated by the pixel will depend upon viewing angle. In one aspect of the present invention either or both types of problems can be solved by using a sub-pixel emissive element layout having certain types of geometric symmetry.

[0016] The present invention will mainly be described with reference to a passive matrix display for which it is ideally suited. However, the present invention may also be used in active matrix displays. The present invention will also mainly be described with reference to depositing light emitting elements onto a transparent substrate. However, the present invention includes deposition onto other substrates, e.g. opaque or translucent substrates. The opaque substrate may be a ceramic material for example. When an opaque substrate is used the arrangement as shown as shown schematically in Fig. 1 may be applied to an opaque substrate 2, being furthest from the viewer and facing away from the display direction. In front of this substrate a series of layers 4-8 are deposited, e.g. at least a first transparent electrode 4, the organic light emitting element 6 and a second electrode 8. An organic LED material is deposited for each color in each pixel structure, e.g. a plurality of color elements 6, red, green and blue, for each pixel structure, whereby there may be more than one color element for each primary color. Each pixel structure can emit white light or any color by controlling the light energy emitted from each color element of a pixel structure. Usually additional layers are deposited such as electron and hole transport layers 7, 5. On top of these elements a transparent encapsulating or sealing layer may be applied, deposited or fixed (not shown in Fig. 1). Just as for the device described with reference to Fig. 1, the light emitting elements 6 are located at a certain distance below encapsulation layer and light can be reflected towards the viewer from the edges of the layer at the tile edges. The tile edge effect of such an arrangement is similar to the effects described for the device of Fig. 1. Also, at the front side an optical element such as a vignetting element, a lens, a mask, a Fresnel lens, a hologram or similar may be applied or fixed.

[0017] The present invention will also mainly be described with reference to a rigid material for the substrate 2. However, the present invention is not limited thereto. The present invention also includes depositing OLED color emitting elements onto flexible substrates such as polyester or polyimide substrates to form a flexible display sheet.

[0018] Fig. 4 is a schematic representation of a front view of an OLED multicolor pixel structure 20 suitable for use with an optical element such as a lens or with a mask or other vignetting element in accordance with one embodiment of the present invention. The lens may have a size (i.e. area) of at least the pixel structure or greater rather than being the size of one color element 24, 26, 28 of the pixel structure 20. The electrodes have been omitted from this drawing for clarity purposes. In this structure, each portion of a color element 24-28, e. g. 241, has an equally sized or equally luminescent area of the same color element 24-28, e.g. 243 located diametrically opposite from it with respect to the optical center 22 of the pixel structure 20. The optical center of a group of emissive sub-pixel elements of the same emissive color is the "center of gravity" of the luminous output of the combined group. Preferably, each color element or combination of color elements for one color 24-28 has an optical center that coincides at least approximately with the optical center 22 of the pixel structure 20. In this way, any color emitting sub-element 24-28 is at least locally diametrically symmetrical with respect to the optical center 22. This symmetrical arrangement with coinciding optical centers for all emissive colors, means, when the pixel structure is combined with a refractive optical element, that the combined light emitted from all of the color elements 24-28 is always projected from the optical element in a similar direction.

[0019] Various degrees of symmetry may be provided in each pixel structure. Some examples are shown schematically in Figs. 5 to 8. In Fig. 5, the three color elements 24, 26, 28 are arranged as pairs of parallel strips 24, 25; 26, 27; with a central single strip 28 in each pixel structure 20 - similar to that shown in Fig. 4. The three color elements are arranged symmetrically around the optical center of gravity 22. In this case lines of symmetry can be identified that are orthogonal lines passing through the optical center 22. In Figs. 6A and B, more symmetry is provided and the areas of light emitting OLED material are no longer parallel strips. Also, in this case, there is local diametrical symmetry about the optical center 22 for each color separately at any orientation angle, but the area of one color element (the outer one) varies with the polar angle. In Figs. 6A and B a central circular color element 28 is surround by a concentric annular color element 26. These two are rota-

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tionally symmetric. The outer color element 24 has an outer rectangular form with an inner circular form. In Figs. 7 and 8 the degree of symmetry is the same as for Fig. 6 as the color elements 24, 26, 28 are arranged symmetrically about the optical center 22 of the pixel structure independent of the orientation of the portion of the color element considered. In Figs. 7 and 8 the color elements have been arranged in a series of concentric areas, e.g. rings in Fig. 8 and rectangular annulae in Fig. 7. In Fig. 7 the area of the color elements vary with the polar angle, i.e. are non-rotationally symmetric. In Fig. 8 the area of any color element remains the same at any angle with respect to the optical center 22, i.e. the structure is perfectly rotationally symmetrical.

[0020] With respect to the arrangement of the electrodes for driving the color elements, the pixel structure of Fig. 5 is similar to the conventional structure but has two extra strips arranged in such a way that the color sequence across the pixel structure is symmetric, which increases the complexity of the electrode structure only slightly. However, the structures shown in Figs. 6 to 8 can cause major changes in the way the electrodes are contacted to each color element as some of the color elements can only be reached for electrical contact by crossing over other color elements. Due to the fact that there are only a limited number of materials which are sufficiently transparent and also conductive, the arrangement of the electrodes is not straight forward. In accordance with an aspect of the present invention, modifications may be made to the shapes of the color element areas to improve electrode accessibility. For example, the structure of Fig. 7 or 8 may be modified as shown schematically in Fig. 9 (for the structure of Fig. 8 only). In this structure access to the inner color elements 26 and/or 28 has been achieved by leaving gaps in the surrounding outer color elements 24 or 26 so that contact strips 248, 268, 288 may be connected to the relevant color element without having to cross over another color element. The disadvantage of this arrangement is that some of the symmetry has been lost.

[0021] A preferred pixel structure 20 is shown in Fig. 11 and will be explained with reference to Fig. 10. In Fig. 10 a schematic fixed format display is shown comprising an array of pixel structures which are addressed in logical rows and columns by means of row and column lines 29, 30 respectively. The display may be a tile of a larger tiled display. For example, the display may be a tile of a module which, when mounted with other modules forms a larger tiled array. It is understood that in the case of an OLED array, the lines 29 and 30 contact respective sides of layers of deposited organic material. By "logical rows and columns" is meant that each pixel structure can be addressed by applying electrical current to both a row line and a column line which cross at a pixel structure 32 to be addressed. However, the actual array of pixel structures need not be in rows and columns, it can be polar, for instance, i.e. radial and circumferential addressing. The word "logical" in the expression "logical rows and columns" means that the method of addressing is as if there were rows and columns of pixel structures but that the physical arrangement of pixel structures could be a different one. Hence, "logical rows and columns" relates to the topology and not necessarily the topography.

[0022] In order to address each one of the pixel structures individually it is necessary to provide both cathode and anode electrode strips 29, 30 which contact opposite sides of the organic material that emits the light in each color element of a pixel structure. Ideally, the arrangement of electrodes should be such that standard manufacturing techniques can be used, e.g. those developed for manufacture of semiconductor devices and other forms of displays such as Liquid Crystal Displays (LCD). Typical for these techniques is multilayer patterning using photoresists. General methods of lithographic patterning using photoresists may be found in the book entitled: "Microlithography" by J. R. Sheats and B. W. Smith, Marcel Dekker, 1998. General methods of deposition and etching of materials may be found in the book "The Science and Engineering of Microelectronics Fabrication", S. A. Campbell, Oxford, 2001.

[0023] The pixel structure 20 of Fig. 11 combines elements of the structures of Figs. 5 and 6 in an optimum way. It comprises a single central area for one color element 28. This central area is preferably circular but other shapes are possible such as square or hexagonal. The central area is preferably a block area rather than being divided into segments. A second color element 26 substantially surrounds the first color element 28 to form a color element substantially concentric with the first color element 28. It is made up of 2, optionally 4 sub-elements 261-264. Each sub-element 261-4 has the form of an approximate sector of an annulus, either approximately 180° of an annulus (not shown) or approximately 90° of an annulus. Again a substantially circular annulus is shown but other shapes are possible such as hexagonal or square. The third color element 24 substantially surrounds the second color element 26. It has an outer polygonal periphery, preferably a substantially rectangular periphery, preferably square, and an inner periphery, which is matched to the outer periphery of the second color element 26, e.g. a substantially circular, hexagonal or square periphery. It is made up of two sub-elements 241, 242 located symmetrically on either side of the pixel structure 20. Each sub-element is separated from at least one sub-element of another color element by means of a gap 23 which is an electrically isolating gap so that each element is electrically isolated from the others and each is individually contactable.

[0024] The first and central color element 28 has two elongate areas 281, 282 which extend away from the center 22 of the pixel structure 20 in opposite directions and terminate at a position co-located with the envelope of the outer periphery of the third color element 24. Each of the two or four sub-elements 261-264 of the second color element 26 has an elongate area 265-268 which

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extends generally away from the center 22 of the pixel structure 20 and runs parallel to one of the elongate areas 281, 282 of the first color element 28. Each of these elongate areas 265-268 terminates at a position co-located with the envelope of the outer periphery of the third color element 24. The shape of the pixel structure 20 is generally rectangular. Additionally, the quadratic area of the pixel structure is substantially filled up with light emitting sub-elements except for the isolating gaps 23. This is efficient on area when many such pixel structures are arranged in a Cartesian array on a transparent or an opaque substrate. This arrangement has also been found to be particularly easy to integrate into conventional thin-film processing techniques and provides a degree of symmetry for use with an optical element such as a lens having a size as large as or larger than the area of one pixel structure 20 and such as to reduce color shifts.

[0025] Fig. 12 shows a further embodiment of the present invention which at least partially solves the symmetry problem generated by use with an optical component or the tile edge effect and/or the mask vignetting effect. This pixel structure resembles the one of Fig. 4 but is rotated through an angle such as 45° and two more strips 23 and 29 have been added. The red sub-elements 23, 28, 29 are symmetrically arranged. To make the pixel structure symmetrical about the optical center 22 for the other color elements as described for the pixel structures of the previous embodiments it is necessary to arrange the size and distance of each color element form the center such that the optical centers of all the color element coincide at the optical center 22. Thus, the green sub-element 24 is further away from the optical center 22 but is smaller in size so that its effective weight is the same as the larger green sub-element 25 placed closer to the center 22. The additional characteristic is that the pixel presents all color elements to either edge 10, 12 of a tile. In this way any light which is reflected form the edge of the transparent or opaque substrate contains the same ratio of color elements as the complete pixel. Thus this pixel structure avoids color shifts at tile edges. Further, if rectangular or square holes are formed in a mask above each pixel structure vignetting effects do not change the color seen at different viewing angles as the area of the pixel structure blocked by vignetting always contains the same proportion of the primary colors emitted by the pixel structure. Further, each color sub-element is easily accessible for contacting.

[0026] Fig. 13 shows a cross-section through a pixel structure according to Fig. 5 arranged with a non-occluding mask 9 and an optical element such as a lens 11. The layer thicknesses and the size of the pixel structure has been exaggerated compared to other dimensions for clarity reasons. Lens 11 is large enough to cover the complete pixel structure and the use of microlenses has been avoided.

[0027] From the above description certain aspects of the present invention can be appreciated. First of all, the optical centers of the color elements of a multi-color OLED pixel structure substantially coincide to form a single optical center for the pixel structure. This means that for any local portion of a color element of a multi-color OLED pixel structure, there is an equal location portion or an equal luminosity local portion located at a diametrically opposite location with respect to the optical center of the pixel structure. With these pixel structures, emitted light strikes an optical element in equal portions on both sides of the optical axis thereof. In certain embodiments the color elements are arranged as a sequence of substantially concentric areas, whereby the word "substantially" means that a color element does not have to surround another color element completely.

[0028] The outer color of each pixel is at each point the same as the outer color of a pixel located on the other side of a mask portion or across a join in tiles. Whatever light is emitted from one pixel close to a tile edge that is refracted or reflected from the substrate edge to thereby change, modulate, increase or decrease the luminance and/or color from that pixel, an equal and opposite effect is generated in the pixel on the other side of a join between tiles. Thus, the total light combined from two pixels lying across the join between two tiles is the total from two pixels. If the eye resolves these two pixels into a single light unit, i.e. the distance between the two pixels is less than the acuity of the eye, then the two pixels appear to emit the correct light with the correct color and luminance. However, the present invention does not require that the display is viewed at such a distance that two pixels across a mask portion are resolved as a single light entity. Even when the eye can resolve each pixel, the present invention has advantages. The effect is then to maintain the color but to have a luminance difference between pixels located across a mask portion. This luminance difference is not associated with a color shift and therefore the disturbing effect is reduced.

[0029] The outer contour of the pixel structure is preferably rectangular more preferably square when the pixel structures are arranged in a Cartesian array of a plurality of such pixel structures. Where the array has a different symmetry, e.g. polar or hexagonal, the outer shape of the pixel structure may be adapted accordingly so that the pixel structures can be tiled easily and efficiently together.

[0030] Pixels having certain forms of symmetry as included within the scope of the present invention can have additional advantages for improving the viewing characteristics of a display which are in addition to improved convergence and lack of color shifts. In one aspect of the invention, the sub-elements of one particular color will be addressed at the same time. This can be done by either having separate electrical contacts on each, addressed at the same time or by electrically connecting the sub-elements such that a single electrical signal addresses both sub-elements at the same time.

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[0031] On the other hand, sub-elements can be addressed separately and used to create an additional virtual pixel with optical center in the middle between two or more pixels by simultaneously applying a current through sub-elements of neighboring pixels. Hence, sub-groups of sub-elements are addressed independently in each pixel structure. Since the central sub-element of a pixel cannot be split, a virtual pixel contains one color less but is still symmetric in at least the same directions as the real pixel. This is particularly effective when the central sub-element is highly saturated blue, since the human eye has a low detection capability for that color and does not contribute to resolution or sharpness experience.

[0032] To provide addressing of each pixel structure a drive circuit is preferably provided. this drive circuit is adapted to provide power to each pixel structure, to each pixel sub-element or to groups of sub-elements in accordance with the various embodiments of the present invention.

[0033] The present invention may be used with occluded or non-occluded masks. In the case of an occluded mask, it is preferred if concentric color elements are used. The emitted light that is obscured by one side of the mask as the viewing angle is changed is provided by a portion of the pixel structure diametrically opposite which becomes visible due to the change in viewing angle.

[0034] Fig. 14 shows how a passive matrix addressing can be obtained for a passive matrix with symmetrical pixels without increasing the number of addressing lines. In a conventional passive matrix arrangement, horizontally and vertically arranged anode and cathode lines, respectively, address a pixel as in Fig. 2. In total 4 lines are required for a pixel of Fig. 2, such as is shown in Fig. 15. Each pixel is addressed by two main electrodes, i.e. a cathode and an anode. A first main electrode comprises three transparent conductive columns 51, 52, 53, such as made from ITO, and the second main electrode is provided by a row electrode 50, usually a metal such as aluminum, in order to address each pixel. Separation between the individual elements of the main electrodes is usually done by means of insulating separators. The OLED device stack (Fig. 2) is deposited in-between the electrodes, where they intersect. When the pixel is made symmetric, e.g. using more sub-elements as shown for instance in Fig. 5, it is preferable to keep this number of address lines and not to increase it. One possible solution is demonstrated in Fig. 14a. The second main electrode line 404 covers the complete pixel area while on the other side of the pixel structure, three color emitting sub-elements are covered with pixel-local conducting, e.g. metal electrodes 412, 43, 421 of the same size. Further, pixel local conducting electrodes 422 and 411 have an extension in an L-shape. On top of these electrodes, an insulating material is deposited, with via's 405 through to the underlying electrodes. Conductive, addressing Lines 401, 402, 403 are then deposited, e.g. by metal deposition by sputtering or vapor deposition. By strategically positioning the via's 405 it is possible to contact the pixel-local electrodes 411, 412, 421, 422, 43 to the deposited first main electrode addressing lines 401, 402, 403. Additionally, this arrangement allows using at least the width of the pixel structure or more for creating the first main electrode addressing lines and thus greatly reducing the resistance, which allows increasing the number of addressable pixels in an array or increasing the currents for higher light output. Fig. 14b shows a cross-section of the arrangement through the pixel structure passing through one via 405 of the arrangement in Fig. 14a. The transparent row addressing electrodes 404 are deposited onto the transparent substrate 2. The OLED stacks 24, 26, 28, 27, 25 are deposited onto this electrode 404. Pixel-local electrodes 412, 422, 43, 421, 411 are deposited over the OLED stacks 24, 26, 28, 27, 25, respectively with insulating spacers 413 therebetween. Then an insulating layer 410 is deposited over the complete back of the display and vias opened to the pixel-local electrodes. Then three metal addressing electrodes 401, 402, 403 are deposited in such a way that the make contact with the pixel-local electrodes 412, 422, 43, 421, 411.

[0035] Another arrangement in accordance with an embodiment of the present invention is as shown in Fig. 16. This figure shows an electrode arrangement of the pixel demonstrated in Fig. 11. The sub-elements are addressable by addressing lines 511, 512, 521, 522, 530. On a second layer, the isolating gap 23 in the quarter segments of the intermediate pixel element 26 is bridged on either side by conductive strips 504. Then the addressing lines 511, 512; 521, 522 left and right of the center are electrically connected by conductive strips to pads 502 and 503, respectively. The central line 530 is connected to a further pad 501 by a conductive strip. In this embodiment, the addressing lines may be linked through larger contact pads 501-503, accessible from the rear of the display, for interconnection to a backplane. This is done to move the interconnection region of the electrodes to the electronics of a display away from the edges of a display array and reducing the required minimum seams between tiles for a tiled display. Also, this back interconnection method allows for redundant contact to pixel structures, increasing reliability and reducing the resistance of the addressing lines. Indeed, the resistance is no longer determined by the distance between the edge where the display is connected and a particular pixel, but the distance between the pixel and its nearest interconnection. In Fig. 17A the pads 501-3 of a display 411 are connected to a PCB 412 via conductive connections, e.g. by conductive adhesive or solder.

[0036] Instead of creating a second layer with electrode material, is also possible to address the pixels and its sub-elements through a back panel, connected to via's 405 as shown in Fig. 17B with a conductive material, e.g. a conductive adhesive as also is demonstrated

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in Fig. 17A. The number and diameter of via's 405 can be adapted to the current required for each sub-element.

[0037] It is to be understood that although preferred embodiments, specific constructions and configurations have been discussed herein for devices according to the present invention, various changes or modifications in form and detail may be made without departing from the scope and spirit of this invention.

Claims

1. A multicolor OLED pixel structure, comprising:

   a plurality of light emitting color elements, each color element emitting light of a particular color;
   the optical centers of the color elements coinciding substantially at an optical center for the pixel structure;
   any portion of a color element of the pixel structure having an equally luminous portion of the same color element located diametrically opposite thereto with respect to the optical center of the pixel structure.

2. The pixel structure of claim 1, wherein light from all the color elements adds to be able to form emitted white light.

3. The pixel structure of claim 1, wherein the outer shape of the pixel structure is polygonal, circular or rectangular.

4. The pixel structure of any of claims 1 to 3, wherein each one or more color elements which emit one color are arranged symmetrically about a line passing through the optical center.

5. The pixel structure according to claim 4 wherein each one or more color elements which emit one color are arranged symmetrically about a second line passing through the optical center which is perpendicular to the first line.

6. The pixel structure according to any previous claim, wherein the plurality of light emitting color elements comprise elements which emit light of one of three primary colors, and one or more color elements emitting one primary color are arranged substantially concentrically with respect to one or more color elements emitting another primary color.

7. The pixel structure according to any of the claims 1 to 5, wherein the plurality of light emitting color elements comprise rectangular elements arranged in a row.

8. The pixel structure according to any previous claim, wherein the pixel structure has light emitting area defined by an outer envelope and the plurality of light emitting color elements comprise elements which emit light of one of a number of primary colors, a light emitting element of each primary color extending to the outer envelope.

9. The pixel structure according to any previous claim, wherein the pixel structure is sandwiched between a first main electrode common to all light emitting color elements and a plurality of second electrodes, each second electrode contacting at least one of the light emitting color elements.

10. The pixel structure according to claim 9, wherein the pixel structure has a plurality of conducting areas local to each pixel for connection to an electrical power supply.

11. The pixel structure of claim 9 or 10, wherein a second electrode contacts at least two light emitting color elements of one color.

12. An array of pixel structures, each pixel structure being in accordance with one of the claims 1 to 11.

13. The array according to claim 12, further comprising a drive circuit for driving the pixel structures.

14. The array according to claim 13, wherein the drive circuit is adapted to drive each color element separately.

15. The array according to claim 13, wherein the drive circuit is adapted to drive a first group of color elements of a pixel structure independently of a second group of color elements of the same pixel.

16. The array according to any of the claims 13 to 15, wherein each pixel structure has a plurality of conducting areas local to each pixel for connection to an electrical power supply.

17. The array according to any of the claims 13 to 16, wherein each pixel structure has a plurality of conducting areas local to each pixel for connection to a PCB.

18. The array according to any of the claims 12 to 17, wherein the array has a display direction and further comprising an optical element located on the display direction side of the array.

19. The array according to claim 18, wherein the optical element is a vignetting element.

20. The array according to claim 18 or 19, wherein the

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optical element is a lens.

21. The array according to any of claims 18 to 20 further comprising a mask.

22. A passive or active matrix OLED display comprising an array according to any of the claims 12 to 21.

23. The passive or active matrix OLED display according to claim 22, wherein the display is a display tile.

24. A method of manufacture of a multicolor OLED pixel structure, comprising:

forming a plurality of light emitting color elements on a substrate, each color element being for emitting light of a particular color; the optical centers of the color elements coinciding substantially at an optical center for the pixel structure; any portion of a color element of the pixel structure having an equally luminous portion of the same color element located diametrically opposite thereto with respect to the optical center of the pixel structure.

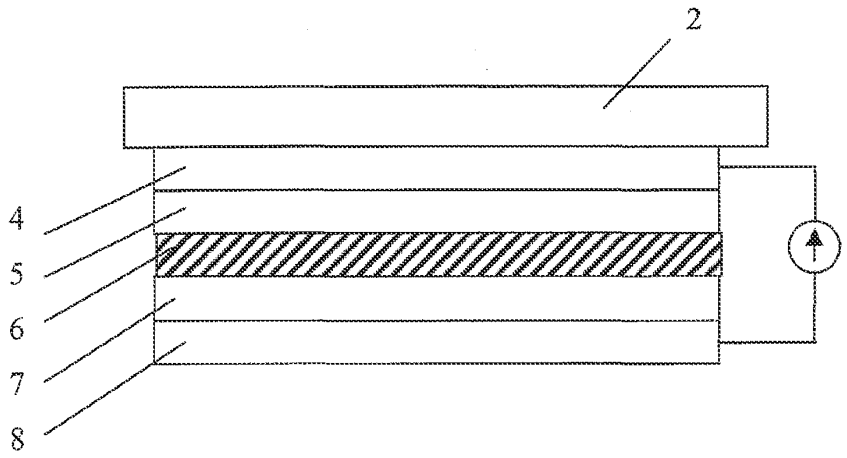


Fig. 1

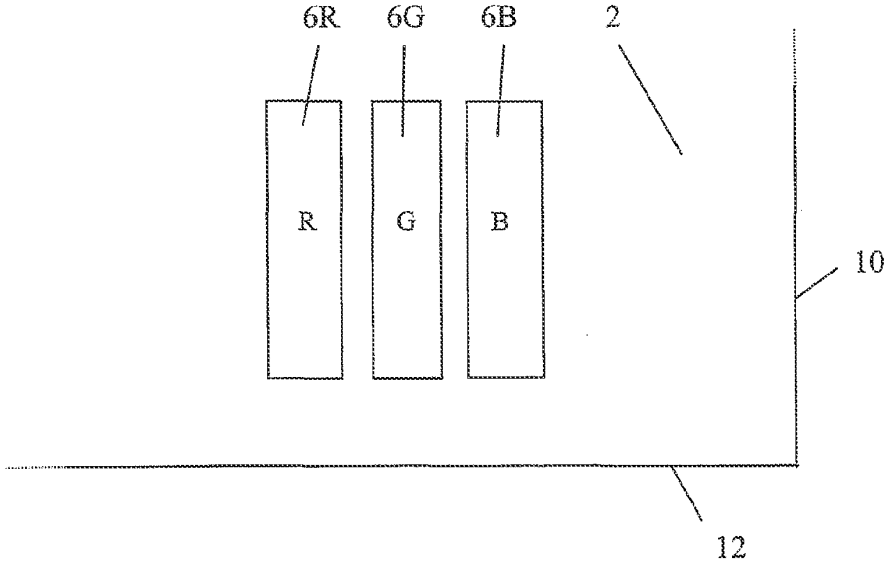


Fig. 2

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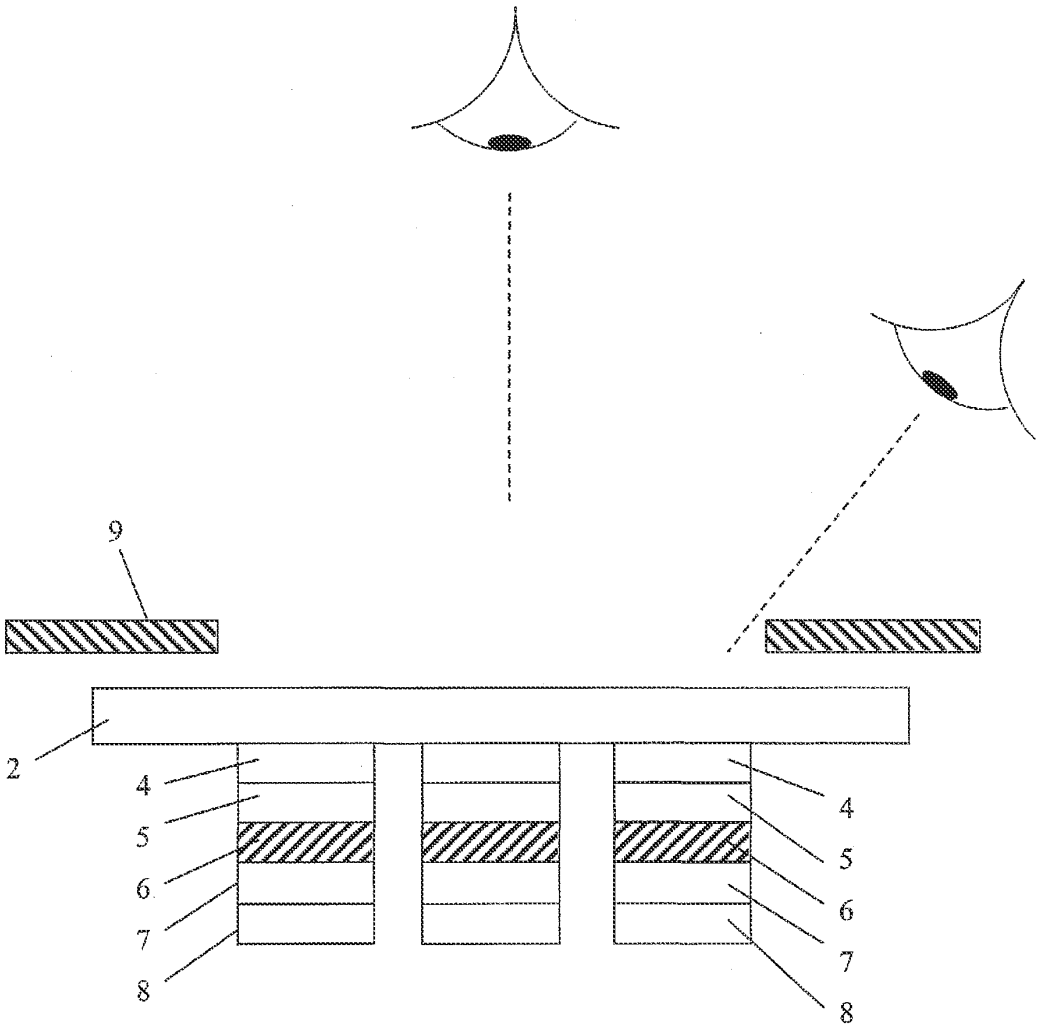


Fig. 3A

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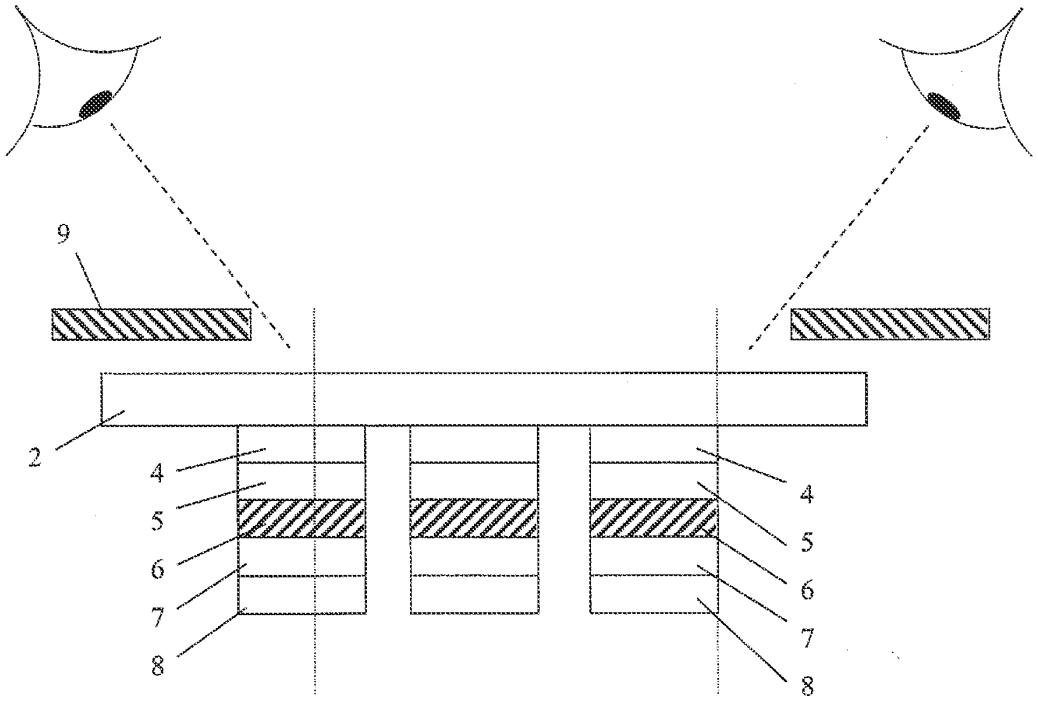


Fig. 3B

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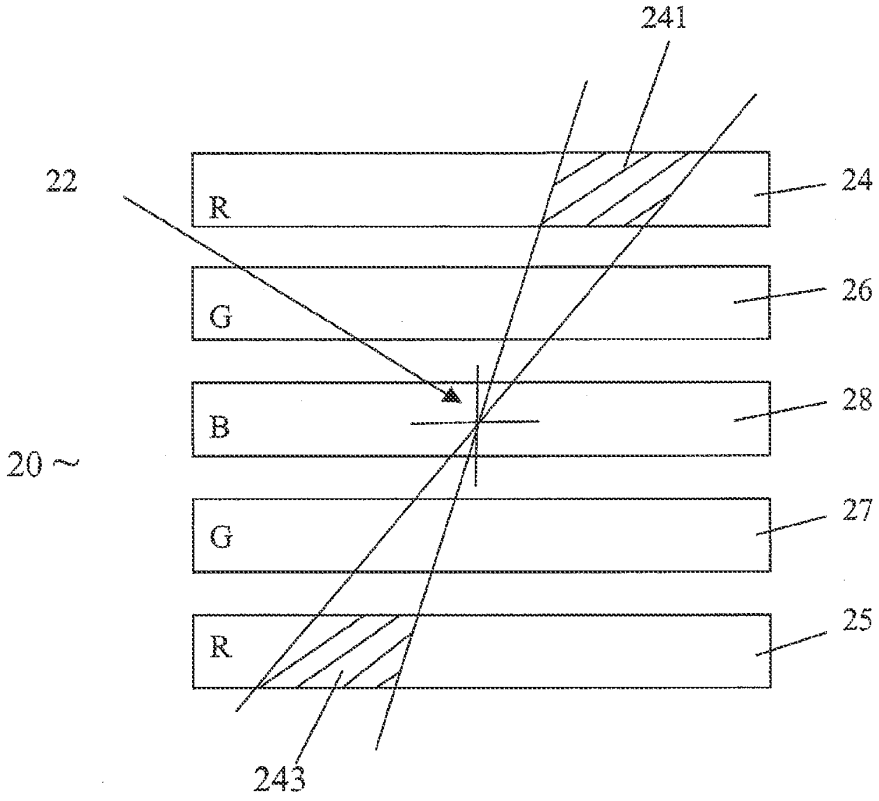


Fig. 4

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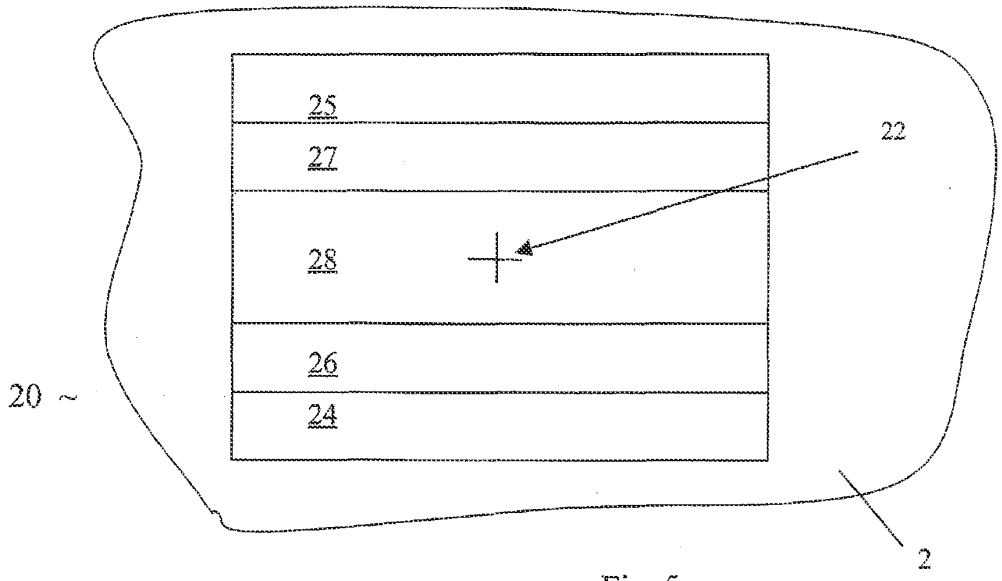


Fig. 5

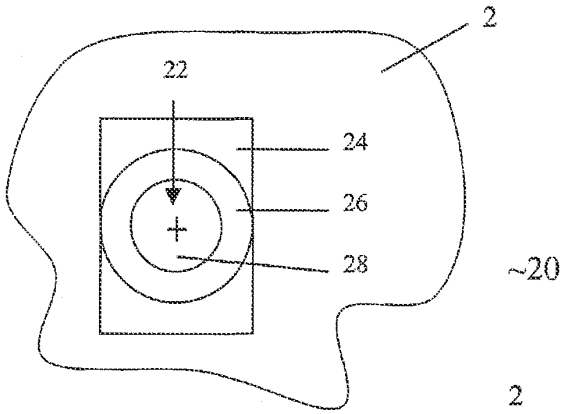


Fig. 6A

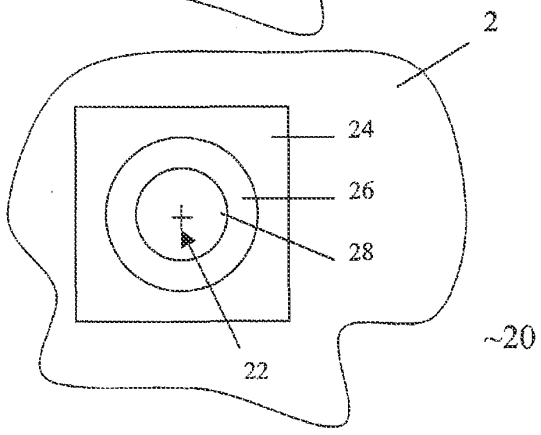


Fig. 6B

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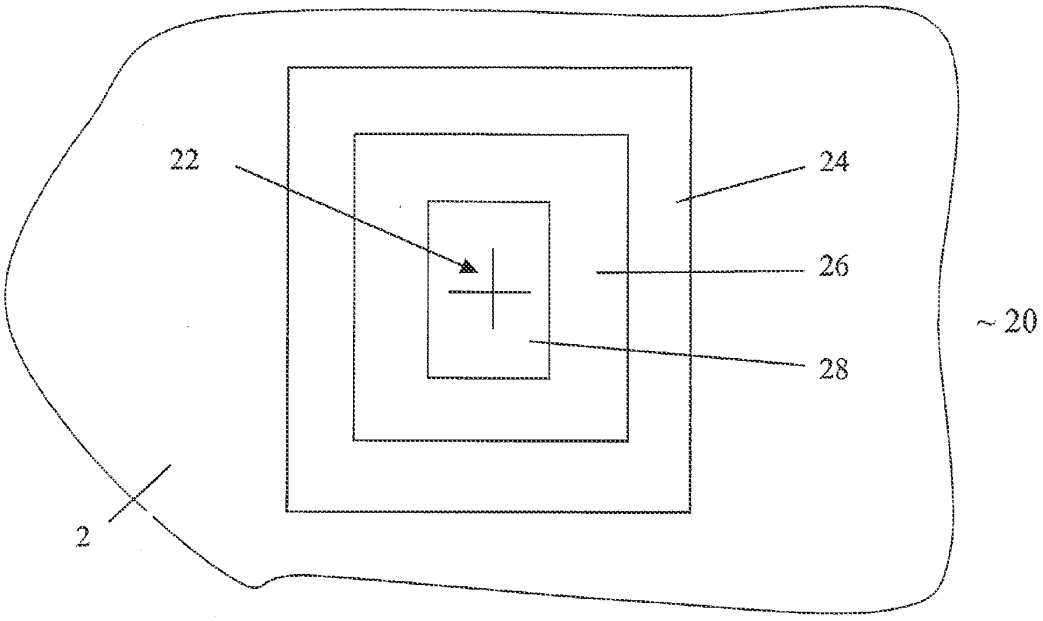


Fig. 7

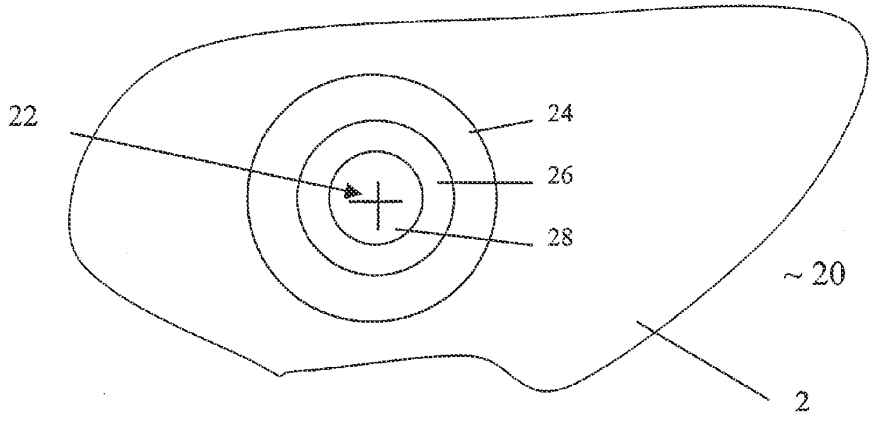


Fig. 8

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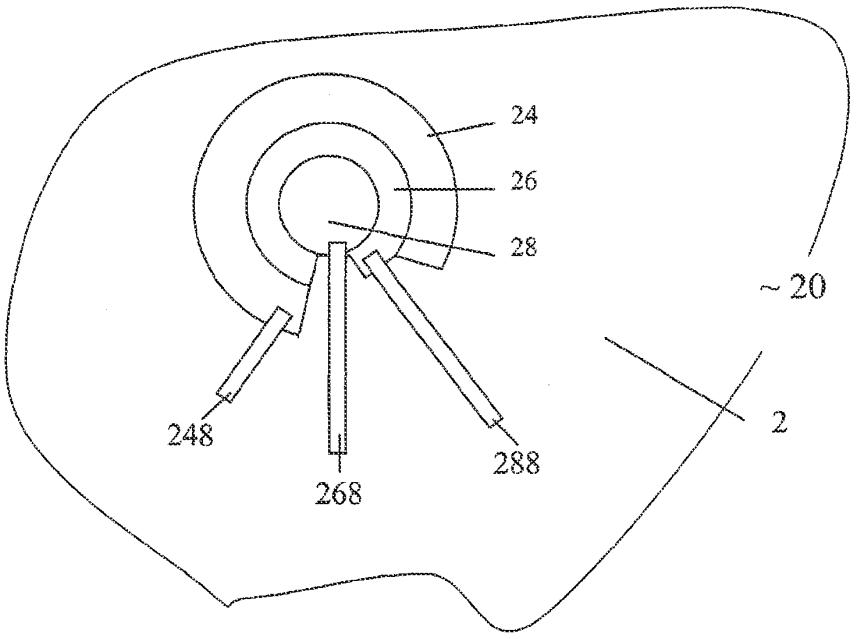


Fig. 9

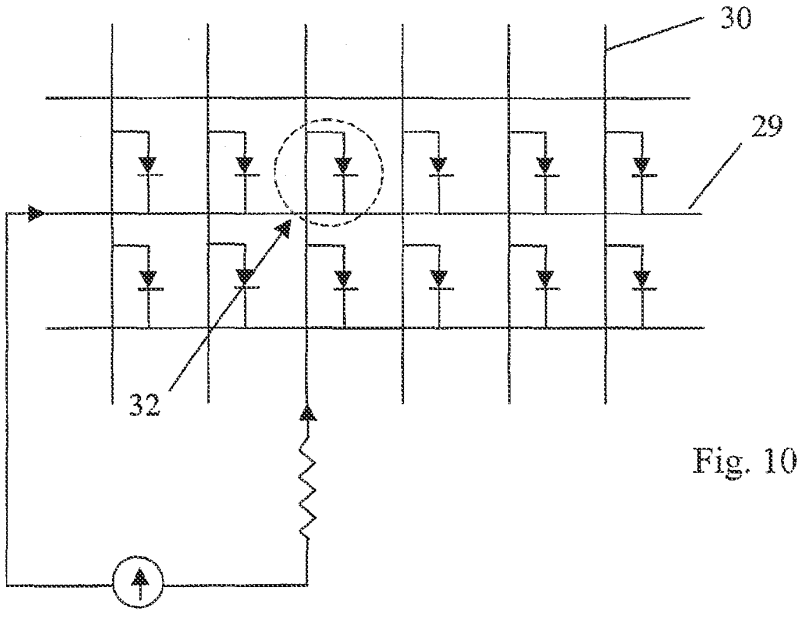


Fig. 10

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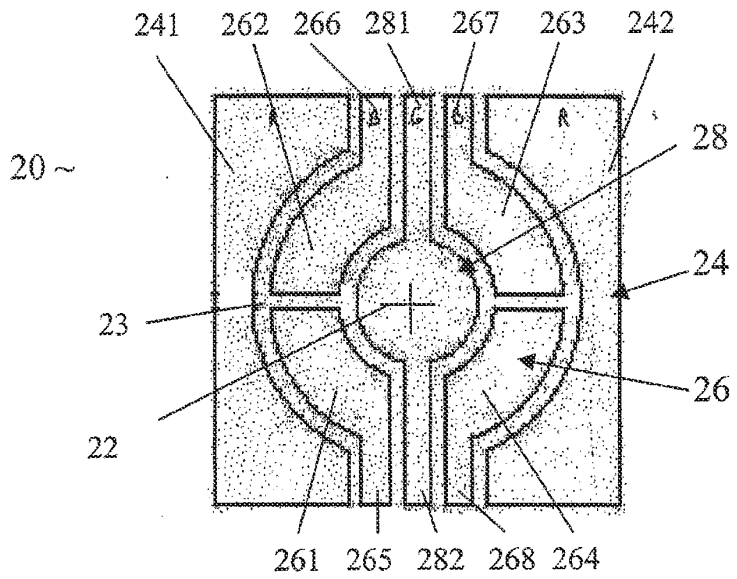


Fig. 11

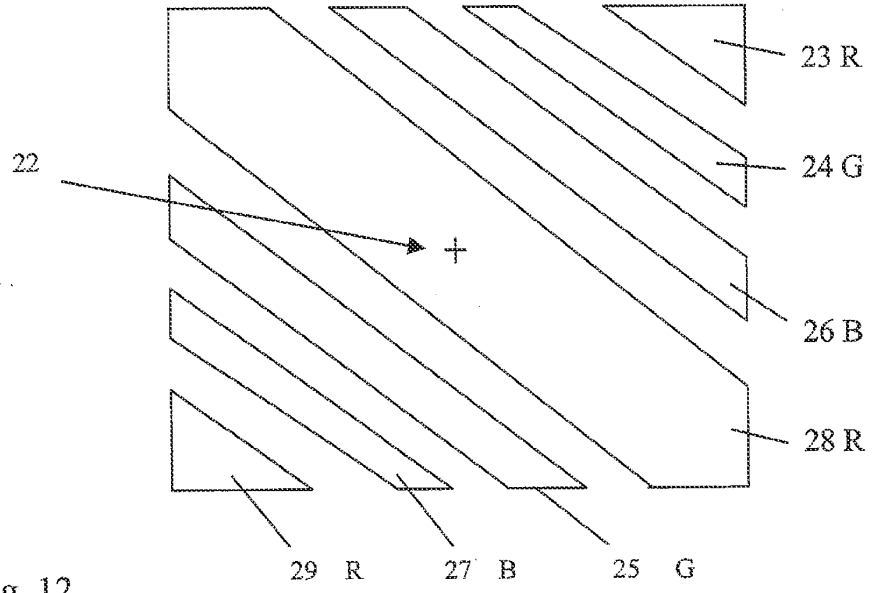


Fig. 12

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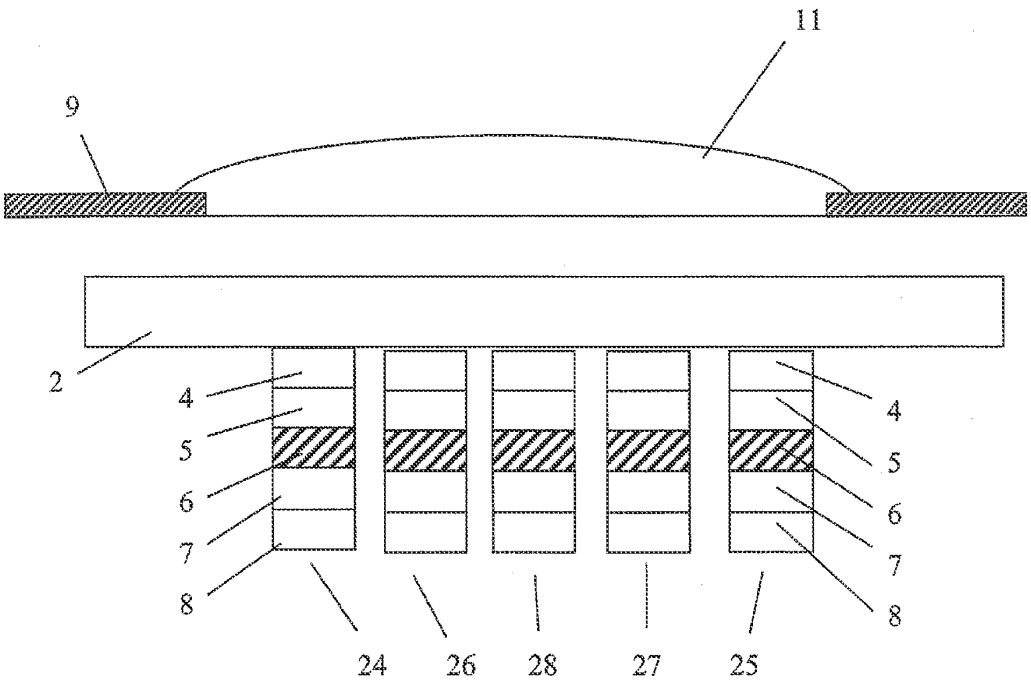


Fig. 13

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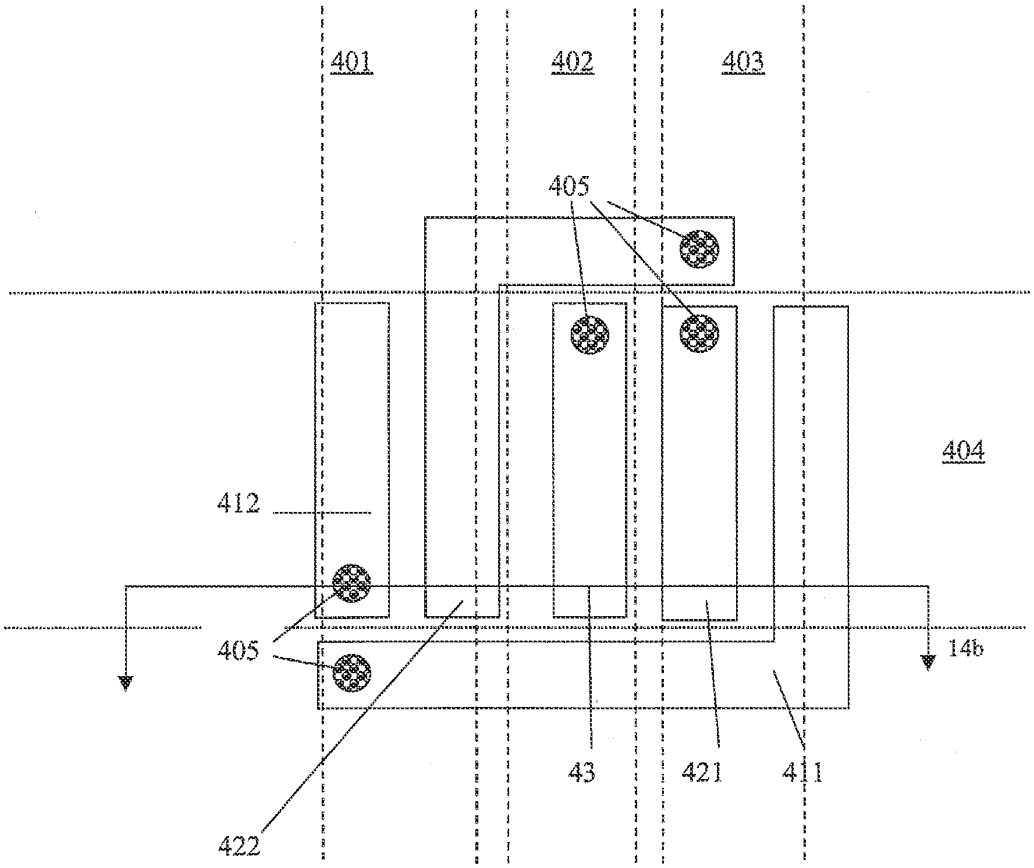


Fig. 14a

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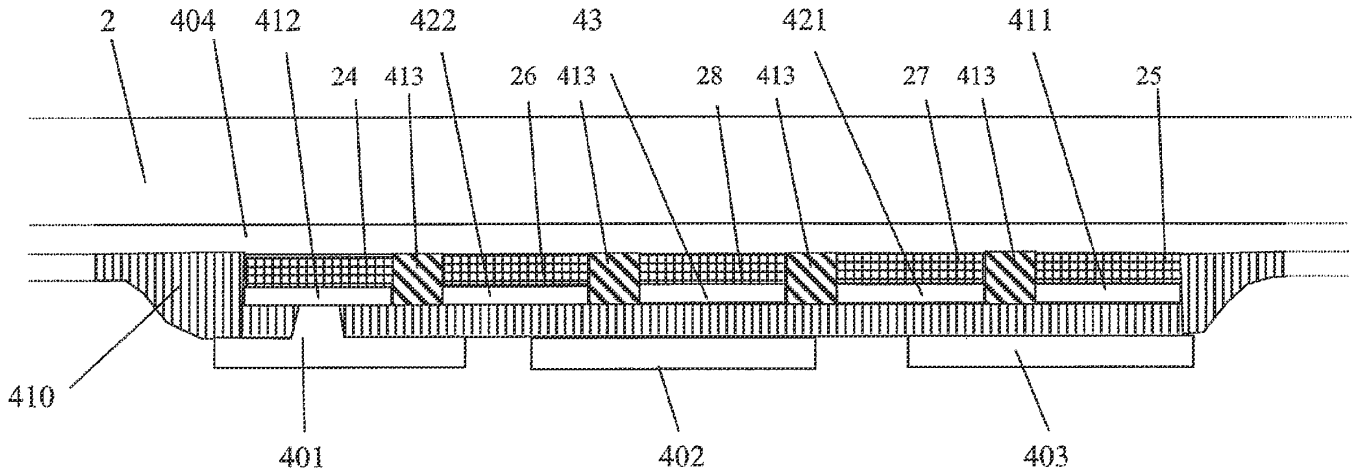

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Fig. 14b

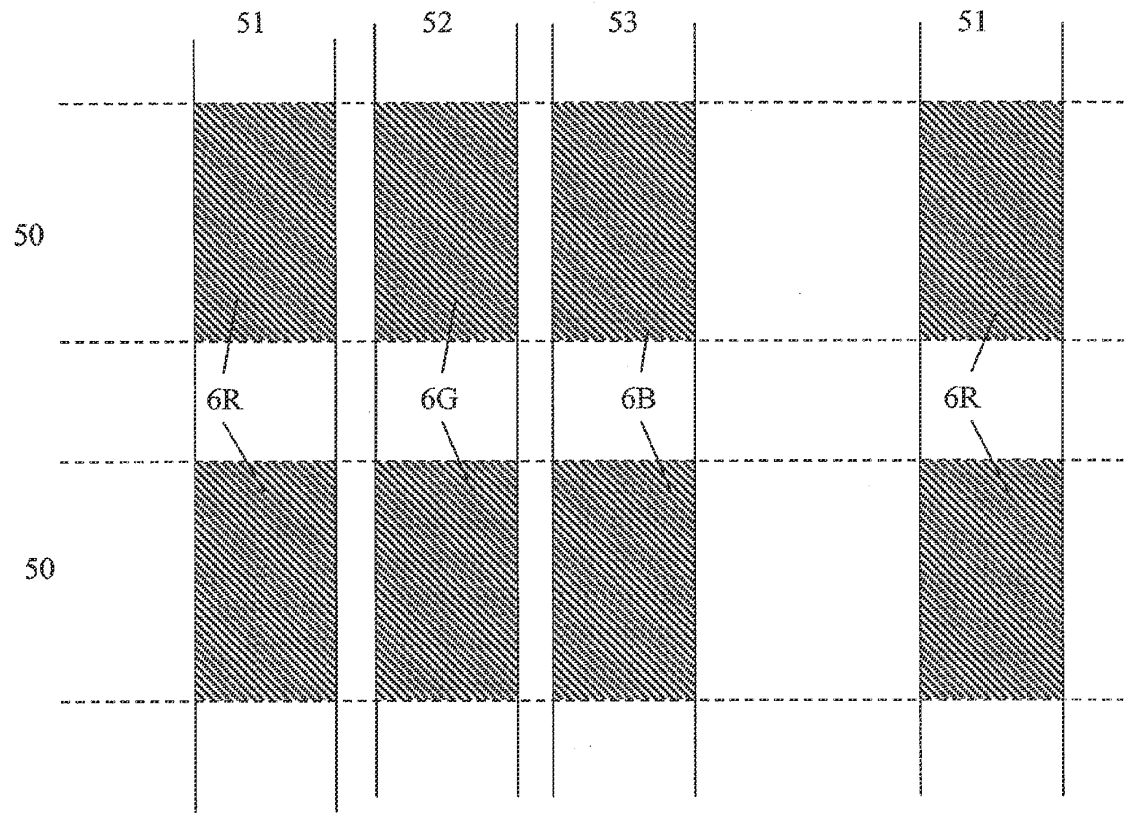


Fig. 15

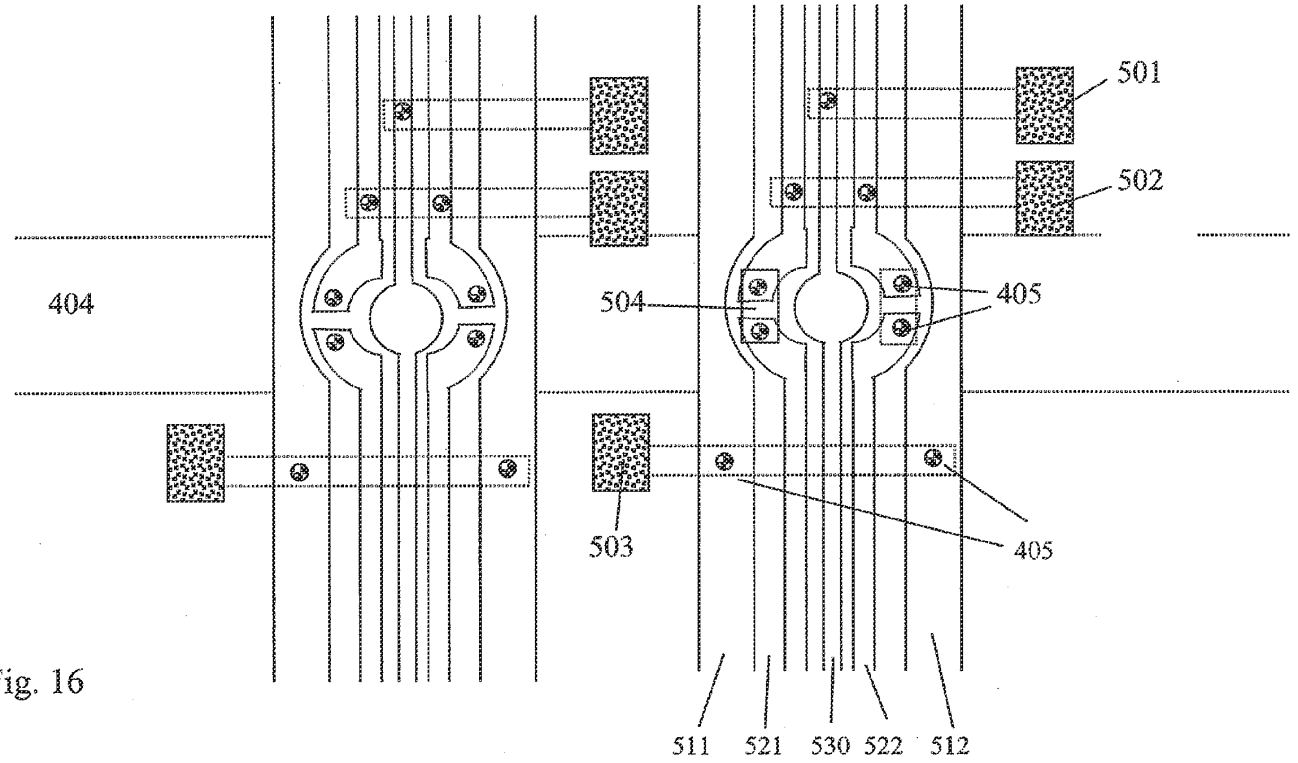


Fig. 16

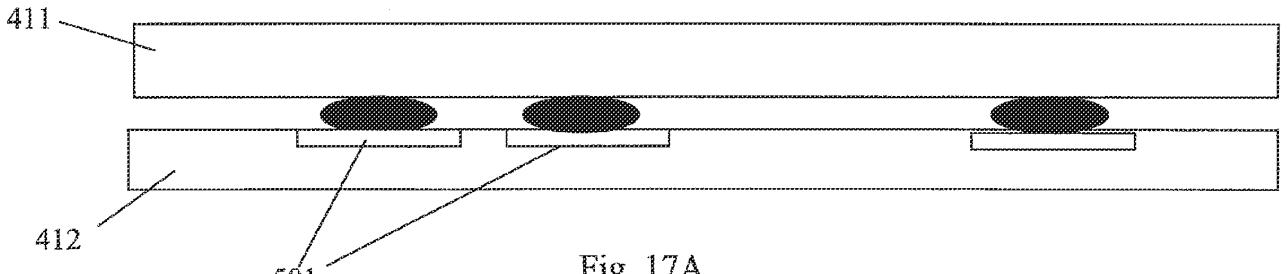


Fig. 17A

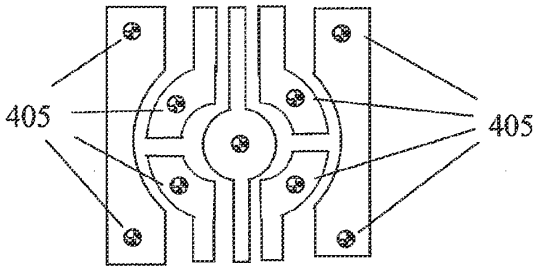


Fig. 17B

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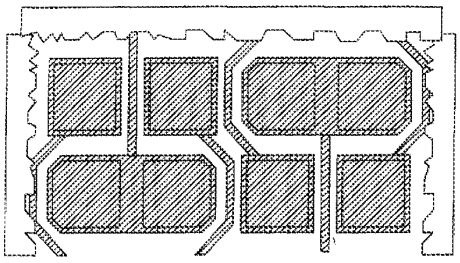
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(54) **Full color organic EL display panel, manufacturing method thereof and driving circuit thereof**

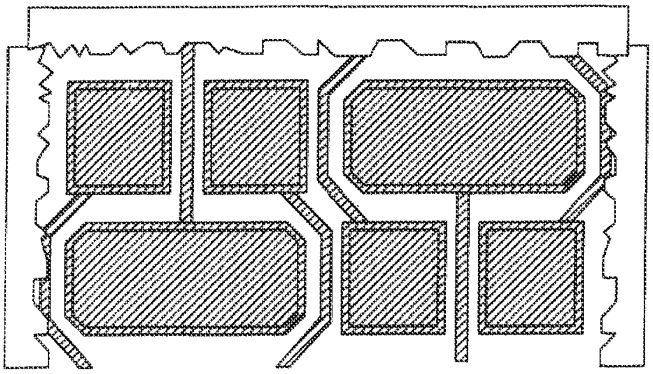
(57) Disclosed is a full color flat display panel by using an organic electro-luminescent(EL) device, a manufacturing method thereof and a driving circuit of the organic EL device, in particular, which includes first, second and third pixels, a plurality of first electrodes, and a plurality of second electrodes perpendicularly intersecting the first electrodes, in which each of the first, second and third light emitting pixels is arranged in each of intersecting positions of the first and second electrodes. Light emitting pixels are arranged to have different areas according to luminous efficiency so that a red light emitting area with relatively poorer efficiency is sized larger than a blue or green light emitting area thereby manufacturing an efficient full color organic EL display panel. Also, the influence from the line resistance in the anode lines and the cathode lines is reduced when a constant current is introduced into the device structured of the RGB array in order to realize the white light as full color. Thus, the voltage loss on the line resistance is prevented and the area ratio of the device is adjusted to make each of the RGB pixels for generating the white light have the similar value of drive voltage thereby minimizing power loss.

FIG. 6A



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FIG. 6B



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a full color flat display panel by using an organic electro-luminescent (EL) device, a manufacturing method thereof and a driving circuit of the organic EL device.

2. Description of the Related Art

[0002] Lately, the flat display industry has been remarkably developed. In particular, an organic EL array is gradually gaining interest as an image source in a direct display or a virtual display since the organic EL array can generate a relatively large amount of light and a display adopting the organic EL array can be used under various surrounding conditions.

[0003] In other words, the organic EL array can emit light in a sufficient amount so as to be used as the display under the various surrounding conditions ranging from those with no or little amount of light to those with sufficient amount of light.

[0004] Also, the organic EL array can be manufactured in a low price, and variously applied from a very small size of under 1 inch up to a considerably large size of tens of inches.

[0005] Further, the organic EL array provides a very wide range of view angle.

[0006] An example of the organic EL array as a small sized article is applied to portable electronic articles such as a pager, a cellular phone and a portable phone.

[0007] Such an organic EL device is comprised of a first electrode layer, an electron transporting layer, a light emitting layer, a hole transporting layer and a second electrode layer.

[0008] Here, light can be emitted in one or both directions of an electrode, and the most efficient EL device has one transparent electrode layer in a light emitting side.

[0009] Also, one the most widely used transparent electrodes is made of an indium-tin oxide(ITO), which is deposited on a transparent substrate such as a glass panel.

[0010] However, the major problem of the organic EL device is the connection capacitance, which includes the capacitance within the device composed of the material and the electrode and the capacitance from column and line electrodes in an array structure.

[0011] In other words, since the EL device is driven by a current unlike a liquid crystal display(LCD) which is driven by a voltage, an initially supplied current is used for charging the connection capacitance when the organic EL device is driven in the array structure.

[0012] Therefore, if the connection capacitance increases as the array increases or the device is enlarged, a larger amount of current should be supplied for the initial charge.

[0013] Also, the resistance of an anode line and a cathode line in the array structure gives a very important influence not only to response features of the device but also to the whole power.

[0014] In other words, a time for charging the capacitance or an RC time is influenced not only from the size of the capacitance but also to the resistance connected to the capacitance so that the response speed of the device is considerably influenced also as the resistance size of anode and cathode lines increases.

[0015] Further, the transparent electrode layer is made of a high resistive material thereby increasing such a problem.

[0016] Therefore, the connection capacitance and the electrode layer having high resistance of the organic EL device hinder producing the EL device in a large array structure.

[0017] In order to reduce such an influence, the anode and cathode lines can be made of a metal excellent in conductivity and low in resistance to reduce the line resistance in the anode and cathode lines thereby improving the response features of the device and simultaneously to reduce the voltage loss in the line resistance thereby lowering a drive voltage and reducing power consumption.

[0018] However, in a delta shaped array structure, such line resistance can be a more serious obstacle due to the fine cathode line. In other words, in a full color device structure, the voltage and current ratio among R, G and B pixels is 3:6:1 for expressing a white light. Therefore, the G(Green) pixel requires a smaller amount of voltage and current than the B(Blue) pixel in expressing the same value of luminance.

[0019] FIG. 1 shows a structure of RGB stripe-type pixels, and the current and voltage features in a, a' and a" positions of an A material which composes one of the RGB pixels and b, b' and b" positions of another B material which composes another one of the RGB pixels.

[0020] As can be seen in FIG. 1, the RGB pixels have their own physical properties different from one another so that the current-voltage features may be different in this case.

[0021] Referring to FIG. 1, the current-voltage features of the B material is better than those of the A material.

[0022] As an example, the A material can be regarded as the R(Red) pixel, and the B material can be regarded as the G or B pixel.

[0023] This can be varied according to the properties of materials, in which the A material can be regarded as having the poorest properties.

[0024] Also, referring the current-voltage features of each material, if the device has an array structure, there is a difference in the voltage-current features as in a, a' and a' and a" even in the same material due to the effect of line resistance observed along the anode line and

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along the cathode line.

[0025] The properties of the material like this increase the voltage applied to the line resistance of the anode and the cathode such as b, b' and b" and a, a' and a" to cause the increase of the drive voltage.

[0026] In particular, in the case of the A material (for the R pixels for example) which is poor in the current-voltage features, a higher current is required to obtain the white light thereby causing a voltage drop due to line resistance to be more serious.

[0027] Here, if the RGB pixels do not have their own power, the driver power should be determined according to a material having the poorest current-voltage features so that the drive voltage in another material having better current-voltage features is elevated thereby incurring overall power loss.

[0028] In driving the circuit in practice, the drive voltage is determined according to the pixel having the highest voltage. If the G light emitting pixels are assumed to have the luminance v. current features at least two times better than the R pixels, the drive voltage should be determined by the R pixel so that the drive voltage of the R pixels increases in respect to the G pixels thereby incurring power loss.

[0029] As a method of solving this case, the drive voltage is determined different for each of the RGB pixels to reduce power consumption.

[0030] However, when each of the RGB pixels is applied with a different voltage from one another, a reverse voltage should be applied to prevent crosstalk according to the features of the organic EL device. Here, the reverse voltage should be applied so that a positive voltage applied to the device does not exceed the threshold voltage.

[0031] Therefore, since the reverse voltage is applied according to the drive voltage of the R light emitting pixels if the R light emitting pixels have the highest drive voltage, the higher reverse voltage should be applied as the drive voltage of the R light emitting pixels is stepped up. So, many problems are caused in using the reverse voltage.

[0032] Meanwhile, FIG. 2A is a sectional view of the full color organic EL display device driven by the driving circuit of FIG. 1.

[0033] In manufacturing the organic EL display device, a shadow mask is used to form the RGB light emitting pixels having the optimal luminous efficiency as shown in FIG. 2A.

[0034] Also, the shadow mask as above is also used in a line method as shown in FIG. 2B, and in a method of arranging the pixels into a delta shape as shown in FIG. 2C.

[0035] In other words, as shown in FIG. 2A, anode lines 2-2 (only one is shown) are formed on a glass 1, and partitions 7 are formed before forming cathode lines in the organic EL display device. Then, red, green and blue emitting material layers 8-1, 8-2 and 8-3 are formed by using a shadow mask 9 followed by forming cathodes 10 for forming cathode lines in the front surface.

[0036] However, a cell array structure of the full color organic EL device of the related art described hereinbefore has the following problems:

[0037] In arranging the pixels according to the line method or the delta shape, the RGB light emitting pixels are sized almost the same so that the R pixel relatively poor in luminance and luminous efficiency is not properly expressed thereby degrading the texture.

[0038] Also, the opening ratio is lowered and ITO lines for connecting the light emitting pixels are thinned and elongated to increase resistance so that the uniformity across the screen is degraded and the drive voltage is elevated.

SUMMARY OF THE INVENTION

[0039] Embodiments of the present invention seek to address the foregoing problems of the related art. It would be desirable to provide a full color organic EL display panel and a manufacturing method thereof, in which, for the compensation of the low luminance of red, a red light emitting area is enlarged to upgrade the texture and elevate the opening ratio for increasing the efficiency of the device.

[0040] It would also be desirable to provide a full color EL display panel and a manufacturing method in which a shadow mask used for depositing red, green and blue organic EL layers can be used in common.

[0041] It would also be desirable to provide a full color EL display panel and a manufacturing method in which auxiliary electrodes are provided in a certain area of anode lines to reduce resistance thereby increasing the uniformity across a screen and lowering the drive voltage of the device.

[0042] It would also be desirable to provide a driving circuit of an organic EL device which can minimize the driving power of the organic EL device while improving response features of the organic EL device driven by using a current source.

[0043] It would also be desirable to provide a driving circuit of an organic EL device having an RGB array structure which rapidly controls the response features of the organic EL device by reducing effects of the line resistance in anode lines and cathode lines, adjusts the area ratio of the organic EL device to make the drive voltage of each of the RGB pixels similar to one another, and reduces the drive voltage to minimize power loss when constant current is applied to the organic EL device for realizing a white light.

[0044] According to an embodiment of the invention there is provided a full color organic EL display panel comprising: first, second and third pixels; a plurality of first electrodes; and a plurality of second electrodes perpendicularly intersecting the first electrodes; wherein each of the first, second and third light emitting pixels is arranged in each of intersecting positions of the first and second electrodes; wherein each of the first, second and

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third light emitting pixels has the area different from one another according to luminous efficiency.

[0045] It is preferred that each of the first light emitting pixels is arranged colinearly with each of the second light emitting pixels; wherein each of the third light emitting pixels is arranged between each of the first and second light emitting pixels to alternate with each of the first and second light emitting pixels.

[0046] The full color organic EL display panel further comprises auxiliary electrodes arranged at least around the first, second and third light emitting pixels and in portions of the first electrodes.

[0047] The full color organic EL display panel further comprises insulating layers, wherein each of the auxiliary electrodes is arranged at least one of around each of the first, second and third light emitting pixels and a central portion of each of the third light emitting pixel.

[0048] The full color organic EL display panel further comprises partitions arranged among the second electrodes for electrically insulating the second electrodes.

[0049] The full color organic EL display panel further comprises encapsulating plates for encapsulating organic EL layers arranged on the first, second and third light emitting pixels; and an encapsulating material for bonding the encapsulating plates to a substrate in non-light emitting areas.

[0050] It is preferred that the first electrodes have zigzag-shaped electrodes having partitions inclined at a certain angle for connecting between each of the first light emitting pixels and each of the second light emitting pixels, and stripe shaped electrodes for connecting between each of the third light emitting pixel.

[0051] It is also preferred that the partitions are arranged so as not to overlap with corner portions of the third light emitting pixels.

[0052] Also, it is preferred that the third light emitting pixels have the area larger than that of the first or second light emitting pixels.

[0053] Preferably, the first, second and third light emitting pixels have quadrangular structures which are the same or different from one another.

[0054] Preferably also, the first, second and third light emitting pixels are arranged into a delta structure.

[0055] Also preferably, the first electrodes are transparent; and wherein the second electrodes are made of metal.

[0056] According to another embodiment of the invention there is provided a method of manufacturing a full color organic El display panel which includes first, second and third pixels, a plurality of first electrodes, and a plurality of second electrodes perpendicularly intersecting the first electrodes, in which each of the first, second and third light emitting pixels is arranged in each of intersecting positions of the first and second electrodes, the method comprising the following steps of: (a) forming the first electrodes on a substrate, wherein the first electrodes include stripe-shaped electrodes for connecting between each of the third light emitting pixels, and zigzag-shaped electrodes having partitions inclined at a certain angle for connecting between each of the first light emitting pixels and each of the second light emitting pixels; (b) forming insulation partitions in areas excepting the light emitting pixels perpendicular to the first electrodes to insulate the first, second and third light emitting pixels; (c) forming organic EL layers on the first, second and third light emitting pixels for emitting lights corresponding to the light emitting pixels respectively; and (d) depositing an electrode material on the whole surface including the organic EL layers to form a plurality of second electrodes.

[0057] According to another embodiment of the invention there is provided a full color organic EL display panel comprising: a unit light emitting pixel having first, second and third pixels; a plurality of first electrodes; and a plurality of second electrodes perpendicularly intersecting the first electrodes; wherein each of the first, second and third light emitting pixels is arranged in each of intersecting positions of the first and second electrodes; wherein the unit light emitting pixel has sub-pixels divided along diagonal directions; and wherein each of the first, second and third light emitting pixels is arranged in each of the sub-pixels with an area different from one another according to the luminous efficiency of each of the first, second and third light emitting pixels.

[0058] It is preferred that the first light emitting pixel is positioned in a pair of the sub-pixels opposed along one diagonal direction; and wherein each of the second and third light emitting pixels is positioned in another pair of the sub-pixels opposed along another diagonal direction.

[0059] It is also preferred that the first light emitting pixel has the luminous efficiency lower than that of the second and third light emitting pixels.

[0060] Preferably, each of the first electrodes is formed under each of the first, second and third light emitting pixels and each of connected portions of the first, second and third light emitting pixels.

[0061] The full color organic EL display panel further comprises auxiliary electrodes formed on the first electrodes at the connected portions.

[0062] The full color organic EL display panel further comprises auxiliary electrodes formed in edge portions of the first, second and third light emitting pixels.

[0063] The full color organic EL display panel further comprises insulation layers formed in non-light emitting areas around the first, second and third light emitting pixels.

[0064] Also, the full color organic EL display panel further comprises insulation partitions formed among the second electrodes for electrically insulating the second electrodes.

[0065] It is preferred that the first electrodes are transparent lower electrodes; and wherein the second electrodes are upper electrodes made of metal.

[0066] According to still another embodiment of the invention there is provided a method of manufacturing

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a full color organic EL display panel which includes unit light emitting pixels having first, second and third pixels, a plurality of first electrodes, and a plurality of second electrodes perpendicularly intersecting the first electrodes, in which each of the first, second and third light emitting pixels is arranged in each of intersecting positions of the first and second electrodes, the method comprising the following steps of: (a) forming first electrodes on a substrate in a repeated pattern having a certain polygonal shape connected to stripe shape; (b) forming insulation partitions among the unit light emitting pixels adjacent to the first electrodes in the perpendicular direction; (c) forming organic EL layers on the first, second and third light emitting pixels for emitting lights corresponding to the first, second and third light emitting pixels respectively; and (d) depositing an electrode material on the whole surface including the organic EL layers to form a plurality of second electrodes.

[0067] According to other embodiment of the invention there is provided a driving circuit of a display device having anode and cathode lines, comprising: an anode circuit for outputting a different drive voltage for each of RGB light emitting pixels so as to correspond to the drive voltage varying according to the line resistance and the material features of the anode lines and the cathode lines; a cathode circuit connected to both ends of the cathode lines for outputting the same signals; and a display unit where the area ratio of each of the RGB light emitting pixels and the width of the anode lines are adjusted according to the features of the applied drive voltage.

[0068] It is preferred that the cathode circuit is arranged at the both sides of the cathode lines for applying the same signals to the display unit.

[0069] The light emitting pixels are composed into an array structure in which red, green and blue pixels have different areas according to luminous efficiency so that the luminous efficiency of the red pixel relatively poor in luminance and luminance efficiency can be enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0070] The above and other objects, features and other advantages of the present invention will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which

FIG. 1 shows a driving circuit of a device having a stripe-type array structure of the related art and the current v. voltage features of the circuit according to light emitting position.

FIG. 2A is a sectional view of a full color organic EL display device;

FIG. 2B is a plan view for showing a structure of an organic display device by using a line method of the related art;

FIG. 2C is a plan view for showing a structure of an organic display device by using a method of arranging pixels into a delta shape of the related art;

FIG. 3A to FIG. 3K are plan views for showing a process of manufacturing a full color EL display device according to a first embodiment of the invention;

FIG. 4 is a magnification of FIG. 3B;

FIG. 5 is a plan view for showing a shadow mask according to the first embodiment of the invention;

FIG. 6A and FIG. 6B are plan views for showing a completed full color organic EL display device according to the first embodiment of the invention;

FIG. 7 is a plan view for showing a connection structure of anode lines for connecting between light emitting pixels;

FIG. 8A to FIG. 8L are a plan view for showing a process for manufacturing a full color organic EL display device according to a second embodiment of the invention;

FIG. 9 shows a shadow mask according to the second embodiment of the invention;

FIG. 10 shows a driving circuit of an RGB device having an array structure according to a third embodiment of the invention;

FIG. 11 shows a driving circuit for reducing a voltage applied to the line resistance of cathodes in the structure of FIG. 10;

FIG. 12 shows a driving circuit for reducing power consumption by reducing a voltage applied to the line resistance of cathodes in the structure of FIG. 10; and

FIG. 13 shows alternative embodiment of the driving circuit shown in FIG. 12.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0071] Preferred embodiments of a full color organic EL display panel will be described in reference to the appended drawings as follows:

[0072] The full color organic EL display panel and a manufacturing method thereof will be described as divided in the first, the second and the third embodiments, and a driving circuit for the organic EL display device will be described in the third embodiment.

First Embodiment

[0073] FIG. 3A to FIG. 3K are plan views for showing a process of manufacturing a full color EL display device according to a first embodiment of the invention.

[0074] As shown in FIG. 3A, a pattern of anode lines 102-2 is formed on a glass 101 by using ITO or other transparent electrodes. Here, light emitting pixels 102-1 are formed into the shape of a polygon with at least three angles, and have the area for emitting a red light larger than that for emitting blue and green lights. Half of the area of the light emitting pixels 102-1 is arranged for red,

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and the other area is arranged for blue and green. Another pattern of anode lines is also formed under light emitting pixels 102-1.

[0075] Then, as shown in FIG. 3B, auxiliary electrodes 105 are formed in anode lines 102-2 which connect the light emitting pixels 102-1, in order to reduce the resistance of the anode lines 102-2. When the auxiliary electrodes 104 are provided around the light emitting pixels 102-1 also, the resistance can be further reduced than provided only in the anode lines 102-2.

[0076] FIG. 4 is a partial magnification of FIG. 3B, in which it can be seen that the auxiliary electrodes 104 and 105 are formed both around the light emitting pixels 102-1 and in the anode lines 102-2 for connecting the light emitting pixels 102-1. Here, a material used for the auxiliary electrodes 104 and 105 includes a metal such as Cr, Al, Cu, W, Au, Ni, Ag and the like which has relatively smaller resistance than ITO.

[0077] Then, an insulating layer 106 is formed as shown in FIG. 3C. Here, the insulating layer 106 is made of an organic or inorganic insulator. The inorganic insulator includes oxide, nitride. Also, those spinably molten to solvents are available also. Polymers are preferred for the organic substance, and photo-resist, polyimide and polyolenfin are more preferred.

[0078] Then, as shown in FIG. 3D, partitions 107 are formed for the insulation among cathodes which will be formed later.

[0079] In sequence, as shown in FIG. 3E, red, green and blue common organic EL layers or common organic EL layers 108 are deposited at a single time by using a blank mask capable of performing deposition on the whole light emitting area.

[0080] Then, a shadow mask 109 shown in FIG. 5 is used to deposit red light emitting material layers 108-1 which are organic EL layers for emitting the red lights as shown in FIG. 3F and FIG. 3G. Also, in the same manner as in the red light emitting material layers, the shadow mask 109 is used to deposit green and blue light emitting material layers 108-2 and 108-3 for generating green and blue lights shown in FIG. 3H and FIG. 3I.

[0081] Here, instead of depositing the common organic EL layers 108 in the whole light emitting area, the common organic EL layers 108 can be formed in each of the RGB pixels by using the single shadow mask 109 shown in FIG. 5 while moving the same.

[0082] Then, as shown in FIG. 3J a metal layer for forming the cathode 110 is formed by using a Mg-Ag alloy, Al or other conductive materials.

[0083] Then, as shown in FIG. 3K, a protective layer such as an oxygen absorbing layer, a moisture absorbing layer and a moisture proof layer is formed, and encapsulation is performed by using encapsulating materials 111 and encapsulating plates 112 to complete the device.

[0084] FIG. 6A and FIG. 6B are plan views for showing the completed device.

[0085] Positions for the deposition of red, green and blue can be located to have a triangular structure and a reverse triangular structure as shown in FIG. 6A and FIG. 6B.

[0086] Here, in the formation of red, green and blue by using the single shadow mask 109, the red light emitting pixels 102-1 are halved by using the insulating layer 106. When a red-dedicated shadow mask 109 is used, the light emitting pixels are formed without being halved as shown in FIG. 6B.

[0087] FIG. 7 is a magnification of the anode lines 102-2 for connecting between the green light emitting pixels 102-1 and the blue light emitting pixels 102-1, and the light emitting pixels 102-1 of the anode lines 102-2 for connecting between the red light emitting pixels 102-1 for showing the minimization of the area of the light emitting pixels 102-1.

[0088] Basically, the anode lines 102-2 for connecting between each of the green light emitting pixels 102-1 and each of the blue light emitting pixels 102-1 should be formed on a straight line A, formed as inclined as in B in portions where two anode lines 102-2 overlap with each other, and formed as inclined as in C also in corners of the red light emitting pixels 102-1 formed beside the two anode lines 102-2. Thus, the size of the red light emitting pixels 102-1 can be maximized.

Second Embodiment

[0089] FIG. 8A to FIG. 8L are a plan view for showing a process for manufacturing a full color organic EL display device according to a second embodiment of the invention.

[0090] First, as shown in FIG. 8A, patterns of anode lines 202-1 and 202-2 are formed on a glass 201 with ITO or other transparent electrodes. The anode lines 202-1 and 202-2 are patterned into the above shape so that each unit of light emitting pixels 202-3 is divided along diagonal directions into four sub-pixels 202-4 shaped as a triangle with smooth corners. The unit light emitting pixel 202-3 comprised of the sub-pixels 202-4 is provided with light emitting material layers for emitting red, green and blue lights.

[0091] In the sub-pixels 202-4 structured as above, a pair of sub-pixels opposed in the diagonal direction applied with red light emitting material layers which will emit low red lights with relatively low luminous efficiency, and another pair of sub-pixels are applied with blue and green light emitting material layers to emit blue and green lights.

[0092] Then, as shown in FIG. 8B, auxiliary electrodes 205 are formed to reduce the resistance of the anode lines 202-2 at portions connecting the light emitting pixel.

[0093] In sequence, as shown in FIG. 8C, when edge portions of each of the light emitting pixels are provided with auxiliary electrodes 204 also, the resistance can be further reduced compared to when the auxiliary electrodes are provided only in the anode lines 202-2 for

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connecting between each of the light emitting pixels.

[0094] Materials available for the auxiliary electrodes 204 and 205 include metals such as Cr, Al, Cu, W, Au, Ni, Ag and the like which have relatively small resistance than ITO.

[0095] As shown in FIG. 8D, an insulating layer 206 is formed to cover anode taps 203-1.

[0096] The insulating layer 206 can be halved by using the red light emitting sub-pixels.

[0097] The insulating layer is formed around the light emitting pixels including the anode taps 203-1 where light is not emitted. The insulating layer 206 is made of an organic or inorganic insulator. The inorganic insulator includes oxide, nitride. Also, those spinably molten to solvents are available also. Polymers are preferred for the organic substance, and photo-resist, polyimide and polyolenfin are more preferred.

[0098] Then, as shown in FIG. 8E, insulating partitions 207 are formed for the insulation among cathodes which will be formed later.

[0099] Next, as shown in FIG. 8F, red, green and blue common organic EL layers or common organic EL layers 208 are deposited at a single time by using a blank mask capable of performing deposition on the whole light emitting area.

[0100] Then, a shadow mask 209 shown in FIG. 9 is used to deposit red light emitting material layers 208-1 which are organic EL layers for emitting the red lights as shown in FIG. 8G and FIG. 8H. In forming light emitting pixels arranged in the upper part as shown in FIG. 8H, the shadow mask 209 is rotated 180°. Alternatively, a shadow mask having triangular holes formed in the upper and lower parts can be used also.

[0101] Then, in the same manner as in the red light emitting material layers, the shadow mask 209 is used to deposit green and blue light emitting material layers 208-2 and 208-3 for generating green and blue lights shown in FIG. 8I and FIG. 8J. Each of the light emitting material layers 208-2 and 208-3 is formed in each of the green and blue sub-pixels by rotating the shadow mask 209 or using another mask.

[0102] Here, instead of depositing the common organic EL layers 208 in the whole light emitting area, the common organic EL layers 208 can be formed in each of the RGB sub-pixels by using the single shadow mask 109 shown in FIG. 9.

[0103] Then, as shown in FIG. 8K, a metal layer for forming the cathode lines 210 is formed by using a Mg-Ag alloy, Al or other conductive materials.

[0104] Then, as shown in FIG. 8L, a protective layer such as an oxygen absorbing layer, a moisture absorbing layer and a moisture proof cover is formed, and encapsulation is performed by using encapsulating materials 211 and encapsulating plates 212 to complete the device.

Third Embodiment

[0105] FIG. 10 shows a driving circuit for an organic EL device having an array structure according to a third embodiment of the invention.

[0106] Referring to FIG. 10, the driving circuit is comprised of an anode circuit 301 for applying a certain drive voltage to each of light emitting RGB pixels, a cathode circuit 302 for outputting scan signals to the cathode lines with both ends of cathode lines being connected in a circuit, and a display unit 303 for being displayed by data signals and the scan signals through the adjustment of the area ratio of each of the RGB light emitting pixels and the width of the anode lines according to the features of a drive voltage applied to each of the light emitting RGB pixels.

[0107] Hereinafter, the current driven organic EL device of the invention as shown in FIG. 10 will be compared with the EL device of the related art as shown in FIG. 1.

[0108] If the different value of drive voltage is outputted from the anode circuit 10 for each of the RGB pixels as in the circuit of the related art in FIG. 1, power consumption can be reduced a little since it should be considered only about power consumption according to the supply voltage of each of the RGB pixels.

[0109] In this case, however, when the reverse voltage is applied for preventing crosstalk which can occur due to the properties of the organic EL device, the reverse voltage should be based upon the A material with the highest drive voltage so that the voltage applied to the A material in the array structure may not exceed threshold voltage. Thus, as a problem, the higher the drive voltage of the A material, the higher reverse voltage is required.

[0110] Therefore, the circuit of the invention, as shown in FIG. 10, can adjust the area ratio of each of the RGB light emitting pixels and the width of the anode lines for emitting a white light under each of the drive voltages which are as similar as possible so that the overall maximum drive voltage can be lowered to reduce power consumption and the reverse voltage for preventing crosstalk can be lowered also.

[0111] To be more specific, if the A material requires the highest voltage for emitting the white light, the area of the A light emitting pixels is enlarged to lower the drive voltage of the A material thereby reducing the overall drive voltage.

[0112] Also, as the area is increased and thus the line width of the A material is increased at the cathode side, the line resistance is reduced and thus the voltage applied to the anode line resistance is reduced also.

[0113] Meanwhile, other materials have better current v. voltage features than the A material and thus require less amount of current for emitting the white light. so, the area can be reduced and the voltage loss in line resistance can be reduced.

[0114] The area ratio of each of the RGB light emitting

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pixels and the width of the anode lines are adjusted like this, the line resistance and the drive voltage may be reduced.

[0115] FIG. 11 shows a driving circuit for reducing the voltage applied to the line resistance of the cathodes in the structure of FIG. 10.

[0116] Referring to FIG. 11, the driving circuit is comprised of an anode circuit 401 for outputting a different drive voltage for each of the RGB pixels so as to correspond to the drive voltage varying according to the line resistance and the material features of the anode lines and the cathode lines, a cathode circuit 402 having both ends of the cathode lines being connected for outputting the same signals to the both ends, and a display unit 403 composed of the RGB light emitting pixels with a certain size ratio and the anode lines and being displayed by applied data and scan signals.

[0117] Hereinafter, the current driven organic EL device of the invention as shown in FIG. 11 will be compared with the EL device of the related art as shown in FIG. 1.

[0118] According to the array structure of the related art shown in FIG. 1, the current of each of the RGB pixels, which flows through the anodes of the light emitting pixels, flows through the cathodes incurring voltage step-up due to the line resistance of cathodes.

[0119] When the light emitting pixels need larger amount of current to obtain higher luminance, the magnitude of voltage applied to the cathode line resistance will increase more.

[0120] Here, if one cathode line is connected with the cathode circuit 20 at only one terminal, one cathode line adjacently connected with the cathode circuit 20 and another cathode line remotely connected with the cathode circuit 20 have line resistance different from each other.

[0121] In other words, the line resistance applied to portions of the RGB light emitting pixels remote from the cathode circuit 20 is enlarged.

[0122] In order to solve such problems, one end of each of the cathode lines is bound with the other end in driving the circuit, the voltage applied to the cathode line resistance can be halved.

[0123] In other words, the voltage is the highest in the center of each of the cathode lines and lowers as approaches the both ends thereof. So, comparing with the circuit as shown in FIG. 1 where the current flows from one end of each of the cathode lines to the other end thereof, the voltage applied to the line resistance of the cathode lines shown in FIG. 11 can be halved if the same current flows through the cathode lines in FIG. 11 and those in FIG. 1.

[0124] FIG. 12 shows a driving circuit in which both ends of each of cathode lines are bound as in FIG. 11 to prevent the voltage step-up shown in the structure of FIG. 10. The circuit is comprised of an anode circuit 501 for outputting a different drive voltage for each of the RGB pixels so as to correspond to the drive voltage varying according to the line resistance and the material features of the anode lines and the cathode lines, a cathode circuit 502 for outputting scan signals to the cathode lines with both ends connected in a circuit, and a display unit 503 for being displayed by data signals and the scan signals through the adjustment of the area ratio of each of the RGB light emitting pixels and the width of the anode lines according to the features of a drive voltage applied to each of the light emitting RGB pixels.

[0125] FIG. 13 shows a driving circuit according to another embodiment of the invention. The driving circuit is comprised of an anode circuit 601 for outputting a different drive voltage for each of the RGB pixels so as to correspond to the drive voltage varying according to the line resistance and the material features of the anode lines and the cathode lines, cathode circuits 602 and 602' arranged at both ends of cathode lines for outputting scan signals to the both ends of the cathode lines, and a display unit 603 for being displayed by data signals and the scan signals through the adjustment of the area ratio of each of the RGB light emitting pixels and the width of the anode lines according to the features of a drive voltage applied to each of the light emitting RGB pixels.

[0126] Considering the difference between FIG. 13 and FIG. 12, the both ends of the cathode lines are bound in applying the scan signals to the both ends of the cathode lines in FIG. 12, and the two cathode circuits are provided to apply the scan signals to the both ends of the cathode lines thereby preventing the voltage step-up due to the current in the cathode lines in FIG. 13.

[0127] Since specific features of FIG. 12 and FIG. 13 can be understood through the description of FIG. 10 and FIG. 11, the specific description thereof will be omitted.

[0128] Meanwhile, the driving circuits of the organic EL device shown in FIG. 10 to FIG. 13 can be adopted to all types of display devices which are powered with electricity.

[0129] As described hereinbefore, the full color organic EL display device, the manufacturing method thereof, and the driving circuit of the organic EL display device embodying the invention have the following effects:

[0130] First, in manufacturing the full color organic EL device, in order to compensate the disadvantage of the red light emitting pixels with the relatively lower luminous efficiency, the red light emitting pixels are sized larger than the green light emitting pixels and the blue light emitting pixels to enhance the luminous efficiency of the red light emitting pixels. Thus, the texture and the opening ratio can be enhanced to raise the efficiency of the device.

[0131] Second, the single shadow mask can be used in depositing the RGB organic EL layers.

[0132] Third, the auxiliary electrodes with low resistance are provided in certain portions of the cathode stripes to reduce resistance so that the uniformity across the screen can be enhanced and the drive voltage of the device can be reduced.

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[0133] Fourth, the influence from the line resistance in the anode lines and the cathode lines is reduced when a constant current is introduced into the device structured of the RGB array in order to realize the white light as full color. Thus, the voltage loss on the line resistance is prevented and the area ratio of the device is adjusted to make each of the RGB pixels for generating the white light have the similar value of drive voltage thereby minimizing power loss.

[0134] Throughout the foregoing description, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope of the invention. Therefore, the technical scope of the invention is not restricted to the description of the foregoing embodiments but will be defined by those disclosed in the accompanying claims.

Claims

1. A full color organic EL display panel comprising:

   first, second and third pixels;
   a plurality of first electrodes; and
   a plurality of second electrodes perpendicularly intersecting said first electrodes;

   wherein each of said first, second and third light emitting pixels is arranged in each of intersecting positions of said first and second electrodes;
   wherein each of said first, second and third light emitting pixels has the area different from one another according to luminous efficiency.

2. A full color organic EL display panel according to claim 1, wherein each of said first light emitting pixels is arranged colinearly with each of said second light emitting pixels; wherein each of said third light emitting pixels is arranged between each of said first and second light emitting pixels to alternate with each of said first and second light emitting pixels.

3. A full color organic EL display panel according to claim 1, further comprising auxiliary electrodes arranged at least around said first, second and third light emitting pixels and in portions of said first electrodes.

4. A full color organic EL display panel according to claim 1, further comprising insulating layers, wherein each of said auxiliary electrodes is arranged at least one of around each of said first, second and third light emitting pixels and a central portion of each of said third light emitting pixel.

5. A full color organic EL display panel according to claim 1, further comprising partitions arranged among said second electrodes for electrically insulating said second electrodes.

6. A full color organic EL display panel according to claim 1, further comprising: encapsulating plates for encapsulating organic EL layers arranged on said first, second and third light emitting pixels; and an encapsulating material for bonding said encapsulating plates to a substrate in non-light emitting areas.

7. A full color organic EL display panel according to claim 1, wherein said first electrodes have zigzag-shaped electrodes having partitions inclined at a certain angle for connecting between each of said first light emitting pixels and each of said second light emitting pixels, and stripe shaped electrodes for connecting between each of said third light emitting pixel.

8. A full color organic EL display panel according to claim 7, wherein said partitions are arranged so as not to overlap with corner portions of said third light emitting pixels.

9. A full color organic EL display panel according to claim 1, wherein said third light emitting pixels have the area larger than that of said first or second light emitting pixels.

10. A full color organic EL display panel according to claim 1, wherein said first, second and third light emitting pixels have quadrangular structures which are the same or different from one another.

11. A full color organic EL display panel according to claim 1, wherein said first, second and third light emitting pixels are arranged into a delta structure.

12. A full color organic EL display panel according to claim 1, wherein said first electrodes are transparent; and wherein said second electrodes are made of metal.

13. A method of manufacturing a full color organic EL display panel which includes first, second and third pixels, a plurality of first electrodes, and a plurality of second electrodes perpendicularly intersecting the first electrodes, in which each of the first, second and third light emitting pixels is arranged in each of intersecting positions of the first and second electrodes, said method comprising the following steps of:

    (a) forming the first electrodes on a substrate, wherein the first electrodes include stripe-shaped electrodes for connecting between each of the third light emitting pixels, and zigzag-shaped electrodes having partitions in-

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clined at a certain angle for connecting between each of the first light emitting pixels and each of the second light emitting pixels;

(b) forming insulation partitions in areas excepting the light emitting pixels perpendicular to the first electrodes to insulate the first, second and third light emitting pixels;

(c) forming organic EL layers on the first, second and third light emitting pixels for emitting lights corresponding to the light emitting pixels respectively; and

(d) depositing an electrode material on the whole surface including the organic EL layers to form a plurality of second electrodes.

14. A method of manufacturing a full color organic EL display panel according to claim 13, further comprising the step of forming auxiliary electrodes at least around the light emitting pixels and in portions of the first electrodes.

15. A method of manufacturing a full color organic EL display panel according to claim 13, wherein said step (a) includes the step of forming insulation layers at least around the first, second and third light emitting pixels and in central portions of the third light emitting pixels.

16. A method of manufacturing a full color organic EL display panel according to claim 13, wherein said step (c) uses a shadow mask in forming the EL organic layers on the first, second and third light emitting pixels while moving the shadow mask,
wherein each of the EL organic layers emit a light corresponding to each of the first, second and third light emitting pixels.

17. A full color organic EL display panel comprising:

a unit light emitting pixel having first, second and third pixels;
a plurality of first electrodes; and
a plurality of second electrodes perpendicularly intersecting said first electrodes;

wherein each of said first, second and third light emitting pixels is arranged in each of intersecting positions of said first and second electrodes;

wherein said unit light emitting pixel has sub-pixels divided along diagonal directions; and

wherein each of said first, second and third light emitting pixels is arranged in each of said sub-pixels with an area different from one another according to the luminous efficiency of each of said first, second and third light emitting pixels.

18. A full color organic EL display panel according to claim 17, wherein said first light emitting pixel is positioned in a pair of said sub-pixels opposed along one diagonal direction; and wherein each of said second and third light emitting pixels is positioned in another pair of said sub-pixels opposed along another diagonal direction.

19. A full color organic EL display panel according to claim 18, wherein said first light emitting pixel has the luminous efficiency lower than that of said second and third light emitting pixels.

20. A full color organic EL display panel according to claim 17, wherein each of said first electrodes is formed under each of said first, second and third light emitting pixels and each of connected portions of said first, second and third light emitting pixels.

21. A full color organic EL display panel according to claim 20, further comprising auxiliary electrodes formed on the first electrodes at the connected portions.

22. A full color organic EL display panel according to claim 21, further comprising auxiliary electrodes formed in edge portions of said first, second and third light emitting pixels.

23. A full color organic EL display panel according to claim 17, further comprising insulation layers formed in non-light emitting areas around said first, second and third light emitting pixels.

24. A full color organic EL display panel according to claim 17, further comprising insulation partitions formed among said second electrodes for electrically insulating said second electrodes.

25. A full color organic EL display panel according to claim 17, further comprising: encapsulating plates for encapsulating organic EL layers arranged on said first, second and third light emitting pixels; and an encapsulating material for bonding said encapsulating plates to a substrate in non-light emitting areas.

26. A full color organic EL display panel according to claim 17, wherein said first electrodes are transparent lower electrodes; and wherein said second electrodes are upper electrodes made of metal.

27. A method of manufacturing a full color organic EL display panel which includes unit light emitting pixels having first, second and third pixels, a plurality of first electrodes, and a plurality of second electrodes perpendicularly intersecting the first electrodes, in which each of the first, second and third light emitting pixels is arranged in each of intersecting positions of the first and second electrodes, said

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method comprising the following steps of:

(a) forming first electrodes on a substrate in a repeated pattern having a certain polygonal shape connected to stripe shape;
(b) forming insulation partitions among the unit light emitting pixels adjacent to the first electrodes in the perpendicular direction;
(c) forming organic EL layers on the first, second and third light emitting pixels for emitting lights corresponding to the first, second and third light emitting pixels respectively; and
(d) depositing an electrode material on the whole surface including the organic EL layers to form a plurality of second electrodes.

28. A method of manufacturing a full color organic EL display panel according to claim 27, wherein said step (a) includes the step of forming auxiliary electrodes in the first electrodes formed in the connecting portions of the first, second and third light emitting pixels and formed in edge portions of the first, second and third light emitting pixels, wherein the auxiliary electrodes have resistance lower than that of the first electrodes.

29. A method of manufacturing a full color organic EL display panel according to claim 27, wherein said step (a) includes the step of forming insulation layers in non-light emitting areas around the first, second and third light emitting pixels.

30. A driving circuit of a display device having anode and cathode lines, comprising:

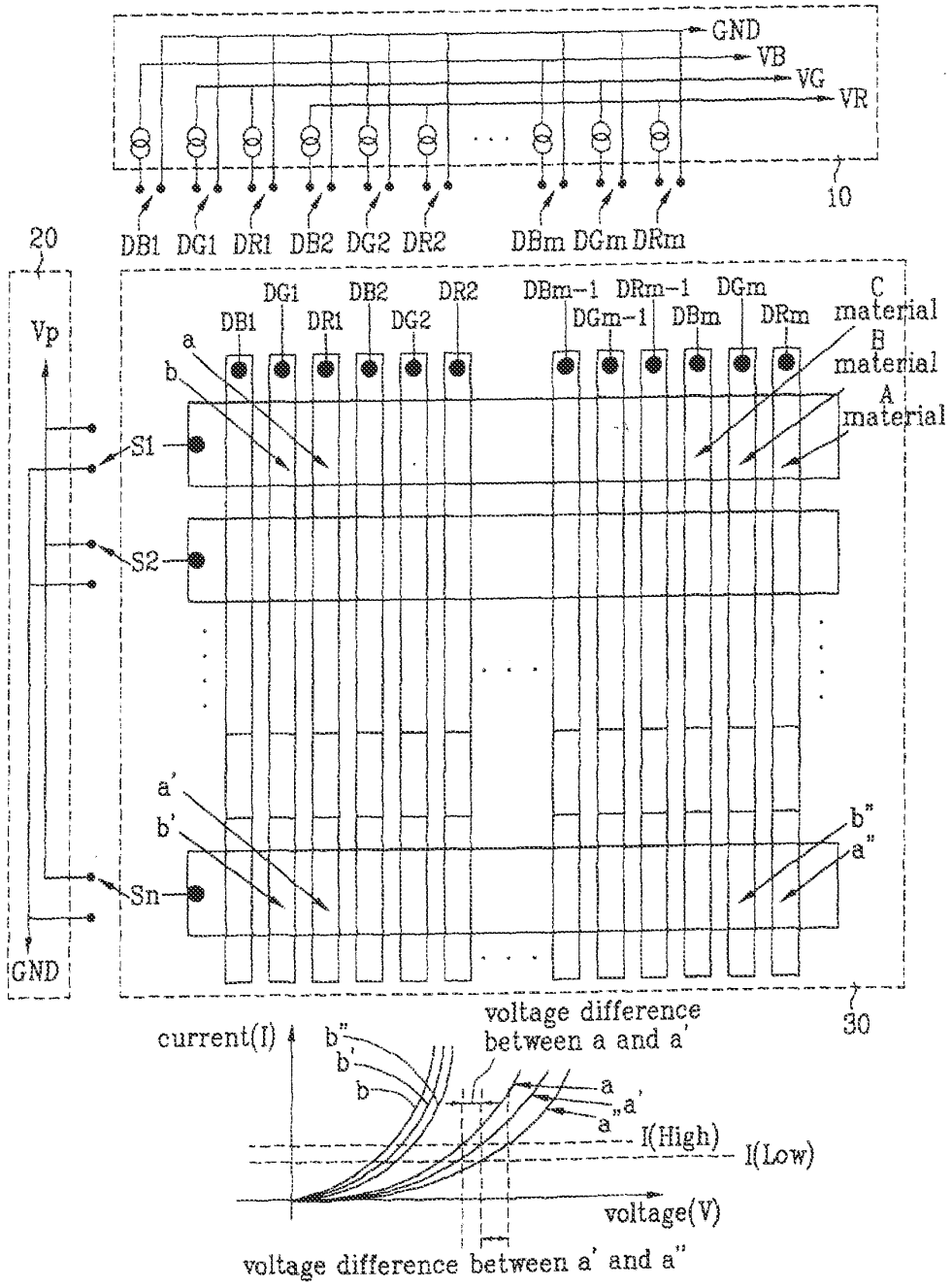
an anode circuit for outputting a different drive voltage for each of RGB light emitting pixels so as to correspond to the drive voltage varying according to the line resistance and the material features of the anode lines and the cathode lines;
a cathode circuit connected to both ends of the cathode lines for outputting the same signals; and
a display unit where the area ratio of each of the RGB light emitting pixels and the width of the anode lines are adjusted according to the features of the applied drive voltage.

31. A driving circuit of a display device according to claim 30, wherein said cathode circuit is arranged at the both sides of the cathode lines for applying the same signals to the display unit.

32. A driving circuit of a display device according to claim 30, wherein the area ratio of each of the RGB light emitting pixels is 3:6:1.

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FIG. 1
Related Art



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FIG. 2A
Related Art

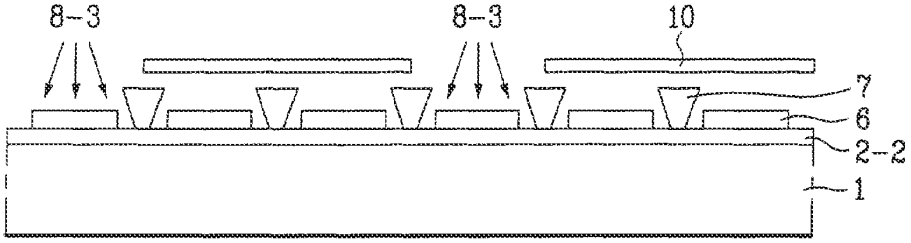
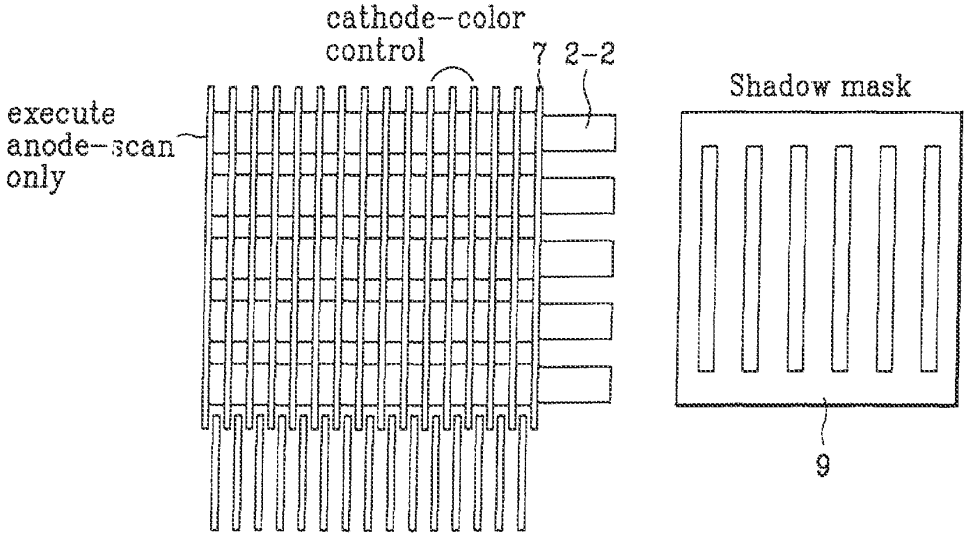


FIG. 2B
Related Art



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FIG. 2C
Related Art

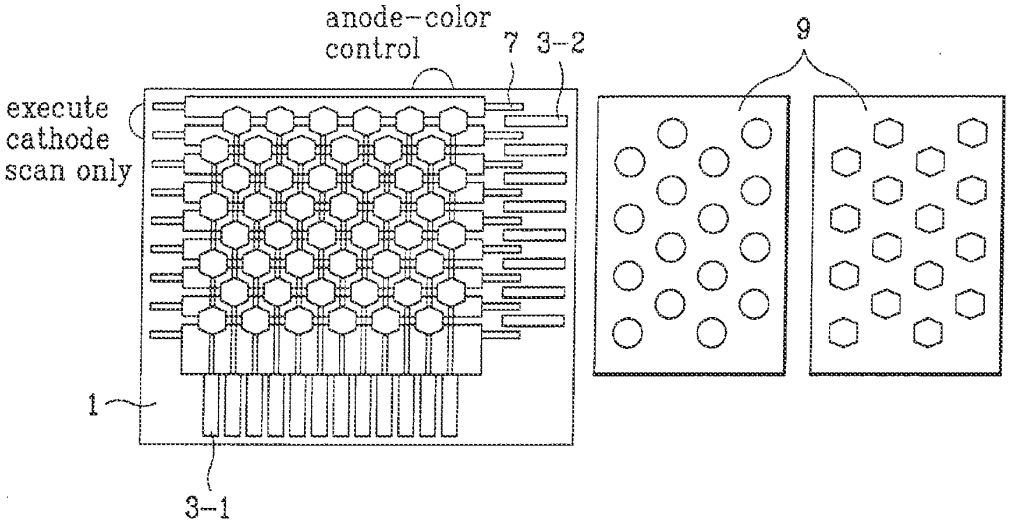
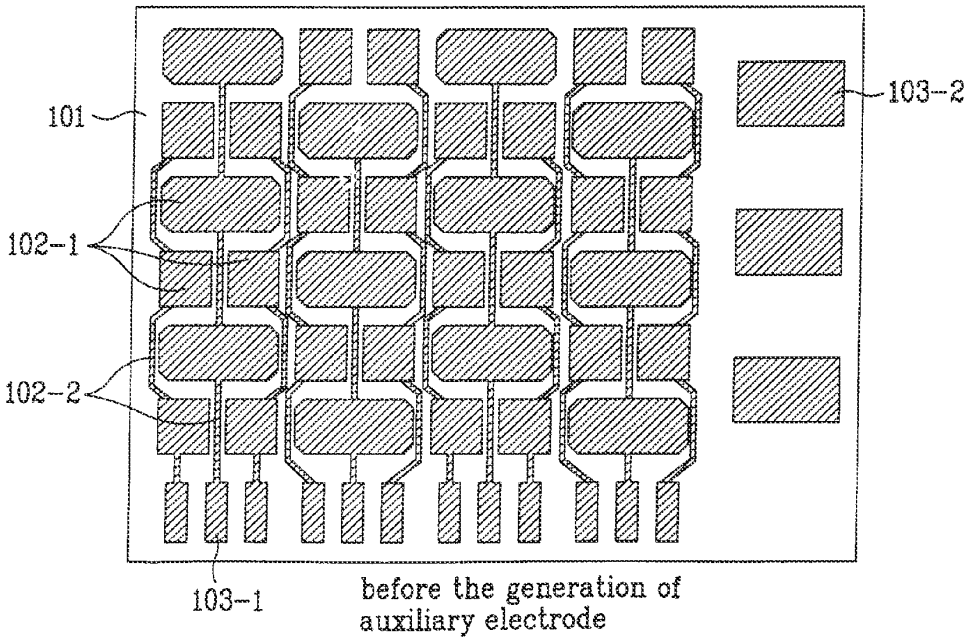


FIG. 3A



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FIG. 3B

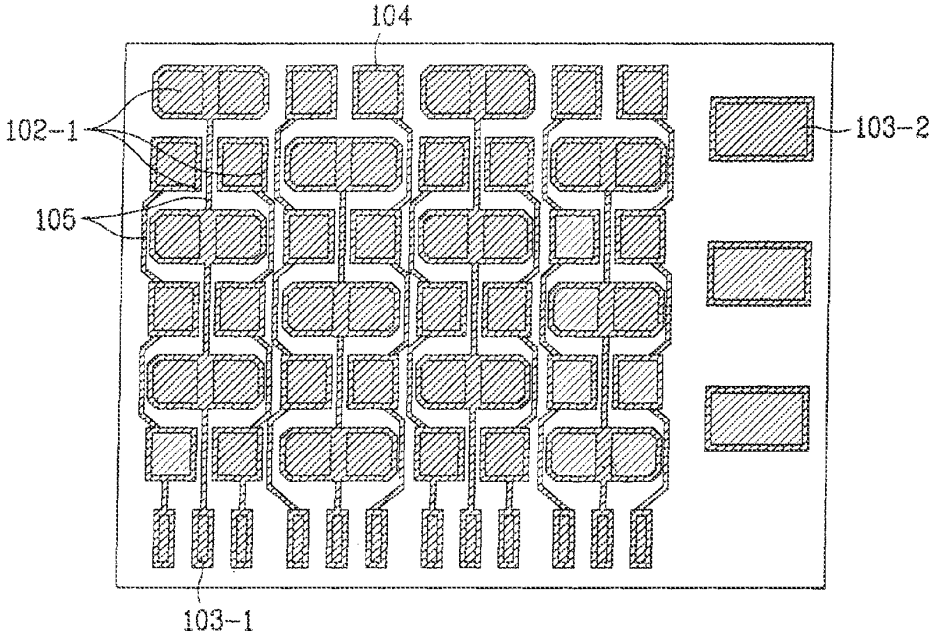
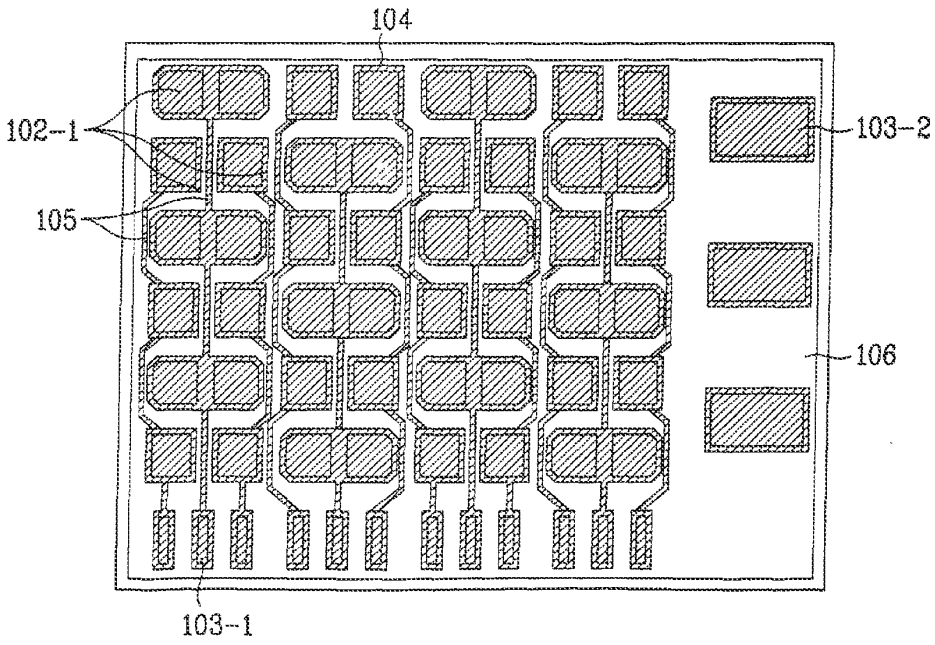


FIG. 3C



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FIG. 3D

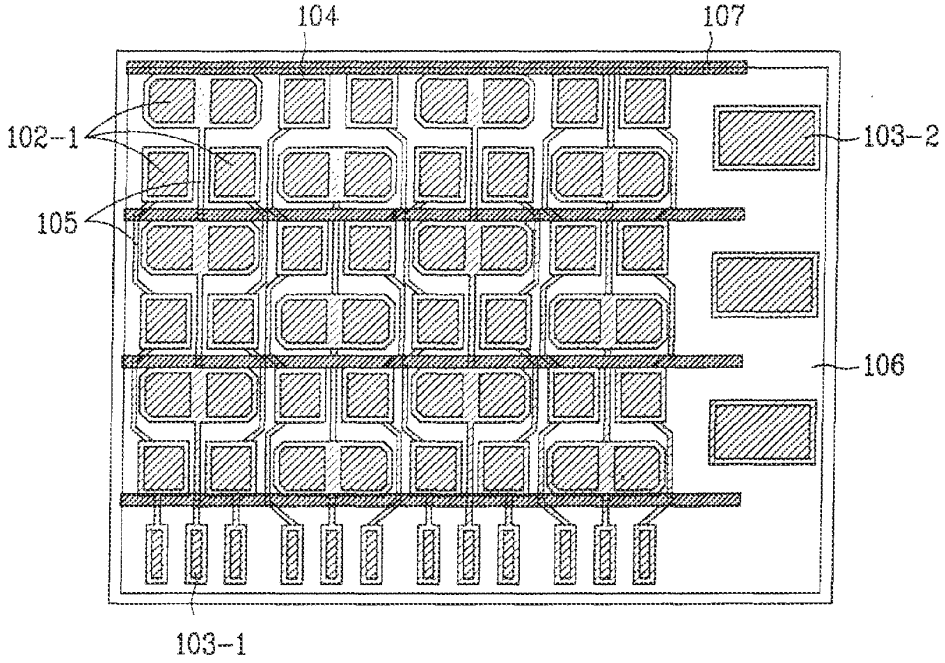
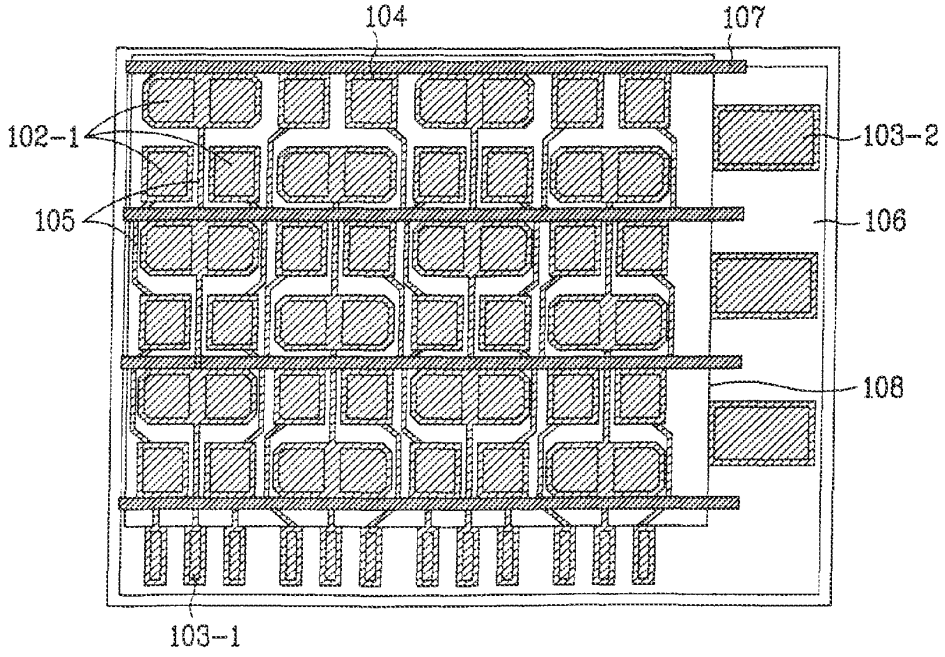


FIG. 3E



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FIG. 3F

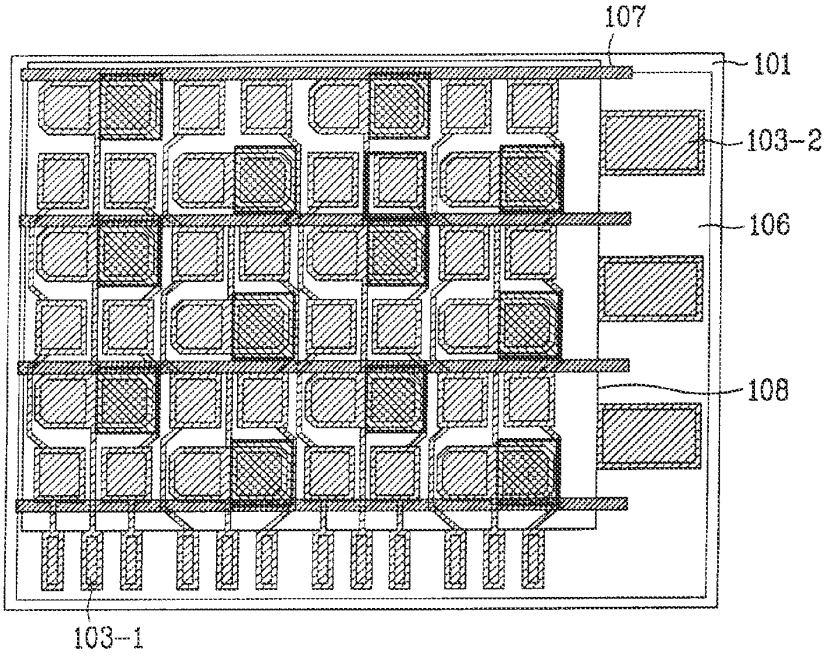
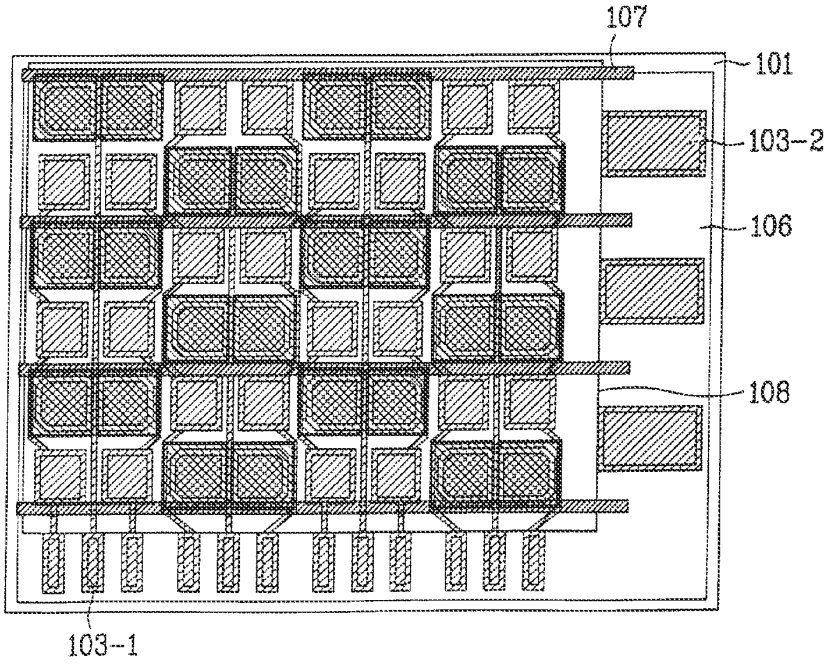


FIG. 3G



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FIG. 3H

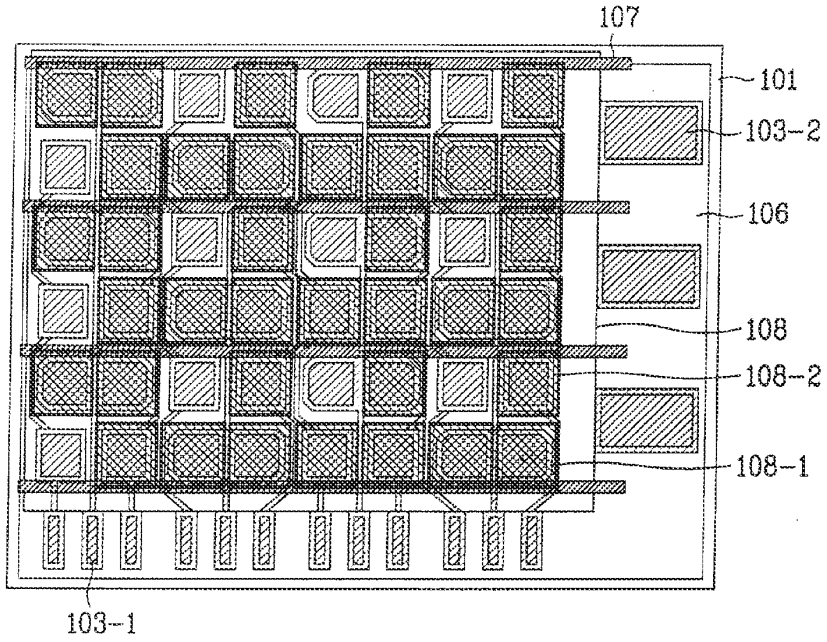
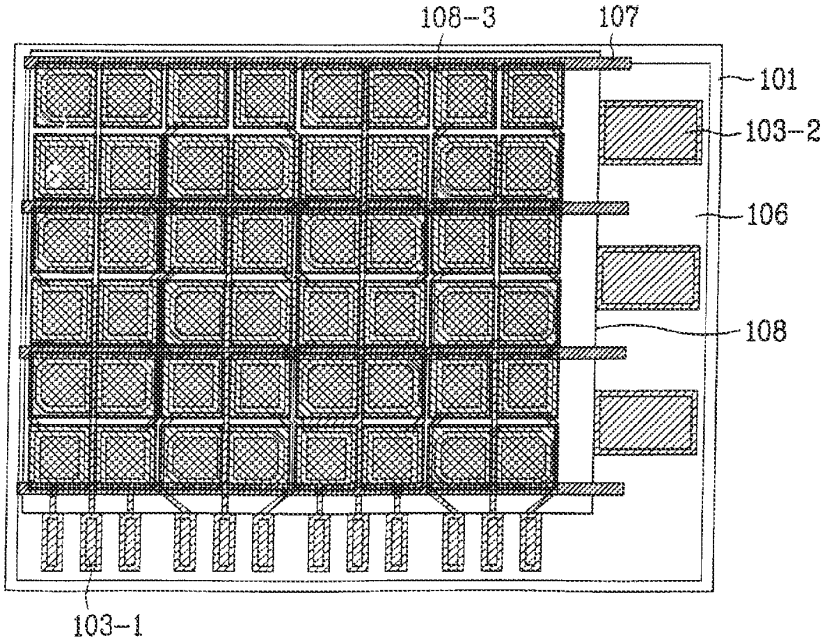


FIG. 3I



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FIG. 3J

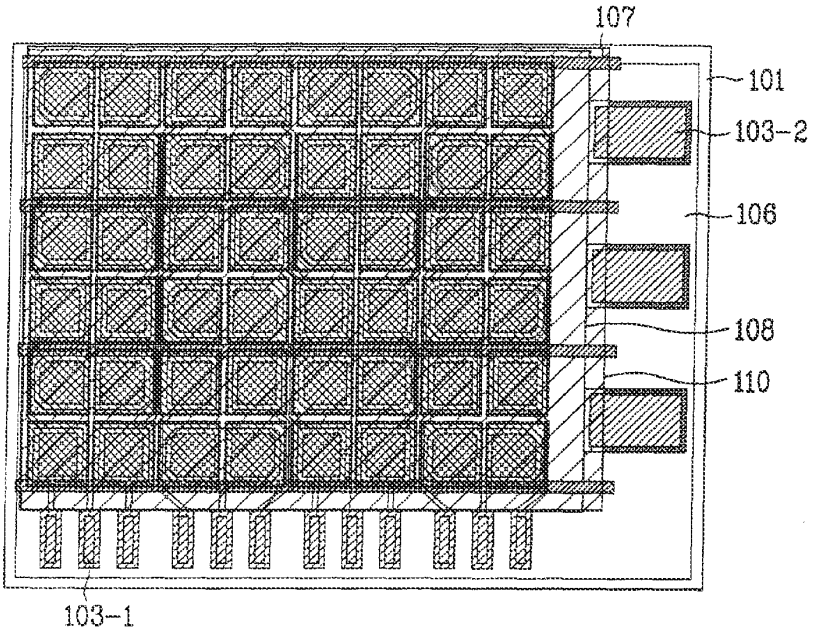
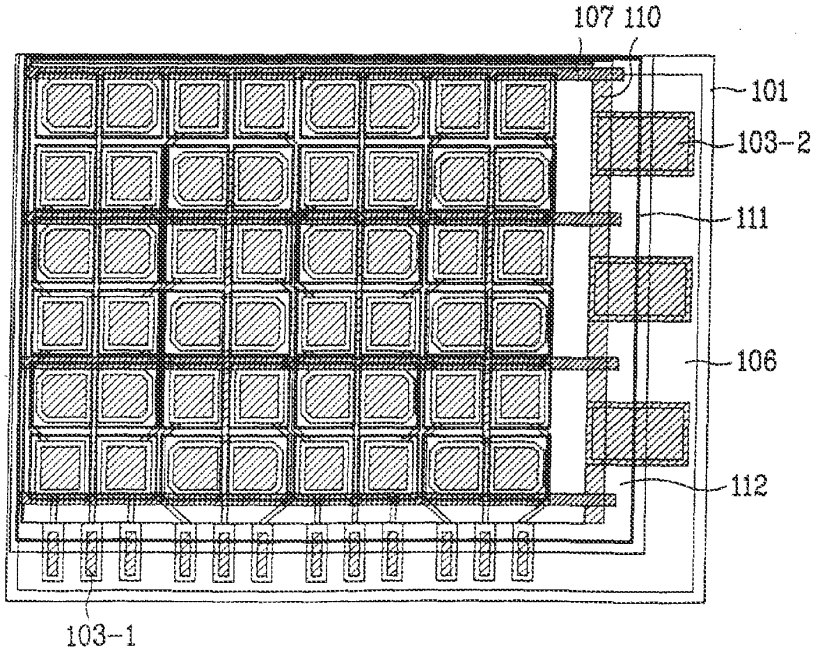
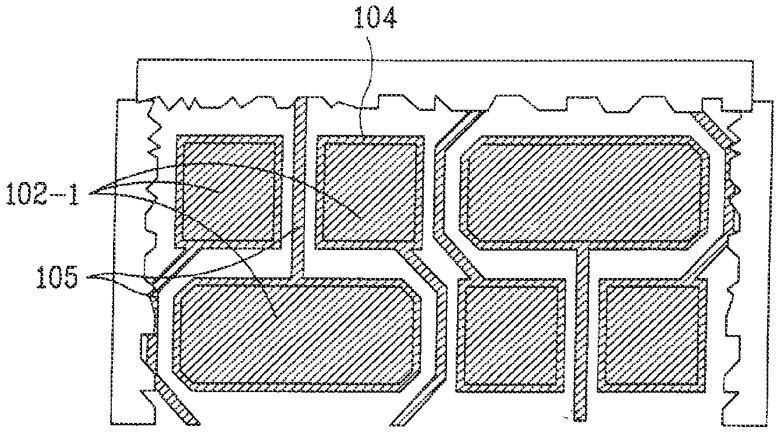


FIG. 3K



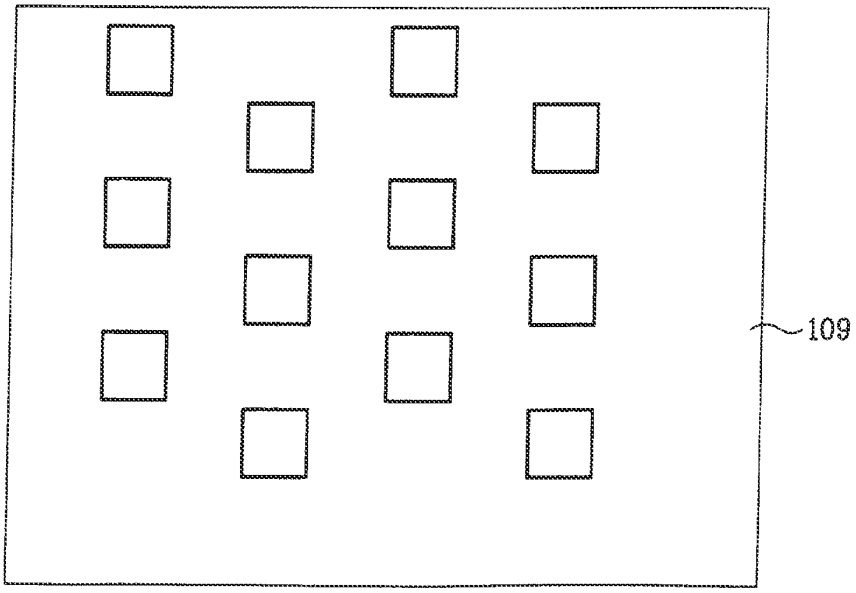
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FIG. 4



after the generation of auxiliary electrode

FIG. 5



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FIG. 6A

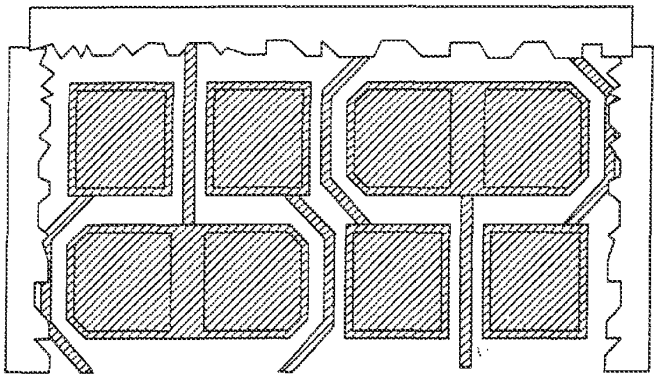
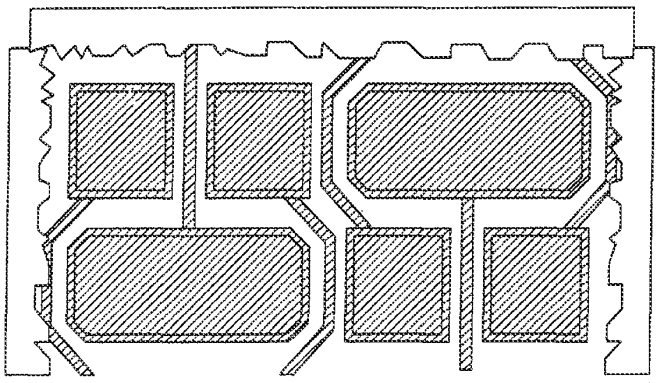
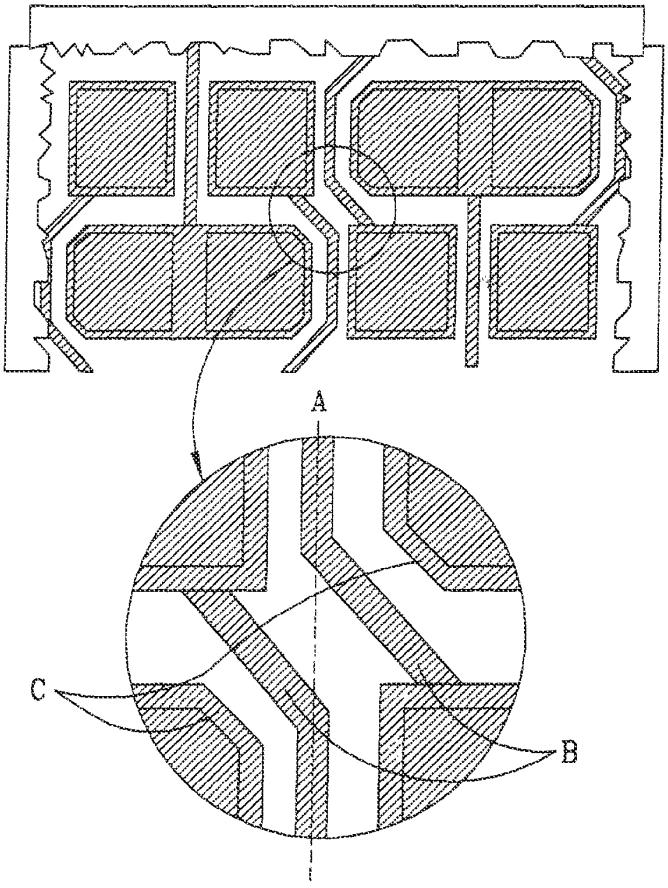


FIG. 6B



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FIG. 7



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FIG. 8A

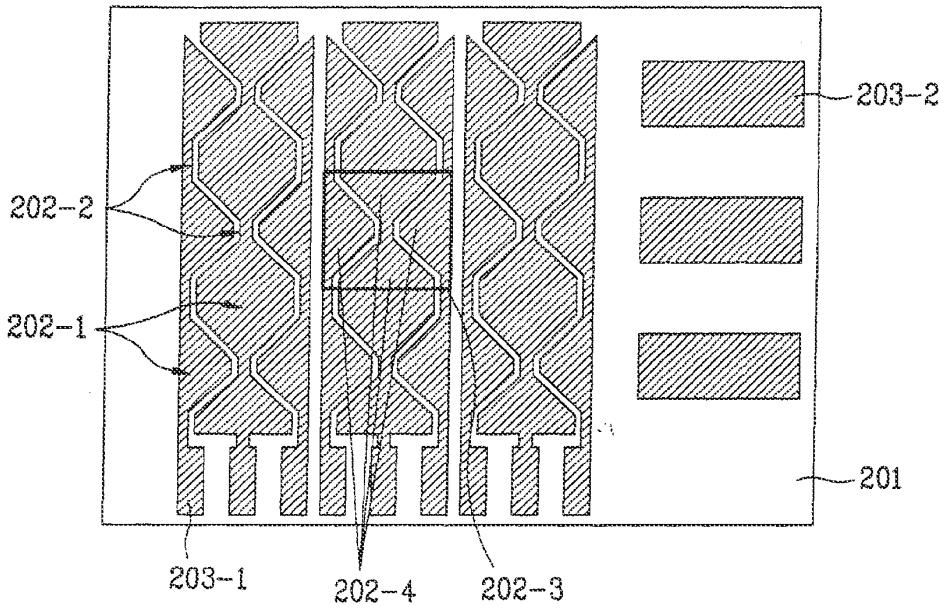
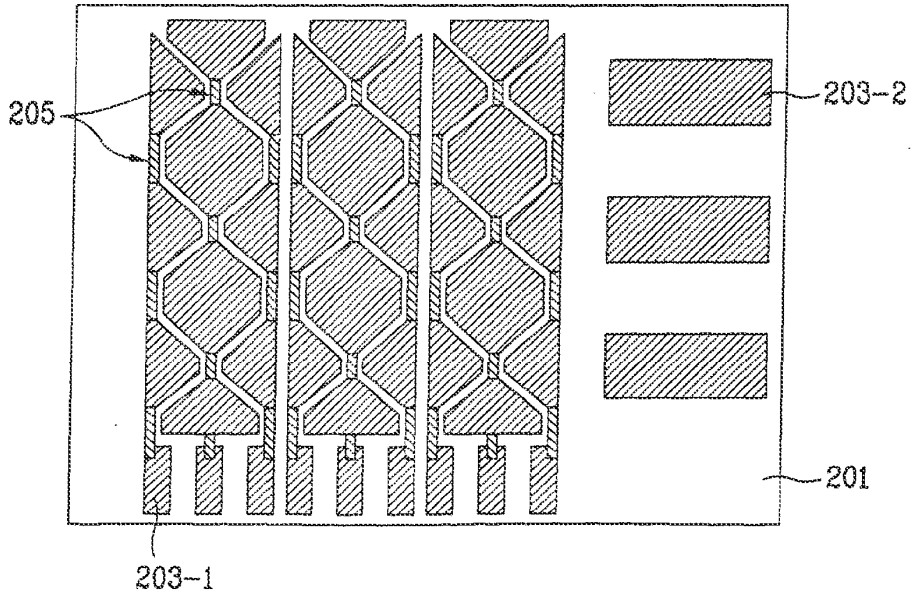


FIG. 8B



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FIG. 8C

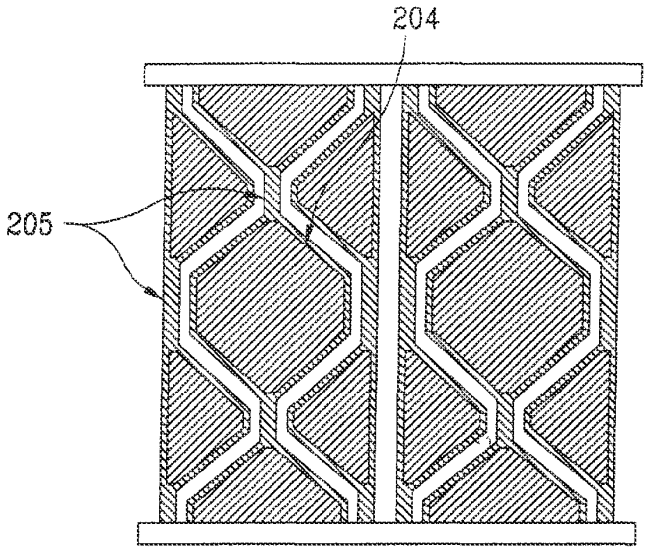
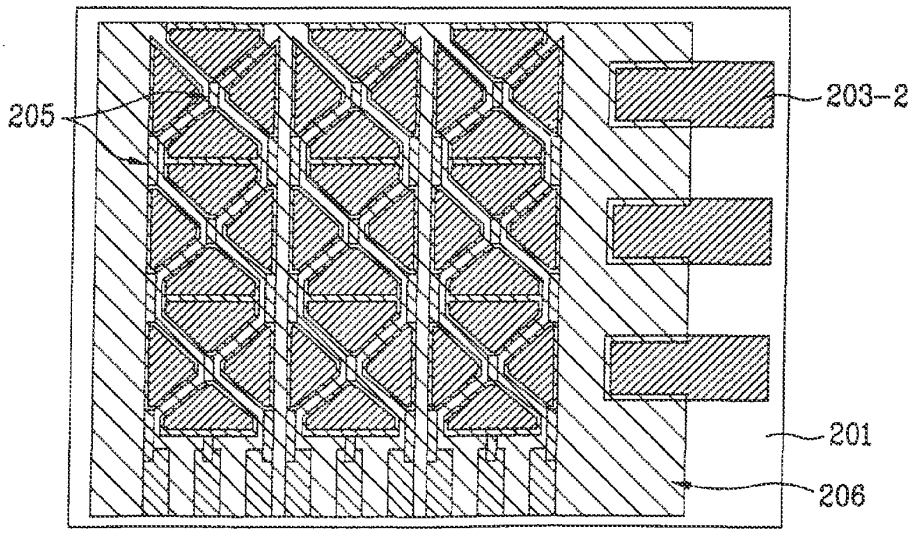


FIG. 8D



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FIG. 8E

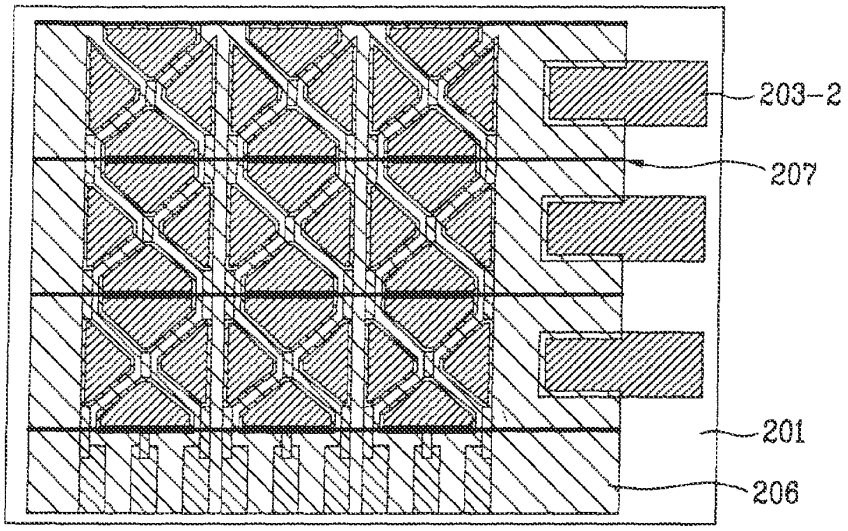
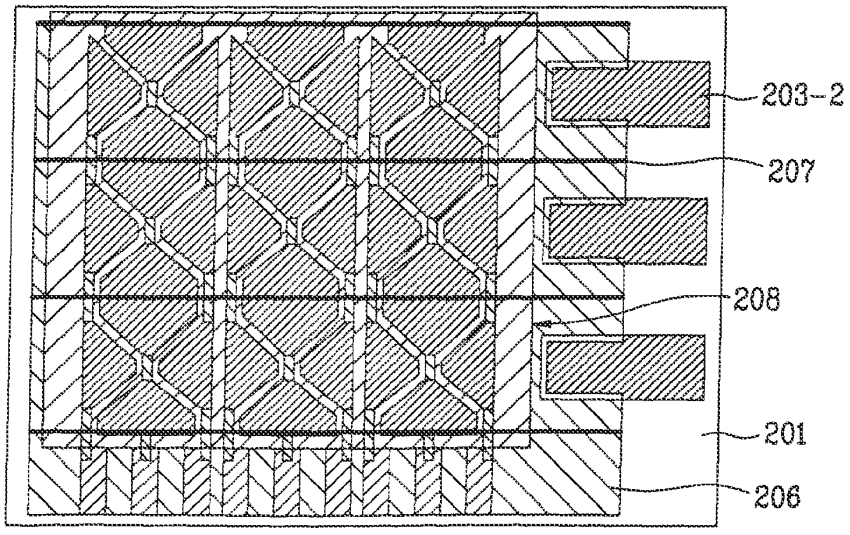


FIG. 8F



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FIG. 8G

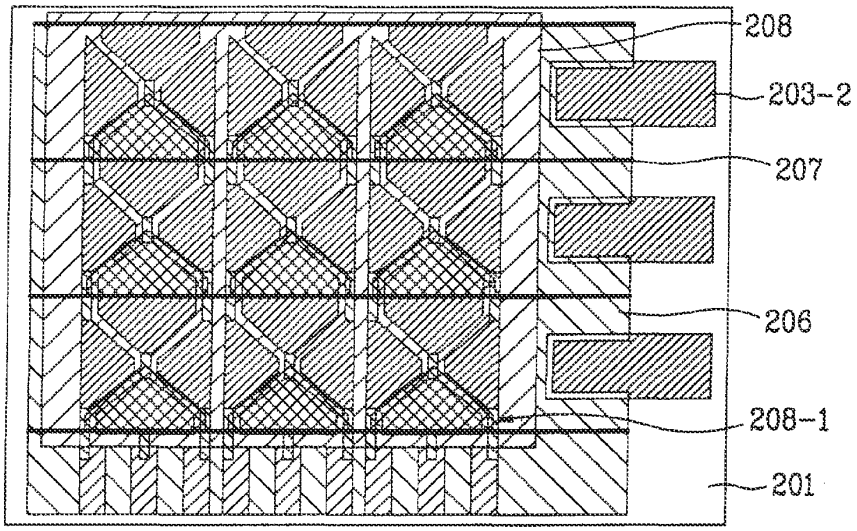
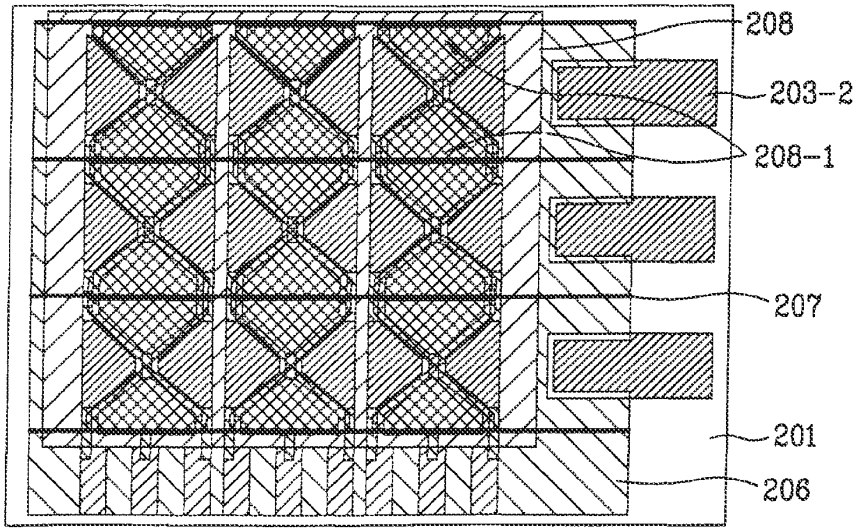


FIG. 8H



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FIG. 8I

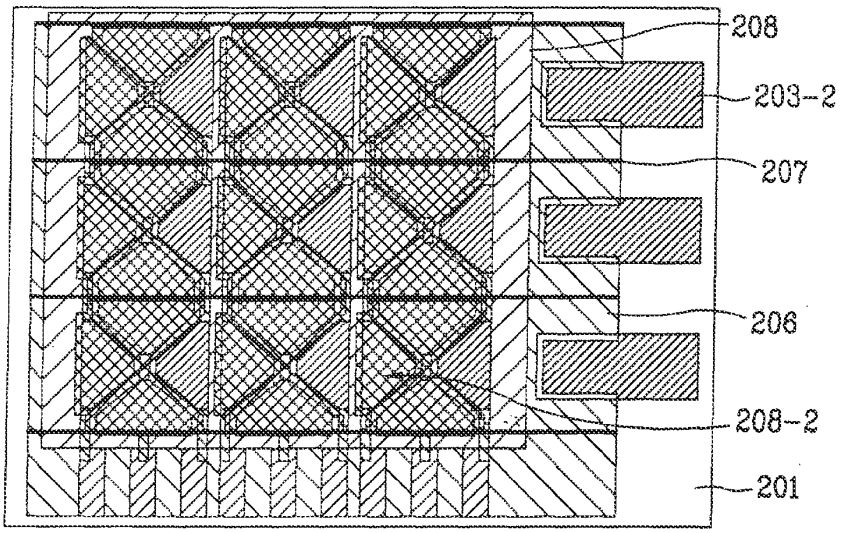
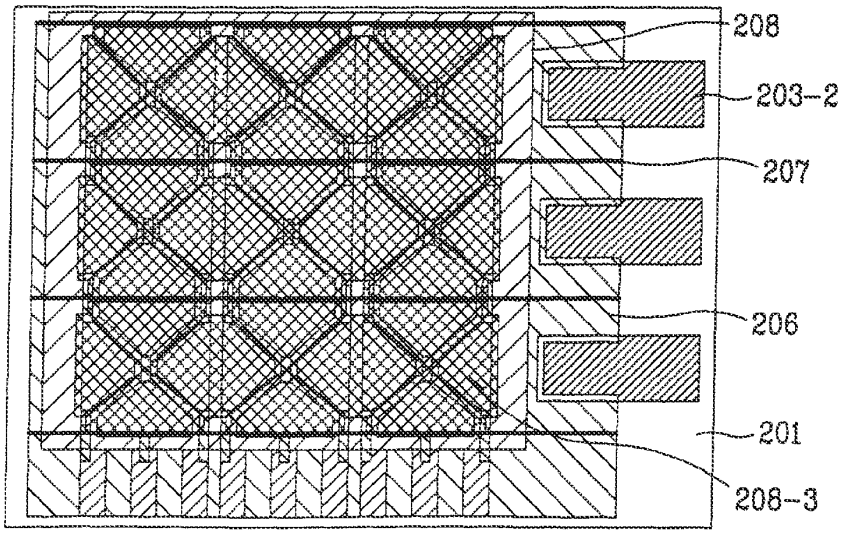


FIG. 8J



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FIG. 8K

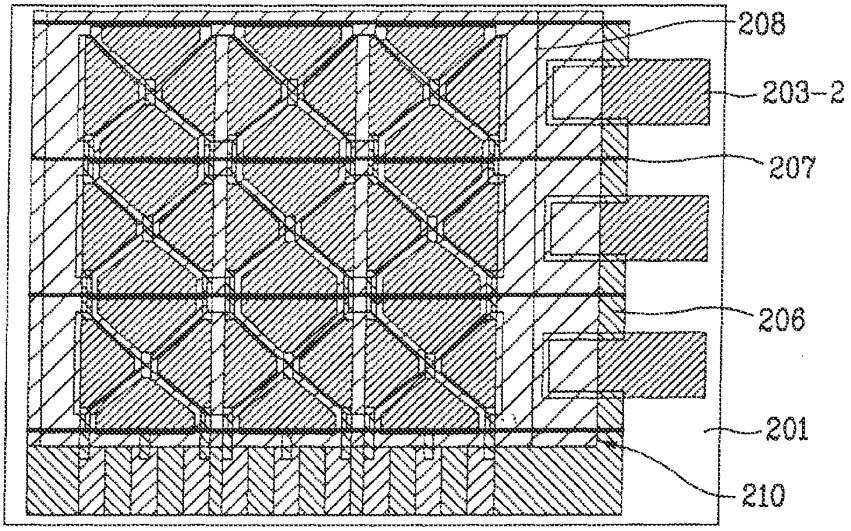
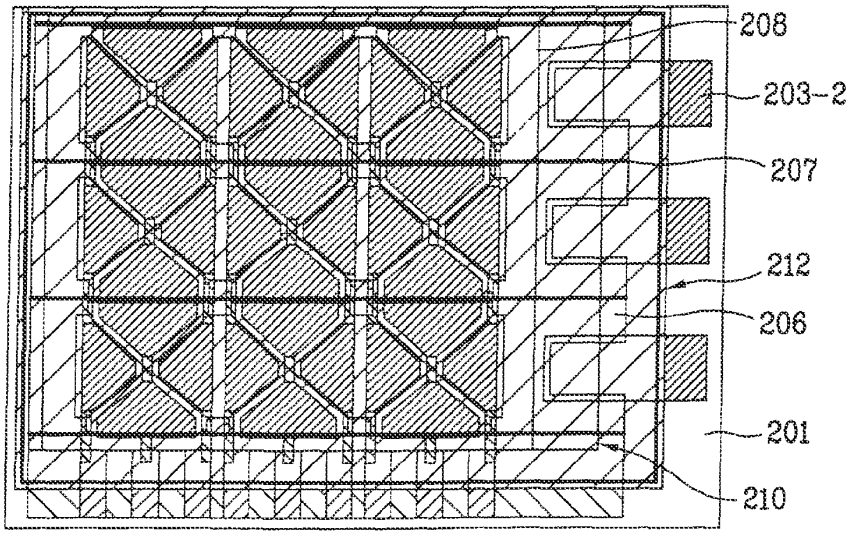
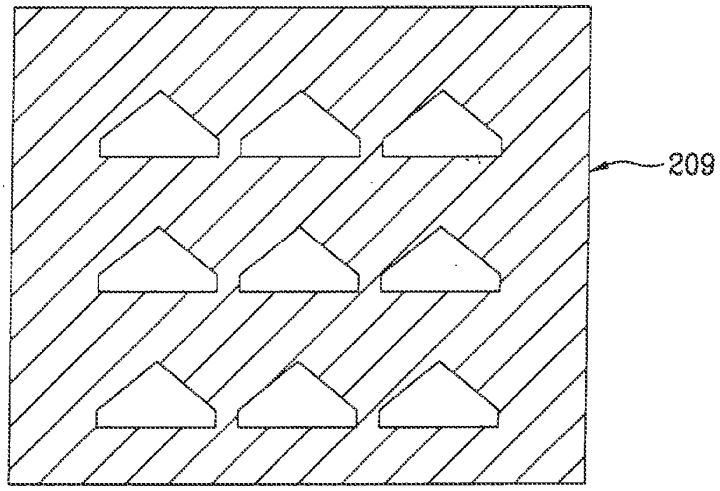


FIG. 8L



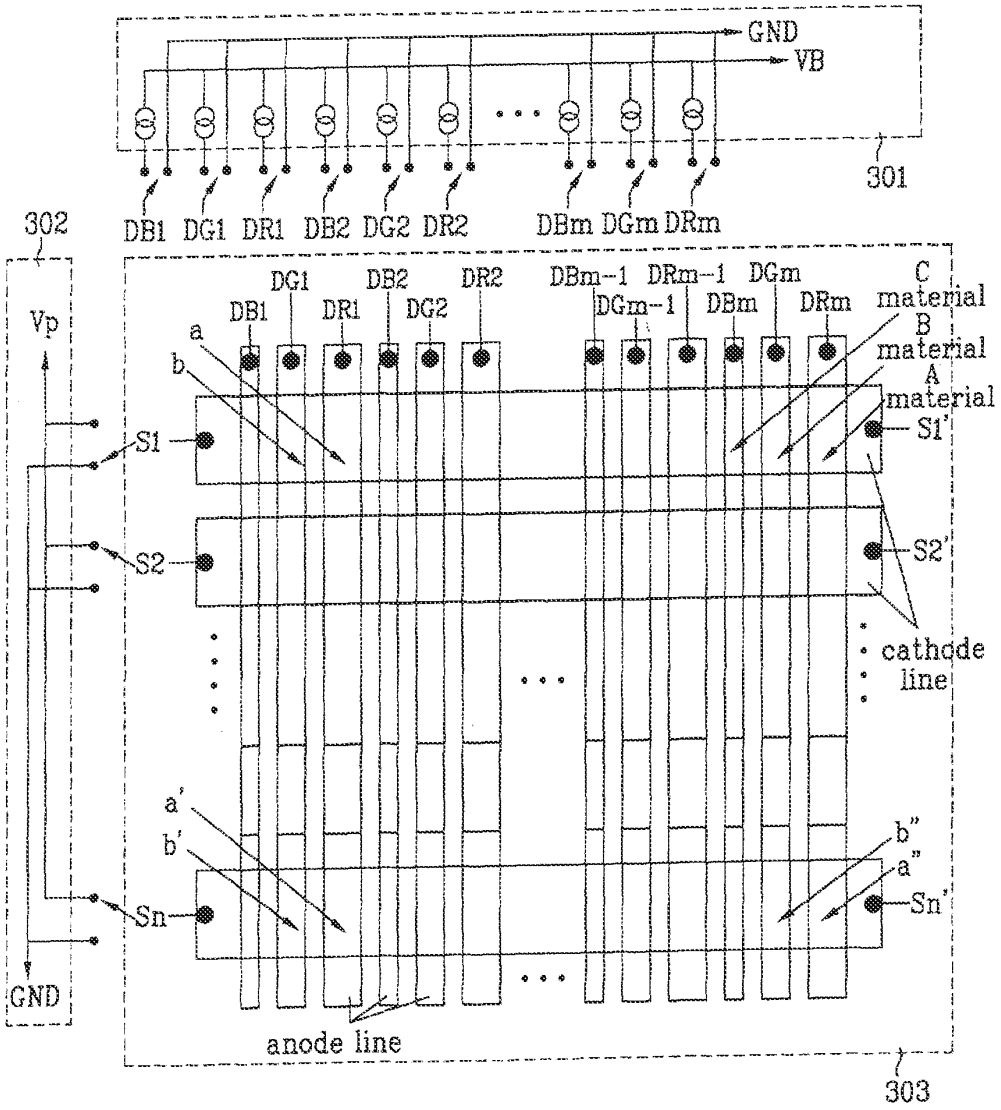
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FIG. 9



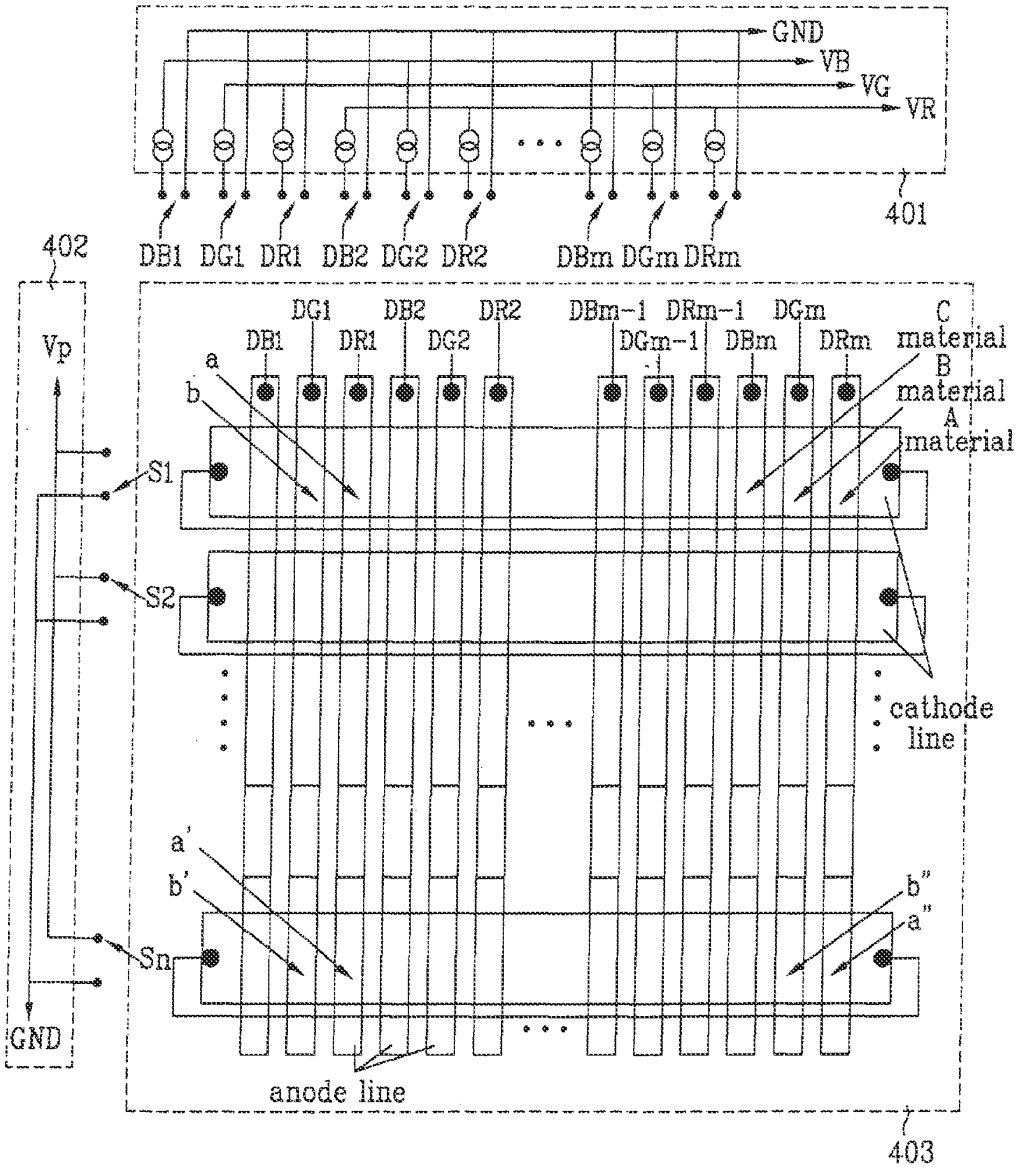
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FIG. 10



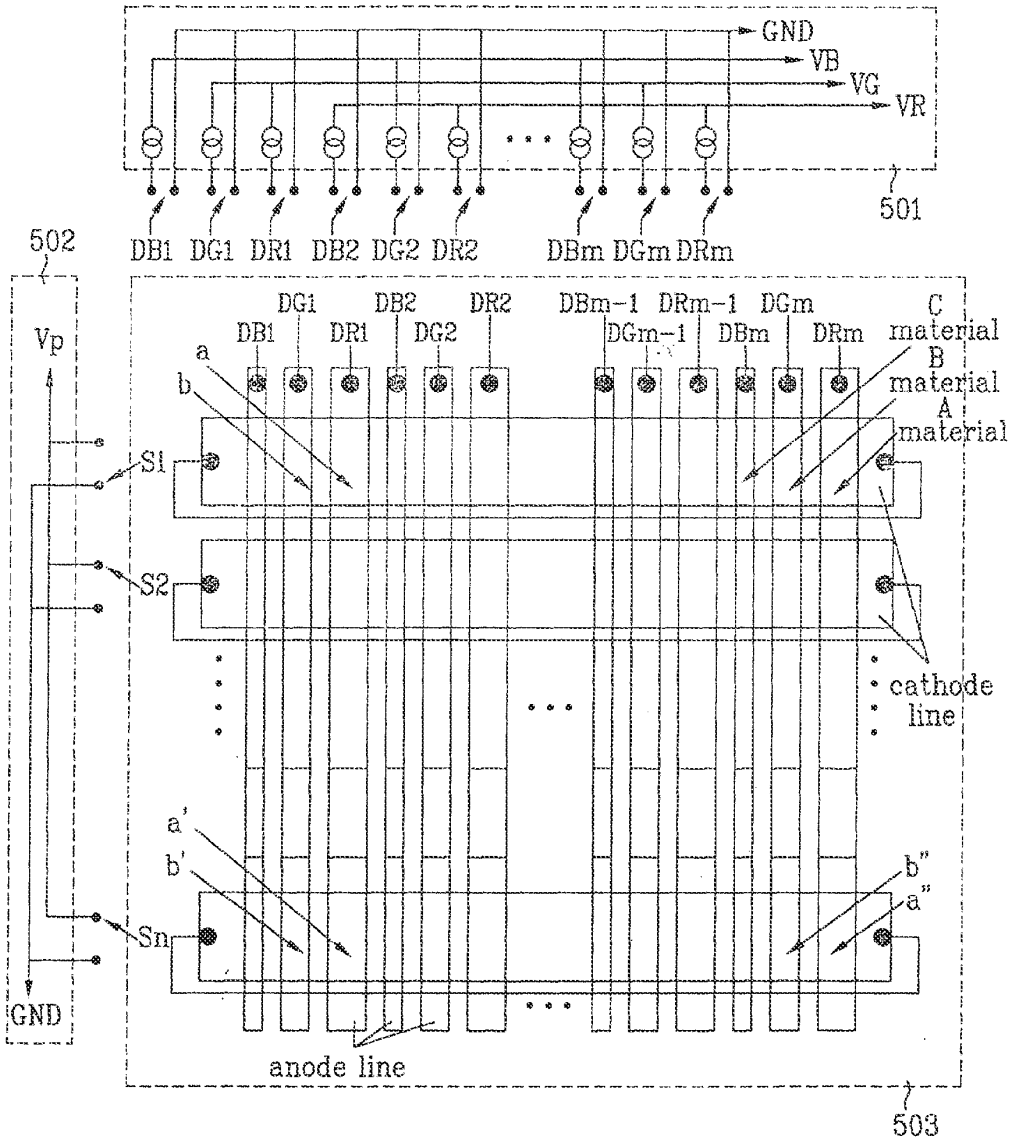
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FIG. 11



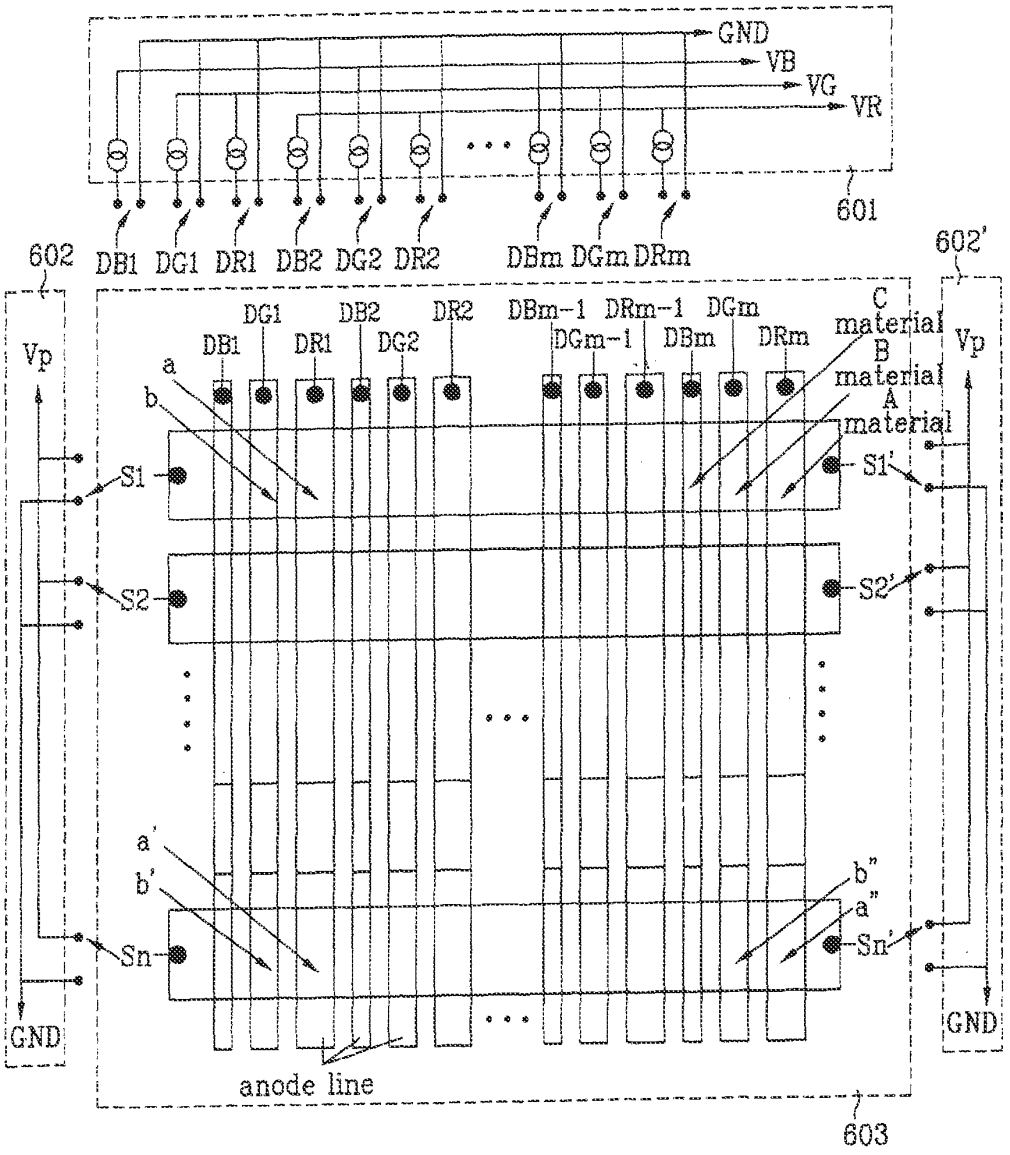
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FIG. 12



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FIG. 13



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(19)日本国特許庁(JP)　(12)公開特許公報(A)　(11)特許出願公開番号
特開2008-277264
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G09F 9/30	(2006.01)	G09F	9/30	339C	5C080
G09G 3/30	(2006.01)	G09G	3/30	Z	5C094
G09G 3/20	(2006.01)	G09G	3/20	642K	
H01L 51/50	(2006.01)	G09G	3/20	621J	

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(32)優先日　平成19年4月3日 (2007.4.3)
(33)優先権主張国　日本国 (JP)

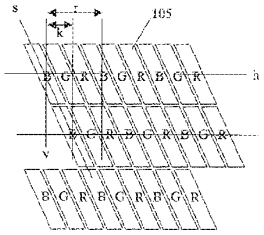
(71)出願人　000001007
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東京都大田区下丸子３丁目３０番２号　キヤノン株式会社内

Ｆターム(参考)　3K107 AA01 BB01 CC02 CC04 CC21 CC45 EE07 FF15 GG00 GG02 GG33

最終頁に続く

(54)【発明の名称】カラー画像表示パネル及びその製造方法、並びにカラー画像表示装置

(57)【要約】
【課題】副画素の配列がデルタ配列やスクランブル配列などの画像表示パネルと同様の表示性能を有する、カラー画像表示パネル及びその製造方法、並びにカラー画像表示装置を提供する。
【解決手段】基板上に形成された第１の電極上に、真空堆積法で有機発光層が堆積され、さらに第２の電極が形成されてなる、少なくとも赤、緑、青の発光色を有する有機ＥＬ素子が一定の順に並んで構成される画素が複数配列された有機エレクトロルミネッセンス型二次元カラー画像表示パネルにおいて、各々の有機ＥＬ素子は平面形状において一組の平行な二辺を有しており、互いに他色の発光色を有する有機ＥＬ素子が、前記平行な二辺で隣接しており、同一の発光色を有する有機ＥＬ素子は、前記平行な二辺の平行線方向に隣接して、垂直線に対して傾斜して平行に並ぶストライプ状に配列されていることを特徴とする。
【選択図】図１



【特許請求の範囲】
【請求項１】
基板上に形成された第１の電極上に、真空堆積法で有機発光層が堆積され、さらに第２の電極が形成されてなる、少なくとも赤、緑、青の発光色を有する有機ＥＬ素子が一定の順に並んで構成される画素が複数配列された有機エレクトロルミネッセンス型二次元カラー画像表示パネルにおいて、
各々の有機ＥＬ素子は平面形状において一組の平行な二辺を有しており、
互いに他色の発光色を有する有機ＥＬ素子が、前記平行な二辺で隣接しており、同一の発光色を有する有機ＥＬ素子は、前記平行な二辺の平行線方向に隣接して、垂直線に対して傾斜して平行に並ぶストライプ状に配列されていることを特徴とする、カラー画像表示パネル。
【請求項２】
水平方向に隣接するように配列された、前記少なくとも赤、緑、青の発光色を有する有機ＥＬ素子を副画素の一組として画素が形成され、水平方向に隣接する前記画素はその重心位置を結ぶ直線が水平線に対して平行となるように配列されていることを特徴とする、請求項１に記載のカラー画像表示パネル。
【請求項３】
前記有機ＥＬ素子は平行四辺形であることを特徴とする、請求項１又は請求項２に記載のカラー画像表示パネル。
【請求項４】
前記有機ＥＬ素子は長方形であることを特徴とする、請求項１又は請求項２に記載のカラー画像表示パネル。
【請求項５】
前記有機ＥＬ素子の短辺は水平線に対して平行であることを特徴とする、請求項１乃至請求項４のいずれか１項に記載のカラー画像表示パネル。
【請求項６】
任意の前記副画素の重心位置と前記副画素と垂直方向に隣接する同一の発光色を有する副画素の重心位置との水平方向のずれ量ｋと、水平方向に隣接する同一の発光色を有する副画素の繰り返しピッチｒとの比の値ｋ／ｒは、１／２あるいは１／３であることを特徴とする、請求項１又は請求項２に記載のカラー画像表示パネル。
【請求項７】
請求項１乃至請求項６のカラー画像表示パネルと表示制御部とを有することを特徴とする、カラー画像表示装置。
【請求項８】
基板上に二次元に配列した複数の第１の電極を形成する工程と、少なくとも赤、緑、青の発光色を有する有機発光材料を、それぞれの発光色ごとに、複数の貫通孔を有するマスクの前記貫通孔を通じて前記第１の電極の形成位置に堆積する工程と、第２の電極を形成する工程とを有する有機エレクトロルミネッセンス型二次元カラー画像表示パネルの製造方法において、
複数の第１の電極を形成する工程では、一組の平行な二辺を有する平面形状の第１の電極を、前記平行な二辺の第一の辺が直線上に並び、前記平行な二辺の第二の辺もまた直線上に並ぶように一次元に配置し、前記電極の一次元配列が垂直線に対して傾斜して平行に並ぶストライプ状となるように二次元に配列を形成すること、
有機発光材料を堆積する工程では、前記第１の電極が形成されてなるストライプに対応するように貫通孔がストライプ状に形成されたマスクを、前記第１の電極が形成されてなるストライプと前記マスクの貫通孔とを対向させるように位置合わせし、有機発光材料の堆積を行うこと、
を特徴とする、カラー画像表示パネルの製造方法。
【請求項９】
水平方向に隣接するように配列した、前記少なくとも赤、緑、青の発光色を有する有機

ＥＬ素子を副画素の一組として画素を形成し、水平方向に隣接する前記画素はその重心位置を結ぶ直線を水平線に対して平行となるように配列していることを特徴とする、請求項８に記載のカラー画像表示パネルの製造方法。

【請求項１０】

前記第１の電極は平行四辺形であることを特徴とする、請求項８又は請求項９に記載のカラー画像表示パネルの製造方法。

【請求項１１】

前記第１の電極は長方形であることを特徴とする、請求項８又は請求項９に記載のカラー画像表示パネルの製造方法。

【請求項１２】

前記第１の電極の短辺は水平線に対して平行であることを特徴とする、請求項８乃至請求項１１のいずれか１項に記載のカラー画像表示パネルの製造方法。

【請求項１３】

任意の副画素の重心位置と前記副画素と垂直方向に隣接する同一の発光色を有する副画素の重心位置との水平方向のずれ量ｋと、水平方向に隣接する同一の発光色を有する副画素の繰り返しピッチｒとの比の値ｋ／ｒは、１／２あるいは１／３であることを特徴とする、請求項８又は請求項９に記載のカラー画像表示パネルの製造方法。

【発明の詳細な説明】

【技術分野】

【０００１】

本発明は、基板上に第１の電極と、少なくとも１種の低分子発光性有機化合物を含む層と、第２の電極とを順に積層した構造の有機エレクトロルミネッセンス素子（有機ＥＬ素子）が複数配列されたカラー画像表示パネルに関する。また本発明は前記カラー画像表示パネルの製造方法、並びに前記カラー画像表示パネルを用いたカラー画像表示装置に関する。

【背景技術】

【０００２】

基板上に形成された第１の電極と、該第１の電極上に形成された有機化合物層と、該有機化合物層上に形成された第２の電極とが積層された構造の有機ＥＬ素子が知られている。

【０００３】

図１１は、有機ＥＬ素子がマトリックス状に配置されている画像表示パネルの一例を示す概略構成図である。（ａ）は各画素の配列を示す平面図である。（ｂ）はＡ－Ａ’の断面図である。図１１において、１０１は基板、１０２は第１の電極、１０３は有機化合物層、１０４は第２の電極である。また１０５は第１の電極１０２と第２の電極１０４との間に有機化合物層が介在している領域で規定される画素である。

【０００４】

図１１においては、基板１０１の表面上に画素としてドット状の有機ＥＬ素子がマトリックス状に配列され、かつ各有機ＥＬ素子が別々に発光できるように構成された例を示している。この画像表示パネルは、発光させる有機ＥＬ素子を適切に選択させることにより、様々な画像を表示することができる。

【０００５】

図１２は、有機ＥＬ素子１０５の周辺部に素子分離膜１１０が形成されており、隣接する素子間を電流が交差して流れない構成とされた画像表示パネルの断面図の一例である。図１２においては、さらに保護層１１１が素子表面に形成されて、素子部に環境から水や空気等が浸入することを防ぐ構造を示している。

【０００６】

カラー画像表示パネルを形成するために、多色の副画素を一組として用いる場合の前記副画素の形状や配列の例について説明する。

【０００７】

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図１３は副画素の配列の平面図である。図１３において（ａ）はストライプ配列と呼ばれる副画素の配列の模式図である。フルカラー画像表示パネルにおいては３原色を必要とするのでそれぞれ赤、緑、青の発光色を有する素子が隣接して形成される。この３つの隣接する素子を副画素とする一組で画素が形成される（図１３において副画素の色を区別する場合には、赤をＲ、緑をＧ、青をＢの記号で表す。以下同様。）。

【０００８】

コンピュータのディスプレイでは正方形の画素が通常用いられるので、前記副画素は長辺／短辺比が約３の長方形に形成され、この長方形の短辺方向で隣接した副画素をもって画素とされる場合が多い。特許文献１はストライプ配列の副画素を有するフルカラー有機ＥＬ画像表示パネルを、ストライプ状のマスクを用いた工程で製造する方法に言及している。

【０００９】

明るさを得る目的や、表示可能な色の範囲を拡張する目的などで４種又はそれ以上の色（白も含む）の副画素をもって１画素とする場合でも、長方形の副画素の短辺方向で隣接した一組により画素が形成されるのが普通である。フルカラーが必要とされず２種の副画素をもって１画素とする場合などにおいても、長方形の副画素の短辺方向で隣接した一組により画素が形成されるのが普通である。

【００１０】

図１３（ｂ）は、ＲＧＢデルタ配列と呼ばれる別の副画素の配列の模式図である。このデルタ配列の特徴は奇数行と偶数行とで色配列が１／２ピッチずれていることである。画素数の限られる携帯型の小画面ディスプレイで自然画を表示した場合の解像感に優れている。

【００１１】

また同図の（ｃ）に示す、副画素の配列が上の行と１／３ピッチずれている、スクランブル配列と呼ばれる副画素の配列も同様に知られている。

【００１２】

特許文献２には、表示画像の画質の向上を目的として、画素内における副画素のカラーの位置構成が、隣接する画素と異なる表示パネルが提案されている。また特許文献２では、インクジェット印刷工程によりエレクトロルミネッセンス材料を堆積する場合に、画素配列に対して傾斜したライン状に連続して堆積する方法が開示されている。これにより堆積層の厚さを安定化し、さらに画素内における副画素のカラーの位置構成が異なる表示パネルが得られる。

【００１３】

図１４は、カラー画像表示パネルをマスクを通じた真空堆積法により製造する一般的工程を説明した斜視図である。図１４において、図１１や図１２と同じ符号は同じ部材を示しており、２０１はマスク、２０２は貫通孔である。図の例ではマスク２０１の貫通孔２０２は前記デルタ配列の特定の一色の副画素の配置に一致するように形成されている。

【００１４】

基板１０１上にアクティブマトリクス駆動回路（不図示）と前記回路に接続された第１の電極１０２が形成されている。この上に、赤、緑、青のいずれか一つの発光をする有機化合物層１０３をマスク２０１の貫通孔２０２を通じて形成する。次にマスク２０１を隣の副画素の位置まで水平方向にシフトし、別の一つの発光をする有機化合物層１０３をマスク２０１の貫通孔２０２を通じて形成する。こうして３回の操作を繰り返すことにより赤、緑、青の各色の有機化合物層１０３をそれぞれ所定の位置に堆積する。最後に全体に第２の電極１０４を形成し、必要ならばさらに保護層１１１を形成して、カラー画像表示パネルを得る。

【００１５】

図１５は、図１４のマスク２０１のＢ－Ｂ’の断面図である。高解像度のカラー画像表示パネルでは、マスク２０１の厚さに匹敵するほど副画素の幅が小さくなる。真空堆積が迅速に行える大きな材料放射源を用いるとき、マスク２０１の小さな貫通孔２０２の中央

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と周辺部とで堆積物の厚さが異なることを軽減するためには、マスク２０１の厚みを薄くする必要がある。しかしマスク２０１は、そのものの耐久性や取扱いの容易性を確保するために、通常少なくとも数十μｍ程度以上の厚みが必要である。そこで図１５のようにマスク２０１の材料放射源側で貫通孔２０２が広がるように削り部分２０３を形成することにより、マスク２０１を厚くして強度を確保しながら、貫通孔２０２の周辺部分を薄くしたマスクが用いられる。

【００１６】

【特許文献１】特開２００２－１１０３４５号公報

【特許文献２】特表２００４－５１６６３０号公報

【発明の開示】

【発明が解決しようとする課題】

【００１７】

２種以上の異なる発光色を有する有機ＥＬ素子を配列したカラー画像表示パネルにおいて、長方形の副画素の配列を上記のデルタ配列やスクランブル配列とする場合には、マスクを用いた真空堆積工程に以下のような問題がある。

【００１８】

図１６は、副画素の配列をデルタ配列とするための真空堆積工程用マスクの模式図である。図において（ａ）は材料放射源側から見たマスクの平面図で、そのＣ－Ｃ’の断面図が（ｂ）である。上記のように貫通孔２０２を材料放射源側ほど大きくなるように削り部分２０３を形成すると、貫通孔２０２の角が近接する部分でそれぞれの削り部分２０３の干渉が起こり、マスク２０１が著しく薄くなる部分ができる。

【００１９】

そのため、外力が加わると特定方向に裂けやすい、強度に問題のあるマスクとなる。強度の不十分なマスクはそれ自体の作成に時間とコストを浪費するばかりでなく、真空堆積工程に繰り返し使用できる回数も短くなる。また充分な張力を加えてマスクを治具に固定することができないため、真空堆積工程の位置精度が低くなり高精細の画像表示パネルを製造する場合に歩留まりが悪くなる。スクランブル配列では特に干渉が強く起こる部分があるため（不図示）斜め方向に特に裂け易く、さらにマスクの作成が困難になる。

【００２０】

貫通孔２０２の大きさを小さくして上記の干渉が起こらないようにするとマスクの強度は確保できる。しかし、各副画素の面積が減少するので所定の発光の明るさを得るには素子の電流密度を上げねばならず、画像表示パネルの発光電流効率や駆動寿命に悪い影響を及ぼす。

【００２１】

つまり、上記のように真空堆積工程を用いて製造した、副画素の配列がデルタ配列やスクランブル配列となるカラー画像表示パネルには歩留まり、コスト、性能、寿命等において改善すべき課題がある。この画像表示パネルを部品として用いた画像表示装置にも課題が継承され、コスト、性能、寿命等に課題がある。

【００２２】

言い換えるならば、従来のデルタ配列やスクランブル配列の位置に並んだ長方形副画素の配列を有するカラー画像表示パネルには、マスクを用いた真空堆積工程で副画素を作成する場合に、副画素の開口率を大きくすることが難しいという問題がある。この原因は副画素の角部が近接する部分が存在することにある。ここに述べた課題は、カラー画像表示パネルを開口率の大きなマスクを介して真空堆積する工程により製造する場合に明らかになるものである。

【００２３】

本発明は、上記のような課題を解決し、副画素の配列がデルタ配列やスクランブル配列などの画像表示パネルと同様の表示性能を有する、カラー画像表示パネル及びその製造方法、並びにカラー画像表示装置を提供することを目的とする。さらに、本発明は、強度に問題のないマスクを用いた真空堆積工程で作製することのできる、カラー画像表示パネル

及びその製造方法、並びにカラー画像表示装置を提供することを目的とする。

【課題を解決するための手段】

【００２４】

上記の課題を解決するための本発明のカラー画像表示パネルは、

基板上に形成された第１の電極上に、真空堆積法で有機発光層が堆積され、さらに第２の電極が形成されてなる、少なくとも赤、緑、青の発光色を有する有機ＥＬ素子が一定の順に並んで構成される画素が複数配列された有機エレクトロルミネッセンス型二次元カラー画像表示パネルにおいて、

各々の有機ＥＬ素子は平面形状において一組の平行な二辺を有しており、

互いに他色の発光色を有する有機ＥＬ素子が、前記平行な二辺で隣接しており、同一の発光色を有する有機ＥＬ素子は、前記平行な二辺の平行線方向に隣接して、垂直線に対して傾斜して平行に並ぶストライプ状に配列されていることを特徴とする。

【発明の効果】

【００２５】

本発明によれば、副画素の配列がデルタ配列やスクランブル配列と同様の自然画像表示性能を有しながら、作成が容易なストライプ状の貫通孔を有するマスクを利用して製造できる。そのため、コスト、表示の明るさなどの性能、寿命等において優れたカラー画像表示パネルを得ることができる。

【００２６】

また、本発明によれば、副画素の配列がデルタ配列やスクランブル配列と同様の自然画像表示性能を有する画像表示パネルの製造方法において、作成が容易で、耐久性のあるマスクを利用するため、製造コストや歩留まりの改善された製造方法とすることができる。

【００２７】

さらに、本発明によれば、副画素の配列がデルタ配列やスクランブル配列と同様の自然画像表示性能を有しながら、コスト、表示の明るさなどの性能、寿命等において優れた有機エレクトロルミネッセンス型カラー画像表示装置を得ることができる。

【発明を実施するための最良の形態】

【００２８】

図１は本発明のカラー画像表示パネル（以下、単に画像表示パネルと省略する場合がある。）の実施形態を示した平面模式図である。

【００２９】

図示する画像表示パネルは、基板上に形成された第１の電極上に、真空堆積法で有機発光層が堆積され、さらに第２の電極が形成されてなる、赤、緑、青の発光色を有する有機ＥＬ素子が一定の順に並んで構成される画素が複数配列された有機ＥＬ型二次元カラー画像表示パネルである。

【００３０】

各々の有機ＥＬ素子は平面形状において一組の平行な二辺を有している。ちなみに、本実施形態では平行四辺形の有機ＥＬ素子とされている。従って前記素子は平行な長辺一組と平行な短辺一組を有し、平面内の素子の重心は平行な二辺から等距離にある。

【００３１】

互いに他色の発光色を有する有機ＥＬ素子が、長辺で隣接しており、同一の発光色を有する有機ＥＬ素子は、短辺（すなわち、平行な長辺の平行線方向）で隣接している。前記有機ＥＬ素子は、重心位置を結ぶ一本の第１の直線ｓが、前記有機ＥＬ素子の長辺に対して平行となる形態で、ストライプ状に配列されている。この有機ＥＬ素子が配列されてなるストライプは、相互に重なることなく、垂直線ｖに対して傾斜して平行に並べられている。

【００３２】

特に、本実施形態では、水平方向に隣接するように配列された、前記赤、緑、青の発光色を有する有機ＥＬ素子を副画素１０５の一組として画素が形成されている。そして、水平方向に隣接する前記画素は、その重心位置を結ぶ第２の直線ｈが水平線に対して平行と

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なるように配列されている。また、副画素１０５の短辺は水平線に対して平行となるように配置される。

【００３３】

つまり、平行四辺形の有機ＥＬ素子からなる副画素１０５はその重心位置を水平方向に引いた直線（第２の直線）ｈに一致させ、さらに一組の平行な二辺を斜め線（第１の直線）ｓの方向に一致させている。同一の発光色を有する前記有機ＥＬ素子は前記斜め線ｓの方向に複数並んだ形態で、ストライプ状に配列している。前記斜め線ｓは垂直線ｖから傾いている。

【００３４】

なお、各有機ＥＬ素子には有機発光層と第１、第２の電極が存在し、これらの電極を駆動する配線、やトランジスタなど（不図示）が接続されて各素子が個別に駆動可能とされている。テレビジョン信号の二次元画像表示の伝統から、ここでは画素データが早い周期で一括書込みされる方向を水平方向、前記の一括書き込みより遅い周期で画像データが位置を逐次ずらしながら繰り返し書き込みされる方向を垂直方向と呼ぶことにする。水平線、垂直線についても、それぞれ前記の水平方向の直線、垂直方向の直線の意味で用いる。

【００３５】

副画素１０５の配列の傾き、すなわち第１の直線ｓの傾きの大きさは、次のように導き出せる。すなわち、任意の副画素１０５の重心位置と前記副画素１０５と垂直方向に隣接する同一の発光色を有する副画素の重心位置との水平方向のずれ量ｋと、水平方向に隣接する同一の発光色を有する副画素の繰り返しピッチｒとの比の値ｋ／ｒで導き出せる。図１は前記の傾きの値が１／２となるものを示している。

【００３６】

この傾きが１／２である場合、平行四辺形の副画素１０５の重心位置は図１３（ｂ）に模式的に例示したデルタ配列の長方形副画素の重心位置と同等となる。したがって、この配列の画像表示パネルは、従来の長方形副画素がデルタ配列の画像表示パネルと同等の駆動データを同等の駆動タイミングで供給することにより、同等のカラー画像の表示を得ることができる。

【００３７】

すなわち、図１の副画素１０５の形状と配列を有する画像表示パネルは、長方形副画素がデルタ配列の画像表示パネルと置き換え可能である。画像入力信号から各副画素の駆動信号を生成する画像表示パネル制御用回路や制御用集積回路には従来のものを利用することができる。また、基板として第１の電極を駆動するトランジスタを形成したアクティブマトリクス回路付きのものを用いる場合、デルタ配列の長方形副画素を駆動するためのアクティブマトリクス回路と同じ設計のものを使用することができる。前記アクティブマトリクス回路の上に形成する、第１の電極や有機発光層の形状と配列は図１に例示されたものにすればよい。

【００３８】

図１では、平行四辺形の副画素１０５の長辺が画面の左方向に傾いた例を示したが、傾斜の向きが右方向である場合でも同様に、デルタ配列の長方形副画素と重心位置が対応することは明らかである。また図１では、副画素１０５の色の並び順を左からＢ、Ｇ、Ｒの順を示したが、もちろんＲ、Ｇ、Ｂの順などとしても何ら問題が無い。

【００３９】

さらにカラー表示範囲を広げる目的で三原色以外の色の副画素を加えて、１画素を４つの副画素により構成するときも同様である。４副画素分の水平方向のピッチをｒ、垂直方向に隣接する同一の発光色を有する副画素の重心位置相互のずれ量をｋとすると、ｋ／ｒの比が１／２となる場合に三原色の副画素がデルタ配列の画像表示パネルと同様に表示の解像感が高く感じられる。一般に１画素をｎ個の副画素で構成する場合、上記と同様にｋ／ｒの比が１／２となるようにすると、三原色の副画素がデルタ配列の画像表示パネルと同様に表示の解像感が高く感じられる。

【００４０】

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三原色の副画素からなる前記の配列の傾きが１／２でなく１／３である場合は、平行四辺形の副画素１０５の重心位置が、スクランブル配列の長方形副画素の重心位置と同等となる。すなわち前記傾きが１／３である配列を有する画像表示パネルは、長方形副画素がスクランブル配列の画像表示パネルと置き換え可能である。基板としてアクティブマトリクス回路を形成したものを用いる場合についても長方形副画素がスクランブル配列用のものと同じ設計のアクティブマトリクス回路を利用できる。

【００４１】

傾きが前記した１／２と１／３以外の場合、従来の長方形副画素の場合のデルタ配列やスクランブル配列との対応は無い。しかし、二次元の規則的カラー画素配列であるので、所定の二次元のカラー画像表示のための各副画素に与える駆動電流の値は必ず決めることができ、所望の画像表示が可能である。前記の傾きが小さい場合、従来の垂直ストライプの場合との差異がなくなり自然画像の表示における解像向上の利点が小さくなる。

【００４２】

一方、前記平行四辺形の副画素の傾きが大きいと副画素の幅は狭くなるため、非画素部分に対する副画素の占有面積比が減少し、画像表示パネルの明るさの低下や素子電流密度の増加、駆動寿命の短縮といった悪影響が無視できなくなる。

【００４３】

したがって、前記傾きの値の好適な範囲に原理的制限は無いが１／５から１／１の範囲が実用的に有効であり、従来のデルタ配列やスクランブル配列の設計が利用可能な１／３と１／２において特に有効である。

【００４４】

図１の副画素１０５の形状と配列の画像表示パネルでは、同一の発光色を有する副画素１０５のみが直線状に配列されている。つまり、同一の発光色を有する副画素１０５は、垂直方向に隣接する前記副画素１０５の重心位置を結ぶ一本の第１の直線ｓが、前記副画素１０５の平行な二辺に対して平行となる形態で、ストライプ状に配列されている。この有機ＥＬ素子が配列されてなるストライプは、相互に重なることなく、垂直線ｖに対して傾斜して平行に並べられている。そのため、各副画素１０５の材料をマスクを通じて基板に堆積する工程において、図２に模式図で例示するようなストライプ状の貫通孔２０２を有するマスク２０１を用いることができる。

【００４５】

図２（ａ）はストライプ状の貫通孔部分の説明図である。マスク２０１に形成されたストライプ状の貫通孔２０２の間隔は副画素配列ピッチの２倍あるため、隣接する貫通孔の削り部分２０３が相互に干渉し合うことなく作成することが可能である。

【００４６】

なお、前記貫通孔２０２は図２（ｂ）に模式的に示すように、マスク２０１に対して斜めに形成してもよいが、図２（ｃ）に示すようにマスク２０１の全体形状に沿って平行に形成し、このマスク２０１を面内で斜めに回転させて用いても良い。マスク２０１は所定の張力を与えて治具に固定して用いることが多いので、図２（ｃ）のように加工すると、ストライプ方向に均等に張力を加えやすいので都合がよい。その場合、基板上の画像表示領域以外に材料が堆積されることを防ぐために、前記画像表示領域の形状に対応した開口を有する第２のマスクを重ねて用いてもよい。

【００４７】

また、基板の背面に磁石を配して磁性材料からなるマスクを磁力により所定の位置に定位させる方法を用いてもよい。

【００４８】

図２のようなマスク２０１を用いると真空堆積材料が貫通孔２０２の形状に従い複数の隣接する副画素１０５に跨って有機化合物層として堆積される。しかし、通常第２の電極も同様に隣接する副画素１０５に跨って形成されて共通電極とされるので、前記有機化合物層を隣接する副画素１０５の間で切断しなくとも、素子間のクロストーク電流は特に問題にはならない。

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【００４９】
また、各副画素１０５の形状は有機層の堆積領域の形状ではなく、基板上の第１の電極及び通常、第１の電極の周縁部に形成された素子分離膜の形状により定まる。この観点からも、ストライプ状の堆積層が隣接する副画素間に跨ることは問題にならない。
【００５０】
図３は、本発明の画像表示パネルの別の副画素の形状と配列の一例を示す平面模式図であって、長方形の副画素をなす素子が傾いて配列している様子を示している。
【００５１】
図３（ａ）でも、図１と同様に、同一の発光色を有する副画素１０５のみが直線状に配列されている。傾きを図１の場合と同様に垂直方向に隣接する副画素の重心位置の水平方向のずれ量ｋと、水平方向に隣接する同一の発光色を有する副画素の繰り返しピッチｒとの比の値ｋ／ｒは１／３である。したがって、各副画素の重心位置が図１３（ｃ）に模式的に例示したスクランブル配列の長方形副画素の重心位置と同等となる。この画像表示パネルでは、従来の長方形副画素がスクランブル配列の画像表示パネルと同等の駆動データを同等の駆動タイミングで供給することにより、同等のカラー画像の表示を得ることができる。
【００５２】
図３（ｂ）は、長方形の副画素の重心を僅かに移動し、副画素からなる各画素を正方形とした例である。この例でも図３（ａ）と同様に傾きを表すｋ／ｒの値は１／３である。
図４は、本発明の画像表示パネルのさらに別の副画素の形状と配列の一例を示す平面模式図であって、さらに異形の副画素をなす素子が傾いて配列している様子を示している。
図４（ａ）と（ｂ）は、副画素の素子形状として台形のものを用いた例を示している。いずれの例も、同一の発光色を有する副画素のみが直線状に配列されており、傾きの値を表すｋ／ｒは１／２である。
【００５３】
図５は、多角形の形状を有する副画素を持つ、本発明の画像表示パネルの一例を示す平面模式図である。図５でも、同一の発光色を有する副画素のみが直線状に配列されており、傾きの値を表すｋ／ｒは１／２である。
【００５４】
図６は、長方形の頂点部分が曲線状の形状を有する副画素を持つ、本発明の画像表示パネルの一例を示す平面模式図である。図６でも、同一の発光色を有する副画素のみが直線状に配列されており、傾きの値を表すｋ／ｒは１／２である。
【００５５】
図７は、曲線を含む輪郭形状を有する副画素を持つ、本発明の画像表示パネルの一例を示す平面模式図である。この例における副画素は平行な二辺と、曲線とにより囲まれた形状をしている。図７でも、同一の発光色を有する副画素のみが直線状に配列されており、傾きの値を表すｋ／ｒは１／２である。
【００５６】
本発明の画像表示パネルの製造方法は、基板上に二次元に配列した複数の第１の電極を形成する工程を有する。そして、少なくとも赤、緑、青の発光色を有する有機発光材料を、それぞれの発光色ごとに、複数の貫通孔を有するマスクの前記貫通孔を通じて前記第１の電極の形成位置に堆積する工程を有する。さらに、第２の電極を形成する工程を有する。
【００５７】
つまり、通例の有機エレクトロルミネッセンス型二次元カラー画像表示パネルの製造方法と略同様である。しかし、複数の第１の電極を形成する工程では、一組の平行な二辺を有する平面形状の第１の電極を、前記平行な二辺の第一の辺が直線上に並び、前記平行な二辺の第二の辺もまた直線上に並ぶように一次元に配置される。前記電極の一次元配列が垂直線に対して傾斜して平行に並ぶストライプ状となるように二次元に並べられる。
【００５８】

そして、有機発光材料を堆積する工程では、前記第１の電極が形成されてなるストライプに対応するように貫通孔がストライプ状に形成されたマスクを、前記第１の電極が形成されてなるストライプと前記マスクの貫通孔とを対向させるように位置合わせする。その後、前記マスクの貫通孔を通じて有機発光材料の堆積を行うことを特徴とする。

【００５９】

具体的に云うと、前記マスクを用いた材料の真空堆積工程は、少なくとも発光層の形成において行われる。

【００６０】

図２に例示したマスク２０１を、その削り部分２０３が材料放射源側となるようにして基板に近接させ、ストライプ状の貫通孔２０２を基板上の所定の色の副画素の並びの上に重ねるように位置合わせを行う。圧力を１０－４Ｐａ程度に減圧して材料放射源から所定の材料を所定量だけ堆積させ、貫通孔２０２の位置に対向した基板上の副画素の並びに、前記材料を成膜する。複数の種類の材料の混合層を堆積する場合には、材料の種類の数だけ別の材料源を用意して前記成膜を行う。

【００６１】

次に、別の発光色を有する副画素に対して別の材料を堆積する場合には、前記マスク２０１を面方向に１副画素のピッチだけシフトして、貫通孔２０２を別の色の副画素の並びに対向するように位置合わせを行う。そして、前記と同様にして別の発光色を有する副画素の並びに別の材料を成膜する。これを繰り返して各色の副画素に対する成膜を行う。又は、別の発光色を有する副画素に対する材料堆積の工程それぞれのために、専用の図２に例示したマスク２０１を別々に用意しても良い。この場合、別の発光色を有する副画素の堆積を行う都度、それぞれ前記別のマスク２０１を基板に対して位置合わせを行い、材料放射源から貫通孔２０２を通じて材料を基板上に堆積して成膜を行う。

【００６２】

別の発光色を有する副画素に対して発光層以外についても、層の材料の組成・種類や堆積量を副画素の色に応じて変える必要がある場合には、上記と同様にして図２に例示したマスク２０１を用いた工程を利用することができる。

【００６３】

例えば、後述する各素子の層方向に光干渉構造を有した画像表示パネルを製造する場合などにおいて、発光層以外についてもそれぞれ発光波長に応じた所定の厚みにする必要がある。また、発光層に電荷を受け渡す電子輸送層やホール輸送層等は材料のＬＵＭＯ、ＨＯＭＯ準位が発光層のそれぞれの準位と適切な関係のものを選ぶ必要があるため、発光層材料に応じて変える場合がある。したがって、これらの場合にも前記のマスク２０１を用いて貫通孔２０２を通じて所定の位置に選択的に堆積を行う。

【００６４】

なお、図３から図７に例示したいずれの副画素の形状と配列の画像表示パネルにおいても、図１と同様に副画素が平行な二辺を有し、同一の発光色を有する副画素を前記二辺の方向に直線状に配列している。したがって、いずれの画像表示パネルの製造においても、上述した図２に例示するような貫通孔２０２を有するマスク２０１を用いた真空堆積工程を利用できる。

【００６５】

次に上記のような副画素の形状と配列を有する画像表示パネルの層構成例について説明する。なお、本発明は層構成、構成材料、各層の厚み等により制限されるものではない。

図８は各有機ＥＬ素子の層構成例を説明する断面図である。（ａ）は基板側陽極型の模式図で第１の電極が陽極、第２の電極が陰極である。（ｂ）は基板側陰極型の模式図で第１の電極が陰極、第２の電極が陽極である。図において１０１は基板、１０２は第１の電極、３０１はホール注入層、３０２はホール輸送層、３０３は発光層、３０４は電子輸送層、３０５は電子注入層、１０４は第２の電極、１１１は保護層である。３０１から３０５の各層は図１１及び図１２において有機化合物層１０３とまとめて記載されたものと同じものを表す。図８は素子の発光が起こる部分の説明の図であるため、図１２に記載の素

子分離膜１１０は不図示である。また、各素子の駆動にアクティブマトリクス回路が用いられる場合は駆動用トランジスタや第１の電極への接続部などが基板１０１の表面に形成されるが、これも不図示である。

【００６６】

基板１０１は、本発明の画像表示パネルの各素子等を表面に機械的に保持するものであって、ガラス、石英やアルミナ等のセラミクス、ポリエチレンナフタレートやポリエーテルエーテルケトン、ポリアミドイミド、ポリイミド等のプラスチックが用いられる。また、ニッケル鋼やステンレス鋼、アルミニウムやチタン等の金属、セラミクスや金属等の繊維状あるいは粉末状の充填材を内部に含んだ、プラスチックやガラス等の複合材料などが用いられる。なお、第１の電極１０２を表面に複数形成し、それらを独立に駆動する必要があるので、基板１０１が導電性である場合はその表面に絶縁層を形成して用いる。

【００６７】

基板１０１の必要とする厚みは画像表示パネルの製造時の取り扱いに必要な強度、及び完成した画像表示パネルの必要強度とから決まるものである。これは前記画像表示パネルの広さとも関わるので一概には言えないが、ガラス、セラミックス等の脆い材料の場合０．３ｍｍから２ｍｍ、プラスチックや金属のような変形に強い材料では０．１ｍｍから２ｍｍ程度が適当である。

【００６８】

第１の電極１０２の材料は、アルミニウム、クロム、ニッケル、銀等の金属、或いは合金、酸化錫、インジウム錫酸化物、インジウム亜鉛酸化物、亜鉛酸化物等の導電性酸化物などが用いられる。前記の金属や導電性セラミクスが単独で用いられても、２層又はそれ以上に重ねて用いられても良い。

【００６９】

第１の電極１０２の個々の平面形状と相互の配列については上述したが、形状と配列を形成するパターニング手段は、例えば湿式、或いは乾式のエッチング技術や、マスクを用いた選択堆積技術、インクジェット技術など従来公知のものから選んで用いればよい。

【００７０】

第１の電極１０２に必要な厚みは、個々の電極内で電位分布が充分小さくなるように選ばれるもので、素子駆動時の電流や材料の伝導度、電極への電流の供給方法などに依存し、通常は金属材料で数１０ｎｍ以上、導電性酸化物材料で数１００ｎｍ以上が選ばれる。もちろん充分な厚みの金属材料を下地に有し、導電セラミクス材料を表面とする複合電極の場合は前記導電性酸化物材料が１００ｎｍ以下であっても問題ない。

【００７１】

素子分離膜の材料は、アクリル樹脂、ポリイミド樹脂等のプラスチックや酸化シリコン、窒化シリコンや酸化アルミニウム等のセラミックスなどの絶縁性材料から選ばれる。プラスチックの場合は、特に光レジスト材料として知られるものを使用してパターニングを行うのが便利である。セラミックスを用いる場合は、マスクを用いた選択堆積技術やレジスト材料を用いたエッチング技術により所望のパターニングを行う。

【００７２】

素子分離膜は上記第１の電極１０２の周縁部を囲むように形成される。素子分離膜は後に行われるマスクを用いた真空堆積工程時に、マスクが素子部に直接接触して堆積膜を傷つけることを防止する役割を持つ。そして、後に第２の電極１０４を形成した際に第１の電極１０２との間で欠陥による短絡を防止する役割を持つ。さらに、前記第１の電極１０２の端部の段差部を被覆することにより短絡を防止するなどの役割を持つ。このような素子分離膜の厚さは２００ｎｍから４μｍの間がよく用いられる。

【００７３】

ホール注入層３０１は、接する電極（陽極）からホールを引き出し後述のホール輸送層３０２に受け渡す役割を有する。その材料としては、酸化モリブデン、酸化タングステン、酸化バナジウム等の遷移金属酸化物や、銅フタロシアニン等の遷移金属錯体などが挙げられる。なお、陽極材料がインジウム錫酸化物やインジウム亜鉛酸化物等の金属酸化物か

らなる場合などで、後述のホール輸送層３０２に対して直接、ホールが注入可能な場合にはホール注入層３０１を省略してもよい。

【００７４】

ホール注入層３０１を設けると、図８（ｂ）の構成の素子を作成する場合、第２の電極１０４を堆積する工程でホール注入層３０１以下の有機化合物層が受けるダメージを低減する効果が期待できる。

【００７５】

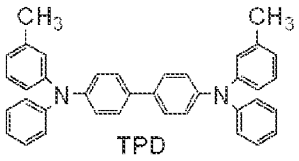
ホール注入層３０１の厚みは通常２ｎｍから１００ｎｍ程度が用いられる。ホール注入層３０１は上記の材料をマスク真空堆積工程などで素子形成部分に選択堆積してもよいが、基板１０１上に非選択的に形成してもよい。

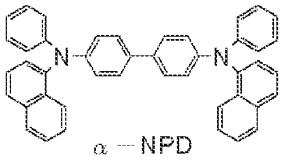
【００７６】

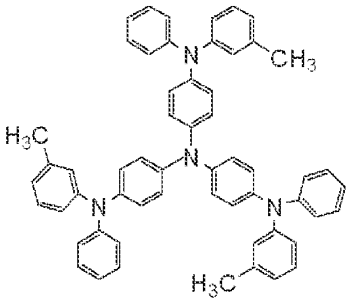
ホール輸送層３０２は、注入されたホールを後述の発光層３０３に受け渡す役割を有する。これを構成するホール輸送材料は、ホールの注入が容易で、またホールを発光層３０３に輸送するに優れたモビリティを有することが好ましい。電子の輸送性は低くてよい。ホール注入輸送性を有する低分子系材料としては、トリアリールアミン誘導体、フェニレンジアミン誘導体、トリアゾール誘導体、オキサジアゾール誘導体、イミダゾール誘導体、ピラゾリン誘導体が挙げられる。また、ピラゾロン誘導体、オキサゾール誘導体、フルオレノン誘導体、ヒドラゾン誘導体、スチルベン誘導体、フタロシアニン誘導体、ポルフィリン誘導体が挙げられるが、もちろんこれらに限定されるものではない。以下に、具体例の一部を示す。

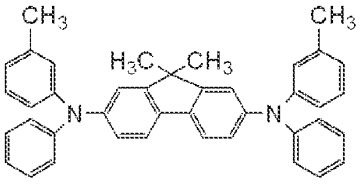
【００７７】

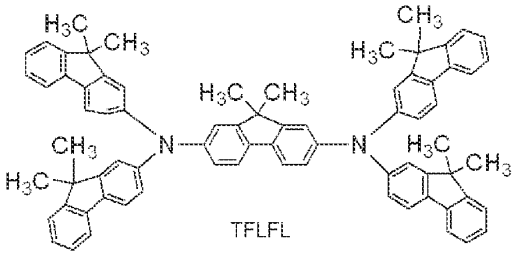
【化１】

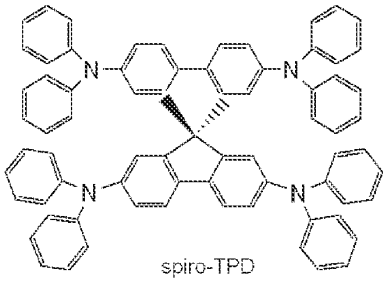

TPD

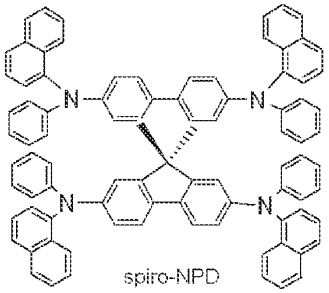

α－NPD

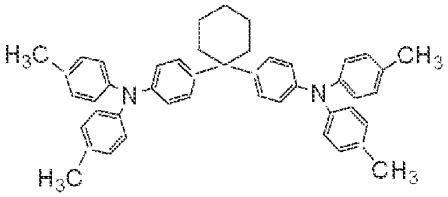

m-MTDATA

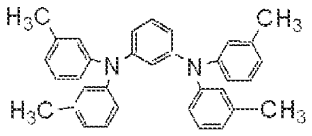

DTDPFL

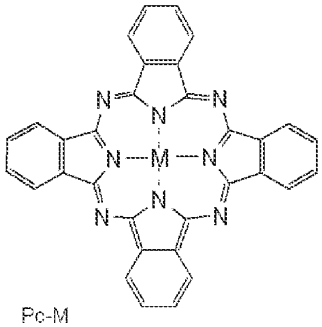

TFLFL


spiro-TPD


spiro-NPD


TPAC


PDA


Pc-M
M : Cu, Mg, AlCl, TiO, $SiCl_2$, Zn , Sn,
MnCl, GaCl, etc

【００７８】

また、高分子のホール輸送材料も知られており、ポリ（ビニルカルバゾール）、ポリ（シリレン）、ポリ（チオフェン）、その他導電性高分子が利用可能である。

【００７９】

ホール輸送材料は単独で用いてもよいが、複数の材料を混合してホール輸送層３０２を形成してもよい。

【００８０】

ホール輸送層３０２は、上記したホール輸送材料をマスクを用いた真空堆積工程などで素子形成部分に選択堆積してもよいが、基板１０１上に非選択的に形成してもよい。高分子材料は適当な溶液を回転塗布法などで成膜し溶媒を乾燥除去するのが普通である。ホール輸送層３０２の厚みは５ｎｍから２００ｎｍとする。

【００８１】

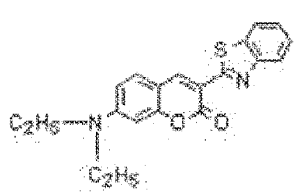
発光層３０３は、前記ホール輸送層３０２からホールを注入され、また後述の電子輸送層３０４から電子が注入されて、層内で両電荷が相殺する際に生じる励起状態により発光する役割を有する。発光材料としては、発光効率の高い蛍光材料や燐光材料が用いられる。発光材料を単独で用いて発光層を形成することもあるが、励起分子の濃度を下げて非発光失活を減らす効果等を目的として発光材料とキャリア輸送材料とを混合して発光層を形成することがよく行われる。このキャリア輸送材料には、前記したホール輸送材料のほか、後述する電子輸送材料や、ホールと電子との両方に対して適当な移動度を有する両極性輸送材料が利用できる。単独で発光性を有する材料であっても、より励起エネルギーの低い発光材料と混合すると、それ自身の発光は抑制されるのでキャリア輸送材料として利用できるものがある。発光層３０３の厚みは５ｎｍから２００ｎｍ程度とする。

【００８２】

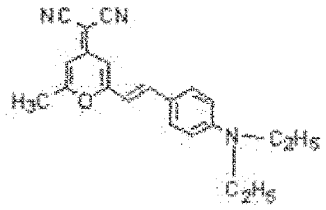
発光材料の具体例の一部を示す。本発明はこれらに限定されるものではない。

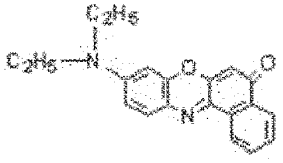
【００８３】

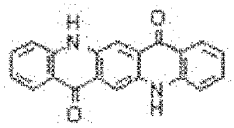
【化２】

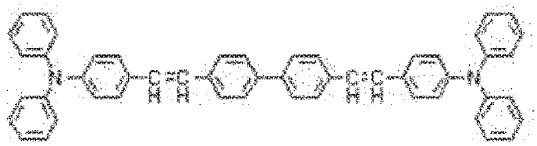


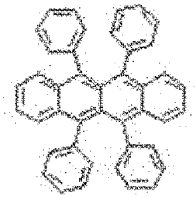
クマリン6

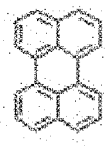


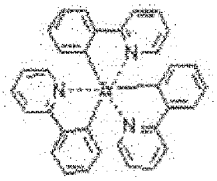






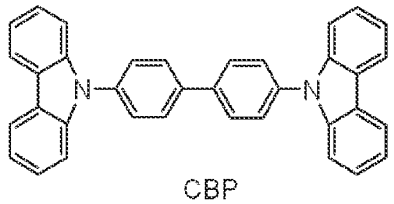






【００８４】

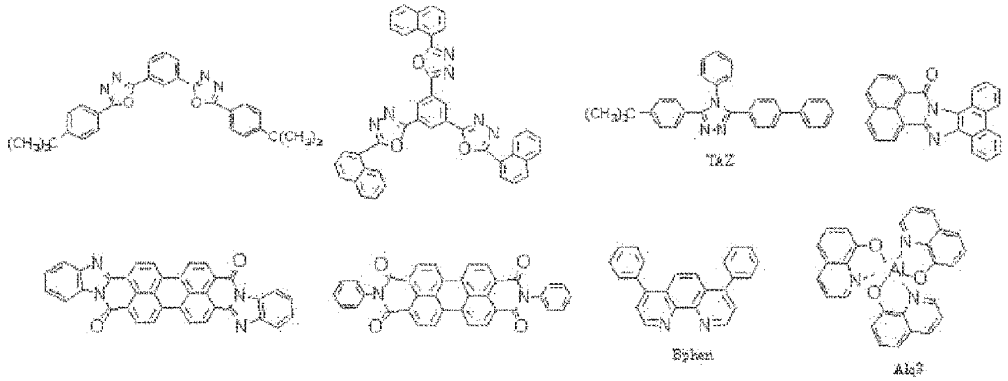
【化３】
両性輸送性発光材料



CBP

【００８５】
電子輸送層３０４は、後述する電子注入層３０５から注入された電子を、前記発光層３０３に受け渡す役割を有する。その材料としては、注入された電子を輸送する機能を有するものから任意に選ぶことができ、ホール輸送材料のキャリア移動度とのバランス等を考慮し選択される。電子注入輸送性能を有する材料としては、オキサジアゾール誘導体、オキサゾール誘導体、チアゾール誘導体、チアジアゾール誘導体、ピラジン誘導体、トリアゾール誘導体、トリアジン誘導体、ペリレン誘導体が挙げられる。また、キノリン誘導体、キノキサリン誘導体、フルオレノン誘導体、アントロン誘導体、フェナントロリン誘導体、有機金属錯体等が挙げられるが、もちろんこれらに限定されるものではない。以下に、具体例の一部を示す。

【００８６】
【化４】
電子輸送性発光材料



【００８７】
電子輸送層３０４は、上記した電子輸送材料をマスクを用いた真空堆積工程などで素子形成部分に選択堆積してもよいが、基板１０１上に非選択的に形成してもよい。電子輸送材料は単独で用いてもよいが、複数の材料を混合して電子輸送層を形成してもよい。電子輸送層３０４の厚みは２ｎｍから８０ｎｍの範囲とする。

【００８８】
電子注入層３０５は、接する電極（陰極）から電子を引き出し電子輸送層３０４に受け渡す役割を有する。電子注入材料としては、前述した電子輸送性材料に、リチウムやセシウム等のアルカリ金属やマグネシウム、カルシウム等のアルカリ土類金属、若しくはその化合物を用いることができる。例えば炭酸セシウム等を０．１％～数十％含有させて電子注入性を付与したものを用いることができる。また、フッ化リチウムのようなアルカリ金属塩を電子注入層として用いることができる。

【００８９】
電子注入層３０５は必須な層ではないが、界面に大きな電位降下を生じることなく、接する電極から電子を取り出す効果が期待できる。また、図８（ａ）の構成の素子を作成す

BOE
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る場合、第２の電極１０４を堆積する工程で電子輸送層３０４以下の有機化合物層が受けるダメージを低減する効果が期待できる。電子注入層３０５は良好な電子注入性や前記のダメージ低減効果等を確保するために２ｎｍから１００ｎｍ程度挿入するのが好ましい。

場合によっては、作成された素子が酸素や水分等と接触することを防止する目的で保護層１１１が設けられる。保護層１１１としては、窒化シリコン、窒化酸化シリコン等の金属窒化物膜や、酸化タンタル等の金属酸化物膜、ダイヤモンドライクカーボン（ＤＬＣ）薄膜が挙げられる。また、フッ素樹脂、ポリパラキシレン、ポリエチレン、シリコーン樹脂、ポリスチレン樹脂等の高分子膜、さらには、光硬化性樹脂等が挙げられる。

【００９０】

また、図８のように第２の電極１０４に重ねて保護層１１１を設けなくとも、不浸透性のキャップを被せることにより素子を保護することもできる。すなわち、窒素やアルゴンなど不活性雰囲気、或いは減圧雰囲気下で前記の素子形成部分をガラス、気体不透過性フィルム、金属など（不図示）でカバーし、適当な封止材料により基板１０１の成膜部分全体をパッケージングすることで保護を行うこともできる。

【００９１】

防湿性を高めるために、前記保護層１１１内や前記パッケージ内に吸湿材を含有、或いは配置しても良い。

【００９２】

基板１０１と第１の電極１０２とを透光性とした場合、発光層３０３で生じた光を基板１０１側から取り出せるボトムエミッション構成の画像表示パネルとなる。この場合、基板１０１及び第１電極１０２は、発光層３０３に生じる光の主要波長に対して５０％以上の透過率を有するべきである。

【００９３】

また、基板１０１の表面に配線やアクティブマトリクス回路がある場合、ボトムエミッション構成の画像表示パネルではそれらの回路も基板１０１側への光の透過性を阻害しないように設計する必要がある。

【００９４】

前記のボトムエミッション構成の画像表示パネルでは、第２の電極１０４側に光反射面を設けることにより基板１０１側に取り出せる光を増して表示される画像を明るくすることができる。反射面としては金属面や、屈折率の異なる透明層の界面などを用いることができる。例えば第２の電極１０４を金属とすることや、第２の電極１０４を透明材料と金属との積層とすることで構成できる。第２の電極１０４を透明材料としても、第２の電極１０４上に屈折率の異なる透明材料を積層（不図示）することで基板１０１側に取り出せる光を増すことが可能である。前記光反射面の反射率は７０％以上とすべきである。

【００９５】

第２の電極１０４及び保護層１１１を透光性とした場合、発光層３０３で生じた光を基板１０１と反対側から取り出せるトップエミッション構成の画像表示パネルとなる。この場合、前記第２の電極１０４及び保護層１１１は、発光層３０３に生じる光の主要波長に対して５０％以上の透過率を有するべきである。トップエミッション構成の画像表示パネルでは、第１の電極１０２側に光反射面を設けることにより、基板１０１と反対側に取り出せる光を増して表示される画像を明るくすることができる。上記のボトムエミッション構成の場合と同様に、反射面としては金属面や、屈折率の異なる透明層の界面などを用いることができる。前記光反射面の反射率は発光層３０３に生じる光の主要波長に対して７０％以上とすべきである。

【００９６】

前記反射面と発光層との光学距離を調節し、発光層３０３から直接、取り出される光と反射面で反射されてから取り出される光とが強め合う条件を満たすと、特定の波長の光を強く取り出すことができる。金属面のような固定端反射面の場合、反射で光の位相が約１８０度ずれるので、発光層３０３内の発光が起こる位置と反射面との光学距離を光の波長の約ｎ／４倍（ｎは奇数）とすると前記の条件が満たされる。屈折率のより低い材料に接

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する透明体界面のような開放端反射面の場合、反射で光の位相がほとんどずれないで、発光層３０３と反射面との光学距離を光の波長の約ｎ／２倍（ｎは自然数）とすると前記の条件が満たされる。さらに光の取り出し側にも、光を一部反射する半透過反射面を形成し上記と同様に発光層３０３と半透過反射面との光学距離を調節することにより、特定の波長の光に対する微小共振器構造を形成することもできる。

【００９７】

上記のような光の干渉による波長選択構造を用いることにより、画像表示パネルを構成する各副画素（赤、緑、青）に対してそれぞれ所定の波長を強めれば、それぞれの発光が高い彩度となる。そのため、表示のＧＡＭＵＴが広くなり、色の再現範囲を改善することができる。

【００９８】

なお、反射面における前記位相ずれの大きさは、実際には反射界面を形成する材料の物性や厚み等に依存し、発光層３０３の層内で主に発光が生じている位置や、各堆積層の屈折率の値などに若干の不確定要素がある。そのため、実際に素子を試作して適切な光干渉構造を見出すのがよい。

【００９９】

基板１０１、第１の電極１０２、第２の電極１０４及び保護層１１１を透光性（半透過性も含む）とした場合、発光層３０３で生じた光を両面から取り出せる、両面画像表示パネルとなる。

【０１００】

また、複数の有機ＥＬ素子が積層されたマルチフォトン構成や多段階積層構成に対しても本発明は実施可能である。所望の光学特性を得る目的でホトニック結晶等を組み合わせてもよい。

【０１０１】

本発明の画像表示パネルの表面には視認性を高めるために、反射防止層、防眩層を設けたり、金属電極で反射して視認される外光を低減するために円偏光板やカラーフィルタを組み合わたりするなど、従来公知の技術を利用することができる。

【０１０２】

図９は、本発明の画像表示パネルの一副画素当たりの制御回路の一例を表す図である。図において、１０５は前記有機ＥＬ素子による副画素で、この例においては第２の電極を共通陰極とし、第１の電極を個別にトランジスタで駆動する陽極としている。

【０１０３】

トランジスタＴｒ１は、ゲート電位に加えられる選択信号線（走査信号線）４１０の電位により制御され、所定のタイミングでＯＮ状態とされて、データ信号線４１１の電位をトランジスタＴｒ２のゲートに加える。トランジスタＴｒ２は、加えられたゲートの電位により決まる電流を電源線４１２から有機ＥＬ素子の副画素１０５に流す。前記トランジスタＴｒ２のゲートには容量Ｃｇが接続されており、トランジスタＴｒ１がＯＦＦの期間は両端電位差をほぼ一定に保持するので、トランジスタＴｒ２は保持されたゲート電位に応じたほぼ一定の電流を副画素１０５に流しつづける。トランジスタＴｒ１、Ｔｒ２及び容量Ｃｇは副画素１０５付近の基板表面に形成されている。

【０１０４】

図１０は、本発明の画像表示装置の一例を表す機能ブロック図であり、本発明の画像表示パネルと表示制御部とを有する構成とされている。図において、４０１は本発明の画像表示パネル、４０２は表示制御部である。画像表示パネル４０１の表面には表示部４０３が形成されており、これは上記図１に例示した副画素配列からなる画素４０４が配列され、また図９に例示した制御回路が各副画素に形成されている。画像表示パネル４０１の表面には、また画像データ信号を所定のタイミングで取り込み表示部４０３へのデータ信号線４１１の電位を保持する要素の並んだラッチアレイ４０６が形成されている。前記ラッチアレイ４０６の各要素にデータ取り込みのタイミングを与えるＨシフトレジスタ４０５が形成されている。表示部４０３への選択（走査）信号線４１０を順次選択するためのＶ

シフトレジスタ４０７が形成されている。

【０１０５】

表示制御部４０２は画像データを入力し、前記画像表示パネル４０１が必要とする映像信号と、Ｈシフトレジスタ４０５及びＶシフトレジスタ４０７のタイミング信号を供給するものである。

【０１０６】

表示制御部４０２は映像信号変換メモリ４０８とタイミング信号を制御するコントローラ４０９を有する。コントローラ４０９は映像信号メモリから映像信号をシリアル出力しラッチアレイ４０６に送る。

【０１０７】

コントローラ４０９は同時に、水平方向のラッチタイミングを生成するためにＨシフトレジスタ４０５の初期化を行うＨスタートパルスと、同Ｈシフトレジスタ４０５のシフトを行うＨシフトクロックを生成する。Ｈシフトレジスタ４０５はコントローラ４０９から受け取る前記信号により、ラッチ４０６に対するラッチ信号を生成する。ラッチ４０６は前記ラッチ信号のタイミングで前記映像信号を取り込み、その値に従い各データ信号４１１への出力電位を固定する。

【０１０８】

また、コントローラ４０９は垂直方向選択タイミングを生成するために、Ｖシフトレジスタ４０７の初期化を行うＶスタートパルスと、同Ｖシフトレジスタ４０７のシフトを行うＶシフトクロックを生成する。Ｖシフトレジスタ４０７はコントローラ４０９からの前記信号により走査信号線４１０の一つに選択信号を与える。

【０１０９】

表示部４０３に並んだ素子は図９に例示される制御回路により制御されており、前記の選択された走査信号線４１０に接続された制御回路が、データ信号線４１１の電位を容量Ｃｇに貯えて、この電位に応じた電流が画素４０４の有機ＥＬ素子に供給される。

【０１１０】

図１０において、画素４０４は平行四辺形の形状で垂直方向に対して傾斜して配列するように描かれているが、図９に示したデータ信号線４１１は、この見かけの斜め配列に沿って結線される必要は無い。垂直方向に隣接する副画素を互いに結線して図１０のデータ信号線４１１としてよい。

【０１１１】

本発明の画像表示パネルは、上述したように傾きが１／２、或いは１／３である副画素配列の場合、従来の長方形副画素によるデルタ配列、或いはスクランブル配列と同等の副画素の重心位置を有する。前記のように結線することによって、従来の直交座標系で表された画像データをそのまま表示することが可能である。

【０１１２】

なお、画素を形成する副画素の配置を前記の画素内で一定とすることにより、各画素の重心と副画素の重心とのオフセットが一定となる。もし画素内の副画素の配置を一定としない場合、前記のオフセットのムラが画面内に生じるため、例えば単色のなだらかなグラデーションを表示する場合に、オフセットのムラに起因する色ムラが視認される。画素内の副画素の配置を一定にするならば、上記の色ムラを防ぐことができる。

【０１１３】

従来の長方形副画素によるデルタ配列の場合のデータ信号線４１１の結線方法には、少なくとも二つの結線方法がある。そのひとつは、奇数行と偶数行及び副画素の色を区別せずに垂直方向に最短距離にある二つの副画素のうち一方に結線して、水平方向の副画素数と同数のデータ線を引き出す方法である。

【０１１４】

別のひとつは、奇数行同士、偶数行同士についてそれぞれ独立に、同一の発光色を有する副画素について垂直方向の最短距離を結線して、各列の水平方向に隣接する副画素の数の２倍のデータ線を引き出す方法である。本発明の画像表示パネルは、前記のいずれの結

線方法によってもよい。

【０１１５】

もちろん、本発明の画像表示パネルでは、見かけの傾斜配列に沿ってデータ信号線４１１を斜めに結線しても、データ信号線４１１と選択信号線とにより原理的に表示部４０３の全ての画素に駆動情報を与えることができる。したがって、前記の斜めの結線でも、二次元画像情報の座標変換を行えば直交座標系で表れた所望の画像情報の表示は可能である。

【実施例】

【０１１６】

以下に実施例を示してさらに具体的に本発明を説明する。なお本発明はこれらの実施例に限定されるものではない。

【０１１７】

＜実施例１＞

本発明の画像表示パネルの製造方法を具体的に説明する。ガラス基板に１００ｐｐｉ相等のシリコンＴＦＴアクティブマトリクス駆動回路を形成し、この上にアクリル樹脂による絶縁・平坦化層を重ねる。前記アクリル樹脂層に開けたスルーホールを通じて前記駆動トランジスタに接続した３００ｎｍの厚さのクロム反射層と、０．６μｍの厚さのインジウム錫酸化物とを形成する。前記クロム反射層と錫酸化物層とを図１の平面形状にパターニングして第１の電極とする。前記第１の電極の大きさは、平行四辺形の長辺を２３７μｍ、短辺は７５μｍとし、垂直方向に隣接する第１の電極の間隔を３０μｍ、水平方向に隣接する電極間隔を１０μｍとする。

【０１１８】

次に、ポリイミド樹脂を１．８μｍの厚さに基板表面に形成し、パターニングを行って各第１の電極を取り囲む周縁部位置に幅２０μｍの素子分離膜を形成する。前記の基板をＵＶ／オゾン洗浄した後、厚さ５０ｎｍのＮ、Ｎ’－α－ジナフチルベンジジン（α－ＮＰＤ）を堆積してホール輸送層とする。

【０１１９】

次に、スリット幅７１μｍの図２の形状のマスクを基板に重ね、赤色副画素の第１の電極上に重なるように、Ｉｒ（ｐｐｙ）$_3$（イリジウム－フェニルピリジン錯体）と、４、４’－Ｎ、Ｎ’－ジカルバゾールビフェニル（ＣＢＰ）との堆積重量比１４：８６の混合真空堆積膜を４０ｎｍの厚さに形成して赤色発光層とする。

【０１２０】

同じマスクを面内シフトして、緑色副画素の第１の電極上に重なるように、クマリン６（１．０ｖｏｌ％）と、
トリス［８－ヒドロキシキノリナート］アルミニウム（Ａｌｑ$_3$）との堆積重量比１：９９の混合真空堆積膜を３０ｎｍの厚さに形成して緑色発光層とする。

【０１２１】

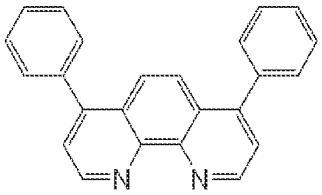
さらに、同じマスクを面内シフトして、青色副画素の第１の電極上に重なるように、ペリレンとトリス［８－ヒドロキシキノリナート］アルミニウム（Ａｌｑ$_3$）との堆積重量比１：９９の混合真空堆積膜を４０ｎｍの厚さに形成して青色発光層とする。

【０１２２】

次に、

【０１２３】

【化５】



で表されるパソフェナントロリン（Ｂｐｈｅｎ）を１０ｎｍの厚さで成膜して電子輸送層とする。さらに、炭酸セシウムとＢｐｈｅｎとの混合真空堆積膜（堆積重量比１：９９）を４０ｎｍの厚さで堆積して電子注入層とする。

【０１２４】

さらに２５０ｎｍの厚さのインジウム錫酸化物を堆積し、第２の電極とする。最後に窒素雰囲気下で、この基板に乾燥剤を付けたガラスキャップを被せ、ＵＶ硬化樹脂により封止する。

【０１２５】

＜実施例２＞

本発明の画像表示パネルの別の製造例を説明する。

【０１２６】

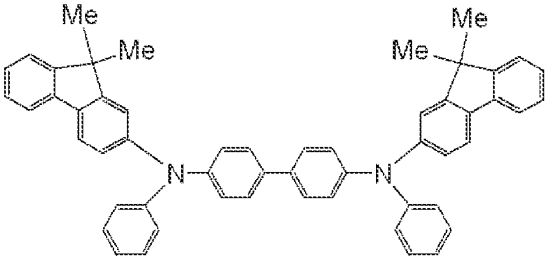
ガラス基板に図９に従うアクティブマトリクス駆動回路を９６０列２４０行配列した画像表示部と、図１０のラッチ４０６、シフトレジスタ４０５，４０７を形成したシリコンＴＦＴ基板を作成する。データ信号線４１１は、奇数行青－偶数行赤、奇数行緑－偶数行青、奇数行赤－偶数行緑を垂直方向に結線する。前記画像表示部の表面にアクリル樹脂による絶縁・平坦化層を重ねる。前記アクリル樹脂層に開けたスルーホールを通じて前記駆動トランジスタに接続した１００ｎｍの厚さのＡｇ合金（ＡｇＰｄＣｕ）層を堆積して、さらに２０ｎｍの厚さのインジウム亜鉛酸化物ＩＺＯを堆積し、図１の形状にパターニングして第１の電極とする。

【０１２７】

さらにアクリル樹脂からなる素子分離膜を、前記第１の電極の周囲にパターニングして形成し、熱処理後放冷し、ＵＶ／オゾン洗浄した後、図２（ｃ）のパターンのマスクを重ねて、

【０１２８】

【化６】



化合物［Ｉ］

で表される化合物［Ｉ］を赤色副画素のホール輸送層として５０ｎｍの厚さ、緑色副画素のホール輸送層として３０ｎｍの厚さ、青色副画素のホール輸送層として２０ｎｍの厚さで、各々前記のマスクを副画素のピッチずつシフトして真空堆積する。

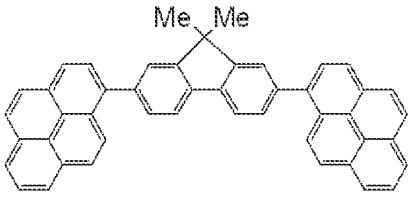
【０１２９】

次に、発光層として、前記マスクを用いて、赤、緑、青（ＲＧＢ）それぞれの発光層を成膜する。前記Ｒの発光層としては、ホストとしてＣＢＰと、燐光発光性化合物ＢｔｐＩｒ（ａｃａｃ）とを混合真空堆積して６０ｎｍの厚さの発光層とする。前記Ｇの発光層としては、ホストとしてＡｌｑ３と、発光性化合物クマリン６とを混合真空堆積して４０ｎｍの厚さの発光層とする。前記Ｂの発光層としては、ホストとして、

【０１３０】

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【化７】

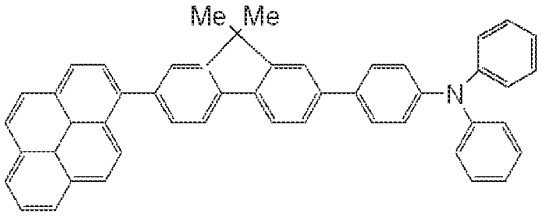


化合物［Ｉｉ］

で表される化合物［ＩＩ］と、

【０１３１】

【化８】



発光性化合物［Ｉｉｉ］

で表される発光性化合物［ＩＩＩ］とを混合真空堆積して２０ｎｍの厚さの発光層とする。

【０１３２】

更に、共通の電子輸送層として、バソフェナントロリン（ＢＰｈｅｎ）を真空堆積法にて１０ｎｍの厚さに形成する。堆積時の真空度は１×１０－４Ｐａ、成膜速度は０．２ｎｍ／ｓｅｃの条件である。次に、共通の電子注入層として、ＢＰｈｅｎと炭酸セシウムとを混合真空堆積（重量比９０：１０）し、２０ｎｍの厚さに形成する。

【０１３３】

この上に、透明陰極１０３としてＩＴＯの透明電極を６０ｎｍの厚さに成膜する。さらに保護膜として、窒化酸化シリコンを７００ｎｍの厚さに成膜し、画像表示パネルを得る。

【０１３４】

＜実施例３＞

本発明の画像表示装置の製造例を説明する。実施例２の画像表示パネルに対して図１０の表示制御部４０２を接続する。コントローラ４０９はＶスタートパルスを出力し、次に表示部４０３の第１行のそれぞれの副画素の明るさを、映像信号変換メモリ４０８を参照し演算により求める。

【０１３５】

次にコントローラ４０９はＨシフトレジスタのリセット信号を出力する。この後、コントローラ４０９は前記の演算により求めた各副画素の明るさのデータを、Ｈシフトクロックとともに順次シリアルに出力する。１行分の出力が終了したら、コントローラ４０９はＶシフトクロックを出力し、次の行について上記と同様の処理を行う。

【０１３６】

以下、最後の行まで処理が終了したら、コントローラ４０９は所定の時間待機し、再び上記Ｖスタートパルス出力から同じ動作を繰り返す。

【図面の簡単な説明】

【０１３７】

【図１】本発明の画像表示パネルの副画素の形状と配列の一例を示す平面図である。

【図２】本発明の画像表示パネルの製造に用いるマスクの一例を示す平面図である。

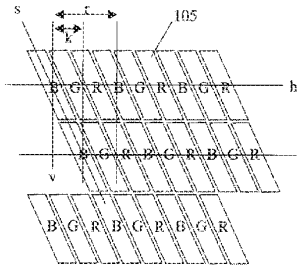
【図３】本発明の別の画像表示パネルの副画素の形状と配列の一例を示す平面図である。

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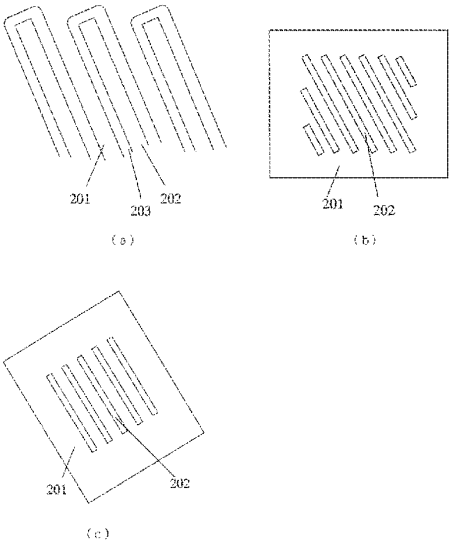
【図４】本発明の別の画像表示パネルの副画素の形状と配列の一例を示す平面図である。
【図５】本発明の別の画像表示パネルの副画素の形状と配列の一例を示す平面図である。
【図６】本発明の別の画像表示パネルの副画素の形状と配列の一例を示す平面図である。
【図７】本発明の別の画像表示パネルの副画素の形状と配列の一例を示す平面図である。
【図８】本発明の画像表示パネルの副画素の層構成の例を示す模式図である。
【図９】本発明の画像表示パネルの副画素の制御回路の一例を示す回路図である。
【図１０】本発明の画像表示装置の一例を示す構成図である。
【図１１】有機ＥＬ素子がマトリックス状に配置されている画像表示パネルの一例を示す概略構成図で、（ａ）は各画素の配列を示す平面図、（ｂ）はＡ－Ａ’の断面図である。
【図１２】素子周辺に素子分離膜が形成された画像表示パネルの一例を示す断面図である。
【図１３】従来の画像表示パネルの副画素の形状と配列を示す平面図で、（ａ）ストライプ配列、（ｂ）デルタ配列、（ｃ）スクランブル配列を示す平面図である。
【図１４】従来の方法により、有機ＥＬ素子の有機化合物層を形成している様子を模式的に示す斜視図である。
【図１５】従来のマスクの断面を示す模式図である。
【図１６】長方形副画素がデルタ配列の画像表示パネルのためのマスクの例を示す模式図で、（ａ）材料放射源側から見たマスクの平面図、（ｂ）Ｃ－Ｃ’の断面図である。
【符号の説明】
【０１３８】
１０１　基板
１０２　第１の電極
１０３　有機化合物層
１０４　第２の電極
１０５　副画素
１１０　素子分離膜
１１１　保護層
２０１　マスク
２０２　貫通孔
２０３　削り部分
３０１　ホール注入層
３０２　ホール輸送層
３０３　発光層
３０４　電子輸送層
３０５　電子注入層
４０１　画像表示パネル
４０２　表示制御部
４０３　表示部
４０４　画素
４０５　Ｈシフトレジスタ
４０６　ラッチアレイ
４０７　Ｖシフトレジスタ
４０８　映像信号変換メモリ（記憶手段）
４０９　コントローラ
４１０　選択（走査）信号線
４１１　データ信号線
４１２　電源線

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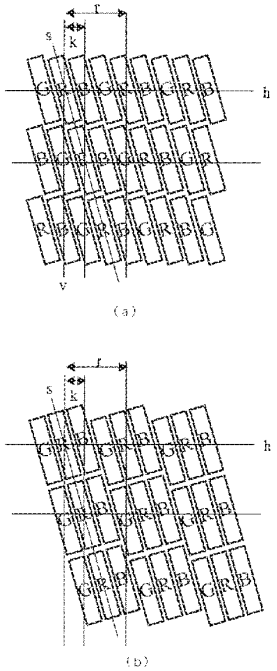
【図１】


s
105
h
v
B G R B G R B G R

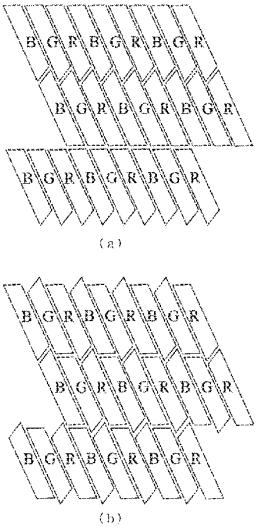
【図２】


201
202
203
(a)
201
202
(b)
201
202
(c)

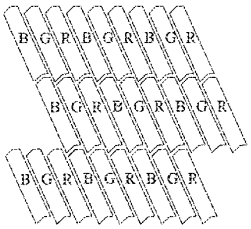
【図３】


s
k
h
v
(a)
s
k
h
(b)

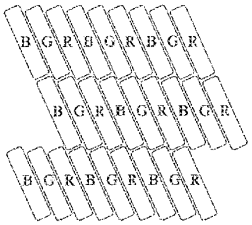
【図４】


B G R B G R B G R
(a)
(b)

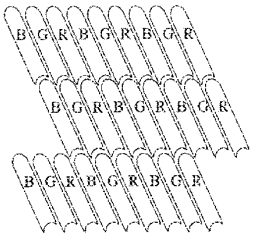
【図５】


B G R B G R B G R
B G R B G R B G R
B G R B G R B G R

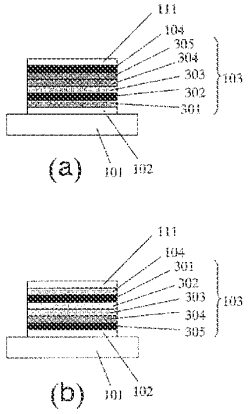
【図６】


B G R B G R B G R
B G R B G R B G R
B G R B G R B G R

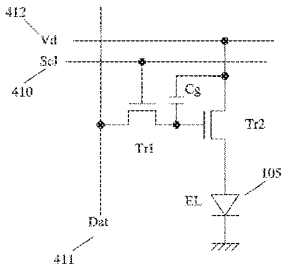
【図７】


B G R B G R B G R
B G R B G R B G R
B G R B G R B G R

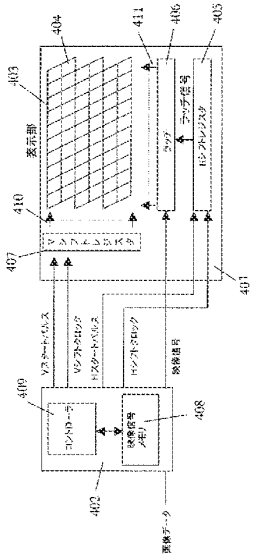
【図８】


111
104
305
304
303
302
301
103
(a)
101
102
111
104
301
302
303
304
305
103
(b)
101
102

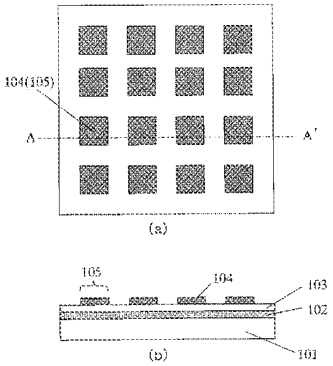
【図９】


412
Vd
Scl
410
Cs
Tr2
Tr1
105
EL
Dat
411

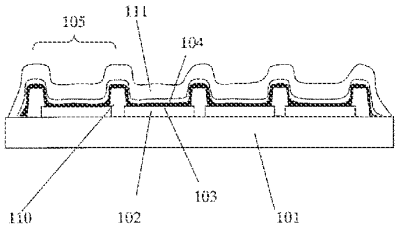
【図１０】



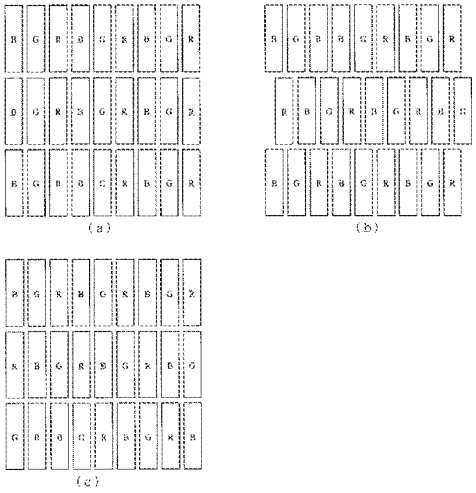
【図１１】



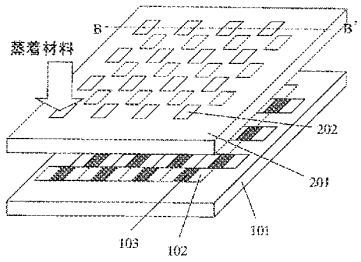
【図１２】



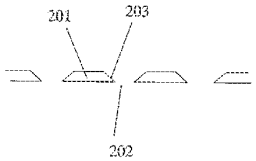
【図１３】



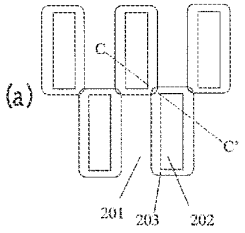
【図１４】

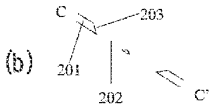

蒸着材料
B
B'
202
201
101
103
102

【図１５】


201
203
202

【図１６】


(a)
C
C'
201
203
202


(b)
C
203
201
202
C'

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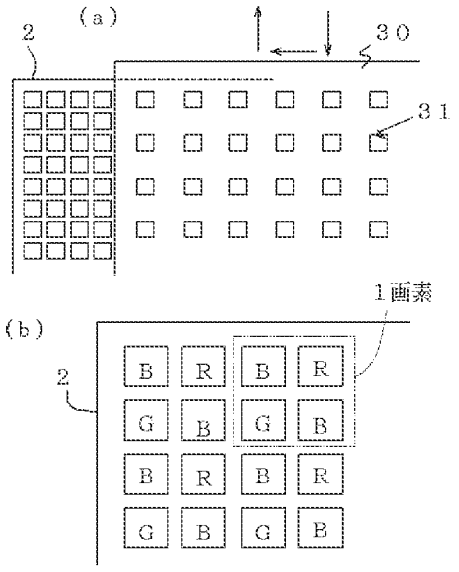
(74)代理人　弁理士　藤村　元彦

(54)【発明の名称】　有機エレクトロルミネッセンスディスプレイパネルとその製造方法

(57)【要約】

【目的】　簡素な工程で製造できる有機エレクトロルミネッセンス（ＥＬ）ディスプレイパネル及びその製造方法を提供する。

【構成】　マトリクス状配置された発光画素からなる画像表示配列の有機ＥＬディスプレイパネルの製造方法は、第１表示電極が形成された基板上に、第１表示電極の各々を囲み基板上に突出する電気絶縁性の隔壁を形成する工程と、隔壁内の第１表示電極を露出せしめる複数の開口を有するマスクを、隔壁の上面に載置し、有機ＥＬ媒体を開口を介して隔壁内の第１表示電極の各々上に堆積させ、有機ＥＬ媒体の薄膜を形成する発光層形成工程と、第２表示電極を有機ＥＬ媒体薄膜の複数の上に共通に形成する工程とを含む。また、上記発光層形成工程において、１つの開口が１つの第１表示電極上からその隣接する第１表示電極上へ配置されるようにマスクを順次移動せしめてを順次繰り返す。



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【特許請求の範囲】
【請求項１】　マトリクス状に配置された複数の発光部からなる画像表示配列を有している有機エレクトロルミネッセンスディスプレイパネルであって、
前記発光部に対応する複数の第１表示電極が表面上に形成された基板と、
前記第１表示電極の各々を囲み前記基板上に突出する電気絶縁性の隔壁と、
前記隔壁内の前記第１表示電極の各々上に形成された少くとも１層の有機エレクトロルミネッセンス媒体の薄膜と、
前記有機エレクトロルミネッセンス媒体の薄膜の複数の上に共通に形成された第２表示電極とからなることを特徴とする有機エレクトロルミネッセンスディスプレイパネル。
【請求項２】　前記基板の略同一平面上に形成されかつ、互いに直交する位置に離間して配列された共通走査信号ライン及び共通データ信号ラインと、前記走査信号ライン、前記データ信号ライン及び前記第１表示電極に接続された非線形素子をさらに有することを特徴とする請求項１記載の有機エレクトロルミネッセンスディスプレイパネル。
【請求項３】　前記非線形素子は互いに接続された薄膜トランジスタ及びコンデンサからなることを特徴とする請求項２記載の有機エレクトロルミネッセンスディスプレイパネル。
【請求項４】　前記基板及び前記第１表示電極が透明であることを特徴とする請求項１記載の有機エレクトロルミネッセンスディスプレイパネル。
【請求項５】　前記第２表示電極上に形成された反射膜を有することを特徴とする請求項４記載の有機エレクトロルミネッセンスディスプレイパネル。
【請求項６】　前記第２表示電極が透明であることを特徴とする請求項１記載の有機エレクトロルミネッセンスディスプレイパネル。
【請求項７】　前記第１表示電極の外側に形成された反射膜を有することを特徴とする請求項６記載の有機エレクトロルミネッセンスディスプレイパネル。
【請求項８】　マトリクス状に配置された複数の発光部からなる画像表示配列を有している有機エレクトロルミネッセンスディスプレイパネルの製造方法であって、
基板上に、前記発光部に対応する複数の第１表示電極を形成するパターン工程と、
前記第１表示電極の各々を囲み前記基板上に突出する電気絶縁性の隔壁を形成する工程と、
前記隔壁内の前記第１表示電極を露出せしめる複数の開口を有するマスクを、前記隔壁の上面に載置し、有機エレクトロルミネッセンス媒体を前記開口を介して前記隔壁内の前記第１表示電極の各々上に堆積させ、少くとも１層の有機エレクトロルミネッセンス媒体の薄膜を形成する発光層形成工程と、
前記有機エレクトロルミネッセンス媒体の薄膜の複数の上に第２表示電極を共通に形成する工程とを含むことを特徴とする有機エレクトロルミネッセンスディスプレイパネルの製造方法。
【請求項９】　前記パターン工程は、互いに直交する位置に離間して配列された共通走査信号ライン及び共通データ信号ラインと、前記走査信号ライン及びデータ信号ラインに接続された非線形素子と、前記非線形素子に接続された前記発光部に対応する複数の島状の第１表示電極とを形成する工程を含むことを特徴とする請求項８記載の有機エレクトロルミネッセンスディスプレイパネルの製造方法。
【請求項１０】　前記非線形素子は互いに接続された薄膜トランジスタ及びコンデンサからなることを特徴とする請求項９記載の有機エレクトロルミネッセンスディスプレイパネルの製造方法。
【請求項１１】　１つの前記開口が１つの前記第１表示電極上からその隣接する前記第１表示電極上へ配置されるように前記マスクを順次移動せしめて前記発光層形成工程を順次繰り返すことを特徴とする請求項８記載の有機エレクトロルミネッセンスディスプレイパネルの製造方法。

【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、電流の注入によって発光する有機化合物材料のエレクトロルミネッセンス（以下、ＥＬという）を利用して、かかる有機ＥＬ材料の薄膜からなる発光層を備えた有機ＥＬ素子の複数をマトリクス状に配置した有機ＥＬディスプレイパネルに関し、特に有機ＥＬ素子を用いたフルカラーディスプレイに関する。
【０００２】
【従来の技術】現在、有機ＥＬ材料を用いたフルカラーディスプレイとしては、特開平５-２７５１７２号特開平第５-２５８８５９号及び特開平第５-２５８８６０号の公報に開示されているものがある。このフルカラーディスプレイは、交差している行と列において配置された複数の発光画素からなる画像表示配列を有している発光装置である。
【０００３】この発光装置においては、各々の画素が共通の電気絶縁性の光透過性基板上に配置されている。各行内の画素は、基板上に伸長して配置された共通の光透過性第１電極を含有し且つ該電極によって接合されている。隣接行内の第１電極は、基板上で横方向に間隔をあけて配置されている。有機ＥＬ媒体は、第１電極及び基板によって形成された支持面の上に配置されている。各列の画素は、有機ＥＬ媒体上に配置された共通に伸長した第２電極を含有し且つ該電極によって接続されている。隣接列内の第２電極は、有機ＥＬ媒体上で横方向に

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間隔をあけて配置されている。該有機ＥＬ媒体の厚さを上回る高さの壁が、隣接列内の画素の共通の境界に沿って予め配置されている。この発光装置においては有機ＥＬ媒体を挟んで交差している第１及び第２電極のラインを用いた単純マトリクス型を採用している。

【０００４】また、この従来の発光装置において、第１電極ライン及び有機ＥＬ媒体の薄膜を、予め基板に設けられている境界の高い壁により所定気体流れを遮って、選択的に斜め真空蒸着して形成する製造方法が採用されている。

【０００５】

【発明が解決しようとする課題】この従来技術は基板に垂直な高い壁を設けてその高い壁を蒸着マスクとして使用するというものだが、特にパターンが微細になった場合、断面のアスペクト比（底辺／高さ）の非常に大きな高い壁をレジスト等で形成するのは困難であり、また、その形成後の第１及び第２電極ライン及び有機ＥＬ媒体膜の信頼性に不安定要素が大きい。また、斜め真空蒸着の精度、工程の複雑さ等の問題点がある。

【０００６】本発明の目的は、かかる問題点を解消するべく簡素な工程で製造できる有機ＥＬディスプレイパネル及びその製造方法を提供することにある。

【０００７】

【課題を解決するための手段】本発明は、マトリクス状に配置された複数の発光部からなる画像表示配列を有している有機エレクトロルミネッセンスディスプレイパネルであって、前記発光部に対応する複数の第１表示電極が表面上に形成された基板と、前記第１表示電極の各々を囲み前記基板上に突出する電気絶縁性の隔壁と、前記隔壁内の前記第１表示電極の各々上に形成された少くとも１層の有機エレクトロルミネッセンス媒体の薄膜と、前記有機エレクトロルミネッセンス媒体の薄膜の複数の上に共通、またはマスクによってストライプ状に形成された第２表示電極とからなることを特徴とする。

【０００８】上記有機ＥＬディスプレイパネルにおいて、前記基板の略同一平面上に形成されかつ、互いに直交する位置に離間して配列された共通走査信号ライン及び共通データ信号ラインと、前記走査信号ライン、前記データ信号ライン及び前記第１表示電極に接続された非線形素子をさらに有することが好ましい。上記有機ＥＬディスプレイパネルにおいて、前記非線形素子は互いに接続された薄膜トランジスタ及びコンデンサからなることが好ましい。

【０００９】また、上記有機ＥＬディスプレイパネルにおいて、前記基板及び前記第１表示電極が透明であること、また、前記第２表示電極に金属光沢があるか、前記第２表示電極上に形成された反射膜を有することが好ましい。さらにまた他の実施例の有機ＥＬディスプレイパネルにおいて、前記第２表示電極が透明である場合、前記第１表示電極に金属光沢があるか、前記前記第１表示電極の外側に形成された反射膜を有することが好ましい。

【００１０】本発明は、マトリクス状に配置された複数の発光部からなる画像表示配列を有している有機エレクトロルミネッセンスディスプレイパネルの製造方法であって、基板上に、前記発光部に対応する複数の第１表示電極を形成するパターン工程と、前記第１表示電極の各々を囲み前記基板上に突出する電気絶縁性の隔壁を形成する工程と、前記隔壁内の前記第１表示電極を露出せしめる複数の開口を有するマスクを、前記隔壁の上面に載置し、有機エレクトロルミネッセンス媒体を前記開口を介して前記隔壁内の前記第１表示電極の各々上に堆積させ、少くとも１層の有機エレクトロルミネッセンス媒体の薄膜を形成する発光層形成工程と、前記有機エレクトロルミネッセンス媒体の薄膜の複数の上に第２表示電極を共通、またはマスクによってストライプ状に形成する工程とを含むことを特徴とする。

【００１１】また、上記有機ＥＬディスプレイパネルの製造方法において、１つの前記開口が１つの前記第１表示電極上からその隣接する前記第１表示電極上へ配置されるように前記マスクを順次移動せしめて前記発光層形成工程を順次繰り返し、より効率良く製造することも可能である。このように、有機ＥＬ膜の発光層を隔壁により保護するので、マスクが発光層に損傷を与えることが少なくなり、隔壁及びマスクによりＲＧＢ有機層の分離が確実に行なえ、精度良くＲＧＢの媒体の塗り分けができる。

【００１２】

【実施例】以下に、本発明による実施例を図面を参照しつつ説明する。図１に示すように、実施例の有機ＥＬディスプレイパネルはマトリクス状に配置されかつ各々が赤Ｒ、緑Ｇ及び青Ｂの発光部からなる発光画素１の複数からなる画像表示配列を有している。

【００１３】図２に示すように、この有機ＥＬディスプレイパネルの基板２上には、互いに直交する位置に電気的に離間して配列された共通走査信号ライン３及び共通データ信号ライン４が設けられ、さらに走査信号ライン及びデータ信号ラインに接続された非線形素子５と、非線形素子に接続された発光部Ｒ、Ｇ及びＢに対応する複数の島状の第１表示電極６とが表面の略同一平面上に形成されている。

【００１４】さらに基板２上には、図２及び図３に示すように、第１表示電極６の各々を囲み基板上に突出する電気絶縁性の隔壁７が形成されている。隔壁７内凹部の第１表示電極６の各々上には、少くとも１層の有機ＥＬ媒体たとえば、有機正孔輸送層、有機発光層及び有機電子輸送層の３層構造の媒体または有機正孔輸送層及び有機発光層２層構造の媒体などの薄膜が形成されている。

【００１５】有機ＥＬ媒体８の薄膜の複数の上に共通に形成された第２表示電極９が形成されている。第２表示

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電極９の上には保護膜１０または保護基板が設けられることが好ましい。さらに、具体的な実施例のアクティブマトリクス形有機ＥＬディスプレイパネルでは、図４に示すように、ガラスなどの透明な基板２の上にインジウム錫酸化物（以下、ＩＴＯという）の複数の島状の第１表示電極６と、この第１表示電極に接続された非線形素子５、たとえば互いに接続された薄膜トランジスタ（ＴＦＴ）T1，T2及びコンデンサCとがフォトリソグラフィ真空蒸着技術などにより形成され、さらに、同様にデータ信号ラインの共通ドレインライン４と走査信号ラインの共通ゲートライン３が略一基板平面上に直交する位置に配列されている。そして、図５に示すように、第１のＴＦＴ（T1）のソース電極にはコンデンサCと第２のＴＦＴ（T2）のゲートが接続され、ソース電極はコンデンサCとともにアースラインEに接続されている。また、T2のドレインラインは第１表示電極６に接続されている。このような発光部組合せユニットが各画素ごとに全画素数の数だけ集積され、マトリクス状に配置された複数の発光画素からなる画像表示配列の有機ＥＬディスプレイパネルの基板が形成されている。

【００１６】なお、上記実施例では、非線形素子は互いに接続された薄膜トランジスタ及びコンデンサからなる３端子タイプで構成しているが、薄膜トランジスタはp-Si、a-Si、CdSe、Teが採用され得、また代わりにMOS-FETを用いた回路としても良い。さらに、３端子タイプではなく、２端子タイプのMIMなどを用いて構成することもできる。

【００１７】このアクティブマトリクス回路基板２上に、フォトリソグラフィなどにより図６及び図７に示すように、Si_3N_4などの保護膜７aを、非線形素子５並びにデータ信号ラインの共通ドレインライン４及び走査信号ラインの共通ゲートライン３上に選択的に蒸着して形成し、その上に、所定高さまでレジストまたは感光性ポリイミド等を選択的に形成し隔壁７を形成する。また、図８に示すように、保護膜を形成せずに、非線形素子５並びにデータ信号ラインの共通ドレインライン４及び走査信号ラインの共通ゲートライン３上にレジストを選択的に形成し隔壁７を形成することもできる。

【００１８】また、上記実施例の有機ＥＬディスプレイパネルにおいて、基板及び第１表示電極が透明であり、発光は基板側から放射されるので、図３に示すように、発光効率を高めるために第２表示電極上または保護膜を介して反射膜２１を設けることが好ましい。逆に、他の実施例の有機ＥＬディスプレイパネルにおいて、第２表示電極を透明材料で構成して、発光を第２表示電極側から放射させることもできる。この場合、発光効率を高めるために第１表示電極の外側に反射膜を設けることが好ましい。

【００１９】次に、図５を用いて、アクティブマトリクス駆動方法について簡単に説明する。ドレインライン群Ｘi，Ｘi+1，Ｘi+2，…とゲートライン群Ｙj，Ｙj+1，Ｙj+2，…の選択交点にパルス電圧が印加されると、Ｔ１はオン状態になり、コンデンサを充電する。この充電電圧はゲートへ印加されるパルス幅で決まる。充電電圧が十分大きい場合は、Ｔ２のゲート電圧が大きくオン状態になるので、ＥＬ層８を介して上部の透明電極に印加設定されている電圧がＥＬ層８に印加される。そして、コンデンサの放電が進み、ゲート電圧は徐々に減少してゆく。このためコンデンサの充電電圧でＴ２の導通時間が決定される。発光部の明るさは、この導通時間にも関係している。ドレインラインへのＲＧＢ信号に応じてＸ電極群とＹ電極群を順次走査して、交点画素を選択発光させる。

【００２０】次に、有機ＥＬディスプレイパネル製造工程を説明する。まず、ゲートライン、ゲート絶縁膜、チャネル層、コンタクト層、第１表示電極の透明電極（ＩＴＯ陽極）、ソース、ドレインライン、信号線等、所定のＴＦＴアレイをガラス基板上に形成する。図９は、得られたＴＦＴ等所定の機能素子を備えている基板２の上に、レジストあるいは感光性ポリイミド等で、個々の画素を囲む絶縁性の隔壁７をフォトリソグラフィ等で形成した後の状態の斜視図である。例えば隔壁７の凸部の幅は、いずれも０．０２mm程度、隔壁凹部の底面積は、０．３mm×０．１mm程度であり、この寸法であれば６４０×４８０画素の１０インチフルカラーディスプレイが実現できる。また後の工程で複数回成膜する有機ＥＬ媒体を分離する隔壁は、成膜用マスクが隔壁に突き合わされた際にマスクで既に成膜された有機ＥＬ媒体８を傷つけない程度の高さ（０．５μm以上）であればよい。また隔壁が高すぎても壊れやすくなるので１０μm以下程度、できれば１～２μm程度が望ましい。更に、その後の工程で成膜する第２表示電極の陰極が隔壁によって断線しない程度に、隔壁の断面が略台形の形状になることが望ましい。なお、マトリクス状隔壁は、ガラスペーストの光吸収性物質を塗布するスクリーン印刷法により、基板上に形成することもできる。隔壁は、目視側から見て長方形底面の壁となるように形成しているが、正方形、円形などその形状は如何なるものでも良い。

【００２１】図１０に示すように、この成膜用マスク３０を千鳥格子状に配列した開口３１を有するものとして、これを図の矢印に示すように隔壁付き基板２上にて順次移動して、Ｒ媒体、Ｇ媒体及びＢ媒体の最低３回のマスク蒸着を行う。図１１（ａ）～（ｄ）で、この隔壁付き基板を用いて有機ＥＬディスプレイパネルを作製する発光層形成工程及び第２表示電極形成工程を順を追って説明する。図ではＲＧＢ３色のみの１画素のみの説明であるが、実際は２次元に複数個の画素を同時に形成するのはもちろんである。

【００２２】図１１（ａ）の工程では、隔壁７が形成された基板２の凹部の各１つに成膜用マスク３０の各１つ

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の穴部３１を位置合わせした後、隔壁上にマスクを載置して、１番目（例えば赤色）の有機ＥＬ媒体８ａを例えば蒸着などの方法を用いて０．１～０．２μm程度の厚さに成膜する。尚、成膜用マスク３０の開口３１の各々は、図に示すように隔壁凹部の底面の第１表示電極を全て覆う有機ＥＬ媒体層を形成できるような大きさを有している。

【００２３】図１１（ｂ）の工程では、例えば成膜用マスクを左に隔壁１個分ずらして位置合わせをした後、隔壁上にマスクを載置して２番目（例えば緑色）の有機ＥＬ媒体８ｂを所定膜厚に成膜する。図１１（ｃ）の工程で残った１個の凹部に成膜用マスクを位置合わせをした後、隔壁上にマスクを載置して３番目（例えば青色）の有機ＥＬ媒体８ｃを所定膜厚に成膜する。

【００２４】このように、１つの開口が１つの第１表示電極上からその隣接する第１表示電極上へ配置されるようにマスクを順次移動せしめる発光層形成工程を順次繰り返すことが好ましい。また、隔壁７があるので、成膜用マスクの位置合わせ、移動、載置して蒸着する際に、マスクによる有機ＥＬ媒体層を傷つけることがない。図１１（ｄ）の第２表示電極形成工程では、成膜用マスクを取り除き、Ａｌ、Ａｕ等の低抵抗金属を、成膜された３種類の有機ＥＬ媒体の上に全体が電気的に導通するように蒸着、あるいはスパッタ等の手段を用いて陰極として例えば０．１～１０μm程度被着させる。この金属膜の膜厚は支障のない限り厚く被着させても構わない。

【００２５】このように隔壁とマスクとを突き合わせて有機ＥＬ媒体を成膜することで、有機ＥＬ媒体を劣化させる事なく、また隔壁があるため隣接した画素に成膜された有機ＥＬ媒体が回り込まずに微細な領域に塗り分けることが可能となり、高精彩なフルカラーディスプレイが実現できる。この時、基板のＩＴＯやＴＦＴと陰極がショートしないよう、また隣接した凹部にまで成膜しないように、有機ＥＬ媒体成膜用マスクの穴部を最適な大きさにするのはもちろんである。ただし有機ＥＬ媒体が隔壁凸部に成膜されるのは問題ない。

【００２６】図１０に示す成膜用マスク３０の代わりに、図１２（ａ）に示す千鳥格子状に配列した開口３１を有するマスクを用いて、これを図の矢印に示すように隔壁付き基板２上にて順次移動して、ＲＧＢの有機ＥＬ媒体を蒸着することもできる。この場合、図１２（ｂ）に示すように、もともと輝度がとれないＢ媒体領域を１画素あたり広く取れ、マスク剛性も更に上がるが、蒸着回数が最低４回に増える。

【００２７】他の実施例の有機ＥＬディスプレイパネルとして、有機ＥＬ媒体を挟んで交差する第１及び第２表示電極のラインを用いた単純マトリクス型のパネルがある。図１３に示すかかる単純マトリクス型有機ＥＬディスプレイパネルの基板２上には、互いに直交する位置に電気的に離間して配列された第１表示電極ライン５１が設けられている。さらに基板２上には、発光部Ｒ、Ｇ及びＢに対応する複数の島状の第１表示電極部分６１をなすように、各々を囲み基板から突出する電気絶縁性の隔壁７が形成されている。隔壁７内凹部の第１表示電極６１の各々上には、少くとも１層の有機ＥＬ媒体たとえば、有機正孔輸送層、有機発光層及び有機電子輸送層の３層構造の媒体または有機正孔輸送層及び有機発光層２層構造の媒体などの薄膜が形成されている。有機ＥＬ媒体８の薄膜の複数の上に、第１表示電極ライン５１と交差した第２表示電極ライン７１が形成されている。第２表示電極ライン５１の上には、保護膜または保護基板が設けられることが好ましい。

【００２８】図１４に、単純マトリクス型有機ＥＬディスプレイパネルの製造手順を簡単に示す。まずガラス基板２上に、ストライプ状に複数の平行第１表示電極ライン５１をＩＴＯなどで成膜する（図１４（ａ））。次に、図１４（ｂ）に示すように、第１表示電極ラインが設けられている基板２の上に、レジストあるいは感光性ポリイミド等で、個々の島状の第１表示電極部分６１を囲む絶縁性の隔壁７をフォトリソグラフィ等で形成する。

【００２９】次に、上記図１１（ａ）～（ｃ）で示した工程と同様に、この隔壁付き基板２の凹部の各１つに、ＲＧＢ有機ＥＬ媒体の発光層を、蒸着マスクを順次移動せしめて形成する。図１４（ｃ）に示すように、隔壁７及び発光層上に、第１表示電極ライン５１と交差した複数のストライプ状平行第２表示電極ライン７１を低抵抗金属で蒸着マスクを用いて蒸着形成する。

【００３０】

【発明の効果】以上の如く本発明によれば、以下の効果が得られる。

(1) 有機ＥＬ膜を成膜後はパターニング等有機ＥＬ媒体に損傷を与える工程を行う必要がない。

(2) 陰極はベタ付けで成膜でき効率が良い。

【００３１】(3) 従来の有機ＥＬディスプレイパネル製造方法より工程が少なく、ＲＧＢ有機層の分離が確実に行なえ、精度良くＲＧＢの媒体の塗り分けができる。

(4) 隔壁により、有機ＥＬ媒体層へ傷付けを防止でき有機機能層の保護が達成できる。

(5) 金属マスクを千鳥格子状にする事により、マスクの剛性が増し、移動及び位置合わせのマスクの撓みによる有機ＥＬ媒体層及び隔壁へ傷付けをさらに防止する。

【図面の簡単な説明】

【図１】　本発明による有機ＥＬディスプレイパネルの部分拡大平面図。

【図２】　本発明による有機ＥＬディスプレイパネルの概略部分拡大平面図。

【図３】　図２の線ＡＡの断面図。

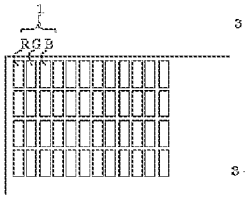
【図４】　本発明による実施例の有機ＥＬディスプレイパネルの基板の概略部分拡大平面図。

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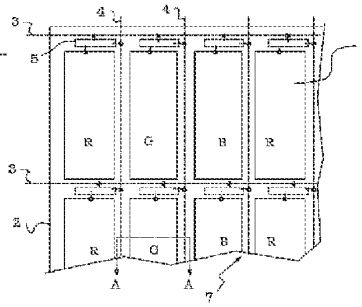
【図５】　本発明による実施例の有機ＥＬディスプレイパネルの基上に形成された非線形素子を示す回路図。
【図６】　本発明による実施例の有機ＥＬディスプレイパネルの隔壁付き基板の概略部分拡大平面図。
【図７】　図６の線ＡＡにおける断面図。
【図８】　本発明による他の実施例の有機ＥＬディスプレイパネルの隔壁付き基板の概略部分拡大断面図。
【図９】　本発明による実施例の有機ＥＬディスプレイパネルの隔壁付き基板の概略斜視図。
【図１０】　本発明の有機ＥＬディスプレイパネル製造方法に用いる成膜用マスクの概略部分拡大平面図。
【図１１】　本発明の有機ＥＬディスプレイパネル製造方法における有機ＥＬディスプレイパネルの隔壁付き基板の概略部分拡大平面図。
【図１２】　本発明の有機ＥＬディスプレイパネル製造方法に用いる他の成膜用マスクの概略部分拡大平面図。
【図１３】　本発明による他の実施例の有機ＥＬディスプレイパネルの概略部分拡大断面図。
【図１４】　本発明による他の実施例の有機ＥＬディスプレイパネルの隔壁付き基板の概略斜視図。

【主要部分の符号の説明】
１　発光画素
２　基板
３　走査信号ライン
４　データ信号ライン
５　非線形素子
６　第１表示電極
７　隔壁
８　有機ＥＬ媒体
９　第２表示電極
１０　保護膜
３０　成膜用マスク
３１　開口
５１　第１表示電極ライン
６１　第１表示電極部分
７１　第２表示電極ライン

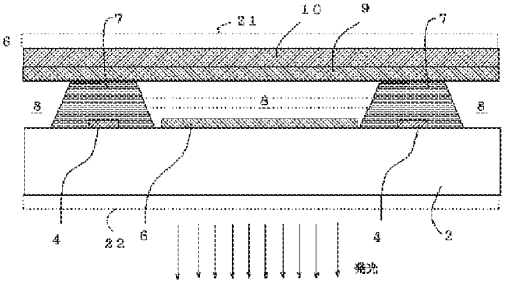
【図１】



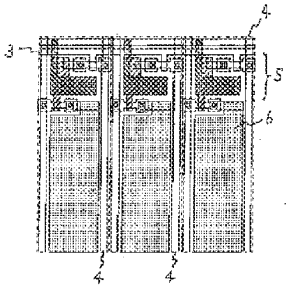
【図２】



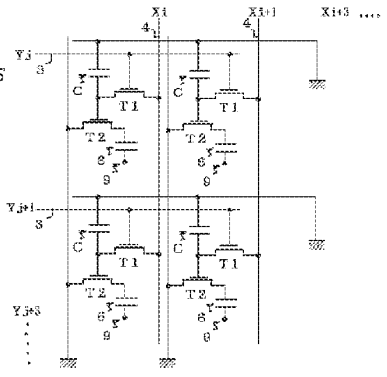
【図３】



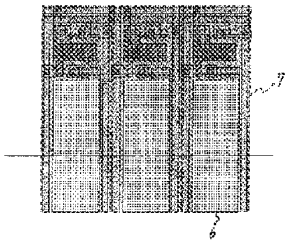
【図４】



【図５】



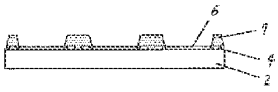
【図６】



【図７】

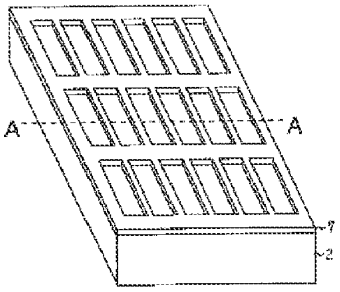


【図８】

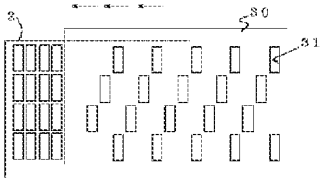


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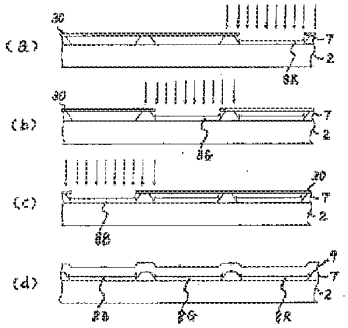
【図９】



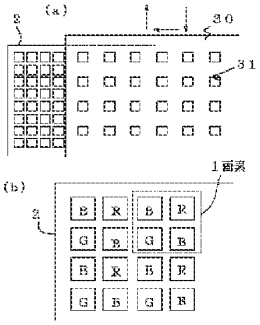
【図１０】



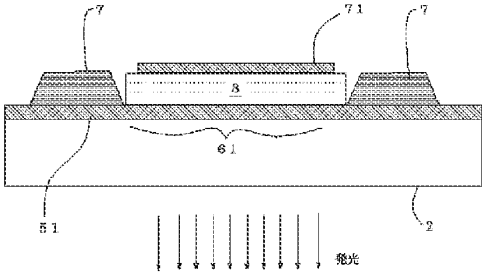
【図１１】



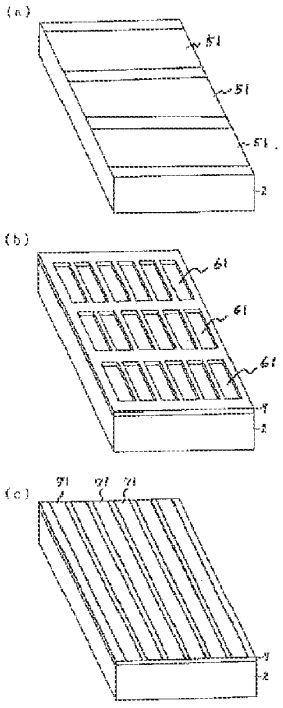
【図１２】



【図１３】



【図１４】



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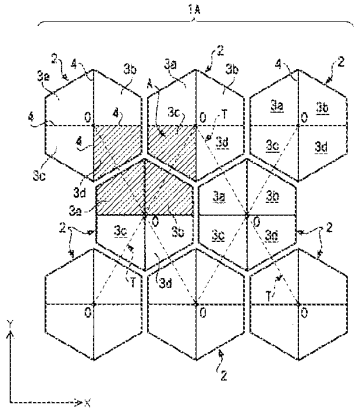
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(54)【発明の名称】画素構造、電気光学装置及び電子機器

(57)【要約】
【課題】　非常に簡単な構造により、自然画等といった画像と文字等といった線画の両方をきれいに表示できる画素構造、電気光学装置及び電子機器を提供する。
【解決手段】　デルタ配列された複数の画素２を有し、複数の画素２のそれぞれはその画素２を４分割した形状の４つの副画素３ａ，３ｂ，３ｃ，３ｄを有する画素構造である。個々の副画素３ａ，３ｂ，３ｃ，３ｄの分割辺４は縦方向Ｙ又は横方向Ｘに沿うように配列される。複数の画素２を使ってデルタ配列で表示を行えば、自然画等といった画像をきれいに表示できる。一方、複数の第２画素Ａを使って正方配列で表示を行えば、文字、数字等といった線画をきれいに表示できる。副画素は、画素を２分割した形状とすることもできる。
【選択図】　図１



【特許請求の範囲】
【請求項１】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、さらに
個々の副画素の分割辺は縦方向又は横方向に沿うように配列される
ことを特徴とする画素構造。
【請求項２】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列される
ことを特徴とする画素構造。
【請求項３】
請求項１又は請求項２において、前記画素は６角形形状であり、前記副画素は台形形状であることを特徴とする画素構造。
【請求項４】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、
前記複数の副画素の選択の仕方を切り替えることによりデルタ配列及び正方配列を選択的に実現する制御手段を有する
ことを特徴とする電気光学装置。
【請求項５】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、
前記複数の副画素の選択の仕方を切り替えることによりデルタ配列及び直線的な配列を選択的に実現する制御手段を有する
ことを特徴とする電気光学装置。
【請求項６】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、
前記４つの副画素のそれぞれに対応してＲ色光，Ｇ色光，Ｇ色光，Ｂ色光を配置して空間加法混色によるカラー表示を行う
ことを特徴とする電気光学装置。
【請求項７】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、さらに
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
前記４つの副画素のそれぞれに対応して異なる４色の光を配置して空間加法混色によるカラー表示を行う
ことを特徴とする電気光学装置。
【請求項８】
請求項７において、前記異なる４色の光は、Ｒ色光，Ｇ色光，Ｗ色光，Ｂ色光であることを特徴とする電気光学装置。
【請求項９】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
Ｒ色光，Ｇ色光，Ｂ色光のそれぞれに対応したライトバルブを用いて積分的加法混色に

よるカラー表示を行う
ことを特徴とする電気光学装置。
【請求項１０】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
Ｒ色光，Ｇ色光，Ｂ色光のそれぞれに対応したライトバルブを用いて積分的加法混色によるカラー表示を行う
ことを特徴とする電気光学装置。
【請求項１１】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
Ｒ色光，Ｇ色光，Ｂ色光を時分割方式でライトバルブへ供給して積分的加法混色によるカラー表示を行う
ことを特徴とする電気光学装置。
【請求項１２】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
Ｒ色光，Ｇ色光，Ｂ色光を時分割方式でライトバルブへ供給して積分的加法混色によるカラー表示を行う
ことを特徴とする電気光学装置。
【請求項１３】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
４色以上の光で積分的加法混色によるカラー表示を行う
ことを特徴とする電気光学装置。
【請求項１４】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
４色以上の光で積分的加法混色によるカラー表示を行う
ことを特徴とする電気光学装置。
【請求項１５】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
前記副画素を用いて面積階調による多階調化された表示を行う
ことを特徴とする電気光学装置。
【請求項１６】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに
前記副画素を用いて面積階調による多階調化された表示を行う
ことを特徴とする電気光学装置。
【請求項１７】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、

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個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、
前記副画素は当該副画素と相似形の画素電極によって形成され、
観察側から見て前記画素電極の裏側に配線が形成され、さらに
前記配線は観察側から見て前記副画素を通過する直線状の配線を含む
ことを特徴とする電気光学装置。

【請求項１８】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、
前記副画素は当該副画素と相似形の画素電極によって形成され、
観察側から見て前記画素電極の裏側に配線が形成され、さらに
前記配線は観察側から見て前記副画素を通過する直線状の配線を含む
ことを特徴とする電気光学装置。

【請求項１９】
請求項１７又は請求項１８において、観察側から順に、透光性を有する電極、液晶層、配線層及び光反射層を有することを特徴とする電気光学装置。

【請求項２０】
請求項１７又は請求項１８において、観察側から順に、透光性を有する電極、ＥＬ発光層及び配線層を有することを特徴とする電気光学装置。

【請求項２１】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、
前記副画素と相似形に形成された画素電極と、
該画素電極の辺縁に沿って配置された配線と
を有することを特徴とする電気光学装置。

【請求項２２】
デルタ配列された複数の画素を有し、
該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、
個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、
前記副画素と相似形に形成された画素電極と、
該画素電極の辺縁に沿って配置された配線と
を有することを特徴とする電気光学装置。

【請求項２３】
請求項２１又は請求項２２において、互いに隣り合う副画素のための一対の配線を該副画素の直線状の分割辺に沿って直線状に配置することを特徴とする電気光学装置。

【請求項２４】
請求項４から請求項２３のいずれか１つにおいて、前記画素は６角形形状であり、前記副画素は台形形状であることを特徴とする電気光学装置。

【請求項２５】
請求項４から請求項２４のいずれか１つに記載の電気光学装置と、該電気光学装置の動作を制御する制御手段とを有することを特徴とする電子機器。

【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、液晶装置、有機ＥＬ装置等といった電気光学装置に好適な画素構造、その画素構造を用いた電気光学装置、及び液晶プロジェクタ、携帯電話機、携帯情報端末機等といった電子機器に関する。

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【背景技術】
【０００２】
デルタ配列は低容量の画像データで高品位の表示ができ、それ故、自然画等といった画像の表示に適している。しかしながら、文字、図形等といった線画は輪郭が不鮮明になるという問題がある。そのため、コンピュータのモニター等のように文字データの表示を主とする電気光学装置では、Ｒ，Ｇ，Ｂのストライプ配列等が用いられてきた。しかしながら、このストライプ配列はデルタ配列に比べて高容量の画像データが必要となり、限られた帯域でデータ送信する場合は負荷となり、大容量の画像メモリも必要となる。また、電気光学装置も高解像度の装置が必要であった。
【０００３】
近年、携帯機器の発達により、モバイルディスプレイで映像を見たり、インターネット等で得た情報をモバイルディスプレイで表示したりする機会が増えている。今後、地上波デジタル放送のＭＰＥＧ－４配信が行われれば、テレビ映像もモバイルディスプレイで視聴が可能である。ところで、携帯機器向けの無線通信網は、携帯電話網も含めて、ＡＤＳＬやＦＴＴＨ（Fiber to the Home）と比較して通信速度が遅いため、なるべく低容量のデータで高品位の表示が行えることが望ましい。しかしながら、画像と線画とを両立して高品位に表示することができなかった。
【０００４】
一方、家庭内で用いるテレビやパーソナルコンピュータ等といった固定機器では、充実した高速通信網やデジタル放送を用いて高品位の映像等を入手する環境が整いつつある。しかし、人間の視覚特性は水平方向及び垂直方向の感度が高いため、四角形の画素構造を用いると、いくら高解像度のデータを用いても画素構造を知覚し易いという問題がある。よって、このような環境においても、画像と線画を両立して高品位に表示できる装置が望まれている。
【０００５】
従来、四角形の画素をデルタ配列する構造に代えて、６角形又は多数の画素を用いて擬似６角形の画素をデルタ配列して、いわゆるハニカム構造を構成し、四角形の画素を用いた場合に知覚され易かった水平及び垂直のラインを低減した技術が提案されている（例えば、特許文献１参照）。
【０００６】
また、デルタ配列における文字データの表示品位を改善するための手段として、ストライプ配列の画素電極に対応して画素電極よりも面積が小さいカラーフィルタを有し、且つ各カラーフィルタの中心が略デルタ配列になるように配置した構造が知られている（例えば、特許文献２参照）。
【０００７】
また、有機ＥＬ装置等といった電気光学装置において、副画素（すなわち、サブピクセル）の画素配列をデルタ配列とする技術が開示されている（例えば、特許文献３参照）。
【０００８】
【特許文献１】特開平９－２３３３８３号公報（第４～５頁、図４）
【特許文献２】特開２００１－３３７３１７号公報（第３頁、図１）
【特許文献３】特開２００２－２２１９１７号公報（第３頁、図１）
【発明の開示】
【発明が解決しようとする課題】
【０００９】
上記特許文献１に開示された方式は、自然画等といった画像を表示するのには適しており、特に撮像システムとの親和性は高い。しかしながら、文字等といった線画の表示についての対策はされていない。また、四角形の多数画素で擬似６角形のブロックを表示する方法が開示されているが、副画素を用いるという技術思想は示されていない。また、四角形の多数画素で擬似６角形ブロックを構成するには非常に高解像度の表示装置が必要となり、現実的でない。

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【００１０】
また、上記特許文献２に開示された方式では、輝度に寄与する面積が小さいため、表示が暗くなるという問題がある。また、四角形画素を用いているので画素構造を知覚し易く、さらには厳密にはデルタ配列ではないため表示品位が劣るという問題がある。
【００１１】
また、上記特許文献３に開示された電気光学装置では、副画素をデルタ配列させているが、デルタ配列させた画素を分割して副画素を設けるという技術思想は示されていない。このため、この従来の電気光学装置では、ＴＦＴ（Thin Film Transistor）等といったスイッチング素子の配列の仕方が複雑になるという問題がある。
【００１２】
本発明は、上記の問題点に鑑みて成されたものであって、非常に簡単な構造により、自然画等といった画像と文字等といった線画との両方をきれいに表示できる画素構造、電気光学装置及び電子機器を提供することを目的とする。
【課題を解決するための手段】
【００１３】
上記の目的を達成するため、本発明に係る画素構造は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、さらに個々の副画素の分割辺は縦方向又は横方向に沿うように配列されることを特徴とする。
【００１４】
この画素構造によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。ここで、正方配列とは、画素が縦横に直線状に並ぶ配列であり、例えば、ストライプ配列、モザイク配列等である。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。
【００１５】
次に、本発明に係る他の画素構造は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列されることを特徴とする。
【００１６】
この画素構造によれば、上記と同様に、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は垂直若しくは水平の直線的な配列のいずれかを選択できる。そして、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、文字等といった線画データは直線的な配列によりデルタ配列に比べてきれいな表示を行うことができる。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。
【００１７】
なお、上記構成の各画素構造において、前記画素は６角形形状であり、前記副画素は台形形状であることが望ましい。こうすれば、画素同士を密着させて並べることができ、しかも副画素への分割が容易である。
【００１８】
次に、本発明に係る電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、該複数の副画素の選択の仕方を切り替えることによりデルタ配列及び正方配列を選択的に実現する制御手段を有することを特徴とする。
【００１９】

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この電気光学装置によれば、制御手段の働きにより副画素の選択の仕方を簡単に変えることができ、この簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る電気光学装置によれば、非常に簡単な構造により、画像と線画の両方をきれいに表示できる。

【００２０】

次に、本発明に係る他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、該複数の副画素の選択の仕方を切り替えることによりデルタ配列及び直線的な配列を選択的に実現する制御手段を有することを特徴とする。

【００２１】

この電気光学装置によれば、制御手段の働きにより副画素の選択の仕方を簡単に変えることができ、この簡単な操作によって、デルタ配列又は直線的な配列のいずれかを選択できる。そして、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、文字等といった線画データは直線的な配列によりデルタ配列に比べてきれいな表示を行うことができる。つまり、本発明に係る電気光学装置によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００２２】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、前記４つの副画素のそれぞれに対応してＲ色光，Ｇ色光，Ｇ色光，Ｂ色光を配置して空間加法混色によるカラー表示を行うことを特徴とする。

【００２３】

この電気光学装置によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る電気光学装置によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００２４】

この構成では、デルタ配列及び正方配列の両方ともに１画素をＲ，Ｇ，Ｇ，Ｂでカラー表示する。ここで、人間の眼はＧ色光の視感度が高いため、Ｇ色光を２つ配置することで良好な表示を得ることができる。また、正方配列では副画素を１／２画素ずらした周期構造とすることができ、解像度感が高い。

【００２５】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、さらに個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに前記４つの副画素のそれぞれに対応して異なる４色の光を配置して空間加法混色によるカラー表示を行うことを特徴とする。

【００２６】

この電気光学装置によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画デー

タは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００２７】

この構成では、デルタ配列及び正方配列の両方ともに１画素を異なる４色の光でカラー表示する。異なる４色としてＲ，Ｇ，Ｂの３原色と４色目にＷ（白）を加えれば高輝度化が達成でき、省電力化を達成できる。またＷ以外の４色目を選べば色再現範囲が広がる。

【００２８】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらにＲ色光，Ｇ色光，Ｂ色光のそれぞれに対応したライトバルブを用いて積分的加法混色によるカラー表示を行うことを特徴とする。

【００２９】

この電気光学装置によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００３０】

また、この構成では、大画面で使用するプロジェクタにおいて、水平及び垂直の画素構造が知覚され難くなるので、特に、ホームシアター等で映像を楽しむときに好適である。

【００３１】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらにＲ色光，Ｇ色光，Ｂ色光のそれぞれに対応したライトバルブを用いて積分的加法混色によるカラー表示を行うことを特徴とする。

【００３２】

この電気光学装置によれば、制御手段の働きにより副画素の選択の仕方を簡単に変えることができ、この簡単な操作によって、デルタ配列又は直線的な配列のいずれかを選択できる。そして、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、文字等といった線画データは直線的な配列によりデルタ配列に比べてきれいな表示を行うことができる。つまり、本発明に係る電気光学装置によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００３３】

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次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらにＲ色光，Ｇ色光，Ｂ色光を時分割方式でライトバルブへ供給して積分的加法混色によるカラー表示を行うことを特徴とする。

【００３５】

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この電気光学装置によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００３６】

この構成においても、水平及び垂直の画素構造を知覚され難くなるので、特に、ホームシアター等で映像を楽しむときに好適である。

【００３７】

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【００３８】

この電気光学装置によれば、制御手段の働きにより副画素の選択の仕方を簡単に変えることができ、この簡単な操作によって、デルタ配列又は直線的な配列のいずれかを選択できる。そして、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、文字等といった線画データは直線的な配列によりデルタ配列に比べてきれいな表示を行うことができる。つまり、本発明に係る電気光学装置によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００３９】

この構成においても、水平及び垂直の画素構造を知覚され難くなるので、特に、ホームシアター等で映像を楽しむときに好適である。

【００４０】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに４色以上の光で積分的加法混色によるカラー表示を行うことを特徴とする。

【００４１】

この電気光学装置によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００４２】

この構成においては、水平及び垂直の画素構造が知覚され難くなるのに加えて、多原色とすることで色再現性に優れ、特に、ホームシアター等で映像を楽しむときに好適である。

【００４３】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに４色以上の光で積分的加法混色によるカラー表示を行うことを特徴とする。

【００４４】

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この電気光学装置によれば、制御手段の働きにより副画素の選択の仕方を簡単に変えることができ、この簡単な操作によって、デルタ配列又は直線的な配列のいずれかを選択できる。そして、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、文字等といった線画データは直線的な配列によりデルタ配列に比べてきれいな表示を行うことができる。つまり、本発明に係る電気光学装置によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００４５】

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【００４６】

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【００４７】

この画素構造によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００４８】

また、従来の振幅変調や時間変調による階調表示に加えて、副画素の階調の組み合わせによる面積階調を行うことで、より多階調の表示を行うことができる。

【００４９】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに前記副画素を用いて面積階調による多階調化された表示を行うことを特徴とする。

【００５０】

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【００５１】

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次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、前記副画素は当該副画素と相似形の画素電極によって形成され、観察側から見て前記画素電極の裏側に形成され、さらに前記配線は観察側から見て前記副画素を通過する直線状の配線を含むことを特徴とする。

【００５３】

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この電気光学装置によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００５４】

この構成においては、配線の引き回しが表示に影響を与えないので、画素電極の配置状態に関わらず、配線を自由にパターニングできる。このため、配線を最短でレイアウトでき、その結果、時定数を低減でき、信号遅延等を抑制できる。

【００５５】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、前記副画素は当該副画素と相似形の画素電極によって形成され、観察側から見て前記画素電極の裏側に配線が形成され、さらに前記配線は観察側から見て前記副画素を通過する直線状の配線を含むことを特徴とする。

【００５６】

この電気光学装置によれば、制御手段の働きにより副画素の選択の仕方を簡単に変えることができ、この簡単な操作によって、デルタ配列又は直線的な配列のいずれかを選択できる。そして、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、文字等といった線画データは直線的な配列によりデルタ配列に比べてきれいな表示を行うことができる。つまり、本発明に係る電気光学装置によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００５７】

この構成においては、配線の引き回しが表示に影響を与えないので、画素電極の配置状態に関わらず、配線を自由にパターニングできる。このため、配線を最短でレイアウトでき、その結果、時定数を低減でき、信号遅延等を抑制できる。

【００５８】

上記構成の電気光学装置は、観察側から見て、透光性を有する電極、液晶層、配線層及び光反射層を有することが望ましい。この構成の電気光学装置は、電気光学物質として液晶層を用いる電気光学装置である。この構成では光反射層の下の配線は表示に影響しない。

【００５９】

また、上記構成の電気光学装置は、観察側から見て、透光性を有する電極、ＥＬ発光層及び配線層を有することが望ましい。この構成の電気光学装置は、電気光学物質として有機ＥＬ層を用いる電気光学装置である。この構成では有機ＥＬ層の下の配線は表示に影響しない。

【００６０】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を４分割した形状の４つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、前記画素と相似形に形成された画素電極と、該画素電極の辺縁に沿って配置された配線とを有することを特徴とする。

【００６１】

この画素構造によれば、副画素の選択の仕方を変えるだけという簡単な操作によって、デルタ配列又は正方配列のいずれかを選択できる。そして、文字等といった線画データは正方配列で表示でき、自然画等といった画像データはデルタ配列で表示できる。デルタ配

列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、正方配列では、垂直方向又は水平方向で副画素ずらしの繰り返しになっているため解像度が高い。つまり、本発明に係る画素構造によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００６２】

本構成によれば、配線が副画素に対応する電極の辺縁に沿って配置されるので、当該副画素電極による表示が配線によって受ける悪影響を低減できる。本構成は、例えば透過型液晶装置や配線が副画素電極よりも観察側に存在するボトムエミッション型のＥＬ装置等に好適である。

【００６３】

次に、本発明に係るさらに他の電気光学装置は、デルタ配列された複数の画素を有し、該複数の画素のそれぞれは該画素を２分割した形状の２つの副画素を有し、個々の副画素の分割辺は縦方向又は横方向に沿うように配列され、さらに、前記副画素と相似形に形成された画素電極と、該画素電極の辺縁に沿って配置された配線とを有することを特徴とする。

【００６４】

この電気光学装置によれば、制御手段の働きにより副画素の選択の仕方を簡単に変えることができ、この簡単な操作によって、デルタ配列又は直線的な配列のいずれかを選択できる。そして、自然画等といった画像データはデルタ配列で表示できる。デルタ配列によれば、低容量のデータで斜め方向の解像度が向上し、自然画などを高品位の表示ができる。また、文字等といった線画データは直線的な配列によりデルタ配列に比べてきれいな表示を行うことができる。つまり、本発明に係る電気光学装置によれば、非常に簡単な画素構造により、画像と線画の両方をきれいに表示できる。

【００６５】

本構成によれば、配線が副画素に対応する電極の辺縁に沿って配置されるので、副画素に対応する電極による表示が配線によって受ける悪影響を低減できる。本構成は、例えば透過型液晶装置や配線が副画素電極よりも観察側に存在するボトムエミッション型のＥＬ装置等に好適である。

【００６６】

副画素電極の辺縁に沿って配線を配置するようにした上記構成の電気光学装置においては、互いに隣り合う副画素のための一対の配線を該副画素の直線状の分割辺に沿って直線状に配置することが望ましい。

【００６７】

こうすれば、配線がジグザグ構造にならないで直線状に形成でき、それ故、最短距離の状態に配置できる。このように配線レイアウトを最短にできるので、時定数を低減でき、信号遅延を抑制できる。

【００６８】

以上に記載した全ての構成の電気光学装置において、前記画素は６角形形状であり、前記副画素は台形形状であることが望ましい。６角形形状の複数の画素をデルタ配列で並べれば、いわゆるハニカム構造の配列を実現できる。

【００６９】

次に、本発明に係る電子機器は、以上に記載した構成の電気光学装置と、該電気光学装置の動作を制御する制御手段とを有することを特徴とする。このような電子機器としては、例えば、液晶プロジェクタ、携帯電話機、携帯情報端末機等が考えられる。

【発明を実施するための最良の形態】

【００７０】

（画素構造の第１実施形態）

以下、本発明に係る画素構造をその一実施形態を挙げて説明する。なお、本発明がこの実施形態に限定されるものでないことは、もちろんである。図１は、本発明に係る画素構造の一実施形態の平面構造の一部分を示している。ここに示す画素構造１Ａは、６角形形

状の複数の画素２をデルタ配列に並べることによって、いわゆるハニカム状に形成されている。デルタ配列とは、各画素２の中心点Ｏが破線で示す三角形Ｔの頂点に位置するような配列である。

【００７１】

各画素２は、それらの画素を４分割した形状の４つの副画素３ａ，３ｂ，３ｃ，３ｄを、各分割辺４が概接するように並べることによって形成されている。この場合、各分割辺４は、縦方向Ｙ又は横方向Ｘに沿うように配置される。縦方向Ｙは画素配列の列方向に一致し、横方向Ｘは画素配列の行方向に一致する。画素２に対する分割辺４をこのように設定したことにより、各副画素３ａ～３ｄは台形形状となっている。

【００７２】

画素とは、文字、数字、図形等といった像を表示する際の、表示の単位となる領域である。また、副画素とは、その画素をどのような状態で点灯させるかを決めるための最小単位の表示用ドットである。副画素３ａ～３ｄのうちの１つが点灯すれば、その点灯した１つの副画素によって画素が表示され、副画素３ａ～３ｄのうちの２つが点灯すれば、その点灯した２つの副画素によって画素が表示される。つまり、１つの画素２の表示状態は、副画素３ａ～３ｄのうちの点灯したものによって決められる。

【００７３】

副画素３ａ～３ｄの個々は、一般に、液晶、有機ＥＬ等といった電気光学物質を一対の電極によって挟持したときに、それらの電極が平面的に重なり合う領域として構成される。つまり、副画素３ａ～３ｄ及び画素２は、電極をそれらに対応した形状に形成することによって形成できる。なお、画素２の平面形状は、６角形に限られず、円形、多角形等とすることもできる。

【００７４】

本実施形態の画素構造によれば、複数の画素２を用いて表示を行えばデルタ配列の画素配列が構成され、それ故、低容量の画像データで斜め方向の解像度が向上して高品位の表示ができ、画像、例えば自然画の映像の表示に適した表示を行うことができる。一方、本実施形態では、１つの画素２内の副画素３ｄと、その１つの画素２に対して横方向Ｘで隣りの画素２内の副画素３ｃと、それら２つの画素と協働してデルタ配列を構成する他の画素２内の副画素３ａ及び３ｂとによって１つの画素を構成することもできる。以下、このような画素を第２画素Ａと呼ぶことにする。図１では、１つの第２画素Ａを斜線で示してある。

【００７５】

第２画素Ａの１つは略正方形又は略長方形であり、さらに、複数の第２画素Ａは縦方向Ｙ及び横方向Ｘの両方向へ直線状に並んでいる。つまり、複数の第２画素Ａは正方配列に並んでいる。この結果、複数の第２画素Ａを画素として表示を行えば、自然画等といった画像ではない、文字、図形等といった線画を鮮明な輪郭で表示することができる。

【００７６】

（画素構造の第２実施形態）

図２は、本発明に係る画素構造の他の実施形態の平面構造の一部分を示している。ここに示す画素構造１Ｂが、図１の画素構造１Ａと異なる点は、図２の画素２が図１の画素２を角度９０度だけ回転させた状態になっていることである。本実施形態では、１つの画素２内の副画素３ｄと、その１つの画素２に対して縦方向Ｙで隣りの画素２内の副画素３ｃと、それら２つの画素と協働してデルタ配列を構成する他の画素２内の副画素３ａ及び３ｂとによって斜線で示す１つの第２画素Ａが構成される。そして、複数の第２画素Ａが縦方向Ｙ及び横方向Ｘに直線状に配列されている。

【００７７】

図２の実施形態において、６角形形状の複数の画素２をデルタ配列に並べること、各画素２がそれらの画素を４分割した形状の４つの副画素３ａ，３ｂ，３ｃ，３ｄによって形成されること、各分割辺４が縦方向Ｙ又は横方向Ｘに沿うように配置されること、そして、各副画素３ａ～３ｄが台形形状となっていること、の各点は図１の実施形態の場合と同

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じである。

【００７８】

本実施形態の画素構造によれば、複数の画素２を用いて表示を行えばデルタ配列の画素配列が構成され、それ故、低容量の画像データで斜め方向の解像度が向上して高品位の表示ができ、画像、例えば自然画の映像の表示に適した表示を行うことができる。一方、正方配列に並べられた複数の第２画素Ａを用いて表示を行えば、画像ではない、文字、図形等といった線画を鮮明な輪郭で表示することができる。

【００７９】

（画素構造の第３実施形態）

図３は、本発明に係る画素構造のさらに他の実施形態の平面構造の一部分を示している。ここに示す画素構造１Ｃが、図１の画素構造１Ａと異なる点は、副画素を形成するにあたって、画素２を４つに分割することに代えて、２つに分割したことである。つまり、本実施形態では、２つの台形形状の副画素３ａ及び３ｂによって１つの画素２が形成されている。

【００８０】

この実施形態において、複数の画素２はデルタ配列に並べられている。そして、第２画素Ａは、図３に実線の斜線で示すように、１つの画素２の右側の副画素３ｂと、その横方向Ｘで隣りの画素２の左側の副画素３ａとによって形成されるか、又は、破線の斜線で示すように、１つの画素２のそれ自体によって形成される。これにより、複数の第２画素Ａが縦方向Ｙに直線状に配列されている。

【００８１】

本実施形態の画素構造によれば、複数の画素２を用いて表示を行えばデルタ配列の画素配列が構成され、それ故、低容量の画像データで斜め方向の解像度が向上して高品位の表示ができ、画像、例えば自然画の映像の表示に適した表示を行うことができる。一方、縦に直線状に並べられた複数の第２画素Ａを用いて表示を行えば、画像ではない、文字、図形等といった線画を鮮明な輪郭で表示することができる。

【００８２】

（画素構造の第４実施形態）

図４は、本発明に係る画素構造のさらに他の実施形態の平面構造の一部分を示している。ここに示す画素構造１Ｄでは、図３に示した画素構造と同様に、２つの台形形状の副画素３ａ及び３ｂによって１つの画素２が形成されている。この画素構造１Ｄが図３の画素構造１Ｃと異なる点は、図４の画素２が図３の画素２を角度９０度だけ回転させた状態になっていることである。

【００８３】

この実施形態において、複数の画素２はデルタ配列に並べられている。そして、第２画素Ａは、図３に実線の斜線で示すように、１つの画素２の下側の副画素３ａと、その縦方向Ｙで隣りの画素２の上側の副画素３ｂとによって形成されるか、又は、破線の斜線で示すように、１つの画素２のそれ自体によって形成される。これにより、複数の第２画素Ａが横方向Ｘに直線状に配列されている。

【００８４】

本実施形態の画素構造によれば、複数の画素２を用いて表示を行えばデルタ配列の画素配列が構成され、それ故、低容量の画像データで斜め方向の解像度が向上して高品位の表示ができ、画像、例えば自然画の映像の表示に適した表示を行うことができる。一方、横に直線状に並べられた複数の第２画素Ａを用いて表示を行えば、画像ではない、文字、図形等といった線画を鮮明な輪郭で表示することができる。

【００８５】

（電気光学装置の第１実施形態）

図５は、本発明に係る電気光学装置の一実施形態であって、本発明に係る画素構造を駆動するのに適した制御回路を備えた電気光学装置を示している。この電気光学装置は、自然画等といった画像のデータ及び文字、数字等といった線画のデータを入力するデータ入

力部５１と、圧縮データを解凍したり画像データと線画データとを判別したりするデータ処理部５２と、データ出力部５３と、像を表示する表示部５４とを有する。表示部５４は、自然画等といった画像や、文字、数字等といった線画を映像として表示するものであり、例えば、ＣＲＴ（Cathode Ray Tube）や液晶装置等を用いて構成できる。

【００８６】

データ出力部５３は、データ処理部５２で判別された画像データと線画データとを分配するデータ分配部５６と、データ分配部５６の一方の出力端子から出力される画像データに好適な処理を行う画像データ処理部５７と、データ分配部５６の他方の出力端子から出力される線画データに好適な処理を行う線画データ処理部５８と、画像データ処理部５７からの出力データと線画データ処理部５８からの出力データとを合成して表示部５４へ供給するデータ合成部５９とを有する。画像データ処理部５７は、例えば図１においてデルタ配列された複数の画素２を用いて表示を行うためのデータ処理を行う。一方、線画データ処理部５８は、例えば図１において正方配列された複数の第２画素Ａを用いて表示を行うためのデータ処理を行う。

【００８７】

図５に示す制御回路によれば、画像データと線画データとを別々に処理した後、それらを合成して出力データとして出力する。これにより、表示しようとしているデータの種類に応じて、デルタ配列と図１及び図２における正方配列との選択、あるいは、デルタ配列と図３及び図４における直線状の配列との選択、を必要に応じて切り替えることができる。これにより、高品位の表示を行うことができる。なお、データ合成部５９は、画像データと線画データとが重複する場合に、どちらを強調するかを判断してそれらのデータの合成を行うことが望ましい。

【００８８】

表示データとしてインターネットからの情報を考えると、その情報はＨＴＭＬ（Hyper Text Markup Language）という表現言語で記述される。また、表示データとしてデジタル放送を考えると、その情報はＢＭＬ（Broad Markup Language）という表示言語で記述される。例えば、データのうち画像データはデルタ配列で表示し、線画データは正方配列又は直線状の配列で表示するように分配することにより、それぞれのデータに適した表示を行うことができる。

【００８９】

また、ＤＶＤ等で使われるＭＰＥＧ－２ＰＳ（プログラム・ストリーム）では、ビデオやオーディオの圧縮符号化データであるＥＳ（エレメンタリー・ストリーム）を複数多重化している。画像データと字幕等といった文字データ（すなわち、線画データ）は異なるＥＳとしてあるので、それらを分配してそれぞれに適した表示を行うことができる。

【００９０】

また、デジタル放送等で使われるＭＰＥＧ－２ＴＳ（トランスポート・ストリーム）では、ＭＰＥＧ－２ＰＳとは多重化の方法が異なっているが、同時に画像データ、文字データが異なるＰＥＳ（パケット化されたＥＳ）としてあるので、それらを分配してそれぞれのデータに適した表示を行うことができる。

【００９１】

また、携帯電話機等で用いられるＭＰＥＧ－４は、ＭＰＥＧ－２と異なり、画面を人物、背景、文字、図形、音声等といったオブジェクトに分け、それぞれに適した符号化を行っている。従って、この場合には、画像データと線画データを分配してそれぞれに適した表示を行うことができる。

【００９２】

また、アナログ放送等では、画像データと文字データとが１枚の絵として送られる。よって、画像データと文字データとを分配してそれぞれに適した表示を行うには、適当な処理によって画像データと文字データをそれぞれに検出する処理を行うことが望ましい。

【００９３】

（電気光学装置の第２実施形態）

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図６及び図７は本発明に係る電気光学装置の第２実施形態を示している。この実施形態は、電気光学装置の１つである液晶装置に本発明を適用して、空間加法混色によってカラー表示を行う場合の実施形態である。空間加法混色とは、周知の通り、Ｒ，Ｇ，Ｂ等といった複数色が互いに重なることなく、しかし近接して配置されているときに、人間がこれらの色を見たときに混色を知覚することにより、カラー表示を行う手法である。

【００９４】

液晶装置としては、ＴＦＴ（Thin Film Transistor）等といった３端子型のアクティブ素子をスイッチング素子として用いるアクティブマトリクス型の液晶装置や、ＴＦＤ（Thin Film Diode）等といた２端子型のアクティブ素子をスイッチング素子として用いるアクティブマトリクス型の液晶装置や、スイッチング素子を用いないパッシブマトリクス型の液晶装置等を用いることができる。本実施形態では、ＴＦＤ（Thin Film Diode）を用いたアクティブマトリクス型で半透過反射方式の液晶装置を例示する。なお、図６及び図７において、各種の構成要素は、それらを分かり易く示すために実際のものと異なる縮尺で示されている。

【００９５】

図６に示す液晶装置２０は、液晶パネル２１及び照明装置２２を有する。照明装置２２は、冷陰極管、ＬＥＤ（Light Emitting Diode）等によって構成される光源１９と、その光源１９からの光を導入して面状の光として出射する導光体１８とを有する。また、液晶パネル２１は、素子基板２３ａと対向基板２３ｂとを矢印Ｂで示す観察側から見て四角形状でリング状のシール材２４によって貼り合わせることによって形成されている。両基板２３ａ及び２３ｂの間には、スペーサ２５によって保持された微小な間隙、いわゆるセルギャップが形成され、そのセルギャップ内に電気光学物質としての液晶が封入されて液晶層２６が形成されている。

【００９６】

素子基板２３ａは、透光性を有するガラス、透光性を有するプラスチック等によって形成された基材２７ａを有し、その基材２７ａの液晶側表面上に、ＴＦＤ素子２８、画素電極２９、及び配向膜３０ａが形成されている。また、基材２７ａの外側表面には、偏光板、その他の必要な光学要素３１ａが設けられる。配向膜３０ａはポリイミド等によって形成され、その表面に配向処理、例えばラビング処理が施される。

【００９７】

ＴＦＤ素子２８は、例えば、第１金属／絶縁層／第２金属の３層構造（すなわち、Metal／Insulator／Metalの積層構造、いわゆる、ＭＩＭ構造）を有し、所定の閾値以上の電圧が印加されたときに通電を許容する、すなわちスイッチング動作する。画素電極２９はその１つずつが、例えば図１に示すような副画素３ａ～３ｄに対応した台形形状に形成され、それらの台形形状の画素電極２９の集まりによって画素２が構成されている。なお、画素電極２９はＩＴＯ（Indium Tin Oxide）その他の透明導電材料によって形成される。

【００９８】

図６において、対向基板２３ｂは、透光性を有するガラス、透光性を有するプラスチック等によって形成された基材２７ｂを有し、その基材２７ｂの液晶側表面上に、光反射膜３２、カラーフィルタ３３、ストライプ状の対向電極３４、及び配向膜３０ｂが形成されている。配向膜３０ｂはポリイミド等によって形成され、その表面に配向処理、例えばラビング処理が施される。なお、基材２７ｂの外側表面には、偏光板、その他の必要な光学要素３１ｂが設けられる。

【００９９】

光反射膜３２は、Ａｌ（アルミニウム）等といった光反射性の金属材料によって形成されている。また、光反射膜３２のうち各副画素３ａ～３ｄに対応する位置には、光透過用の開口３５が形成されている。光反射膜３２の光反射部分は反射型表示時において観察側Ｂから入射した光を反射して液晶層２６へ供給する。一方、光反射膜３２に形成した開口３５は透過型表示時において照明装置２２から発生した面状の光を透過して液晶層２６へ供給する。

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【０１００】
カラーフィルタ３３は、矢印Ｂ方向から見て所定のパターンで配列されたＲ，Ｇ，Ｂの３色の着色要素３６と、それらの着色要素３６の間を埋めるように形成された遮光層３７とによって構成されている。遮光層３７は、Ｃｒ（クロム）その他の遮光性材料によって形成される。また、着色要素３６は、Ｒ，Ｇ，Ｂの各色に相当する顔料、染料等を含んだ材料によって形成される。本実施形態では、Ｒ，Ｇ，Ｂの配色は素子基板２３ａ側の画素電極２９との関連で決められており、具体的には、図７に示すように、各副画素３ａ～３ｄごとにＲ，Ｇ，Ｇ，Ｂの色配置で割り当てられる。より具体的には、副画素３ａにＧ色、副画素３ｂにＢ色、副画素３ｃにＲ色、そして副画素３ｄにＧ色が割り当てられる。このような色配置により、空間加法混色によるカラー表示が行われる。１つの画素内にＧ色を２個配置するのは、人間の眼はＧ色の視感度が高いためである。

【０１０１】
図６において、対向電極３４の１本は図６の左右方向へ延びる直線状、すなわち帯状であり、その帯状電極の複数本が図６の紙面垂直方向へ適宜の間隔をおいて平行に並べられている。これにより、複数本の対向電極３４が矢印Ｂ方向から見てストライプ状に形成されている。なお、対向電極３４はＩＴＯ等といった透明導電材料によって形成されている。

【０１０２】
素子基板２３ａは、対向基板２３ｂの外側へ張り出す張出し部３８を有する。この張出し部３８には配線３９が形成され、この配線３９がシール材２４の内側へ延びて画素電極２９や対向電極３４に接続されている。また、張出し部３８の辺縁には外部回路（図示せず）との間で電気的な接続をとるための外部接続端子４０が形成されている。張出し部３８の表面には駆動用ＩＣ４１が実装され、その駆動用ＩＣ４１の入力側バンプが外部接続端子４０に接続し、その出力側バンプが配線３９に接続している。駆動用ＩＣ４１の働きにより、画素電極２９及び対向電極３４に走査信号及びデータ信号が印加される。

【０１０３】
本実施形態の液晶装置２０によれば、図７において、複数の画素２を用いて表示を行えばデルタ配列の画素配列が構成され、それ故、低容量の画像データで斜め方向の解像度が向上して高品位の表示ができ、画像、例えば自然画の映像の表示に適した表示を行うことができる。一方、複数の第２画素Ａ（図１参照）を画素として表示を行えば、ストライプ、モザイク等といった正方配列の画素配列が構成され、それ故、画像ではない、文字、図形等といった線画を鮮明な輪郭で表示することができる。

【０１０４】
なお、本実施形態で採用できる画素構造は図７の画素構造、すなわち図１の画素構造に限られない。例えば、図２、図３、図４、その他本発明の範囲内にある任意の画素構造を採用できる。

【０１０５】
（電気光学装置の第３実施形態）
図８は本発明に係る電気光学装置のさらに他の実施形態を示している。この実施形態は、構造的には概ね図６及び図７に示した先の液晶装置と同じであるが、図８に示す画素構造１Ａに対する各色光の配置の仕方に改変が加えられている。具体的には、本実施形態では、副画素３ａ～３ｄに対応させて全て異なる色を配置する。例えば、Ｒ，Ｇ，Ｂに加えてＷ（すなわち、白）を加え、それらの各色の配色が図６の素子基板２３ａ側の画素電極２９との関連で決められている。より具体的には、図８に示すように、副画素３ａにＷ色、副画素３ｂにＢ色、副画素３ｃにＲ色、そして副画素３ｄにＧ色が割り当てられる。このような色配置により、空間加法混色によるカラー表示が行われる。Ｗ色を配置することにより、本実施形態では白表示を明るく表示できる。また、Ｗ以外の４色目を選べば色再現範囲が広がる。

【０１０６】
なお、本実施形態で採用できる画素構造は図７の画素構造、すなわち図１の画素構造に

限られない。例えば、図２、図３、図４、その他本発明の範囲内にある任意の画素構造を採用できる。

【０１０７】

（電気光学装置の第４実施形態及び電子機器の第１実施形態）

次に、本発明に係る電子機器の一実施形態を説明すると共に、その電子機器に用いられる本発明に係る電気光学装置のさらに他の実施形態を説明する。これから説明する実施形態は、図７に示した画素構造、すなわち図１に示した画素構造を用いて、積分的加法混色によってカラー表示を行う構造の液晶装置及びそれを用いた液晶プロジェクタに関するものである。ここで、積分的加法混色について簡単に説明すれば、前述した空間加法混色がＲ，Ｇ，Ｂ等といった各色を実際には重ね合わせないことに対し、積分的加法混色は異なる色を実際に重ね合わせてカラー表示を行う手法である。

【０１０８】

図９は、その積分的加法混色を実現する液晶装置を含んで構成される電子機器の一例である液晶プロジェクタを示している。この液晶プロジェクタ６０は、光を放出する光源６３と、Ｒ色光を反射してその他の波長の光を透過するダイクロイックミラー６４ｒと、Ｇ色光を反射してその他の波長の光を透過するダイクロイックミラー６４ｇと、Ｂ色光を反射してその他の光を透過するダイクロイックミラー６４ｂと、反射ミラー６５と、Ｒ色光の光路上に配置されたＲ色液晶ライトバルブ６６ｒと、Ｇ色光の光路上に配置されたＧ色光液晶ライトバルブ６６ｇと、Ｂ色光の光路上に配置されたＢ色液晶ライトバルブ６６ｂと、各色光を合成するダイクロイックプリズム６７と、投射レンズ６８と、スクリーン６９とを有する。光源６３は、白色光を発生するランプ６１と、リフレクタ６２とによって構成される。

【０１０９】

本実施形態で液晶装置は、個々の液晶ライトバルブ６６ｒ，６６ｇ，６６ｂと、対応する波長の光をそれらの液晶ライトバルブに供給する光供給系とによって構成される。光供給系は、本実施形態の場合、光源６３、ダイクロイックミラー６４ｒ，６４ｇ，６４ｂ、及び反射ミラー６５によって構成される。

【０１１０】

各液晶ライトバルブ６６ｒ，６６ｇ，６６ｂは、それぞれ、図１０に示すように、素子基板７１ａと対向基板７１ｂとを矢印Ｂ方向から見て四角形状でリング状のシール材７２によって貼り合わせることによって形成されている。両基板７１ａ及び７１ｂの間には、微小な間隙、いわゆるセルギャップが形成され、そのセルギャップ内に電気光学物質としての液晶が封入されて液晶層７３が形成されている。液晶層７３は、例えば、１種又は数種類のネマチック液晶を混合した液晶によって形成される。

【０１１１】

素子基板７１ａは、透光性を有するガラス、透光性を有するプラスチック等によって形成された基材７４ａを有し、その基材７４ａの液晶側表面上に、ＴＦＴ素子７５、画素電極７６、及び配向膜７７ａが形成されている。また、基材７４ａの外側表面には、偏光板、あるいはその他の必要な光学要素７８ａが設けられる。配向膜７７ａはポリイミド等によって形成され、その表面に配向処理、例えばラビング処理が施される。

【０１１２】

対向基板７１ｂは、透光性を有するガラス、透光性を有するプラスチック等によって形成された基材７４ｂを有し、その基材７４ｂの液晶側表面上に、対向電極７９及び配向膜７７ｂが形成されている。また、基材７４ｂの外側表面には、偏光板、その他の必要な光学要素７８ｂが設けられる。対向電極７９は、有効表示領域の略全面にわたってＩＴＯ等といった透明導電材料によって共通電極として形成されている。また、配向膜７７ｂはポリイミド等によって形成され、その表面に配向処理、例えばラビング処理が施される。

【０１１３】

素子基板７１ａの表面に形成される複数の画素電極７６は、その１つずつが、例えば図１に示すような副画素３ａ～３ｄに対応した台形形状に形成され、それらの台形形状の画

素電極７６の集まりによって画素２が構成されている。なお、画素電極７６はＩＴＯその他の透明導電材料によって形成される。

【０１１４】

素子基板７１ａは、対向基板７１ｂの外側へ張り出す張出し部１０１を有する。この張出し部１０１には配線１０２が形成され、この配線１０２がシール材７２の内側へ延びて画素電極７６や対向電極７９に接続されている。また、張出し部１０１の辺縁には外部回路（図示せず）との間で電気的な接続をとるための外部接続端子１０３が形成されている。張出し部１０１の表面には駆動用ＩＣ１０４が実装され、その駆動用ＩＣ１０４の入力側バンプが外部接続端子１０３に接続し、その出力側バンプが配線１０２に接続している。駆動用ＩＣ１０４の働きにより、画素電極７６及び対向電極７９に走査信号及びデータ信号が印加される。

【０１１５】

以下、素子基板７１ａの液晶側表面上に形成されるＴＦＴ素子７５及び画素電極７６について簡単に説明する。図１１は、ＴＦＴ素子７５、画素電極７６、さらに、それらに付随する各種要素についての等価回路を示している。また、図１２は、素子基板７１ａにおけるＴＦＴ素子７５の近傍の断面構造を示している。なお、図１２においては、各要素の構造を分かり易く示すために、各要素の寸法の縮尺を実際のものと異ならせてある。

【０１１６】

図１１において、画像信号Ｓ１，Ｓ２，…，Ｓｎを供給するための配線であるデータ線８１が設けられる。また、走査信号Ｇ１，Ｇ２，…，Ｇｍを供給するための配線である走査線８２が設けられる。また、容量線８３が設けられる。ＴＦＴ素子７５のソースはデータ線８１に接続され、ＴＦＴ素子７５のゲートは走査線８２に接続される。画素電極７６は、ＴＦＴ素子７５のドレインに接続され、ＴＦＴ素子７５を一定期間だけ閉じることにより、データ線８１から供給される画像信号Ｓ１，Ｓ２，…を所定のタイミングで書き込む。書き込まれた画像信号は、対向基板に形成された対向電極との間で一定期間保持される。

【０１１７】

また、保持された画像信号のリークによってコントラスト比の低下やフリッカと呼ばれるちらつき等を防ぐため、画素電極７６と対向電極７９（図１０参照）との間に形成される液晶容量と並列に蓄積容量８４を付加する。このような蓄積容量８４を形成するため、例えば、走査線８２と同層に容量線８３を設ける。

【０１１８】

次に、図１２に基づいて、図１０のＴＦＴ素子７５の近傍の断面構造を説明する。同図において、素子基板７１ａは、石英等から成る基材７４ａと、画素電極７６と、ＴＦＴ素子７５と、配向膜７７ａとを有する。ＴＦＴ素子７５は各画素電極７６をスイッチング制御する。一方、対向基板７１ｂは、透明なガラス、透明な石英等といった光透過性材料から成る基材７４ｂを有し、その基材７４ｂの液晶側表面上に、対向基板遮光層８６と、対向電極７９と、配向膜７７ｂとが形成される。

【０１１９】

素子基板７１ａは、例えば基材７４ａ上に単結晶シリコン基板を貼り合わせて成る複合基板を用いたものであり、基材７４ａの液晶側表面上に設けられた下側貼り合わせ膜８７と、その下側貼り合わせ膜８７の上に設けられている上側貼り合わせ膜８８との間が、基材７４ａと半導体基板との貼り合わせの界面となっている。上側貼り合わせ膜８８の表面上において、各ＴＦＴ素子７５に対応する位置には、不透明な高融点金属、例えばＴｉ，Ｃｒ等から成る遮光層８９が埋め込まれている。この遮光層８９は、単結晶シリコン基板の基材７４ａと貼り合わされる側の面に形成され、その後、基材７４ａ上に単結晶シリコン基板を貼り合わせることにより基材７４ａ上に形成されたものである。従って、遮光層８９は、遮光層８９が設けられた単結晶シリコン基板上に遮光層８９を覆うように形成された上側貼り合わせ膜８８によって埋め込まれた状態となっている。

【０１２０】

上側貼り合わせ膜８８上及び遮光層８９上には、第１層間絶縁膜９１が設けられている。この第１層間絶縁膜９１は、ＴＦＴ素子７５を構成する半導体層９２を遮光層８９から電気的に絶縁するためのものであり、基材７４ａの表面上の全面に形成されている。また、第１層間絶縁膜９１は、遮光層８９がＴＦＴ素子７５等を汚染するのを防止する。なお、複合基板ではなく公知の高温多結晶シリコンプロセスを用いて素子基板７１ａを形成できることは言うまでもない。

【０１２１】

遮光層８９及びこれに電気的に接続された容量線８３は、第１層間絶縁膜９１を貫通して遮光層８９に達するコンタクトホール９３を介して、定電位源に電気的に接続されることにより、定電位とされている。従って、遮光層８９に対向して配置されるＴＦＴ素子７５に対して遮光層８９の電位変動が悪影響を及ぼすことはない。

【０１２２】

ゲート絶縁膜９４を走査線８２に対向する位置から延設して誘電体膜として用い、半導体膜９２を延設して第１蓄積容量電極９２ｆとし、さらに、これらに対向する容量線８３の一部を第２蓄積容量電極とすることにより、蓄積容量９５が構成されている。より詳細には、半導体層９２の高濃度ドレイン領域９２ｅがデータ線８１及び走査線８２の下に延設されて、同じくデータ線８１及び走査線８２に沿って延びる容量線８３の部分に絶縁膜９４を介して対向配置されて、第１蓄積容量電極９２ｆとされている。特に、蓄積容量９５の誘電体としての絶縁膜９４は、高温酸化により単結晶半導体層上に形成されるＴＦＴ素子７５のゲート絶縁膜９４に他ならないので、薄く且つ高耐圧の絶縁膜とすることができ、蓄積容量９５は比較的小面積で大容量の蓄積容量として構成できる。

【０１２３】

ＴＦＴ素子７５は、ＬＤＤ（Lightly Doped Drain）構造を有しており、走査線８２と、該走査線８２からの電界によりチャネルが形成される半導体層９２のチャネル領域９２ａと、走査線８２と半導体層９２とを絶縁するゲート絶縁膜９４と、データ線８１と、半導体層９２の低濃度ソース領域（すなわち、ソース側ＬＤＤ領域）９２ｂと、低濃度ドレイン領域（すなわち、ドレイン側ＬＤＤ領域）９２ｃと、半導体層９２の高濃度ソース領域９２ｄと、高濃度ドレイン領域９２ｅとを有する。

【０１２４】

また、走査線８２、ゲート絶縁膜９４及び第１層間絶縁膜９１の上には、第２層間絶縁膜９６が形成されている。この第２層間絶縁膜９６には、高濃度ソース領域９２ｄへ通じるコンタクトホール９７及び高濃度ドレイン領域９２ｅへ通じるコンタクトホール９８が各々形成されている。ソース領域９２ｄへのコンタクトホール９７を介して、データ線８１は高濃度ソース領域９２ｄに電気的に接続されている。さらに、データ線８１及び第２層間絶縁膜９６の上には、第３層間絶縁膜９９が形成され、その第３層間絶縁膜９９には高濃度ドレイン領域９２ｅへのコンタクトホール９８が形成される。このコンタクトホール９８を介して、画素電極７６が高濃度ドレイン領域９２ｅに電気的に接続されている。

【０１２５】

上記構成より成る液晶ライトバルブ６６ｒ，６６ｇ，６６ｂには、図９に示したように、それぞれにＲ色光、Ｇ色光、Ｂ色光が供給される。各液晶ライトバルブで変調された後、ダイクロイックプリズム６７で合成され、積分的加法混色によるカラー表示が行われる。

【０１２６】

本実施形態の液晶ライトバルブ６６ｒ，６６ｇ，６６ｂによれば、図７において、複数の画素２を用いて表示を行えばデルタ配列の画素配列が構成され、それ故、低容量の画像データで斜め方向の解像度が向上して高品位の表示ができ、画像、例えば自然画の映像の表示に適した表示を行うことができる。一方、複数の第２画素Ａ（図１参照）を画素として表示を行えば、ストライプ、モザイク等といった正方配列の画素配列が構成され、それ故、画像ではない、文字、図形等といった線画を鮮明な輪郭で表示することができる。

【０１２７】

なお、本実施形態で採用できる画素構造は図７の画素構造、すなわち図１の画素構造に限られない。例えば、図２、図３、図４、その他本発明の範囲内にある任意の画素構造を採用できる。

【０１２８】

（電気光学装置の第５実施形態及び電子機器の第２実施形態）

図１３は、積分的加法混色を実現する液晶装置を含んで構成される電子機器の一例である液晶プロジェクタを示している。この液晶プロジェクタ１０６は、光を放出する光源６３と、フィルタ装置１０７と、液晶ライトバルブ６６と、投射レンズ６８と、スクリーン６９とを有する。光源６３は、白色光を発生するランプ６１と、リフレクタ６２とによって構成される。

【０１２９】

フィルタ装置１０７は、軸線Ｘ０を中心として矢印Ｃのように回転可能な回転体１０８と、その回転体１０８の円周軌跡上に設けられた複数、本実施形態では８個のフィルタ要素１０９とを有する。回転体１０８の回転移動は、モータ等といった駆動源を用いて画像データと同期して自動的に行われる。複数のフィルタ要素１０９は、Ｒ，Ｇ，Ｂを含んで９種類の異なった色に対応している。例えば、Ｒ，Ｇ，Ｂ，Ｗ，Ｒ’，Ｇ’，Ｂ’等といった色を含むものとする。ここで、Ｗは白、Ｒ’はＲではないがＲに近い色、Ｇ’はＧではないがＧに近い色、Ｂ’はＢではないがＢに近い色を示している。

【０１３０】

複数のフィルタ要素１０９に関しては、回転体１０８の回転に従って、希望するいずれか１つを光源６３から液晶ライトバルブ６６へ至る光路Ｌ０上に配置できる。これにより、希望する色を液晶ライトバルブへ供給できる。また、回転体１０８の回転速度を高速にすれば、異なる複数の色を重ねた状態で人間の眼に表示できる。これにより、積分的加法混色によるカラー表示を行うことができる。本実施形態で液晶装置は、液晶ライトバルブ６６と、複数波長の光を液晶ライトバルブ６６に供給する光供給系とによって構成される。光供給系は、本実施形態の場合、光源６３及びカラーフィルタ装置１０７によって構成される。

【０１３１】

本実施形態では、液晶ライトバルブ６６内に図１に示すような画素２及び副画素３ａ～３ｄが設けられている。Ｗ，Ｂ，Ｒ，Ｇの色、あるいは、それ以上の種類の色を設定できる。図１において複数の画素２を用いて表示を行えばデルタ配列の画素配列が構成され、それ故、低容量の画像データで斜め方向の解像度が向上して高品位の表示ができ、画像、例えば自然画の映像の表示に適した表示を行うことができる。一方、複数の第２画素Ａ（図１参照）を画素として表示を行えば、ストライプ、モザイク等といった正方配列の画素配列が構成され、それ故、画像ではない、文字、図形等といった線画を鮮明な輪郭で表示することができる。

【０１３２】

なお、本実施形態で採用できる画素構造は図１の画素構造に限られない。例えば、図２、図３、図４、その他本発明の範囲内にある任意の画素構造を採用できる。

【０１３３】

（電気光学装置の第６実施形態）

図１２に示した液晶ライトバルブ６６ｒ，６６ｇ，６６ｂは、素子基板７１ａ内の画素電極７６を透明材料によって形成し、さらに対向基板７１ｂ内の対向電極７９も透明材料によって形成した。このため、液晶ライトバルブ６６ｒ，６６ｇ，６６ｂは透過型の液晶装置として構成されている。これに対し、画素電極７６を光反射性の導電材料によって形成すれば、液晶ライトバルブ６６ｒ，６６ｇ，６６ｂを対向基板７１ｂ側を観察側とする反射型の液晶装置として使用できる。

【０１３４】

この場合には、データ線８１及び走査線８２は観察側から見て画素電極７６の裏側に配置されると共に、画素電極７６は不透明であるので、データ線８１及び走査線８２の引き

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回しは画素電極７６の位置に関わらず、比較的自由に行うことができる。例えば、図１４に示す例では、走査線８２の一部８２ａが副画素３ａ～３ｄのいずれかを横切るように配置されているが、それらの副画素が不透明な反射層を兼用するのであれば、走査線８２ａが表示に悪影響を及ぼすことはない。

【０１３５】

また、図１５に示すように画素２が２つの副画素３ａ及び３ｂによって形成される場合、走査線８２が副画素３ａ及び３ｂを横切る配置となることがある。しかしながら、この場合でも、走査線８２が表示に悪影響を及ぼすことはない。

【０１３６】

なお、以上の説明では、走査線８２等が副画素を横切る場合でも表示に悪影響が及ばない例として反射型液晶装置を例示した。しかしながら、トップエミッション型のＥＬ装置に関しても同様のことが言える。何故ならば、トップエミッション型のＥＬ装置では、ＴＦＴ素子、走査線、データ線等が形成された素子基板の上に電極を形成し、その電極の上に有機ＥＬ発光層を形成し、さらにその有機ＥＬ発光層の上に透明電極を形成するという構成が採用されるので、走査線やデータ線が表示の邪魔にならないからである。

【０１３７】

（電気光学装置の第７実施形態）

図１２に示した液晶ライトバルブ６６ｒ，６６ｇ，６６ｂは、素子基板７１ａ内の画素電極７６を透明材料によって形成し、さらに対向基板７１ｂ内の対向電極７９も透明材料によって形成した。このため、液晶ライトバルブ６６ｒ，６６ｇ，６６ｂは透過型の液晶装置として構成されている。このような透過型の液晶装置では、走査線、データ線等といった配線が図１の副画素３ａ～３ｄを横切ると、表示に悪影響が及ぶおそれがある。これを回避するため、配線は副画素３ａ～３ｄを横切らないよう、副画素３ａ～３ｄの分割辺４やその外周辺縁に沿って配置することが望ましい。例えば、図１６に示す実施形態では、走査線８２ａを副画素３ａ～３ｄの外周辺縁に沿うように配置してある。

【０１３８】

図１６は画素２を４つの副画素３ａ～３ｄに分割する場合の適用例であるが、図１７に示すように、画素２を２分割する場合にも、走査線８２、データ線８１、あるいはその他の配線を副画素３ａ及び３ｂの分割辺４や外周辺縁に沿わせて配置することが望ましい。

【０１３９】

なお、走査線８２等といった配線を副画素の分割辺や外周辺縁に沿わせるという構成は、上記のような透過型の液晶装置に限られず、ボトムエミッション型の有機ＥＬ装置に対しても好適である。何故ならば、ボトムエミッション型の有機ＥＬ装置では、ＴＦＴ素子、走査線、データ線等が形成された素子基板の上に透明電極を形成し、その透明電極の上に有機ＥＬ発光層を形成し、さらにその有機ＥＬ発光層の上に不透明電極を形成することにより、素子基板側を観察側とするので、走査線、データ線、その他の配線が表示の邪魔になるからである。

【０１４０】

（電気光学装置の第８実施形態）

図１６の実施形態や図１７の実施形態では、走査線８２等といった配線がジグザグの配列構造をとっているので、配線抵抗や断線を考慮すると好ましくない。このことを解消するため、図１８に示すように、配線、例えば走査線８２を副画素３ａ～３ｄの分割辺４に沿って２本まとめて直線的に配置することが望ましい。この場合、複数の走査線８２の間隔は等間隔ではなくて不等間隔になるが、表示上は何等の問題はない。

【０１４１】

（その他の実施形態）

以上、好ましい実施形態を挙げて本発明を説明したが、本発明はその実施形態に限定されるものでなく、請求の範囲に記載した発明の範囲内で種々に改変できる。

【０１４２】

例えば、以上の説明では電気光学装置として、液晶装置、有機ＥＬ装置を例示したが、

本発明はその他任意の電気光学装置、例えば、ＰＤＰ（Plasma Display：プラズマディスプレイ装置）、ＦＥＤ（Field Emission Display：フィールドエミッションディスプレイ装置）、ＳＥＤ（Surface-Conduction Electron-Emitter Display）等にも適用できる。

【産業上の利用可能性】

【０１４３】

本発明に係る画素構造は、液晶装置、有機ＥＬ装置等といった電気光学装置において画像や線画を表示する際に好適に用いられる。また、本発明に係る電気光学装置は、電子機器としての液晶プロジェクタにおけるライトバルブとして用いられたり、携帯電話機、携帯情報端末機等といった電子機器において各種の表示を行うための表示装置として用いられたりする。また、本発明に係る電子機器は、液晶プロジェクタ、携帯電話機、携帯情報端末機等として利用される。

【図面の簡単な説明】

【０１４４】

【図１】本発明に係る画素構造の一実施形態を示す平面図である。

【図２】本発明に係る画素構造の他の一実施形態を示す平面図である。

【図３】本発明に係る画素構造のさらに他の一実施形態を示す平面図である。

【図４】本発明に係る画素構造のさらに他の一実施形態を示す平面図である。

【図５】本発明に係る電気光学装置の一実施形態を示す制御ブロック図である。

【図６】本発明に係る電気光学装置の他の一実施形態である液晶装置の断面構造を示す断面図である。

【図７】図６の電気光学装置で用いる画素構造と光の色との関連の一例を示す平面図である。

【図８】図６の電気光学装置で用いる画素構造と光の色との関連の他の一例を示す平面図である。

【図９】本発明に係る電子機器の一実施形態である液晶プロジェクタの構造を示す図である。

【図１０】図９の液晶プロジェクタで用いられる液晶ライトバルブの一例を示す断面図である。

【図１１】図１０の液晶ライトバルブで用いられるＴＦＴ素子及びそれに接続される各要素の等価回路を示す図である。

【図１２】図１１に示す等価回路内のＴＦＴ素子の具体的な構造の一例を示す断面図である。

【図１３】本発明に係る電子機器の一実施形態である液晶プロジェクタの構造の他の例を示す図である。

【図１４】本発明に係る電気光学装置のさらに他の実施形態の要部である、画素と配線との関係を示す平面図である。

【図１５】本発明に係る電気光学装置のさらに他の実施形態の要部である、画素と配線との関係を示す平面図である。

【図１６】本発明に係る電気光学装置のさらに他の実施形態の要部である、画素と配線との関係を示す平面図である。

【図１７】本発明に係る電気光学装置のさらに他の実施形態の要部である、画素と配線との関係を示す平面図である。

【図１８】本発明に係る電気光学装置のさらに他の実施形態の要部である、画素と配線との関係を示す平面図である。

【符号の説明】

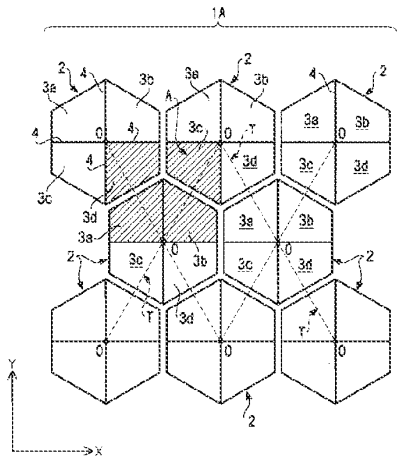
【０１４５】

１Ａ，１Ｂ，１Ｃ，１Ｄ：画素構造、　２：画素、　３ａ，３ｂ，３ｃ，３ｄ：副画素、　４：分割辺、　２０：液晶装置（電気光学装置）、　２１：液晶パネル、　２２：照明装置、　２３ａ：素子基板、　２３ｂ：対向基板、　２６：液晶層、　２７ａ，２７ｂ：基材、　２８：ＴＦＤ素子、　２９：画素電極、　３３：カラーフィルタ、

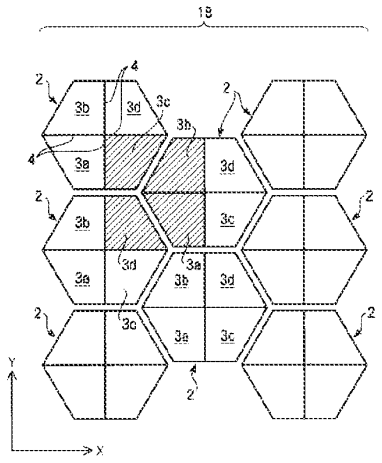
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３４：対向電極、　３６：着色要素、　６０：液晶プロジェクタ（電子機器）、
６６ｒ，６６ｇ，６６ｂ：液晶ライトバルブ（電気光学装置）、　６４：ダイクロイックミラー、　６５：反射ミラー、　７１ａ：素子基板、　７１ｂ：対向基板、
７３：液晶層、　７４ａ，７４ｂ：基材、　７５：ＴＦＴ素子、　７６：画素電極、
７９：対向電極、　８１：データ線、　８２：走査線、　８３：容量線、
１０６：液晶プロジェクタ（電子機器）、　１０７：フィルタ装置、　１０８：回転体、
１０９：フィルタ要素、　Ａ：第２画素、

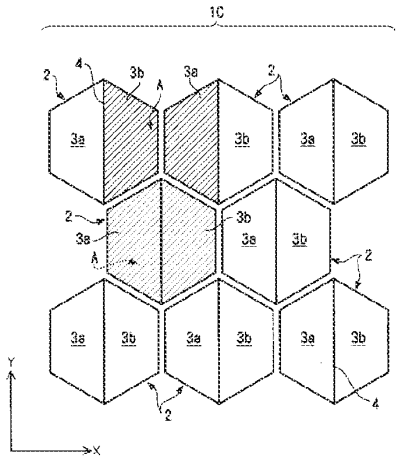
【図１】



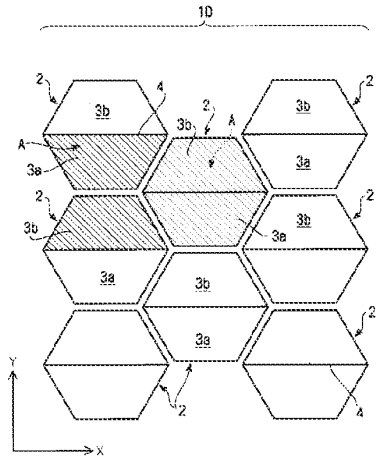
【図２】



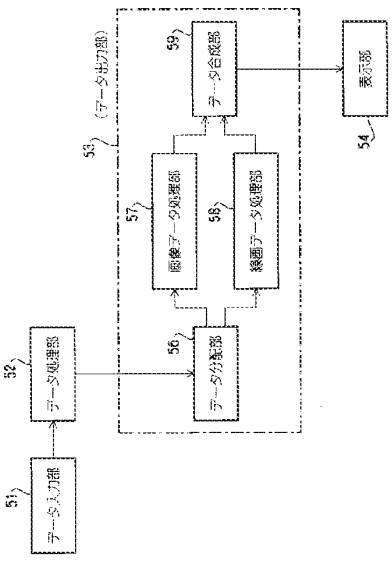
【図３】


1C
2
4
3b
A
3a
Y
X

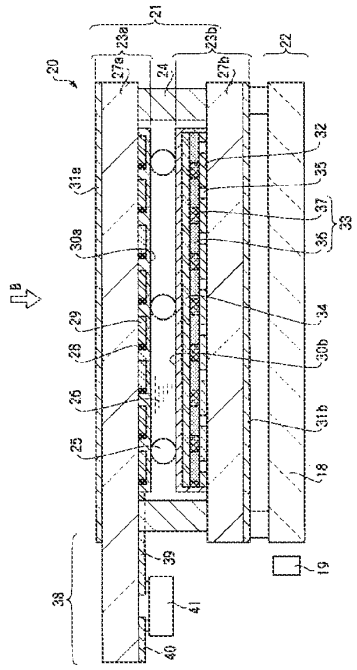
【図４】


1D
2
4
3b
A
3a
Y
X

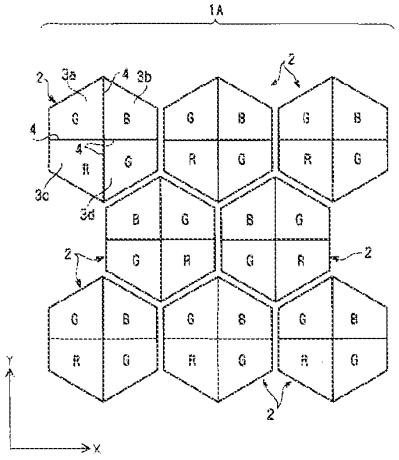
【図５】


データ入力部
51
データ処理部
52
データ出力部
53
データ分配部
56
画像データ処理部
57
線画データ処理部
58
データ合成部
59
表示部
54

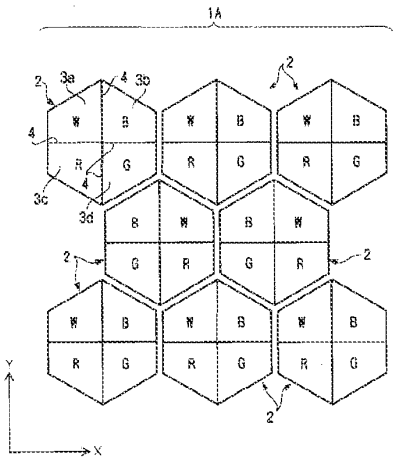
【図６】


21
23a
23b
22
20
27a
24
27b
32
31a
35
30a
37
33
36
B
29
34
28
30b
26
31b
25
18
39
19
38
41
40

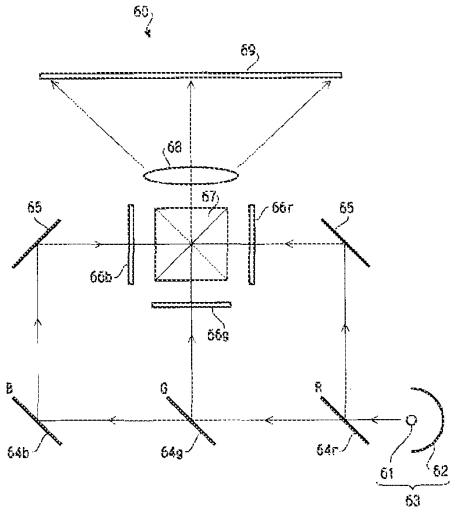
【図７】


1A
2
3a
3b
3c
3d
4
G
B
R
X
Y

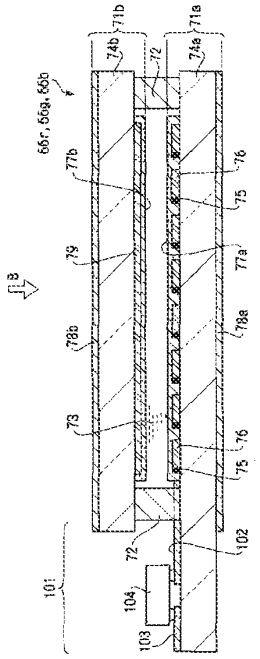
【図８】


1A
2
3a
3b
3c
3d
4
W
G
B
R
X
Y

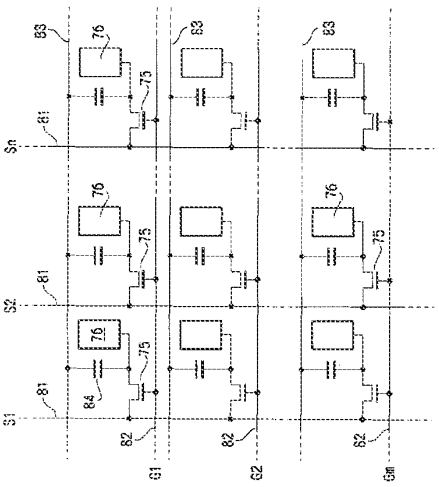
【図９】


60
69
68
67
65
66r
66b
66g
64b
64g
64r
61
62
63
B
G
R

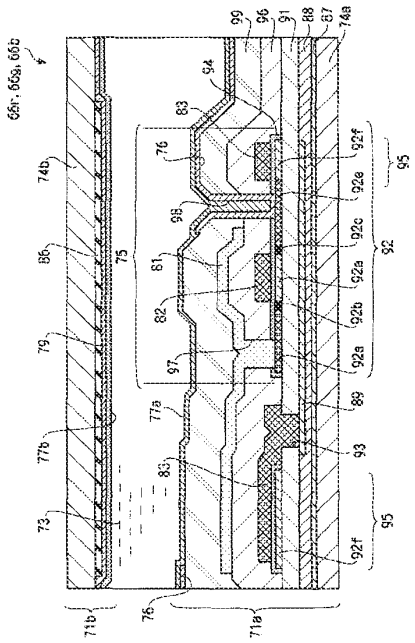
【図１０】


71b
71a
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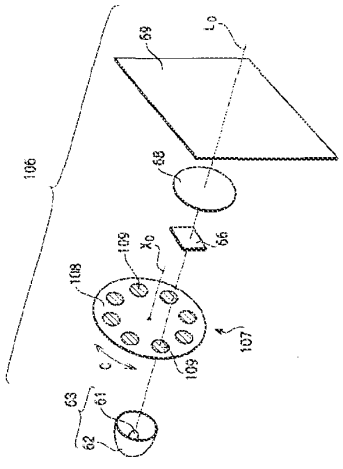
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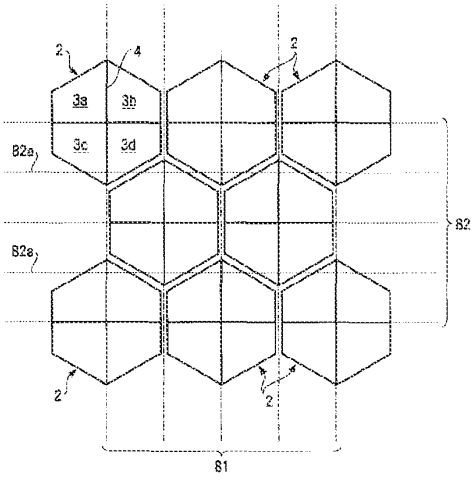
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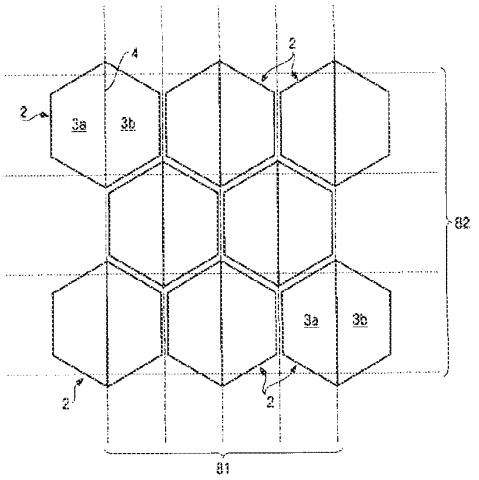
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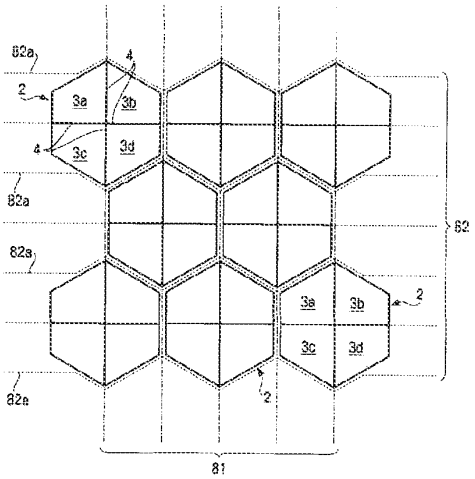
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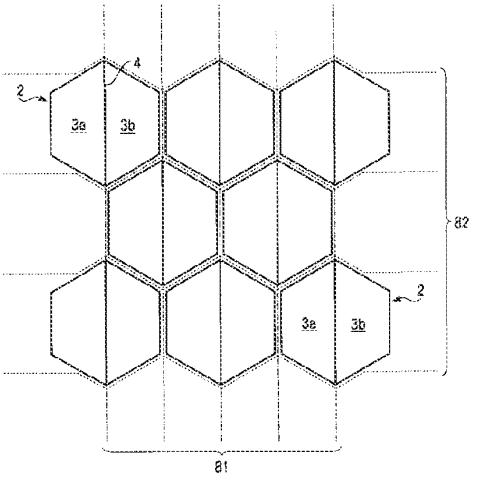
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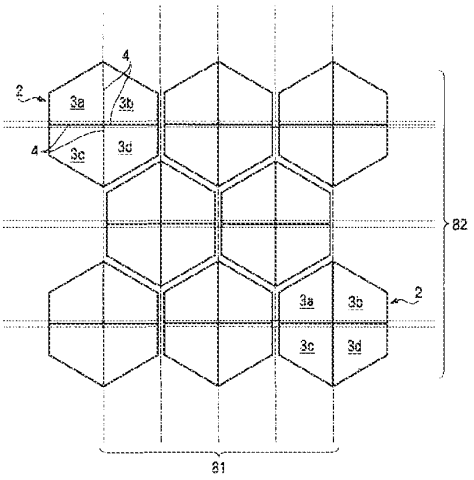
【図１６】



【図１７】



【図１８】



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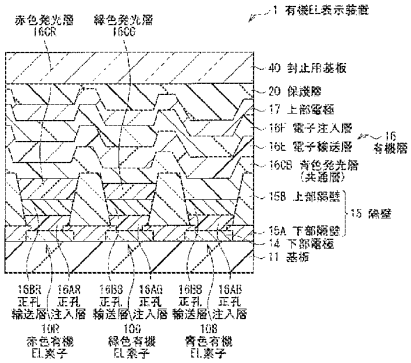
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(54)【発明の名称】有機ＥＬ表示装置およびその製造方法

(57)【要約】
【課題】青の画素に隣接する有機層の膜厚の均一性を向上させることが可能な有機ＥＬ表示装置およびその製造方法を提供する
【解決手段】赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを塗布法、青色発光層１６ＣＢを蒸着法により共通層として形成する。赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの各々を、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接させる。青色有機ＥＬ素子１０Ｂに隣接している辺では、製造工程における塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の片寄りが低減される。よって、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の均一性または対称性が向上する。
【選択図】図３



【特許請求の範囲】
【請求項１】
基板に、青色の第１有機ＥＬ素子およびその他の色の第２有機ＥＬ素子の各々ごとに設けられた下部電極と、
前記下部電極の上に前記第１有機ＥＬ素子および第２有機ＥＬ素子の各々ごとに設けられた正孔注入または正孔輸送の少なくとも一方の特性を有する第１正孔注入・輸送層と、
前記第２有機ＥＬ素子用の第１正孔注入・輸送層上に設けられたその他の色の第２有機発光層と、
前記第２有機発光層および前記第１有機ＥＬ素子用の第１正孔注入・輸送層の全面に設けられた低分子材料よりなる青色の第１有機発光層と、
前記第１有機発光層の全面に順に設けられた電子注入または電子輸送の少なくとも一方の特性を有する電子注入・輸送層および上部電極と
を備え、
前記第１有機ＥＬ素子と前記第２有機ＥＬ素子とを同一の配列で含む複数の画素を有し、前記第２有機ＥＬ素子のうち少なくとも２色は、少なくとも対向する２辺で同一画素内または隣接画素内の前記第１有機ＥＬ素子と隣接している
有機ＥＬ表示装置。
【請求項２】
前記第２有機ＥＬ素子は、赤色有機ＥＬ素子、緑色有機ＥＬ素子、黄色有機ＥＬ素子または白色有機ＥＬ素子のうちの少なくとも１色である
請求項１記載の有機ＥＬ表示装置。
【請求項３】
前記第２有機ＥＬ素子は、前記複数の画素の各々の対角線上の二つの角に配置されている
請求項２記載の有機ＥＬ表示装置。
【請求項４】
前記第１有機ＥＬ素子および前記第２有機ＥＬ素子は細長い矩形であり、
前記第２有機ＥＬ素子は、前記矩形の短辺に平行な方向に等間隔で配列され、前記第１有機ＥＬ素子は、前記第２有機ＥＬ素子の間に配置されている
請求項２記載の有機ＥＬ表示装置。
【請求項５】
前記第２有機ＥＬ素子は、一方向に配列されている
請求項２記載の有機ＥＬ表示装置。
【請求項６】
前記第２有機ＥＬ素子の面積は、前記第１有機ＥＬ素子の面積とは異なる
請求項４または５記載の有機ＥＬ表示装置。
【請求項７】
前記第２有機発光層および前記第１有機ＥＬ素子用の前記第１正孔注入・輸送層の全面と、前記青色の第１有機発光層との間に、低分子材料からなる第２正孔注入・輸送層を備えた
請求項１記載の有機ＥＬ表示装置。
【請求項８】
前記第１有機ＥＬ素子の前記第１正孔注入・輸送層は、高分子材料よりなる正孔注入層のみを有し、前記第２有機ＥＬ素子の第１前記正孔注入・輸送層は高分子材料からなる
請求項７記載の有機ＥＬ表示装置。
【請求項９】
前記第１有機ＥＬ素子の前記第１正孔注入・輸送層は、高分子材料よりなる正孔注入層および前記正孔注入層上の低分子材料よりなる正孔輸送層を有し、前記第２有機ＥＬ素子の前記第１正孔注入・輸送層は高分子材料からなる
請求項１記載の有機ＥＬ表示装置。

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【請求項１０】
前記第２有機ＥＬ素子の第２有機発光層は、それぞれ高分子材料および低分子材料を含み、前記高分子材料と前記低分子材料との混合比は、高分子材料：低分子材料が１０：１以上１：２以下である
請求項７ないし９のいずれか１項に記載の有機ＥＬ表示装置。
【請求項１１】
基板に下部電極を青色の第１有機ＥＬ素子およびその他の色の第２有機ＥＬ素子の各々ごとに形成する工程と、
前記下部電極の上に正孔注入または正孔輸送の少なくとも一方の特性を有する第１正孔注入・輸送層を第１有機ＥＬ素子および第２有機ＥＬ素子の各々ごとに塗布法により形成する工程と、
前記第２有機ＥＬ素子用の前記第１正孔注入・輸送層の上にその他の色の第２有機発光層を塗布法により形成する工程と、
前記第２有機発光層および前記第１有機ＥＬ素子用の第１正孔注入・輸送層の全面に、低分子材料からなる青色の第１有機発光層を蒸着法により形成する工程と、
前記第１発光層の全面に電子注入または電子輸送の少なくとも一方の特性を有する電子注入・輸送層および上部電極を順に形成する工程と
を含み、
前記第１有機ＥＬ素子と前記第２有機ＥＬ素子とを同一の配列で含む複数の画素を設け、前記第２有機ＥＬ素子のうち少なくとも２色を、少なくとも対向する２辺で同一画素内または隣接画素内の前記第１有機ＥＬ素子と隣接させる
有機ＥＬ表示装置の製造方法。
【請求項１２】
前記塗布法として、インクジェット，ノズルプリンティング，凸版印刷，グラビア印刷または反転オフセット印刷を用いる
請求項１１記載の有機ＥＬ表示装置の製造方法。
【請求項１３】
前記第２有機ＥＬ素子は、赤色有機ＥＬ素子、緑色有機ＥＬ素子、黄色有機ＥＬ素子または白色有機ＥＬ素子のうちの少なくとも１色である
請求項１２記載の有機ＥＬ表示装置の製造方法。
【請求項１４】
前記第２有機ＥＬ素子を、前記複数の画素の各々の対角線上の二つの角に配置する
請求項１３記載の有機ＥＬ表示装置の製造方法。
【請求項１５】
前記第１有機ＥＬ素子および前記第２有機ＥＬ素子を細長い矩形とし、
前記第２有機ＥＬ素子を、前記矩形の短辺に平行な方向に等間隔で配列し、前記第１有機ＥＬ素子を、前記第２有機ＥＬ素子の間に配置する
請求項１３記載の有機ＥＬ表示装置の製造方法。
【請求項１６】
前記第２有機ＥＬ素子を、一方向に配列する
請求項１３記載の有機ＥＬ表示装置の製造方法。
【請求項１７】
前記第２有機ＥＬ素子の面積を、前記第１有機ＥＬ素子の面積とは異ならせる
請求項１５または１６記載の有機ＥＬ表示装置の製造方法。
【発明の詳細な説明】
【技術分野】
【０００１】
本発明は、有機エレクトロルミネセンス（ＥＬ；Electro Luminescence）現象を利用して発光する有機ＥＬ表示装置およびその製造方法に関する。
【背景技術】

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【０００２】
情報通信産業の発達が加速するにつれて、高度な性能を有する表示素子が要求されている。その中で、次世代表示素子として注目されている有機ＥＬ素子は自発発光型表示素子として視野角が広くコントラストが優秀なだけでなく応答時間が速いという長所がある。
【０００３】
有機ＥＬ素子を形成する発光層等は、低分子材料と高分子材料に大別される。一般に、低分子材料の方がより高い発光効率、長寿命を示すことが知られており、特に青色の性能は高いとされる。
【０００４】
また、その有機膜の形成方法として、低分子材料は真空蒸着法等の乾式法（蒸着法）、高分子材料は、スピンコーティング、インクジェット、ノズルプリンティング等の湿式法（塗布法または印刷法）により成膜されている。
【０００５】
真空蒸着法は、有機薄膜の形成材料を溶媒に溶解させる必要がなく、成膜後に溶媒を除去する工程が不要という利点がある。しかし、メタルマスクによる塗り分けが難しく、特に大型のパネルの作製における設備製造コストが高いため、大画面基板への適用が難しく、量産にも難があるなどの欠点を有していた。そこで表示画面の大面積化が比較的容易なインクジェットやノズルプリンティングなどの湿式法が注目されている。
【０００６】
しかしながら、インクジェットやノズルプリンティングにおいて用いられる高分子材料の中で、特に青色の発光材料は発光輝度および寿命特性が低いため、湿式法による実用的なディスプレイの製品化が困難であった。
【０００７】
そこで、例えば特許文献１では、赤，緑の発光層をインクジェット方式により画素毎にパターニングし、その上に青色の発光層を真空蒸着法により形成する製造方法が提案されている。
【先行技術文献】
【特許文献】
【０００８】
【特許文献１】特開２００７－７３５３２号公報
【発明の概要】
【発明が解決しようとする課題】
【０００９】
しかしながら、特許文献１のように赤，緑の有機層を印刷法、青の有機層を蒸着法で形成する製造方法では、成膜材料の溶液が赤，緑の画素にのみ塗布され、青の画素には塗布されない工程が含まれる。この場合、塗布液の乾燥速度が青の画素に隣接する部分で速くなり、未乾燥の塗布液が乾燥済みの部分に引き寄せられる。その結果、乾燥後の有機層の膜厚が均一または対称にならず、青の画素に隣接する部分の膜厚が厚くなってしまうという問題が生じていた。
【００１０】
本発明はかかる問題点に鑑みてなされたもので、その目的は、青の画素に隣接する有機層の膜厚の均一性または対称性を向上させることが可能な有機ＥＬ表示装置およびその製造方法を提供することにある。
【課題を解決するための手段】
【００１１】
本発明による有機ＥＬ表示装置は、基板に、青色の第１有機ＥＬ素子およびその他の色の第２有機ＥＬ素子の各々ごとに設けられた下部電極と、下部電極の上に第１有機ＥＬ素子および第２有機ＥＬ素子の各々ごとに設けられた正孔注入または正孔輸送の少なくとも一方の特性を有する第１正孔注入・輸送層と、第２有機ＥＬ素子用の第１正孔注入・輸送層上に設けられたその他の色の第２有機発光層と、第２有機発光層および第１有機ＥＬ素

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子用の第１正孔注入・輸送層の全面に設けられた低分子材料よりなる青色の第１有機発光層と、第１有機発光層の全面に順に設けられた電子注入または電子輸送の少なくとも一方の特性を有する電子注入・輸送層および上部電極とを備え、第１有機ＥＬ素子と第２有機ＥＬ素子とが同一位置関係で配列された複数の画素を有し、第２有機ＥＬ素子の各々は、少なくとも対向する２辺で同一画素内または隣接画素内の第１有機ＥＬ素子と隣接しているものである。

【００１２】

本発明による有機ＥＬ表示装置の製造方法は、基板に下部電極を青色の第１有機ＥＬ素子およびその他の色の第２有機ＥＬ素子の各々ごとに形成する工程と、下部電極の上に正孔注入または正孔輸送の少なくとも一方の特性を有する第１正孔注入・輸送層を第１有機ＥＬ素子および第２有機ＥＬ素子の各々ごとに塗布法により形成する工程と、第２有機ＥＬ素子用の第１正孔注入・輸送層の上にその他の色の第２有機発光層を塗布法により形成する工程と、第２有機発光層および第１有機ＥＬ素子用の第１正孔注入・輸送層の全面に、低分子材料からなる青色の第１有機発光層を蒸着法により形成する工程と、第１発光層の全面に電子注入または電子輸送の少なくとも一方の特性を有する電子注入・輸送層および上部電極を順に形成する工程とを含み、第１有機ＥＬ素子と第２有機ＥＬ素子とを同一位置関係で配列した複数の画素を設け、第２有機ＥＬ素子の各々を、少なくとも対向する２辺で同一画素内または隣接画素内の第１有機ＥＬ素子と隣接させるようにしたものである。

【００１３】

本発明の有機ＥＬ表示装置、または本発明の有機ＥＬ表示装置の製造方法では、第２有機ＥＬ素子の各々が、少なくとも対向する２辺で同一画素内または隣接画素内の第１有機ＥＬ素子と隣接しているので、第１有機ＥＬ素子に隣接している辺では、製造工程における塗布液の乾燥速度の不均一が抑えられ、乾燥後の有機層の膜厚の片寄りが低減されている。よって、第２有機ＥＬ素子の有機層の膜厚の均一性または対称性が向上する。

【発明の効果】

【００１４】

本発明の有機ＥＬ表示装置、または本発明の有機ＥＬ表示装置の製造方法によれば、第２有機ＥＬ素子の各々を、少なくとも対向する２辺で同一画素内または隣接画素内の第１有機ＥＬ素子と隣接させるようにしたので、第２有機ＥＬ素子の有機層の膜厚の均一性または対称性を向上させることが可能となる。

【図面の簡単な説明】

【００１５】

【図１】本発明の第１の実施の形態に係る有機ＥＬ表示装置の構成を表す図である。
【図２】図１に示した画素駆動回路の一例を表す図である。
【図３】図１に示した表示領域の構成を表す断面図である。
【図４】有機ＥＬ素子の平面的な配列の第１例を表す図である。
【図５】有機ＥＬ素子の平面的な配列の第２例を表す図である。
【図６】有機ＥＬ素子の平面的な配列の第３例を表す図である。
【図７】有機ＥＬ素子の平面的な配列の第４例を表す図である。
【図８】有機ＥＬ素子の平面的な配列の第５例を表す図である。
【図９】有機ＥＬ素子の平面的な配列の第６例を表す図である。
【図１０】図１に示した有機ＥＬ表示装置の製造方法の流れを表す図である。
【図１１】図１０に示した製造方法を工程順に表す断面図である。
【図１２】図１１に続く工程を表す断面図である。
【図１３】従来の製造方法の問題点を説明するための図である。
【図１４】図１２に続く工程を表す断面図である。
【図１５】本発明の第２の実施の形態に係る有機ＥＬ表示装置の製造方法の流れを表す図である。
【図１６】図１５に示した製造方法を工程順に表す断面図である。

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【図１７】図１６に続く工程を表す断面図である。
【図１８】図１７に続く工程を表す断面図である。
【図１９】本発明の第４の実施の形態に係る有機ＥＬ表示装置の構成を表す断面図である。
【図２０】図１９に示した有機ＥＬ表示装置の製造方法の流れを表す図である。
【図２１】図２０に示した製造方法を工程順に表す断面図である。
【図２２】図２１に続く工程を表す断面図である。
【図２３】図２２に続く工程を表す断面図である。
【図２４】本発明の第４の実施の形態に係る有機ＥＬ表示装置の構成を表す断面図である。
【図２５】上記実施の形態の表示装置を含むモジュールの概略構成を表す平面図である。
【図２６】上記実施の形態の表示装置の適用例１の外観を表す斜視図である。
【図２７】（Ａ）は適用例２の表側から見た外観を表す斜視図であり、（Ｂ）は裏側から見た外観を表す斜視図である。
【図２８】適用例３の外観を表す斜視図である。
【図２９】適用例４の外観を表す斜視図である。
【図３０】（Ａ）は適用例５の開いた状態の正面図、（Ｂ）はその側面図、（Ｃ）は閉じた状態の正面図、（Ｄ）は左側面図、（Ｅ）は右側面図、（Ｆ）は上面図、（Ｇ）は下面図である。
【図３１】４色の場合の問題点を説明するための図である。
【図３２】４色の場合の有機ＥＬ素子の平面的な配列の第１例を表す図である。
【図３３】４色の場合の有機ＥＬ素子の平面的な配列の第２例を表す図である。
【図３４】４色の場合の有機ＥＬ素子の平面的な配列の第３例を表す図である。
【図３５】４色の場合の有機ＥＬ素子の平面的な配列の第４例を表す図である。
【図３６】４色の場合の有機ＥＬ素子の平面的な配列の第５例を表す図である。
【発明を実施するための形態】
【００１６】
以下、本発明の実施の形態について図面を参照して詳細に説明する。なお、説明は以下の順序で行う。
１．第１の実施の形態（赤色・緑色発光層を塗布法により形成し、青色発光層を共通層として蒸着法により形成した例）
２．第２の実施の形態（青色正孔輸送層を低分子材料により構成した例）
３．第３の実施の形態（赤色・緑色発光層に低分子材料を含む例）
４．第４の実施の形態（赤色・緑色発光層および青色正孔輸送層の上に第２の正孔注入・輸送層を設けた例）
５．第５の実施の形態（青色正孔輸送層を設けず、青色正孔注入層上に第２の正孔注入・輸送層を設けた例）
６．適用例
７．変形例（４色の場合）
【００１７】
（第１の実施の形態）
図１は、本発明の第１の実施の形態に係る有機ＥＬ表示装置の構成を表すものである。この有機ＥＬ表示装置は、有機ＥＬテレビジョン装置などとして用いられるものであり、例えば、基板１１の上に、表示領域１１０として、後述する複数の赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂがマトリクス状に配置されたものである。表示領域１１０の周辺には、映像表示用のドライバである信号線駆動回路１２０および走査線駆動回路１３０が設けられている。
【００１８】
表示領域１１０内には画素駆動回路１４０が設けられている。図２は、画素駆動回路１４０の一例を表したものである。画素駆動回路１４０は、後述する下部電極１４の下層に

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形成されたアクティブ型の駆動回路である。すなわち、この画素駆動回路１４０は、駆動トランジスタＴｒ１および書き込みトランジスタＴｒ２と、これらトランジスタＴｒ１，Ｔｒ２の間のキャパシタ（保持容量）Ｃｓと、第１の電源ライン（Ｖｃｃ）および第２の電源ライン（ＧＮＤ）の間において駆動トランジスタＴｒ１に直列に接続された赤色有機ＥＬ素子１０Ｒ（または緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂ）とを有する。駆動トランジスタＴｒ１および書き込みトランジスタＴｒ２は、一般的な薄膜トランジスタ（ＴＦＴ（Thin Film Transistor））により構成され、その構成は例えば逆スタガ構造（いわゆるボトムゲート型）でもよいしスタガ構造（トップゲート型）でもよく特に限定されない。

【００１９】

画素駆動回路１４０において、列方向には信号線１２０Ａが複数配置され、行方向には走査線１３０Ａが複数配置されている。各信号線１２０Ａと各走査線１３０Ａとの交差点が、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂのいずれか一つ（サブピクセル）に対応している。各信号線１２０Ａは、信号線駆動回路１２０に接続され、この信号線駆動回路１２０から信号線１２０Ａを介して書き込みトランジスタＴｒ２のソース電極に画像信号が供給されるようになっている。各走査線１３０Ａは走査線駆動回路１３０に接続され、この走査線駆動回路１３０から走査線１３０Ａを介して書き込みトランジスタＴｒ２のゲート電極に走査信号が順次供給されるようになっている。

【００２０】

また、表示領域１１０には、赤色の光を発生する赤色有機ＥＬ素子１０Ｒと、緑色の光を発生する緑色有機ＥＬ素子１０Ｇと、青色の光を発生する青色有機ＥＬ素子１０Ｂとが、順に全体としてマトリクス状に配置されている。なお、隣り合う赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの組み合わせが一つの画素（ピクセル）を構成している。ここで、青色有機ＥＬ素子１０Ｂは、本発明における「第１有機ＥＬ素子」の一具体例に対応する。赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子は、本発明における「第２有機ＥＬ素子」の一具体例に対応する。

【００２１】

図３は図１に示した表示領域１１０の断面構成を表したものである。赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂは、それぞれ、基板１１の側から、上述した画素駆動回路１４０の駆動トランジスタＴｒ１および平坦化絶縁膜（図示せず）を間にして、陽極としての下部電極１４、隔壁１５、後述する発光層１６Ｃを含む有機層１６および陰極としての上部電極１７がこの順に積層された構成を有している。

【００２２】

このような赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂは、保護層２０により被覆され、更にこの保護層２０上に熱硬化型樹脂または紫外線硬化型樹脂などの接着層（図示せず）を間にしてガラスなどよりなる封止用基板４０が全面にわたって貼り合わされることにより封止されている。

【００２３】

基板１１は、その一主面側に赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂが配列形成される支持体であって、公知のものであって良く、例えば、石英、ガラス、金属箔、もしくは樹脂製のフィルムやシートなどが用いられる。この中でも石英やガラスが好ましく、樹脂製の場合には、その材質としてポリメチルメタクリレート（ＰＭＭＡ）に代表されるメタクリル樹脂類、ポリエチレンテレフタレート（ＰＥＴ）、ポリエチレンナフタレート（ＰＥＮ）、ポリブチレンナフタレート（ＰＢＮ）などのポリエステル類、もしくはポリカーボネート樹脂などが挙げられるが、透水性や透ガス性を抑える積層構造、表面処理を行うことが必要である。

【００２４】

下部電極１４は、基板１１に、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青

色有機ＥＬ素子１０Ｂの各々ごとに設けられている。下部電極１４は、例えば、積層方向の厚み（以下、単に厚みと言う）が１０ｎｍ以上１０００ｎｍ以下であり、クロム（Ｃｒ），金（Ａｕ），白金（Ｐｔ），ニッケル（Ｎｉ），銅（Ｃｕ），タングステン（Ｗ）あるいは銀（Ａｇ）などの金属元素の単体または合金が挙げられる。また、下部電極１４は、これらの金属元素の単体または合金よりなる金属膜と、インジウムとスズの酸化物（ＩＴＯ）、ＩｎＺｎＯ（インジウム亜鉛オキシド）、酸化亜鉛（ＺｎＯ）とアルミニウム（Ａｌ）との合金などの透明導電膜との積層構造を有していてもよい。なお、下部電極１４が陽極として使われる場合には、下部電極１４は正孔注入性の高い材料により構成されていることが望ましい。ただし、アルミニウム（Ａｌ）合金のように、表面の酸化皮膜の存在や、仕事関数が大きくないことによる正孔注入障壁が問題となる材料においても、適切な正孔注入層を設けることによって下部電極１４として使用することが可能である。

【００２５】

隔壁１５は、下部電極１４と上部電極１７との絶縁性を確保すると共に発光領域を所望の形状にするためのものであると共に、後述する製造工程においてインクジェットまたはノズルプリンティング方式による塗布を行う際の隔壁としての機能も有している。隔壁１５は、例えば、ＳｉＯ２ 等の無機絶縁材料よりなる下部隔壁１５Ａの上に、ポジ型感光性ポリベン ゾオキサゾール，ポジ型感光性ポリイミドなどの感光性樹脂よりなる上部隔壁１５Ｂを有している。隔壁１５には、発光領域に対応して開口が設けられている。なお、有機層１６ないし上部電極１７は、開口だけでなく隔壁１５の上にも設けられていてもよいが、発光が生じるのは隔壁１５の開口だけである。

【００２６】

赤色有機ＥＬ素子１０Ｒの有機層１６は、例えば、下部電極１４の側から順に、正孔注入層１６ＡＲ，正孔輸送層１６ＢＲ，赤色発光層１６ＣＲ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆを積層した構成を有する。緑色有機ＥＬ素子１０Ｇの有機層１６は、例えば、下部電極１４の側から順に、正孔注入層１６ＡＧ，正孔輸送層１６ＢＧ，緑色発光層１６ＣＧ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆを積層した構成を有する。青色有機ＥＬ素子１０Ｂの有機層１６は、例えば、下部電極１４の側から順に、正孔注入層１６ＡＢ，正孔輸送層１６ＢＢ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆを積層した構成を有する。これらのうち青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆは、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの共通層として設けられている。

【００２７】

正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢは、正孔注入効率を高めるためのものであると共に、リークを防止するためのバッファ層であり、下部電極１４の上に赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの各々ごとに設けられている。

【００２８】

正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢの厚みは例えば５ｎｍ～１００ｎｍであることが好ましく、より好ましくは８ｎｍ～５０ｎｍである。正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢの構成材料は、電極や隣接する層の材料との関係で適宜選択すればよく、ポリアニリン及びその誘導体、ポリチオフェン及びその誘導体、ポリピロール及びその誘導体、ポリフェニレンビニレン及びその誘導体、ポリチエニレンビニレン及びその誘導体、ポリキノリン及びその誘導体、ポリキノキサリン及びその誘導体、芳香族アミン構造を主鎖又は側鎖に含む重合体等の導電性高分子、金属フタロシアニン（銅フタロシアニン等）、カーボン等が例示される。

正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢに用いられる材料が、高分子材料である場合、その高分子の重量平均分子量（Ｍｗ）は、２０００～１万程度のオリゴマーや１万～３０万の範囲であることが好ましい。特に、５０００～２０万程度が好ましい。Ｍｗが５０００未満では、正孔輸送層以降を形成する際に、正孔注入層が溶解してしまう恐れがある。また３０万を超えると、材料がゲル化し、成膜が困難になる恐れがある。

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【００２９】
正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢの構成材料として使用される典型的な導電性高分子としては、ポリアニリンおよび／またはオリゴアニリン、及びポリ（３，４－エチレンジオキシチオフェン）（ＰＥＤＯＴ）などのポリジオキシチオフェンが挙げられる。例えば、エイチ・シー・スタルク製 Nafion(商標）で市販されているポリマー、または溶解形態で商品名 Liquion(商標）で市販されているポリマーや、日産化学製エルソース（商標）や、綜研化学製導電性ポリマーベラゾール（商標）などがある。
【００３０】
正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢは、赤色発光層１６ＣＲ，緑色発光層１６ＣＧおよび青色発光層１６ＣＢへの正孔輸送効率を高めるためのものである。正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢは、正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢの上に赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの各々ごとに設けられている。
【００３１】
正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢの厚みは、素子の全体構成にもよるが、例えば１０ｎｍ～２００ｎｍであることが好ましく、さらに好ましくは１５ｎｍ～１５０ｎｍである。正孔輸送層１６ＢＲ，１６ＢＧを構成する高分子材料としては、有機溶媒に可溶な発光材料、例えば、ポリビニルカルバゾール及びその誘導体、ポリフルオレン及びその誘導体、ポリアニリン及びその誘導体、ポリシラン及びその誘導体、側鎖又は主鎖に芳香族アミンを有するポリシロキサン誘導体、ポリチオフェン及びその誘導体、ポリピロール等が使用できる。
【００３２】
高分子材料の重量平均分子量（Ｍｗ）は、５万～３０万であることが好ましく、特に、１０万～２０万であることが好ましい。Ｍｗが５万未満では、発光層を形成するときに、高分子材料中の低分子成分が脱落し、正孔注入・輸送層にドットが生じるため、有機ＥＬ素子の初期性能が低下したり、素子の劣化を引き起こすおそれがある。一方、３０万を越えると、材料がゲル化するため、成膜が困難になるおそれがある。
尚、重量平均分子量（Ｍｗ）は、テトラヒドロフランを溶媒として、ゲルパーエミーションクロマトグラフィー（ＧＰＣ）により、ポリスチレン換算の重量平均分子量を求めた値である。
【００３３】
赤色発光層１６ＣＲ，緑色発光層１６ＣＧは、電界をかけることにより電子と正孔との再結合が起こり、光を発生するものである。赤色発光層１６ＣＲ，緑色発光層１６ＣＧの厚みは、素子の全体構成にもよるが、例えば１０ｎｍ～２００ｎｍであることが好ましく、さらに好ましくは１５ｎｍ～１５０ｎｍである。赤色発光層１６ＣＲ，緑色発光層１６ＣＧを構成する高分子発光材料としては、ポリフルオレン系高分子誘導体や、（ポリ）パラフェニレンビニレン誘導体、ポリフェニレン誘導体、ポリビニルカルバゾール誘導体、ポリチオフェン誘導体、ペリレン系色素、クマリン系色素、ローダミン系色素、あるいは上記高分子に有機ＥＬ材料をドープして用いることができる。例えば、ルブレン、ペリレン、９，１０ジフェニルアントラセン、テトラフェニルブタジエン、ナイルレッド、クマリン６等をドープすることにより用いることができる。
【００３４】
青色発光層１６ＣＢは、電界をかけることにより電子と正孔との再結合が起こり、光を発生するものであり、赤色発光層１６ＣＲ，緑色発光層１６ＣＧおよび青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの全面に共通層として設けられている。青色発光層１６ＣＢは、アントラセン化合物をホスト材料として青色もしくは緑色の低分子蛍光性色素，りん光色素、金属錯体等の有機発光材料よりなるゲスト材料がドーピングされており、青色もしくは緑色の発光光を発生する。
【００３５】
電子輸送層１６Ｅは、赤色発光層１６ＣＲ，緑色発光層１６ＣＧ，青色発光層１６ＣＢ

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への電子輸送効率を高めるためのものであり、青色発光層１６ＣＢの全面に共通層として設けられている。電子輸送層１６Ｅの材料としては、例えば、キノリン、ペリレン、フェナントロリン、ビススチリル、ピラジン、トリアゾール、オキサゾール、フラーレン、オキサジアゾール、フルオレノン、またはこれらの誘導体や金属錯体が挙げられる。具体的には、トリス（８－ヒドロキシキノリン）アルミニウム（略称Ａｌq_3）、アントラセン、ナフタレン、フェナントレン、ピレン、アントラセン、ペリレン、ブタジエン、クマリン、Ｃ６０、アクリジン、スチルベン、１，１０－フェナントロリンまたはこれらの誘導体や金属錯体が挙げられる。

【００３６】

電子注入層１６Ｆは、電子注入効率を高めるためのものであり、電子輸送層１６Ｅの全面に共通層として設けられている。電子注入層１６Ｆの材料としては、例えばリチウム（Ｌｉ）の酸化物である酸化リチウム（Li_2O）や、セシウム（Ｃｓ）の複合酸化物である炭酸セシウム（Cs_2CO_3）、さらにはこれらの酸化物及び複合酸化物の混合物を用いることができる。また、電子注入層１６Ｆは、このような材料に限定されることはなく、例えば、カルシウム（Ｃａ）、バリウム（Ｂａ）等のアルカリ土類金属、リチウム、セシウム等のアルカリ金属、さらにはインジウム（Ｉｎ）、マグネシウム（Ｍｇ）等の仕事関数の小さい金属、さらにはこれらの金属の酸化物及び複合酸化物、フッ化物等を、単体でまたはこれらの金属および酸化物及び複合酸化物、フッ化の混合物や合金として安定性を高めて使用しても良い。

【００３７】

上部電極１７は、例えば、厚みが３ｎｍ以上８ｎｍ以下であり、金属導電膜により構成されている。具体的には、アルミニウム（Ａｌ），マグネシウム（Ｍｇ），カルシウム（Ｃａ）またはナトリウム（Ｎａ）の合金が挙げられる。中でも、マグネシウムと銀との合金（Ｍｇ－Ａｇ合金）は、薄膜での導電性と吸収の小ささとを兼ね備えているので好ましい。Ｍｇ－Ａｇ合金におけるマグネシウムと銀との比率は特に限定されないが、膜厚比でＭｇ：Ａｇ＝２０：１～１：１の範囲であることが望ましい。また、上部電極１７の材料は、アルミニウム（Ａｌ）とリチウム（Ｌｉ）との合金（Ａｌ－Ｌｉ合金）でもよい。

【００３８】

更に、上部電極１７は、アルミキノリン錯体、スチリルアミン誘導体、フタロシアニン誘導体等の有機発光材料を含有した混合層でもよい。この場合には、さらに第３層としてＭｇＡｇのような光透過性を有する層を別途有していてもよい。なお、上部電極１７は、アクティブマトリックス駆動方式の場合、有機層１６と隔壁１５とによって、下部電極１４と絶縁された状態で基板１１上にベタ膜状に形成され、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの共通電極として用いられる。

【００３９】

保護層２０は、例えば厚みが２～３μｍであり、絶縁性材料または導電性材料のいずれにより構成されていてもよい。絶縁性材料としては、無機アモルファス性の絶縁性材料、例えばアモルファスシリコン（α－Ｓｉ），アモルファス炭化シリコン（α－ＳｉＣ），アモルファス窒化シリコン（$\alpha-Si_{1-x}N_x$）、アモルファスカーボン（α－Ｃ）などが好ましい。このような無機アモルファス性の絶縁性材料は、グレインを構成しないため透水性が低く、良好な保護膜となる。

【００４０】

封止用基板４０は、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの上部電極１７の側に位置しており、接着層（図示せず）と共に赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂを封止するものである。封止用基板４０は、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂで発生した光に対して透明なガラスなどの材料により構成されている。封止用基板４０には、例えば、カラーフィルタおよびブラックマトリクスとしての遮光膜（いずれも図示せず）が設けられており、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂで発生した光を取り出すと共に、赤色有機ＥＬ素子１０Ｒ，緑色有

機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂ並びにその間の配線において反射された外光を吸収し、コントラストを改善するようになっている。

【００４１】

カラーフィルタは、赤色フィルタ，緑色フィルタおよび青色フィルタ（いずれも図示せず）を有しており、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂに対応して順に配置されている。赤色フィルタ，緑色フィルタおよび青色フィルタは、それぞれ例えば矩形形状で隙間なく形成されている。これら赤色フィルタ，緑色フィルタおよび青色フィルタは、顔料を混入した樹脂によりそれぞれ構成されており、顔料を選択することにより、目的とする赤，緑あるいは青の波長域における光透過率が高く、他の波長域における光透過率が低くなるように調整されている。

【００４２】

遮光膜は、例えば黒色の着色剤を混入した光学濃度が１以上の黒色の樹脂膜、または薄膜の干渉を利用した薄膜フィルタにより構成されている。このうち黒色の樹脂膜により構成するようにすれば、安価で容易に形成することができるので好ましい。薄膜フィルタは、例えば、金属，金属窒化物あるいは金属酸化物よりなる薄膜を１層以上積層し、薄膜の干渉を利用して光を減衰させるものである。薄膜フィルタとしては、具体的には、クロムと酸化クロム（ＩＩＩ）（Cr_2O_3）とを交互に積層したものが挙げられる。

【００４３】

図４ないし図９は、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの配列の第１例ないし第６例をそれぞれ表したものである。有機ＥＬ表示装置１は、行列状（マトリクス状）に配置された複数の画素１０を有している。各画素１０は、例えば正方形の平面形状を有し、少なくとも一つの青色有機ＥＬ素子１０Ｂを含むと共に、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇを一つずつ含んでいる。

【００４４】

赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび青色有機ＥＬ素子１０Ｂは、すべての画素１０に同一の配列で含まれている。赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの各々は、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。これにより、この有機ＥＬ表示装置１では、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの有機層１６の膜厚の均一性または対称性を向上させることが可能となっている。

【００４５】

例えば図４に示した第１例および図５に示した第２例では、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂは細長い矩形（短冊状）の平面形状を有している。赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇは、矩形の短辺に平行な方向に等間隔で配列されている。青色有機ＥＬ素子１０Ｂは、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの間に配置されている。この場合、赤色有機ＥＬ素子１０および緑色有機ＥＬ素子１０Ｇの各々は、二本の長辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。

【００４６】

図６に示した第３例では、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇは、各画素１０の対角線上の二つの角に配置（いわゆる千鳥配置）されている。すなわち、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇは、矩形（例えば正方形）の平面形状を有し、対角線を同一線上にして斜めに（例えば図６では赤色有機ＥＬ素子１０Ｒが画素１０の左上、緑色有機ＥＬ素子１０Ｇが画素１０の右下）に配列されている。青色有機ＥＬ素子１０Ｂは、矩形（例えば正方形）の平面形状を有し、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇ以外の領域に（画素１０の右上および左下）配置されている。この場合、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの各々は、四辺のすべてで同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。

【００４７】

図７に示した第４例、図８に示した第５例および図９に示した第６例では、赤色有機Ｅ

Ｌ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇは、一方向に（直線状に）配列されている。すなわち、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇは、矩形（例えば正方形）の平面形状を有し、横並びに（赤色有機ＥＬ素子１０Ｒが画素１０の左上、緑色有機ＥＬ素子１０Ｇが画素１０の右上）配列されている。青色有機ＥＬ素子１０Ｂは、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇ以外の領域に（画素１０の左下および右下）配置されている。この場合、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの各々は、上下の二辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。

【００４８】

青色有機ＥＬ素子１０Ｂは、図７に示した第４例のように、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇと同じ形状（例えば正方形）の平面形状を有していてもよいし、図８に示した第５例または図９に示した第６例のように、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇをつなげた細長い矩形でもよい。

【００４９】

第１例ないし第６例のいずれも、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの面積は同一であることが望ましい。面積および印刷するインク量を同一にすることで乾燥時間を同等にすることができ、これにより赤と緑の膜厚分布をより均一化することができるからである。

【００５０】

一方、青色有機ＥＬ素子１０Ｂの面積は、必ずしも赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの面積と同一である必要はない。例えば、青色有機ＥＬ素子１０Ｂは、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇに比べて発光寿命が短いので、青色有機ＥＬ素子１０Ｂの面積を赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの面積よりも広い面積となるよう設計する場合がある。従って、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの面積は、青色有機ＥＬ素子１０Ｂの面積とは異なっていてもよい。図６に示した第３例以外は、青色有機ＥＬ素子１０Ｂの面積を任意に設計することが可能である。

【００５１】

例えば、図４に示した第１例では、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの短辺の長さが等しいのに対して、図５に示した第２例では、各青色有機ＥＬ素子１０Ｂの短辺の長さが赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの短辺よりも短く、各青色有機ＥＬ素子１０Ｂの面積が赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの面積よりも小さくなっている。これにより、各画素１０内での赤色有機ＥＬ素子１０Ｒの面積と、緑色有機ＥＬ素子１０Ｇの面積と、二つの青色有機ＥＬ素子１０Ｂの合計面積とがほぼ等しくされている。

【００５２】

また、例えば図８に示した第５例では、青色有機ＥＬ素子１０Ｂの短辺の長さが赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの一辺の長さに等しいのに対して、図９に示した第６例では、青色有機ＥＬ素子１０Ｂの短辺の長さが赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの一辺の長さよりも短くされている。これにより、第２例と同様に、各画素１０内での赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの面積がほぼ等しくされている。

【００５３】

なお、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの配列は、第１例ないし第６例以外にも可能であることは言うまでもない。

【００５４】

この有機ＥＬ表示装置は、例えば次のようにして製造することができる。

【００５５】

図１０は、この有機ＥＬ表示装置の製造方法の流れを表したものであり、図１１，図１２および図１４は図１０に示した製造方法を工程順に表したものである。まず、上述した

材料よりなる基板１１の上に駆動トランジスタＴｒ１を含む画素駆動回路１４０を形成し、例えば感光性樹脂よりなる平坦化絶縁膜（図示せず）を設ける。

【００５６】

（下部電極１４を形成する工程）

次いで、基板１１の全面に例えばＩＴＯよりなる透明導電膜を形成し、この透明導電膜をパターニングすることにより、図１１（Ａ）に示したように、下部電極１４を赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの各々ごとに形成する（ステップＳ１０１）。その際、下部電極１４を、平坦化絶縁膜（図示せず）のコンタクトホール（図示せず）を介して駆動トランジスタＴｒ１のドレイン電極と導通させる。

【００５７】

（隔壁１５を形成する工程）

続いて、同じく図１１（Ａ）に示したように、下部電極１４上および平坦化絶縁膜（図示せず）上に、例えばＣＶＤ（Chemical Vapor Deposition ；化学気相成長）法により、ＳｉＯ２ 等の無機絶縁材料を成膜し、フォトリソグラフィー技術およびエッチング技術を用いてパターニングすることにより、下部隔壁１５Ａを形成する。

【００５８】

そののち、同じく図１１（Ａ）に示したように、下部隔壁１５Ａの所定位置、詳しくは画素の発光領域を囲む位置に、上述した感光性樹脂よりなる上部隔壁１５Ｂを形成する。これにより、上部隔壁１５Ａおよび下部隔壁１５Ｂよりなる隔壁１５が形成される（ステップＳ１０２）。

【００５９】

隔壁１５を形成したのち、基板１１の下部電極１４および隔壁１５を形成した側の表面を酸素プラズマ処理し、その表面に付着した有機物等の汚染物を除去して濡れ性を向上させる。具体的には、基板１１を所定温度、例えば７０～８０℃程度に加熱し、続いて大気圧下で酸素を反応ガスとするプラズマ処理（O_2 プラズマ処理）を行う。

【００６０】

（撥水化処理を行う工程）

プラズマ処理を行ったのち、撥水化処理（撥液化処理）を行う（ステップＳ１０３）ことにより、特に上部隔壁１５Ｂの上面及び側面の濡れ性を低下させる。具体的には、大気圧下で４フッ化メタンを反応ガスとするプラズマ処理（CF_4 プラズマ処理）を行い、その後、プラズマ処理のために加熱された基板１１を室温まで冷却することで、上部隔壁１５Ｂの上面及び側面を撥液化し、その濡れ性を低下させる。

【００６１】

なお、このCF_4 プラズマ処理においては、下部電極１４の露出面および下部隔壁１５Ａについても多少の影響を受けるが、下部電極１４の材料であるＩＴＯおよび下部隔壁１５Ａの構成材料であるＳｉＯ２ などはフッ素に対する親和性に乏しいため、酸素プラズマ処理で濡れ性が向上した面は濡れ性がそのままに保持される。

【００６２】

（正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成する工程）

撥水化処理を行ったのち、図１１（Ｂ）に示したように、上部隔壁１５Ｂに囲まれた領域内に、上述した材料よりなる正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成する（ステップＳ１０４）。この正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢは、インクジェット，ノズルプリンティング，凸版印刷，グラビア印刷または反転オフセット印刷などの塗布法により形成する。特に、上部隔壁１５Ｂに囲まれた領域に正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢの形成材料を選択的に配する必要上、液滴吐出法であるインクジェット法や、ノズルプリンティング法を用いることが好ましい。

【００６３】

具体的には、例えばインクジェット法により、正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢの形成材料であるポリアニリンやポリチオフェン等の溶液または分散液を下部電極１４の露出面上に配する。その後、熱処理（乾燥処理）を行うことにより、正孔注入層１６Ａ

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Ｒ，１６ＡＧ，１６ＡＢを形成する。

【００６４】

熱処理においては、溶媒または分散媒を乾燥後、高温で加熱する。ポリアニリンやポリチオフェン等の導電性高分子を用いる場合、大気雰囲気、もしくは酸素雰囲気が好ましい。酸素による導電性高分子の酸化により、導電性が発現しやすくなるためである。

【００６５】

加熱温度は、１５０℃～３００℃が好ましく、さらに好ましくは１８０℃～２５０℃である。時間は、温度、雰囲気にもよるが、５分～３００分程度が好ましく、さらに好ましくは、１０分～２４０分である。この乾燥後の膜厚みは、５ｎｍ～１００ｎｍが好ましい。さらに好ましくは、８ｎｍ～５０ｎｍが好ましい。

【００６６】

（正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢを形成する工程）

正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成したのち、図１１（Ｃ）に示したように、正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢの上に、上述した高分子材料よりなる正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢを赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの各々ごとに形成する（ステップＳ１０５）。この正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢは、インクジェット，ノズルプリンティング，凸版印刷，グラビア印刷または反転オフセット印刷などの塗布法により形成する。特に、上部隔壁１５Ｂに囲まれた領域に正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢの形成材料を選択的に配する必要上、液滴吐出法であるインクジェット法や、ノズルプリンティング法を用いることが好ましい。

【００６７】

具体的には、例えばインクジェット法により、正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢの形成材料である高分子ポリマーの溶液または分散液を正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢの露出面上に配する。その後、熱処理（乾燥処理）を行うことにより、正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢを形成する。

【００６８】

熱処理においては、溶媒または分散媒を乾燥後、高温で加熱する。塗布する雰囲気や溶媒を乾燥、加熱する雰囲気としては、窒素（N_2）を主成分とする雰囲気中が好ましい。酸素や水分があると、作成された有機ＥＬ表示装置の発光効率や寿命が低下する恐れがある。特に、加熱工程においては、酸素や水分の影響が大きいため、注意が必要である。好ましい酸素濃度は、０．１ｐｐｍ以上１００ｐｐｍ以下が好ましく、５０ｐｐｍ以下であればより好ましい。１００ｐｐｍより多い酸素があると、形成した薄膜の界面が汚染され、得られた有機ＥＬ表示装置の発行効率や寿命が低下する恐れがある。また、０．１ｐｐｍ未満の酸素濃度の場合、素子の特性は問題ないが、現状の量産のプロセスとして、雰囲気を０．１ｐｐｍ未満に保持するための装置コストが多大になる可能性がある。

また、水分については、露点が例えば－８０℃以上－４０℃以下であることが好ましい。更に、－５０℃以下であればより好ましく、－６０℃以下であれば更に好ましい。－４０℃より高い水分があると、形成した薄膜の界面が汚染され、得られた有機ＥＬ表示装置の発光効率や寿命が低下する恐れがある。また、－８０℃未満の水分の場合、素子の特性は問題ないが、現状の量産のプロセスとして、雰囲気を－８０℃未満に保持するための装置コストが多大になる可能性がある。

【００６９】

加熱温度は、１００℃～２３０℃が好ましく、さらに好ましくは１００℃～２００℃である。少なくとも、正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢ形成時の温度よりも低いことが好ましい。時間は、温度、雰囲気にもよるが、５分～３００分程度が好ましく、さらに好ましくは、１０分～２４０分である。乾燥後の膜厚みは、素子の全体構成にもよるが、１０ｎｍ～２００ｎｍが好ましい。さらに、１５ｎｍ～１５０ｎｍであればより好ましい。

【００７０】

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（赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを形成する工程）

正孔輸送層１６ＢＲ，１６ＢＧ，１６ＢＢを形成したのち、図１２（Ａ）に示したように、赤色有機ＥＬ素子の正孔輸送層１６ＢＲの上に上述した高分子材料よりなる赤色発光層１６ＣＲを形成する。また、緑色有機ＥＬ素子の正孔輸送層１６ＢＧの上に上述した高分子材料よりなる緑色発光層１６ＣＧを形成する（ステップＳ１０６）。赤色発光層１６ＣＲおよび緑色発光層１６ＣＧは、インクジェット，ノズルプリンティング，凸版印刷，グラビア印刷または反転オフセット印刷などの塗布法により形成する。特に、上部隔壁１５Ｂに囲まれた領域に赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの形成材料を選択的に配する必要上、液滴吐出法であるインクジェット法や、ノズルプリンティング法を用いることが好ましい。

【００７１】

具体的には、例えばインクジェット法により、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの形成材料である高分子ポリマーの溶液または分散液を正孔輸送層１６ＢＲ，１６ＢＧの露出面上に配する。その後、熱処理（乾燥処理）を行うことにより、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを形成する。

【００７２】

熱処理においては、溶媒または分散媒を乾燥後、高温で加熱する。塗布する雰囲気や溶媒を乾燥、加熱する雰囲気としては、窒素（N_2）を主成分とする雰囲気中が好ましい。酸素や水分があると、作成された有機ＥＬ表示装置の発光効率や寿命が低下する恐れがある。特に、加熱工程においては、酸素や水分の影響が大きいため、注意が必要である。好ましい酸素濃度は、０．１ｐｐｍ以上１００ｐｐｍ以下が好ましく、５０ｐｐｍ以下であればより好ましい。１００ｐｐｍより多い酸素があると、形成した薄膜の界面が汚染され、得られた有機ＥＬ表示装置の発光効率や寿命が低下する恐れがある。また、０．１ｐｐｍ未満の酸素濃度の場合、素子の特性は問題ないが、現状の量産のプロセスとして、雰囲気を０．１ｐｐｍ未満に保持するための装置コストが多大になる可能性がある。

また、水分については、露点が例えば－８０℃以上－４０℃以下であることが好ましい。更に、－５０℃以下であればより好ましく、－６０℃以下であれば更に好ましい。－４０℃より高い水分があると、形成した薄膜の界面が汚染され、得られた有機ＥＬ表示装置の発光効率や寿命が低下する恐れがある。また、－８０℃未満の水分の場合、素子の特性は問題ないが、現状の量産のプロセスとして、雰囲気を－８０℃未満に保持するための装置コストが多大になる可能性がある。

【００７３】

加熱温度は、１００℃～２３０℃が好ましく、さらに好ましくは１００℃～２００℃である。少なくとも、正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢ形成時の温度よりも低いことが好ましい。時間は、温度、雰囲気にもよるが、５分～３００分程度が好ましく、さらに好ましくは、１０分～２４０分である。乾燥後の膜厚みは、素子の全体構成にもよるが、１０ｎｍ～２００ｎｍが好ましい。さらに、１５ｎｍ～１５０ｎｍであればより好ましい。

【００７４】

ここでは、赤色有機ＥＬ素子１０および緑色有機ＥＬ素子１０Ｇの各々が、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接しているので、青色有機ＥＬ素子１０Ｂに隣接している辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の片寄りが低減されている。よって、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の均一性または対称性が向上する。

【００７５】

例えば図４に示した第１例および図５に示した第２例では、短冊状の赤色有機ＥＬ素子１０Ｒおよび短冊状の緑色有機ＥＬ素子１０Ｇの間に短冊状の青色有機ＥＬ素子１０Ｂが配置されている。赤色有機ＥＬ素子１０および緑色有機ＥＬ素子１０Ｇの各々は、二本の長辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。

この場合、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの長辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の片寄りが低減される。よって、図４または図５において左右方向（短辺に平行な方向）での膜厚分布の均一性または対称性が良くなる。

【００７６】

図６に示した第３例では、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇは、千鳥配置されている。赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの各々は、四辺のすべてで同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。この場合、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの四辺のすべてで、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の片寄りが低減される。よって、図６において左右方向だけでなく上下方向でも膜厚分布の均一性または対称性が良くなり、最も高い効果が得られる。

【００７７】

図７に示した第４例、図８に示した第５例および図９に示した第６例では、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇは、一方向に配列されている。赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの各々は、上下の二辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。この場合、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの上下の二辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の片寄りが低減される。よって、図７または図８において上下方向での膜厚分布の均一性または対称性が良くなる。

【００７８】

これに対して従来では、図１３（Ａ）に示したように、赤色有機ＥＬ素子８１０Ｒ，緑色有機ＥＬ素子８１０Ｇ，青色有機ＥＬ素子８１０Ｂが順に配列されていた。そのため、赤色発光層８１６ＣＲおよび緑色発光層８１６ＣＧの青色有機ＥＬ素子８１０Ｂと隣接している辺では、塗布液の乾燥速度が速くなり、いわゆるコーヒーステイン現象により未乾燥のインクが乾燥済のインクに引き寄せられ、結果として、図１３（Ｂ）に示したように、青色有機ＥＬ素子８１０Ｂと隣接している辺の膜厚が厚くなり、膜厚分布の均一性または対称性が悪くなっていた。ここにいうコーヒーステイン現象とは、基板に広がった液膜の外縁部つまり周縁部の蒸発量が他の部分よりも多いため、それを補うように液が周縁部に向かって流れ、その結果、乾燥後、周縁部が盛り上がった膜が形成される現象である。なお、図１３では、図１２と同一の構成要素には８００番台の符号を付して表している。

【００７９】

これを回避するため、青色有機ＥＬ素子８１０Ｂ上に溶剤のみ塗布し、乾燥速度を均等化することも考えられるが、塗布装置のヘッド数を増やす必要があるのでコスト増加の原因となる。

【００８０】

また、青色有機ＥＬ素子８１０Ｂは、材料の問題から、赤色有機ＥＬ素子８１０Ｒ，緑色有機ＥＬ素子８１０Ｇに比べて発光寿命が短いので、青色有機ＥＬ素子１０Ｂの面積を赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの面積よりも広い面積として長寿命化を図る場合がある。しかし、その場合には、より乾燥ムラが発生しやすくなり、図１３（Ｂ）を参照して説明したコーヒーステイン現象による膜厚の不均一の問題が更に顕著なものとなっていた。

【００８１】

（青色発光層１６ＣＢを形成する工程）

青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢおよび赤色発光層１６ＣＲ，緑色発光層１６ＣＧまで形成したのち、図１２（Ｂ）に示したように、蒸着法により、赤色発光層１６ＣＲ，緑色発光層１６ＣＧおよび青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの全面に、上述した低分子材料よりなる青色発光層１６ＣＢを共通層として形成する（ステップＳ１０９）。

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【００８２】
（電子輸送層１６Ｄ，電子注入層１６Ｅおよび上部電極１７を形成する工程）
青色発光層１６ＣＢを形成したのち、図１４（Ａ），図１４（Ｂ）および図１４（Ｃ）に示したように、この青色発光層１６ＣＢの全面に、蒸着法により、上述した材料よりなる電子輸送層１６Ｅ，電子注入層１６Ｆおよび上部電極１７を形成する（ステップＳ１１０，Ｓ１１１，Ｓ１１２）。
【００８３】
上部電極１７を形成したのち、図３に示したように、下地に対して影響を及ぼすことのない程度に、成膜粒子のエネルギーが小さい成膜方法、例えば蒸着法やＣＶＤ法により、保護層２０を形成する。例えば、アモルファス窒化シリコンからなる保護層２０を形成する場合には、ＣＶＤ法によって２～３μｍの膜厚に形成する。この際、有機層１６の劣化による輝度の低下を防止するため、成膜温度を常温に設定すると共に、保護層２０の剥がれを防止するために膜のストレスが最小になる条件で成膜することが望ましい。
【００８４】
青色発光層１６ＣＢ，電子輸送層１６Ｅ，電子注入層１６Ｆ，上部電極１７および保護層２０は、マスクを用いることなく全面にベタ膜として形成される。また、青色発光層１６ＣＢ，電子輸送層１６Ｅ，電子注入層１６Ｆ，上部電極１７および保護層２０の形成は、望ましくは、大気に暴露されることなく同一の成膜装置内において連続して行われる。これにより大気中の水分による有機層１６の劣化が防止される。
【００８５】
なお、下部電極１４と同一工程で補助電極（図示せず）を形成した場合、補助電極の上部にベタ膜で形成された有機層１６を、上部電極１７を形成する前にレーザアブレーションなどの手法によって除去してもよい。これにより、上部電極１７を補助電極に直接接続させることが可能となり、コンタクトが向上する。
【００８６】
保護層２０を形成したのち、例えば、上述した材料よりなる封止用基板４０に、上述した材料よりなる遮光膜を形成する。続いて、封止用基板４０に赤色フィルタ（図示せず）の材料をスピンコートなどにより塗布し、フォトリソグラフィ技術によりパターニングして焼成することにより赤色フィルタを形成する。続いて、赤色フィルタ（図示せず）と同様にして、青色フィルタ（図示せず）および緑色フィルタ（図示せず）を順次形成する。
【００８７】
そののち、保護層２０の上に、接着層（図示せず）を形成し、この接着層を間にして封止用基板４０を貼り合わせる。以上により、図１ないし図３に示した表示装置が完成する。
【００８８】
この有機ＥＬ表示装置では、各画素に対して走査線駆動回路１３０から書き込みトランジスタＴｒ２のゲート電極を介して走査信号が供給されると共に、信号線駆動回路１２０から画像信号が書き込みトランジスタＴｒ２を介して保持容量Ｃｓに保持される。すなわち、この保持容量Ｃｓに保持された信号に応じて駆動トランジスタＴｒ１がオンオフ制御され、これにより、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂに駆動電流Ｉｄが注入され、正孔と電子とが再結合して発光が起こる。この光は、下面発光（ボトムエミッション）の場合には下部電極１４および基板１１を透過して、上面発光（トップエミッション）の場合には上部電極１７，カラーフィルタ（図示せず）および封止用基板４０を透過して取り出される。
【００８９】
その際、赤色有機ＥＬ素子１０Ｒでは、赤色発光層１６ＣＲと青色発光層１６ＣＢとが設けられているが、最もエネルギー準位の低い赤色にエネルギー移動が起こり、赤色発光が支配的となる。緑色有機ＥＬ素子１０Ｇでは、緑色発光層１６ＣＧと青色発光層１６ＣＢとが設けられているが、よりエネルギー準位の低い緑色にエネルギー移動が起こり、緑色発光が支配的となる。青色有機ＥＬ素子１０Ｂでは、青色発光層１６ＣＢのみを有する

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ので、青色発光が生じる。ここでは、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの各々が、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接しているので、青色有機ＥＬ素子１０Ｂに隣接している辺では、製造工程における塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の片寄りが低減されている。よって、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の均一性または対称性が向上し、実効的な発光面積を広くとることが可能となり、発光寿命が改善される。

【００９０】

このように本実施の形態では、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの各々を、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接させるようにしたので、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の均一性または対称性を向上させることが可能となる。よって、実効的な発光面積を広くとることが可能となり、発光寿命の改善が可能となる。

【００９１】

また、青色有機ＥＬ素子１０Ｂの面積を赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの面積よりも広くした場合にも、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の不均一が抑えられる。よって、青色有機ＥＬ素子１０Ｂの面積を広くして、赤色有機ＥＬ素子１０および緑色有機ＥＬ素子１０Ｇとの発光寿命のバランスをとることが可能となる。

【００９２】

（第２ないし第５の実施の形態）

以下、第２ないし第５の実施の形態について説明する。これらの実施の形態はいずれも、上記第１の実施の形態において図４ないし図９を参照して説明した画素配列の効果を特に高めることが可能な素子構造に関するものである。また、以下の実施の形態において、第１の実施の形態と同一の構成要素については同一符号を付してその説明は省略する。

【００９３】

（第２の実施の形態）

第２の実施の形態は、青色有機ＥＬ素子１０Ｂの正孔輸送層１６ＢＢに低分子材料を含ませることにより、青色の発光効率および寿命を向上させるようにしたことを除いては、上記第１の実施の形態と同様の構成を有している。ここで、低分子材料とは、低分子化合物が同じ反応又は類似の反応を連鎖的に繰り返すことにより、生じた高分子量の重合体又は縮合体の分子からなる物質以外のものであって、分子量が実質的に単一である化合物を指す。また加熱により、実質的に分子間の新たな化学結合は生まれず、単分子で存在する。

【００９４】

正孔輸送層１６ＢＢの具体的な材料としては、例えば、ベンジン、スチリルアミン、トリフェニルアミン、ポルフィリン、トリフェニレン、アザトリフェニレン、テトラシアノキノジメタン、トリアゾール、イミダゾール、オキサジアゾール、ポリアリールアルカン、フェニレンジアミン、アリールアミン、オキザゾール、アントラセン、フルオレノン、ヒドラゾン、スチルベンあるいはこれらの誘導体、または、ポリシラン系化合物、ビニルカルバゾール系化合物、チオフェン系化合物あるいはアニリン系化合物等の複素環式共役系のモノマー、オリゴマーあるいはポリマーを用いることができる。

【００９５】

さらに具体的な材料としては、α－ナフチルフェニルフェニレンジアミン、ポルフィリン、金属テトラフェニルポルフィリン、金属ナフタロシアニン、ヘキサシアノアザトリフェニレン、７，７，８，８－テトラシアノキノジメタン（ＴＣＮＱ）、７，７，８，８－－テトラシアノ－２，３，５，６－テトラフルオロキノジメタン（Ｆ４－ＴＣＮＱ）、テトラシアノ４、４、４－トリス（３－メチルフェニルフェニルアミノ）トリフェニルアミン、Ｎ、Ｎ、Ｎ’、Ｎ’－テトラキス（ｐ－トリル）ｐ－フェニレンジアミン、Ｎ、Ｎ、

Ｎ’、Ｎ’－テトラフェニル－４、４’－ジアミノビフェニル、Ｎ－フェニルカルバゾール、４－ジ－ｐ－トリルアミノスチルベン、ポリ（パラフェニレンビニレン）、ポリ（チオフェンビニレン）、ポリ（２、２’－チエニルピロール）等が挙げられるが、これらに限定されるものではない。

【００９６】

この表示装置は、例えば、次のようにして製造することができる。

【００９７】

図１５は、本実施の形態の有機ＥＬ表示装置の製造方法の流れを表したものであり、図１６ないし図１８は、図１５に示した製造方法を工程順に表したものである。

【００９８】

（下部電極１４を形成する工程）

まず、第１の実施の形態と同様にして、図１６（Ａ）に示したように、画素駆動回路１４０および平坦化絶縁膜を形成した基板１１の上に下部電極１４を形成する（ステップＳ２０１）。

【００９９】

（隔壁１５を形成する工程）

次いで、第１の実施の形態と同様にして、同じく図１６（Ａ）に示したように、下部隔壁１５Ａおよび上部隔壁１５Ｂよりなる隔壁１５を形成する（ステップＳ２０２）。

【０１００】

（撥水化処理を行う工程）

続いて、第１の実施の形態と同様にして、基板１１の下部電極１４および隔壁１５を形成した側の表面に対して酸素プラズマ処理を行ったのち、撥水化処理（撥液化処理）を行う（ステップＳ２０３）ことにより、特に上部隔壁１５Ｂの上面及び側面の濡れ性を低下させる。

【０１０１】

（正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成する工程）

そののち、第１の実施の形態と同様にして、図１６（Ｂ）に示したように、上部隔壁１５Ｂに囲まれた領域内に、上述した材料よりなる正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成する（ステップＳ２０４）。

【０１０２】

（正孔輸送層１６ＢＲ，１６ＢＧを形成する工程）

正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成したのち、第１の実施の形態と同様にして、図１６（Ｃ）に示したように、正孔注入層１６ＡＲ，１６ＡＧの上に、上述した高分子材料よりなる正孔輸送層１６ＢＲ，１６ＢＧを赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの各々ごとに形成する（ステップＳ２０５）。

【０１０３】

ここでは、赤色有機ＥＬ素子１０および緑色有機ＥＬ素子１０Ｇの各々が、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接しているので、第１の実施の形態と同様に、青色有機ＥＬ素子１０Ｂに隣接している辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の正孔輸送層１６ＢＲ，１６ＢＧの膜厚の片寄りが低減されている。よって、正孔輸送層１６ＢＲ，１６ＢＧの膜厚の均一性または対称性が向上する。

【０１０４】

（赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを形成する工程）

正孔輸送層１６ＡＲ，１６ＡＧを形成したのち、第１の実施の形態と同様にして、図１７（Ａ）に示したように、赤色有機ＥＬ素子１０Ｒの正孔輸送層１６ＢＲの上に上述した高分子材料よりなる赤色発光層１６ＣＲを形成する。また、緑色有機ＥＬ素子１０Ｇの正孔輸送層１６ＢＧの上に上述した高分子よりなる緑色発光層１６ＣＧを形成する（ステップＳ２０６）。

【０１０５】

ここでもまた、赤色有機ＥＬ素子１０および緑色有機ＥＬ素子１０Ｇの各々が、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接しているので、第１の実施の形態と同様に、青色有機ＥＬ素子１０Ｂに隣接している辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の片寄りが低減されている。よって、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の均一性または対称性が向上する。

【０１０６】

（青色有機ＥＬ素子１０Ｂの正孔輸送層１６ＢＢを形成する工程）

赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを形成したのち、図１７（Ｂ）に示したように、青色有機発光素子１０Ｂ用の正孔注入層１６ＡＢの上に、上述した低分子材料よりなる正孔輸送層１６ＢＢを形成する（ステップＳ２０７）。正孔輸送層１６ＢＢは、インクジェット，ノズルプリンティング，凸版印刷，グラビア印刷または反転オフセット印刷などの塗布法により形成する。特に、上部隔壁１５Ｂに囲まれた領域に正孔輸送層１６ＢＢの形成材料を選択的に配する必要上、液滴吐出法であるインクジェット法や、ノズルプリンティング法を用いることが好ましい。

【０１０７】

具体的には、例えばインクジェット法により、正孔輸送層１６ＢＢの形成材料である低分子の溶液または分散液を正孔注入層１６ＡＢの露出面上に配する。その後、熱処理（乾燥処理）を行うことにより、正孔輸送層１６ＢＢを形成する。

【０１０８】

熱処理においては、溶媒または分散媒を乾燥後、高温で加熱する。塗布する雰囲気や溶媒を乾燥、加熱する雰囲気としては、窒素（N_2）を主成分とする雰囲気中が好ましい。酸素や水分があると、作成された有機ＥＬ表示装置の発光効率や寿命が低下する恐れがある。特に、加熱工程においては、酸素や水分の影響が大きいため、注意が必要である。好ましい酸素濃度は、０．１ｐｐｍ以上１００ｐｐｍ以下が好ましく、５０ｐｐｍ以下であればより好ましい。１００ｐｐｍより多い酸素があると、形成した薄膜の界面が汚染され、得られた有機ＥＬ表示装置の発光効率や寿命が低下する恐れがある。また、０．１ｐｐｍ未満の酸素濃度の場合、素子の特性は問題ないが、現状の量産のプロセスとして、雰囲気を０．１ｐｐｍ未満に保持するための装置コストが多大になる可能性がある。

また、水分については、露点が例えば－８０℃以上－４０℃以下であることが好ましい。更に、－５０℃以下であればより好ましく、－６０℃以下であれば更に好ましい。－４０℃より高い水分があると、形成した薄膜の界面が汚染され、得られた有機ＥＬ表示装置の発光効率や寿命が低下する恐れがある。また、－８０℃未満の水分の場合、素子の特性は問題ないが、現状の量産のプロセスとして、雰囲気を－８０℃未満に保持するための装置コストが多大になる可能性がある。

【０１０９】

加熱温度は、材料の特性にもよるが、１００℃～２３０℃が好ましく、さらに好ましくは１００℃～２００℃である。少なくとも、正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢ形成時の温度よりも低いことが好ましい。また低分子材料のＴｇを超えすぎた温度で加熱しつづけると、特性が大きく低下する恐れがある。時間は、温度、雰囲気にもよるが、５分～３００分程度が好ましく、さらに好ましくは、１０分～２４０分である。乾燥後の膜厚みは、素子の全体構成にもよるが、１０ｎｍ～２００ｎｍが好ましい。さらに、１５ｎｍ～１５０ｎｍであればより好ましい。

【０１１０】

（工程の順序について）

赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの正孔輸送層１６ＢＲ，１６ＢＧを形成する工程と、青色有機ＥＬ素子１０Ｂの正孔輸送層１６ＢＢを形成する工程と、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを形成する工程とは、いずれの順番で行ってもよいが、少なくとも、形成する層を展開する下地が先に形成されており、加熱乾燥各工程の加熱工程を経ていることが必要である。また、加熱工程時の温度が、前工程よりも少な

くとも同等もしくは低い温度で行うように、塗布する必要がある。例えば、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの加熱温度が、１３０℃であり、青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの加熱温度が同じ１３０℃である場合、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの塗布を行い、乾燥せずに、続けて、青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの塗布をした後、赤色発光層１６ＣＲ，緑色発光層１６ＣＧおよび青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの乾燥、加熱工程を行ってもよい。

また、上記各工程において、乾燥と加熱とは別個の工程として分けて行うことが好ましい。理由として、乾燥工程では、塗布したウエット膜が、非常に流動しやすいために、膜ムラが起きやすいからである。好ましい乾燥工程は、常圧で均一に真空乾燥する方法であり、さらに、乾燥中に風などをあてずに乾燥させることが望ましい。加熱工程では、ある程度、溶媒が飛んで流動性が低下し、硬化した膜になっており、そこからゆっくりと、熱をかけることにより、微量に残存している溶媒を取り除いたり、発光材料や正孔輸送層の材料を分子レベルで再配列を起こさせることが可能となる。

【０１１１】

（青色発光層１６ＣＢを形成する工程）

青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢおよび赤色発光層１６ＣＲ，緑色発光層１６ＣＧまで形成したのち、第１の実施の形態と同様にして、図１７（Ｃ）に示したように、蒸着法により、赤色発光層１６ＣＲ，緑色発光層１６ＣＧおよび青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの全面に、上述した低分子材料よりなる青色発光層１６ＣＢを共通層として形成する（ステップＳ２０９）。

【０１１２】

（電子輸送層１６Ｄ，電子注入層１６Ｅおよび上部電極１７を形成する工程）

青色発光層１６ＣＢを形成したのち、第１の実施の形態と同様にして、図１８（Ａ），図１８（Ｂ）および図１８（Ｃ）に示したように、この青色発光層１６ＣＢの全面に、蒸着法により、上述した材料よりなる電子輸送層１６Ｅ，電子注入層１６Ｆおよび上部電極１７を形成する（ステップＳ２１０，Ｓ２１１，Ｓ２１２）。

【０１１３】

上部電極１７を形成したのち、第１の実施の形態と同様にして、図３に示したように、保護層２０を形成する。また、第１の実施の形態と同様にして、上述した材料よりなる封止用基板４０に、遮光膜，赤色フィルタ（図示せず），青色フィルタ（図示せず）および緑色フィルタ（図示せず）を順次形成する。

【０１１４】

そののち、保護層２０の上に、接着層（図示せず）を形成し、この接着層を間にして、封止用基板４０を貼り合わせる。以上により、図１ないし図３に示した表示装置が完成する。

【０１１５】

この有機ＥＬ表示装置では、各画素に対して第１の実施の形態と同様にして駆動制御がなされることにより、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂに駆動電流Ｉｄが注入され、正孔と電子とが再結合して発光が起こる。この光は、下面発光（ボトムエミッション）の場合には下部電極１４および基板１１を透過して、上面発光（トップエミッション）の場合には上部電極１７，カラーフィルタ（図示せず）および封止用基板４０を透過して取り出される。

【０１１６】

その際、赤色有機ＥＬ素子１０Ｒでは、赤色発光層１６ＣＲと青色発光層１６ＣＢとが設けられているが、最もエネルギー準位の低い赤色にエネルギー移動が起こり、赤色発光が支配的となる。緑色有機ＥＬ素子１０Ｇでは、緑色発光層１６ＣＧと青色発光層１６ＣＢとが設けられているが、よりエネルギー準位の低い緑色にエネルギー移動が起こり、緑色発光が支配的となる。青色有機ＥＬ素子１０Ｂでは、青色発光層１６ＣＢのみを有するので、青色発光が生じる。ここでは、青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢが低分子材料により構成されているので、低分子材料よりなる青色発光層１６ＣＢとの界面

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状態が改善され、青色の発光効率および寿命が向上する。

【０１１７】

このように本実施の形態では、青色有機ＥＬ素子１０Ｂの正孔注入層１６ＡＢの上に低分子材料よりなる正孔輸送層１６ＢＢを塗布法により形成するようにしたので、第１の実施の形態の効果に加えて、低分子材料よりなる青色発光層１６ＣＢとの界面状態を改善し、青色の発光効率および寿命を向上させることが可能になる。よって、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび青色有機ＥＬ素子１０Ｂを配列形成してなるカラー有機ＥＬ表示装置のさらなる高発光効率化、長寿命化が可能になる。また、蒸着時のパターニングの困難さを解消し、かつ印刷プロセスによる低コスト化を実現することが可能となる。

【０１１８】

（第３の実施の形態）

第３の実施の形態は、赤色発光層１６ＣＲおよび緑色発光層１６ＣＣＧが低分子材料を含むようにしたことを除いては、上記第２の実施の形態と同様の構成を有している。

【０１１９】

赤色発光層１６ＣＲ，緑色発光層１６ＣＣＧは高分子（発光）材料に低分子材料が添加された混合材料により構成されている。これにより本実施の形態では、共通層である青色発光層１６ＣＢから赤色発光層１６ＣＲまたは緑色発光層１６ＣＣＧへの正孔および電子の注入効率を向上させることが可能となっている。ここで低分子材料とは、モノマーまたはこのモノマーを２～１０個結合したオリゴマーとし、５万以下の重量平均分子量を有するものが好ましい。なお、重量平均分子量が上記範囲を超えた低分子材料を必ずしも除外するものではない。

【０１２０】

赤色発光層１６ＣＲおよび緑色発光層１６ＣＣＧは、例えばインクジェット等の塗付法により形成する。その際、高分子材料および低分子材料を例えばトルエン、キシレン、アニソール、シクロヘキサノン、メシチレン（１，３，５－トリメチルベンゼン）、プサイドクメン（１，２，４－トリメチルベンゼン）、ジハイドロベンゾフラン、１，２，３，４－テトラメチルベンゼン、テトラリン、シクロヘキシルベンゼン、１－メチルナフタレン、ｐ－アニシルアルコール、ジメチルナフタレン、3-メチルビフェニル、４－メチルビフェニル、３－イソプロピルビフェニル、モノイソプロピルナフタレンなどの有機溶媒に少なくとも１種類以上使って溶解し、この混合溶液を用いて形成する。

【０１２１】

赤色発光層１６ＣＲ，緑色発光層１６ＣＣＧを構成する高分子材料としては、例えばポリフルオレン系高分子誘導体や、（ポリ）パラフェニレンビニレン誘導体、ポリフェニレン誘導体、ポリビニルカルバゾール誘導体、ポリチオフェン誘導体、ペリレン系色素、クマリン系色素、ローダミン系色素、あるいは上記高分子に有機ＥＬ材料をドープしたものが挙げられる。ドープ材料としては、例えばルブレン、ペリレン、９，１０ジフェニルアントラセン、テトラフェニルブタジエン、ナイルレッド、クマリン６等を用いることができる。

【０１２２】

以下、赤色発光層１６ＣＲ，緑色発光層１６ＣＣＧを構成する高分子材料に低分子材料を添加することにより、共通層である青色発光層１６ＣＢから赤色発光層１６ＣＲまたは緑色発光層１６ＣＣＧへの正孔および電子の注入効率が向上する原理について説明する。

【０１２３】

第１および第２の実施の形態では、高分子材料のみから構成される赤色発光層１６ＣＲ，緑色発光層１６ＣＣＧの上部に共通層として低分子材料からなる青色発光層１６ＣＢを形成しており、赤色発光層１６ＣＲ，緑色発光層１６ＣＣＧのエネルギー準位と、青色発光層１６ＣＢのエネルギー準位との差は大きい。このため、青色発光層１６ＣＢと赤色発光層１６ＣＲおよび緑色発光層１６ＣＣＧ各々との間の正孔または電子の注入効率は非常に低く、本来の高分子材料からなる発光層が有する特性を十分に得ることができないおそれがあ

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った。本実施の形態では、この正孔または電子の注入特性を向上させるために、赤色発光層１６ＣＲ，緑色発光層１６ＣＧが有するエネルギー準位と、青色発光層１６ＣＢが有するエネルギー準位との差を小さくする低分子材料（モノマーまたはオリゴマー）を赤色発光層１６ＣＲ，緑色発光層１６ＤＧに添加するものである。ここでは、赤色発光層１６ＣＲ，緑色発光層１６ＣＲの最高占有分子軌道（ＨＯＭＯ）準位および最低非占有分子軌道（ＬＵＭＯ）準位と、青色発光層１６ＣＢのＨＯＭＯ（最高占有分子軌道）準位および最低非占有分子軌道（ＬＵＭＯ）準位と赤色発光層１６ＣＲおよび緑色発光層１６ＣＧに添加する低分子材料のＨＯＭＯ（最高占有分子軌道）準位および最低非占有分子軌道（ＬＵＭＯ）準位との関係を考慮する。具体的な添加する低分子材料としては、赤色発光層１６ＣＲまたは緑色発光層１６ＣＧのそれぞれのＬＵＭＯより低い値を有すると共に、青色発光層のＬＵＭＯより高い値を有し、かつ、赤色発光層１６ＣＲまたは緑色発光層１６ＣＧのそれぞれのＨＯＭＯより高い値を有すると共に、青色発光層のＨＯＭＯより低い値を有する化合物を選択する。

【０１２４】

また、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧに添加する低分子材料は、低分子化合物が同じ反応または類似の反応を連鎖的に繰り返すことにより生じた高分子量の重合体または縮合体の分子からなる化合物以外のものであって、分子量が実質的に単一であるものを指す。また加熱による分子間の新たな化学結合は生じず、単分子で存在する。このような低分子材料の重量平均分子量（Ｍｗ）は５万以下であることが好ましい。これは分子量の大きい、例えば５万以上の材料に比べてある程度小さい分子量の材料のほうが多様な特性を有し、正孔または電子の移動度やバンドギャップあるいは溶媒への溶解度などを調整しやすいためである。また、低分子材料の添加量は、赤色発光層１６ＣＲまたは緑色発光層１６ＣＧに用いられる高分子材料：低分子材料の混合比率が、その重量比で１０：１以上１：２以下になるようにすることが好ましい。高分子材料：低分子材料の混合比率が１０：１未満では、低分子材料の添加による効果が低くなるためである。また、この混合比率が１：２を超える場合には、発光材料としての高分子材料が有する特性が得られにくくなるためである。

【０１２５】

このような低分子材料としては、例えば、ベンジン、スチリルアミン、トリフェニルアミン、ポルフィリン、トリフェニレン、アザトリフェニレン、テトラシアノキノジメタン、トリアゾール、イミダゾール、オキサジアゾール、ポリアリールアルカン、フェニレンジアミン、アリールアミン、オキザゾール、アントラセン、フルオレノン、ヒドラゾン、スチルベンあるいはこれらの誘導体、または、ポリシラン系化合物、ビニルカルバゾール系化合物、チオフェン系化合物あるいはアニリン系化合物等の複素環式共役系のモノマーあるいはオリゴマーを用いることができる。

【０１２６】

さらに具体的な材料としては、α－ナフチルフェニルフェニレンジアミン、ポルフィリン、金属テトラフェニルポルフィリン、金属ナフタロシアニン、ヘキサシアノアザトリフェニレン、７，７，８，８－テトラシアノキノジメタン（ＴＣＮＱ）、７，７，８，８－テトラシアノ－２，３，５，６－テトラフルオロキノジメタン（Ｆ４－ＴＣＮＱ）、テトラシアノ４、４、４－トリス（３－メチルフェニルフェニルアミノ）トリフェニルアミン、Ｎ、Ｎ、Ｎ’、Ｎ’－テトラキス（ｐ－トリル）ｐ－フェニレンジアミン、Ｎ、Ｎ、Ｎ’、Ｎ’－テトラフェニル－４、４’－ジアミノビフェニル、Ｎ－フェニルカルバゾール、４－ジ－ｐ－トリルアミノスチルベン、ポリ（パラフェニレンビニレン）、ポリ（チオフェンビニレン）、ポリ（２、２’－チエニルピロール）などが挙げられるが、これらに限定されるものではない。

【０１２７】

なお、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧに添加する低分子材料は１種類だけでなく、複数種類を混合して用いてもよい。

【０１２８】

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この有機ＥＬ表示装置は、例えば、第２の実施の形態と同様にして製造することができる。

【０１２９】

この有機ＥＬ表示装置では、各画素に対して第１の実施の形態と同様にして駆動制御が行われることにより、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂに駆動電流Ｉｄが注入され、正孔と電子とが再結合して発光が起こる。この光は、下面発光（ボトムエミッション）の場合には下部電極１４および基板１１を透過して、上面発光（トップエミッション）の場合には上部電極１７，カラーフィルタ（図示せず）および封止用基板４０を透過して取り出される。

【０１３０】

その際、赤色有機ＥＬ素子１０Ｒでは、赤色発光層１６ＣＲと青色発光層１６ＣＢとが設けられているが、最もエネルギー準位の低い赤色にエネルギー移動が起こり、赤色発光が支配的となる。緑色有機ＥＬ素子１０Ｇでは、緑色発光層１６ＣＧと青色発光層１６ＣＢとが設けられているが、よりエネルギー準位の低い緑色にエネルギー移動が起こり、緑色発光が支配的となる。青色有機ＥＬ素子１０Ｂでは、青色発光層１６ＣＢのみを有するので、青色発光が生じる。前述のように第１および第２の実施の形態では、青色発光層１６ＣＢから赤色発光層１６ＣＲまたは緑色発光層１６ＣＧへの正孔または電子の注入効率が低く、高分子材料からなる赤色発光層１６ＣＲまたは緑色発光層１６ＣＧが有する本来の特性が発揮されていなかった。

【０１３１】

ここでは、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを、高分子材料に低分子材料を添加した構成としているので、低分子材料からなる青色発光層１６ＣＢとのエネルギー準位の差が小さくなる。これにより青色発光層１６ＣＢから赤色発光層１６ＣＲまたは緑色発光層１６ＣＧへの正孔または電子の注入効率が改善され、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧが有する素子特性に近い値を実際に得ることが可能となる。

【０１３２】

このように本実施の形態では、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを、高分子材料および低分子材料の混合材料を用いて塗布法により形成するようにしたので、第１の実施の形態の効果に加えて、青色発光層１６ＣＢから赤色発光層１６ＣＲまたは緑色発光層１６ＣＧへの正孔または電子の移動効率が改善され、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧが有する素子特性に近い値が得られる。すなわち、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび青色有機ＥＬ素子１０Ｂを配列形成してなるカラー有機ＥＬ表示装置のさらなる高発光効率化、長寿命化が可能になる。

【０１３３】

（第４の実施の形態）

図１９は、本発明の第４の実施の形態に係る有機ＥＬ表示装置１Ａの表示領域１１０の断面構成を表したものである。この有機ＥＬ表示装置１Ａは、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧおよび青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの全面と、青色発光層１６ＣＢとの間に、低分子材料からなる共通正孔輸送層１６Ｄを有している。このことを除いては、この有機ＥＬ表示装置１Ａは上記第３の実施の形態と同様の構成を有している。

【０１３４】

赤色有機ＥＬ素子１０Ｒの有機層１６は、例えば、下部電極１４の側から順に、正孔注入層１６ＡＲ，正孔輸送層１６ＢＲ，赤色発光層１６ＣＲ，共通正孔輸送層（第２正孔注入・輸送層）１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆを積層した構成を有する。緑色有機ＥＬ素子１０Ｇの有機層１６は、例えば、下部電極１４の側から順に、正孔注入層１６ＡＧ，正孔輸送層１６ＢＧ，緑色発光層１６ＣＧ，共通正孔輸送層１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆを積層した構成を有する。青色有機ＥＬ素子１０Ｂの有機層１６は、例えば、下部電極１４の側から順に、正孔注入層１６ＡＢ，正孔輸送層１６ＢＢ，共通正孔輸送層１６Ｄ，青色発光

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層１６ＣＢ，電子輸送層１６Ｄおよび電子注入層１６Ｅを積層した構成を有する。これらのうち共通正孔輸送層１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆは、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの共通層として設けられている。

【０１３５】

赤色発光層１６ＣＲ，緑色発光層１６ＣＧは、第３の実施の形態と同様に、高分子（発光）材料に低分子材料が添加された混合材料により構成されている。

【０１３６】

青色有機ＥＬ素子１０Ｂの正孔輸送層１６ＢＢは、低分子材料（モノマーおよびオリゴマー）または高分子材料のいずれでもよい。ここで用いる低分子材料のうちモノマーは赤色発光層１６ＣＲおよび緑色発光層１６ＣＧに添加する低分子材料と同様の低分子化合物の重合体または縮合体等の化合物以外のものであって、分子量が単一であるものであり、単分子で存在するものである。また、オリゴマーはモノマーが複数個結合したものであり、重量平均分子量（Ｍｗ）は５万以下のものを指す。更に高分子材料は正孔輸送層１６ＢＲ，１６ＢＧに用いられる高分子材料と同様に、重量平均分子量が５万～３０万の範囲であればよく、と特に１０万～２０万程度が好ましい。なお、正孔輸送層１６ＢＢに用いる低分子材料および高分子材料は分子量および重量平均分子量の異なる２種以上の材料を混合して用いてもよい。

【０１３７】

共通正孔輸送層１６Ｄは、青色発光層１６ＣＢへの正孔の注入効率を向上させるものであり、赤色発光層１６ＣＲ，緑色発光層１６ＣＧおよび青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの全面に共通層として設けられている。共通正孔輸送層１６Ｄの厚みは、素子の全体構成にもよるが、例えば１ｎｍ～２０ｎｍであることが好ましく、さらに好ましくは１ｎｍ～１０ｎｍである。

【０１３８】

共通正孔輸送層１６Ｄは蒸着法を用いて形成するため、低分子材料、特にモノマーを用いることが好ましい。オリゴマーまたは高分子材料のような重合された分子は蒸着中分解が起こる虞があるためである。なお、共通正孔輸送層１６Ｄに用いる低分子材料は分子量の異なる２種以上の材料を混合して用いてもよい。

【０１３９】

共通正孔輸送層１６Ｄに用いられる低分子材料としては、第３の実施の形態の赤色発光層１６ＣＲ、緑色発光層１６ＣＧおよび青色正孔輸送層１６ＣＢにおいて説明した低分子材料と同様に、例えば、ベンジン、スチリルアミン、トリフェニルアミン、ポルフィリン、トリフェニレン、アザトリフェニレン、テトラシアノキノジメタン、トリアゾール、イミダゾール、オキサジアゾール、ポリアリールアルカン、フェニレンジアミン、アリールアミン、オキザゾール、アントラセン、フルオレノン、ヒドラゾン、スチルベンあるいはこれらの誘導体、または、ポリシラン系化合物、ビニルカルバゾール系化合物、チオフェン系化合物あるいはアニリン系化合物等の複素環式共役系のモノマー、オリゴマーまたはポリマーを用いることができる。

【０１４０】

さらに具体的な材料としては、α－ナフチルフェニルフェニレンジアミン、ポルフィリン、金属テトラフェニルポルフィリン、金属ナフタロシアニン、ヘキサシアノアザトリフェニレン、７，７，８，８－テトラシアノキノジメタン（ＴＣＮＱ）、７，７，８，８－テトラシアノ－２，３，５，６－テトラフルオロキノジメタン（Ｆ４－ＴＣＮＱ）、テトラシアノ４、４、４－トリス（３－メチルフェニルフェニルアミノ）トリフェニルアミン、Ｎ、Ｎ、Ｎ’、Ｎ’－テトラキス（ｐ－トリル）ｐ－フェニレンジアミン、Ｎ、Ｎ、Ｎ’、Ｎ’－テトラフェニル－４、４’－ジアミノビフェニル、Ｎ－フェニルカルバゾール、４－ジ－ｐ－トリルアミノスチルベン、ポリ（パラフェニレンビニレン）、ポリ（チオフェンビニレン）、ポリ（２、２’－チエニルピロール）などが挙げられるが、これらに限定されるものではない。

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【０１４１】
この有機ＥＬ表示装置は、例えば次のようにして製造することができる。
【０１４２】
図２０は、この有機ＥＬ表示装置の製造方法の流れを表したものであり、図２１ないし図２３は図２０に示した製造方法を工程順に表したものである。
【０１４３】
（下部電極１４を形成する工程）
まず、第１の実施の形態と同様にして、図２１（Ａ）に示したように、画素駆動回路１４０および平坦化絶縁膜を形成した基板１１の上に下部電極１４を形成する（ステップＳ３０１）。
【０１４４】
（隔壁１５を形成する工程）
次いで、第１の実施の形態と同様にして、同じく図２１（Ａ）に示したように、下部隔壁１５Ａおよび上部隔壁１５Ｂよりなる隔壁１５を形成する（ステップＳ３０２）。
【０１４５】
（撥水化処理を行う工程）
続いて、第１の実施の形態と同様にして、基板１１の下部電極１４および隔壁１５を形成した側の表面に対して、酸素プラズマ処理を行ったのち、撥水化処理（撥液化処理）を行う（ステップＳ３０３）ことにより、特に上部隔壁１５Ｂの上面及び側面の濡れ性を低下させる。
【０１４６】
（正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成する工程）
そののち、第１の実施の形態と同様にして、図２１（Ｂ）に示したように、上部隔壁１５Ｂに囲まれた領域内に、上述した材料よりなる正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成する（ステップＳ３０４）。
【０１４７】
（正孔輸送層１６ＢＲ，１６ＢＧを形成する工程）
正孔注入層１６ＡＲ，１６ＡＧ，１６ＡＢを形成したのち、第１の実施の形態と同様にして、図２１（Ｃ）に示したように、正孔注入層１６ＡＲ，１６ＡＧの上に、上述した高分子材料よりなる正孔輸送層１６ＢＲ，１６ＢＧを赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの各々ごとに形成する（ステップＳ３０５）。
【０１４８】
ここでは、赤色有機ＥＬ素子１０および緑色有機ＥＬ素子１０Ｇの各々が、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接しているので、第１の実施の形態と同様に、青色有機ＥＬ素子１０Ｂに隣接している辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の正孔輸送層１６ＢＲ，１６ＢＧの膜厚の片寄りが低減されている。よって、正孔輸送層１６ＢＲ，１６ＢＧの膜厚の均一性または対称性が向上する。
【０１４９】
（赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを形成する工程）
正孔輸送層１６ＡＲ，１６ＡＧを形成したのち、第１の実施の形態と同様にして、図２２（Ａ）に示したように、赤色有機ＥＬ素子１０Ｒの正孔輸送層１６ＢＲの上に上述した高分子材料よりなる赤色発光層１６ＣＲを形成する。また、緑色有機ＥＬ素子１０Ｇの正孔輸送層１６ＢＧの上に上述した高分子よりなる緑色発光層１６ＣＧを形成する（ステップＳ３０６）。
【０１５０】
ここでもまた、赤色有機ＥＬ素子１０および緑色有機ＥＬ素子１０Ｇの各々が、少なくとも対向する２辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接しているので、第１の実施の形態と同様に、青色有機ＥＬ素子１０Ｂに隣接している辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲおよび緑色発

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光層１６ＣＧの膜厚の片寄りが低減されている。よって、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧの膜厚の均一性または対称性が向上する。

【０１５１】

（青色有機ＥＬ素子１０Ｂの正孔輸送層１６ＢＢを形成する工程）

赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを形成したのち、第３の実施の形態と同様に、図２２（Ｂ）に示したように、青色有機発光素子１０Ｂ用の正孔注入層１６ＡＢの上に、上述した材料よりなる正孔輸送層１６ＢＢを形成する（ステップＳ３０７）。

【０１５２】

（工程の順序について）

赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇの正孔輸送層１６ＢＲ，１６ＢＧを形成する工程と、青色有機ＥＬ素子１０Ｂの正孔輸送層１６ＢＢを形成する工程と、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを形成する工程との順序については、第２の実施の形態と同様である。

【０１５３】

（共通正孔輸送層１６Ｄを形成する工程）

青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢおよび赤色発光層１６ＣＲ，緑色発光層１６ＣＧまで形成したのち、図２２（Ｃ）に示したように、蒸着法により、赤色発光層１６ＣＲ，緑色発光層１６ＣＧおよび青色有機ＥＬ素子１０Ｂ用の正孔輸送層１６ＢＢの全面に、上述した低分子材料よりなる共通正孔輸送層１６Ｄを共通層として形成する（ステップＳ３０８）。

【０１５４】

（青色発光層１６ＣＢを形成する工程）

共通正孔輸送層１６Ｄを形成したのち、図２２（Ｄ）に示したように、蒸着法により、共通正孔輸送層１６Ｄの全面に、上述した低分子材料よりなる青色発光層１６ＣＢを共通層として形成する（ステップＳ３０９）。

【０１５５】

（電子輸送層１６Ｄ，電子注入層１６Ｅおよび上部電極１７を形成する工程）

青色発光層１６ＣＢを形成したのち、第１の実施の形態と同様にして、図２３（Ａ），図２３（Ｂ）および図２３（Ｃ）に示したように、この青色発光層１６ＣＢの全面に、蒸着法により、上述した材料よりなる電子輸送層１６Ｅ，電子注入層１６Ｆおよび上部電極１７を形成する（ステップＳ３１０，Ｓ３１１，Ｓ３１２）。

【０１５６】

上部電極１７を形成したのち、第１の実施の形態と同様にして、図３に示したように、保護層２０を形成する。このとき、共通正孔輸送層１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅ，電子注入層１６Ｆ，上部電極１７および保護層２０は、マスクを用いることなく全面にベタ膜として形成される。また、共通正孔輸送層１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅ，電子注入層１６Ｆ，上部電極１７および保護層２０の形成は、望ましくは、大気に暴露されることなく同一の成膜装置内において連続して行われる。これにより大気中の水分による有機層１６の劣化が防止される。

【０１５７】

保護層２０を形成したのち、第１の実施の形態と同様にして、上述した材料よりなる封止用基板４０に、遮光膜，赤色フィルタ（図示せず），青色フィルタ（図示せず）および緑色フィルタ（図示せず）を順次形成する。

【０１５８】

そののち、保護層２０の上に、接着層（図示せず）を形成し、この接着層を間にして、封止用基板４０を貼り合わせる。以上により、図１ないし図３に示した表示装置が完成する。

【０１５９】

この有機ＥＬ表示装置１Ａでは、各画素に対して第１の実施の形態と同様の駆動制御がなされることにより、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ

素子１０Ｂに駆動電流Ｉｄが注入され、正孔と電子とが再結合して発光が起こる。この光は、下面発光（ボトムエミッション）の場合には下部電極１４および基板１１を透過して、上面発光（トップエミッション）の場合には上部電極１７，カラーフィルタ（図示せず）および封止用基板４０を透過して取り出される。

【０１６０】

その際、第２または第３の実施の形態のように塗布法によって形成された青色正孔輸送層１６ＢＢ上に直接青色発光層１６ＣＢを設けた場合には、以下の理由により青色発光層１６ＣＢの本来の特性が発揮されないおそれがあった。まず、第１の理由としては塗付法による青色正孔輸送層１６ＢＢの形成時に混入する水分や残存溶媒等による正孔注入性の低下が挙げられる。第２の理由としては、青色正孔輸送層１６ＢＢは大気環境下で形成されるため界面汚染等による劣化が挙げられる。

【０１６１】

本実施の形態の有機ＥＬ表示装置では、青色正孔輸送層１６ＢＢ上に低分子材料からなる共通正孔輸送層１６Ｄを蒸着法により形成するようにしたので、大気中の水分などの混入が抑制され、青色発光層１６ＣＢとの界面が改善される。これにより、青色発光層１６ＣＢへの正孔注入効率が改善され、青色発光層１６ＣＢの本体の特性に近い値を得ることが可能となる。

【０１６２】

なお、共通正孔輸送層１６Ｄは蒸着法によって形成するため、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧ上にも共通正孔輸送層１６Ｄが形成される。これにより赤色発光層１６ＣＲおよび緑色発光層１６ＣＧと、青色発光層１６ＣＢとは共通正孔輸送層１６Ｄを介して積層されることとなる。共通正孔輸送層１６Ｄは、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧ上では通常は電子ブロック性を示すため、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧへの電子注入性は悪化する。また、第１または第２の実施の形態のように、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧが高分子材料のみから構成されている場合には、低分子材料からなる共通正孔輸送層１６Ｄとのエネルギーレベルの差が大きいため正孔輸送性能が低下するおそれがあった。そのため、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧへ注入される電子および正孔が不足し、駆動電圧が増大したり、発光効率が低下したりする可能性があった。また、正孔および電子の注入が適切に行われないため、赤色有機ＥＬ素子１０Ｒまたは緑色有機ＥＬ素子１０Ｇを発光させた際に、４３０～５００ｎｍにピークを持つ青色の発光を伴うおそれがあった。即ち、赤色光または緑色光に青色光が混色することによって赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの色度が変化してしまう。これは、ディスプレイを構成する表示素子としては大きな問題となる可能性があった。

【０１６３】

これに対して、本実施の形態では、第３の実施の形態と同様に、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧを、高分子材料に低分子材料を添加した混合材料により形成しているので、エネルギーレベルの差が小さくなり、正孔輸送性能が改善されると共に適宜調整することが可能となる。また、共通正孔輸送層１６Ｄは、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧに添加した低分子材料と同系統の材料により形成されているため、各層のエネルギーレベル等の差を小さくする。更に、共通正孔輸送層１６Ｄは、青色発光層１６ＣＢを形成する材料とも同系統の材料で形成されているため、青色発光層１６ＣＢを介して赤色発光層１６ＣＲおよび緑色発光層１６ＣＧへ注入される電子の輸送性能も優れている。従って、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧと共通正孔輸送層１６Ｄとの間の正孔輸送性および電子輸送性の障壁が軽減され、上述した駆動電圧および発光効率の問題が解決される。また、赤色有機ＥＬ素子１０Ｒまたは緑色有機ＥＬ素子１０Ｇを発光させた際の青色の発光が抑えられるため、赤色発光素子１０Ｒおよび緑色発光素子１０Ｇの色度変化が抑制される。即ち、表示素子として用いることが可能な赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇを提供することが可能となる。

【０１６４】

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このように本実施の形態では、青色正孔輸送層１６ＢＢおよび赤色発光層１６ＣＲおよび緑色発光層１６ＣＢ上の全面に低分子材料からなる共通正孔輸送層１６Ｄを蒸着法により形成するようにしたので、第１ないし第３の実施の形態の効果に加えて、青色発光層１６ＣＢの界面が改善される。これにより、青色発光層１６ＣＢへの正孔の注入効率が改善され、青色発光層１６ＣＢの本体の特性に近い値を得ることが可能となる。すなわち、青色有機ＥＬ素子１０Ｂの発光効率および寿命特性が向上するため、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび青色有機ＥＬ素子１０Ｂを配列形成してなるカラー有機ＥＬ表示装置のさらなる高発光効率化、長寿命化が可能になる。

【０１６５】

また、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧへ低分子材料を添加することにより、正孔および電子のキャリアバランスを調整することがより簡易になる。これにより、共通正孔輸送層１６Ｄと青色発光層１６ＣＢおよび電子輸送層１６Ｅを形成することによって起こる、赤色発光層１６ＣＲおよび緑色発光層１６ＣＧへの電子注入性の低下および正孔輸送性の低下を抑制することが可能となる。即ち、赤色有機ＥＬ素子１０Ｒおよび緑色有機ＥＬ素子１０Ｇの発光効率および寿命の低下、駆動電圧の上昇および発光色度の変化を抑えることが可能となる。

【０１６６】

（第５の実施の形態）

図２４は本発明の第５の実施の形態における有機ＥＬ表示装置１Ｂの表示領域の断面構成を表したものである。この有機ＥＬ表示装置１Ａは、青色有機ＥＬ素子１０Ｂの正孔輸送層１６ＢＢを設けず、正孔注入層１６ＡＢ上に共通正孔輸送層１６Ｄを直接設けたことを除いては、第４の実施の形態と同様の構成を有している。

【０１６７】

赤色有機ＥＬ素子１０Ｒの有機層１６は、例えば、第１の実施の形態における赤色有機ＥＬ素子１０Ｒと同様に下部電極１４の側から順に、正孔注入層１６ＡＲ，正孔輸送層１６ＢＲ，赤色発光層１６ＣＲ，共通正孔輸送層（第２正孔注入・輸送層）１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆを積層した構成を有する。緑色有機ＥＬ素子１０Ｇの有機層１６は、例えば、第１の実施の形態における緑色有機ＥＬ素子１０Ｇと同様に下部電極１４の側から順に、正孔注入層１６ＡＧ，正孔輸送層１６ＢＧ，緑色発光層１６ＣＧ，共通正孔輸送層１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆを積層した構成を有する。青色有機ＥＬ素子１０Ｂの有機層１６は、例えば、下部電極１４の側から順に、正孔注入層１６ＡＢ，共通正孔輸送層１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆを積層した構成を有し、青色の正孔輸送層がない点が第４の実施の形態と異なる。これらのうち共通正孔輸送層１６Ｄ，青色発光層１６ＣＢ，電子輸送層１６Ｅおよび電子注入層１６Ｆは、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇ，青色有機ＥＬ素子１０Ｂの共通層として設けられている。

【０１６８】

本実施の形態の有機ＥＬ装置では第４の実施の形態の効果に加えて、更に青色有機ＥＬ素子１０Ｂの寿命特性を向上させることができる。また、青色有機ＥＬ素子１０Ｂの正孔注入層１６ＡＢ上に直接共通正孔輸送層１６Ｄを設けることにより、製造工程数が削減されると共に、コストを抑えることも可能となる。

【０１６９】

（モジュールおよび適用例）

以下、上記実施の形態で説明した有機ＥＬ表示装置の適用例について説明する。上記実施の形態の有機ＥＬ表示装置は、テレビジョン装置，デジタルカメラ，ノート型パーソナルコンピュータ、携帯電話等の携帯端末装置あるいはビデオカメラなど、外部から入力された映像信号あるいは内部で生成した映像信号を、画像あるいは映像として表示するあらゆる分野の電子機器の表示装置に適用することが可能である。

【０１７０】

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（モジュール）
上記実施の形態の有機ＥＬ表示装置は、例えば、図２５に示したようなモジュールとして、後述する適用例１～５などの種々の電子機器に組み込まれる。このモジュールは、例えば、基板１１の一辺に、保護層３０および封止用基板４０から露出した領域２１０を設け、この露出した領域２１０に、信号線駆動回路１２０および走査線駆動回路１３０の配線を延長して外部接続端子（図示せず）を形成したものである。外部接続端子には、信号の入出力のためのフレキシブルプリント配線基板（ＦＰＣ；Flexible Printed Circuit）２２０が設けられていてもよい。

【０１７１】
（適用例１）
図２６は、上記実施の形態の有機ＥＬ表示装置が適用されるテレビジョン装置の外観を表したものである。このテレビジョン装置は、例えば、フロントパネル３１０およびフィルターガラス３２０を含む映像表示画面部３００を有しており、この映像表示画面部３００は、上記実施の形態に係る有機ＥＬ表示装置により構成されている。

【０１７２】
（適用例２）
図２７は、上記実施の形態の有機ＥＬ表示装置が適用されるデジタルカメラの外観を表したものである。このデジタルカメラは、例えば、フラッシュ用の発光部４１０、表示部４２０、メニュースイッチ４３０およびシャッターボタン４４０を有しており、その表示部４２０は、上記実施の形態に係る有機ＥＬ表示装置により構成されている。

【０１７３】
（適用例３）
図２８は、上記実施の形態の有機ＥＬ表示装置が適用されるノート型パーソナルコンピュータの外観を表したものである。このノート型パーソナルコンピュータは、例えば、本体５１０，文字等の入力操作のためのキーボード５２０および画像を表示する表示部５３０を有しており、その表示部５３０は、上記実施の形態に係る有機ＥＬ表示装置により構成されている。

【０１７４】
（適用例４）
図２９は、上記実施の形態の有機ＥＬ表示装置が適用されるビデオカメラの外観を表したものである。このビデオカメラは、例えば、本体部６１０，この本体部６１０の前方側面に設けられた被写体撮影用のレンズ６２０，撮影時のスタート／ストップスイッチ６３０および表示部６４０を有しており、その表示部６４０は、上記実施の形態に係る有機ＥＬ表示装置により構成されている。

【０１７５】
（適用例５）
図３０は、上記実施の形態の有機ＥＬ表示装置が適用される携帯電話機の外観を表したものである。この携帯電話機は、例えば、上側筐体７１０と下側筐体７２０とを連結部（ヒンジ部）７３０で連結したものであり、ディスプレイ７４０，サブディスプレイ７５０，ピクチャーライト７６０およびカメラ７７０を有している。そのディスプレイ７４０またはサブディスプレイ７５０は、上記実施の形態に係る有機ＥＬ表示装置により構成されている。

【０１７６】
以上、実施の形態を挙げて本発明を説明したが、本発明は上記実施の形態に限定されるものではなく、種々変形が可能である。

【０１７７】
例えば、上記実施の形態において説明した各層の材料および厚み、または成膜方法および成膜条件などは限定されるものではなく、他の材料および厚みとしてもよく、または他の成膜方法および成膜条件としてもよい。

【０１７８】

また、上記実施の形態では、有機ＥＬ素子１０Ｒ，１０Ｇ，１０Ｂの構成を具体的に挙げて説明したが、全ての層を備える必要はなく、また、他の層を更に備えていてもよい。

【０１７９】

更に、上記実施の形態では、青色以外の有機ＥＬ素子（第２有機ＥＬ素子）として赤色および緑色の有機ＥＬ素子を備えた３原色表示の表示装置について説明したが、第２有機ＥＬ素子は、赤色有機ＥＬ素子、緑色有機ＥＬ素子、黄色有機ＥＬ素子または白色有機ＥＬ素子のうちの少なくとも１色、好ましくは少なくとも２色である。例えば、本発明は青色有機ＥＬ素子と黄色有機ＥＬ素子からなる２原色表示の表示装置への適用も可能である。

【０１８０】

加えて、本発明は、第２有機ＥＬ素子として、赤色有機ＥＬ素子および緑色有機ＥＬ素子と共に、黄色または白色の有機ＥＬ素子を備えた４原色表示の場合にも適用可能である。この場合、図３１に示したように、赤色有機ＥＬ素子８１０Ｒ，青色有機ＥＬ素子８１０Ｂ，緑色有機ＥＬ素子８１０Ｇおよび黄色有機ＥＬ素子８１０Ｙを順に配列した場合には、緑色有機ＥＬ素子８１０Ｇの左側と、赤色有機ＥＬ素子８１０Ｒの右側とにおいて乾燥速度が速くなり膜厚が厚めになる。

【０１８１】

そこで、例えば図３２ないし図３４に示したように、矩形（例えば正方形）の赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび黄色有機ＥＬ素子１０Ｙを各画素１０の三つの角に配置し、青色有機ＥＬ素子１０Ｂを残りの一つの角に配置する。このようにすれば、例えば図３２に示した第１例では、緑色有機ＥＬ素子１０Ｇの各々は、左右の二辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。よって、緑色有機ＥＬ素子１０Ｇの左右辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の緑色発光層１６ＣＧの膜厚の片寄りが低減され、左右方向での膜厚分布の均一性または対称性が良くなる。また、赤色有機ＥＬ素子１０Ｒの各々は、上下の二辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。よって、赤色有機ＥＬ素子１０Ｒの上下辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲの膜厚の片寄りが低減され、上下方向での膜厚分布の均一性または対称性が良くなる。

【０１８２】

図３３に示した第２例では、黄色有機ＥＬ素子１０Ｙの各々は、左右の二辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。よって、黄色有機ＥＬ素子１０Ｙの左右辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の黄色発光層の膜厚の片寄りが低減され、左右方向での膜厚分布の均一性または対称性が良くなる。赤色有機ＥＬ素子１０Ｒについては第１例と同様である。

【０１８３】

図３４に示した第３例では、赤色有機ＥＬ素子１０Ｒの各々は、左右の二辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。よって、赤色有機ＥＬ素子１０Ｒの左右辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＧの膜厚の片寄りが低減され、左右方向での膜厚分布の均一性または対称性が良くなる。また、緑色有機ＥＬ素子１０Ｇの各々は、上下の二辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。よって、緑色有機ＥＬ素子１０Ｇの上下辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の緑色発光層１６ＣＧの膜厚の片寄りが低減され、上下方向での膜厚分布の均一性または対称性が良くなる。

【０１８４】

あるいは、図３５に第４例として示したように、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび黄色有機ＥＬ素子１０Ｙは、一方向に配列されていてもよい。赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび黄色有機ＥＬ素子１０Ｙの各々は、上下の二辺で同一画素１０内または隣接画素１０内の青色有機ＥＬ素子１０Ｂと隣接している。この場合、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび黄色有機ＥＬ素

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子１０Ｙの上下の二辺では、塗布液の乾燥速度の不均一が抑えられ、乾燥後の赤色発光層１６ＣＲ，緑色発光層１６ＣＧおよび黄色発光層の膜厚の片寄りが低減され、上下方向での膜厚分布の均一性または対称性が良くなる。この第４例は、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび黄色有機ＥＬ素子１０Ｙが同一形状（同一面積）になるので、より好ましい。更に、図３６に示した第５例のように、青色有機ＥＬ素子１０Ｂの短辺を短くする一方、赤色有機ＥＬ素子１０Ｒ，緑色有機ＥＬ素子１０Ｇおよび黄色有機ＥＬ素子１０Ｙの長辺を長くして、開口率を調整することも可能である。

【０１８５】

なお、図３２ないし図３６は、黄色有機ＥＬ素子１０Ｙを白色有機ＥＬ素子に代えた場合にも同様にあてはまる。

【０１８６】

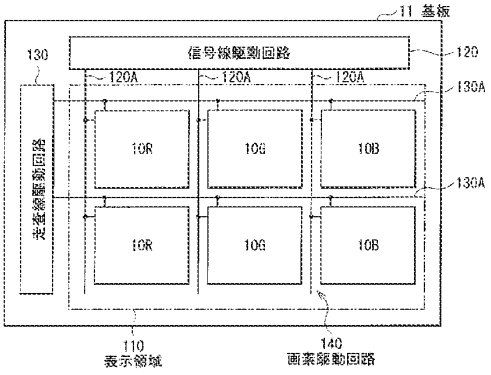
更にまた、上記実施の形態では、アクティブマトリクス型の表示装置の場合について説明したが、本発明はパッシブマトリクス型の表示装置への適用も可能である。更にまた、アクティブマトリクス駆動のための画素駆動回路の構成は、上記実施の形態で説明したものに限られず、必要に応じて容量素子やトランジスタを追加してもよい。その場合、画素駆動回路の変更に応じて、上述した信号線駆動回路１２０や走査線駆動回路１３０のほかに、必要な駆動回路を追加してもよい。

【符号の説明】

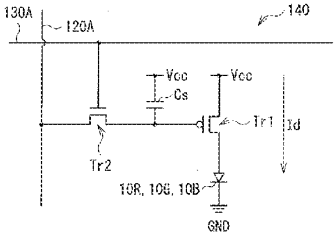
【０１８７】

１０Ｒ…赤色有機ＥＬ素子、１０Ｇ…緑色有機ＥＬ素子、１０Ｂ…青色有機ＥＬ素子、１０Ｙ…黄色有機ＥＬ素子、１１…基板、１４…下部電極、１５…隔壁、１６…有機層、１６ＡＲ，１６ＡＧ，１６ＡＢ…正孔注入層、１６ＢＲ，１６ＢＧ，１６ＢＢ…正孔輸送層、１６ＣＲ…赤色発光層、１６ＣＧ…緑色発光層、１６ＣＢ…青色発光層、１６Ｄ…共通正孔輸送層、１６Ｅ…電子輸送層、１６Ｆ…電子注入層、１７…上部電極、３０…保護層、４０…封止用基板

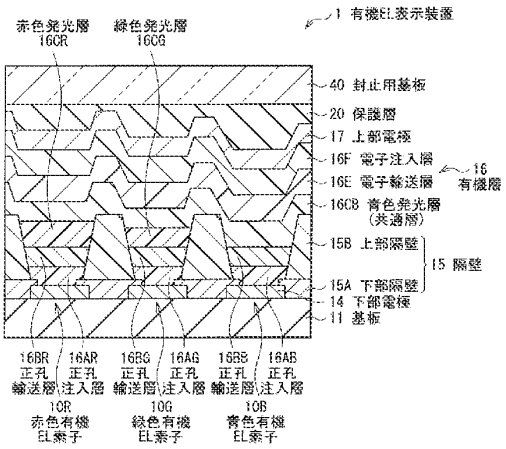
【図１】



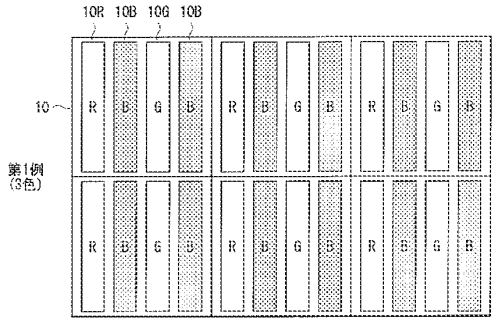
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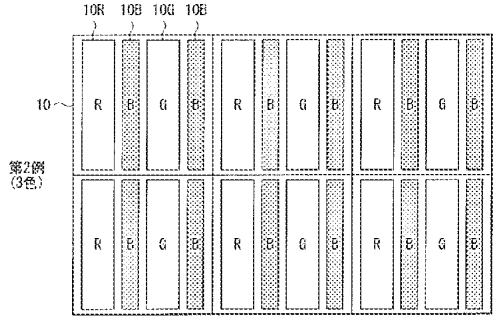
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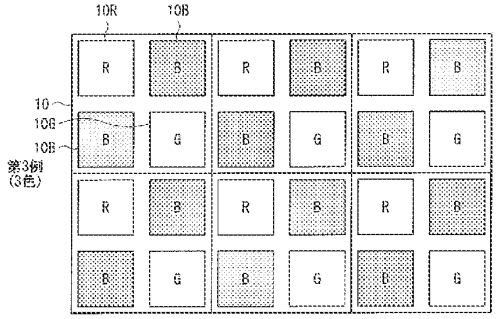
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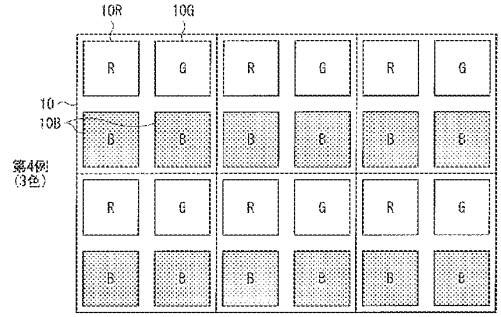
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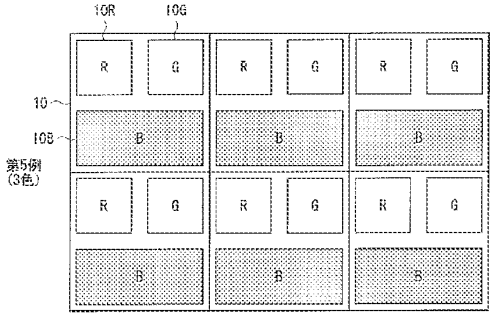
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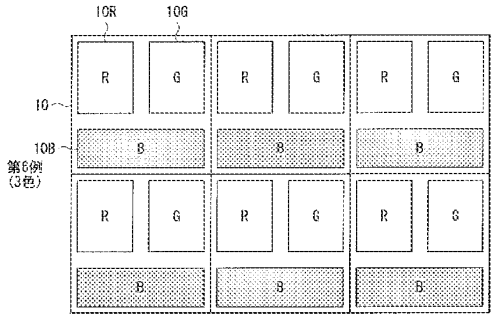
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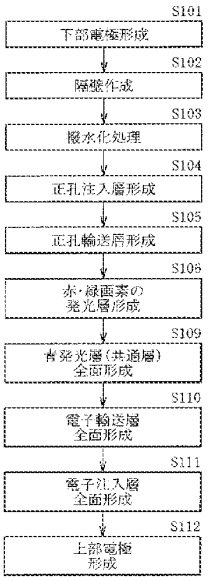
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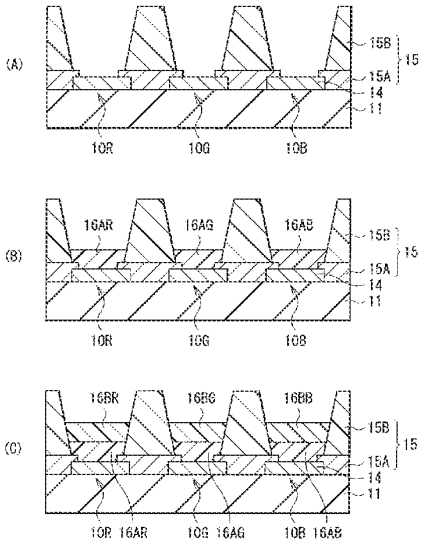
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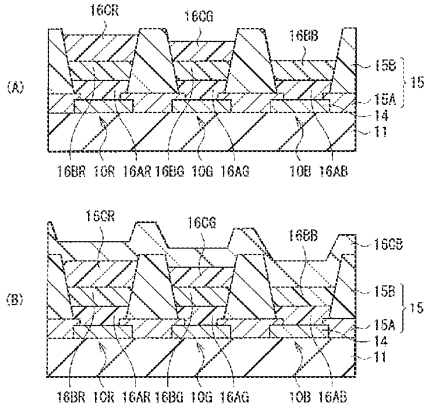
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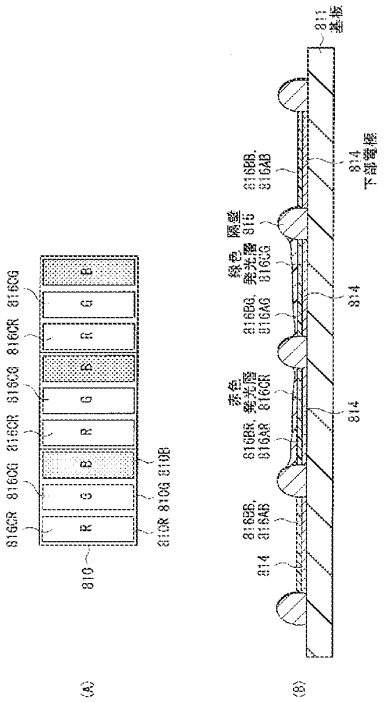
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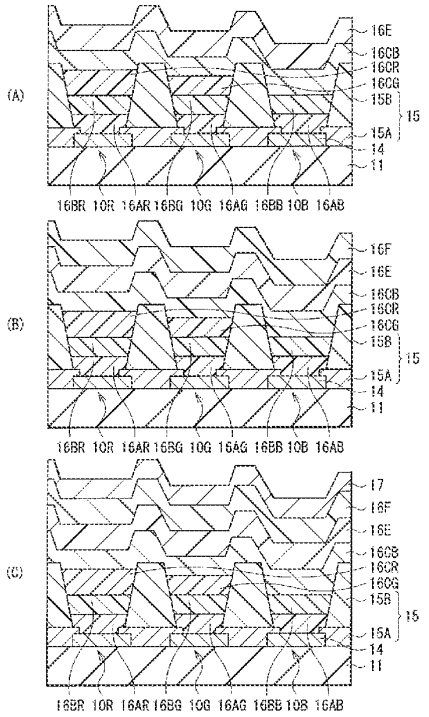
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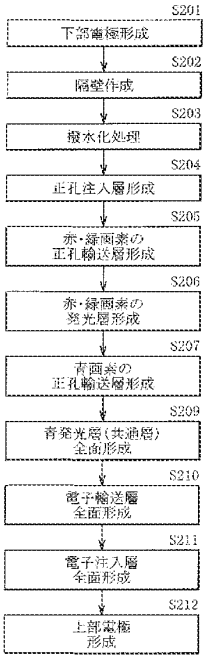
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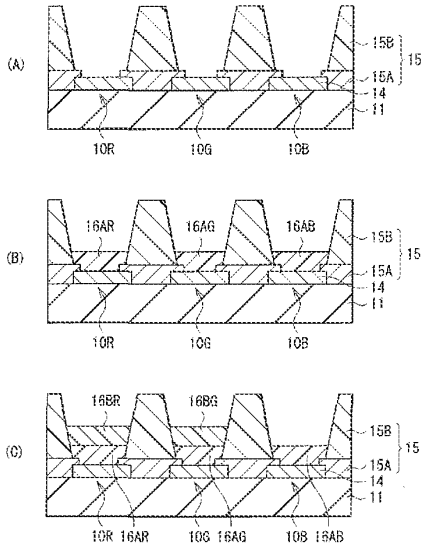
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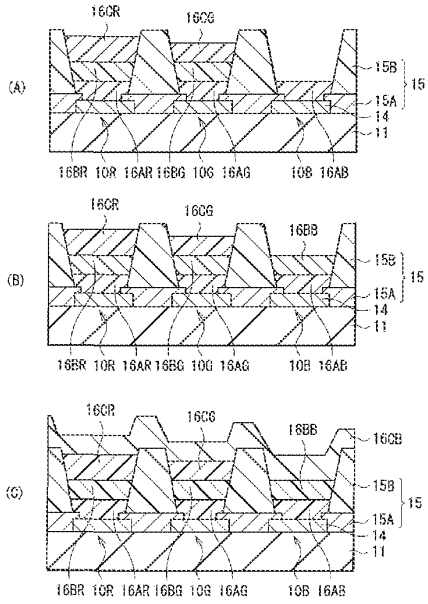
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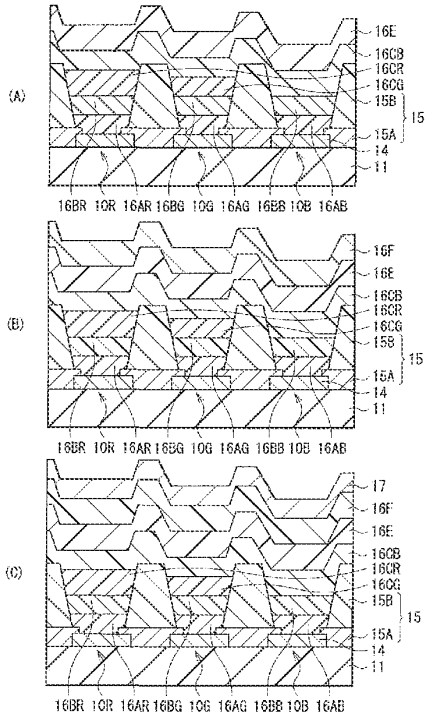
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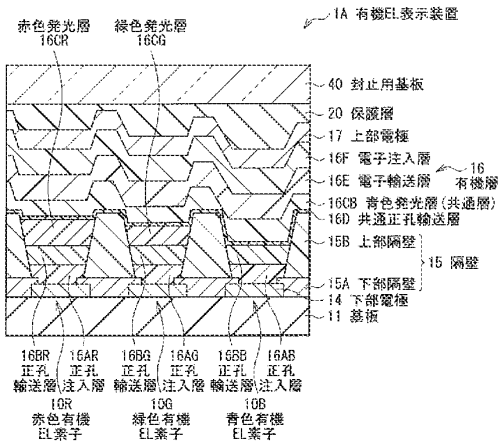
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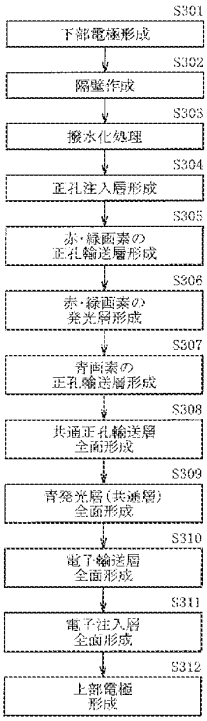
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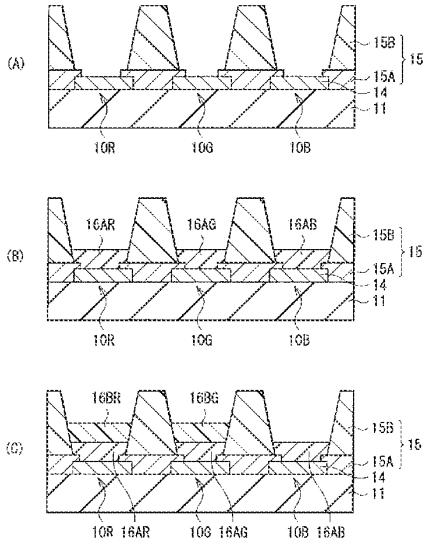
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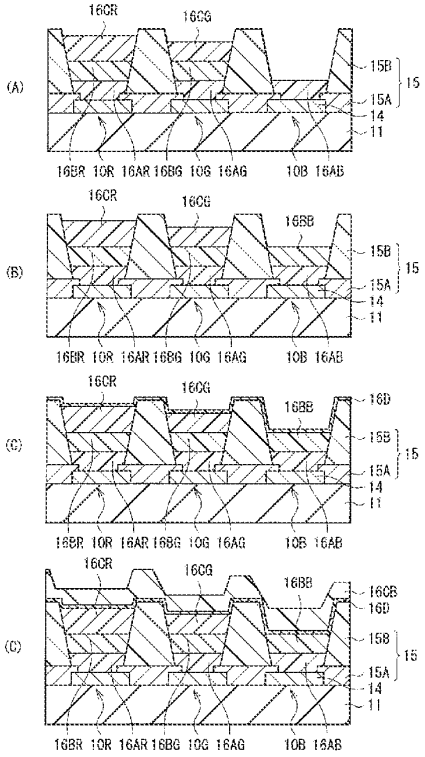
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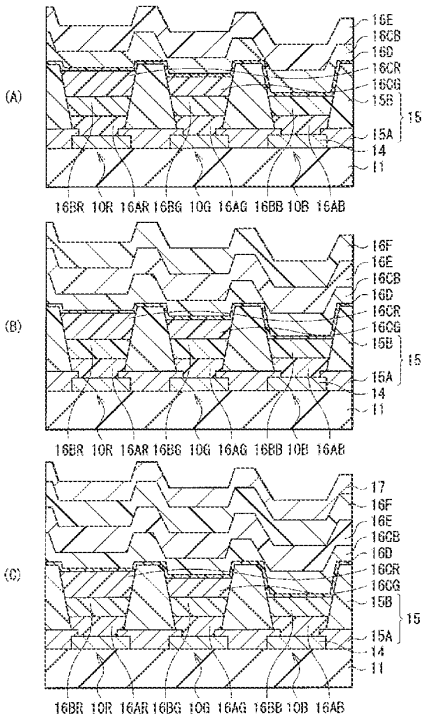
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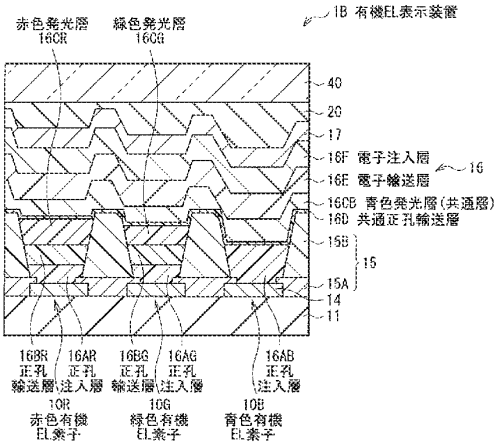
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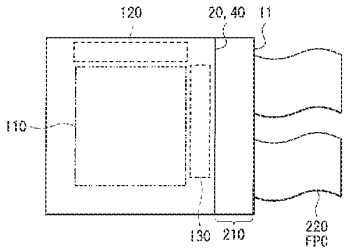
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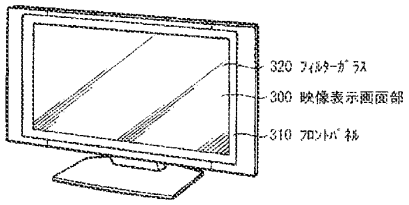
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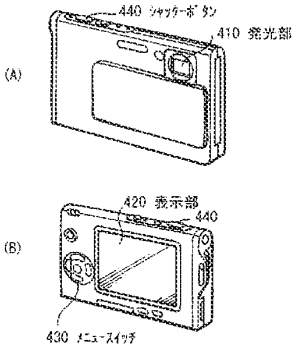
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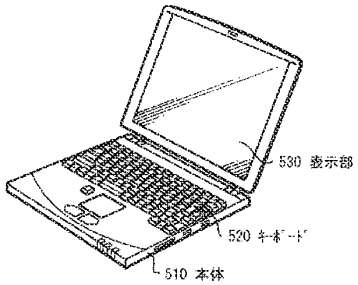
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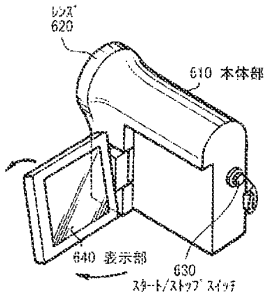
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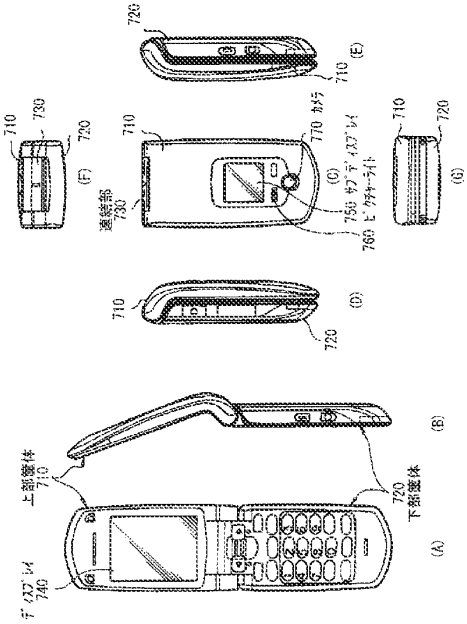
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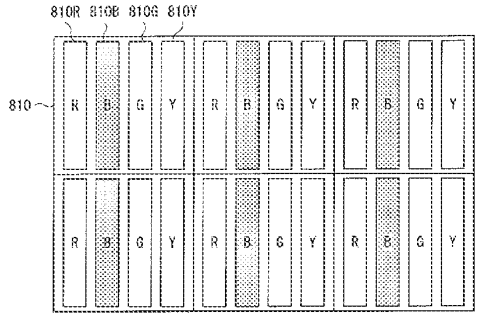
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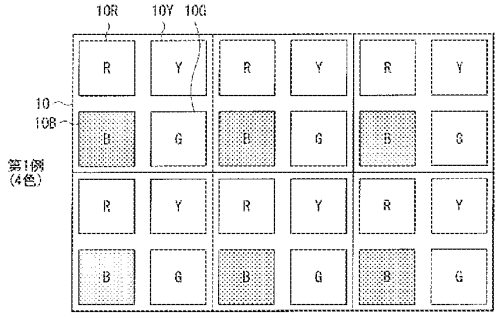
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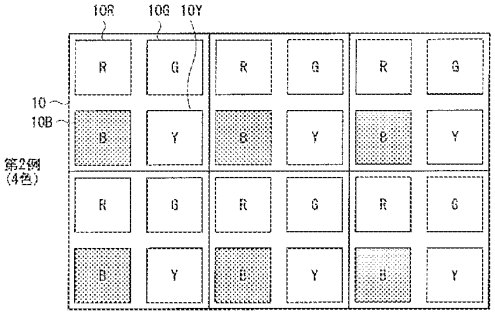
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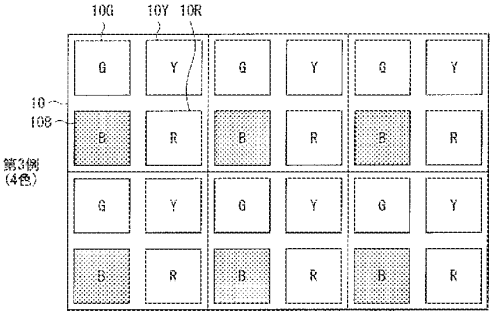
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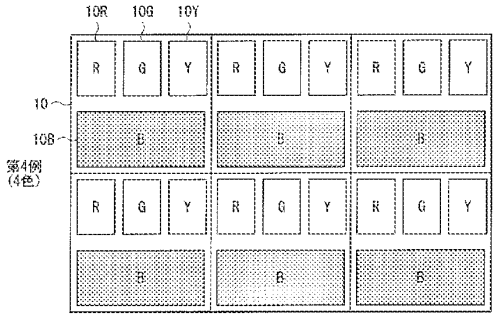
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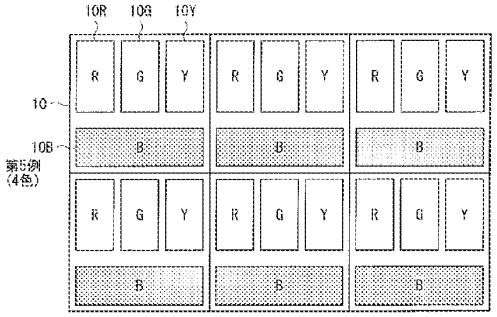
【図３４】



【図３５】



【図３６】



フロントページの続き

Fターム(参考) 3K107 AA01 BB01 CC06 CC45 DD51 DD71 DD72 DD78 DD79 DD87
EE06 EE07 FF14 FF15 GG06 GG07 GG08

Espacenet

Bibliographic data: JP2001076881 (A) — 2001-03-23

ORGANIC LIGHT-EMITTING DEVICE AND MANUFACTURE THEREFOR

Inventor(s): FUJITA YOSHIMASA ± (FUJITA YOSHIMASA)

Applicant(s): SHARP KK ± (SHARP CORP)

Classification: - **international:** ***H01L51/50; H05B33/10; H05B33/12; H05B33/14; H05B33/22;*** *H01L27/32;* (IPC1-7): H05B33/22
- **cooperative:** **H01L27/3246 (US);** H01L27/3246 (EP)

Application number: JP19990253541 19990907

Priority number(s): JP19990253541 19990907

Abstract of JP2001076881 (A)

PROBLEM TO BE SOLVED: To enhance a display quality by the emitting light, and to restrain the degradation with the lapse of time by forming a barrier rib vicinal surface of a recessed cross-sectional shape in an organic layer of at least one layer. SOLUTION: This organic light-emitting device 10 is formed by laminating a polarizing plate 7, a base board 1, a first electrode 2, an organic layer 3, a second electrode 4 and a sealing film 6 in this order, and at least a barrier rib 5 is formed in a part on the periphery of the organic layer 3 to form one picture element. One layer in at least the organic layer 3 is formed by solidifying a recessed meniscus when injecting an organic layer forming painting liquid. The barrier rib 5 has critical surface tension larger than surface tension at 20 deg.C of the organic layer forming painting liquid injected inside, and this painting liquid is formed of an inorganic material and an organic material such as forming the recessed meniscus by wetting the inside of the barrier rib 5. A difference between the critical surface tension of a material of such a barrier rib 5 and surface tension of the organic layer forming painting liquid is desirably 5 dyne/cm or more (20 deg.C).

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号
特開2001－76881
（P2001－76881A）
(43)公開日　平成13年３月23日(2001.3.23)

(51)Int.Cl.[7]	識別記号	ＦＩ		ﾃｰﾏｺｰﾄﾞ(参考)
Ｈ０５Ｂ　33/22		Ｈ０５Ｂ　33/22	Ｚ	３Ｋ００７
33/10		33/10		
33/12		33/12	Ｂ	
33/14		33/14	Ａ	

審査請求　未請求　請求項の数９　ＯＬ　（全 10 頁）

(21)出願番号　特願平11－253541

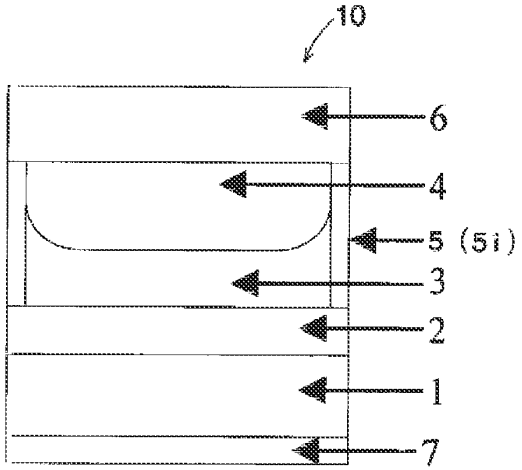
(22)出願日　平成11年９月７日(1999.9.7)

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大阪府大阪市阿倍野区長池町22番22号　シャープ株式会社内
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弁理士　野河　信太郎

Ｆターム(参考)　3K007 AB03 AB15 AB17 AB18 BA00 BB00 BB01 CA01 CA02 CA05 CB01 DA00 DB03 EB00 FA00 FA01

(54)【発明の名称】　有機発光素子及びその製造方法

(57)【要約】
【課題】　発光による表示の品質が高く、かつ経時的劣化が抑制され、製造が容易な有機発光素子及びその製造方法を提供する。
【解決手段】　有機発光素子は、第１電極と、第１電極上に形成され、少なくとも隣接する画素間の一部を区画する隔壁と、隔壁の内側に形成された有機層と、有機層上に形成された第２電極とを有し、少なくとも１層の有機層は、隔壁近傍の表面が、凹状の断面形状からなる。



【特許請求の範囲】
【請求項１】　第１電極と、第１電極上に形成され、少なくとも隣接する画素間の一部を区画する隔壁と、隔壁の内側に形成された有機層と、有機層上に形成された第２電極とを有する有機発光素子において、
少なくとも１層の有機層は、隔壁近傍の表面が、凹状の断面形状からなることを特徴とする有機発光素子。
【請求項２】　有機層は、有機発光材料および／または有機電荷輸送材料を含む溶液または分散液を隔壁の内側に注入した際の凹状のメニスカスが固化されて形成される請求項１に記載の有機発光素子。
【請求項３】　少なくとも隣接する画素間の一部を区画する隔壁を第１電極上に形成し、有機発光材料を含む溶液または分散液を隔壁の内側に注入して有機層を形成し、次いでこの有機層上に第２電極を形成する工程を有する有機発光素子の製造方法において、
隔壁の２０℃における臨界表面張力が、隔壁の内側に注入する有機発光材料を含む溶液または分散液の２０℃における表面張力よりも大きいことを特徴とする有機発光素子の製造方法。
【請求項４】　隔壁の２０℃における臨界表面張力と有機発光材料を含む溶液または分散液の２０℃における表面張力の差が、少なくとも５dyne/cm 以上である請求項３記載の有機発光素子の製造方法。
【請求項５】　隔壁が、さらに、第１電極から遠位の上部隔壁を重畳してなり、上部隔壁の２０℃における臨界表面張力が、有機発光材料を含む溶液または分散液の２０℃における表面張力よりも小さいことを特徴とする請求項３または４に記載の有機発光素子の製造方法。
【請求項６】　上部隔壁の２０℃における臨界表面張力と有機発光材料を含む溶液または分散液の２０℃における表面張力の差が、少なくとも５dyne/cm 以上である請求項５記載の有機発光素子の製造方法。
【請求項７】　第１電極の２０℃における臨界表面張力が、有機発光材料を含む溶液または分散液の２０℃における表面張力よりも大きい請求項３～６のいずれか一つに記載の有機発光素子の製造方法。
【請求項８】　第１電極の２０℃における臨界表面張力と有機発光材料を含む溶液または分散液の２０℃における表面張力の差が、少なくとも５dyne/cm 以上である請求項７記載の有機発光素子の製造方法。
【請求項９】　少なくとも１層の有機層が、有機発光材料を含む溶液または分散液からスピンコート法、印刷法、インクジェット法あるいはノズル噴射法から選択されるいずれかの注入方法を用いて形成される請求項３～８のいずれか一つに記載の有機発光素子の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、ディスプレイの画素として使用される有機発光素子及びその製造方法に関する。
【０００２】
【従来の技術】従来、湿式法による有機発光素子の形成には、スピンコート法、ディップ法、ドクターブレード法等の塗布法が用いられていたが、これらの方法では、発光層のパターニングによって画素をカラー化することは非常に困難であった。しかし、近年、この問題に対する一つの解決法として、発光層を、インクジェット法（特開平１０－１２３７７、Appl.Phys.Lett. No.72, 519頁,1998 年）、印刷法等の湿式法によりパターン化して形成する方法が提案されている。
【０００３】
【発明が解決しようとする課題】しかし、湿式法による画素のカラー化に際しては、発光層形成時に各色の発光層が混じり合って混色したり、あるいはエネルギー移動に伴ってエネルギーの高い色が発光しない現象が生じたりして、表示品質を低下させるという問題がある。この現象を防止するため、樹脂ブラックレジスト（特開平１０－１５３９６７号公報、特開平１１－４０３５８号公報、特開平１１－５４２７０号公報）等の隔壁で、あるいは撥水撥油性のバンク（特開平１１－８７０６２号公報）等の隔壁で各画素を囲む方法が提案されている。
【０００４】有機発光素子の一例を図7に示す。有機発光素子（有機ＬＥＤ媒体）１１０は、偏向板１０７、基板１０１、陽極１０２、有機層１０３及び陰極１０４が、この順に積層されてなり、隔壁１０５が有機層１０３の周囲を取り囲み、１つの画素（ピクセル）を形成する。有機層１０３は、陽極１０２上に隔壁１０５を形成した後、有機発光材料および／または有機電荷輸送材料を含む溶液あるいは分散液（以下、「有機層形成用塗液」と略称する）を隔壁１０５の内側に注入することにより形成される。陰極１０４は、有機層１０３上に直接、あるいはさらに有機層を形成した上に（図示せず）蒸着等により形成される。
【０００５】有機発光材料は、通常、有機高分子材料あるいは有機低分子材料からなり、これらの溶液あるいは分散液を隔壁１０５の内側に注入する際、これらの液が隔壁１０５の内側をぬらさないので、有機層１０３のメニスカスは凸状となる。この場合、有機層形成用塗液の表面張力γと隔壁１０５の臨界表面張力γｃは、γｃ＜γの関係となる。このような有機層形成用塗液を固化して有機層１０３が形成された有機発光素子１１０に電圧を印加すると、有機層１０３の最も薄い部分、つまり、有機層１０３と隔壁１０５が接する界面部分が強く発光し、ディスプレイとしての表示品質が低下する。さらに、局所的に電界が集中するので、有機層１０３の劣化の原因にもなる。
【０００６】図8は、上記の問題を解決するために、有機層１０３の比較的平坦な中央部分に陰極１０４を形成した有機発光素子１２０を示す。有機発光素子１２０で

は、陰極１０４が隔壁１０５から離れて形成されているので、有機層１０３と隔壁１０５が接する界面部分での発光を抑えることができるが、これによって開口率が低下する。また、シャドウマスク等を用いてパターン化した陰極１０４を形成する際に、陰極１０４の形成が有機層１０３の中央部分に限定されるので、シャドウマスクの位置合わせが困難になる。

【０００７】本発明は、上記の問題点に鑑みてなされたものであり、発光による表示の品質が高く、かつ経時的劣化が抑制され、製造が容易な有機発光素子及びその製造方法を提供する。

【０００８】

【課題を解決するための手段】本発明によれば、第１電極と、第１電極上に形成され、少なくとも隣接する画素間の一部を区画する隔壁と、隔壁の内側に形成された有機層と、有機層上に形成された第２電極とを有する有機発光素子において、少なくとも１層の有機層は、隔壁近傍の表面が、凹状の断面形状からなることを特徴とする有機発光素子が提供される。

【０００９】すなわち、本発明者らは、隔壁に対する有機層形成用塗液の「ヌレ性」の度合いに着目し、少なくとも１層の有機層の断面形状が、隔壁近傍の表面において凹状となるよう、有機層形成用塗液及び隔壁の双方をそれぞれの材料面から鋭意検討を行った。その結果、有機層が、有機層形成用塗液を隔壁の内側に注入した際の凹状のメニスカスが固化されて形成される有機発光素子を得る手法を完成するに至った。本発明により、有機層と隔壁との界面での局所発光及びこの局所発光に伴う経時的劣化が抑制された有機発光素子ならびにシャドウマスク等により有機層の表面に電極を形成する際に、シャドウマスクの位置合わせが容易となる有機発光素子の製造方法を完成するに至った。このような有機発光素子を用いることにより、表示品質が優れ、かつ開口率の高い有機発光ディスプレイを提供できる。

【００１０】この発明の別の観点によれば、少なくとも隣接する画素間の一部を区画する隔壁を第１電極上に形成し、有機発光材料を含む溶液または分散液を隔壁の内側に注入して有機層を形成し、次いでこの有機層上に第２電極を形成する工程を有する有機発光素子の製造方法において、隔壁の２０℃における臨界表面張力が、隔壁の内側に注入する有機発光材料を含む溶液または分散液の２０℃における表面張力よりも大きいことを特徴とする有機発光素子の製造方法が提供される。

【００１１】この発明における画素とは、単色またはゾーンカラーのディスプレイの場合にはピクセルを意味し、マルチカラー、フルカラーディスプレイの場合にはサブピクセルを意味する。画素の形状は特に限定されないが、多角形状、円形状、楕円形状が例示される。画素の角部まで均一な膜を形成するためには、俯瞰したときに、画素の角部が中心に向かって凹状をなす円弧状のものが好ましい。

【００１２】この発明におけるメニスカスとは、隔壁の近傍における有機層形成用塗液の自由表面であって、有機層形成用塗液が隔壁をぬらす場合、すなわち、有機層形成用塗液の隔壁に対する付着力が大なる場合には、凹状のメニスカスとなり、有機層形成用塗液が隔壁をぬらさない場合、すなわち、有機層形成用塗液の隔壁に対する付着力が小なる場合には、凸状のメニスカスとなる。

【００１３】この発明における臨界表面張力とは、固体の表面における液体の「ヌレ性」の度合いを規定する「ジスマン（Zisman）の臨界表面張力」を意味する。すなわち、低エネルギー表面をもつ大部分の有機高分子や有機化合物等の固体の表面上に、種々の表面張力をもつ極性の有機液体や飽和炭化水素、水等を滴下し、それらの接触角θを測定し、これらの$\cos\theta$をそれぞれの液体の表面張力γ〔dyne/cm〕に対してプロットし、得られた近似直線が接触角$\theta=0°$の水平線と交わる点の表面張力の値γc〔dyne/cm〕が、この発明における臨界表面張力となる。この発明における有機層形成用塗液の表面張力とは、液体が単位面積〔cm^2〕の表面をつくるための仕事〔erg〕として表示される表面張力の値γ〔dyne/cm〕を意味する。

【００１４】隔壁の内側壁面の２０℃における臨界表面張力と有機層形成用塗液の２０℃における表面張力の差が、５dyne/cm以上あれば、前記の問題点を解消するのに充分な凹状のメニスカスを隔壁内側の近傍表面に形成することができる。隔壁が、さらに、第１電極から遠位の上部隔壁を重畳してなり、上部隔壁の内側壁面の臨界表面張力が、有機層形成用塗液の表面張力よりも小さくなるよう構成することにより、有機層形成用塗液を隔壁の内側に注入する際に、上部隔壁の内側壁面が有機層形成用塗液に対して撥水性または撥油性となるので、すなわち、有機層形成用塗液が上部隔壁の内側をぬらさないので、有機層形成用塗液が隔壁を伝って隣接する画素にまたがることがなく、画素間における短絡を防止できる。また、隣接する画素の有機層形成用塗液による汚染が防止されるので、混色等の問題も回避できる。また、上部隔壁の内側壁面の２０℃における臨界表面張力と有機層形成用塗液の２０℃における表面張力の差が、５dyne/cm以上あれば、有機層形成用塗液が隔壁を伝って隣接する画素にまたがることがなく、上部隔壁の効果を充分に発揮させることができる。

【００１５】第１電極の２０℃における臨界表面張力が、有機層形成用塗液の２０℃における表面張力よりも大きくなるよう構成することにより、電極に対する有機層形成用塗液のヌレ性が向上し、隔壁の内側の角部および隅部にまで有機層形成用塗液を充満させることができる。第１電極の２０℃における臨界表面張力と有機層形成用塗液の２０℃における表面張力の差が、５dyne/cm以上あれば、電極に対する有機層形成用塗液のヌレ性が

向上し、より有効な有機層を形成できる。その結果、有機層形成時に電極と有機層の密着性が向上し、電極から有機層への電荷の注入効率が向上する。

【００１６】有機層形成用塗液を隔壁の内側へ注入する方法としては、スピンコート法、印刷法、インクジェットヘッドから有機層形成用塗液を吐出するインクジェット法あるいはノズル又はニードルから有機層形成用塗液を吐出するノズル噴射法等の公知の方法を採用できる。

【００１７】

【発明の実施の形態】以下、図１から図６を参照して、本発明の有機発光素子及びその製造方法の実施の形態を説明するが、この実施の形態によって本発明は限定されない。図１に、本発明の有機発光素子の基本的な構造を示す。図１において、有機発光素子１０は、偏向板７、基板１、第１電極２（陽極）、有機層３、第２電極４（陰極）及び封止膜６が、この順に積層されてなり、少なくとも隔壁５が有機層３の周囲の一部に形成され、１つの画素（ピクセル）を形成する。少なくとも有機層３のうちの１層は、有機層形成用塗液を注入した際の凹状のメニスカスが固化されて形成される。基板１としては、石英基板、ガラス基板、プラスチック基板等が使用される。

【００１８】第１電極２及び第２電極４は、陽陰両極を形成する電極対であり、基板１及び第１電極２が透明である場合は、有機層３からの発光が基板１側から出射されるので、発光効率を高めるためには、第２電極４が反射電極であること、あるいは第２電極４の有機層３と隣接しない側に反射膜を有することが好ましい。逆に、第２電極４を透明材料で構成して、有機層３からの発光を第２電極４側から出射させることもできる。この場合には、第１電極２が反射電極であること、基板１が反射基板であること、あるいは第１電極２と基板１との間に反射膜を有することが好ましい。

【００１９】透明電極としては、ＣｕＩ、ＩＴＯ、SnO_2、ＺｎＯ、$CuAlO_2$等の透明電極が使用される。また、反射電極としては、アルミニウム、カルシウム等の金属、マグネシウム－銀、リチウム－アルミニウム等の合金、マグネシウム／銀等の金属同士の積層膜、フッ化リチウム／アルミニウム等の絶縁体と金属との積層膜等が使用される。偏向板７は、ディスプレイにおける良好なコントラストを得るために基板１の外側に設けられる。封止膜６（または封止基板）は、第２電極４の損傷あるいは有機層及び電極の劣化を防止するために設けられる。

【００２０】隔壁５は、隔壁５の内側に注入される有機層形成用塗液の２０℃における表面張力よりも大きい臨界表面張力を有し、有機層形成用塗液が隔壁５の内側をぬらすことによって、凹状のメニスカスが形成されるような無機材料もしくは有機材料で形成される。したがって、隔壁５は、有機層形成用塗液の表面張力との関係でその材料が選択される。隔壁５を形成するための好ましい材料を以下に列挙する。なお（　）内は、２０℃における隔壁材料の臨界表面張力の値γｃ〔dyne/cm〕を示す。

【００２１】隔壁５を形成するための好ましい材料としては、例えば、ポリ６フッ化プロピレン（γｃ＝１６dyne/cm）、ポリ４フッ化エチレン（γｃ＝１８dyne/cm）、ポリ３フッ化エチレン（γｃ＝２２dyne/cm）、ポリフッ化ビニリデン（γｃ＝２５dyne/cm）、ポリエチレン（γｃ３１dyne/cm）、ポリブタジエン（γｃ＝３１dyne/cm）、ポリスチレン（γｃ＝３３dyne/cm）、ポリアクリル酸エチル（γｃ＝３５dyne/cm）、ポリビニルアルコール（γｃ＝３７dyne/cm）、クロロプレン（γｃ＝３８dyne/cm）、ポリ塩化ビニル（γｃ＝３９dyne/cm）、ポリアクリル酸メチル（γｃ＝３９dyne/cm）、ポリ塩化ビニリデン（γｃ＝４０dyne/cm）、６ナイロン（γｃ＝４２dyne/cm）、６－６ナイロン（γｃ＝４２dyne/cm）、７－７ナイロン（γｃ＝４３dyne/cm）、ポリエチレンテレフタレート（γｃ＝４３dyne/cm）、ポリヘキサメチレンアジパミド（γｃ＝４６dyne/cm）、ガラス（γｃ＝５５dyne/cm）等が挙げられる。また、ポジ型レジスト中に、信越化学社製のＫＢＭ７１０３（γｃ＝２０dyne/cm）を混合したものも好ましい材料として挙げられる。

【００２２】あるいは、これらの材料を用いて隔壁５を形成した後、プラズマ処理、ＵＶ処理、ガス処理等を行うことにより、隔壁５の表面の臨界表面張力γｃの値を制御してもよい。隔壁５は、上記のような材料を使用すること、あるいは上記のような処理を施すことにより、隔壁５が構成されるが、より有効な凹状のメニスカスを形成するには、隔壁５の材料の臨界表面張力γｃと、後述する有機層３となる有機層形成用塗液の表面張力γの差が、少なくとも５dyne/cm以上であることが好ましい。

【００２３】図２は、第１隔壁５１と第２隔壁５２とからなる隔壁５の構成例を示す。ここでは、隔壁５が、第１隔壁５１（下部隔壁）に第１電極２から遠位の第２隔壁５２（上部隔壁）を重畳してなり、第２隔壁５２の内側壁面の２０℃における臨界表面張力$\gamma c_{(52)}$が、有機層形成用塗液の２０℃における表面張力γよりも小さくなるように構成されている。なお、第１隔壁５１の材料は、前記の隔壁５の材料と同様である。第２隔壁５２の材料は、第１隔壁５１を形成する前記のような材料を用いることができるが、第２隔壁５２の内側壁面の２０℃における臨界表面張力$\gamma c_{(52)}$と有機層形成用塗液の２０℃における表面張力γが$\gamma c_{(52)} < \gamma$の関係を満たすべく、第１隔壁５１の内側壁面の２０℃における臨界表面張力$\gamma c_{(51)}$よりもさらに小さい臨界表面張力γｃの値を有する材料の使用が好ましい。あるいは、これらの材料を用いて第２隔壁５２を形成した後、プラズマ処

理、ＵＶ処理、ガス処理等を行うことにより、第２隔壁５２の表面の臨界表面張力γｃの値を制御してもよい。第２隔壁５２の２０℃における臨界表面張力γｃと有機層形成用塗液の２０℃における表面張力γの差が、少なくとも５dyne/cm 以上であれば、有機層形成用塗液による第２隔壁５２の内側壁面のヌレを有効に防ぐことができる。

【００２４】第１隔壁５１及び第２隔壁５２は、少なくとも画素間の一部に形成されていればよく、これら隔壁５１及び５２の構造は、それぞれの隔壁を重ねた多層構造であってもよく、有機層形成用塗液の溶媒に対して不溶もしくは難溶であることが好ましい。また、ディスプレイとしての表示品質を上げるために、ブラックマトリックス用の材料を用いることが好ましい。第１隔壁５１及び第２隔壁５２の断面形状は、特に限定されないが、特開平１１－８７０６３号公報に開示されているような逆テーパー状の断面形状にすることにより、陰極のパターニングを行ってもよい。

【００２５】有機層３は、少なくとも１層の有機層を有する構造であって、有機層のみからなる単層構造、あるいは、電荷輸送層と有機層との多層構造であってもよい。電荷輸送層と有機層との多層構造とする場合には、電荷輸送層及び有機層を各一層ずつとしてもよいし、上記の各層を複数ずつ用いてもよい。また、有機層３を、複数層の有機層からなる多層構造とする場合には、有機層の少なくとも一層が湿式法により形成されていることが必要である。このとき、他の有機層は湿式法により形成されていてもよいし、真空蒸着法等のドライプロセスにより形成されてもよい。

【００２６】有機層３は、少なくとも一層が塗液（有機層形成用塗液）の状態から薄膜を形成できる湿式法によるものであれば、材料は特に限定されない。湿式法としては、例えば、スピンコート法、印刷法、ディップ法、ドクターブレード法、電着法、インクジェットヘッド、ノズル、またはニードルから液を吐出する方法等、各種の薄膜形成方法があるが、後述するように、使用する方法によって適する材料（有機層形成用塗液）は若干異なる。しかし、有機層形成用塗液の２０℃における表面張力γが、第１隔壁５１の２０℃における臨界表面張力γｃより小さく、さらには電極２の２０℃における臨界表面張力γｃより小さいことが条件となる。

【００２７】湿式法で用いられる有機層形成用塗液は、発光層形成用塗液と電荷輸送層形成用塗液に分けることができる。発光層形成用塗液としては、有機ＬＥＤ用の公知の高分子発光材料、例えば、ポリ〔２－デシルオキシ－１，４－フェニレン〕（ＤＯ－ＰＰＰ）、ポリ〔２，５－ビス〔２－（Ｎ，Ｎ，Ｎ－トリエチルアンモニウム）エトキシ〕－１，４－フェニレン－アルト－１，４－フェニレン〕ジブロマイド（ＰＰＰ－ＮＥｔ$_8^+$）、ポリ〔２－（２’－エチルヘキシルオキシ）－５－メトキシ－１，４－フェニレンビニレン〕（ＭＥＨ－ＰＰＶ）、ポリ〔５－メトキシ－（２－プロパノキシサルフォニド）－１，４－フェニレンビニレン〕（ＭＰＳ－ＰＰＶ）、ポリ〔２，５－ビス（ヘキシルオキシ）－１，４－フェニレン－（１－シアノビニレン）〕（ＣＮ－ＰＰＶ）等を、溶解あるいは分散させた塗液、もしくは、有機ＬＥＤ用の公知の低分子発光材料、例えばテトラフェニルブタジエン（ＴＰＢ）、クマリン、ナイルレッド、オキサジアゾール誘導体等と、公知の高分子材料、例えばポリカーボネート（ＰＣ）、ポリメタクリル酸メチル（ＰＭＭＡ）、ポリビニルカルバゾール（ＰＶＣｚ）等を溶解もしくは分散させた塗液を用いることができる。また、これらの塗液には、必要に応じてｐＨ調整用、粘度調整用、充満促進用、レベリング用、表面張力調整用等の添加剤、有機ＬＥＤ用及び有機光導電体用の公知のホール輸送材料（例えば前記のＮ，Ｎ’－ビス－（３－メチルフェニル）－Ｎ，Ｎ’－ビス－（フェニル）－ベンジジン（ＴＰＤ）、Ｎ，Ｎ’－ジ（ナフタレン－１－イル）－Ｎ，Ｎ’－ジフェニル－ベンジジン（ＮＰＤ）等）、電子輸送材料（例えば、３－（４－ビフェニルイル－４－フェニレン－５－ｔ－ブチルフェニル－１，２，４－トリアゾール（ＴＡＺ）、トリス（８－ヒドロキシキノリノナト）アルミニウム（Ａｌｑ$_3$）等）等の電荷輸送材料、アクセプター、ドナー等のドーパント等を添加してもよい。

【００２８】電荷輸送層形成用塗液としては、有機ＬＥＤ用、有機光導電体用の公知の高分子電荷輸送材料（例えば、ポリアニリン（ＰＡＮＩ）、３，４－ポリエチレンジオキシチオフェン（ＰＥＤＴ）、ポリ〔トリフェニルアミン誘導体〕（Ｐｏｌｙ－ＴＰＤ）、ポリ〔オキサジアゾール誘導体〕（Ｐｏｌｙ－ＯＸＺ等）、前記ＰＶＣｚを溶解もしくは分散させた塗液、もしくは、有機ＬＥＤ用、有機光導電体用の公知の低分子電荷輸送材料（例えば、前記のＴＰＤ、ＮＰＤ、オキサジアゾール誘導体等）と公知の高分子材料（例えば、前記のＰＣ、ＰＭＭＡ、ＰＶＣｚ等）を溶解もしくは分散させた塗液を用いることができる。また、これらの液に、必要に応じてｐＨ調整用、粘度調整用、充満促進用、レベリング用、表面張力調整用等の添加剤、アクセプター、ドナー等のドーパント等を添加してもよい。

【００２９】また、インクジェット法を用いる場合には、前記の高分子材料を溶解もしくは分散させる溶媒として、従来の溶媒を用いることができるが、これらの溶媒中には、低蒸気圧の溶剤、例えばエチレングリコール、プロピレングリコール、トリエチレングリコール、エチレングリコールモノメチルエーテル、エチレングリコールモノエチルエーテル、トリエチレングリコールモノメチルエーテル、トリエチレングリコールモノエチルエーテル、グリセリン、ホルムアミド、Ｎ－メチル－２－ピロリドン、シクロヘキサン、１－プロパノール、オ

クタン、ノナン、デカン等が含まれることが好ましい。固形分と溶媒の混合比率は、塗液の２０℃における粘度が１０ｍＰａ・ｓ以下になるように調整することが好ましく、また、表面張力γを少なくとも３０dyne/cm 以上になるように調整することが好ましい。

【００３０】また、従来のドライプロセス、例えば、抵抗加熱蒸着法、ＥＢ蒸着法、イオンプレーティング法等で有機層３中の他の有機層を電極２及び４間に形成することもできる。ドライプロセスで使用できる有機発光材料としては、有機ＬＥＤ用の公知の発光材料が使用可能であり、有機発光材料のみから構成されてもよいし、添加剤等を含有していてもよい。また、電荷輸送材料としては、有機ＬＥＤ用、有機光導電体用の公知の材料が使用可能であり、電荷輸送材料のみから構成されてもよいし、添加剤等を含有していてもよい。

【００３１】次に、図３の平面図を参照しながら有機発光素子１０を複数配置して有機ＬＥＤディスプレイを形成するための有機層３の配置について説明する。有機層３には、赤色（Ｒ）発光画素１１、緑色（Ｇ）発光画素１２及び青色（Ｂ）発光画素１３の３種類があり、本発明の有機ＬＥＤディスプレイ２０は、これら３種類の有機層３を所定の配置パターンで、マトリックス状に配置して構成される。

【００３２】図３（ａ）は、上記した各色の発光画素がストライプ状に配列されてなる。図３（ｂ）は、上記した各色の発光画素が隔壁５の角で隣接した斜行ストライプ状に配列されてなる。図３（ｃ）は、有機層３（隔壁５）が蛇行し、かつ上記した各色の発光画素が千鳥状に配列されてなる。これらの発光画素の配列において、図３（ｄ）に示すように、赤色（Ｒ）発光画素１１、緑色（Ｇ）発光画素１２及び青色（Ｂ）発光画素１３の配列数は、必ずしも、１：１：１の比でなくともよい。また、各画素の面積は、同一であってもよいし、各画素で異なっていてもよい。また、３種類（３色）でなく、１種類（１色）であってもよい。

【００３３】次に、図４及び図５の平面図を参照しながら各画素に対応した第１電極２どうしと第２電極４どうしの接続方法について説明する。本発明の有機ＬＥＤディスプレイ２０は、図４に示すように、有機層３を挟持する第１電極２と第２電極４が共通の基板１上で互いに直交する斜行ストライプ状の電極構成としてもよい。また、図５に示すように、第１電極２あるいは第２電極４が、所定のソースバスライン２２及びゲートバスライン２３で接続される薄膜トランジスタ２１（ＴＦＴ）を介して共通の電極に接続していてもよい。ただし、ここで１画素に用いるＴＦＴは、１つでもよいし、複数個でもよい。

【００３４】

【実施例】以下、実施の形態の具体例を示すが、これらの実施例により本発明が限定されるものではない。

実施例１

まず、１３０ｎｍの膜厚をもつＩＴＯ付きガラス基板１を、フォトリソグラフィ法により第１電極２として２４０μｍピッチで２００μｍ幅のＩＴＯ透明ストライプ電極を形成した。次に、ＩＴＯ付きガラス基板１を、例えばイソプロピルアルコール、アセトン、純水を用いた従来のウェットプロセスによる洗浄法及びＵＶオゾン処理、プラズマ処理等の従来のドライプロセスにより洗浄する。このとき、ＩＴＯ表面の臨界表面張力γｃは、５６dyne/cm であった。

【００３５】次に、この基板１上に臨界表面張力γｃが３８dyne/cm のポリイミドからなるレジストをスピンコート法により塗布し、膜厚３０μｍのレジスト膜を形成した。次に、マスクを用いて露光し、レジストの残渣を洗い流し、ＩＴＯと平行の方向には５４０μｍピッチ、ＩＴＯと直交する方向には２３０μｍピッチで、４０μｍ幅の第１隔壁５１を形成した。

【００３６】次に、この基板１をF_2含有ガスを用いて乾式親水化処理を行うことでＩＴＯ表面の臨界表面張力γｃを６１dyne/cm にし、第１隔壁５１の臨界表面張力γｃを６０dyne/cm とした。次に、市販のディスペンサーにより、表面張力γが３３dyne/cm の３，４－ポリエチレンジオキシチオフェン水溶液を用い、厚さ５０ｎｍの正孔注入層を形成した。

【００３７】次に、市販のディスペンサーにより、赤、緑、青色に発光する発光材料をパターニング塗布し、厚さ５０ｎｍの有機層３を形成した。ここで、赤色発光材料としては、シアノポリフェニレンビニレン前駆体、緑色発光材料としては、ポリフェニレンビニレン前駆体、青色発光材料として、ポリパラフェニレンを使用した。このとき、すべての有機層形成用塗液の表面張力γは、３８dyne/cm であった。ただし、シアノポリフェニレンビニレン前駆体とポリフェニレンビニレン前駆体に関しては、膜を形成後、Ａｒ雰囲気下で１５０℃、６時間の加熱処理を行うことで、それぞれをシアノポリフェニレンビニレンとポリフェニレンビニレンに変換した。

【００３８】次に、第２電極４として、厚さ０．２μｍ、幅５１０μｍ、ピッチ５４０μｍのシャドウマスクを用いて、ＡｌとＬｉを共蒸着することにより、ＡｌＬｉ合金電極を形成した。最後にエポキシ樹脂を用いて封止を行った。以上のようにして形成した有機ＬＥＤディスプレイは、第１電極２と第２電極４との間、第１電極２どうし及び第２電極４どうしでのショートは発生せず、また、有機層３及び電荷輸送層の膜厚の不均一に伴う画素部のエッジからの不均一発光は見られなかった。また、このディスプレイに３０Ｖのパルス電圧を印加することで、すべての画素から発光が得られた。

【００３９】実施例２

まず、１３０ｎｍの膜厚をもつＩＴＯ付きガラス基板１を、フォトリソグラフィ法により第１電極２として２４

０μｍピッチで２００μｍ幅のＩＴＯ透明ストライプ電極を形成した。次に、ＩＴＯ付きガラス基板１を、例えばイソプロピルアルコール、アセトン、純水を用いた従来のウエットプロセスによる洗浄法及びＵＶオゾン処理、プラズマ処理等の従来のドライプロセスにより洗浄する。このとき、ＩＴＯ表面の臨界表面張力γｃは、５６dyne/cm であった。

【００４０】次に、この基板１上に臨界表面張力γｃが４３dyne/cm のポリエチレンテレフタレートを用いてスピンコート法により膜厚０．１μｍのレジスト膜を形成した。次に、マスクを用いて露光し、レジストの残渣を洗い流し、ＩＴＯと平行の方向には３４０μｍピッチ、ＩＴＯと直交する方向には２３０μｍピッチで、４０μｍ幅の第１隔壁５１を形成した。次に、第１電極２上に臨界表面張力γｃ１５dyne/cm のパーフルオロオクチルエチルメタクリレートを用いてスピンコート法により膜厚２０μｍのレジスト膜を形成した。次に、第１電極２と同様のパターンのマスクを用いて露光し、レジストの残渣を洗い流し、ＩＴＯと平行の方向には５４０μｍピッチ、ＩＴＯと直交する方向には２３０μｍピッチで、４０μｍ幅の第２隔壁５２を形成した。

【００４１】次に、市販のスピンコーターにより、表面張力γが３３dyne/cm の３，４－ポリエチレンジオキシチオフェン水溶液を用い、厚さ５０ｎｍの正孔注入層を形成した。次に、市販のディスペンサーにより、赤、緑、青色に発光する発光材料をパターニング塗布し、厚さ５０ｎｍの発光層を形成した。ここで、赤色発光材料としては、シアノポリフェニレンビニレン前駆体、緑色発光材料としては、ポリフェニレンビニレン前駆体、青色発光材料としてポリパラフェニレンを使用した。このとき、すべての有機層形成用塗液の表面張力γは３８dyne/cm であった。ただし、シアノポリフェニレンビニレン前駆体とポリフェニレンビニレン前駆体に関しては、膜を形成後、Ａｒ雰囲気下で１５０℃、６時間の加熱処理を行うことで、それぞれをシアノポリフェニレンビニレンとポリフェニレンビニレンに変換した。

【００４２】次に、第２電極４として、厚さ０．２μｍ、幅５１０μｍ、ピッチ５４０μｍのシャドウマスクを用いて、ＡｌとＬｉを共蒸着することにより、ＡｌＬｉ合金電極を形成した。最後にエポキシ樹脂を用いて封止を行った。以上のようにして形成した有機ＬＥＤディスプレイは、第１電極２と第２電極４との間、第１電極２どうし及び第２電極４どうしでのショートは発生せず、また、有機層３及び電荷輸送層の膜厚の不均一に伴う画素部のエッジからの不均一発光は見られなかった。また、このディスプレイに３０Ｖのパルス電圧を印加することで、すべての画素から発光が得られた。

【００４３】実施例３

有機層形成用塗液の吐出方法として、ディスペンサーの代わりに、市販のインクジェットプリンターを用いたこと以外は、実施例２と同様にして有機ＬＥＤディスプレイを形成した。インクジェットプリンターによる有機層形成用塗液の吐出は、図６に示すように、所定の配置パターンでマトリックス状に形成された隔壁５の間隔に対応して３つのインクジェットヘッド２４を配置し、これらのインクジェットヘッド２４から赤色（Ｒ）発光画素１１、緑色（Ｇ）発光画素１２及び青色（Ｂ）発光画素１３を隔壁５の内側の第１電極２上に吐出させ、さらにこれらのインクジェットヘッド２４を平行移動させて前記した発光画素の吐出を繰り返して有機層３を形成した。形成された有機ＬＥＤディスプレイは、第１電極２と第２電極４との間、第１電極２どうし及び第２電極４どうしでのショートは発生せず、また、有機層３及び電荷輸送層の膜厚の不均一に伴う画素部のエッジからの不均一発光は見られなかった。また、このディスプレイに３０Ｖのパルス電圧を印加することで、すべての画素から発光が得られた。

【００４４】実施例４

まず、ガラス基板１上に、薄膜トランジスタを形成した後、第１電極２として、長辺が５００μｍで、短辺が２２０μｍになるようにＩＴＯ透明電極を形成した。このときＩＴＯ表面の臨界表面張力γｃは、５６dyne/cm であった。次に、この基板上に臨界表面張力γｃが４３dyne/cm のポリエチレンテレフタレートを用いてスピンコート法により膜厚０．１μｍのレジスト膜を形成した。次に、マスクを用いて露光し、レジストの残渣を洗い流し、ＩＴＯ間に４０μｍ幅の第１隔壁５１を形成した。

【００４５】次に、第１電極２上に臨界表面張力γｃが１５dyne/cm のパーフルオロオクチルエチルメタクリレートを用いてスピンコート法により膜厚２０μｍのレジスト膜を形成した。次に、第１電極２と同様のパターンのマスクを用いて露光し、レジストの残渣を洗い流し、ＩＴＯ間に４０μｍ幅の第２隔壁５２を形成した。次に、実施例２と同様にして有機層３を形成した。次に、ＡｌとＬｉを共蒸着することにより第２電極４として、ＡｌＬｉ合金電極を形成した。最後にエポキシ樹脂を用いて封止を行った。

【００４６】以上のようにして形成した有機ＬＥＤディスプレイは、第１電極２と第２電極４との間、第１電極２どうし及び第２電極４どうしでのショートは発生せず、また、有機層３及び電荷輸送層の膜厚の不均一に伴う各画素での発光の不均一は見られなかった。また、このディスプレイに３０Ｖのパルス電圧を印加することで、すべての画素から発光が得られた。

【００４７】

【発明の効果】本発明では、有機層と隔壁との界面での局所発光及びこの局所発光に伴う経時的劣化が抑制された有機発光素子ならびに、シャドウマスク等により有機層の表面に電極を形成する際に、シャドウマスクの位置合わせが容易となる有機発光素子の製造方法を提供でき

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る。また、表示品質が優れ、かつ開口率の高い有機発光ディスプレイを提供できる。

【００４８】また、発光層の混じり合いによる混色、または、発光層の混じり合いにより発光材料間に起こるエネルギー移動に伴うエネルギーの低い発光色の発光を抑え、表示品質を著しい低下を防止できる。さらに、シャドウマスクを用いて第２電極を形成した際に、シャドウマスクの密着による有機層へのダメージを防止することができる。この場合、隔壁の形状を適切な形、例えば、逆テーパー状とすることにより、シャドウマスクを用いなくても、第２電極のパターニングが可能となる。

【００４９】また、隣接する画素の材料による汚染を防止できるため、混色等の問題を排除することができる。また、２０℃における臨界表面張力γｃが、有機層形成用塗液の２０℃における表面張力γよりも大きい電極を用いることで、電極への有機層形成用塗液のヌレ性が高まり、画素の角部および隅部にまで有機層形成用塗液を充満させることが可能となり、画素の全域に均一な有機層を形成できる。また、有機層と電極との密着性が向上し、電極から有機層への電荷の注入効率が向上する。

【図面の簡単な説明】

【図１】本発明による有機発光素子の構成例を示す概略断面図である。

【図２】本発明による有機発光素子の他の構成例を示す概略断面図である。

【図３】本発明による有機ＬＥＤディスプレイの発光層の配置例を示す概略部分平面図である。

【図４】本発明による有機ＬＥＤディスプレイの電極の構成例を説明する概略部分透視平面図である。

【図５】図４に対応する、有機ＬＥＤディスプレイの電極の他の構成例を説明する概略部分透視平面図である。

【図６】本発明の有機層の形成方法の一例を説明する概念図である。

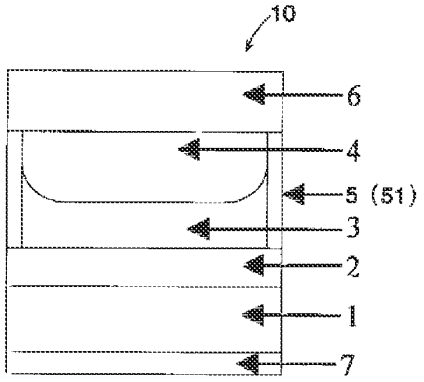
【図７】従来の有機発光素子の構成例を示す概略断面図である。

【図８】従来の有機発光素子の他の構成例を示す概略断面図である。

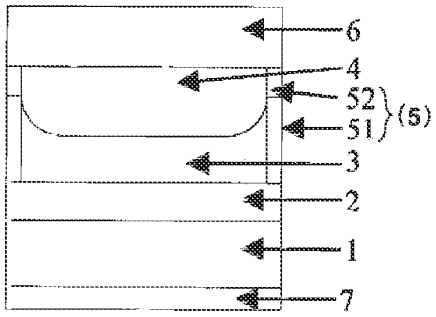
【符号の説明】

１　基板
２　第１電極
３　有機層
４　第２電極
５　隔壁
６　封止膜
７　偏向板
１０　有機発光素子
１１　赤色発光画素
１２　緑色発光画素
１３　青色発光画素
２０　有機ＬＥＤディスプレイ
２１　薄膜トランジスタ（ＴＦＴ）
２２　ソースバスライン
２３　ゲートバスライン
２４　インクジェットヘッド
５１　第１隔壁
５２　第２隔壁

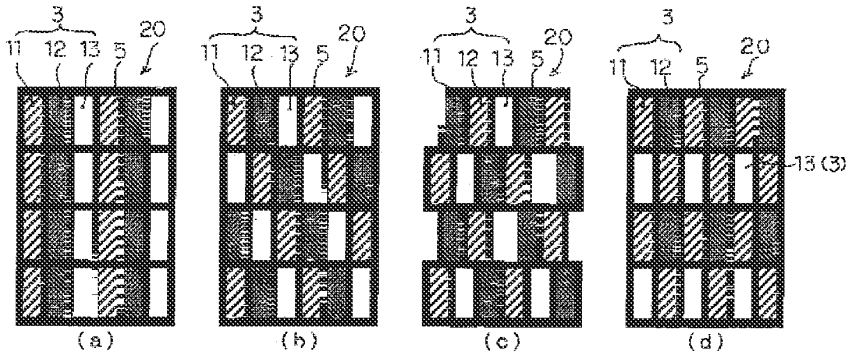
【図１】



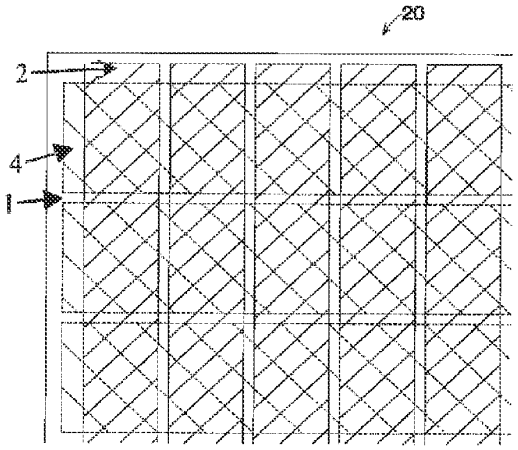
【図２】



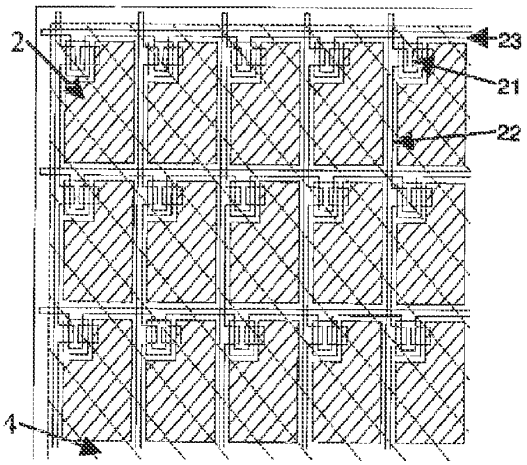
【図3】


3
11
12
13
5
20
(a)
(b)
(c)
(d)
13(3)

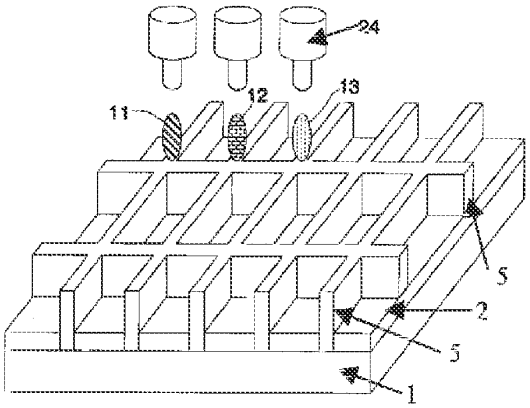
【図4】


20
2
4
1

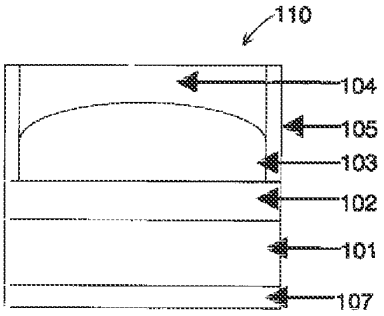
【図5】


2
23
21
22
4

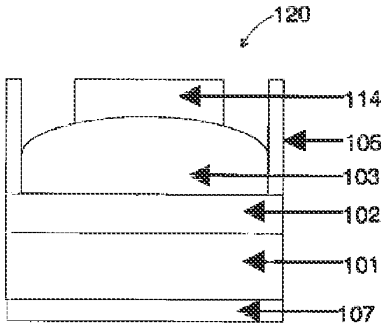
【図6】


24
11
12
13
5
2
5
1

【図7】


110
104
105
103
102
101
107

【図8】



Espacenet

Bibliographic data: JP2008298966 (A) — 2008-12-11

IMAGE DISPLAY DEVICE

Inventor(s): TAKASUGI CHIKATOMO ± (TAKASUGI CHIKATOMO)

Applicant(s): KYOCERA CORP ± (KYOCERA CORP)

Classification: - **international:** ***G09F9/30; G09G3/20; G09G3/30; H01L27/32; H01L51/50; H05B33/12***
- **cooperative:** **H01L27/3218 (EP)**

Application number: JP20070143422 20070530 Global Dossier

Priority number(s): JP20070143422 20070530

Also published as: JP5173264 (B2)

Abstract of JP2008298966 (A)

PROBLEM TO BE SOLVED: To provide an image display device wherein pixels of different color can be vapor-deposited with the same evaporation mask while increasing an effective aperture ratio, and pixels of different color are equally arranged in all picture elements. ;SOLUTION: In the image display device, a plulality of picture elements 100 composed of three pixels of different color 110R, 110G, and 110B which comprise organic EL devices are arranged in a lateral and vertical directions like a lattice pattern. The picture element 100 is arranged so that none of the three pixels 110R, 110G, and 110B are arranged in one direction within the picture element 100. Each of the pixels 110R, 110G, and 110B are configured so that its size is equal to quarter area of the picture element 100. The pixels 110R, 110G, and 110B of the same color in the picture element 100 are arranged linearly in a lateral direction. The pixels 110R, 110G, and 110B of the same color in the picture element 100 are arranged linearly in a vertical direction. ;COPYRIGHT: (C)2009,JPO&INPIT

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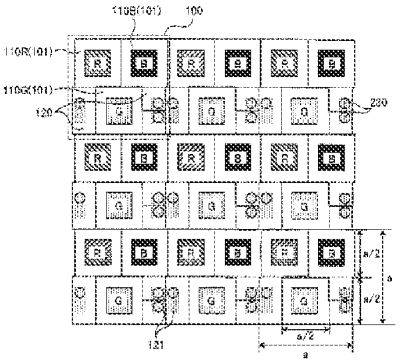
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5C080 AA06 BB05 CC03 DD01 DD28 EE30 JJ02 JJ03 JJ06
5C094 AA02 BA27 CA20 DA20 DB04 EA04 FA04

(54)【発明の名称】画像表示装置

(57)【要約】
【課題】開口率を大きくしつつ、異なる色の画素を同じ蒸着マスクで蒸着することができ、かつ全絵素で絵素内の異なる色の画素の配置が等しい画像表示装置を提供すること。
【解決手段】有機ＥＬ素子を含んで構成される、異なる色の３個の画素１１０Ｒ，１１０Ｇ，１１０Ｂからなる絵素１００が、横方向と縦方向に格子状に複数配列してなる画像表示装置において、前記絵素１００は、３個の画素１１０Ｒ，１１０Ｇ，１１０Ｂの全てが、絵素１００内で一方向に配列しないように配置されるとともに、各画素１１０Ｒ，１１０Ｇ，１１０Ｂは、その大きさが絵素１００の４分の１の面積に等しくなるように構成され、絵素１００内の同じ色の画素１１０Ｒ，１１０Ｇ，１１０Ｂは横方向に直線状に配列するように、そして絵素１００内の同じ色の画素１１０Ｒ，１１０Ｇ，１１０Ｂは縦方向に直線状に配列するように、絵素１００内に配置される。
【選択図】　図4



【特許請求の範囲】
【請求項1】
有機ＥＬ素子を含んで構成される、異なる色のｎ個（ｎは３以上の自然数）の画素からなる絵素が、第１の方向と、前記第１の方向に直角な第２の方向に格子状に複数配列してなる画像表示装置において、
前記絵素は、ｎ個の画素の全てが、前記絵素内で一方向に配列しないように配置されるとともに、各画素は、その大きさが前記絵素のｍ分の１（ｍは４以上の自然数）の面積に等しくなるように構成され、
前記第１の方向に隣接する絵素内の同じ色の画素は、前記第１の方向に直線状に配列するように、前記絵素内に配置され、
前記第２の方向に隣接する絵素内の同じ色の画素は、前記第２の方向に直線状に配列するように、前記絵素内に配置され、
前記絵素内の前記画素が配置されない領域に、前記有機ＥＬ素子と該有機ＥＬ素子を駆動する回路素子とを電気的に接続するコンタクトが形成されることを特徴とする画像表示装置。
【請求項2】
前記絵素は、正方形状を有し、前記絵素の４分の１の面積に等しい３個の正方形状の画素が配置された構造を有することを特徴とする請求項１に記載の画像表示装置。
【請求項3】
前記正方形状の画素は、前記正方形状の絵素を面積の等しい２つの長方形に分割した一方の長方形内に２つ配置され、他方の長方形内の中央に１つ配置されることを特徴とする請求項２に記載の画像表示装置。
【請求項4】
前記絵素は、略正方形状を有し、前記絵素の４分の１の面積に等しい３個の六角形状の画素が、その輪郭を接するように配置された構造を有することを特徴とする請求項１に記載の画像表示装置。
【請求項5】
前記絵素内の前記各画素と前記コンタクトとの間の距離が等しくなるように前記コンタクトが形成されることを特徴とする請求項１～４のいずれか１つに記載の画像表示装置。

【発明の詳細な説明】
【技術分野】
【0001】
本発明は、画像表示装置に関するものである。
【背景技術】
【0002】
一般的なカラー画像を表示する画像表示装置では、画像の表示単位となる１つの絵素がマトリックス状に配列され、そして各絵素が複数の異なる色（たとえば、赤（Ｒ）、緑（Ｇ）、青（Ｂ））の画素によって構成される。従来の絵素においては、Ｒ，Ｇ，Ｂの３種類の各画素の縦横比が３：１の長方形で、これらを横方向に配置して絵素を略正方形状としたものが最も多く採用されている。
【0003】
ところで、トップエミッション型の有機発光ダイオード（Organic Light Emitting Diode：以下、ＯＬＥＤという）を用いた画像表示装置を構成する画素は、トランジスタを含む駆動回路層と、その上の平坦化膜と、平坦化膜上のＯＬＥＤ（すなわち発光素子）を含む発光素子層とで構成されるのが一般的である。ここで、駆動回路層と発光素子層とはコンタクトホールを介して導通接続されるだけでよいため、駆動回路層の各駆動回路と発光素子層の各画素とが一対一に対応していればよく、形状や位置までが一致していなくてもよい（たとえば、特許文献１参照）。
【0004】
この発光素子は、通常、マスクを用いた蒸着やインクジェットを利用した印刷、レーザ

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を用いた転写などの手法を用いて形成される。ただし、ある画素の発光領域（すなわち開口部）に異なる色のＯＬＥＤがはみ出して形成されると色ずれや輝度低下が生じる一方、発光領域の一部領域にＯＬＥＤが形成されなければ減点や輝度低下が生じ、何れにしても画質の不良を招く。

【0005】

このため、蒸着、印刷、転写の位置精度および成膜のぼやけを考慮して、隣接する画素の発光領域の間に十分な隙間を設ける必要がある。しかし、この隙間からは光が発せられないため、画面全体に占める発光領域の比率、すなわち各画素の面積に対する各発光領域の面積の比が小さくなってしまう。

【0006】

また、一般にＯＬＥＤでは電流密度に比例した輝度が得られるが、電流密度が小さいほどＯＬＥＤに印加される電圧が低く、画像表示装置の寿命が長くなることが知られている。このため、画像表示装置の長寿命化に対しては、各画素でＯＬＥＤが発光する領域を大きくすることが重要である。

【0007】

図８は、最も一般的なストライプ状の画素配列を例示する図である。太線で囲まれたＲ，Ｇ，Ｂの３画素３１０Ｒ，３１０Ｇ，３１０Ｂが１つの略正方形の絵素３００を構成し、この絵素３００が格子状に配列されている。この図では、略正方形の絵素３００を左右方向に三等分した各領域がＲ，Ｇ，Ｂ各色の画素３１０Ｒ，３１０Ｇ，３１０Ｂの領域となっている。すなわち、縦横方向における絵素の配列周期（絵素ピッチ）をａとすると、各画素３１０Ｒ，３１０Ｇ，３１０Ｂの寸法は、縦ａ、横ａ／３の長方形となる。なお、この画素３１０Ｒ，３１０Ｇ，３１０Ｂの面積ａ／３×ａは、開口率を計算するときの基準となる論理的な画素面積である。

【0008】

このような画素では、蒸着や印刷、転写の精度（位置精度と成膜のぼやけとを含む）、すなわち生じ得る最大誤差をｘとすると、ＯＬＥＤの形成の過不足による不具合を回避するためには、各画素の発光領域を隣接画素の発光領域から縦横それぞれ２ｘだけ離す必要がある。このため、１画素の発光領域は、最大で（ａ／３－２ｘ）×（ａ－２ｘ）となる。ここで、仮に絵素ピッチａが１５０μｍ、蒸着や印刷などの成膜時の精度（すなわち最大誤差）ｘが１５μｍの場合、ｘ＝０．１ａとなり、開口率（論理的な画素面積に対する発光領域の割合）は、最大で０．３２となる。したがって、画面上で実際に光を発する部分の面積は、最大の場合でも画面全体の面積に対して１／３未満に過ぎず、残りの２／３以上の部分は光を発しない。

【0009】

さらに、実際の画素は、Ｒ，Ｇ，Ｂを同じマスクで蒸着するため、Ｒ，Ｇ，Ｂの各画素は同じ形状と同じ寸法を持たなければならないという制約を有する。また、図８で縦方向に一列に並ぶ同じ色の画素３１０Ｒ（または３１０Ｇ，３１０Ｂ）すべてを含むように蒸着マスクに開口部を設けると、蒸着マスクの強度が不足してしまうので、この強度不足を回避するような蒸着マスクの構造が必要となる。その結果、各画素は蒸着マスクの構造、すなわち開口部の構造に影響を受けてしまうという制約も有する。

【0010】

図９は、ストライプ状の画素配列の各画素を形成するための蒸着マスクの一例を示す図である。この図において、ハッチングが施されている部分が開口部３５１であり、１つの画素（絵素）は、開口部３５１の下部に所定幅ｂの金属部３５２が設けられている。そして、この金属部３５２で上下の開口部３５１間が区切られている。これにより、蒸着マスク３５０の開口部３５１の寸法は、横ａ／３、縦ａ－ｂとなり、蒸着精度をｘとすると、１画素の実際の発光領域の寸法は横ａ／３－２ｘ、縦ａ－ｂ－２ｘとなる。たとえば、ａ＝１５０μｍ、ｂ＝４０μｍ、ｘ＝１５μｍとすると、発光領域の寸法は、横２０μｍ、縦８０μｍとなり、開口率は、０．２１３となる。

【0011】

このような蒸着マスク３５０を用いると、上下の画素間には、図の上下方向の幅がｂ－２ｘの非蒸着領域が形成されるが、この部分は、ＯＬＥＤと画素回路とのコンタクト領域として有効に利用されている。また、陰極と陽極のどちらかを画素ごとに分離する画素境界を設ける必要があるが、この画素境界は、陽極をエッチングで部分除去したり、陰極隔壁を設けて陰極を分離したりして設けられている。

【0012】

図１０は、ストライプ状の画素配列の各画素における発光部と配線とコンタクトとの間の関係を示す上面図である。各画素領域（画素３１０）を囲む実線は、画素境界であり、陽極隙間または陰極隔壁を示している。また、各画素３１０内には発光領域３１１が設けられ、各画素３１０の下部（上下に配置される２つの発光領域３１１の間）には非蒸着領域３３０が形成される。この非蒸着領域３３０には、下層の配線と発光素子層の電極とを接続するためのコンタクト３３１が形成される。

【0013】

ここで、画素の輝度は、発光領域の輝度に、絵素面積に対する開口面積の比とデューティー（１フレームにおける発光時間の比）とを乗じたものである。たとえば、発光領域の輝度が１０００ｃｄ／ｍ^2、開口率が２１．３％、デューティーが３０％ならば、図１０に示されるストライプ状の画素配列を有する画像表示装置での視認される輝度は２１．３ｃｄ／ｍ^{2}となる。

【0014】

このように、一般的なストライプ状の画素配列では、各画素が細長くなるため、また実用に耐え得る強度を有するように形成された蒸着マスクの開口部によって画素の大きさが制限されるため、画面を占める発光領域の比率が小さくなる。そこで、このような問題を解決すべく、絵素の寸法に対して発光領域の面積を増大させるための技術が提案されている（たとえば、特許文献１，２参照）。

【0015】

図１１は、従来の画素配列の一例を示す図である。この図１１に示される画素配列は特許文献１に示されるものであり、Ｒ，Ｇ，Ｂの３画素３１０Ｒ，３１０Ｇ，３１０Ｂが太線で囲まれるようにデルタ状に配置されて１つの絵素３００を構成している。ここで、縦横方向における絵素３００の配列周期をａとすると、各画素３１０Ｒ，３１０Ｇ，３１０Ｂの寸法が縦ａ／２、横２ａ／３となり、上記ストライプ状の画素配列よりも各画素の形状が正方形に近づくため、開口率を高くすることができる。

【0016】

図１２は、従来の画素配列の他の一例を示す図である。この図１２に示される画素配列は特許文献２に示されるものであり、太線で囲まれた相互に横方向に隣接配置されたＲ，Ｇ，Ｂの３画素３１０Ｒ，３１０Ｇ，３１０Ｂが１つの絵素３００を構成しているが、左右に隣接し合う絵素３００ごとにＲ，Ｇ，Ｂの配列が逆転している。これにより、同じ色の画素が横方向に２つ連続して形成されることになる。このような構成では、絵素３００を跨いで左右に隣接し合う赤色（Ｒ）の２画素３１０Ｒまたは青色（Ｂ）の２画素３１０Ｂを、１個の蒸着マスクの開口部を介して蒸着することも可能となり、同時に蒸着される２画素間における蒸着のずれを無視することができる。

【0017】

このような画素配列における蒸着では、一般に１つの蒸着マスクをずらしつつ異なる色を蒸着するため、各色の蒸着領域は所定距離だけずらすと正確に重畳し合うようになっていなければならない。したがって、図１２で示した画素配列では蒸着領域の寸法（蒸着領域寸法）は、横ａ／２、縦ａである必要がある。このとき、緑色（Ｇ）の１画素３１０Ｇ、隣り合う赤色（Ｒ）の２画素３１０Ｒ、および隣り合う青色（Ｂ）の２画素３１０Ｂのそれぞれが同じ蒸着領域寸法となる。そして、このような画素配列でも開口率を高くすることができる。

【0018】

【特許文献1】特許第３６２０４９０号

【特許文献2】

特開２００４－２０７１２６号公報
【発明の開示】
【発明が解決しようとする課題】
【００１９】
しかしながら、特許文献１で提案された構成では、図１１に示されるように、縦方向には同じ画素配列の絵素３００が並ぶが、横方向には１絵素３００ごとに絵素３００の向きが上下逆さになるため、同じ色の画素３１０Ｒ（または３１０Ｇ，３１０Ｂ）が直線上に並ばない。図１３は、図１１の画素配列で１色のみ発光した状態を模式的に示す図である。この図１３に示されるように、単色発光（図１３では、たとえば赤色のみ発光した場合を示している）を行った際、縦方向には、発光している画素３１０Ｒは一列に並ぶが、横方向に関しては、発光している画素３１０Ｒが一列には並ばず、ジグザグ状に配列される。したがって、たとえば、画像上において横方向に沿った輪郭が凸凹状となったり、一般的な動画では被写体や撮影方向が横方向に移動することが多いが、そのような動画における被写体の動きがぎこちないものとなったりするような不具合を生じてしまう。すなわち、画質の低下を招いてしまうという問題点があった。
【００２０】
また、特許文献２で提案された構成では、図１２に示されるように、赤色および青色の画素３１０Ｒ，３１０Ｂについては、同色の画素が離隔される距離が緑色の画素３１０Ｇよりも横方向で長くなっている。図１４は、図１２の画素配列で１色のみ発光した状態を模式的に示す図である。この図１４に示されるように、赤色または青色の単色発光（図１４では、たとえば赤色のみ発光した場合を示している）を行った際、発光していない画素（図１４では、画素３１０Ｇ，３１０Ｂ）によって形成される縦に沿った領域（黒線）の幅が３ａ／２と太くなり、顕在化してしまう。ここで、絵素３００の幅がａであることを考慮すると、幅が３ａ／２の黒線は太すぎて画質上容認できないものとなる。すなわち画質の低下を招いてしまうという問題点があった。
【００２１】
本発明は、上記課題に鑑みてなされたものであり、開口率を大きくしつつ、異なる色の画素を同じ蒸着マスクで蒸着することができ、かつ全絵素で絵素内の異なる色の画素の配置が等しい画像表示装置を提供することを目的とする。
【課題を解決するための手段】
【００２２】
上述した課題を解決し、目的を達成するために、本発明にかかる画像表示装置は、有機ＥＬ素子を含んで構成される、異なる色のｎ個（ｎは３以上の自然数）の画素からなる絵素が、第１の方向と、前記第１の方向に直角な第２の方向に格子状に複数配列してなる画像表示装置において、前記絵素は、ｎ個の画素の全てが、前記絵素内で一方向に配列しないように配置されるとともに、各画素は、その大きさが前記絵素のｍ分の１（ｍは４以上の自然数）の面積に等しくなるように構成され、前記第１の方向に隣接する絵素内の同じ色の画素は、前記第１の方向に直線状に配列するように、前記絵素内に配置され、前記第２の方向に隣接する絵素内の同じ色の画素は、前記第２の方向に直線状に配列するように、前記絵素内に配置され、前記絵素内の前記画素が配置されない領域に、前記有機ＥＬ素子と該有機ＥＬ素子を駆動する回路素子とを電気的に接続するコンタクトが形成されることを特徴とする。
【発明の効果】
【００２３】
この発明によれば、従来のストライプ状の画素配列の画像表示装置に比べて開口率を大きくすることができるとともに、異なる色の画素を同じ蒸着マスクで蒸着することができるという効果を有する。また、全絵素で絵素内の異なる色の画素の配置が等しいので、画像表示装置内ではたとえばある色の画素は、縦方向および横方向に一直線上に配列することになり、従来のデルタ構造などの画素配列を有する画像表示装置などに比して、画像表示装置で表示される画質を低下させずに表示させることができるという効果も有する。

【発明を実施するための最良の形態】

【0024】

以下に添付図面を参照して、本発明にかかる画像表示装置の好適な実施の形態を詳細に説明する。なお、これらの実施の形態により本発明が限定されるものではなく、本発明の要旨を逸脱しない範囲において適宜変更可能である。

【0025】

実施の形態１．

図１は、本発明が適用される画像表示装置の全体構造の一例を模式的に示す図であり、図２は、図１の画素回路の構成の一例を示す図である。図１に示されるように、この画像表示装置は、ガラス基板などの基板１上に第１の方向（横方向）と、第１の方向に垂直な第２の方向（縦方向）に格子状に多数配置された画素回路２と、信号線５に接続され、複数の画素回路２に対して輝度信号を供給する信号線駆動回路３と、走査線６およびアース線７に接続され、輝度信号を供給する画素回路２を選択するための走査信号を画素回路２に供給する走査線駆動回路４と、画素回路２に備えられた電流発光素子に対して電流を供給する電流源８と、を備える。ここで画像表示装置は、アクティブマトリックス方式であるものとする。

【0026】

図２に示されるように、画素回路２は、正側（アノード側）が正電源Ｖｄｄに接続された発光素子２１と、ドレイン電極が発光素子２１の負側（カソード側）に接続され、ソース電極がグランドに接続されたＴＦＴからなるドライバ素子２２と、ドライバ素子２２のゲート電極とグランドとの間に接続されたコンデンサ２３と、ドレイン電極がドライバ素子２２のゲート電極に接続され、ソース電極が信号線５に接続され、ゲート電極が走査線６に接続されたＴＦＴからなるスイッチング素子２４と、を有する構造をとる。

【0027】

ここで、発光素子２１は、電流注入によって発光する機構を有し、たとえば有機ＥＬ素子によって形成される。有機ＥＬ素子は、抵抗率の低い導電性材料によって形成されるアノード層およびカソード層と、アノード層とカソード層との間にフタルシアニン、トリスアルミニウム錯体、ベンゾキノリノラト、ベリリウム錯体などの有機系の材料によって形成された発光層とを少なくとも備えた構造を有し、発光層に注入された正孔と電子とが再結合することによって光を生じる機能を有する。

【0028】

この画素回路２の動作の概略について説明する。走査線６の電位を高レベルとすると、スイッチング素子２４がオン状態となり、信号線５に書き込み電位を印加すると、コンデンサ２３が充電または放電され、ドライバ素子２２のゲート電極には所定の電位が書き込まれる。一方、走査線６の電位を低レベルとすると、スイッチング素子２４は導通せず、走査線６とスイッチング素子２４とは電気的に切り離されるが、ドライバ素子２２のゲート電位はコンデンサ２３によって安定に保持される。

【0029】

そして、ドライバ素子２２と発光素子２１に流れる電流は、ドライバ素子２２のゲート－ソース間電位Ｖｇｓに応じた値となり、発光素子２１はその電流値に応じた輝度で発光し続ける。つまり、図２に示す画素回路２では一度電位の書き込みを行えば、つぎに書き込みが行われるまでの間、発光素子２１は所定の輝度で発光を継続する。

【0030】

つぎに、このような回路構成を有する画像表示装置の構造の一例について説明する。図３は、本発明が適用される画像表示装置の断面構造の一例を模式的に示す図である。この図３は、画像表示装置内における画素１個分の断面構造を模式的に示すものであるが、層の厚みと幅との関係や各層の厚みの比率などは現実のものとは異なる。

【0031】

この図３に示されるように、画像表示装置は、ＴＦＴ２２２，２２４などの回路素子と回路素子間を配線する導電層２２５が配設された基板１上に平坦化層２２１を備え、平坦

化層２２１上に発光素子を配設した立体構造を備える。具体的には、図３に示すように、発光素子２１に対してそれぞれスイッチング素子２４、ドライバ素子２２として機能するＴＦＴ２２４，２２２などの回路素子が基板１上に配設されるのに対し、発光素子２１は、平坦化層２２１上に配設されている。さらに、発光素子２１のアノード側には図示を省略した電源線まで延伸した構造を有するアノード配線層２１２が配設され、カソード側にはカソード配線層２１３が配設され、アノード配線層２１２とカソード配線層２１３との間には、発光層２１１が挟持されている。なお、アノード配線層２１２およびカソード配線層２１３のうち、発光層２１１を挟持する領域に相当する部分はそれぞれ発光素子２１のアノード電極、カソード電極として機能する。

【0032】

発光素子２１とドライバ素子２２としてのＴＦＴとの間を電気的に接続するため、平坦化層２２１は、導電層２２５の一部領域を露出させるための穴構造２２６を有する。そして、カソード配線層２１３はこの穴構造２２６の底の導電層２２５が露出した領域まで延伸して、導電層２２５と電気的に接続した構造を有する。この部分が後述するコンタクト２３０に対応する。

【0033】

この図３の構造では、発光素子２１から発せられる光は鉛直上方に出力されるため、発光素子２１上に配設されるカソード配線層２１３は良好な光透過特性を備える必要がある。そのため、カソード配線層２１３は非常に薄く形成され、１０ｎｍ程度以下の膜厚を有する。一方、平坦化層２２１は寄生容量を低減するため膜厚を大きくする必要があり、一般には２～５μｍ程度の膜厚を有する。このため、カソード配線層２１３を穴構造２２６まで延伸させた場合、特に穴構造２２６の側面において断線するおそれが生じることから、断線を防止するため、穴構造２２６の側面を含む領域において、カソード配線層２１３の下層に十分な膜厚を有する接続補助層２１４を配設している。

【0034】

接続補助層２１４と発光素子２１の下層に位置するアノード配線層２１２とを絶縁するとともに、アノード配線層２１２をその上位に設けられる他の配線層と絶縁するために、発光素子２１と穴構造２２６との境界部分と、発光素子２１と穴構造２２６とを含む画素同士の境界部分には絶縁層２１５が設けられている。また、発光素子２１と穴構造２２６が形成された範囲を１画素として区切るための樹脂で構成された隔壁２２７が所定の絶縁層２１５上に設けられる。この隔壁２２７は、隣接する画素のカソード配線層２１３と自画素内のカソード配線層２１３とを電気的に絶縁する役目も有している。さらに、画像表示装置を構成する基板１の全面を覆うように、隔壁２２７上には封止基板２２８が載置され、隔壁２２７の上端部と封止基板２２８とは密着される。

【0035】

ここで、本発明の実施の形態１にかかる画素配列について説明する。なお、この明細書において、画像表示装置における画像の表示単位を絵素という。また、絵素は、複数の異なる種類の色の画素によって構成される。画像表示装置における画素は通常、光の３原色となる赤（Ｒ）、緑（Ｇ）、青（Ｂ）の３つの色によって構成される。その結果、絵素自体の色は、Ｒ，Ｇ，Ｂの光の組み合わせによって表現されるものとなる。

【0036】

図４は、本発明の実施の形態１にかかる画素配列の一例を示す平面図である。この図４に示されるように、絵素１００は、略正方形状を有している。絵素１００の正方形の１辺をａとすると、絵素１００の面積を４等分して得られる（ａ／２）×（ａ／２）の形状の３つの小正方形１０１を絵素１００内に配置し、残りの１個分の小正方形の面積相当の領域を、絵素内の３つの小正方形１０１が配置されない領域に分配する。

【0037】

ここでは、絵素１００の上半分に、２つの（ａ／２）×（ａ／２）の形状の小正方形１０１を配置し、絵素１００の下半分の横方向の中央に、（ａ／２）×（ａ／２）の形状の小正方形１０１の横方向の中心が重なるように配置する。すなわち、絵素１００の上半分

の長方形を２つの小正方形１０１で埋め、絵素１００の下半分の長方形の右端を基準にしてａ／４～３ａ／４までの範囲に（ａ／２）×（ａ／２）の形状の１つの小正方形１０１を配置する。そして、これらの３つの（ａ／２）×（ａ／２）の形状の小正方形１０１が画素１１０となる。また、絵素１００の下半分の左右の両端～ａ／４の範囲は、各画素１１０のコンタクト２３０が形成されるコンタクト形成領域１２０となる。この図４の場合、各画素１１０とコンタクト２３０との間の距離はすべて等しくなるように形成される。

【0038】

ここで、絵素１００は第１の方向（図の横方向）に高さを同じくして配列されるとともに、第１の方向とは垂直な方向（図の縦方向）にも幅を同じくして配列される。さらに、すべての絵素１００において、その内部の画素の色の配置は一致しているものとする。すなわち、この図４の例では、それぞれの絵素１００内の左上の画素は赤色（Ｒ）の画素１１０Ｒであり、右上の画素は青色（Ｂ）の画素１１０Ｂであり、下の画素は緑色（Ｇ）の画素１１０Ｇである。

【0039】

このように、１つの絵素１００内において、３つの画素１１０Ｒ，１１０Ｂ，１１０Ｇが一方向に配列しないように複数の画素１１０Ｒ，１１０Ｂ，１１０Ｇが配置される領域が分割される。すなわち、１つの絵素１００内において、３つの画素（１１０Ｒ、１１０Ｂ、１１０Ｇ）全てが一直線上に配列されることはない。また、隣接する絵素同士における同じ色の画素１１０が縦方向および横方向に一直線上に配列するように、正方形状の絵素１００が縦横に周期的に配置される。

【0040】

また、この図４において、点線は、画素１１０と当該画素１１０の発光素子２１を回路素子に接続するためのコンタクトが形成されるコンタクト領域１２０との区切りを示す仮想の線を示している。また、画素１１０およびコンタクト形成領域１２０を囲む実線は、画素１１０及びコンタクト形成領域１２０を合わせてなる画素領域の境界を示している。この画素領域の境界に沿って陽極隙間または陰極隔壁が形成される。画素１１０Ｒ，１１０Ｇ，１１０Ｂが形成されないコンタクト形成領域１２０には、画素１１０Ｒ，１１０Ｇ，１１０Ｂ内に形成される有機ＥＬ素子が全く蒸着されない非蒸着領域１２１が存在する。この非蒸着領域１２１中に有機ＥＬ素子と下層の配線層（導電層２２５）と電気的に接続するためのコンタクト２３０が形成される。

【0041】

図５は、図４の画素配列を形成する蒸着マスクの一例を示す図である。この図に示されるように、蒸着マスク１５０の開口部１５１は、正方形状であり、その寸法は、縦横ともにａ／２となる。そして、この開口部１５１が横方向および縦方向にａのピッチで配置されている。この蒸着マスク１５０には、開口部１５１の横方向および上下方向の両方に間隔（ａ／２）が設けられているので、この蒸着マスク１５０は、蒸着時の使用に耐え得るだけの強度を有している。

【0042】

この蒸着マスク１５０で赤色の画素１１０Ｒの有機ＥＬ素子を蒸着する場合には、蒸着マスク１５０を、開口部１５１が基板上の赤色の画素形成位置に一致するように位置合わせを行って配置した後に、赤色の画素１１０Ｒを構成する有機ＥＬ素子を蒸着する。その後、青色の画素１１０Ｂの有機ＥＬ素子を蒸着する場合には、図４において、蒸着マスク１５０を左右いずれかの方向にａ／２だけずらして位置合わせをした後に、青色の画素１１０Ｒを構成する有機ＥＬ素子を蒸着すればよい。また、緑色の画素１１０Ｇの有機ＥＬ素子を蒸着する場合には、図４において、赤色の画素１１０Ｒまたは青色の画素１１０Ｂの形成後に、左右いずれかの方向にａ／４ずらし、さらに上下いずれかの方向にａ／４ずらして位置合わせをした後に、緑色の画素１１０Ｇを構成する有機ＥＬ素子を蒸着すればよい。

【0043】

このような蒸着マスク１５０を使用して有機ＥＬ素子を形成すると、各画素の実際の発

光領域の寸法は、蒸着精度をｘとすると、縦横ともにａ／２－２ｘとなる。たとえば、ａ＝１５０μｍ、ｘ＝１５μｍとすると、発光領域の寸法は縦横ともに４５μｍとなる。また、論理的な画素面積に対する発光領域の面積の比である開口率は、０．２７となり、背景技術で説明した図９の金属部３５２を有するストライプ状の蒸着マスク３５０で画素を形成した場合の開口率の０．２１３に比して大幅に改善される。

【0044】

また、本実施の形態１により得られる開口率０．２７の画像表示装置で、背景技術で説明した開口率０．２１３の画像表示装置と同じ視認輝度２１．３ｃｄ／ｍ^{2}を得るためには、デューティーが３０％とすると、発光領域の輝度は約７９０ｃｄ／ｍ^{2}でよくなる。これは、開口率０．２１３の画像表示装置の発光領域の輝度１，０００ｃｄ／ｍ^{2}の場合に比して２０％以上、輝度を抑制することができる。上述したように、ＯＬＥＤは電流密度と輝度が比例する関係にあり、また電流密度が高いと劣化が速いことが知られているので、発光領域の輝度を抑えることができれば、ＯＬＥＤに注入される電流密度も抑えることができ、その結果、ＯＬＥＤの寿命を伸ばすことができる。

【0045】

なお、図４に示される絵素１００内のＲ，Ｇ，Ｂの配列は一例であり、これに限定される趣旨ではない。つまり、図４に示されるＲ，Ｇ，Ｂの配列はすべて上下逆でもよいし、図４を右にまたは左に９０度回転させて、Ｒ，Ｇ，Ｂのうち２つの画素が縦に並ぶようにしてもよい。さらに、各画素１１０Ｒ，１１０Ｇ，１１０Ｂの１つの絵素１００内での並び順も限定されるものではなく、すべての絵素１００間で統一が取れていれば、各画素１１０Ｒ，１１０Ｇ，１１０Ｂの並び順は任意でよい。

【0046】

図６は、本発明の実施の形態１にかかる画素配列の他の一例を示す平面図である。この図６では、正方形状の１つの絵素１００を、寸法が（ａ／２）×（ａ／２）の形状を有する４つの小正方形１０１－１～１０１－４に分割し、このうち３つの小正方形１０１－１～１０１－３にＲ，Ｇ，Ｂの各画素１１０Ｒ，１１０Ｂ，１１０Ｇを配置し、残りの１つの小正方形１０１－４を各画素１１０Ｒ，１１０Ｇ，１１０Ｂのコンタクト形成領域１２０としている。つまり、１つの絵素１００中で各画素１１０Ｒ，１１０Ｇ，１１０ＢがＬ字状に配列されている。また、コンタクト形成領域１２０の非蒸着領域１２１には、各画素１１０Ｒ，１１０Ｇ，１１０Ｂの３つのコンタクト２３０Ｒ，２３０Ｇ，２３０Ｂが形成される。ただし、この場合Ｌ字型の角部に配置される画素とコンタクト（図６の場合には、Ｒの有機ＥＬ素子が形成される画素１１０Ｒとコンタクト２３０Ｒ）との間の距離が、他の画素とコンタクトとの間の距離よりも長くなることとなる。なお、この画素配列を形成するための蒸着マスクは、図４の画素配列の場合と同じ図５の蒸着マスク１５０を用いることができる。

【0047】

本実施の形態１によれば、従来のストライプ状の画素配列の画像表示装置に比べて開口率を大きくすることができるとともに、異なる色の画素を同じ蒸着マスクで蒸着することができるという効果を有する。また、全絵素１００で絵素１００内の異なる色の画素１１０の配置が等しいので、画像表示装置内ではたとえばある色の画素１１０は、縦方向および横方向に一直線上に配列することになり、従来のデルタ構造などの画素配列を有する画像表示装置などに比して、画像表示装置で表示される画質を低下させずに表示させることができるという効果も有する。さらに、ストライプ状の画素配列の場合と異なり、同色の画素１１０が上下左右ともに離れているので、蒸着マスク１５０の強度が低下することがないという効果も有する。

【0048】

実施の形態２．

図７は、本発明の実施の形態２にかかる画素配列の他の一例を示す平面図である。この図７では、各画素を六角形状としている。つまり、実施の形態１では、１つの絵素を正方形状に４等分していたが、この実施の形態２では、１つの絵素１００を六角形状に４等分

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するようにしている。このとき、１つの絵素１００は略正方形状を有しているが、絵素１１０上下のラインに対応する輪郭線（実線で示される画素領域の境界線）は、六角形の画素１１０の形状に合わせて波打った形状を有している。一方、絵素１１０の左右のラインに対応する輪郭線は、直線となっている。

【0049】

図７の例では、絵素１００の面積をＳとすると、Ｓ／４の面積を有する３つの六角形１１１を絵素１００内に配置する。これによって、絵素１００内の３つの六角形１１１が配置されない領域の面積は、残りの１つの六角形１１１の面積と等しくなる。つまり、絵素１００の上半分に、面積Ｓ／４の２つの合同な六角形１１１を配置して画素１１０Ｒ，１１０Ｂとし、絵素１００の下半分の横方向の中央に、上半分に配置した六角形１１１に接するように面積Ｓ／４の１つの六角形１１１を配置して画素１１０Ｇとする。そして、下半分に配置した六角形１１１の左右両側には、それぞれ、面積（Ｓ／４）／２のコンタクト形成領域１２０が形成される。このコンタクト形成領域１２０は、上記の六角形１１１の画素１１０Ｒ，１１０Ｇ，１１０Ｂを半分にした形状となっている。なお、この図７の場合には、各画素１１０Ｒ，１１０Ｂ，１１０Ｇとコンタクト２３０との間の距離はすべて等しくなるように、コンタクト２３０が形成される。

【0050】

ここで、絵素１００は第１の方向（横方向）に高さを同じくして配列されるとともに、第１の方向とは垂直な方向（縦方向）にも幅を同じくして配列される。さらに、すべての絵素１００において、その内部の画素１１０Ｒ，１１０Ｇ，１１０Ｂの色の配置は一致している必要がある。すなわち、この図７の例では、絵素１００内の左上の画素は赤色（Ｒ）の画素１１０Ｒであり、右上の画素は青色（Ｂ）の画素１１０Ｂであり、下の画素は緑色（Ｇ）の画素１１０Ｇである。

【0051】

このように、１つの絵素１００内においては、異なる色の画素１１０が一直線上に配列せず、かつ表示領域においては、同じ色の画素１１０が縦方向および横方向に一直線上に配列するように、絵素１００が格子状に縦横に周期的に配置される。すなわち、１つの絵素１００内において、３つの画素（１１０Ｒ、１１０Ｂ、１１０Ｇ）全てが一直線上に配列されることはない。

【0052】

この図７において、点線は、画素が形成される画素境界を示し、この点線内にＲ，Ｇ，Ｂの画素１１０Ｒ，１１０Ｇ，１１０Ｂを構成する有機ＥＬ素子が形成される。また、点線に重なって描かれる実線は、画素境界（陽極隙間または陰極隔壁）を示している。画素１１０Ｒ，１１０Ｇ，１１０Ｂが形成されないコンタクト形成領域１２０には、画素を形成する有機ＥＬ素子が全く蒸着されない非蒸着領域１２１が存在する。この非蒸着領域１２１中には有機ＥＬ素子が下層の配線層と電気的に接続するためのコンタクト２３０が形成される。

【0053】

この図７の画素配列を形成する蒸着マスクは、開口部１５１を六角形状としたものである点を除いて、実施の形態１の図５において、図５と同様ものとなる。

【0054】

このような蒸着マスクを使用して有機ＥＬ素子を形成すると、たとえば、画素ピッチをａ＝１５０μｍとし、蒸着誤差をｘ＝１５μｍとした場合に、各画素１１０の実際の発光領域の面積は２，２０６μm^2となる。一方、ストライプ状の画素配列における論理的な画素面積は、７，５００μm^2であるので、論理的な画素面積に対する発光領域の面積の比である開口率は、０．２９４となり、背景技術で説明した図９の金属部３５２を有するストライプ状の蒸着マスク３５０で画素を形成した場合の開口率の０．２１３に比して大幅に改善される。

【0055】

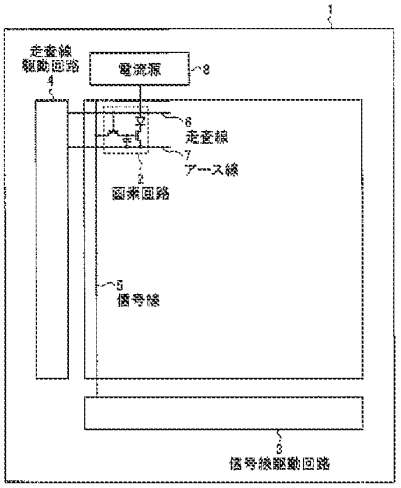
本実施の形態２によっても、実施の形態１と同様の効果を得ることができる。

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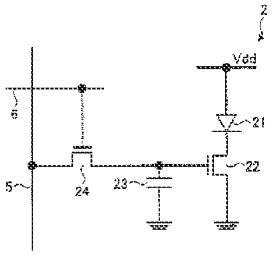
【0056】
なお、上述した説明では、Ｒ，Ｇ，Ｂの３色で画素を形成した場合を例に挙げたが、４色以上の色で画素を形成する場合にも適用することができる。たとえば、１つの絵素内にｎ色の画素を形成する場合には、絵素の面積Ｓをｍ等分し（ここで、ｎ，ｍともに自然数で、ｍ＞ｎ）、Ｓ／ｍの面積を有するｎ個の正方形状または六角形状の画素を絵素内に配置し、残りの領域をコンタクト形成領域とすればよい。そして、絵素内のある色の画素が、横方向と縦方向のそれぞれに一直線上に配列するように、絵素内に画素を配置するとともに、絵素を配置すればよい。
【0057】
また、上述した説明では、トップエミッション型の画像表示装置の場合を例に挙げたが、これに限られる趣旨ではなく、ボトムエミッション型の画像表示装置の場合でも、上記の実施の形態１～２を適用することができる。
【産業上の利用可能性】
【0058】
以上のように、この発明にかかる画像表示装置は、有機ＥＬ素子を発光層として用いる画像表示装置に有用である。
【図面の簡単な説明】
【0059】
【図1】本発明が適用される画像表示装置の全体構造の一例を模式的に示す図である。
【図2】図１の画素回路の構成の一例を示す図である。
【図3】本発明が適用される画像表示装置の断面構造の一例を模式的に示す図である。
【図4】本発明の実施の形態１にかかる画素配列の一例を示す平面図である。
【図5】図４の画素配列を形成する蒸着マスクの一例を示す図である。
【図6】本発明の実施の形態１にかかる画素配列の他の一例を示す平面図である。
【図7】本発明の実施の形態２にかかる画素配列の他の一例を示す平面図である。
【図8】ストライプ状の画素配列を例示する図である。
【図9】ストライプ状の画素配列の各画素を形成するための蒸着マスクの一例を示す図である。
【図10】ストライプ状の画素配列の各画素における発光部と配線とコンタクトとの間の関係を示す上面図である。
【図11】従来の画素配列の一例を示す図である。
【図12】従来の画素配列の他の一例を示す図である。
【図13】図１１の画素配列で１色のみ発光した状態を模式的に示す図である。
【図14】図１２の画素配列で１色のみ発光した状態を模式的に示す図である。
【符号の説明】
【0060】
１　基板
２　画素回路
３　信号線駆動回路
４　走査線駆動回路
５　信号線
６　走査線
７　アース線
８　電流源
２１　発光素子
２２　ドライバ素子
２３　コンデンサ
２４　スイッチング素子
１００　絵素
１０１，１０１－１～１０１－４　小正方形

１１１　六角形
１１０，１１０－１～１１０－３，１１０Ｒ，１１０Ｇ，１１０Ｂ　画素
１２０　コンタクト形成領域
１２１　非蒸着領域
１５０　蒸着マスク
１５１　開口部
２１０　配線領域
２１１　発光層
２１２　アノード配線層
２１３　カソード配線層
２１４　接続補助層
２１５　絶縁層
２２１　平坦化層
２２２，２２４　薄膜トランジスタ（ＴＦＴ）
２２５　導電層
２２６　穴構造
２２７　隔壁
２２８　封止基板
２３０，２３０Ｒ，２３０Ｇ，２３０Ｂ　コンタクト

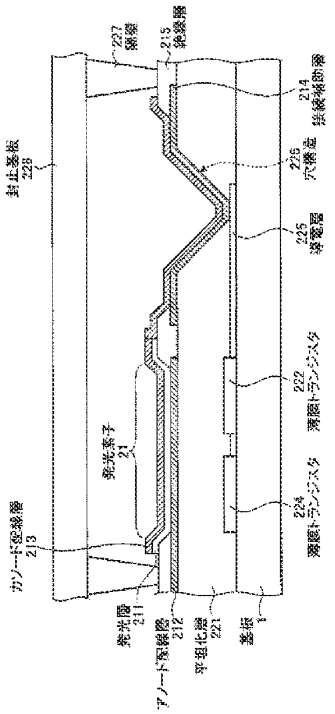
【図1】



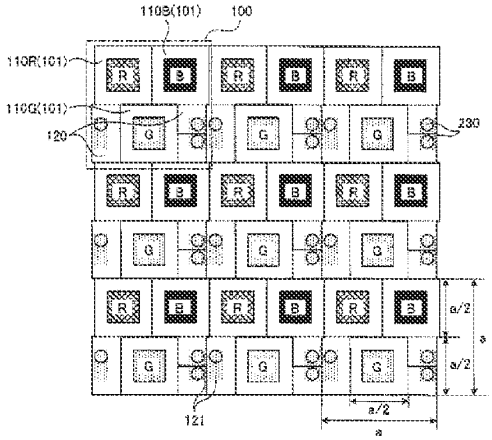
【図2】



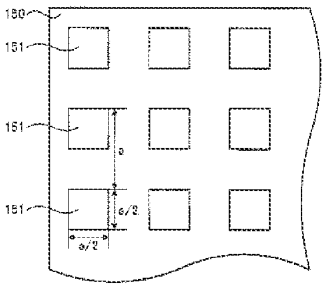
【図3】


227
215
214
封止基板
226
225
222
224
カソード配線層
213
発光層
211
アノード配線層
212
平坦化層
221
基板

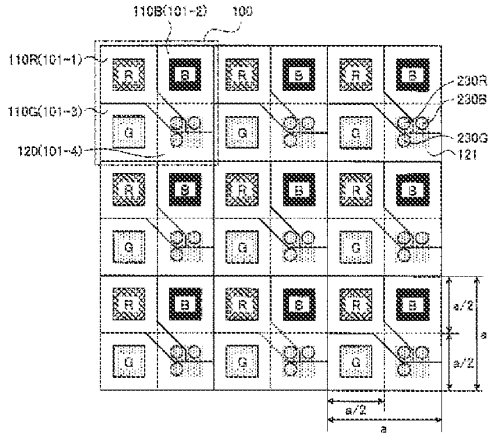
【図4】


110B(101)
100
110R(101)
110G(101)
120
230
a/2
a
121

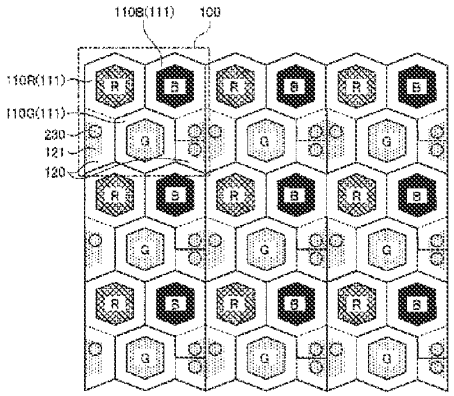
【図5】


180
151
151
151
a
a/2
a/2

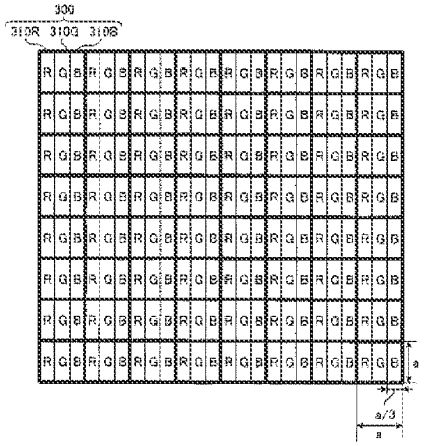
【図6】


110B(101-2)
100
110R(101-1)
110G(101-3)
120(101-4)
230R
230B
230G
121
a/2
a
a/2

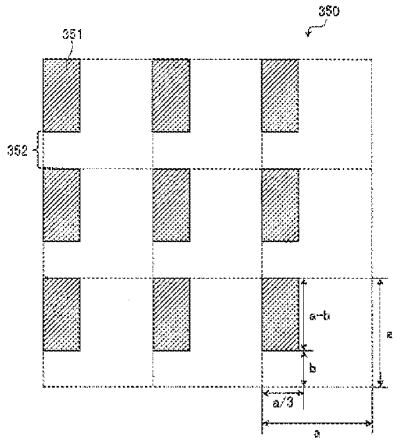
【図7】


110B(111)
100
110R(111)
110G(111)
230
121
120

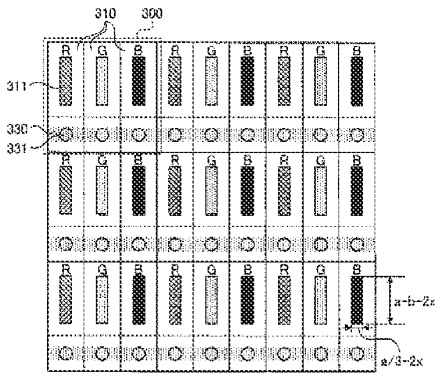
【図8】


300
310R 310G 310B
a
a/3
a

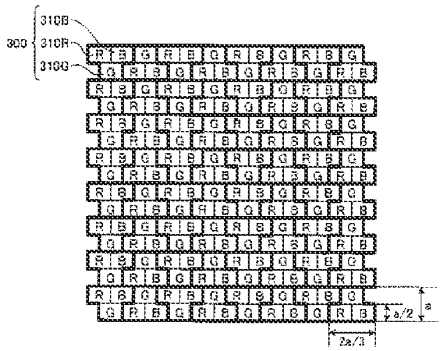
【図9】


350
351
352
a-b
b
a
a/3
a

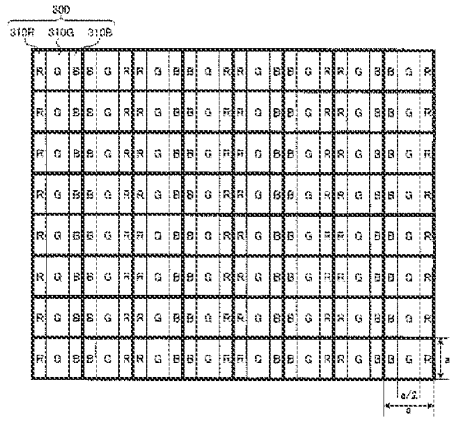
【図10】


310
300
311
330
331
a-b-2x
a/3-2x

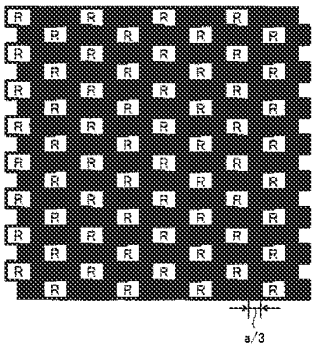
【図11】



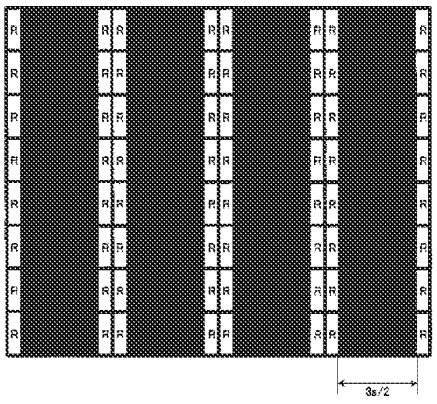
【図12】



【図13】



【図14】



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		Ｈ０５Ｂ 33/14	Ａ	

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ORGANIC LIGHT EMITTING DIODE

Inventor(s): SEONG SUN JOO [KR] ± (SEONG, SUN JOO)

Applicant(s): DAEWOO ELECTRONICS CORP [KR] ± (DAEWOO ELECTRONICS CORPORATION)

Classification: - **international:** ***H05B33/22***
- **cooperative:** **H01L27/3211 (KR)**; **H01L51/5012 (KR)**; **H01L51/5203 (KR)**; H01L2924/12044 (KR)

Application number: KR20050041281 20050517 Global Dossier

Priority number(s): KR20050041281 20050517

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Abstract of KR20060118868 (A)

An organic light emitting diode is provided to improve the quality the organic light emitting diode and every kind of display devices using the same, by displaying round type characters or figures clearly. A plurality of first electrodes(110) is arranged on a transparent substrate(100) along one direction. An insulation film(120) is formed on the transparent substrate and the plurality of first electrodes in a hexagonal honey comb shape, and defines a hexagonal pixel on the plurality of first electrodes. An organic thin film layer and a second electrode(140) are formed on the first electrode in sequence. A barrier rib(150) is formed on the insulation film in order to prevent short-circuit of the second electrode among adjacent pixels along one direction of the arrangement of the first electrode.

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전체 청구항 수 : 총 5 항

(54) 유기 발광 소자

(57) 요약

본 발명은 곡선을 포함하는 라운드형 윤곽의 그림 또는 문자에 대한 표시를 더욱 선명하게 할 수 있는 유기 발광 소자에 관한 것이다. 본 발명에 의한 유기 발광 소자는 투명 기판 위에 한 쪽 방향으로 배열되는 복수의 제 1 전극과, 상기 투명 기판 및 복수의 제 1 전극 위에 복수의 육각형이 모인 벌집 형태로 형성되어 상기 복수의 제 1 전극 상에 육각형 모양의 화소를 정의하는 절연막과, 상기 육각형 모양 화소의 상기 제 1 전극 위에 순차 형성되는 유기 박막층 및 제 2 전극과, 상기 제 1 전극이 배열된 한 쪽 방향을 따라 서로 인접하는 화소 간의 제 2 전극의 단락을 방지하도록 소정 영역의 상기 절연막 위에 형성되는 격벽을 포함한다.

대표도

도 1

특허청구의 범위

청구항 1.

투명 기판 위에 한 쪽 방향으로 배열되는 복수의 제 1 전극과,

상기 투명 기판 및 복수의 제 1 전극 위에 복수의 육각형이 모인 벌집 형태로 형성되어 상기 복수의 제 1 전극 상에 육각형 모양의 화소를 정의하는 절연막과,

상기 육각형 모양 화소의 상기 제 1 전극 위에 순차 형성되는 유기 박막층 및 제 2 전극과,

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상기 제 1 전극이 배열된 한 쪽 방향을 따라 서로 인접하는 화소 간의 제 2 전극의 단락을 방지하도록 소정 영역의 상기 절연막 위에 형성되는 격벽을 포함하는 유기 발광 소자.

청구항 2.

제 1 항에 있어서, 상기 복수의 제 1 전극은 세 개씩의 제 1 전극이 한 세트로 되어,

이 중 첫 번째 제 1 전극이 각 육각형 모양 화소의 윗변을 따라 지그재그 형태로 투명 기판의 한 쪽 방향으로 배열되어 있고,

두 번째 제 1 전극이 각 육각형 모양 화소의 중앙부를 가로질러 투명 기판의 한 쪽 방향으로 배열되어 있으며,

세 번째 제 1 전극이 각 육각형 모양 화소의 아랫변을 따라 지그재그 형태로 투명 기판의 한 쪽 방향으로 배열되어 있는 유기 발광 소자.

청구항 3.

제 1 항에 있어서, 상기 복수의 제 1 전극은 각 육각형 모양의 화소 영역에 대응하는 하나씩의 제 1 전극이 투명 기판의 한 쪽 방향으로 늘어선 줄무늬 형태로 배열되어 있는 유기 발광 소자.

청구항 4.

제 1 항 내지 제 3 항에 있어서, 상기 각 육각형 모양 화소는 적색(R), 녹색(G) 및 청색(B)를 각각 표시하기 위한 세 개의 부화소를 포함하는 유기 발광 소자.

청구항 5.

제 4 항에 있어서, 상기 청색을 표시하기 위한 부화소가 상기 적색 및 녹색을 표시하기 위한 부화소보다 작은 면적으로 형성되는 유기 발광 소자.

명세서

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 곡선을 포함하는 라운드형 윤곽의 그림 또는 문자에 대한 표시를 더욱 선명하게 할 수 있는 유기 발광 소자에 관한 것이다.

일반적으로, 유기 발광 소자는 평판 디스플레이 소자의 하나로서 투명 기판 상의 양전극층과 음전극층 사이에 유기 발광층을 포함하는 유기 박막층 등을 개재하여 구성하며, 매우 얇은 두께의 매트릭스 형태를 이룬다.

이러한 유기 발광 소자는 15V 이하의 낮은 전압으로 구동이 가능하고, 다른 디스플레이 소자, 예를 들어, TFT-LCD에 비해 휘도, 시야각 및 소비 전력 등에서 우수한 특성을 나타낸다. 더구나, 유기 발광 소자는 다른 디스플레이 소자에 비해 1㎲의 빠른 응답 속도를 가지기 때문에 동영상 구현이 필수적인 차세대 멀티미디어용 디스플레이에 적합한 소자이다.

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통상적으로, 이러한 유기 발광 소자에서는 투명 기판 위에 줄무늬 형상으로 배열되는 복수의 양전극층이 형성되어 있고, 이러한 양전극층 위에 상기 양전극층과 직교하도록 줄무늬 형상으로 배열되는 복수의 음전극층이 형성되어 있다. 이와 같이 서로 직교하는 복수의 양전극층과 음전극층이 서로 만나는 부분에서 사각형 모양을 띄는 유기 발광 소자의 각 화소가 정의된다. 또한, 상기 각 화소의 양전극층 및 음전극층 사이에는 유기 발광층 등을 포함하는 유기 박막층이 형성되어 있다.

이러한 구조를 가지는 종래 기술에 의한 유기 발광 소자는, 상기 복수의 양전극층 및 음전극층에 각각 소정의 전기장이 인가되면, 상기 양전극층 및 음전극층으로부터 각각 정공 및 전자가 유기 박막층 중의 유기 발광층으로 전달된다. 이러한 정공과 전자가 유기 발광층 내에서 서로 만나 전자-정공 쌍(electron-hole pair)을 형성하고 높은 에너지를 갖는 여기자를 생성하게 되는데, 이러한 여기자가 낮은 에너지의 바닥상태로 떨어지면서 이 과정에서의 에너지에 의해 사각형 모양의 각 화소가 빛을 발생시키게 된다.

그런데, 상기 종래의 유기 발광 소자에서는 각 화소가 사각형 모양으로 형성되기 때문에, 각 화소의 결합에 의해 직선 및 직각을 포함하는 사각형 윤곽의 글자 또는 그림을 표시하는데는 유리하지만, 곡선을 포함하는 라운드형 윤곽의 글자 또는 그림을 표시하는데에는 불리하다.

특히, 상기 종래 기술에 의한 사각형 모양의 화소를 포함하는 유기 발광 소자로, 곡선을 포함하는 라운드형 윤곽의 글자 또는 그림 등을 표시하게 되면, 곡선 부분이 각 사각형 모양 화소의 조합으로 표시될 수 밖에 없기 때문에, 상기 라운드형 윤곽의 글자 또는 그림 등이 선명하게 표시되지 못하는 문제점이 발생한다.

이러한 종래 기술의 문제점으로 인하여, 곡선을 포함하는 라운드형 윤곽의 그림 또는 글자 또한 선명하게 표시할 수 있도록 하는 신규한 유기 발광 소자의 개발이 계속적으로 요구되어 왔다.

발명이 이루고자 하는 기술적 과제

이에 본 발명은 상기와 같은 종래 기술의 문제점을 해결하기 위하여, 곡선을 포함하는 라운드형 윤곽의 그림 또는 글자 또한 선명하게 표시할 수 있는 유기 발광 소자를 제공하기 위한 것이다.

발명의 구성

상기의 목적을 달성하기 위하여, 본 발명은 투명 기판 위에 한 쪽 방향으로 배열되는 복수의 제 1 전극과, 상기 투명 기판 및 복수의 제 1 전극 위에 복수의 육각형이 모인 벌집 형태로 형성되어 상기 복수의 제 1 전극 상에 육각형 모양의 화소를 정의하는 절연막과, 상기 육각형 모양 화소의 상기 제 1 전극 위에 순차 형성되는 유기 박막층 및 제 2 전극과, 상기 제 1 전극이 배열된 한 쪽 방향을 따라 서로 인접하는 화소 간의 제 2 전극의 단락을 방지하도록 소정 영역의 상기 절연막 위에 형성되는 격벽을 포함하는 유기 발광 소자를 제공한다.

상기 본 발명에 의한 유기 발광 소자에서는 각 화소가 육각형 모양으로 형성되어 있는 바, 이러한 육각형 모양 화소의 조합에 의해 곡선을 보다 실제 곡선에 가까운 윤곽 형태로 부드럽게 표시할 수 있게 되므로, 곡선을 포함하는 라운드형 윤곽의 글자 또는 그림을 보다 선명하게 표시할 수 있다.

상기 본 발명에 의한 유기 발광 소자에서, 상기 복수의 제 1 전극 상의 육각형 모양의 각 화소는 적색(R), 녹색(G) 및 청색(B)를 각각 표시하기 위한 세 개의 부화소를 포함할 수 있는데, 여기서 세 개의 부화소는 동일한 면적으로 형성될 수도 있고, 서로 다른 면적으로 형성될 수도 있다.

그런데, 적색(R), 녹색(G) 및 청색(B)를 표시하기 위한 각 부화소를 형성하기 위해서는 각 색채의 빛을 발생시킬 수 있는 형광 또는 인광 물질을 사용하여 유기 박막층 중의 유기 발광층을 형성하지 않으면 안되는데, 현재까지 개발된 청색 형광 또는 인광 물질은 다른 색채의 빛을 내는 형광 또는 인광 물질에 비해 짧은 수명을 가지므로, 청색 부화소를 적색 및 녹색 부화소보다 작은 면적으로 형성함으로서, 유기 발광 소자의 전체적인 수명을 연장시킬 수 있어서 보다 바람직하다.

이하 첨부한 도면을 참고로 본 발명의 일 실시예에 따른 유기 발광 소자의 구조에 대하여 본 발명이 속하는 기술 분야에서 통상의 지식을 가진 자가 용이하게 실시할 수 있도록 상세히 설명한다.

도면에서는 여러 층 및 영역을 명확하게 표현하기 위하여 두께를 확대하여 나타내었다. 또한, 본 명세서 전체를 통하여 유사한 부분에 대해서는 동일한 도면 부호를 붙였다.

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도 1은 본 발명의 일 실시예에 따른 유기 발광 소자의 구조를 개략적으로 나타낸 평면도이고, 도 2는 도 1의 A-A'선을 따라 잘라 도시한 단면도로서, 본 발명의 일 실시예에 따른 유기 발광 소자의 구조를 개략적으로 나타낸 단면도이다.

도 1 및 도 2를 참조하면, 본 발명의 일 실시예에 따른 유기 발광 소자에서는, 투명한 글라스 또는 플라스틱 등으로 이루어진 투명 기판(100) 위에 ITO(indium tin oxide) 또는 IZO(indium-doped zinc oxide or IXO) 등의 투명 도전 물질로 이루어지는 복수의 제 1 전극(110)이 양전극층으로서 투명 기판의 어느 한 쪽 방향으로 배열되어 있다.

보다 상세히 설명하면, 본 실시예에 의한 유기 발광 소자에서는 육각형 모양의 각 화소가 적색(R), 녹색(G) 및 청색(B)을 각각 표시하기 위한 세 개의 부화소를 포함하고 있는데(이러한 화소의 구성에 대해서는 이하에서 보다 상술하기로 한다.), 상기 복수의 제 1 전극(110)은 세 개씩의 제 1 전극(110)이 한 세트로 되어, 이중 첫 번째 제 1 전극(110)이, 예를 들어, 적색 부화소가 형성될 영역과 대응하도록 각 육각형 모양 화소의 윗변을 따라 지그재그 형태로 투명 기판(100)의 한 쪽 방향으로 배열되어 있고, 두 번째 제 1 전극(110)이, 예를 들어, 녹색 부화소가 형성될 영역과 대응하도록 각 육각형 모양 화소의 중앙부를 가로질러 투명 기판(100)의 한 쪽 방향으로 배열되어 있으며, 세 번째 제 1 전극(110)이, 예를 들어, 청색 부화소가 형성될 영역과 대응하도록 각 육각형 모양 화소의 아랫변을 따라 지그재그 형태로 투명 기판(100)의 한 쪽 방향으로 배열되어 있다.

다만, 본 발명의 다른 실시예로서, 각 육각형 모양의 화소 영역에서 상기 세 개의 각 부화소에 대응하는 세 개의 제 1 전극(110)이 한 세트로 배열되는 상기 본 실시예의 구성과 달리, 각 육각형 모양의 화소 영역에 대응하는 하나씩의 제 1 전극(110)이 투명 기판의 한 쪽 방향으로 늘어선 줄무늬 형태로 배열될 수도 있다.

한편, 상기 투명 기판(100) 및 제 1 전극(110) 위에는 복수의 육각형이 모인 벌집 형태로 절연막(120)이 형성되어 있다. 이러한 절연막(120)에 의해 상기 복수의 제 1 전극(110) 상에 육각형 모양의 개구부가 정의되는데, 이러한 개구부에 바로 유기 발광 소자의 각 화소가 형성된다.

상기 절연막(120)은 제 1 전극(110) 위에 형성되어 있는 유기 박막층(130) 및 제 2 전극(140)이 절연막(120)을 타고 넘어갈 수 있도록, 단면으로 보아 정경사(positive profile)을 가지도록 형성되어 있다(도 2 참조). 이러한 절연막(120)은 통상적인 유기 발광 소자의 구성에 따라, 감광막 등의 절연 물질로 이루어진다.

본 실시예에서는 상기 절연막(120)에 의해 제 1 전극(110) 상의 각 화소가 사각형이 아닌 육각형 모양으로 정의되므로, 이러한 육각형 모양 화소의 조합에 의해 라운드형 윤곽의 글자 또는 그림에 포함된 곡선을 보다 실제 곡선에 가까운 윤곽 형태로 부드럽게 표현할 수 있다. 따라서, 본 실시예에 의한 유기 발광 소자는 곡선을 포함하는 라운드형 윤곽의 글자 또는 그림을 보다 선명하게 표시할 수 있게 된다.

한편, 상기 절연막(120)에 의해 정의된 육각형 모양 화소의 상기 제 1 전극(110) 위에는, 유기 발광층 등을 포함하는 유기 박막층(130) 및 음전극층으로서의 제 2 전극(140)이 순차 형성되어 있다.

도 1에 도시된 바와 같이, 상기 유기 박막층(130) 및 제 2 전극(140)은 상기 제 1 전극(110)이 배열된 한 쪽 방향과 수직하는 방향으로 정경사를 띄는 절연막(120)을 타고 지그재그로 연결되게 형성되어 있다(도 1의 화살표 - 유기 박막층 및 제 2 전극의 형성 방향 참조).

그리고, 상기 유기 박막층(130)은 유기 발광층 이외에도 제 1 전극(110)으로부터 유기 발광층으로의 정공 전달을 보조하는 정공 주입층 및 정공 수송층과, 제 2 전극으로부터 유기 발광층으로의 전자 전달을 보조하는 전자 주입층 및 전자 전달층 등의 유기 박막을 더 포함할 수도 있다. 이러한 정공 주입층, 정공 수송층, 전자 주입층 및 전자 수송층은 당업자에게 자명한 유기 발광 소자의 통상적인 구성에 따라 종래부터 사용되어 오던 모든 물질을 사용하여 형성할 수 있다.

또한, 상기 유기 박막층(130) 중의 유기 발광층은 Alq_3, Anthrancene $Ir(ppy)_3$ 와 같은 저분자 형광 또는 인광 물질이나, PPV(p-phenylenevinylene), PT(polythiophene) 또는 이들의 유도체와 같은 고분자 발광 물질을 사용하여 형성할 수 있으며, 기타 종래부터 유기 발광층에 사용되어 오던 유기계 형광 또는 인광 물질을 모두 사용하여 형성할 수 있다.

그리고, 본 실시예에서, 이러한 유기 발광층은 적색(R), 녹색(G) 및 청색(B)의 빛을 내는 형광 또는 인광 물질을 사용하여 세 부분으로 나누어 형성되는데, 이러한 경우 각 색채의 빛을 내는 세 부분의 유기 발광층에 의해 육각형 모양 화소 내의 세 개의 부화소가 정의된다.

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즉, 상기 각 육각형 모양 화소 영역에서 한 세트를 이루는 세 개의 제 1 전극(110) 중, 각 육각형 모양의 화소 윗변을 따라 지그재그로 배열되어 있는 첫 번째 제 1 전극(110) 위에, 예를 들어, 적색광을 내는 유기 발광층이 형성됨으로서, 적색 부화소가 정의될 수 있으며, 각 육각형 모양 화소의 중앙부를 가로질러 배열되어 있는 두 번째 제 1 전극(110) 위에, 예를 들어, 녹색광을 내는 유기 발광층이 형성됨으로서, 녹색 부화소가 정의될 수 있고, 각 육각형 모양 화소의 아랫변을 따라 지그재그 형태로 배열되어 있는 세 번째 제 1 전극(110)위에, 예를 들어, 청색광을 내는 유기 발광층이 형성됨으로서 청색 부화소가 정의될 수 있다.

다만, 본 발명의 다른 실시예로서, 각 육각형 모양 화소 영역에 대응하는 줄무늬 형태의 하나씩의 제 1 전극(110)이 형성되어 있는 경우에는, 상기 각 육각형 모양 화소 영역의 하나의 제 1 전극(110) 위에 영역이 나뉘어 적색, 녹색 및 청색의 빛을 내는 각 유기 발광층이 형성됨으로서, 적색, 녹색 및 청색의 각 색채의 빛을 내는 세 개의 부화소가 정의될 수도 있다.

이러한 각 부화소는 동일한 면적으로 형성될 수도 있고, 서로 다른 면적으로 형성될 수도 있는데, 현재까지 개발된 청색 형광 또는 인광 물질은 다른 색채, 즉, 적색 또는 녹색의 빛을 내는 다른 형광 또는 인광 물질에 비해 짧은 수명을 가지므로, 청색 부화소를 적색 및 녹색 부화소보다 작은 면적으로 형성함으로서, 본 실시예에 따른 유기 발광 소자의 전체적인 수명을 연장시킬 수 있어서 보다 바람직하다.

또한, 상기 제 2 전극(140)은 유기 발광 소자의 음전극층으로서 당업자에게 자명한 통상적인 유기 발광 소자의 구성에 따라, 전기 전도도가 양호한 저저항 금속 물질, 예를 들면 Al, Li/Al, Mg/Ag 또는 Ca 등을 사용하여 형성할 수 있다.

한편, 상기 제 1 전극(110) 상의 육각형 모양 화소를 정의하는 소정 영역의 절연막(120) 위에는, 상기 제 1 전극(110)이 배열된 방향을 따라 서로 인접하는 화소에 각각 형성된 제 2 전극(140) 간의 단락을 방지하기 위한 격벽(150)이 형성되어 있다. 이러한 격벽(150)은 도 1에 도시된 바와 같이, 상기 제 1 전극(110)이 배열된 방향과 수직한 방향으로 연결되도록, 상기 육각형 모양으로 형성된 절연막(120)의 소정 영역 위에 형성되어 있다.

또한, 이러한 격벽(150)은 도 2에 도시된 바와 같이, 단면으로 보아 역경사(negative profile)를 가지는 오버행(overhang) 구조로 형성되어 있다. 이러한 오버행 구조의 격벽에 의한 그림자 효과에 따라, 제 1 전극(110)이 배열된 방향을 따라 서로 인접하는 화소에 각각 형성된 제 2 전극(140)이 서로 연결 또는 단락될 수 없게 된다.

이러한 격벽(150)은 당업자에게 자명한 통상적인 유기 발광 소자의 구성에 따라, 상기 절연막(120)과 마찬가지로 감광막 등의 절연 물질로 형성될 수 있다.

이러한 본 실시예의 유기 발광 소자의 구성에 따르면, 유기 박막층(130) 중의 정공 주입층 및 정공 수송층의 보조를 받아 제 1 전극(110)으로부터 정공이 유기 발광층으로 이동하고, 전자 주입층 및 전자 수송층의 보조를 받아 제 2 전극(140)으로부터 전자가 유기 발광층으로 이동한다. 이러한 전자가 정공이 유기 발광층 내에서 서로 만나 전자-정공 쌍을 형성하고 높은 에너지를 갖는 여기자를 생성하게 되는데, 이러한 여기자가 낮은 에너지의 바닥상태로 떨어지면서 이 과정에서의 에너지에 의해 유기 발광 소자의 각 화소가 빛을 발생시키게 된다.

그런데, 본 실시예에서는 각 화소가 사각형 모양이 아닌, 육각형 모양을 띄게 됨에 따라, 이러한 육각형 모양 화소의 조합에 의해 곡선을 보다 실제 곡선에 가까운 윤곽으로 부드럽게 표시할 수 있다. 따라서, 본 실시예에 따르면, 곡선을 포함하는 라운드형 글자 또는 그림을 보다 선명하게 표시할 수 있게 된다.

이상에서 본 발명의 바람직한 실시예에 대하여 상세하게 설명하였지만 본 발명의 권리범위는 이에 한정되는 것은 아니고 다음의 청구범위에서 정의하고 있는 본 발명의 기본 개념을 이용한 당업자의 여러 변형 및 개량 형태 또한 본 발명의 권리범위에 속하는 것이다.

발명의 효과

상기한 바와 같이, 본 발명에 따르면, 곡선을 포함하는 라운드형 글자 또는 그림을 보다 선명하게 표시할 수 있으므로, 유기 발광 소자 및 이를 이용한 각종 표시 장치의 품질 향상에 크게 기여할 수 있다.

도면의 간단한 설명

도 1은 본 발명의 일 실시예에 따른 유기 발광 소자의 구조를 개략적으로 나타낸 평면도이다.

도 2는 도 1의 A-A'선을 따라 잘라 도시한 단면도로서, 본 발명의 일 실시예에 따른 유기 발광 소자의 구조를 개략적으로 나타낸 단면도이다.

- 도면의 주요부분에 대한 부호의 설명 -

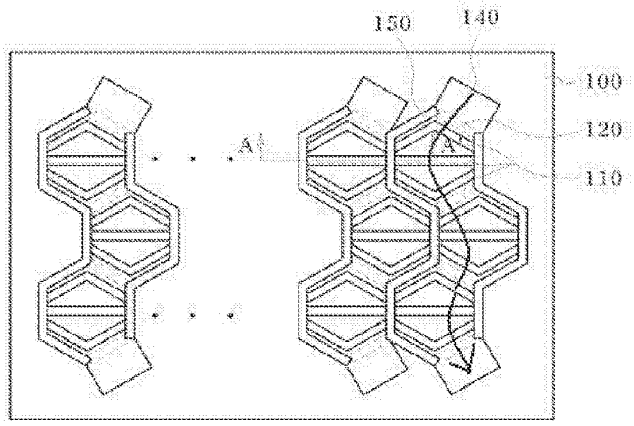
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120 : 절연막 130 : 유기 박막층

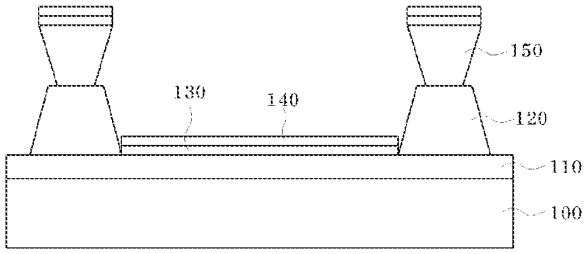
140 : 제 2 전극 150 : 격벽

도면

도면1



도면2



BOE
Exhibit 1003 Page 407

Electronic Patent Application Fee Transmittal

Application Number:	17808982
Filing Date:	24-Jun-2022
Title of Invention:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Sang-Shin LEE
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Attorney Docket Number:	224123/411598-06419

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt	
EFS ID:	47049625
Application Number:	17808982
International Application Number:	
Confirmation Number:	4376
Title of Invention:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Sang-Shin LEE
Customer Number:	23363
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Filer Authorized By:	Jun-Young E. Jeon
Attorney Docket Number:	224123/411598-06419
Receipt Date:	17-NOV-2022
Filing Date:	24-JUN-2022
Time Stamp:	21:12:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$260
RAM confirmation Number	E2022AGL12512798
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	224123_IDS.pdf	1043026 664a4e269c98e598bbb6626022222c04e3e8bf6a	no	6
Warnings:					
Information:					
2	Other reference-Patent/Application/ Search Documents	11-3-22_OA_224129.pdf	1432990 898629bea6f62d61fb909b7c276ab69cabc226fd	no	25
Warnings:					
Information:					
3	Other reference-Patent/Application/ Search Documents	11-10-22_OA_224702.pdf	1311057 82da8986bdd3238bb8edee11ee38be3069857112	no	23
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Information:					
4	Other reference-Patent/Application/ Search Documents	CN_OA_9-13-22_40602.pdf	1116082 10f422429cfd089b51471891af815d92a9370e9f	no	9
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5	Foreign Reference	EP_408.pdf	900339 a62517184c533e8cdf3f969b6a78045d3943dad7	no	24
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Information:					
6	Foreign Reference	EP_448.pdf	3352896 ab97991ff77a336239e67a037770df97f69e8e85	no	34
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Information:					

7	Foreign Reference	JP_264.pdf	807452 f873558cf336340082903c0db5d7c1e98df039cd	no	27
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8	Foreign Reference	JP_276.pdf	182135 17fb59af5aa6b07d5a8014926601660280e28259	no	7
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9	Foreign Reference	JP_416.pdf	678980 40a9b33f25f3662547d40f84f01e12d8e4867934	no	29
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14	Fee Worksheet (SB06)	fee-info.pdf	38361 dc6c5d53c328e9be17142b50d2f915e81e6a4341	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	16688428	

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17808982
Filing Date	2022-06-24
First Named Inventor	Sang-Shin Lee
Art Unit	2691
Examiner Name	YANG, KWANG-SU
Attorney Docket Number	224123/411598-06419

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	YANG, KWANG-SU
	Attorney Docket Number	224123/411598-06419

	1	US Notice of Allowance dated December 23, 2022, issued in US Patent Application No. 16/505,536 (9 pages)	
	2	US Final Office Action dated January 4, 2023, issued in US Patent Application No. 17/808,985 (27 pages)	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	YANG, KWANG-SU
	Attorney Docket Number	224123/411598-06419

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2023-01-11
Name/Print	Jun-Young E. Jeon	Registration Number	43693

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	47357456
Application Number:	17808982
International Application Number:	
Confirmation Number:	4376
Title of Invention:	PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY
First Named Inventor/Applicant Name:	Sang-Shin LEE
Customer Number:	23363
Filer:	Jun-Young E. Jeon/Elizabeth Gomez
Filer Authorized By:	Jun-Young E. Jeon
Attorney Docket Number:	224123/411598-06419
Receipt Date:	11-JAN-2023
Filing Date:	24-JUN-2022
Time Stamp:	23:20:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	224123_IDS.pdf	1042036 82f7aea97ed84785254c5cb1a42b9463f600ba9d	no	4

Warnings:

Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Other reference-Patent/Application/ Search Documents	1-4-23_FOA_224130.pdf	1494028 de7b700aab7a081fb0390e8f0dcc5a75a5fc834c	no	27
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Information:					
3	Other reference-Patent/Application/ Search Documents	12-23-22_NOA_174060.pdf	725197 cceea567d0dd740f20b14242900c13b198926dad	no	9
Warnings:					
Information:					
		Total Files Size (in bytes):	3261261		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/808,982	Filing Date 06/24/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	01/17/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 30	Minus	** 25	= 5		x $100 =	500
	Independent (37 CFR 1.16(h))	* 2	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	500

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/KIMBERLY N PANNELL/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office on January 17, 2023 at or before 11:59 p.m. Mountain Standard Time under the Rules of 37 CFR § 1.8.

/Rose Liu/
Signature

Appl No.	: 17/808,982	Confirmation No. 4376
Inventor	: Sang-Shin Lee	
Filed	: June 24, 2022	
Title	: PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	
TC/A.U.	: 2691	
Examiner	: Yang, Kwang-Su	
Docket No.	: 224123/411598-06419	
Customer No.	: 23363	

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
January 17, 2023

Commissioner:

In response to the Office action of October 14, 2022, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks/Arguments begin on page 11 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An organic light emitting diode (OLED) display, comprising:

a plurality of individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display and comprising:

a plurality of red pixels comprising an organic emission layer for emitting red light;

a plurality of blue pixels comprising an organic emission layer for emitting blue light; and

a plurality of green pixels comprising an organic emission layer for emitting green light[[;]],

wherein the OLED display comprises a pixel defining layer defining areas of the plurality of red pixels, the plurality of blue pixels, and the plurality of green pixels,

wherein each of the plurality of red pixels, the plurality of blue pixels, and the plurality of green pixels are spaced apart from each other[[;]],

wherein a first [[one]] green pixel of the plurality of green pixels has a center coinciding with a center of a virtual square, each vertex of the virtual square coinciding with a center of a different one of the plurality of green pixels and each edge of the virtual square ~~passing through~~ overlapping three consecutive green pixels[[;]],

wherein at least two blue pixels of the plurality of blue pixels and at least two red pixels of the plurality of red pixels are located entirely within [[the]] boundaries of the virtual square[[;]],

~~wherein a shortest distance between the first green pixel and one of the at least two blue pixels within the virtual square as well as a shortest distance between the first green pixel and one of the at least two red pixels within the virtual square is a same first length;~~

~~wherein the first length is smaller than a shortest distance between the first green pixel and an adjacent one of the green pixels;~~

wherein each of the at least two blue pixels has a larger area than each of the at least two red pixels[[;]].

wherein each of the at least two blue pixels has a larger area than that of the first green pixel[[; and]].

wherein the first green pixel has a convex shape such that a line bisecting the first green pixel along [[its]] a long axis thereof has a greater length than a line bisecting the first green pixel along [[its]] a short axis thereof, and

wherein a shortest distance between two nearest ones of the plurality of green pixels is greater than a width of a first red pixel of the plurality of red pixels along a first direction parallel to the short axis of the first green pixel.

2. (Currently Amended) The display of claim 1, wherein ~~the first length is smaller than~~ a shortest distance between one of the at least two blue pixels and one of the at least two red pixels is greater than a shortest distance between the first green pixel and the one of the at least two blue pixels or a shortest distance between the first green pixel and the one of the at least two red pixels.

3. (Currently Amended) The display of claim 2, wherein the first green pixel has a different shape than the one of the at least two blue pixels and the one of the at least two red pixels.

4. (Currently Amended) The display of claim 2, wherein the one of the at least two red pixels has ~~a larger area~~ an area that is larger than that of the first green pixel.

5. (Currently Amended) The display of claim 2, wherein the one of the at least two blue pixels and the one of the at least two red pixels ~~are four-sided polygons~~ have polygonal shapes with at least four sides.

6. (Currently Amended) The display of claim 1, wherein ~~the first length is equal to~~ a shortest distance between one of the at least two blue pixels and one of the at least two red pixels is equal to a shortest distance between the first green pixel and the one of the at least two blue pixels or a shortest distance between the first green pixel and the one of the at least two red pixels.

7. (Currently Amended) The display of claim 6, wherein the first green pixel has a different shape than the one of the at least two blue pixels and the one of the at least two red pixels.

8. (Currently Amended) The display of claim 6, wherein the one of the at least two red pixels has ~~a larger area~~ an area that is larger than that of the first green pixel.

9. (Currently Amended) The display of claim 6, wherein the one of the at least two blue pixels and the one of the at least two red pixels ~~are four-sided polygons~~ have polygonal shapes with at least four sides.

10. (Currently Amended) A method for manufacturing an organic light emitting diode (OLED) display, comprising:

depositing, using a fine metal mask, organic light-emitting material configured to emit a first color of light;

forming a plurality of first pixels to emit the first color of light;

depositing, using a fine metal mask, organic light-emitting material configured to emit a second color of light;

forming a plurality of second pixels to emit the second color of light;

depositing, using a fine metal mask, organic light-emitting material configured to emit a third color of light; and

forming a plurality of third pixels to emit the third color of light[[;]].

~~wherein:~~

wherein the plurality of first pixels, the plurality of second pixels, and the plurality of third pixels are individually addressable pixels for displaying an image, the individually addressable pixels being minimum addressable units of the OLED display[[;]].

wherein the OLED display comprises a pixel defining layer defining areas of the plurality of first pixels, the plurality of second pixels, and the plurality of third pixels,

wherein each of the plurality of first pixels, the plurality of second pixels, and the plurality of third pixels are spaced apart from each other[[;]].

wherein a first one of the plurality of first pixels has a center coinciding with a center of a virtual square, each vertex of the virtual square coinciding with a center of a different one of the plurality of first pixels and each edge of the virtual square ~~passing through~~ overlapping three consecutive first pixels[[;]].

wherein at least two second pixels of the plurality of second pixels and at least two third pixels of the plurality of third pixels are located entirely within [[the]] boundaries of the virtual square[[;]].

~~wherein a shortest distance between the one of the first pixels and one of the at least two second pixels within the virtual square as well as a shortest distance between the one of the first pixels and one of the at least two third pixels within the virtual square is a same first length;~~

~~wherein the first length is smaller than a shortest distance between the one of the first pixels and an adjacent one of the first pixels;~~

wherein each of the at least two second pixels has a larger area than each of the at least two third pixels[[;]].

wherein each of the at least two second pixels has a larger area than that of the first one of the plurality of first pixels[[; and]].

wherein the first one of the plurality of first pixels has a convex shape such that a line bisecting the first one of the plurality of first pixels along [[its]] a long axis thereof has a greater length than a line bisecting the first one of the plurality of first pixels along [[its]] a short axis thereof, and

wherein a shortest distance between two nearest ones of the plurality of first pixels is greater than a width of one of the third pixels along a first direction parallel to the short axis of the first one of the plurality of first pixels.

11.-13. (Cancelled)

14. (Currently Amended) The method of claim 10, wherein the first one of the plurality of first pixels has a different shape than ~~the~~ one of the at least two second pixels and ~~the~~ one of the at least two third pixels.

15. (Currently Amended) The method of claim 10, wherein ~~the~~ one of the at least two third pixels has ~~a larger area~~ an area that is larger than that of the first one of the plurality of first pixels.

16. (Currently Amended) The method of claim 10, wherein ~~the~~ one of the at least two second pixels and ~~the~~ one of the at least two third pixels ~~are four-sided polygons~~ have polygonal shapes with at least four sides.

17. (Currently Amended) The method of claim 10, wherein the plurality of first pixels ~~include~~ comprises an organic emission layer for emitting green light, the plurality of second pixels ~~include~~ comprises an organic emission layer for emitting blue light, and the plurality of third pixels ~~include~~ comprises an organic emission layer for emitting red light.

18. (Currently Amended) The method of claim 17, wherein ~~the first length is smaller than~~ a shortest distance between ~~the~~ one of the at least two second pixels and ~~the~~ one of the at least two third pixels is greater than a shortest distance between the first one of the plurality of first pixels and the one of the at least two second pixels or a shortest distance between the first one of the plurality of first pixels and the one of the at least two third pixels.

19. (Currently Amended) The method of claim 18, wherein the first one of the plurality of first pixels has a different shape than the one of the at least two second pixels and the one of the at least two third pixels.

20. (Currently Amended) The method of claim 18, wherein the one of the at least two third pixels has ~~a larger area~~ an area that is larger than that of the first one of the plurality of first pixels.

21. (Currently Amended) The method of claim 18, wherein the one of the at least two second pixels and the one of the at least two third pixels ~~are four-sided polygons~~ have polygonal shapes with at least four sides.

22. (Currently Amended) The method of claim 17, wherein ~~the first length is equal to~~ a shortest distance between ~~the~~ one of the at least two second pixels and ~~the~~ one of the at least two third pixels is equal to a shortest distance between the first one of the plurality of first pixels and the one of the at least two second pixels or a shortest distance between the first one of the plurality of first pixels and the one of the at least two third pixels.

23. (Currently Amended) The method of claim 22, wherein the first one of the plurality of first pixels has a different shape than the one of the at least two second pixels and the one of the at least two third pixels.

24. (Currently Amended) The method of claim 22, wherein the one of the at least two third pixels has ~~a larger area~~ an area that is larger than that of the first one of the plurality of first pixels.

25. (Currently Amended) The method of claim 22, wherein the one of the at least two second pixels and the one of the at least two third pixels ~~are four-sided polygons~~ have polygonal shapes with at least four sides.

26. (New) The display of claim 1, wherein a shortest distance between the first green pixel and an adjacent one of the plurality of green pixels is greater than a shortest distance between the first green pixel and one of the at least two blue pixels or a shortest distance between the first green pixel and one of the at least two red pixels.

27. (New) The display of claim 1, wherein a shortest distance between the first green pixel and one of the at least two blue pixels is equal to a shortest distance between the first green pixel and one of the at least two red pixels.

28. (New) The display of claim 1, wherein a shortest distance between the first green pixel and an adjacent one of the plurality of green pixels is not equal to a shortest distance between one of the at least two blue pixels and one of the at least two red pixels.

29. (New) The display of claim 1, wherein a width of the first green pixel along the short axis of the first green pixel is different from a width of one of the at least two red pixels along the first direction, or a width of the first green pixel along the long axis of the first green pixel is different from a width of one of the at least two blue pixels along a second direction parallel to the long axis of the first green pixel.

30. (New) The display of claim 1, wherein a shortest distance between the two nearest ones of the plurality of green pixels is greater than a width of the first red pixel along a second direction parallel to the long axis of the first green pixel.

31. (New) The method of claim 10, wherein a shortest distance between the first one of the plurality of first pixels and an adjacent one of the plurality of first pixels is not equal to a shortest distance between one of the at least two second pixels and one of the at least two third pixels.

32. (New) The method of claim 10, wherein a width of the first one of the plurality of first pixels along the short axis of the first one of the plurality of first pixels is

different from a width of one of the at least two third pixels along the first direction, or a width of the first one of the plurality of first pixels along the long axis of the first one of the plurality of first pixels is different from a width of one of the at least two second pixels along a second direction parallel to the long axis of the first one of the plurality of first pixels.

33. (New) The method of claim 10, wherein a shortest distance between the two nearest ones of the plurality of first pixels is greater than a width of the one of the third pixels along a second direction parallel to the long axis of the first one of the plurality of first pixels.

REMARKS/ARGUMENTS

Claims 1-10 and 14-33 are pending, with claims 1 and 10 being independent. Claims 11-13 have been cancelled without prejudice or disclaimer. Claims 1-10 and 14-25 have been amended. Claims 26-33 have been added. No new subject matter has been added. Full support for the amendments to the claims may be found throughout the present application as originally filed. In view of the amendments and remarks made herein, Applicant respectfully requests reconsideration and allowance of claims 1-10 and 14-25, and consideration and allowance of new claims 26-33.

Objection to the Claims

Claims 1-25 were objected to because of alleged informalities. In the interest of expediting allowance of the present application, and without conceding to the correctness of the Office action, Applicant has amended claims 1, 4, 8, 10, 15, and 20, and Applicant respectfully requests, in view of the amendments made herein to the claims, that the objection to the claims be withdrawn.

Provisional Nonstatutory Double Patenting Rejections

Claims 1-7, 9-19, 21-23, and 25 were provisionally rejected on the ground of nonstatutory double patenting as allegedly being unpatentable over claims 1, 3-16, 20, and 23-28 of copending Application No. 17/808,983 in view of Phan (U.S. Pat. 7,215,347 B2), hereinafter Phan.

Applicant respectfully disagrees with the Examiner's characterization of Phan and what it discloses or teaches. Nonetheless, in the interest of expediting allowance of the present application, and without conceding to the correctness of the Office action, Applicant has amended independent claims 1 and 10, and Applicant respectfully submits that claims 1-10 and 14-33 are not unpatentable over the claims of copending Application No. 17/808,983 in view of Phan. Furthermore, because the final subject matter of the present application and of copending Application No. 17/808,983 has not been determined, Applicant hereby reserves the right to file a terminal disclaimer if required during the prosecution of the present application to, for example, expedite allowance.

Rejections under 35 USC § 112

Claims 11-13 were rejected under 35 U.S.C. § 112(a) as allegedly failing to comply with the written description requirement.

Applicant has cancelled claims 11-13 herein, without prejudice. Therefore, the rejections of claims 11-13 under 35 U.S.C. § 112 are now moot.[1]

Rejections under 35 U.S.C. § 102 or § 103

Claims 1-3 and 5 were rejected under 35 U.S.C. § 102(a)(1) as allegedly being anticipated by Phan.

Claims 10, 14, 16-19, and 21 were rejected under 35 U.S.C. § 103 as allegedly being unpatentable over Shim et al. (U.S. Pub. 2014/0191202 A1), hereinafter Shim, in view of Phan.

Applicant respectfully disagrees with the Examiner's characterization of Phan and what it discloses or teaches. Nonetheless, in the interest of expediting allowance of the present application, and without conceding to the correctness of the Office action (with which Applicant respectfully disagrees), Applicant has amended claim 1 to recite, in part (**emphasis** added): "**wherein the OLED display comprises a pixel defining layer defining areas of the plurality of red pixels, the plurality of blue pixels, and the plurality of green pixels**," and "wherein the first green pixel has a convex shape such that a line bisecting the first green pixel along a long axis thereof has a greater length than a line bisecting the first green pixel along a short axis thereof, and **wherein a shortest distance between two nearest ones of the plurality of green pixels is greater than a width of a first red pixel of the plurality of red pixels along a first direction parallel to the short axis of the first green pixel**."

Applicant respectfully submits that Phan does not disclose or even suggest at least the above-recited features of amended claim 1. For example, in rejecting claim 1, page 11 of the Office action appears to equate the green dots G, the blue dots B, and the red

[1] Box No. 10 of the Office action has been checked. Box No. 10 recites: "The specification is objected to by the Examiner." However, the Office action does not appear to describe any explicit objection to the specification. Therefore, Applicant understands that the Office action's objection to the specification is associated with its rejection of claims 11-13 under 35 U.S.C. § 112 for allegedly failing to satisfy the written description requirement. Accordingly, because the rejections of claims 11-13 under 35 U.S.C. § 112 have been rendered moot, the objection to the specification is also rendered moot.

dots R of Phan to the plurality of green pixels, the plurality of blue pixels, and the plurality of red pixels, respectively, of claim 1. The Office action also alleges on page 13 that Phan teaches, "wherein the first green pixel (e.g., the green dot at (3,4) which matches the left lower green dot in Fig. 11b) has a convex shape such that a line bisecting the first pixel along its long axis (a horizontal axis) has a greater length than a line bisecting the first pixel along its short axis (a vertical axis) (Figs. 9.8, 11b and 12)." FIG. 11b of Phan is reproduced below for reference.

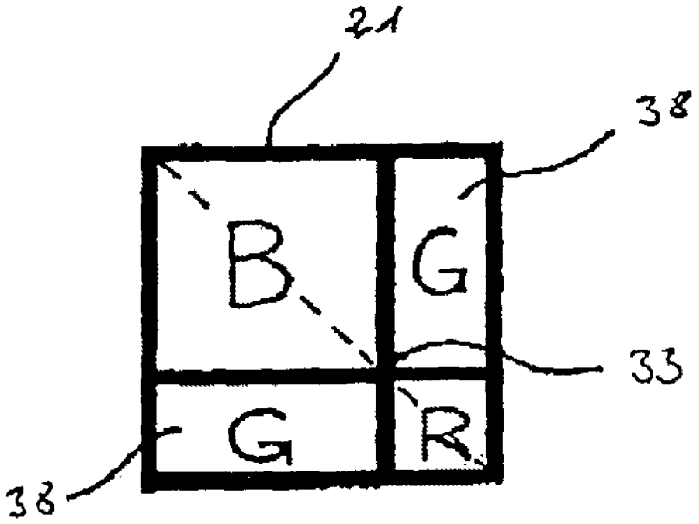


FIG 11b

However, FIG. 11B of Phan does not disclose or suggest, among other things, that a shortest distance between two nearest ones of the plurality of green dots G is greater than a width of the red dot R along a first direction parallel to the vertical axis of the left lower green dot in FIG. 11b of Phan (equated to the short axis of the first green pixel). Phan also does not disclose or suggest that a pixel defining layer defines the areas of green dots G, blue dots B, and red dots R.

Therefore, Phan does not disclose or otherwise suggest a display according to amended claim 1 including at least "wherein the OLED display comprises a pixel defining layer defining areas of the plurality of red pixels, the plurality of blue pixels, and the plurality of green pixels," and "wherein a shortest distance between two nearest ones of

the plurality of green pixels is greater than a width of a first red pixel of the plurality of red pixels along a first direction parallel to the short axis of the first green pixel," as is now recited in claim 1.

Moreover, Applicant respectfully submits that Shim does not cure the above-discussed deficiencies of Phan with respect to claim 1, and that a person of ordinary skill in the art at the time of the effective filing date of the present application would have had no reason or motivation to combine Shim with Phan, let alone in the manner alleged in the Office action. In addition, even if a person of ordinary skill in the art had attempted to combine the references, such a combination would not arrive at the claimed embodiment of claim 1 let alone with a reasonable expectation of success.

Therefore, Applicant respectfully submits that claim 1 is patentable over the art of record, and Applicant respectfully requests that the rejection of claim 1 be withdrawn and that this claim also be allowed.

In the interest of expediting allowance of the present application, and without conceding to the correctness of the Office action, Applicant has amended independent claim 10 to include features that are substantially similar to the above-discussed features of claim 1. Therefore, for at least reasons that are substantially similar to those set forth herein regarding why claim 1 is patentable over the art of record, Applicant respectfully submits that independent claim 10 are also patentable over the art of record.

Therefore, Applicant respectfully requests that the rejection of claim 10 be withdrawn and that claim 10 be allowed as well.

Claims 2-9 and 14-33 are also patentable over the art of record because they each depend from claim 1 or claim 10 and for the further features recited therein. Therefore, Applicant respectfully requests that the rejection of, or objection to, each of claims 2-9 and 14-25 be withdrawn and that these claims also be allowed. Applicant also respectfully requests that claims 26-33 be entered, considered, and allowed.

Concluding Remarks

In view of the foregoing amendments and remarks, Applicant earnestly solicits a timely issuance of a Notice of Allowance with claims 1-10 and 14-33. If there are any remaining issues that can be addressed over the telephone, the Examiner is cordially invited to call Applicant's attorney at the number listed below.

Payment of any fee required to enter and process this amendment is provided. The Director is hereby authorized to charge any underpayment of fees or credit any overpayment of fees to Deposit Account No. 03-1728. Please show our docket number with any charge or credit to our Deposit Account.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Steven French/
Steven J. French
Reg. No. 78,743
626-795-9900

SF/rl

UNITED STATES
PATENT AND TRADEMARK OFFICE

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	**01/17/2023 04:20:59 PM ET**	**224123/411598-06419**

Title of Invention

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4376	FILED BY	Rose Liu
PATENT CENTER #	61447551	FILING DATE	06/24/2022
CUSTOMER #	23363	FIRST NAMED INVENTOR	Sang-Shin LEE
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Steven French

Documents

TOTAL DOCUMENTS: 3

DOCUMENT		PAGES	DESCRIPTION	SIZE (KB)
224123.pdf		15	-	139 KB
224123-A....pdf	(1-1)	1	Amendment/Request for Reconsideration-After Non-Final Rejection	106 KB
224123-CLM.pdf	(2-10)	9	Claims	97 KB
224123-REM.pdf	(11-15)	5	Applicant Arguments/Remarks Made in an Amendment	99 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
224123.pdf	3B572F7E67824E7F13F12EF60B49667DE9B346D17D1161291C 43E753715F13F5E0019C42C0E61A4CBA7E05B033ABF4BA8AB DA86011D98E69111A88A6F33FD0F1
224123-A....pdf	A0CF4932A29141B249CEC858D20CA16223E6AA416DB316972 D0CB2A8B93EEA166A262843738008DA45D81DC56F2A9BEBD EBA9AB7C930694917A966B6F3328F64
224123-CLM.pdf	D9E3418DCA63A58DF8275A757FF11DEC780C8A7C65E716440 B870129F53A1347561C199D825ABDB36389A5552258EF493A8 4AAE4D3D5115557167 3DE110E6E15
224123-REM.pdf	30D524F69D015F8B0DB2C03FC1F7106BFE35243342DA95E93 63B905021FE5ED0E24F4EA8C2B409BA3A8F648B54CEB71497 499E7D28CB420287A14501B6BE859B

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	01/17/2023 04:20:59 PM ET	224123/411598-06419

Title of Invention

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Application Information

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CONFIRMATION #	4376	FILED BY	Rose Liu
PATENT CENTER #	61447551	AUTHORIZED BY	Steven French
CUSTOMER #	23363	FILING DATE	06/24/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Sang-Shin LEE

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 4792	E20231GG23421797	Rose Liu

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1202	EACH CLAIM IN EXCESS OF 20	100.00	5	500.00
			TOTAL AMOUNT:	$500.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C.

371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: ECOMM.AUTH/ECOMM.WTDW
Doc Description: Internet Communications Authorization/Internet Communications Authorization Withdrawal

PTO/SB/439 (11-15)

AUTHORIZATION FOR INTERNET COMMUNICATIONS IN A PATENT APPLICATION OR REQUEST TO WITHDRAW AUTHORIZATION FOR INTERNET COMMUNICATIONS		
	Application No.	17/808,982
	Filing Date	06/24/2022
	First Named Inventor	Sang-Shin LEE
	Art Unit	2691
	Examiner Name	Kwang-Su Yang
	Practitioner Docket No.	224123/411598-06419

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. To authorize permission for Internet Communications.

☒ Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned and practitioners in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via video conferencing, instant messaging, or electronic mail. I understand that a copy of these communications will be made of record in the application file. (MPEP 502.03)

II. To withdraw authorization for Internet Communications.

☐ The authorization given on _____, to the USPTO to communicate with the undersigned and any practitioner in accordance with 37 CFR 1.33 and 37 CFR 1.34 concerning any subject matter of this application via Internet communications such as video conferencing, instant messaging, or electronic mail is hereby withdrawn. I understand that the withdrawal is effective when approved rather than when received.

I am the

☐ applicant.

☒ attorney or agent of record. Registration number 78743.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Steven French/ — Signature

January 24, 2023 — Date

Steven French — Typed or printed name

(626) 683-4585 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Juristic entities must be represented by a patent practitioner (see 37 CFR 1.31, which is applicable to any paper filed on or after September 16, 2012, that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	**01/24/2023 12:29:02 PM ET**	**224123/411598-06419**

Title of Invention

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4376	FILED BY	Rose Liu
PATENT CENTER #	61482423	FILING DATE	06/24/2022
CUSTOMER #	23363	FIRST NAMED INVENTOR	Sang-Shin LEE
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Steven French

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
224123.pdf	2	Internet Communications Authorization	182 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
224123.pdf	5E72D9578A6AACB637546118B0DC4C7985141A8157E751508E A9ABD5D906B6E0ABB2CBC9919D532E4F774DE539626983A45 06126E1884AEF794A761B56A3E4D2

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized

by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/808,982	06/24/2022	Sang-Shin LEE	224123/411598-06419	4376

23363 7590 01/30/2023

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
YANG, KWANG-SU	

ART UNIT	PAPER NUMBER
2691	

NOTIFICATION DATE	DELIVERY MODE
01/30/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PLPrivatePair@lrrc.com
pto@lewisroca.com

Applicant-Initiated Interview Summary	**Application No.** 17/808,982	**Applicant(s)** LEE, Sang-Shin		
	Examiner KWANG-SU YANG	**Art Unit** 2691	**AIA (First Inventor to File) Status** Yes	**Page** 1 of 2

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
KWANG-SU YANG	Primary Examiner	Video Conference
JUN YOUNG JEON	Attorney of Record	
STEVEN FRENCH	Attorney of Record	
RYAN SWANK	Attorney of Record	

Date of Interview: 25 January 2023

Issues Discussed:

35 U.S.C. 102

For application number 17/808,982, Applicant added limitations in claim 1 apparently overcome the current 102 rejection; the examiner agrees that that added limitations appear to overcome the reference Phan.

For application number 17/808,983, Applicant added limitations in claim 1 apparently overcome the current 102 rejection; the examiner agrees that that added limitations appear to overcome the reference Phan.

35 U.S.C. 103

For application number 17/808,982, Applicant added limitations in claim 10 apparently overcome the current 103 rejection; the examiner agrees that that added limitations appear to overcome the reference Phan.

For application number 17/808,983, Applicant added limitations in claim 10 apparently overcome the current 103 rejection; the examiner agrees that that added limitations appear to overcome the reference Phan.

Other

For application number 17/005,753, claims 74, 85 and 96 have been discussed. Applicant further amends claim 74 and examiner needs further search/consideration. Applicant further amends claim 85 and explains how the amended limitations overcome the reference Phan; the examiner agrees that the amended limitations appear to overcome the reference Phan. For claim 96, the examiner agrees with the definition of the limitation "shape" as the Applicant explained in the previous interview. The examiner agrees that the amendment appears to overcome the reference Phan.

☑ Attachment

Applicant-Initiated Interview Summary	**Application No.** 17/808,982	**Applicant(s)** LEE, Sang-Shin		
	Examiner KWANG-SU YANG	**Art Unit** 2691	**AIA (First Inventor to File) Status** Yes	**Page** **2 of 2**

/KWANG-SU YANG/ Primary Examiner, Art Unit 2691	
Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04 Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing	

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

APPLICANT INITIATED INTERVIEW REQUEST FORM		
	Inventor	Sang-Shin Lee
	Application No.	17/808,982
	Examiner	Yang, Kwang-Su
	Art Unit	2691
	Status of Application	Published
	Docket Number	224123

Applicant Initiated Interview Request Form

Tentative Participants:

(1) Kwang-Su Yang **(2) Jun Jeon**

(3) Steven French **(4) Ryan Swank**

Proposed Date of Interview: January 25, 2023 **Proposed Time: 12:00 pm ET**

Type of Interview Requested: (1) __ Telephonic (2) ___ Personal (3) _X_ Video Conference

Applicant would like to discuss the amendments and arguments in Applicant's Amendment filed on January 17, 2023.

APPLICANT INITIATED INTERVIEW REQUEST FORM		
	Inventor	Sang-Shin Lee
	Application No.	17/808,982
	Examiner	Yang, Kwang-Su
	Art Unit	2691
	Status of Application	Published
	Docket Number	224123

Applicant Initiated Interview Request Form

Tentative Participants:

(1) Kwang-Su Yang **(2) Jun Jeon**

(3) Steven French **(4) Ryan Swank**

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Applicant would like to discuss the amendments and arguments in Applicant's Amendment filed on January 17, 2023.

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Exhibit 1003 Page 448

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being transmitted via the United States Patent and Trademark Office's patent electronic filing system (Patent Center or EFS-Web) on January 30, 2023 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Rose Liu/
Rose Liu

Inventor(s)	: Sang-Shin Lee	Confirmation No. 4376
Application No.	: 17/808,982	
Filed	: June 24, 2022	
Title	: PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY	
Grp./Div.	: 2691	
Examiner	: Kwang-Su Yang	
Docket No.	: 224123	

INTERVIEW SUMMARY

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
January 30, 2023

Commissioner:

An interview was conducted on January 25, 2023 with Examiner Kwang-Su Yang and Applicant's attorneys, Jun Jeon, Ryan Swank, and Steven French. Applicant thanks the Examiner for the time and courtesy extended to Applicant's attorneys during this interview. During the interview, Applicant's amendments filed on January 17, 2023 were discussed, and the Examiner indicated during the interview that the amendments filed on January 17, 2023 would overcome the current rejections.

Respectfully submitted,
LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Steven French/
Steven J. French
Reg. No. 78,743
626/795-9900

SJF/rl

120060654.1

UNITED STATES
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P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	**01/30/2023 08:15:53 PM ET**	**224123/411598-06419**

Title of Invention

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4376	FILED BY	Rose Liu
PATENT CENTER #	61516730	FILING DATE	06/24/2022
CUSTOMER #	23363	FIRST NAMED INVENTOR	Sang-Shin LEE
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Steven French

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
224123Summary.pdf	1	Miscellaneous Incoming Letter	98 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
224123Summary.pdf	5007155E811AFECD176EBA624DBDA2FB5A3AAE890BE88CED562E6EF22551F70FAC763D7868C7C00D1E178CE81472CE5B09CB1576F2AB0A7B9CCBB2565F4BC0E8

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described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/808,982	LEE, Sang-Shin
	Examiner	**Art Unit**
	KWANG-SU YANG	2691

CPC							
Symbol						**Type**	**Version**
G09G	/	3	/	3208		F	2013-01-01
H10K	/	59	/	352		I	2023-02-01
H10K	/	59	/	353		I	2023-02-01

CPC Combination Sets								
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/KWANG-SU YANG/ Primary Examiner, Art Unit 2691	10 February 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20230210

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Exhibit 1003 Page 452

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/808,982	LEE, Sang-Shin
	Examiner	**Art Unit**
	KWANG-SU YANG	2691

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G09G	/	3	/	3208
H01L	/	27	/	32

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/KWANG-SU YANG/ Primary Examiner, Art Unit 2691	10 February 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20230210

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Exhibit 1003 Page 453

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/808,982	LEE, Sang-Shin
	Examiner	**Art Unit**
	KWANG-SU YANG	2691

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	10	21	19	12	28								
2	2		11	22	20	13	29								
3	3		12	23	21	14	30								
4	4		13	24	22	28	31								
5	5	16	14	25	23	29	32								
6	6	17	15	26	24	30	33								
7	7	18	16	27	25										
8	8	19	17	10	26										
9	9	20	18	11	27										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/KWANG-SU YANG/ Primary Examiner, Art Unit 2691	10 February 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

U.S. Patent and Trademark Office — Part of Paper No.: 20230210

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Exhibit 1003 Page 454

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/808,982	LEE, Sang-Shin
	Examiner	Art Unit
	KWANG-SU YANG	2691

CPC - Searched*		
Symbol	Date	Examiner
G09G3/3208 H01L27/3218 H01L27/3216	10/06/2022	KY

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
PE2E Search: IDS Search	10/06/2022	KY
PE2E Search: Inventor and Assignee Search	10/06/2022	KY
PE2E Search: Text Search	10/06/2022	KY
PE2E Search: IDS Search	02/10/2023	KY
Updated Classification Search (G09G3/3208 H01L27/3218 H01L27/3216)	02/10/2023	KY
PE2E Search: Updated Text Search	02/10/2023	KY

/KWANG-SU YANG/ Primary Examiner, Art Unit 2691	

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/808,982	LEE, Sang-Shin
	Examiner	Art Unit
	KWANG-SU YANG	2691

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
US-PGPUB; USPAT	((organic OLED) ADJ display SAME pixel adj3 (layer substrate) SAME virtual ADJ square SAME green SAME blue SAME red SAME shortest ADJ distance).clm.	02/10/2023	KY
US-PGPUB; USPAT	(method SAME (organic OLED) ADJ display SAME pixel adj3 (layer substrate) SAME virtual ADJ square SAME third ADJ color SAME shortest ADJ distance).clm.	02/10/2023	KY

/KWANG-SU YANG/ Primary Examiner, Art Unit 2691	

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17808982
Filing Date	2022-06-24
First Named Inventor	Sang-Shin Lee
Art Unit	2691
Examiner Name	KWANG-SU YANG
Attorney Docket Number	224123/411598-06419

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KY/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

	1	US Office Action dated September 19, 2022, issued in US Patent Application No. 17/808,985 (25 pages)	
	2	US Office Action dated October 14, 2022, issued in US Patent Application No. 17/808,983 (23 pages)	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/KWANG-SU YANG/	Date Considered	02/10/2023

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /KY/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17808982
	Filing Date	2022-06-24
	First Named Inventor	Sang-Shin Lee
	Art Unit	2691
	Examiner Name	KWANG-SU YANG
	Attorney Docket Number	224123/411598-06419

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

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☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Peter Hsueh/	Date (YYYY-MM-DD)	2022-10-26
Name/Print	Peter Hsueh	Registration Number	45574

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Bibliographic Data

Application No: 17/808,982

Foreign Priority claimed: (•) Yes ( ) No

35 USC 119 (a-d) conditions met: [✓] Yes [ ] No [ ] Met After Allowance

Verified and Acknowledged: /KWANG-SU YANG/ Examiner's Signature | Initials

Title: PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
06/24/2022	345	2691	224123/411598-06419
RULE			

APPLICANTS

SAMSUNG DISPLAY CO., LTD., Yongin-si, KOREA, REPUBLIC OF

INVENTORS

Sang-Shin LEE, Yongin-si, KOREA, REPUBLIC OF

CONTINUING DATA

This application is a CON of 17005753 08/28/2020

17005753 is a CON of 13872018 04/26/2013 PAT 10832616

13872018 is a CIP of 13614197 09/13/2012 PAT 9818803

FOREIGN APPLICATIONS

KOREA, REPUBLIC OF KR10-2012-0022967 03/06/2012

KOREA, REPUBLIC OF KR10-2013-0044993 04/23/2013

IF REQUIRED, FOREIGN LICENSE GRANTED**

06/30/2022

STATE OR COUNTRY

KOREA, REPUBLIC OF

ADDRESS

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001
UNITED STATES

FILING FEE RECEIVED

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(Not for submission under 37 CFR 1.99)

Application Number	17808982
Filing Date	2022-06-24
First Named Inventor	Sang-Shin Lee
Art Unit	2691
Examiner Name	YANG, KWANG-SU
Attorney Docket Number	224123/411598-06419

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5742129		1998-04-21	Nagayama et al.	
	2	6838819	B2	2005-01-04	Kim et al.	
	3	7187425	B2	2007-03-06	Yamazaki	
	4	7301273	B2	2007-11-27	Dedene et al.	
	5	8118633	B2	2012-02-21	Yuasa	
	6	8587003	B2	2013-11-19	Ando	
	7	8883532	B2	2014-11-11	Ando	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20030218618	A1	2003-11-27	Phan	
	2	20090321727	A1	2009-12-31	Yutani et al.	
	3	20100315318	A1	2010-12-16	Lee et al.	
	4	20120176298	A1	2012-07-12	Suh et al.	
	5	20160124557	A1	2016-05-05	Choi	
	6	20220319406	A1	2022-10-06	Lee	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	1168448	EP	A2	2002-01-02	Kim et al.	Corresponds to US 6838819, listed above	
	2	1450408	EP	A2	2004-08-25	Dedene et al.	Corresponds to US 7301273, listed above	

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	3	8-227276	JP	A	1996-09-03	Nagayama et al.	Corresponds to US 5742129, listed above	
	4	2001-76881	JP	A	2001-03-23	SHARP KK	Abstract	
	5	2005-62416	JP	A	2005-03-10	Yamazaki	Corresponds to US 7187425, listed above	
	6	2008-277264	JP	A	2008-11-13	Yuasa	Corresponds to US 8118633, listed above	
	7	2008-298966	JP	A	2008-12-11	KYOCERA CORP	Abstract	
	8	2012-79631	JP	A	2012-04-19	Ando	Corresponds to US 8587003, listed above	
	9	10-2006-0118868	KR	A	2006-11-24	Seong	Abstract	

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	US Office Action dated November 3, 2022, issued in US Patent Application No. 17/808,984 (25 pages).	
	2	US Office Action dated November 10, 2022, issued in US Patent Application No. 17/865,304 (23 pages).	

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	Attorney Docket Number	224123/411598-06419

	3	Chinese Office Action dated September 13, 2022, issued in Chinese Patent Application No. 201910040602.2 (9 pages).	

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Examiner Signature	/KWANG-SU YANG/	Date Considered	02/10/2023

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Signature	/Jun-Young E. Jeon/	Date (YYYY-MM-DD)	2022-11-17
Name/Print	Jun-Young E. Jeon	Registration Number	43693

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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First Named Inventor	Sang-Shin Lee
Art Unit	2691
Examiner Name	YANG, KWANG-SU
Attorney Docket Number	224123/411598-06419

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	Attorney Docket Number	224123/411598-06419

	1	US Notice of Allowance dated December 23, 2022, issued in US Patent Application No. 16/505,536 (9 pages)	
	2	US Final Office Action dated January 4, 2023, issued in US Patent Application No. 17/808,985 (27 pages)	

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Examiner Signature	/KWANG-SU YANG/	Date Considered	02/10/2023

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L263	37	("5742129" "6838819" "7187425" "7301273" "8118633" "8587003" "8883532" "20030218618" "20090321727" "20100315318" "20120176298" "20160124557" "20220319406").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/02/10 04:11 PM
L265	27604	(G09G3/3208 H10K59/352 H10K59/353).CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/02/10 05:16 PM
L266	232	L265 AND third ADJ (pixel sub$1pixel) AND (organic OLED) SAME third ADJ color	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/02/10 05:17 PM
L267	0	L265 AND third ADJ (pixel sub$1pixel) AND (organic OLED) SAME third ADJ color SAME green SAME blue SAME red SAME shortest ADJ distance	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/02/10 05:18 PM
L268	35816	(G09G3/3208 H01L27/3218 H01L27/3216).CPC.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/02/10 05:26 PM
L269	0	L268 AND (organic OLED) ADJ display SAME pixel adj3 (layer substrate) SAME virtual ADJ square SAME (red third) SAME shortest ADJ distance	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/02/10 05:31 PM
L270	0	(organic OLED) ADJ display SAME pixel adj3 (layer substrate) SAME virtual ADJ square SAME (red third) SAME shortest ADJ distance	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/02/10 05:32 PM

PE2E SEARCH - Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
N111	0	((organic OLED) ADJ display SAME pixel adj3 (layer substrate) SAME virtual ADJ square	(US-PGPUB; USPAT)	OR	ON	ON	2023/02/10 05:21 PM

		SAME green SAME blue SAME red SAME shortest ADJ distance).clm.					
N112	0	(method SAME (organic OLED) ADJ display SAME pixel adj3 (layer substrate) SAME virtual ADJ square SAME third ADJ color SAME shortest ADJ distance).clm.	(US-PGPUB; USPAT)	OR	ON	ON	2023/02/10 05:23 PM

PE2E SEARCH - Search History (Similarity Search)

No Similarity Results available

UNITED STATES PATENT AND TRADEMARK OFFICE

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Alexandria, Virginia 22313-1450
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NOTICE OF ALLOWANCE AND FEE(S) DUE

23363 7590 02/21/2023

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
YANG, KWANG-SU	
ART UNIT	PAPER NUMBER
2691	

DATE MAILED: 02/21/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/808,982	06/24/2022	Sang-Shin LEE	224123/411598-06419	4376

TITLE OF INVENTION: PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	05/22/2023

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

BOE
Exhibit 1003 Page 474

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23363 7590 02/21/2023
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/808,982	06/24/2022	Sang-Shin LEE	224123/411598-06419	4376

TITLE OF INVENTION: PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	05/22/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
YANG, KWANG-SU	2691	345-082000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

BOE
Exhibit 1003 Page 475

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/808,982	06/24/2022	Sang-Shin LEE	224123/411598-06419	4376

23363 7590 02/21/2023

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

EXAMINER	
YANG, KWANG-SU	

ART UNIT	PAPER NUMBER
2691	

DATE MAILED: 02/21/2023

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/808,982	Applicant(s) LEE, Sang-Shin	
	Examiner KWANG-SU YANG	Art Unit 2691	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to amendment filed on 01/17/2023.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-10 and 14-33 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some* c) ☐ None of the:

   1. ☑ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☑ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/KWANG-SU YANG/
Primary Examiner, Art Unit 2691

EXAMINER'S AMENDMENT

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

In line 1 of claims 2-9 and line 1 of claims 26-30: "… The display …" should be changed to --… The OLED display …--.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Inquiry

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KWANG-SU YANG whose telephone number is (571)270-7307. The examiner can normally be reached on Monday - Friday during 9:00am-6:00pm EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen, can be reached on (571)272-7772. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KWANG-SU YANG/
Primary Examiner, Art Unit 2691

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POSTEDIGITAL
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Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

Courtesy Reminder for
Application Serial No: 17/808,982

Attorney Docket No: 224123/411598-06419
Customer Number: 23363
Date of Electronic Notification: 02/23/2023

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:
pto@lewisroca.com
PLPrivatePair@lrrc.com

To view your correspondence online or update your email addresses, please visit us anytime at **https://ppair-my.uspto.gov/pair/PrivatePair.**
If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov or call 1-866-217-9197.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	**03/07/2023 05:31:59 PM ET**	**224123/411598-06419**

Title of Invention

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4376	FILED BY	Si Vuong
PATENT CENTER #	61703381	FILING DATE	06/24/2022
CUSTOMER #	23363	FIRST NAMED INVENTOR	Sang-Shin LEE
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Jun-Young Jeon

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
224123_IssueFeeTransmittal.pdf	1	Issue Fee Payment (PTO-85B)	237 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
224123_IssueFeeTransmittal.pdf	6C7149DBC2BD53B5CF1F7263CD86E3462DEADC18DA431C1E829B37C015E78C9C301E1FE8426859E2B6CAC22F00EF7605441DA38DD1F87063688AE8F1ECE5883D

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized

by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	03/07/2023 05:31:59 PM ET	224123/411598-06419

Title of Invention

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	4376	FILED BY	Si Vuong
PATENT CENTER #	61703381	AUTHORIZED BY	Jun-Young Jeon
CUSTOMER #	23363	FILING DATE	06/24/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Sang-Shin LEE

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
CARD / 4792	E202337H32497301	Si Vuong

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1501	UTILITY ISSUE FEE	1200.00	1	1200.00
			TOTAL AMOUNT:	$1,200.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage

submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

23363 7590 02/21/2023
Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Si Vuong	(Typed or printed name)
/Si Vuong/	(Signature)
March 7, 2023 (E-filed)	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/808,982	06/24/2022	Sang-Shin LEE	224123/411598-06419	4376

TITLE OF INVENTION: PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	05/22/2023

EXAMINER	ART UNIT	CLASS-SUBCLASS
YANG, KWANG-SU	2691	345-082000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Lewis Roca Rothgerber Christie LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Samsung Display Co., Ltd.	Yongin-si, Republic of Korea

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies 0

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 03-1728

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Jun-Young E. Jeon/ Date March 7, 2023

Typed or printed name Jun-Young E. Jeon Registration No. 43,693

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

BOE
Exhibit 1003 Page 486

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/808,982	04/11/2023	11626066	224123/411598-06419	4376

23363 7590 03/22/2023

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA 91209-9001

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Patents Stakeholder Experience (OPSE), Stakeholder Support Division (SSD) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site http://pair.uspto.gov for additional inventors):

Sang-Shin LEE, Yongin-si, KOREA, REPUBLIC OF;

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

SAMSUNG DISPLAY CO., LTD., Yongin-si, KOREA, REPUBLIC OF;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PATENT
224123

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

I hereby certify that this correspondence is being transmitted via the United States Patent and Trademark Office's patent electronic filing system (Patent Center or EFS-Web) on June 21, 2023 at or before 11:59 p.m. Pacific Time under the Rules of 37 CFR § 1.8.

/Christina L. Malinosky/
Christina L. Malinosky

U.S. Patent No. : 11,626,066 Confirmation No. 4376
Issued : April 11, 2023
Inventor(s) : Sang-Shin Lee
Application No. : 17/808,982
Filed : June 24, 2022
Title : PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

REQUEST FOR CERTIFICATE OF CORRECTION

Office of Certificates of Correction
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 29001
Glendale, CA 91209-9001
June 21, 2023

Commissioner:

Attached is a proposed Certificate of Correction to correct errors by the Patent Office appearing in the above-referenced patent. The errors are identified in detail in the proposed certificate, and the corresponding text in the application is located as follows:

Location in Patent In the Claims	**Location in Application**
Col. 13, line 52, Claim 4	Claims 01/17/2023, pg. 4, Claim 4, line 2
Col. 13, line 67, Claim 8	Claims 01/17/2023, pg. 4, Claim 8, line 2
Col. 15, line 20, Claim 17	Claims 01/17/2023, pg. 6, Claim 15, line 1
Col. 16, line 8 (Approx.), Claim 24	Claims 01/17/2023, pg. 8, Claim 22, lines 2-3

121581619.1

Approval of this certificate is respectfully requested.

Respectfully submitted,

LEWIS ROCA ROTHGERBER CHRISTIE LLP

By /Steven French/
Steven J. French
Reg. No. 78,743
626/795-9900

SJF/clm
Enclosures: Certificate of Correction

PTO/SB/44 (09-07)
Approved for use through 03/31/2023. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 11,626,066

APPLICATION NO.: 17/808,982

ISSUE DATE : April 11, 2023

INVENTOR(S) : Sang-Shin Lee

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Col. 13, line 52, Claim 4	Delete “preen” and Insert -- green --
Col. 13, line 67, Claim 8	Delete “preen” and Insert -- green --
Col. 15, line 20, Claim 17	Delete “wherein the one” and Insert -- wherein one --
Col. 16, line 8 (Approx.), Claim 24	Delete “and the one” and Insert -- and one --

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Lewis Roca Rothgerber Christie LLP
P.O. Box 29001
Glendale, CA 91209-9001

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/808,982	**06/21/2023 12:28:03 PM ET**	**224123/411598-06419**

Title of Invention

PIXEL ARRANGEMENT STRUCTURE FOR ORGANIC LIGHT EMITTING DIODE DISPLAY

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	11626066
CONFIRMATION #	4376	FILED BY	Christina Malinosky
PATENT CENTER #	62308705	FILING DATE	06/24/2022
CUSTOMER #	23363	FIRST NAMED INVENTOR	Sang-Shin LEE
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Steven French

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
224123 - Request for Cert of Correction.pdf	3	Request for Certificate of Correction	260 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
224123 - Request for Cert of Correction.pdf	538E71F8BDE6F9B1BFF8D0880F5F671102DC2888C1B6CA8BD135AD457E35901A19F22CFF6F8211C8AD931B303CD180B142847A08D617AB6FC1DE95B4FA8A1719

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized

by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 11,626,066 B2
APPLICATION NO. : 17/808982
DATED : April 11, 2023
INVENTOR(S) : Sang-Shin Lee

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

Column 13, Line 52, Claim 4	Delete "preen" and Insert -- green --
Column 13, Line 67, Claim 8	Delete "preen" and Insert -- green --
Column 15, Line 20, Claim 17	Delete "wherein the one" and Insert -- wherein one --
Column 16, Line 8 (Approx.), Claim 24	Delete "and the one" and Insert -- and one --

Signed and Sealed this
Eighteenth Day of July, 2023

Katherine Kelly Vidal

Katherine Kelly Vidal
Director of the United States Patent and Trademark Office